

Mobile Displays

Technology and Applications

Edited by

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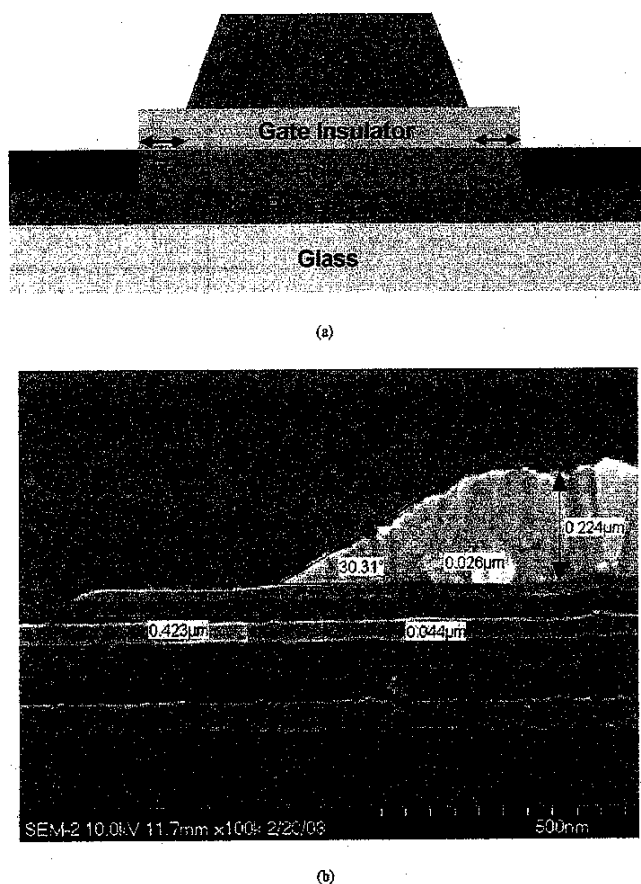


Figure 14.18 (a) TFT structure and (b) SEM micrograph of FAST LDD.

TFTs due to these created defects in the upper half of the band gap. Compared to the conventional LDD TFTs, FAST TFTs show better HCS endurance in the mobility and on-current parameters.

Table 14.6 shows the degradation of electrical characteristics of LTPS TFTs under 100 second DAHC stress. The results show good stress endurance of FAST LDD LTPS TFTs in comparison with general LDD LTPS TFTs, even with a smaller physical size. The high reliability of FAST LDD LTPS TFTs is attributed to the elaborate engineering of the doping process for LDD and the source/drain.

14.4 AMOLED Pixel Circuit Design

14.4.1 Pixel Circuit

LTPS was considered mandatory for AMOLEDs because it has the advantages of higher driving capability, superior reliability, and higher thermal endurance compared to a-Si [44]. However, the non-uniformity caused by LTPS process variations [45] as well as its high-cost technology impede large-panel

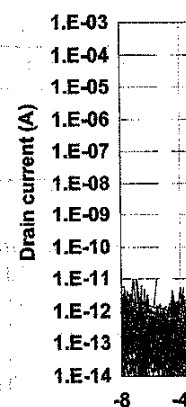


Figure 14.19 The trans on 620×750 mm glass.

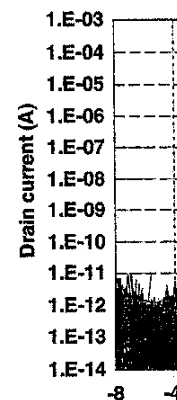


Figure 14.20 The trans after hot carrier stress. T

Table 1

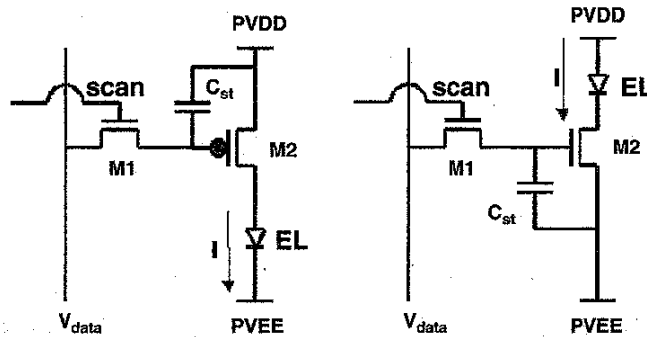
V_{th} (V)
SS (V/dec)

Table 14.6 The degradation of electrical characteristics of LTPS TFTs under 100 second DAHC stress.

	FASt LDD TFT	STD LDD TFT
ΔV_{th} (V)	0.018	0.025
$\Delta \mu / \mu_0$	0.19	0.47
$\Delta I_{on} / I_{on0}$ ($V_d = 0.1$ V)	0.14	0.48

AMOLED applications. Although it was generally believed that a-Si tends to generate uniform initial characteristics [46], the instability and low mobility of a-Si [47] have been a bottleneck for AMOLED applications. Typical 2T pixel circuits for LTPS and a-Si TFTs are shown in Figures 14.21(a) and (b), respectively. Both have an addressing TFT M1, a driving TFT M2, and one storage capacitor C_{st} . When the scan line is selected, M1 is open and V_{data} will be transferred to the gate of M2. As the scan line is disabled, V_{data} on the gate of M2 still holds due to the fact that charge is stored across C_{st} . The current I flowing to the EL has the following relation:

$$I = (1/2) C_{ox} (\mu W/L) (V_{gs} - V_{th})^2 = (1/2) C_{ox} (\mu W/L) (PVDD - V_{data} - V_{th})^2 \quad (3)$$

**Figure 14.21** (a) LTPS 2T1C pixel circuit; (b) a-Si 2T1C pixel circuit.

where C_{ox} , μ , W , and L are the channel capacitance per area, channel mobility, channel width, and channel length of M2, respectively. V_{gs} and V_{th} are the gate-source voltage and the threshold voltage of M2, respectively. PVDD is changed to PVEE in Equation (3) if the a-Si pixel circuit is referred to.

Since the OLED is a current-driven device, the brightness uniformity over the panel is susceptible to variations in device characteristics of TFTs and EL itself. However, the EL process can be well controlled and uniformity of EL is not a big issue. Figure 14.22 below gives one example showing the front-of-screen non-uniformity of the brightness for the LTPS-driven AMOLED display [48]. The non-uniformity is attributed mainly to the ELA, cleaning, and CVD process of LTPS. Equation (3) indicates two factors of TFTs that influence the uniformity: the mobility and threshold voltage. By simple calculation, it can be shown that the percentage current variation $\sigma(I)/I$ with respect to the threshold voltage variation $\sigma(V_{th})$ and mobility $\sigma(\mu)$ are given by

$$\sigma(I)/I = -2\sigma(V_{th})/(PVDD - V_{data} - V_{th}) \quad (4)$$

$$\sigma(I)/I = \sigma(\mu)/\mu \quad (5)$$

As $(PVDD - V_{data})$ large, resulting in series mobility variation is threshold voltage can in the center of Figure uniformities in output uniform current through during operation, leading issues for both LTPS proposed and will be

Figure 14.23

14.4.1.1 Pixel Compensation

One of the solutions to tackle the non-uniformity issues is to apply compensation circuits in every pixel. Compensation means that the driving TFT in a pixel has to be compensated for parameters such as threshold voltage and/or mobility, so that the output current becomes independent of the parameters. In real cases, there are too many factors; for example, the parasitic effects and load-dependent RC time delay of the signal lines cause the compensation not to be perfect. The more the circuit can compensate, the more uniform will become the front-of-screen brightness of the panel. Since every panel has uniformity specifications for long range and short range, the compensation circuits, together with the TFT process window, must be fine-tuned to meet them. In this section, several published pixel compensation circuits are reviewed, analyzed, and compared.

The pixel compensation circuits can be categorized in two parts: the analog and digital driving circuits. The analog driving circuits comprise voltage compensation, current compensation, and hybrid compensation, while the digital driving circuits include time-ratio grayscale and area-ratio grayscale.

14.4.1.2 Analog Driving Circuits

By analog driving circuits we mean that the grayscale is defined by the data signal, either voltage or current. Figures 14.24(a) and (b) show typical data signals versus grayscale in the 2T pixel (Figure 14.21) for data voltage and data current, respectively. Note that a gamma factor equal to 2.2 is applied in Figure 14.24. Suppose there are 256 grayscales for each color; there should be 256 corresponding V_{data} or I_{data} .

14.4.1.3 Voltage Compensation

Dawson *et al.* [50] from the Sarnoff Corporation proposed a voltage-driven pixel compensation circuit which contains four transistors and two capacitors. The circuit and its corresponding timing are shown in Figure 14.25 below. The additional transistors, M3 and M4, automatically zero the threshold voltage of the driving transistor, M2. During this period, M4 turns off and M3 turns on. M2 and M3 form a diode-connected structure and the disconnection of M4 forces the voltage at the gate of M2 to be $V_g = V_{DD} - V_{th}$. V_{th} is the threshold voltage of M2. Now the voltage across the capacitor C1 is V_{th} . In the second period, M3 is disconnected and V_{data} is applied. The voltage across C1 now becomes

$$(V_{DD} - V_{data}) \times C2 / (C1 + C2) + V_{th} \quad (6)$$

Equation (6) is the voltage across V_{gs} of M2. From (3), it can be found that in the emission period, the current flowing to the OLED is independent of V_{th} of M2 and is given by

$$I = (1/2)C_{ox}(\mu W/L)\{(V_{DD} - V_{data}) \times C2 / (C1 + C2)\}^2 \quad (7)$$

The improvement in the pixel-to-pixel brightness uniformity is demonstrated in Figure 14.26 below. After compensation, the image becomes more uniform, and according to ref. [50], the standard deviation of the pixel luminance changes from 16.1% (2T) to 4.7% (4T) at a panel luminance of 15 cd/m². This is a simple example of a voltage-controlled pixel compensation circuit, and the basic principle is the diode-connected structure to sense and store the threshold voltage of the driving TFT. Although there are many voltage-driven compensation circuits with 4–6 transistors and 1–2 capacitors,

V_{high}
 V_{data}
 V_{low}
 I_{high}
 I_{data}
 I_{low}

Figure 14.24 (a) V_{data}
(b) I_{data} with respect to t

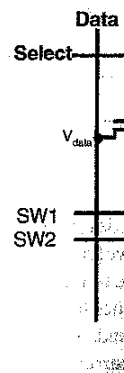


Figure 14

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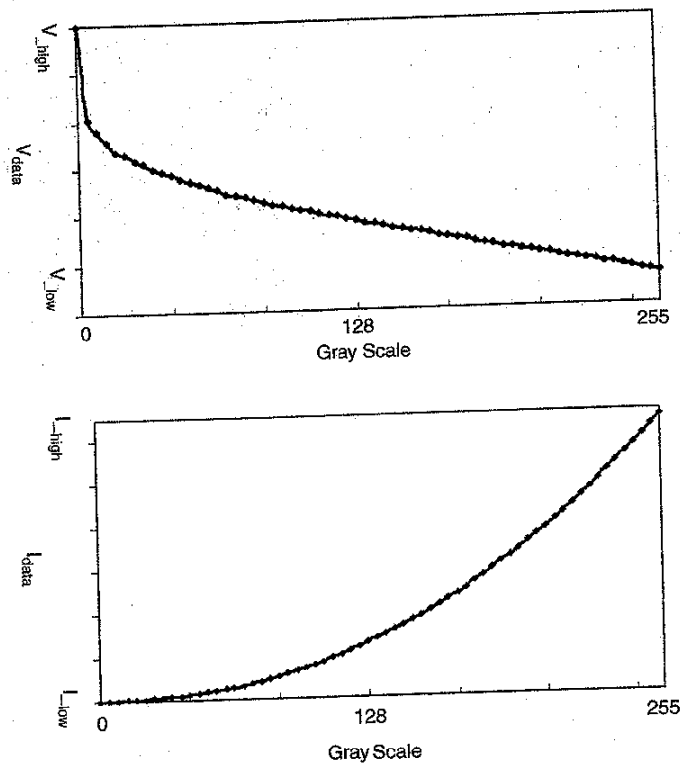


Figure 14.24 (a) V_{data} with respect to the grayscale for a voltage-driven pixel; gamma has been considered. (b) I_{data} with respect to the grayscale for a current-driven pixel; gamma has been considered.

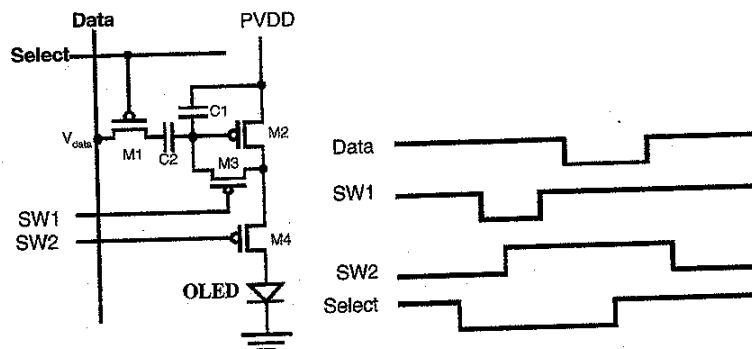


Figure 14.25 The 4T2C voltage-driven pixel compensation circuit and its timing.

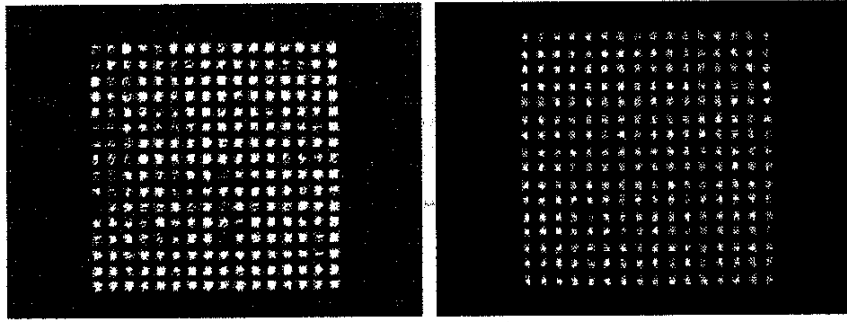


Figure 14.26 Comparison of the light-on results before and after correction.

they follow the same basic principle. From a design point of view, fewer control lines and power lines are preferred for a compensation circuit in one limited pixel size and, moreover, easier operation of the pixel is also desired.

Ono *et al.* [51], from IDT, proposed a voltage-controlled 4T1C pixel circuit for an a-Si AMOLED. Figure 14.27 shows the proposed pixel circuit and its corresponding timing. There are four control lines: MRG, RST, SCT, and COM. These control lines can be generated externally in the driver IC or power IC. During the compensation cycle, the OLED device serves as a capacitor, C_{OLED} . The pixel operation can be divided into four periods, as indicated in the timing in Figure 14.27. The operation of each period will be analyzed as follows:

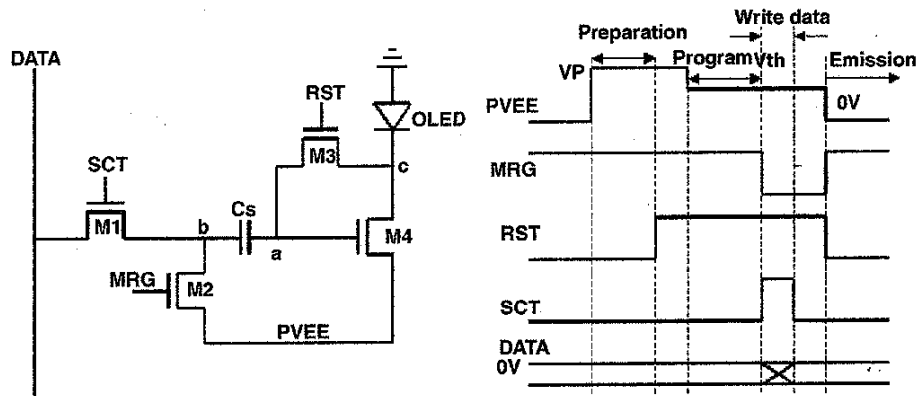


Figure 14.27 The 4T1C voltage-driven pixel compensation circuit for a-Si TFT and its corresponding timing.

(1) *Preparation*: The purpose of this period is to prepare the voltage at some nodes for programming V_{th} . The voltage of the COM line rises to some voltage level, e.g. V_p , and the voltage at node B (V_b) will become V_p as well. The voltage at node A (V_a) becomes higher than V_p due to the fact that in the emission period from the last frame, V_a was higher than that at V_b . If V_p is higher than V_{th} of T4, T4 would conduct reversely, i.e. current would flow from the COM line to ground. At the end of the preparation period, the voltage at node C (V_c) approaches V_p since very low current is flowing. The turn-on of T3 turns off T4 and V_a equals V_c .

(2) *Program V_{th}* : The voltage at node A (V_a) is programmed to be the V_{th} of the pixel.

(3) *Write data*: $-V_{data}$ is written to the pixel.

The V_{gs} of T4 is the voltage at node A (V_a).

In the last period, (4) *Emission*: The current through the pixel is controlled by the voltage at node A (V_a).

Equation (10) is independent of the variation of V_{th} of the pixel. The variation of V_{th} is less than 15% for dV_{th} of the V_{th} programming period. Row by row programming for all pixels in the frame. The control lines of the pixel power line has three levels. The V_{th} resulting from the