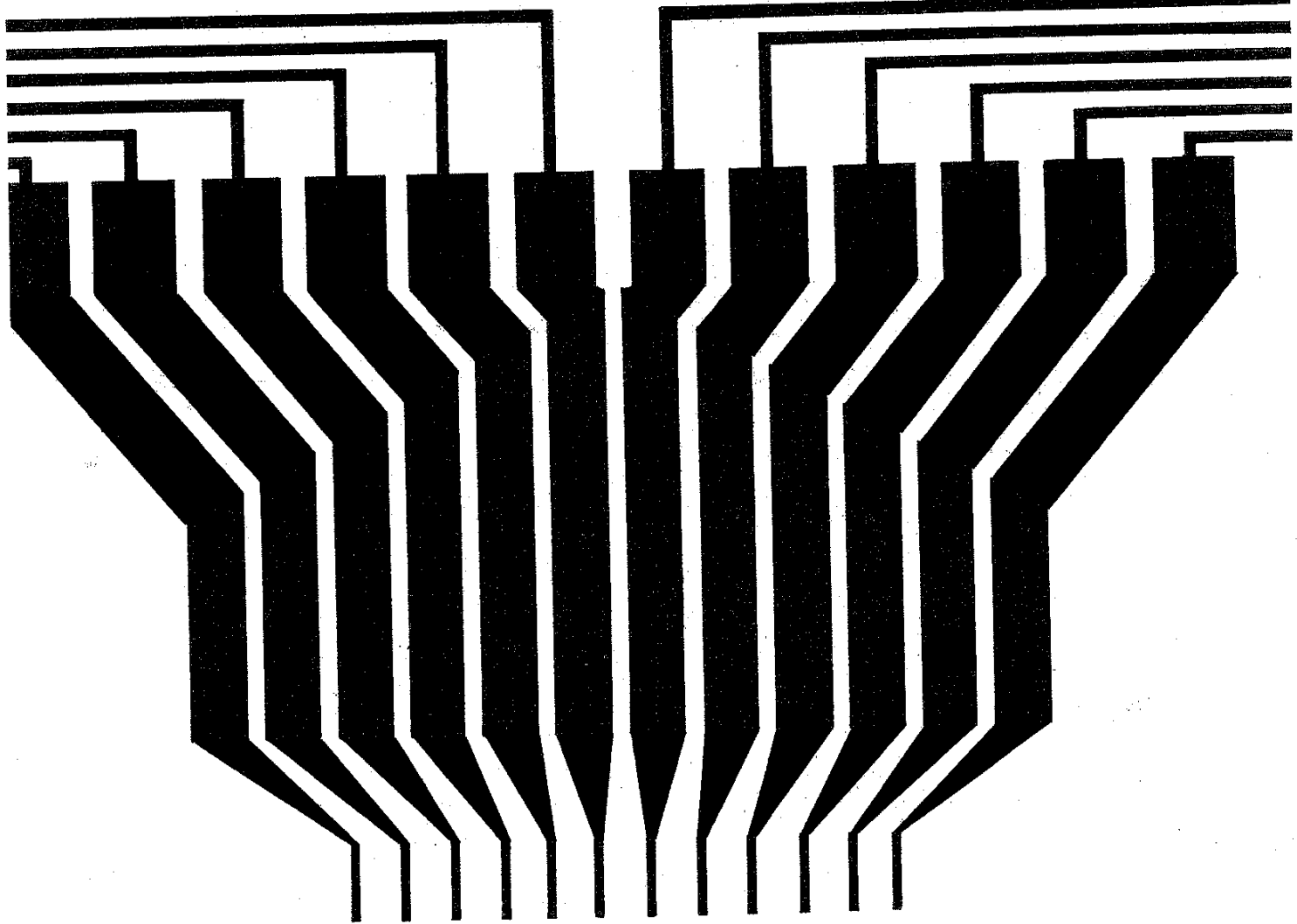




Electronic Materials Handbook™

Volume 1 Packaging



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Rigid Printed Wiring Board Fabrication Techniques

Larry Lynch and Raymond A. Nesbitt, AT&T Microelectronics

PRINTED WIRING BOARDS (PWBs) are manufactured in several ways using a variety of materials and processes. There are two distinct approaches to rigid PWB manufacture. Subtractive technology begins with copper foil on an insulating substrate as the primary workpiece, and the copper is selectively removed except where the circuitry is desired. Additive technology begins with unmetallized substrate, on which copper is selectively added to provide the interconnection circuitry.

Materials

Substrate (dielectric) materials are thermosetting or thermoplastic polymers, usually reinforced with woven nonconducting fibers, although random and unwoven reinforcement materials are also used. By far the most common substrate material is glass-reinforced epoxy, with glass-reinforced polyimide a distant second. The substrate materials provide the base for the printed circuitry in its finished form and serve as the vehicle or workpiece upon which the numerous processes are performed during printed circuit manufacture. Substrate properties can be categorized as mechanical, electrical, thermal, and chemical. A relatively wide range of properties are available for various end-product and processing characteristics.

The principal substrate mechanical properties are strength, stiffness, impact resistance, flexibility, and dimensional stability. These properties are important for end-product applications, but the materials must also withstand and be amenable to such mechanical processes as drilling, routing, punching, blanking, chamfering, and slotting.

The principal electrical properties are dielectric strength, insulation resistance, permittivity or dielectric constant, and ac loss-tangent or dissipation factor. These are important for end-product performance characteristics. They also influence PWB manufacture because the various materials

that provide specific electrical properties require different sets of processing parameters.

The primary thermal characteristics are coefficient of thermal expansion, maximum service temperature, and maximum temperature tolerated for short times without permanent damage to the chemical, mechanical, or electrical properties. Typical values for the last two parameters are 100 °C (212 °F) and 260 °C (500 °F), respectively. Special product applications may require the ability to withstand extended periods below freezing or above 100 °C (212 °F), or repeated thermal cycling.

The more important chemical properties of the substrate are its ability to withstand harsh acids, alkaline chemicals, and organic solvents, all of which are used in printed circuit manufacture or in component assembly processes. Also important is the tendency of the substrate material to absorb water and organic solvents, as well as the dimensional changes and resin deterioration associated with such absorption.

Details. The base material for rigid single-sided, double-sided, or multilayer PWBs is purchased in flat laminated sheets. These can be purchased in the final workpiece dimensions or in larger sizes that are then sheared to the desired size by the PWB manufacturer. The dielectric thickness of these materials typically ranges from 0.1 to 3.18 mm (0.004 to 0.125 in.), with 1.5 mm (0.059 in.) being the most common because it is used for most double- and single-sided products. The substrate sheets can be purchased with copper foil clad on one or both sides. The foil thicknesses are normally expressed in ounces of copper per square foot. The most common cladding is 1 oz copper, which is nominally 0.036 mm (0.0014 in.) thick. Also commonly used are ½ oz copper and 2 oz copper. Thinner copper (down to ¼ oz) and thicker copper (up to 5 oz) are available for special applications. A more thorough discussion of substrate materials appears in the article "Resins and Reinforcements" in this Volume.

The substrate material is made from resin-impregnated glass cloth. The cloth is purchased in a number of glass fiber thicknesses and weave styles. Rolls of glass cloth are coated with liquid resin (A-stage). The resin is partially cured to a semistable state (B-stage, or prepreg). The rolls are then cut into relatively large sheets, and several sheets are stacked to form the desired final thickness. If the eventual laminates are to be copper clad, copper foil sheets form the outside of the stack. This package is then laminated in steam-heated hydraulic presses. At temperatures of approximately 170 °C (350 °F) and pressures up to 10.3 MPa (1.5 ksi), the resin melts and flows somewhat, dissolving air and volatiles in the B-stage resin. It then cures, irreversibly, to form the final resin state, which is called C-stage. The outer inch or so of the laminate is then trimmed off, and the remainder is sheared to the size required by the PWB manufacturer.

Some manufacturers order the laminate sheared to the final workpiece size, while others choose to purchase larger sheets and do the shearing themselves. In either case the eventual workpiece is referred to as a panel. Panels are the basic units on which the PWB makers operate to produce the finished PWBs.

The conducting materials used on printed circuits are primarily metals. The most common basis metal is copper (Cu). The Cu is derived from Cu cladding that is integrated to the purchased substrate material and/or from the electrolytic and electroless Cu plating operations used in PWB processing. Tin (Sn) or tin-lead (Sn-Pb) is commonly electroplated and used as an etch resist during circuit pattern definition. The Sn-Pb may remain on the finished PWB either in its as-plated form or fused to form a solder alloy. The Sn-Pb solder can also be applied by dipping the PWB into molten solder using a special process called hot-air solder leveling (HASL). In HASL, liquid solder is applied, and the excess solder is removed with high-velocity hot air. The principal

function of the solder that remains on the PWB is to provide solderability during subsequent assembly soldering operations.

Other metals that may appear on PWBs are nickel (Ni) and gold (Au). Hard gold, alloyed with a hardening element such as cobalt, is electroplated onto sliding contact areas such as edge-card connector fingers. The Au provides permanent low electrical contact resistance. Nickel is usually electroplated onto the copper before the Au is applied and serves as a diffusion barrier between the Cu and Au. Typical Ni thicknesses are 2.5 μm (100 $\mu\text{in.}$), and gold thicknesses range from 0.65 to 2.54 μm (25 to 100 $\mu\text{in.}$). Palladium (Pd) is sometimes used as a less expensive noble metal, but is usually coated with a very thin layer of Au to achieve a metallic sandwich of Cu-Ni-Pd-Au. A less common use of Au plating is to replace Sn or Sn-Pb as an etch resist and to provide a solderable surface.

The Sn-Pb solder in the form of paste can also be stenciled onto PWB terminal areas. Solder paste is commonly applied to surface-mounted device pads on the PWB just prior to attachment of the devices, and it serves to hold the devices in place until the solder is fused. A less common use of stenciled solder paste is to provide additional solder, selectively, to areas where the relatively thin solder applied with HASL processes may not be sufficient.

Other conducting materials that are finding increasing use are selectively screened or stenciled pastes that contain silver or carbon. The carbon inks are sometimes used in place of more expensive gold plating as electrical contact materials.

The other materials that appear on finished PWBs are solder mask or cover coat materials. These materials are polymeric films that coat the PWB surfaces. The solder mask provides two functions. First, it protects closely spaced circuit elements from solder bridges during assembly soldering operations, and second, it is a permanent environmental protective coating. Solder mask typically covers the entire PWB surface, except areas that are used for device or connector attachment or for electrical test points. Other regions that are sometimes left free of solder mask are large solder-plated areas and outer board perimeters.

Types of Rigid PWBs

Conventional rigid PWBs can be categorized as single-sided, double-sided, and multilayer. The characteristics and differences are briefly discussed below.

Single-sided PWBs, as the name suggests, have circuitry on only one side. The substrate materials used for single-sided manufacture are usually the less expensive materials, such as phenolic or polyester resins with random mat glass or paper rein-

forcement. The material is clad on one side with copper foil. Panels are drilled or punched to provide holes for component leads. Two procedures can be used to create the circuits. First, product is printed and etched using the resist as etch resist, resulting in bare copper circuitry. Second, panels are printed with opposite tonality artwork from above and electroplated with Sn-Pb, with the resist serving as a plating resist; the resist is removed; and the exposed copper is etched away, with the Sn-Pb acting as an etch resist.

Double-sided PWBs have circuits defined on both sides. However, in this case, the through holes can be plated with copper to provide electrical access from side to side. The plated-through holes (PTHs) allow significantly greater circuit density because they provide crossover capability; a circuit can cross over another simply by entering a PTH, continuing on the other side, then back through another PTH and so on. Double-sided substrate materials are usually glass-reinforced epoxy, but less expensive materials are sometimes used for consumer products.

Subtractive technology manufacturing steps always include drilling (or punching) the holes, metallizing (electroless Cu plating), imaging (printing), electrolytic Cu plating, and etching. Other processes are also necessary to finish the product, but the interconnection circuitry is completed with these five steps. Additive technology processing is somewhat more involved, but drilling, plating, and imaging are still used in combination with resin surface sensitization.

Multilayer PWBs have more than two layers of circuitry. Access to the internal layers is again made with holes drilled through the internal circuits and plated through. The internal circuits are made on either single- or double-sided copper clad laminates. The conventional internal circuit (inner layer) processes include imaging, etching that utilizes the imaging material as an etch resist, and oxidizing the copper conductor surface. The inner layers are then stacked up, using rigid pins to establish layer-to-layer orientation with B-stage polymeric sheets separating the layers.

This sandwich is then laminated in a heated press similar to those used for laminating the substrate material by the laminate vendors. The B-stage prepreg melts under pressure, and then flows, dissolving air and volatiles. When it cures, it glues the entire package into a rigid assembly. The remaining processes for multilayer PWBs are very nearly the same as the entire process sequence for double-sided products. Most multilayer PWBs use epoxy-glass substrate materials, but glass-reinforced polyimide is often used for more complex or higher layer count products and for harsh-temperature applications. Other resins are polytetrafluoroethylene (PTFE)

and various resin combinations of epoxy, polyimide, cyanate esters, and others, such as bismaleimide triazene (BT), which are blended to enhance performance properties.

Printed Board Manufacturing Overview

Types of PWB Manufacturing Operations

Printed board manufacturing steps are commonly separated into imaging operations, chemical operations, and mechanical operations. The reason for these separations is that the work areas in which the different types of operations are performed are significantly different. For example, imaging operations are usually performed in relatively clean environments, with well-controlled temperature and humidity. Chemical operations do not require atmospheric control, but require piping access to storage tanks and waste treatment facilities, acid-resistant flooring, and so on. The mechanical operations generally do not require special building facilities or environmental controls, so they can be located in less expensive general-purpose manufacturing areas. One additional step is normally performed in an atmosphere-controlled, relatively clean environment. This is the multilayer PWB stack-up operation.

The common PWB mechanical manufacturing operations are drilling, deburring, punching, routing, blanking, chamfering, and slotting. Imaging processes are actually a series of steps that include scrubbing or cleaning, printing (either photo printing or screen printing), developing, and curing (with heat, ultraviolet energy, or both). The chemical processes include electroless and electrolytic plating, etching, resist removal, oxidizing, fluxing, and cleaning. Typical remaining operations are laminating (for multilayer PWBs), baking, testing, and inspecting.

Standard Multilayer Inner Layer Processing

A typical multilayer PWB inner layer panel is a relatively thin (0.13 to 0.75 mm, or 0.005 to 0.030 in.) copper clad laminate with $\frac{1}{2}$, 1, or 2 oz copper on both sides. A possible process sequence is shown in Fig. 1. The patterning operations shown are called print and etch because the circuitry is defined with just those operations. This term has, perhaps, been overused, to the point that the entire inner layer process sequence is called print-and-etch technology. Figure 2 illustrates inner layer sections from the raw material stage through the various patterning steps.

Subtractive Multilayer Assembly and Double-Sided Processing

Figure 3 shows a flow chart for pattern-plated multilayer PWBs that contain no noble metal plating and are manufactured

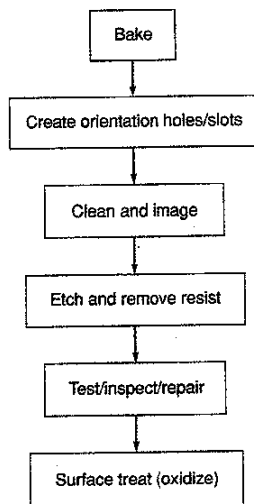


Fig. 1 Multilayer inner layer process sequence

with fused solder beneath the solder mask. Figure 4 illustrates an individual drilled hole as it proceeds from the drilling operation through the etching operation. It is important to note that double-sided product would not undergo the stack-up, lamination, and etchback or smear removal steps.

Through the etching operation the process sequence is relatively standard. However, from the etching step onward a variety of sequences are possible, depending on the product design or choice of manufacturing technologies. For example, a PWB that contains gold-plated edge-card connector fingers would require stripping of the Sn-Pb from the finger areas, Ni and Au plating of the fingers, and most likely chamfering and slotting of the connector portion of the board. Another set of operations often used for more complex surface layer designs involves stripping of the Sn-Pb after the Cu etching step, applying the solder mask over bare Cu, and hot-air solder leveling to apply fused solder selectively to the exposed circuitry.

Pattern Plating Versus Panel Plating. There are two distinct technologies for subtractive PWB manufacture. These are pattern plating and panel plating. For pattern plating, the imaging and electrolytic plating steps follow the sequence shown in Fig. 2. The only areas that are electroplated are the surface layer circuits and the PTHs. These regions are plated first with copper and then with Sn-Pb, which serves as the etch resist when the unwanted copper is etched away. This technology is sometimes referred to as print, plate, and etch because these processes, in that order, provide the final copper thickness and define the surface layer circuitry.

Panel plating reverses the order for imaging and electroplating. After drilling and electroless copper plating, the entire panel is electroplated with copper. With artwork

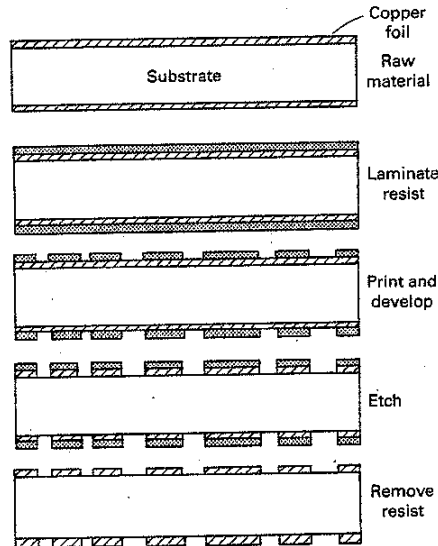


Fig. 2 Inner layer sections through patterning steps

reversed in tonality from pattern plating, the panel is then imaged. The photoresist serves as the etch resist, and the unwanted copper is etched away. This technique requires that the photoresist protect the circuitry copper, including that which was plated in the holes. The resist must, therefore, tent over the holes and not break down on rupture before or during the etching operation. This technology can be described as plate, print, and etch. In this respect, the technique is closely related to multilayer inner layer processing.

Panel plating predates pattern plating. However, panel plating has undergone a resurgence in popularity. Its principal advantage over pattern plating is the uniformity of the electroplated deposit. Some manufacturers believe that panel plating offers improved circuit definition over pattern plating, and they use this approach to manufacture designs with more complex surface layer circuitry. The disadvantages are the potential for photoresist tent breakdown, which causes the plating in the holes to be etched away, and the extra cost of electroplating copper over the entire workpiece.

An advantage of pattern plating is that copper is electroplated only on those areas where it is required. A disadvantage is that the plated copper thickness varies considerably, with isolated circuit areas being plated thicker than areas of denser circuitry.

Additive PWB Processing

Additive processes include drilling, plating, and printing, but, in general, no etching is involved. The material is unclad laminate. Typical processing steps are drilling, catalyzing, printing, and full-build electroless copper plating. At this stage the circuitry is complete; copper has been added only where it was required. After the resist is

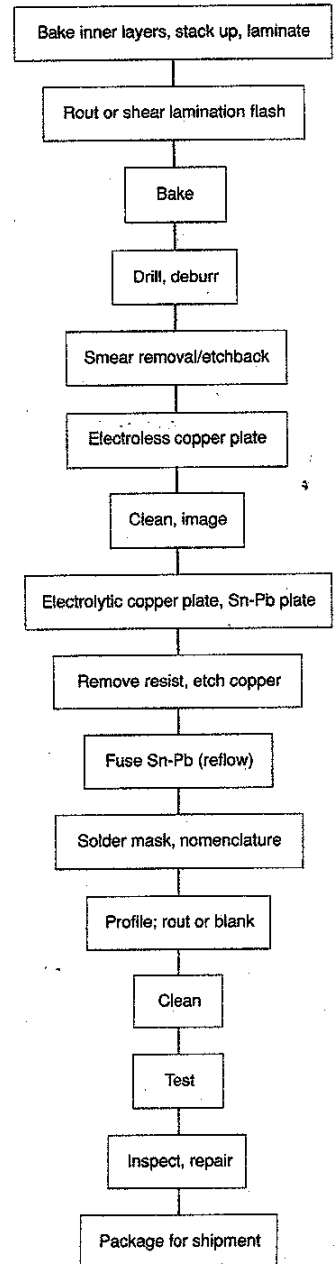


Fig. 3 Typical multilayer assembly process sequence

removed, product is solder mask coated and so on. The remaining processes are the same as those for subtractive product.

In-Depth Printed Circuit Manufacturing Panel Layout

PWB manufacturing methodologies, for the most part, build panels, not boards. The automation of PWB fabrication drives manufacturers toward a few or even one panel size. Standard practice is to build panels having as many boards as possible. With the

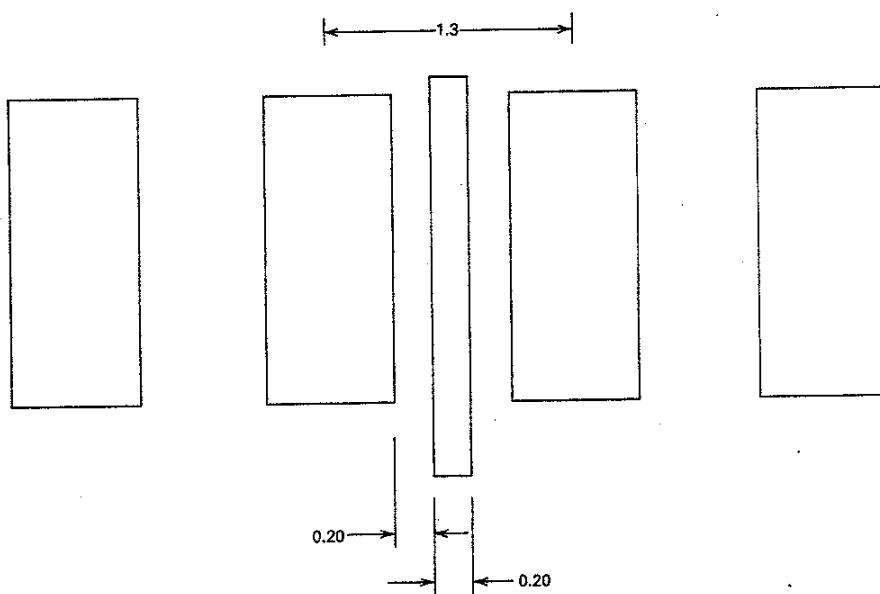


Fig. 15 Signal path between 1.3 mm (0.050 in.) center surface-mount pads. Dimensions given in millimeters

circuits. DIPs are by far the most common IC configuration, and millions of DIPs are assembled onto printed boards each day. The DIP leads are on 2.5 mm (0.100 in.) centers. To accommodate the DIP configuration, most printed circuits are laid out with PTHs and their associated terminal areas, or lands, on 2.5 mm (0.100 in.) gridded arrays. The reader is referred to the articles "Design" and "Printed Wiring Board Technology: Current Capabilities and Limitations" in this Volume.

As designs became more complex, designers were forced to rout signal paths between the 2.5 mm (0.100 in.) center lands. A typical configuration with a single path between lands is shown in Fig. 14(a). This is commonly referred to as one-track technology. As printed circuit technology improved, the ability to define two tracks became possible, and two-track designs became commonplace (Fig. 14b). Further improvements brought about three-track designs (Fig. 14c).

The descriptive references to one-track, two-track, and three-track imply line width and spacing dimensions of approximately 0.30, 0.20, and 0.015 mm (0.012, 0.008, and

0.006 in.), respectively. More recent device technologies, such as surface mounting and tape automated bonding, have leads on 1.3 mm (0.050 in.) centers and considerably smaller. Signal paths between surface-mount pads on 1.3 mm (0.050 in.) centers (Fig. 15) result in lines and spaces of approximately 0.20 mm (0.008 in.) and equate to two-track in terms of printed wiring complexity.

Multilayer Hole-to-Internal-Feature Registration. As routing densities increased, the circuitry internal to multilayer structures became more dense. However, the plated-hole sizes were not allowed to decrease proportionately, because device lead sizes and the tolerances associated with automatic DIP insertion did not change appreciably. With smaller internal layer features and approximately the same drill bit sizes for drilling component lead holes, the hole-to-internal-feature misregistration allowance became smaller. With the feature sizes shown in Fig. 14, the one-track hole-to-internal-land misregistration allowance (assuming that the drilled holes are not allowed to break out of the internal lands) is 240 μ m (9.5 mils). The two-track geometry

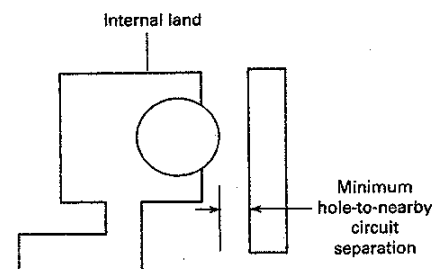


Fig. 16 Internal layer hole breakout

allows only 190 μ m (7.5 mils) misregistration. Surface-mount designs that use smaller through-hole vias often decrease this allowance to approximately 0.13 mm (0.005 in.). The material movement that was discussed in the section "Orientation/Registration Schemes" in this article, along with positioning errors, makes these tolerances very difficult to satisfy.

Some PWB specifications do not allow hole-to-internal-land breakout, and others insist on a 0.05 mm (0.002 in.) minimum annular ring, which makes the registration requirement that much more difficult to satisfy. Several companies have modified their specifications to allow internal breakout, determining that this condition does not pose long-term reliability risks. In these cases, the internal registration requirement is based on the minimum separation between the drilled holes and the circuit adjacent to the internal PTH lands (Fig. 16). The use of electrically testable registration coupons or x-ray coupons, strategically placed on multilayer panels, can provide very accurate determination of hole-to-internal-feature misregistration. The reader is referred to the article "Printed Board Coupon Metallographic Evaluation" in this Volume. When such coupons are used, some specifications allow the drilled holes to break out and encroach to within 0.010 or 0.13 mm (0.004 or 0.005 in.) of nearby circuits.

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