COMPACT MODELING OF HIGH VOLTAGE MOSFETs

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Abstract

In the automotive industry, there is a strong trend that has increased the electronics in cars for various functions like fuel injection, electric control of doors and windows, electric chair adjustment, air conditioning etc. The 12V battery used in the present cars will not be sufficient for the increasing number of functions, as a consequence, a change towards 42V batteries will be necessary. For these automotive systems, so called smart power ICs must be used. These are the chips in which the power functionality e.g. control of motor is integrated with logic control. There is also a trend towards operation at high voltages and integrating more intelligence using a microcontroller's RAM/ROM memory and several other sensors and interfaces. The final goal is the integration of a complete system on a single chip, so called power system on chip (SoC).

The interest in accurate modeling of high voltage transistors has increased in recent years due to the compatibility of these devices with standard CMOS technology. However, existing LDMOS models are not accurate enough for this task and SPICE models are specially weak for AC performance. The limitation of these models lies in their lack of capability to physically model some of the characteristic phenomena observed in high voltage devices. The increased difficulty is related to complex 2D effects specific to asymmetric high voltage device architectures.

This thesis presents the compact modeling of high voltage devices. First, a highly scalable general high voltage MOSFET model, for the first time, is presented, which can be used for any high voltage MOSFET with extended drift region. This model includes physical effects like the quasi-saturation, impact-ionization and self-heating, and a new general model for drift resistance. The model is validated on the measured characteristics of two widely used high voltage devices in the industry i.e. LDMOS and VDMOS devices, and implemented in Verilog-A code and tested on commercial circuit simulators like SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) and UltraSim (Cadence). The model exhibits excellent scalability with transistor width, drift length, number of fingers and temperature. Second, the compact modeling of lateral non-uniform doping is presented, which has great impact on the AC behavior. Third, the invalidity of Ward-Dutton charge partitioning scheme for lateral non-uniformly doped MOSFET is explained. A novel partitioning scheme is then developed and validated on the device simulation. For the first time, noise modeling of lateral non-uniformly doped MOSFET is carried out and validated on the device simulation.

Keywords: High Voltage MOSFET, DMOS, LDMOS, VDMOS, DEMOS, LAC, LAMOS, Drift, Model, DC, AC, Capacitance, EKV, HV-EKV, Partitioning, Noise, Lateral Non-uniform Doping, Scaling

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Résumé

L'industrie automobile a alimenté une forte tendance d'intégrer de plus en plus de composants électroniques dans les voitures afin d'accomplir des fonctions diverses telles que le contrle de l'injection de carburant, des vitres électriques, des siges automatiques ou de la climatisation. Les batteries de 12V utilisées dans les véhicules actuels seront bientt insuffisantes pour toutes les fonctions envisagées et par conséquent l'utilisation des sources de 42V est nécessaire. Un nouveau type de circuit intégré de puissance, appelé " smart power " IC en anglais, doit tre utilisé dans lequel la fonctionnalité du contrle de la puissance sera intégrée avec celle de la logique, par exemple pour la gestion du moteur. Il existe, d'ailleurs, une tendance vers des dispositifs haute tension avec la co-intégration d'intelligence accrue, en utilisant la mémoire RAM/ROM de microcontrleurs, en parallle avec des capteurs et d'autres interfaces. Finalement, le but sera la fabrication d'un systme complet sur puce, le systme de puissance sur puce (SoC, " System on Chip ").

La compatibilité de ces composants avec la technologie standard CMOS a récemment augmenté l'intért pour une modélisation précise des transistors haute tension. Toutefois, les modles existants LDMOS ne sont pas suffisamment précis et les models SPICE s'avrent particulirement faibles quant la performance AC. La limitation des modles mentionnés se situe dans leur incapacité de modéliser physiquement des phénomnes caractéristiques observés dans les dispositifs haute tension. La difficulté principale est liée des effets bidimensionnels spécifiques aux architectures asymétriques de ces composants.

Ce travail de thse est consacré la modélisation compacte de dispositifs haute tension. Tout d'abord, un modle MOSFET général de scalabilité accrue est présenté pour la premire fois et qui peut tre utilisé pour tous les MOSFET haute tension avec une région de " drift " étendue. Le modle en question prend en compte des phénomnes physiques tels que la quasi-saturation, l'ionisation par impact, l'autoéchauffement et il introduit une nouvelle description pour la résistance de " drift ". Par ailleurs, le modle a été validé sur des caractéristiques mesurées de deux types de composants, largement répandus dans l'industrie comme le LDMOS et le VD-MOS, mis en uvre en code Verilog-A et testé sur des simulateurs commerciaux comme SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) et UltraSim (Cadence). D'une part, le modle présente une scalabilité excellente avec la largeur du transistor, la longueur de " drift ", le nombre d'électrodes interdigitées et la température. D'autre part, la modélisation compacte du dopage non-uniforme latéral est présentée, qui a un impact considérable sur le comportement AC. En outre, l'invalidité de la théorie de Ward-Dutton sur la répartition des charges dans les MOSFET dopage uniforme est expliquée. Une nouvelle théorie sur cette répartition a été développée et validée par simulation numérique. Finalement, pour la premire fois, la

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modélisation du bruit des MOSFET dopage latéral non-uniforme a été élaborée et vérifiée par simulation numérique.

Keywords: High Voltage MOSFET, DMOS, LDMOS, VDMOS, DEMOS, LAC, LAMOS, Drift, Model, DC, AC, Capacitance, EKV, HV-EKV, Partitioning, Noise, Lateral Non-uniform Doping, Scaling

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Chapter 1

Introduction

1.1 Background

The transistor and subsequently the integrated circuits certainly qualify as two of the greatest inventions of the twentieth century. In a certain sense, all of solid-state electronics goes back to the invention by Ferdinand Braun of the solid-state rectifier in 1874 [1, 2]. That was a full 73 years before the discovery of the transistor. His work centered around the solid-state rectifier using a point contact based on lead sulfide. Of course, this configuration made for a very unstable device. In fact, after the invention of the vacuum tube, later in the century, this device very quickly became obsolete. But, later when people wanted to go to very high frequencies, and vacuum tubes would not work at the frequencies desired, the idea of the point contact rectifier made a comeback.

The theoretical development of quantum mechanics during the 1920s also played an important role in driving solid-state electronics. Without quantum mechanics, there would never have been any comprehensive understanding of solids. The understanding of the differences between metals, insulators, and semiconductors was quickly developed. The concept of electronic band structure, due to quantum mechanics, was the key to that insight. Following these advances, was the development of the quantum theory of solids led by Peierls, Wilson, Mott, Franck, and others, largely in England. These researchers added much to the understanding about electron conductivity in metals. Those days were truly the beginnings of establishing a picture of the electronic structure of metals. Metallic sodium is the simplest of all metals from an electronics point of view and was often studied in that era. A simple theory of Schottky barriers led to a crude understanding of the rectifiers discussed above, but the theory did not work quantitatively. These dedicated researchers brought the understanding forward, but semiconductors sat in the middle between the metal and the insulator, and in those days semiconductors were still a puzzle.

The continued efforts extended toward the discovery of new devices. For example, in 1926, Lilienfeld invented the concept of a field effect transistor (FET) [3]. He believed that applying a voltage to a poorly conducting material would change its conductivity and thereby achieve amplification. He patented this concept in 1926, but no one was able to do anything with it until much later.

By the late 1930s, it was beginning to be more widely accepted that there may be opportunities to create some form of solid-state devices. At this time Mervin Kelly, at Bell Labs, decided

in 1936 that he should start a solid-state device group. He challenged a number of people, Bill Shockley, Russell Ohl, Jack Scaff, and others, to begin work on solid-state devices. Kelly had a feeling that the vacuum tube was not going to be the ultimate answer to electronics. Its reliability and size were such that something needed to be done, besides making more efficient and smaller vacuum tubes. It is interesting to note that by 1938, two Germans (Pohl and Hilsch) described a solid amplifier made using potassium bromide that had three metal leads. However, this device turned out to have too low operating frequency. Also, it was not a device that could be used in any true sense for electronics. That such a device came along about the same time that Kelly created the Bell Labs solid-state group shows that other engineers were thinking along the same lines. By 1940, Russell Ohl had done a great deal of work, along with others at Bell Labs, in an attempt to understand silicon crystals. Ohl learned that depending on how you prepared single crystals of silicon, you could get either $n-$ or $p-$type silicon. What was meant by n or p type back in those days was whether it was a positive or negative rectifier. That was where the notation n or p came from. It was a question of which direction the rectification occurred; they defined these terms by that criterion. It is also interesting that a little later on, Ohl actually was able to make a sample in which the top part was a p-type region and the bottom was n type, and he found that when light was shone on it, it actually developed a voltage [4].

This was the status of solid-state electronics near the beginning of WWII, and it really did not change all that much during the war except in technology areas influenced by the work on radar. Radar requirements produced a very strong desire to fine-tune solid-state rectifiers, and this resulted in some effort to try to improve silicon and germanium materials. In this era, there was a lot of solid-state detector work done, mostly by trial and error. After WWII, the discovery of point contact transistor by Berdeen and Brattain in 1947 and the theory of the bipolar junction transistor by Shockley [5] at the Bell Telephone Laboratories [6] changed the future of microelectronics. By April 1950, Shockley et al. actually succeeded in growing the first junction npn device [7]. In fact, the device behaved essentially as predicted by Shockleys theory. Progress was supported by a series of important inventions that led to better and better devices. In fact, Shockley wrote a book titled Electrons and Holes in Semiconductors. Still it took several years before the first Si/SiO_2 MOSFET, which is now so widely used, was demonstrated by Kahng and Atalla [8, 9]. But, this turned out to be a pretty poor device. It took until the early 1970s, 15 years before planar FETs came into common use. The first integrated circuits (IC) were developed by Noyce at Fairchild Semiconductor and by Kilby at Texas Instruments. Kilby's circuits consisted of transistors fabricated using the mesa technique, where the collector contact is made to the backside of the wafer, and bonded gold wire is used for interconnect. Noyce's ICs more closely resembled present day chips because they used a planar fabrication technique developed by Hoerni at Fairchild, where oxide masking and diffusion were used to form the transistor [10].

The initial circuits were oscillators and simple digital flip-flops using two or three active devices along with passive elements, but by 1971, the technology had advanced to the stage, where the first microprocessor (Intel 4004) was fabricated with 2300 transistors. In 1965, Moore published a paper on the state of the semiconductor industry, which predicted that the number of devices in an integrated circuit would double each year [11, 12]. This prediction became the famous "Moore's Law". Today the density of transistors in a chip has crossed the billion mark.

1.2 High Voltage MOSFET models

The interest in the high voltage (HV) MOS devices has dramatically increased as these devices were integrated with the low power modules in MOS technology. Today, HV-MOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies and power amplifiers. In addition, Lateral double-Diffused MOSFET (LDMOS) devices processed in thin-film silicon-on-insulator (SOI) provides a new and attractive technology for smart power integrated circuits in consumer and automotive applications [13]. Optimal design of these power circuits requires HV-MOS models for circuit simulation, which describe the device characteristics accurately over a wide range of biases.

The accurate compact modeling of high voltage MOS transistors has always been a challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. Though many groups around the world have attempted to model the different architectures of HV-MOS transistors using different approaches, most of these are sub-circuit or macro-models. Acceptable simulation accuracy is obtained by the use of these macro-models based on conventional low voltage modules [14, 15], but these macro-models are not physical and do not take into account the special phenomena of HV devices.

The LDMOS macro model proposed by Frere et al. [15], which is being used in AMI Semiconductor (AMIS), is based on BSIM3v3.2. The model uses an adapted JFET to model the drift region and shorted PMOS transistors to model the capacitance behavior of the drift region. The drift region modeling using JFET is carried out by equations based on Schichman & Hodges [16]. The equations were implemented in Verilog-A module. The gate voltage of the JFET was tied to the intrinsic drain potential of intrinsic MOS, which provided variable threshold voltage of JFET. Two shorted PMOS transistors were used to model the gate overlap over thin and thick oxide, respectively. Even though this LDMOS model provides good behavior for both DC and AC operations, the scalability of model especially for drift length was never demonstrated.

Some other compact models have also been reported in the literature with better accuracy [17, 18, 19, 20, 21, 22, 23, 24]. Other models reported in the literature show reasonable accuracy in DC operation [17, 18, 19, 20, 22], but do not show model validity for AC operation under different biasing conditions. Although the physical LDMOS model developed by Anghel et al. demonstrated good accuracy in DC regions, it was very difficult to implement and use it for industrial purposes because of the convergence problems in the simulator. There has also been some work in the development of DMOS models using neural network based approach [25, 26]. This approach provides excellent results with speed, provided the model is trained on wide range of measurement data. The major weakness of neural network based models is that they are not scalable and can be used only for the particular device structure for which it has been trained.

The MOS model 20 (MM20) [23, 24] from NXP (earlier Philips Semiconductor) is the famous LDMOS compact model. This model has shown capability to model both DC and AC operations including quasi-saturation and self-heating effects. MM20 is a surface potential based model, whose intrinsic MOS model is similar to the MM11 or PSP [27, 28], while drift region is modeled using MM31 or MM40 [27]. MM20 model has several variations for different LDMOS structures. One model is for LDMOS with thin gate oxide all over the drift region.

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Another variation of this model is for the partial gate overlap in the drift region and uses a resistance to described the non-overlapped drift region. Then there is different model for drift region with both thin and thick gate oxides. Even though all of these models have demonstrated good results for different LDMOS devices, one has to choose different model for different devices. Also none of these models take into account the lateral non-uniform doping in the intrinsic MOS, which may result in poor accuracy in the transient operations [29, 30].

Recently Hiroshima University has developed an HiSim-LDMOS model [31, 32]. This LDMOS model is the modular extension of HiSim model, which is a surface potential based model. There has been no publication of this LDMOS model yet.

Although efforts mentioned have been successful in solving some modeling problems in high voltage devices, still there are several open challenges. Following are some of the key challenges in this field, which are also the must have features of any standard high voltage model by compact modeling council (CMC):

➤ Accurate modeling of DC/AC behavior as well as the derivatives of terminal currents and node charges with respect to node voltages for all working modes (off, linear, saturation regions and reverse modes).

➤ Charge model has to be charge conservative, and intrinsic charge model has to take into account the effects of voltage drop across the source and drain resistances.

➤ Accurate modeling of drain extension (drift) region resistance including velocity saturation.

➤ Accurate modeling of gate/drain overlap region bias dependent capacitance and resistance.

➤ Accurate modeling of parasitic effects (gate, source and drain, and substrate resistances, and source/drain-body junction diodes)

➤ Accurate modeling of the 1/f, thermal, and gate induced noise.

➤ Capable of modeling accurately with power supplies up to 200 volts and temperature ranges from -50 °C to 200 °C.

➤ Capable of modeling self-heating effects accurately and efficiently, which requires scalable temperature-dependence modeling.

➤ Capable of modeling accurately quasi-saturation effects and g_m fall-off in the saturation region, namely, the channel current compressions at higher V_{GS} when V_{DS} is greater than V_{dsat}.

➤ Capable of modeling accurately C_{GD} drop at higher external V_{GS} biases.

➤ Capable of accurate modeling of the true asymmetry of the source and drain resistances and the source and drain junctions in $I - V$ and $C - V$.

➤ Capable of modeling substrate current behavior correctly including the impact ionization taking place in the drain drift extension regions.

➤ Capable of handling scalability over a wide range of geometries, biases, and temperatures with one set of global model parameter set to cover the entire device matrix provided for model extraction. Provides drain drift region length as an instance parameter.

➤ Capable of covering reverse working mode for both symmetric and asymmetric structure (i.e. when $V_{DS} < 0$)

➤ Capable of handling of p-type devices as well as n-type devices.

➤ Good convergence in reasonable scale circuit simulation.

➤ Capable of modeling accurately a wide array of HV-MOSFET process technologies and device structures, which would include LDMOS and EDMOS (Extended Drain), both symmetrical and asymmetrical, and other drain drift extension structures including, but not limited to, those of various RESURF flavors.

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➤ Capable of modeling layout dependent characteristics including multi-finger device structures that have separate, merged, and shared source and drain connections, and point and wide source/drain contacts.
➤ Capable of modeling body bias dependency of DC and AC characteristics.
➤ Capable of providing optional temperature node for thermal electrical coupling simulation.
➤ Capable of modeling parasitic BJT effects.

In this thesis, a detailed analysis and modeling of high voltage MOSFETs will be presented. Some of the key challenges mentioned above will be addressed here.

1.3 Thesis Structure

This section briefly outlines the contents of the chapters.

- **Chapter 2: DC and AC behavior of High-Voltage MOSFETs**

A basic overview of the architectures of high voltage MOSFETs is presented. Impact of lateral non-uniform doping and drift region on both the DC and AC behavior is analyzed which paves the way to develop an accurate HV-MOS model [33].

- **Chapter 3: EKV-based Scalable General High Voltage MOSFET Model**

A new high voltage MOSFET model is developed in this chapter. The model uses charge based EKV model for the modeling of intrinsic MOS channel while drift region is modeled using bias dependent drift resistance. The model is validated on the AMIS I2T100 and I3T50 technologies. The scaling of the model is tested for different temperatures, drift length and number of fingers [34, 35, 36, 37].

- **Chapter 4: Compact Modeling of Lateral Non-uniform doping**

For the first time, true compact modeling of lateral non-uniform doping is presented. The impact of this model is emphasized on the capacitance behavior of high voltage MOSFETs. The model is validated on the AMIS I2T100 and I3T50 technologies especially for the AC behavior [29, 38, 39, 30].

- **Chapter 5: Partitioning Scheme and Noise Modeling in the Lateral Non-Uniformly doped MOSFET**

The invalidity of Ward-Dutton charge partitioning scheme for lateral non-uniformly doped MOSFET is explained. A novel partitioning scheme is then developed and validated on the device simulation [40, 41, 42]. For the first time, noise modeling of lateral non-uniformly doped MOSFET is carried out and validated on the device simulation [43].

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Chapter 2

DC and AC behavior of High-Voltage MOSFETs

The interest in the high-voltage (HV) MOS devices has dramatically increased as these devices were integrated with the low power modules in MOS technology [1, 2, 3, 4, 5]. Today, HV-MOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies, motor drivers and, power amplifiers. In addition, LDMOS devices processed in thin-film silicon-on-insulator (SOI) provide a new and attractive technology for smart power integrated circuits in consumer and automotive applications [6]. The discussion in this chapter will be focused on different HV-MOS architectures and special effects occurring in these devices.

2.1 High Voltage MOSFET architectures

There are three different types of high-voltage devices, normally used with CMOS technology. These are Drain-Extended MOSFET [4, 5, 7, 8], Lateral double-diffused MOSFET [9, 10, 11] and Vertical double-diffused MOSFET [12, 13]. Only N-channel devices are considered here but all of them have their P-channel counterparts.

2.1.1 Drain-Extended MOSFET (DEMOS)

Modern digital VLSI circuits are presently operating at the voltage levels of 1.8 V and below. However, circuit requirements often call for design and interface with other circuits operating at 3.3/5.0 V or even higher. Example circuits are input/output interface circuits with various off-chip system components, such as power management switches that regulate power from battery or system supplies, analog input circuits conditioning transducer signals, or output analog drive functions for speakers or other actuators. System designers increasingly want all of these functions in a monolithic IC to decrease system size and increase reliability. One solution to this problem of two voltage levels on an integrated circuit is to use two gate oxides and two sets of lightly-doped drain (LDD) implants [4], but this method increases the process complexity and cost. The alternate solution is to use drain extended (DE) MOS transistors [7, 8] that can operate at much higher drain voltages without significant loss of performance and without added

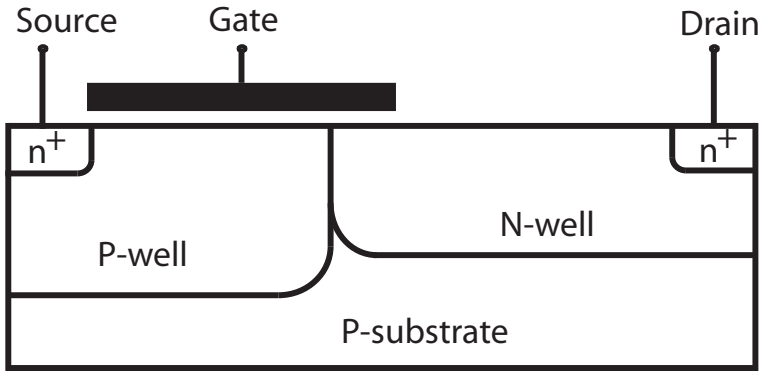


Figure 2.1: Schematic representation of the Drain-Extended MOSFET (DEMOS).

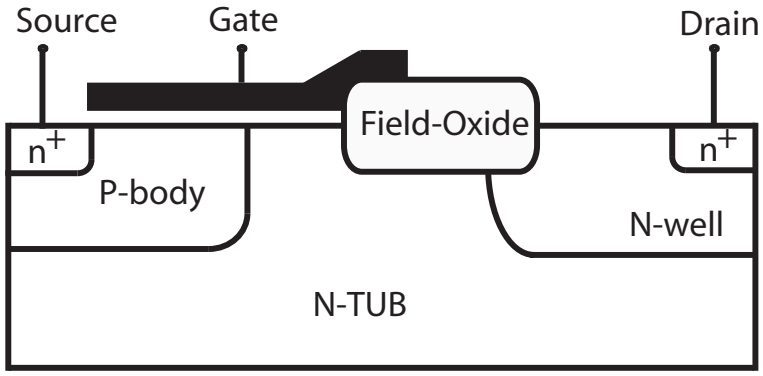


Figure 2.2: Schematic representation of the Lateral double-Diffused MOSFET (LDMOS).

process complexity. Another solution to this problem of two voltage levels on an integrated circuit that is widely used is circuit techniques such as cascading low-voltage transistors. This approach adds considerable circuit complexity and uses more power to maintain intermediate voltages for the gate drive. The use of DEMOS instead of cascaded circuits or other circuit methods offers significant die size area and power savings. It is well known that a LDD extension increases the drain breakdown voltage by reducing the electric field under the gate at the drain end of the transistor. The difficulty here has to do with achieving the goal with a higher than the very thin 4 nm oxides can normally withstand, without the luxury of a LOCOS oxide used in conventional DE style devices for the poly to terminate on. A typical twin well CMOS process, that uses p-substrate wafers, allows DE MOS transistors to be built with the n-well as the NMOS drain extension. Fig. 2.1 shows the schematic representation of N-type DEMOS device. These devices are generally used for 5V operation range especially as in input/output interfaces.

2.1.2 Lateral double-Diffused MOSFET (LDMOS)

Due to the inherent limitations of CMOS technology, DEMOS device characteristics, especially avalanche breakdown and on-resistance, are highly dependent on the n-well doping profile and surface concentration. As CMOS technology is maturing in deep-submicron lithography, other approaches were investigated in order to make available high voltage devices with

improved characteristics. The LDMOS device architecture, which actually originated from DEMOS/LDD-MOS, has much higher breakdown voltage than DEMOS architectures. Fig. 2.2 shows the schematic representation of N-type LDMOS device. The LDMOS devices are useful in high-voltage switching because of their switching speeds and relative simplicity in processing [14]. There are many variations of LDMOS devices [9, 10, 11, 15]. The device shown in Fig. 2.2 is generally used for 20-100V application e.g switch-mode power supplies and power amplifiers etc. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effective gate length is shorter than the physical length of the gate electrode. The drift region is lightly doped N-type whose length varies with increasing voltage blocking capability in the drain side. The maximum drain-source voltage, that can be applied, is determined by the breakdown voltage of the p-n junction, which is limited by the n layer doping, thickness and field crowding at the junction edge.

The electric field in the LDMOS near the silicon surface is considerably lower than in the conventional MOS or DEMOS. However, the maximum field still remains on the surface and avalanche breakdown may occur there [16]. The surface electric field can be reduced significantly by the use of thick oxide (as shown in Fig. 2.2) or field plate as the maximum field is now located inside the bulk. To reduce the on-resistance in LDMOS (with field plate), the length of the field plate should be as small as possible. The effect of field plate on LDMOS characteristics e.g. breakdown voltage, quasi-saturation effect has been studied in the literature in detail [17, 18, 19, 20, 21, 22]. The on-resistance of the LDMOS can also be decreased by using the ion-implantation in the drift region [23]. The field plate also shields the gate from the drain potential, thus minimizing the feedback (drain-to-gate) capacitance, which means improvement of RF signal gain. The p-n junction and the field plate form a fairly uniform field between gate and the drain, thus giving better breakdown voltage.

The LDMOS transistors fare much better at higher frequencies compared to their vertical counterpart (VDMOS) devices. The LDMOS transistors with frequencies more than 2.7GHz are already available in the market. Freescale has recently announced 3.8GHz high power LDMOS for coming WIMAX applications [24]. Since in the LDMOS design, the gate, source and drain are all on the top surface, chip size grows rapidly for high voltage handling capability above 200V.

2.1.3 Vertical double-Diffused MOSFET (VDMOS)

The growing chip size problem for higher operating voltages is addressed by the VDMOS transistor technology [25]. Fig. 2.3 shows the schematic representation of N-type VDMOS device [12, 13]. Since these devices have the drain at the back surface, a variety of junction edge termination schemes can be utilized at the perimeter of the die. However, the channel region itself is on the top surface and thus the current flow is lateral through the channel and vertical through the lightly doped drift. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effect of lateral non-uniform doping and lightly doped drift region on device characteristics is explained in the next section. The VDMOS design sacrifices speed for lower on-resistance and denser high-voltage layout due to large gate/drift overlap. A lower on-resistance than VDMOS is produced in VVMOS devices with similar speed as VDMOS. High speed Vertical V-groove MOS (VVMOS) devices, on the other hand, minimize gate-drain overlap at the cost of an on-resistance increase [26].

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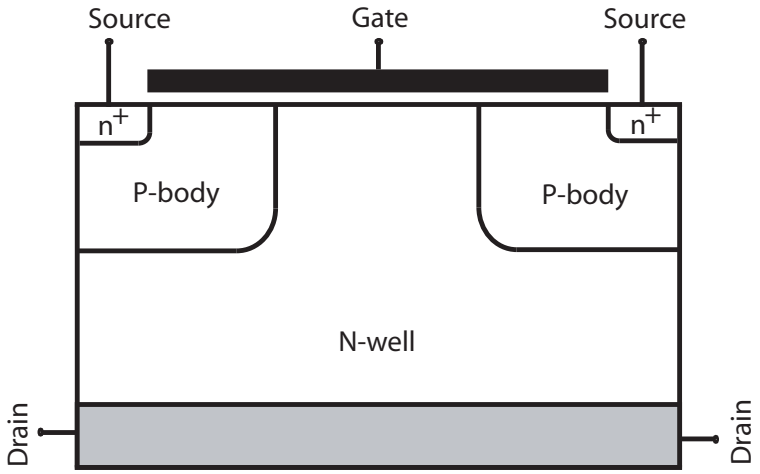


Figure 2.3: Schematic representation of the Vertical double-Diffused MOSFET (VDMOS).

2.2 DC behavior of HV-MOSFETs

The high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact, some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Even though above mentioned effects arise due to high electric fields in the device, some other special effects are also observed due to different device processes in these devices compared to conventional MOSFETs. One of the major difference in terms of device process is the lateral non-uniform doping in the channel and drift region in the drain side of HV devices. Here we will discuss the physical origin of these effects and their impact on device characteristics.

2.2.1 Quasi-Saturation Effect

The quasi-saturation effect [27, 28, 29, 30, 31] is one of the unique effect observed in HV devices other than bipolar devices [32, 33, 34, 35, 36, 37]. To explain the quasi-saturation effect, first let's discuss the saturation mechanisms in HV devices [38] using output characteristics of VDMOS transistor shown in Fig. 2.4. The current saturation on $I_{DS} - V_{DS}$ characteristics can occur due to following three mechanisms:

(a) Pinch-off in the channel: For a fixed gate voltage, if drain voltage is increased, the channel gets depleted and current saturates. This effect is called pinch-off and it is also the normal saturation mechanism in long channel MOSFETs. In HV devices, the channel pinch-off is generally observed at low V_{GS} (see $V_{GS} = 1V$ curve in Fig. 2.4).

(b) Velocity saturation in the channel: If the lateral electric field in the channel is more than certain limit called as critical field, the velocity of the electrons get saturated and thus there will be no further increase in the current for any further increase in the drain voltage. This effect is called velocity saturation, which is quite common phenomenon in short channel MOSFETs. In HV devices, this effect is generally observed for medium to high V_{GS} (see $I_{DS} - V_{DS}$ curves for $V_{GS} = 1.5, 2, 2.5, 3V$ at V_{DS}=30V in Fig. 2.4). A simple way to see this effect is that when intrinsic MOS is velocity saturated, the output characteristics become equidistant for equal

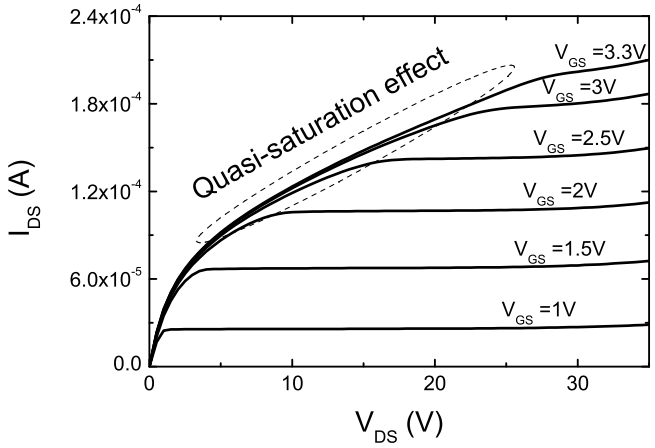


Figure 2.4: I_{DS} vs. V_{DS} from device simulation of 50V VDMOS transistor. The quasi-saturation effect is evident at higher V_{GS} for this device.

increase in V_{GS}.

(c) Velocity saturation in the drift region: Another saturation mechanism can occur due to velocity saturation in the drift while intrinsic MOS is still not saturated. Actually this cannot be called saturation as current does not get saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has no or little effect (see $V_{GS} = 2, 2.5, 3, 3.3V$ in Fig. 2.4). This effect is called quasi-saturation, which is generally observed at high V_{GS}.

Note that all or any two of the three effects described above may superimpose with each other and, sometimes, they may not be separable from each other.

The quasi-saturation effect can be reduced by reducing the resistivity of the drift region and parasitic JFET in VDMOS transistor [27]. The reduction in the quasi-saturation effect increases the current carrying capability of the devices and decreases the on-resistance. One possible method of achieving this is to exploit the trench technology [39], which allows the gate to be extended down into the intercell region. Even though it reduces the quasi-saturation effect, it introduces a corner in the trench which affects the blocking capability of the device. Another method is to use the ion-implantation into the JFET structure of VDMOS, which reduces the quasi-saturation effect with little change in the blocking capability [27].

2.2.2 Self-Heating Effect

The self-heating effect (SHE) [40, 41, 42, 43, 44, 45, 46, 47] represents the heating of the device due to its internal power dissipation. This effect appears, when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device and modifies the $I - V$ characteristics. Fig. 2.5 shows the $I_{DS} - V_{DS}$ characteristics of a 40V LDMOS transistor. The decrease in the current with increasing V_{DS} is caused by the self heating effect. As V_{DS} increases, the current starts rising. The increase in the current (I_{DS}) as well as voltage across the device (V_{DS}) increase the power dissipation ($I_{DS}V_{DS}$) inside the device. As

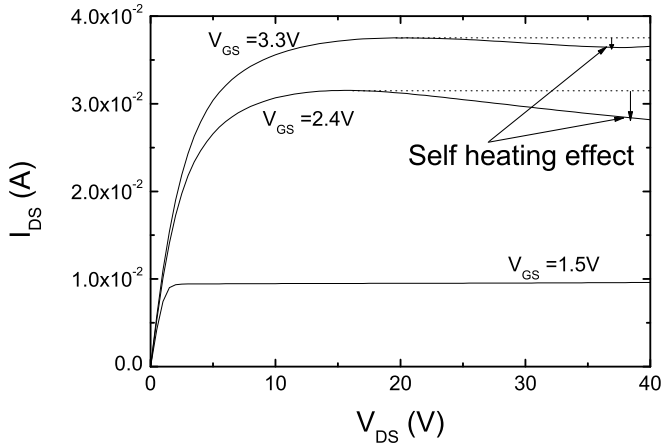


Figure 2.5: Measured I_{DS} vs. V_{DS} of 40V LDMOS transistor. The decrease in the current with increasing V_{DS} is due to self heating effect.

discussed above, the increase in power dissipation increases temperature which affects other transistor parameters (e.g. mobility, threshold voltage etc.). The rise in temperature decreases mobility due to scattering which in turn decreases the current showing negative resistance on output characteristics.

The internal temperature increase due to self heating effect influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy is obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. The detailed discussion of self-heating effect and its modeling has been covered in [47] and also in section 3.4.2 of chapter 3.

2.2.3 Impact Ionization Effect

Before discussing the impact ionization effect is HVMOS, lets review this effect for conventional low voltage MOSFETs [48].

The increase in the V_{DS} in the MOSFET increases the longitudinal electric field in the channel increasing from source to drain. For abrupt source and drain junctions, the peak field is at the drain-to-channel junction, and its value depends on V_{DS} and channel length L. When carriers move in the fields that exceed the value of the onset of velocity saturation, they continue to acquire kinetic energy from the field but their velocity is randomized by the excessive collisions such that their velocity along the field direction no longer increases but their kinetic energy does. Depending on the statistics of scattering, a small fraction of the overall carrier population acquires a significant amount of energy, and these are called hot carriers. Clearly, the higher the field, the higher the proportion of hot carriers. Generally, in MOSFETs, the high

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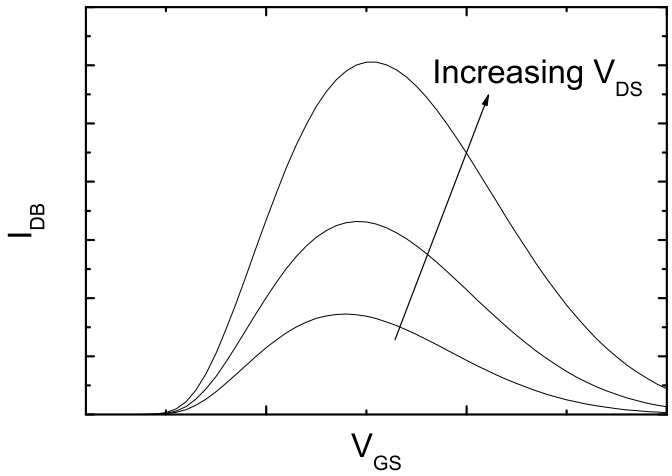


Figure 2.6: Substrate current vs. gate-source voltage, with drain-source voltage as a parameter.

fields are encountered in saturation in the pinchoff region. For large longitudinal electric field, the cool electrons are coming into the pinchoff region and are heated by the field. Some of them acquire enough energy to create impact ionization of silicon atoms, whereby new electrons and holes are created; this effect is also referred to as weak avalanche. The new electrons join the stream of channel electrons and move toward the drain. The normal depletion field in the channel pushes the holes into the substrate, where they give rise to drain-to-substrate current (I_{DB}). This current is proportional to the number of electrons available per unit time, which in turn is proportional to I_{DS}. Also, according to above discussion, I_{DB} is an increasing function of the maximum field at the drain; this field is, in turn, a function of the excess drain voltage (V'_{DS}). Fig. 2.6 shows the typical $I_{DB} - V_{GS}$ curve for MOSFET. For a given V_{DS}, when V_{GS} is increased starting from low values, I_{DS} increases, and thus I_{DB} increases too, according to above discussion. Further increase in V_{GS} increases the saturation voltage significantly, causing a strong decrease in $V_{DS} - V'_{DS}$, and thus in the maximum field at the drain. The maximum I_{DB} is observed, roughly, at $V_{GS} = V_{DS}/2$.

The impact ionization in the HVMOS device has the contributions from both the channel region and the drift region. Fig. 2.7 shows the $I_{DB} - V_{GS}$ curve for LDMOS transistor. At low current, the hot carriers are generated near the channel while at high current levels, hot carriers are generated near the drain end in the drift region. This is why there is an increase in the I_{DB} at higher V_{GS}. The impact ionization in the drift can be reduced with the field plate configuration [49]. The step drift region or deep drift design proposed in the literature also helps in the reduction of hot carriers in the drift region [49].

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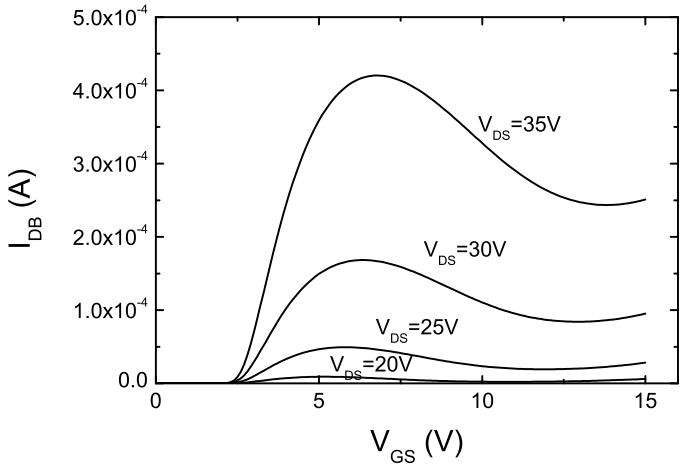


Figure 2.7: Measured substrate current vs. gate-source voltage for 40V LDMOS transistor.

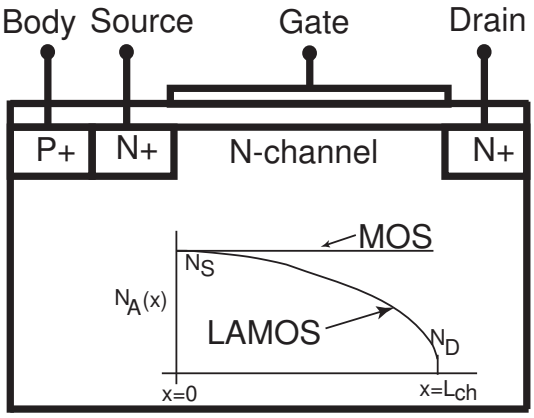
2.3 AC behavior of HV-MOSFETs

The special behavior of HV-MOS e.g. LDMOS, VDMOS capacitances has been under study in research community for many years [50, 51, 52, 53, 54, 55]. In literature, generally the HV-MOS capacitances have been studied together with drift region [52, 53], which makes it difficult to separately understand and analyze the impact of lateral non-uniform doping and drift region. The unique capacitance characteristics of HV-MOS originates from the device architecture of HV-MOS. The major difference between HV-MOS and conventional MOS is the lateral non-uniform doping in the channel and the drift region, which affects the capacitances depending on the bias regime. The unique behavior of C_{GD} in high voltage devices has been analyzed in detail in the literature [50, 51, 53]. Frére et al. [50] showed that the peaks in C_{GD} are actually originating from LAMOS. Liu et al. [53] reproduced the peaks in C_{GD} of VDMOS transistor using small signal analysis. Here, the effect of lateral non-uniform doping and drift region on capacitance characteristics of HV-MOS will be separately analyzed and compared with conventional MOS characteristics [56]. To analyze the capacitance behavior of HV-MOS, we will divide the analysis in two parts - Impact of lateral non-uniform doping and drift region. For this we will have four cases as shown in Fig. 2.8: (1) Conventional MOS with uniform doping in the channel and (2) Lateral Non-uniformly doped or Lateral Asymmetric MOS (LAMOS) with lateral doping gradient in the channel, (3) Conventional MOS with uniform doping in the channel and a drift region to sustain high voltage, and (4) LAMOS with a drift region to sustain high voltage. The intrinsic drain potential in Fig. 2.8(b) will be called V_K, which is the point where channel meets the drift region.

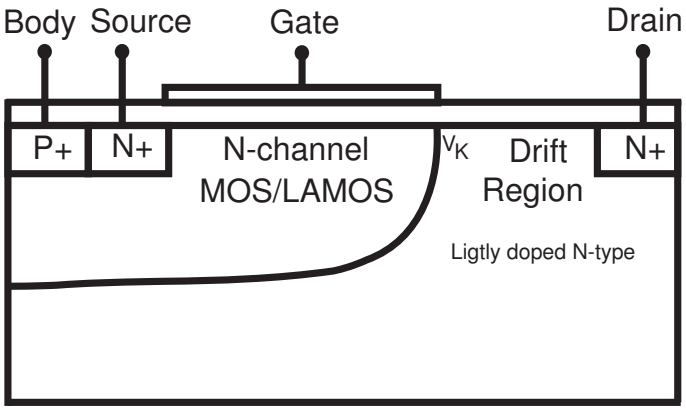
2.3.1 Effect of Lateral Non-uniform doping

Here we will explain, how lateral non-uniform doping affects the small signal capacitance behavior of high-voltage MOSFETs. Fig. 2.8(a) shows the device architecture under study. To see the impact of lateral non-uniform doping on capacitances, let's start with C_{GD} capacitance. Fig.

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(a)



(b)

Figure 2.8: Device architectures of (L_{ch}=2μm): (a) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel. The lateral doping gradient is approximated by the complementary error function $N_A(x) = N_S.erfc[k_n(\xi)]$ [57, 58, 59], where $\xi = \frac{x}{L_{ch}}$ is the normalized position along the channel, k_n is a parameter representing the doping gradient. The doping level at the source side of the channel (N_S) is highest and decreases towards the drain in the channel region. Higher k_n means sharp decrease in the doping level from source to drain and vice-versa. (b) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel and a drift region to sustain high voltage.

2.9 shows the C_{GD} vs. V_{GS} using device simulation for different drain voltages. As expected, the C_{GD} at $V_{DS} = 0$ for conventional MOS stays low values for $V_{GS} < V_T$ (threshold voltage). As V_{GS} starts to increase beyond V_T, the C_{GD} increases sharply and saturates to $\frac{1}{2}WLC_{OX}$. The situation is completely different for LAMOS. Due to lateral non-uniform doping, the C_{GD} starts increasing as soon as V_{GS} is more than the surface inversion potential at drain side. It means that the inversion at the drain side starts at lower values of V_{GS} than source side because of the lower doping at the drain end compared to source end. As V_{GS} keeps on increasing, the inversion in the channel propagates from drain towards source and C_{GD} keeps on rising. Once V_{GS} is greater than the surface inversion potential at source side (or V_T of LAMOS), the C_{GD} starts to fall [51]. This can be explained by the fact the rise in inversion charge is exponential for $V_{GS} < V_T$ and after that rise gets slower ultimately becoming linear function of V_{GS}. In strong

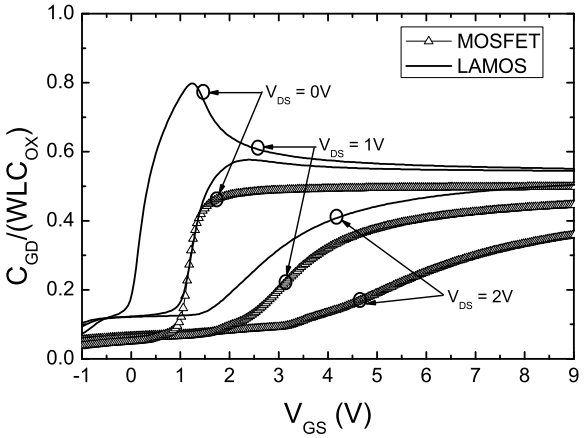


Figure 2.9: The gate-to-drain capacitance C_{GD} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GD} capacitances at low drain bias.

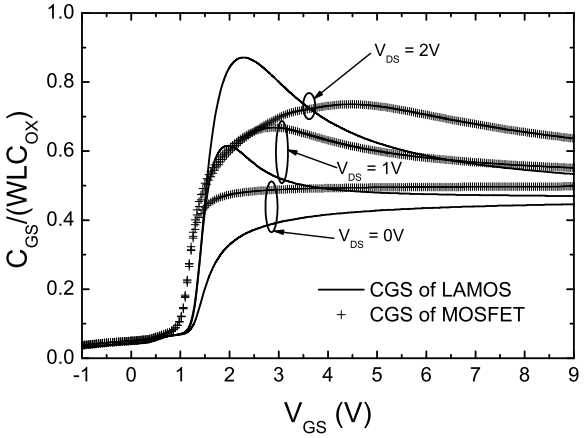


Figure 2.10: The gate-to-source capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GS} capacitances around $V_{GS} = V_T$.

inversion ($V_{GS} >> V_T$), the C_{GD} saturates to some value equal to or higher than $\frac{1}{2}WLC_{OX}$ depending on the doping gradient in the channel [58, 59]. The impact of different doping gradients on capacitances will be explained later in this section. Increasing drain voltage reduces the peak due to depletion at drain side. For sufficiently high values of drain voltages, there may not exist any peak in C_{GD} (e.g. $V_{DS} \geq 2V$ in Fig. 2.9).

Another interesting property of LAMOS capacitances is seen on C_{GS} and C_{GG} behavior as shown in Fig. 2.10 and Fig. 2.11. The C_{GS} at $V_{DS} = 0$ is similar to MOSFET (except lower values due to low doping in the drain side), where the increase in C_{GS} occurs when channel gets inverted ($V_{GS} \geq V_T$). The situation is quite different for $V_{DS} > 0$. For $V_{DS} < V_{GS} - V_{TD}$ (threshold voltage corresponding to the doping at drain), the C_{GS} is slightly higher than its value at $V_{DS} = 0$ and behaves similar to the MOS capacitance. But if $V_{DS} > V_{GS} - V_{TD}$, the

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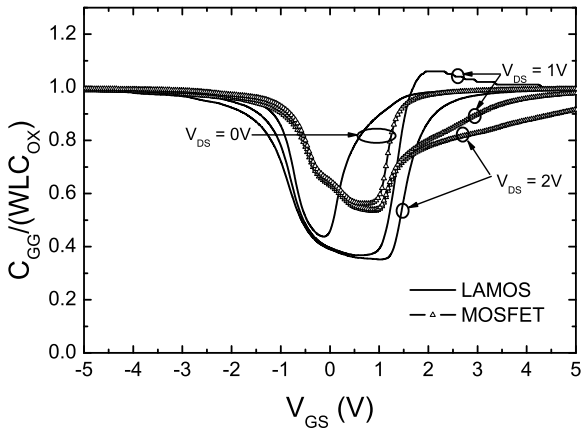


Figure 2.11: The gate-to-gate capacitance C_{GG} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GG} capacitances, when V_{GS} is around threshold voltage for small nonzero V_{DS}.

drain end is depleted. For these drain voltages, as V_{GS} increases, there will be small increase in the channel charge from drain side until $V_{GS} < V_T$. At $V_{GS} = V_T$, there is sudden flow of large amount of charges from source end (the small signal resistance seen from any point in the channel towards the drain will be higher than towards the source and charges choose the least resistive path, which is source side in this case) and whole of the channel gets filled up by these charges. This sudden rise in the charge from source side gives rise to increased peaks in C_{GS} for higher drain voltages as shown in Fig. 2.10.

It is interesting to note that C_{GG} also has small peaks for V_{DS} =1V as shown in Fig. 2.11, which was also shown in [60] for nonzero small V_{DS}. These peaks in C_{GG} can be explained by the fact that for $V_{GS} \leq V_T$, the source end of the channel is still in weak inversion while drain end is in depletion. Once V_{GS} reaches close the V_T, there will be sudden flow of charge from source side giving sharp increase in C_{GG}. This is not the case with the C_{GG} of conventional MOS, where continuous supply of charge is maintained from source side due to uniform doping. Also note that for low drain voltages, there will be large supply in the charge from drain end also once it comes out of depletion which again helps in increasing the total channel charge. Note that the peak vanishes as V_{GS} increases significantly above threshold voltage as now inversion charge is being supplied from both source and drain, and now gate charge is a linear function of gate voltage. For high values of drain voltages, no peak is observed, as charges entering from source end also contributes in removing the depletion at the drain side. Hence, the peak in C_{GG} occurs for small nonzero values of V_{DS}, when V_{GS} is around threshold voltage (source end entering into strong inversion from weak/moderate inversion). Another note on the C_{GG} of LAMOS is that the dip (lowest value) is lower compared to C_{GG} of MOS. This is due to the lower doping in the drain side which produces sharper and lower dip on C_{GG}. This can also be analyzed using segmentation approach, where LAMOS channel can be divided in several smaller channel length MOS with uniform doping in each channel but varying across different MOS giving equivalent non-uniform doping also called graded channel approach [60, 61].

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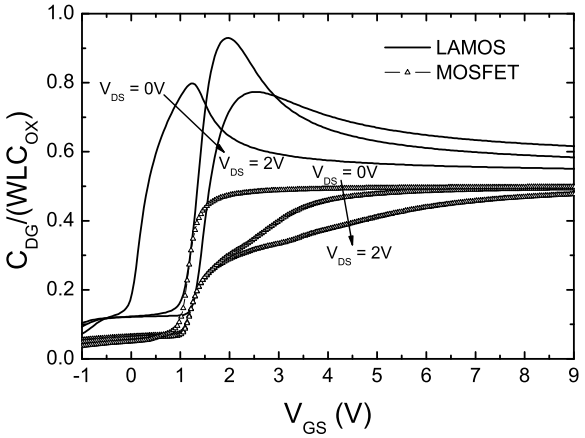
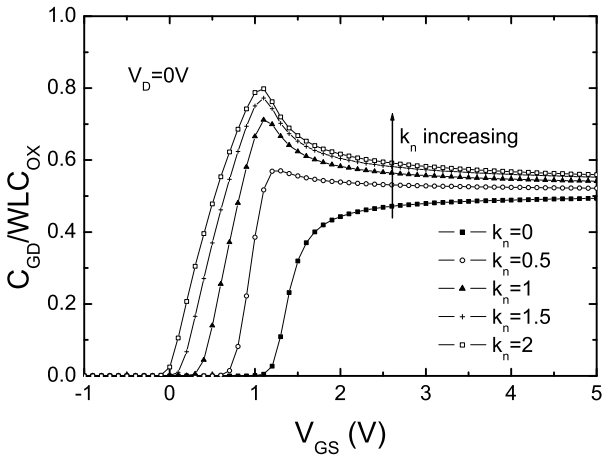


Figure 2.12: The drain-to-gate capacitance C_{DG} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{DG} capacitances. The peaks in the C_{DG} can be higher than WLC_{OX} depending on the doping profile and drain voltage [58]. The bias dependent partitioning scheme [62, 63] also explain these peaks.

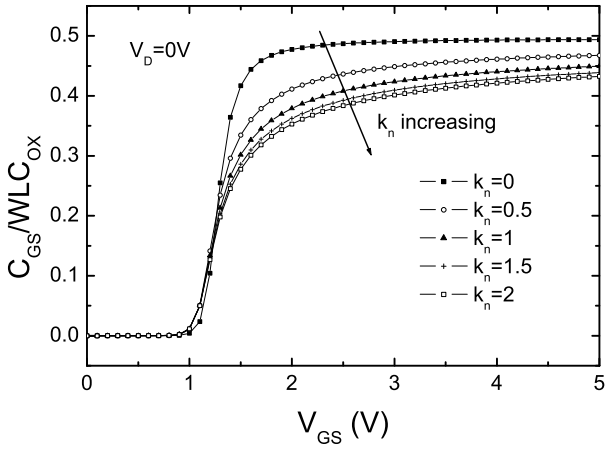
The behavior of C_{DG} capacitances is also quite different for LAMOS [60, 64, 62, 63] as shown in Fig. 2.12. Similar to other capacitances of LAMOS, peaks are also observed on C_{DG}. The peak in C_{DG} at $V_{DS} = 0$ can be explained similar to the peak in C_{GD} at $V_{DS} = 0$. As gate voltage increases, the drain end of the channel gets inverted and C_{DG} starts increasing till source end get inverted and after that it decreases and saturates. In fact C_{GD} and C_{DG} are exactly same for $V_{DS} = 0$. But for nonzero drain voltages, C_{DG} has totally different behavior than C_{GD}. At $V_{DS} = 1V$, note that the peak increases because a change in gate voltage induces a change in the channel potential (the perturbed channel potential becomes negative), which in turn causes a change in charge distribution and the combined effect increases the peak [62, 63]. To understand why perturbed channel potential can become negative to increase the small signal charge, consider the situation, when the source end is weakly inverted and drain end is strongly inverted. In this case the transistor can be thought of a series combination of two transistors with different threshold voltages, where the one near the source is weakly inverted and near the drain end is strongly inverted. Now let Q_S and Q_D be the charge at the source and drain end of the strongly inverted transistor. The current flowing through the transistor is proportional to $Q_S^2 - Q_D^2$ [62, 63, 65, 66]. The weakly inverted transistor in series forces current to be very small, therefore $Q_S^2 \approx Q_D^2$. Now as gate voltage increases both Q_S and QD will change and we have $\delta Q_S \cdot Q_S \approx \delta Q_D \cdot Q_D$. As drain end is kept at a fixed channel potential and is in strong inversion $\delta Q_D \approx C_{OX}\delta V_{GS}$. So we have $\delta Q_S/\delta V_{GS} = (Q_D/Q_S)C_{OX}$. As $Q_D > Q_S$ in this situation (because the drain end has lower doping), we have $\delta Q_S/\delta V_{GS} > C_{OX}$, which is only possible if the channel potential goes negative and aids the gate voltage. Depending on the doping profile in the channel and drain voltage, the peak in C_{DG} may even increase above WLC_{OX} in presence of a gate voltage [62, 58].

The above analysis was made using single value of doping gradient (k_n) in the channel of LAMOS. If the value of doping gradient (k_n) is increased giving sharper doping profile

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(a)



(b)

Figure 2.13: Effect of different doping gradients (k_n) on LAMOS: (a) Normalized C_{GD} and (b) normalized C_{GS} at V_{DS}=0. Note that the peak in C_{GD} increases, while C_{GS} in strong inversion decreases with increase in doping gradient. The k_n=0 corresponds to uniformly doped MOSFET.

in the channel, the peaks on C_{GD} increases and value of C_{GS} decreases in strong inversion, while the rising slope on both capacitances decreases [58] as shown in Fig. 2.13(a) and (b). The lateral doping gradient in the channel also affects DC characteristics of LAMOS. Higher doping gradient increases the saturation voltage and saturation current on the output characteristics as shown in Fig. 2.14. The prolonged linear region in the output characteristics and peaks/slopes on capacitances can be explained by the fact that doping gradient changes the surface potential required for the inversion across the channel decreasing from source to drain.

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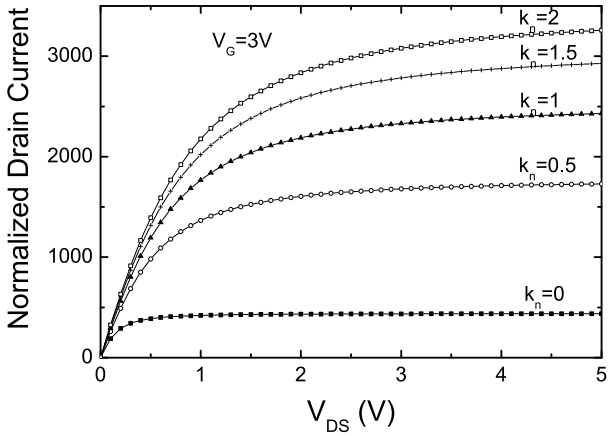


Figure 2.14: Effect of different doping gradients (k_n) on LAMOS: Normalized drain current $\frac{I_D}{2n_q\mu_0\frac{W}{L}C_{OX}U_T^2}$ at V_{GS}=3V (strong inversion). Note that the linear region extends, current as well as saturation voltage increases and R_{ON} decreases with increase in doping gradient. The k_n=0 corresponds to uniformly doped MOSFET.

2.3.2 Effect of drift region

Fig. 2.8(b) shows the device architecture under study. The effect of the drift region (without any gate overlap) is to lower the C_{GD} capacitance value in strong inversion (see LAMOS with drift region in Fig. 2.15). It is interesting to note that the C_{GD} for a conventional MOS with drift (e.g. DEMOS or LDD-MOS transistor) also shows decrease of capacitance at higher gate bias, but it should not be confused as peak in capacitance because it is always less than or equal to $\frac{1}{2}WLC_{OX}$ (see MOS with drift in Fig. 2.15). The rising part of C_{GD} is mainly given by lateral asymmetry in the channel as explained above, while the fall in C_{GD} is heavily affected by the drift region also demonstrated in Fig. 2.15. As mentioned earlier, the lateral non-uniform doping produces peaks in C_{GG} and C_{GS} around threshold voltage. The drift region gives higher peaks and also shifts the position of peaks as shown in Fig. 2.16 and Fig. 2.17 for nonzero V_{DS}. To understand it better, we can write the normalized C_{GG} expression as,

$$\begin{aligned} C_{GG} &= \frac{dQ_G(V_G,V_K,V_S,V_B)}{dV_{GS}} \\ &= \frac{\partial Q_G(V_G,V_K,V_S,V_B)}{\partial V_G} + \frac{\partial Q_G(V_{GS},V_K,V_S,V_B)}{\partial V_K}\frac{dV_K}{dV_G} \\ &= C_{GG(LAMOS)} - C_{GD(LAMOS)}\frac{dV_K}{dV_G} \end{aligned} \tag{2.1}$$

Here V_K is the intrinsic drain potential (the point where LAMOS meets drift region in high voltage devices) as shown in Fig. 2.8. If there is no drift region, then $V_K = V_D$ and second term in (4.26) vanishes as $\frac{dV_K}{dV_G} = 0$. In the presence of the drift region, V_K is not fixed and will vary to maintain a constant current from drain to source. If there is a slight positive change ∂V_G in V_G, the LAMOS current will increase. Now to increase the current in the drift region to the level of LAMOS, V_K should decrease as V_D is fixed. Larger the drift resistance, larger

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APPENDIX J

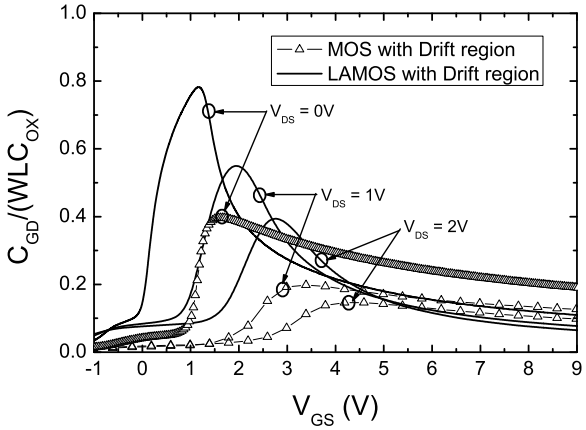


Figure 2.15: The gate-to-drain capacitance C_{GD} vs. V_{GS} for V_{DS} =0,1 and 2V. The value of C_{GD} is lowered due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be the decrease in C_{GD} capacitance.

should be the drop in V_K. Thus $\frac{dV_K}{dV_G}$ will be negative for positive values of ∂V_G and from (4.26), it is evident that C_{GG} of any high voltage device would be larger than $C_{GG(LAMOS)}$ and will increase with higher drift resistance for nonzero V_{DS}. From modeling point of view, a good model for HV-MOS needs both excellent modeling of intrinsic MOS channel (which provides $C_{GG(LAMOS)}$) and drift region (which dictates derivative of V_K) [58, 54, 67].

Similarly C_{GS} can be expressed as,

$$\begin{aligned} C_{GS} &= -\frac{Q_G(V_G, V_K, V_S, V_B)}{dV_S} \\ &= -\frac{\partial Q_G(V_G, V_K, V_S, V_B)}{\partial V_S} - \frac{\partial Q_G(V_G, V_K, V_S, V_B)}{\partial V_K}\frac{dV_K}{dV_S} \\ &= C_{GS(LAMOS)} + C_{GD(LAMOS)}\frac{dV_K}{dV_S} \end{aligned} \tag{2.2}$$

If there is a slight positive change ∂V_S in V_S, the LAMOS current will decrease. Now to decrease the current in the drift region to the level of LAMOS, V_K should increase as V_D is fixed. Larger the drift resistance, larger should be the increase in V_K. Thus $\frac{dV_K}{dV_{GS}}$ will be positive for positive values of ∂V_S and from (2.2), it is evident that C_{GS} of any high voltage device would be larger than $C_{GS(LAMOS)}$ and will increase with higher drift resistance for nonzero V_{DS}.

Above analysis of capacitances did not include the drift region with gate overlap. The effect of gate overlap in the drift region is to increase the capacitances as the total gate charge increases due to the accumulation of electrons in the overlap region for positive gate voltages or vice-versa. There is also diffusion of charges from gate overlapped drift region into LAMOS in HV-MOS, which again helps in increasing the total gate charge [52].

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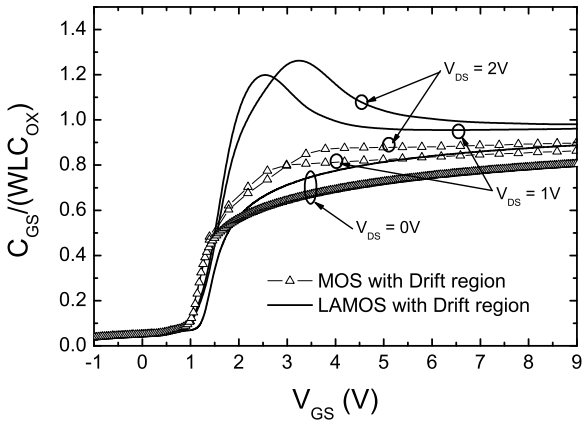


Figure 2.16: The gate-to-source capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The peak and value of C_{GS} is increased due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be the increase in C_{GS} capacitance.

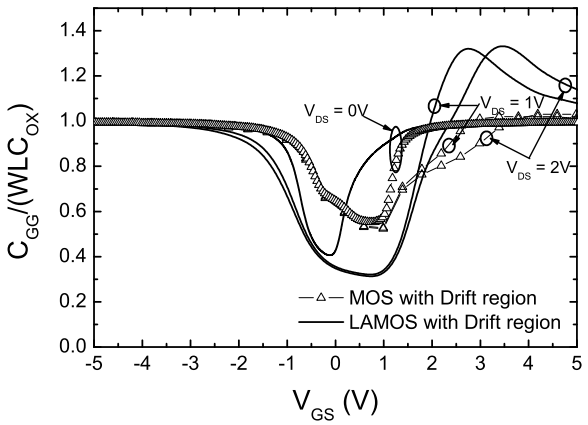


Figure 2.17: The gate-to-gate capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The peaks in C_{GG} is increased due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be thepeaks in C_{GG} capacitance.

2.4 Conclusion

In this chapter, an overview of high voltage MOSFET architecture was presented. Three main device architectures of high-voltage devices, Drain-Extended MOSFET, Lateral double-diffused MOSFET and Vertical double-diffused MOSFET, normally used with CMOS technology, were discussed. Several advantages and disadvantages of these architectures were also pointed out. Due to several different types of asymmetric architectures, there has been no single model for these devices.

The important DC effects quasi-saturation, self-heating and impact ionization were described. The quasi-saturation effect, which originates due to velocity saturation or current crowding in the drift region has been a major problem in these devices as it gives high on resistance, which is not desired. Also modeling of this effect has been a great challenge. The self-heating effect is another unwanted effect observed in high voltage devices. The high voltage and current gives rise to high power dissipation, which in turn increases the temperature inside the device. The rise in temperature severely affects the device characteristics giving rise to negative resistance on output characteristics. The modeling of this effect has also been a problem in the past. Even today, there are no compact expressions to describe this effect in high voltage devices. The impact ionization effect occurs due to high field in the device. The impact ionization in the high voltage devices occurs at both places, the intrinsic MOS and drift region. The impact ionization in the intrinsic MOS region occurs at low to medium V_{GS} for certain V_{DS}, while impact ionization in the drift region dominates at higher gate voltages. Also the impact ionization current in the drift region does not decrease with increase in gate voltage, which is not the case in conventional MOSFET, where it decreases after giving a peak in the drain current.

An in depth study of high voltage MOSFET capacitance was carried out by separately analyzing the impact of lateral non-uniform doping and drift region. It was demonstrated that the capacitance peaks in high voltage MOSFET at low gate bias are dominated by lateral non-uniform doping while at higher gate bias, the decrease in capacitances is affected by both the lateral non-uniform doping as well as the drift region. One of the major capacitance, which gets affected by lateral non-uniform doping is the C_{GD}. The early rise in C_{GD} was explained by the early inversion at the drain side which then propagates towards source with increase in the gate voltage. It was demonstrated that the drift resistance will always decrease the capacitance value for positive gate bias in N-type DMOS and for negative gate bias in P-type DMOS. The effect of gate overlap in the drift region is to increase the capacitance due to accumulation charge for positive gate bias for N-type DMOS or vice-versa. From this study, it is clear that an accurate high voltage MOS model needs to correctly model the lateral non-uniform doping (which has been a great challenge) and drift region behavior especially for RF LDMOS, where small signal capacitances plays the main role in device performance.

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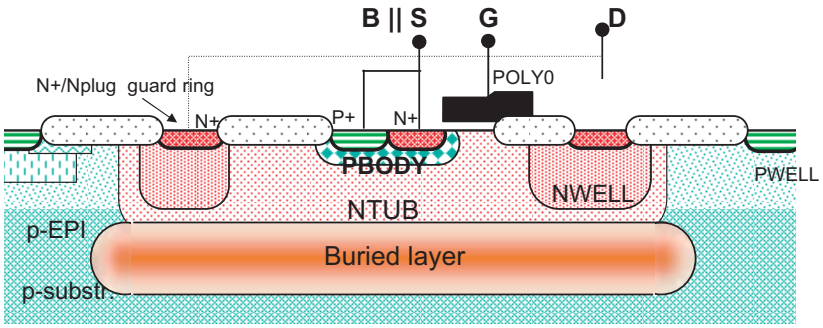
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Chapter 3

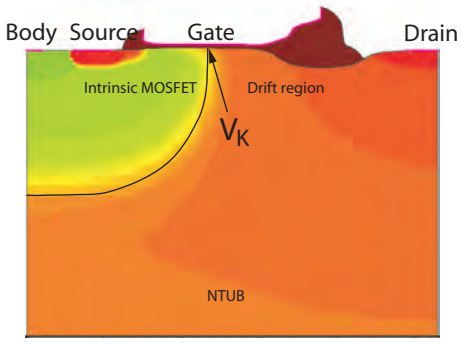
EKV-based Scalable General High Voltage MOSFET Model

The accurate compact modeling of High Voltage (HV) MOS transistors has always been a great challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. Though many groups around the world have attempted to model the different architectures of HV MOS transistors using different approaches, most of these are sub-circuit models. To the best of our knowledge, in the literature, there is no available compact *general* HV MOS model (i.e. a single model for any HV MOS device e.g. LDMOS and VDMOS) capable of combining the accuracy, speed, scalability for both DC and AC domains. Acceptable simulation accuracy is obtained by the use of adopted macro-models based on conventional low voltage modules [1, 2], but these macro-models are not physical and do not take into account the special phenomena of HV devices. Some compact models have also been reported in the literature with better accuracy [3, 4, 5, 6, 7, 8, 9, 10]. Halleweyen et al. [3] and Aarts et al. [8] reported surface potential based LDMOS models but only for DC operations. Previously Aarts et al. [7] reported a physical LDMOS model for both DC and AC operations, however scalability of the model has not been shown. Other models reported in the literature show reasonable accuracy in DC operation [4, 5, 6, 9, 10], but do not show model validity for AC operation under different biasing conditions and model scalability especially with temperature, drift length and number of fingers.

In this chapter, a modeling strategy for HV MOS transistors based on the scalable drift resistance [11, 12] and the use of EKV2.6 MOSFET model [13] as a core for the intrinsic MOS channel is presented [14, 15]. The strategy is optimized according to the fast convergence and good accuracy criteria. The model is stable and robust in the entire bias range useful for circuit design purpose. An important aspect of this *general* model is the scalability of the model with physical and electrical parameters along with the correct modeling of quasi-saturation and self-heating effect. The model is validated on the measured characteristics of two widely used high voltage devices in the industry i.e. LDMOS [16] and VDMOS [17] devices, and implemented on commercial circuit simulators like SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) and UltraSim (Cadence). The accuracy of the model is better than 10% for DC I-V and g-V characteristics and shows good behavior for all capacitances which are unique for these devices showing peaks and shift of peaks with bias variation. Also the model exhibits excellent



(a)



(b)

Figure 3.1: (a) Schematic representation and (b) device architecture of 40V SOI-LDMOS transistor from I2T100 AMIS technology. The separation boundary between the intrinsic MOSFET and the drift region is the metallurgical junction of the PIN diode.

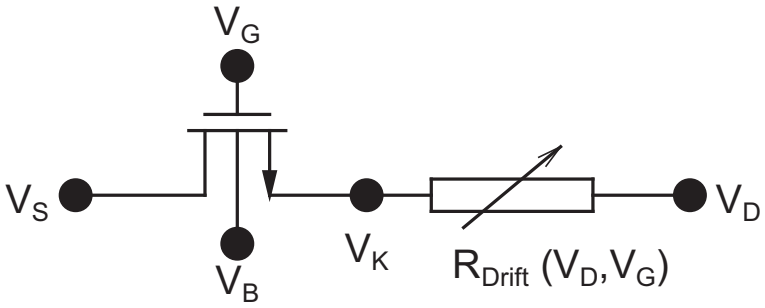


Figure 3.2: High Voltage MOSFET modeling strategy.

scalability with transistor width, drift length, number of fingers and temperature.

3.1 Behavior of surface potential in the drift region

The LDMOS device architecture under study is shown in Fig. 3.1(a). The channel of the LDMOS transistor is obtained by a double diffusion process and not by photolithographic process. Consequently, this transistor has gradual doping profile in the channel decreasing from source to the intrinsic drain (V_K) of the device. The second part of the device, i.e. the drift zone,

sustains the high voltage applied on the drain terminal of the device. The device presents a gate overlap over both the channel and the drift region, involving the possibility to obtain operation regions where the intrinsic channel is inverted and accumulation/depletion may exist in the drift region under gate.

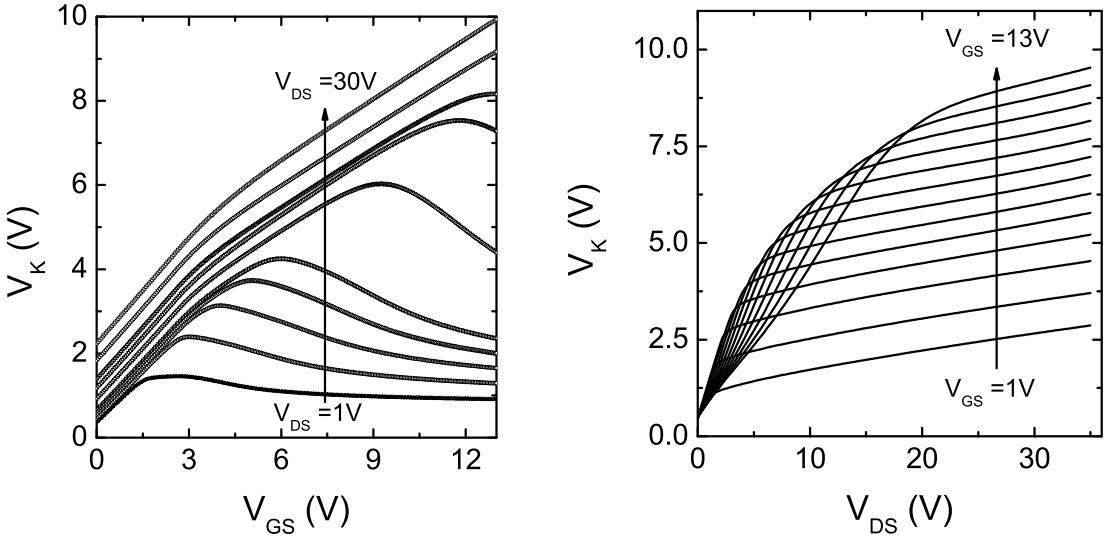
Fig. 3.2 shows the modeling strategy used in this chapter. The HV MOS is divided into low voltage MOS channel and a drift region. The major issue in HV MOS modeling that make standard low-voltage MOSFET models un-applicable is the bias dependence of the drift resistance (R_{Drift}) with both gate and drain voltages. Consequently, the efforts in this chapter will be concentrated on different solutions to analytically describe the main dependencies of R_{Drift}, in all operation regimes using simple analytical expressions. The modeling of the intrinsic MOS channel is carried out using EKV model [13]. To understand the behavior of drift region, 2-D numerical device simulation is performed using ISE-DESSIS. The idea is to separate the device into physically significant regions and then to inspect and model them independently. The separation boundary between the intrinsic MOS transistor and the drift region is the metallurgical junction of the PIN diode (see V_K point in Fig. 3.1(b)). Fig. 3.3 shows the plot of V_K for different gate and drain voltages. Fig. 3.3(a) and Fig. 3.3(b) show the V_K vs. V_{GS} and V_{DS} respectively [18]. The unique behavior of V_K can be explained by considering the variation of the channel and drift resistance with bias. Initially as V_{GS} increases, most of the drain voltage drop occurs across intrinsic MOS channel as channel resistance is very high compared to drift resistance. With increasing V_{GS}, channel resistance drops sharply compared with drift resistance and at some bias condition, channel resistance becomes equal to drift resistance. This is the point, where, the peak in V_K occurs on $V_K - V_{GS}$ characteristics (see Fig. 3.3(a)). If V_{GS} keeps on increasing after this point, V_K keeps on decreasing as drift resistance now dominates compared to channel resistance. This same explanation can be easily associated with $V_K - V_{DS}$ characteristics also (Fig. 3.3(b)). Please note that the effect of drift resistance is observed in the linear region only (see Fig. 3.3(b)). There are two interesting points to note here. First, the major V_{DS} drop occurs across the drift region, which is also the desired feature. Second, the V_K behavior is quite different in the linear region while it saturates or varies slowly at higher drain voltages. This analysis also points out the importance of the modeling of the drift region in the linear region.

3.2 GENERAL DRIFT RESISTANCE MODEL

Fig. 3.4(a) and 3.4(b) show the schematics of high voltage VDMOS and LDMOS devices, respectively. Even though, here simple device architectures are shown, the model can be used, as described earlier for any HV device which uses extended drift region to handle the high voltage applied at the drain terminal e.g. LDMOS with thin or thick oxide (shown in Fig. 3.1(a)) etc.

As discussed in the previous chapter, the intrinsic drain voltage (V_K) always remains at low values for entire bias domain [18]. Based on this understanding, we consider our device divided into an intrinsic MOSFET region and a drift region, where the intrinsic transistor part is modeled by using low voltage EKV model [13] described in the next section while modeling of drift region is carried out by using bias dependent resistance explained below. The motivation to use a resistance to model the drift region is to get the fast convergence along with excellent

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(a) (b)

Figure 3.3: Behavior of intrinsic drain potential (V_K) from numerical device simulation: (a) Plot of V_K vs. V_{GS}. (b) Plot of V_K vs. V_{DS}.

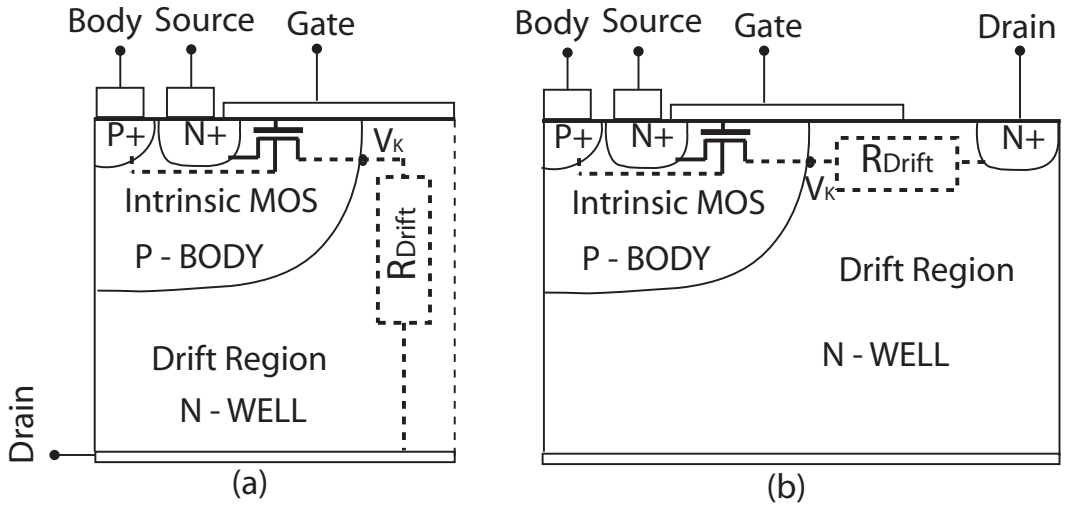


Figure 3.4: Schematic representation of high voltage (a) Vertical DMOS (VDMOS) and (b) Lateral DMOS (LDMOS) device Architecture.

accuracy. The simplest resistance expression could be a constant resistance. Fig. 3.5 shows the transfer characteristics ($I_{DS} - V_{GS}$) using constant resistance (dash lines) as drift resistance. It can be seen that the constant resistance accurately models the low drain and low to medium gate bias behavior, as at low drain bias, the intrinsic transistor drives the current while the drift region behaves like a constant resistor. Another interesting remark is that the fixed resistance cannot model the behavior of the device at low V_{DS}, when high gate voltage is applied. The explanation for this deviation comes from the accumulation charge sheet, which extends into

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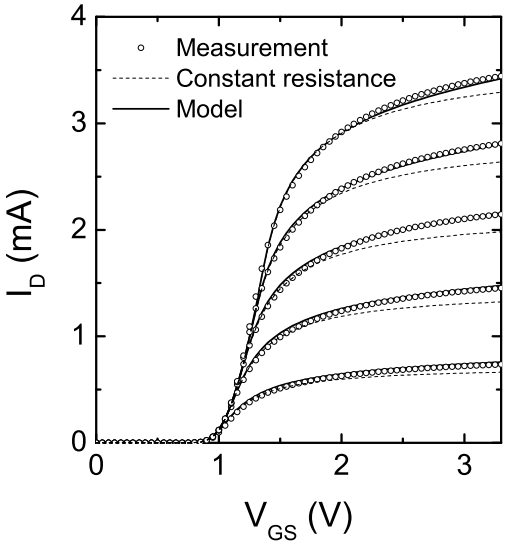


Figure 3.5: I_{DS} vs. V_{GS} for V_{DS}=0.1 to 0.5V for 50V VDMOS transistor. The constant resistance along with the accumulation charge sheet effect provides excellent accuracy at low drain bias.

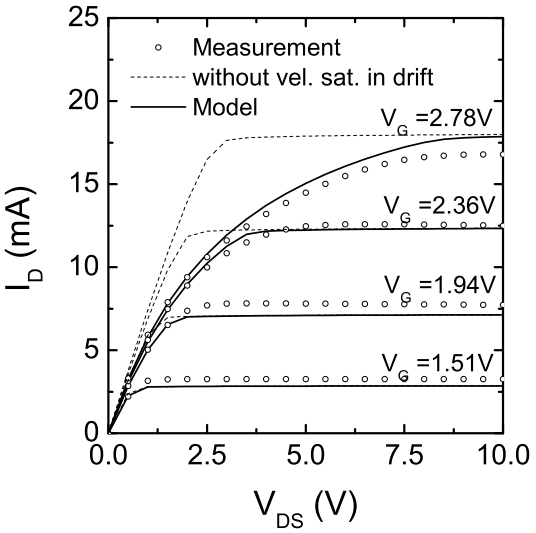


Figure 3.6: I_{DS} vs. V_{DS} for 50V VDMOS transistor. The modeling of velocity saturation effect on drift resistance provides good behavior in the linear region.

the drift region with the increase of the gate voltage and lowers the resistance of the drift part. In order to simulate the above described effect, a slight reduction of the drift resistance with the gate voltage is introduced in the model:

$$R_{Drift} = \frac{R}{1 + \theta_{Acc} \cdot |V_{GS}|} \tag{3.1}$$

where R is the constant resistance, θ_{Acc} is the gate bias modulation parameter (effect of accumulation charge sheet on R_{Drift}) and V_{GS} is the applied gate voltage. The value of R can be obtained by extracting the silicon resistivity and then calculating the global resistance function of the geometrical dimensions, if the doping concentration of the drift zone is known. The model behavior using (3.1) is shown in Fig. 3.5 by solid lines. It can be observed that the matching between the simulation and measured data is excellent. Thus, it can be concluded that (3.1) correctly reproduces the physics inside the device. Moreover, this expression proves to be highly efficient in terms of implementation as it uses the simplest representation and the minimum number of parameters for the description of the physical phenomenon at low gate and drain bias. Fig. 3.6 shows the $I_{DS} - V_{DS}$ characteristics using drift resistance derived above by dash lines. It is easily observable that even though above derived expression showed excellent characteristics at low V_{DS}, it is not working well at higher V_{DS}. It is also important to mention that once the current saturates in the intrinsic MOS transistor, the drift part has no influence on the current. Consequently, the drift part only affects the linear regime of the output characteristics. Although, this influence seems to be limited, the transition from linear to saturation is very sensitive to the drift resistance variation. The delayed transition between linear and satu-

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ration regime at high gate voltages occurs due to the carrier velocity saturation in the drift and is equivalent to an increase in the resistance of the drift region. In literature, the carrier velocity saturation effect on the current is modeled using hyperbolic dependence of the electric field across the region. It means that this dependence would be linear for the resistance. Thus, in order to simulate the carrier velocity saturation dependence using the drift resistance expression, a direct dependence on the field applied in the drift region is introduced as:

$$R_{Drift} = R \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \tag{3.2}$$

where $VSAT$ and α_{vsat} are the velocity saturation parameters. L_{DR} is the length of the drift region. The mobility is considered constant all over the current path and the electric field uniformly distributed along the length of the drift region. Solid lines in Fig. 3.6 show the drain current using (5.3), which proves that this expression takes into account major physical phenomena in the drift region.

The final expression for the drift resistance including geometry and temperature effects can be written as [11, 12]:

$$R_{Drift} = R_{Drift0} \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \cdot \left[1 \pm (k_{rd} - 1) \cdot \left(\frac{N_F - 1}{N_F + N_{CRIT}} \right) \right] \cdot (1 + \alpha_T \cdot \Delta T) \tag{3.3}$$

where R_{Drift0} is the value of the drift resistance at low bias voltage defined as

$$R_{Drift0} = \rho_{_{Drift}} \cdot \left[\frac{L_{DR}}{(W + \Delta W) \cdot N_F} \right] \tag{3.4}$$

Where $\rho_{_{Drift}}$ is the resistivity per unit length at room temperature ($T = 300K$). W, ΔW and N_F represent the width, width offset and number of fingers respectively. N_{CRIT} and k_{rd} are the parameters for drift scaling with number of fingers. The "+" sign is used for drain-on-side devices while "−" sign is used for drain-all-around devices. α_T is the temperature coefficient of the drift region and ΔT is the difference in ambient temperature with normal room temperature ($T = 300K$).

3.3 CHARGE EVALUATION based on EKV MODEL

The main reason behind using EKV MOSFET model [13] for intrinsic channel is that EKV model has physical expression for current and charges, which are continuous from weak to moderate to strong inversion. Another important characteristic of the EKV model is that compared with other existing MOS models (e.g. BSIM), it uses less number of parameters, most of which are all physical. The intrinsic drain-to-source current (V_K to V_S in our model) in EKV model is given as

$$I_{KS} = I_S(i_f - i_r) \tag{3.5}$$

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where I_S is the specific current [13] defined as

$$I_S = 2 \cdot n \cdot \beta \cdot U_T^2 \tag{3.6}$$

$$n = \frac{1}{1 - \frac{\gamma}{2 \cdot \sqrt{V_{GS} - V_T + (\frac{\gamma}{2} + \sqrt{\psi_0})^2}}} \tag{3.7}$$

$$\psi_0 = 2\phi_F + several\ U_T \tag{3.8}$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \tag{3.9}$$

where U_T=$\frac{kT}{q}$ is the thermal voltage, n is the slope factor, V_T is the threshold voltage, γ is the body effect parameter and, C_{ox} is the oxide capacitance per unit area. The normalized forward current i_f and normalized reverse current i_r are defined as

$$i_f = \left[ln(1 + e^{\frac{v_p - v_s}{2}}) \right]^2, \tag{3.10}$$

and

$$i_r = \left[ln(1 + e^{\frac{v_p - v_k}{2}}) \right]^2, \tag{3.11}$$

where $v_p = \frac{V_P}{U_T}$, $v_s = \frac{V_S}{U_T}$, $v_k = \frac{V_K}{U_T}$ are the normalized pinch-off ($V_P = \frac{V_{GS} - V_T}{n}$), source and intrinsic drain voltage respectively [13].

The total gate charge is the sum of the charges related to intrinsic-drain (V_K), source, body and drift. The charges associated with the intrinsic MOS are directly obtained from EKV model [13].

The R_{Drift} expression (3.3) used above for current modeling does not provide the correct behavior for intrinsic drain voltage (V_K) at low-gate/high-drain biases, as this resistance in actual case should rise to Giga-ohm at low-gate/high-drain biases. The preceding statement is verified by the fact that at low gate bias, the drift region is in depletion and most of the voltage drop applied on drain terminal occurs in this region and the current is very small. But this resistance provides accurate current prediction because at low-gate/high-drain bias (intrinsic MOS in saturation), the current is well modeled by the intrinsic MOS part. The impact of the intrinsic drain potential (V_K) on AC characteristics was shown by Hefyene et al. [19, 20]. The correct V_K behavior is not only important for the peaks of capacitances which are very specific to high voltage devices, it is also extremely important for the position of the peaks with gate and drain bias. Thus it is extremely important to first obtain the correct V_K behavior with gate and drain bias. In literature, this is obtained using interpolation between V_K in the linear region and V_{Ksat} in the saturation region to limit the value of V_K to V_{Ksat} [3]. In this work, the accurate V_K value, which is used in the calculation of accumulation charge, can be obtained by backtracking of K-node charge as given below. The motivation for this strategy is to get the impact of current saturation on charge and then on V_K.

The V_K behavior which has great impact on capacitance of high voltage devices [19, 20], is obtained by backtracking of K-node charge or current backtracking [21, 14]. The normalized potential v_k is expressed as a function of v_p and q_k (normalized inversion charge density at V_K) as [21]

$$v_k = v_p - (2 \cdot q_k + \ln q_k) \tag{3.12}$$

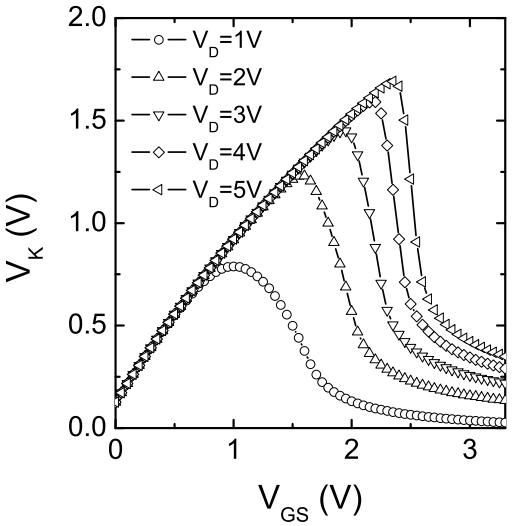


Figure 3.7: Intrinsic-drain potential V_K vs. V_{GS} for V_{DS}=1 to 5V in steps of 1V for VDMOS transistor. The decrease in V_K is caused by drift region.

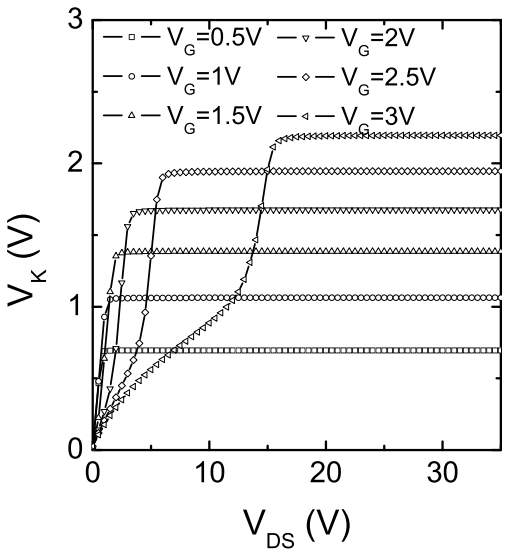


Figure 3.8: Intrinsic-drain potential V_K vs. V_{DS} for V_{GS}=0.5 to 3V in steps of 0.5V for VDMOS transistor.

where q_k is expressed as [21]

$$q_k = \sqrt{i_r + 0.25} - 0.5. \tag{3.13}$$

Thus V_K can be easily expressed as

$$V_K = U_T \cdot [v_p - \{2 \cdot (\sqrt{i_r + 0.25} - 0.5) + \ln(\sqrt{i_r + 0.25} - 0.5)\}] \tag{3.14}$$

The intrinsic drain potential (V_K) behavior obtained by this method shows excellent agreement with literature [22] (see Fig. 3.7 and 3.8).

The normalized drift accumulation charge density can be written as

$$q_{drift} = v_g - v_{fb\_drift} - \psi_{s\_drift}. \tag{3.15}$$

where v_{fb_drift} is the normalized flat-band voltage of drift region and ψ_{s_drift} is the normalized surface potential in the drift region. The total drift accumulation charge is obtained by integrating the drift charge density over the gate overlap length, assuming ψ_{s_drift} varies linearly in the drift region also validated from numerical device simulation.

Thus total gate charge can be written as,

$$Q_G = Q_S + Q_K + Q_B + Q_{Drift}, \tag{3.16}$$

where Q_S, Q_K and Q_B are the charges related to source, intrinsic drain and body node respectively, obtained from EKV MOS model [13].

The capacitances are defined using standard method as:

$$C_{ij} = \begin{cases} -\frac{\delta Q_i}{\delta V_j} & i \neq j \\ +\frac{\delta Q_i}{\delta V_j} & i = j \end{cases}$$

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APPENDIX J

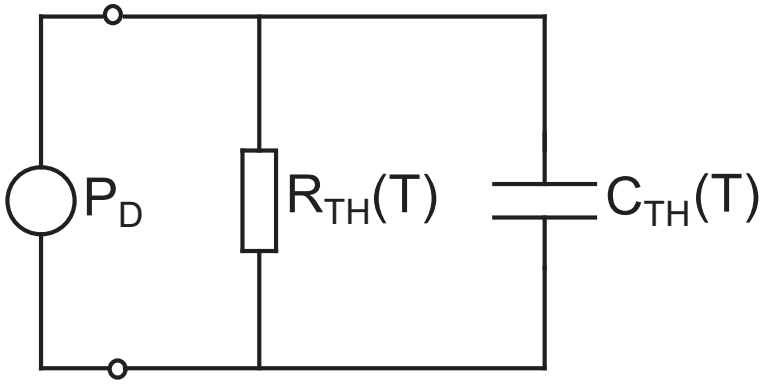


Figure 3.9: Representation of the electro-thermal circuit for self-heating effect simulation (Power dissipation $P_D = I_{DS}V_{DS}$, thermal resistance R_{TH}(T)=R_{THNOM}(1+$\alpha\Delta T$) and thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$) [23, 24].

3.4 Modeling of Quasi-Saturation and Self-Heating Effects

As discussed in the previous chapter, the high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Here we will discuss, the modeling of these effects.

3.4.1 Quasi-Saturation Effect

The quasi-saturation effect is one of the unique effect observed in HV devices. This effect originates due to velocity saturation in the drift region when intrinsic MOS is still not saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has small effect. As our drift resistance already includes the velocity saturation in the drift, the quasi-saturation effect is easily modeled by this model.

3.4.2 Self-Heating Effect

The self-heating effect (SHE) represents the heating of the device due to its internal power dissipation. This effect appears when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device. The internal temperature increase influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy was obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. Fig. 3.9 shows the equivalent sub-circuit used for the self-heating

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representation. This classical representation can be used for the DC, AC or transient simulation of the device in some critical regimes (other than analog operation).

In our model, the SHE is modeled using standard circuit shown in Fig. 3.9, where the thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) varies dynamically with the device temperature [23, 24]. The extraction procedure for R_{TH} and C_{TH} has been discussed in [23, 24]. The expressions for thermal resistance and capacitance from [23, 24] are re-written here to complete this discussion.

The thermal resistance is expressed as [23, 24]

$$R_{TH} = R_{THNOM}(T_e) \cdot [1 + \alpha \cdot (T_i - T_e)] \tag{3.17}$$

where T_e, T_i are the ambient and internal device temperatures, respectively and R_{THNOM} is also considered a linear function of the ambient temperature as follows:

$$R_{THNOM}(T_e) = R_{THNOM}(300K) \cdot [1 + \alpha \cdot (T_e - 300K)] \tag{3.18}$$

One should note that in (4.12), the temperature increase, $\Delta T = T_i - T_e$, at known ambient temperature is essentially given by SHE (related to the injected electrical power P_D), and consequently, R_{THNOM} could be considered as the nominal thermal resistance at zero injected power (at given ambient temperature T_e). The thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$ and temperature coefficient of thermal resistance α are extracted from $I_{DS} - V_{DS}$ characteristics for different pulse widths τ_w [23, 24].

3.4.3 Impact Ionization Effect

When the drain bias across the device increases, the electric field in the drift region also increases as a function drain bias. In this high field zone, the longitudinal electric field varies linearly and reaches its peak value at the drain junction. The impact ionization current (or avalanche current) can be expressed as

$$I_{avl} = (M - 1) \cdot I_D \tag{3.19}$$

Where M is called as Multiplication factor. Rossel et al. [25] developed the following approximate expression for M from impact ionization integral assuming low multiplication level.

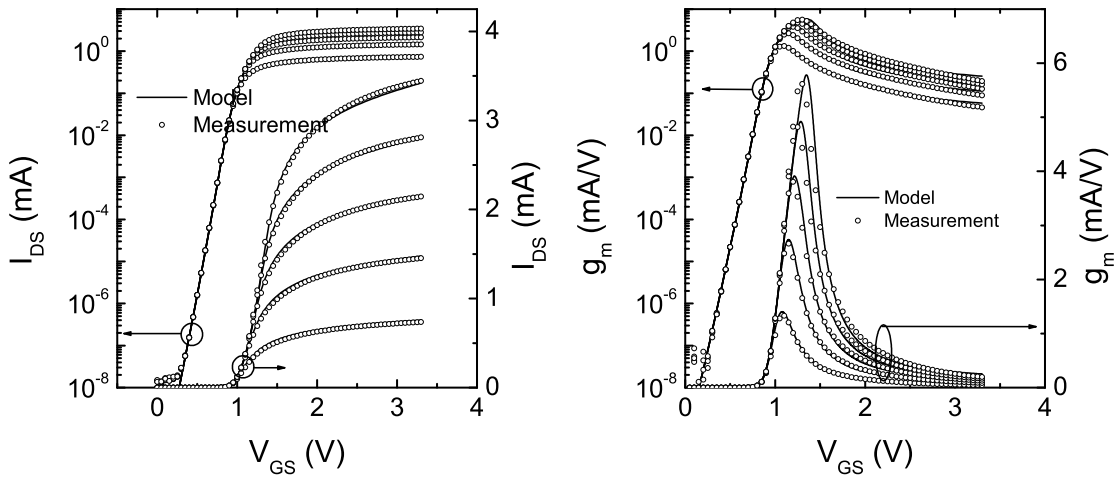
$$M - 1 \simeq 1 - \frac{1}{M} = (2.8 \cdot 10^{-73}) \cdot N_{eff}^3 \cdot V_{DS}^4 \tag{3.20}$$

In the model implementation, we combined the constant $(2.8 \cdot 10^{-73})$ with N_{eff} and used a single parameter N_{EFF}. Thus multiplication factor M can be written as:

$$M - 1 = N_{EFF}^3 \cdot V_{DS}^4 \tag{3.21}$$

3.5 MODEL VALIDATION and RESULTS

This model is calibrated on the measured characteristics of a 50V VDMOS and 40V LDMOS devices provided by AMIS and BOSCH [17, 16]. The source and body are tied to avoid parasitic bipolar transistor for all measurements.



(a) (b)

Figure 3.10: Transfer characteristics of VDMOS transistor at low drain bias for W=40μm, L=0.6μm and N_F=2 at T=30°C: (a) I_{DS}-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V. The current at higher V_{GS} is heavily affected by drift region. (b) g_m-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V. The sharp decrease in transconductance at higher gate bias can be explained by the dominance of drift resistance over channel resistance.

3.5.1 Case Study 1: VDMOS Transistor

The schematic representation of the VDMOS device (half of the device is shown as it is symmetrical along the vertical axis) under study is shown in Fig. 3.4(a). Fig. 3.10(a) shows the transfer characteristics for low drain bias, which demonstrates that the model provides accurate simulation of current and subthreshold slope. From Fig. 3.10(b), it can be observed that the model not only gives accurate values of peak in transconductance and its slope in the subthreshold regime but also predicts the correct behavior after the peak, which is very important in circuit design. Fig. 3.11 shows the transfer characteristics for medium drain bias (V_{DS}=1V to 5V in steps of 1V). The drain current at higher gate voltages is heavily affected by the drift region. Fig. 3.12 (a) and (b) show the output characteristics and output-conductance, respectively, for different gate bias which show that not only the transition from linear to saturation regime in I_{DS} is well simulated by the model, validating correct drift model, it also correctly simulates the self-heating effect in the output characteristics. The dips in output-conductance are also well predicted by the model. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect. Capacitances C_{GD} and $C_{GS} + C_{GB}$ obtained using this model, are shown in Fig. 3.13 (a) and (b), respectively. The special behavior of the high voltage capacitances, i.e. the peaks [7, 20] in C_{GD} and C_{GS} are well modeled. It can be seen that all the capacitances show good trend for the entire gate and drain bias range. It should be noted that in literature very few models have been successful in modeling the correct behavior of capacitances of HV MOS devices [1, 2, 7, 11, 12]. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS

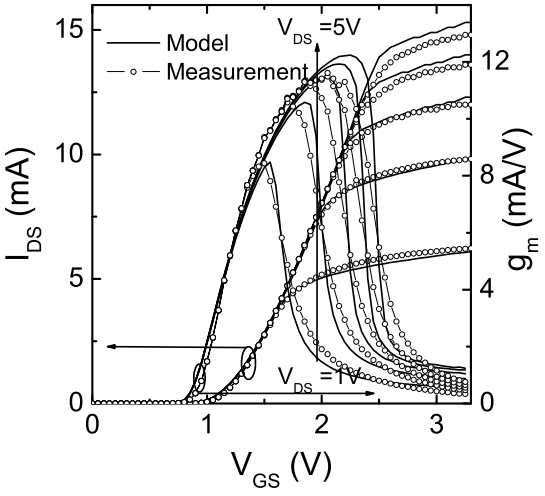
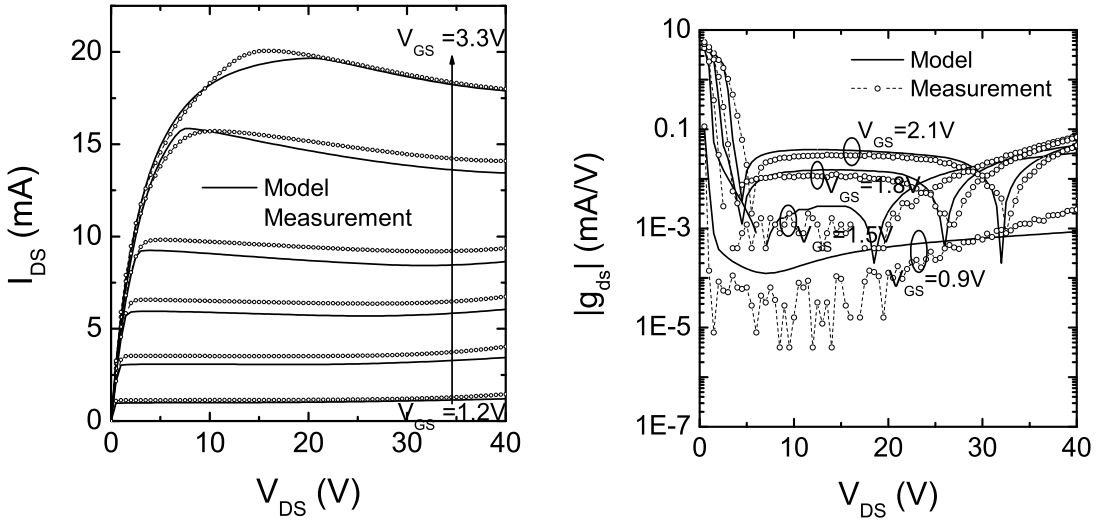
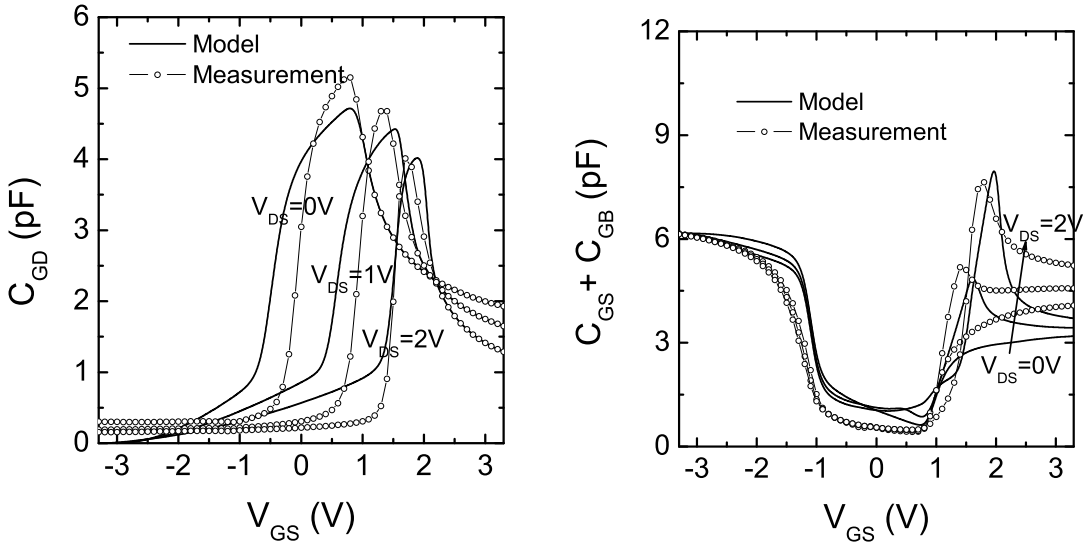


Figure 3.11: Transfer characteristics at medium drain bias for W=40μm, L=0.6μm and N_F=2 at T=30°C: I_{DS} and g_m-V_{GS} for V_{DS}= 1V-5V in steps of 1V for VDMOS transistor.



(a) (b)

Figure 3.12: Output characteristics of VDMOS transistor for W=40μm, L=0.6μm and N_F=2 at T=30°C (a) I_{DS} vs. V_{DS} for V_{GS} =1.2,1.5,1.8,2.1,2.7 and,3.3V. Note self-heating effect (decrease in I_{DS} with increase in V_{DS}) is correctly simulated. The discrepancy in the curves can be explained by the simultaneous optimization of drift resistance, self-heating effect, impact ionization effect and velocity saturation in MOSFET at high V_{DS}. (b) $|g_{ds}|$ vs. V_{DS}. Note peaks in output-conductances are correctly matched. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect.



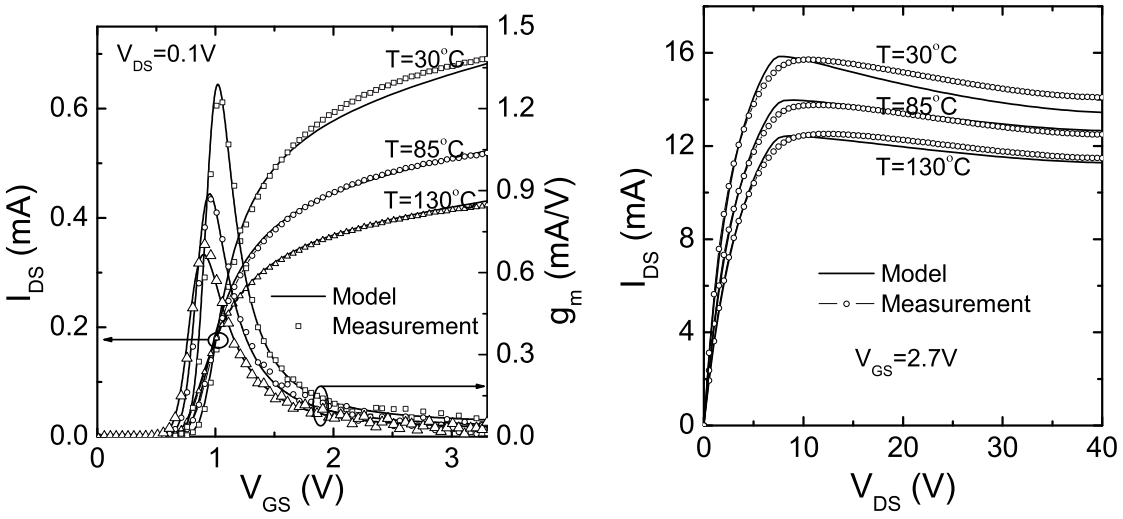
(a) (b)

Figure 3.13: (a) C_{GD} vs. V_{GS} and, (b) C_{GS}+C_{GB} vs. V_{GS} of VDMOS transistor for V_{DS}=0, 1V, and 2V. The sharp decrease in C_{GD} at higher V_{GS} is heavily affected by drift region. The discrepancy in the curves is due to assumption of constant doping in the channel and simplified drift charge evaluation. The accuracy on capacitances can be improved by modeling the lateral non-uniform doping present in the intrinsic MOS channel [20, 26, 27, 28].

channel of high voltage devices [26, 27, 28]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

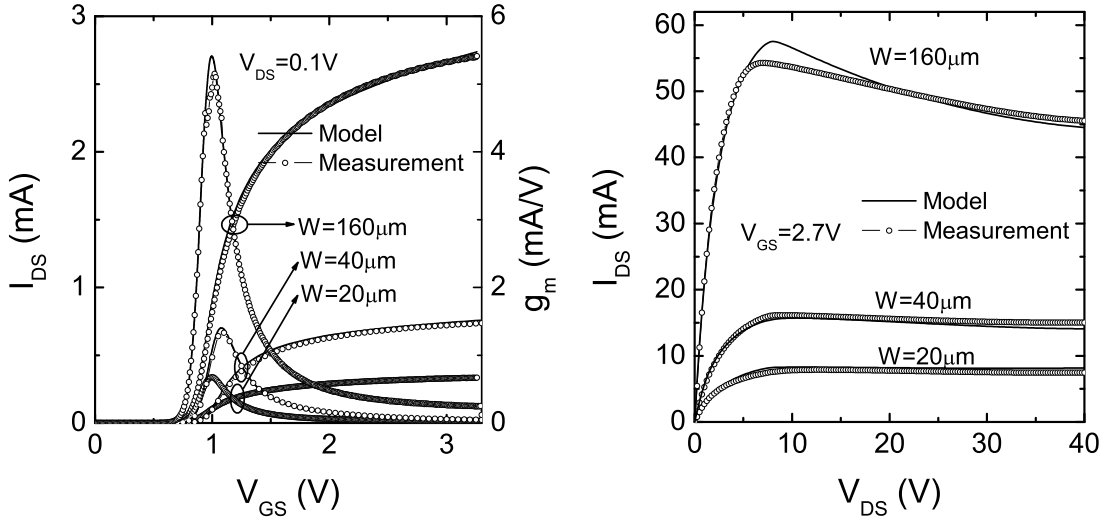
Model Scalability: An important characteristic of any model is the scalability with physical and electrical parameters. Fig. 3.14 (a) shows the I_{DS} and $g_m - V_{GS}$ characteristics for different temperatures. It can be seen that the model correctly simulates the variation of drain current, transconductance and most importantly the threshold voltage shift with temperature. An important observation is that ZTC (Zero-Temperature-Coefficient) point [29, 30, 31, 32, 33] is also well modeled in Fig. 3.14 (a). Fig. 3.14 (b) shows the I_{DS}-V_{DS} curves for different temperatures, which demonstrates that the SHE is correctly modeled for entire temperature range. The scaling of the model is also tested for different device geometries. The transfer and output characteristics shown in Fig. 3.15 (a) and (b), respectively, demonstrate that the model scales well with different transistor widths. Note that the self-heating effect is more prominent for higher widths due to increased power dissipation. The variation of ON resistance (R_{ON}) with number of fingers (N_F) is modeled using k_{rd} and N_{CRIT} parameters in (3.3). Fig. 3.16 (a) shows that the R_{ON} scaling with N_F is well modeled for different widths for *drain-all-around* device. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. Fig. 3.16 (b) shows the R_{ON} scaling with N_F for *drain-on-side* device. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers. The R_{ON} scalability with temperature is shown in Fig. 3.17 for different transistor widths. It can be seen that the increase

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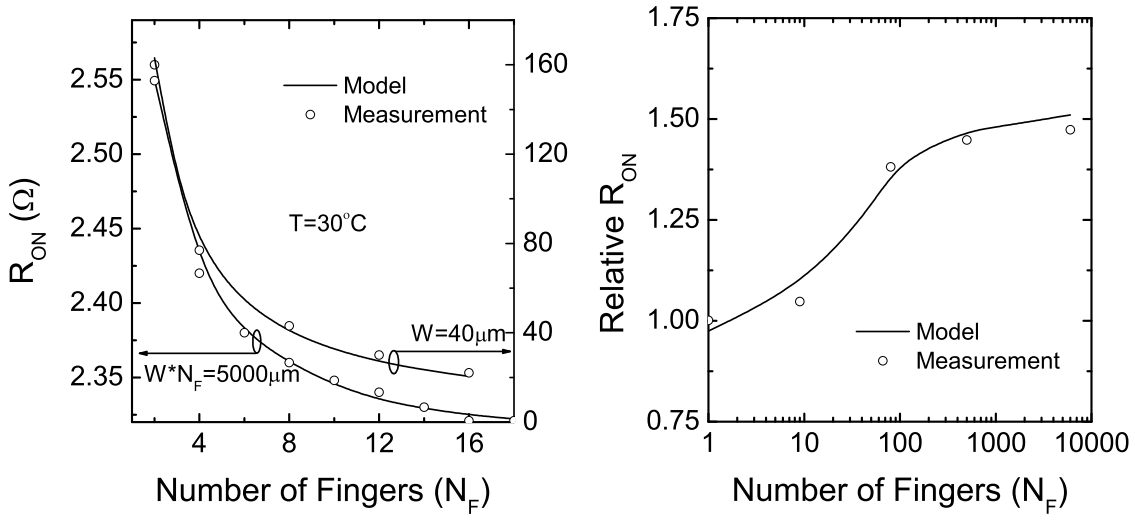
(a) (b)

Figure 3.14: Demonstration of temperature scaling of VDMOS transistor for W=40μm, L=0.6μm and N_F=2: (a) I_{DS}-V_{GS} and g_m-V_{GS} at T=30°C, 85°C and, 130°C. Note, the change in threshold voltage with temperature and peak in transconductance are correctly modeled. The ZTC-point [29, 30] is also well simulated. (b) I_{DS}-V_{DS} at T=30°C, 85°C and, 130°C. Note self-heating effect is very well modeled at different temperatures. The decrease in slope in the linear region is caused by the increase in drift resistance with temperature.



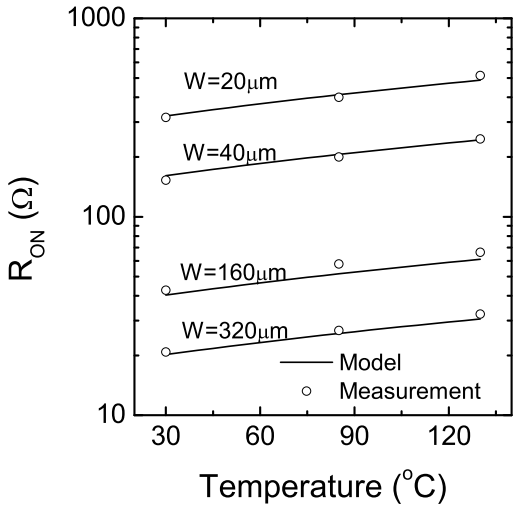
(a) (b)

Figure 3.15: Demonstration of width Scaling of VDMOS transistor for W=20μm, 40μm, 160μm, L=0.6μm and N_F=2 at T=30°C: (a) I_{DS}-V_{GS} and g_m-V_{GS} for V_{DS}=0.1V. (b) I_{DS}-V_{DS} for V_{GS}=2.7V. The self-heating effect is more prominent for higher widths due to increased power dissipation.

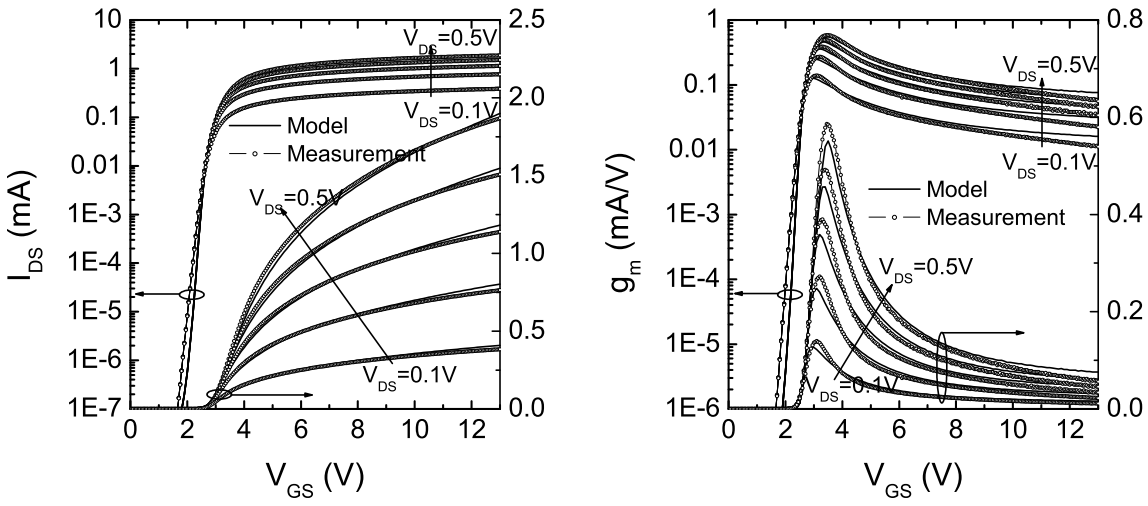


(a) (b)

Figure 3.16: (a) R_{ON} with Number of fingers (N_F) for W=40μm and $W \cdot N_F$=5000μm at V_{GS}=3.3V and V_{DS}=0.5V for *drain-all-around* VDMOS transistor at T=30°C. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. (b) Relative On-resistance $\frac{R_{ON}}{R_{ON}|_{N_F=1}}$ with Number of fingers (N_F) for *drain-on-side* VDMOS transistor. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers.



in R_{ON} with temperature is excellently modeled for different transistor widths.
Figure 3.17: R_{ON} variation with temperature for N_F=2 and W=20μm, 40μm, 160μm, 320μm for VDMOS transistor.



(a) (b)

Figure 3.18: Transfer characteristics of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1 at T=30°C): (a) I_{DS}-V_{GS} and, (b) g_m-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V .

3.5.2 Case Study 2: LDMOS Transistor

The LDMOS devices (FND40 and FND100) used for the validation of the model are obtained from I2T100 AMIS Technology. The schematic representation of the LDMOS device under study is shown in Fig. 3.4(b) while device architecture of FND40 device is shown in Fig. 3.1. Fig. 3.18 (a) and (b) show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ for V_{DS}=0.1V to 0.5V, respectively. Fig. 3.19 and 3.20 show the I_{DS} and $g_m - V_{GS}$ for V_{DS}=1V to 5V, and $I_{DS} - V_{DS}$ characteristics respectively for 40V LDMOS, which demonstrate that the model provides correct simulation of current and transconductance for different bias conditions. The gate-to-drain and gate-to-gate capacitance curves shown in Fig. 3.21 (a) and (b) respectively demonstrate that the model predicts correct trend for capacitances. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [26, 27, 28]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

Model Scalability: An important issue in any LDMOS model is the scalability with drift length for different voltage handling capability. Fig. 3.22 (a) and (b) show the transfer and output characteristics, respectively, of a 100V LDMOS transistor (FND100 device) on the same technology (as of FND40), which demonstrates that the model scales well with drift length. It should be noted that not only the self-heating effect [24] is well modeled in Fig. 3.22 (b) but also the quasi-saturation effect observed at higher gate biases. The 100V LDMOS transistor (FND100) has longer drift length, in comparison to 40V LDMOS transistor (FND40), to handle the higher drain voltages at drain terminal. The scalability of the model is also tested for R_{ON} for different widths of LDMOS device. Fig. 3.23 shows the R_{ON} vs. V_{GS} for three different widths of 40V LDMOS device.

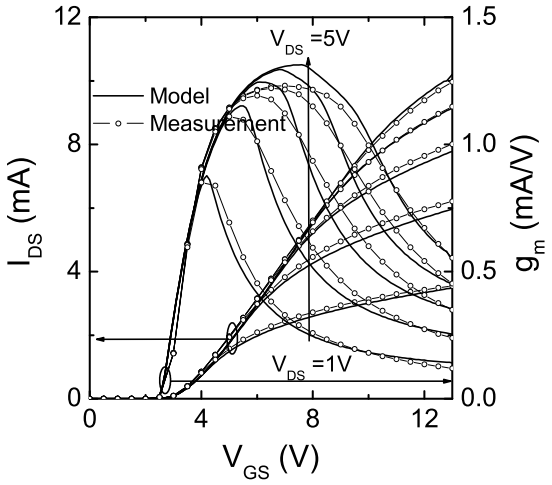


Figure 3.19: Transfer characteristics of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1): I_{DS}-V_{GS} for V_{DS}=1V-5V in steps of 1V at T=30°C.

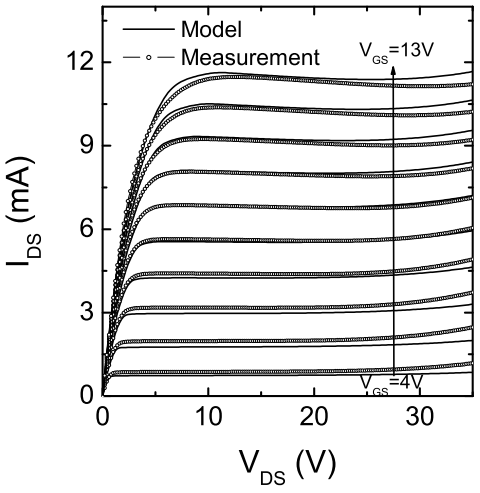
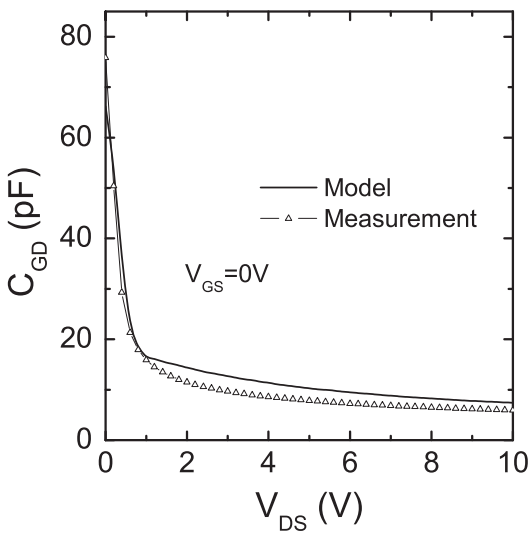
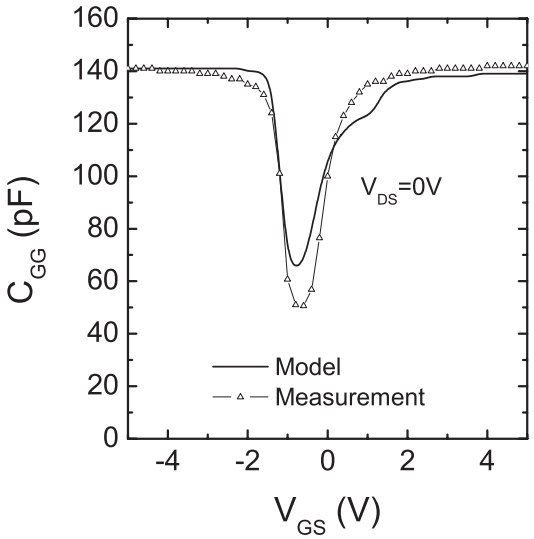


Figure 3.20: Output characteristics: I_{DS}-V_{DS} of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1) at T=30°C. Note, the self-heating and impact ionization effects are correctly simulated.

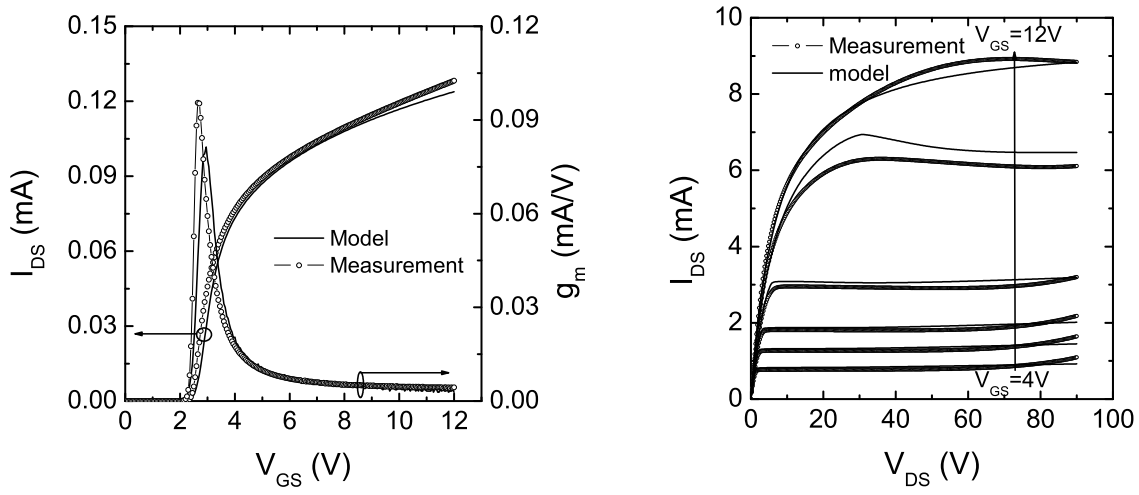


(a)



(b)

Figure 3.21: (a) Plot of C_{GD} vs. V_{DS} at V_{GS}=0V for 40V Bosch LDMOS device. (b) Plot of C_{GG} vs. V_{GS} at V_{DS}=0V for 40V Bosch LDMOS device.



(a) (b)

Figure 3.22: Drift Scaling (W=40μm, L=1.2μm and N_F=1 at T=30°C): (a) I_{DS}-V_{GS} and g_m-V_{GS} at $V_{DS} = 0.1V$, (b) I_{DS}-V_{DS} for V_{GS}=4, 4.5, 5, 6, 9 and 12V for 100V LDMOS device.

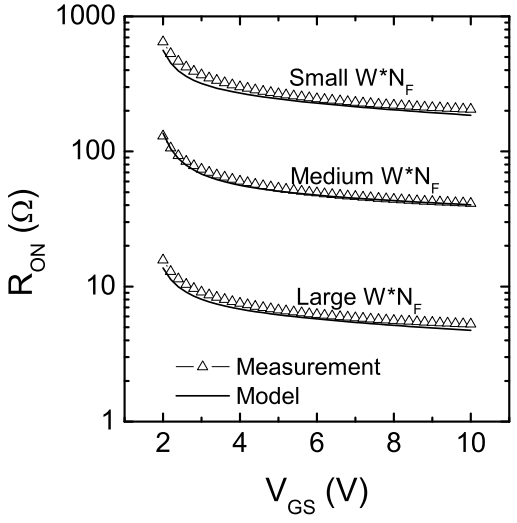


Figure 3.23: Width Scaling: R_{ON} vs. V_{GS} for three different $W * N_F$ for 40V LDMOS device at T=30°C.

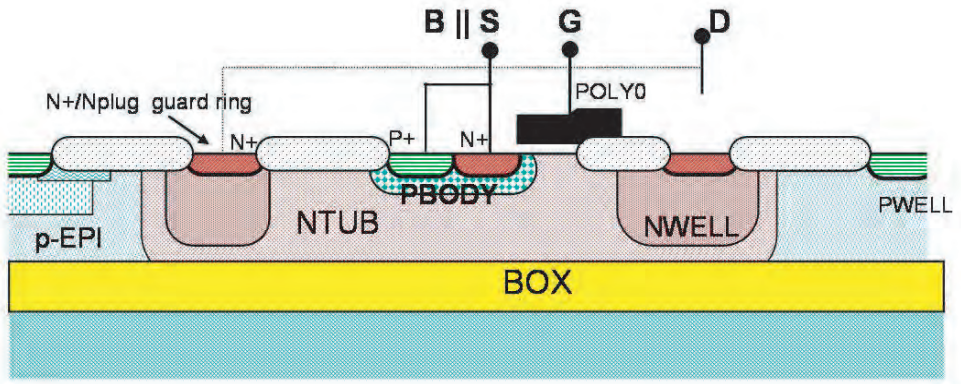
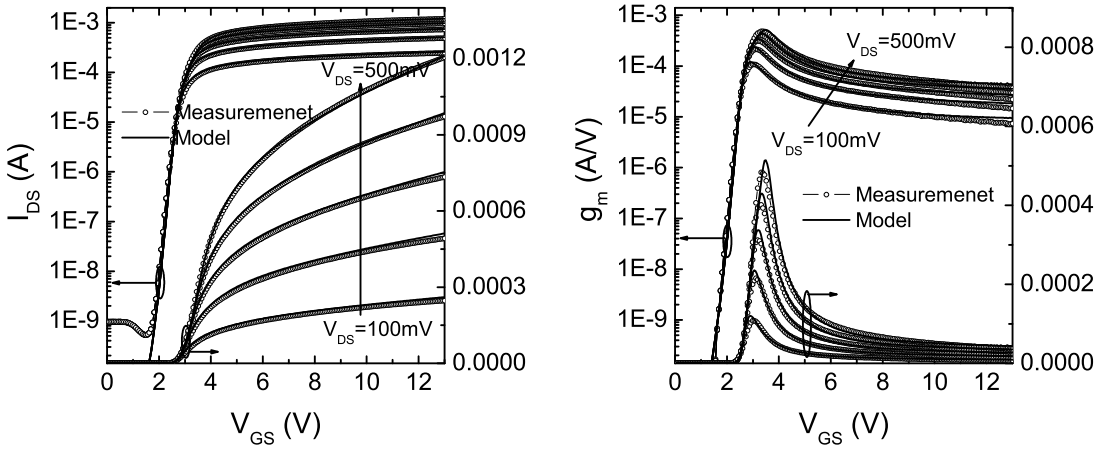


Figure 3.24: Schematic representation of 40V SOI-LDMOS transistor from I2T100 AMIS technology.



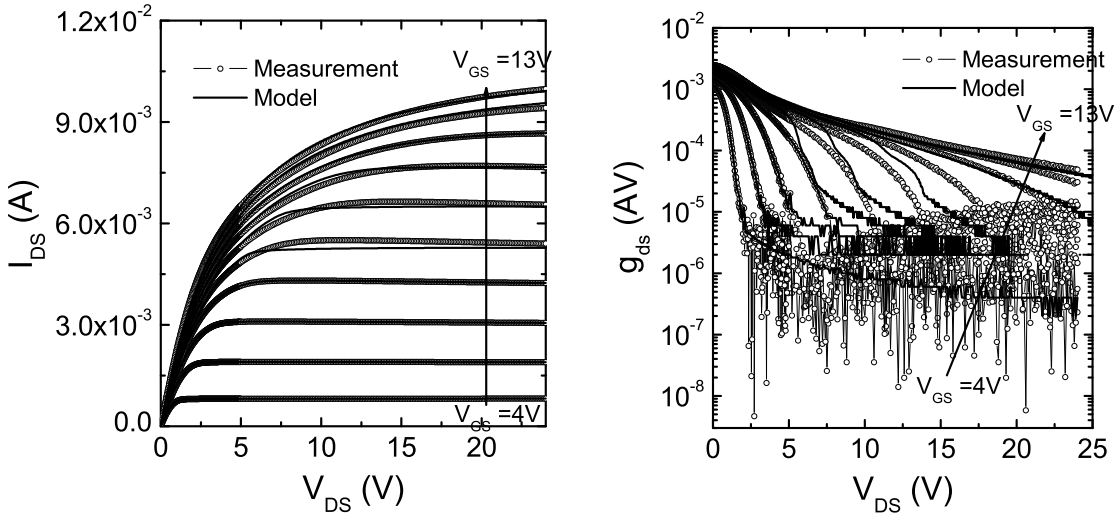
(a) (b)

Figure 3.25: Transfer characteristics of 40V SOI-LDMOS transistor from I2T100 AMIS technology (W=40μm, L=1.2μm): (a)$I_{DS} - V_{GS}$ and, (b) $g_m - V_{GS}$ for $V_{DS} = 0.1 - 0.5V$ in steps of $0.1V$. Note that, the value and position of the peaks on g_m has been modeled very well.

3.5.3 Case Study 3: SOI - LDMOS device

Fig. 3.24 shows the device architectures of SOI-LDMOS transistor [34] on AMIS technology.

The proposed model is also validated on the measured characteristics of SOI-LDMOS transistor from I2T100 AMIS technology. It should be noted that the model is same for all devices, thus showing the versatility of the model and hence called *general model*. Fig. 3.25 shows the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ characteristics for $V_{DS} = 0.1 - 0.5V$ in steps of $0.1V$. Fig. 3.26 (a) and (b) show the the output characteristics ($I_{DS} - V_{DS}$ and $g_{ds} - V_{DS}$) for $V_{GS} = 4 - 13V$. Note, significant quasi-saturation effect can be seen on the output characteristics at higher gate voltages. It can be seen that model shows good behavior across different gate and drain bias region.



(a) (b)

Figure 3.26: Output characteristics of 40V SOI-LDMOS transistor on I2T100 AMIS technology (W=40μm, L=1.2μm): (a)$I_{DS} - V_{DS}$ and, (b) $g_{ds} - V_{DS}$ for $V_{GS} = 4 - 13V$ in steps of $1V$.

Table 3.1: Main EKV Parameters

Name	Description	Units
TYPE	P-tpe/N-type	-
W	Channel Width	m
L	Channel Length	m
N_F	Number of fingers	-
COX	Oxide Capacitance	F/m^2
VT0	Long-channel Threshold Voltage	V
U0	Low Field mobility	cm^2/Vs
GAMMA	Body Effect Parameter	$\sqrt{V}$
PHI	Bulk Fermi Potential	V
E0	Mobility Reduction Coefficient	V/m
UCRIT	Longitudinal Critical Field	V/m
LAMBDA	Channel Length Modulation	-

3.6 Parameter Extraction and Model Calibration

Table 3.1, 3.2 and 3.3 show the list of main parameters used in the model. These basic parameters are used for modeling of any high voltage device at room temperature. The calibration procedure is described below and also shown in the flowchart (see Fig. 3.27). First threshold voltage and mobility is extracted using any standard extraction method [35, 36, 37, 38, 39]. Other standard EKV parameters [40] are extracted using methodology proposed in [41]. Once

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Table 3.2: Drift Parameters

Name	Description	Units
L_{DR}	Drift length	m
L_{OV}	Gate overlap in the drift region	m
ρ_{Drift}	Drift resistivity	V-m/A
VSAT	Velocity saturation parameter	V/m
α_{vsat}	”	-
θ_{Acc}	Accumulation charge effect	1/V
k_{rd}	Effect of number of fingers	-
N_{CRIT}	”	-
α_T	Thermal coefficient of drift resistance	$1/K$

Table 3.3: Self-heating and impact ionization parameters

Name	Description	Units
R_{THNOM}	Thermal resistance	Ks/J
α	Temperature coefficient of R_{THNOM}	1/K
C_{TH}	Thermal capacitance	J/K
$NEFF$	Effective doping in the drift	$V^{-\frac{4}{3}}$

we have all of these parameters, $GAMMA$ and PHI are tuned for subthreshold slope on $I_{DS} - V_{GS}$ characteristics. $E0$ is tuned on $I_{DS} - V_{GS}$ characteristics in strong inversion for mobility degradation due to vertical field. $UCRIT$ and $LAMBDA$ are tuned on $I_{DS} - V_{DS}$ characteristics for velocity saturation and channel length modulation, respectively. Drift parameters $VSAT$ and α_{vsat} are fitted in the linear region of $I_{DS} - V_{DS}$ characteristics while θ_{Acc} is used to lower the drift resistance on $I_{DS} - V_{GS}$ characteristics at high V_{GS} as described earlier. k_{rd} and N_{CRIT} parameters are fitted to model the effect of number of fingers on drift resistance.

The extraction of self-heating parameters requires dedicated measurement setup. The extraction of thermal resistance and capacitance has been discussed in detail in [4, 23, 24, 42]. The impact ionization parameter N_{EFF} is used as a fitting parameter to model the impact ionization in the drift region.

Fig. 3.28 shows the worst case errors for transfer and output characteristics and also for their derivatives using proposed model on different HV-MOS architectures. The accuracy target required by the industry for high voltage models are also included in the figure [43]. It can be seen that model fulfils all the targets of the industrial model.

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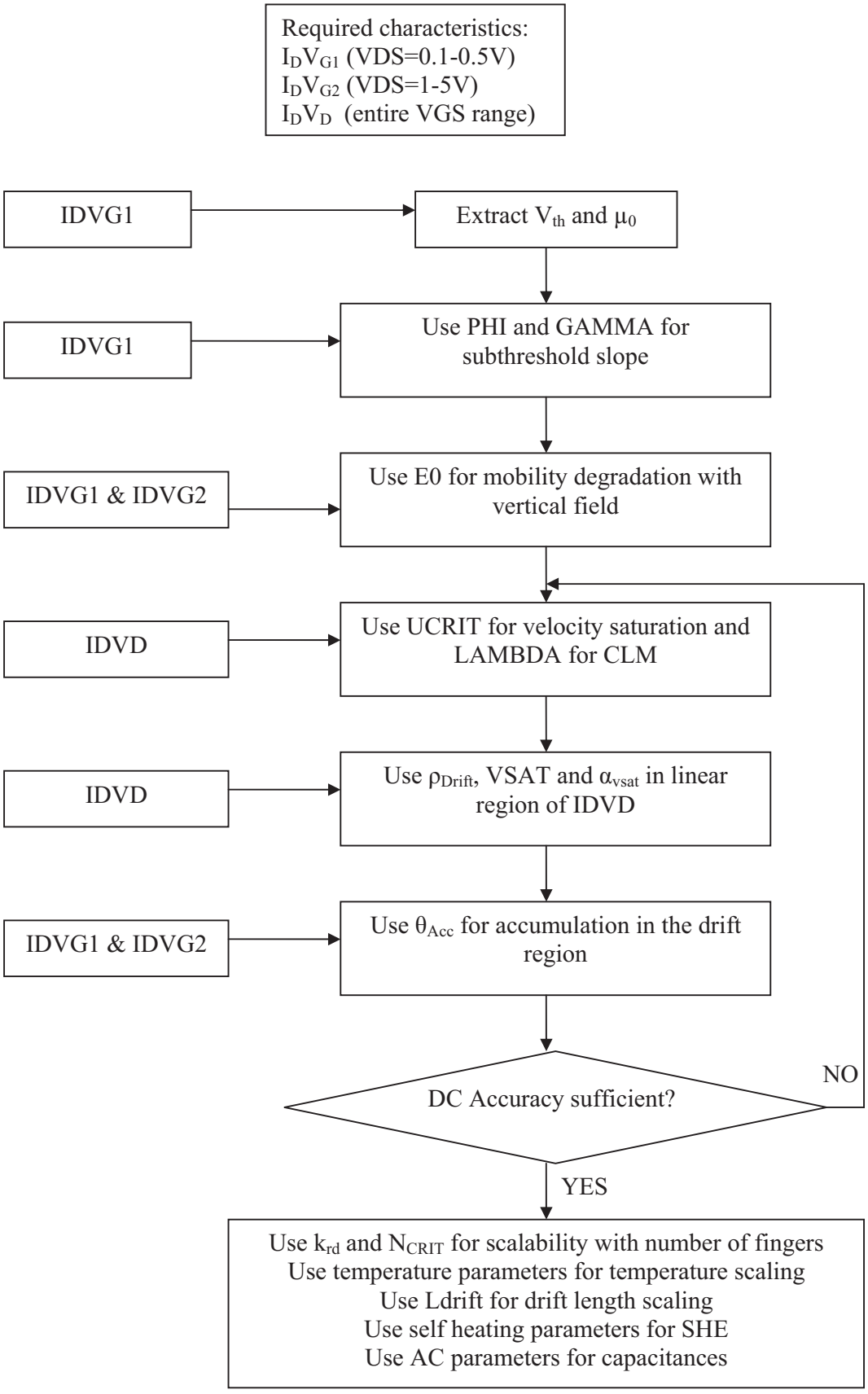


Figure 3.27: Flowchart of parameter extraction procedure.

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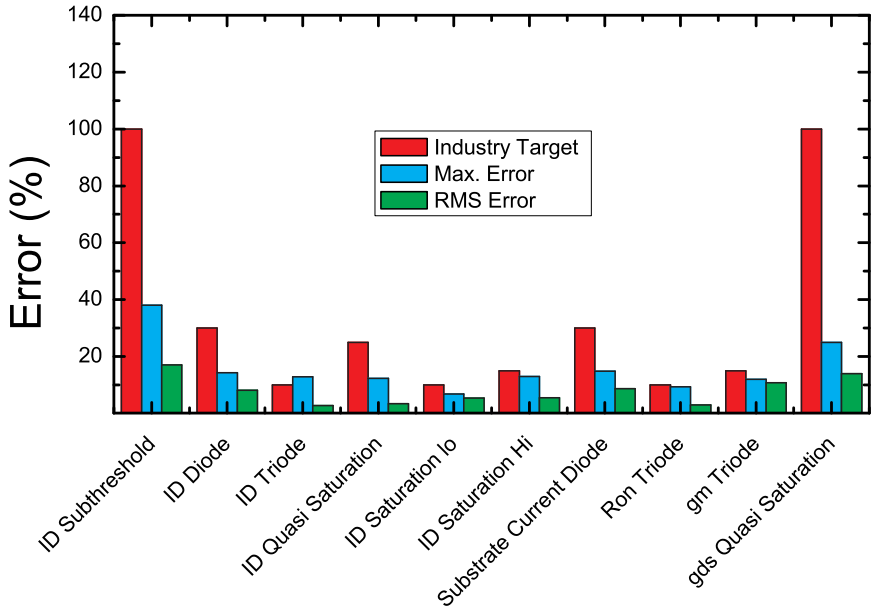


Figure 3.28: RMS and Max errors of the model.

3.7 Conclusion

A new *general* High Voltage MOSFET model based on the EKV model as a core and new bias dependent drift resistance is presented. The drift resistance includes major effects originating from the drift region like quasi-saturation and accumulation in the gate overlapped drift region. The impact ionization effect was modeled for both the regions i.e. the intrinsic MOSFET and the drift region, where impact ionization in the intrinsic MOSFET dominates at low to medium gate voltages while impact ionization at higher gate voltages is dominated by the drift region for higher drain voltages. The self heating effect was incorporated using sub-circuit approach. The thermal resistance and capacitance are dynamically varying with temperature inside the device giving better results compared to constant thermal resistance.

The model performance was demonstrated for three industrial devices: VDMOS, bulk-LDMOS and SOI-LDMOS. The model correctly reproduces the special effects of high voltage devices like the quasi-saturation and self-heating effect, and is highly scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. For the first time, the *scalability with drift length* in LDMOS transistor was demonstrated using this model. The model shows good results for entire DC bias range and good behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics) and Cadence‘s Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use.

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Chapter 4

Compact Modeling of Lateral Non-uniform doping

Here the detailed analysis and modeling of lateral non-uniform doping present in the intrinsic MOS channel of high voltage MOSFETs e.g. VDMOS and LDMOS is presented. It is shown that the conventional long channel MOSFET models using uniform lateral doping can never correctly model the capacitance behavior of these devices. A new analytical compact model for lateral non-uniformly doped MOSFET is developed [1, 2, 3, 4]. The intrinsic non-uniformly doped MOS model is first validated on the numerical simulation and then on measured characteristics of VDMOS and LDMOS transistors including drift region. The model shows good results in DC and, most importantly in AC regime, especially in simulating the peaks on C_{GD}, C_{GS} and C_{GG} capacitances. This new model improves the accuracy of high voltage MOS models, especially output characteristics and during transient response (i.e. amplitude and position of peaks as well as slope of capacitances).

4.1 Introduction

The lateral non-uniformly doped MOSFET or Lateral Asymmetric MOSFET (LAMOS), which has longitudinal doping variation in the channel, is the building block of many categories of high-voltage MOSFETs e.g. LDMOS and VDMOS transistors [5, 6, 7, 8, 9, 10]. The lateral asymmetric channel devices have also caught attention in deep sub-micron devices for higher performance in analog, RF and mixed signal design [11, 12, 13, 14]. In fact, lateral non-uniform doping is inherent in halo-doped nano-MOSFETs [15, 16, 17]. Recently physical modeling of LAMOS has received considerable attention as the Compact Modeling Council (CMC) [18] has started efforts to get a compact physical model for LDMOS as an industry standard model. Very few models have been reported [6, 7] in the literature for modeling of lateral non-uniform doping while majority of the models published [5, 6, 7, 19, 20, 21, 22, 23, 24, 25] use constant doping in the channel. Accurate modeling of the capacitances in high-voltage devices is a prerequisite for integrated RF design of, for instance, switched-mode power supplies and power amplifiers.

Modeling of LAMOS has been a great challenge due to the lateral doping gradient in the channel region. The main difficulty in the modeling of LAMOS arises as expressions become

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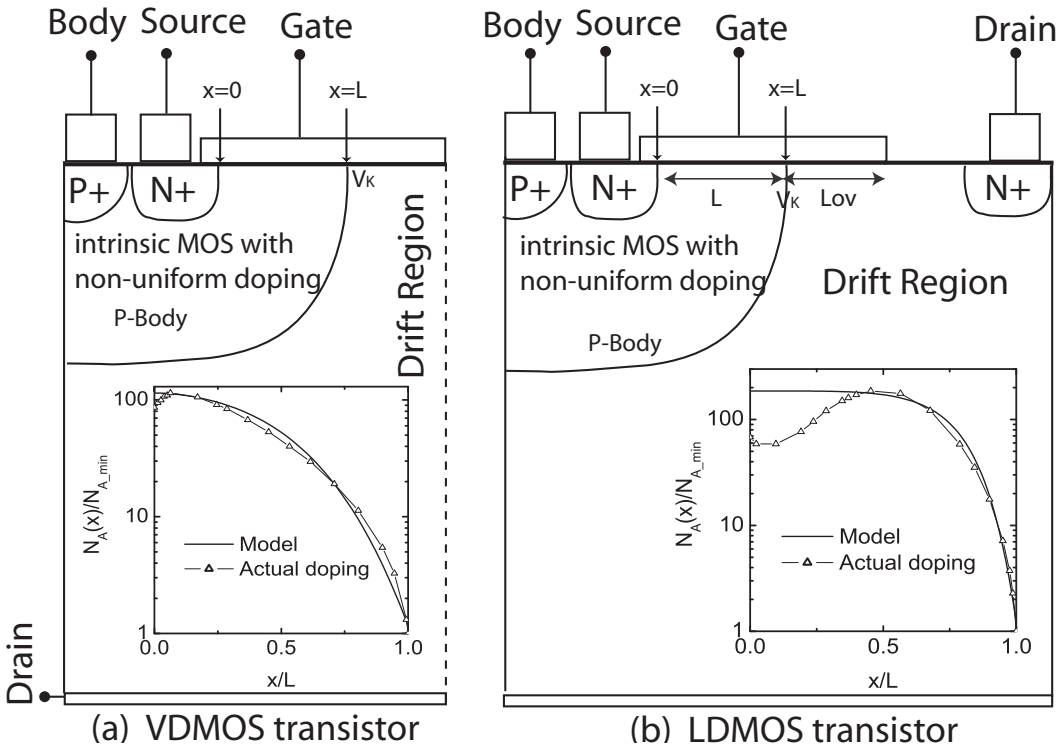


Figure 4.1: Schematic representation of VDMOS and LDMOS transistors. Note that the intrinsic MOS has a lateral doping gradient. The channel extends from x=0 to L. L_{ov} is the gate overlap in the drift region. Figures in the inset show the doping profiles normalized by $min\{N_A(x = L)\}$ in the AMI Semiconductor devices. Solid line in the doping profile represents the function $\left\{N_A(x) = N_S.erfc\left[k_n(\frac{x}{L})^a\right]\right\}$ used to model the doping in the channel. N_S is taken as highest doping in the channel, which is generally near source end of the channel. k_n and a are the parameters.

non-integrable/non-implicit due to the lateral asymmetry in the channel. In this chapter, a new compact model for LAMOS is derived in detail [1, 2, 3, 4]. Furthermore, the intrinsic LAMOS model is validated on the numerical device simulation of LAMOS structure, while the LAMOS along with the drift region is validated on the measured characteristics of LDMOS and VDMOS transistors with laterally diffused channel doping profile. The source and body are tied to avoid parasitic bipolar transistor for all measurements.

4.2 Modeling of Lateral Non-uniform doping

Fig. 4.1 shows the schematic representation of VDMOS (half of the device) and LDMOS transistors. In the inset of both figures, the lateral non-uniform doping profile of the respective devices along the channel is also shown. The doping level at the source side of the channel is highest and decreases towards the drain in the channel region. The lateral doping gradient is approximated by the complementary error function $N_A(x) = N_S.erfc[k_n(\xi)^a]$, where $\xi = \frac{x}{L}$ is the normalized position along the channel, k_n is a parameter representing the doping gradient and a is a fitting parameter. Higher k_n means sharp decrease in the doping level from source to

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drain and vice-versa.

The well-known drift-diffusion current expression is given by

$$I_{DS} = I_{Drift} + I_{Diff} = \mu W \left(-Q_i \frac{d\Psi_S}{dx} + U_T \frac{dQ_i}{dx} \right) \tag{4.1}$$

where, μ, W, Q_i, and Ψ_S are the mobility, width, inversion charge, and surface potential, respectively, at any position x in the channel. The thermal voltage has been denoted by U_T. The inversion charge linearization relation between Q_i and Ψ_S using EKV formalism [26, 27] can be expressed as

$$-Q_i = n_q C_{ox} (\Psi_P - \Psi_S) \tag{4.2}$$

where slope factor n_q and pinch-off surface potential Ψ_P are defined as [26, 27]

$$n_q = 1 + \frac{\Gamma}{\sqrt{\Psi}_P + \sqrt{\Psi_P + U_T(q_s + q_d)}} \tag{4.3}$$

$$V_G - V_{FB} = \Psi_P + sign(\Psi_P)\Gamma \sqrt{U_T e^{-\frac{\Psi_P}{U_T}} + \Psi_P - U_T} \tag{4.4}$$

where C_{ox} and Γ are the oxide capacitance per unit area and body effect coefficient, respectively. The q_d and q_s are the normalized charge densities at drain and source, respectively, described later in this section. Note that the Ψ_P is a function of x now, while in a conventional long channel MOSFET, it is independent of x. The approximate solution of the transcendental equation of Ψ_P or ψ_p is given in Appendix A.

The first order mobility model can be derived as follows [28]

$$\mu = \frac{v_{drift}}{E_x} = \frac{\mu_v}{1 + \left| \frac{E_x}{E_c} \right|} = \frac{\mu_v}{1 + \left| \frac{d\Psi_S / dx}{v_{sat} / \mu_v} \right|} \tag{4.5}$$

where

$$\mu_v = \frac{v_{sat}}{E_c} = \left[\frac{1 + \left(\frac{E_{ref}}{E_{ph}} \right)^{\alpha_{ph}} + \left(\frac{E_{ref}}{E_{sr}} \right)^{\alpha_{sr}}}{1 + \left(\frac{E_{eff}}{E_{ph}} \right)^{\alpha_{ph}} + \left(\frac{E_{eff}}{E_{sr}} \right)^{\alpha_{sr}}} \right] \mu_0 = \rho_v \mu_0 \tag{4.6}$$

where v_{drift}, v_{sat}, E_x and E_c are the drift velocity, saturation velocity, longitudinal electric field and critical electric field, respectively. The mobility μ_v is a function of the vertical electric field only, through ρ_v, where ρ_v is a function of bias condition and doping level. To simplify the expressions into compact form, we will assume that ρ_v is independent of doping variation in the channel and only a function of vertical electrical field. Without loss of generality, the low field mobility μ_0 is considered constant along the channel and defined at $E_{eff} = E_{ref}$, where E_{ref} is the reference electric field. E_{ph}, α_{ph} are electric field and exponent, respectively, related to phonon scattering and E_{sr}, α_{sr} are the electric field and exponent, respectively, related to surface roughness [28]. From (5.3), (5.7) and (4.6), I_{DS} can be written as

$$I_{DS} = \frac{\mu_v}{1 + \frac{\mu_v}{v_{sat}} \left| \frac{d\Psi_s}{dx} \right|} W \left(-Q_i \frac{d\Psi_s}{dx} + U_T \frac{dQ_i}{dx} \right) \tag{4.7}$$

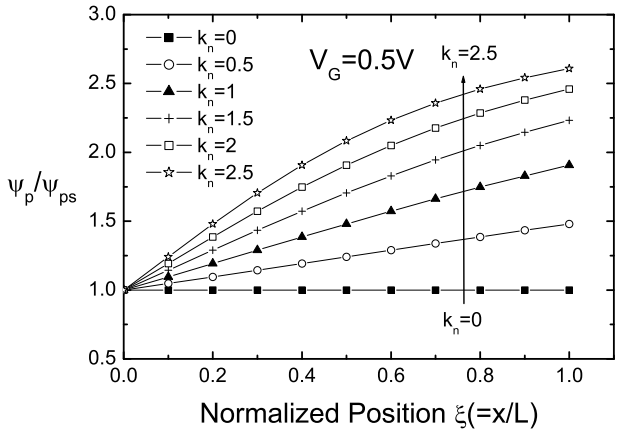


Figure 4.2: Plot of pinch off potential normalized to pinch off potential at source end ($\frac{\psi_p}{\psi_{ps}}$) vs. normalized position ($\xi = x/L$) along the channel for different values of doping gradients. The doping at the source (N_S) is taken as $5 \cdot 10^{16} cm^{-3}$. Here $k_n = 0$ refers to the case of conventional MOSFET. Note that ψ_p is almost linear along the channel for different values of k_n.

Using (4.2) and (4.6) for $\frac{d\Psi_s}{dx} > 0$, (4.7) can be rewritten as

$$\frac{dq}{d\xi} = -\frac{i_{ds} + \rho_v \left(i_{ds} \frac{\delta_{sat}}{2} - q \right) \frac{d\Psi_p}{d\xi}}{\rho_v \left(1 + 2q - \delta_{sat} i_{ds} \right)} \tag{4.8}$$

where variables and constants are normalized from EKV formalism [26, 27] as follows

$$q = \frac{-Q_i}{2 n_q C_{ox} U_T}, i_{ds} = \frac{I_{DS}}{2 n_q \frac{W}{L} \mu_0 C_{ox} U_T^2}, \delta_{sat} = \frac{2\mu_0 U_T}{v_{sat} L}, \psi_p = \frac{\Psi_P}{U_T}. \tag{4.9}$$

Notice that q, i_{ds}, δ_{sat}, ψ_p and ρ_v are all dimensionless quantities. The relation between normalized inversion charge density q and normalized current i_{ds} given by (4.8) cannot be solved analytically as it is a nonlinear ODE of q, where ψ_p [26, 27] is a function of normalized position ξ in the channel.

Following approximations are made to solve this differential equation (4.8).

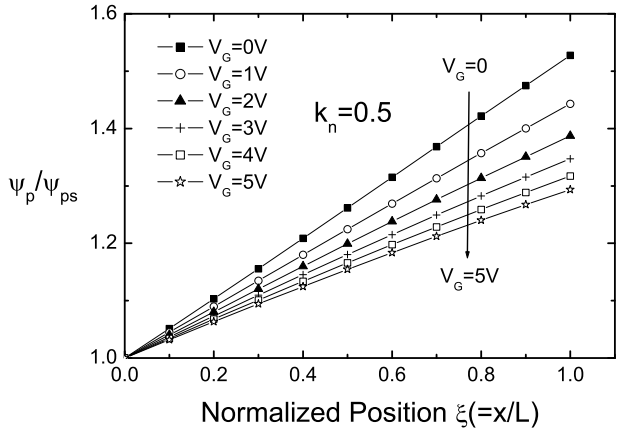
a) The slope factor n_q is independent of position ξ. Although n_q is a function of doping through Ψ_P and Γ in (5.5), dependence of n_q on ξ is weak.

b) $\frac{d\psi_p}{d\xi}$ is assumed to be independent of ξ (i.e. $\frac{d\psi_p}{d\xi} = \Delta\psi_p$ is constant with ξ). In other words, ψ_p varies linearly with ξ. The above assumption holds very good for the entire practical range of k_n(=0-2.5) as shown in Fig. 4.2 and 4.3.

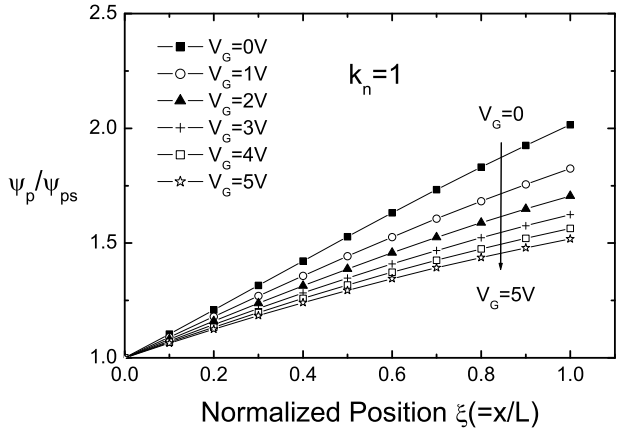
Using above approximations, (4.8) is integrated along the channel from $\xi = 0$ to $\xi = 1$, to obtain the drain to source current i_{ds} and total normalized inversion charge density q_c in the channel as

$$\Delta\psi_p = 2(q_d - q_s) + \left(1 + \frac{2 i_{ds}}{\rho_v \Delta\psi_p} \right) \cdot \left[\ln \left(\frac{q_d - i_{ds} \left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2} \right)}{q_s - i_{ds} \left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2} \right)} \right) \right] \tag{4.10}$$

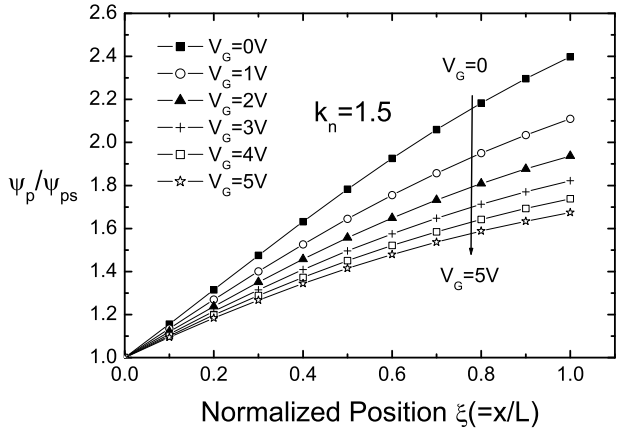
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(a)



(b)



(c)

Figure 4.3: Plot of pinch off potential normalized to pinch off potential at source end ($\frac{\psi_p}{\psi_{ps}}$) vs. normalized position ($\xi = x/L$) along the channel for V_G=0 to 5V (covering weak-moderate-strong inversion) in steps of 1V for (a) k_n=0.5, (b) k_n=1, (a) k_n=1.5. The doping at the source (N_S) is taken as $5 \cdot 10^{16} cm^{-3}$. It demonstrate that the approximation $\frac{d\psi_p}{d\xi} = \Delta\psi_p$ is constant with ξ holds true for different values of doping gradients and gate biases.

$$q_c = \int_0^1 q d\xi = \frac{1}{\Delta\psi_p}\left[\left(q_d^2 - q_s^2\right) + \left(q_d - q_s\right)\left(1 - i_{ds}\delta_{sat}\right)\right] + \left[i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)\right]. \quad (4.11)$$

The normalized charge densities at drain (q_d) and source (q_s) are defined as [26]

$$2q_d + \ln(q_d) = v_p - v_d, \quad (4.12)$$

$$2q_s + \ln(q_s) = v_p - v_s. \quad (4.13)$$

where $v_d = \frac{V_D}{U_T}$, $v_s = \frac{V_S}{U_T}$ are the normalized bias voltages and v_p is the normalized pinch off voltage and defined as [26]

$$v_p = \psi_p - \psi_0, \quad (4.14)$$

where ψ_0 is the inversion surface potential and defined as [26]

$$\psi_0 = 2\phi_f + mU_T \quad (4.15)$$

Where m is few U_T or more accurate value can be obtained from [26]. The normalized bulk Fermi potential $\phi_f = ln\left(\frac{N_A}{n_i}\right)$ is assumed to be constant along the channel and taken as the value at source end i.e. $\phi_f = ln\left(\frac{N_S}{n_i}\right)$. The approximate solutions of transcendental equations of q_s or q_d is given in Appendix A.

It should be noted that the expression for current (4.10) is not an explicit function. To derive an explicit expression for current, we use interpolation between asymptotic behavior in linear and saturation region on $i_{ds} - v_{ds}$ characteristics. Using an interpolation function, i_{ds} can be written as

$$i_{ds} = g_{on}\frac{v_d - v_s}{\left[1 + \left(\frac{v_d - v_s}{v_{dsat}}\right)^n\right]^{\frac{1}{n}}} \quad (4.16)$$

where v_{dsat} is the normalized saturation voltage and can be expressed as,

$$v_{dsat} = \frac{i_{dsat}}{g_{on}}. \quad (4.17)$$

Additionally, from (4.10), the small signal conductance at $v_{ds} = 0$ is found to be,

$$g_{on} = \left.\frac{\partial i_{ds}}{\partial v_d}\right|_{v_{ds}=0.} = \left.\frac{\rho_v \Delta\psi_p q_s}{\left(1 + \frac{\delta_{sat}\rho_v\Delta\psi_p}{2}\right)\left(1 - \frac{q_s}{q_d}\right) - 2q_s ln\left(\frac{q_s}{q_d}\right)}\right|_{v_{ds}=0} \quad (4.18)$$

It should be noted that the interpolation function used in (4.16) is an infinitely differentiable mathematical smoothing function and n is an empirical fitting parameter, which can take any positive number. The larger the value of n, the more abrupt is the transition from linear to saturation on $i_{ds} - v_{ds}$ characteristics and vice-versa. The normalized saturation current i_{dsat} is evaluated iteratively from (4.10), by knowing the normalized inversion charge density at drain end of the channel in saturation ($q_{dsat} = \frac{\delta_{sat} i_{dsat}}{2}$). It is observed that within 2-3 iterations, accuracy on i_{dsat} is better than 0.01% compared with numerical solution of (4.10). Once we

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know i_{ds} from (4.16), the total normalized inversion charge density q_c can be evaluated from (5.17).

The gate charge density at any position in the channel can be expressed as

$$Q'_g = C_{ox}\left(V_G - V_{FB} - \Psi_S\right). \tag{4.19}$$

The normalization of (4.19) and using (4.2) gives

$$q'_g = \frac{Q'_g}{C_{ox}U_T} = \left(v_g - v_{fb} - \psi_p + 2q\right) \tag{4.20}$$

where $v_g = \frac{V_G}{U_T}$, $v_{fb} = \frac{V_{FB}}{U_T}$ are the normalized gate and flat-band voltage, respectively. Integrating (4.20) from source to drain provides the total gate charge density in the channel as

$$q_g = v_g - \overline{v_{fb}} - \overline{\psi_p} + 2q_c \tag{4.21}$$

where $\overline{v_{fb}} = \frac{v_{fbs}+v_{fbd}}{2}$ and $\overline{\psi_p} = \frac{\psi_{ps}+\psi_{pd}}{2}$ are the arithmetic mean of the flat band voltage [29] and normalized pinch off potential, respectively, at source and drain. The final expressions for drain to source current, total inversion charge, total bulk charge and total gate charge in the LAMOS can be written as,

$$I_D = \left(2n_q\frac{W}{L}\mu_0 C_{ox}U_T^2\right) i_{ds} \tag{4.22}$$

$$Q_I = -\left(2n_q WLC_{ox}U_T\right) q_c \tag{4.23}$$

$$Q_B = -WLC_{ox}U_T\left[v_g - \overline{v_{fb}} - \overline{\psi_p} - 2\left(n_q - 1\right) q_c\right] \tag{4.24}$$

$$Q_G = WLC_{ox}U_T\left(V_{GS} - \overline{v_{fb}} - \overline{\psi_p} + 2q_c\right) \tag{4.25}$$

Even though we have obtained the expressions for Q_G and Q_B (which gives all capacitances related to gate and body node), the question which remains open is how to get the drain charge (Q_D) and source charge (Q_S), which in turn can be used for the evaluation of trans-capacitances (e.g. C_{DG}, C_{SG} etc.). Recently, it has been shown that the large signal drain and source charges do not exist for LAMOS [30, 31] and the famous Ward-Dutton charge partitioning approach [32] is not valid for LAMOS. The trans-capacitance evaluation using small signal analysis has been explained in [30, 31]. We have recently proposed a new partitioning scheme for LAMOS [33], which can be used for the evaluation of trans-capacitances. This novel development will be explained in Chapter 6.

4.3 DISCUSSION and RESULTS

4.3.1 Validation of the LAMOS model on numerical device simulation

The proposed compact model for the LAMOS device is validated on numerical device simulations performed with ISE-DESSIS. The doping level at the source end of the channel is kept at $5 \cdot 10^{16} cm^{-3}$ and value of k_n is chosen as 1.5, generally used in the 50V VDMOS devices in the industry [34, 35]. Fig. 4.4 and fig. 4.5 show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ characteristic for V_{DS}=50mV. The model exhibits good trend for the subthreshold slope and values at higher

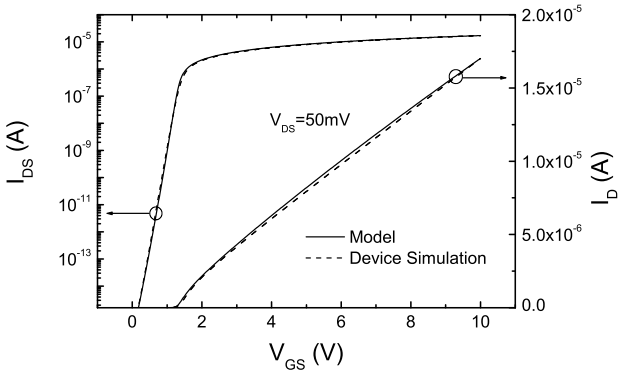


Figure 4.4: Drain current I_{DS} vs. gate voltage V_{GS} for V_{DS}=50mV on linear and logarithmic scale ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

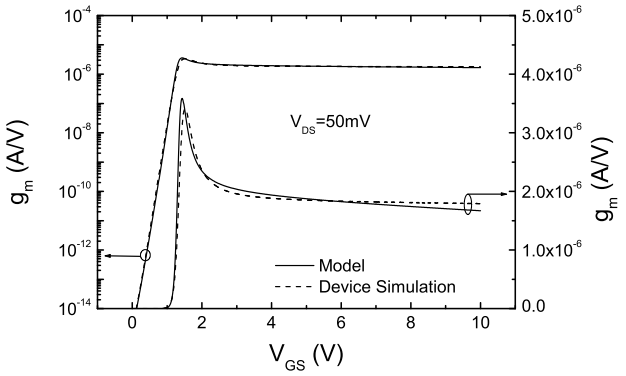


Figure 4.5: Transconductance g_m vs. gate voltage V_{GS} for V_{DS}=50mV ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

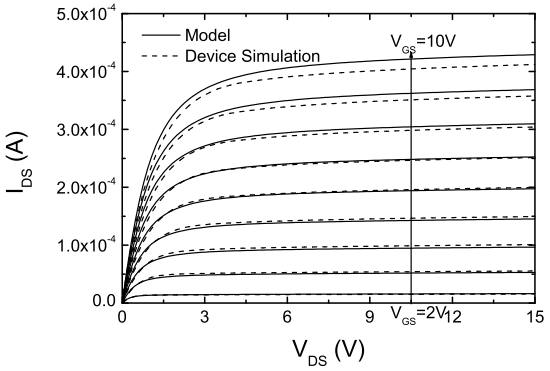


Figure 4.6: Output characteristics: drain current I_{DS} vs. drain voltage V_{DS} for V_{GS}=2-10V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). The prolonged linear region at higher gate voltage arises due to lateral nonuniform doping.

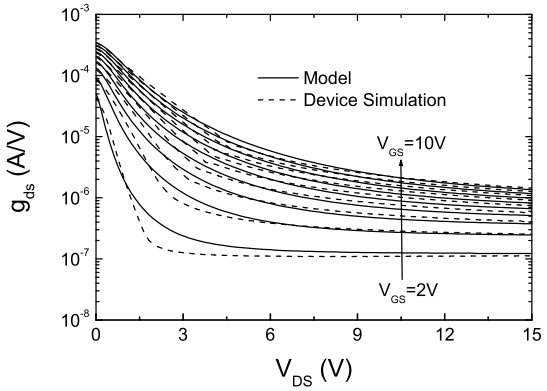


Figure 4.7: Output conductance g_{ds} vs. drain voltage V_{DS} for V_{GS}=2-10V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

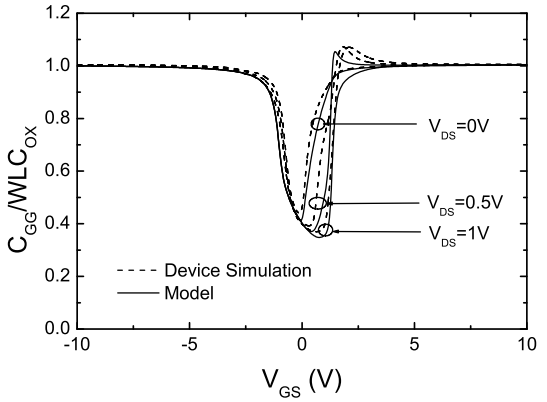


Figure 4.8: Gate-to-Gate capacitance C_{GG} vs. gate voltage V_{GS} for V_{DS}=0, 0.5 and 1V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). Notice that peak in C_{GG} occurs, when V_{GS} is around threshold voltage. The peak in C_{GG} at low drain bias is given by lateral nonuniform doping [30].

gate bias for current and transconductance. Fig. 4.6 and 4.7 show the output characteristics ($I_{DS} - V_{DS}$) and output conductance ($g_{ds} - V_{DS}$), respectively, for V_{GS}=2-10V. It can be seen that the current as well as its slope is well simulated by the model. As mentioned in chapter 2, the prolonged linear region on output characteristics is due to lateral asymmetry in the channel. Fig. 4.8 shows the gate-to-gate capacitance C_{GG} at V_{DS}=0, 0.5 and 1V. It is interesting to note that C_{GG} has peaks at V_{DS}=0.5 and 1V, which was also shown in [30] for nonzero V_{DS}. These peaks can be explained by the fact that the drain end of the channel is in depletion while the source end of the channel is in weak/moderate inversion and source end suddenly it enters into strong inversion with slight increase in V_{GS}. Note that the peak vanishes as V_{GS} increases significantly above threshold voltage as now charge is being supplied from source. Thus, the peak in C_{GG} occurs for small nonzero values of V_{DS}, when V_{GS} is around threshold voltage (source end entering into strong inversion from weak/moderate inversion). Fig. 4.9 shows the gate-to-drain (C_{GD}) and gate-to-source (C_{GS}) capacitance at V_{DS}=0. The rising slope and value of the

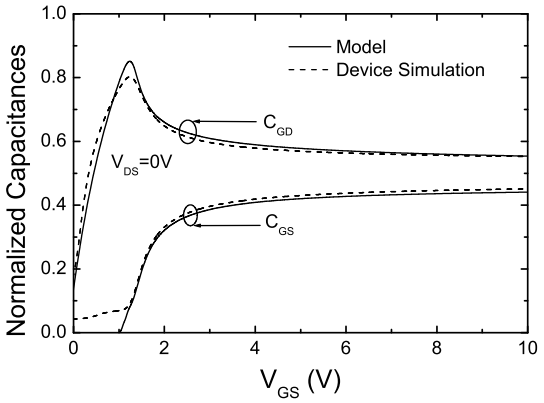


Figure 4.9: Gate-to-Drain C_{GD} and Gate-to-Source C_{GS} capacitance vs. gate voltage V_{GS} for V_{DS}=0 ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). The peak in C_{GD} is given by lateral asymmetry in the LAMOS channel [1, 36, 37, 2].

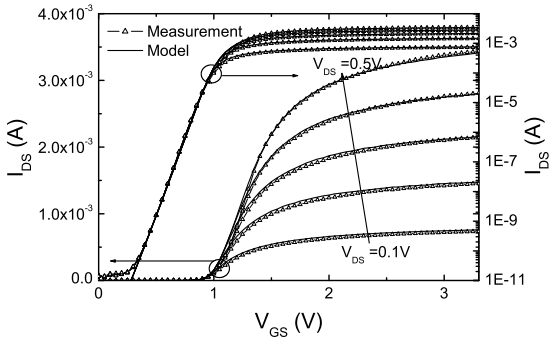
peak in C_{GD} is given by the lateral asymmetry in the LAMOS channel. The discrepancy in the capacitance behavior is due to the charge sheet approximation and the various approximations taken in the model development.

4.3.2 Model validation on the measured data of VDMOS and LDMOS

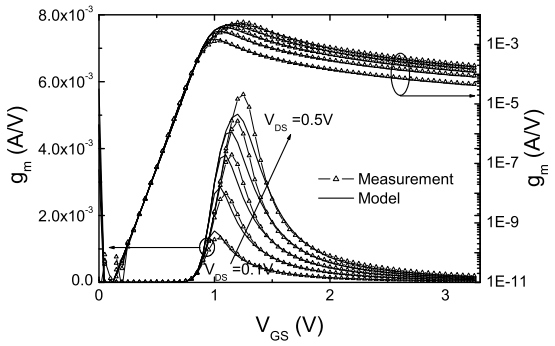
The proposed LAMOS model is also validated on the measured characteristics of 50V VDMOS and 40V LDMOS transistors obtained from AMI Semiconductor. Both devices have lateral non-uniform doping in the channel as shown in the inset of Fig. 4.1. The drift model is conveniently chosen from chapter 2 [35, 38]. The Self-heating effect is modeled in the similar way as in chapter 3 using standard thermal circuit [39, 40].

VDMOS- Fig. 4.10(a) and 4.10(b) show the transfer characteristics for low drain bias. The subthreshold current and transconductance are mainly dictated by the LAMOS while current at higher V_{GS} is also affected by drift region. It can be seen that the subthreshold slope as well as current at higher V_{GS} is excellently modeled. Fig. 4.10(c) shows the $\frac{g_m}{I_{DS}}$ vs. I_{DS} for low drain bias, which is an important parameter for analog design. Fig. 4.11 shows the drain current vs. gate bias for medium drain voltages. The drain current at higher gate bias is heavily affected by the drift region. The accuracy in g_m and $\frac{g_m}{I_{DS}}$ curves can be improved with better mobility models using more fitting parameters [42]. Fig. 4.12(a) and 4.12(b) show the output characteristics ($I_{DS} - V_{DS}$) and output conductance ($|g_{ds}| - V_{DS}$), respectively, for V_{GS}=1.4-2.78V, which demonstrates that the self-heating [39, 24, 40] as well as the impact ionization effect [43] is also well simulated. The delayed transition at higher V_{GS} from linear to saturation on $I_{DS} - V_{DS}$ characteristics owes to the lateral nonuniform doping in the channel as well as the effect of drift region. The first dip in $|g_{ds}|$ in Fig. 4.12(b) is given by the self-heating effect, while the second dip is given by the impact-ionization effect. Fig. 4.13(a), 4.13(b) and 4.13(c) show the normalized gate-to-gate capacitance (C_{GG}), gate-to-drain capacitance (C_{GD}) and gate-to-source+gate-to-body capacitance ($C_{GS} + C_{GB}$), respectively, for V_{DS}=0-5V in steps of 1V. It can be seen that the model shows good behavior for peaks as well as amplitude of peaks in

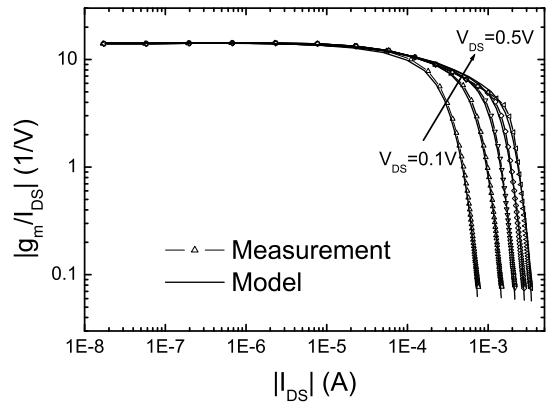
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(a)



(b)



(c)

Figure 4.10: Transfer characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): (a) I_{DS}-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. Note that the subthreshold slope and transition from weak to strong inversion are excellently modeled. The current at higher V_{GS}, which is heavily affected by the drift region, is also correctly modeled by the drift model [38, 41], (b) g_m-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (c) $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V.

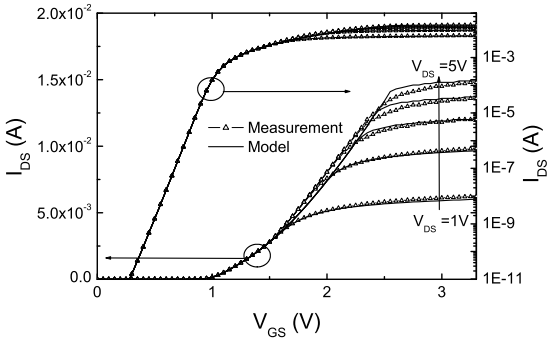


Figure 4.11: Transfer characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): I_{DS}-V_{GS} for V_{DS}=1 to 5V in steps of 1V. Note that the subthreshold slope and transition from weak to strong inversion are well modeled. The current at higher V_{GS} is heavily affected by the drift region.

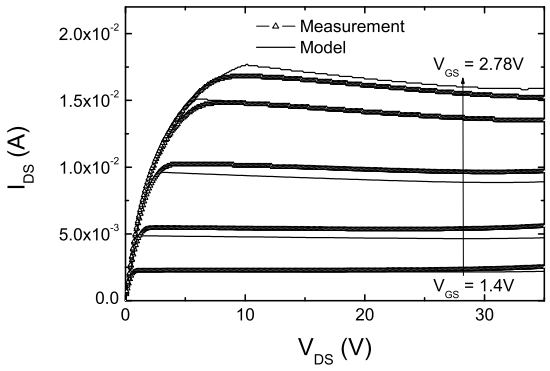
all capacitances, where peaks are dominated by doping gradient in the channel at low V_{DS}, and by the drift region at higher V_{DS}. The rising part of C_{GD} is mainly given by lateral asymmetry in the channel while the fall in C_{GD} is heavily affected by the drift region also demonstrated in section 2.3. As mentioned earlier in Fig. 4.8 and explained in chapter 2, the lateral non-uniform doping produces peaks in C_{GG} and C_{GS} around threshold voltage. The drift region gives higher peaks and also shifts the position of peaks as shown in 4.13(a) and 4.13(c) for nonzero V_{DS}. To understand it better, we can write the normalized C_{GG} expression as,

$$\begin{aligned} C_{GG} &= \frac{dQ_G(V_{GS},V_K,V_S)}{dV_{GS}} \\ &= \frac{\partial Q_G(V_{GS},V_K,V_S)}{\partial V_{GS}} + \frac{\partial Q_G(V_{GS},V_K,V_S)}{\partial V_K}\frac{dV_K}{dV_{GS}} \\ &= C_{GG(LAMOS)} - C_{GD(LAMOS)}\frac{dV_K}{dV_{GS}} \end{aligned} \tag{4.26}$$

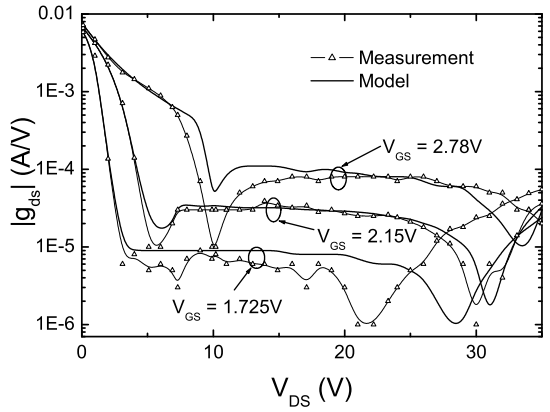
Here V_K is the intrinsic drain potential (the point where LAMOS meets drift region in high voltage devices) shown in Fig. 4.1 [35, 38]. If there is no drift region, then $V_K = V_D$ and second term in (4.26) vanishes as $\frac{dV_K}{dV_{GS}} = 0$. In the presence of the drift region, V_K is not fixed and will vary to maintain a constant current from drain to source. If there is a slight positive change ∂V_{GS} in V_{GS}, the LAMOS current will increase. Now to increase the current in the drift region to the level of LAMOS, V_K should decrease as V_{DS} is fixed. Larger the drift resistance, larger should be the drop in V_K. Thus $\frac{dV_K}{dV_{GS}}$ will be negative for positive values of ∂V_{GS} and from (4.26), it is evident that C_{GG} of any high voltage device would be larger than C_{GG} of LAMOS and will increase with higher drift resistance for nonzero V_{DS}. Thus a good model for HV-MOS needs both excellent modeling of intrinsic MOS channel (which provides $C_{GG(LAMOS)}$) and drift region (which dictates derivative of V_K). The source of discrepancy in Fig. 4.13(a) for V_G higher than threshold voltage and high V_D is still not clear and needs more investigation on these capacitances. It could be due to the function used for the doping concentration in the LAMOS region, which is not fitting well towards source side of the device.

LDMOS- Fig. 4.14(a) and 4.14(b) show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ for low drain bias

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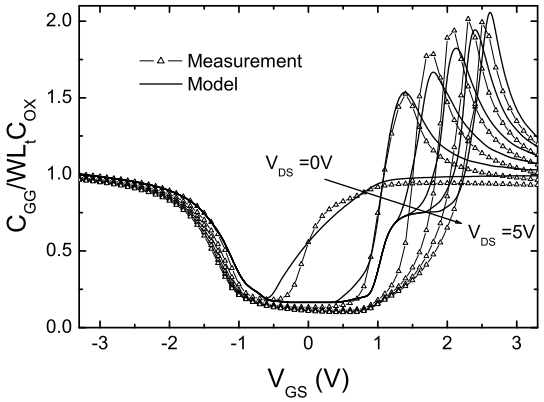
(a)



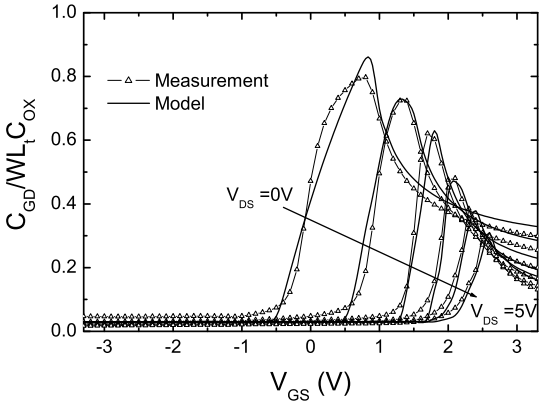
(b)

Figure 4.12: Output characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): (a) Drain current I_{DS} vs. V_{DS} for V_{GS}=1.4, 1.725, 2.15, 2.58 and 2.78V. The linear region is affected by doping gradient in LAMOS channel and drift region. (b) Output conductance $|g_{ds}|$ vs. V_{DS} for three different gate voltages. The first dip in $|g_{ds}|$ is given by self-heating effect [39, 40], while second dip is given by impact-ionization effect [41].

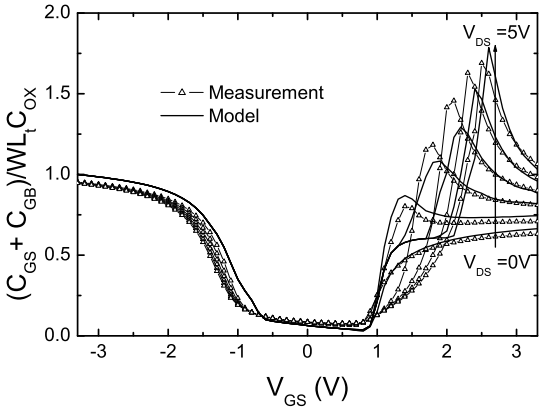
(V_{DS}=0.1 to 0.5V in steps of 0.1V). The current as well as the peaks in transconductance are very well simulated by the model, which proves correct modeling of mobility behavior with transverse field [28] and drift resistance [35, 38]. Fig. 4.14(c) shows the $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. Fig. 4.15(a) and 4.15(b) show the transfer characteristics ($I_D - V_{GS}$) and transconductance ($g_m - V_{GS}$) for medium drain bias (V_{DS}=1 to 5V in steps of 1V). The subthreshold slope as well as value of current for higher gate bias is correctly modeled for all drain voltages. The current at higher gate and drain bias in Fig. 4.15(a) is heavily affected by the drift region. Fig. 4.16 shows the output characteristics ($I_{DS} - V_{DS}$) for V_{GS}= 4-12V in steps of 2V. The prolonged linear region on output characteristics is affected by both, the lateral non-uniform doping and the drift region. The self-heating and the impact ionization effect are also well simulated [24, 39, 40]. It should be noted that even though the DC curves can be fitted with existing low voltage MOS models with uniform doping in the



(a)



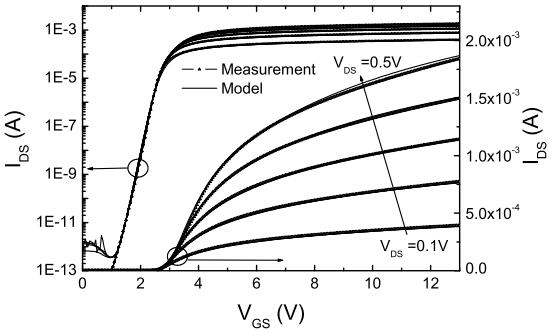
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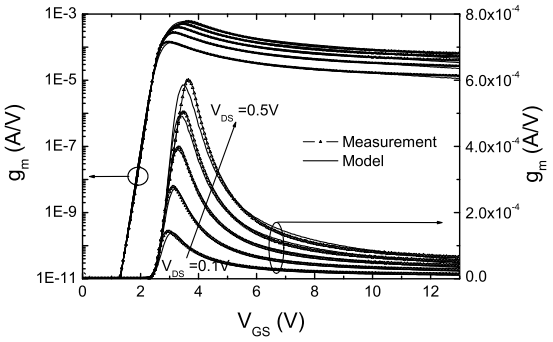
(c)

Figure 4.13: AC Characteristics of 50V VDMOS: (a) Normalized C_{GG} capacitance vs. V_{GS} for V_{DS}=0-5V in steps of 1V. The peaks in C_{GG} at low V_{DS} are dominated by doping gradient while increase in peaks with higher V_{DS} is dictated by drift region. (b) Normalized C_{GD} capacitance vs. V_{GS} for V_{DS} =0-5V. The C_{GD} peak at V_{DS}=0 is around threshold voltage due to lateral doping [36, 37, 2], but it shifts towards left with higher drift resistance (higher drift length/resistivity) or higher lateral doping gradient. (c) Normalized $C_{GS}+C_{GB}$ capacitance vs. V_{GS} for V_{DS}=0-5V. The peaks in $C_{GS}+C_{GB}$ are combined effect of both lateral doping and drift region. For capacitance normalization, $L_t = L + L_{ov}$ denotes the total gate length.

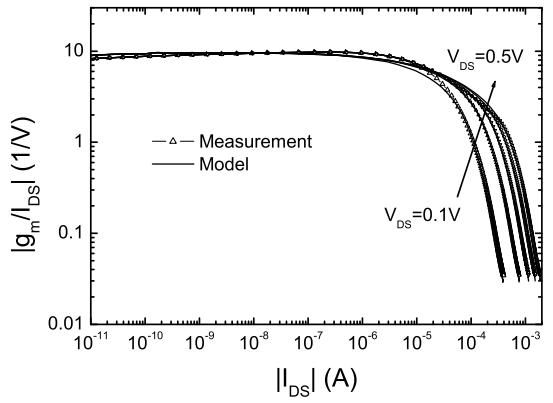
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(a)



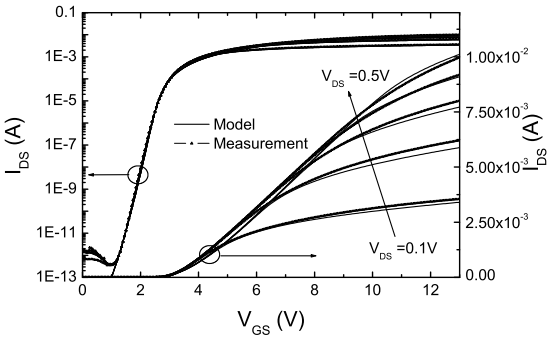
(b)



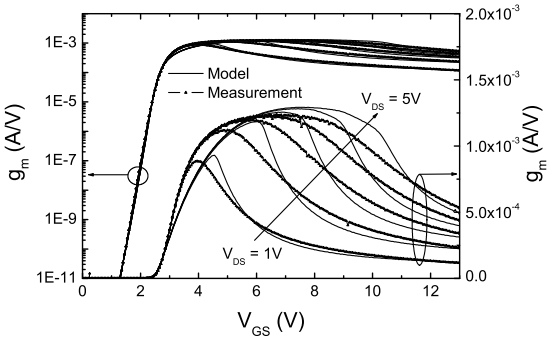
(c)

Figure 4.14: Transfer characteristics of 40V LDMOS (W=40μm, L=1.2μm at T=30°C): (a) I_{DS}-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (b) g_m-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (c) $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V.

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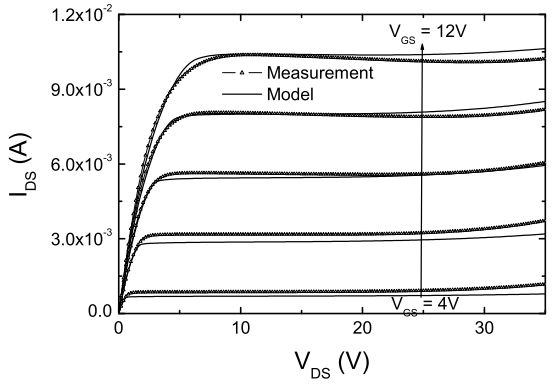


(a)



(b)

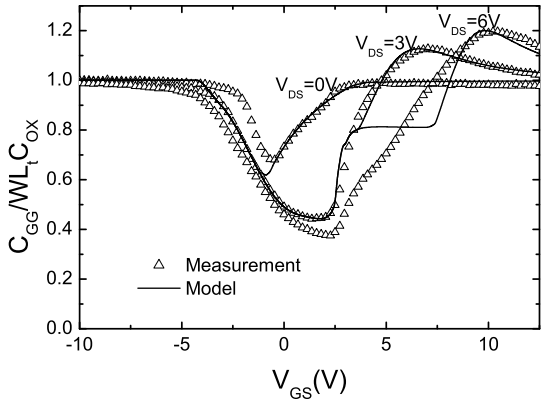
Figure 4.15: Transfer characteristics of 40V LDMOS at medium drain bias (W=40μm, L=1.2μm at T=30°C): (a) I_{DS}-V_{GS} (b) g_m-V_{GS} for V_{DS}=1 to 5V in steps of 1V. Note that the subthreshold slope and transition from weak to strong inversion are well modeled. The current at higher V_{GS} is heavily affected by the drift region.



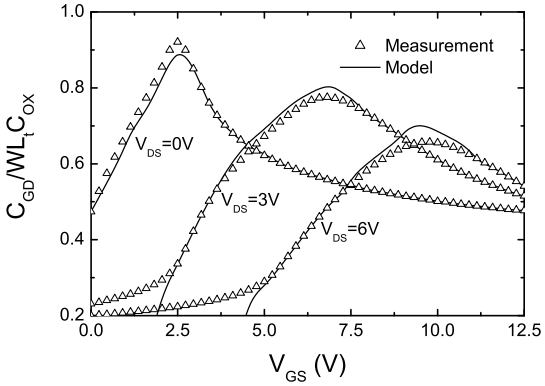
(a)

Figure 4.16: Output characteristics of 40V LDMOS (W=40μm, L=1.2μm at T=30°C): Drain current I_D vs. V_{DS} for V_{GS}=4 to 12V in steps of 2V. The linear region is affected by both the lateral non-uniform doping in the LAMOS channel and drift region.

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(a)



(b)

Figure 4.17: AC characteristics of 40V LDMOS: (a) Normalized C_{GG} vs. V_{GS} for V_{DS}=0, 3 and 6V. The peak in C_{GG} at low drain bias arises due to lateral asymmetry. The peaks at higher drain and gate bias can be explained by the combined effect of lateral non-uniform doping and effect on drift region. (b) Normalized gate-to-drain capacitance (C_{GD}) vs. V_{GS} for V_{DS}=0 3 and 6V. The peak in C_{GD} at V_{DS}=0 is around threshold voltage [37, 2] while it shifts towards left with higher drift resistance (higher drift length/resistivity) or higher lateral doping gradient. For capacitance normalization, $L_t = L + L_{ov}$ denotes the total length.

channel as shown in chapter 3 [35, 38], the modeling of lateral non-uniform doping provides more physical tuning of parameters e.g. threshold voltage, body effect coefficient etc. in the model. Fig. 4.17(a) shows the $C_{GG} - V_{GS}$ for V_{DS}=0, 3 and 6V. The C_{GG} behavior at low gate bias is dominated by the lateral doping while at higher gate bias the peaks are dictated by drift region. The higher the drift resistance (large drift length or high value of drift resistivity), higher the peak in C_{GG} and vice-versa. Fig. 4.17(b) shows the $C_{GD} - V_G$ for V_{DS}=0, 3 and 6V. As mentioned earlier, the peak in C_{GD} can be explained by the lateral asymmetry present in the intrinsic MOS. The decreasing part of C_{GD} is affected by both the nonuniform doping in the channel and the drift region as explain in chapter 2. It should be noted that it is very important

to correctly model the drift region (or V_K behavior [41]) for the correct behavior after the peaks in all capacitances [44]. The peak in C_{GD} at V_{DS}=0 is around threshold voltage due to lateral doping [37, 2], but the position of the peak will shift towards left and amplitude of the peak will decrease with higher drift resistance (large drift length or high value of drift resistivity). To understand it, we can express C_{GD} of LDMOS as $C_{GD(LAMOS)}\frac{dV_K}{dV_{DS}}$, and can apply same analysis as for C_{GG} discussed above. Higher difference in doping between source and drain produces higher peaks on C_{GD}, already shown in chapter 2. The discrepancy in the results is due to the charge sheet approximation and various approximations taken in model development.

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4.4 Conclusion

A *novel* charge based compact analytical model for lateral non-uniformly doped MOSFET was developed in this chapter. The model is developed using charge based EKV formalism. The major impact of the lateral non-uniform doping was seen on the capacitances, whose modeling has been a daunting task till now as expressions become non-integrable and non-implicit for current and charges. The inversion charge linearization paved the way to approximate the surface pinch-off potential across the channel. This led to develop integrable expressions for current and then charges. The inversion and gate charge in this model have clear dependence on the drain current, which is not the case in the conventional MOSFET models.

The proposed model was used for modeling of high voltage devices with a lateral doping gradient using an appropriate drift model. To the best of our knowledge, *this is the first time, the modeling of lateral non-uniform doping has been implemented in any high voltage compact model.* The model shows good behavior for all capacitances as well as for DC, when compared with device simulation and measurements. The position of the capacitance peaks as well as their amplitude are correctly simulated by the model. The major impact of the proposed model is on the accuracy improvement of high voltage MOSFET models especially during transient operations (i.e. modeling of the bias-dependent peaks and slopes of device capacitances).

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Chapter 5

Partitioning Scheme and Noise Modeling in the Lateral Non-Uniformly doped MOSFET

The Ward-Dutton partitioning scheme [1] is used extensively to develop transient and high frequency advanced compact models in MOSFET analysis [2]. Recently, it has been recognized that capacitance property of Lateral Non-Uniformly doped or Lateral Asymmetric MOSFET (LAMOS) [3, 4, 5, 6, 7] is fundamentally different from conventional MOSFET [6, 4] because Ward-Dutton partitioning is not applicable to this kind of devices. In this work, it will be shown that although it is not possible to guaranty a partitioning scheme for general operation of the MOSFET but it is possible to show the existence of a partitioning scheme for small-signal operation of the device in LAMOS [8]. Application of this new concept in capacitance evaluation of LAMOS considerably simplifies the existing capacitance evaluation methodology [4, 6]. This work also provides a simpler way to physically understand the unusual behavior of drain-to-gate capacitance C_{DG} in LAMOS. The proposed theory is validated by extensive numerical and device simulation. Recently generalization of this partitioning scheme including mobility degradation has also been published in the literature [9].

In the second part of this chapter, for the first time, an analytical noise modeling methodology in presence of lateral asymmetry will be presented [10]. It will be shown that noise properties of LAMOS are considerably different from the prediction of conventional Klaassen-Prins [11] based methods and at low gate voltages, they can overestimate the noise by 2-3 orders of magnitude.

5.1 Introduction

All of the advanced compact MOSFET models (PSP, MM11, HISIM, BSIM, EKV etc., see [2] and the references therein) dedicated to even sub 100 nm devices are entirely built on the Ward-Dutton partitioning [1], which was originally derived for long-channel uniformly doped MOSFET. Recently, in the pioneering work by Aarts et. al. [4], it has been recognized that the Ward-Dutton charge partitioning [1] is not applicable in LAMOS and it has been concluded that "no terminal charges exist from which the capacitances can be derived". Therefore, [4] is

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forced to solve the small-signal continuity equation under quasi-static assumption for both real and imaginary part of perturbed channel potential and calculate the capacitances from them.

Although it is not possible to guaranty a partitioning scheme for general operation of the LAMOS but it is possible to show the existence of a partitioning scheme for small-signal operation of the device in LAMOS [8]. Existence of the small signal partitioning implies that we can always define a partitioning of small-signal/perturbed charges to calculate the terminal capacitances. This alternate approach has major advantage over the existing approach as it eliminates the need of solving the continuity equation for the imaginary part of perturbed channel potential which results in a saving of one level of numerical numerical integration compared to [4]. In addition to these, it provides thorough physical insight to understand the unusual behavior of C_{DG}. This concept can also be used in the partitioning of gate tunnelling current and even noise, which are of importance in the standard CMOS devices, where, lateral asymmetry is inherent due to halo implant.

5.2 Partitioning Scheme

The current at any position x in the LAMOS/MOSFET can be written as

$$I(x) = g(x, V) \cdot \frac{dV}{dx}, \tag{5.1}$$

where $g = \mu W Q_i$ and μ, W, Q_i and V are the mobility, width, inversion charge density and channel potential respectively. Please note that in presence of velocity saturation, μ starts to depend on the electric field, so g will be a function of V and $\frac{dV}{dx}$ [12, 9] but in the present work we will consider μ to be independent of electric field. The explicit dependence of g on x implies that the doping may also vary along the channel, which is the case for a LAMOS [5, 3, 7]. Let's assume the general form of continuity equation as

$$\frac{dI}{dx} = \widehat{s}. \tag{5.2}$$

Please note that this $\widehat{s}$ expression of source term is completely general. It can be a term like $W\frac{dQ}{dt}$ (rate of change of charge per unit length) in case of a transient or term like $i_g(x)$ (gate current per unit length) in case of a gate tunnelling current. Existence of a partitioning scheme means that it is possible to decouple the current when $\widehat{s} = 0$ (we will call this current as I_0) and the effect of source term. In other words, the terminal current can be expressed as a sum of I_0 and a weighted integral of $\widehat{s}$. To see why Ward-Dutton scheme [1] fails in presence of lateral asymmetry [5, 3, 7] or mobility degradation [12], We first multiply (5.2) by x and integrate from 0 to L,

$$\int_0^L x\frac{dI}{dx}dx = \int_0^L x\widehat{s}dx \tag{5.3}$$

and integrating by parts yields

$$xI|_0^L - \int_0^L I(x)dx = \int_0^L x\widehat{s}dx \tag{5.4}$$

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Substituting (5.1) in the above equation, we obtain

$$I(L) = \frac{1}{L}\int_{V_s}^{V_d} g(x,V)dV + \int_0^L \frac{x}{L}\widehat{s}dx \tag{5.5}$$

When g is a function of V only (the classical constant mobility case), the first integral depends only on the value of V at the boundaries. The point is, even if the function $V(x)$ (the channel potential distribution) changes because of the $\widehat{s}$ term, the value of the integral does not change and remains equal to the case when $\widehat{s} = 0$. In the case when $\widehat{s} = 0$, we can easily identify the integral as DC current I_0 and we get back the Ward-Dutton partitioning scheme. But when g starts to depend also on x, the situation is different. As $V(x)$ changes due to the presence of the source term in the continuity equation, the value of the integral starts to depend on the profile of V(x). Therefore, $\frac{1}{L}\int_{V_s}^{V_d} g(x,V)dV$ is different in the presence of the source term. So in the presence of lateral asymmetry,

$$I(L) \neq I_0 + \int_0^L \frac{x}{L}\widehat{s}dx \tag{5.6}$$

To extend the concept of partitioning, Let's define a quantity $\widehat{I}(x) = I(x) - I_0$. It trivially follows that $\widehat{I}(x)$ satisfies

$$\frac{d\widehat{I}(x)}{dx} = \widehat{s} \tag{5.7}$$

Let us now consider an arbitrary function $F(x) = \int_0^x f(x)dx$ and multiply (5.7) by $F(x)$ and integrate by parts from 0 to L to obtain

$$F(x)\widehat{I}(x)|_0^L - \int_0^L \widehat{I}(x)d[F(x)] = \int_0^L F(x)\widehat{s}dx \tag{5.8}$$

or

$$\Big[F(L)\widehat{I}(L) - F(0)\widehat{I}(0)\Big] - \int_0^L \widehat{I}(x)f(x)dx = \int_0^L F(x)\widehat{s}dx \tag{5.9}$$

or

$$I(L) = I_0 + \int_0^L \frac{F(x)}{F(L)}\widehat{s}dx + \frac{1}{F(L)}\int_0^L f(x)(I(x) - I_0)dx \tag{5.10}$$

Note that an existence of partitioning scheme implies that the terminal current can be expressed as a sum of I_0 and a weighted integral of $\widehat{s}$. So in order to have a partitioning scheme, the last term in (5.10) must vanish or in other words, the existence of a function such that for any given $\widehat{s}$, the following holds

$$\int_0^L f(x)I(x)dx = \int_0^L f(x)I_0dx \tag{5.11}$$

or from (5.1)

$$\int_0^L f(x)g(x,V)\cdot\frac{dV}{dx}dx = \int_0^L f(x)g\left(x,V_0\right)\cdot\frac{dV_0}{dx}dx \tag{5.12}$$

Please note that when g does not depend on x, $f(x) = 1$ trivially satisfies the above criterion and we get back the original Ward-Dutton charge partitioning. In general we can not guarantee the existence of the funtion $f(x)$ and hence the charge partitioning scheme. But we will prove

that, when $\widehat{s}$ can be considered as a small perturbation, we can always find out the function $f(x)$ for any general form of g.

As we are considering the case when $\widehat{s}$ can be treated as a small perturbation, we will start with a perturbation analysis of $I(x)$. In the subsequent analysis subscript $'0'$ will be used to denote the situation when $\widehat{s} = 0$. The perturbed current $i(x)$ can be obtained from

$$I(x) = I_0 + i(x) = g\left(x, V_0 + v\right) \frac{d(V_0 + v)}{dx} \tag{5.13}$$

where I_0 and V_0 are the unperturbed current and voltage respectively, in the channel. Taking a first order Taylor series expansion around V_0 (the unperturbed point), we obtain

$$I(x) = I_0 + i(x) = \left[g\left(x, V_0\right) + \frac{\partial g\left(x, V_0\right)}{\partial V_0} v\right] \left(\frac{dV_0}{dx} + \frac{dv}{dx}\right) \tag{5.14}$$

Neglecting second order term we obtain

$$i(x) = g\left(x, V_0\right) \frac{dv}{dx} + \frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} v \tag{5.15}$$

To proceed further, we note that

$$\frac{dg\left(x, V_0\right)}{dx} = \frac{\partial g\left(x, V_0\right)}{\partial x} + \frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} \tag{5.16}$$

or

$$\frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} = \frac{dg\left(x, V_0\right)}{dx} - \frac{\partial g\left(x, V_0\right)}{\partial x} \tag{5.17}$$

Substituting (5.17) into (5.15), we obtain

$$i(x) = \left[g\left(x, V_0\right) \frac{dv}{dx} + \frac{dg\left(x, V_0\right)}{dx} v\right] - \frac{\partial g\left(x, V_0\right)}{\partial x} v \tag{5.18}$$

or

$$i(x) = \left[\frac{d[g\left(x, V_0\right) v]}{dx} - \frac{\partial g\left(x, V_0\right)}{\partial x} v\right] \tag{5.19}$$

As $i(x) = I(x) - I_0$, we seek a function from (5.10) such that

$$\int_0^L f(x) i(x) dx = 0 \tag{5.20}$$

Now from (5.19) and (5.20), if we can find a function $f(x)$ such that

$$\int_0^L f(x) \left[\frac{d\left[g(x, V_0) v\right]}{dx} - \frac{\partial g(x, V_0)}{\partial x} v\right] dx = 0 \tag{5.21}$$

for all v then we can define a partitioning scheme. Then $f(x)$ must satisfy

$$\int_0^L f(x) \frac{d\left[g(x, V_0) v\right]}{dx} dx = \int_0^L f(x) \frac{\partial g(x, V_0)}{\partial x} v dx \tag{5.22}$$

Now we integrate the LHS by parts and use the fact that v vanishes at the boundary to obtain

$$\int_0^L \left[\frac{df(x)}{dx}g(x,V_0) + f(x)\frac{\partial g(x,V_0)}{\partial x}\right] v dx = 0 \tag{5.23}$$

This criterion gives a differential equation of $f(x)$ as

$$\frac{df(x)}{dx}g(x,V_0) = -f(x)\frac{\partial g(x,V_0)}{\partial x} \tag{5.24}$$

or

$$\frac{\left[\frac{df(x)}{dx}\right]}{f(x)} = -\frac{\left[\frac{\partial g(x,V_0)}{\partial x}\right]}{g(x,V_0)} \tag{5.25}$$

which can be solved at once as

$$f(x) = \exp\left[-\int_0^x \left(\frac{\frac{\partial g(x',V_0)}{\partial x'}}{g(x',V_0)}\right) dx'\right] \tag{5.26}$$

Note that for a conventional MOSFET $\frac{\partial g(x',V_0)}{\partial x'} = 0$ and so $f(x)$ becomes 1 and we get back the original Ward-Dutton scheme. For LAMOS, the final result from (5.10) and (5.26) becomes

$$I(L) = I_0 + \int_0^L \frac{\int_0^x \exp\left[-\int_0^x \left(\frac{\frac{\partial g(x_1,V_0)}{\partial x_1}}{g(x_1,V_0)}\right) dx_1\right] dx}{\int_0^L \exp\left[-\int_0^x \left(\frac{\frac{\partial g(x_1,V_0)}{\partial x_1}}{g(x_1,V_0)}\right) dx_1\right] dx} \widehat{s} dx \tag{5.27}$$

5.3 APPLICATION of small signal partitioning

In this section we will show how the concept of small signal partitioning can be applied to (a) capacitance and admittance calculation in the LAMOS (b) calculation of gate tunneling current and (c) partitioning of gate tunneling noise between the source and the drain.

5.3.1 Capacitance Evaluation of LAMOS

In small signal analysis, the drain current i_d can be expressed as

$$i_d = \sum_m Y_{dk} v_k + j\omega \sum_m C_{dk} v_k \tag{5.28}$$

where v_k are the terminal small signal voltage, Y's are the admittances and C's are the capacitances.

In case of transient, the source term $\widehat{s}$ is $W\frac{dQ}{dt}$. For small signal analysis, it reduces to $Wj\omega q$, where q is the perturbed inversion charge and can be expressed as

$$q(x) = \frac{\partial Q}{\partial V_G} v_g + \frac{\partial Q}{\partial V} v(x) \tag{5.29}$$

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where v_g and $v(x)$ are the perturbed gate voltage and channel potential respectively. In order to obtain the terminal currents we need to solve the coupled small signal and continuity equation [4]. But thanks to the small signal partitioing , we can express the drain current as

$$i_d = i_0 + \omega W \int_0^L \frac{F(x)}{F(L)} \left[\frac{\partial Q}{\partial V_G} v_g + \frac{\partial Q}{\partial V} v(x) \right] dx \tag{5.30}$$

where i_0 is the current when $\frac{di}{dx} = 0$.

As we have already derived the partitioning scheme in the previous section, all it remains is to express $v(x)$ and i_0 in terms of perturbed terminal voltage v_g,v_s and v_d, so that (5.28) and (5.30) can be compared to derive the capacitances as well as admittances. Under quasi-static assumption (also used in [4]) $v(x)$ becomes real and equal to the value when $\frac{di}{dx} = 0$. As we are now taking variation of V_G into account, the perturbed current becomes

$$i(x) = g(x, V_0 + v, V_G + v_g) \frac{d(V_0 + v)}{dx} - g(x, V_0, V_G) \frac{dV_0}{dx} \tag{5.31}$$

or

$$i(x) = \frac{\partial g(x, V_0, V_G)}{\partial V_0} \frac{dV_0}{dx} v + g(x, V_0, V_G) \frac{dv}{dx} + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.32}$$

Using (5.17) into (5.32),

$$i(x) = \left[\frac{dg(x, V_0, V_G)}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} \right] v + g(x, V_0, V_G) \frac{dv}{dx} + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.33}$$

or

$$i(x) = \frac{d[g(x, V_0, V_G)v]}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} v + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.34}$$

It should be noticed that appearance of an extra v_g term does not change the partitioning function. Now under QS assumption the differential equation for $v(x)$ satisfies

$$\frac{d[g(x, V_0, V_G)v]}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} v + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g = i_0 \tag{5.35}$$

where i_0 is to be determined. This ODE is solved below to obtain $v(x)$ and i_0.

The differential equation for $v(x)$ (5.35) can be rewritten as

$$\frac{d[g(x, V_0, V_G)v]}{dx} - \frac{1}{g(x, V_0, V_G)} \frac{\partial g(x, V_0, V_G)}{\partial x} [g(x, V_0, V_G)v] = i_0 - \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.36}$$

We can consider this as a linear ODE with respect to $g(x, V_0, V_G)v(x)$ and can be solved using the integration factor $R(x)$ which is given by

$$R(x) = exp \left[- \int_0^x \frac{1}{g(x, V_0, V_G)} \frac{\partial g(x, V_0, V_G)}{\partial x} dx \right] \tag{5.37}$$

Multiplying (5.36) by R(x) we obtain

$$\frac{d[R(x)g(x, V_0, V_G)v(x)]}{dx} = i_0 R(x) - R(x) \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.38}$$

Let's define two auxiliary variables $\lambda_v(x)$ and $\lambda_g(x)$ as

$$\lambda_v(x) = \int_0^x R(x)dx \tag{5.39}$$

$$\lambda_g(x) = \int_0^x R(x)\frac{\partial g(x, V_0, V_G)}{\partial V_G}\frac{dV_0}{dx}dx \tag{5.40}$$

Using the definition of $\lambda_v(x)$ and $\lambda_g(x)$, and integrating (5.38) from 0 to x we obtain

$$R(x)g_0(x)v(x) - g(0, V_S, V_G)v_s = i_0\lambda_v(x) - v_g\lambda_g(x) \tag{5.41}$$

where we have used the fact that $R(0) = 1$, $V_0(0) = V_S$ and $v(0) = v_s$. Now i_0 from (5.41) can be obtained using the fact that $V_0(L) = V_D$, $v(L) = v_d$ as

$$i_0 = \frac{\lambda_g(L)}{\lambda_v(L)}v_g - \frac{g(0, V_S, V_G)}{\lambda_v(L)}v_s + \frac{R(L)g(L, V_D, V_G)}{\lambda_v(L)}v_d \tag{5.42}$$

Substituting i_0 from (5.42) in (5.41), we obtain

$$v(x) = G(x)v_g + S(x)v_s + D(x)v_d \tag{5.43}$$

where $G(x)$, $S(x)$ and $D(x)$ are given by

$$G(x) = \frac{\lambda_g(L)}{\lambda_v(L)}\frac{\lambda_v(x)}{R(x)g(x, V_0, V_G)} - \frac{\lambda_g(x)}{R(x)g(x, V_0, V_G)} \tag{5.44}$$

$$S(x) = \frac{g(0, V_S, V_G)}{R(x)g(x, V_0, V_G)}(1 - \frac{\lambda_v(x)}{\lambda_v(L)}) \tag{5.45}$$

$$D(x) = \frac{\lambda_v(x)}{\lambda_v(L)}\frac{R(L)g(L, V_D, V_G)}{R(x)g(x, V_0, V_G)} \tag{5.46}$$

Now comparing (5.28) with (5.30), one can easily calculate the capacitances and admittances. For instance C_{DG} and C_{SG} can be expressed as

$$C_{DG} = W\int_0^L \frac{F(x)}{F(L)}\left[\frac{\partial Q}{\partial V_G} + \frac{\partial Q}{\partial V}G(x)\right]dx \tag{5.47}$$

$$C_{SG} = W\int_0^L \left[1 - \frac{F(x)}{F(L)}\right]\left[\frac{\partial Q}{\partial V_G} + \frac{\partial Q}{\partial V}G(x)\right]dx \tag{5.48}$$

Please note that above expressions have similar appearance as Ward-Dutton partitioning scheme where $F(x) = x$. Also by applying the concept of small signal partitioning, we have achieved a considerable simplification over the existing capacitance calculation method for LAMOS. Given the $g(x, V_0)$, development reported in [6, 4] requires 4 level of numerical integration, whereas our approach eliminates a whole level of integration with out sacrificing any accuracy.

Similarly all other capacitances associated with drain and source terminals can be expressed as

$$C_{DS} = W\int_0^L \frac{F(x)}{F(L)}\left[\frac{\partial Q}{\partial V}S(x)\right]dx \tag{5.49}$$

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$$C_{DD} = W \int_0^L \frac{F(x)}{F(L)} \left[\frac{\partial Q}{\partial V} D(x) \right] dx \tag{5.50}$$

$$C_{DB} = W \int_0^L \frac{F(x)}{F(L)} \left[-\frac{\partial Q}{\partial V_G} - \frac{\partial Q}{\partial V} \left[G(x) + S(x) + D(x) \right] \right] dx \tag{5.51}$$

$$C_{SD} = W \int_0^L \left[1 - \frac{F(x)}{F(L)} \right] \left[\frac{\partial Q}{\partial V} D(x) \right] dx \tag{5.52}$$

$$C_{SS} = W \int_0^L \left[1 - \frac{F(x)}{F(L)} \right] \left[\frac{\partial Q}{\partial V} S(x) \right] dx \tag{5.53}$$

$$C_{SB} = W \int_0^L \left[1 - \frac{F(x)}{F(L)} \right] \left[-\frac{\partial Q}{\partial V_G} - \frac{\partial Q}{\partial V} \left[G(x) + S(x) + D(x) \right] \right] dx \tag{5.54}$$

Please note all the terminal voltages are defined with respect to body terminal. Thus the expressions of terminal small signal voltages in C_{DB} and C_{SB} have $v_s = v_d = v_g = -v_b$.

The admittances of LAMOS from (5.42) are given by

$$Y_{DG} = \frac{\lambda_g(L)}{\lambda_v(L)}, Y_{DS} = -\frac{g_0(0)}{\lambda_v(L)}, Y_{DD} = \frac{R(L)g_0(L)}{\lambda_v(L)}, \tag{5.55}$$

5.3.2 Partitioning of Gate Tunnelling Current

When we consider gate tunnelling current as a perturbation , we use (5.2) with $\widehat{s} = i_g(x)$, where $i_g(x)$ is the gate tunnelling current per unit length. Therefore, under the presence of a gate tunnelling current, the drain current becomes

$$I_D = I_0 + \int_0^L \frac{F(x)}{F(L)} i_g(x) dx \tag{5.56}$$

It should be noticed that as gate tunnelling current increases, it may not be possible to consider $\widehat{s}$ as a perturbation, and in presence of high gate current, there can be a significant de-biasing of channel and full solution of coupled continuity and transport equation may be needed.

5.3.3 Partitioning of Gate Tunnelling Noise

For noise partitioning, we need to relate drain current fluctuation δi_d to gate current fluctuation δi_g. Following [13], from (5.56) we obtain

$$\delta i_d = \frac{1}{F(L)} \int_0^L F(x) \delta i_g(x) dx \tag{5.57}$$

then in terms of noise

$$S_{i_d}^g = \frac{1}{F(L)^2} \int_0^L \int_0^L F(x_1) F(x_2) \overline{\delta i_g(x_1) \delta i_g(x_2)} dx_1 dx_2 \tag{5.58}$$

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Assuming that the noise sources at different position are uncorrelated $\overline{\delta i_g(x_1)\delta i_g(x_2)} = S_g(x_1)\delta(x_1 - x_2)$, we finally obtain

$$S_{i_d}^g = \frac{1}{F(L)^2}\int_0^L \int_0^L F(x)^2 S_g(x)dx \tag{5.59}$$

We can split the local gate noise $S_g(x)$ into two parts as $S_g(x) = S_g^{shot}(x) + S_g^{flicker}(x)$. Now $S_g^{shot}(x)$ and $S_g^{flicker}(x)$ must have different x dependence because [13]

$$\int_0^L S_g^{shot}(x)dx \propto I_G \tag{5.60}$$

and

$$\int_0^L S_g^{flicker}(x)dx \propto I_G^2 \tag{5.61}$$

Therefore a bit detailed analysis by us clearly shows that the noise partitioning depends on the details of the noise mechanism (the $S_g(x)$ term) and will be different for shot and flicker noise, even in the conventional MOSFET.

5.4 Discussion and Results

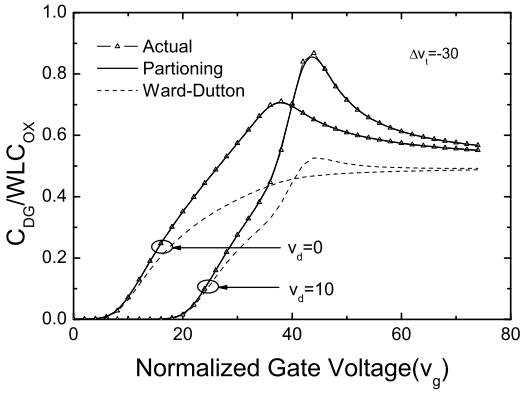
In this section, we address how a bias dependent partitioning function gives rise to peaks in C_{DG} and validates our approach by comparing our scheme with numerical and device simulation. In order to study the impact of lateral asymmetry we take a position dependent threshold voltage $V_T(x)$ as [6, 4, 14]

$$V_T(x) = v_{t0} \cdot U_T + \Delta v_t \cdot U_T(1 - exp(-\alpha \cdot (x/L)^2)) \tag{5.62}$$

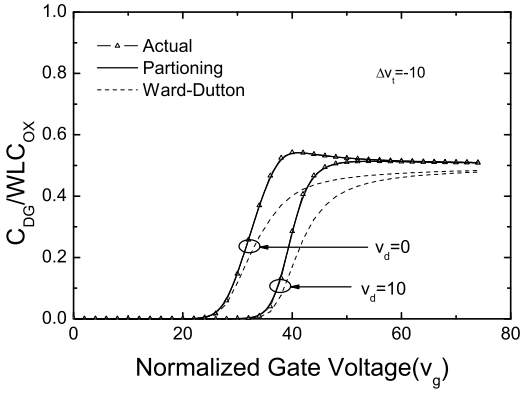
where U_T is the thermal voltage v_{t0} is the normalized threshold voltage at the source, Δv_t is indicative of the difference between the source and drain threshold voltages and α determines the sharpness of the profile. Now we calculate the capacitances numerically as follows: we first vary any terminal voltages by δv_k and solve the small signal version of (5.2) to obtain $v(x)$ and substitute this in (5.34) to obtain the imaginary part of the current (i_y^{im}) at the source or the drain. By definition the capacitance becomes $C_{yk} = i_y^{im}/(j\omega\delta v_k)$. We will call these capacitances as actual capacitances. We also calculate the capacitances using our partitioning scheme (5.51) and (5.54) and Ward-Dutton partitioning scheme. For numerical simulation, we will take v_{t0}=40, $\alpha = 1.3$, $\Delta v_t = -10, -30$ and $v_d = 0, 10$. It has been confirmed that at low frequency, the actual capacitances are independent of the frequency, which means as expected the quasi-static assumption holds quite well.

Fig. 5.1(a) shows the plot of C_{DG} calculated by the three different methods for $\Delta v_t = -30$. As expected, our partitioning scheme and exact numerical solution show the perfect agreement and captures the peaks in C_{DG} which is a typical characteristics of LAMOS. The peak in C_{DG} can be explained by the bias dependence of partition function. First, consider the situation, when the source is in weak inversion and the drain is in strong inversion. This situation will occur because the threshold voltage at the source is greater than the threshold voltage at drain. In this case, as $g(x, V_0, V_G)$ is very small near the source, the function $f(x)$ decays off very rapidly

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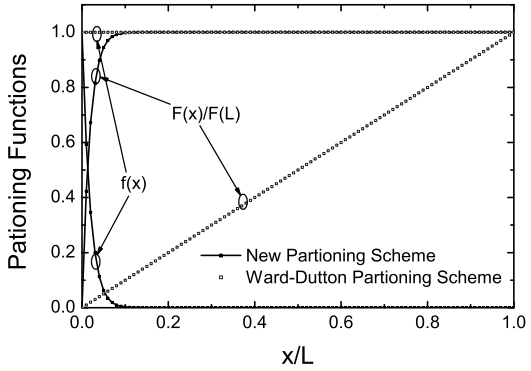
(a)



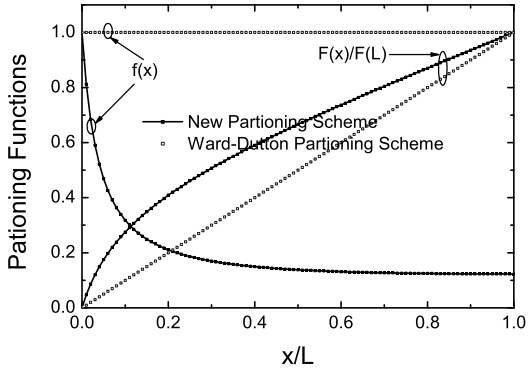
(b)

Figure 5.1: The plot of drain-to-gate capacitance C_{DG} vs v_g for (a) $\Delta v_t = -30$ and (b) $\Delta v_t = -10$. All the voltages have been normalized by thermal voltage U_T.

near the source because of the $\frac{1}{g(x,V_0,V_G)}$ term present in the exponential of $f(x)$. As a result, the partition function $F(x)$ (which is the integral of $f(x)$) remains constant almost all over the channel except a very small region near the source where it increases to take the saturation value (see Fig. 5.2(a)). Now in this situation as the gate voltage increases a part of channel gradually comes out of the weak inversion and enters the strong inversion. Therefore C_{DG} increases with gate voltage. This situation continues till the gate voltage is less than the threshold voltage of the source end. As the gate voltage exceeds the threshold voltage of the source end, the region near the source starts to enter into the strong inversion because of this the $g(x, V_0, V_G)$ starts to increase. As a result, the function $f(x)$ decays less rapidly and $F(x)$ increases continuously (see Fig. 5.2(b)). It means that the capacitance near the strongly inverted source region now gradually getting a lesser weight, as a consequence C_{DG} decreases with the gate voltage. Note that as Ward-Dutton partitioning function always take $F(x) = x$, it can never explain the sharp peak in C_{DG} curve. Also note that for $v_d = 10$, the peak increases because a change in gate voltage induces a change in the channel potential (the perturbed channel potential becomes



(a)

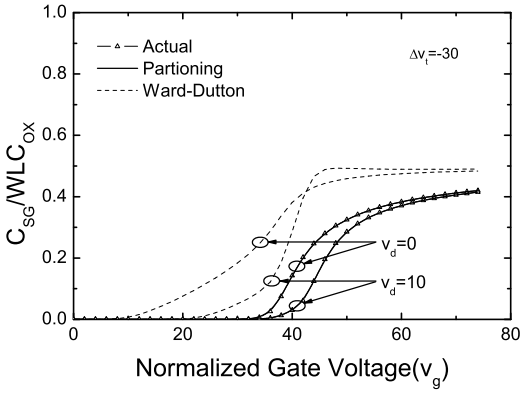


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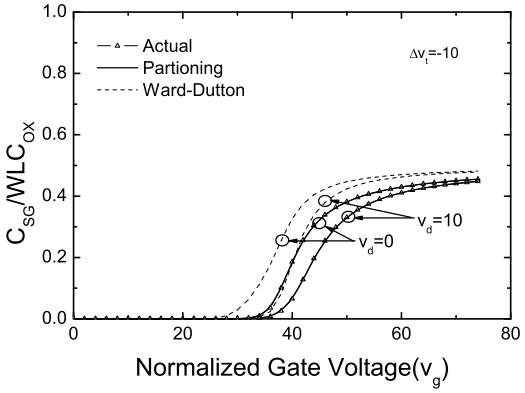
Figure 5.2: Profile of partitioning functions for (a) $v_g < v_{t0}$ and (b) $v_g > v_{t0}$. In the first case, as $g(x, V_0, V_G)$ is very small near the source, the function f(x) decays off very rapidly near the source (because of the $\frac{1}{g(x,V_0,V_G)}$ term present in the $\widehat{s}$ term). As a result, the partition function $F(x)$ (which is the integral of $f(x)$) remains constant almost all over the channel. In the second case, $f(x)$ decays less rapidly in strong inversion and thus $F(x)$ is increasing continuously from source to drain.

negative), which in turn causes a change in charge distribution and the combined effect increases the peak. To understand why perturbed channel potential can become negative to increase the small signal charge, consider the situation, when the source end is weakly inverted and drain end is strongly inverted. In this case the transistor can be thought of a series combination of two transistors with different threshold voltage, where the one near the source is weakly inverted and near the drain end is strongly inverted. Now let Q_S and Q_D be the charge at the source and drain end of the strongly inverted. The current I flowing through this transistor is proportional to $Q_S^2 - Q_D^2$. The weakly inverted transistor in series forces I to be very small, therefore $Q_S^2 \approx Q_D^2$. Now as gate voltage increases both Q_S and Q_D will increase and we have $\delta Q_S Q_S \approx \delta Q_D Q_D$. As drain end is kept at a fixed channel potential and is in strong inversion

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(a)

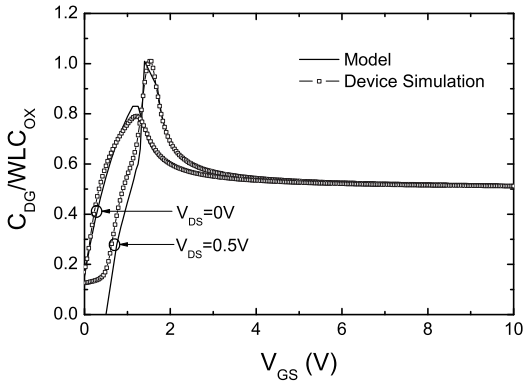


(b)

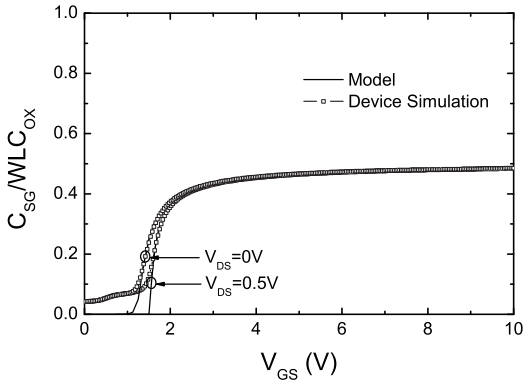
Figure 5.3: The plot of source-to-gate capacitance C_{SG} vs v_g for (a) $\Delta v_t = -30$ and (b) $\Delta v_t = -10$. All the voltages have been normalized by thermal voltage U_T.

$\delta Q_D \approx C_{ox}\delta V_G$. So we have $\delta Q_S/\delta V_G \approx (Q_D/Q_S)C_{ox}$. As $Q_D > Q_S$ in this situation (because the source end has higher doping), we have $\delta Q_S/\delta V_G > C_{ox}$, which is only possible, if the channel potential goes negative and adds in the gate voltage. Depending on the profile and drain voltage, the peak in C_{DG} vs V_{GS} curve may even increase above C_{ox} in presence of the gate voltage [5]. Fig. 5.1(b) shows the C_{DG} for $\Delta v_t = -10$. As the doping difference between the source and drain is now much less, the peak is less pronounced. From this discussion, it should be clear that if one chooses sufficiently large drain voltage to prevent the drain region entering into strong inversion before the source region, the peak in C_{DG} should disappear. Our numerical simulation $\Delta v_t = -10, v_d = 10$ represents this situation in Fig. 5.1(b). Fig. 5.3 shows the plot for C_{SG}, where our partitioning scheme and exact numerical solution also show perfect agreement. Fig. 5.4 shows a comparison with device simulation for C_{DG} and C_{SG}, where we also obtain a satisfactory agreement. The discrepancy is due to the approximations that are inherent in the expression of $g(x, V_0, V_G)$ (charge sheet approximation, inversion charge linearization etc.)

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(a)



(b)

Figure 5.4: Model validation on device simulation: (a) Drain-to-gate capacitance C_{DG} vs V_{GS} for $V_{DS} = 0$ and 0.5V (b) Source-to-gate capacitance C_{SG} vs V_{GS} for $V_{DS} = 0$ and 0.5V.

Although we are able to provide a considerable simplification over the existing approach [6, 4], work needs to be done to get a more simpler approximate compact models [2] depending on specific models of $g(x, V_0, V_G)$. This new insight and a correspondence with existing Ward-Dutton partitioning may be helpful for this purpose. Even if a simplification of our exact formulation is done, the model will be a QS capacitance based model which may have some problems [15].

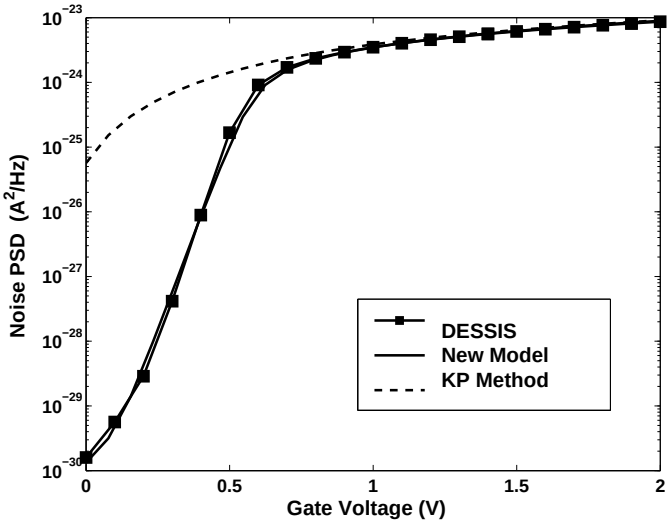


Figure 5.5: Plot of drain thermal noise power spectral density (PSD) vs. gate voltage for LAMOS at $V_{DS} = 0$. The KP method grossly overestimates the noise current especially at low gate voltages. The dotted line represents noise calculated using KP method, which is valid for conventional MOSFET and states that the drain noise current PSD is proportional to total inversion charge in the channel. We see that this approach grossly overestimates the noise current especially at low gate voltages. This suggests that the noise properties of LAMOS is considerably different from conventional MOSFET. Our proposed model correctly captures the trend and gives very good match with device simulation.

5.5 Noise Modeling in the Lateral Non-uniformly doped MOSFET

As the efforts for a compact LDMOS model [16, 17, 18, 19] for standardization is going on by the Compact Model Council (CMC) [20], the noise modeling has been set a mandatory feature for an industry standard compact model. The MOSFET noise models are either built on Klaassen-Prins (KP) [11] or some equivalent methods [21, 22, 23, 24], which are all denoted here as KP method. Fig. 5.5 shows the plot of the drain current power spectral density (PSD) in equilibrium versus the gate voltage obtained from a 2-D device noise simulation (DESSIS) and the noise PSD predicted by KP method. It shows that even in equilibrium, the KP method grossly overestimates the noise at low value of gate voltages, which reveals the importance of a new noise calculation method. Starting from a Langevin description [24], we will develop an analytical noise model for LAMOS [10, 25] and explain why the KP method fails.

5.5.1 Development of the noise model

Let's start with the basic principles of the Langevin method as shown in Fig. 5.6. The current at any position in the MOSFET channel has two components. One component is set up by the voltage perturbation caused by the noise source (which can be thought of flowing through the resistances) and other one is the noise current itself (which is represented by the noisy current source $\delta i_n(x)$). Δi_d is the total noise current flowing through the channel and is constant along

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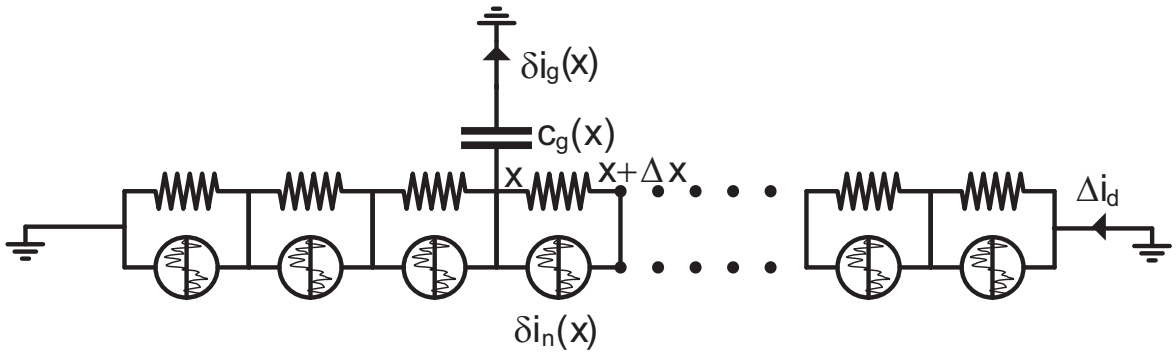


Figure 5.6: Illustration of the noise calculation by using a Langevin approach. $\delta i_n(x)$ is the noise current source, Δi_d is the terminal noise current, $\Delta i_g(x)$ is induced gate noise, which originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$. The current at any position has two components. One component is set up by the voltage perturbation caused by the noise source (which can be thought of flowing through the resistances) and other one is the noise current itself (which is represented by the noisy current source $\delta i_n(x)$). Δi_d is the total noise current flowing through the channel and is constant along the channel. The induced gate current noise $\Delta i_g(x)$ originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$ and lies in quadrature with the drain current noise.

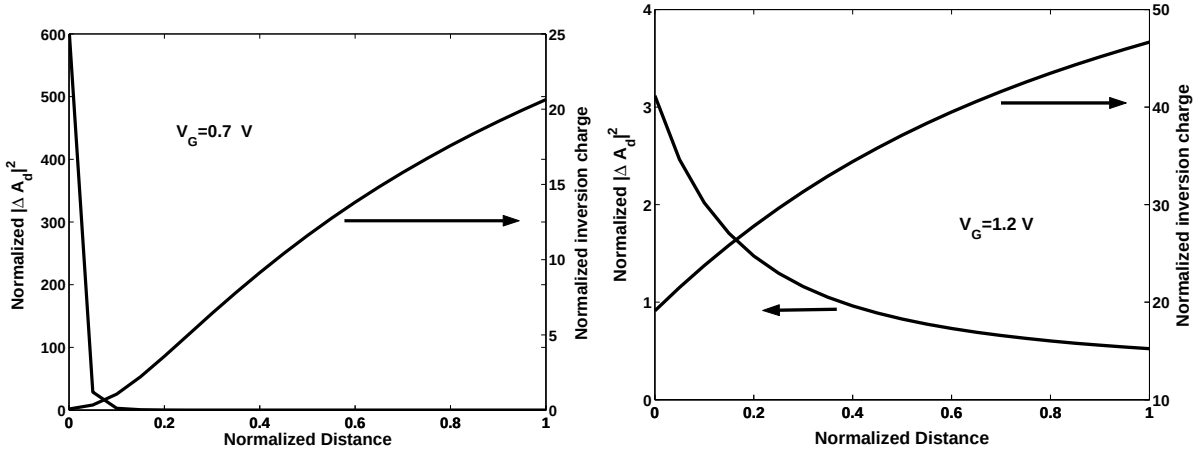
the channel. The induced gate current noise $\Delta i_g(x)$ originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$ and lies in quadrature with the drain current noise.

The basic mathematical steps have been derived in Appendix B. Note that, to keep our analysis general, mobility degradation has also been taken into account. One of the essential steps in noise calculation is to find a proper small-signal description of the transport equation as shown in (B.2)-(B.8). One of the interesting results is (B.7), which illustrates the impact of the mobility degradation in the chain rule. Instead of trying to solve (B.8) directly, the 'trick' we apply is to rewrite (B.8) as a linear ODE with respect to the quantity $g(x, V, \frac{dV}{dx}) \cdot v$ with an integration factor $R(x)$ (see (B.9)). Using $R(x)$, we put the perturbed channel potential v inside a proper differential (B.10). Next we use the facts that total noise current Δi_d is constant along the channel and v vanishes at the boundaries to obtain drain current (B.13). Please note that when there is no lateral asymmetry, $\partial g(x, V, \frac{dV}{dx})/\partial x$ vanishes and one get back to the noise expression of [24]. In addition when there is also no mobility degradation, we get back the conventional KP equation [11]. To obtain the gate current (B.14), we apply a variant of the techniques developed in [24]. Once the current is obtained, PSDs can be easily calculated (see (B.18)-(B.22)).

5.5.2 Result and discussion

Let's first discuss, why conventional KP based methods fail for LAMOS. If we integrate (B.8) (as done in the original derivation [11]), the presence of lateral asymmetry generates an additional term, which depends on the profile of perturbed channel potential v. This fact drastically changes the so called vector impedance field (IF) [24, 26] of the device. Eq. (B.13) reveals that the contribution to the terminal drain noise from any point gets determined by the product of two terms. First one is the IF for drain, ΔA_d (see (B.16)), which represents the noise propagation

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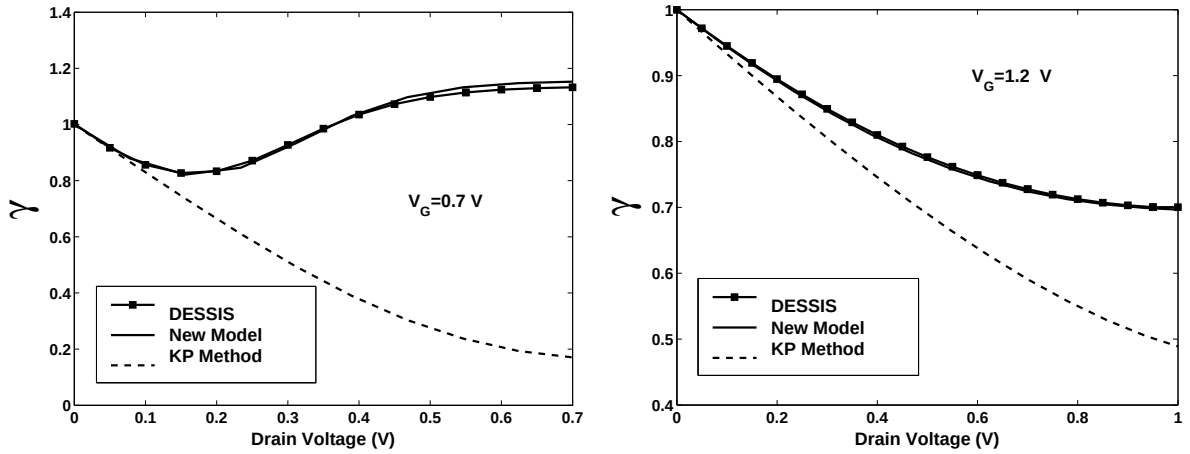


(a) (b)

Figure 5.7: Profile of squared drain IF (normalized with respect to the inverse of channel length) and inversion charge density (normalized by $C_{ox}U_T$) at $V_{DS} = 0$ (a) for low gate voltage ($V_G = 0.7$ V) and (b) for high gate voltage ($V_G = 1.2$ V). The PSD of the local noise source is proportional to the inversion charge. For normal MOSFET the normalized IF is equal to 1 but it is peaked near the source for lateral MOSFET. This considerably changes the noise behavior of LA MOSFET.

and the second term is the local noise source, whose PSD is proportional to the inversion charge (see (B.22)). Fig. 5.7 shows the plot of IF and inversion charge density versus normalized position. For a conventional MOSFET, IF is independent of position and equal to the inverse of the channel length [24, 27]. But the lateral asymmetry causes ΔA_d to highly peak near the source end and this effect is much more prominent at low gate voltages (Fig. 5.7(a)). As the source end is highly doped compared to the drain end, the inversion charge towards the drain end is much higher. These immediately reveal that KP grossly overestimates the noise current because it assigns the same weight to both strongly inverted region near the drain and weak/moderately inverted region near the source. Whereas in reality, the weak/moderately inverted region near the source gets a much higher weight and dominates the noise behavior. As the gate voltage increases, ΔA_d becomes less sharply peaked and also the difference between drain and source end charge decreases (Fig. 5.7(b)). Therefore, at high gate voltages KP can give an 'order of magnitude' kind of estimate (Fig. 5.5). The reason for the sharp peaking of the IF mathematically follows from (B.11). At low gate voltages, the value of $g(x, V, E)$ at source end will be very low, therefore the factor inside the exponential present in ΔA_d is very high, which causes this sharp peak. At higher gate voltages the value of $g(x, V, E)$ near the source is large so the exponential decays slowly. A 'crude' physical reasoning of this behavior is the following: if we lump the effect of distributed doping into two transistors, at low gate voltages the transistor near the source end will be weakly inverted and transistor near drain end will be strongly inverted. As the weakly inverted transistor has a much higher resistance and noise voltage (which, as a first order approximation, is proportional to the resistance), it follows that the noise current of the total combination will be determined by the weakly inverted transistor. In order to validate our theory, we made extensive comparison with ISE-DESIS, which calculates noise using a 2-D

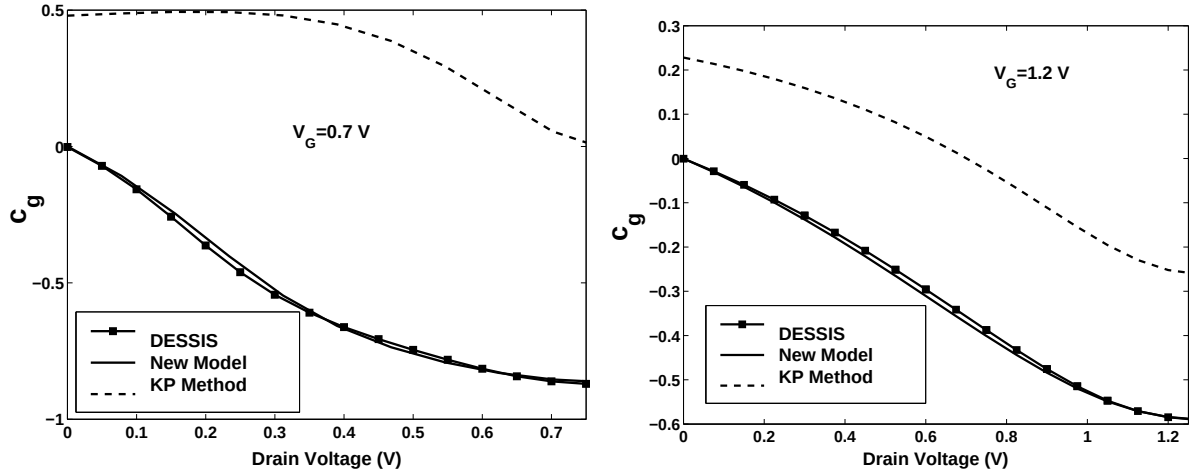
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(a) (b)

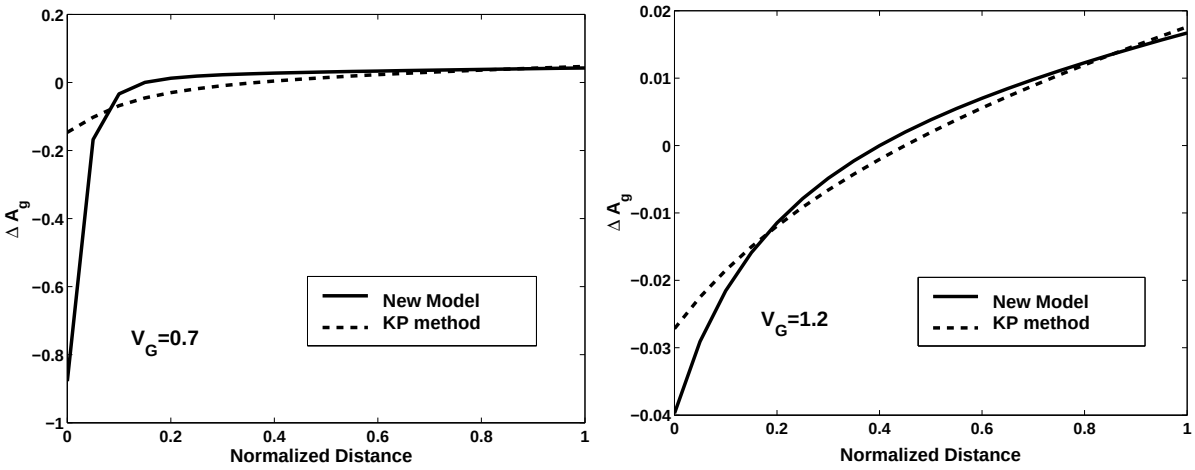
Figure 5.8: Model validation on numerical device simulation (DESSIS): Plot of γ versus drain voltage (a) at low gate voltage ($V_G = 0.7$ V) and (b) at high gate voltage ($V_G = 1.2$ V). At low gate voltage the shape can not be captured by KP method.

Greens function method. The structure simulated has a source doping of 5×10^{17} cm^{-3} and a drain doping of 1×10^{16} cm^{-3}, channel length of 2 μm, width of 1 μm, and a oxide thickness of 8 nm. Fig. 5.5 shows that our model is in close agreement with the device noise simulation in equilibrium. In order to check the bias dependence, we plot the noise factor γ (see (B.23)) as a function of drain voltage in Fig. 5.8. As an increase in drain voltage always decreases the total charge, the KP method can only predict a monotonically decreasing behavior of γ but both TCAD and our model predicts a minimum at low gate voltages (Fig. 5.8(a)) and our model satisfactorily matches the TCAD. The valley appears because the drain voltage also influences ΔA_d in a complicated way. Fig. 5.8(b) shows the same plot at high gate voltage, where we get back the expected monotonic decrease. In order to validate our induced gate noise modeling approach, we plot the correlation between drain and induced gate noise, c_g (see (B.24)), as function of drain voltage. Fig. 5.9(a) and Fig. 5.9(b) show the plots of c_g for low and high gate voltages respectively and our model again gives a very good match. Note that this term also behaves considerably different from conventional MOSFET where c_g saturates to 0.6 at weak inversion and to 0.4 at strong inversion [28, 29]. It is very interesting to note that KP based methods [24, 30, 31] for induced gate noise produces even a sign error in the correlation coefficient. This can be understood by noticing that the induced gate current changes sign as one moves from source to drain [24]. Fig. 5.10 shows the profile of IF for induced gate current ΔA_g (see (B.17)). Here also the conventional method incorrectly puts a lower weight to the source end, and as the charge is much higher near drain end, the total contribution gets dominated by the drain end. But in reality, as actual IF plots show, the gate noise gets dominated by the source end. As IF changes sign from source to drain, it is evident that KP method will cause a sign error.



(a) (b)

Figure 5.9: Model validation on numerical device simulation (DESSIS): Plot of the imaginary part of c_g versus drain voltage at (a) low gate voltage ($V_G = 0.7$ V) and (b) at high gate voltage ($V_G = 1.2$). KP method is totally incapable of predicting the behavior and even gives a wrong sign.



(a) (b)

Figure 5.10: Model validation on numerical device simulation (DESSIS): Profile of impedance field for gate current (at $V_{DS} = 0$) at (a) low gate voltage ($V_G = 0.7$ V) and (b) high gate voltage ($V_G = 1.2$ V). For gate impedance field also, KP underestimates the value at source end. As ΔA_g changes sign from source to drain, this underestimation gives a sign error in the correlation coefficient.

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5.6 Conclusion

In this chapter, we discussed the *limitation of the Ward-Dutton partitioning scheme* with focus on lateral non-uniformly doped MOSFET. We showed the *existence of the small-signal partitioning scheme* for the situation when lateral asymmetry can be present in the MOSFET channel. The concept of the small signal partitioning is then successfully used to define the partitioning of perturbed charge from which the capacitances are calculated. This development provides a simple way of calculating capacitances. The proposed development was validated on the numerical device simulation and showed good results. As failure of Ward-Dutton scheme makes the concept of terminal charge invalid, the future compact modeling methodologies may undergo major changes. This new insight and a correspondence with existing Ward-Dutton partitioning will be helpful for developing simpler compact models for high voltage MOSFETs.

For the first time, *a general analytical noise modeling methodology* accounting for both lateral asymmetry and field dependent mobility was presented. This methodology is applicable to any kind of noise mechanism. The model was validated on the numerical device simulation and it was also explained why the noise properties in presence of lateral asymmetry are drastically different from conventional MOSFET.

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Chapter 6

Conclusion

The major achievements of this work can be summarized as follows:

I. EKV based General High Voltage MOSFET Model

A *general* High Voltage MOSFET model based on the EKV model as a core and new bias dependent drift resistance was developed. The model performance was demonstrated for three industrial devices: VDMOS, bulk-LDMOS and SOI-LDMOS. The model correctly reproduces the special effects of high voltage devices like the quasi-saturation and self-heating effect, and is highly scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. The model shows good results for entire DC bias range and good behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics) and Cadence's Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use. The model fulfils all the accuracy target required by the industry for high voltage MOSFET models.

II. Compact Modeling of Lateral Non-uniform doping

A *novel* charge based compact analytical model for lateral non-uniformly doped MOSFET was developed in this chapter. The model is developed using charge based EKV formalism. The major impact of the lateral non-uniform doping was seen on the capacitances, whose modeling has been a daunting task till now as expressions become non-integrable and non-implicit for current and charges. The inversion charge linearization paved the way to approximate the surface pinch-off potential across the channel. This led to develop integrable expressions for current and then charges. The inversion and gate charge in this model have clear dependence on the drain current, which is not the case in the conventional MOSFET models. Although this model was developed primarily for high voltage MOS devices, the lateral asymmetric channel devices have also demonstrated good behavior in deep sub-micron devices for higher performance in analog, RF and mixed signal design. In fact, lateral non-uniform doping is inherent in halo-doped nano-MOSFETs.

The proposed model was used for modeling of high voltage devices with a lateral doping gradient using an appropriate drift model. To the best of our knowledge, *this is the first time,*

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the modeling of lateral non-uniform doping has been implemented in any high voltage compact model. The model shows good behavior for all capacitances as well as for DC, when compared with device simulation and measurements. The position of the capacitance peaks as well as their amplitude are correctly simulated by the model. The major impact of the proposed model is on the accuracy improvement of high voltage MOSFET models especially during transient operations (i.e. modeling of the bias-dependent peaks and slopes of device capacitances).

III. Partitioning Scheme and Noise Modeling in LAMOS

The limitation of the Ward-Dutton partitioning was explained. The existence of the small-signal partitioning scheme for the lateral non-uniformly doped MOSFET was developed. The concept of the small signal partitioning was successfully used to define the partitioning of perturbed charge from which the capacitance were calculated. This development provided a simple mean of evaluating capacitances of lateral non-uniformly doped MOSFET. It was evident, as failure of Ward-Dutton scheme makes the concept of terminal charge invalid, the future compact modeling methodologies may undergo major changes. This new insight and a correspondence with existing Ward-Dutton partitioning will be helpful for developing simpler compact models for high voltage MOSFETs. Also, for the first time, a general analytical noise modeling methodology accounting for both lateral asymmetry and field dependent mobility was presented. This methodology is applicable to any kind of noise mechanism. It was also explained why the noise properties in presence of lateral asymmetry are drastically different from conventional MOSFET.

The research work in this thesis has been successful in solving several problems related to high voltage MOS modeling. Still there are several things which should be improved or solved for a better high voltage MOS model. Following is the list of tasks which needs to be done in future to get high performance HVMOS model:

➤ Length Scaling in Lateral Non-uniformly doped transistor
➤ Noise modeling and implementation in HVMOS
➤ Simplified partitioning scheme for Lateral Non-uniformly doped transistor
➤ Charge or surface potential based modeling of drift region
➤ Accurate modeling of the overlap capacitance in the drift region

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Appendix A

Solutions of transcendental equations of ψ_p, q_s and q_d

A.1 Evaluation of ψ_p

The transcendental equation for ψ_p in normalized form can be rewritten from (5.6) as

$$v_g - v_{fb} = \psi_p + sign(\psi_p)\gamma\sqrt{e^{-\psi_p} + \psi_p - 1} \tag{A.1}$$

where $\psi_p = \frac{\Psi_P}{U_T}$, $v_{fb} = \frac{V_{FB}}{U_T}$ and $\gamma = \frac{\Gamma}{U_T}$ are in the normalized forms. A simple routine for approximation of ψ_p has been developed to get the solution of this transcendental equation given below.

$$\psi_{p0} = \left[\frac{v_g - v_{fb}}{2} - 3\left(1 + \frac{\gamma}{\sqrt{2}}\right)\right] + \sqrt{\left[\frac{v_g - v_{fb}}{2} - 3\left(1 + \frac{\gamma}{\sqrt{2}}\right)\right]^2 + 6(v_g - v_{fb})} \tag{A.2}$$

Then

$$\psi_p = \begin{cases} -ln\left[1 - \psi_{p0} + \left(\frac{v_g - v_{fb} - \psi_{p0}}{\gamma}\right)^2\right], & \text{if } v_g < v_{fb}; \\ \left[\sqrt{v_g - v_{fb} - (1 - e^{-\psi_{p0}}) + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 + \left(1 - e^{-\psi_{p0}}\right), & \text{otherwise} \end{cases} \tag{A.3}$$

A.2 Evaluation of q $(= q_s$ or $q_d)$

The transcendental equation for q can be rewritten from (4.12) or (4.13) as

$$2q + ln(q) = v_p - v_{ch} \tag{A.4}$$

where q and v_{ch} can be "q_s and v_s" or "q_d and v_d". A simple routine for approximation of q has been developed to get the solution of this transcendental equation given below.

$$v = v_p - v_{ch} \tag{A.5}$$

if $v > -0.6$

$$\begin{aligned} q_0 &= \frac{1}{4}\left[v - 1.4 + \sqrt{v(v - 0.394036) + 9.662671}\right] \\ \delta_0 &= \frac{v - [2q_0 + ln(q_0)]}{2q_0 + 1} \\ q &= q_0\left[1 + \delta_0(1 + 0.07\delta_0)\right] \end{aligned} \tag{A.6}$$

otherwise

$$\begin{aligned} q_0 &= e^{\frac{1}{2}\left[v - 0.201491 - \sqrt{v(v + 0.402982) + 2.446562}\right]} \\ \delta_0 &= \frac{v - [2q_0 + ln(q_0)]}{2q_0 + 1} \\ q &= q_0\left[1 + \delta_0(1 + 0.483\delta_0)\right] \end{aligned}$$

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Appendix B

Noise Modeling of LAMOS

The channel current can be written as

$$I(x) = g(x, V, E)E \tag{B.1}$$

where $g(x, V, E) = W\mu(x, E)Q_i(x, V)$ and $E = \frac{dV}{dx}$. Here Q_i is the inversion charge, V is the channel potential and E is the electric field at any position x in the channel. W is the width of the device. Fig. 5.6 can be mathematically represented as

$$I(x) + i_d(x) = g\left(x, V + v, \frac{d(V + v)}{dx}\right)\frac{d(V + v)}{dx} + \delta i_n(x) \tag{B.2}$$

The perturbation analysis of (B.2) in the similar way as in section 5.3.1 yields

$$i_d(x) = \left(g(x, V, E) + \frac{\partial g(x, V, E)}{\partial E}\frac{dV}{dx}\right)\frac{dv}{dx} + \left(\frac{\partial g(x, V, E)}{\partial V}\frac{dV}{dx}\right)v + \delta i_n(x) \tag{B.3}$$

The impact of lateral asymmetry and mobility degradation on $g(x, V, E)$ can be written as

$$\frac{dg(x, V, E)}{dx} = \frac{\partial g(x, V, E)}{\partial x} + \frac{\partial g(x, V, E)}{\partial V}E + \frac{\partial g(x, V, E)}{\partial E}\frac{dE}{dx} \tag{B.4}$$

It should be noted that the extra term $\frac{\partial g(x,V,E)}{\partial x}$ appears due to lateral asymmetry while $\frac{\partial g(x,V,E)}{\partial E}$ term appears due to mobility degradation. In conventional MOSFET, both of these terms would be zero.

At this point it is important to recognize that we have additional constraint on $\frac{dE}{dx}$ from the fact that $\frac{dI}{dx} = 0$. Thus, as E and $\frac{dE}{dx}$ are not independent because the unperturbed current is constant, we have from (B.1)

$$\frac{dI}{dx} = 0 = \frac{dg(x, V, E)}{dx}E + g(x, V, E)\frac{dE}{dx} \tag{B.5}$$

or

$$\frac{dE}{dx} = -\frac{\left(\frac{dg(x,V,E)}{dx}\right)E}{g(x, V, E)} \tag{B.6}$$

In the presence of mobility degradation, the "chain rule" becomes

$$\frac{dg(x,V,E)}{dx} = \frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\left(\frac{\partial g(x,V,E)}{\partial V}E + \frac{\partial g(x,V,E)}{\partial x}\right) \tag{B.7}$$

Using (B.7), the final expression of $i_d(x)$ from (B.3) can be written as

$$i_d(x) = \left[\frac{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}{g(x,V,E)}\right]\frac{d}{dx}\left[g(x,V,E)v\right] - \frac{\partial g(x,V,E)}{\partial x}v + \delta i_n(x) = \Delta i_d \tag{B.8}$$

where Δi_d is the constant noise current flowing through the channel. Rearranging (B.8) as a ODE of gv

$$\frac{d}{dx}\left[g(x,V,E)v\right] - \left(\frac{\frac{\partial g(x,V,E)}{\partial x}}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right)\left[g(x,V,E)v\right] = \frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\left(\Delta i_d - \delta i_n(x)\right) \tag{B.9}$$

Using integration factor $R(x)$, the above ODE can be written as

$$\frac{d[R(x)g(x,V,E)v]}{dx} = f(x)\left(\Delta i_d - \delta i_n(x)\right) \tag{B.10}$$

where

$$R(x) = \exp\left[-\int_0^x \left(\frac{\frac{\partial g(x,V,E)}{\partial x}}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right)dx\right] \tag{B.11}$$

and

$$f(x) = \left[\frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right]R(x) \tag{B.12}$$

As v vanishes at the 0 and L (L is the length of the device), the integration of (B.10) gives

$$\Delta i_d = \frac{\int_0^L f(x)\delta i_n(x)dx}{\int_0^L f(x)dx} \tag{B.13}$$

The expression of Induced gate noise can be written as

$$\Delta i_g = -j\omega W\frac{\int_0^L f(x)\left(\int_0^L f(x_1)(\lambda(x_1) - \lambda(x))dx_1\right)\delta i_n(x)dx}{\int_0^L f(x)dx} \tag{B.14}$$

where Δi_g is the total gate noise current (integral of $\delta i_g(x)$ in Fig. 5.6) and

$$\lambda(x) = \int_0^x \frac{\partial Q_g}{\partial V}\frac{1}{R(x)g(x,V,E)}dx \tag{B.15}$$

Q_g is the gate charge density at any position in the channel.

The impedance fields for drain and gate respectively are obtained as

$$\Delta A_d = \frac{f(x)}{\int_0^L f(x)dx} \tag{B.16}$$

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$$\Delta A_g = -j\omega W \left[\frac{f(x)}{\int_0^L f(x)dx}\right] \left[\int_0^L f(x_1)(\lambda(x_1) - \lambda(x))dx_1\right] \tag{B.17}$$

The expressions of power spectral densities (PSD) are obtained as

Drain PSD:

$$S_{I_D^2} = \int_0^L |\Delta A_d|^2 S_{\delta i_n^2} dx \tag{B.18}$$

Gate PSD:

$$S_{I_G^2} = \int_0^L |\Delta A_g|^2 S_{\delta i_n^2} dx \tag{B.19}$$

Drain-Gate PSD:

$$S_{I_D I_G} = \int_0^L \Delta A_d \Delta A_g S_{\delta i_n^2} dx \tag{B.20}$$

where $S_{\delta i_n^2}$ is the power spectral density (PSD) of the elementary noise current δi_n [1]. Assuming the noise sources are spatially uncorrelated, we have

$$\overline{\delta i_n(x_1)\delta i_n(x_2)} = S_{\delta i_n^2}\delta(x_1 - x_2) \tag{B.21}$$

where the local noise PSD for thermal noise can be expressed as

$$S_{\delta i_n^2} = 4 \cdot q \cdot W \cdot Q_i \cdot D_n \cdot \Delta f \tag{B.22}$$

where D_n is the noise diffusivity [1]. For simple electron mobility model this definition of $S_{\delta i_n^2}$ reduces to the one used in [2] i.e. $S_{\delta i_n^2} = 4kT_L g \Delta f$, where T_L is the lattice temperature and k is the Boltzmann's constant. Finally the noise parameters are obtained as

$$\gamma = \frac{S_{I_D^2}}{4kT_L g_{ds0}} \tag{B.23}$$

$$c_g = \frac{S_{I_D I_G}}{\sqrt{S_{I_D^2} S_{I_G^2}}} \tag{B.24}$$

where g_{ds0} is the drain to source conductance at $V_{DS} = 0$.

APPENDIX J

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Bibliography

[1] A. S. Roy and C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," *IEEE Transactions Electron Devices*, vol. 52, no. 4, pp. 611–614, Apr. 2005.

[2] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalisations of the Klaassen-Prins Equation for Calculating the Noise of Semiconductor Devices," *IEEE Transactions Electron Devices*, vol. 52, no. 11, pp. 2463– 2472, Nov. 2005.

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Appendix C

Curriculum Vitae

Name: **YOGESH SINGH CHAUHAN**
Date of Birth: 22^{nd} May, 1978
Nationality: Indian
Sex: Male
Languages: English, Hindi and French

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Professional Associations and Responsibilities
➢ Student Member of IEEE, USA
➢ Reviewer of IEEE Transactions on Electron Devices
➢ Reviewer of Solid State Electronics
➢ Former reviewer of IEEE International Conference on VLSI Design, India

Work Experience

EPFL, Lausanne, Switzerland	Designation: Research Engineer Duration: March, 2004 to July 2007 Responsibilities: Modeling of High Voltage MOSFETs
ST Microelectronics, Noida, India	Designation: Associate Design Engineer Duration: June, 2003 to Feb., 2004 Responsibilities: VLSI I/O Library Design and Validation on MAT10 quality
IIT Kanpur, India	Position: Teaching Assistant Duration: Aug., 2001 to Dec., 2002

Educational Qualifications

Master of Technology (M. Tech.)

Specialization	Microelectronics, VLSI and Display Technologies
Institute	Indian Institute of Technology (IIT), Kanpur, India
Year	April, 2003
Thesis Title	Design of Current Programmed Active Matrix Organic Light Emitting Diode Pixel Circuits

Bachelor of Engineering (B. E.)

Specialization	Electronics and Telecommunication Engineering
Institute	Shri Govindram Seksaria Institute of Technology and Science (SGSITS), Indore, India
Year	June, 2001

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Appendix D

List of Publications

Journal Publications:

1. K. Akarvardar, C. Eggimann, D. Tsamados, **Y. Chauhan**, G. C. Wan, A. M. Ionescu, R. T. Howe, and H.-S.P. Wong, "Analytical Modeling of the Suspended-Gate FET and Design Insights for Low Power Logic", accepted in IEEE Transactions on Electron Devices (TED).

2. Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. Declercq, and A. M. Ionescu, "An EKV-based High Voltage MOSFET Model with improved mobility and drift model", accepted in Solid State Electronics (SSE).

3. Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Compact Modeling of Lateral Non-uniform Doping in High-Voltage MOSFETs", IEEE Transactions on Electron Devices (TED), Vol. 54, No. 6, pp. 1527-1539, June 2007.

4. Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. Baguenier Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model inlcuding Quasi-Saturation and Self-Heating effect", Solid State Electronics (SSE), Vol. 50, Issues 11-12, pp. 1801-1813, Nov.-Dec. 2006.

5. C. Anghel, B. Bakeroot, **Y. S. Chauhan**, R. Gillon, C. Maier, P. Moens, J. Doutreloigne, and A. M. Ionescu, "New Method for Threshold Voltage Extraction of High Voltage MOSFETs based on Gate-to-Drain Capacitance Measurement", IEEE Electron Device Letters (EDL), Vol. 27, No. 7, pp. 602-604, July 2006.

Conference Publications:

1. Y. S. Chauhan, D. Tsamados, N. Abele, C. Eggimann, M. Declercq, and A. M. Ionescu, "Compact Modeling of Suspended Gate FET", accepted in IEEE International Conference on VLSI Design, Hyderabad, India, Jan. 2008.

2. Y. S. Chauhan, R. Gillon, M. Declercq, and A. M. Ionescu, "Impact of Lateral Non-uniform Doping and hot carrier degradation on Capacitance behavior of High-Voltage MOS-

FETs", IEEE European Solid-State Device Research Conference (ESSDERC), Munich, Germany, Sept. 2007.

3. D. Tsamados, **Y. S. Chauhan**, C. Eggimann, K. Akarvardar, H.S. Philip Wong, and A. M. Ionescu, "Numerical and analytical simulations of Suspended-Gate FET for ultra-low power inverters", IEEE European Solid-State Device Research Conference (ESSDERC), Munich, Germany, Sept. 2007.

4. K. Akarvardar, C. Eggimann, D. Tsamados, **Y. Chauhan**, G. C. Wan, A. M. Ionescu, and H.-S.P. Wong, "Analytical Modeling of the Suspended-Gate FET and Design Insights for Digital Logic", IEEE Device Research Conference (DRC), Bend, USA, June 2007.

5. W. Grabinski, T. Grasser, G. Gildenblat, G. Smit, M. Bucher, A. C. T. Aarts, A. Tajic, **Y. S. Chauhan**, A. Napieralski, T. A. Fjeldly, B. Iniguez, G. Iannaccone, M. Kayal, W. Posch, G. Wachutka, F. Pregaldiny, C. Lallement, L. Lemaitre, "MOS-AK: Open Compact Modeling Forum", (invited) International Workshop on Compact Modeling (IWCM), Yokohama, Japan, Jan. 2007.

6. Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling", IEEE International Conference on VLSI Design, Bangalore, India, Jan. 2007.

7. Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs", IEEE International Electron Devices Meeting (IEDM), San Francisco, USA, Dec. 2006.

8. A. S. Roy, **Y. S. Chauhan**, C. C. Enz, J.-M. Sallesse, "Noise Modeling in Lateral Asymmetric MOSFET", IEEE International Electron Devices Meeting (IEDM), San Francisco, USA, Dec. 2006.

9. Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete,"A Highly Scalable High Voltage MOSFET Model", IEEE European Solid-State Device Research Conference (ESSDERC), Montreux, Switzerland, Sept. 2006.

10. A. S. Roy, **Y. S. Chauhan**, J.-M. Sallesse, C. C. Enz, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in the Lateral Asymmetric MOST", IEEE European Solid-State Device Research Conference (ESSDERC), Montreux, Switzerland, Sept. 2006.

11. Y. S. Chauhan, C. Anghel, F. Krummenacher, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu and M. Declercq, "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor", IEEE International Symposium on Quality Electronic Design (ISQED), San Jose, USA, March 2006.

12. C. Anghel, **Y. S. Chauhan**, N. Hefyene and A. M. Ionescu, "A Physical Analysis of High

Voltage MOSFET Capacitance Behaviour", IEEE International Symposium on Industrial Electronics (ISIE), Dubrovnik, Croatia, June 2005.

13. B. Mazhari, **Yogesh S. Chauhan**, "Design of current-Programmed amorphous-Silicon AMOLED Pixel Circuit", The 8th Asian Symposium on Information Display (ASID), China, 2003.

14. B. Mazhari, **Yogesh S. Chauhan**, "A New Negative Feedback based poly-Silicon AMOLED Pixel Circuit with Highly Linear Transfer Characteristics", 10th International Display Workshop (IDW), Fukuoka, Japan, 2003.

Invited Presentation:

1. "A Compact Model for Circuit Simulation of High Voltage Lateral & Vertical DMOS Transistors", ROBUSPIC Power Device Workshop at 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Napoli, Italy, June 2006.

2. "The HV-EKV MOSFET Model", Compact Model Council (CMC) meeting, Boston, USA, May 2006.

APPENDIX J

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MSP430i204x, MSP430i203x, MSP430i202x Mixed-Signal Microcontrollers

1 Features

- Supply voltage range: 2.2 V to 3.6 V
- High-performance analog
  - MSP430i204x: Four 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
  - MSP430I203x: Three 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
  - MSP430I202x: Two 24-bit sigma-delta analog-to-digital converters (ADCs) with differential PGA inputs
- Ultra-low power consumption
  - Active mode (AM):
    All system clocks active
    275 µA/MHz at 16.384-MHz, 3.0 V, flash program execution (typical)
  - Standby mode (LPM3):
    Watchdog timer active, full RAM retention
    210 µA at 3.0 V (typical)
  - Off mode (LPM4):
    Full RAM retention
    70 µA at 3.0 V (typical)
  - Shutdown mode (LPM4.5):
    75 nA at 3.0 V (typical)
- Intelligent digital peripherals
  - Two 16-bit timers with three capture/compare registers each
  - Hardware multiplier supports 16-bit operations
- Enhanced universal serial communication interfaces (eUSCIs)
  - eUSCI_A0
    - Enhanced UART with automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - eUSCI_B0
    - Synchronous SPI
    - I^2C
- Flexible power management system
  - Integrated LDO with 1.8-V regulated core supply voltage
  - Supply voltage monitor with programmable level detection
  - Brownout detector
  - Built-in voltage reference
  - Temperature sensor
- Clock system
  - 16.384-MHz internal digitally controlled oscillator (DCO)
  - DCO operation with internal or external resistor
  - External digital clock source
- Development tools and software (also see Tools and Software)
  - EVM430-I2040S evaluation module (EVM) for metering
  - MSP-TS430RHB32A 100-pin target development board
  - MSP430Ware™ code examples
- Wake up from standby mode in 1 µs
- 16-bit RISC architecture, up to 16.384-MHz system clock
- Serial onboard programming, no external programming voltage needed
- Available in 28-pin TSSOP (PW) and 32-pin VQFN (RHB) packages
- Device Comparison summarizes the available family members
- Featured software and reference designs
  - Energy Measurement Design Center for MSP430 MCUs application software and frameworks
  - Digital Signal Processing (DSP) Library for MSP430 Microcontrollers software libraries
  - Single Phase and DC Embedded Metering reference design
  - Three Output Smart Power Strip reference design

2 Applications

- Metering
- Submetering
- Power monitoring and control
- Industrial sensors
- 1-phase AC and DC power monitoring
- 2-phase electronic meters
- Smart plugs
- Smart power strips
- Medical – multiple-parameter patient monitoring

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3 Description

The Texas Instruments MSP430i204x, MSP430I203x and MSP430I202x microcontrollers (MCUs) are part of the MSP430™ Metrology and Monitoring portfolio. The architecture and integrated peripherals, combined with five extensive low-power modes, are optimized to achieve extended battery life in portable and battery-powered measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430i204x MCUs include four high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

The MSP430I203x MCUs include three high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

The MSP430I202x MCUs include two high-performance 24-bit sigma-delta ADCs, two eUSCIs (one eUSCI_A module and one eUSCI_B module), two 16-bit timers, a hardware multiplier, and up to 16 I/O pins.

Typical applications for these devices include energy measurement, analog and digital sensor systems, LED lighting, digital power supplies, motor controls, remote controls, thermostats, digital timers, and hand-held meters.

The MSP430i204x, MSP430I203x and MSP430I202x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits include the EVM430-I2040S evaluation module (EVM) for metering and the MSP-TS430RHB32A 100-pin target development board. The Energy Measurement Design Center for MSP430 MCUs is provided as a rapid development tool that enables energy measurement on these devices. TI also provides free MSP430Ware™ software, which is available as a component of Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer. The MSP430 MCUs are also supported by extensive online collateral, training, and online support through the TI E2E™ support forums.

For complete module descriptions, see the MSP430i2xx Family User's Guide.

Device Information

(1)PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430i2041TPW	TSSOP (28)	9.7 mm × 4.4 mm
MSP430i2041TRHB	VQFN (32)	5 mm × 5 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 12.

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4 Functional Block Diagram

Figure 4-1 shows the functional block diagram for the MSP430i204x devices in the RHB package. For the functional block diagrams of all device variants and packages, see Section 9.2.

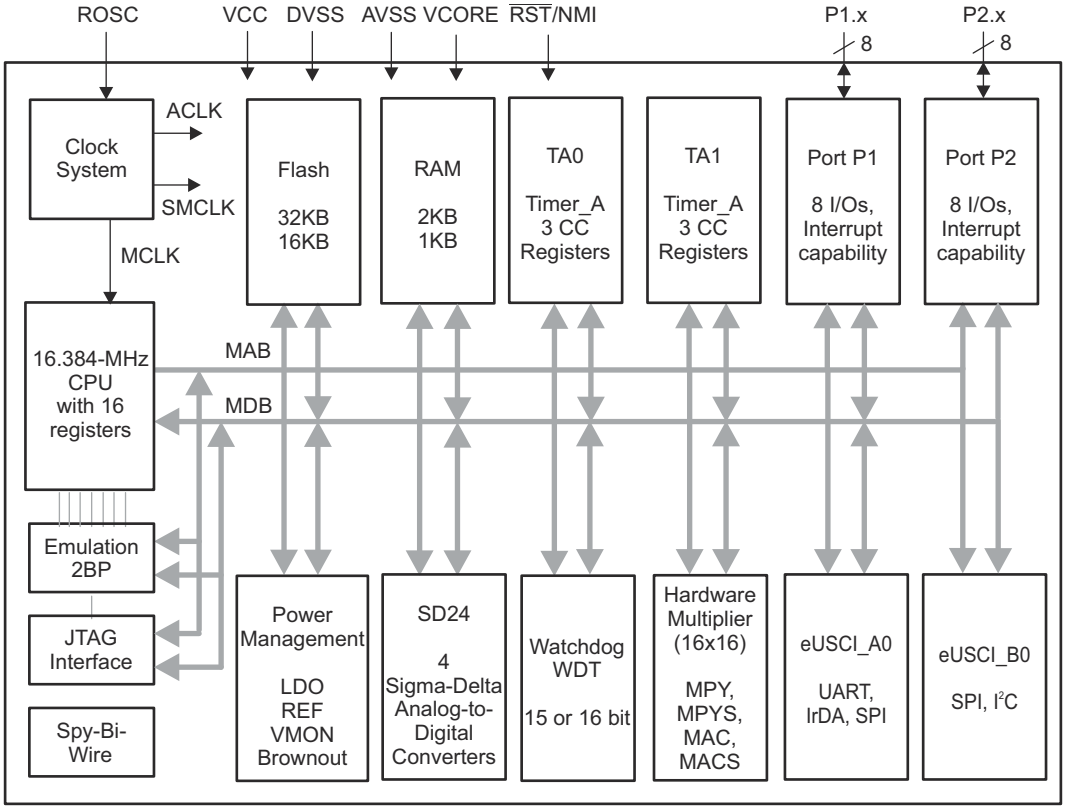


Figure 4-1. Functional Block Diagram – RHB Package – MSP430i204x

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision B to revision C

Changes from March 4, 2020 to March 16, 2021	Page
• Updated the numbering format for tables, figures, and cross references throughout the document	1
• Updated "Featured software and reference designs" in Section 1, *Features*	1

Changes from revision A to revision B

Changes from May 3, 2018 to March 3, 2020	Page
• Updated Section 1, *Features*	1
• Updated Section 3, *Description*	2
• Added 2 and 4 to the SD24GAINx options in the test conditions of the "Gain error" parameter in Section 8.7.7.5, *SD24 Performance, Internal Reference (SD24REFS = 1, SD24OSRx = 256)*	23
• Added 2 and 4 to the SD24GAINx options in the test conditions of the "Gain error" parameter in Section 8.7.7.6, *SD24 Performance, External Reference (SD24REFS = 0, SD24OSRx = 256)*	24
• Changed the MIN values for the $t_{HD,STA}$, $t_{SU,STA}$, $t_{HD,DAT}$, $t_{SU,DAT}$, and $t_{SU,STO}$ parameters in Section 8.7.8.6, *eUSCI (I^2C Mode) Timing*	30
• Updated descriptions and links in Section 10, *Applications, Implementation, and Layout*	61

Changes from the initial release to revision A

Changes from August 31, 2014 to May 2, 2018	Page
• Changed the list of applications in Section 2, *Applications*	1
• Added Section 6.1, *Related Products*	6
• Added typical conditions statements at the beginning of Section 8, *Specifications*	13
• Added SD24 input pins and AUXVCCx pins to exception list on "Voltage applied to pins" parameter, and added SD24 input pin limits in "Diode current at pins" parameter in Section 8.1, *Absolute Maximum Ratings*	13
• Added Section 8.2, *ESD Ratings*	13
• Added Section 8.6, *Thermal Resistance Characteristics*	15
• Changed the MAX value of the $t_{WAKE-UP-LPM4}$ parameter from 35 µs to 45 µs in Section 8.7.3.1, *Wake-up Times From Low Power Modes*	17
• Added the CAUTION that begins "The CPU will lock up if..." in Section 9.3, *CPU*	38

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6 Device Comparison

Table 6-1 summarizes the available family members.

Table 6-1. Device Comparison

DEVICE(1)	FLASH (KB)	SRAM (KB)	SD24 CONVERTERS	MULTIPLIER	Timer_A(2)	eUSCI_A: UART, IrDA, SPI	eUSCI_B: SPI, I²C	I/O	PACKAGE
MSP430i2041	32	2	4	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2040	16	1	4	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2031	32	2	3	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2030	16	1	3	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2021	32	2	2	1	3, 3	1	1	16	32 RHB
								12	28 PW
MSP430i2020	16	1	2	1	3, 3	1	1	16	32 RHB
								12	28 PW

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website at www.ti.com.

(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

MSP430 ultra-low-power sensing and measurement microcontrollers

One platform. One ecosystem. Endless possibilities.

Reference designs for MSP430i2041

Find reference designs leveraging the best in TI technology to solve your system-level challenges. All designs include a schematic, test data and design files.

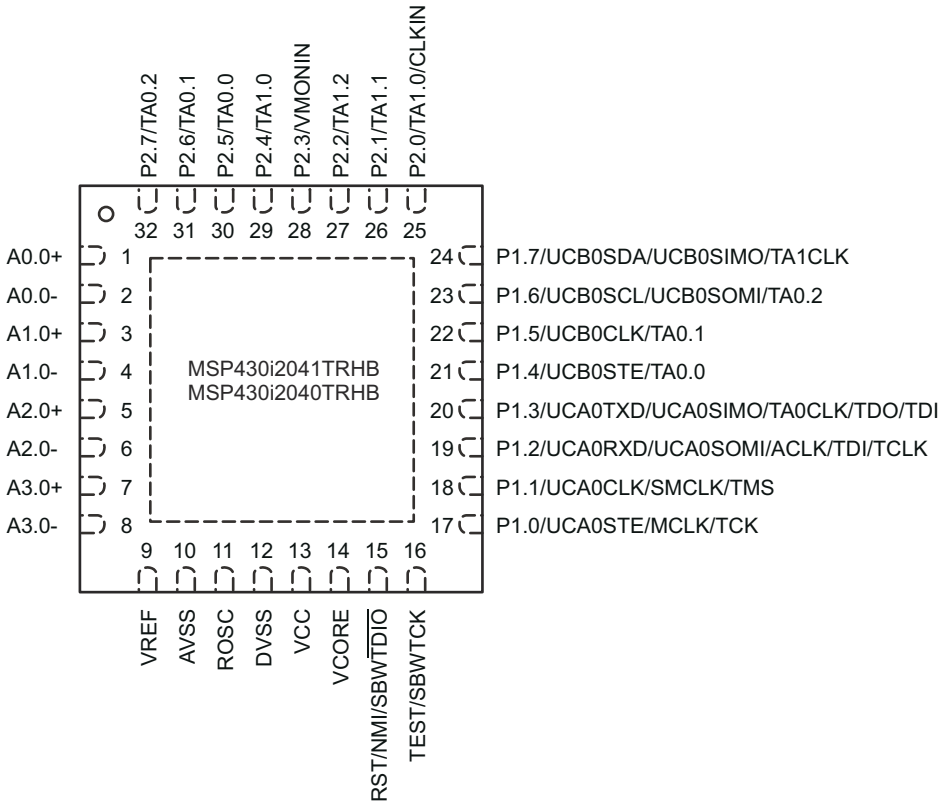
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7 Terminal Configuration and Functions

7.1 Pin Diagrams

Figure 7-1 shows the pin assignments for the MSP430i2041 and MSP430i2040 devices in the RHB package.



NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

Figure 7-1. 32-Pin RHB Package (Top View) – MSP430i2041, MSP430i2040

Figure 7-2 shows the pin assignments for the MSP430i2041 and MSP430i2040 devices in the PW package.

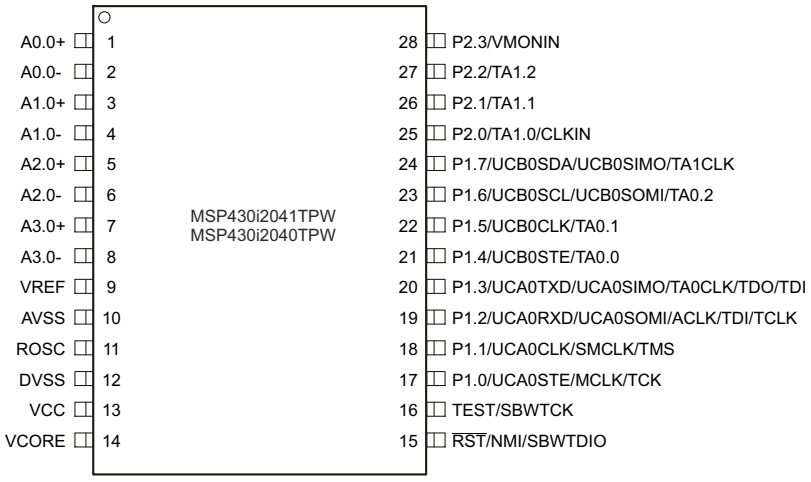
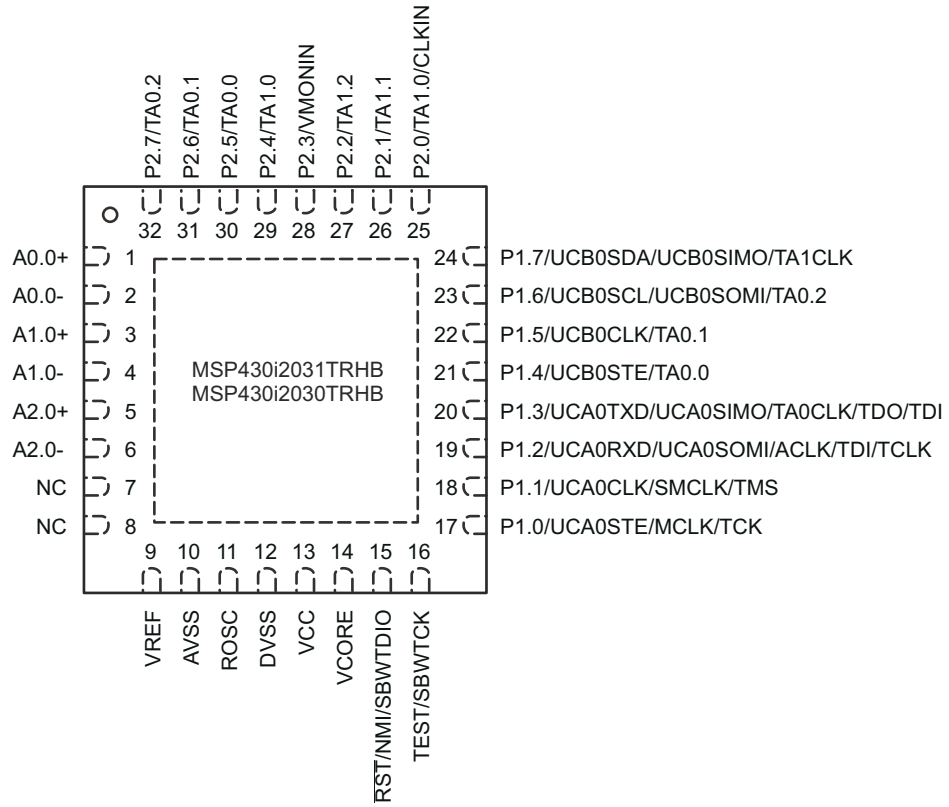


Figure 7-2. 28-Pin PW Package (Top View) – MSP430i2041, MSP430i2040

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Figure 7-3 shows the pin assignments for the MSP430i2031 and MSP430i2030 devices in the RHB package.

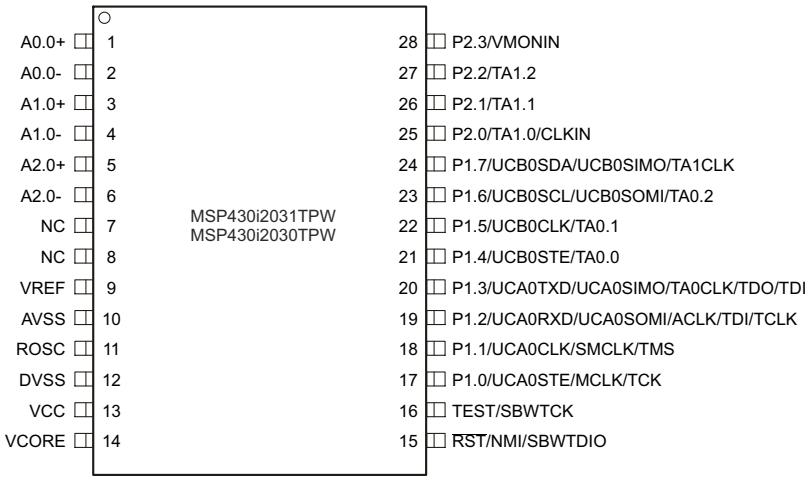


NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

NOTE: TI recommends connecting NC pins to AVSS.

Figure 7-3. 32-Pin RHB Package (Top View) – MSP430i2031, MSP430i2030

Figure 7-4 shows the pin assignments for the MSP430i2031 and MSP430i2030 devices in the PW package.



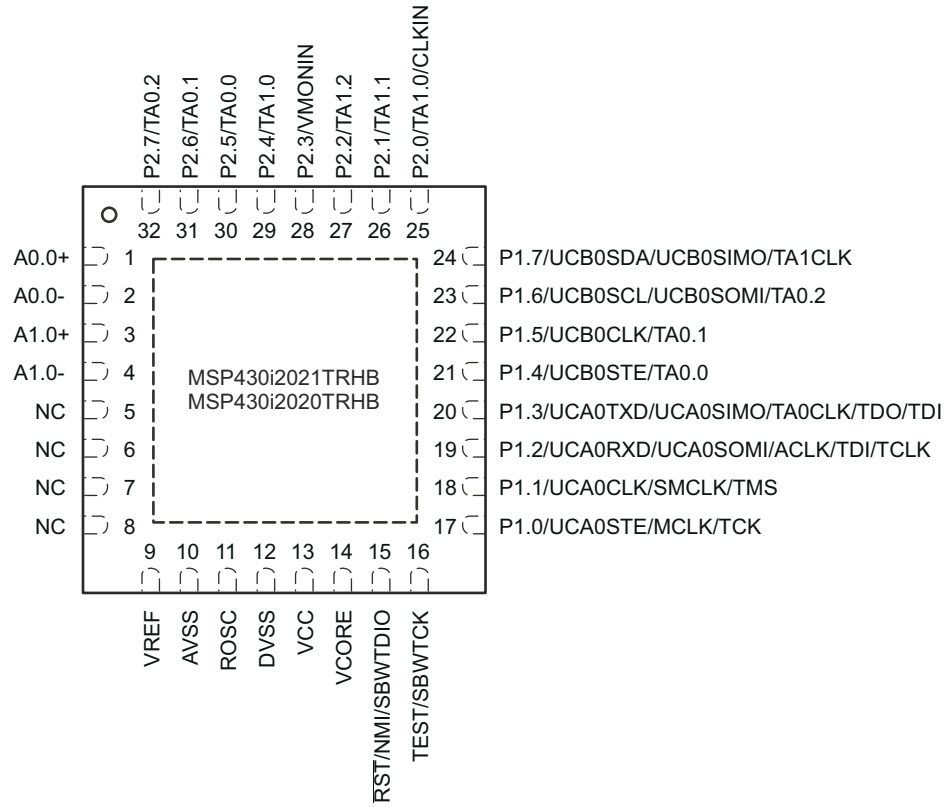
NOTE: TI recommends connecting NC pins to AVSS.

Figure 7-4. 28-Pin PW Package (Top View) – MSP430i2031, MSP430i2030

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Figure 7-5 shows the pin assignments for the MSP430i2021 and MSP430i2020 devices in the RHB package.

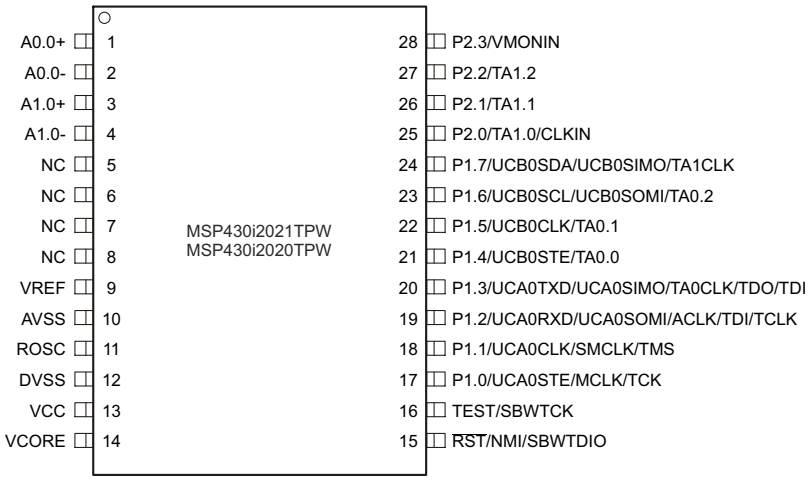


NOTE: TI recommends connecting the thermal pad on the RHB package to DVSS.

TI recommends connecting NC pins to AVSS.

Figure 7-5. 32-Pin RHB Package (Top View) – MSP430i2021, MSP430i2020

Figure 7-6 shows the pin assignments for the MSP430i2021 and MSP430i2020 devices in the PW package.



TI recommends connecting NC pins to AVSS.

Figure 7-6. 28-Pin PW Package (Top View) – MSP430i2021, MSP430i2020

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7.2 Signal Descriptions

Section 7.2 describes the signals for all device variants and package options.

Table 7-1. Signal Descriptions

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.[2]			
	PW	RHB		
A0.0+	1	1	I	SD24 positive analog input A0.0[3]
A0.0-	2	2	I	SD24 negative analog input A0.0[3]
A1.0+	3	3	I	SD24 positive analog input A1.0[3]
A1.0-	4	4	I	SD24 negative analog input A1.0[3]
A2.0+	5	5	I	SD24 positive analog input A2.0[3] [4]
A2.0-	6	6	I	SD24 negative analog input A2.0[3] [4]
A3.0+	7	7	I	SD24 positive analog input A3.0 [3] [4] [5]
A3.0-	8	8	I	SD24 negative analog input A3.0 [3] [4] [5]
VREF[6]	9	9	I	SD24 external reference voltage input
AVSS	10	10		Analog supply voltage, negative terminal
ROSC	11	11		External resistor pin for DCO. Connect recommended resistor between ROSC and AVSS for DCO operation in external resistor mode. Connect ROSC to AVSS while operating DCO in internal resistor mode.
DVSS	12	12		Digital supply voltage, negative terminal
VCC	13	13		Analog and digital supply voltage, positive terminal
VCORE [7]	14	14		Regulated core power supply (internal use only, no external current loading)
$\overline{\text{RST}}$/NMI/SBWTDIO	15	15	I/O	Reset or nonmaskable interrupt input. Spy-Bi-Wire test data input/output for device programming and test.
TEST/SBWTCK	16	16	I	Selects test mode for JTAG pins on P1.0 to P1.3. Spy-Bi-Wire test clock input for device programming and test.
P1.0/UCA0STE/MCLK/TCK	17	17	I/O	General-purpose digital I/O pin. eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI). MCLK output. JTAG test clock. TCK is the clock input port for device programming and test.
P1.1/UCA0CLK/SMCLK/TMS	18	18	I/O	General-purpose digital I/O pin. eUSCI_A0 clock input/output (direction controlled by eUSCI). SMCLK output. JTAG test mode select. TMS is used as an input port for device programming and test.
P1.2/UCA0RXD/UCA0SOMI/ ACLK/TDI/TCLK	19	19	I/O	General-purpose digital I/O pin. eUSCI_A0 UART receive data or eUSCI_A0 SPI slave out/master in (direction controlled by eUSCI). ACLK output. JTAG test data input or test clock input for device programming and test.
P1.3/UCA0TXD/UCA0SIMO/ TA0CLK/TDO/TDI	20	20	I/O	General-purpose digital I/O pin. eUSCI_A0 UART transmit data or eUSCI_A0 SPI slave in/master out (direction controlled by eUSCI). Timer external clock input TACLK for TA0. JTAG test data output port. TDO/TDI data output or programming data input terminal.
P1.4/UCB0STE/TA0.0	21	21	I/O	General-purpose digital I/O pin. eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI). Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output.

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Table 7-1. Signal Descriptions (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.[2]			
	PW	RHB		
P1.5/UCB0CLK/TA0.1	22	22	I/O	General-purpose digital I/O pin. eUSCI_B0 clock input/output (direction controlled by eUSCI). Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output.
P1.6/UCB0SCL/UCB0SOMI/ TA0.2	23	23	I/O	General-purpose digital I/O pin. eUSCI_B0 I^2C clock or eUSCI_B0 SPI slave out/master in (direction controlled by eUSCI). Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output.
P1.7/UCB0SDA/UCB0SIMO/ TA1CLK	24	24	I/O	General-purpose digital I/O pin. eUSCI_B0 I^2C data or eUSCI_B0 slave input/master output (direction controlled by eUSCI). Timer external clock input TACLK for TA1.
P2.0/TA1.0/CLKIN	25	25	I/O	General-purpose digital I/O pin. Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output. DCO bypass clock input.
P2.1/TA1.1	26	26	I/O	General-purpose digital I/O pin. Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output.
P2.2/TA1.2	27	27	I/O	General-purpose digital I/O pin. Timer TA1 CCR2 capture: CCI2A input, compare: Out2 output.
P2.3/VMONIN	28	28	I/O	General-purpose digital I/O pin. Voltage monitor input.
P2.4/TA1.0[8]	N/A	29	I/O	General-purpose digital I/O pin. Timer TA1 CCR0 capture: CCI0B input, compare: Out0 output.
P2.5/TA0.0[8]	N/A	30	I/O	General-purpose digital I/O pin. Timer TA0 CCR0 capture: CCI0B input, compare: Out0 output.
P2.6/TA0.1[8]	N/A	31	I/O	General-purpose digital I/O pin. Timer TA0 CCR1 compare: Out1 output.
P2.7/TA0.2[8]	N/A	32	I/O	General-purpose digital I/O pin. Timer TA0 CCR2 compare: Out2 output.

(1) I = input, O = output

(2) N/A = not available

(3) Short unused analog input pairs and connect them to analog ground (see Section 7.4 for recommendations on all unused pins).

(4) Not available on MSP430i2021 and MSP430i2020 devices.

(5) Not available on MSP430i2031 and MSP430i2030 devices.

(6) When the SD24 operates with the internal reference (SD24REFS = 1), the VREF pin must not be loaded externally. Connect only the recommended capacitor value (C_{VREF}) from the VREF pin to AVSS (see Section 8.7.7.2).

(7) VCORE is for internal use only. No external current loading is possible. Connect VCORE to only the recommended capacitor value (C_{VCORE}) (see Section 8.3).

(8) These pins are not available on the 28-pin PW package. Program these four pins to output direction and drive value 0 in software.

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7.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 9.11.

7.4 Connection of Unused Pins

Table 7-2 lists the correct termination of all unused pins.

Table 7-2. Connection of Unused Pins

PIN(1)	POTENTIAL	COMMENT
AVCC	DVCC	
AVSS	DVSS	
VREF	Open	
ROSC	AVSS	Connect the ROSC pin to AVSS when the DCO is used in internal resistor mode.
Px.0 to Px.7	Open	Set to port function, output direction.
Ax.0+ and Ax.0-	AVSS	Short unused analog input pairs and connect them to analog ground.
$\overline{\text{RST}}$/NMI	DVCC or VCC	47-kΩ pullup with 10 nF (or 2.2 nF(2)) pulldown
TEST	Open	This pin always has an internal pulldown enabled.
P1.3/TDO P1.2/TDI P1.1/TMS P1.0/TCK	Open	The JTAG pins are shared with general-purpose I/O function (P1.x). If these pins are not used, set them to port function and output direction. When used as JTAG pins, leave these pins open.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 unused pin connection.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

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8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage applied at VCC		–0.3	4.1	V
Voltage applied to pins	All pins except VCORE(3), ROSC(4), and SD24 input pins (A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-)(5)	–0.3	V_{CC} + 0.3	V
Diode current at pins	All pins except SD24 input pins (A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-)		±2	mA
	A0.0+, A0.0-, A1.0+, A1.0-, A2.0+, A2.0-, A3.0+, A3.0-(6)		2	
Maximum junction temperature, $T_{J,MAX}$			115	°C
Storage temperature, T_{stg} (7)		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are referenced to V_{SS}.

(3) VCORE is for internal device use only. Do not apply external DC loading or voltage at VCORE.

(4) Do not apply external DC loading or voltage at ROSC. Connect the recommended resistor at ROSC using the DCO in external resistor mode. Connect ROSC to AVSS when operating the DCO in internal resistor mode.

(5) See Section 8.7.7.1 for SD24 specifications.

(6) A protection diode is connected to V_{CC} for the SD24 input pins. No protection diode is connected to V_{SS}.

(7) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming or erase (VCC = V_{CC})		2.2		3.6	V
V_{SS}	Supply voltage (AVSS = DVSS = V_{SS})			0		V
T_A	Operating free-air temperature	T temperature range	–40		105	°C
T_J	Operating junction temperature	T temperature range	–40		105	°C
C_{VCORE}	Recommended capacitor at VCORE			470		nF
C_{VCC}/ C_{VCORE}	Capacitor ratio of VCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) (1) (2)		0		16.384	MHz

(1) The MSP430i CPU is clocked directly with MCLK.

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(2) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

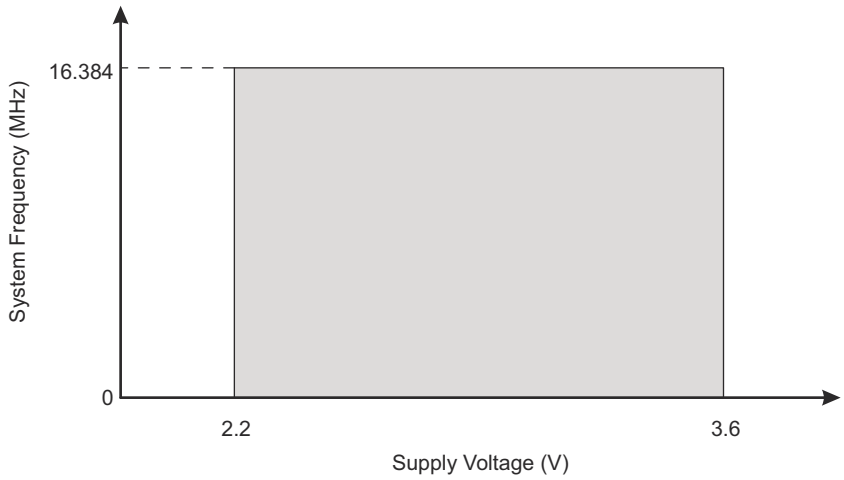


Figure 8-1. Maximum System Frequency

8.4 Active Mode Supply Current (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM, 1.024MHz}$	Active mode current at 1.024 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 1.024 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		1.6		mA
$I_{AM, 8.192MHz}$	Active mode current at 8.192 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 8.192 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		3.0		mA
$I_{AM, 16.384MHz}$	Active mode current at 16.384 MHz	f_{DCO} = f_{MCLK} = f_{SMCLK} = 16.384 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		4.5		mA

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

(2) All peripherals are inactive.

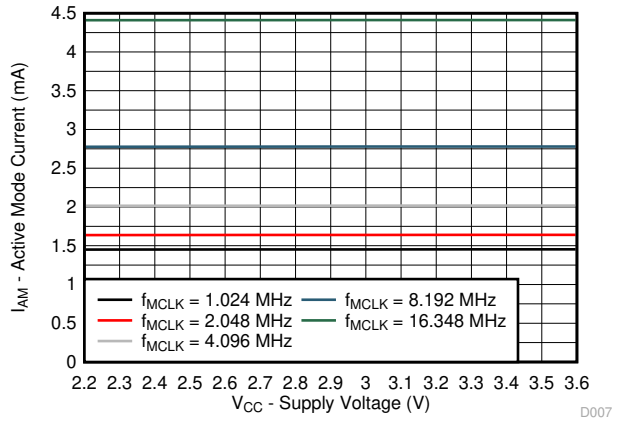


Figure 8-2. Active Mode Current vs Supply Voltage

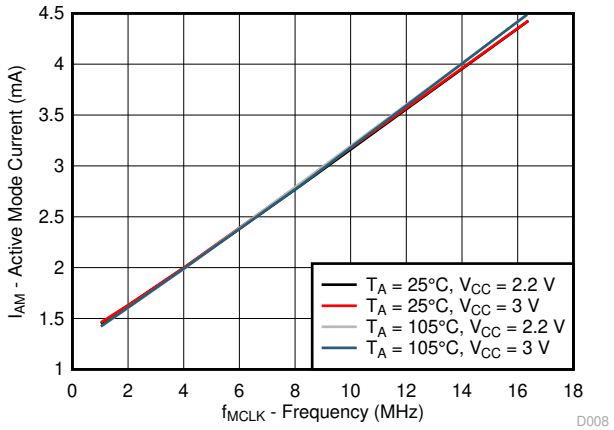


Figure 8-3. Active Mode Current vs MCLK Frequency

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8.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
I_{LPM3}	Low-power mode 3 (LPM3) current (2)	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32 kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	3 V		210		µA
I_{LPM4}	Low-power mode 4 (LPM4) current (3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0 MHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	3 V		70		µA
$I_{LPM4.5}$	Low-power mode 4.5 (LPM4.5) current (3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0 MHz, REGOFF = 1, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	3 V		75		nA
			105°C			325		nA

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by ACLK included. All other peripherals are inactive.

(3) All peripherals are inactive.

8.6 Thermal Resistance Characteristics

THERMAL METRIC(1)		PACKAGE	VALUE(2) (3)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	QFN-32 (RHB)	35.9	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		25.5	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		8.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		8.6	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.3	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		1.4	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	TSSOP-28 (PW)	77.5	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		18.2	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		35.5	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		35.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.5	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC package thermal metrics.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = Not applicable

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8.7 Timing and Switching Characteristics

8.7.1 Reset Timing

8.7.1.1 Reset Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{RESET}	Pulse duration required at the $\overline{RST}$/NMI pin to accept a reset	4		µs

8.7.2 Clock Specifications

8.7.2.1 DCO in External Resistor Mode

recommended resistor at ROSC pin: 20 kΩ, 0.1%, ±50 ppm/°C)(1)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DCO}	DCO current consumption			85		µA
f_{DCO}	DCO frequency calibrated			16.384		MHz
	DCO absolute tolerance calibrated	V_{CC} = 3 V, T_A = 25°C			±0.25%	
df_{DCO}/d_T	DCO frequency temperature drift				±20	ppm/°C
df_{DCO}/dVCC	DCO frequency supply voltage drift			200	600	ppm/V
DC_{DCO}	Duty cycle			50%		
T_{dcoon}	DCO start-up time			40		µs

(1) The maximum parasitic capacitance at ROSC pin should not exceed 5 pF to ensure the specified DCO start-up time.

8.7.2.2 DCO in Internal Resistor Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DCO}	DCO current consumption			85		µA
f_{DCO}	DCO frequency calibrated			16.384		MHz
	DCO absolute tolerance calibrated	V_{CC} = 3 V, T_A = 25°C			±0.9%	
df_{DCO}/d_T	DCO frequency temperature drift				±200	ppm/°C
df_{DCO}/dVCC	DCO frequency supply voltage drift			200	600	ppm/V
DC_{DCO}	Duty cycle			50%		
T_{dcoon}	DCO start-up time			40		µs

8.7.2.3 DCO Overall Tolerance Table

over operating free-air temperature range (unless otherwise noted)

RESISTOR OPTION	TEMPERATURE CHANGE	TEMPERATURE DRIFT (%)	VOLTAGE CHANGE	VOLTAGE DRIFT (%)	OVERALL DRIFT (%)	OVERALL ACCURACY (%)
Internal resistor	–40°C to 105 °C	±2.9	2.2 V to 3.6 V	±0.084	±2.984	±3.884
	0°C	0	2.2 V to 3.6 V	±0.084	±0.084	±0.984
	–40°C to 105 °C	±2.9	0 V	0	±2.9	±3.8
External resistor with 50-ppm TCR	–40°C to 105 °C	±0.29	2.2 V to 3.6 V	±0.084	±0.374	±0.624
	0°C	0	2.2 V to 3.6 V	±0.084	±0.084	±0.334
	–40°C to 105 °C	±0.29	0 V	0	±0.29	±0.54

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8.7.2.4 DCO in Bypass Mode Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
f_{DCOBYP}	Frequency in DCO bypass mode(1)	0	16.384	MHz

(1) External digital clock frequency in DCO bypass mode must be 16.384 MHz for the SD24 module to meet the specified performance.

8.7.3 Wake-up Characteristics

8.7.3.1 Wake-up Times From Low Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE-UP-LPM3}$	Wake-up time from LPM3 to active mode	MCLK = SMCLK = 1.024 MHz		1		µs
$t_{WAKE-UP-LPM4}$	Wake-up time from LPM4 to active mode	MCLK = SMCLK = 1.024 MHz		45		µs
$t_{WAKE-UP-LPM4.5-IO}$	Wake-up time from LPM4.5 to active mode upon I/O event(1)	C_{VCORE} = 470 nF		0.45		ms
$t_{WAKE-UP-LPM4.5-RESET}$	Wake-up time from LPM4.5 to active mode upon external reset ($\overline{RST}$)(1)	C_{VCORE} = 470 nF		0.45		ms

(1) This value represents the time from the wake-up event to the reset vector execution by CPU.

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8.7.4 I/O Ports

8.7.4.1 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.5 V_{CC}		0.7 V_{CC}	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		3 V	0.4		1.1	V
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

8.7.4.2 Inputs – Ports P1 and P2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing(1)	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

8.7.4.3 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Py.x)}$	High-impedance leakage current	See (1) (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input.

8.7.4.4 Outputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –6 mA(1)	3.0 V	V_{CC} – 0.60	V_{CC}	V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.60	V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

8.7.4.5 Output Frequency – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{Py.x}$	Port output frequency (with load)	Py.x, C_L = 20 pF, R_L = 3.2 kΩ (1) (2)	3 V	16.384	MHz
f_{Port_CLK}	Clock output frequency	Py.x, C_L = 20 pF(2)	3 V	16.384	MHz

(1) A resistive divider with two times 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

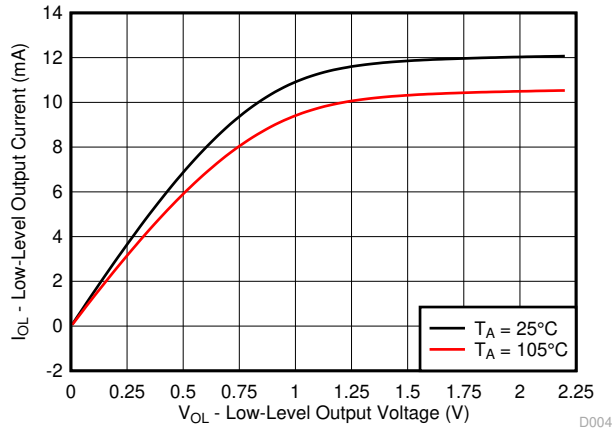
(2) The output voltage reaches at least 10% and 90% of V_{CC} at the specified toggle frequency.

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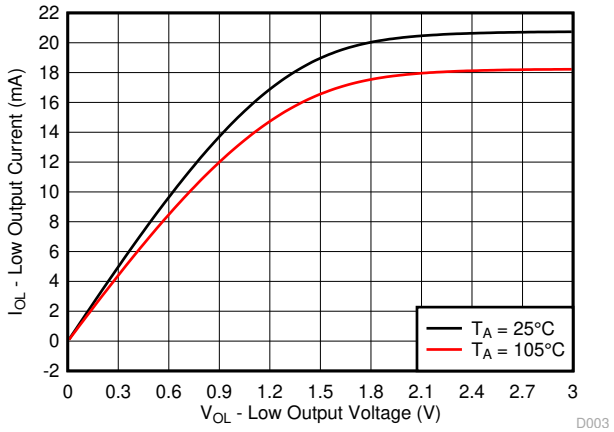
8.7.4.6 Typical Characteristics – Outputs

One output loaded at a time.



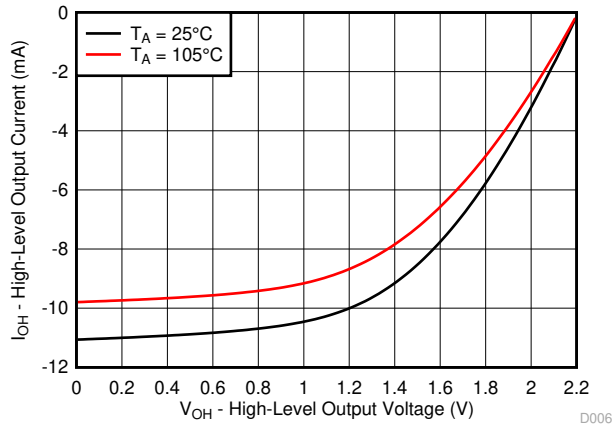
V_{CC} = 2.2 V Measured at P1.3

Figure 8-4. Typical Low-Level Output Current vs Low-Level Output Voltage



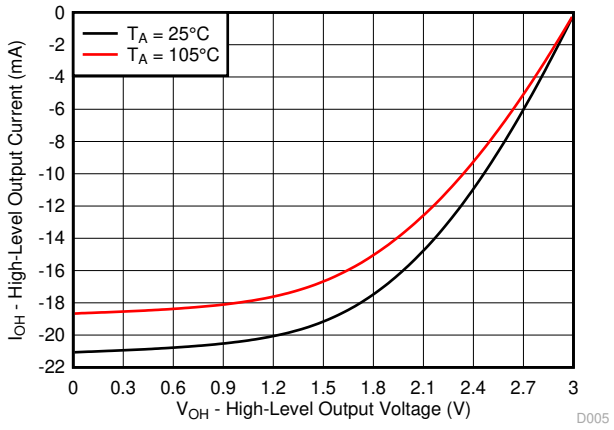
V_{CC} = 3 V Measured at P1.3

Figure 8-5. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.2 V Measured at P1.3

Figure 8-6. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3 V Measured at P1.3

Figure 8-7. Typical High-Level Output Current vs High-Level Output Voltage

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8.7.5 Power Management Module

8.7.5.1 PMM, High-Side Brownout Reset (BORH)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(V_{CC}\_BOR\_IT-)$	BOR_H on voltage, V_{CC} falling level	$\lvert dV_{CC}/d_t \rvert < 3$ V/s		1.08		V
$V(V_{CC}\_BOR\_IT+)$	BOR_H off voltage, V_{CC} rising level	$\lvert dV_{CC}/d_t \rvert < 3$ V/s		1.18		V
$V(V_{CC}\_BOR\_hys)$	BOR_H hysteresis			100		mV
$t_{POWERUP}$ (1)	Cold power-up time				0.75	ms

(1) This is the time duration between application of V_{CC} and execution of reset vector by CPU.

8.7.5.2 PMM, Low-Side SVS (SVSL)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V(SVSL)	SVSL trip voltage on VCORE		1.70		V
V(SVSL_hys)	SVSL hysteresis		14		mV
I(SVSL)	SVSL current consumption		3		µA

8.7.5.3 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{CORE}	Core voltage		1.83		V

8.7.5.4 PMM, Voltage Monitor (VMON)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VMON_{trip\_level}$	VMONIN trip level	VMONLVLx = 111b		1.17		V
	VCC trip level – 1	VMONLVLx = 001b		2.32		
	VCC trip level – 2	VMONLVLx = 010b		2.62		
	VCC trip level – 3	VMONLVLx = 011b		2.82		
I_{VMON}	VMON current consumption			6		µA
t_{VMON}	VMON settling time			0.5		µs

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8.7.6 Reference Module

8.7.6.1 Voltage Reference (REF)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		2.2		3.6	V
V_{BG}	Bandgap output voltage calibrated	V_{CC} = 3 V	1.146	1.158	1.17	V
PSRR_DC	Power supply rejection ratio (DC)	V_{CC} = 2.2 V to 3.6 V		50		µV/V
PSRR_AC	Power supply rejection ratio (AC)	V_{CC} = 2.2 V to 3.6 V, f = 1 kHz, ΔV_{pp} = 100 mV		0.35		mV/V
dV_{BG}/d_T	Bandgap reference temperature coefficient	V_{CC} = 3 V		10	50	ppm/°C

8.7.6.2 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{sensor}	Temperature sensor output voltage	V_{CC} = 3 V, T_A = 30°C	610	650	690	mV
		V_{CC} = 3 V, T_A = 105°C	765	805	845	
I_{sensor}	Temperature sensor quiescent current consumption			3		µA
TC_{sensor}	Temperature coefficient of sensor		1.96	2.07	2.17	mV/°C

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8.7.7 SD24

8.7.7.1 SD24 Power Supply and Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	AVSS = DVSS = 0 V			2.2		3.6	V
I_{SD24}	Analog plus digital supply current per converter (reference current not included)	SD24OSRx = 256	GAIN: 1, 2, 4, 8, 16	3 V		190		µA
			GAIN: 1, 16	3 V			250	

8.7.7.2 SD24 Internal Voltage Reference

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{SD24REF}$	SD24 internal reference voltage	SD24REFS = 1	3 V	1.146	1.158	1.17	V
C_{VREF}	Recommended capacitor at VREF				100		nF
$t_{SD24REF\_settle}$	SD24 reference buffer settling time	SD24REFS = 0 → 1, C_{VREF} = 100 nF			200		µs

(1) When SD24 operates with internal reference (SD24REFS = 1), the VREF pin must not be loaded externally. Only the recommended capacitor value, C_{VREF} must be connected at the VREF pin to AVSS.

8.7.7.3 SD24 External Voltage Reference

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD24REFS = 0	3 V	1.0	1.2	1.5	V
$I_{REF(I)}$	Input current	SD24REFS = 0	3 V			50	nA

8.7.7.4 SD24 Input Range

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full-scale input voltage range	$V_{ID} = V_{I,A+} - V_{I,A-}$			$-V_{REF}$/GAIN		$+V_{REF}$/GAIN	V
V_{ID}	Differential input voltage range for specified performance(2)	SD24REFS = 1	SD24GAINx = 1			±928		mV
			SD24GAINx = 2			±464		
			SD24GAINx = 4			±232		
			SD24GAINx = 8			±116		
			SD24GAINx = 16			±58		
Z_I	Input impedance (pin A+ or A- to AV_{SS})(3)	SD24GAINx = 1, 16		3 V		200		kΩ
Z_{ID}	Differential input impedance (pin A+ to pin A-)(3)	SD24GAINx = 1, 16		3 V	300	400		kΩ
V_I	Absolute input voltage range				AV_{SS} – 1		V_{CC}	V
V_{IC}	Common-mode input voltage range				AV_{SS} – 1		V_{CC}	V

(1) All parameters pertain to each SD24 channel.

(2) The full-scale range is defined by $V_{FSR+} = +V_{REF}/GAIN$ and $V_{FSR-} = -V_{REF}/GAIN$; $FSR = V_{FSR+} - V_{FSR-} = 2xV_{REF}/GAIN$. If VREF is sourced externally, the analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}; that is, V_{ID} = 0.8 V_{FSR-} to 0.8 V_{FSR+}. If VREF is sourced internally, the given V_{ID} ranges apply.

(3) Applicable for SD24 modulator OFF as well as ON conditions.

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8.7.7.5 SD24 Performance, Internal Reference (SD24REFS = 1, SD24OSRx = 256)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V	84	89		dB
		SD24GAINx = 2				89		
		SD24GAINx = 4				87		
		SD24GAINx = 8				83		
		SD24GAINx = 16				77		
THD	Total harmonic distortion	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
SFDR	Spurious-free dynamic range	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
INL	Integral nonlinearity, end-point fit	SD24GAINx: 1, 8, 16		3 V	–0.003		0.003	% FSR
G	Nominal gain	SD24GAINx = 1		3 V		1		
		SD24GAINx = 2				2		
		SD24GAINx = 4				4		
		SD24GAINx = 8				8		
		SD24GAINx = 16				16		
E_G	Gain error	SD24GAINx: 1, 2, 4, 8, 16		3 V	–2%		2%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient	SD24GAINx: 1, 8, 16		3 V			50	ppm/°C
E_{OS}	Offset error	SD24GAINx = 1		3 V			4	mV
		SD24GAINx = 16					2	
ΔEOS/ΔT	Offset error temperature coefficient	SD24GAINx = 1		3 V		±5	±25	ppm FSR/°C
		SD24GAINx = 16				±3	±10	
CMRR,50Hz	Common-mode rejection ratio at 50 Hz	SD24GAINx = 1, Common-mode input signal: V_{ID} = 928 mV, f_{IN} = 50 Hz		3 V		–55		dB
		SD24GAINx = 16, Common-mode input signal: V_{ID} = 58 mV, f_{IN} = 50 Hz				–60		
AC PSRR	AC power supply rejection ratio	SD24GAINx: 1, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–90		dB
		SD24GAINx: 8, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
		SD24GAINx: 16, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
XT	Crosstalk between converters	Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 1		3 V		–120		dB
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 8				–110		
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 16				–110		

(1) The following voltages are applied to the SD24 inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24 input range).

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8.7.7.6 SD24 Performance, External Reference (SD24REFS = 0, SD24OSRx = 256)

external reference voltage is 1.2 V., over operating free-air temperature range (unless otherwise noted)

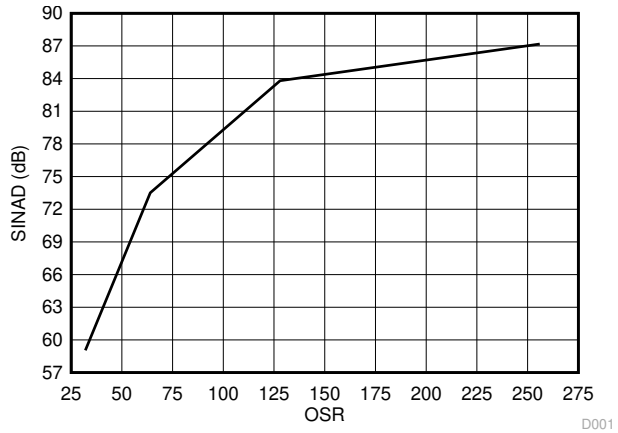
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		91		dB
		SD24GAINx = 2				90		
		SD24GAINx = 4				88		
		SD24GAINx = 8				83		
		SD24GAINx = 16				77		
THD	Total harmonic distortion	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
SFDR	Spurious-free dynamic range	SD24GAINx = 1	f_{IN} = 50 Hz(1)	3 V		100		dB
		SD24GAINx = 8				95		
		SD24GAINx = 16				90		
INL	Integral nonlinearity, end-point fit	SD24GAINx: 1, 8, 16		3 V	–0.003		0.003	% FSR
G	Nominal gain	SD24GAINx = 1		3 V		1		
		SD24GAINx = 2				2		
		SD24GAINx = 4				4		
		SD24GAINx = 8				8		
		SD24GAINx = 16				16		
E_G	Gain error	SD24GAINx: 1, 2, 4, 8, 16		3 V	–1%		+1%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient	SD24GAINx: 1, 8, 16		3 V			10	ppm/°C
E_{OS}	Offset error	SD24GAINx = 1		3 V			4	mV
		SD24GAINx = 16					2	
ΔEOS/ΔT	Offset error temperature coefficient	SD24GAINx = 1		3 V		±5	±25	ppm FSR/°C
		SD24GAINx = 16				±3	±10	
CMRR,50Hz	Common-mode rejection ratio at 50 Hz	SD24GAINx = 1, Common-mode input signal: V_{ID} = 928 mV, f_{IN} = 50 Hz		3 V		–55		dB
		SD24GAINx = 16, Common-mode input signal: V_{ID} = 58 mV, f_{IN} = 50 Hz				–60		
AC PSRR	AC power supply rejection ratio	SD24GAINx: 1, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–90		dB
		SD24GAINx: 8, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
		SD24GAINx: 16, V_{CC} = 3 V ±50 mV × sin(2π × f_{VCC} × t), f_{VCC} = 50 Hz, Inputs grounded (no analog signal applied)		3 V		–95		
XT	Crosstalk between converters	Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 1		3 V		–120		dB
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 8				–110		
		Crosstalk source: SD24GAINx = 1, Sine-wave with maximum possible V_{PP}, f_{IN} = 50 Hz or 100 Hz, Converter under test: SD24GAINx = 16				–110		

(1) The following voltages are applied to the SD24 inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24 input range).

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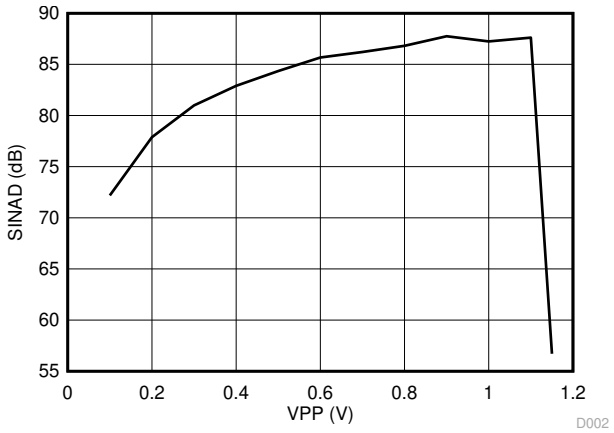
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8.7.7.7 Typical Characteristics



A. f_{SD24} = 1.024 MHz SD24REFS = 1 SD24GAINx = 1

Figure 8-8. SINAD vs OSR



A. f_{SD24} = 1.024 MHz SD24REFS = 1
OSR = 256 SD24GAINx = 1

Figure 8-9. SINAD vs VPP

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8.7.8 eUSCI

8.7.8.1 eUSCI (UART Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

8.7.8.2 eUSCI (UART Mode) Deglitch Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0	2.2 V, 3 V	8	15	20	ns
		UCGLITx = 1		30	50	60	
		UCGLITx = 2		50	70	100	
		UCGLITx = 3		70	100	150	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

8.7.8.3 eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz

8.7.8.4 eUSCI (SPI Master Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10	2.2 V, 3 V	150		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10	2.2 V, 3 V	200		ns
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V		40	ns
			3 V		30	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V		40	ns
			3 V		30	
$t_{SU,MI}$	SOMI input data setup time		2.2 V	50		ns
			3 V	30		
$t_{HD,MI}$	SOMI input data hold time		2.2 V, 3 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		7	ns
			3 V		5	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V, 3 V	0		ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, refer to the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-10 and Figure 8-11.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 8-10 and Figure 8-11.

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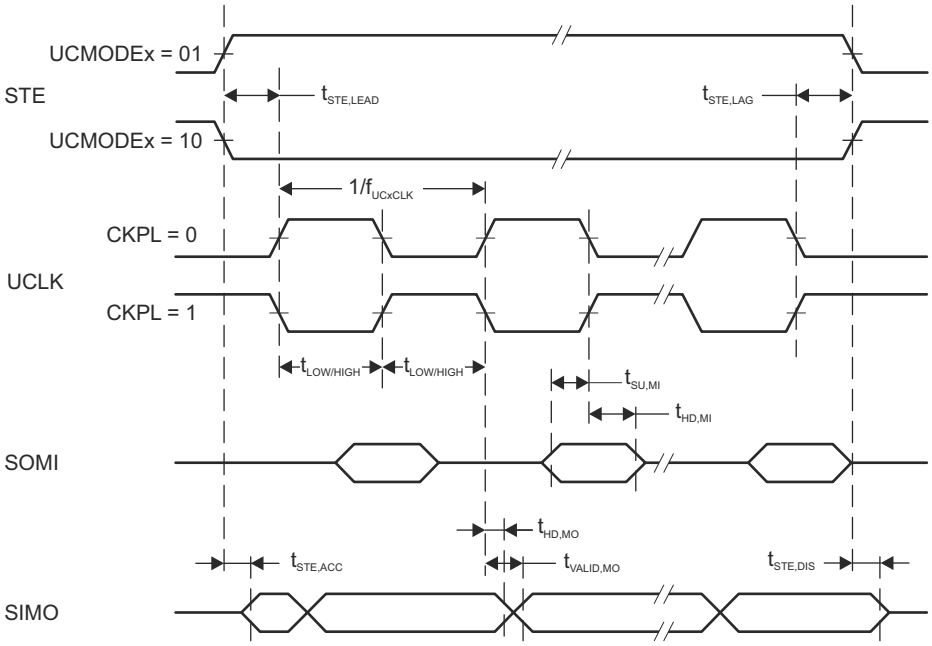


Figure 8-10. SPI Master Mode, CKPH = 0

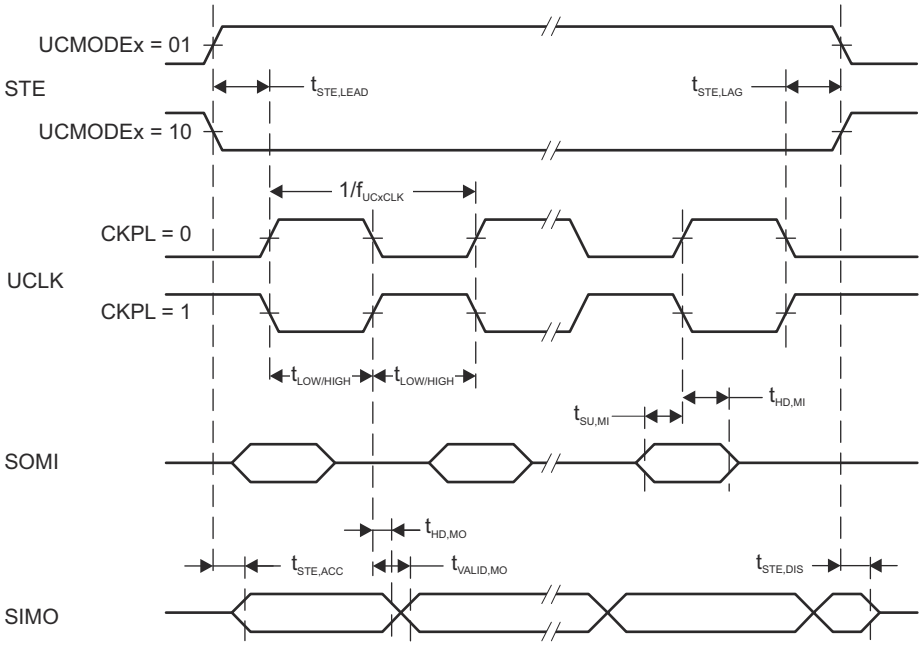


Figure 8-11. SPI Master Mode, CKPH = 1

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8.7.8.5 eUSCI (SPI Slave Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.2 V, 3 V	3		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2.2 V, 3 V	0		ns
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.2 V		35	ns
			3 V		25	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.2 V, 3 V		35	ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V, 3 V	1		ns
$t_{HD,SI}$	SIMO input data hold time		2.2 V, 3 V	5		ns
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		35	ns
			3 V		25	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	2.2 V	35		ns
			3 V	25		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, refer to the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-12 and Figure 8-13.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 8-12 and Figure 8-13.

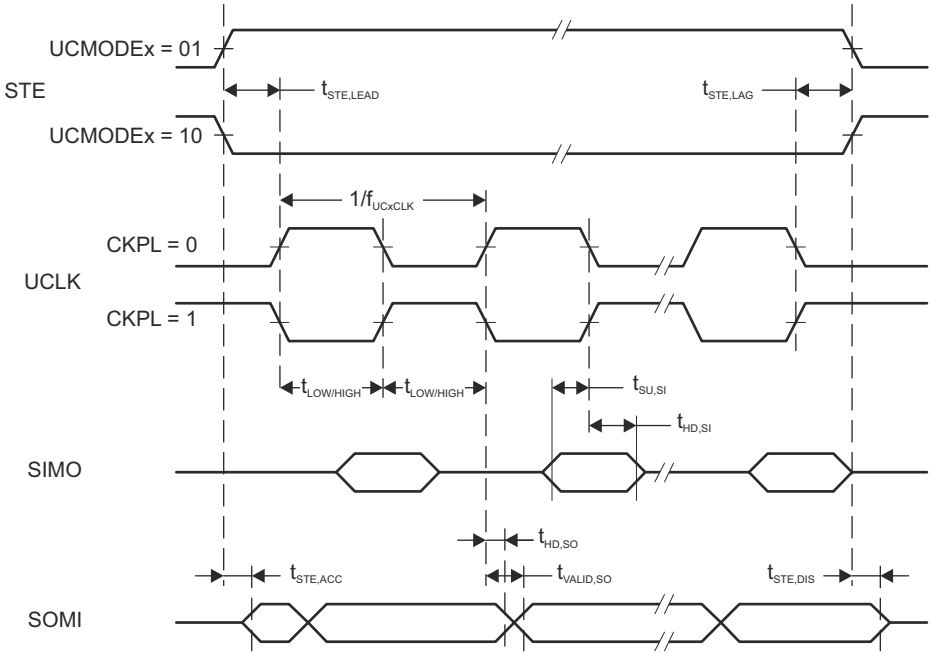


Figure 8-12. SPI Slave Mode, CKPH = 0

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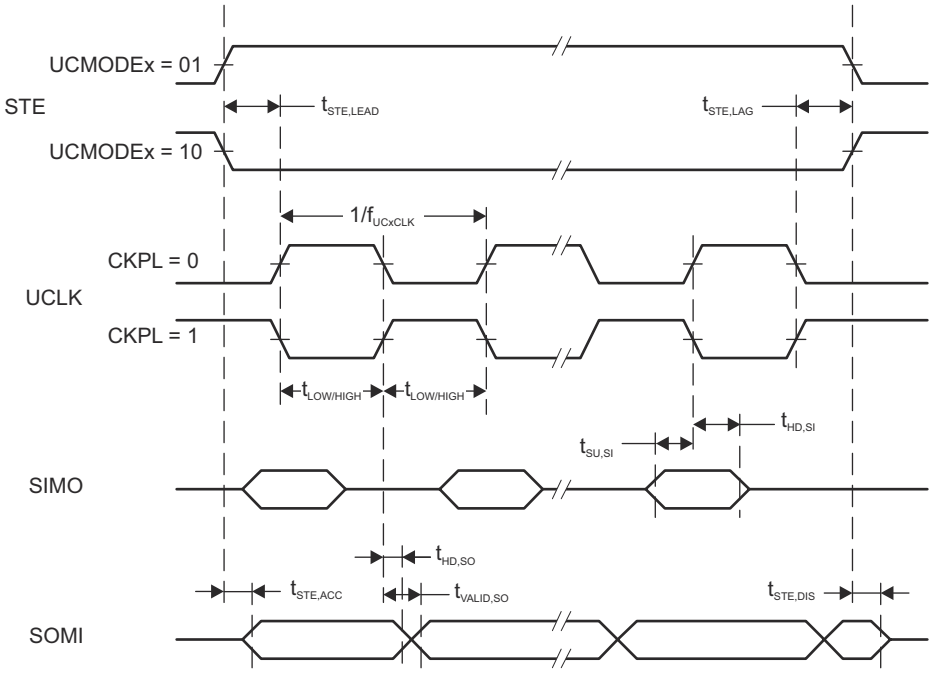


Figure 8-13. SPI Slave Mode, CKPH = 1

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8.7.8.6 eUSCI (I²C Mode) Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3 V	4.8			µs
		f_{SCL} > 100 kHz		1.2			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3 V	4.9			µs
		f_{SCL} > 100 kHz		1.26			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0.12			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		1.08			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3 V	4.9			µs
		f_{SCL} > 100 kHz		1.18			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3 V	75	110	160	ns
		UCGLITx = 1		35	50	80	
		UCGLITx = 2		15	25	40	
		UCGLITx = 3		10	15	20	
$t_{TIMEOUT}$	Clock low timeout	UCCLTOx = 1	2.2 V, 3 V		33		ms
		UCCLTOx = 2			37		
		UCCLTOx = 3			41		

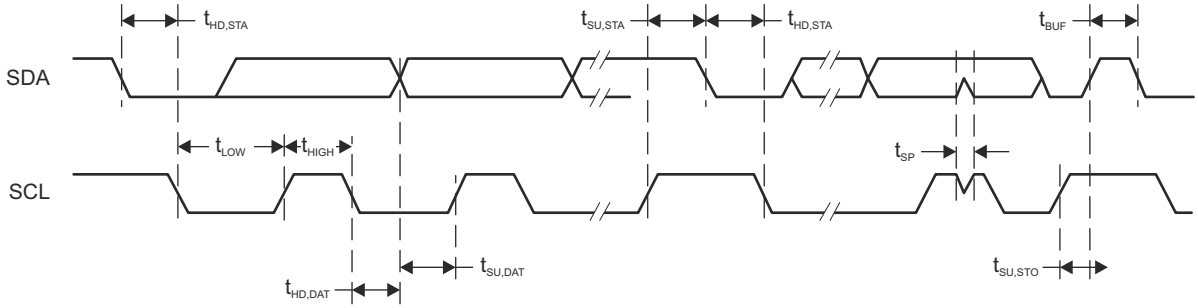


Figure 8-14. I²C Mode Timing

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8.7.9 Timer_A

8.7.9.1 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK External: TACLK	3.0 V			16.384	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	3.0 V	20			ns

8.7.10 Flash

8.7.10.1 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V			8	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V			13	mA
t_{CPT}	Cumulative program time(1)		2.2 V, 3.6 V			8	ms
	Program and erase endurance			20000			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			25		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			20		
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			11		
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		
$t_{Mass Erase}$	Mass erase time	(2)			10593		
$t_{Seg Erase}$	Segment erase time	(2)			9628		

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word-write mode, individual byte-write mode, and block-write mode.

(2) These values are hardwired into the state machine of the flash controller ($t_{FTG} = 1/f_{FTG}$).

8.7.11 Emulation and Debug

8.7.11.1 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	3.0 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	3.0 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	3.0 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time	3.0 V	15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG(2)	3.0 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	3.0 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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9 Detailed Description

9.1 Overview

The MSP430i204x, MSP430i203x, MSP430i202x devices consist of a powerful 16-bit RISC CPU, a DCO-based clock system that generates system clocks, a power-management module (PMM) with built-in voltage reference and voltage monitor, two to four 24-bit sigma-delta analog-to-digital converters (ADCs), a temperature sensor, a 16-bit hardware multiplier, two 16-bit timers, one eUSCI-A module and one eUSCI-B module, a watchdog timer (WDT), and up to 16 I/O pins.

9.2 Functional Block Diagrams

Figure 9-1 shows the functional block diagram for the MSP430i2041 and MSP430i2040 in the RHB package.

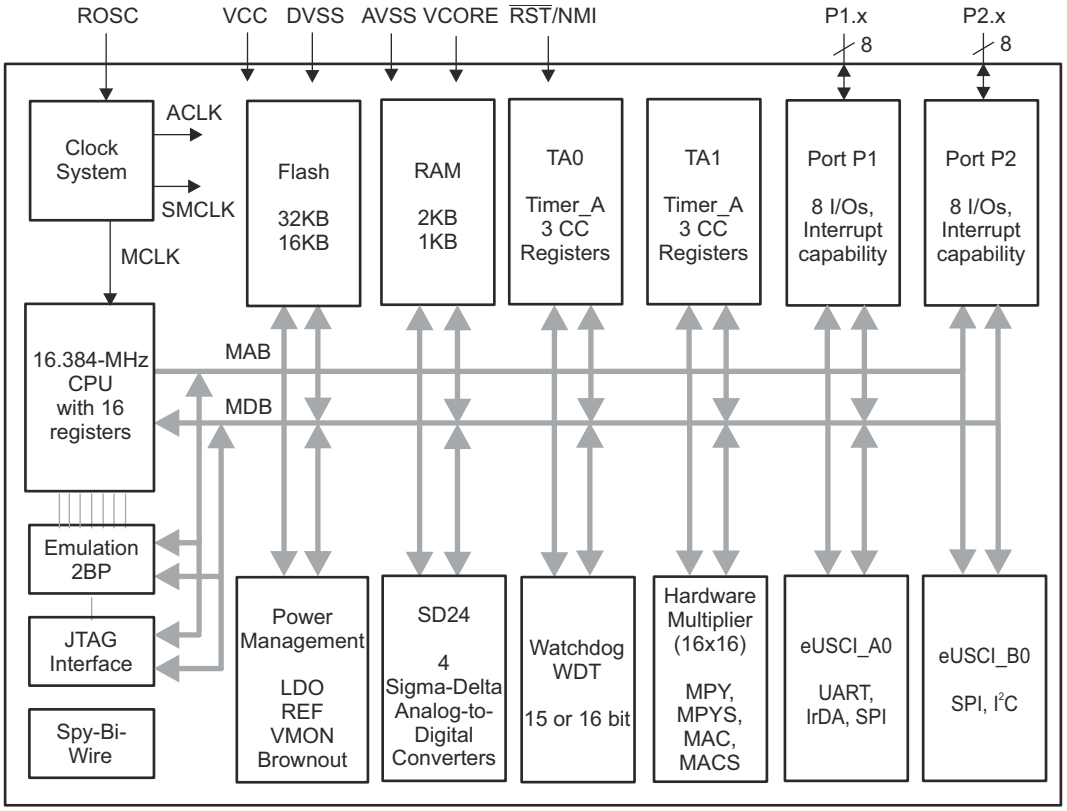


Figure 9-1. Functional Block Diagram – RHB Package – MSP430i2041, MSP430i2040

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Figure 9-2 shows the functional block diagram for the MSP430i2041 and MSP430i2040 in the PW package.

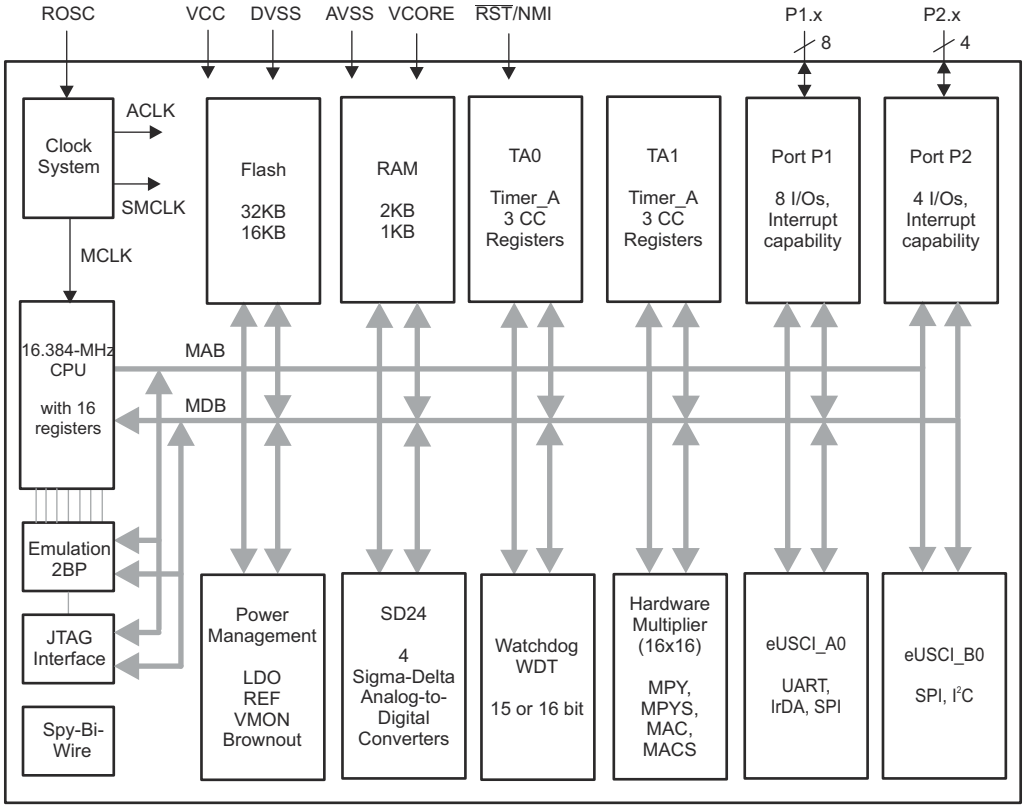


Figure 9-2. Functional Block Diagram – PW Package – MSP430i2041, MSP430i2040

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Figure 9-3 shows the functional block diagram for the MSP430i2031 and MSP430i2030 in the RHB package.

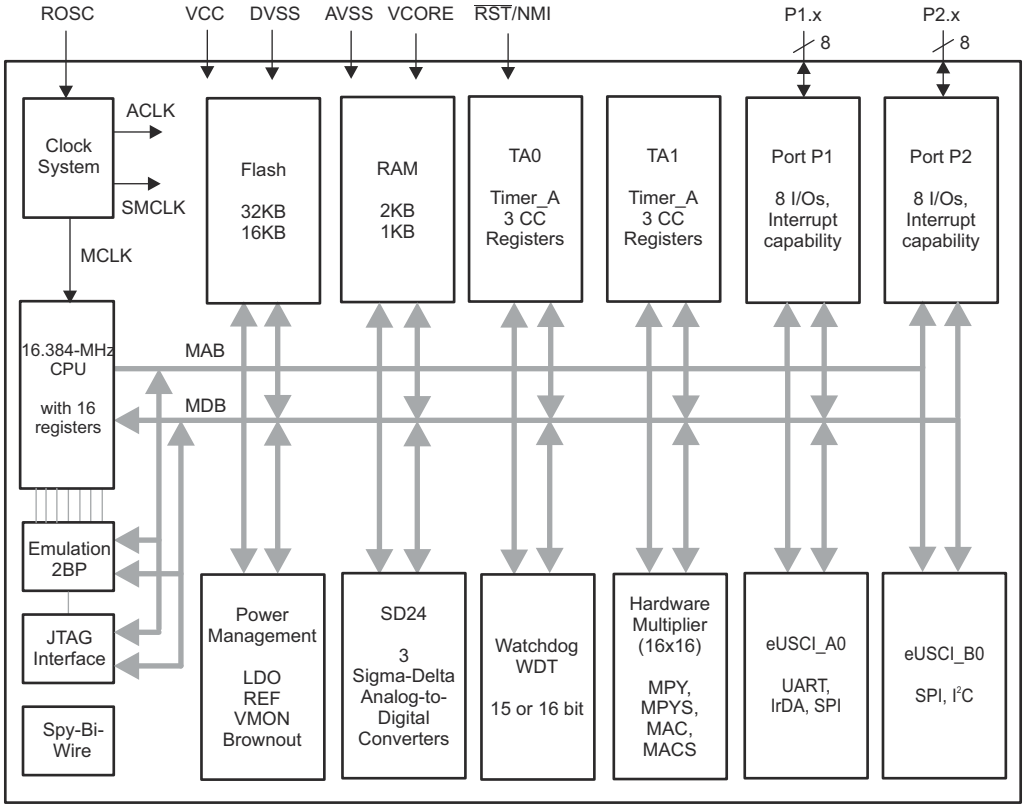


Figure 9-3. Functional Block Diagram – RHB Package – MSP430i2031, MSP430i2030

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Figure 9-4 shows the functional block diagram for the MSP430i2031 and MSP430i2030 in the PW package.

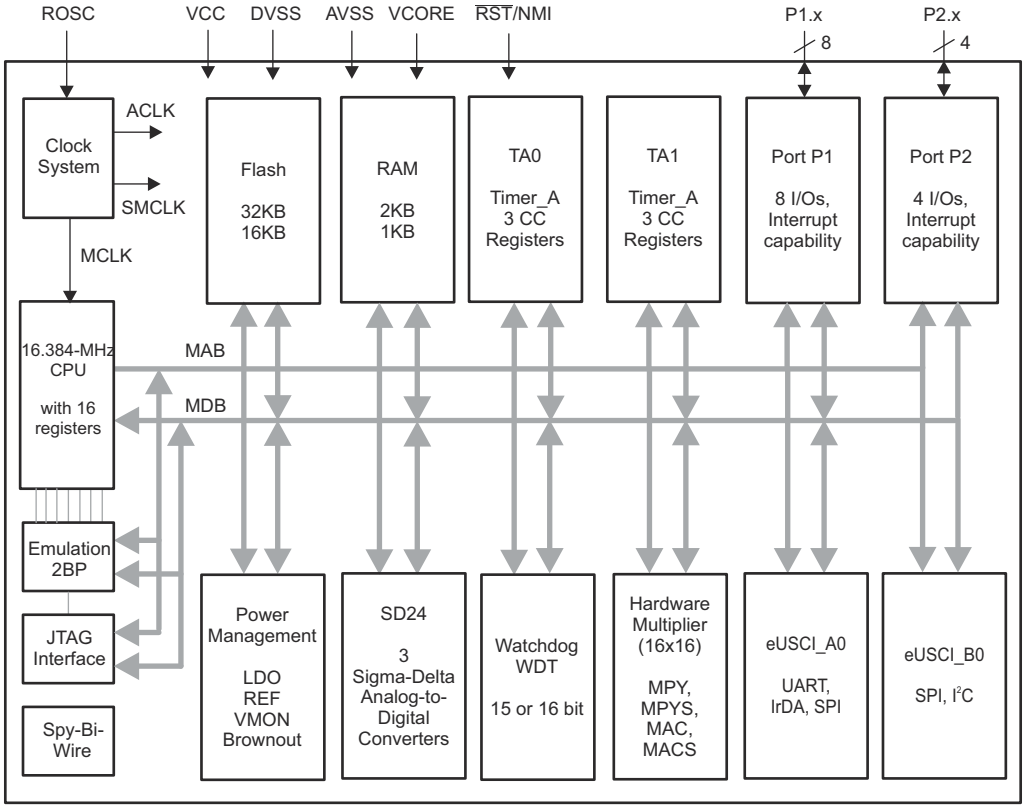


Figure 9-4. Functional Block Diagram – PW Package – MSP430i2031, MSP430i2030

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Figure 9-5 shows the functional block diagram for the MSP430i2021 and MSP430i2020 in the RHB package.

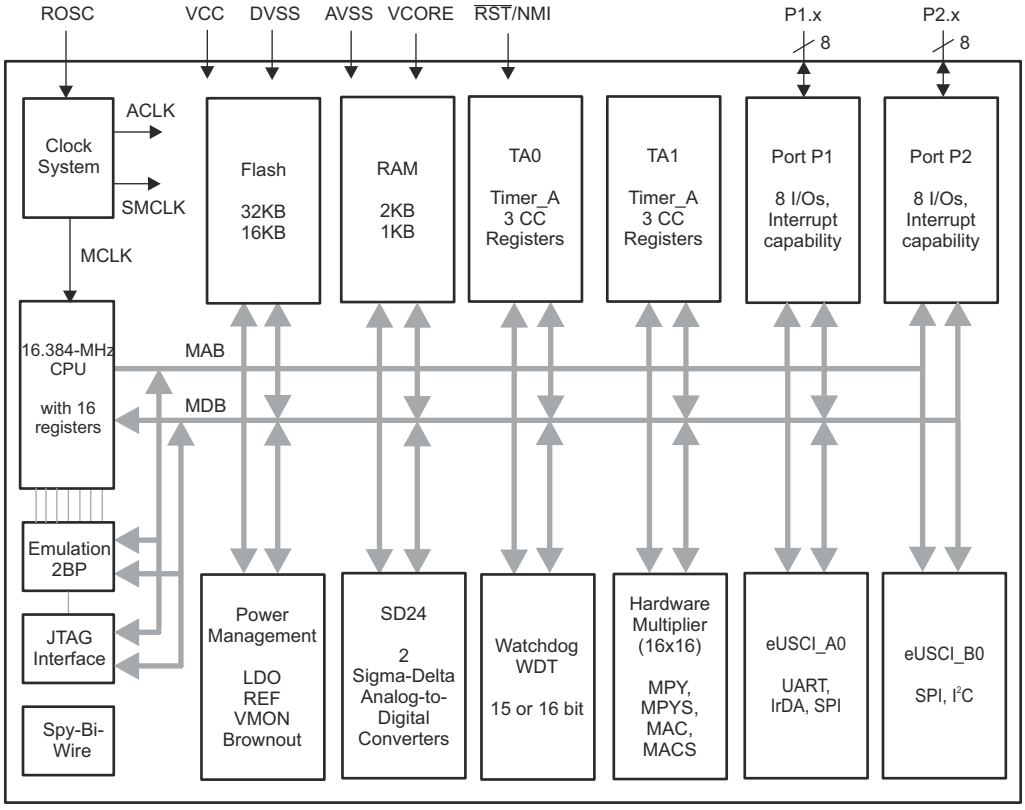


Figure 9-5. Functional Block Diagram – RHB Package – MSP430i2021, MSP430i2020

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Figure 9-6 shows the functional block diagram for the MSP430i2021 and MSP430i2020 in the PW package.

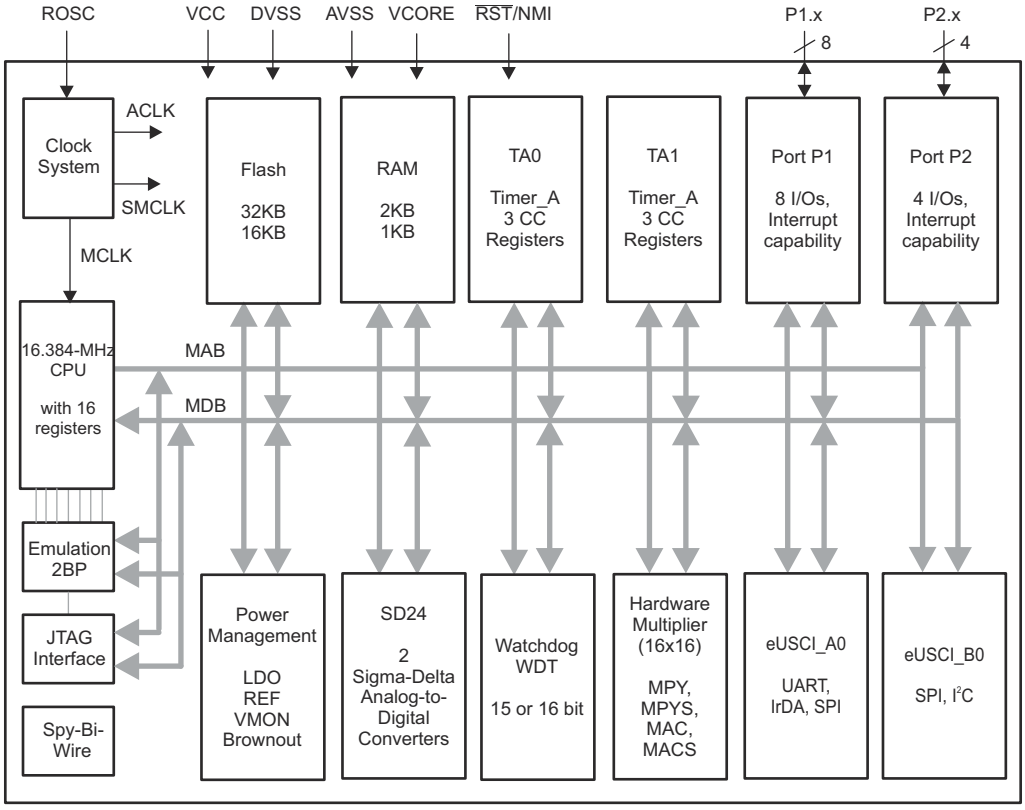


Figure 9-6. Functional Block Diagram – PW Package – MSP430i2021, MSP430i2020

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9.3 CPU

The MSP430i CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers (see Figure 9-7).

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

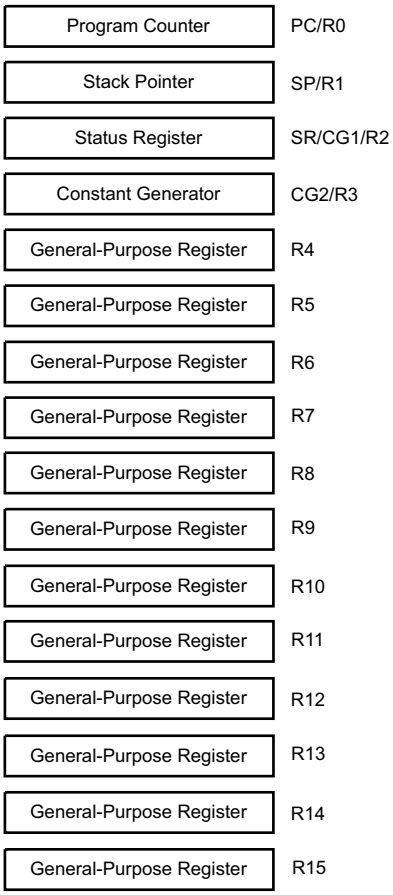


Figure 9-7. CPU Registers

CAUTION

The CPU will lock up if the device enters a low-power mode (CPU off) within 64 cycles after reset.

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9.4 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 9-1 gives examples of the three types of instruction formats; Table 9-2 lists the address modes.

Table 9-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source and destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 9-2. Address Mode Descriptions

ADDRESS MODE	S (1)	D (2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source

(2) D = destination

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9.5 Operating Modes

MSP430i204x, MSP430i203x, MSP430i202x devices have one active mode and four software-selectable low-power modes. An interrupt event can wake up the device from the low-power modes LPM0 to LPM4, service the request, and restore back to the low-power mode on return from the interrupt program.

The following five operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 or low-power mode 1 (LPM0 = LPM1)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO remains enabled
  - MCLK is disabled
  - ACLK and SMCLK remain active
- Low-power mode 2 or low-power mode 3 (LPM2 = LPM3)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO remains enabled
  - MCLK and SMCLK are disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - Internal regulator remains enabled
  - DCO is disabled
  - MCLK, SMCLK, and ACLK are disabled
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator is disabled
  - No RAM retention
  - I/O pad state retention
  - Wake from $\overline{\text{RST}}$/NMI, ports pins P2.1 or P2.2

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9.6 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 9-3. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash key violation PC out-of-range (1)	BORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2) (4)	(Non)maskable, (Non)maskable, (Non)maskable	0FFFCh	14
Timer TA1	TA1CCR0 CCIFG (3)	Maskable	0FFFAh	13
Timer TA1	TA1CCR1 CCIFG, TA1CCR2 CCIFG, TA1CTL TAIFG (2) (3)	Maskable	0FFF8h	12
Voltage monitor	VMONIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
eUSCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG	Maskable	0FFF2h	9
eUSCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG	Maskable	0FFF0h	8
SD24	SD24CCTLx SD24OVIFG, SD24CCTLx SD24IFG(2) (3)	Maskable	0FFEEh	7
Timer TA0	TA0CCR0 CCIFG (3)	Maskable	0FFECh	6
Timer TA0	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG (2) (3)	Maskable	0FFEAh	5
I/O port P1	P1IFG.0 to P1IFG.7 (2) (3)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2	P2IFG.0 to P2IFG.7 (2) (3)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.

(2) Multiple source flags

(3) Interrupt flags are in the module.

(4) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

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9.7 Special Function Registers

Some interrupt enable and interrupt flag bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is Reset or Set by POR.
rw-[0], rw-[1]	Bit can be read and written. It is Reset or Set by BOR.
	SFR bit is not present in device.

Table 9-4. Interrupt Enable 1 (Address = 00h)

7	6	5	4	3	2	1	0
		ACCVIE	NMIIE			OFIE	WDTIE
		rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 9-5. Interrupt Flag Register 1 (Address = 02h)

7	6	5	4	3	2	1	0
			NMIIFG	RSTIFG	BORIFG	OFIFG	WDTIFG
			rw-0	rw-[0]	rw-[1]	rw-0	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault. This flag can be cleared by software when the oscillator runs free of fault.
BORIFG	Brown out reset flag. This bit is set after V_{CC} power up and can be cleared by software.
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
NMIIFG	Set by the $\overline{RST}$/NMI pin in NMI configuration.

9.8 Flash Memory

The flash memory can be programmed through the Spy-Bi-Wire or JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory:

- Flash memory has n segments of main memory and one segment of information memory.
- Segment size is 1KB for both main memory and information memory.
- Segments 0 to n in main memory can be erased in one step, or each segment may be individually erased.
- Information memory segment can be erased separately or as a group with main memory segments 0 to n.
- Information memory segment contains calibration data. After reset, information memory segment is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

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9.9 JTAG Operation

9.9.1 JTAG Standard Interface

The MSP430i family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430i development tools and device programmers. Table 9-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide.

Table 9-6. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
P1.0/UCA0STE/MCLK/TCK	IN	JTAG clock input
P1.1/UCA0CLK/SMCLK/TMS	IN	JTAG state control
P1.2/UCA0RXD/UCA0SOMI/ACLK/TDI/TCLK	IN	JTAG data input/TCLK input
P1.3/UCA0TXD/UCA0SIMO/TA0CLK/TDO/TDI	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
DVSS		Ground supply

9.9.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430i family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430i development tools and device programmers. Table 9-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide.

Table 9-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
DVSS		Ground supply

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9.9.3 JTAG Disable Register

The SYSJTAGDIS register can disable the JTAG port to provide code protection and device security. JTAG is disabled when software writes the value 0xA5A5 to this register within 64 MCLK clock cycles after a BOR or POR reset; otherwise, the JTAG port is enabled. Any writes to this register after the first 64 MCLK clock cycles are ignored. Reads from this register at any time return the JTAG enable or disable status. The value 0xA5A5 indicates that JTAG is disabled, and 0x9696 indicates that JTAG is enabled. The SYSJTAGDIS register is mapped to address 01FEh.

Note

Application programming the device to any of the low power modes within first 64 MCLK clock cycles after a BOR or POR reset will lock the device for any JTAG/SBW access.

Table 9-8. SYSJTAGDIS Register

15	14	13	12	11	10	9	8
JTAGKEY							
rw-[1]	rw-[0]	rw-[1]	rw-[0]	rw-[0]	rw-[1]	rw-[0]	rw-[1]
7	6	5	4	3	2	1	0
JTAGKEY							
rw-[1]	rw-[0]	rw-[1]	rw-[0]	rw-[0]	rw-[1]	rw-[0]	rw-[1]

JTAGKEY	0xA5A5 indicates JTAG is disabled and 0x9696 indicates JTAG is enabled.

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9.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the MSP430i2xx Family User's Guide.

9.10.1 Clock System

The clock system consists of a fixed 16.384-MHz frequency internal DCO. The DCO can operate in internal resistor mode or external resistor mode. The DCO clock accuracy is higher when operating in external resistor mode especially upon variation in operating temperature. This feature can be useful in applications like utility metering in which accurate clock is necessary under varying operating temperature. When external resistor mode is selected by application, the resistor of recommended value must be connected to ROSC pin of the device. Refer to Section 8.7.2.1 for the recommended value of the resistor at the ROSC pin. TI recommends connecting the ROSC pin to AVSS when operating the DCO in internal resistor mode. When a resistor fault is detected in the external resistor mode, the DCO automatically switches to the internal resistor mode as a fail-safe mechanism to keep the system clocks active.

The DCO can be completely bypassed and the system clocks can be sourced by an external digital clock. The clock system generates MCLK, SMCLK, and ACLK. MCLK is used by the CPU, while SMCLK and ACLK are used by the peripheral modules. There are programmable clock dividers for MCLK and SMCLK. ACLK runs at a fixed 32-kHz frequency. The clock system supports active mode and four low-power modes.

9.10.2 Power-Management Module (PMM)

The PMM consists of voltage regulator that generates 1.8-V regulated core voltage. There is a brownout reset (BOR) circuit on the high-voltage domain, and a supply voltage supervisor (SVS) module on the low-voltage domain. The BOR and SVS provide the proper internal reset signal to the device during power on and power off.

A built-in voltage reference is used by submodules of the PMM and by the analog modules on the device. A temperature sensor is also available in the built-in voltage reference.

The voltage monitor (VMON) on the high-voltage domain can monitor external voltage on the VMONIN pin against the internal reference voltage or by comparing the on-chip V_{CC} to one of three programmable threshold voltages. During the LPM4.5 mode, the reference, voltage regulator, temperature sensor, and voltage monitor are turned off, and only the high-side brownout circuit is active.

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9.10.3 Digital I/O

Two 8-bit I/O ports (P1 and P2) are implemented on the MSP430i204x, MSP430i203x, MSP430i202x devices. On 32-pin RHB devices, ports P1 and P2 are complete, and 16 I/Os are available. On 28-pin PW devices, port P2 is reduced to 4 bits, and 12 I/Os are available. On 28-pin PW devices, the unavailable pins (P2.4 to P2.7) must be programmed to port function, output direction, and be driven with value 0.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all 8 bits of port P1 and P2
- LPM4.5 wake-up capability for Port pins P2.1 and P2.2
- Read and write access to port-control registers is supported by all instructions.

9.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

9.10.5 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 9-9). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-9. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.3	TA0CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.3	$\overline{\text{TA0CLK}}$	INCLK				
P1.4	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.4
P2.5	TA0.0	CCI0B				P2.5
	DVSS	GND				
	VCC	VCC				
P1.5	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.5
	ACLK (internal)	CCI1B				P2.6
	DVSS	GND				
	VCC	VCC				
P1.6	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.6
	TA1 CCR2 output (internal)	CCI2B				P2.7
	DVSS	GND			TA1 CCI2B input	
	VCC	VCC				

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9.10.6 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 9-10). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9-10. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.7	TA1CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.7	$\overline{\text{TA1CLK}}$	INCLK				
P2.0	TA1.0	CCI0A	CCR0	TA0	TA1.0	P2.0
P2.4	TA1.0	CCI0B				P2.4
	DVSS	GND				
	VCC	VCC				
P2.1	TA1.1	CCI1A	CCR1	TA1	TA1.1	P2.1
	ACLK (internal)	CCI1B				
	DVSS	GND				
	VCC	VCC				
P2.2	TA1.2	CCI2A	CCR2	TA2	TA1.2	P2.2
	TA0 CCR2 output (internal)	CCI2B				
	DVSS	GND			TA0 CCI2B input	
	VCC	VCC				

9.10.7 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

One eUSCI_A and one eUSCI_B module are implemented on MSP430i20xx devices.

9.10.8 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16-bit, 16×8-bit, 8×16-bit, and 8×8-bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

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9.10.9 SD24

There are up to four independent 24-bit sigma-delta ADCs. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. Also the converters are based on second-order oversampling sigma-delta modulators and digital decimation filters. The decimation filters are comb-type filters with selectable oversampling ratios of up to 256.

The SD24 converters can operate with internal reference (SD24REFS = 1) or with external reference (SD24REFS = 0). When SD24 operates with internal reference the VREF pin must not be loaded externally. Connect only the recommended capacitor value (C_{VREF}) at VREF pin to AVSS (see Section 8.7.7.2).

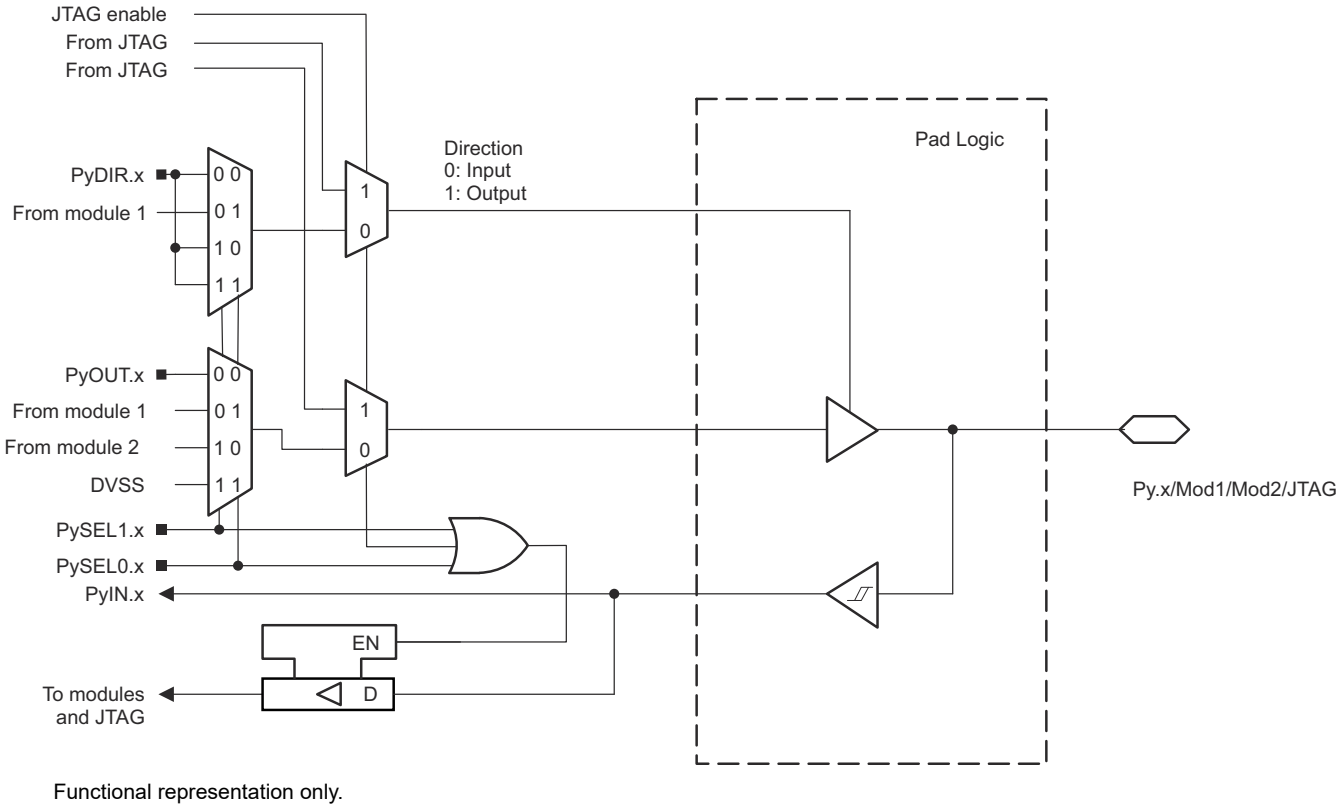
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9.11 Input/Output Diagrams

9.11.1 Port P1, P1.0 to P1.3, Input/Output With Schmitt Trigger

Figure 9-8 shows the pin diagram. Table 9-11 summarizes the selection of the pin function.



Functional representation only.

Figure 9-8. Py.x/Mod1/Mod2/JTAG Pin Diagram

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Table 9-11. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P1DIR.x	P1SEL1.x	P1SEL0.x	JTAG Enable
P1.0/UCA0STE/MCLK/TCK	0	P1.0 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0STE	X[3]	0	1	0
		N/A	0	1	0	0
		MCLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TCK[4]	X	X	X	1
P1.1/UCA0CLK/SMCLK/TMS	1	P1.1 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0CLK	X[3]	0	1	0
		N/A	0	1	0	0
		SMCLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TMS[4]	X	X	X	1
P1.2/UCA0RXD/UCA0SOMI/ ACLK/TDI/TCLK	2	P1.2 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0RXD/UCA0SOMI	X[3]	0	1	0
		N/A	0	1	0	0
		ACLK	1			
		N/A	0	1	1	0
		DVSS	1			
		TDI/TCLK[4]	X	X	X	1
P1.3/UCA0TXD/UCA0SIMO/ TA0CLK/TDO/TDI	3	P1.3 (I/O)[2]	I: 0; O: 1	0	0	0
		UCA0TXD/UCA0SIMO	X[3]	0	1	0
		TA0CLK	0	1	0	0
		DVSS	1			
		N/A	0	1	1	0
		DVSS	1			
		TDO/TDI[4]	X	X	X	1

(1) X = Don't care

(2) Default condition

(3) Direction is controlled by eUSCI_A0 module.

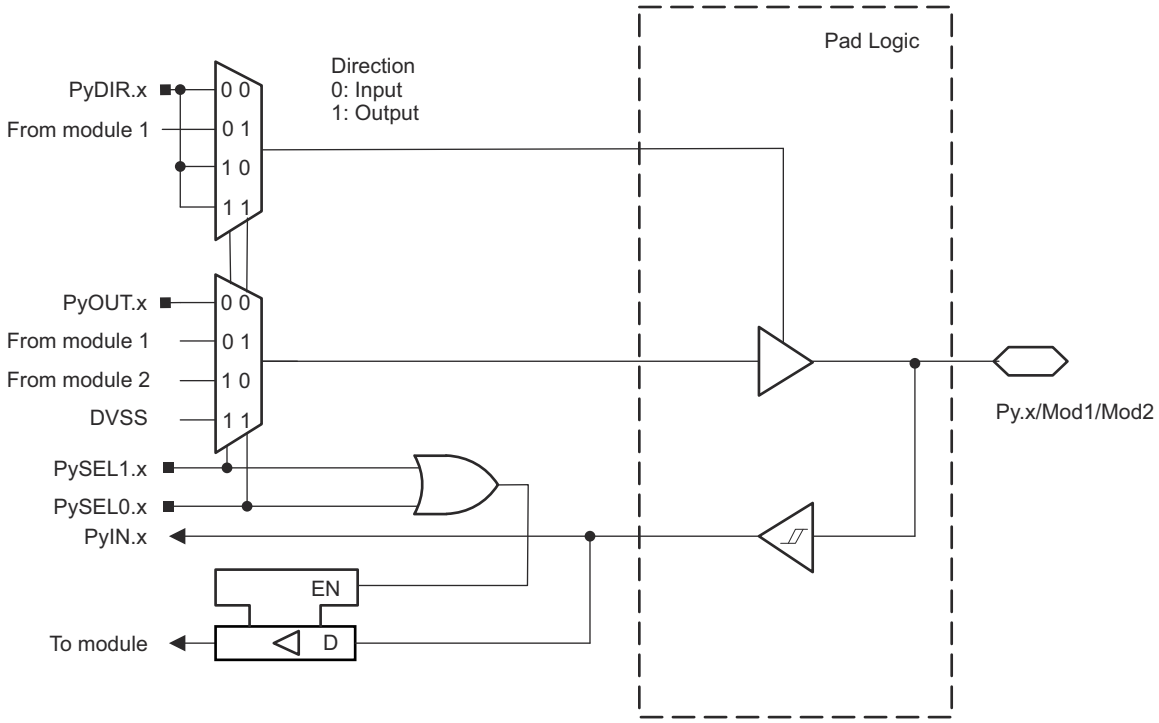
(4) The pin direction is controlled by the JTAG module. The JTAG mode selection is made through the Spy-Bi-Wire 4-wire entry sequence. Neither P1SEL0.x and P1SEL1.x nor P1DIR.x have an effect in these cases.

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9.11.2 Port P1, P1.4 to P1.7, Input/Output With Schmitt Trigger

Figure 9-9 shows the pin diagram. Table 9-12 summarizes the selection of the pin function.



Functional representation only.

Figure 9-9. Py.x/Mod1/Mod2 Pin Schematic

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Table 9-12. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.4/UCB0STE/TA0.0	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X(2)	0	1
		TA0.CCI0A	0	1	0
		TA0.0	1		
		N/A	0	1	1
		DVSS	1		
P1.5/UCB0CLK/TA0.1	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X(2)	0	1
		TA0.CCI1A	0	1	0
		TA0.1	1		
		N/A	0	1	1
		DVSS	1		
P1.6/UCB0SCL/UCB0SOMI/ TA0.2	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SCL/UCB0SOMI	X(2)	0	1
		TA0.CCI2A	0	1	0
		TA0.2	1		
		N/A	0	1	1
		DVSS	1		
P1.7/UCB0SDA/UCB0SIMO/ TA1CLK	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SDA/UCB0SIMO	X(2)	0	1
		TA1CLK	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care

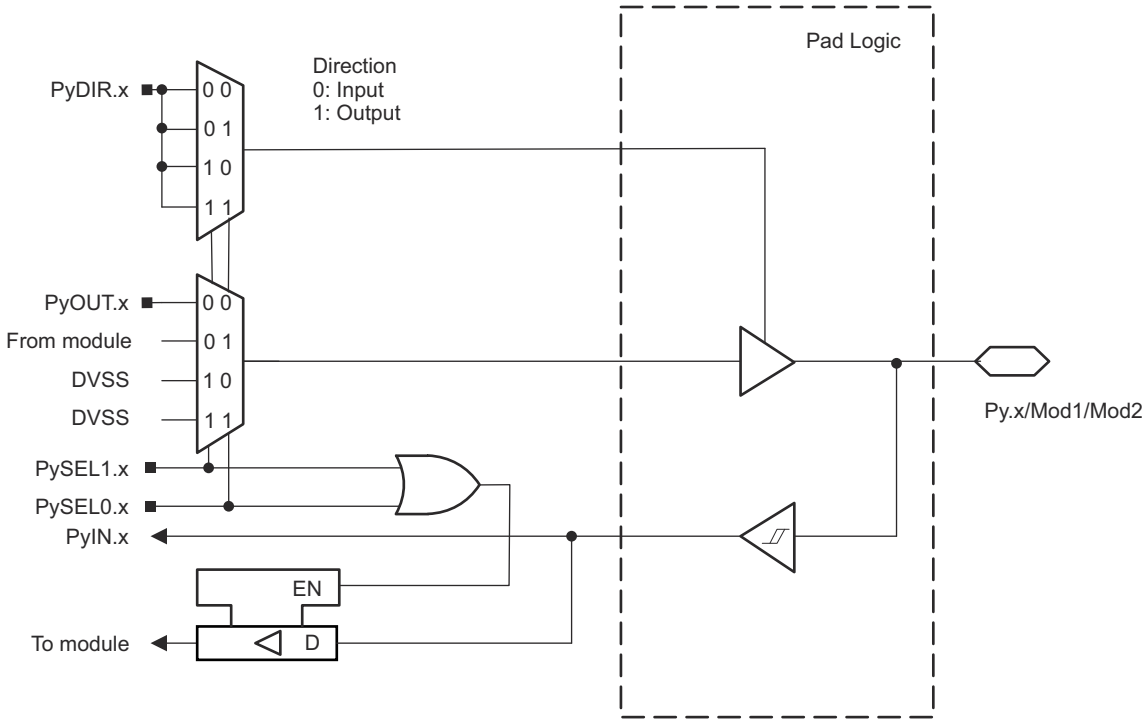
(2) Direction is controlled by eUSCI_B0 module.

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9.11.3 Port P2, P2.0 to P2.2 and P2.4 to P2.7, Input/Output With Schmitt Trigger

Figure 9-10 shows the pin diagram. Table 9-13 summarizes the selection of the pin function.



Functional representation only.

Figure 9-10. Py.x/Mod1/Mod2 Pin Schematic

Table 9-13. Port P2 (P2.0 to P2.2 and P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/TA1.0/CLKIN	0	P2.0 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0A	0	0	1
		TA1.0	1		
		CLKIN (DCO bypass clock)	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.1/TA1.1	1	P2.1 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

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Table 9-13. Port P2 (P2.0 to P2.2 and P2.4 to P2.7) Pin Functions (continued)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.2/TA1.2	2	P2.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.4/TA1.0(1)	4	P2.4 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0B	0	0	1
		TA1.0	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.5/TA0.0(1)	5	P2.5 (I/O)	I: 0; O: 1	0	0
		TA0.CCI0B	0	0	1
		TA0.0	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.6/TA0.1(1)	6	P2.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TA0.1	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P2.7/TA0.2(1)	7	P2.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TA0.2	1		
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

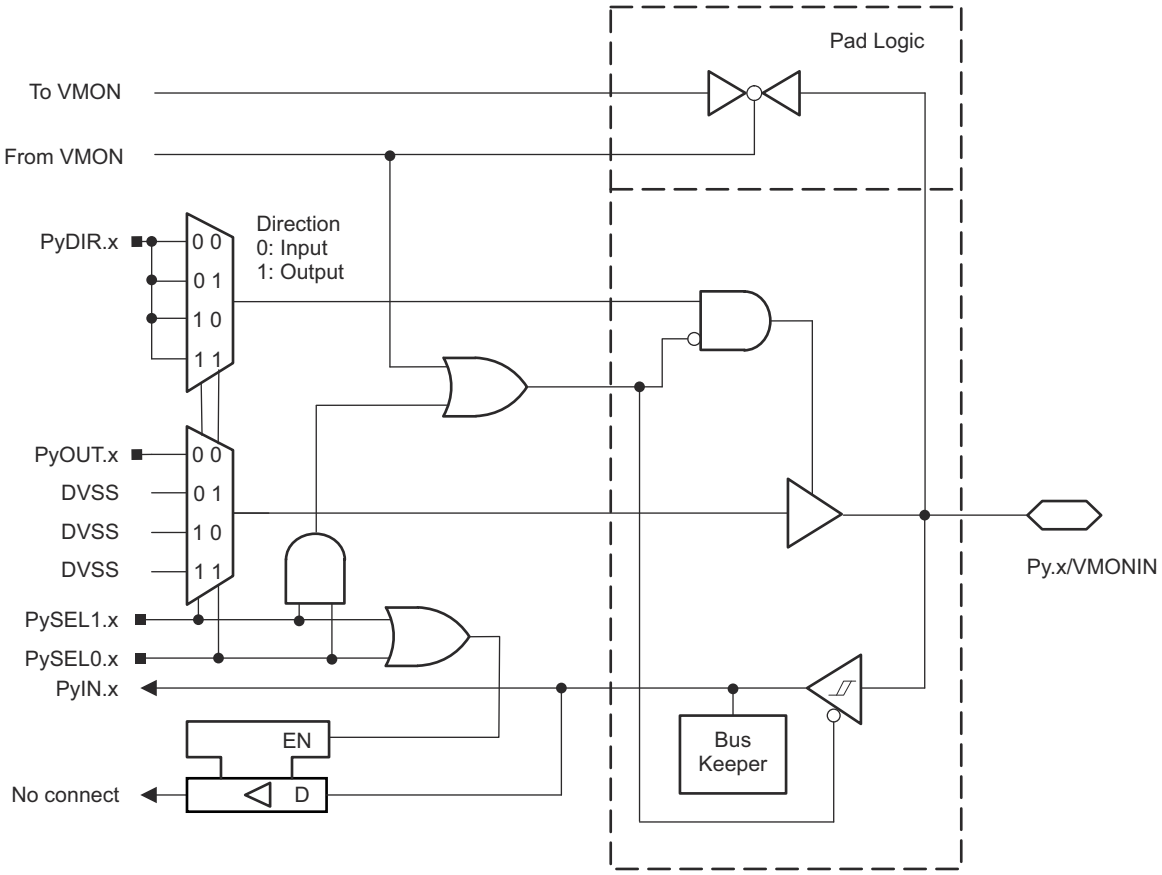
(1) Available only on 32-pin RHB devices.

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9.11.4 Port P2, P2.3, Input/Output With Schmitt Trigger

Figure 9-11 shows the pin diagram. Table 9-14 summarizes the selection of the pin function.



Functional representation only.

Figure 9-11. Py.x/VMONIN Pin Schematic

Table 9-14. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.3/VMONIN	3	P2.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		VMONIN(2)	X	1	1

(1) X = Don't care

(2) Setting P2SEL1.3 and P2SEL0.3 disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying voltage at VMONIN pin. To enable the VMONIN function, VMONLVLx bits must be set to 3'b111 in the VMONCTL register.

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9.12 Device Descriptor

Table 9-15 lists the contents of the tag-length-value (TLV) device descriptor structure for the MSP430i204x, MSP430i203x, and MSP430i202x devices.

Table 9-15. MSP430i204x, MSP430i203x, MSP430i202x TLV

DESCRIPTION		ADDRESS	SIZE (BYTES)	VALUE
Checksum	TLV checksum	013C0h	2	Per unit
Die Record	Die Record Tag	013C2h	1	01h
	Die Record Length	013C3h	1	0Ah
	Lot/Wafer ID	013C4h	4	Per unit
	Die X position	013C8h	2	Per unit
	Die Y position	013CAh	2	Per unit
	Test results	013CCh	2	Per unit
REF Calibration	REF Calibration Tag	013CEh	1	02h
	REF Calibration Length	013CFh	1	02h
	Calibrate REF – for REFCAL1 register	013D0h	1	Per unit
	Calibrate REF – for REFCAL0 register	013D1h	1	Per unit
DCO Calibration	DCO Calibration Tag	013D2h	1	03h
	DCO Calibration Length	013D3h	1	04h
	Calibrate DCO – for CSIRFCAL register	013D4h	1	Per unit
	Calibrate DCO – for CSIRTCAL register	013D5h	1	Per unit
	Calibrate DCO – for CSERFCAL register	013D6h	1	Per unit
	Calibrate DCO – for CSERTCAL register	013D7h	1	Per unit
SD24 Calibration	SD24 Calibration Tag	013D8h	1	04h
	SD24 Calibration Length	013D9h	1	02h
	Calibrate SD24 – for SD24TRIM register	013DAh	1	Per unit
	Empty	013DBh	1	FFh
Empty	Tag Empty	013DCh	1	FEh
	Empty Length	013DDh	1	22h
	Empty	013DEh	34	FFh

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9.13 Memory

Table 9-16 lists the memory organization for the specified devices.

Table 9-16. Memory Organization

		MSP430i2040 MSP430i2030 MSP430i2020	MSP430i2041 MSP430i2031 MSP430i2021
Memory	Size	16KB	32KB
Main: interrupt vector	Flash	0xFFFF to 0xFFE0	0xFFFF to 0xFFE0
Main: code memory	Flash	0xFFFF to 0xC000	0xFFFF to 0x8000
Information memory	Size	1KB	1KB
	Flash	0x13FFh to 0x1000	0x13FFh to 0x1000
RAM	Size	1KB	2KB
	Address	0x05FF to 0x0200	0x09FF to 0x0200
Peripherals	16-bit	0x01FF to 0x0100	0x01FF to 0x0100
	8-bit	0x00FF to 0x0010	0x00FF to 0x0010
	8-bit SFR	0x000F to 0x0000	0x000F to 0x0000

9.13.1 Peripheral File Map

Table 9-17 lists the peripherals that support word access, and Table 9-18 lists the peripherals that support byte access. Peripherals that support both access types are listed in both tables.

Table 9-17. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
SYS	JTAG disable register	SYSJTAGDIS	0x01FE
Timer TA1	Capture/compare register 2	TA1CCR2	0x0196
	Capture/compare register 1	TA1CCR1	0x0194
	Capture/compare register 0	TA1CCR0	0x0192
	Timer_A register	TA1R	0x0190
	Capture/compare control 2	TA1CCTL2	0x0186
	Capture/compare control 1	TA1CCTL1	0x0184
	Capture/compare control 0	TA1CCTL0	0x0182
	Timer_A control	TA1CTL	0x0180
	Timer_A interrupt vector	TA1IV	0x011E
Timer TA0	Capture/compare register 2	TA0CCR2	0x0176
	Capture/compare register 1	TA0CCR1	0x0174
	Capture/compare register 0	TA0CCR0	0x0172
	Timer_A register	TA0R	0x0170
	Capture/compare control 2	TA0CCTL2	0x0166
	Capture/compare control 1	TA0CCTL1	0x0164
	Capture/compare control 0	TA0CCTL0	0x0162
	Timer_A control	TA0CTL	0x0160
	Timer_A interrupt vector	TA0IV	0x012E

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Table 9-17. Peripherals With Word Access (continued)

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A0	USCI_A control word 0	UCA0CTLW0	0x0140
	USCI _A control word 1	UCA0CTLW1	0x0142
	USCI_A baud rate 0	UCA0BR0	0x0146
	USCI_A baud rate 1	UCA0BR1	0x0147
	USCI_A modulation control	UCA0MCTLW	0x0148
	USCI_A status	UCA0STAT	0x014A
	USCI_A receive buffer	UCA0RXBUF	0x014C
	USCI_A transmit buffer	UCA0TXBUF	0x014E
	USCI_A LIN control	UCA0ABCTL	0x0150
	USCI_A IrDA transmit control	UCA0IRTCTL	0x0152
	USCI_A IrDA receive control	UCA0IRRCTL	0x0153
	USCI_A interrupt enable	UCA0IE	0x015A
	USCI_A interrupt flags	UCA0IFG	0x015C
	USCI_A interrupt vector word	UCA0IV	0x015E
eUSCI_B0	USCI_B control word 0	UCB0CTLW0	0x01C0
	USCI_B control word 1	UCB0CTLW1	0x01C2
	USCI_B bit rate 0	UCB0BR0	0x01C6
	USCI_B bit rate 1	UCB0BR1	0x01C7
	USCI_B status word	UCB0STATW	0x01C8
	USCI_B byte counter threshold	UCB0TBCNT	0x01CA
	USCI_B receive buffer	UCB0RXBUF	0x01CC
	USCI_B transmit buffer	UCB0TXBUF	0x01CE
	USCI_B I2C own address 0	UCB0I2COA0	0x01D4
	USCI_B I2C own address 1	UCB0I2COA1	0x01D6
	USCI_B I2C own address 2	UCB0I2COA2	0x01D8
	USCI_B I2C own address 3	UCB0I2COA3	0x01DA
	USCI_B received address	UCB0ADDRX	0x01DC
	USCI_B address mask	UCB0ADDMASK	0x01DE
	USCI I2C slave address	UCB0I2CSA	0x01E0
	USCI interrupt enable	UCB0IE	0x01EA
	USCI interrupt flags	UCB0IFG	0x01EC
	USCI interrupt vector word	UCB0IV	0x01EE
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed + accumulate/operand 1	MACS	0x0136
	Multiply + accumulate/operand 1	MAC	0x0134
	Multiply signed/operand 1	MPYS	0x0132
	Multiply unsigned/operand 1	MPY	0x0130
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog Timer	Watchdog/timer control	WDTCTL	0x0120

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Table 9-17. Peripherals With Word Access (continued)

MODULE	REGISTER DESCRIPTION	ACRONYM	ADDRESS
SD24 (also see Table 9-18)	SD24 interrupt vector word register	SD24IV	0x01F0
	Channel 3 conversion memory(1) (2)	SD24MEM3	0x0116
	Channel 2 conversion memory(2)	SD24MEM2	0x0114
	Channel 1 conversion memory	SD24MEM1	0x0112
	Channel 0 conversion memory	SD24MEM0	0x0110
	Channel 3 control(1) (2)	SD24CCTL3	0x0108
	Channel 2 control(2)	SD24CCTL2	0x0106
	Channel 1 control	SD24CCTL1	0x0104
	Channel 0 control	SD24CCTL0	0x0102
	General Control	SD24CTL	0x0100

(1) Not available on MSP430i2031 and MSP430i2030 devices.

(2) Not available on MSP430i2021 and MSP430i2020 devices.

Table 9-18. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	ADDRESS
SD24 (also see Table 9-17)	SD24 trim	SD24TRIM	0x00BF
	Channel 3 preload(1) (2)	SD24PRE3	0x00BB
	Channel 2 preload(2)	SD24PRE2	0x00BA
	Channel 1 preload	SD24PRE1	0x00B9
	Channel 0 preload	SD24PRE0	0x00B8
	Channel 3 input control(1) (2)	SD24INCTL3	0x00B3
	Channel 2 input control(2)	SD24INCTL2	0x00B2
	Channel 1 input control	SD24INCTL1	0x00B1
	Channel 0 input control	SD24INCTL0	0x00B0
PMM	Reference calibration 1	REFCAL1	0x0063
	Reference calibration 0	REFCAL0	0x0062
	Voltage monitor control	VMONCTL	0x0061
	LPM4.5 control	LPM45CTL	0x0060
Clock System	Clock system external resistor temperature calibration	CSERTCAL	0x0055
	Clock system external resistor frequency calibration	CSERFCAL	0x0054
	Clock system internal resistor temperature calibration	CSIRTCAL	0x0053
	Clock system internal resistor frequency calibration	CSIRFCAL	0x0052
	Clock system control 1	CSCTL1	0x0051
	Clock system control 0	CSCTL0	0x0050
Port P2	Port P2 interrupt flag	P2IFG	0x002D
	Port P2 interrupt enable	P2IE	0x002B
	Port P2 interrupt edge select	P2IES	0x0029
	Port P2 interrupt vector word	P2IV	0x002E
	Port P2 selection 1	P2SEL1	0x001D
	Port P2 selection 0	P2SEL0	0x001B
	Port P2 direction	P2DIR	0x0015
	Port P2 output	P2OUT	0x0013
	Port P2 input	P2IN	0x0011

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Table 9-18. Peripherals With Byte Access (continued)

MODULE	REGISTER DESCRIPTION	REGISTER NAME	ADDRESS
Port P1	Port P1 interrupt flag	P1IFG	0x002C
	Port P1 interrupt enable	P1IE	0x002A
	Port P1 interrupt edge select	P1IES	0x0028
	Port P1 interrupt vector word	P1IV	0x001E
	Port P1 selection 1	P1SEL1	0x001C
	Port P1 selection 0	P1SEL0	0x001A
	Port P1 direction	P1DIR	0x0014
	Port P1 output	P1OUT	0x0012
	Port P1 input	P1IN	0x0010
Special Function	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 1	IE1	0x0000

(1) Not available on MSP430i2031 or MSP430i2030 devices.

(2) Not available on MSP430i2021 or MSP430i2020 devices.

9.14 Identification

9.14.1 Device Identification

The device type can be identified from the top-side marking on the device package. See the packaging information page or the device errata sheets listed in Section 11.4 for help.

9.14.2 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the MSP430 Programming With the JTAG Interface.

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10 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The following resources provide application guidelines and best practices when designing with the MSP430i20xx devices.

Implementation of a One- or Two-Phase Electronic Watt-Hour Meter Using MSP430i20xx application report

This application report describes the implementation of a low-cost 1- or 2-phase electronic electricity meter that uses the TI MSP430i20xx metering processor. This application report includes information on metrology software and hardware procedures for this single-chip implementation.

Single-Phase and DC Embedded Metering Power Using MSP430i2040 application report

This application report describes an EVM that uses the MSP430i2040 microcontroller for embedded metering (submetering). In this application, the electricity measuring device is embedded in the end application and gives the user information about the voltage, current, and power consumption of the device. In addition, the EVM can compensate for line resistance and EMI filter capacitance.

Single Phase and DC Embedded Metering (Server Power Monitor) reference design

This reference design implements a high-accuracy single-phase embedded meter using an MSP430 MCU. This EVM has built-in support to measure AC voltage, current, active power, reactive power, apparent power, frequency, power factor, voltage THD, current THD, fundamental voltage, fundamental current, fundamental power and DC voltage, DC current, DC active power. It can detect the input voltage to work in DC or AC mode. It can also compensate for the effects of the wire resistance and the EMI filter capacitance so that the reading of voltage and power matches the reading of an external meter when EMI filter is connected to the input.

Three Output Smart Power Strip reference design

This reference design implements a high-accuracy single-phase embedded metering smart power strip using an MSP430 MCU. This design supports measurement of AC voltage, current, active power, reactive power, apparent power, frequency, and power factor with 3 sockets measured individually. Additional hardware is added to provide futher development like relay control and wired or wireless communication.

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11 Device and Documentation Support

11.1 Getting Started and Next Steps

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430™ ultra-low-power sensing & measurement MCUs overview.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

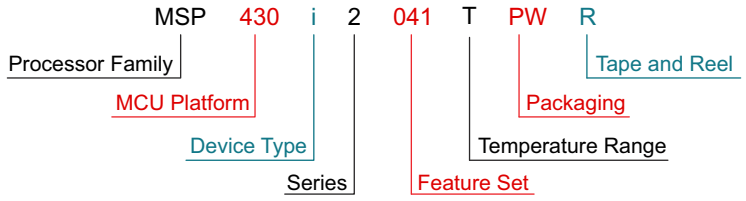
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 11-1 provides a legend for reading the complete device name.



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon
MCU Platform	430 = TI's MSP430 Microcontroller Platform
Device Type	Specialized Application i = Flash Industrial
Series	2 = Flash 2 series up to 16.384 MHz
Feature Set	Various levels of integration within a series
Temperature Range	T = –40°C to 105°C
Packaging	http://www.ti.com/packaging
Tape and Reel	T = Small Reel R = Large Reel No markings = Tube or tray

Figure 11-1. Device Nomenclature

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11.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 ultra-low-power MCUs – Design & development.

Design Kits and Evaluation Modules

32-pin target development board and MSP-FET programmer bundle for MSP430i2x MCUs

The MSP-FET430U32A is a stand-alone ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy-Bi-Wire (2-wire JTAG) protocol.

MSP430 LaunchPad™ Value Line Development Kit

The MSP-EXP430G2 LaunchPad development kit is an easy-to-use microcontroller development board for the low-power and low-cost MSP430G2x MCUs. It has on-board emulation for programming and debugging and features a 14/20-pin DIP socket, on-board buttons and LEDs and BoosterPack plug-in module pinouts that support a wide range of modules for added functionality such as wireless, displays, and more.

MSP430i2040 Submetering EVM

This embedded metering (sub-meter or e-meter) EVM is designed based on the MSP430i2040. The EVM can be connected to the mains (or to DC) and the load directly. The EVM measures the electrical parameters of the load and the result of measurement can be read from the UART port. This EVM provided with built-in power supply and isolated serial connect to facilitate user quick start to the evaluation of the MSP430i2040 in embedded metering application.

Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430i20xx Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

Floating Point Math Library for MSP430

Leveraging the intelligent peripherals of TI devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs.

Fixed Point Math Library for MSP

The TI MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

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Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

MSP Flasher - Command Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

11.4 Documentation Support

The following documents describe the MSP430i20xx MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, MSP430i2041). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430i2041 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2040 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2031 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2031 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2021 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430i2021 Device Erratasheet

Describes the known exceptions to the functional specifications.

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User's Guides

MSP430i2xx Family User's Guide

Detailed description of all modules and peripherals available in this device family.

MSP430™ Flash Device Bootloader (BSL) User's Guide

The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators

Selection of the correct crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses different ESD topics to help board designers and OEMs understand and design robust system-level designs.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

MSP430Ware™, MSP430™, Code Composer Studio™, TI E2E™, LaunchPad™, are trademarks of Texas Instruments.
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11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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11.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

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8-Mar-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430I2020TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T	Samples
MSP430I2020TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T	Samples
MSP430I2020TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T	Samples
MSP430I2020TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2020T	Samples
MSP430I2021TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T	Samples
MSP430I2021TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T	Samples
MSP430I2021TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T	Samples
MSP430I2021TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2021T	Samples
MSP430I2030TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T	Samples
MSP430I2030TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T	Samples
MSP430I2030TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T	Samples
MSP430I2030TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2030T	Samples
MSP430I2031TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T	Samples
MSP430I2031TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T	Samples
MSP430I2031TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T	Samples
MSP430I2031TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2031T	Samples
MSP430I2040TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T	Samples
MSP430I2040TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T	Samples
MSP430I2040TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T	Samples
MSP430I2040TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2040T	Samples

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PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430I2041TPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T	Samples
MSP430I2041TPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T	Samples
MSP430I2041TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T	Samples
MSP430I2041TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	I2041T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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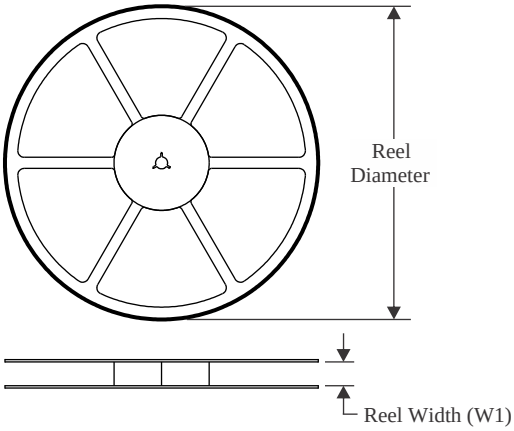
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

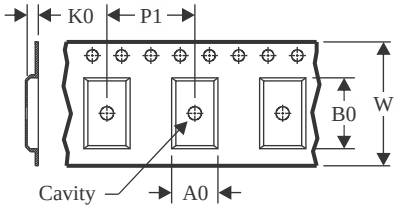
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

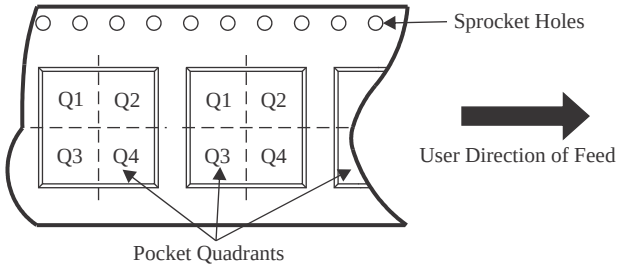


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

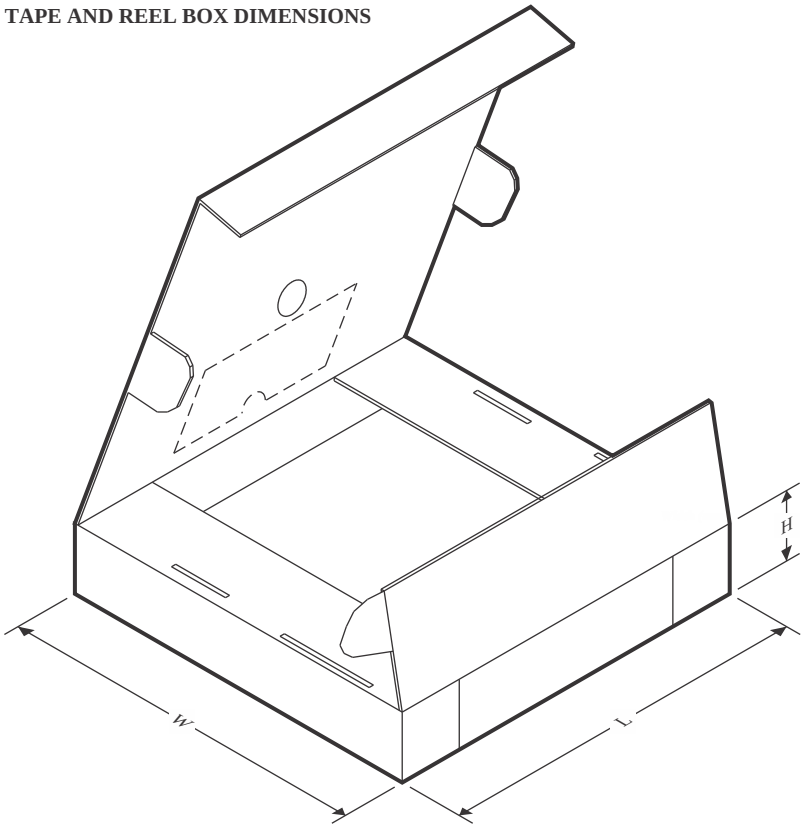
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430I2020TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2020TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2020TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2021TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2021TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2030TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2030TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2031TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2031TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2031TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2040TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430I2040TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2040TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2041TPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430I2041TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430I2041TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

TAPE AND REEL BOX DIMENSIONS

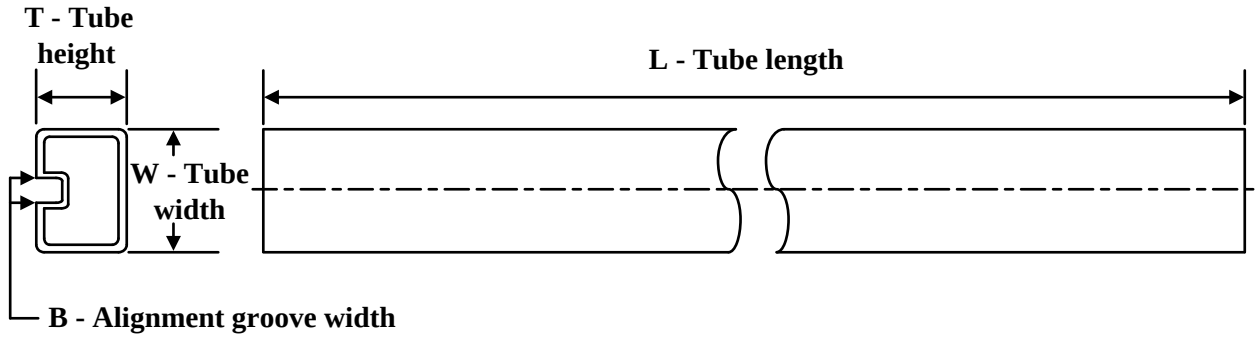


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430I2020TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2020TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2020TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2021TPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430I2021TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2021TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2030TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2030TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2030TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2031TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2031TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2031TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2040TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2040TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2040TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430I2041TPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430I2041TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430I2041TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430I2020TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2021TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2030TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2031TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2040TPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430I2041TPW	PW	TSSOP	28	50	530	10.2	3600	3.5

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

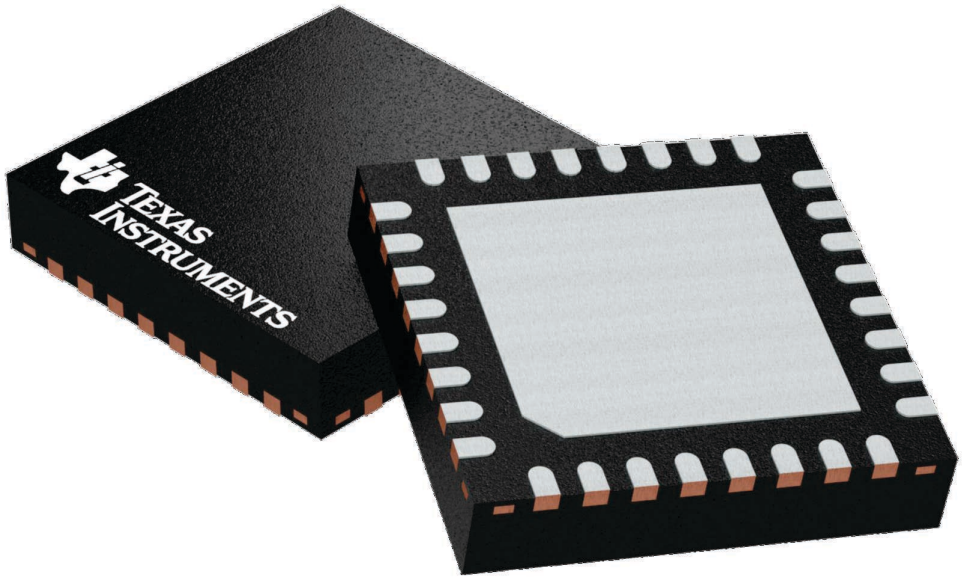
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

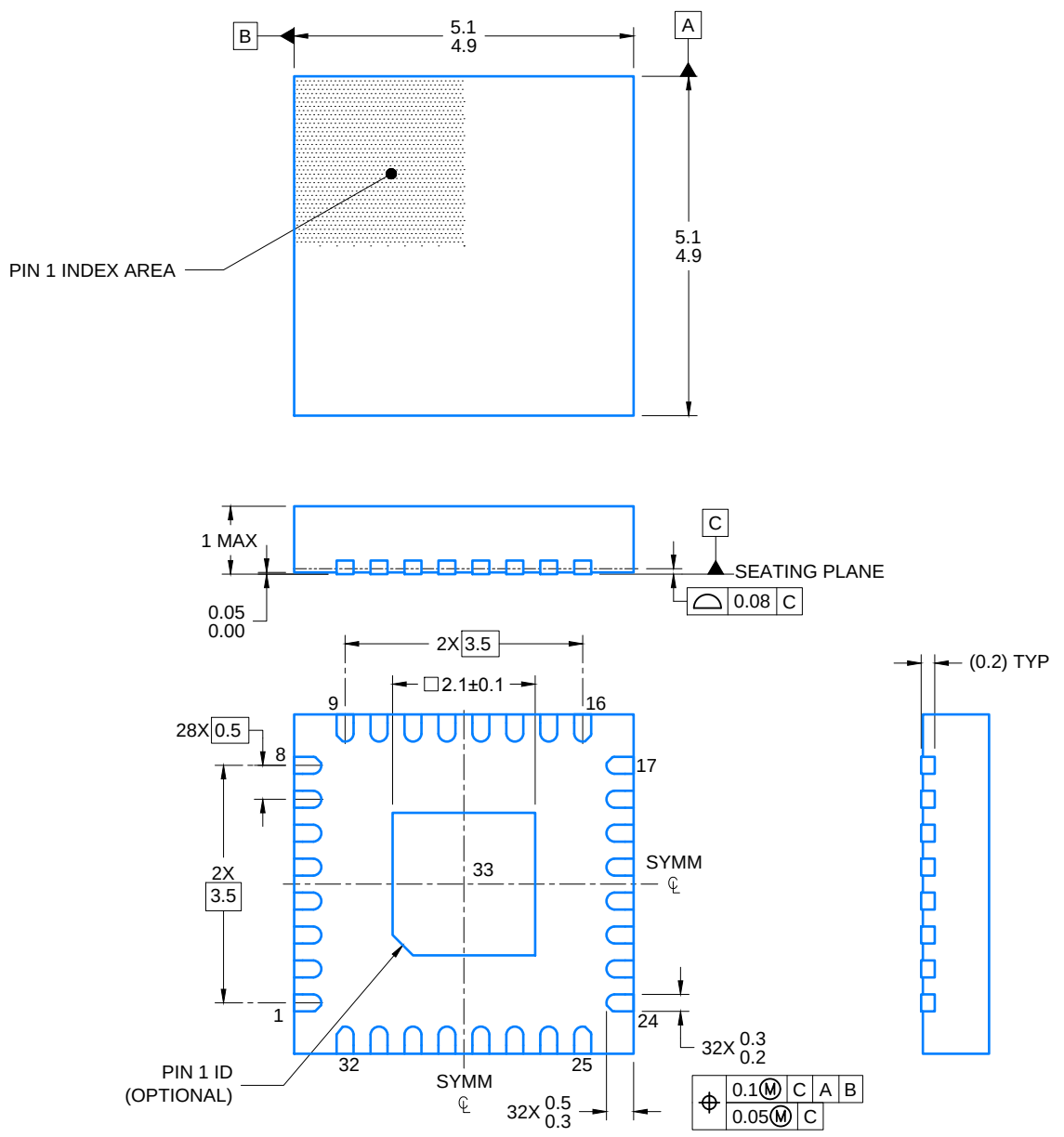
Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

PACKAGE OUTLINE

RHB0032M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

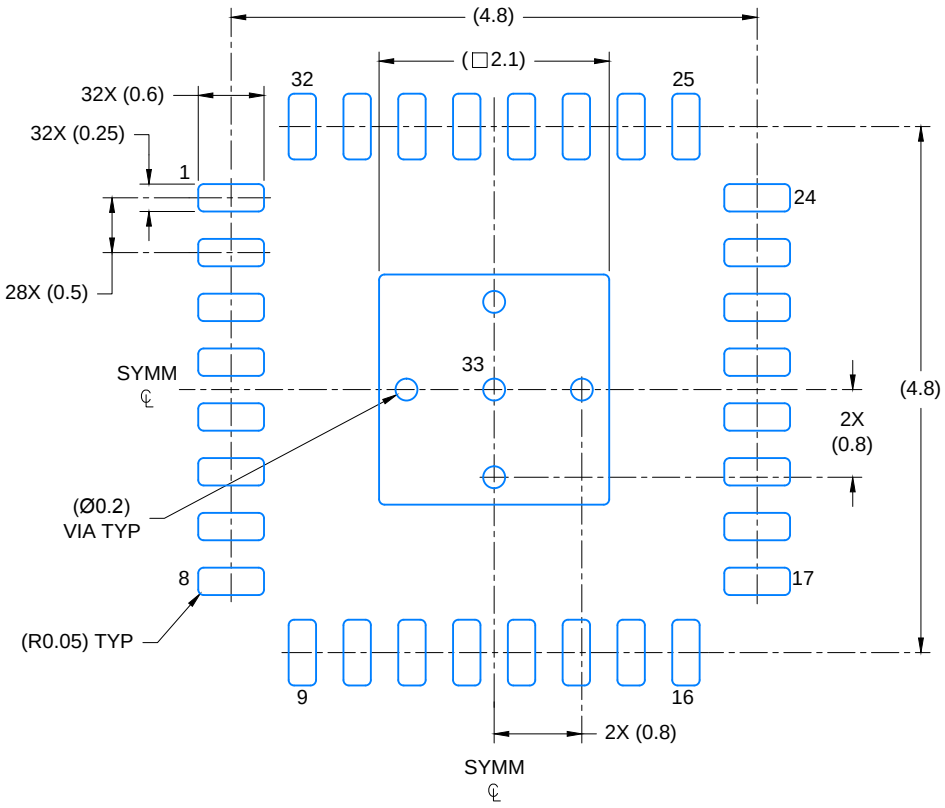
Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

EXAMPLE BOARD LAYOUT

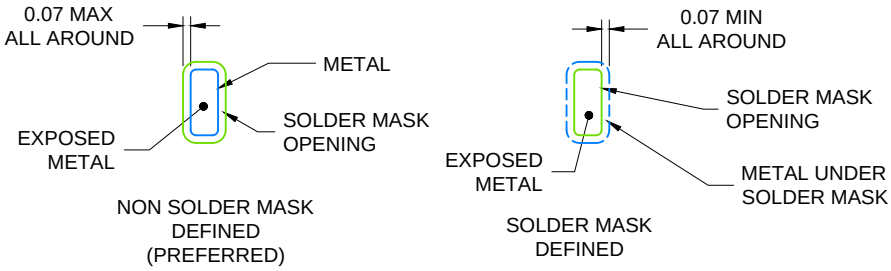
RHB0032M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4223725/A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

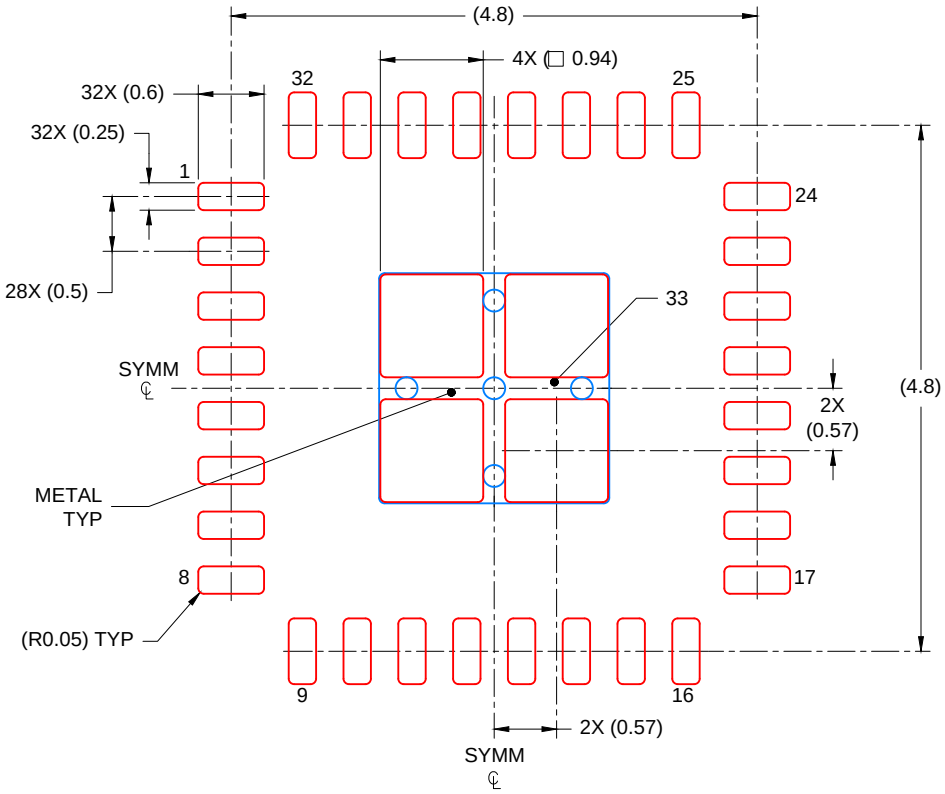
Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

EXAMPLE STENCIL DESIGN

RHB0032M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

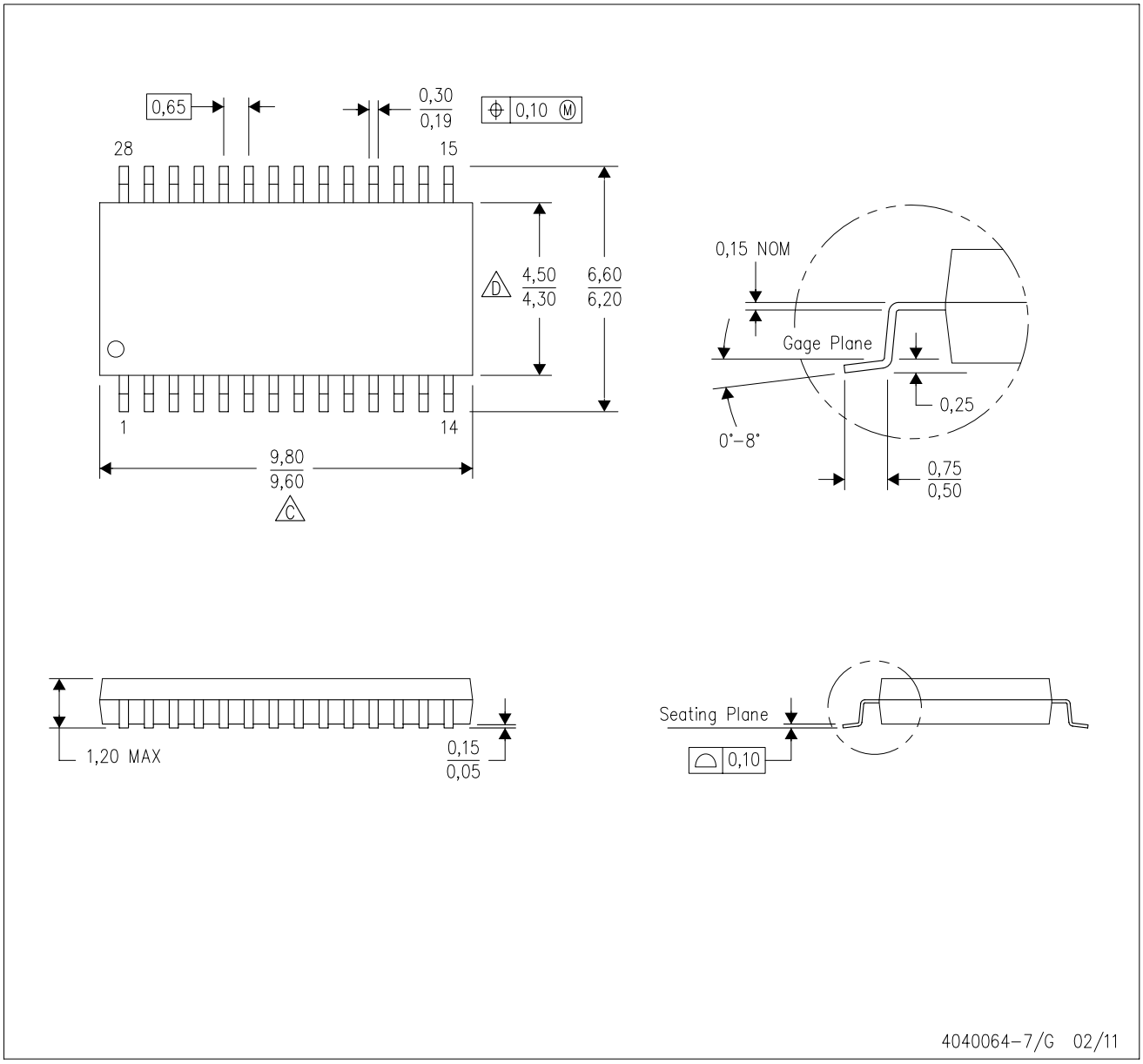
4223725/A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

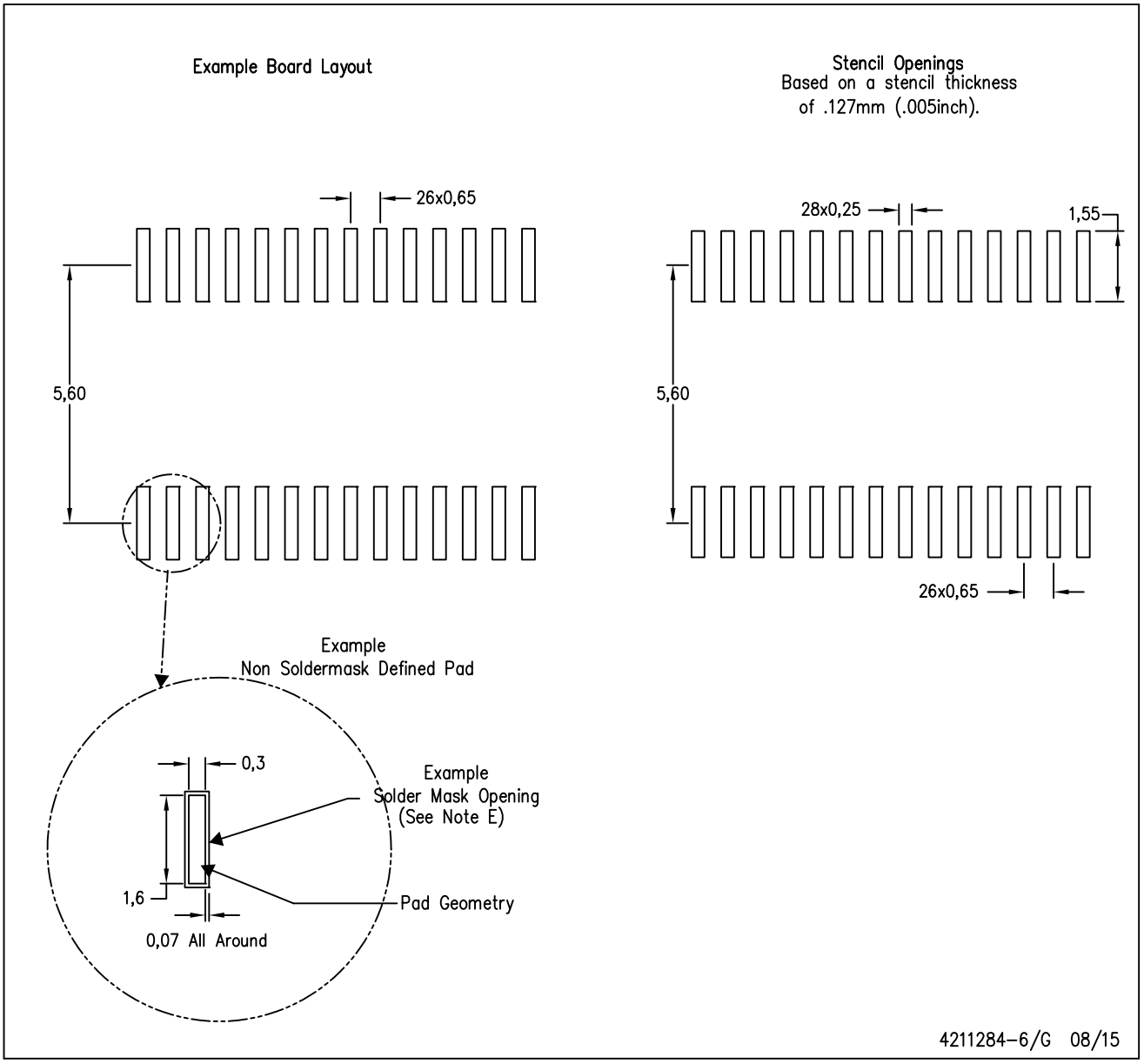
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

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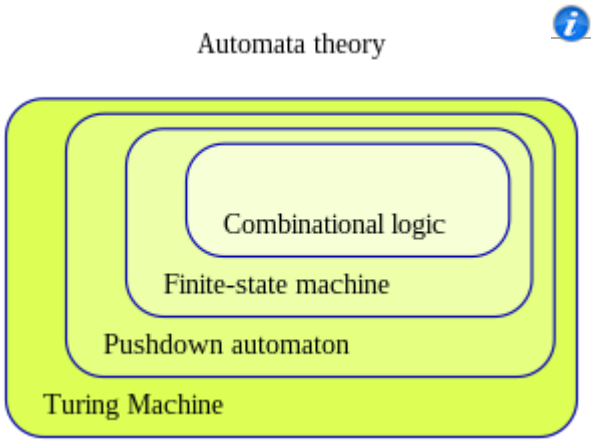
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Finite-state machine

A **finite-state machine** (**FSM**) or **finite-state automaton** (**FSA**, plural: *automata*), **finite automaton**, or simply a **state machine**, is a mathematical model of computation. It is an abstract machine that can be in exactly one of a finite number of *states* at any given time. The FSM can change from one state to another in response to some inputs; the change from one state to another is called a *transition*.[1] An FSM is defined by a list of its states, its initial state, and the inputs that trigger each transition. Finite-state machines are of two types—deterministic finite-state machines and non-deterministic finite-state machines.[2] A deterministic finite-state machine can be constructed equivalent to any non-deterministic one.



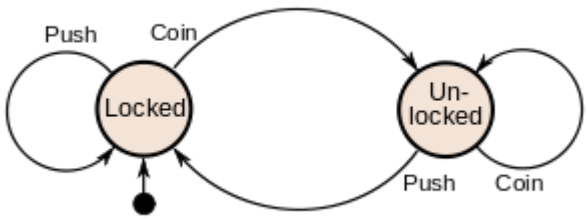
Classes of automata

The behavior of state machines can be observed in many devices in modern society that perform a predetermined sequence of actions depending on a sequence of events with which they are presented. Simple examples are: vending machines, which dispense products when the proper combination of coins is deposited; elevators, whose sequence of stops is determined by the floors requested by riders; traffic lights, which change sequence when cars are waiting; combination locks, which require the input of a sequence of numbers in the proper order.

The finite-state machine has less computational power than some other models of computation such as the Turing machine.[3] The computational power distinction means there are computational tasks that a Turing machine can do but an FSM cannot. This is because an FSM's memory is limited by the number of states it has. A finite-state machine has the same computational power as a Turing machine that is restricted such that its head may only perform "read" operations, and always has to move from left to right. FSMs are studied in the more general field of automata theory.

Example: coin-operated turnstile

An example of a simple mechanism that can be modeled by a state machine is a turnstile.[4][5] A turnstile, used to control access to subways and amusement park rides, is a gate with three rotating arms at waist height, one across the entryway. Initially the arms are locked, blocking the entry, preventing patrons from passing through. Depositing a coin or token in a slot on the turnstile unlocks the arms, allowing a single customer to push through. After the customer passes through, the arms are locked again until another coin is inserted.



State diagram for a turnstile

Considered as a state machine, the turnstile has two possible states: ***Locked*** and ***Unlocked***.[4] There are two possible inputs that affect its state: putting a coin in the slot (***coin***) and pushing the arm (***push***). In the locked state, pushing on the arm has no effect; no matter how many times the input ***push*** is given, it stays in the locked state. Putting a coin in – that is, giving the machine a ***coin*** input – shifts the state from ***Locked*** to ***Unlocked***. In the unlocked state, putting additional coins in has no effect; that is, giving additional ***coin*** inputs does not change the state. However, a customer pushing through the arms, giving a ***push*** input, shifts the state back to ***Locked***.



A turnstile

The turnstile state machine can be represented by a state-transition table, showing for each possible state, the transitions between them (based upon the inputs given to the machine) and the outputs resulting from each input:

Current State	Input	Next State	Output
Locked	coin	Unlocked	Unlocks the turnstile so that the customer can push through.
	push	Locked	None
Unlocked	coin	Unlocked	None
	push	Locked	When the customer has pushed through, locks the turnstile.

The turnstile state machine can also be represented by a directed graph called a state diagram *(above)*. Each state is represented by a node (*circle*). Edges (*arrows*) show the transitions from one state to another. Each arrow is labeled with the input that triggers that transition. An input that doesn't cause a change of state (such as a ***coin*** input in the ***Unlocked*** state) is represented by a circular arrow returning to the original state. The arrow into the ***Locked*** node from the black dot indicates it is the initial state.

Concepts and terminology

A *state* is a description of the status of a system that is waiting to execute a *transition*. A transition is a set of actions to be executed when a condition is fulfilled or when an event is received. For example, when using an audio system to listen to the radio (the system is in the "radio" state), receiving a "next" stimulus results in moving to the next station. When the system is in the "CD" state, the "next" stimulus results in moving to the next track. Identical stimuli trigger different actions depending on the current state.

In some finite-state machine representations, it is also possible to associate actions with a state:

- an entry action: performed *when entering* the state, and
- an exit action: performed *when exiting* the state.

Representations

State/Event table

Several state-transition table types are used. The most common representation is shown below: the combination of current state (e.g. B) and input (e.g. Y) shows the next state (e.g. C). The complete action's information is not directly described in the table and can only be added using footnotes. An FSM definition including the full action's information is possible using state tables (see also virtual finite-state machine).

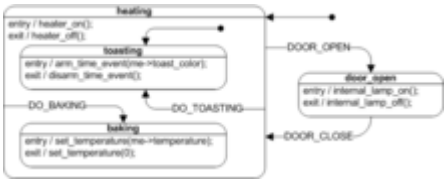


Fig. 1 UML state chart example (a toaster oven)

State-transition table

Current state / Input	State A	State B	State C
Input X	...	...	...
Input Y	...	State C	...
Input Z	...	...	...



Fig. 2 SDL state machine example

UML state machines

The Unified Modeling Language has a notation for describing state machines. UML state machines overcome the limitations of traditional finite-state machines while retaining their main benefits. UML state machines introduce the new concepts of hierarchically nested states and orthogonal regions, while extending the notion of actions. UML state machines have the characteristics of both Mealy machines and Moore machines. They support actions that depend on both the state of the system and the triggering event, as in Mealy machines, as well as entry and exit actions, which are associated with states rather than transitions, as in Moore machines.

SDL state machines

The Specification and Description Language is a standard from ITU that includes graphical symbols to describe actions in the transition:

- send an event
- receive an event
- start a timer
- cancel a timer
- start another concurrent state machine
- decision

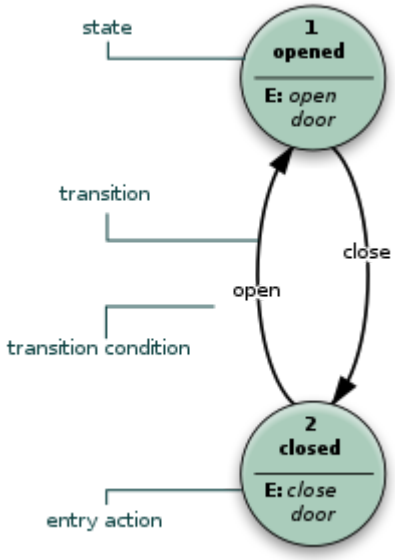


Fig. 3 Example of a simple finite-state machine

SDL embeds basic data types called "Abstract Data Types", an action language, and an execution semantic in order to make the finite-state machine executable.

Other state diagrams

There are a large number of variants to represent an FSM such as the one in figure 3.

Usage

In addition to their use in modeling reactive systems presented here, finite-state machines are significant in many different areas, including electrical engineering, linguistics, computer science, philosophy, biology, mathematics, video game programming, and logic. Finite-state machines are a class of automata studied in automata theory and the theory of computation. In computer science, finite-state machines are widely used in modeling of application behavior (control theory), design of hardware digital systems, software engineering, compilers, network protocols, and computational linguistics.

Classification

Finite-state machines can be subdivided into acceptors, classifiers, transducers and sequencers.[6]

Acceptors

Acceptors (also called **detectors** or **recognizers**) produce binary output, indicating whether or not the received input is accepted. Each state of an acceptor is either *accepting* or *non accepting*. Once all input has been received, if the current state is an accepting state, the input is accepted; otherwise it is rejected. As a rule, input is a sequence of symbols (characters); actions are not used. The start state can also be an accepting state, in which case the acceptor accepts the empty string. The example in figure 4 shows an acceptor that accepts the string "nice". In this acceptor, the only accepting state is state 7.

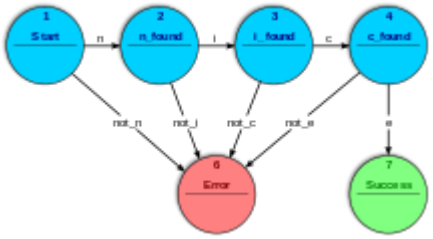


Fig. 4: Acceptor FSM: parsing the string "nice".

A (possibly infinite) set of symbol sequences, called a formal language, is a regular language if there is some acceptor that accepts *exactly* that set. For example, the set of binary strings with an even number of zeroes is a regular language (cf. Fig. 5), while the set of all strings whose length is a prime number is not.[7]:18,71

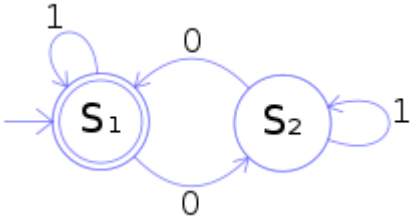


Fig. 5: Representation of an acceptor; this example shows one that determines whether a binary number has an even number of 0s, where S_1 is an *accepting state* and S_2 is a *non accepting state*.

An acceptor could also be described as defining a language that would contain every string accepted by the acceptor but none of the rejected ones; that language is *accepted* by the acceptor. By definition, the languages accepted by acceptors are the regular languages.

The problem of determining the language accepted by a given acceptor is an instance of the algebraic path problem—itself a generalization of the shortest path problem to graphs with edges weighted by the elements of an (arbitrary) semiring.[8][9]

An example of an accepting state appears in Fig. 5: a deterministic finite automaton (DFA) that detects whether the binary input string contains an even number of 0s.

S_1 (which is also the start state) indicates the state at which an even number of 0s has been input. S_1 is therefore an accepting state. This acceptor will finish in an accept state, if the binary string contains an even number of 0s (including any binary string containing no 0s). Examples of strings accepted by this acceptor are ε (the empty string), 1, 11, 11..., 00, 010, 1010, 10110, etc.

Classifiers

Classifiers are a generalization of acceptors that produce *n*-ary output where *n* is strictly greater than two.[10]

Transducers

Transducers produce output based on a given input and/or a state using actions. They are used for control applications and in the field of computational linguistics.

In control applications, two types are distinguished:

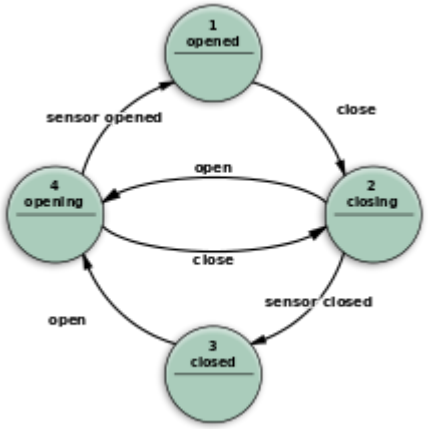


Fig. 6 Transducer FSM: Moore model example

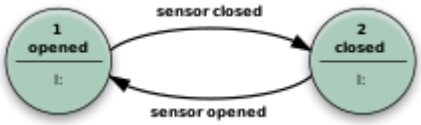


Fig. 7 Transducer FSM: Mealy model example

Moore machine

The FSM uses only entry actions, i.e., output depends only on state. The advantage of the Moore model is a simplification of the behaviour. Consider an elevator door. The state machine recognizes two commands: "command_open" and "command_close", which trigger state changes. The entry action (E:) in state "Opening" starts a motor opening the door, the entry action in state "Closing" starts a motor in the other direction closing the door. States "Opened" and "Closed" stop the motor when fully opened or closed. They signal to the outside world (e.g., to other state machines) the situation: "door is open" or "door is closed".

Mealy machine

The FSM also uses input actions, i.e., output depends on input and state. The use of a Mealy FSM leads often to a reduction of the number of states. The example in figure 7 shows a Mealy FSM implementing the same behaviour as in the Moore example (the behaviour depends on the implemented FSM execution model and will work, e.g., for virtual FSM but not for event-driven FSM). There are two input actions (I:): "start motor to close the door if command_close arrives"

and "start motor in the other direction to open the door if command_open arrives". The "opening" and "closing" intermediate states are not shown.

Sequencers

Sequencers (also called **generators**) are a subclass of acceptors and transducers that have a single-letter input alphabet. They produce only one sequence, which can be seen as an output sequence of acceptor or transducer outputs.[6]

Determinism

A further distinction is between **deterministic** (DFA) and **non-deterministic** (NFA, GNFA) automata. In a deterministic automaton, every state has exactly one transition for each possible input. In a non-deterministic automaton, an input can lead to one, more than one, or no transition for a given state. The powerset construction algorithm can transform any nondeterministic automaton into a (usually more complex) deterministic automaton with identical functionality.

A finite-state machine with only one state is called a "combinatorial FSM". It only allows actions upon transition *into* a state. This concept is useful in cases where a number of finite-state machines are required to work together, and when it is convenient to consider a purely combinatorial part as a form of FSM to suit the design tools.[11]

Alternative semantics

There are other sets of semantics available to represent state machines. For example, there are tools for modeling and designing logic for embedded controllers.[12] They combine hierarchical state machines (which usually have more than one current state), flow graphs, and truth tables into one language, resulting in a different formalism and set of semantics.[13] These charts, like Harel's original state machines,[14] support hierarchically nested states, orthogonal regions, state actions, and transition actions.[15]

Mathematical model

In accordance with the general classification, the following formal definitions are found.

A *deterministic finite-state machine* or *deterministic finite-state acceptor* is a quintuple $(\Sigma, S, s_0, \delta, F)$, where:

- Σ is the input alphabet (a finite non-empty set of symbols);
- S is a finite non-empty set of states;
- s_0 is an initial state, an element of S;
- δ is the state-transition function: $\delta : S \times \Sigma \to S$ (in a nondeterministic finite automaton it would be $\delta : S \times \Sigma \to \mathcal{P}(S)$, i.e. δ would return a set of states);
- F is the set of final states, a (possibly empty) subset of S.

For both deterministic and non-deterministic FSMs, it is conventional to allow δ to be a partial function, i.e. $\delta(s, x)$ does not have to be defined for every combination of $s \in S$ and $x \in \Sigma$. If an FSM M is in a state s, the next symbol is x and $\delta(s, x)$ is not defined, then M can announce an error (i.e. reject the input). This is useful in definitions of general state machines, but less useful when transforming the machine. Some algorithms in their default form may require total functions.

A finite-state machine has the same computational power as a Turing machine that is restricted such that its head may only perform "read" operations, and always has to move from left to right. That is, each formal language accepted by a finite-state machine is accepted by such a kind of restricted Turing machine, and vice versa.[16]

A *finite-state transducer* is a sextuple $(\Sigma, \Gamma, S, s_0, \delta, \omega)$, where:

- Σ is the input alphabet (a finite non-empty set of symbols);
- Γ is the output alphabet (a finite non-empty set of symbols);
- S is a finite non-empty set of states;
- s_0 is the initial state, an element of S;
- δ is the state-transition function: $\delta : S \times \Sigma \rightarrow S$;
- ω is the output function.

If the output function depends on the state and input symbol ($\omega : S \times \Sigma \rightarrow \Gamma$) that definition corresponds to the *Mealy model*, and can be modelled as a Mealy machine. If the output function depends only on the state ($\omega : S \rightarrow \Gamma$) that definition corresponds to the *Moore model*, and can be modelled as a Moore machine. A finite-state machine with no output function at all is known as a semiautomaton or transition system.

If we disregard the first output symbol of a Moore machine, $\omega(s_0)$, then it can be readily converted to an output-equivalent Mealy machine by setting the output function of every Mealy transition (i.e. labeling every edge) with the output symbol given of the destination Moore state. The converse transformation is less straightforward because a Mealy machine state may have different output labels on its incoming transitions (edges). Every such state needs to be split in multiple Moore machine states, one for every incident output symbol.[17]

Optimization

Optimizing an FSM means finding a machine with the minimum number of states that performs the same function. The fastest known algorithm doing this is the Hopcroft minimization algorithm.[18][19] Other techniques include using an implication table, or the Moore reduction procedure.[20] Additionally, acyclic FSAs can be minimized in linear time.[21]

Implementation

Hardware applications

In a digital circuit, an FSM may be built using a programmable logic device, a programmable logic controller, logic gates and flip flops or relays. More specifically, a hardware implementation requires a register to store state variables, a block of combinational logic that determines the state transition,

and a second block of combinational logic that determines the output of an FSM. One of the classic hardware implementations is the Richards controller.

In a *Medvedev machine*, the output is directly connected to the state flip-flops minimizing the time delay between flip-flops and output.[22][23]

Through state encoding for low power state machines may be optimized to minimize power consumption.

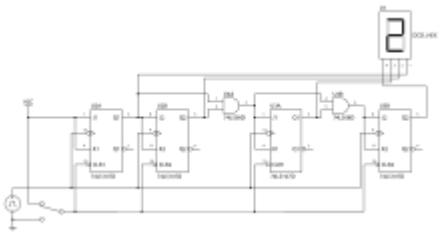


Fig. 9 The circuit diagram for a 4-bit TTL counter, a type of state machine

Software applications

The following concepts are commonly used to build software applications with finite-state machines:

- Automata-based programming
- Event-driven finite-state machine
- Virtual finite-state machine
- State design pattern

Finite-state machines and compilers

Finite automata are often used in the frontend of programming language compilers. Such a frontend may comprise several finite-state machines that implement a lexical analyzer and a parser. Starting from a sequence of characters, the lexical analyzer builds a sequence of language tokens (such as reserved words, literals, and identifiers) from which the parser builds a syntax tree. The lexical analyzer and the parser handle the regular and context-free parts of the programming language's grammar.[24]

See also

- Abstract state machines
- Alternating finite automaton
- Communicating finite-state machine
- Control system
- Control table
- Decision tables
- DEVS
- Hidden Markov model
- Petri net
- Pushdown automaton
- Quantum finite automaton
- SCXML
- Semiautomaton
- Semigroup action
- Sequential logic
- State diagram
- Synchronizing word
- Transformation semigroup
- Transition system
- Tree automaton
- Turing machine
- UML state machine

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Finite Markov chain processes

> "We may think of a Markov chain as a process that moves successively through a set of states s_1, s_2, …, s_r. … if it is in state s_i it moves on to the next stop to state s_j with probability p_{ij}. These probabilities can be exhibited in the form of a transition matrix" (Kemeny (1959), p. 384)

Finite Markov-chain processes are also known as subshifts of finite type.

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External links

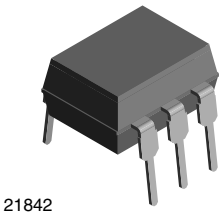
- Finite State Automata (https://curlie.org/Computers/Computer_Science/Theoretical/Automata_Theory/Finite_State_Automata/) at Curlie
- *Modeling a Simple AI behavior using a Finite State Machine* (https://archive.today/20121202054532/http://blog.manuvra.com/modeling-a-simple-ai-behavior-using-a-finite-state-machine/) Example of usage in Video Games
- Free On-Line Dictionary of Computing (https://web.archive.org/web/20171211180457/http://foldoc.org/finite+state+machine) description of Finite-State Machines
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- A brief overview of state machine types (https://blogs.itemis.com/en/a-brief-overview-of-state-machine-types), comparing theoretical aspects of Mealy, Moore, Harel & UML state machines.

Retrieved from "https://en.wikipedia.org/w/index.php?title=Finite-state_machine&oldid=1145287359"

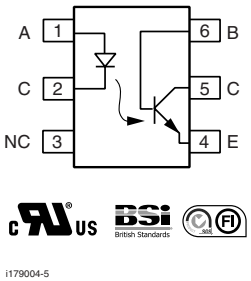
4N25, 4N26, 4N27, 4N28

Vishay Semiconductors

Optocoupler, Phototransistor Output, with Base Connection



21842



FEATURES

- Isolation test voltage 5000 V_{RMS}
- Interfaces with common logic families
- Input-output coupling capacitance < 0.5 pF
- Industry standard dual-in-line 6 pin package
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Pb-free

e3

RoHS COMPLIANT

APPLICATIONS

- AC mains detection
- Reed relay driving
- Switch mode power supply feedback
- Telephone ring detection
- Logic ground isolation
- Logic coupling with high frequency noise rejection

AGENCY APPROVALS

- UL1577, file no. E52744
- BSI: EN 60065:2002, EN 60950:2000
- FIMKO: EN 60950, EN 60065, EN 60335

DESCRIPTION

The 4N25 family is an industry standard single channel phototransistor coupler. This family includes the 4N25, 4N26, 4N27, 4N28. Each optocoupler consists of gallium arsenide infrared LED and a silicon NPN phototransistor.

ORDER INFORMATION	
PART	**REMARKS**
4N25	CTR > 20 %, DIP-6
4N26	CTR > 20 %, DIP-6
4N27	CTR > 10 %, DIP-6
4N28	CTR > 10 %, DIP-6

ABSOLUTE MAXIMUM RATINGS (1)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
INPUT				
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Surge current	t ≤ 10 µs	I_{FSM}	3	A
Power dissipation		P_{diss}	100	mW
OUTPUT				
Collector emitter breakdown voltage		V_{CEO}	70	V
Emitter base breakdown voltage		V_{EBO}	7	V
Collector current		I_C	50	mA
	t ≤ 1 ms	I_C	100	mA
Power dissipation		P_{diss}	150	mW

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

ABSOLUTE MAXIMUM RATINGS (1)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
COUPLER				
Isolation test voltage		V_{ISO}	5000	V_{RMS}
Creepage distance			≥ 7	mm
Clearance distance			≥ 7	mm
Isolation thickness between emitter and detector			≥ 0.4	mm
Comparative tracking index	DIN IEC 112/VDE 0303, part 1		175	
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}	Ω
Storage temperature		T_{stg}	- 55 to + 125	°C
Operating temperature		T_{amb}	- 55 to + 100	°C
Junction temperature		T_j	125	°C
Soldering temperature (2)	max.10 s dip soldering: distance to seating plane ≥ 1.5 mm	T_{sld}	260	°C

Notes

(1) T_{amb} = 25 °C, unless otherwise specified.
Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

(2) Refer to reflow profile for soldering conditions for surface mounted devices (SMD). Refer to wave profile for soldering condditions for through hole devices (DIP).

ELECTRICAL CHARACTERISTICS (1)							
PARAMETER	**TEST CONDITION**	**PART**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
INPUT							
Forward voltage (2)	I_F = 50 mA		V_F		1.3	1.5	V
Reverse current (2)	V_R = 3 V		I_R		0.1	100	µA
Capacitance	V_R = 0 V		C_O		25		pF
OUTPUT							
Collector base breakdown voltage (2)	I_C = 100 µA		BV_{CBO}	70			V
Collector emitter breakdown voltage (2)	I_C = 1 mA		BV_{CEO}	30			V
Emitter collector breakdown voltage (2)	I_E = 100 µA		BV_{ECO}	7			V
I_{CEO}(dark) (2)	V_{CE} = 10 V, (base open)	4N25			5	50	nA
		4N26			5	50	nA
		4N27			5	50	nA
		4N28			10	100	nA
I_{CBO}(dark) (2)	V_{CB} = 10 V, (emitter open)				2	20	nA
Collector emitter capacitance	V_{CE} = 0		C_{CE}		6		pF
COUPLER							
Isolation test voltage (2)	Peak, 60 Hz		V_{IO}	5000			V
Saturation voltage, collector emitter	I_{CE} = 2 mA, I_F = 50 mA		$V_{CE(sat)}$			0.5	V
Resistance, input output (2)	V_{IO} = 500 V		R_{IO}	100			GΩ
Capacitance, input output	f = 1 MHz		C_{IO}		0.6		pF

Notes

(1) T_{amb} = 25 °C, unless otherwise specified.
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

(2) JEDEC registered values are 2500 V, 1500 V, 1500 V, and 500 V for the 4N25, 4N26, 4N27, and 4N28 respectively.

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CURRENT TRANSFER RATIO (1)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC current transfer ratio	V_{CE} = 10 V, I_F = 10 mA	4N25	CTR_{DC}	20	50		%
		4N26	CTR_{DC}	20	50		%
		4N27	CTR_{DC}	10	30		%
		4N28	CTR_{DC}	10	30		%

Note

(1) Indicates JEDEC registered values.

SWITCHING CHARACTERISTICS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Rise and fall times	V_{CE} = 10 V, I_F = 10 mA, R_L = 100 Ω	t_r, t_f		2		µs

TYPICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

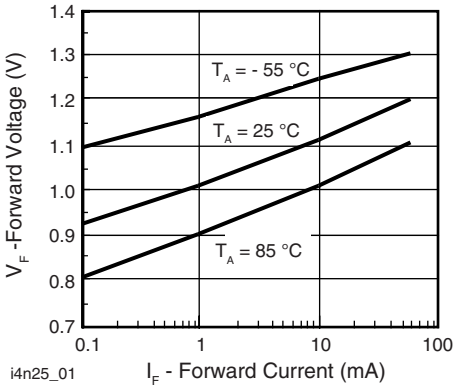


Fig. 1 - Forward Voltage vs. Forward Current

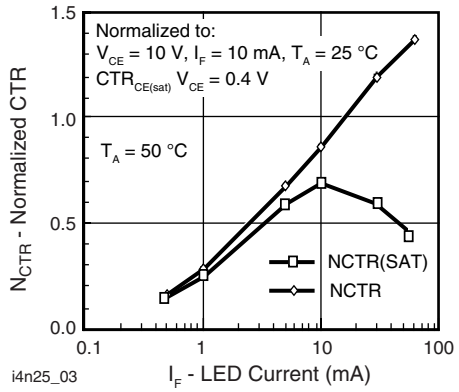


Fig. 3 - Normalized Non-Saturated and Saturated CTR vs. LED Current

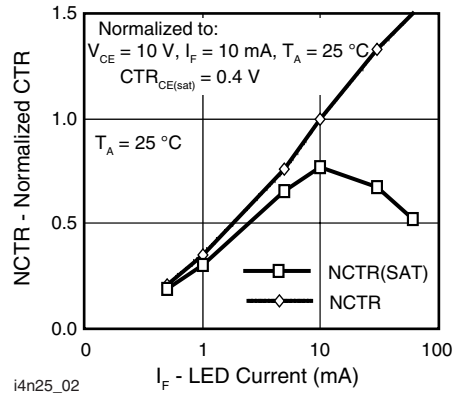


Fig. 2 - Normalized Non-Saturated and Saturated CTR vs. LED Current

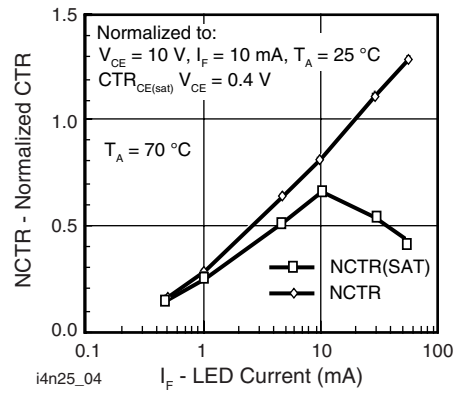


Fig. 4 - Normalized Non-Saturated and Saturated CTR vs. LED Current

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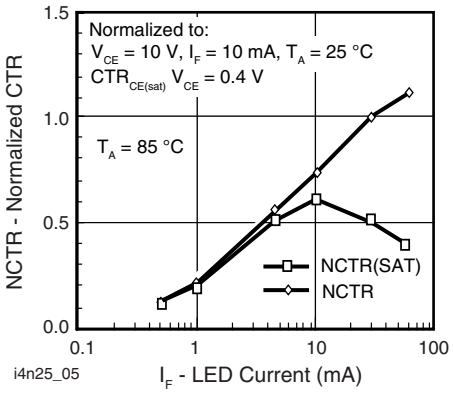


Fig. 5 - Normalized Non-Saturated and Saturated CTR vs. LED Current

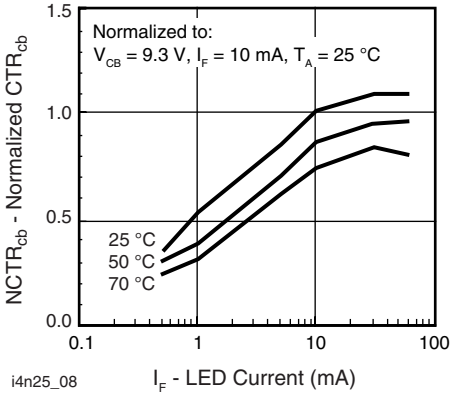


Fig. 8 - Normalized CTRcb vs. LED Current and Temperature

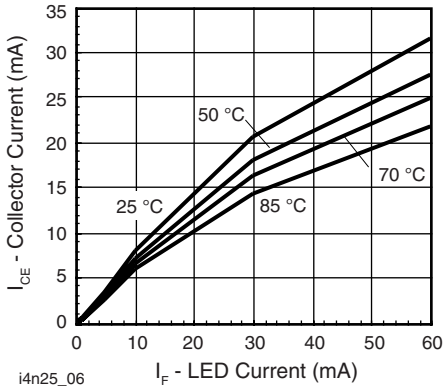


Fig. 6 - Collector Emitter Current vs. Temperature and LED Current

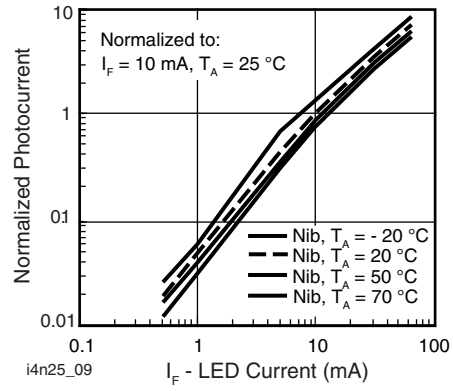


Fig. 9 - Normalized Photocurrent vs. I_F and Temperature

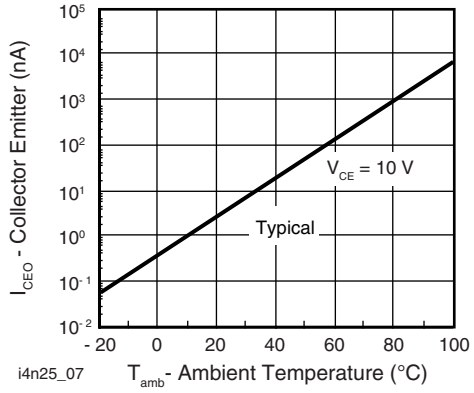


Fig. 7 - Collector Emitter Leakage Current vs. Temperature

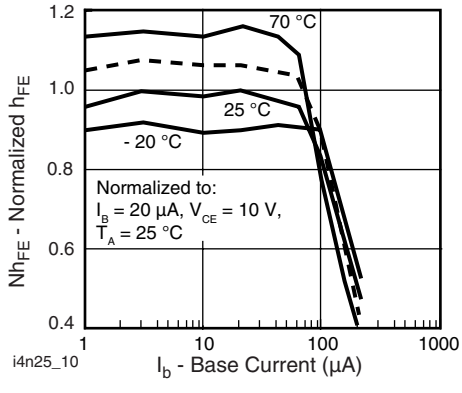


Fig. 10 - Normalized Non-Saturated h_{FE} vs. Base Current and Temperature

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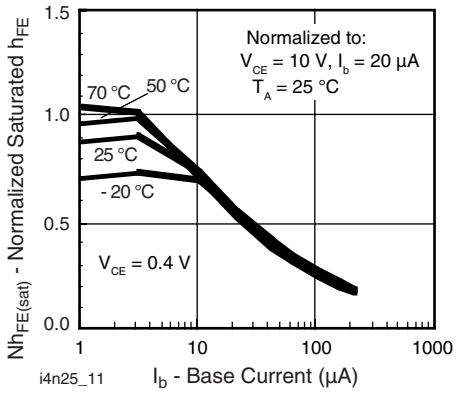


Fig. 11 - Normalized h_{FE} vs. Base Current and Temperature

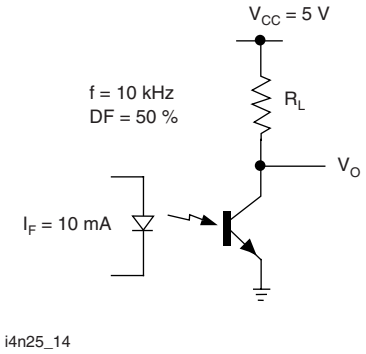


Fig. 14 - Switching Schematic

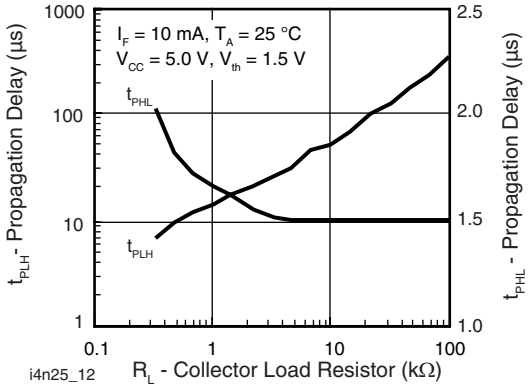


Fig. 12 - Propagation Delay vs. Collector Load Resistor

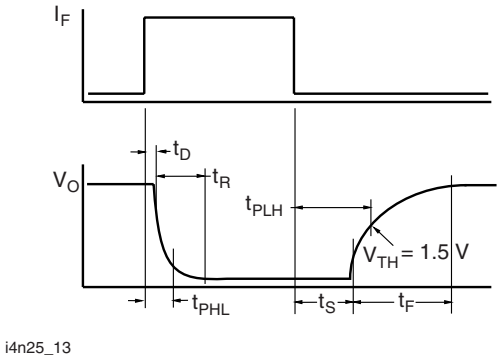
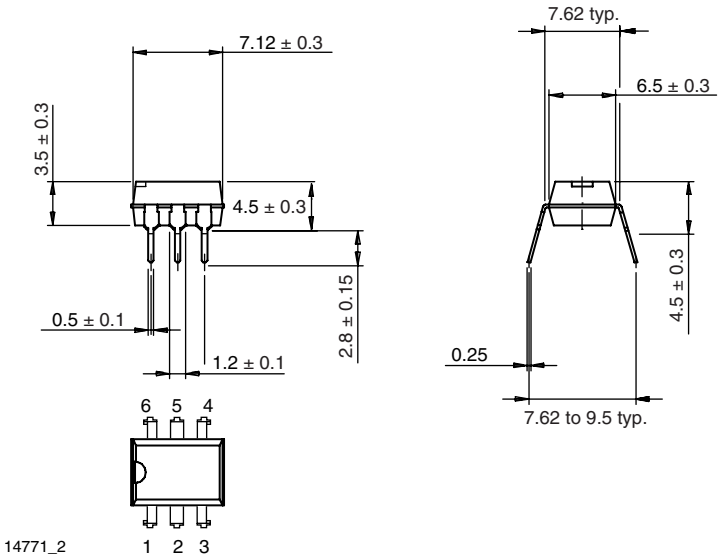


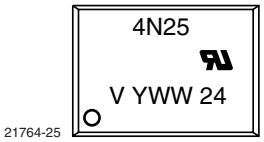
Fig. 13 - Switching Timing

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PACKAGE DIMENSIONS in millimeters



PACKAGE MARKING



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in ELECTRONIC COMPONENTS

Optocoupler devices and application

JANUARY 23, 2011

An optocoupler (or an optoelectronic coupler) is basically an interface between two circuits which operate at (usually) different voltage levels. The key advantage of an optocoupler is the electrical isolation between the input and output circuits. With an optocoupler, the only contact between the input and the output is a beam of light. Because of this it is possible to have an insulation resistance between the two circuits in the thousands of megohms. Isolation like this is useful in high voltage applications where the potentials of two circuits may differ by several thousand volts.

The most common industrial use of the optocouplers (or optically-coupled isolators) is as a signal converter between high-voltage pitot devices (limit switches etc.) and low voltage solid-state logic circuits. Optical isolators can be employed in any situation where a signal must be passed between two circuits which are isolated from each other. Complete electrical isolation between two circuits (i.e. the two circuits have no conductors in common) is often necessary to prevent noise generated in one circuit from being passed to the other circuit. This is especially necessary for the coupling between high-voltage information-gathering circuits and low-voltage digital logic circuits. The information circuits are almost badly exposed to noise sources and the logic circuits cannot tolerate noise signals.

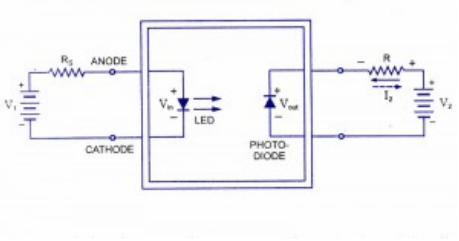
In many applications SCR and triac power circuits are under the control of sensitive electronic systems. For example, it is not unusual to have a microprocessor system programmed to turn motors, lights, and heaters on and off. To reduce the possibility of power-line noise being induced into the control electronics, and to protect it in the event of an SCR or triac failure, it is highly desirable to provide isolation.

The ideal isolation scheme should only allow signal flow in one direction, should respond to dc levels, and should offer an extremely large resistance between the input and output circuits. These features are available in a class of optoelectronic devices called *optocouplers* or *optoisolators.*

The optical coupling method eliminates the need for a relay-controlled contact or an isolating transformer, which are traditional methods of providing electrical isolation between circuits. The optical coupling method is superior in many applications, because it gets rid of some of the less desirable features of relays and transformers.

The optocouplers works well on either ac or dc high-voltage signals. For this reason, signal converters employing optical coupling are sometimes referred to the *universal* signal converters.

The optocoupler is a device that contains an infra-red LED and a photodetector (such as a photodiode, phototransistor, Darlington pair, SCR or triac) combined in one package.

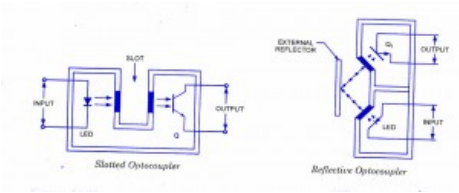


optocoupler

An autocoupler combining a LED and a photodiode in a single package is shown in figure. It has a LED on the input side and a photodiode on the output side. The left source voltage and the series resistor set up a current through the LED. Then the. light from the LED impinges on the photo-diode, and this sets up a reverse current in the output circuit. This reverse current develops a voltage across the output resistor R. The output

voltage then equals the output supply voltage V_2 minus the voltage drop across the load resistor R. When the input voltage is varied, the amount of light fluctuates.

Types of Optocouplers:

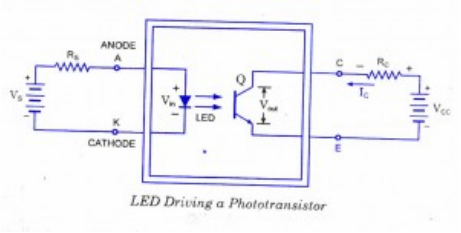


reflective-slotted-optocoupler

1. Slotted Optocoupler – A *slotted optocoupler* has a slot moulded into the package between the LED light source and the phototransistor light sensor; the slot houses transparent windows, so that the LED light can normally freely reach the face of transistor , but can be interrupted or blocked via opaque object placed within the slot. The slotted optocoupler can thus be employed in a variety of presence detecting applications, including end-of-tape detection, limit switching, and liquid level detection.

2. Reflective Optocoupler – Here the LED and phototransistor are optically screened from each other within the package, and both face outwards (in same direction) from the package. The construction is such that an optocoupled link can be set up by a reflective object (such as metallic paint or tape, or even smoke particles) placed a short distance outside the package, in line with both the LED . The reflective coupler can thus be employed in applications such as tape-position detection, engine-shaft revolution counting or speed measurement, or smoke or fog detection etc.

Characteristics of an Optocoupler:



optocoupler-characteristics

Current Transfer Ratio (CTR). One of the most important parameters of an optocoupler device is its optocoupling efficiency. This parameter is maximized by closely matching spectrally the LED and the phototransistor (which usually operate in the infra-red range). The optocoupling efficiency of an optocoupler may be conveniently specified by the output-to-input *current transfer ratio* (CTR) i.e., the ratio of the output current I_C (measured at the collector terminal of the phototransistor), to the input current I_F flowing into the LED.

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Input-to-Output Isolation Voltage (V_{iso}). This is the maximum potential difference (dc) that can be allowed to exist between the input and output terminals. Typical values range

from 500 V to 4 kV.

Maximum Collector-Emitter Voltage, V_{CE} (max). This is the maximum allowable dc voltage that can be applied across the output transistor. Typical values may vary from 20 to 80 volts.

Bandwidth. This is the typical maximum signal frequency (in kHz) that can be usefully passed through the optocoupler when the device is operated in its normal mode. Typical values vary from 20 to 500 kHz, depending on the type of device construction.

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Response Time. Divided into rise time t_r and fall time *t*.* For a phototransistor output stages, t_r and *tr* are usually around 2 to 5 us.

A **simple isolating optocoupler** uses a single phototransistor output stage and is usually housed in a six-pin package, with the base terminal of the phototransistor externally available. In normal use the base is left open circuit, and under such a condition the optocoupler has a minimum CTR value of 20 % and a useful bandwidth of 300 kHz.

How to Select the Right Galvanic Isolation Technology for IoT Sensors

By Bill Schweber
Contributed By Digi-Key's North American Editors
2017-12-07

The growth of diverse, new IoT applications has exposed many designers to the challenge of providing galvanic (ohmic) isolation between the sensor and the rest of the electronics. This isolation is critical for signal integrity, system protection, and user safety, but designers have to pick from three main isolation technologies: magnetic, optical, and capacitive barriers.

Each of these options has similar performance characteristics, but have subtle differences that designers need to appreciate before choosing between them. To that end, this article will discuss the role of isolation in sensors, before introducing the various options, their different characteristics, and how to apply them.

It will also introduce digital isolation, and provide further examples of digital isolators.

The essentials of isolation

When a sensor or sensor sub circuit is “isolated”, there is no electrical path between it and the rest of the circuit, and a basic measurement using an ohmmeter would show no current flow between the two sections (Figure 1). As a consequence of this barrier, the challenge is to get signal from the isolated sub circuit to the rest of the system. In many cases, there’s an additional challenge: provide power to the isolated sub circuit without having a “sneak-around path” via the power supply subsystem, which will negate any isolation.

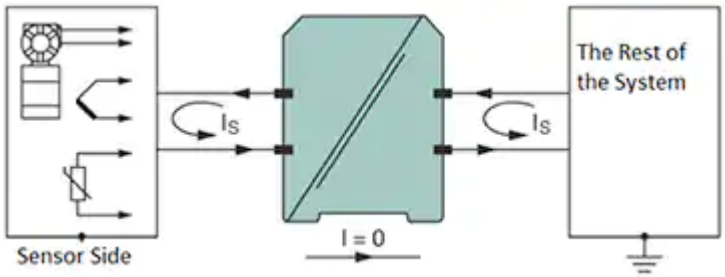


Figure 1: In an isolated system there is no current path between the ungrounded sensor and system (which may be grounded), yet information bearing energy of some type must get from one side to the other. (Image source: Digi-Key, based on original material at www.ee.co.za)

Reasons for isolation include:

- The sensor is “floating” and must not have any connection with the system “ground” (system “common” is a more accurate term, but “ground” is the commonly used misnomer here).

- Even if the system is battery operated and so has no connection to “AC ground”, the sensor output may, if it is on top of a high common-mode voltage (CMV). This CMV will damage the rest of the electronics. For example, the voltage of a single battery cell which is at the top of a series stack.
- The sensor may inadvertently get connected to a high-voltage source or even the AC line. This will not only damage the electronics, but also puts users at risk.

Fortunately, there are viable options for implementing analog sensor isolation that provide both low-level and high-level isolation, from tens of volts up to thousands of volts. The latter is needed in mass-market applications such as EV/HEVs, and often for regulatory safety mandates. The three most common approaches for providing isolation use magnetic, optical, and capacitive techniques, with each rated to >1000 V and higher.

These techniques have significant overlap in their primary performance attributes, but also some differences. The decision about which one is most appropriate in the application is often a difficult one.

Among the factors to consider are bandwidth, size and footprint, cost, isolation rating (volts), longevity rating, and personal “comfort.” Finding the right balance of performance parameters depends on the application. Battery monitoring, for example, does not need a fast response, while a high-speed test sensor does.

Magnetic isolation: The starting point

Magnetic-based isolation uses a transformer and is the oldest technique; for many years it was the only technique. The isolation transformer usually has a 1:1 turns ratio and can be fairly small, as it is handing signals rather than power, and dissipation is quite low.

Since a transformer cannot pass DC, nor can it handle very low frequencies well (unless it has a large core), the signal to be isolated cannot be applied directly to the primary (input) side. Instead, the sensor signal is amplified, if need be, and then used to modulate a carrier at much higher frequency (amplitude modulation), or used for pulse-width modulation (PWM).

On the output (secondary) side, the signal is demodulated using conventional techniques to extract and recover the original signal. Isolated power must be provided to the primary side, so there is usually a separate, dedicated, isolated side supply while the output side uses the system rail.

An early drop-in isolated op amp is the AD215 from Analog Devices (Figure 2). Its functionality looks like that of a non-isolated op amp, but it offers 1500 V (rms) isolation and 120 kHz bandwidth. It contains a signal modulator, transformer, and signal demodulator, as well as an isolated DC power supply. All are needed to provide galvanic isolation yet allow analog signals to pass from input side to output side.

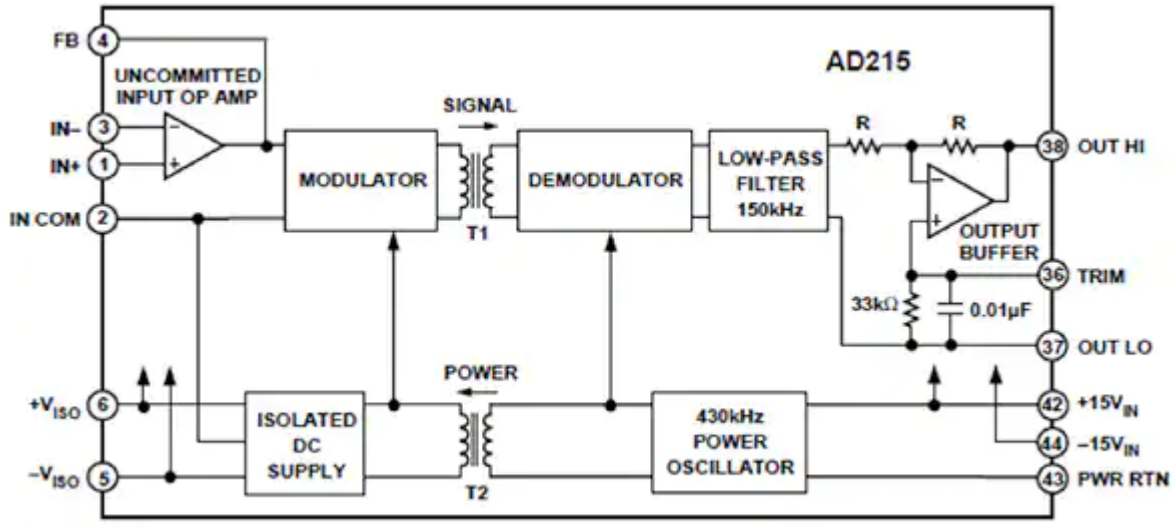


Figure 2: Within the AD215 magnetic isolator are a signal modulator, transformer, and signal demodulator, plus an isolated DC power supply. (Image source: Analog Devices)

The device has a ±10 volt (V) input/output range with a specified gain range of 1 V/V to 10 V/V, and includes an internal, isolated DC/DC power supply for the front end, so no separate supply is required.

Although primarily intended to be used in the feedback loop of switched power supplies, the AD215 can also be used for voltage monitors, motor current sensing, and large battery systems, all of which are well within its 400 kHz bandwidth (Figure 3).

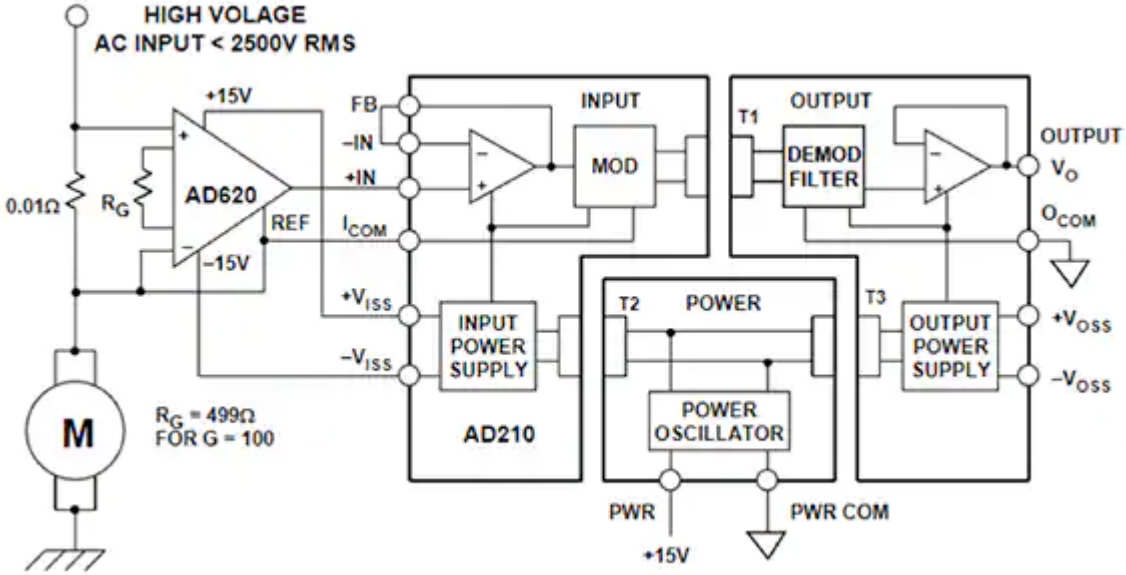


Figure 3: Though primarily intended for use in the feedback loop of switched power supplies, the AD215 also be used for voltage monitors, motor current sensing, and large battery systems. The AD210 shown here is a functionally identical version of the AD215 but with relaxed specifications; the AD620 is a precision instrumentation amplifier. (Image source: Analog Devices)

In such applications, analog isolation is often needed when measuring the voltage across a motor's sense resistor to determine the current through the motor. This is necessary because the sense resistor is not ground referenced but is instead "floating", and may be at a very high potential with respect to ground.

These earlier magnetic-based isolation devices used discrete transformers and so were relatively large and expensive. Newer designs use proprietary versions of flat, co-planar transformers that are compatible with IC packaging. For example, the ADuM3190 isolated error amplifier from Analog Devices is housed in a 16-lead QSOP package yet provides a 2.5 kV isolation rating. Its planar transformers are positioned parallel to each other for maximum energy transfer (Figure 4).

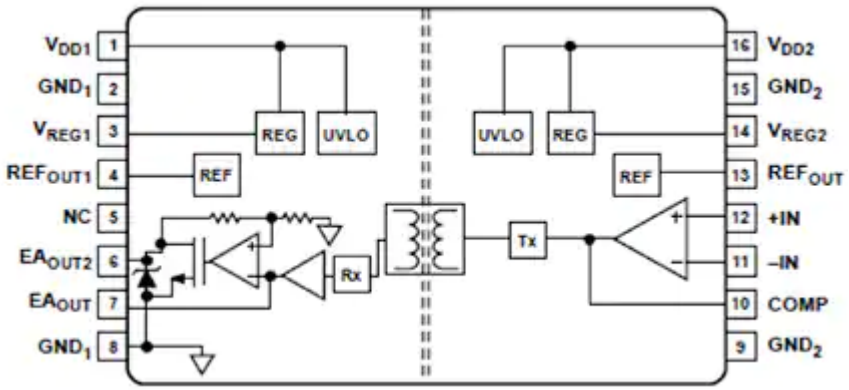


Figure 4: The ADuM3190 isolated error amplifier is packaged to look and handle like an IC, yet contains silicon die and a pair of planar transformers that are positioned parallel to each other for maximum energy transfer. (Image source: Analog Devices)

Although it looks like a standard op amp, it actually takes the input signal and uses it to generate a PWM signal that is passed through the planar transformer. This PWM signal is demodulated and filtered at the secondary side to generate the analog output signal. The data sheet includes standard op amp Bode plots for phase and gain margin (Figure 5). Designers who use this device (or similar ones) can expect to go through standard amplifier loop stability and related modeling and simulation. The Bode plots will help.

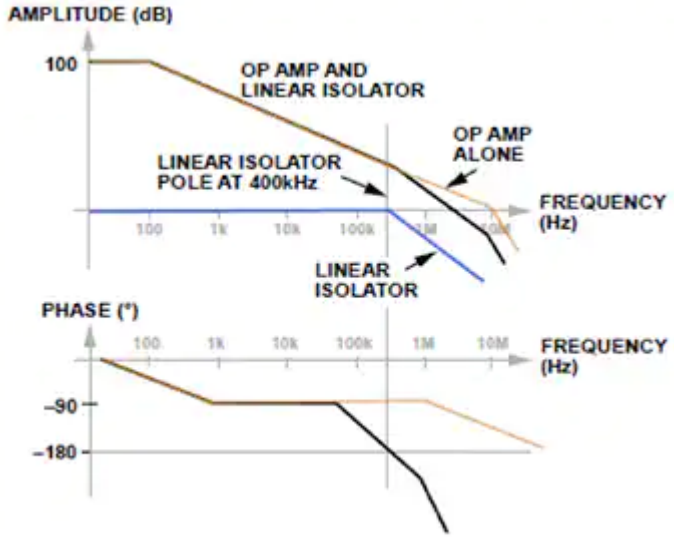


Figure 5: Although it has a complicated, isolated internal architecture, the ADuM3190 from Analog Devices appears to the designer as a conventional op amp. (Image source: Analog Devices)

The ADuM3190 is rated for −40°C to +125°C ambient operating temperature, which is a reality in some of the target applications. Note that since the isolating element is a just wound wire, there is no “wear-out” mechanism in the conventional sense, unless the device is operated beyond its specifications.

However, all insulation materials eventually break down over a sufficiently long period due to voltage stress, with the rate of degradation as a function of the magnitude and type of voltage waveform applied across the voltage barrier. For the ADuM3190, the vendor guarantees a 50 year life even at a maximum rated bipolar AC waveform, which is more stressful than unipolar AC or DC of the same magnitude.

Optical isolation: a newer option

An alternative to magnetic isolation is optical isolation, which is conceptually simple: the input side drives an LED, the output of the LED impinges on a co-packaged phototransistor, and the output is the phototransistor current (Figure 6). The short optical path between LED and phototransistor within the package provides the desired galvanic isolation.

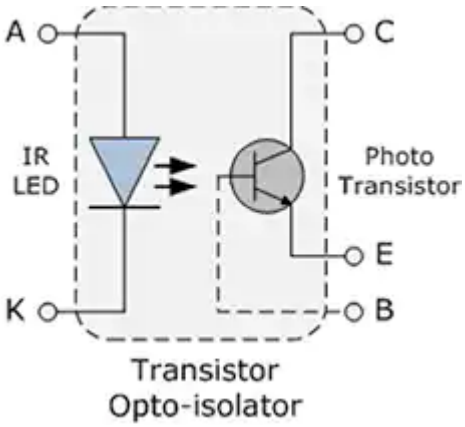


Figure 6: An optoisolator requires two active elements: an LED to source IR, and a phototransistor to convert received photons into electrical current. The galvanic isolation is provided by the optical path within the package. (Image source: Sunpower UK)

As with transformer-based isolation, the input signal is used to modulate the LED current in a digital mode, using PWM or other approaches. The Broadcom (Avago) ACPL-C87B/C87A/C870 family of optical isolation amplifiers is a good example of devices that can be used for voltage sensing across a current sense resistor (Figure 7).

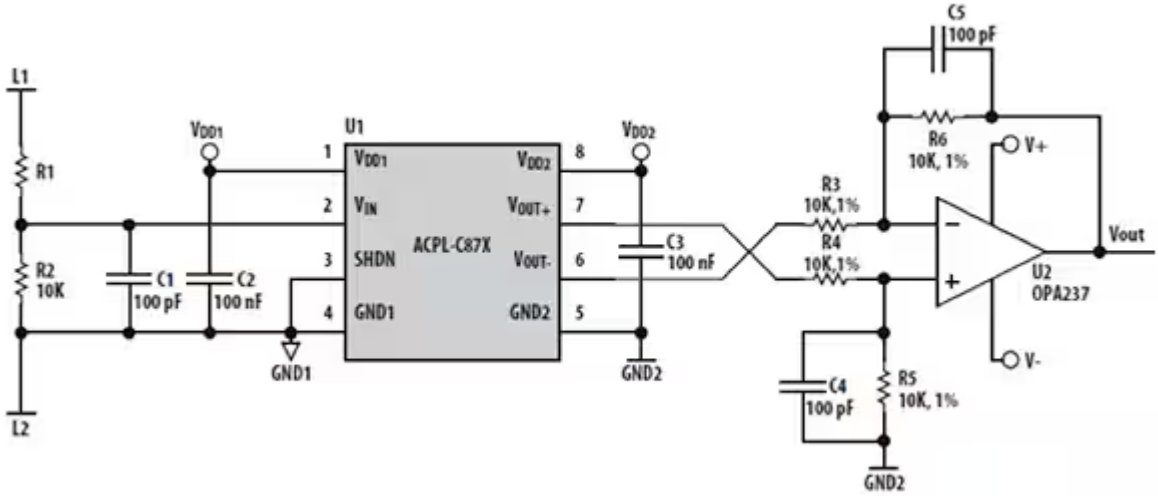


Figure 7: Optoisolators in the Broadcom ACPL-C87B/C87A/C870 family target lower level voltages, and use sigma-delta modulation with a chopper stabilized amplifier for precision, accuracy, and consistency. (Image source: Broadcom)

Isolators in this family have a 2 volt input range and high 1 GΩ input impedance. These specs make them a good fit for isolated voltage sensing requirements in power converter applications, including motor drives and renewable energy systems. The devices combine optical coupling technology along with sigma-delta (Σ-Δ) modulation, chopper stabilized amplifiers, and differential outputs to provide high isolation mode noise rejection, low offset, high gain accuracy and stability. These are all housed in a stretched SO-8 (SSO-8) package.

The devices are well suited to power converter applications due to their 100 kHz bandwidth (Figure 8) and high common-mode transient immunity (15 kV/μs). Such transients are common with motor drives.

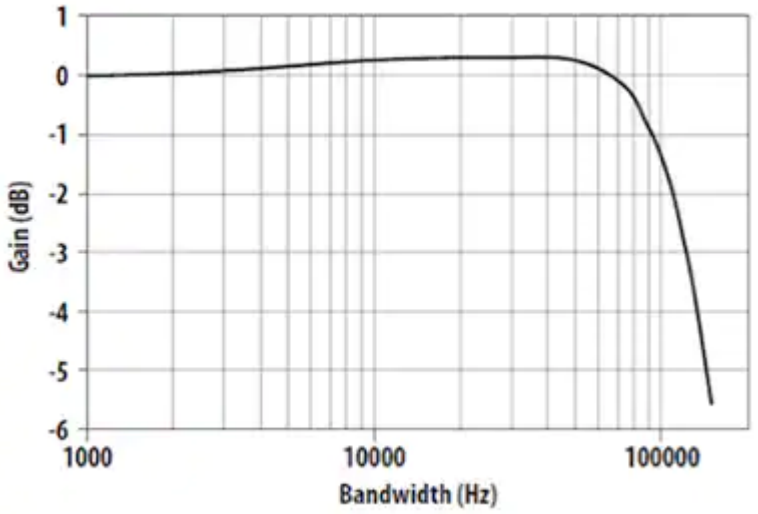


Figure 8: Using its internal sigma-delta analog-to-digital conversion technique, the Broadcom ACPL-C87B/C87A/C870 family of optical isolation amplifiers easily achieves 100 kHz bandwidth with flat response out to 100 kHz. (Image source: Broadcom)

Capacitive isolation: The newest option

Another isolation technique uses capacitance and a minute separation between a capacitor's "plates" for isolation. The technique has become feasible and cost-effective in recent years due to advances in IC and packaging technologies. A good implementation example is the Texas Instruments ISO124. This is a precision isolation amplifier with its input and output sections galvanically isolated via matched 1 picofarad (pF) capacitors built into the SOIC-16 (or SOIC-18) surface mount plastic package.

Like other analog isolation amplifiers, its high level functional diagram is simple (Figure 9).

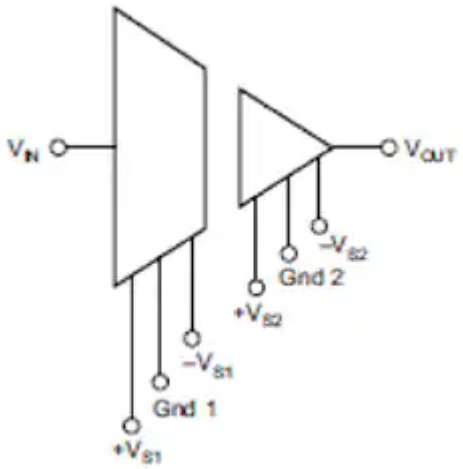


Figure 9: One commonly used symbol for an analog isolation amplifier is this "split" op amp, used on the ISO124 data sheet; this clearly shows that the input and output sections have their own, separate "grounds" (though "common" would be a more correct designation). (Image source: Texas Instruments)

At the same time, the detailed block diagram reveals the complexity of what's inside and invisible to the user (Figure 10).

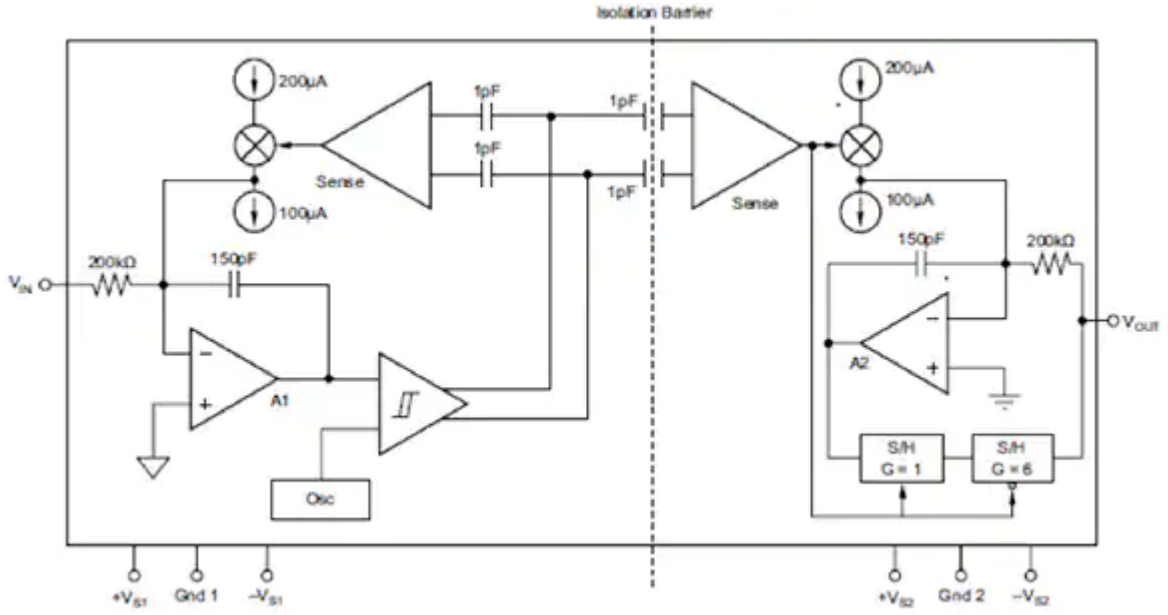


Figure 10: As with the magnetic and optical isolation devices, there is a significant amount of analog and digital circuitry within the ISO124 to make its unique capacitive-based isolation operate. (Image source: Texas Instruments)

The ISO124 input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. It features 0.010% maximum nonlinearity, 50 kHz signal bandwidth, and 200 microvolt (µV)/°C V_{OS} drift, and requires a single power supply between ±4.5 V and ±18 V.

As with non-isolated op amps, the data sheet has both tabular data as well as graphical information on sine wave and step response performance under a variety of conditions (Figure 11). Potential users of these isolation devices need to study the data and diagrams to ensure the device performance is commensurate with the application needs.

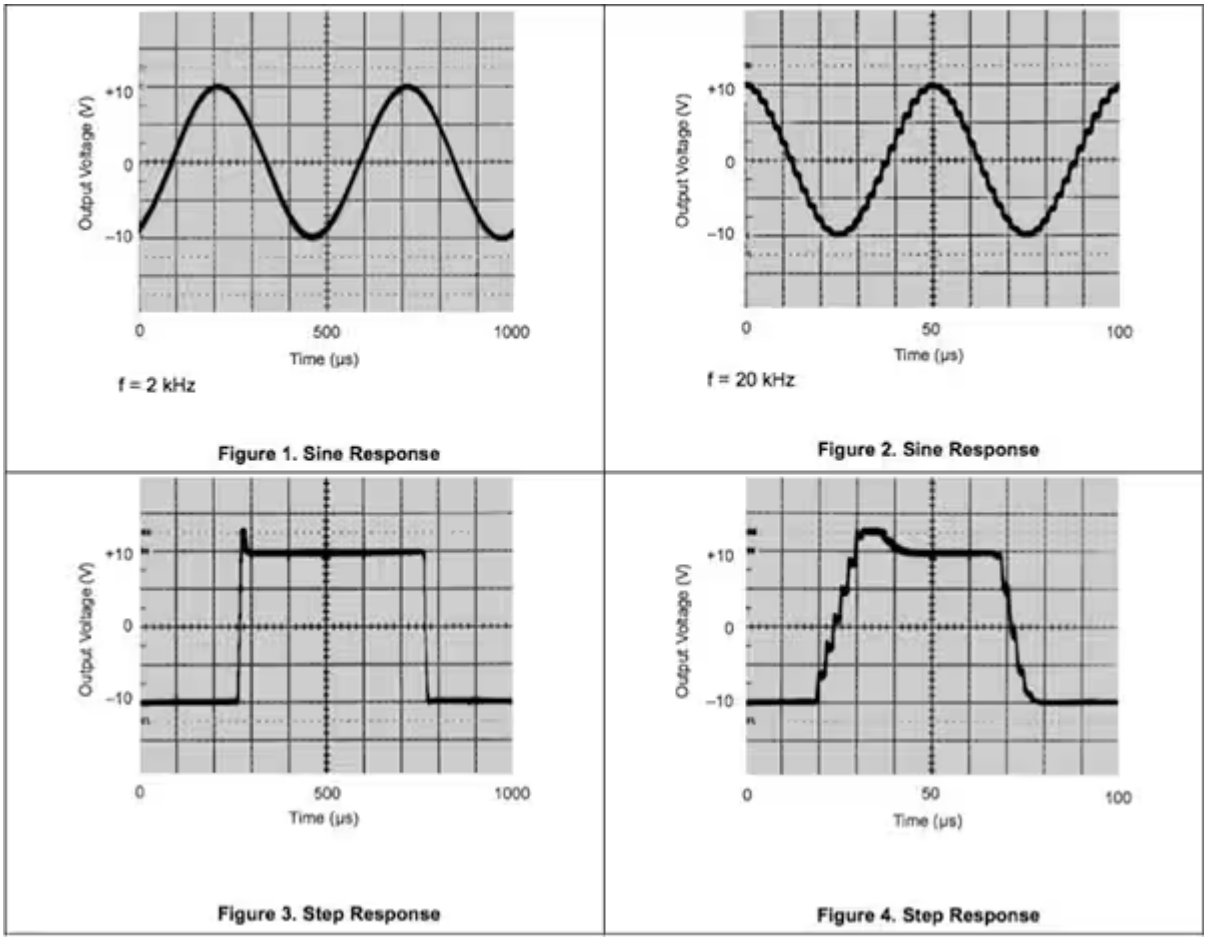


Figure 11: Due to the op amp-like nature of the ISO124 analog-based devices, designers need to pay close attention to the many graphs and tables, including the standard sine and step response graphs. (Image source: Texas Instruments)

The ISO124 is a good fit for low-speed applications, such as isolating the signal from resistance temperature detector (RTD) and thermocouple temperature sensors on a 4-20 mA current loop at the receiver end, and transforming it into a voltage (Figure 12).

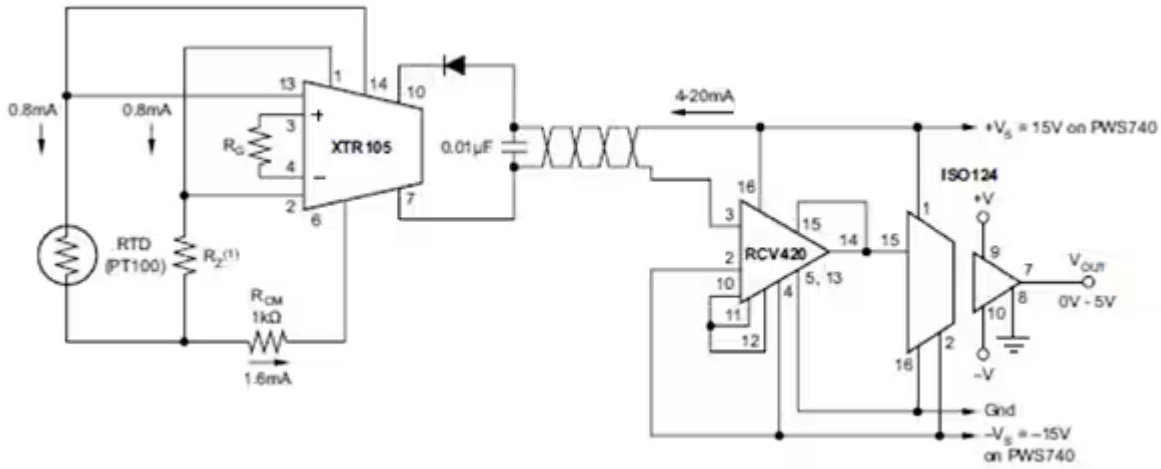


Figure 12: The ISO124 is used to isolate an RTD connected via a standard 4-20 mA current loop, and also convert that current signal into a 0-5 V signal for control system compatibility. (Image source: Texas Instruments)

Temperature measurement applications often require that the sensor be isolated from the rest of the system circuitry due to the potentially high voltage point to which they are directly affixed, such as a motor housing. This

voltage is then used by a system analog-to-digital converter (ADC) for readout or closed-loop control, both of which are common industrial situations.

Making the decision

All three analog isolation technologies – magnetic, optical, and capacitive – can provide excellent results under the right conditions. The designer's dilemma then becomes how to decide on the "best" one in a given situation.

Among the factors to consider are bandwidth, expected lifetime (time to failure or wear out), size, and power requirements. Each isolation technology balances these attributes and may offer specific products with different tradeoffs within a family, thus complicating the decision.

Regarding the amount of voltage isolation, all three types are certified to at least 1 kV (some go to 5 kV and even higher) and meet relevant regulatory standards (IEEE, VDE, CIE, UL, CSA). Therefore, maximum isolation voltage is not an issue for most IoT applications. If this should become an issue, specialty isolators are available which are certified for higher voltages.

There are some general statements that can be made about each isolation technology, but for each statement there are exceptions, and vendors of each technology make effective and legitimate arguments as to why their approach is better. In general:

Magnetic isolation has very long life and its passive barrier can withstand surges and spikes that are much greater than the continuous voltage rating. However, due to its inductive coupling via magnetic fields, it can be susceptible to interference from external magnetic fields. Some of the newer designs successfully minimize this issue to such a degree that the units are certified against such interference susceptibility using industry standard tests.

Optical isolation has high immunity to electrical and magnetic noise, but has modest speed due to LED switching speed, higher power dissipation, and concerns about LED wear. The last issue is the most serious one, as LEDs do experience degradation (dimming) in normal use, with typical half-brightness periods of about ten years. However, companies such as Broadcom/Avago have pushed the state-of-the art in LED materials and so are guaranteed to meet specifications for twenty years, which is often sufficient for the situation.

Capacitive isolation has high immunity to magnetic noise, and compared to optical isolation, it can support wider bandwidth because there are no LEDs that need to be switched. In reality, most IoT sensor applications are low bandwidth situations. Capacitive coupling also involves the use of electric fields for data transmission, so it can be susceptible to interference from external electric fields.

Analog versus digital isolation

Thus far, we have looked at analog isolation techniques for IoT sensors (Figure 13).

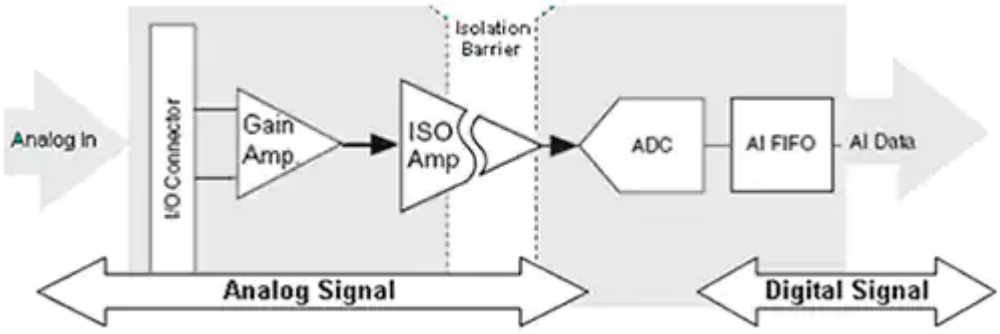


Figure 13: In the analog isolation topology, the sensor signal remains as analog information (regardless of what happens within the isolator itself) until it reaches the non-isolated side, where it can be converted to digital format for further use. (Image source: National Instruments)

However, there is a fundamental architectural alternative: digital isolation, where the analog sensor's output is conditioned and digitized on the isolated side, and the digital output is then passed through a digital isolation barrier (Figure 14).

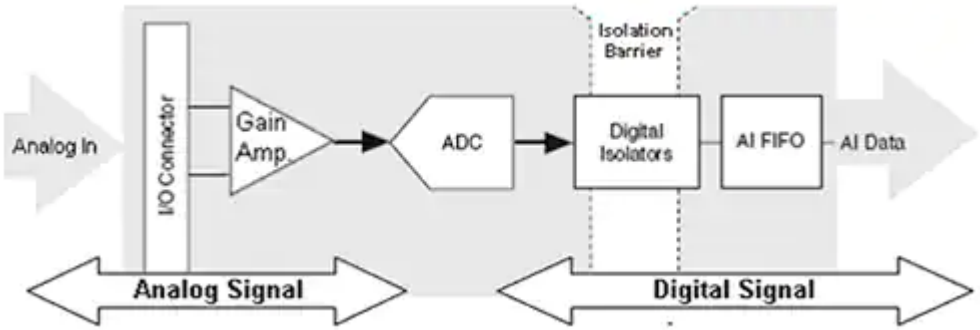


Figure 14: An alternate and often attractive approach is to digitize the signal on the isolated side, then pass the conversion result through a digital isolation barrier. This allows for a very different isolation function implementation, compared to an analog isolation design. (Image source: National Instruments)

As with analog isolation, this barrier can use any of the three technologies, but their internal design is optimized specifically for digital signals and can usually support data at tens of Mbps. Further, for digital isolation there is a new, fourth category option that uses a modulated RF carrier instead of modulated (LED) light. The Si863x series from Silicon Labs is a good example of such a device (Figure 15).

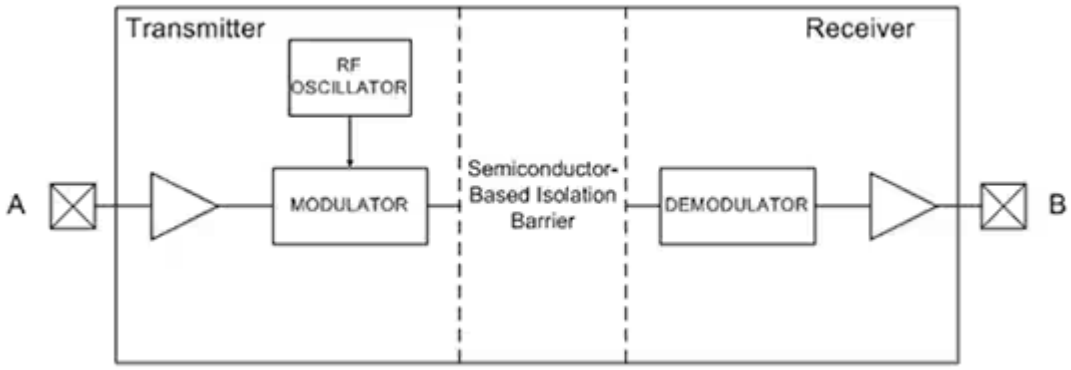


Figure 15: The Si863x series of digital isolators from Silicon Labs use a modulated RF carrier instead of light to carry the signal while providing isolation. (Image source: Silicon Labs)

As the cost of ADCs has gone down, and vendors have standardized around interfaces such as I^2C and LVDS, the use of digital isolation becomes more attractive. The downside is that more circuitry is required on the isolated side. This means that more isolated power is needed, adding to cost and footprint.

Once again, though, advances in lower power high-performance ADCs are making this less of a problem. Standard interface digital isolators, such as the 1 MHz ADUM1250 for I^2C and 600 Mbit/sec ADN4651 for LVDS, both from Analog Devices, simplify this design alternative. There are also ADCs with integral isolation in their multi-chip IC package, such as the 16-bit Analog Devices AD7401A which make the entire conversion and isolation process transparent to the user.

Finally, there's the issue of multichannel isolation. While many IoT applications have just one or two sensors that need isolation, others may have four, eight, or more. In those cases, the individual analog isolators in aggregate

may be too large, costly, and power hungry,

An alternative approach is to use a multichannel ADC or a single channel device with a front-end multiplexer, all on the isolated side, with higher speed digital isolation to transfer the results. This may be more power, space, and cost-effective than simple per channel isolation.

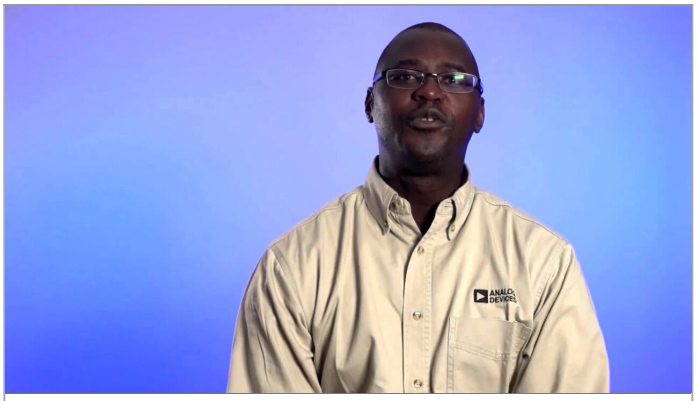
Conclusion

Analog sensor isolation is a critical issue in many IoT applications for signal integrity, system safety, and user protection. Three viable competing technologies can implement isolation, each offering many similarities in performance but with some subtle differences. Digital isolation, with sensor digitization on the isolated side, is also an option to consider in many applications.

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Study of Current Optocoupler Techniques and Applications for Isolation of Sensing and Control Signals in DC-DC Converters

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APPENDIX P

STUDY OF CURRENT OPTOCOUPLER TECHNIQUES AND APPLICATIONS FOR ISOLATION OF SENSING AND CONTROL SIGNALS IN DC-DC CONVERTERS

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

STUDY OF CURRENT OPTOCOUPLER TECHNIQUES AND APPLICATIONS FOR ISOLATION OF SENSING AND CONTROL SIGNALS IN DC-DC CONVERTERS

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

By

Jacob Thomas Williams
University of Arkansas
Bachelor of Science in Electrical Engineering, 2010

December 2012
University of Arkansas

ABSTRACT

There is a need for power switches that can operate at high voltage, high temperature, and high switching frequencies with low losses. Power switches fabricated from wide bandgap materials such as silicon carbide (SiC) or gallium nitride (GaN) can outperform conventional silicon switches due to material property advantages. Another common problem in grid-connected applications is the need for high voltage-isolation of gate drivers and control circuitry while operating efficiently at the high switching frequencies, high power density, and high temperatures made possible by wide bandgap devices. Transformers cannot operate at the temperatures of these wide bandgap devices and a new solution needs to be determined to operate at higher temperatures with smaller footprints. The purpose of this research is to determine the baseline performance of the current technologies used to isolate gate driver and control signals from high voltage power electronics. Research was conducted to determine the characteristics of current optical isolation technologies and implementation techniques in the specific areas of propagation delay, linearity, power consumption, and voltage isolation to determine the baseline performance that future devices could improve upon. The techniques employed to operate the current optocoupler technology were looked at individually and implemented in a Buck converter to determine the performance characteristics with respect to the figures of merit above. The results of the research were that although optocouplers can be used in many different functions the current technology benchmark lacks the robustness of speed, noise immunity, and easy implementation to compete with current workhorse technologies like transformers. The linearity of transmitted analog signals, transmission speed of digital control signals, and the maximum allowable voltage between power stage and control circuitry will need to be improved by future optocoupler technologies like GaN to compete with current isolation techniques.

This thesis is approved for recommendation
to the Graduate Council.

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Dr. H. Alan Mantooth

Thesis Committee:

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DEDICATION

To Jesus, my friend and Hero

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1 INTRODUCTION

Power electronics are increasing in power level and switching frequencies while decreasing in size because of increased power density, operating temperature, and breakdown voltage due to the innovation of power semiconductor devices like SiC MOSFET's and IGBT's [1]. Power electronics, no matter how simple or complex, need control circuitry of some form to control how the power system reacts to line and load changes. The controller uses system variables from the power electronics system, like input current or output voltage, to analyze the condition of the power electronic circuitry so that control signals can be produced to regulate and stabilize the behavior of the power circuitry to keep the system stable in a dynamic environment. These control circuits work at relatively low voltages while the power electronic circuits can operate at increasingly high voltages due to the aforementioned innovations in semiconductor technology. If direct connections are made between the power circuitry and control circuitry via the network that senses the control variable (i.e., a voltage divider sensing an output voltage) the large noise associated with power circuitry will influence the operation and distort the control circuitry – possibly destroying it. The control circuitry needs to be electrically isolated from the power circuitry. This is done by isolating the two circuits' grounds from each other and removing any electrical connections between the two. Figure 1.1 shows this concept.

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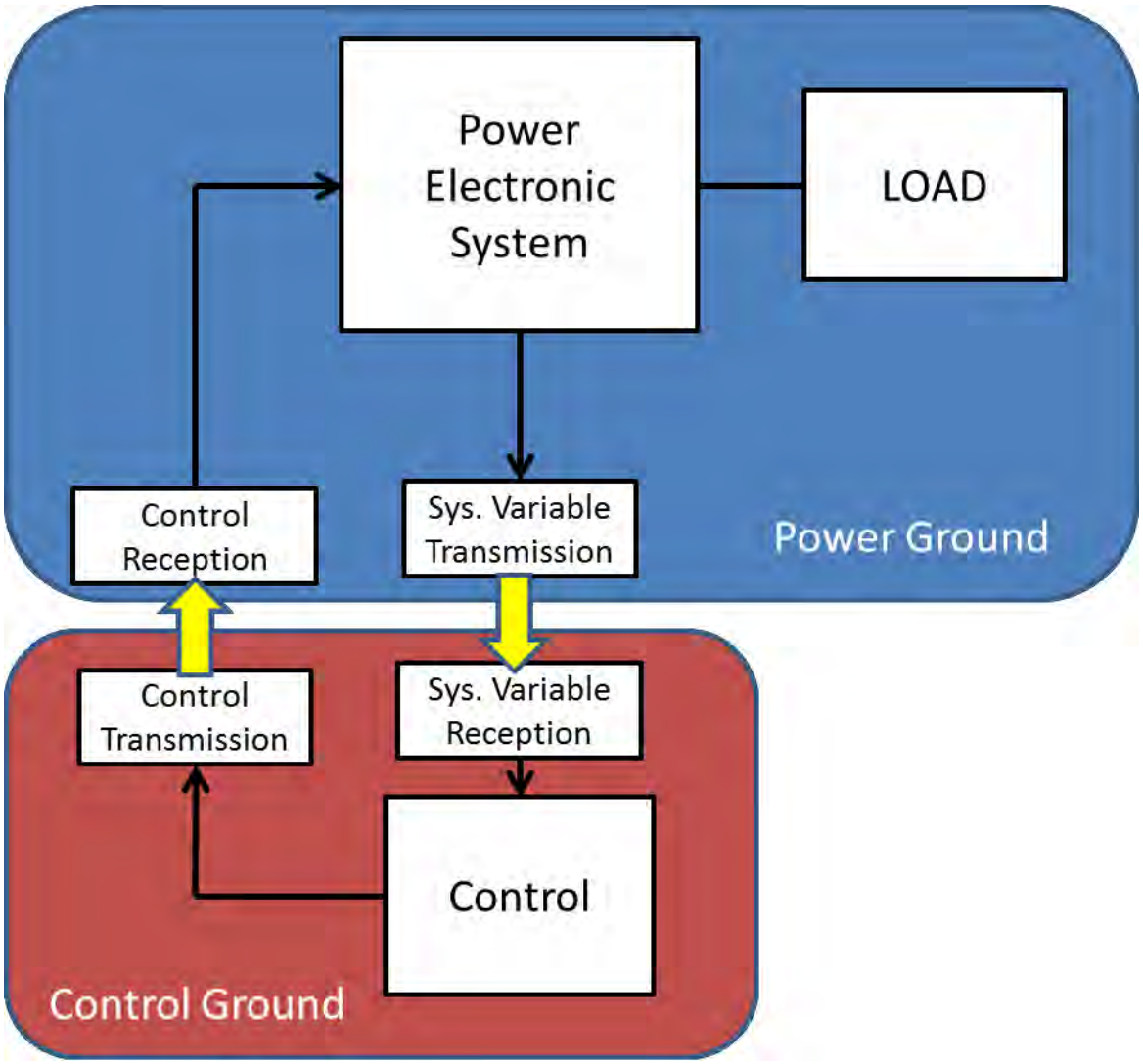


Figure 1.1 Concept of isolated grounds for control and power circuit

The first role for isolation is isolating power supplies from each other. The two isolated grounds (represented as the red control ground and blue power ground) would require two separate power supplies to power their respective circuitry. The power ground is established by the power input to the power electronics system and no connection is made to the power input to the control circuitry so that the grounds are electrically separate from each other. This means that all the signals in the power circuit will be referenced to a different potential than the signals in the control circuit. This potential difference between the two separate grounds can be large. How can the sensed system variables and control

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signals be sent between separately referenced circuits without electrical connections (shown as the yellow arrows in Figure 1.1)? This question is answered by special devices that can transmit through the isolation barriers without electrically coupling the two circuits. These devices operate by converting the electrical signals into other forms (i.e. magnetic or optical) to be transmitted through the isolation barrier and then converted back to an electrical signal referenced to the correct ground potential. Three common techniques have been developed to implement both types of isolation: transformers, optical devices, and capacitors. Research is being done in these three areas to follow the trend in power electronic systems to have greater switching frequencies and higher power with smaller footprints, which in isolation technology means faster transmitting speeds and greater voltage isolation in a smaller package.

1.1 Purpose of the Thesis

The purpose of this thesis is conveying the results of research into only one of the different isolation devices, the optocoupler. The principal objective is to determine the state of commercially available optocoupler technology. A benchmark will be created to determine the baseline performance of these optical isolation devices. This benchmark can be used to compare new optical isolation technology with future technologies like gallium nitride (GaN) optical devices. GaN is expected to be the improvement in optical isolation that will allow optical isolation to be implemented within the higher power and higher frequencies of current and future power electronics. This means isolation is needed between a larger voltage difference, but with the very fast transmitting speeds needed for faster switching frequencies. A parallel purpose is to create an all-optical control loop for a specific power electronic design. The design of the power electronic system is included to show the current optical limitations on a power electronics system. The application context power electronic system is chosen to be a current-mode optically-controlled Buck converter with an isolated resonant energy recovery

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MOSFET gate driver as presented in [2]. The reasons for choosing this specific design are to display the many uses for optical isolation and these reasons are elaborated on in the following chapters. To understand the need for optocoupler technology and the improvements possible with GaN the other two isolation techniques, capacitive and transformer isolation will be briefly discussed.

1.2 Broader Context of Thesis

1.2.1 Capacitive Isolation

Isolation with capacitors is used to isolate a voltage potential from earth ground and reference it to a floating node within the circuit, and to transmit information through an isolation barrier between two different references. In the former application the energy transfer is done through the charging of the capacitor which is a limiting factor in that the capacitor will need a time when it is not used and recharged. The first example of capacitive isolation is a bootstrapping circuit which allows a power source to keep its voltage potential (in relationship to its actual reference node) even when it is referenced to a floating node [3]. Switches are always present in capacitive isolation because there must be a time when the bootstrap capacitor is recharged through a switch connected to actual ground potential. This is isolation between the actual ground of a power supply and a floating node within the circuit with a few extra, small components. Figure 1.2 shows a bootstrap circuit [3]. The disadvantage is that this circuitry only allows a floating reference point and does not isolate voltages. In Figure 1.2, when Q_1 is on, the bootstrap diode D_B and the high-side driver are subjected to V_{DD} which can be very large in a power electronics circuit. With optical isolation the optocoupler is the only component that must withstand this voltage so the other circuitry can be rated much lower.

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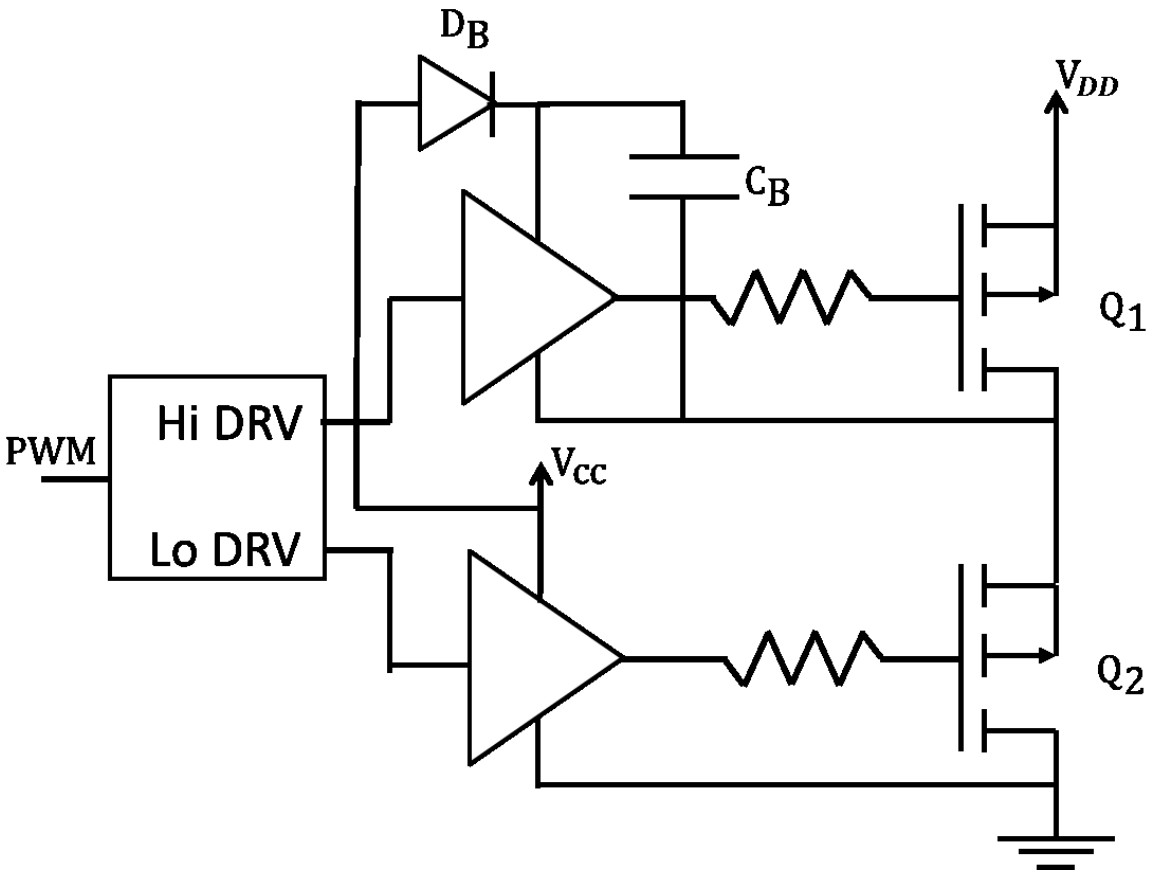


Figure 1.2 Bootstrap circuit [3]

Another circuit employing capacitive isolation is a charge pump [4]. A fully isolated voltage potential can be generated from a grounded source voltage using a square wave, diodes, and capacitors as shown in Figure 1.3 [4]. The components (IC's and external diodes) are subjected to the full system voltage so they have to withstand large voltages as in the bootstrap topology. Also, capacitors can be used to transmit through isolation barriers as shown in [5]. Optocouplers cannot reach the transmission speeds of capacitive isolation with the current technology, but it can transmit signals across its entire bandwidth without the use of pulse width modulation and it is a much smaller footprint [5].

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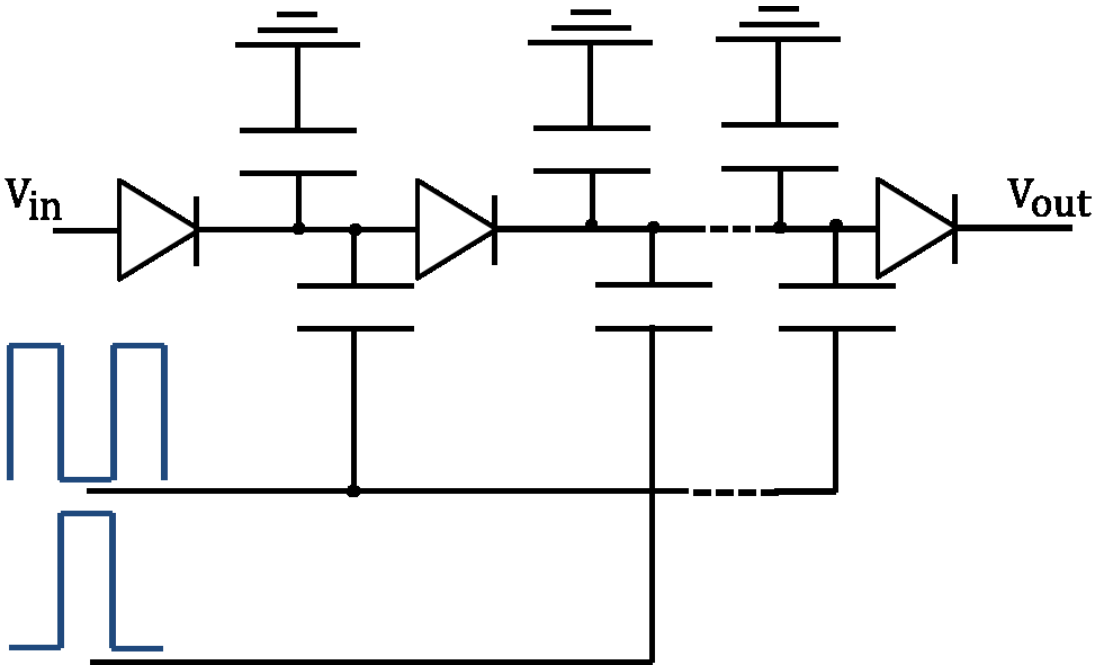


Figure 1.3 Dickson charge pump [4]

1.2.2 Transformer Isolation

Transformers are the current workhorse for isolation. The secondary windings are electrically isolated from the primary windings. The magnetic field produced by the primary winding induces a current on the secondary winding determined by the ratio of the number of turns. In a transformer the power is transferred by the use of this magnetic field so there is no direct electrical connection. Transformers are also very efficient, but their footprint is larger than the capacitive isolation schemes. The size of the transformer is dependent on the number of windings and the frequency at which it is operating. The size decreases as the frequency increases, but it remains a larger footprint than the circuitry necessary for capacitive isolation. Transformers can be used for both isolation purposes, creating isolated power supplies as shown in Figure 1.4a and transmitting signals in Figure 1.4b [1].

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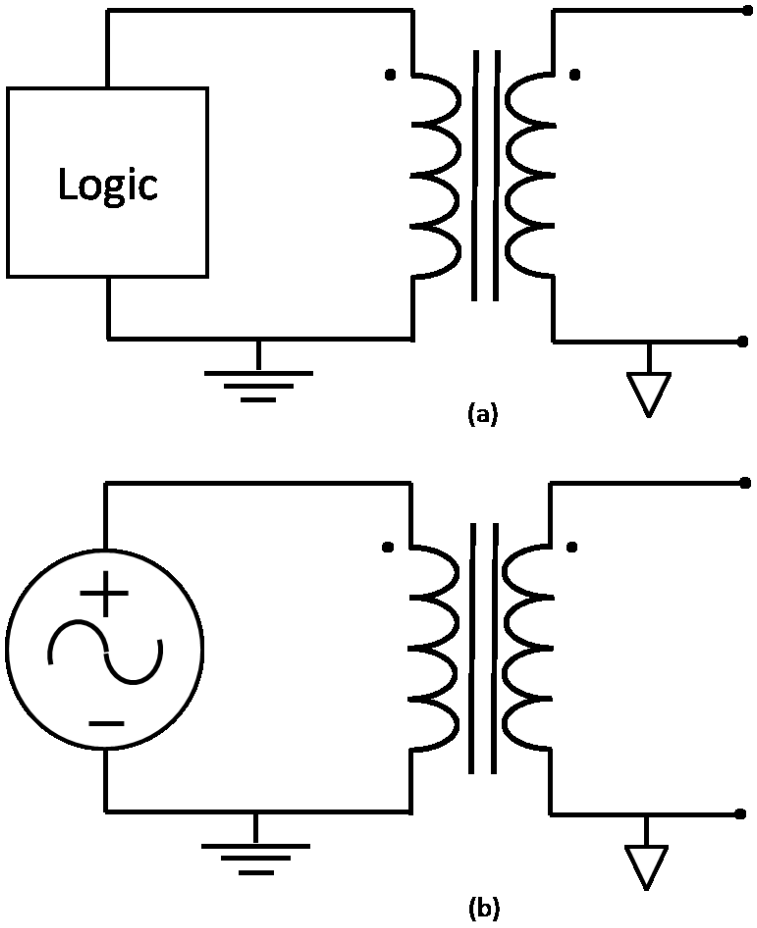


Figure 1.4 Transformer isolation for logic signals (a) and power (b)

The scope of this thesis is the transmission of signals through isolation and in this application the duty cycle is limited to less than 50%, so the transformer will not saturate. The size of the transformer limits it to large circuits that do not need to save space. With optical isolation the optocoupler is very small and can be implemented on chip [1]. It can be used to transmit digital information with large voltage isolation and an analog current signal without the limiting duty cycle.

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1.3 Optocoupler Introduction

1.3.1 Optocoupler's Basic Structure and Isolation Applications

Now that the other two isolation technologies are understood the use of optocouplers can be appreciated. Optocouplers, most simply put, are a combination of a diode, that emits light when current flows through it, and a diode that absorbs the light and produces a proportional current (like a solar cell) [6]. Figure 1.5 shows a simple schematic of an optocoupler.

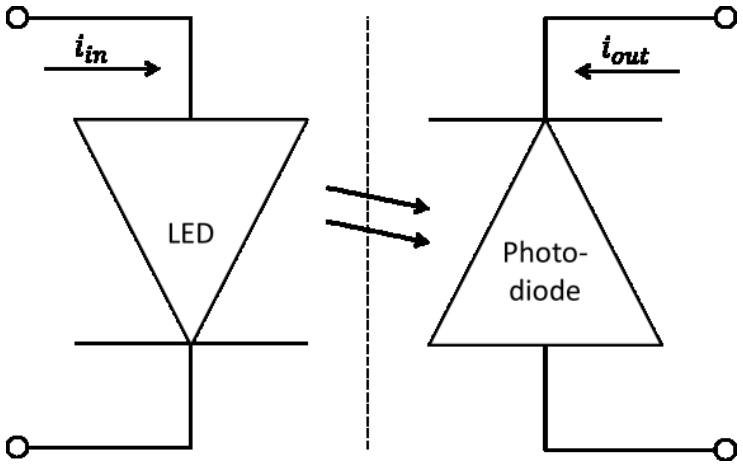


Figure 1.5 Basic structure of optocoupler

Just like a solar cell, the optocoupler can be used to generate isolated power from a ground referenced power supply by sending the power via light. This is an extremely important application of the optocoupler because of its very small size and large operating range (compared to transformer saturation).[1] The optocoupler is most useful transmitting sensed information measured from the power circuitry that is needed by the control circuitry. As seen in Figure 1.5, the output signal is isolated from

[1] Research into improving this power isolation technique is being done in collaboration with the University of South Carolina and will not be covered in this thesis.

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the input, where the transmission medium is light so there is no electrical connection between the input and output.

There are many different types of optocouplers available commercially (operating with digital signals or analog signals as inputs), and this thesis defines an application context to test these optocouplers in a high speed, high power, and high temperature environment to determine a benchmark for current technologies to be compared to future technologies like GaN. This is important to find the areas that GaN can improve upon with its inherent higher temperature, lower power consumption, shorter propagation delays, and higher voltage isolation capabilities. It is important in order to determine the current limitations of commercially available technologies in the four areas that GaN optocouplers are supposed to improve upon because when GaN devices can be fully tested there will be a benchmark to quantitatively compare GaN's improvements or trade-offs to the developed technologies in the market.

1.3.2 Determining the Benchmark

There are two main components to determining the benchmark set by commercially available optocouplers. Because optocouplers do not operate independently, the first is to separately test the different kinds of optocouplers with an application specific circuit that will employ different types of optocouplers and determine the limiting characteristics of each kind of optocoupler application. The two types of applications are analog and digital transmission. The analog optocouplers transmit information accurately with the use of op amp circuitry around the optocoupler. In this optocoupler application the accuracy and propagation delay from input to output are the important figures of merit. They will be measured in the presence of temperature and input changes to determine the baseline performance of these types of optocouplers. The importance is maintaining an output that tracks the input linearly over a large range of temperature and inputs. This range will be quantified and recorded as the benchmark

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that future analog optocouplers will improve upon. The digital optocouplers only transmit ones and zeros by employing an output stage that swings from on to off very quickly. The figures of merit for these circuits are their propagation delay, minimum pulse width, and power consumption. Just like the analog transmission optocouplers these parameters will be analyzed in the presence of temperature and biasing changes to determine the digital benchmark.

The second component is implementing an all-optical closed loop power converter with the commercially available optocouplers. The power converter application context will be used to display the same limits (propagation delay, temperature, accuracy, power consumption, etc.) in a practical power electronics system with very specific requirements for the optocouplers operation. The design process will be parallel to the first component. This will create a viewpoint into the functionality of the optocouplers in the presence of noise and timing constraints compared to the ideal bench top testing of the optocouplers with ideal inputs and biasing. The future work will be to implement the GaN optocouplers into the same application context to determine the benefits.

1.4 Thesis Organization

The Background chapter presents a foundational understanding of the optocoupler technologies available and their different uses. It also defines the application context for the first component of experimentation that will be implemented to find the speed and temperature limits of the available optocouplers independent from the full system implementation. In the next chapter, Optocoupler Characterization Experiments, experiments are conducted on the individual topologies to determine the benchmark for each of the topologies and to understand the design decisions that have to be made to implement the optocouplers into the Buck converter. The second component of experimentation is determined to be a current-mode optically-controlled Buck converter. This is chosen because it needs isolated current and voltage sensing and gate drive control. These reasons are elaborated upon in the

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Background chapter. The Implementation of Optocouplers in a Closed-Loop Buck Converter Chapter shows the design procedure of the current-mode optically-controlled Buck. The Buck converter implements the best of the analog and digital design to determine their performance in an application context with real power, noise, and stability requirements. Simulation results are recorded for the design in this chapter. The final PCB implementation and experimental results are recorded as well. The Conclusions chapter records the final benchmark for each of the individual optocoupler topologies. The final chapter will also describe conclusions on the overall advantages and disadvantages of optocouplers in the Buck converter. Future work will also be discussed in the Conclusions chapter.

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2 BACKGROUND

This chapter describes the information needed to understand the basic concepts of the technology that is analyzed in this thesis. The foundations that are laid in this chapter are broken down into three sections. The first section reveals the needed information to understand what an optocoupler is, how it works, and the different devices available. The next section defines the Buck converter, the application context for testing the optocouplers functions in a real world circuit. It discusses why the Buck converter was chosen, its basic operation principles, where the optocoupler is an integral part to its operation and the control methods that need to be implemented. Finally, the gate driver options for the isolated, wide bandgap switch are introduced and its need and operation are outlined. These three foundations are needed so that the experiments that determine the benchmark performance of the current optocouplers can be understood. Once the optocoupler is understood the optimal topology can be chosen to implement in optical Buck converter and the final conclusions about the optocoupler's use in a DC-DC converter system can be drawn.

2.1 Optocouplers

The conventional technique to transmit electrical information without direct electrical connections is transformers, as discussed in the introduction. Because of the inherent advantages of an optocoupler, for instance its smaller size and possible monolithic integration onto a power electronics chip, it is desirable to improve the current technology to eliminate their inherent disadvantages like long propagation delays so they can compete with transformers in the isolation market.

Optocouplers are the key component of research in this thesis. All the circuitry around it, from the application context to the auxiliary circuits that optimize the optocouplers is there to test and enhance its operation and performance. To fully understand the design process of testing, enhancing, and finally

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characterizing a benchmark for the optocouplers, the basic operation of the fundamental optocoupler structure and operation must be understood.

2.1.1 Optocoupler Basics

Optocouplers are used, similarly to transformers, to transmit electrical information without electrically coupling the transmitter and receiver. Optocouplers use light generated by current flowing through a light emitting diode (LED) to transmit signals and that light needs to be converted back to voltage signals at the output to be useful. A photodiode (or phototransistor) is the second half of an optocoupler, which creates an electrical potential when light impinges on its p-n junction. Figure 2.1 shows a simple schematic representation of an optocoupler, it can be seen that no electrical connection is made between the input LED and output photodiode. The photodiode has a single PN junction that generates electrical power from the impinged light [6].

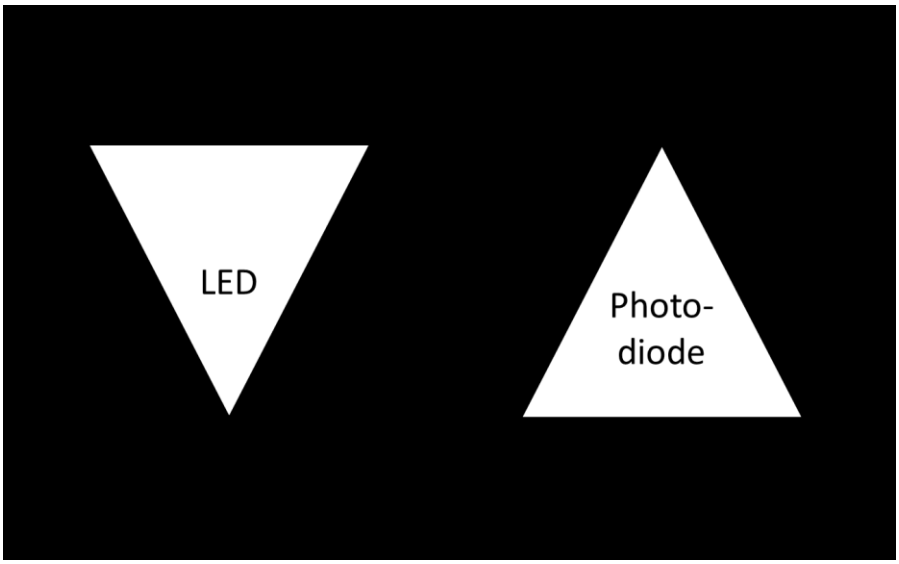


Figure 2.1 Basic structure of optocoupler

Since the photodiode is basically a diode that has enhanced light sensitivity the I-V relationship is inspected to determine its operating characteristics. For the operation of transmitting signals through

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an isolation barrier the photodiode will act as a receiver. To operate as a receiver the PN junction needs to be reverse-biased. Ideally, if the junction is uniformly illuminated with photons with an energy greater than the energy of the bandgap $\left(hv>E_g\right)$ then electron hole pairs (EHPs) are generated at a rate of g_{op} (EHP/cm^3-s) and swept out of the depletion region participating in current flow [6]. This current is defined by:

$$I_{op}=qAg_{op}\left(L_p+L_n+W\right) \quad \textbf{(2-1)}$$

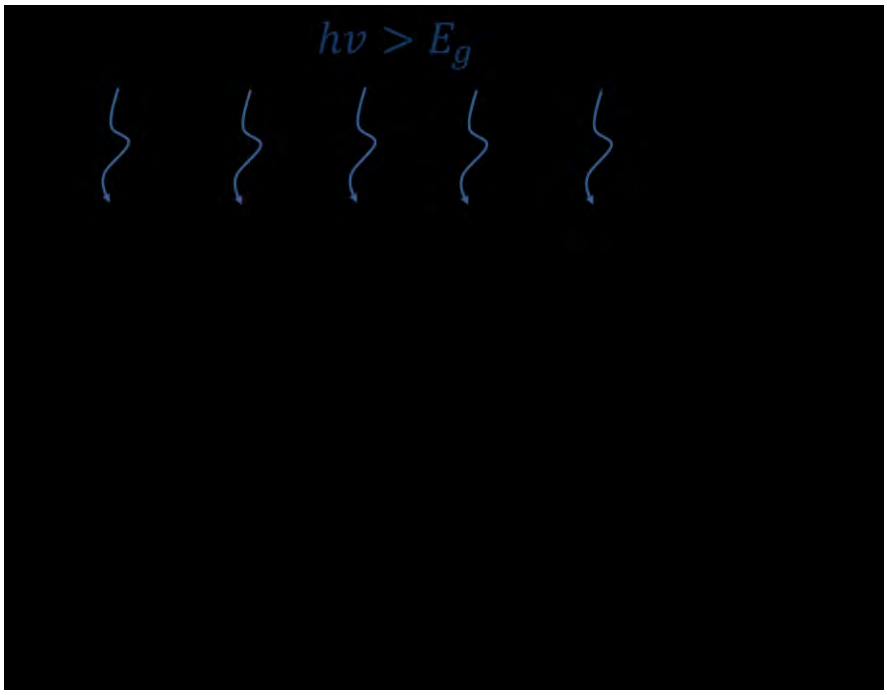


Figure 2.2 Structure of photodiode [6]

This equation states that the current is determined by the rate at which the EHPs are created in the depletion region $\left(Ag_{op}W\right)$, holes created per second within a diffusion length on the *n*-side $\left(Ag_{op}L_n\right)$, and electrons created per second within a diffusion length on the *p*-side $\left(Ag_{op}L_p\right)$. This current is directed from the *n*-region in Figure 2.2 to the *p*-region, so it subtracts from the diodes fundamental current to become [6]:

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$$I=I_{th}\left(e^{\frac{qV}{kT}}-1\right)-I_{op} \quad \textbf{(2-2)}$$

The I-V curve shifts downward (increasing current in the negative direction) by increasing values of g_{op}. Figure 2.3 shows the I-V curve for increasing g_{op}. Through investigation of the I-V curve the photodiode has three quadrants of operation while light is impinged on the junction.

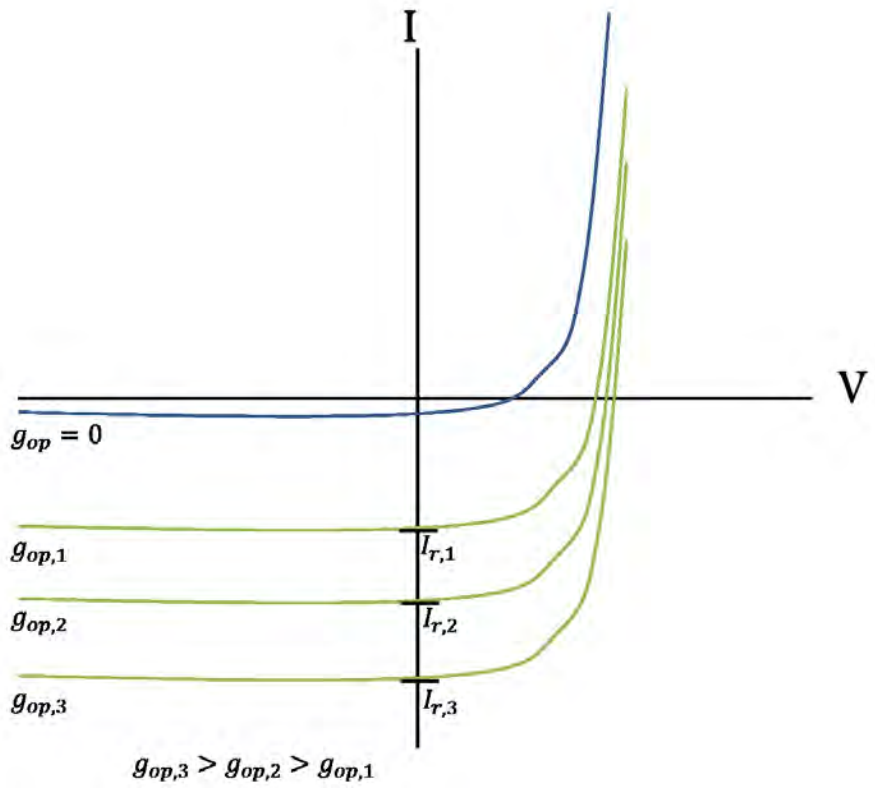


Figure 2.3 I-V curve for photodiode [6]

The three different quadrants of operation each have different desirable characteristics. In the first quadrant the photodiode characteristics follow that of a normal diode with an increased cut-in voltage. This quadrant is avoided in optocoupler applications because current will flow independent of the operation of the LED. In quadrant three the diode is reversed biased and without any added optical energy the reverse current equals the leakage current of the diode. As the optical energy increases

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(increasing g_{op}) the current increases from $I_{r,1}$ to $I_{r,3}$. This current flows from the *n*-region to the *p*-region as shown in Figure 2.4a and consumes energy [6]. This is called the photoconductive mode of operation [7]. In the fourth quadrant the photodiode is forward biased but the current is still negative. In this case, the photodiode delivers energy [6], [7]. This is the photovoltaic mode (same operation of a solar cell), and it is shown in Figure 2.4b.



Figure 2.4 Two quadrants of operation, photoconductive (a) and photovoltaic (b)

Photovoltaic mode is not discussed further in this thesis. This regime is fully investigated by the University of South Carolina in a collaborative project. As stated, the photoconductive mode is used to transmit signals through an isolation barrier because the LED controls the output current by impinging light on a reverse biased junction of a PN Photodiode. All the current created is due to the input LED current. Now that the basic operation is understood the specific parameters of the optocoupler can be discussed. These parameters are important to the benchmark to be set because they are the factors that

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affect the key merits of performance like speed, propagation delay, operation over temperature, and power consumption.

2.1.2 Optocoupler Parameters

The LED emits light depending on the amount of current flowing through it. This light impinges on the photosensitive part of a reverse biased photodiode and, as can be seen above, causing a current to flow through the photodiode. This is the basic building block of an optocoupler. There are important parameters to notice when discussing optocouplers as a whole that will determine the baseline performance in the areas that have been described. The first parameter is the ratio between the forward current of the LED and the photodiode current it induces through the mechanism explained above. This ratio is called the current transfer ratio (CTR). The CTR is around 0.2% [8] naturally. Meaning if there is 10 mA flowing through the LED there will be 20 μA flowing in the photodiode. This is obviously a very small current gain. Another problem with the CTR of an optocoupler is its non-linearity. It will be shown in later sections that as temperature or even forward LED current increases the CTR will change. This nonlinearity needs to be reduced for analog transmission. Topologies will be discussed that can employ a feedback scheme to overcome some of these issues.

Two other important figures of merit that specifically affect the maximum speed of the optocoupler are the propagation delay and the minimum pulse width due to the turn on and off times of the device (the rise and fall times). The propagation delay is the amount of time it takes to see a response in the output photodiode current due to a change in the input LED current. This can be due to the time it takes the light radiating from the LED to reach the threshold at which the photodiode begins to produce current. Another aspect of propagation delay that will directly affect the minimum pulse width is the turn on and off times of the device. These are determined by the process of injecting and dissipating the minority carriers to turn on or off the device. The overall effect of longer turn on and turn

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off times is that the minimum pulse width will increase. In the next section it will be shown that these parameters will be more disadvantages depending on the application context in which the optocoupler is used.

Something to note here is that temperature and biasing are very important in the discussion of optocouplers because temperature will affect the CTR, propagation delay, and minimum pulse width due to how it affects the semiconductor devices. The individual optocoupler experiments defined in the Optocoupler Characterization Experiments chapter will be conducted over temperature to find how it affects these parameters and the overall benchmark. All these characteristics are not well defined in datasheets, they are given at one or two operating points and in this thesis these will be exhaustively tested over the entire range of biasing and temperature. Because future devices will be made from GaN, which is a wide bandgap device, they will be able to operate over a larger temperature range and this data will need to be compared to the current technologies.

Other important features of any optocoupler are withstanding voltage and a secondary parameter, transient common-mode immunity. These characteristics are not specifically tested in the experiments to determine a benchmark because they are well defined in datasheets, but they will be described here. The transient common-mode immunity is the maximum rate of rise or fall time of a common-mode voltage on the input and output of the optocoupler that causes the output to change states [9]. This output state change is due to the common-mode noise coupling through the parasitic capacitances of the LED or the coupling capacitance from the LED to the photodiode [9]. The rate of rise or fall is around 10 $\frac{\text{kV}}{\text{us}}$ with a minimum common-mode voltage potential of 1 kV in the current technologies [9]. The withstanding voltage is simply the voltage potential that the optocoupler can isolate from one side of isolation to the other. Currently, this is on average 5 kV for 60 seconds and 1.4 kV for dc voltages [7], [10], [11], [12].

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2.1.3 Optocoupler Application Topologies

Thus far the optocoupler has been presented as a stand-alone device, but it is always implemented within a specific application with auxiliary circuitry to compensate for its disadvantages. Because of the parameters discussed in the previous section, circuitry needs to be implemented around the optocoupler to negate the disadvantages of CTR, propagation delay, minimum pulse width, and optimize the device, so that the maximum speed can be achieved in a variety of roles in which the optocoupler is placed. Two general categories can be made for all the functions of the optocoupler in an application. The first category is the optocoupler implemented in an analog role and the second is a digital role.

For the analog role, small changes to the input current cause even smaller changes to the output current. The optocoupler, in this sense, can be classified as a current amplifier or current-controlled current source. It is desired that the output tracks the input accurately and linearly over a desired range. In the digital role, the optocoupler is a switch. In this digital role, an input over a certain threshold causes the output state to change to a high or low state. In both roles the basic optocoupler operates in the same way that has been described up to this point, the difference is the circuitry around the optocoupler. So, to use these devices within a specific application (i.e. transmitting analog or digital information) they will not operate independently from the circuitry that implements the optocoupler in the two different roles described. The different topologies for each role are introduced here and the Optocoupler Characterization Experiments chapter determines the experiments that are used to determine which topology is optimal for the application context and the overall benchmark for the current optocouplers. The future GaN devices will also be used within these two different roles, so a standard benchmark of these circuits is important because the GaN optocouplers should enhance these

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circuits so they can operate with less propagation delay, high linearity at greater temperatures, and with larger voltage isolation.

2.1.3.1 Role One: Analog Transmission

The important characteristics of the analog transmission role are linearity and propagation delay. The parameters that affect the important characteristics of the first role are the CTR, temperature, and biasing. The CTR is not linear over a particular bias point and temperature, so the output will not track the input linearly over a very large range, see Figure 2.5. Also, the propagation delay will determine the maximum frequency at which the analog optocouplers can be operated. One reason analog topologies used to transmit analog signals need auxiliary circuitry is to compensate for this nonlinear CTR parameter; generally this is done by employing feedback so that the output can accurately track the input. Another reason is that the CTR is naturally low from LED current to photodiode current. Increasing this low gain is done by adding gain into the topology with the same feedback. In some situations an open loop circuit can be used if the input LED is maintained within a small biasing range and the output stage has enough gain to overcome the low CTR gain, and this topology will be discussed later. To understand how each circuit topology effects the natural transmission of data from the input to output the natural transfer function of the most simplistic optocoupler topology method is shown in Eq. (2-6) and the schematic and waveforms in Figure 2.5.

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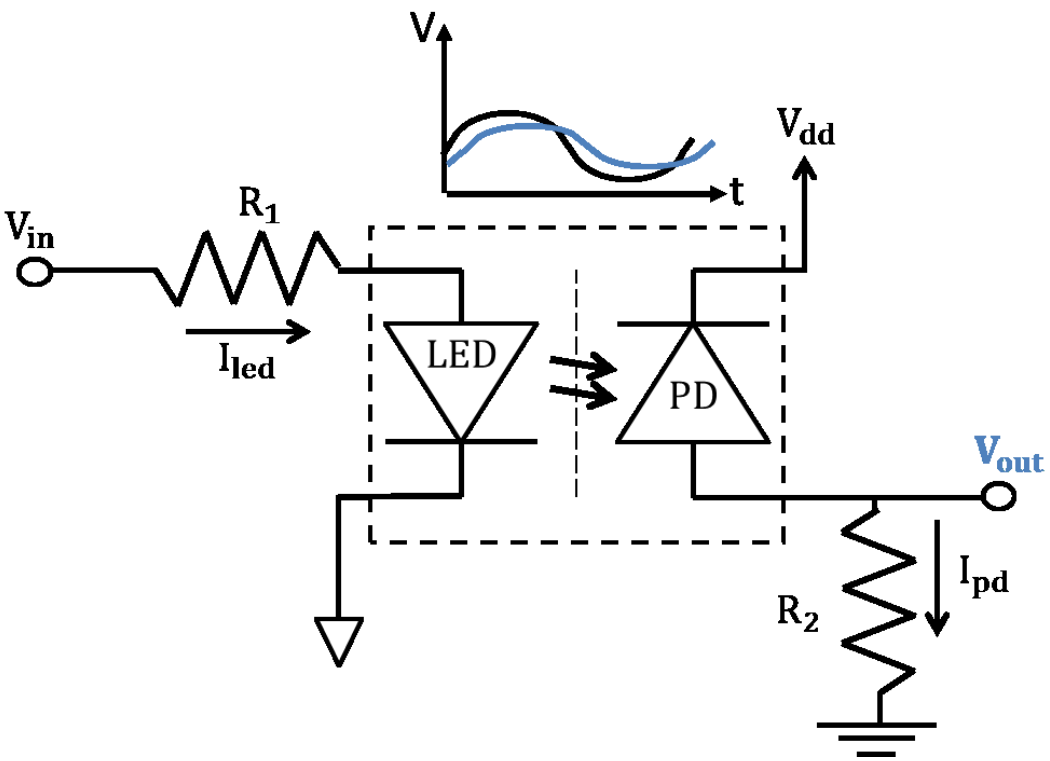


Figure 2.5 Basic transmission topology with waveform for input and output voltage

$$\frac{V_{in}}{R_1} = I_{led} \quad \textbf{(2-3)}$$

$$V_{out} = I_{pd} * R_2 \quad \textbf{(2-4)}$$

$$I_{pd} = I_{led} * CTR \quad \textbf{(2-5)}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} CTR \quad \textbf{(2-6)}$$

The input resistance R_1 is used to convert the input voltage to a current I_{led}. The photodiode current I_{pd} is generated by I_{led} at a gain equal to the current transfer parameter, CTR. I_{pd} is then converted to a voltage by the resistor R_2. The final transfer function is shown in Eq. (2-6) and Figure 2.5 shows a waveform of the input and output to illustrate the nonlinearity of the CTR parameter over a range of I_{led} and the propagation delay. Along with the nonlinearity, the output current is so small that a very large resistance would have to be chosen for R_2 to have unity gain. Even in the case that a large

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resistance is chosen, the amount of current this topology could provide to an output load (usually a capacitance) is miniscule. Topologies have been defined to circumvent these issues [7], [12].

The next analog transmission topology, shown in Figure 2.6, shows the same method of converting an input voltage and transferring it to an output photodiode current where it is then converted back to a voltage with an amplifier that can drive a load more realistically [7]. This topology also employs feedback to cancel the CTR parameter out of the transfer gain.

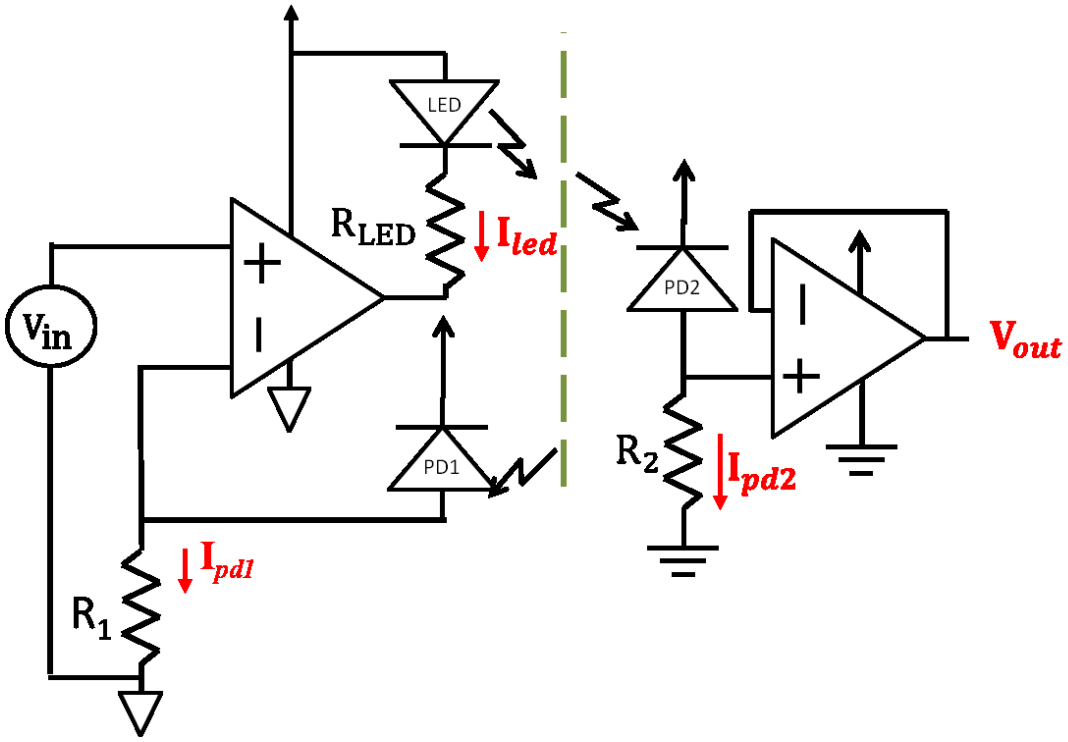


Figure 2.6 Analog transmission topology from [7]

The working principles start at an input applied to the positive node which causes the same voltage potential on the negative node (because of the virtual short of an op amp). The voltage on the negative node causes a current to flow called I_{pd1} that satisfies $\frac{V_{in}}{R_1}$. This current flows through the first photodiode as well, called the servo diode. Because this servo diode is reversed biased the current has

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to be produced by light radiating onto its PN junction from the LED. So, for the op amp to reach a steady-state (where the input terminals are at an equal voltage potential) it has to sink current equal to $\frac{I_{pd1}}{CTR}$ through the LED. This relationship is summarized in the equations below [7].

$$I_{pd1}=\frac{V_{in}}{R_1}=CTR*I_{led} \quad \textbf{(2-7)}$$

The light that impinges on the servo diode also impinges on the second photodiode. This current generates an output voltage by a current-to-voltage conversion through the resistor, R_2, connected to voltage follower configured op amp. A voltage follower is used because the voltage will have a unity gain but the op amp will be able to supply much more than the micro-amps of current that the photodiode can supply to a load [7].

$$V_{out}=I_{pd2}*R_2 \quad \textbf{(2-8)}$$

$$I_{pd2}=I_{pd1}=CTR*I_{led}=\frac{V_{in}}{R_1} \quad \textbf{(2-9)}$$

$$\frac{V_{out}}{V_{in}}=\frac{R_2}{R_1} \quad \textbf{(2-10)}$$

The transfer function shows that the feedback on the LED side of the isolation, caused by the servo diode, eliminates CTR from the transfer function. This is extremely powerful for operating the optocoupler in an analog regime over a wide range of temperatures. This means that the input voltage can be a very wide range of voltages without distorting the output because the nonlinear CTR will not affect the output voltage. Conceptually, this works because the photodiode is forced to change exactly as the input voltage changes. The LED provides the correct amount of light to bias the photodiode to satisfy the op amp's virtual short on the input. The photodiode currents will be linear in respect to the input voltage while the LED current will be non-linear, which is the opposite of normal operation. This is why this is an important topology for linear analog transmission optocouplers.

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There are a couple of problems to be analyzed in this circuit. One is that the optocouplers in this topology need to optimize propagation delays from the input to output so that the aggregate propagation delay from the op amps and optocoupler will be minimized. Also, the light that is radiated from the LED must impinge equally on the servo diode and output photodiode. A ratio, K_3, is determined to define the difference in the light shining on the two photodiodes from the LED. If this ratio is implemented into the transfer function it shows that there can still be variations, or nonlinearities, in the transfer gain if the amount of light is not the same [7]. Another trade-off is that the addition of the op amps has added more power consumption into the circuit.

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} K_3 \qquad \textbf{(2-11)}$$

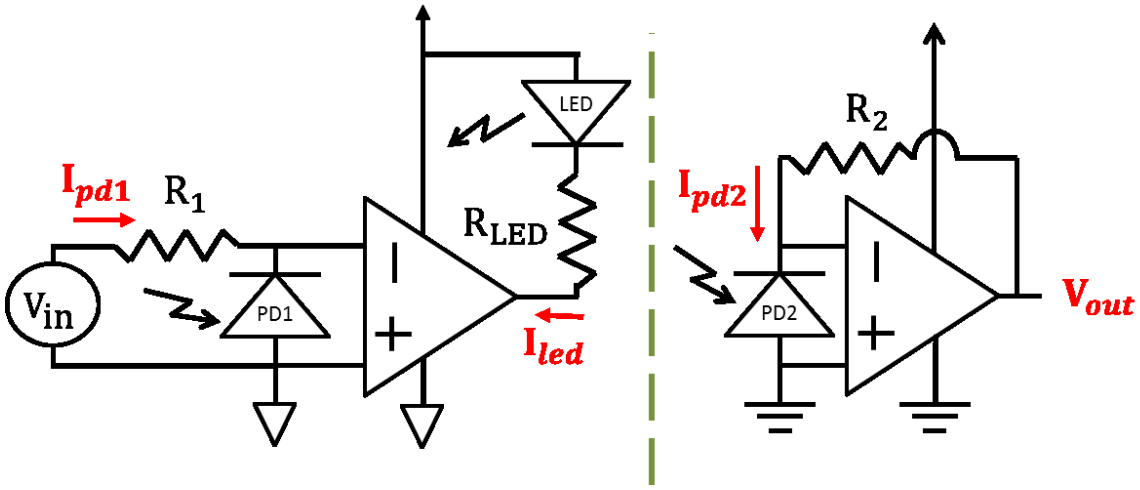


Figure 2.7 Analog transmission topology from [12]

The topology shown in Figure 2.7 is a little bit different than the previous topology but it employs the same optocoupler with a feedback photodiode. The servo diode is now connected between the positive and negative input nodes of the op amp. At a first level approximation the photocurrent, I_{pd1}, is equal to $\frac{V_{in}}{R_1}$ because the negative input is virtually grounded, since the negative and positive nodes are held equal to each other by the virtual short circuit of the op amp. The photodiode is reversed

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biased so the current must be generated by light radiating from the LED. The op amp sinks the correct amount of current through the LED (equal to $\frac{Ipd1}{CTR}$ where the actual I_{pd1} is equal to $\frac{V_{in}-V_{pd1}}{R_1}$ due to the voltage drop over the photodiode) that satisfies the small voltage difference across the inputs due to the reverse biased photodiode. The same concept is used on the output as the input, by generating the output voltage with the photodiode current, I_{pd2}, flowing through the feedback resistor R_2 [12].

$$I_{pd1}=\frac{V_{in}}{R_1}=CTR*I_{led} \quad \textbf{(2-12)}$$

$$I_{pd2}=I_{pd1}*K_3=\frac{V_{in}}{R_1}K_3 \quad \textbf{(2-13)}$$

$$\frac{V_{out}}{V_{in}}=\frac{R_2}{R_1}K_3 \quad \textbf{(2-14)}$$

The same transfer function is derived in this topology as on the previous topology. The Implementation of Optocouplers in the Buck Converter chapter will propose methods to determine to implement this linear analog transmission optocoupler into the Buck converter's feedback and the test setup to determine the benchmark for this topology.

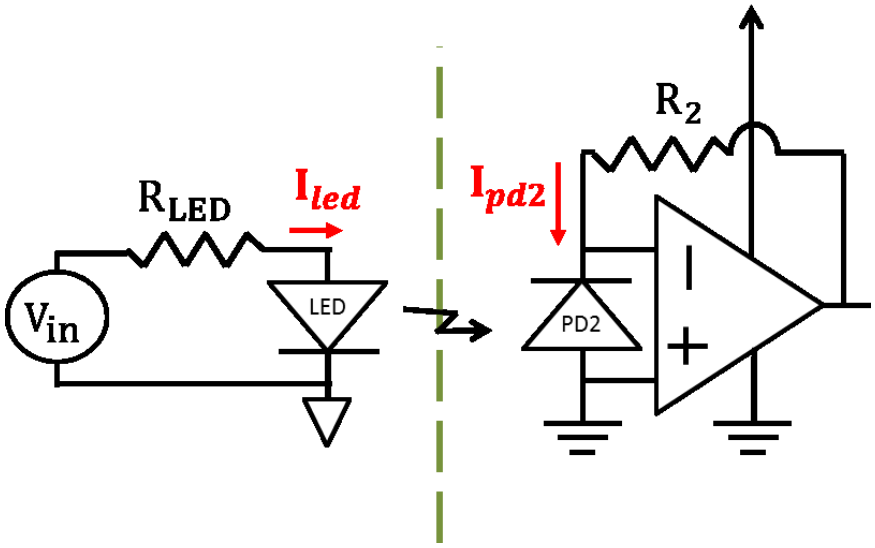


Figure 2.8 Open-loop analog transmission topology

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The topology in Figure 2.8 does not have feedback like the previous two circuits so the CTR will appear in the transfer function. It employs the same output concept as the previous topology so it is a simple derivation of the transfer gain.

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_{LED}} * CTR \qquad \textbf{(2-15)}$$

The reason this circuit would be used, even with the presence of the CTR term, would be because the input does not use a power supply. The previous two topologies utilized isolated power supplies for the input and output. Depending on where they are used in the circuit this could mean a dedicated power supply just for one op amp. The topology in Figure 2.8 is useful in these applications where an isolated power supply would have to be used to power an op amp. If the input is very well understood and kept within a small range then the CTR term can be considered constant with very small variations on the input bias of the LED. This will minimize the effect of biasing on the CTR so it will be more predictable. Temperature will cause a problem in this circuit, especially if there is a constant current flowing through the LED, not allowing the optocoupler to cool over a period of time which will create more non-linearities in the output. The Optocoupler Characterization Experiments Chapter will define experiments to test this topology over temperature and biasing to understand the benchmark performance of this application circuit that can be implemented in the Buck converter.

2.1.3.2 Role Two: Digital Transmission

The digital transmission role of optocouplers is accomplished by using circuitry around the optocoupler that allows for a voltage to be applied to the input above a threshold and a corresponding rail to rail change on the output. A digital one will be represented by the upper rail of the output and a zero by the grounded rail of the output. There are many different configurations in this category but they all use some mechanism to first, greatly amplify the overall CTR and second, use a device that is

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either on or off. This can be done using a BJT, Darlington pair, or even dedicated amplifiers. The most common and simple is a BJT configured with the photodiode supplying current to the base to turn the BJT on. The output current will have a gain of β in this case. Another common configuration is to have an amplifier with hysteresis as the output stage. The Darlington pair will not be analyzed because speed is one of the parameters that need to be optimized and Darlington pairs have very long reverse recoveries because of minority carriers in both transistors that must be swept out.

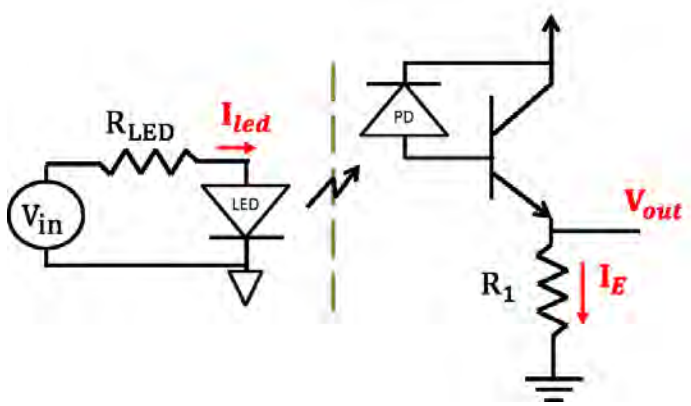


Figure 2.9 Emitter follower digital transmission topology

Figure 2.9 shows the emitter follower configuration. When there is not any current flow in the device the output BJT is off and the output on the emitter is connected to ground. When a voltage is applied to the input that causes enough current to flow in the output photodiode the BJT will turn on and the output will be connected to the supply rail. R_1 is used to bias the BJT so it does not reach saturation and can be switched on and off faster. Most data sheets will record the CTR as the ratio between the LED current and the collector current which causes the CTR term to be very large.

$$I_C=I_{led}*CTR*\beta \quad \textbf{(2-16)}$$

$$V_{CE}>1.4>V_{DD}-I_C*R_1 \quad \textbf{(2-17)}$$

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$$CTR_2 = \frac{I_C}{I_{led}} = CTR * \beta \qquad \textbf{(2-18)}$$

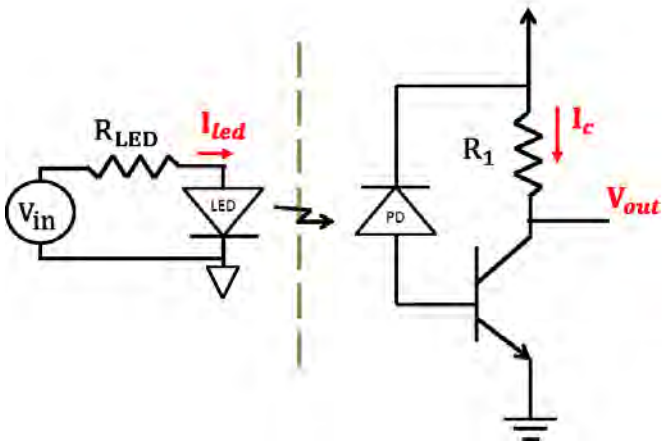


Figure 2.10 Common emitter digital transmission topology

The common emitter configuration shown in Figure 2.10 is very similar but the output is inverted from the input [13]. When there is no voltage applied on the input the output is connected to the supply rail and vice versa when a voltage is applied to the input. Most optocouplers in the digital realm operate better as common emitters because they are much faster, and because speed is important the emitter follower will not be analyzed to determine its benchmark. The figures of merit that will determine the benchmark is propagation delay, the minimum pulse width, and the power consumption. These are chosen because in an isolated transmission circuit speed is the limiting factor for the rest of the system and the power consumption determines the type of isolated supply is needed. GaN will be able to improve mostly the propagation delay because the other two are due to the technology of the BJT, but this topology will be analyzed as well so that the best digital scheme can be chosen for the all optical Buck converter design.

Something to note is the power consumption when the output is on. Both of these circuits draw power through the BJT to ground the entire duration they are on even if they supply a capacitive load.

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$$P_{out} \cong I_C^2 * R_1 \quad \textbf{(2-19)}$$

This is where the amplifier output configuration can be useful. There are various different kinds of amplifier schemes used but they all operate in the same way. The photodiode is connected to some kind of drive circuit (usually through a Schmitt trigger) that drives a totem pole configuration. Another difference is the input. It can be either a bare LED or an amplifier controlling the LED biasing as seen in Figure 2.11 [11], [10].

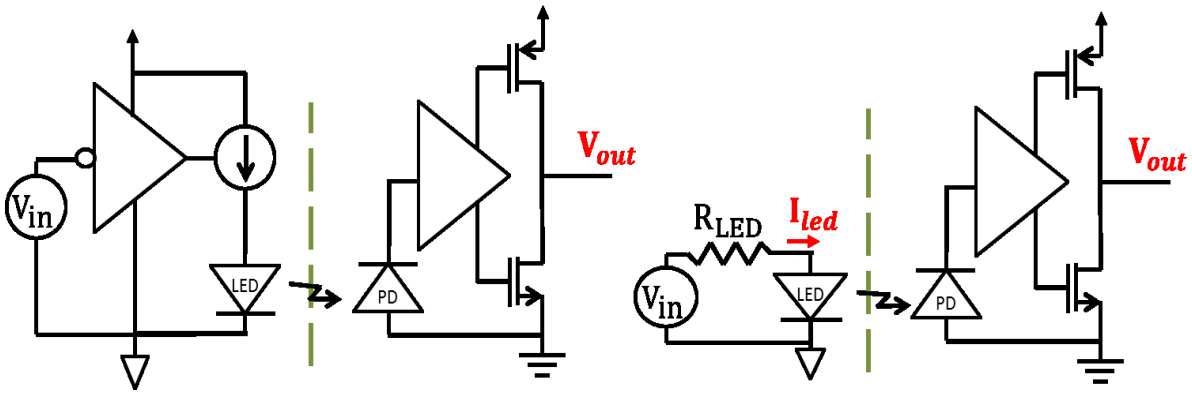


Figure 2.11 Two different digital optocouplers with different input stages and output amplifier configuration [11], [10]

The Optocoupler Characterization Experiments chapter will analyze the differences between these three types (LED and BJT pair), LED and amplifier pair, and amp-LED and amplifier pair) to determine the fastest and shortest pulse width available. There is no need to analyze the transfer functions because these devices are truly on and off devices.

It can be seen that the parameters of the overall transfer gain, propagation delay from input to output, bandwidth, fall and rise time, and isolation voltage are an aggregate of the components within the circuit. Op amp selection, along with passive component selection will affect the circuit's operation. The importance of defining these circuits is twofold: to determine the benchmarks of the overall circuits

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with various optocouplers – seen in the Optocoupler Characterization Experiments Chapter – and to design an optical Buck converter that operates to its maximum switching frequencies and temperatures determined by current optocoupler technologies and circuit schemes. Now that all the application topologies for the two different categories are understood the Buck converter will be analyzed.

2.2 Buck Converter

The current-mode optically-controlled Buck converter can now be analyzed since the basic operation of the optocoupler and its applications that will be tested to determine a benchmark for current optocoupler technologies is understood. This section will break down the application system in which the optocouplers will be applied. The basic Buck converter's operation will be presented along with the current-mode control scheme.

The choices to apply the optocouplers in this specific system have to do with the needs that this system will create that can be satisfied by the optocoupler. The Buck converter has a switch that is not connected to ground. Since an *n*-type MOSFET will be used the gate will have to be 10 to 15 V above the source potential. Since the source is floating, the gate driver (to be presented in much greater detail in the next section) will have to be isolated from any other ground reference in either the Buck circuit or the control circuit. This will be called the high-side because the power supplied to the gate driver will be referenced to the source node of the MOSFET. Current-mode control will be explained in greater detail, but the overall reason for choosing it as the control scheme is because there are two feedback loops. The reason two feedback loops are desirable is because this thesis is not trying to determine the best Buck converter, but to determine how optocouplers affect a dc-dc converter when they are used to transmit information to the control circuitry. Current-mode control has two feedback loops that need to transmit a floating referenced current signal, and a ground referenced voltage signal. Using the optocoupler in these two completely different signal paths will give a better insight into its overall

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capabilities. The first loop measures the output voltage and this sensed signal must be transmitted across the isolation barrier between the Buck converter circuitry to the control circuitry. The second loop is also referenced to the source node of the MOSFET and this loop will measure the inductor current and transmit it to the control circuitry through the isolation barrier. Figure 2.12 is a very basic graphical representation of all the different isolation barriers and blocks in the overall system. With this system in place the Buck converter can operate with an input voltage up to the withstanding voltage of the optocouplers and still have very low voltage, isolated control circuitry.

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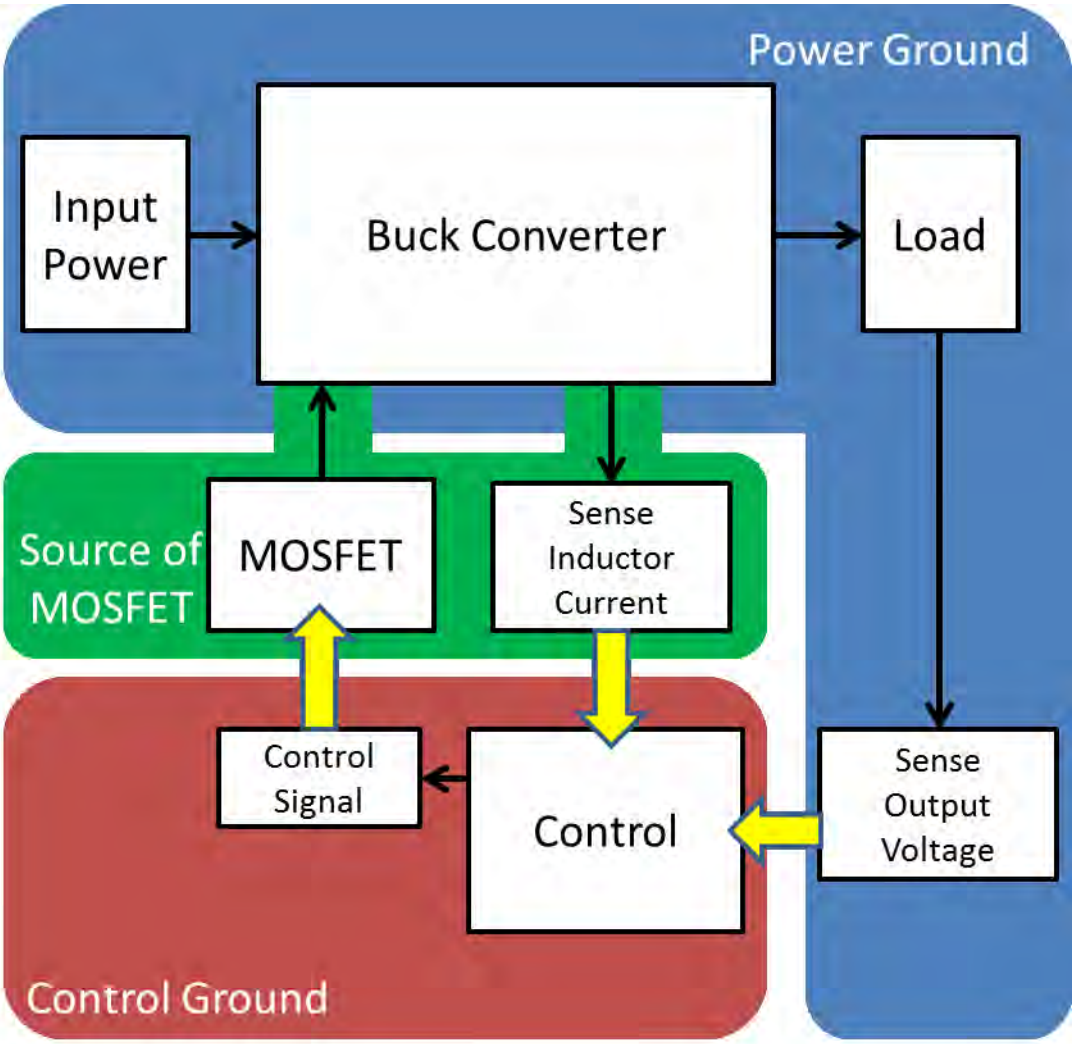


Figure 2.12 Graphical representation showing the control reference's isolation from 1) power ground (Buck converter and output load and voltage sensing), and 2) source of the MOSFET (gate driver and inductor current sensing reference) – yellow arrows are signals transmitted through the isolation barrier between the control circuitry and the rest of the circuitry

2.2.1 Buck Converter Operation

The Buck converter is a specific topology in the class of dc to dc converters. It is one of the building blocks for other, more complicated, converters. Figure 2.13 shows the schematic representation of an open-loop Buck converter. At steady-state the output voltage is held at a fraction

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of the input voltage. When the loop is closed by feeding back the output voltage state to control circuitry the output voltage can stay at a specified value with varying input voltage and load conditions (this is called voltage mode control). The key component of the circuit is the switch. It turns on and off at a specific frequency, and the ratio of the on time to the period of the switching time determines the output voltage.

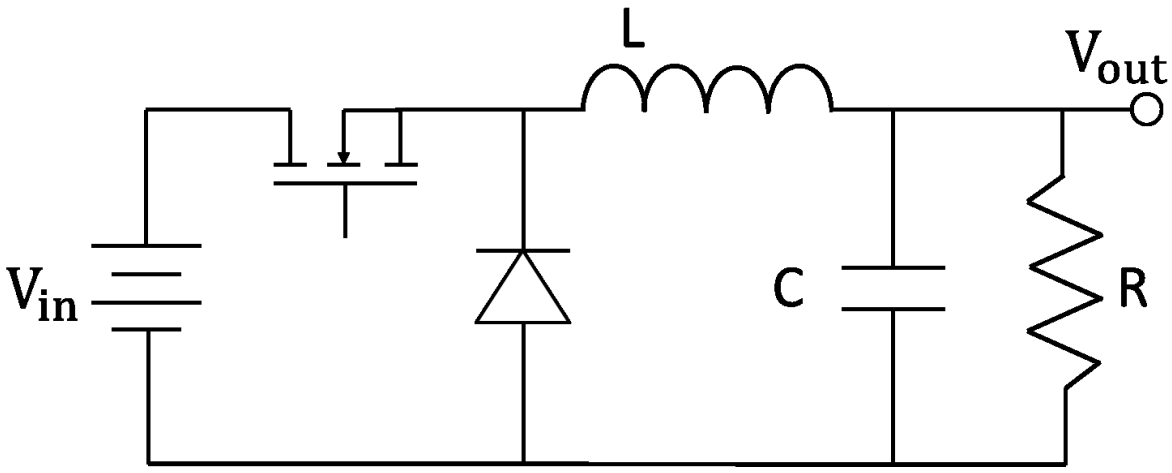


Figure 2.13 Open-loop Buck converter schematic

$$V_{out}=\left(\frac{t_{on}}{T}\right)V_{in}=D*V_{in} \qquad \textbf{(2-20)}$$

This ratio is called the duty cycle (D) and its relationship with the output voltage will be quantified thoroughly later. To understand the operation of the Buck converter the converter must be analyzed during the two different switching events, while the switch is on, which is mode one, and while it is off, called mode two [14]. There are also two different operating regimes of a Buck converter, continuous and discontinuous. This relates to the current in the inductor. In the continuous regime the current of the inductor is always positive and in the discontinuous regime the current in the inductor becomes zero before the end of the switching cycle [14]. The continuous regime is analyzed below and is used in the final system.

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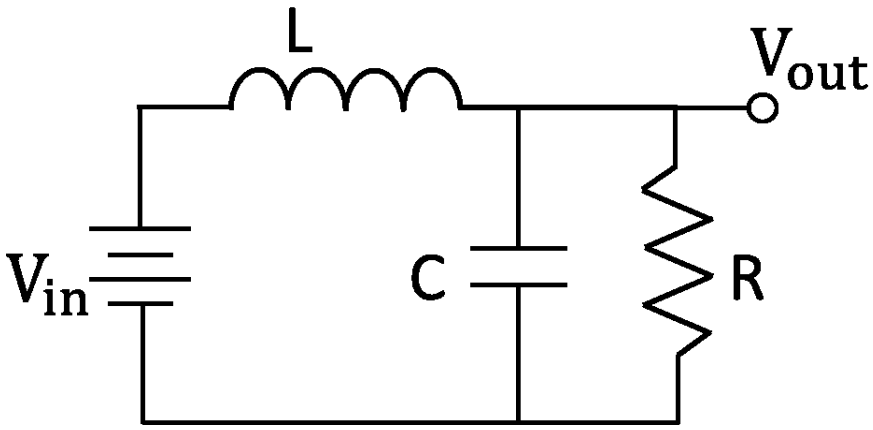


Figure 2.14 Equivalent circuit when switch is closed (mode one)

The beginning of mode one happens when the switch is closed. The equivalent circuit is shown in Figure 2.14. The input voltage is larger than the output voltage so the current through the inductor (L) ramps up and energy is stored in the inductor and capacitor. If the inductor is large enough the rise in inductor current is approximately linear [14].

$$V_{in}-V_{out}=L\frac{di_L}{dt}=L\frac{I_2-I_1}{t_{on}}=L\frac{\Delta I}{t_{on}} \qquad \textbf{(2-21)}$$

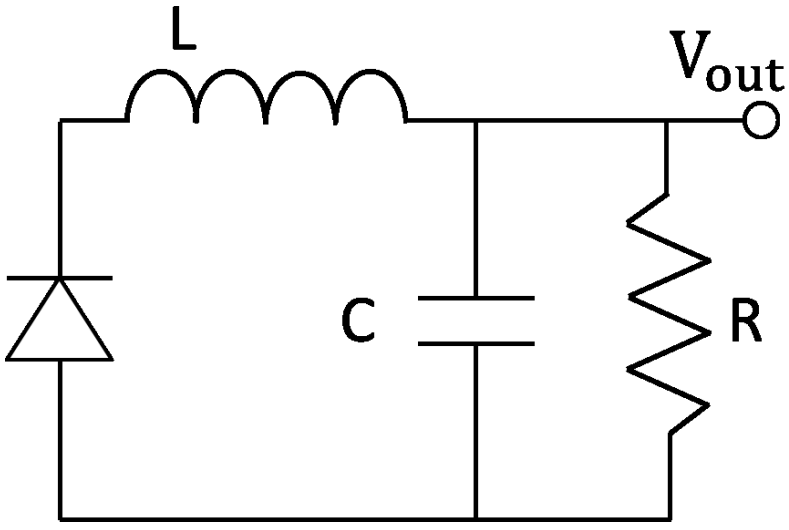


Figure 2.15 Equivalent circuit when switch opens (mode two)

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When the switch opens mode two begins. The equivalent circuit is shown in Figure 2.15, it can be seen that this mode is characterized by the stored energy in the inductor and capacitor discharging through the resistor. The diode allows the current in the inductor to flow continuously when the switch is turned off, since it is not possible for the current in the inductor to change instantaneously. To maintain this current the voltage polarity across the inductor reverses. The inductor current decays (approximately linearly if L is large enough) from I_2 to I_1 in this mode [14].

$$-V_{out}=L\frac{di_L}{dt}=L\frac{I_1-I_2}{t_{off}} \quad \textbf{(2-22)}$$

$$V_{out}=L\frac{I_2-I_1}{t_{off}}=L\frac{\Delta I}{t_{off}} \quad \textbf{(2-23)}$$

Now the average output voltage can be found by solving the equation for mode one and two for ΔI and setting them equal to each other. The duty cycle (D) is the ratio of the on-time to the period of the switching time determines the output voltage, $D=\frac{t_{on}}{T}$, and the period is the sum of the on- and off-time, $T=t_{on}+t_{off}$ [14].

$$\Delta I=\frac{(V_{in}-V_{out})t_{on}}{L}=\frac{V_{out}t_{off}}{L} \quad \textbf{(2-24)}$$

$$(V_{in}-V_{out})DT=V_{out}(1-D)T \quad \textbf{(2-25)}$$

$$V_{out}=D*V_{in} \quad \textbf{(2-26)}$$

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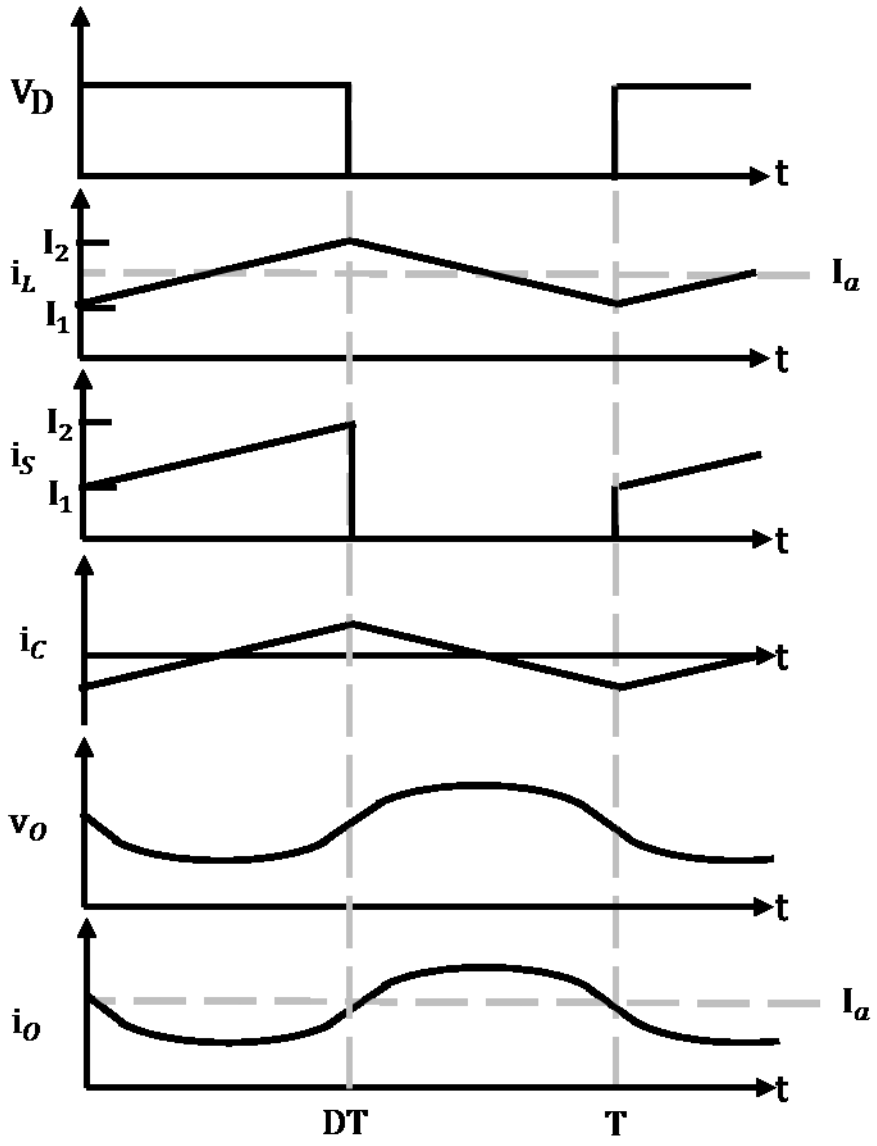


Figure 2.16 Waveforms for Buck converter [14]

The waveforms of the duty cycle, load current (i_o), and output voltage (v_O), are shown in Figure 2.16. The output voltage is related directly to the duty cycle and the input voltage. If the on-time of the switch is half of the off-time then the output voltage will be half of the input voltage at steady state. This is just the average value; there are also ripples in the current (ΔI) and voltage (Δv_c) because of the charge and discharge actions of the inductor and capacitor.

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$$T=\frac{L\Delta I}{V_{in}-V_{out}}+\frac{L\Delta I}{V_{out}}=\frac{LV_{in}\Delta I}{V_{out}(V_{in}-V_{out})} \quad \textbf{(2-27)}$$

$$\Delta I=\frac{DV_{in}(1-D)}{f_s L} \quad \textbf{(2-28)}$$

$$\Delta v_c=\frac{1}{c}\int_0^{\frac{T}{2}}\frac{\Delta I}{4}dt=\frac{\Delta I}{8f_s C}=\frac{V_{in}D(1-D)}{8f_s^2 LC} \quad \textbf{(2-29)}$$

Eq.'s (2-27) – (2-29) show that as the inductor and capacitor increase the current and voltage ripple will decrease. These are important design equations that will be used to determine the ripples of the final system. All of these equations are correct for steady-state operation, but how does the effect of line or load changes and start-up affect the open-loop Buck converter? Without controlling the duty cycle this circuit will be unstable in open-loop. The loop is closed by using system variables, in this case inductor current and output, or capacitor, voltage to control the duty cycle. This technique is called current-mode control [1].

2.2.2 Peak Current-Mode Control Feedback

It is desired to hold the output voltage constant even if the input voltage has a transient or changes to a different voltage level indefinitely. Following Eq. (2-20), without controlling the duty cycle of the converter the output voltage will follow the changes in the input voltage directly. Also, if the load changes and starts to draw more or less current the output voltage would change if the duty cycle in Eq. (2-20) was not controlled for that transient. It is possible that the open-loop Buck converter would reach its steady-state output voltage again, but it might also go unstable and stop functioning properly. The goal of any control system for a Buck converter is to control the on- and off-time of the switch at a given frequency to maintain a constant output voltage in lieu of line or load changes. Pulse width modulation (PWM) is used to vary the duty cycle by controlling the on- and off-time of the switching transistor. This is a square wave signal that can be a fixed or variable frequency signal. A fixed frequency signal is generated by changing the on- and off-time of the switch while maintaining a constant period. To do this

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the switch is turned on at a fixed period so the duration of the on-time determines the amount of off-time. A variable frequency is generated by keeping the on-time fixed and varying the off-time [14].

Generally there are numerous schemes to do this broken up into two main categories, voltage- and current-mode control. Within the two categories there is a variety of more specific schemes. To simplify this background section only current-mode control will be discussed because it is the only scheme that is used. This is not the procedure for designing the optimal Buck converter, but because this design's purpose is to create an application to demonstrate an all optical control scheme, current-mode control is better because of its multiple feedback loops.

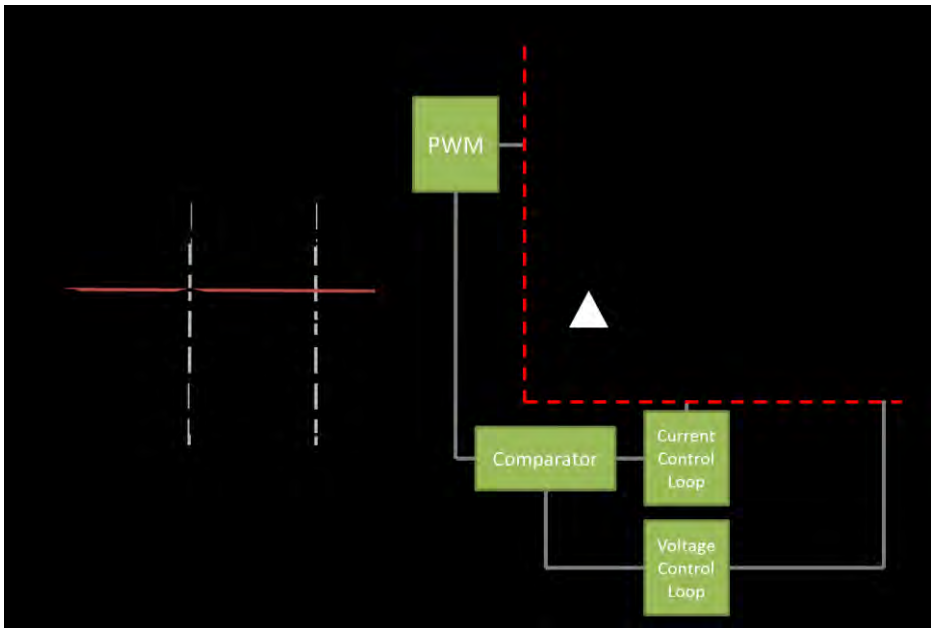


Figure 2.17 Block diagram showing two loop feedback system of the peak current mode control scheme

Current-mode control basically senses the inductor current and compares it to the output voltage to generate a PWM that controls the switches duty cycle. The comparator commands a square wave to turn off and an external oscillator commands the square wave to turn on, thus creating a PWM.

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The inner current loop senses the inductor current, scales, adds compensation (discussed later), and compares it to the error voltage generated in the outer voltage loop. Figure 2.17 shows a simple schematic for current-mode control and the waveforms that go along with it. The error voltage generated in the voltage loops becomes the upper limit to the inductor current. When the inductor current intersects the error voltage the PWM signals the switching transistor to turn off. This function's obvious advantage is that it allows for cycle to cycle overcurrent protection. The switch is then turned on again by an external clock to set a fixed period. So the duty cycle is controlled by how fast the current intersects the error voltage [1]. One additional element that current-mode control needs is slope compensation. This compensates for the sub-harmonic oscillations that are present in the current of the inductor when the duty cycle is greater than 50% [15].

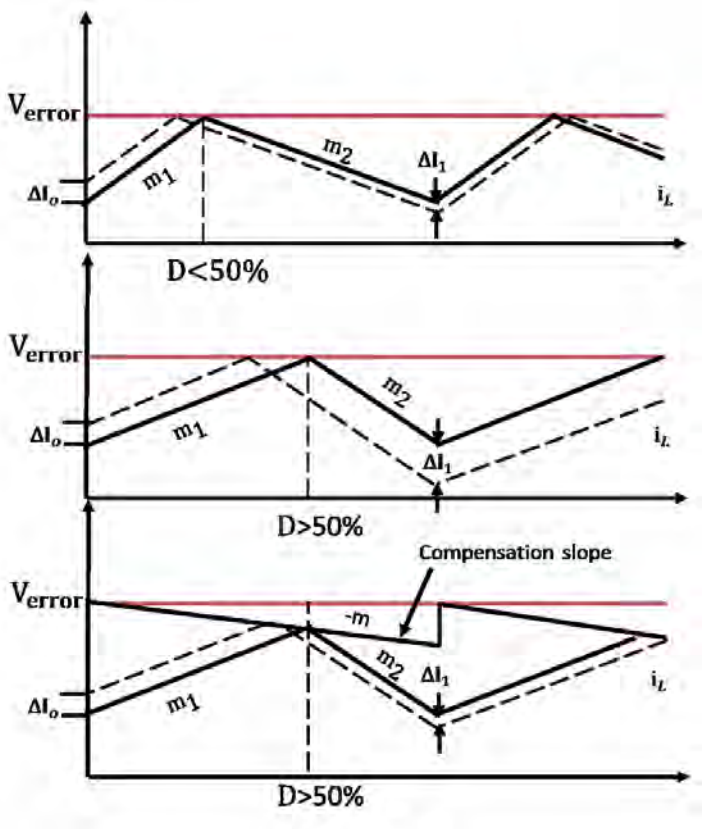


Figure 2.18 Waveforms showing the problem of sub-harmonic oscillations [15]

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In Figure 2.18 the waveforms of the inductor current signal being compared to an error voltage are shown. In the top graph the duty cycle is less than 50% so any oscillation (shown as ΔI_o) in the current will die out over multiple cycles quantified in Eq. (2-30) [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right); m_1 > m_2 \quad \textbf{(2-30)}$$

If the duty cycle increases beyond 50% the oscillations will grow each cycle, as shown in the middle graph of Figure 2.18. The equation below quantifies this behavior [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right); m_1 < m_2 \quad \textbf{(2-31)}$$

With the same duty cycle an additional slope (slope compensation) is added to the current signal (or subtracted from the error voltage, depending on the implementation method), and the bottom graph shows that with even a duty cycle greater than 50% the oscillations are attenuated each cycle. Eq. (2-32) shows this quantitatively by adding slope to the current signal [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2+m}{m_1+m}\right); \text{solving for m at 100\% duty cycle} \quad \textbf{(2-32)}$$

$$m > -\frac{1}{2} m_2 \quad \textbf{(2-33)}$$

Implementing slope compensation will be discussed with the design of the current-mode optically-controlled Buck converter because there are various methods depending on configuration of the current sensing network and the external clock. The main reason current-mode control is chosen over voltage mode control is because of the need for high-side current sensing. At high voltages this becomes a problem because the reference node for sensing the current is at a high, floating, voltage. Optocouplers with high speed transmission of analog signals are needed to overcome this problem.

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2.2.3 Optocoupler's Role in the Buck Converter

Understanding the application topologies of the optocouplers and how current-mode control is implemented in a Buck converter the need for optocouplers can now be seen. The current-mode control needs the inductor current and output voltage information. But as in Figure 2.12 (the overall block diagram) it is seen that both of these signals are referenced to different potentials in the power stage part of the circuit. This information needs to be transmitted through the isolation barrier to the control part of the circuit. Once there the information is processed to determine the correct duty cycle to apply to the Buck converter to maintain a stable output voltage. Now that the duty cycle is determined the switching commands need to be sent back across the isolation barrier to the isolated gate driver on the power stage side of the circuit. The different application topologies of the optocoupler will be implemented to transmit both the inductor current and output voltage along with sending the switching commands to the gate driver. Figure 2.19 shows a block diagram of the optocoupler's location in the Buck converter closed loop system as blue arrows pointing in the direction of signal flow through the isolation barrier. The only missing block in this diagram is the gate driver. Another section is needed to fully describe the gate driver.

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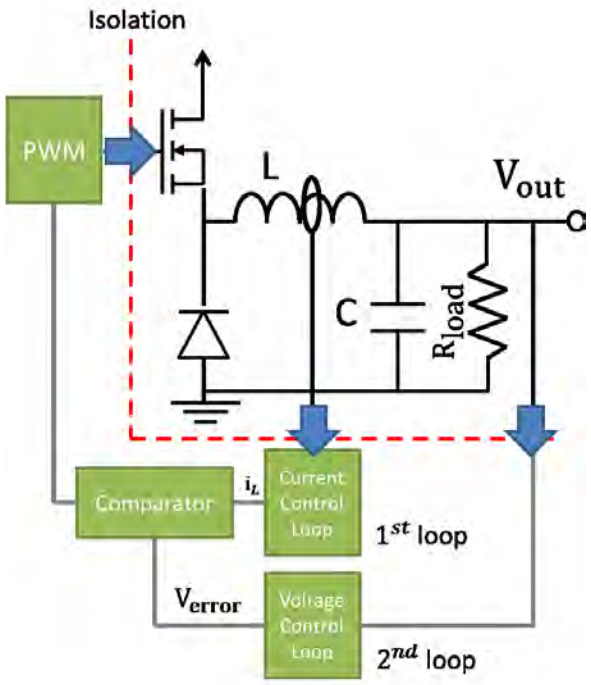


Figure 2.19 Current mode optically controlled Buck converter with blue arrows showing placement of optocouplers. Take note of the type of signals transmitted for each optocoupler (digital gate signal and two analog system variables).

2.3 Gate Drivers

The gate driver is important for multiple reasons; the first of which is to the Buck converter. The MOSFET must be turned on and off with a device that can buffer the low power PWM signal to the power level needed to turn on a MOSFET quickly. Another reason is to expose the digital optocouplers minimum pulse width. The optocoupler will need to transmit the PWM information through the isolation barrier to the isolated power supply with a minimum pulse width. Two gate drivers that need two separate on and off commands (requiring two separate optocouplers) with small pulse widths will be compared (with a conventional gate driver as a control) to determine which one is applicable to this design. A tertiary reason is to determine the lowest power consuming gate driver in the collaborative research with South Carolina.

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As stated earlier the switch in the Buck converter does not have a source referenced to ground. A PWM signal referenced to the control circuitry ground is used to tell the switching transistor in a switch-mode power supply when to turn off and on, but there is a problem. The MOSFET needs about a 15 V difference between the gate and source terminals for it to turn completely on and the voltage to keep the gate off will have to be equal to and typically below the source voltage while it is floating. The optocoupler will allow for a control ground referenced PWM signal to be transmitted through the isolation barrier so that on the output it is referenced to the source's reference point, but there is another problem. The PWM signal on the output of the optocoupler can usually only source or sink milliamps of current and for a power MOSFET to be turned on and off in the nanosecond range it will needs Amps of current. This is where the isolated gate driver will occupy. It will be a buffer between the low power PWM signal and high power needed to turn the gate of a MOSFET on quickly. To better understand the gate driver's purpose of buffering the PWM signal the turn on and off of a gate driver must be understood, the next section discusses the way a MOSFET turns on in more depth.

2.3.1 MOSFET Turn-On Analysis

The turn on procedure of a MOSFET needs to be understood to realize the need and purpose of a gate driver. Figure 2.20 shows the schematic used to describe the switching transient of a power MOSFET. The load inductance charges to the drain current of the power MOSFET while it is on and the current discharges through the freewheeling diode when the MOSFET is off. The change in the inductor current during charge and discharge is very small during one switching cycle [7].

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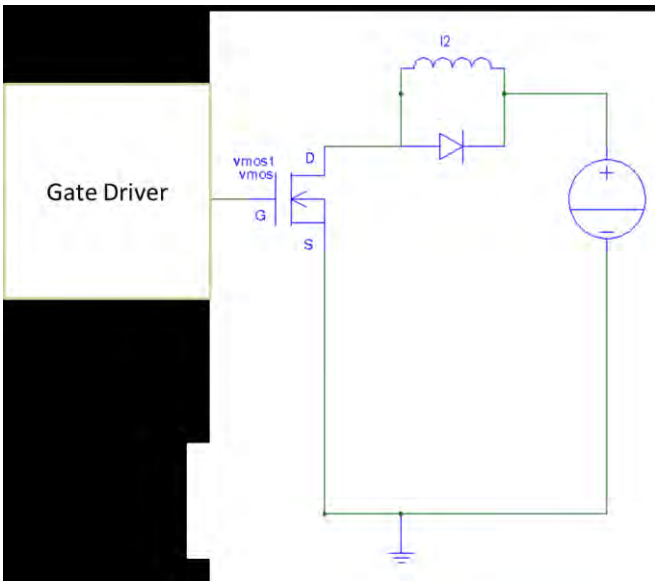


Figure 2.20 Clamped inductive load test setup

The switch is initially off and the load current flows through the diode. The gate voltage (v_G) and drain current (i_D) equals zero while the drain voltage (v_D) equals the input voltage (V_{DD}). The gate driver is also turned on and starts to charge the capacitances (C_{GD} and C_{GS}) of the power MOSFET. No drain current can flow until the gate-source voltage (v_{GS}) exceeds the threshold voltage of the device so the drain voltage stays at V_{DD}. Because the drain voltage is constant this means that C_{GD} stays constant. So until drain current begins to flow only C_{GS} is charging. The gate voltage reaches the threshold voltage at t_1 in Figure 2.21. At this point drain current starts to flow but the drain voltage remains constant because, until the MOSFET can accept the entire load current, the freewheeling diode cannot sustain a voltage other than its forward voltage [16].

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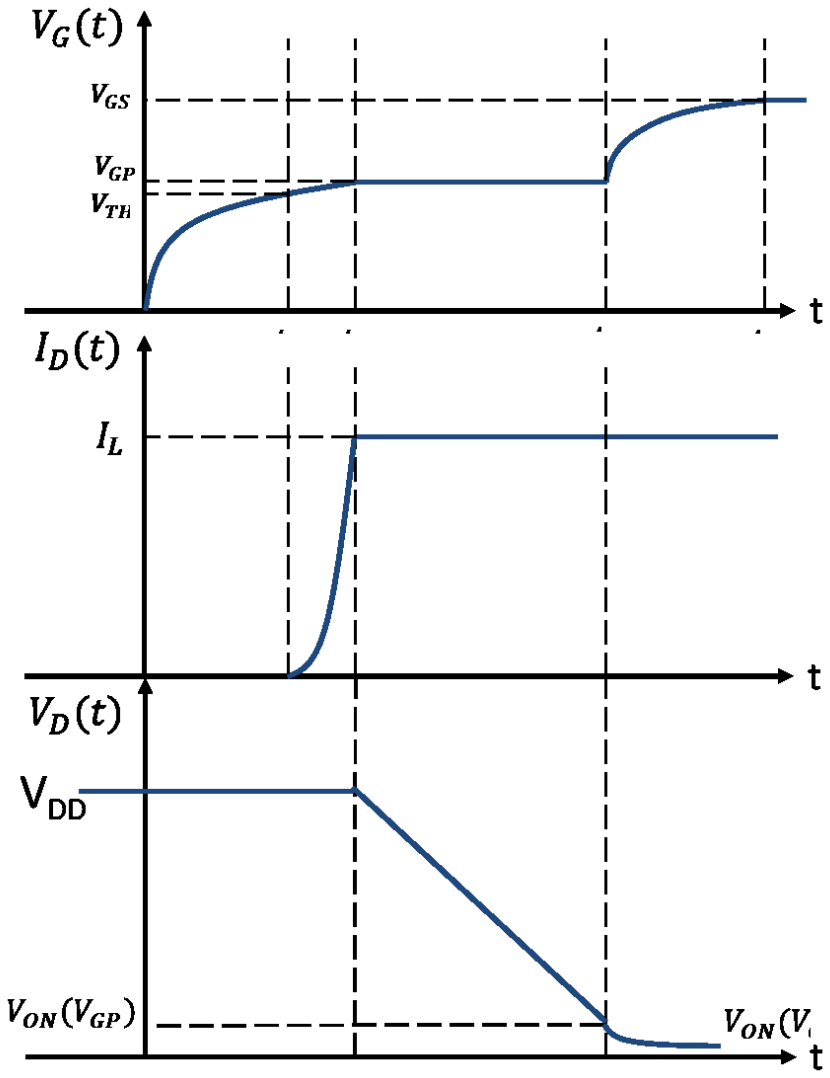


Figure 2.21 Turn-on waveforms for MOSFET [16]

At t_2 in Figure 2.21 the drain current equals the load current and now the drain voltage starts to decrease toward the forward voltage of the MOSFET ($V_{ON}(V_{GP})$). It can be seen that the gate voltage flattens out while the drain voltage decreases to the on-state voltage between t_2 and t_3. This is due to all of the gate current charging the gate-drain capacitance; this is called the Miller capacitance. The drain voltage becomes equal to the on-state voltage of the MOSFET with a gate voltage of V_{GP} at t_3 where the gate voltage, again, increases to the voltage applied by the gate driver, V_{GS} [16]. The turn-off

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transient is similar enough in operation to the turn-on operation that it will not be described in full detail here but the reader is directed to [16] for an in-depth analysis. The gate driver is the main focus in this section and in the circuits that will be analyzed the turn-off procedure is symmetrical to turn-on, even in the presence of slightly different phenomena that occur in the turn-off transient of the MOSFET.

It can be seen that the gate voltage increases in a finite amount of time determined by the time it takes to charge C_{GS} and C_{GD}. Three different gate drivers are presented below that will control this charge time, the conventional gate driver, a resonant switching gate driver, and finally a resonant switching gate driver with an energy recovery function [2], [17]. The first gate driver is the most basic gate driver and it is presented to get a basic understanding of the procedure a gate driver goes through to turn on and off a MOSFET and to be a control to compare the other two more exotic gate drivers to. The next gate driver is presented in [17] uses resonance to charge the gate capacitances. This is analyzed because with resonant switching the peak current can be shaved and the input power decreased [17]. The final gate driver uses resonance and then a freewheeling diode scheme to return energy stored in the inductor back to the source and is presented in [2]. Power consumption is important because the power supply to the gate driver is a separate isolated power supply referenced to the source of the MOSFET and must be supplied through means of the isolation techniques that have been discussed. This technique to use optocouplers for sending isolated power will not be analyzed further in this thesis because this is another component of research being done by the University of South Carolina. The gate driver selection is important in the research presented here because either one chosen needs the small pulse width pulses that will help determine the baseline performance of the digital transmission optocouplers.

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2.3.2 Specific Gate Drivers Examined

In these three gate drivers the operation will be analyzed. What is not shown is how the switches in the gate driver are turned on and off. This will be discussed further in a different section because it is a topic in itself and has to do with the overall design of the full system.

2.3.2.1 Conventional Gate Driver

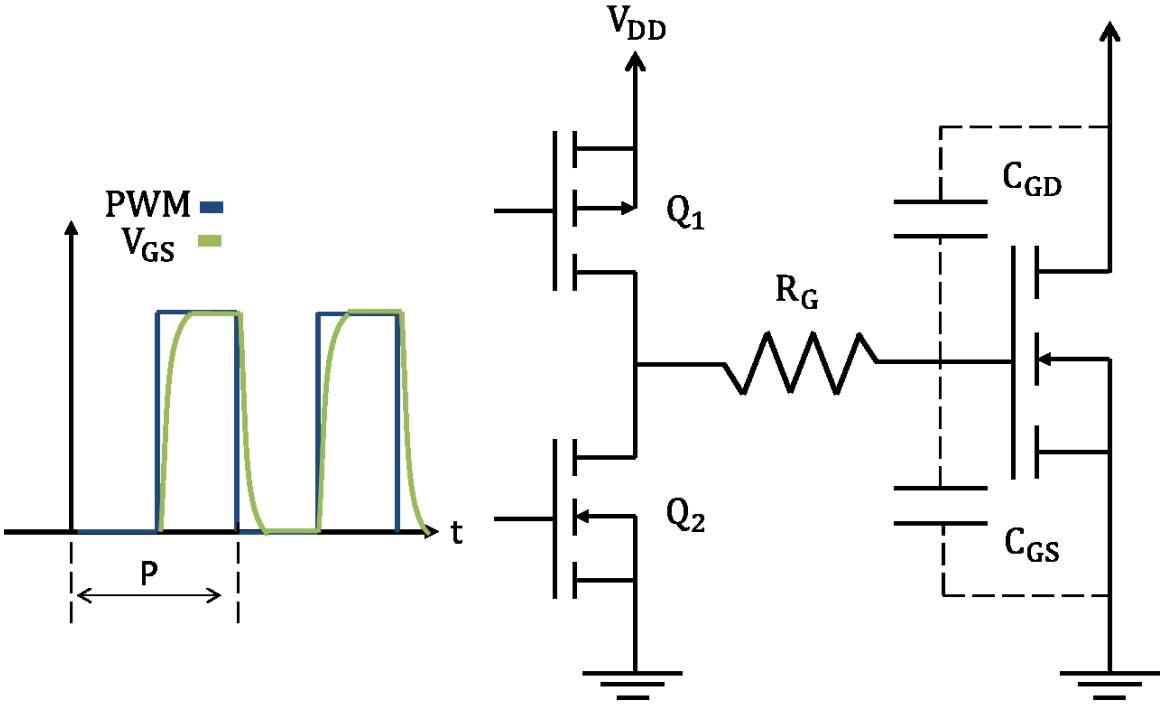


Figure 2.22 Conventional gate driver with basic waveforms

The conventional gate driver is a well-known, fundamental topology with a half-bridge (or totem pole) configuration of two complimentary switching transistors, Q_1 and Q_2. The PWM signal turns on and off Q_1 and Q_2 to control the switching event of the MOSFET shown in Figure 2.22. When the PWM is high the top MOSFET is on and when the PWM is low the bottom MOSFET is on. The MOSFETS are never allowed to be on at the same time. The circuit operates by sourcing current through the gate resistor to charge the gate source capacitance of the MOSFET to V_{DD} when Q_1 is on. The high-side transistor must

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stay on to maintain the MOSFET in its on-state. To turn the MOSFET off the high-side transistor turns off and the low-side transistor turns on, connecting the gate terminal of the power FET to the source terminal of Q_2 and discharging the gate source capacitance to the source potential of Q_2, so that V_{GS} is zero.

2.3.2.2 Resonant Gate Driver

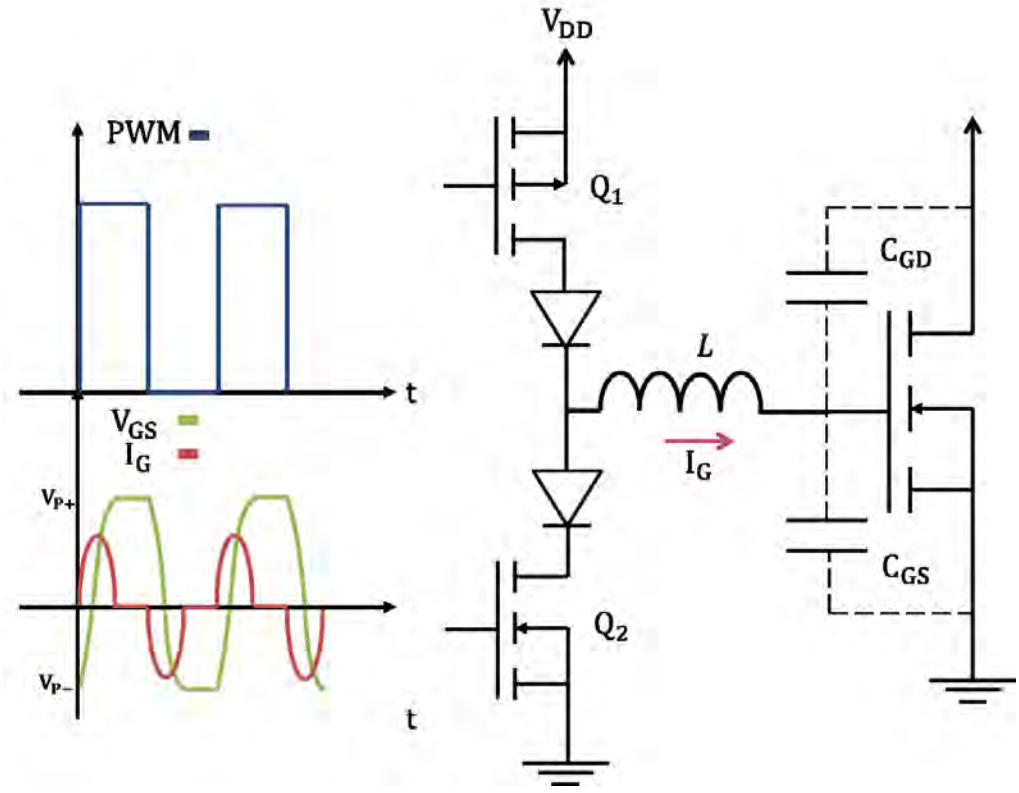


Figure 2.23 Resonant gate driver with basic waveforms [17]

This gate driver adds two diodes and an inductor into the path of the current shown in Figure 2.23. The turn on and off action of this gate driver is characterized by a resonant transition. "Initially Q_1 is on and Q_2 is off, and V_{GS} is at a negative peak (V_{p-} in Figure 2.23)" [17]. The transistors change switching positions and current flows through Q_1 and into the negatively charged C_{GS} storing energy in the inductor. The current flowing through the inductor peaks as V_{GS} reaches zero. The energy stored in

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the inductor begins to discharge into C_{GS} causing V_{GS} to rise above zero as current decreases. V_{P+} is reached when the current in the inductor is fully dissipated and will be greater than V_{DD}. This is allowed because the diode will block any possible discharge path. The turn off operation is the same with current flowing in the reverse direction. Again the gate voltage is charged to a voltage less than the ground reference due to the resonant action and the diode [17].

2.3.2.3 Energy Recovery Resonant Gate Driver

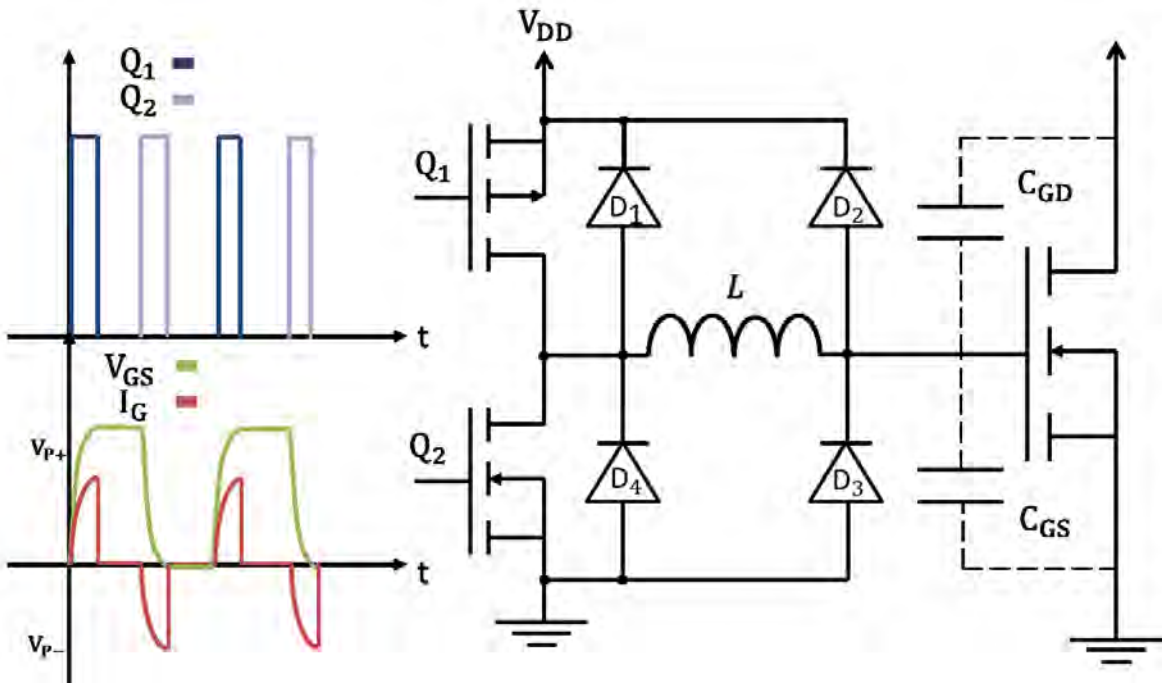


Figure 2.24 Energy recovery gate driver with basic waveforms [2]

The difference in resonant gate driver in Figure 2.24 is its ability to capture energy in the resonant transition and recover it using two added freewheeling diodes. While Q_1 is on the gate capacitances resonate with the inductor charging the gate to V_{DD}. When the gate reaches this voltage the current is at a peak and the D_2 diode clamps the gate from be charged any higher than V_{DD}. When Q_1 is turned off the current in the inductor cannot change direction and causes the freewheeling diodes (D_2,D_4) to conduct which returns the energy stored in the inductor back to the source. This is the energy

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recovery action of the circuit. It is important to note that to return the energy the MOSFET must be turned off; otherwise the energy will circulate between the inductor, D_2, and the MOSFET, being dissipated by the stray resistances. The turn off event is exactly the same but with Q_2 and D_1,D_3 acting in the discharge and energy recovery paths [2].

Also, the control scheme for the two resonant gate drivers needs to be described because it differs largely from the control scheme of the conventional gate driver topology. This is due to the need to have a single pulse for the on command and another, separate pulse, for the off command. By comparison the conventional topology only needs one signal to drive both the *p*-type and *n*-type MOSFETs.

Specifically for the energy recovery gate driver the energy recovery action cannot occur until the circulating current is directed back to the source by turning off all MOSFET's as talked about above, so the MOSFET is only pulsed the duration of the on or off time [2]. Adding the separate pulse control scheme adds some complexity in controlling this gate driver.

2.3.3 Controlling Gate Driver Switching Events

A half-bridge is the control action of the gate driver's above, a simple cascade of MOSFETs with the common connection between the two as the output. It is a simple topology that controls the flow of power to the output. If the high-side (HS) MOSFET is on power flows to the output and if the low-side (LS) MOSFET is on the output is connected to ground. An avoided event is when both MOSFETs are on. This short circuits the supply to ground through the on-resistances of the two MOSFETs producing large currents that can damage the switches and the power supply depending on the duration of the event. The half-bridge is a useful topology to charge and discharge the gate of a MOSFET. The MOSFETS can either be CMOS (LS NMOS and HS PMOS) or a fully NMOS configuration.

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The CMOS configuration is simpler to control because it takes advantage of the fact that the PMOS gate must be at a lower potential than the source to conduct and the NMOS gate needs a higher potential on the gate relative to the source. Even though control is simplified there are many disadvantages. PMOS has a slower turn on time and their conduction resistance is higher. The solution is using an NMOSFET in place of the PMOSFET. The disadvantage to this scheme is the voltage of the gate on the HS MOSFET needs to float above the source node to be turned on. A simple solution is using a method called boot-strapping, Figure 2.25 shows the schematic for a simple boot-strapping network [3].

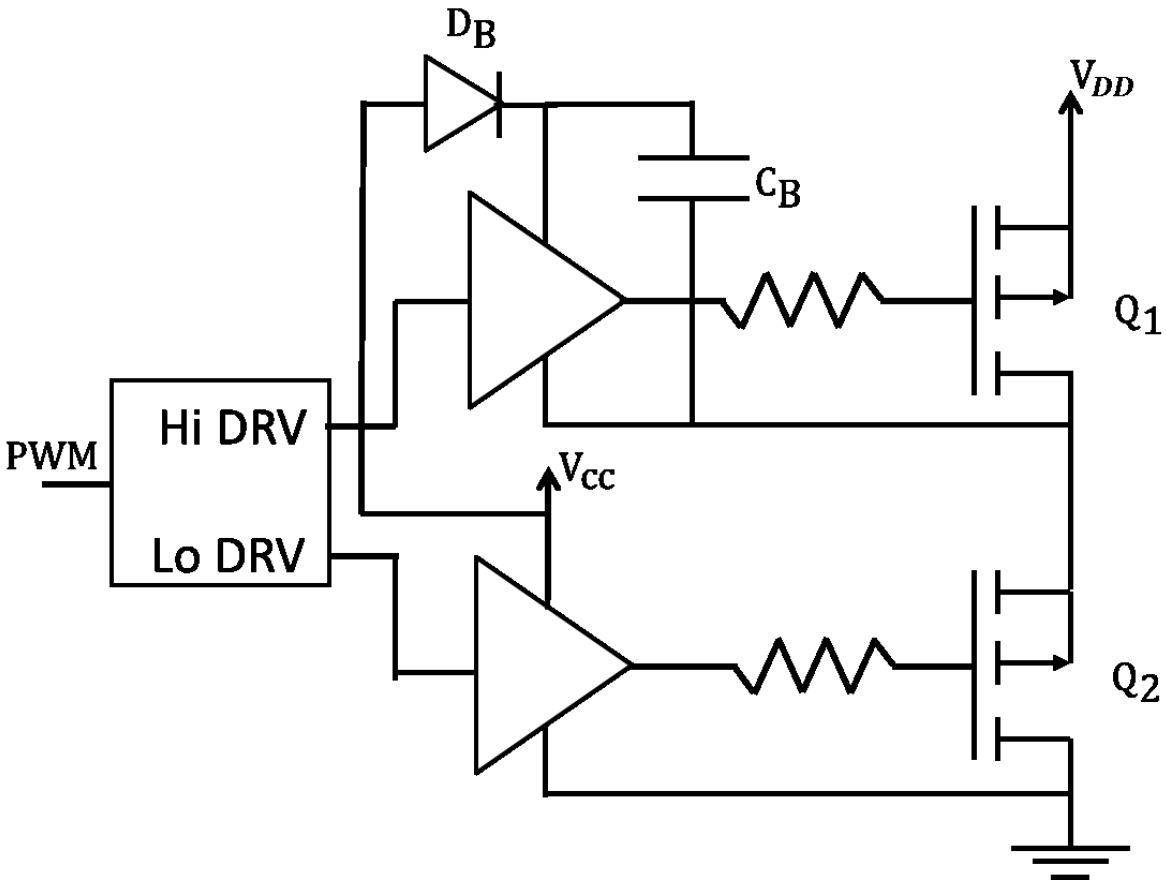


Figure 2.25 Bootstrap circuit for half-bridge topology [3]

Bootstrapping works by using the rule of a capacitor that its voltage cannot change instantaneously. First, Q_2 is on and the output is pulled to ground through this transistor. Q_2 being on

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first is important because it also allows the bootstrap capacitor C_B to charge to V_{cc} through the diode. When Q_2 turns off and Q_1 is commanded to turn on the bootstrap diode D_B stops C_B from discharging and the voltage potential V_{cc} is across the source of the HS NMOS and its gate. If C_B has much greater charge than is needed for the HS NMOS C_{GS} then the gate will be charged to $V_{cc}+V_{source}$, thus turning it on. Any charge that was lost on C_B will be replaced when Q_2 turns on again [3].

This chapter discussed the theory behind the functionality, control, and operation of three gate drivers that will be used to operate the MOSFET in the Buck converter. The basic operation of the Buck converter was analyzed along with the control method and the value optocouplers will add to the overall design. The optocouplers natural parameters where analyzed along with the two different categories, analog and digital transmission, and the topologies that allow that operation. The next chapter will evaluate the gate driver that consumes the least amount of power in simulation and the design choices made in its PCB construction to be used in the final system. Another chapter, Optocoupler Characterization Experiments, is dedicated to the experimental setups that are used to determine the benchmark of the currently available optocouplers operating in the most fundamental topologies and discussing the results from these experiments. Once the individual optocoupler topologies are understood the Buck converter with optocouplers implemented in the full system will then be designed. The design procedure will be analyzed and presented to choose both the needed parts for the open-loop Buck converter, its feedback and control circuitry, and the optocoupler topologies that will be used to implement the isolation. Finally, in the Conclusions Chapter, the impact of optocouplers on the Buck converter system is discussed and the final benchmark for the optocouplers is presented.

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3 GATE DRIVER DESIGN

The goal of this chapter is to determine the gate driver with the least power consumption and determine the most stable two pulse gate driver. As stated in the previous chapter, it is important to minimize the power that is needed for the isolated power supply that powers the gate driver because it will need to be generated independently from the power supply for the control circuitry or Buck converter. Also, stability is important to the operation of the system with non-ideal components that introduce noise through parasitics that can disrupt the operation of the gate driver.

3.1 Stage One: Validation of Gate Driver Designs

The gate driver design goes through three different stages: from the initial simulation tests to evaluating the best gate driver for the system with a non-ideal simulation, and finally, a gate driver on a printed circuit board (PCB). The first stage is validating with a simulator that the resonant designs presented in the two papers cited will work.

The next stage is implementing a more realistic model in the simulator with more non-ideal components focused on obtaining the total power consumption. This will include using a fully modeled MOSFET for the load of the gate driver. The SiC MOSFET is chosen for the final design because of its commercial availability and the in house model designed by Mihir Mudholkar at the University of Arkansas. This SiC MOSFET will be the switch that needs to be controlled in the Buck converter. Table 3.1 shows its notable parameters [18].

Table 3.1 SiC MOSFET Parameters [18]

SiC MOSFET Parameters	
Irated	20 A
Breakdown Voltage	1200 V
Nominal On Gate Voltage	18 V
Total Gate Charge	90.1 nC
C_{iss}	1.9 nF

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With the non-ideal implementation the two resonant designs will be compared with the conventional design to see if they truly improve over hard switching in the simulations. The design with the best performance will be implemented in hardware, and the final stage will be designing and testing the best gate driver on a PCB. This section will give simulation results so that a choice on the best gate driver can be made for the design of the Buck converter, and the following sections will display the results of the gate driver implemented on a PCB.

Something to notice initially is the desired turn on voltage of the SiC MOSFET. A graph, shown in Figure 3.1, is made of the on-resistance of the SiC MOSFET on the y-axis, and the on-voltage on the x-axis to determine the lowest on-voltage that can be utilized. The purpose of this is to decrease the requirements of the gate driver's power supply at the smallest cost to conduction losses. The gate voltage is optimized at 15 V because between 15 and 20 V the on-resistance changes from 150 mΩ to 100 mΩ. Also, increasing to 16 V only provides a 16% decrease in the on resistance while decreasing the gate voltage to 14 V there is about a 25% increase. Because of the test setup for the full Buck converter system a compromise had to be made and the final gate voltage selected is 10 V. This is due to the upper limit of the voltage supplies that will drive the gate of the power FET is 10 V. The drain current is only going to be 5 A so the on-resistance will still be less than 1 Ω. If this thesis was to determine the optimum Buck converter this compromise would not be possible. But, the 1 Ω on-resistance that a 10 V gate voltage will cause is not a hindrance in this system because the power of the Buck converter will not be analyzed. The only important aspect is that the power FET can operate at the voltages levels that are needed to fully test the optocouplers, and that it doesn't impede the switching frequency of the Buck converter before the optocoupler transmission circuitry does.

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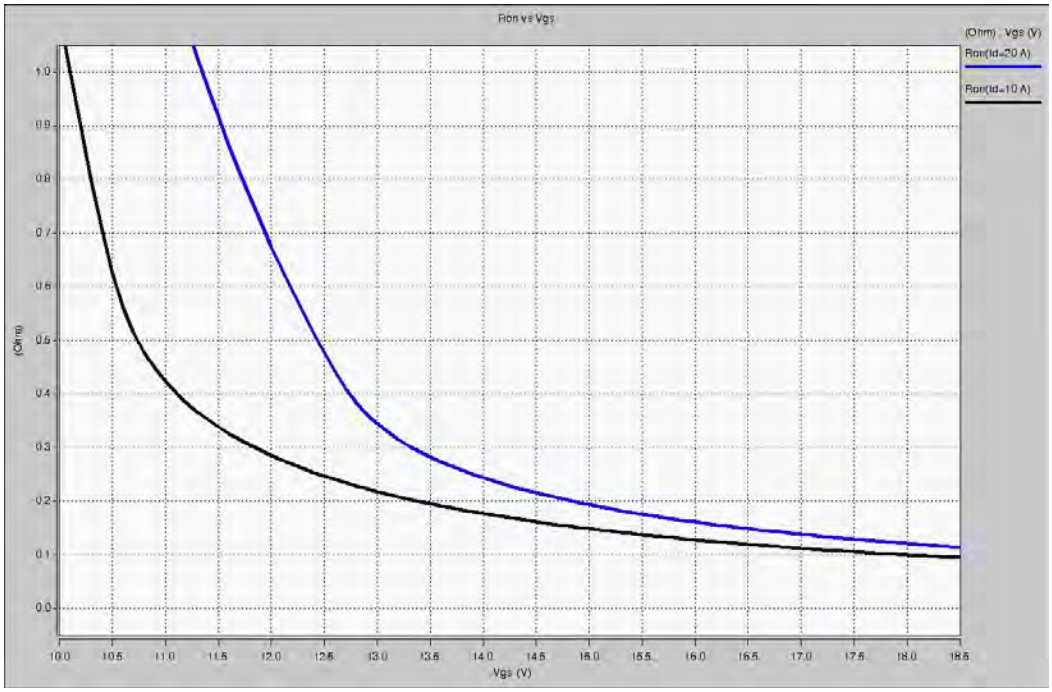


Figure 3.1 On-resistance vs. gate voltage derived from SiC MOSFET model

Some simplifications are made to the circuits to quickly validate the gate driver designs. A capacitor is put in place of the gate of the MOSFET to represent the C_{gs} of the SiC MOSFET. The total input capacitance is 1915 pF [18].This simplification takes away the Miller capacitance effect discussed in Chapter 2. Voltage-controlled switches are put in place of the half-bridge MOSFET configuration. The voltage-controlled switches are used because for validation a full MOSFET model is not needed and too complex to troubleshoot the main function of the gate driver, charging and discharging the gate to source capacitance.

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3.1.1 Conventional Gate Driver

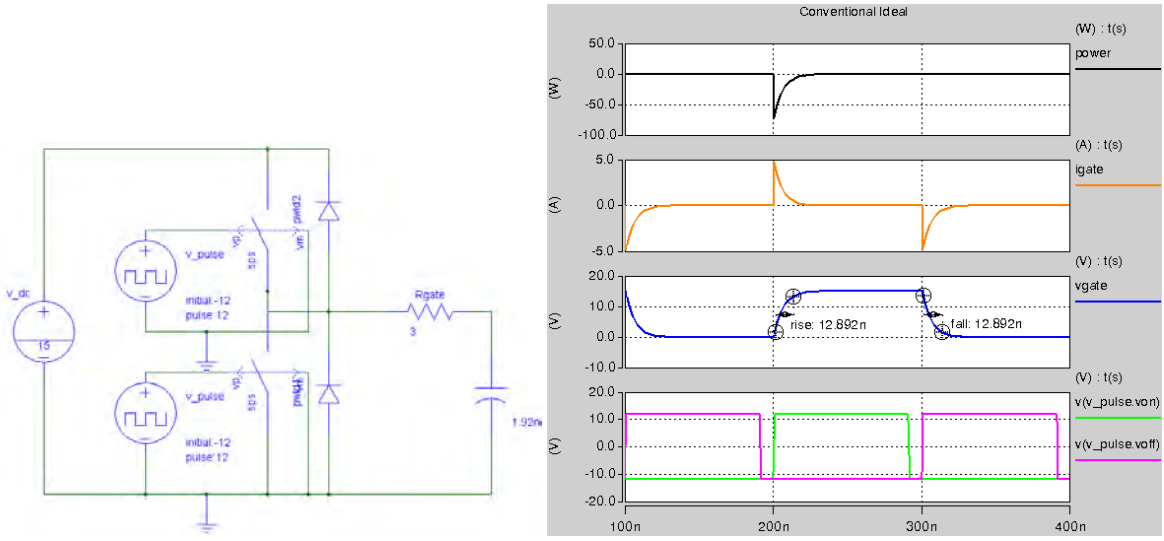


Figure 3.2 Conventional gate driver simulation schematic and waveforms

The conventional gate driver is easily verified in Figure 3.2, where the schematic of the simulated circuit and the respective waveforms are shown. The gate voltage at turn-on is equivalent to a figure shown in the previous chapter of the gate voltage of a power FET turning on. The gate current spikes initially and then exponentially decays, as expected for a capacitor charging. The turn on and off times are determined by the gate resistance and voltage supply. The equations below give a good approximation of turn on time while neglecting the miller capacitance, C_{GD}.

$$C_{GS}\frac{dV_{GS}}{dt}=\frac{(V_{DD}-V_{GS})}{R_G} \qquad \textbf{(3-1)}$$

$$V_{GS}(t_{90\%})=V_{DD}-\frac{V_{DD}}{e^{\frac{t_{90\%}}{R_G C_{GS}}}} \qquad \textbf{(3-2)}$$

$$t_{90\%}=2.3*R_G C_{GS}=13.2\text{ ns} \qquad \textbf{(3-3)}$$

This equation says that V_{GS} reaches 90% of its final value in about two time-constants, which is a good estimation for turn-on time. The waveforms show this estimation is correct. Another thing to note

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is the shape and magnitude of the current, or more specifically the power. This is what will need to be decreased by the resonant designs if they are to be implemented.

3.1.2 Resonant Gate Driver

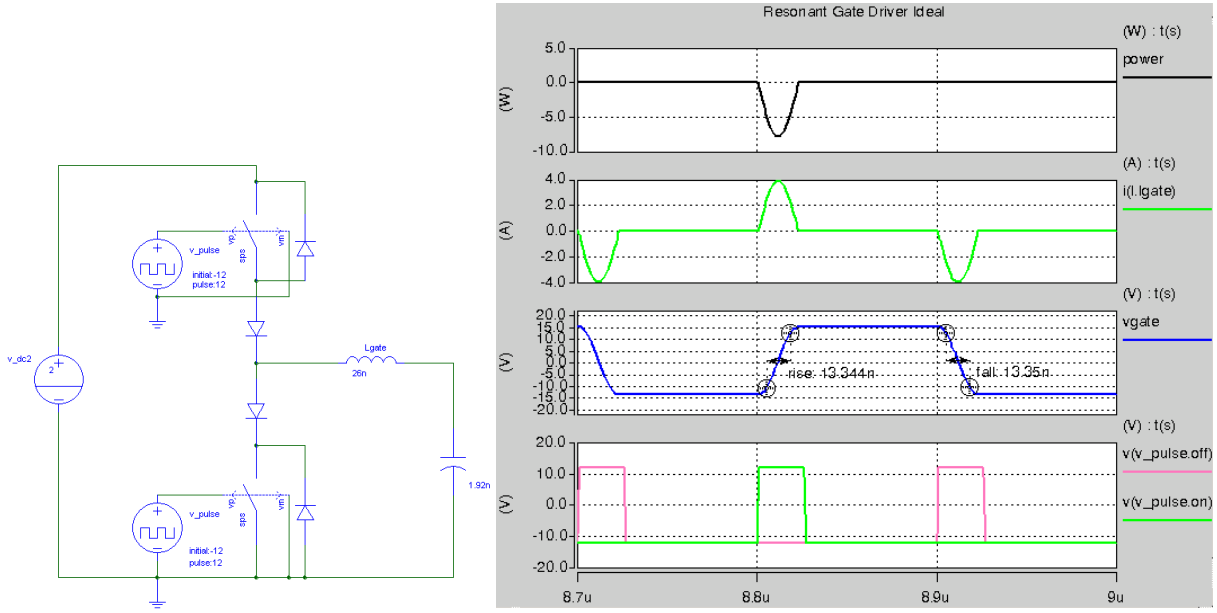


Figure 3.3 Resonant gate driver simulation schematic and switching waveforms

Figure 3.3 shows the resonant gate driver's schematic and waveforms. The gate voltage profile is very similar to the conventional gate driver waveforms except that it swings from -15 to 15 V. The difference is in the current waveform (green). Because of the inductor the current is initially zero. The current peak corresponds with 0 V, thus minimizing turn-on power consumption. The natural resonance frequency is used to approximate the turn-on time [17]. The inductor and capacitor are allowed to resonate for only one half of a resonance frequency of $\frac{1}{2\pi\sqrt{LC}}$.

$$t_{90\%}=0.9\pi\sqrt{LC}=19 \text{ ns} \quad \textbf{(3-4)}$$

The input source only needs to be 2 V in order to achieve the 15 V on-voltage because the resonance of the circuit allows the gate voltage to increase much larger than the input voltage and the diode clamps that increased gate voltage so it won't dissipate back to 2 V [17]. This is very desirable

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because it effectively decreases the power consumption by 87% (assuming the same magnitude of the charging current). It can also be seen that the switches do not need to stay on to maintain the gate potential because the added diodes prevent the gate from discharging to the 2 V source through the body diode.

3.1.3 Energy Recovery Resonant Gate Driver

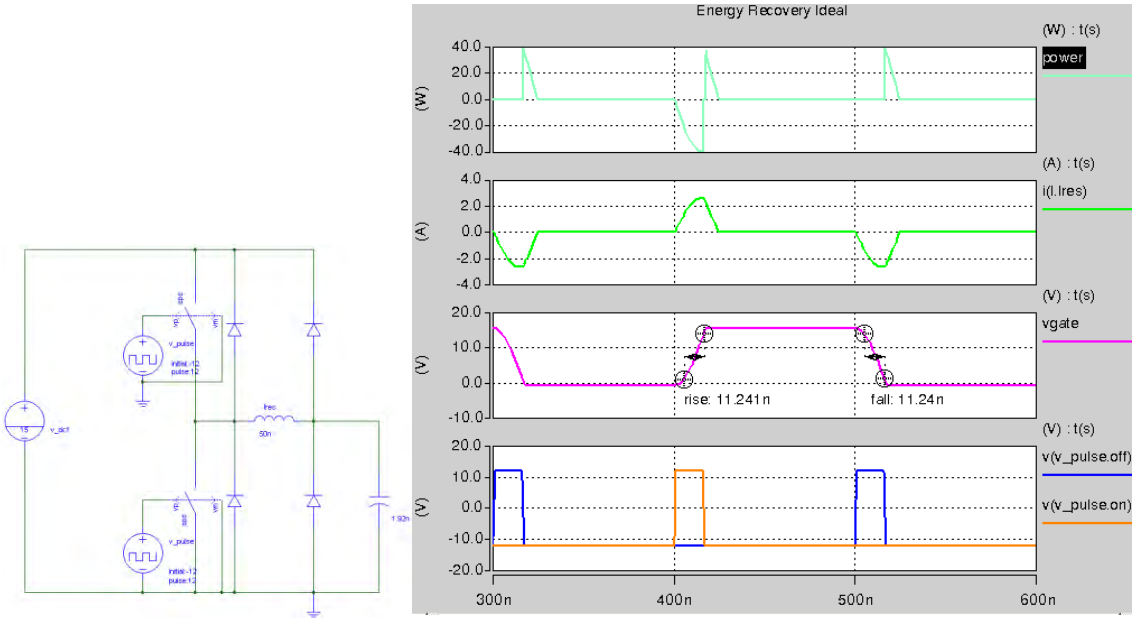


Figure 3.4 Energy recovery resonant gate driver simulation schematic with waveforms

Figure 3.4 shows the schematic and waveforms of the energy recovery resonant gate driver. The profiles of the gate current and voltage are identical to the previous resonant gate driver except that the gate voltage is initially 0 V and is charged to 15 V. The greatest difference in this design is in the power waveform (light green). When the gate voltage reaches the input voltage the high-side MOSFET is turned off (shown as the orange control signal). The power waveform then becomes positive as the current is directed back to the source. In this resonant gate driver the gate voltage is equal to the power supply when the gate is fully charged. The on-time is now only one-fourth of a resonant period.

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$$t_{90\%}=0.9*\frac{\pi\sqrt{LC}}{2}=13.8\text{ ns}$$

The energy consumption is larger than the simple resonant gate driver but this gate driver returns energy to the source whenever the high-side switch turns off and during the discharge period. It is seen here that in order to get the energy recovery, like it is stated in the background chapter, the switches must be turned off at the right time. If they stay on too long the energy in the inductor will be discharged through the conduction resistances and not transferred back to the source.

3.2 Stage Two: Non-ideal Implementation and Evaluation Setup

Now that the gate drivers are validated the non-ideal elements replace all the simplifications made in the previous section. The SiC MOSFET model replaces the capacitor so now a simple circuit is designed to allow for the Miller capacitance effect to factor into the power consumption of the gate driver. A simple test circuit is used to bias the SiC MOSFET, and the setup is shown in Figure 3.5. It is designed to set the drain current to 10 A (within the 20 A current range), and the blocking voltage to 100V (The maximum voltage the MOSFET will block in the Buck converter). Each gate driver is implemented in the same design so that the results are consistent with each gate driver so power consumption comparisons can be made.

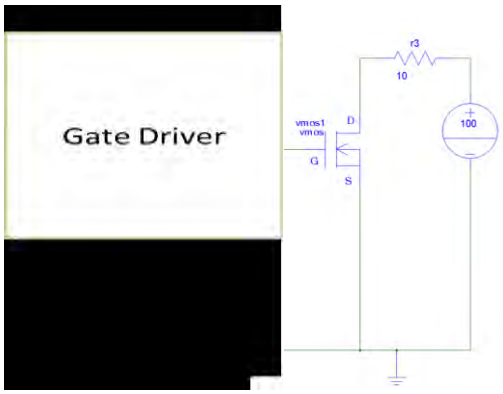


Figure 3.5 Clamped Inductive load test for evaluation purposes

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The voltage-controlled switches are not replaced with models of the MOSFET's that will be used in the final hardware implementation because the losses due to the MOSFET will be consistent across all three devices and thus can be eliminated. In the final circuit the IRLM2030 is chosen for the MOSFET's because they have very fast turn-on times and they can easily conduct enough current [19]. They will be placed on the low-side and high-side of the totem pole in an NMOS half-bridge configuration. When implemented this will use the bootstrapping circuit discussed in the background section to control the turn-on and turn-off of the high-side NMOS because the source node is floating. Because this driving scheme is used in all of the gate drivers and the power consumed by charging the bootstrap capacitor is common among all three, it will be excluded from the simulation evaluation.

The final selection will keep the turn-on time of the SiC MOSFET constant while analyzing the average power consumption over a period. Another aspect that will determine selection will be the stability of the gate voltage while it is turned on. Because the resonant gate drivers have short duration command pulses, the gate driver will float between switching events. If there are large transients in application circuit in which the SiC MOSFET is placed, the gate drain capacitance could cause a false switching event. The simulation results and evaluation will be presented in the following section along with the PCB implementation and validation.

The three gate drivers to be compared were presented and validated in the previous section. Now the validation goes one step further by simulating a non-ideal version of the gate driver to determine the least power consuming, and most stable, gate driver. This one will be implemented in a PCB to be used with the full system.

Figure 3.6 through Figure 3.8 show the waveform comparisons of the final test over an entire period, turn-on, and turn-off time, respectively.

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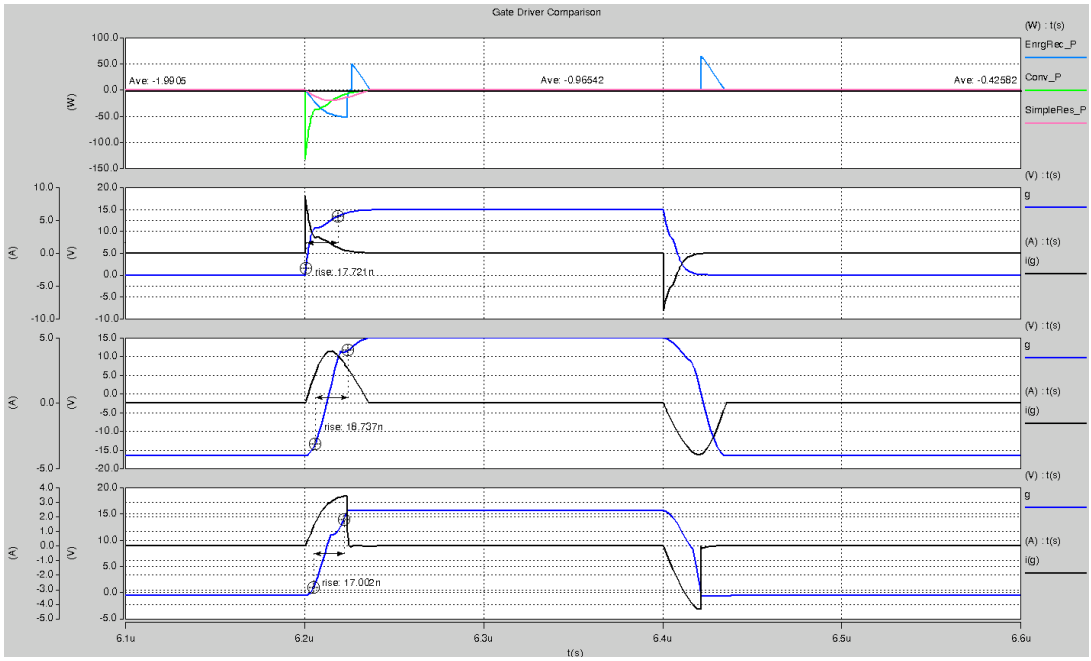


Figure 3.6 Full period comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

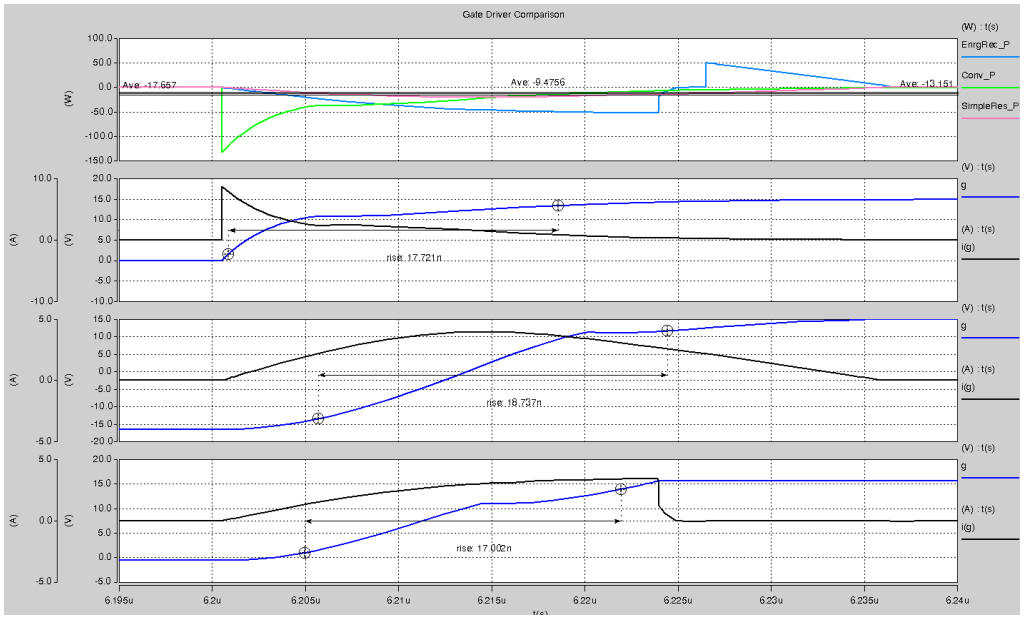


Figure 3.7 Turn-on comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

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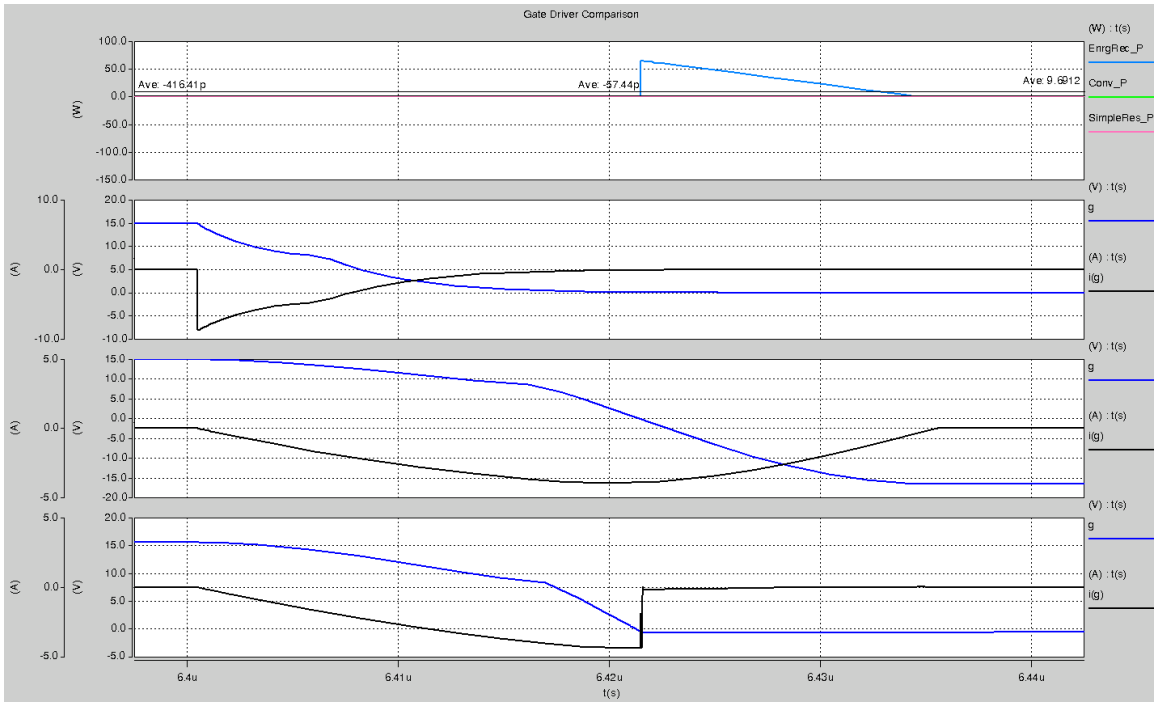


Figure 3.8 Turn-off comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

The waveforms are very similar to the simulation results with the gate represented by a capacitance. The greatest difference in the waveforms is the Miller effect that causes a plateau in the turn-on and –off. The current is the same when compared with the previous simulations except for the energy recovery resonant gate driver. The current decays sharply when the gate voltage reaches its final value. This is due to the current in the gate terminal being reduced to zero and the current in the inductor being redirected to the source through the diode configuration. The top signals show the power consumption. The important characteristic is the average power; this is compared between the three in Table 3.2. The energy recovery resonant gate driver has the least power consumption. This gate driver was also the most stable. The simple resonant gate driver needed multiple cycles to get to the steady-state voltage of the on-voltage because the resonance was used to charge up the gate to 15 V

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while the input voltage was 2 V. These reasons determine the energy recovery resonant gate driver to be selected as the gate driver to be implemented on a printed circuit board (PCB).

Table 3.2 Summary of Power Consumption Comparison

	Turn-on	Turn-off	Total
Conventional (W)	-17.67	0	-17.67
Resonant (W)	-9.48	0	-9.48
Energy Recovery (W)	-13.15	9.69	-3.46

3.3 Stage Three: PCB Implementation of Selected Gate Driver

The energy recovery resonant gate driver is chosen for implementation on a PCB. Parts are chosen to implement the functions needed for the full gate driver. The important things to note are control of the two switches, current rating and the desired turn-on time of the MOSFET. The MAX15018a is used as the control IC for the totem pole because it can handle the two different on-pulses needed to turn on the high-side and low-side NMOSFETs [20]. This IC also implements the bootstrapping function with an external bootstrap capacitor. This capacitor is chosen to be 10 nF because it needs to be large enough to supply the charge to the IRLM2030 gates and small enough to be charged up every time the low-side NMOS is on. This is only the turn-off time of the MOSFET. There are two inductor components on the PCB, one surface mount and the other through hole, so that the inductor can easily be changed to modify the turn-on time. The inductor is first chosen to be 22 nH so the charge time can be calculated as follows.

$$t_{charge\text{-}time}=5*R_{on}*C_B=\frac{\pi\sqrt{LC}}{2}=10\text{ ns} \quad \textbf{(3-5)}$$

$$C_{Bootstrap}=\frac{\pi\sqrt{LC}}{10*R_{on}}\cong 20\text{ nF} \quad \textbf{(3-6)}$$

A 10 nF capacitor is under this limit and will decrease the power consumption and still have enough charge to turn on the high-side MOSFET. The diodes used are ZLLS2000 Schottky diodes [21].

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The final schematic with all of the chosen parts implemented is shown in Figure 3.9 along with the PCB layout in Figure 3.10. Much time was taken to implement very tight traces and a ground well is used to minimize noise and implement ground distribution. Figure 3.11 shows a picture of the populated board in the lab.

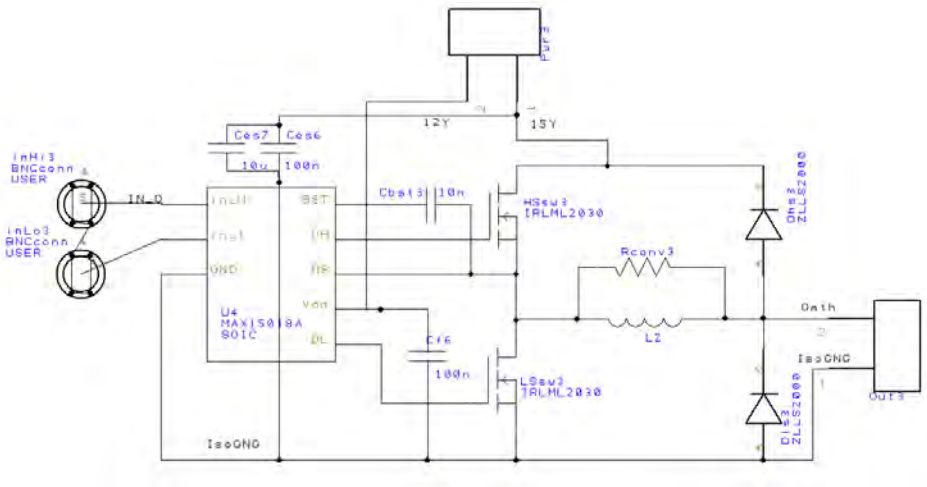


Figure 3.9 Schematic for energy resonant gate driver to be laid out on a PCB

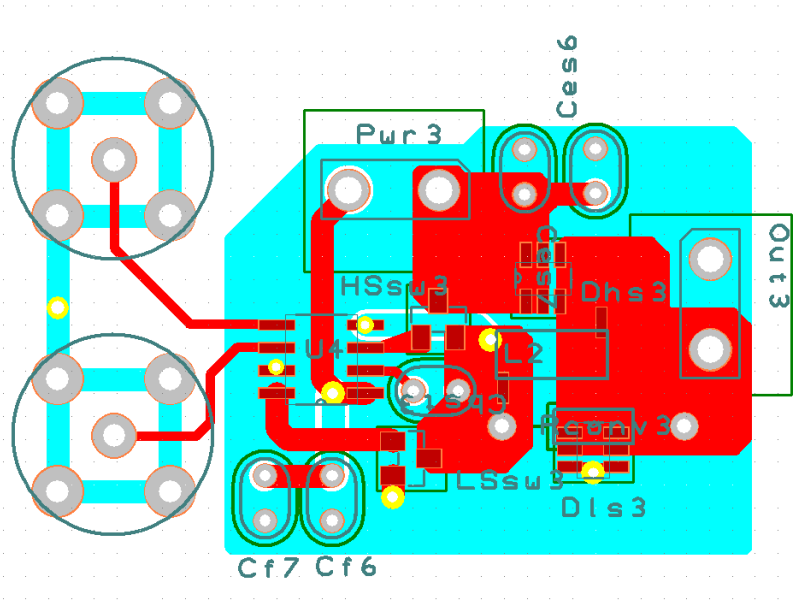


Figure 3.10 PCB layout of energy recovery resonant gate driver

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Figure 3.11 PCB populated in the lab (same orientation of previous schematic and layout pictures)

Figure 3.12 shows the energy recovery gate driver waveforms when it is charging a capacitor representing the gate of a MOSFET. This waveform verifies the operation of the gate driver PCB. The on- and off-pulses are very wide because of the waveform generators minimum pulse width (shown in blue for the on-pulse, and orange for the off-pulse).

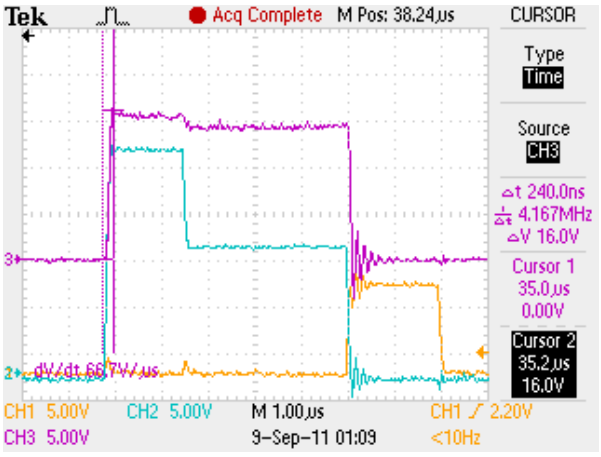


Figure 3.12 100kHz results with a capacitive load, gate (purple), off-pulse (yellow), on-pulse (blue)

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The drop in voltage when the high-side NMOS turns off is due to the unclamped gate voltage charging up stray capacitances in the circuit and loosing charge. The solution for this will not be shown because the University of South Carolina is proposing a new gate driver to solve this problem along with the unclamped gate voltage problem in the collaborative research.

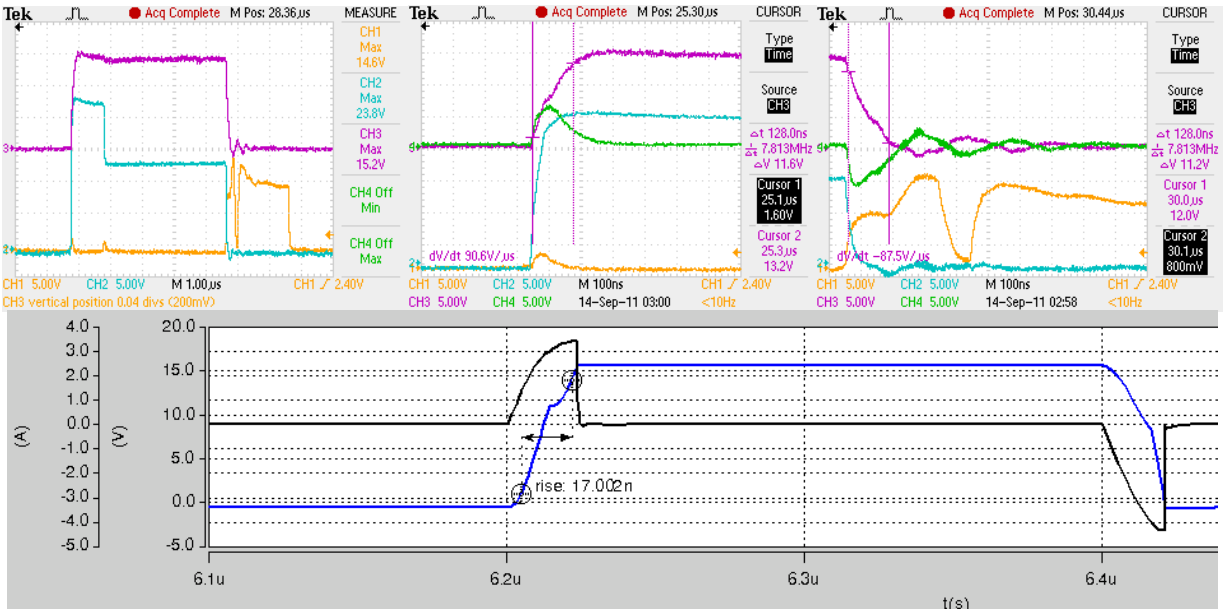


Figure 3.13 100kHz results with SiCMOS load, gate (purple), off-pulse (yellow), on-pulse (blue), gate current (green)

Figure 3.13 compares the waveforms of the simulated gate driver with the PCB gate driver. The waveforms are very similar other than oscillations due to parasitic caused by the tracks and wire connections. Also, the pulse widths for the experimental results are so long that the current during turn-on dissipates before the turn-on time is complete. The current during turn-off matches the simulated value very well. It is not expected to be needed, but the gate driver can switch at 700 kHz with the only limiting factor from going higher is the bootstrap capacitor not being charged fully every off cycle. The gate driver is now fully designed and verified and will be implemented in the final Buck converter system described in Chapter 5.

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4 OPTOCOUPLER CHARACTERIZATION EXPERIMENTS

The Buck converter needs to have isolation between the system variables and the control circuit that will use them to control the overall operation of the converter. This isolation is created via optocouplers and the different functions of the optocoupler need to be used to transmit the different kinds of data between the circuits, i.e. voltage, current, and digital signals. This requires optimizing different aspects of the optocouplers. As shown in the Background chapter there are different topologies to use that will enhance certain functions of the optocoupler. There are two primary roles of the optocoupler, to accurately transmit analog voltage and current signals to the control circuitry and to transmit the on and off control signals to the gate driver. Although the optocoupler device might be the same in each of the two different roles, the topology, or circuitry around the optocoupler device, will be different between the optocoupler used in either role as presented in the Background chapter. The analog transmission topologies will allow the output to copy the input levels, while adding desired gain to the signal. The digital transmission topologies cause the output of the optocoupler to reproduce the digital signal applied to the input.

There is another reason to analyze each topology in this section -- to determine the benchmarks for the optocoupler whether analog or digital. Speed, power consumption, and operation over temperature are the important benchmarks for optocouplers to be compared to the other isolation techniques. These are important to be able to understand how optocouplers could be implemented in other power systems and the characteristics that need to be improved to surpass the comparable solutions. The endeavors of the experiments in this section determine the best topology and optocoupler commercially available to use in the two different roles for the Buck converter and the final benchmark for the optocouplers available today. The experiments in this section will pursue both objectives in the same experiments because the parameters that need to be determined and enhanced

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for the benchmark are the same key parameters that need to be optimized for use in the Buck converter system.

4.1 Introduction of Commercially Available Optocouplers and Defining the Optimum Application Topology

Each topology will be analyzed based on power consumption, propagation delay, temperature, linearity, minimum pulse width (rise and fall time), and optimum biasing. This design section will define the procedures of determining which topologies will be applicable to this research, and understanding the best possible optocoupler circuit for optimizing the aforementioned parameters and determining the final benchmarks for that topology. The first step in finalizing the design and implementation of the optocoupler topologies is to select the basic building block of all the topologies, the optocoupler. They must be analyzed to select the technology that inherently has the best performance with respect to the key parameters, power consumption, propagation delay, temperature, linearity, etc. The optocouplers that do not meet that standard will not even be tested within the topologies that are defined because they will inherently impede the optimization of the important characteristics.

The currently available optocouplers are broken into three different materials, gallium arsenide (GaAs), gallium arsenide phosphorus (GaAsP), and aluminum gallium arsenide (AlGaAs). The material refers to the type of LED and determines the types of properties like optimum wavelength of light, heat dissipation, and mobility. Also, the different materials can each be packaged in three different ways. One way is as an LED and photodiode pair (applied in analog topologies), as an LED and photodiode with transistor (or phototransistor) pair (basic package for digital topologies), or as an LED and photodiode connected to an amplifier stage. These three types of packages were described in the Background chapter and the type of package is important because the correct one must be selected for the correct topology. Typically, each package is available in any of the three materials so the different materials can

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all be implemented in any of the topologies, thus there is the ability to compare between the materials for the same application.

In the graph below the three materials are compared to each other, but the different types of packages have not been broken apart in this comparison. This is due to the fact that propagation delay, power consumption, and isolation voltage are common characteristics that need to be analyzed no matter which output stage is used. If this were a graph comparing CTR then the materials would have to be broken out by package type because the CTR's would be very different. This is due to the different standards for measuring CTR for each output stage.

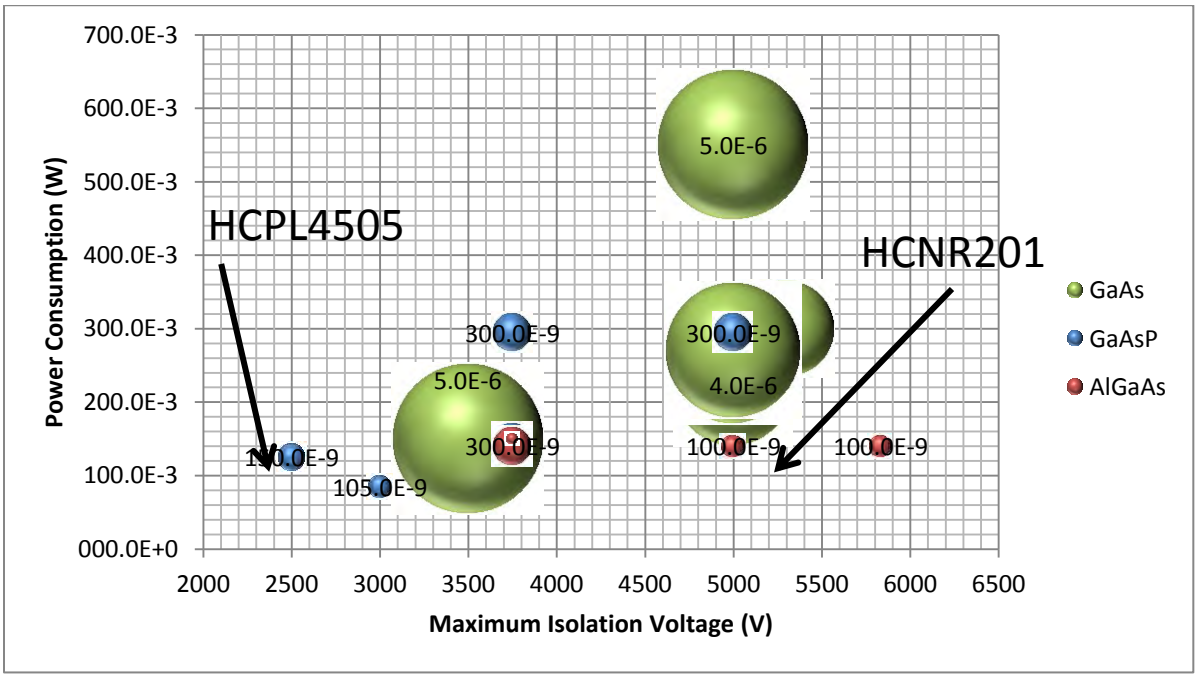


Figure 4.1 Technology versus specification chart comparing power consumption, max isolation voltage (60 s duration), and propagation delay of three different materials

Figure 4.1 compares optocouplers of the three different materials. They are compared on the x- and y-axes by their power consumption and maximum isolation voltage (for 60 s duration). The size of

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the bubble indicates the propagation delay, the bigger the bubble the longer the propagation delay. The GaAs devices are quickly ruled out because the propagation delays are as large as the period of a 200 kHz switching frequency which is not uncommon in many dc-dc converter systems. The GaAsP and AlGaAs devices show minimal propagation delays and lower power consumption. The only difference between the two is the maximum isolation voltage. This is not a large hindrance because the SiC MOSFET switch is only rated at 1.2 kV and all these materials are above that. For a final benchmark for determining the possible applications for these optocouplers this plays a larger role. The AlGaAs would be the best choice in this respect because a device is possible with an isolation voltage larger than 5.5 kV. There are some problems relying solely on this graph to make any design decisions. The data is from the datasheets referenced above and the experiments to find them do not necessarily use the same application circuits that will be used to determine the final benchmarks, and the ranges of values are too large to fully understand the benchmark when just analyzing this data. Also, to complete the two objectives, the topologies from the Background section need to be analyzed to determine the final benchmarks and to select the optimized topology for the Buck converter. These topologies are not analyzed in the datasheets. The next sections define the bench top experiments that are used to analyze the different topologies and the results will determine a final benchmark and the topologies that will be used in the Buck converter system. Table 4.1 lists the part names of the chosen optocouplers, broken out by material and role (digital or analog), that will be used in the following experiments. The digital topologies will implement GaAsP and AlGaAs optocouplers and comparisons between the materials will be made. The analog topologies can only implement the AlGaAs material because the GaAsP optocouplers were not available with a servo-diode packaged with the optocoupler (needed for linear analog transmission). Further explanation of the decisions made for the particular parts are presented in their respective experimental section to follow. All of the results from these experiments will be cataloged and discussed in the following sections.

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Table 4.1 Optocouplers Experimented to Determine Benchmark

Role	Part	Material
Analog (w/servo-diode)	HCNR201	AlGaAs
Digital (LED/BJT)	HCPL4505	GaAsP
Digital (LED/BJT)	HCNW4505	AlGaAs
Digital (LED/Amp)	ACPL-071L	GaAsP
Digital (Amp-LED/Amp)	HCPL7723	AlGaAs

4.2 Benchmark Experiments for Analog Application Topologies

This section defines experiments and presents the results for the analog transmission topologies. The Background Chapter shows the different topologies used to transmit analog. Experiments are designed with the objective of collecting raw data to understand the key parameters of propagation delay, biasing point, accuracy, power consumption, and temperature for each topology and optocoupler material. A benchmark will be determined based on these results and in the Implementation of Optocouplers in the Buck Converter Chapter the results will be used to determine the topology used in the Buck converter. Only two analog transmission topologies out of the three presented in the Background chapter were chosen for experimentation. The topology shown in Figure 4.2 is not experimented with any further because it has the same working principle of the other feedback analog topology and it would be repetitious to investigate this topology. Also, when implemented on a bread board this topology not only consumed more power with equivalent components, it adds more complexity because the photodiodes are connected to the power supply and the use of an uncompensated voltage follower op amp. The other topology improves upon these weak points by eliminating the output stage's photodiode connection to the supply and a stable feedback network for the output op amp.

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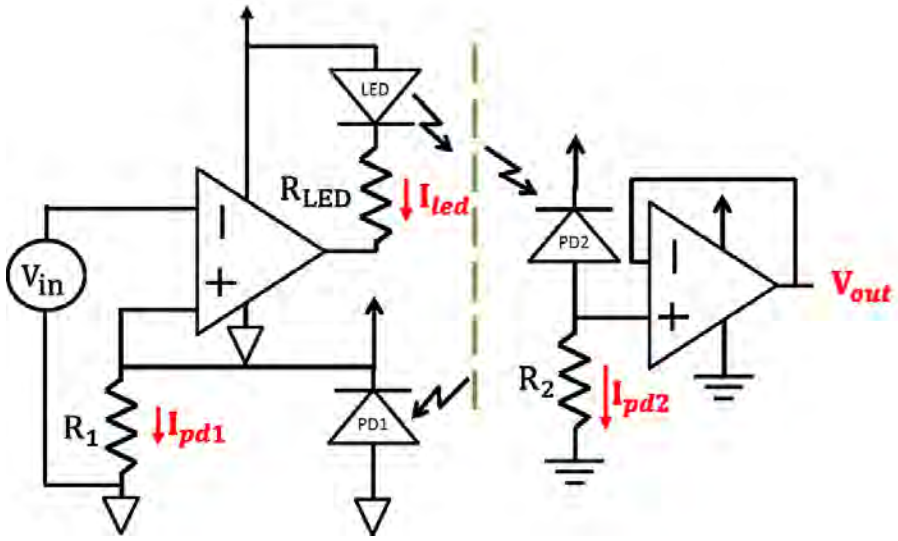


Figure 4.2 Second analog feedback transmission topology not tested further [7]

The remaining analog topologies analyzed are the feedback topology that uses a servo-diode to linearize the transfer function and the open-loop topology that does not need an isolated supply for the input stage. These analog optocoupler topologies each undergo three experiments. The first experiment is defined to understand how biasing affects the circuit. The following section will discuss the test setup and procedure for the experiment. In this experiment a dc voltage is applied at the input to bias the circuit at one operating point and then the response of the output and various other system variables are recorded to determine the key characteristics of the circuit. Then the dc operating point is swept between a minimum and maximum allowable operation range. In the next experiment the biasing results are used to create a sinusoidal waveform, which is applied to the input, with a peak-to-peak voltage of all the reasonable biasing points found in the first test. The final experiment sweeps the temperature of the optocoupler in the same test setup as the second experiment. A conclusion is drawn for the final benchmark for the analog transmission scheme in the Conclusions Chapter using the results from these experiments and Chapter 5 determines the optimal topology based on these results.

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Now that the experiments and objectives have been presented the specific device selections need to be understood. The analog topologies only need the optocoupler (packaged with a servo-diode) and an op amp with some external, tunable resistors. The two different topologies will utilize equivalent devices so that comparisons can be drawn. For the optocoupler selection there are two to choose from: Avago's HCNR201 and Vishay's IL300. The HCNR201 is selected for all analog transmission topologies because it has the best raw propagation delay, linear CTR, and temperature operation as seen in the datasheet compared to any other analog optocoupler [12]. The IL300 was another analog optocoupler that is of similar quality of the HCNR201, but is not analyzed because the switching characteristics are a factor of 10 less than the HCNR201 [7]. Table 4.2 presents the data that determined this decision.

Table 4.2 Comparison of IL300 and HCNR201

	HCNR201 (AlGaAs)	**IL300 (AlGaAs)**
Input Current	1 – 20 mA	1 – 60 mA
Peak Input Current	35 mA	250 mA
LED Forward Voltage I_F=10 mA	1.3 – 1.85 V	1.25 – 1.5 V
Max Reverse Voltage	15 V	50 V
Transfer Gain K_3	0.95 – 1.05	0.75 – 1.25
CTR	0.36 – 0.72%	0.4 – 0.8%
PD Leakage Current	0.5 – 25 nA	1 – 25 nA
Bandwidth	1.5 MHz	200 kHz
Withstand Voltage	5000rms	5300rms

The op amp used is the MAX4450 [22]. This op amp was selected based on the criteria to have a maximum output slew rate an order of magnitude larger than the speed of the optocoupler. Also a single supply op amp was chosen. A final note is that the experiments to determine the benchmark presented below is for the design with circuit parameters and component selections shown above. They were chosen to optimize the circuit as much as possible. For example, choosing an op amp with a limited

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slew rate would limit the slew rate of the overall topology to the value of the op amp and thus skew the gain of the voltage transfer. The final benchmark that is found through the experiments below is a representation of the advantages and limitations of optocouplers. For any design implementing these optocoupler topologies this benchmark should be considered as the general baseline performance in which these devices should operate when optimized for speed and linearity. Other topologies that optimize other key parameters will have different benchmarks.

4.2.1 Feedback Analog Transmission Topology Bias Experiment Setup

The first experiment, the biasing test, is performed on the topology shown in Figure 4.3. As stated and justified earlier, the HCNR201 and MAX4450 are the optocoupler and op amp, respectively. Figure 4.3 also shows the test setup that is used to measure the key system variables. It can be seen that the system variables measured are V_{in}, V_{out}, I_{pd1}, I_{pd2}, I_{LED}, I_{src1}, and I_{src2}. There are also important calculated parameters that are measured to determine the impact biasing has on the performance of this analog transmission topology. The propagation delay, t_{prop}, is measured from the positive edge of the input to the positive edge of the output. The values of I_{src1} and I_{src2} are used to measure the power consumption on the input and output, respectively. The HCRN201 is biased when the photodiode on the input has tens of micro-amps flowing through it. The input resistor is set to 100 kΩ while the input voltage is swept from 0.5 to 6 V which corresponds to 0.5 µA to 60 µA through the photodiode. The value of R_2 is selected to be 100 kΩ to attain unity gain. The CTR is calculated ($\frac{I_{pd1}}{I_{led}}$) along with the gain ($\frac{V_{out}}{V_{in}}$). If the gain is not unity, then the K_3 factor discussed in the Background chapter is not unity, and would denote there is an unequal amount of light impinging on PD1 and PD2. The final calculated values are the rise and fall times of the output voltage. The input is applied ten times via a pulse at 50 kHz with a positive width of 10 µs to bias the circuit with a dc voltage. There are multiple cycles to make sure the topology is operating in steady-state. This is done at each input voltage level from 0.5 V to 6 V. The

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response of the circuit is measured and calculated to determine how the PD1 current affects the performance of the circuit. This experiment is completed for three iterations, one for each R_{LED} value; 110 Ω, 310 Ω, and 510 Ω. This does not bias the LED current differently since the PD1 current sets the LED current, but this does show the impact of the voltage drop across R_{LED} on the LED response.

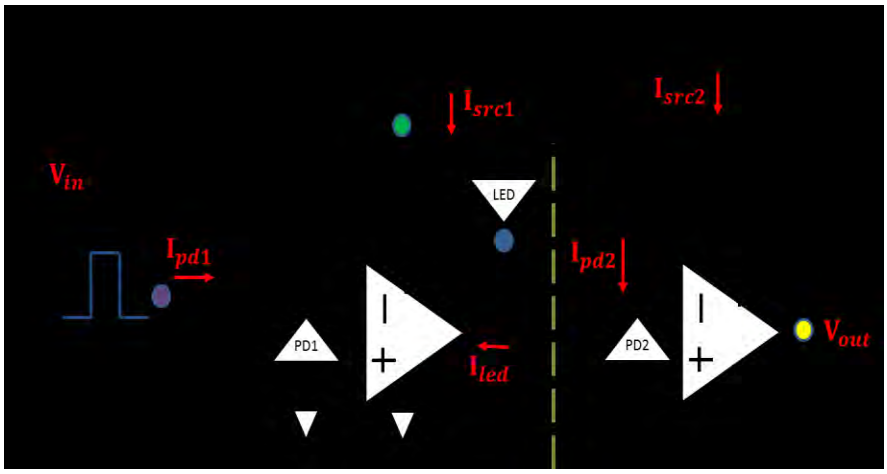


Figure 4.3 Biasing test setup schematic for HCNR201 feedback analog topology (colored nodes show the probe placement (further discussed in following section)

4.2.1.1 Feedback Topology Bias Experimental Results

Before the results can be presented an important comment needs to be made about how the measurements are taken with the oscilloscope probes; circuit placement has an effect on the measurement. The measuring scheme for this experiment and all following analog transmission experiments had to be altered so that the probe capacitance would not skew the results. Although the scope allows for floating measurements, some floating measurements could not be taken because of the 16 pF capacitance of the probe. When the probe is placed across the feedback path of the op amp, which is used for the I_{pd2} measurements, a pole is introduced at 99 kHz $\left(=\frac{1}{2\pi*16p*100k}\right)$. This pole decreases the response time of the output voltage by more than 750%. This difference is shown in

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Figure 4.4. Because the probe cannot be used, I_{pd1} and I_{pd2} had to be calculated from the measured values of V_{in} and V_{out} as can be done via the transfer function. This has little impact on the accuracy of the measurements because the calculation only neglects the 10 to 20 mV across the photodiodes during operation and the 1 to 5 µA op amp input current. This introduces a ±4% error for a 500 mV signal which decreases quickly to 1% as the magnitude increases.

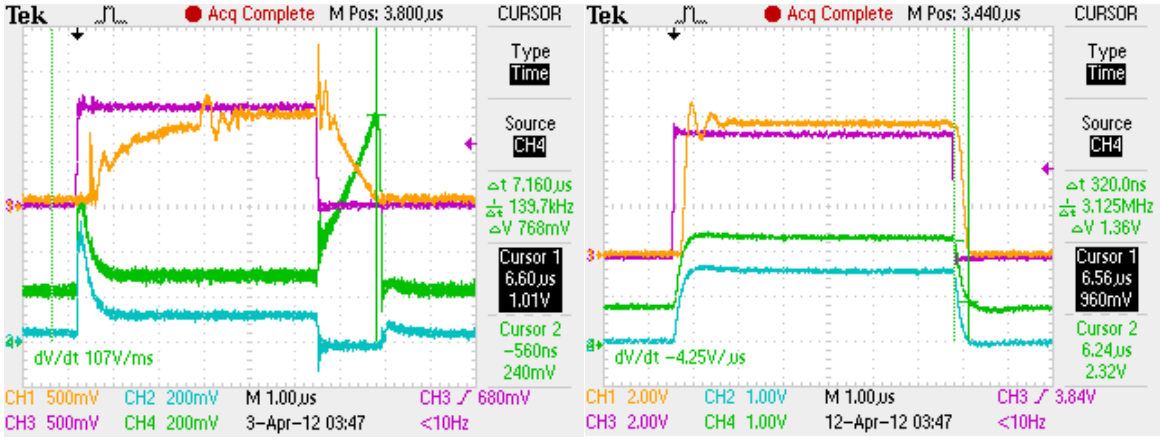


Figure 4.4 Old measurements (left) , new measurements (right); input (purple), output (yellow), LED current (blue), source current (green)

While there is no input applied the LED branch draws 0.7 mA and the op amp draws 6.5 mA for all values of R_{LED}. A figure of merit is created to show the trend of the key parameters as the LED resistance is changed. The trends are created by averaging each respective parameter across all biasing points. These values are only showing trends to introduce the circuit's characteristics. In-depth graphs for each biasing point will be shown in the following sections. Table 4.3 shows the trends of the propagation delay and power consumption as the LED resistance is increased.

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Table 4.3 Power Consumption and Propagation Delay Trend as R_{LED} Increases

R_{LED}(Ω)	110	310	510
$t_{prop,avg}$ (ns)	225	390	550
$P_{input,avg}$(mW)	446	258	200

The trend is that for increasing value of R_{LED} the propagation delay decreases while the power consumption also decreases, when the LED resistance is increased 450% (from 110 Ω to 510 Ω), the propagation delay increases by 250% and the power decreases by 220%. The mechanism for the delay in optocouplers is not well understood. The delay is seen to have a dependence on LED resistor values and as the value increases the delay increases. This could be due to the larger voltage transition the output of the op amp must swing through. Also, the input power is based on the forward current of the LED, and as this increases, the propagation delay decreases. But these are simple explanations for a complex phenomenon, as seen in [23], the delay can also be a minimum at the middle of the range of LED currents for other optocoupler devices. Further research in this area, to determine the mechanism of the propagation delay, is required. What is understood is that the bandwidth of the circuit is determined by the propagation delay and desired linearity as corroborated in [23]. Another possible reason for the changing propagation delay in this circuit could be, although the output gain stage is not changed, the input stage's feedback gain and bandwidth is determined by the value of R_{LED} and I_{LED}, when these increase the bandwidth decreases. The important note is that the trend is predictable and the mechanism does not need to be fully understood to conclude a benchmark for the propagation delay.

The next sets of figures are broken out for each value of R_{LED} that the experiment was conducted. The graphs show the different key parameters compared between the ranges of the value of R_{LED}. The propagation delay versus power consumption is defined by normalizing the power consumption by subtracting the $I_{LED}^2 * R_{LED}$ from the total input stage power consumption, which

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compensates for the LED resistance component of the measured total power consumption. This is done to look at the power consumed by the op amp, LED, and filter capacitor, since these are the components that will increase or decrease propagation delay. But it is noted that the overall power consumption of the input stage does increase as the photodiode current increases, but not as the R_{LED} decreases, because as R_{LED} increases the current decreases enough to keep the overall power consumption equal even though the op amp is consuming more power.

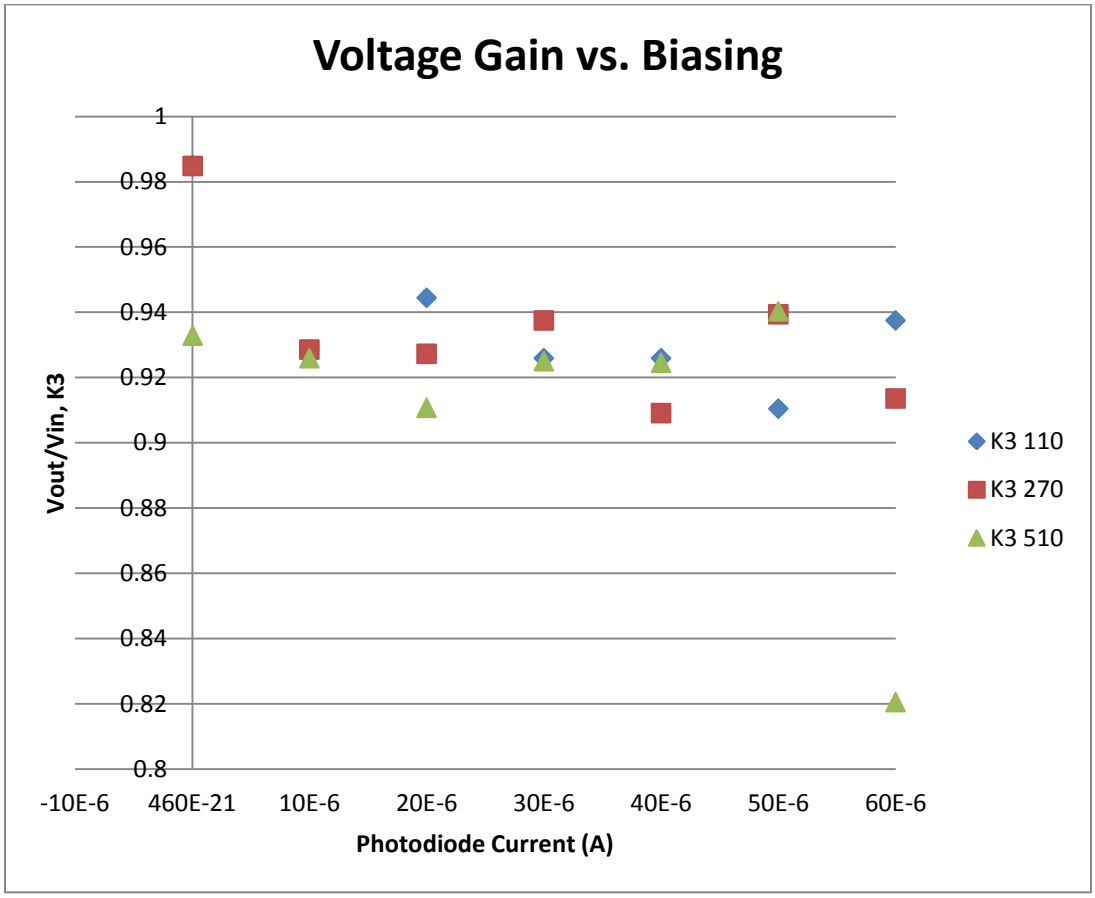


Figure 4.5 Voltage gain versus biasing for different values of R_{LED}

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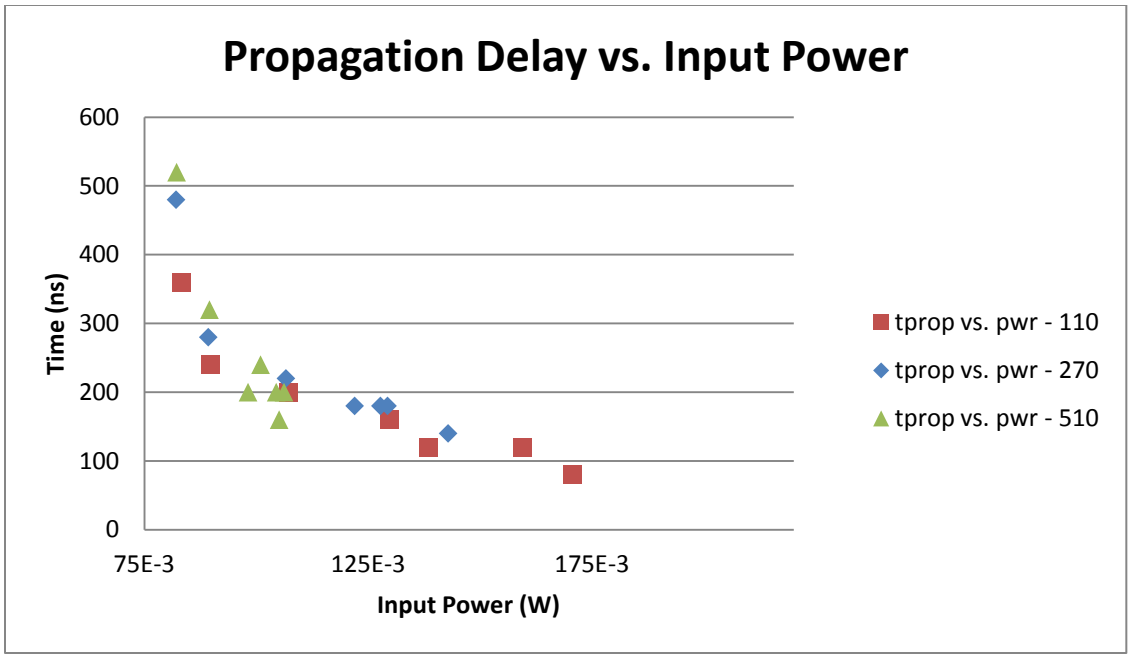


Figure 4.6 Propagation delay versus input power for different values of R_{LED}

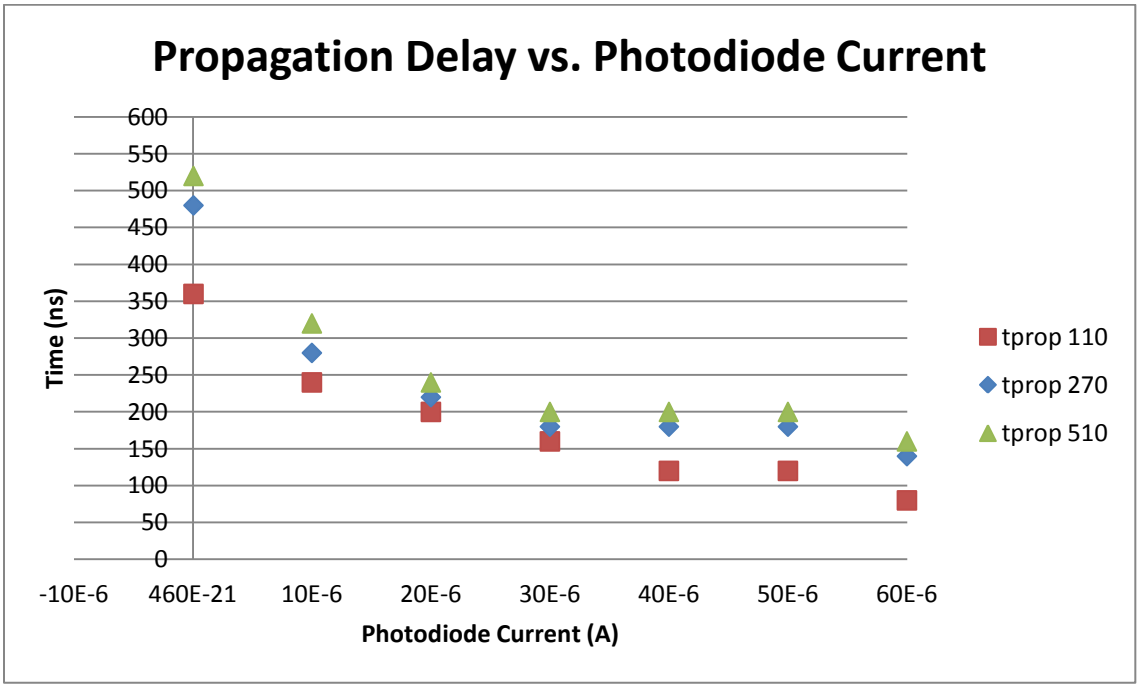


Figure 4.7 Propagation delay versus photodiode current for different values of R_{LED}

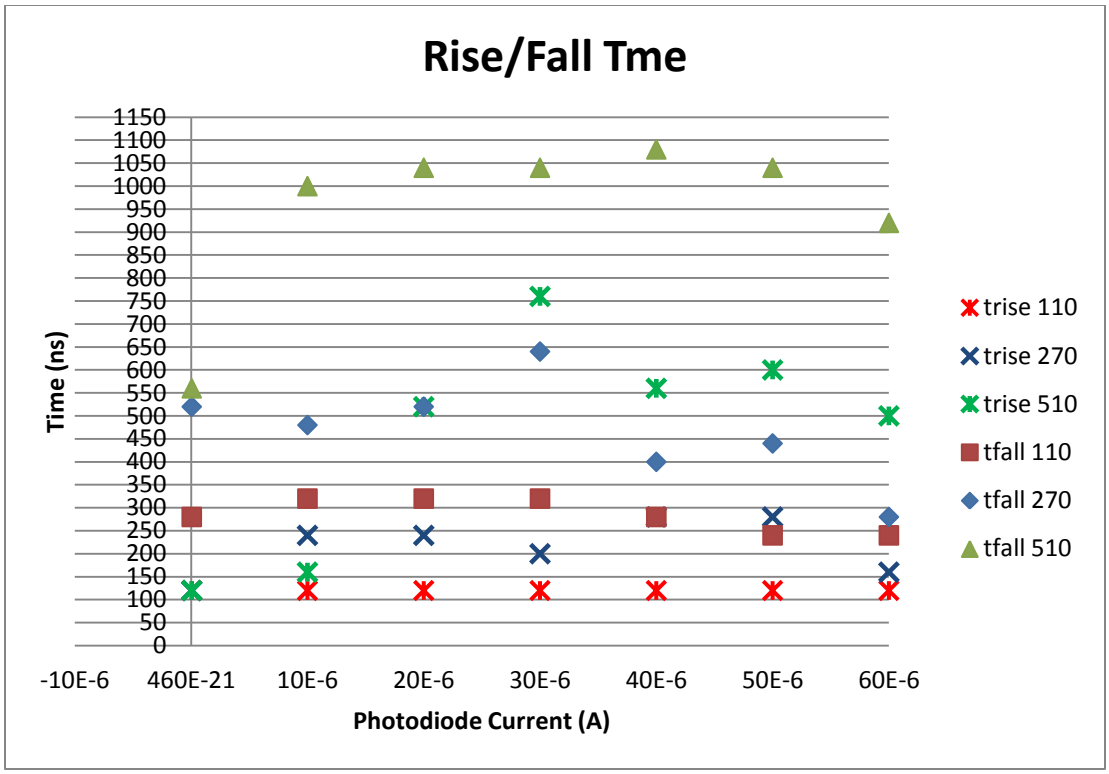


Figure 4.8 Rise and fall times versus photodiode currents for different values of R_{LED}

These figures show the effect of R_{LED} on the response of the circuit. Also, it is seen that as the input photodiode current increases from 0.5 µA to 60 µA the circuit parameters respond in the following ways. The propagation delay decreases by 66% while rise and fall time and voltage gain stay constant. The decrease in the propagation delay cannot be improved further by changing the biasing because 60 µA is the absolute maximum current. The range where the voltage gain is constant is important for the next experiment, the linearity experiment. The voltage gain needs to be constant across a range of biasing so that an input voltage within that range can be expected to cause a linear response in the output. This is shown more in-depth in the next section. The propagation delay has already been discussed, and the affect of the value of R_{LED} is shown more completely in Figure 4.6 and 4.7. Also, the value of R_{LED} impacts the rise and fall time of the output response; an 80% reduction in resistance causes and 80% and 60% decrease in the rise and fall time, respectively. This information is important to

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determine the final benchmark, and to determine which topology will be implemented in the Buck converter and how the different values are selected to obtain the optimum performance of the analog transmission circuitry. The next section applies a sinusoidal input to measure the linearity and propagation delay of this feedback analog transmission optocoupler topology.

4.2.2 Feedback Analog Transmission Topology Linearity and Temperature Experimental Setup

Now that the different biasing points are understood independently, a sinusoidal input is applied and the temperature scaled to see what those changes do to the parameters analyzed in the previous experiment. This experiment will completely determine the benchmark for this topology, because it shows the full operation of the circuit while the previous experiment only discovered the correct operating point. The values of R_1 and R_2 are set to 100 kΩ to create a unity gain at nominal operation. The experiment is repeated for the value of the LED resistor from 110 Ω to 270 Ω, and finally 510 Ω, like the previous experiment. The temperature sweep is applied over all values of R_{LED} to determine the best operating point in terms of propagation delay, linearity, and rise and fall times. In each of these experiments the input will be an 80 kHz sinusoidal waveform with 0 V minimum and 6.5 V maximum. Each of these tests will be repeated at 25 °C, 50 °C, and 70 °C. This range is chosen because it stays well below the maximum temperature of 85 °C. The output voltage and LED current are measured while the propagation delay, voltage gain, and K_3 term are calculated via the transfer function. Because CTR is not in the transfer function for this topology the K_3 term is the only thing that will affect the gain during temperature operation. Figure 4.9 shows the experimental setup for the linearity and temperature experiment. The optocoupler is isolated and its temperature is increased. This procedure is included in the experiment so that the effect of temperature on the propagation delay, voltage gain, and K_3 parameter is only caused by the response of the optocoupler to the temperature increase. The

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auxiliary circuit is removed from the equation so that the results are only dependent on the optocoupler.

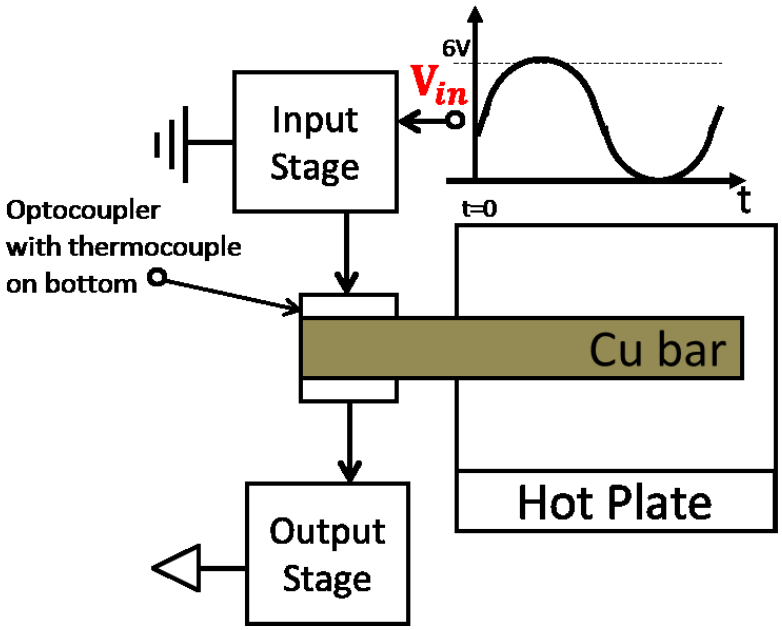


Figure 4.9 Temperature and linearity experimental setup for feedback topology, the probe measurements are the same while the input waveform changes as seen

4.2.2.1 Feedback Topology Linearity Experimental Results

This section shows the linearity and temperature experimental results for the analog transmission feedback topology described above. Figure 4.10 shows the input voltage waveform and the output voltage and LED current waveform measured in this experiment.

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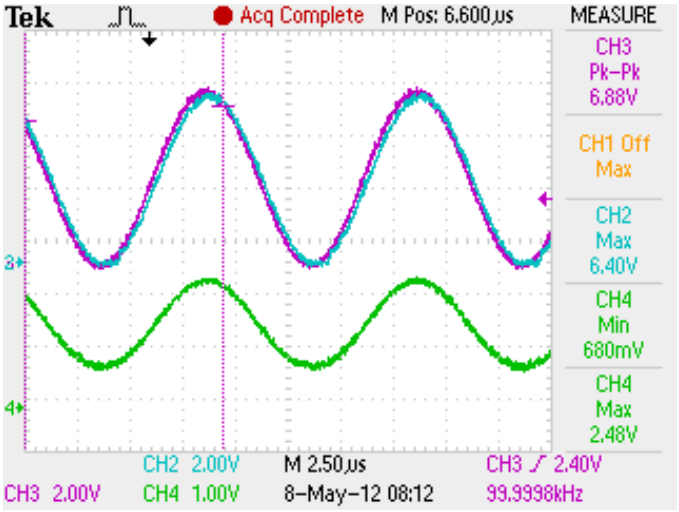


Figure 4.10 Waveform of test, R_{LED} 110 Ω at 70 °C input (purple), output (blue), I_{LED} (green)

The waveforms are extracted to Excel to calculate the propagation delay, voltage gain, and K_3. The first step is to define the propagation delay for each value of the LED resistance at every temperature. Table 4.4 shows these results.

Table 4.4 Propagation Delay Over Temperature for Different R_{LED}'s

	t_{prop}(ns)		
	25°C	**50°C**	**70°C**
110Ω	100	110	180
270Ω	200	230	300
510Ω	300	400	520

While the optocoupler's temperature increases to 70 °C the LED resistance is increased and the propagation delay increases with the same trend as the previous experiment. The temperature causes, on average, a 50% increase in the propagation delay. The next step is to analyze the voltage gain over the entire input range to determine the linearity of this design at various LED resistances. The nominal voltage gain should be unity because both R_1 and R_2 are 100 kΩ.

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To analyze the voltage gain ($\frac{V_{out}}{V_{in}}$), an important comment needs to be made. The output is shifted by the propagation delay. This affects the voltage gain measurements because if the input voltage and output voltage are compared at one moment in time an input voltage at t_1 would be compared to an output voltage corresponding to the input voltage at t_1-t_{prop}. To get an accurate value for the voltage gain the output waveform data is shifted by a time step equal to the propagation delay. Figure 4.11 through Figure 4.13 show the voltage gain for each temperature set versus the input voltage plotted on the x-axis. At each temperature each value of R_{LED} is plotted to show the effect of the LED resistance over temperature.

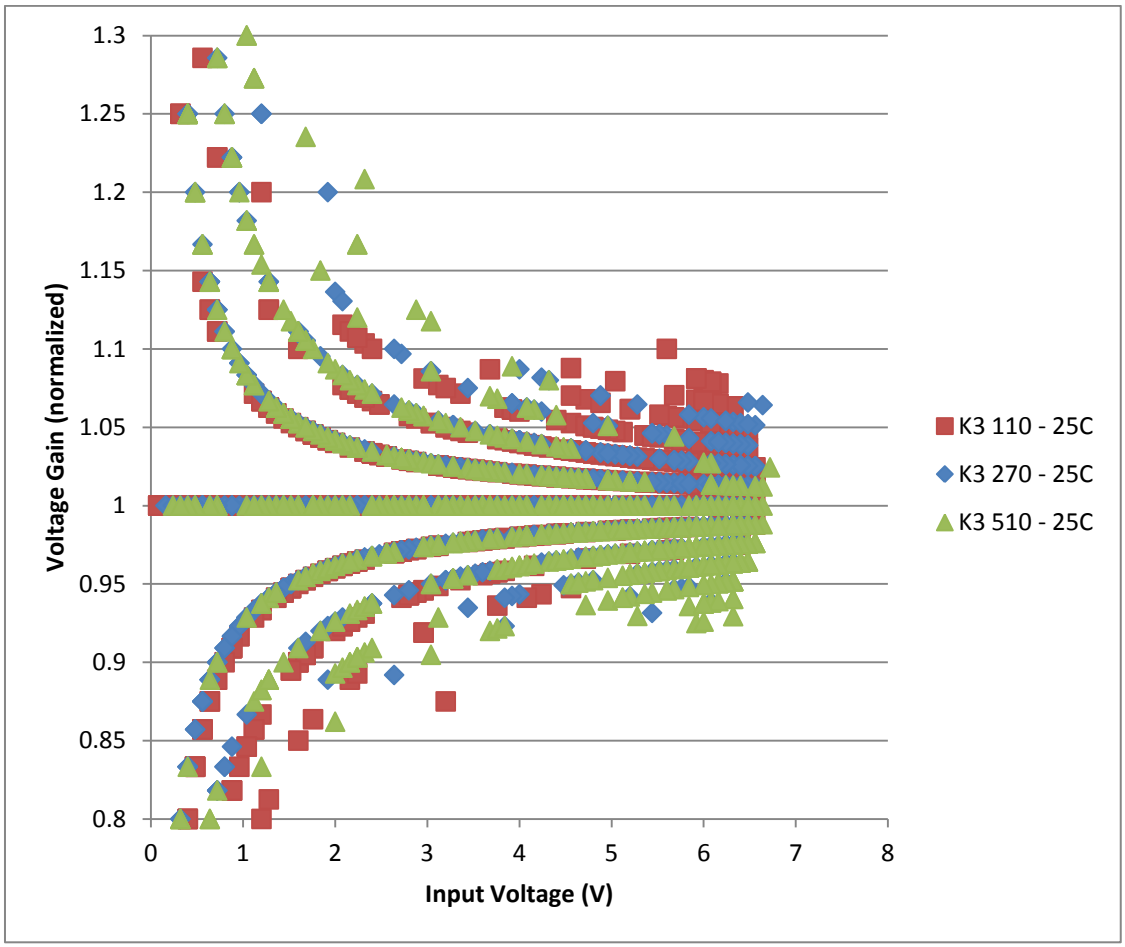


Figure 4.11 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 25 °C

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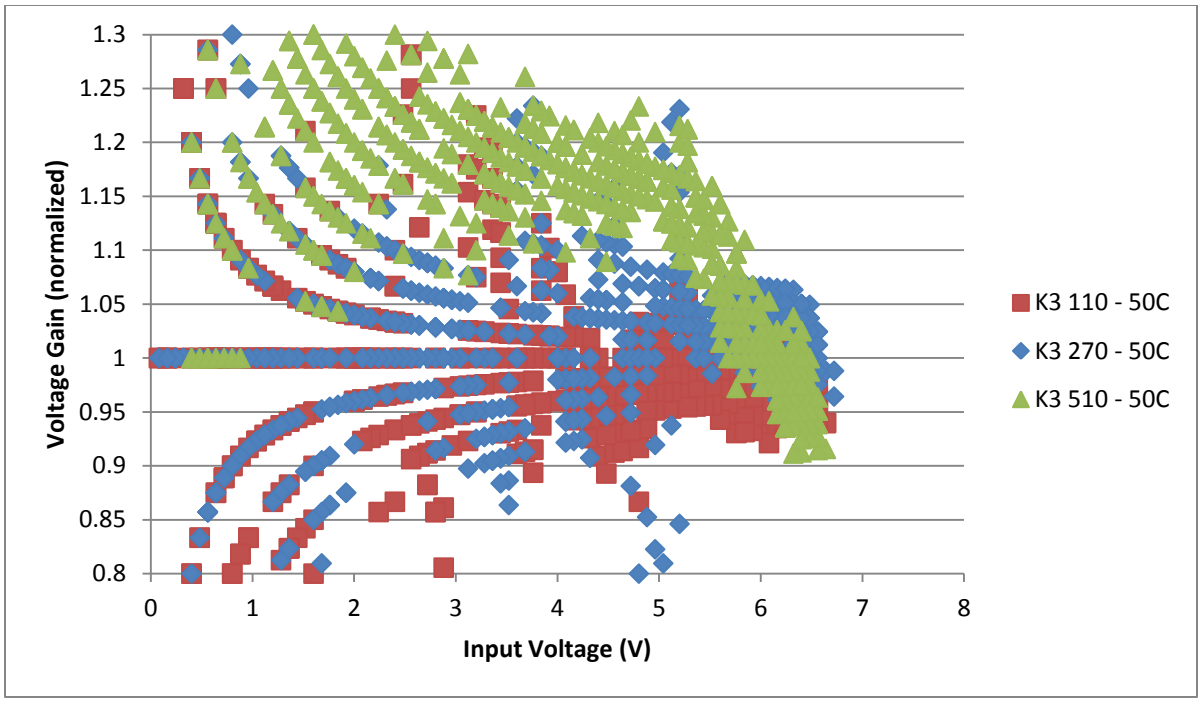


Figure 4.12 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 50 °C

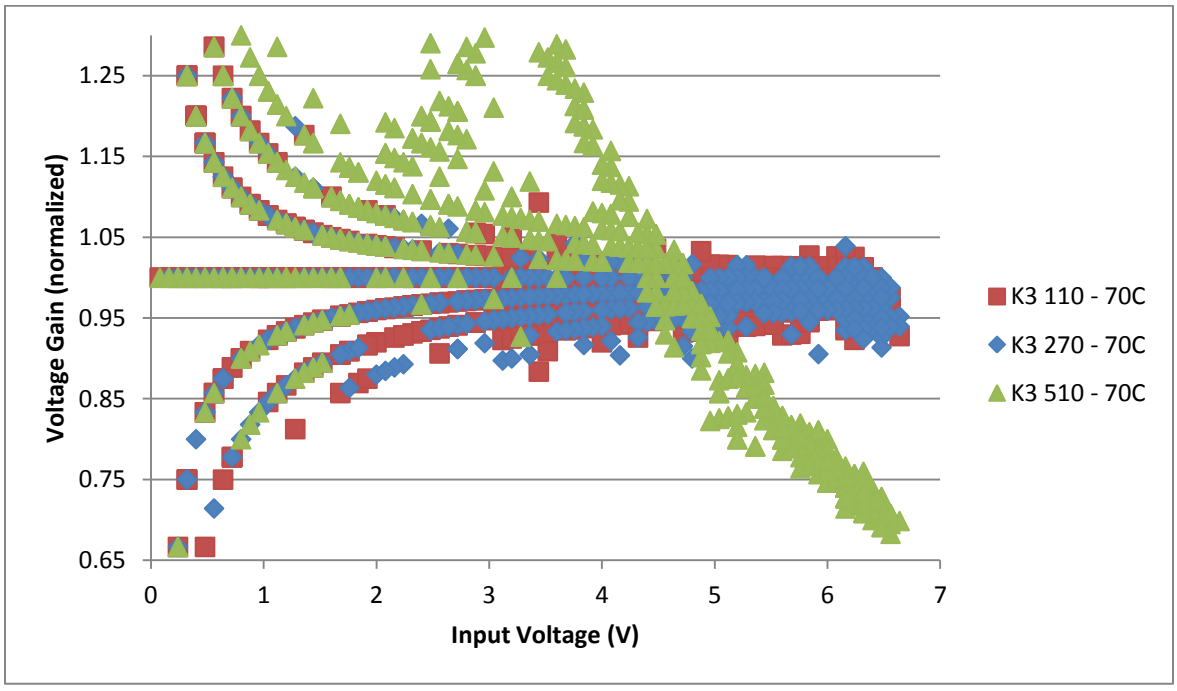


Figure 4.13 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 70 °C

In this breakout the difference the LED resistance makes can truly be seen by the change in the voltage gain versus the input voltage for each temperature and LED resistance. A perfect optocoupler system would have a straight line at 1 $\frac{V}{V}$ for every temperature. This experiment shows that the voltage gain is not constant across temperatures, LED resistances, and input voltage. The voltage gain starts to spread out from unity as the input voltage decreases below 2 V for 25 °C and below 4 V for 70 °C (excluding the 510 Ω case for now). This non-linear spreading can be avoided by operating above the input voltage thresholds. In this region the voltage gain kept within ±5% of unity.

A note about these graphs on the number of data points needs to be made. The Excel manipulation allowed for every data point taken by the oscilloscope to be used in the calculations. Over two cycles of an 80 kHz signal (25 µs) allowed for over two thousand data points to be used in the calculations. The artifacts in the graphs are due to small voltage variations in the waveforms being measured. All of the data points are left in because it shows two things. First, the trend is shown very well with the mass of data points on the graph, and any shift from the temperature and LED resistance in the response can be seen very well. Second, the data points show that even as the input voltage is decreased below the point of unity gain, there are still data points that show unity gain.

Another note is on the 510 Ω R_{LED} results. The sharp decrease in the voltage gain is due to the large voltage drop over the LED resistance causing the output voltage to clip because it increases above the supply rail. The voltage drop is large because the LED current is created independent of the LED resistance (by the current flowing through the photodiode), and the voltage drop caused by the LED current adds with the LED forward voltage and causes the clipping affect. This shows up as a decrease in the voltage gain at 5 V input for the 50 °C and 4 V for the 70 °C data. The reason why this phenomenon is present at decreasing voltages as temperature increases is explained later.

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Figure 4.14 through Figure 4.16 show the same results as before but with the voltage gain versus input voltage broken out for each set of LED resistances compared with the same resistances as temperature increases.

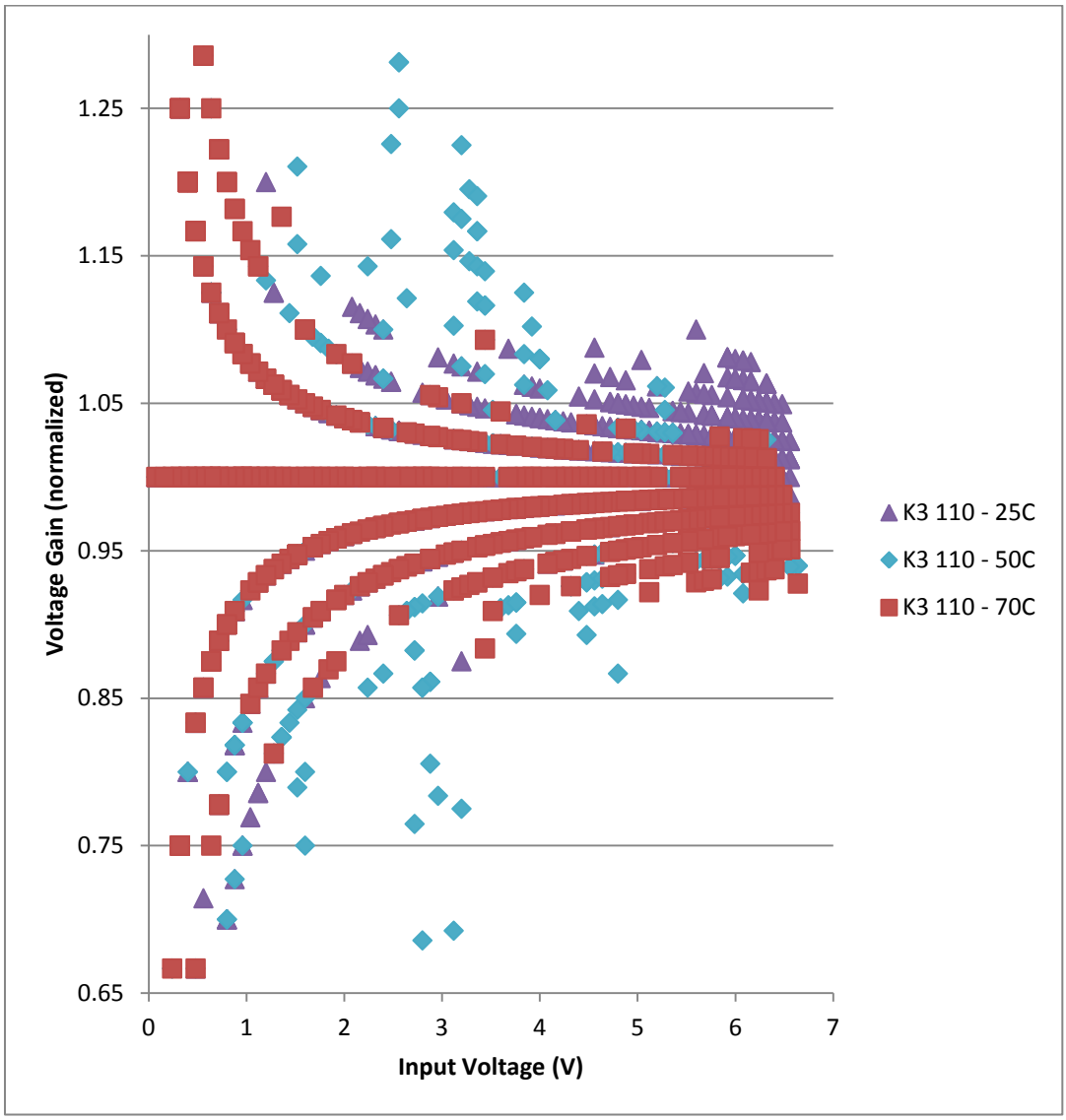


Figure 4.14 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 110 Ω

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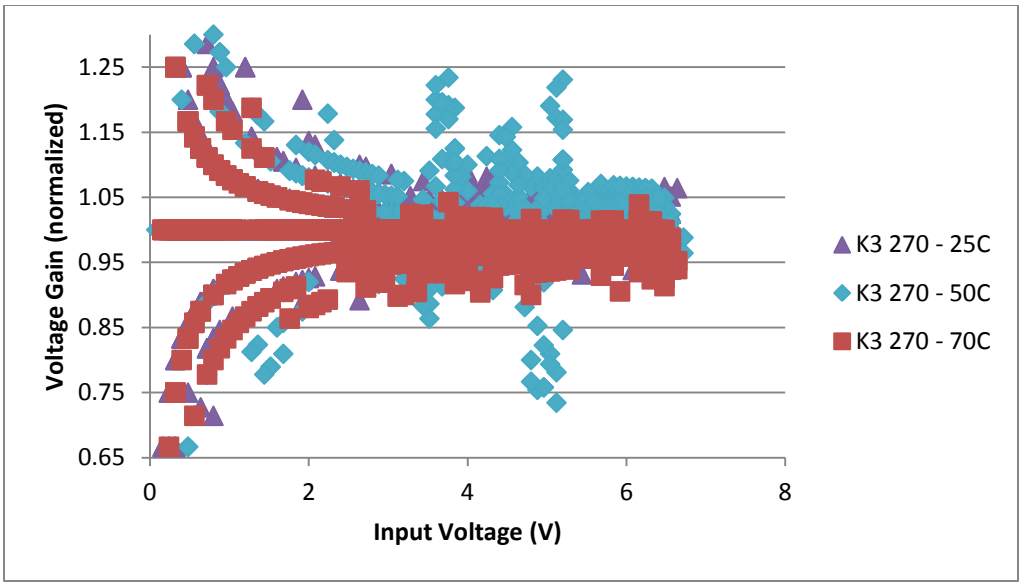


Figure 4.15 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 270 Ω

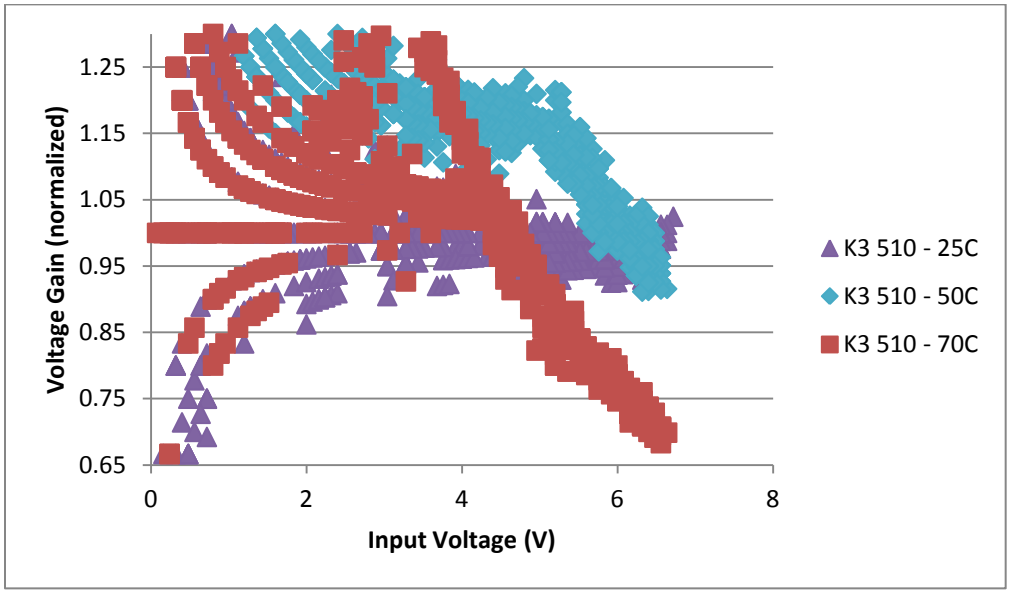


Figure 4.16 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 510 Ω

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The 110 Ω and 270 Ω graph are relatively stable as temperature increases. The average gain should be unity gain when the circuit stabilizes above 2 V input but the average gain decreases from unity as temperature increases. This is consistent with the datasheet of the HCNR201, where the K3 decreases with temperature, which would cause a decrease in the voltage gain [12]. There is an approximate 6% decrease in overall voltage gain with temperature. In the 510 Ω graph the temperature affects are more prevalent. The cause of this change can be better seen in the LED current which is formed by the input voltage causing a current to flow in the photodiode. Because the LED needs at least 1.55 V when it is correctly biased the voltage across R_{LED} has to be less than V_{DD}-V_{LED}. In the 510 Ω case the voltage gets above this whenever 16.5 mA flows through the LED. This is the reason for the voltage gain decreasing as the input voltage increases above this threshold. As the temperature increases the LED transfers less energy to the servo diode (6% decrease in CTR over temperature), this means that at the same input voltage for the 70 °C operation there is more current flowing through the diode which causes the voltage across R_{LED} to be greater than V_{DD}-V_{LED} sooner. This causes the decrease in voltage gain much sooner as the temperature increases.

These results will be compared with the voltage gain from the open-loop analog transmission topology seen in the next section in the Conclusions Chapter and it will describe the benchmark for this analog transmission topology. Next, the benchmark experimental results for the analog transmission topology without feedback are discussed.

4.2.3 Open-Loop Analog Transmission Topology Bias Experimental Setup

The open-loop topology is analyzed with experiments in the same way as the previous optocoupler topology. The first, a biasing experiment, determines the output's response to different biasing points of the input LED with the test setup in Figure 4.17 using the MAX4450 and HCNR201 as described previously. The input is a 4 V pulse at 30 kHz with a 50% duty cycle. The value of R_2 is set to

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100 kΩ and R_{LED} is swept from 8 kΩ to 110 Ω so that the LED current is biased from 0.5 mA to 18 mA, which covers the entire safe operating range [14]. Data is taken when the topology reaches a steady-state. The values of V_{in}, V_{out}, I_{pd2}, I_{LED}, and I_{src2} are measured while the power consumption, the propagation delay from the input positive edge to the output positive edge, the CTR, and the voltage gain are calculated. The biasing experiment is repeated with R_{LED} set to 510 Ω while the value of R_2 is swept from 22 kΩ to 200 Ω. The propagation delay and the voltage gain is measured and calculated, respectively. This second phase of the experiment is an important step because it will determine if the propagation delay of the op amp is affecting the overall propagation delay for this analog transmission topology. If the propagation delay changes while R_2 changes then the op amp is adding to the overall delay. The following section presents the results from the described experiments.

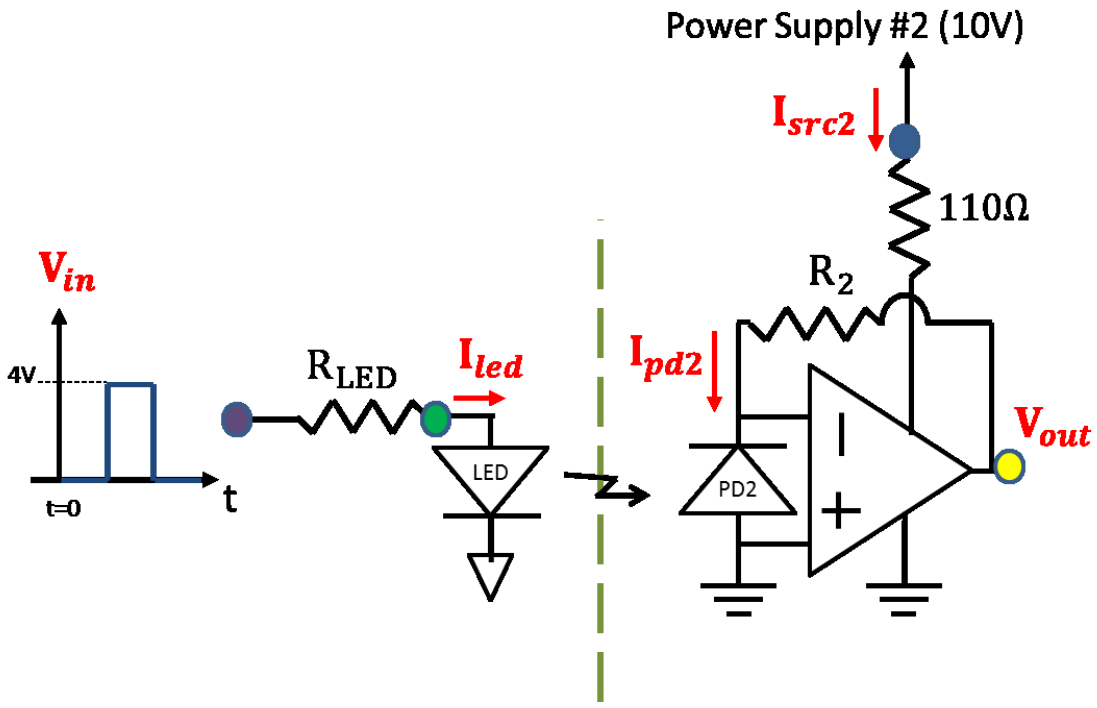


Figure 4.17 Biasing test setup schematic for HCNR201 open-loop analog topology showing the probe placements (the input LED current is measured using the MATH command)

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4.2.3.1 Open-Loop Topology Bias Experimental Results

The result of the basing experiment of the open-loop analog transmission topology is shown below. The waveforms in Figure 4.18 show the type of results that were obtained from this experiment. The yellow signal is the input, purple is the output, green is the output stage power consumption, and the red is the input LED current. To measure this topology without skewing the results with the probe capacitance, the output photodiode current is calculated with the output voltage instead of being directly measured like the experimental measurements for the previous topology.

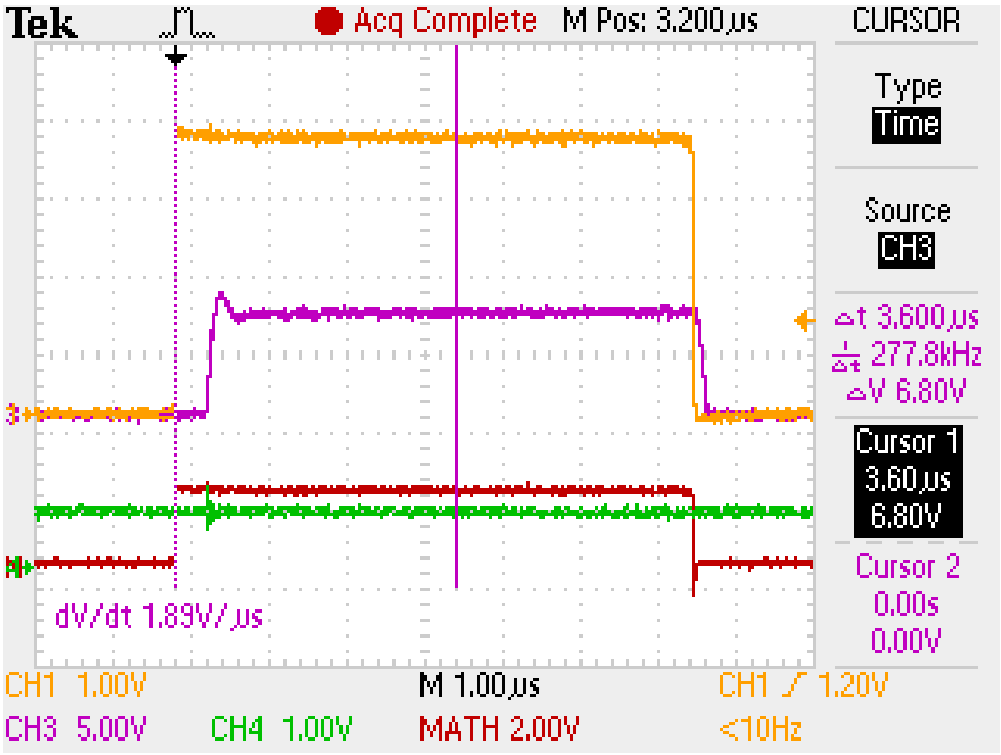


Figure 4.18 Biasing test waveforms for open-loop analog transmission topology, yellow (input), output (purple), output supply current (green), LED current (red)

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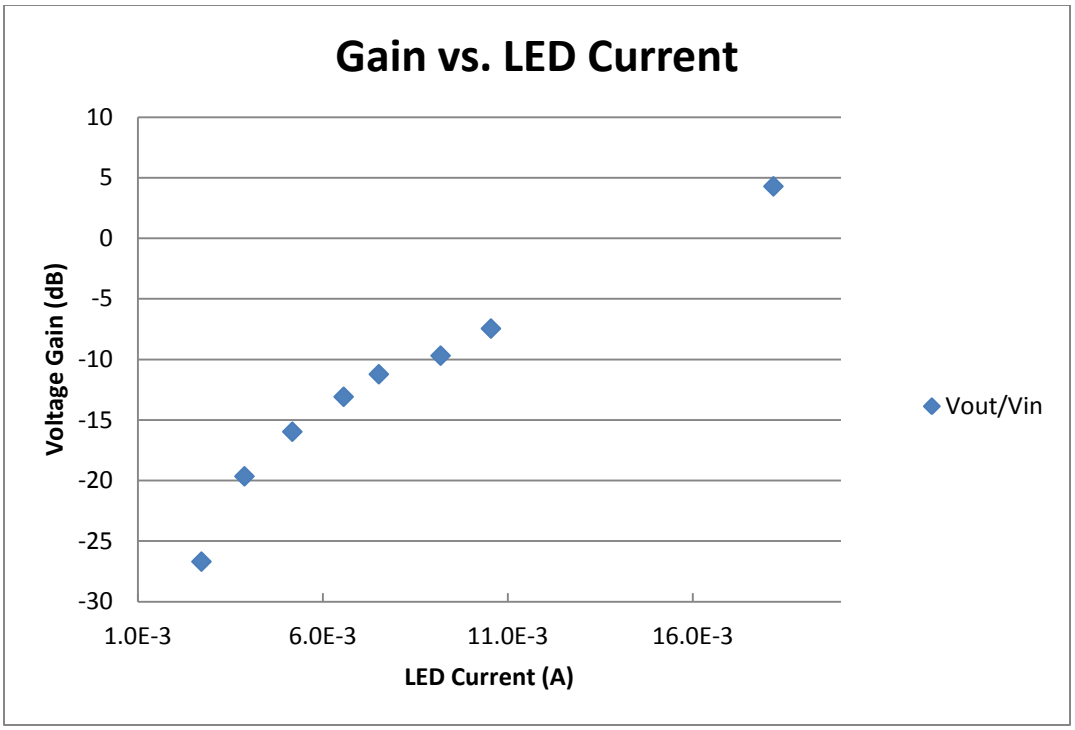


Figure 4.19 Voltage gain versus LED current

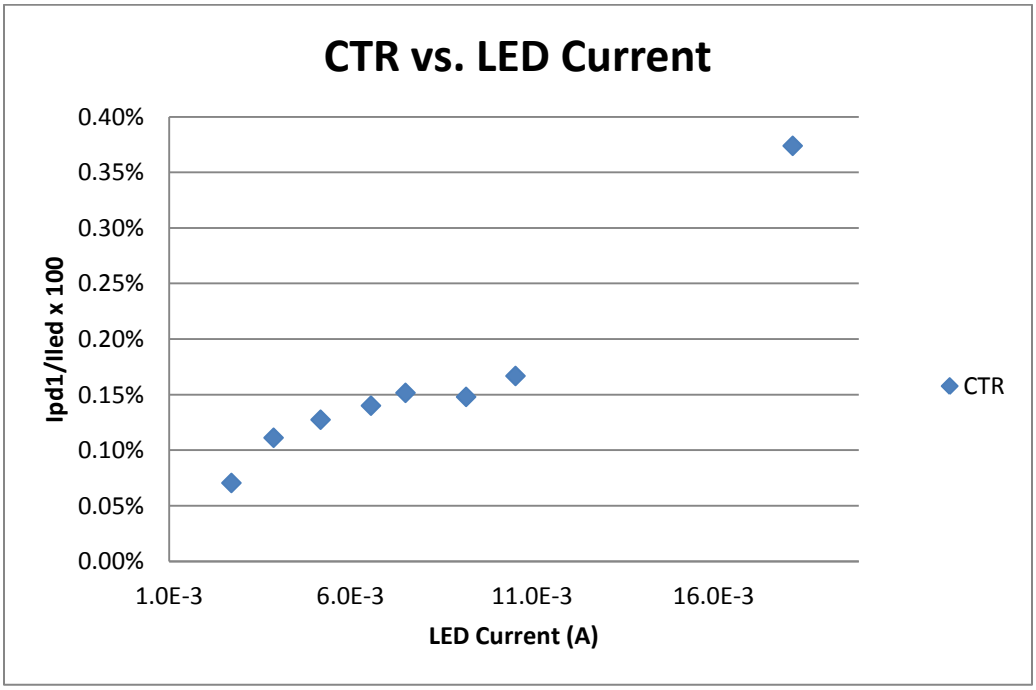


Figure 4.20 CTR versus LED current

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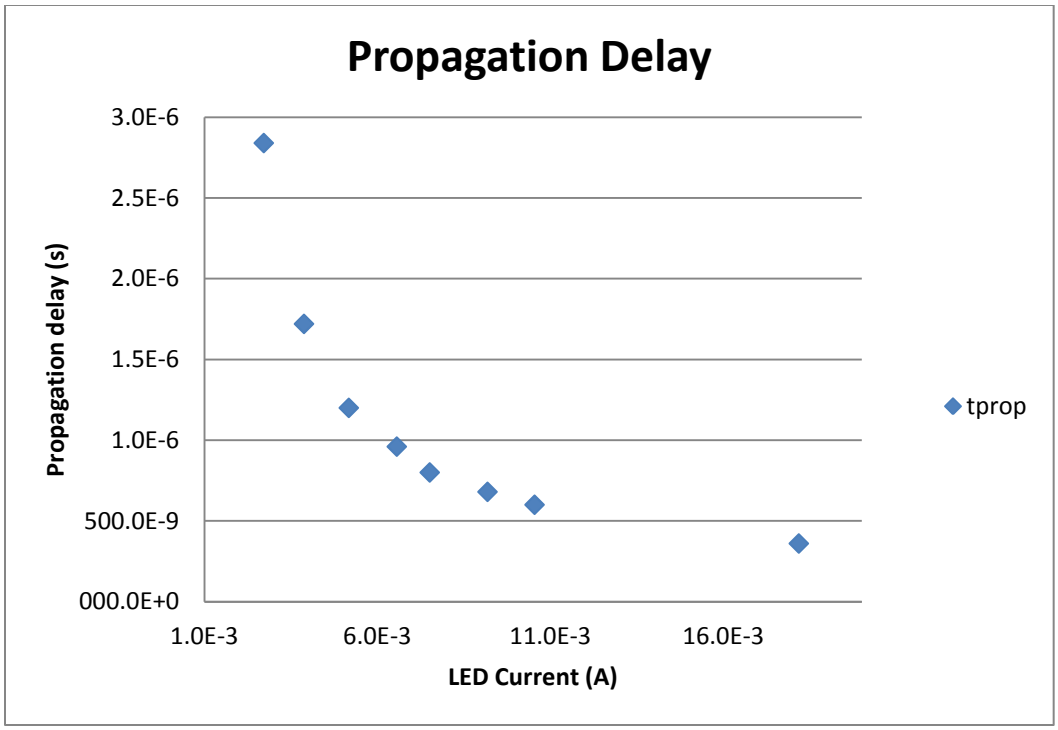


Figure 4.21 Propagation delay versus LED current

Figure 4.19 shows the voltage gain over the changing input bias currents. Also, the change in the CTR can be seen in Figure 4.20 to be non-linear as it increases from 0.10% to just under 0.20% as the input LED current increases. Note that the 0.40% outlier is not an artifact but obtained with a biasing point that is at the extreme edge of the safe operating area so it is not taken into account, but it can be seen to cause another 10 dB increase in the voltage gain. So, a tenth of a percent change in the CTR is seen as a 30 dB change in the voltage gain. This is due to the value of R_2 being so large. It has to be so large to get a voltage at the output that is of a comparable magnitude of the input. To achieve that, R_2 must compensate for the inherent low gain of the optocoupler due to the very small CTR value (about 0.2%). In the previous topology it was seen that the circuit removed the effect of CTR so it had a much more stable gain. This will affect both the outcome of the final benchmark, and the selection and design of the specific topologies for implementation in the Buck converter.

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The rise and fall times are not recorded because they do not change with each biasing point (the slope increases as the output voltage increases). The effects of LED current on the propagation delay are shown in Figure 4.21. The propagation delay of the input voltage triggering the output voltage to change decreases as the LED is biased with more current, from 3 μs to 500 ns. The propagation delay could not be decreased any further because the LED cannot be operated with more current. Recall that in the second part of the biasing experiment the value of R_{LED} is held constant (I_{LED}=5.2 mA) and R2 is swept from 22 kΩ to 200 kΩ. The results are shown in Figure 4.22. This shows that the propagation delay of the op amp is affecting the overall propagation delay for this analog transmission optocoupler. The larger the resistance in the feedback path of the output op amp the larger the effect on the propagation delay the op amp has. The 200 kΩ resistor increases the delay by 1 μs. This is difficult to overcome because the CTR is so low a very high gain needs to be added by the output op amp which decreases its bandwidth and thus adds to the delay of the positive edge of the input voltage causing a reaction by the output. This will be a very important design trade-off between the correct voltage gain and the needed propagation delay. These results will be used to determine the benchmark in the Conclusions Chapter and the selection of the specific topologies to be used in the Buck converter. The next section also describes an experiment that will use the biasing information from this experiment to determine more dynamic characteristics of the open-loop analog transmission topology.

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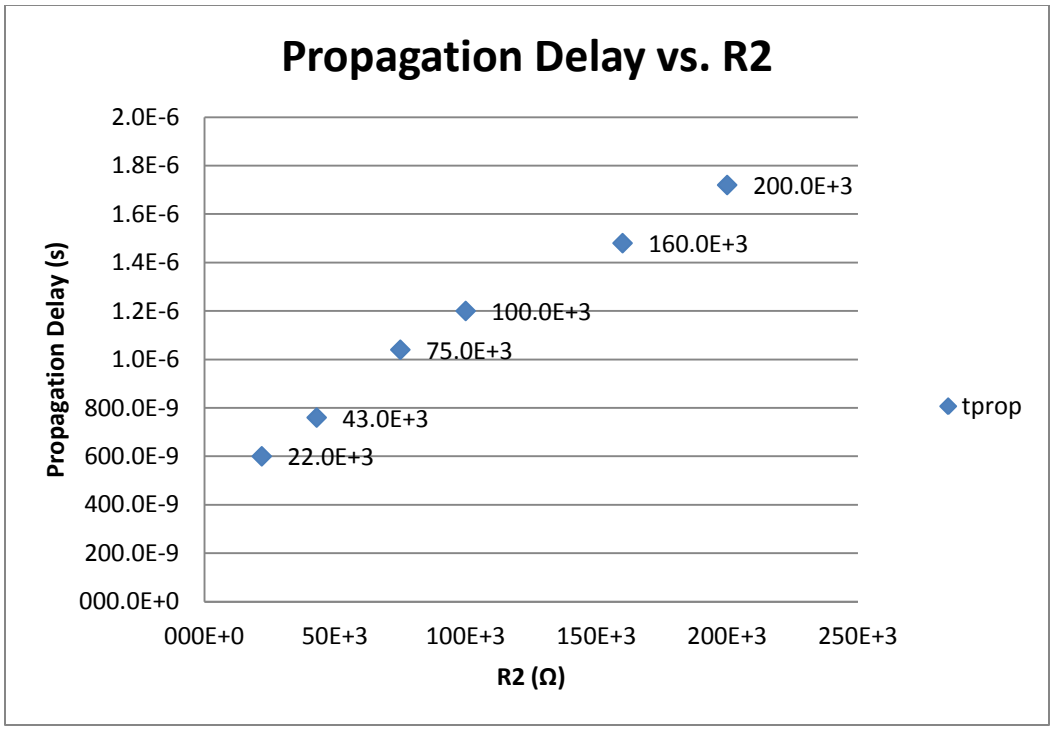


Figure 4.22 Propagation delay versus changes in R_2

4.2.4 Open-Loop Analog Transmission Topology Linearity and Temperature Experimental Setup

Now that the biasing is understood for this topology, a sinusoidal input with a peak-to-peak voltage that spans the entire biasing range is applied and the experiment described below is repeated while the optocoupler is at 25 °C, 50 °C, and 70 °C. This range of temperatures is chosen because it stays well below the maximum temperature of 85 °C. The experiment is repeated for different values of R_{LED}; 110 Ω, 270 Ω, and finally 510 Ω. These are chosen as a good range of biasing from the previous experiment. The experiment is also repeated at each R_{LED} for different values of R_2; 100 kΩ, 75 kΩ, and 45 kΩ. This is performed to understand the impact the op amp's propagation delay on the dynamics of the system while operating with a sinusoidal input. The temperature experiments are not repeated for all the other values of R_{LED} and R_2 from the previous experiment because it was already shown that the biasing points chosen above are the best for this topology in terms of propagation delay, voltage gain, and power consumption. This decision is made because it is the purpose of this research to optimize

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these key parameters for the final benchmark and the implementation into the dc-dc converter system. The experimental results at the other non-optimal biasing points would be extraneous.

There are two different input voltages applied over the course of this experiment. Both of them are applied as an 80 kHz sinusoidal waveform. The first input voltage is from 0 to 3.8 V. This is chosen because the input voltage needs to be above a threshold voltage to bias the LED. This threshold is different for each value of R_{LED} since it will decrease the voltage potential at the anode of the LED. This threshold is discovered using the 0 to 3.8 V input waveform. There is also a ceiling because of the variable voltage gain while changing the LED resistance. This maximum input voltage changes for each resistor because the voltage gain will cause the output to increase above the supply rail which clips the output voltage. Once these considerations are determined a second input voltage is applied that changes for each $\mathrm{R_{LED}}$ used in the experiment. The input voltage peak-to-peak differs for each value of $\mathrm{R_{LED}}$ but the circuit is biased consistently so comparisons can still be made. The output peak-to-peak voltage is measured along with the LED current. The CTR is calculated and will be analyzed over the whole input biasing range. This is important because an analysis of CTR will show how it changes over temperature. Also, the voltage gain will be measured and recorded in this same way. Figure 4.23 shows the test setup. To summarize this complex experiment, two main experiments are repeated for different resistor values. The first determines the minimum and maximum input voltage that can be applied for each resistor. The second applies the correct input voltage waveform at 80 kHz for each biasing point and is repeated at each temperature. This experiment will determine the benchmark for this topology and aid in the future selection of the correct topology for the Buck converter.

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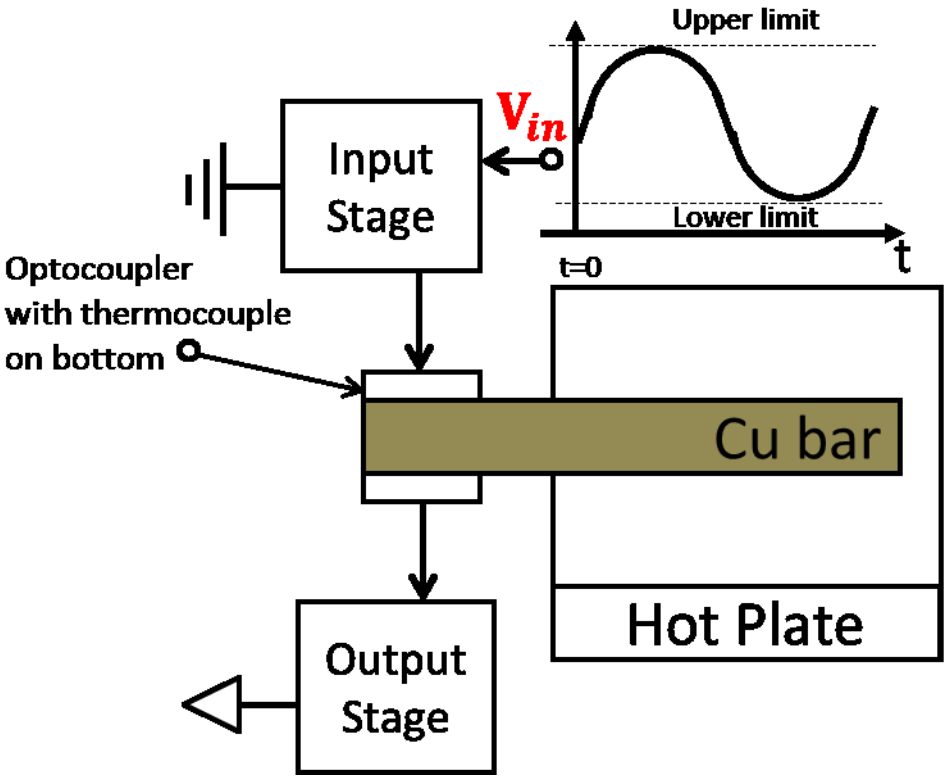


Figure 4.23 Temperature and linearity test setup, probe placement is the same as in the bias test but the input waveform is changed based on discussion above

4.2.4.1 Open-loop Linearity and Temperature Experimental Results

The first results recorded are for the first input voltage applied at 25 °C to show the threshold that the input has to be to initially bias the circuit enough to achieve an output voltage. Figure 4.24 shows the waveforms that present threshold on the input voltage and current. The LED current threshold will be the same at every input LED resistance, but the voltage drop over the resistor causes a larger voltage drop at the same current so more voltage needs to be applied to overcome the larger voltage drop. The thresholds are shown for the different input LED resistances in Table 4.5.

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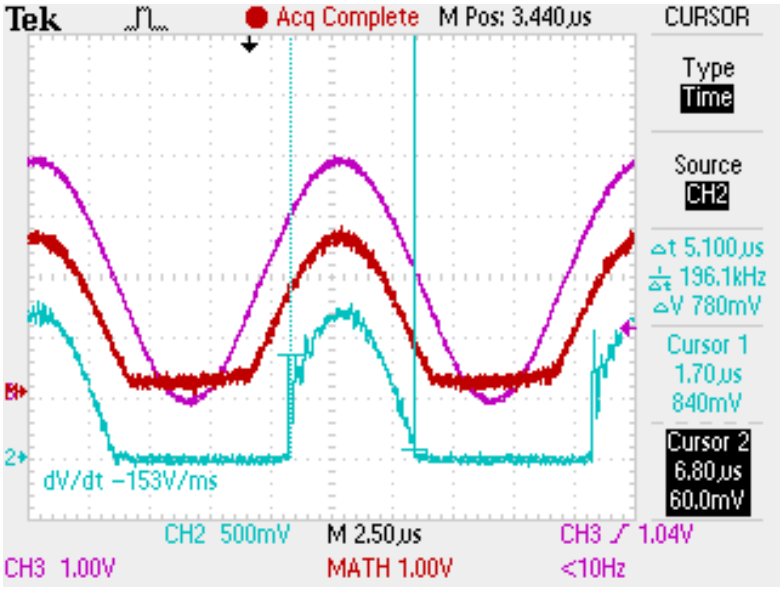


Figure 4.24 Waveform showing input threshold that must be overcome before output has voltage, input (purple), output (blue), I_{LED} (red)

Table 4.5 Input Threshold for Different Values of R_{LED}

R_{LED} (Ω)	Input Threshold (V)
110	1.6
270	1.9
510	2.5

The second part of the experiment applies the correct input voltages repeated for the different resistances and temperatures. This will provide understanding for how CTR changes with respect to input LED resistance, output resistance, and temperature in the open-loop analog transmission topology. The CTR is recorded over the entire range of the input voltage applied by using Excel to calculate the results point by point (the same propagation delay shifts are made on the output as in the previous experiment). The x-axis in the following graphs displays the time the input voltage is applied for one cycle and the y-axis is the CTR as a percentage. The time is arbitrary but it represents one cycle of

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the 80 kHz input voltage. In following sections the data will be broken out with the input voltage as the x-axis.

The CTR in these graphs can only be seen as a trend since it is not directly measured against the input voltage, but this will be done more concisely following the explanation of the CTR trends over biasing. The graphs in Figure 4.25 through Figure 4.27 show that with changing output resistances (R_2) the CTR is held constant, which is expected, but showing it verifies the results are accurate with the understood concepts, the output resistor should not have an effect on the current transfer ratio of LED current to photodiode current. Also, the CTR is very non-linear for regions outside of what will be defined as the plateau region. The plateau region is defined by a region where the CTR is within ±5% of a flat value. The non-linear region is located on either side of the plateau region and is seen by a sharp decrease from the value of the plateau region to 0% where the LED current reaches 0 A.

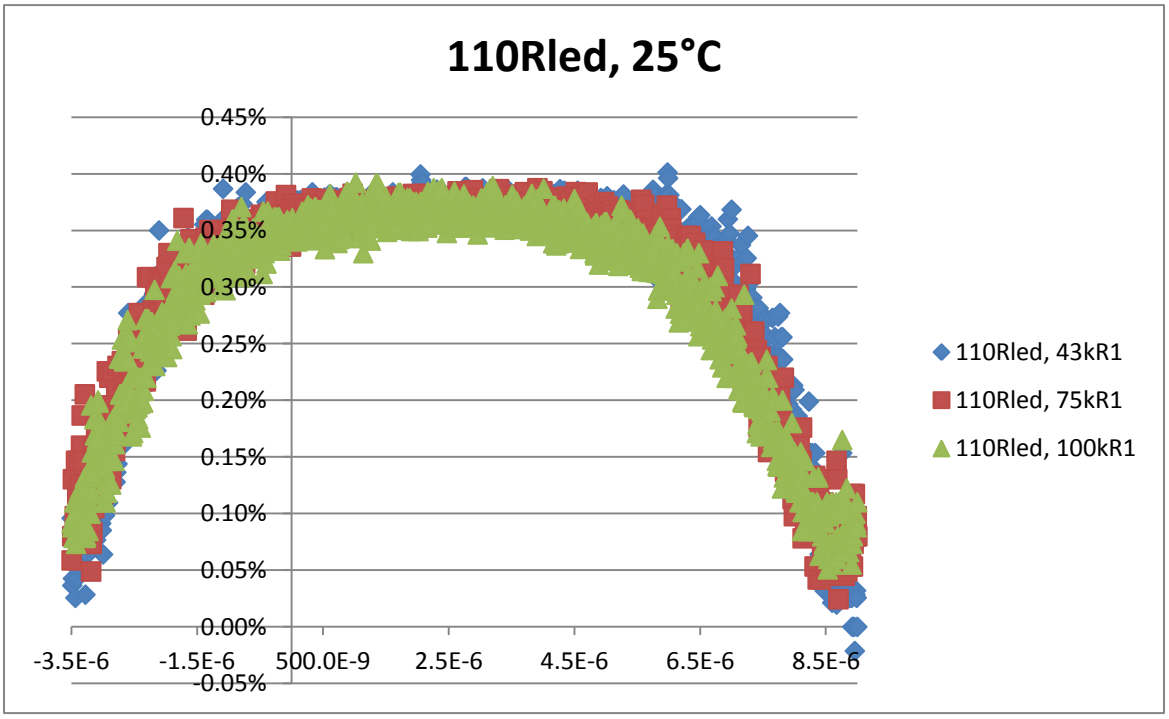


Figure 4.25 CTR over entire time of input voltage range for different R2's with R_{LED} equal to 110 Ω

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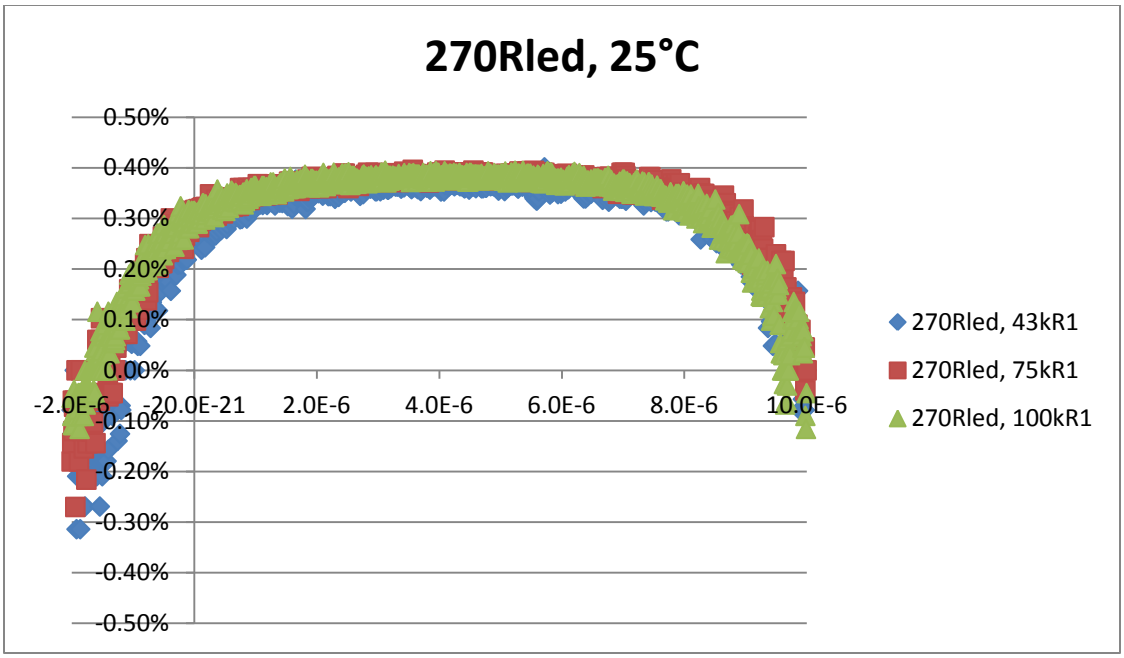


Figure 4.26 CTR over entire time of input voltage range for different R2's with R_{LED} equal to 270 Ω

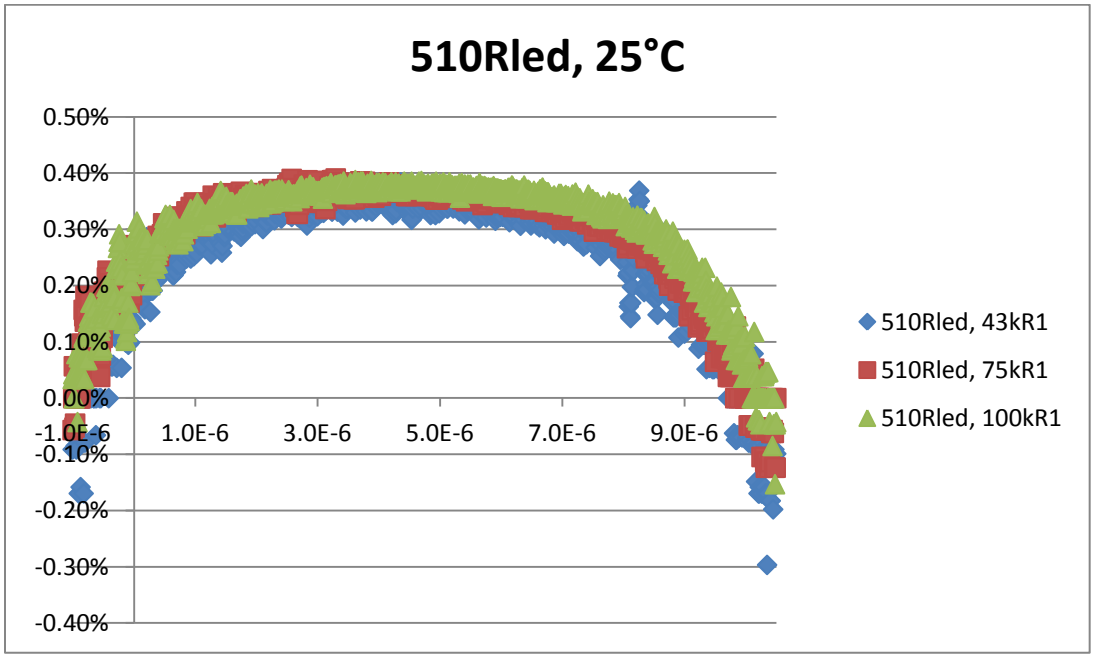


Figure 4.27 CTR over entire time of input voltage range for different R2's with R_{LED}equal to 510 Ω

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The relationship between the plateau region, the input voltage, and current is better presented when the x-axis is in terms of the input voltage and the input LED current. This is shown in Figure 4.28 and Figure 4.29, respectively, at 25 °C. Because there is not a noticeable change when the different output resistances are used (as seen in the trends in the previous figures), the 43 kΩ resistor experimental results are arbitrarily chosen to be displayed to simplify the presentation. The threshold voltages can also be seen in these figures at the point the CTR starts to increase representing the LED current being above 0 A. The graph in Figure 4.29 shows that the CTR trend with respect to LED current is the same for all of the different LED resistors; this verifies the results are consistent. It also shows that the plateau region starts at the same current value of 16 mA. The input current in the 270 Ω and the 510 Ω plots do not go as far as the 110 Ω plot because the input voltage is limited to a smaller voltage maximum due to the voltage gain increasing with decreasing resistance, but the trend is still shown to be consistent. The plateau region is defined in Table 4.6.

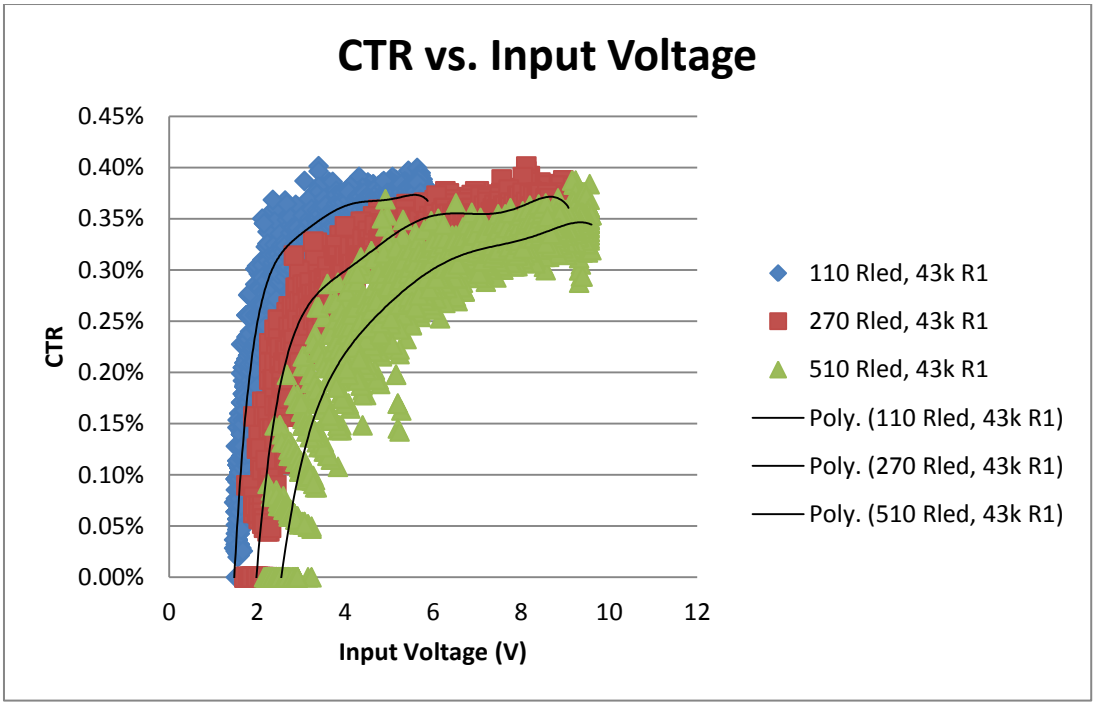


Figure 4.28 Relationship between CTR and input voltage for different R_{LED}s

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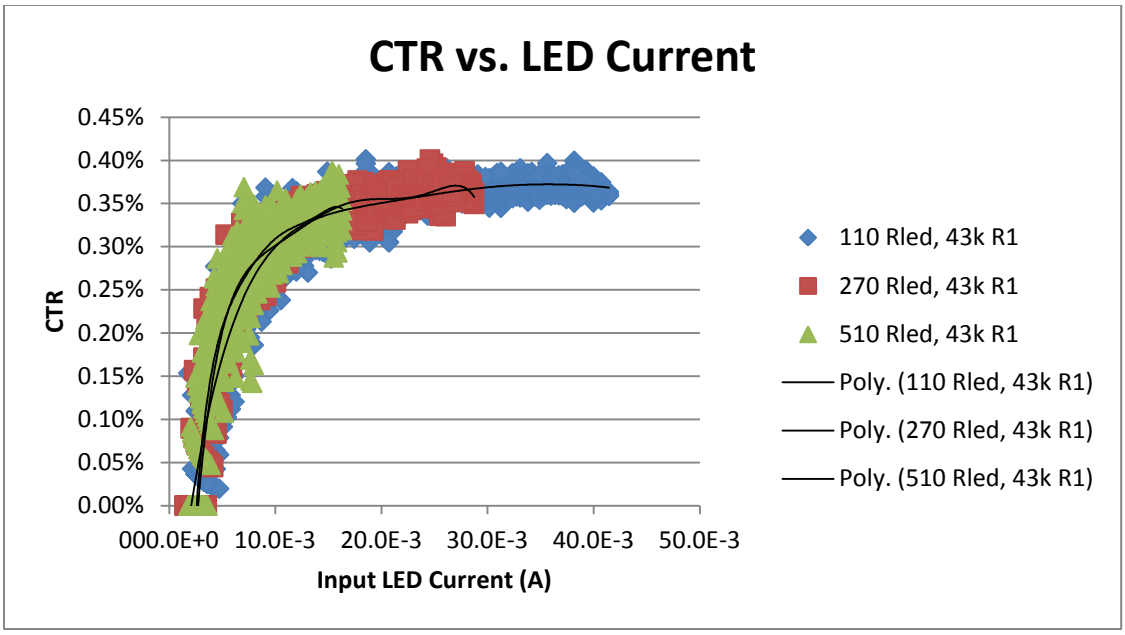


Figure 4.29 Relationship between CTR and LED current for different R_{LED}'s

Table 4.6 Plateau Region for Different R_{LED}'s

	Plateau Region (V)	
R_{LED} (Ω)	Input Voltage (V)	LED Current (mA)
110	3	16
270	5	16
510	7	16

Table 4.7 Propagation Delay for Different R_{LED}'s

		Propagation Delay (ns)		
R_{LED} (Ω)	R_2 (Ω)	25°C	50°C	70°C
110	43k	120	90	100
	75k	140	130	120
	100k	190	210	140
270	43k	120	110	160
	75k	130	150	180
	100k	140	130	180
510	43k	210	150	140
	75k	240	210	180
	100k	180	200	180

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The data in

Table 4.7 shows the propagation delay with respect to temperature and LED resistor. The trend for the propagation delay for this topology is to stay within ±20% of 200 ns for all ranges of temperature and output resistance. This continues the trend of the mechanism of propagation delay to be complex. This topology does have a more stable propagation delay over a sinusoidal input than when a dc value is applied. Figure 4.30 through Figure 4.32 show the CTR change over temperature for each LED resistor plotted against the input voltage. The output resistor is held constant but arbitrary to the results as stated earlier, it does not affect CTR.

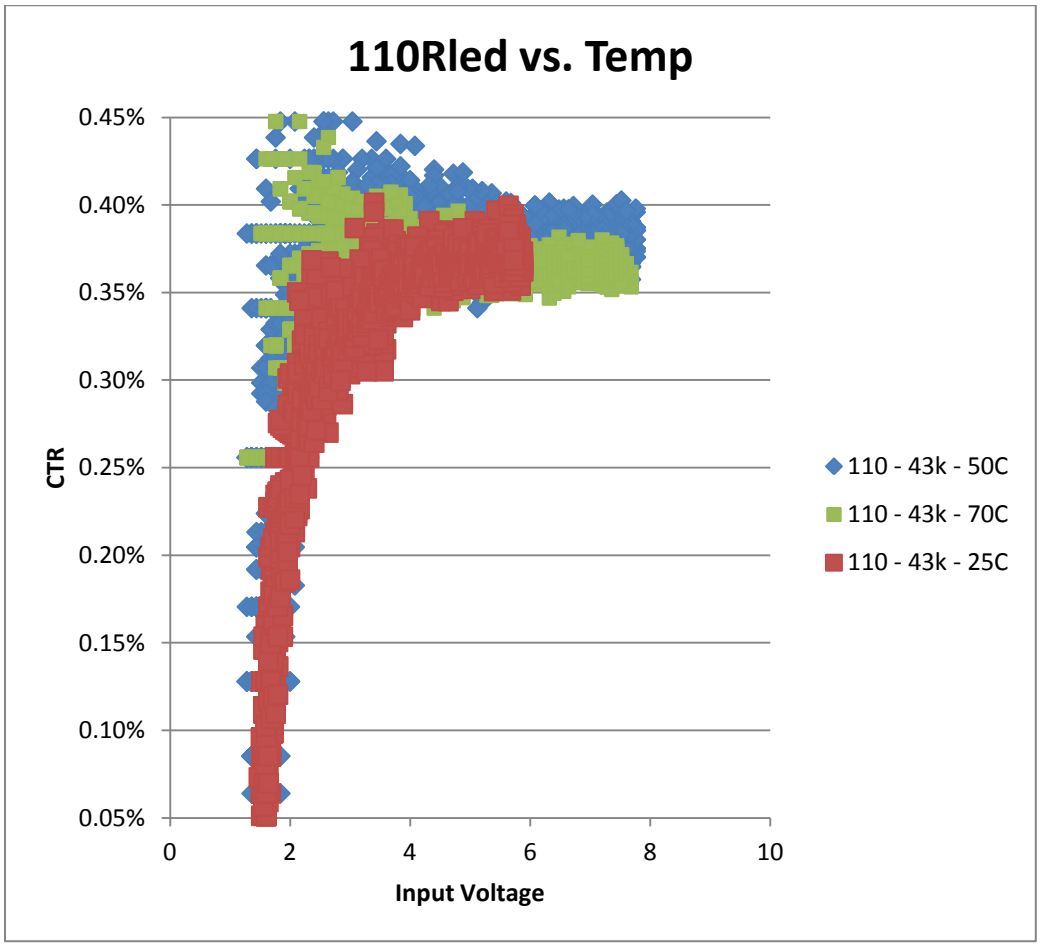


Figure 4.30 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 110 Ω

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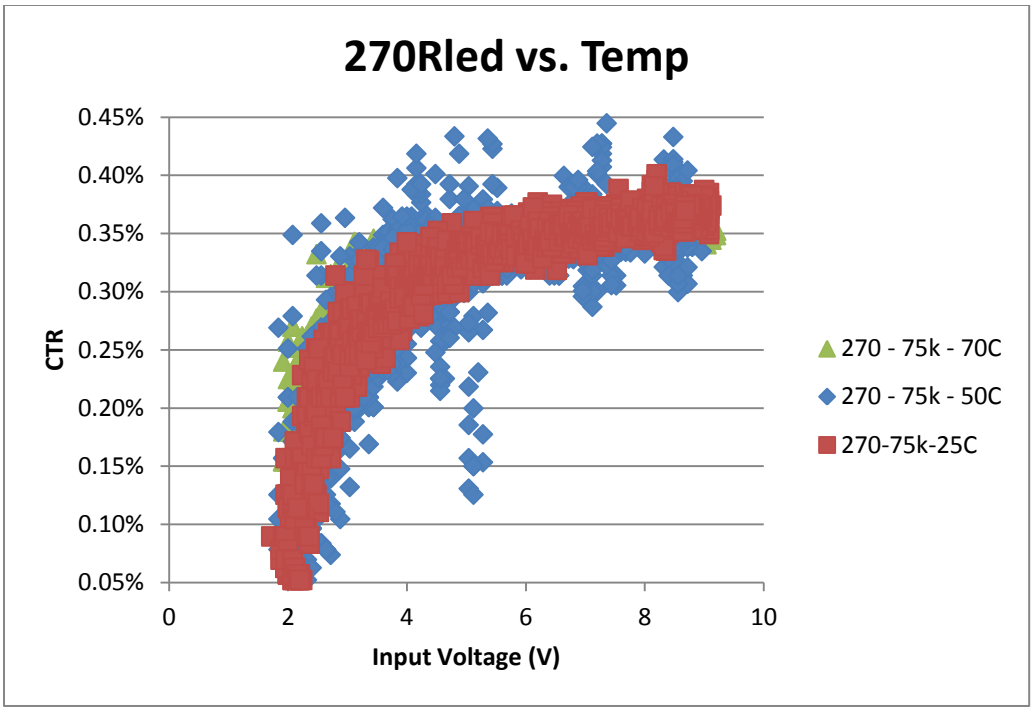


Figure 4.31 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 270 Ω

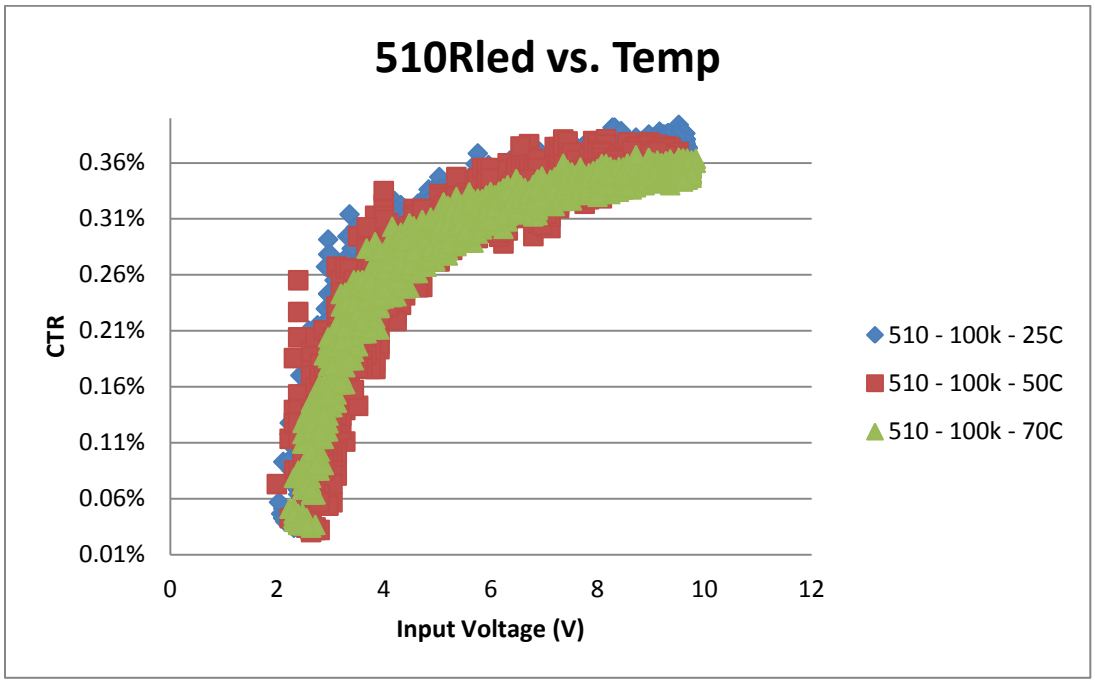


Figure 4.32 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 510 Ω

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The CTR decreases by 4% on average as temperature increases. As shown in the biasing experiment this is represented by a much larger voltage gain decrease. This introduces very large non-linearities and will be summarized in the Conclusions Chapter in the final benchmark.

This concludes the discussion of the results from both of the analog transmission topologies. The design decisions for the implementing the correct topology is made in the Optocoupler and Buck Converter Chapter. The next section describes the experiments to determine which digital transmission approach will be implemented in the Buck converter and the final digital optocoupler benchmark.

4.3 Benchmark Experiments for Digital Transmission Topologies

The optocouplers in this section were shown in Table 4.1 and were chosen because a comparison between GaAsP and AlGaAs needs to be made. The optocouplers have the auxiliary circuitry internal to the package except for the topology with the LED and photodiode base BJT pair. The latter type needs an external pull-up resistor that affects power consumption and minimum pulse width. The analysis of these topologies is to find the best one for the Buck converter and determine the benchmark of the digital optocoupler topology. The analysis is broken down into five distinct experiments. The first four experiments are used to analyze the two different optocoupler topologies. Note that there are two different optocouplers representing the two materials in each topology – the two material types in the NPN BJT category and the two for the totem pole amplifiers. The fifth experiment takes the best topologies (ranked by the key parameters that have been discussed -- power consumption, propagation delay, and minimum pulse width) and implements the same experiments at the best operating point of the devices over temperature. The CTR is not an important parameter in these tests because the output stage is forced to switch fully on, or off, depending on the input. The optocoupler in each category was specifically chosen because it was the fastest and least power consuming of the optocouplers analyzed in the chart at the beginning of this chapter, Figure 4.1.

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4.3.1 LED BJT Pair Digital Transmission Optocoupler Experimental Setup

The first topology to be analyzed is the LED and BJT pair. The two optocouplers in this category are the GaAsP HCPL4505 and the AlGaAs HCNW4505 [13]. These optocouplers will be put through the same experiments and compared to each other to find the one that has the best power consumption, propagation delay, and rise and fall times. The values of V_{in}, V_{out}, I_{LED}, I_C, and I_{src} are measured while the power consumption, rise and fall time, and the propagation delay are calculated. The input is a ten cycle pulse of 10 V and the steady-state values are recorded. To find the best biasing point R_2 is held at a constant 1 kΩ while R_{LED} is swept from 16 kΩ to 400 Ω corresponding to an LED current of 0.5 mA to 20 mA, which is within the safe operating range for both optocouplers. This part of the experiment will discover which operating point optimizes the key parameters. The best biasing point then selected and an experiment is repeated with the same input waveform and the LED resistance held constant while the output resistance R_2 is changed from 510 Ω to 16 kΩ to find the minimum rise and fall times for each optocoupler. The experimental setup is shown in Figure 4.33.

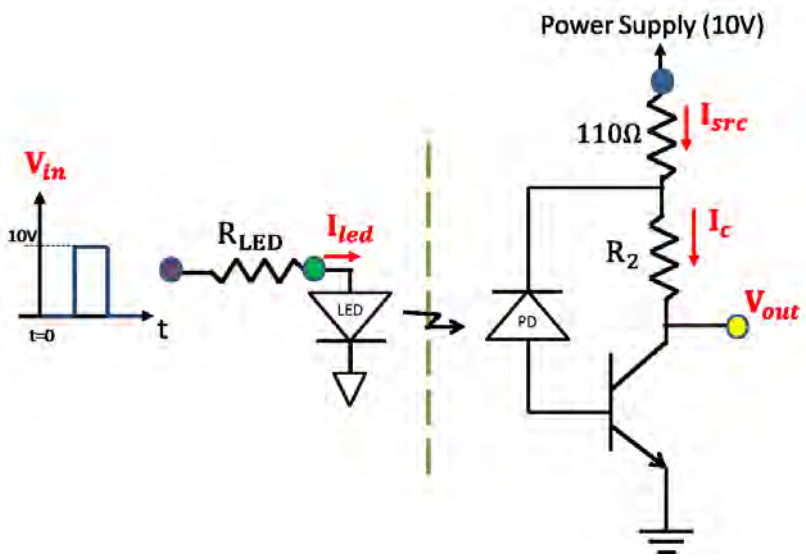


Figure 4.33 Experimental setup schematic for HCPL4505 and HCNW4505 LED/BJT pair digital topology with probe locations shown (LED current is measured with MATH)

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The first results represent the data recorded for both the HCNW4505 and the HCPL4505 when the output resistance R_1 is set to 1 kΩ and the experiment is repeated for different values of the input LED resistance. Note that the output is inverted from the input signal. With an output resistance of 1.5 kΩ the HCNW output BJT is in the active mode and the output can only be as low as 0.2 V, but at 1 kΩ the output voltage is only 1.2 V, in saturation mode. The HCPL output BJT never falls below 0.8 V. The trade-off between saturation and active mode is that the fall time is much slower because of minority carriers having to be swept out of the base region. Figure 4.34 presents the raw waveforms for the experiment before the data is extracted and presented. Note that as it has been defined, the rise time is when the output changes to the low-state, and the fall time is when the output changes to the high-state. This is to be consistent when compared to the analog transmission rise and fall time corresponding to the input being applied and removed, respectively.

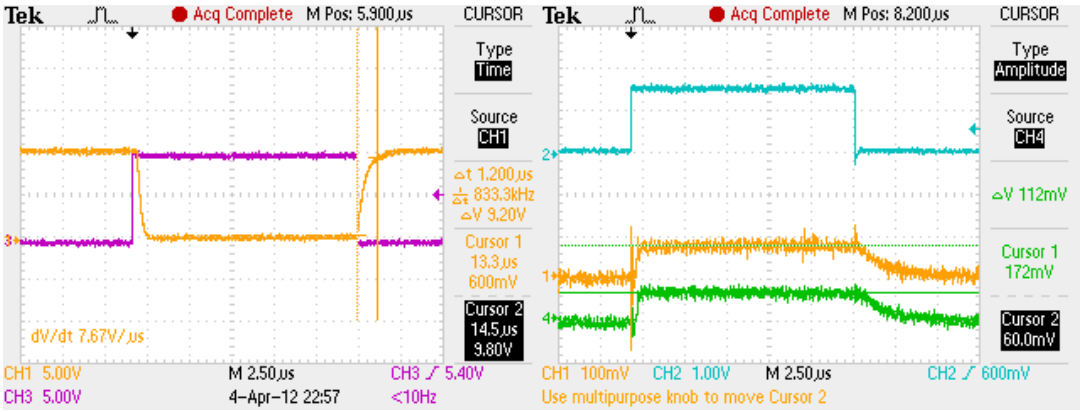


Figure 4.34 Waveform from test; (left) input (purple), output (yellow); (right) LED current (blue), power supply current (yellow), collector current (green)

Figure 4.35 shows the comparison of the propagation delay and the rise and fall time compared across all of the different biasing points showing off the differences between the HCNW4505 and the HCPL4505.

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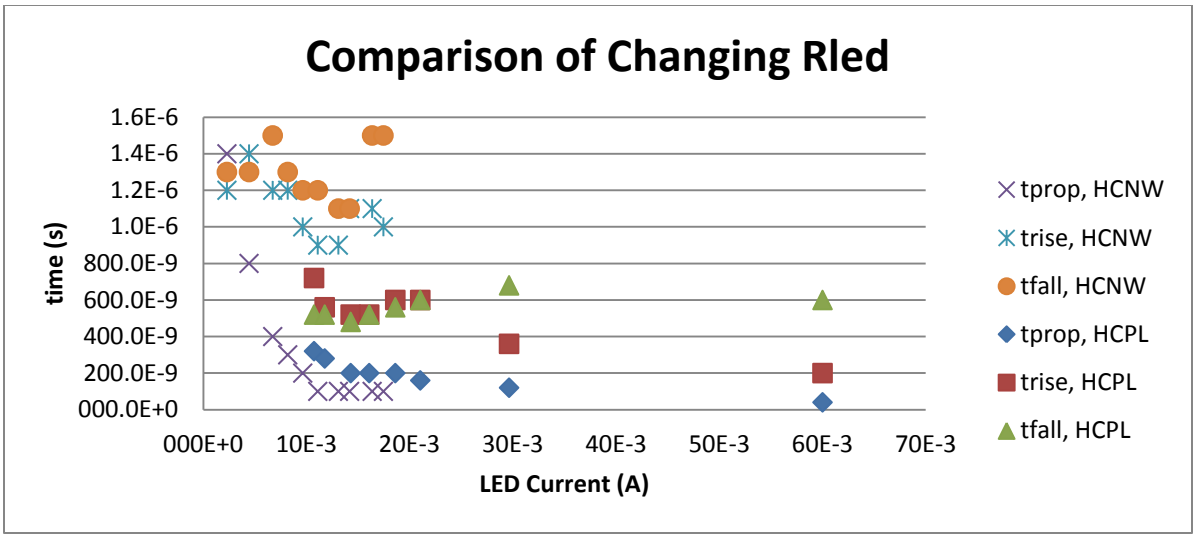


Figure 4.35 Comparison between HCNW4505 and HCPL4505 of rise/fall and propagation times versus LED current and changing R_{LED}

In the initial parts of the biasing experiment (when the input LED resistor is a large value) the output of either of the optocouplers does not fully switch to the low-state. For the output to completely switch the LED needs to be biased with at least 10 mA for the HCNW4505 and 21 mA for the HCPL4505. The HCNW4505 requires 20 mA less current to be at the same propagation delay, but its fall and rise times are 50% to 100% larger. The 400 Ω LED resistance is chosen as the optimal biasing point for the HCNW because the output response is the fastest. Following the same analysis for the HCPL, the LED resistance is chosen to be 270 Ω.

Now that the nominal R_{LED} is chosen, the second part of the experiment can be performed. Figure 4.36 shows the propagation delay and rise and fall times with changing output resistances. The x-axis is shown as power dissipation of the output stage to show the relationship between power consumption and turn-off time (fall time). Because the LED is biased properly the propagation delay stays constant.

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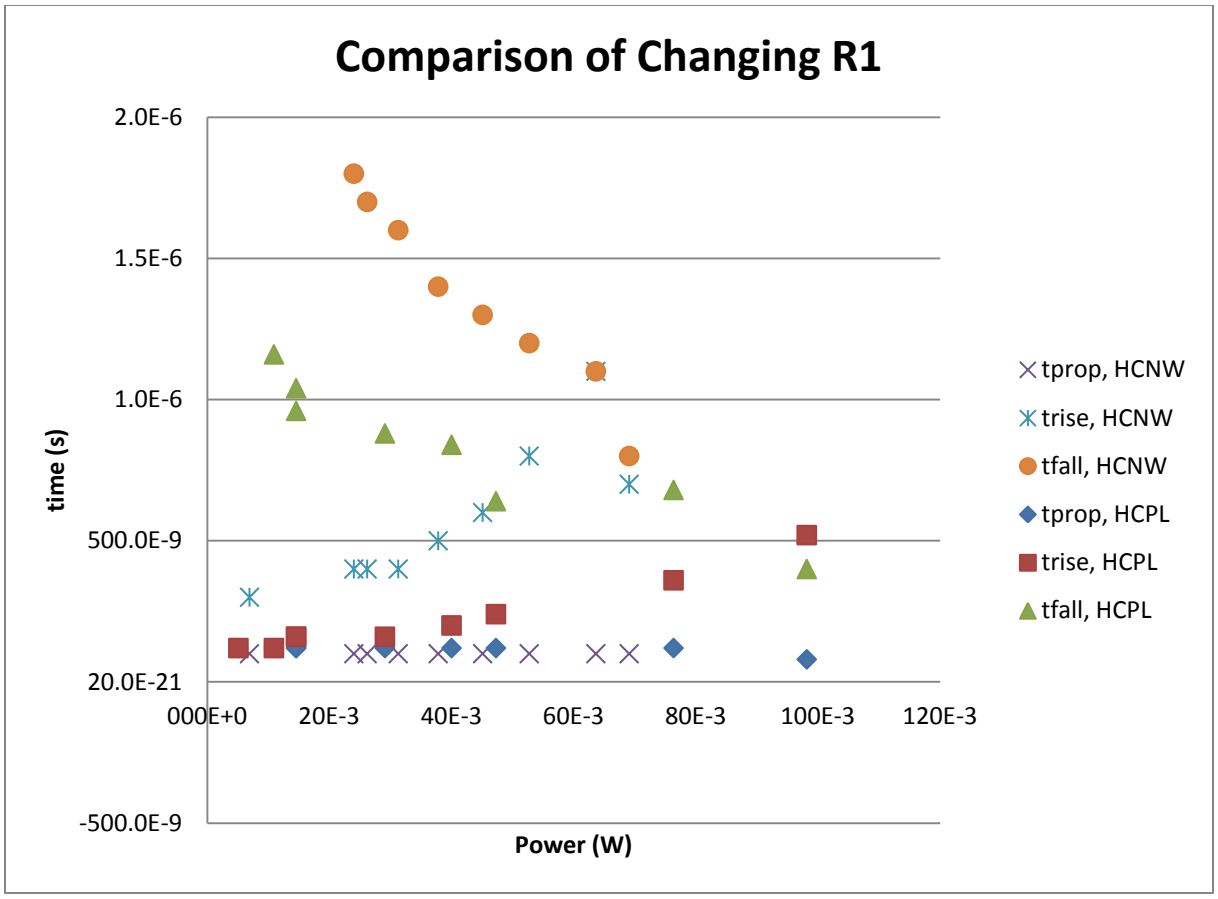


Figure 4.36 Comparison between HCNW4505 and HCPL4505 of rise/fall and propagation times versus power consumption for changing R_2

As the output power increases from 20 mW to 100 mW (representing decreasing output resistances) two things happen. First, the fall time for the HCPL decreases from 1.2 µs to 400 ns and the HCNW from 1.8 µs to 750 ns. Secondly, the rise time for the HCPL increases from 100 ns to 500 ns and the HCNW from 250 ns to 750 ns The HCPL4505 has the same propagation delay and smaller fall and rise times with the same power dissipation on the output. Because of this and the fact that the topology selection for the Buck converter and benchmark are determined by the optimal values for propagation delay, rise and fall times, and power consumption, the HCPL4505 is chosen for the final experiment that repeats the previous procedures at varying temperatures.

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4.3.2 Amplifier Digital Optocoupler Benchmark Experimental Setup

The two optocouplers in this category are the GaAsP ACPL-071L and AlGaAs HCPL-7723 [11], [10]. These two optocouplers have output amplifiers internal to the package that magnify the photodiode current with a CMOS totem pole output stage. The HCPL-7723 also has an input amplifier internal to the package. These optocouplers can only utilize a maximum of 5 V on output stage power supply. The only thing that can be changed about the biasing is the input LED current. The input voltage is pulsed to 4 V (the maximum input voltage) for the ACPL-071L, and the value of R_{LED} is changed from 820 Ω to 270 Ω corresponding to an LED current of 4 mA to 9 mA [11]. The system variables V_{in}, I_{led}, I_{src}, and V_{out} are measured and the power consumption of the output, the propagation delay, and the rise and fall time are calculated. Figure 4.37 shows the experimental setup for the ACPL-071L.

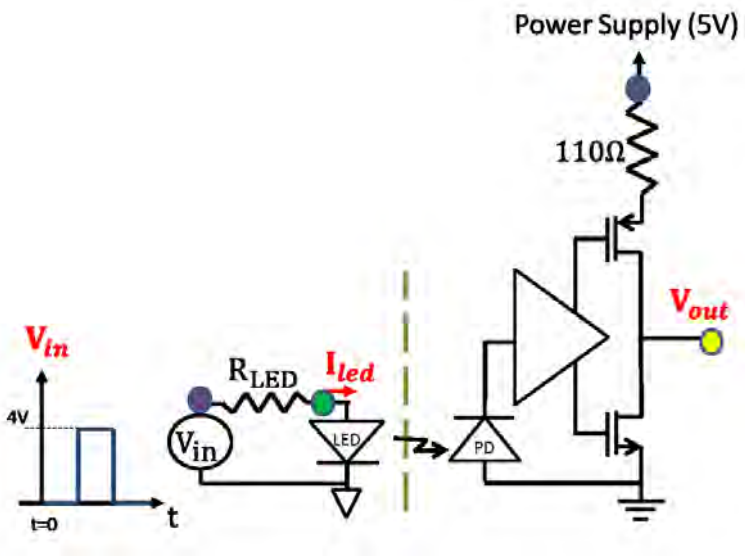


Figure 4.37 Experimental setup for the ACPL-071L LED/amp digital topology with probe locations

The HCPL-7723 has to have a slightly different experimental setup. The input does not need an LED resistance to bias the LED. Figure 4.38 shows the experimental setup, which shows the input stage is a buffer that biases the LED internally. The input voltage is pulsed to 2 V which is the maximum while

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the input power supply is at 5 V [10]. V_{in}, I_{src1}, I_{src2}, and V_{out} are measured so that the power consumption, the propagation delay, and the rise and fall times can be calculated.

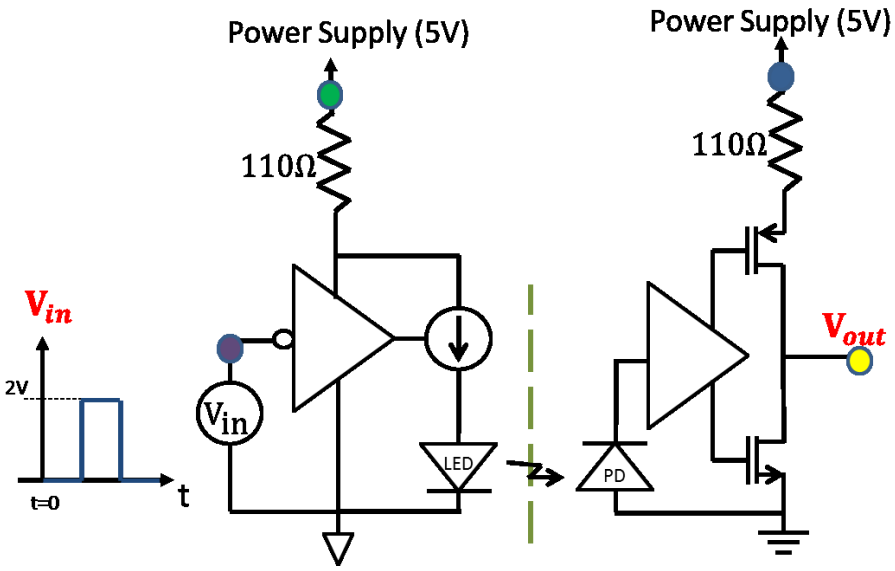


Figure 4.38 Experimental setup for the HCPL7723 amp-LED/amp digital topology with probe locations

The amplifier digital topologies are discovered to be very stiff systems; the measured parameters stay very consistent throughout the experiments. The ACPL-071L experimental results are presented below. This optocoupler uses a complete system in a package. The input LED is biased with a resistor that can be anywhere from 680 Ω to 110 Ω without changing the output characteristics. The maximum input voltage and output supply voltage is 5 V, so the power calculations cannot be compared with the other digital transmission topologies unless they are scaled by a factor of 2. Also, because these devices utilize an optimized output stage the propagation delay and rise and fall times are so short that the input pulse had to be increased to 1 MHz. At this speed the parameters can be more easily measured and Table 4.8 shows the recorded data and Figure 4.39 show the corresponding waveforms.

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Table 4.8 Results for Two Different Operating Points

Recorded at 1 MHz		
R_{LED} (Ω)	**270**	**110**
V_{in} (V)	4	3.52
V_{out} (V)	0.32	0.32
I_{LED} (mA)	9.2	18.2
P_{out} (mW)	22.5	22.5
t_{prop} (ns)	50	48
t_{rise} (ns)	20	12
t_{fall} (ns)	30	16

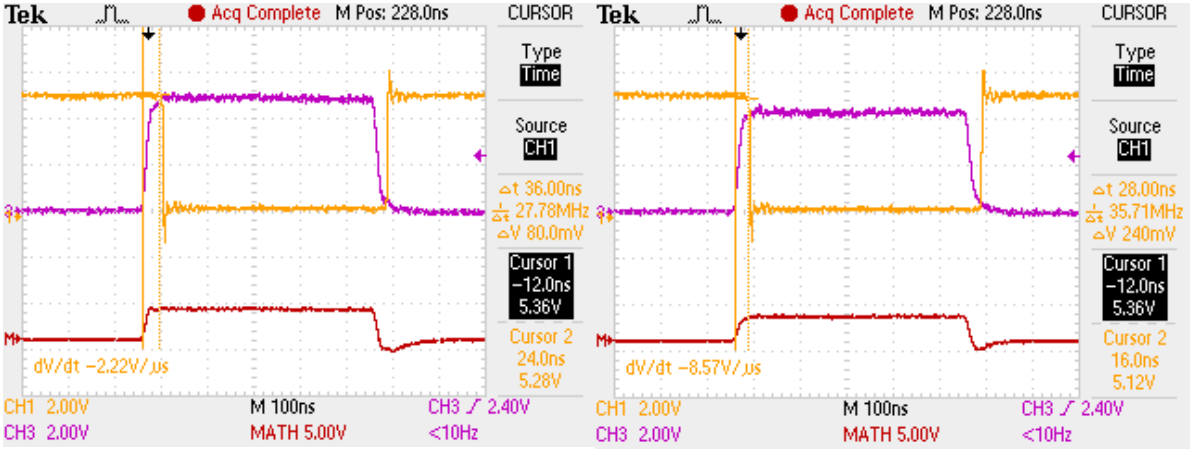


Figure 4.39 Waveforms for data points shown in Table 4.8 (left) 270 Ω, (right)) 110 Ω; output (yellow), input (purple), LED current (red)

The HCPL7723 is an even more all-in-one package with an amplifier biasing the LED and an output stage consisting of another amplifier. The experimental results are recorded below. Because of the all-in-one package, there is no need for an input LED resistor. The input voltage can be a maximum of 2 V to change the output and the input and output supply voltages must be 5 V, and there is not anything to do to bias it differently. Figure 4.40 and Table 4.9 show the only needed data point.

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Table 4.9 Results for HCPL7723

V_{in} (V)	2
V_{out} (V)	4.08
P_{in} (W)	0.06
P_{out} (W)	0.013
t_{prop} (ns)	24
t_{rise} (ns)	20
t_{fall} (ns)	44

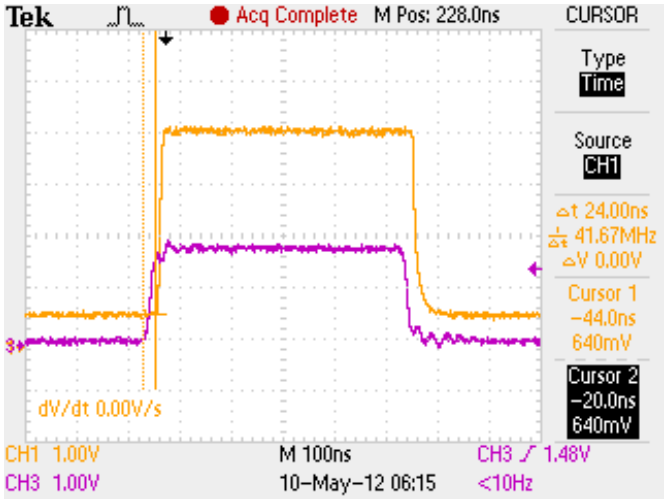


Figure 4.40 Waveforms for data points shown in Table 4.9, input (yellow), output (purple)

4.3.3 Digital Optocoupler Temperature Experimental Setup

The temperature experiments use the best of the previous digital schemes and scales their temperatures to 50 °C and 70 °C, at their best operating points, to find the benchmark for the digital optocouplers currently available. This final test will not have as many data points as the previous tests because each optocoupler will be biased at the optimized point so that the benchmark is found at these different temperatures. The test setup is the same hot plate setup as shown earlier and the input voltage does not change for each respective topology since linearity is not an aspect of these optocouplers.

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The temperature experiment for the HCPL4505, ACPL071L and the HCPL7723 are repeated at 25 °C, 50 °C, and 70 °C. The results are shown in Table 4.10 through Table 4.12.

Table 4.10 HCPL4505 Temperature Results

R_{LED} (Ω)	270			390		
Temp (°C)	25	50	70	25	50	70
V_{in} (V)	10	10	10	10	10	10
V_{out} (V)	1.2	1.2	1.8	1.6	1.8	2.2
I_{LED} (A)	29.6E-3	30.4E-3	28.1E-3	21.5E-3	21.5E-3	22.1E-3
I_{src} (A)	4.7E-3	5.1E-3	5.1E-3	4.4E-3	4.6E-3	5.1E-3
P_{out} (W)	47.3E-3	50.9E-3	50.9E-3	43.6E-3	46.4E-3	50.9E-3
t_{prop} (s)	120.0E-9	80.0E-9	120.0E-9	160.0E-9	160.0E-9	160.0E-9
t_{rise} (s)	240.0E-9	360.0E-9	360.0E-9	400.0E-9	440.0E-9	480.0E-9
t_{fall} (s)	640.0E-9	920.0E-9	1.0E-6	840.0E-9	880.0E-9	1.0E-6

As the temperature is increased the rise time increases by 50% and the fall time increases by about 50% as well when the LED is biased at 30 mA. When the biasing is decreases to 20 mA the rise and fall times only increase by 20%. The low-logic output voltage also increases with temperature to a maximum of 2.2 V due to the increased BJT saturation voltage.

Table 4.11 ACPL-071L Temperature Results

R_{LED} (Ω)	110		
Temp (°C)	25	50	70
V_{in} (V)	4	4	4
V_{out} (V)	0.32	0.32	0.4
I_{LED} (A)	2.4	2.6	2.4
I_{src} (A)	0.003	0.003	0.003
t_{prop} (ns)	28	28	28
t_{rise} (ns)	8	8	12
t_{fall} (ns)	8	8	12

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Table 4.12 HCPL7723 Temperature Results

Temp (°C)	25	50
Vin (V)	2	2
Vout (V)	4.08	4.08
Isrc1,avg (A)	0.006	0.006
Isrc2,avg (A)	0.013	0.14
t_{prop} (ns)	24	24
t_{rise} (ns)	20	16
t_{fall} (ns)	44	52

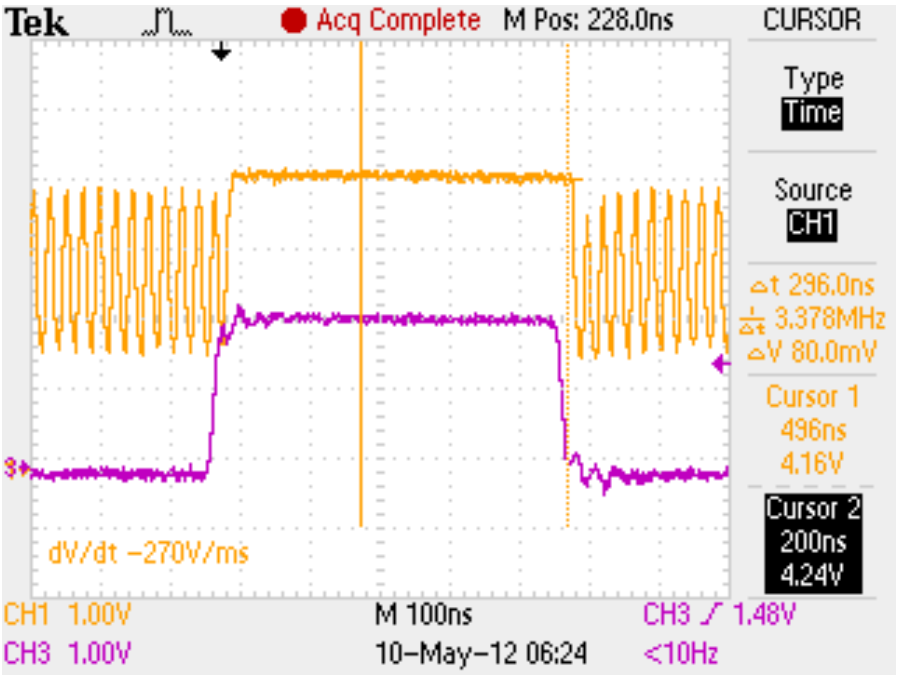


Figure 4.41 Oscillations in HCPL7723 at 70°C, input (yellow), output (purple)

The ACPL071L was stable across the temperatures except for the rise and fall times which began to increase at 70 °C by 100%. The final value was still only 12 ns which is two orders of magnitude below the BJT topology of the HCPL4505. The HCPL7723 was unstable with temperatures over 50 °C as seen in Figure 4.41. This oscillation was present when the optocoupler had no input applied at 70 °C. Nothing was changed between the low temperature experiments and the 70 °C testing of this circuit. A filter

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capacitor of 10 nF was applied and the experiment was repeated at all temperatures and the oscillations were still present at 70 °C.

Now that the optocoupler topologies are well understood, because of the experiments in this chapter, selections will be made in the next chapter of the correct topology for the Buck converter. Finally, in the Conclusions Chapter, the benchmark for the analog and digital topologies will be discussed and presented.

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5 IMPLEMENTATION OF OPTOCOUPLERS IN CLOSED-LOOP BUCK CONVERTER

Now that the gate driver that controls the main switch and the optocoupler schemes to transmit information between the actual Buck converter and its control circuitry have been defined, the closed-loop optically controlled Buck converter can be designed and implemented. The Buck converter's operation, and reason for choosing it as the application context to demonstrate the optocoupler's qualities, is generally discussed in the Background section. Now the goal is to design a working, closed-loop, current-mode optically-controlled Buck converter. This is accomplished in steps; the first is to present the final goal. That is, to have a Buck converter with a 100 V nominal input and an output of 5 A and 50 V (representing a 250 W load). This is the first and most important design choice. It is the operating point of the Buck converter that ultimately determines all the other selections, excluding the operating frequency. The switching frequency is chosen below but will just be a starting point because the final experiment to determine the impact of the optocouplers on the Buck converter system will increase the switching frequency until the circuit cannot operate any further.

The reason for choosing a 100 V input and a 250 W load is due to multiple reasons. This value is centered on the maximum voltage and power ratings of the different dc sources that are available in the lab, more specifically the input dc supply and floating dc supply. There are facilities that can implement up to 750 kW loads with a range of input dc levels. If that is possible then why choose the 100 V, 250 W design? Why not increase the input voltage to that of the withstanding voltage of the optocouplers at 1 kV? Firstly, the floating supplies can only float to 250 Vdc, so that is the maximum input voltage. Also the withstanding voltages of the optocouplers are very well determined and future optocoupler technologies will also have well determined withstanding voltages because the withstanding voltage is determined by the material properties and not the dynamics of the circuit. Also the design of a 1 kV system would be greatly complicated because the SiC MOSFET switch is only safe switching a dc link, or

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input voltage of 600 to 800 V to stay well below its 1.2 kV blocking voltage rating due to the inevitable transients that occur. What truly needs to be tested is not the power of a Buck converter (that can be scaled relatively easily), nor the voltage isolation of the optocouplers (determined already), but a test that determines a benchmark for the speed at which the optocouplers will allow the Buck converter to operate correctly. Frequency is practically independent of power between 100 V and 1 kV so there is no need to complicate the design to determine the impact of the optocouplers.

This design will be presented in two steps. First, the procedures, reasons, and design equations for the various circuits and their components and IC's will be presented. Secondly, these procedures will be followed and design equations used to select the final circuitry and specific component values needed for this design. Finally, after the design is complete the procedures to implement the full Buck converter system on a PCB and the experimental procedures and results are presented.

One note before the design is presented, simulation results will be presented with the appropriate circuit topologies presented in the design and a final full system simulation will be presented to verify the overall design. Circuits that will not be simulated are circuits that are too simple to require simulation to verify their operation, or the optocoupler topologies chosen. The optocouplers are not simulated for two reasons. First, the optocoupler topologies have been extensively verified in the experiments presented in the previous chapter. Second, the optocoupler is not dynamically modeled in any simulation environment. Simple models based on current controlled current sources can be implemented to verify static effects but, as stated in the previous chapter, this is not useful for this design because the optocouplers are used in a dynamic state to transmit constantly changing signals. A static model will not properly validate this functionality. But the purpose of the previous chapter was to not only determine the benchmark for these topologies, but to understand their implementation of the

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optocouplers into the Buck converter. With the results of the previous chapter as a guide the correct design decisions for selecting the right topology and the component values can be made.

5.1 Design Method and Implementation

As stated above, another important choice in the initial operating point of the design is the switching frequency. The integrated circuit chosen to close the loop and generate a PWM signal using current-mode control (comparing the inductor current and output voltage) has a minimum switching frequency of 80 kHz, so the initial frequency is set to 85 kHz to operate the PWM within a safe margin [24]. This is still relatively fast since some available optocouplers were shown to have a propagation delay between the order of microseconds and hundreds of nanoseconds depending on the biasing point. The on-time at a 50% duty cycle is only about 6 μs which shows that the optocoupler propagation delay is a very important characteristic to minimize. This propagation delay determines how long it takes for the system variables of the Buck converter to be transmitted to the controller. The benchmark frequency will be limited to the minimum propagation delay that can be achieved by the optocouplers. For example, if the propagation delay of the optocoupler is 500 ns then any on-time for the Buck converter that is less than 1 μs will cause the system variables to distort the PWM generation because the PWM will be comparing old current and voltage data to calculate the new duty cycle. This will introduce large instabilities into the circuit. The other impact the optocouplers will have will be on the accuracy of the system variables that they transmit to the control circuitry. With the linearity described in the Optocoupler Characterization Experiment Chapter, the data transmitted can be skewed by the non-linearities of the optocoupler transmission scheme. This will also cause incorrect duty cycles to be calculated and therefore cause instabilities in the Buck converter system.

Now that a conceptual understanding of the impact of the optocouplers on the converter system, the design procedures can be presented for the Buck converter system shown in Figure 5.1.

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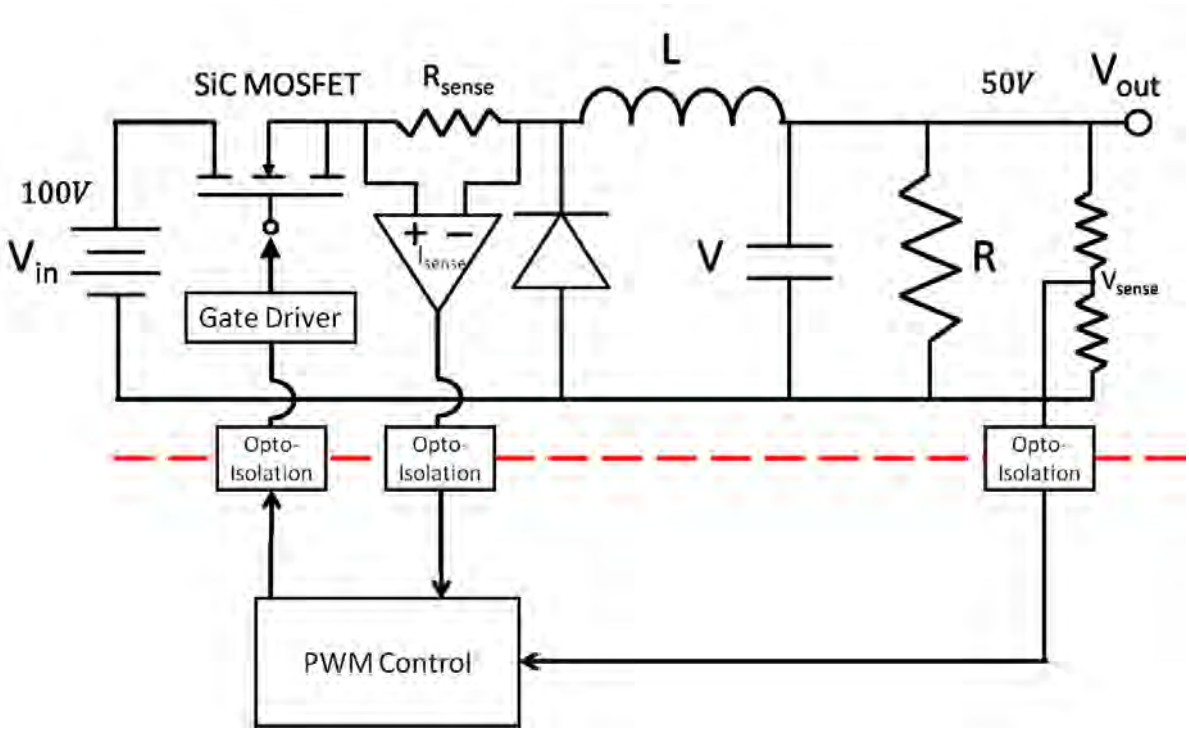


Figure 5.1 Block diagram of Buck converter system

The first part of the design method is to determine the Buck converter inductor and capacitor component values at the operating point that has been selected (100 V input, 250 W load at 50 V, and 85 kHz switching) and at steady-state (50% duty cycle with continuous current). The next step is to determine the steady-state values and waveforms of the inductor current and output voltage so that the sensing network for those system variables can be better defined. The sensing networks are determined next and then the transmission of these analog values through the isolation barrier with the correct optocoupler topology and optocoupler is described and the correct topology selected. The gain of the sensing networks needs to be set so that the PWM IC will generate a 50% duty cycle (allowing 50 V at this steady-state operating point) when the selected PWM IC compares the current and voltage. The final step is determining the digital transmission optocoupler topology to be used to send this PWM information to the gate driver to implement the calculated duty cycle by turning on and off the MOSFET with the correct timing.

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5.1.1 Open-Loop Buck Converter

The switch selection is the first step in determining the open-loop Buck converter. The switching transistor was chosen before the Buck converter was chosen as the application context to determine the impact of the optocouplers. The SiC MOSFET became commercially available with a rated blocking voltage of 1.2 kV and drain current of 20 A, and this is the switch that the gate driver is designed around [18]. The diode will also be a SiC device, a SiC Schottky diode rated at 1.2 kV and 20 A [25]. Also, since wide bandgap GaN optocouplers could be prototyped in this application context in future research, it is useful to have a fully wide bandgap system to take advantage of the wider temperature ranges these devices can handle compared to silicon and the other current optocoupler technologies.

The output filter is the combination of an inductor and capacitor. Since the steady-state operating point is known, these values are chosen based on the desired voltage, current ripple, and mode of operation. If the inductance chosen is lower than the critical inductance then the Buck converter will operate in discontinuous mode. The main factor for theoretical design is limiting the voltage and current ripple. A practical design also needs to consider the rated current and voltages as well as the equivalent series resistances (ESR). The two design equations for the current and voltage ripple are shown below.

$$\text{current ripple: } \Delta I = \frac{DV_{in}(1\text{-}D)}{f_s L} \qquad \textbf{(5-1)}$$

$$\text{voltage ripple: } \Delta v_c = \frac{V_{in}D(1\text{-}D)}{8f_s^2 LC} \qquad \textbf{(5-2)}$$

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Table 5.1 Available Inductor Values at Specific Current Ratings [26]

Current rating (A)	L (µH)
20	33
15	68
10	150
6.7	390

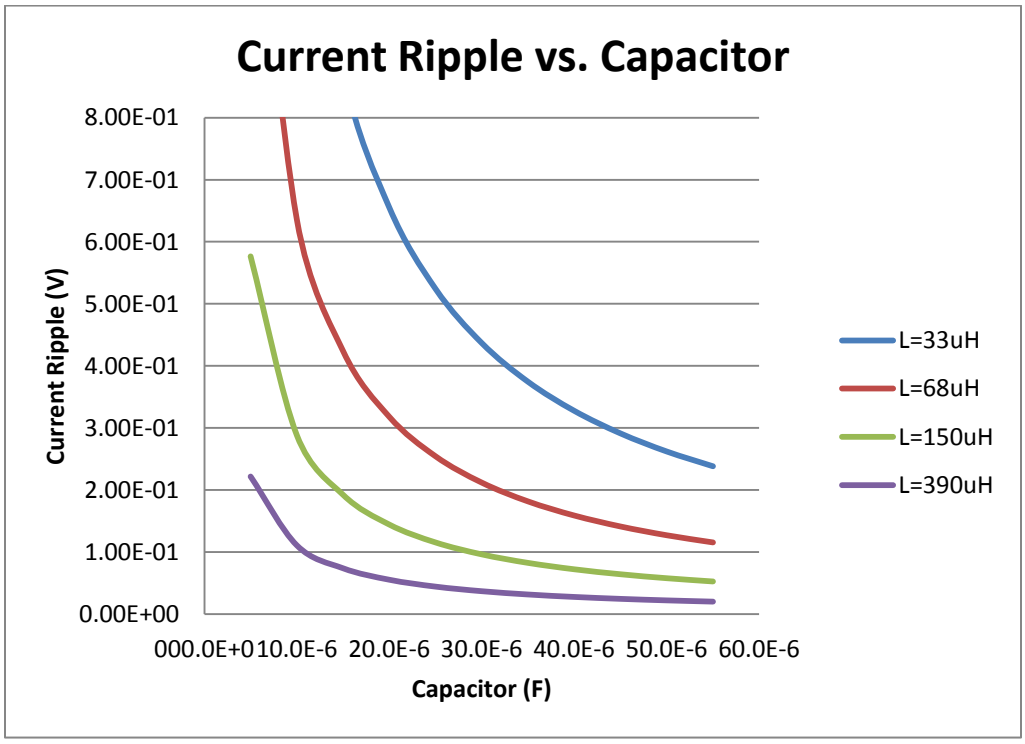


Figure 5.2 Current ripple vs. capacitor values for the different inductors available

Since the load current will be 5 A and the voltage will be 50 V, a desirable current ripple would be less than 100 mA (2%) and a voltage ripple less than 1 V (2%). Figure 5.2 shows a graph of the L and C values that correspond to a range of ripple currents.

Table 5.1 shows the rated amperage of available inductances. The correct choice is an inductance value of 390 µH because there will be 5 A flowing. The only available inductors range from 390 µH and smaller; and the smaller the inductance the larger the current and voltage ripple as seen in

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Figure 5.2. With the inductor selected a capacitor value of 10 µF is chosen which is equivalent to a 100 mV voltage ripple and 750 mA current ripple. The current ripple is larger than desired but as seen in

Table 5.1 a larger inductor cannot be used, and a larger capacitance would increase the footprint of the final PCB. An electrolytic capacitor is used because of its size at a 100 V rating. Figure 5.3 shows the simulation validating the calculations. The current ripple is seen to be from 4.76 A to 5.51 A, which corresponds to the 750 mA that was calculated. The voltage ripple cannot be seen because at 50 V the scale is too large to see 100 mV ripple. Note that as the frequency is increased the output filter will not be changed, so the ripples will decrease.

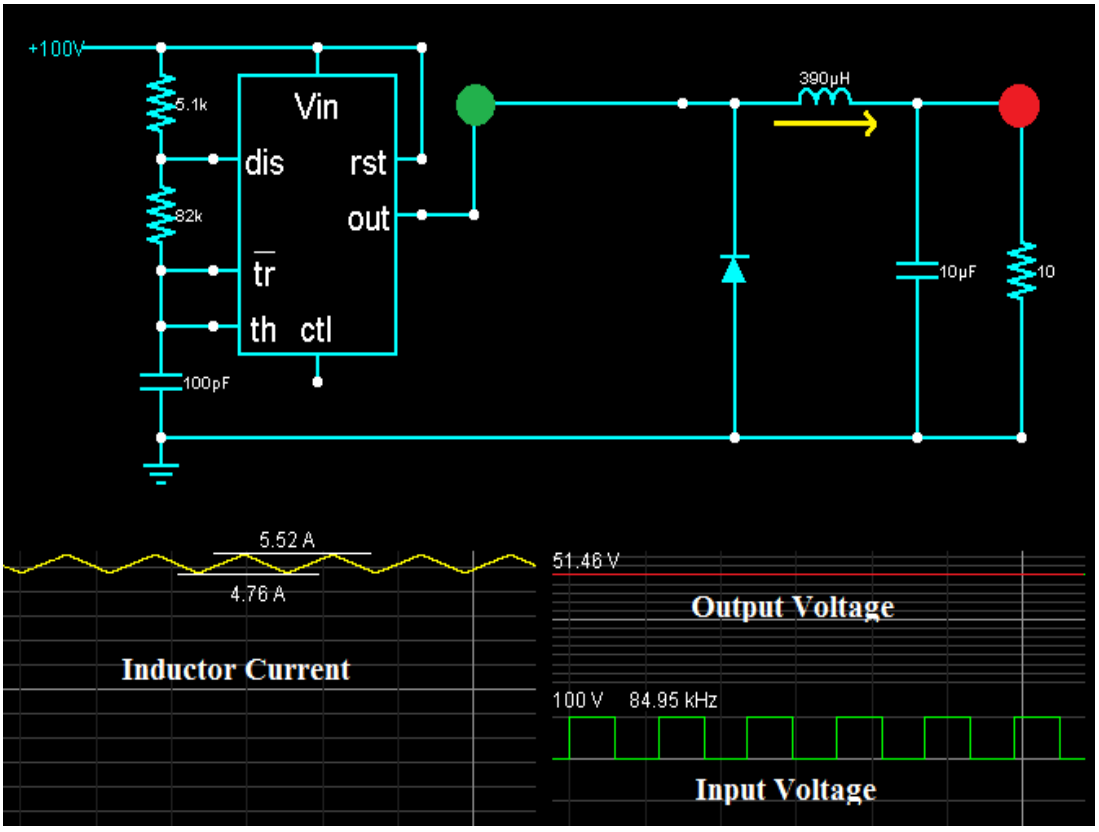


Figure 5.3 Open-loop Buck converter simulation verification, inductor current (yellow), output voltage (red), input voltage (green)

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Now that the open-loop Buck converter components have been chosen, the sensing networks implemented in the system can be discussed and designed. For this design to be current-mode control the inductor current and output voltage need to be sensed, scaled, and sent to the controller [15]. For the design to be optically isolated these sensed system variables need to be transmitted through optocouplers from the Buck converter side to the controller side of the circuit. The first step in the design will be to break apart the current sensing network, design it, and then focus on the output voltage sensing network.

5.1.2 Current Sensing Inner Feedback Loop

The current feedback design first determines how to sense the current, then to transmit the signal through the isolation barrier and, finally add slope compensation. There are multiple current feedback sensing schemes, and for current-mode control it depends on what type of current measurement is needed. A simple method is to measure the current in the inductor when the switch is off. This configuration is shown in Figure 5.4 and is called valley current-mode control [27].

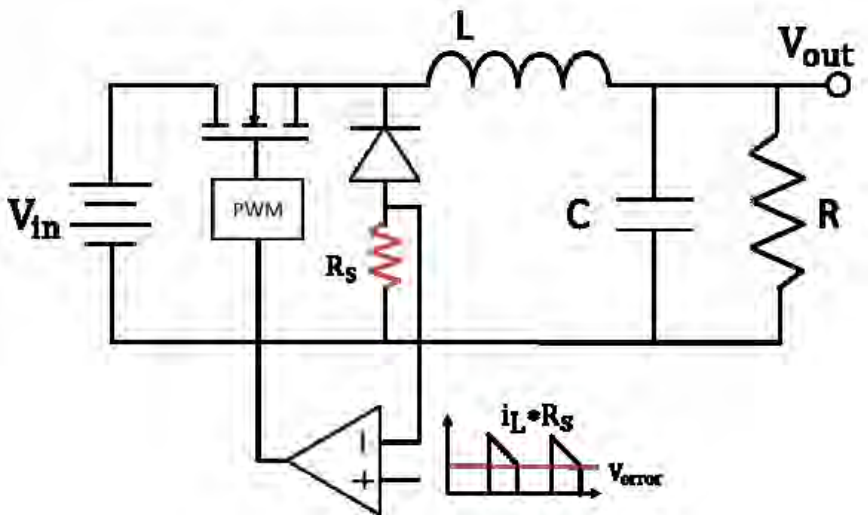


Figure 5.4 Valley current mode (sense resistor placement emphasized) [27]

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A small sense resistor is placed between the diode and ground and the sensing network can be referenced to the Buck converter's ground, and a specific current sensing differential amplifier measures the small voltage difference between the two terminals of the resistor. This is not desired for this design because this type of sensing network could be developed without optocouplers since the reference of the sensing circuitry would not be floating at a high voltage. This method controls the on-event of the high-side MOSFET by the sending of an on-control signal to the gate driver when the sensed current signal crosses the error voltage signal as shown in Figure 5.4. This sensing method only captures the downward slope of the current, it cannot protect against overcurrent because of too heavy of a load being driven [27].

Peak current-mode control is chosen for the two reasons valley current-mode control could not be used. It requires high-side current sensing with a floating ground reference and it has inherent overcurrent protection. The same type of sensing resistor in the valley current-mode is placed between the source of the MOSFET and the inductor as shown in Figure 5.5. This sensing method uses a current sense amplifier referenced to the source of the MOSFET to measure the voltage difference the output current will cause over the sense resistor. This method captures the upward current slope and controls the off-event of the MOSFET by sending an off control signal to the gate driver whenever the current intersects the error voltage [27].

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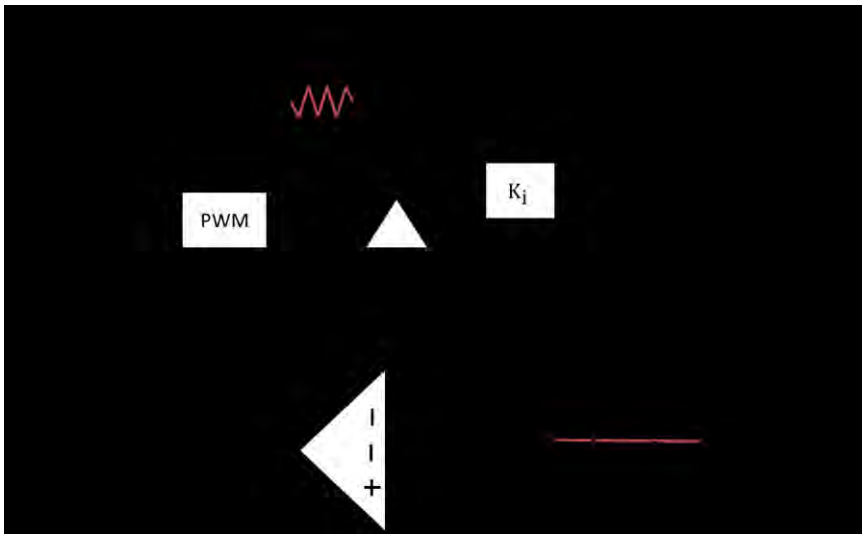


Figure 5.5 Peak current mode control (sense resistor placement emphasized) [27]

The addition of an optocoupler allows signals to be sensed and transmitted to the low voltage control circuitry even if the floating, high-side, reference of the sensed signal is much greater than the ground of the control circuitry[28]. This is defined as the isolation that the optocoupler can provide. For this design, the sensed signal is referenced to a signal that floats between the 100 V input voltage and 50 V output voltage. The control circuitry is at zero volts. If these two circuit grounds were directly connected the control circuitry would be destroyed. Now that an optocoupler is used the input voltage could be as high as the withstanding voltage of the optocoupler.

Now a current sensing network needs to be designed to measure the voltage drop across the sense resistor and send it to the analog transmission optocoupler topology to be sent to the controller circuitry through the isolation barrier. Two key things need to be kept in mind while designing the current sensing network, the gain of the sense network and the slope of the sensed signal. The slope information needs to be known to calculate the amount of slope compensation (as discussed in the background section) needed, and the gain will be factored in because it changes the original slope of the current signal.

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5.1.3 High-Side Current Sensing Design and Analog Current Transmission Optocoupler Topology Selection

The actual method of obtaining and transmitting the current sensed signal to the control circuitry follows. Figure 5.6 shows the overall design for completeness, while each subsection's design and selection will be discussed individually [28]. The first step for sensing the peak current is sensing the current as an analogous voltage signal that is obtained from the sense resistor.

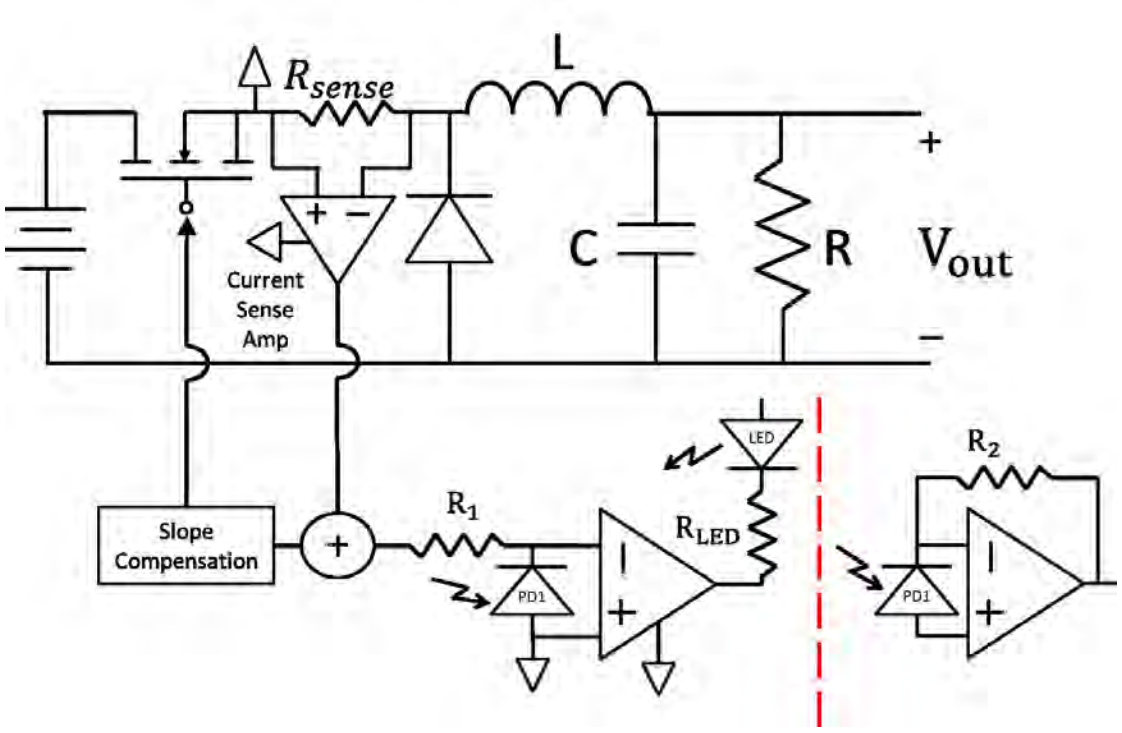


Figure 5.6 Current sense scheme implementing peak current mode scheme with analog transmission optocoupler [28]

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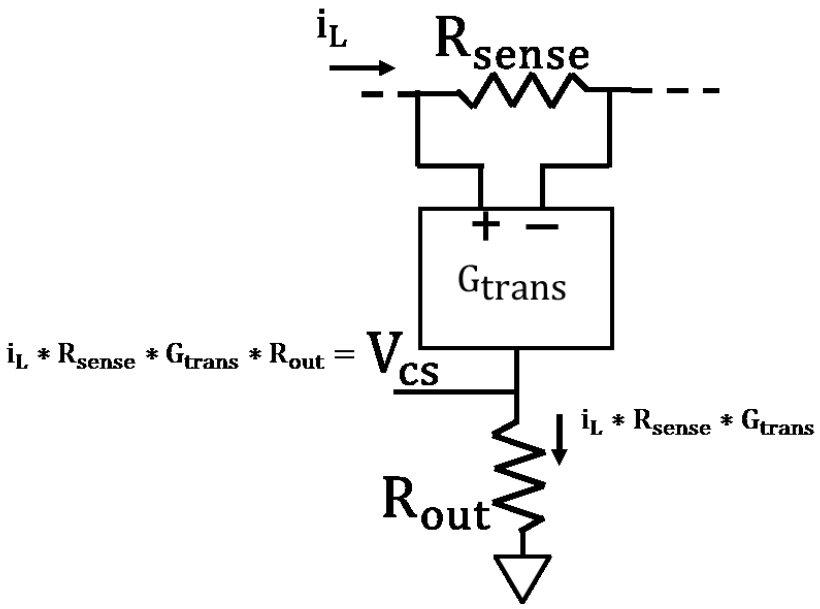


Figure 5.7 Simple block diagram of current sense amplifier [29]

The current sense amplifier block diagram is shown in more detail in Figure 5.7 [29]. It senses the voltage drop over the sense resistor and multiplies it by a transconductance gain parameter, G_{trans}, to produce a current through the output. The output is connected to the floating ground reference through a resistor (R_{out}) which converts the output current of the sense amplifier into a voltage again [28]. Keeping account of the key parameters, overall gain and slope, the gain from the current flowing through the sensed resistor to the voltage at the output of the current sense amp is shown below.

$$\frac{V_{cs}}{i_L} = G_{csamp} = R_{sense} * G_{trans} * R_{out} \quad \textbf{(5-3)}$$

$$\text{Slope: } S_n = \frac{G_{csamp} * (I_{L2} - I_{L1})}{t_{on}} \quad \textbf{(5-4)}$$

I_{L2} and I_{L1} are the minimum and maximum currents due to the current ripple around the 5 A steady state value. S_n is the slope of the current signal after the gain of the sensing network. This will be used in the next section to calculate the slope compensation requirements.

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The next step is adding slope compensation to the sensed current signal, as discussed in the background chapter for current-mode control, to compensate for the sub-harmonic oscillations. There are numerous ways to generate a ramp signal to add to the current sense signals. Some methods use the oscillator in the PWM IC to generate a triangle wave with the correct slope and sum the current sense signal together with it. This method has been proven to load the oscillator pin enough to cause the oscillator frequency to shift [30]. Another inherent oscillator in the system is the gate driver output. Since this output drives a large amount of current a small amount (micro-amp range) can be used to charge a specifically sized capacitor to generate a ramp signal [31]. Another advantage to this is that this signal is on the high-side so it can be directly summed with the voltage output of the current sense amp since they are referenced to the same high-side floating ground. This solution is shown in Figure 5.8.

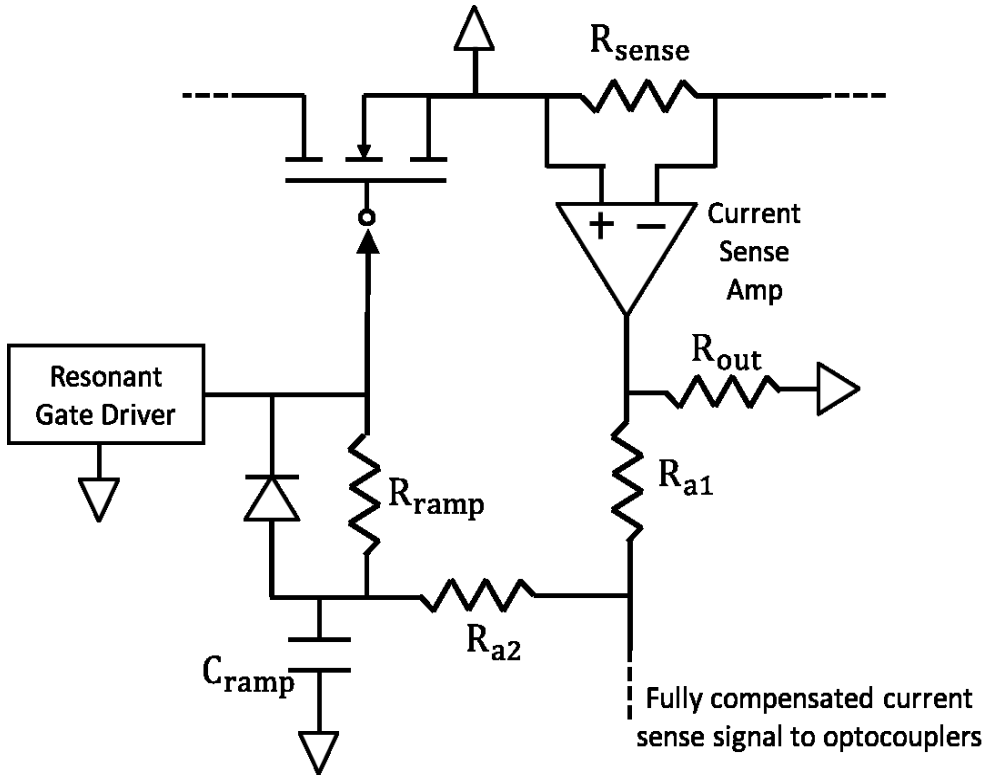


Figure 5.8 Adding ramp compensation on high-side of isolation barrier [31]

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The gate signal output goes high turning on the MOSFET, and current flows through R_{ramp} which charges C_{ramp} to a specific voltage V_{ramp}. These two components are chosen for a desired slope and minimal loading of the gate driver. R_{a1} and R_{a2} form a voltage divider to resistively add the output of the current sense amplifier with the slope compensation generated by C_{ramp} (S_{ramp}). R_{a1} and R_{a2} are determined by the desired amount of slope (S_{comp}) needed to stabilize the current signal. This amount is determined by a value titled m_c, which represents how much slope compensation is supplied [31].

$$m_c=1+\frac{S_{comp}}{S_n} \quad \textbf{(5-5)}$$

With an m_c of one there is no external ramp supplied. The factor that determines the amount of external ramp to be added is the value of Q, the quality factor [31].

$$Q=\frac{1}{\pi\left(m_c*D'-0.5\right)} \;;\; D'=(1-D) \quad \textbf{(5-6)}$$

When there is no external slope and the duty cycle is 50% (0.5) the Q will become infinite, representing the sub-harmonic oscillations of the current-mode controlled Buck converter [31], [32]. For a stable system, slope compensation corresponding to a value of m_c greater than one needs to be added to keep Q below one. This corresponds to the design equations for R_{ramp}, S_{ramp}, C_{ramp}, m_c, and S_{comp} [31].

$$\text{For minimal loading: } R_{ramp}=\frac{V_{gate,supply}}{I_{ramp}};50\ \mu A<I_{ramp}<200\ \mu A \quad \textbf{(5-7)}$$

$$C=I\frac{dt}{dv}=\frac{I_{ramp}*t_{on}}{V_{ramp}} \quad \textbf{(5-8)}$$

$$S_{ramp}=\frac{V_{ramp}}{t_{on}} \quad \textbf{(5-9)}$$

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$$m_c = \left(\frac{1}{\pi} + 0.5\right)\left(\frac{1}{D'}\right) \quad \textbf{(5-10)}$$

$$S_{comp} = (m_c - 1)S_n;\ \text{remember } S_n = \frac{G_{csamp} * (I_{L2} - I_{L1})}{t_{on}} \quad \textbf{(5-11)}$$

Once the desired amount of compensation slope is calculated, the values of R_{a1} and R_{a2} can be calculated to add the right amount of the slope from the ramp to the current sense information [31].

$$\text{division ratio, } d_r = \frac{S_{comp}}{S_{ramp}} = \frac{r_{a1}}{r_{a1} + r_{a2}} \quad \textbf{(5-12)}$$

Something to note is that not only is the ratio of R_{a1} and R_{a2} important, but their respective size is too, because if they are two small they will draw more current than the ramp circuit or current sense amplifier will be able to supply. Also, if they are too large they will not be able to supply the correct amount of current for the next stage, the analog transmission optocoupler topology. Figure 5.9 shows the behavioral model of the current sensing circuit that is simulated to validate the design approach chosen. The simulation applies a signal to the current sensing resistor that emulates a 5A current signal. The result shows that the slope of the output signal can be correctly compensated with the correct values of the addition circuit chosen.

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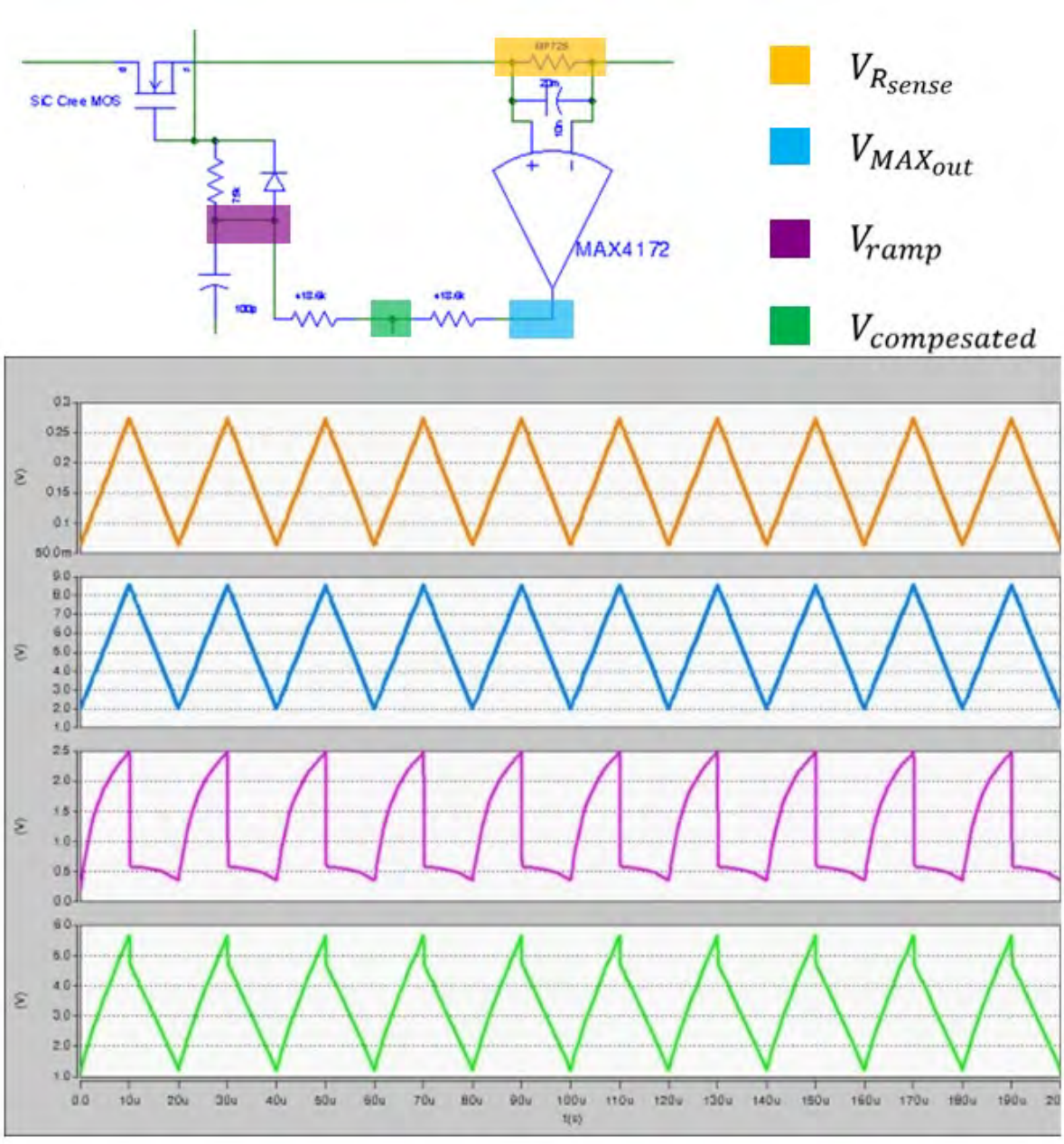


Figure 5.9 Simulation results of the current sensing network; input (yellow), output of differential sensing amplifier (blue), slope generation (purple) compensated signal consisting of output of sense amp added with compensation slope (green)

The fully compensated current signal on the high voltage isolated side of the circuit now needs to be transmitted to the low voltage control circuitry with the optocoupler. Choosing which analog

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topology and which optocoupler to use depends on which topology and optocoupler are the fastest and most accurate for transmitting the sensed current signal, which is determined in the Optocoupler Characterization Experiments Chapter to be the topology with a feedback servo-diode that removes the non-linear CTR parameter from the transfer function. This optocoupler topology is chosen because it can linearly track the input voltage (analogous to the sensed current) applied to the photodiode input. This means that small changes of light intensity radiating from the LED due to the sinusoidal sensed signals must be amplified by the photodiode and output scheme linearly and without added propagation delay. Linearly transmitting the signal with a very small propagation delay between the input and the output are the two restricting parameters that helped determine the optocoupler topology that will be used. Although the open-loop analog transmission topology had a smaller propagation delay by 100 ns, this small value would increase because the output voltage of the current sensing network would require a large output resistance. This was seen to increase the propagation delay by as much as 1 μs in the Optocoupler Experimental Chapter. This effect disqualifies the open-loop topology. How the propagation delay will affect the Buck converter and the maximum switching frequency has already been discussed and the final results will be presented when the full Buck converter system has been designed and implemented. With a final decision made for the current sensing optocoupler scheme, the design equations for transmission are described below [12], [28].

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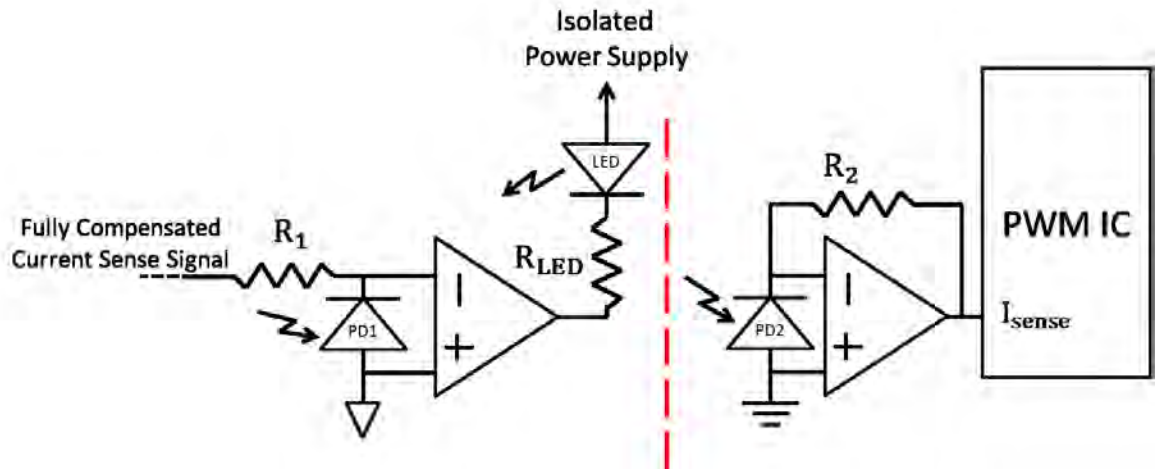


Figure 5.10 Analog transmission optocoupler scheme for current sensing transmission to control IC [12]

The topology shown in Figure 5.10 is discussed in the background section and the design equation is just the transfer function presented in Eq. (2-14) and rewritten in Eq. (5-13). The design decision for the value of R_{LED} is a little more complex because it does not determine any current in the circuit. It will affect the power consumption and also if it is too large the output voltage of the first op amp will not be able to swing far enough and will not provide the correct LED biasing voltage, as shown in Chapter 4.

$$G_{opto}=\frac{V_{out}}{V_{in}}=\frac{R_2}{R1} \qquad \textbf{(5-13)}$$

It is also imperative to bias the LED, PD1, and PD2 correctly. This will be done for the specific parameters of the optocoupler selected. The final value selections for the current sensing network can now be discussed. The current sense amplifier is chosen to be the MAX4172 which allows all the variables in Eq. (5-3) for G_{csamp} to be determined [29]. It can handle a maximum input voltage of 175 mV. So R_{sense} is chosen to be 20 mΩ so that at 5 A the voltage drop will be 100 mV. This leaves the selection of R_{out}. The gain of this transconductance amplifier is 10 $\frac{mA}{V}$, so at 100 mV the current through

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the sense resistor is 5 A and the output current of the sense amplifier is 1 mA. The selection of the value of R_{out} is a very big decision. If the optocoupler's transmission gain is set to one, then the value of R_{out} will set the voltage that is seen by the comparator. This is where scaling the sensed current plays a crucial role. For this design the switch needs to be turned off at 5 A (the maximum allowed current), the value of the analogous voltage of the sensed current that will cause the PWM to generate an off-command to the gate driver at this current level needs to be understood. Once this is known the parameters can be chosen to produce this output when 5 A is present on the input to the sensing network. This voltage value is determined by the PWM IC that is chosen; for this design a HV9123 will be optimal because it has simple implementation and allows for a fully analog control system which simplifies the design of the control circuitry interface to the optocouplers [24]. This PWM IC will turn off the switch whenever 1.3 V is seen at the current sense pin. Finally, R_{out} is determined to be 1.3 kΩ so that at 5 A of current flowing through R_{sense}, 1.3 V will be at the output of the current sense amplifier. Now G_{csamp} can be found.

$$G_{csamp}=R_{sense}*G_{trans}*R_{out}=20m*10m*1.3k=0.26 \quad \textbf{(5-14)}$$

So the slope of the inductor reflected to the output of the amplifier can now be calculated along with the rest of the current sensing network. The values of I_{ramp} and V_{ramp} are chosen to be 100 µA and 1.3 V, respectively, and R_{a1} is chosen to be 10 kΩ.

$$S_n=\frac{G_{csamp}*(I_{L2}-I_{L1})}{t_{on}}=\frac{0.26*(5-4.75)}{5.88\mu}=11\ \frac{mV}{\mu s} \quad \textbf{(5-15)}$$

$$m_c=\left(\frac{1}{\pi}+0.5\right)\left(\frac{1}{D'}\right)=\left(\frac{1}{\pi}+0.5\right)\left(\frac{1}{0.5}\right)=1.64 \quad \textbf{(5-16)}$$

$$S_{comp}=(m_c-1)S_n=(1.64-1)*11\ \frac{mV}{\mu s}=7\ \frac{mV}{\mu s} \quad \textbf{(5-17)}$$

$$R_{ramp}=\frac{V_{ramp}}{I_{ramp}}=\frac{1.3}{100\mu}=150\ k\Omega \quad \textbf{(5-18)}$$

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$$C=\frac{I_{ramp}*t_{on}}{V_{ramp}}=\frac{100\mu*5.88\mu}{1.3}=440\text{ pF} \quad \textbf{(5-19)}$$

$$S_{ramp}=\frac{V_{ramp}}{t_{on}}=\frac{1.3}{5.88\mu}=227\frac{mV}{\mu s} \quad \textbf{(5-20)}$$

$$d_r=\frac{S_{comp}}{S_{ramp}}=0.466 \quad \textbf{(5-21)}$$

$$r_{a2}=\frac{r_{a1}-r_{a1}d_r}{d_r}=11.5k\Omega \quad \textbf{(5-22)}$$

Now the input to the analog transmission optocoupler is known to be 1.3 V when the current through the sense resistor is 5 A. We want this current to be sent across the isolation barrier with unity gain. The optocoupler chosen in the Optocoupler Experimental Chapter is the HCNR201 [12]. It has a nominal CTR of 0.2%. The nominal current through the LED is about 10 mA, but for this design the operating point will be set around 8.5 mA because of the increase performance seen in the Experimental Chapter without increasing the power consumption too much. This means the photodiode current will need to be about 40 µA when the input is at 1.3 V. This operating points sets R_1 and R_2 [12].

$$R_1=R_2=\frac{V_{in}}{I_{pd1}}=\frac{1.3}{40\mu}=32.5\text{ k}\Omega \quad \textbf{(5-23)}$$

Now that the analogous voltage of the sensed current is on the control side of the system at the current sense pin of the PWM IC, the corresponding sensed output voltage must be found and the voltage sense network must be designed.

5.1.4 Voltage Sensing Outer Feedback Loop

The voltage pin of the PWM IC needs to be at 4 V when the output voltage is at its nominal value of 50 V in order to be compared correctly with the sensed current signal and produce the nominal 50% duty cycle [24]. This criterion determines that the overall gain of the voltage sensing system needs to be 0.08. The voltage on the output is sensed with a simple voltage divider, shown in the design scheme for

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the voltage sensing network in Figure 5.11, using two resistors chosen to output a voltage equal to the voltage required by the PWM IC referenced above which will be called V_{th} in the design equations.

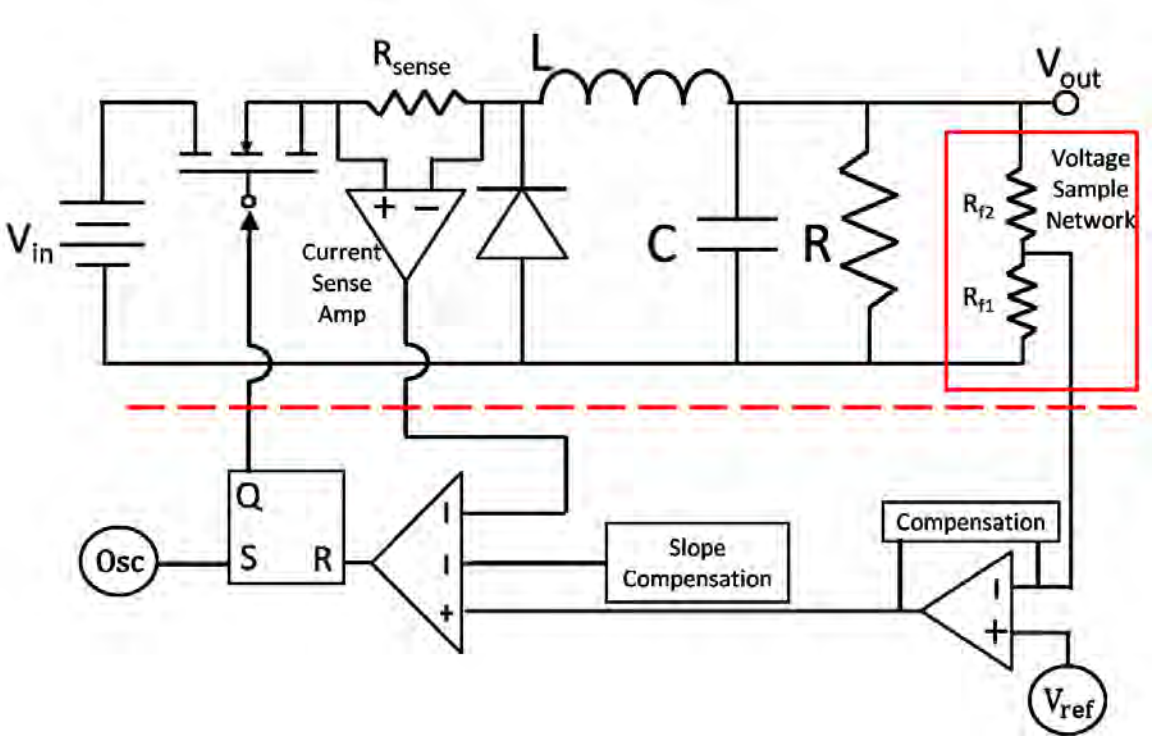


Figure 5.11 Full design scheme for voltage sense network and placement within overall current-mode control scheme

If the load changes then the output voltage will start to change. This will cause an error voltage to change (positive for smaller output voltages and negative for larger output voltages) which in turn changes the duty cycle (compensating the amount of energy transferred from the inductor to the output) until the error voltage is zero again and V_{th} is back to its nominal value of 4 V [14]. The voltage divider design equation can now be determined.

$$\frac{R_{f1}}{R_{f2}+R_{f1}}=0.08 \qquad \textbf{(5-24)}$$

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The output of this voltage divider is the input to the analog transmission topology. Obviously the feedback analog topology presented in Chapter 4 will be the best design because of its accuracy and speed. This is the first assumption, but would be an incorrect design decision for a couple reasons. First, the voltage signal does not change as much as the current signal; it is very well defined and stays within a small range of voltage levels because the voltage divider causes a very small fraction of the output voltage to be applied to the input of the transmission circuitry. Also, the current sensing feedback topology needs a dedicated isolated supply for the input stage. This is okay for the current transmission because one is already available due to the need of the high-side gate driver. The voltage sensing network cannot use this isolated supply. If the same supply is used for the current sensing signal the voltage sense scheme will be referenced to a floating ground (specifically, the source node of the switch), but the voltage sampling network is referenced to the Buck converter ground. If the current sense network configuration is used the LED will be biased completely incorrectly, more easily seen in Figure 5.12.

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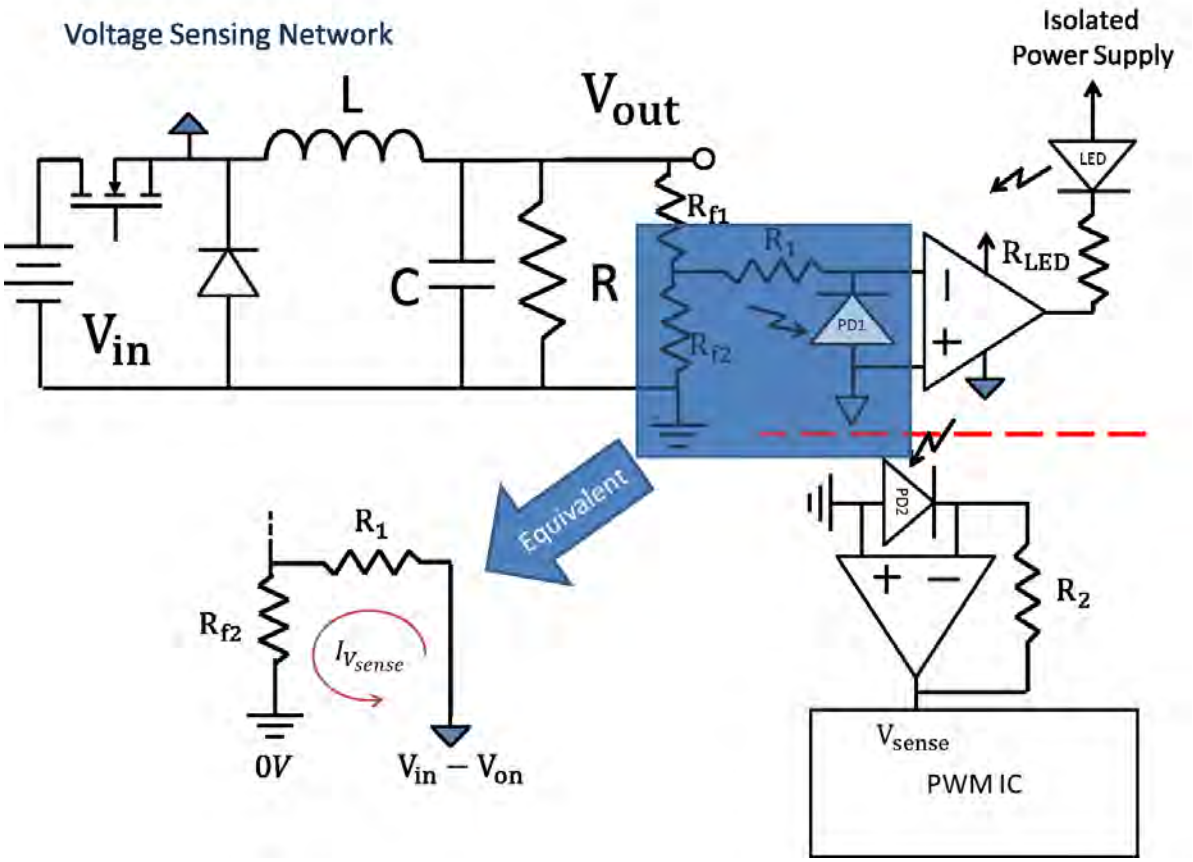


Figure 5.12 Incorrect grounding of voltage sensing network optocoupler

Because the voltage sensing circuit will mostly be a dc value that only fluctuates during transients, an open-loop analog transmission topology can be used by operating in the plateau region described in the experimental results of this topology in Chapter 4. This is a benefit so that another isolated voltage supply does not have to be implemented. Another thing to note is that the different optocouplers are used between the two sensing networks will not have a matched propagation delay (reference the propagation delay results from the two topologies). There will be mismatch of propagation delays because of processing differences and topology selection. With different propagation delays the information at the PWM IC would not accurately represent the actual circuit conditions. . Two facts allow for this mismatch to be present in the system without impeding the

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operation of the Buck converter. The first is that the output voltage does not change unless the load changes, and other than the initial transient the time scale is orders of magnitude slower than the current signal cycle to cycle change. This difference in time scale is much larger than a 100 to 200 ns mismatch in propagation delay. The second fact is better explained qualitatively Figure 5.13. During any transient change that takes place on the same time scale as the current signal the instability in the duty cycle introduced by the mismatch will be quickly compensated over a short amount of cycles. One final note, it is still possible for the mismatch to affect the operation. If the mismatch does cause a problem in the operation of the Buck converter then it will become another aspect of the optocouplers impact on the full system.

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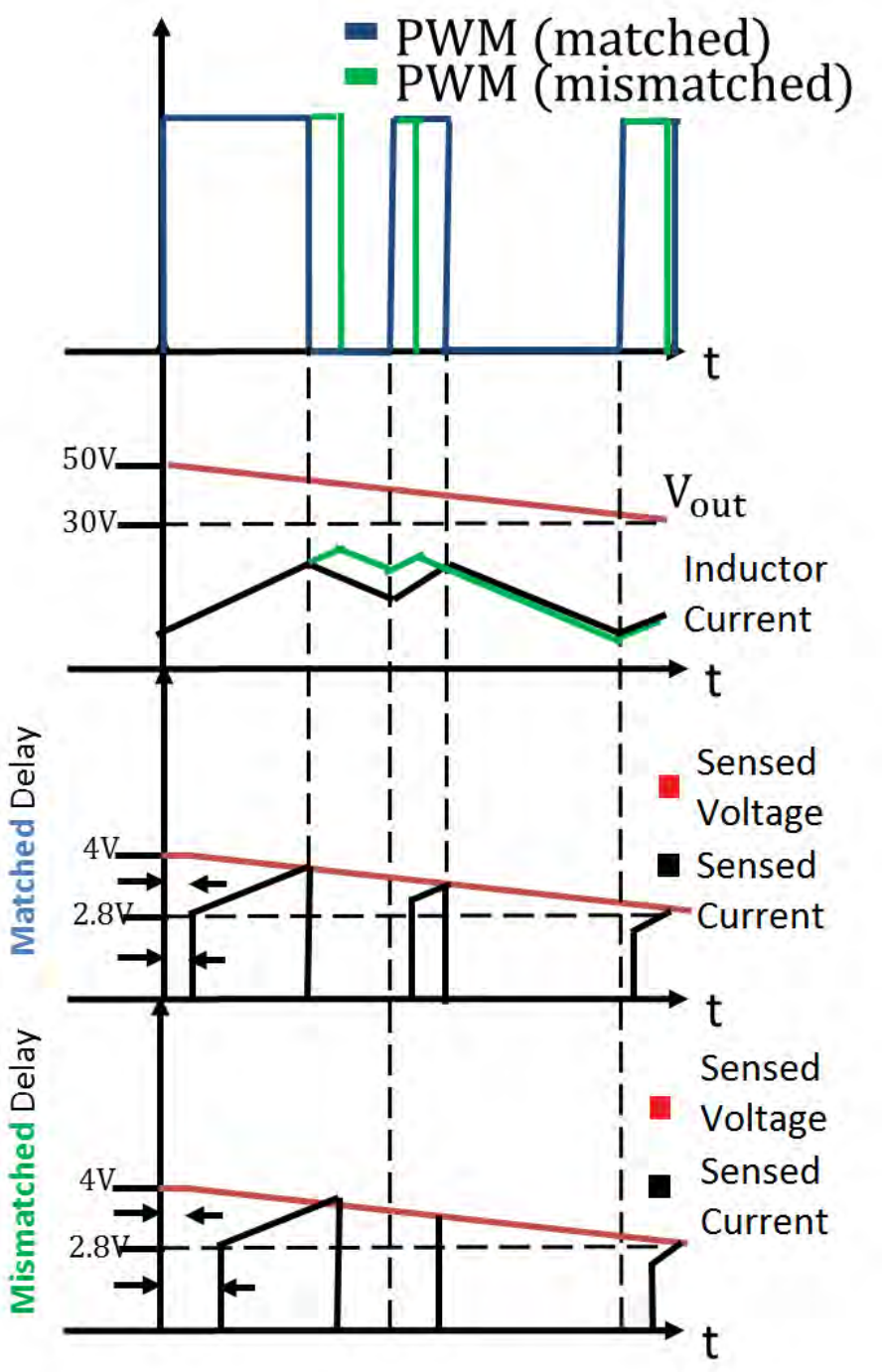


Figure 5.13 Graphical representation of mismatched delay causing different results over multiple cycles (assumed transient causing steady decrease in output voltage)

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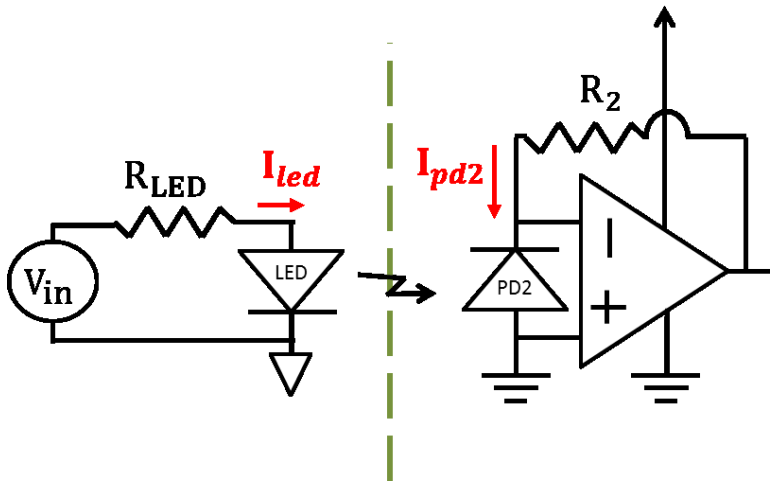


Figure 5.14 Open-loop analog transmission used so the side referenenced to power gound does not need isolated supply

Figure 5.14 shows the open-loop analog transmission topology to be used with the HCNR201.

The new steady state design equations will now change for the correct topology, shown in Figure 5.15.

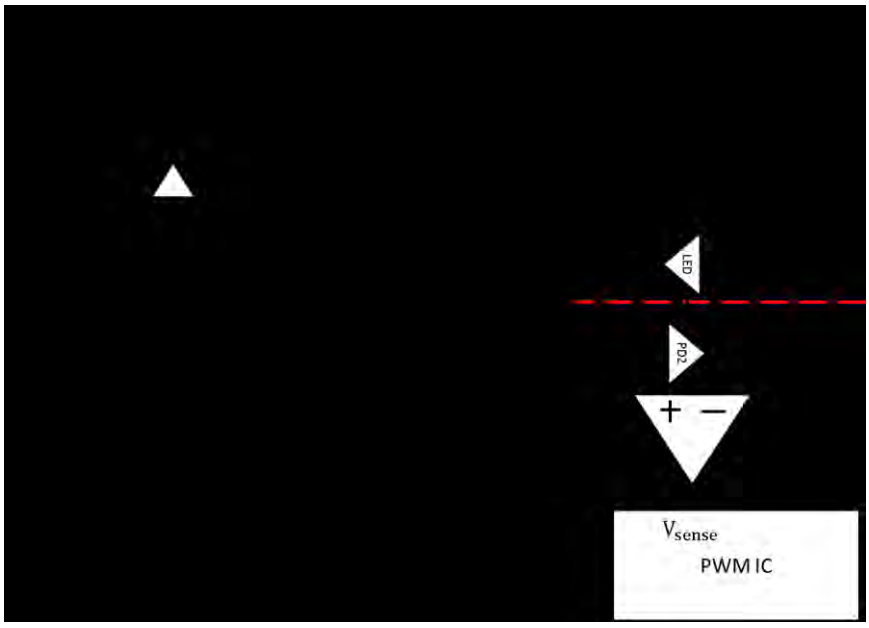


Figure 5.15 Final voltage sensing network detailed schematic

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The voltage divider in the original circuit is now no longer a voltage divider because R_{f2} is in parallel with the equivalent resistance of the LED and R_{LED}. Also, the transfer function of the optocoupler topology has CTR in it. So the new design equations need to be defined. Since the solution must be found for the point at which the output is at 4 V a biasing point for the optocoupler is chosen to be the nominal value of 10 mA which is 1.55 V drop across the LED [14]. With an operating point set, the LED is converted to an equivalent resistance. The LED resistance and the biasing resistor R_{LED} are in series and both are in parallel with R_{f2}. Now the design equation can be found for the nominal output of 4 V, which is what the voltage sense pin of the HV9123 needs when the output voltage is at its nominal value of 50 V.

$$I_{V_{sense}}=\frac{V_{out}}{R_{f1}+R_{f2}\,||\left(R_{LED}+\left(\frac{V_{LED}}{I_{LED}}\right)\right)}=I_{LED}+\frac{V_{in}}{R_{f2}} \quad \textbf{(5-25)}$$

$$V_{out}=50V,\ V_{in}=4V,\ V_{LED}=1.55V,\ I_{LED}=10\ mA \quad \textbf{(5-26)}$$

$$R_{led}=\frac{V_{in}-V_{led}}{I_{LED}}=245\ \Omega \quad \textbf{(5-27)}$$

$$\frac{50}{R_{f1}+\frac{400*R_{f2}}{R_{f2}+400}}=10m+\frac{4}{R_{f2}} \quad \textbf{(5-28)}$$

This system is easier if it is solved graphically. The best solution for this design equation is found when both R_{f1} and R_{f2} are equal to 4.2 kΩ. Once this is set the transfer function for the open-loop analog transmission optocoupler can be determined when a nominal CTR is 0.2%.

$$R_2=\frac{R_{LED}}{CTR}*\frac{V_{out}}{V_{in}}=\frac{245}{0.002}\left(\frac{4}{4}\right)=122.5\ k\Omega \quad \textbf{(5-29)}$$

This size of an output resistance increases the propagation delay as seen in the Optocoupler Experimental Chapter. This is an acceptable design trade-off for two reasons. The value of R_{LED} is small enough to compensate some of that propagation delay increase, and the speed of the voltage signal

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transmission is not as important as the current sensed signal. Cycle to cycle it stays constant at steady state and is regulated more so by the inductor current. Also, a large output resistance is needed to get the required gain which is the most important for accurately transmitting the output voltage information.

The biasing limits of this circuit need to be determined. This will determine how much the output voltage can change before this sampling network and transmission network will not be biased correctly. Figure 5.16 shows a graph with output voltage of the Buck converter as the x-axis and the output voltage of the transmission network (input voltage to the PWM voltage sense pin) and the LED current plotted as the y-axis. R_{LED}, R_{f1} and R_{f2} are constant while the equivalent resistance of the LED changes with the changing I_{LED} (CTR is held constant).

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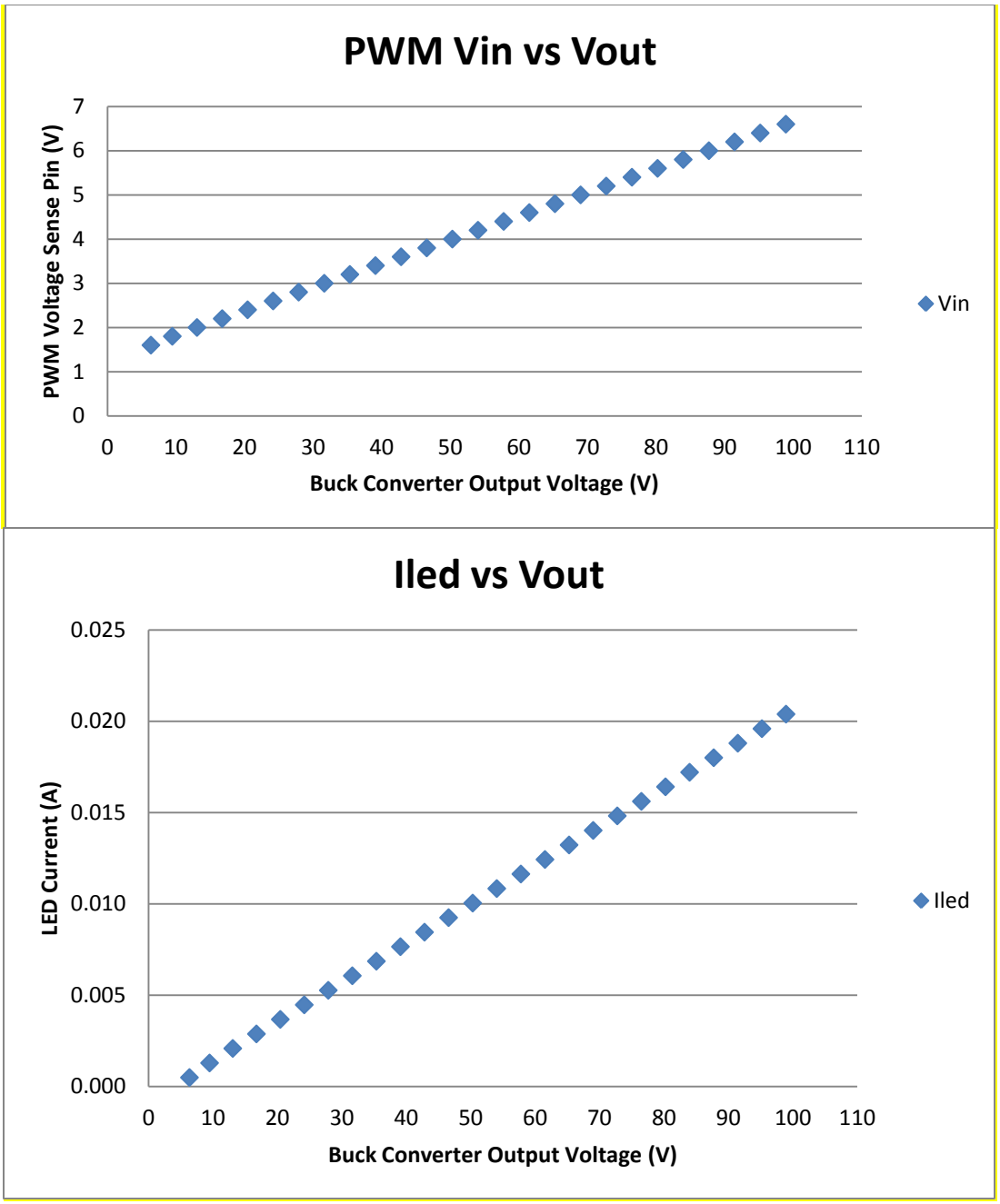


Figure 5.16 PWM voltage sense pin and input LED current versus Buck converter output voltage

The graphs above show that the range of operation for this circuit is from 9 V of the output voltage of the Buck converter to 100 V and greater. The LED current stays within a range of 3 mA to 20 mA which will cause some non-linear responses on the output of the open-loop analog transmission

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topology (operation outside of the plateau region). With an R_{LED} value of 275 Ω this region starts at an LED current of 16 mA which corresponds to an 80 V output. This shows that the inabilities of this optocoupler topology to have a constant voltage gain over a range of inputs will affect any transient voltages below 80 V. This trade-off for a decreased propagation delay with this value of R_{LED} is acceptable though. At the nominal 50 V output the open-loop topology will transmit 4 V to the PWM correctly. If the output voltage droops the CTR will decrease causing the voltage gain to decrease but still reflect a decreasing output voltage. This is not a desired effect for a transient drop in the output voltage, but for an output voltage spike the CTR will increase and increase the voltage gain. This will actually increase the response of the control circuitry to dampen the output voltage by decreasing the duty cycle.

Now system variables, the inductor current and output voltage, have been sensed and scaled to the correct values needed by the PWM IC to set the steady-state parameters for the current (5 A) and output voltage (50 V). Now the PWM IC needs to be analyzed more in-depth. The biasing of the IC must be correctly implemented, along with determining how to send the PWM output to the gate driver through the isolation barrier.

5.1.5 Control Circuitry

The PWM IC has been determined to be the HV9123 [24], and now it must be set up properly. This includes biasing the chip, setting the internal oscillator to the correct frequency, using the start-up function correctly, and correctly connecting the compensation pin. The pin diagram is shown in Table 5.2.

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Table 5.2 Pin Diagram for HV9123 [24]

Pin #	Description	Pin #	Description
1	+VIN	9	Oscillator In
-		10	Discharge
-		11	VREF
4	Current Sense	12	$\overline{\text{Shutdown}}$
5	Output	13	Reset
6	-VIN	14	Compensation
7	VDD	15	Voltage Sense
8	Oscillator Out	16	Bias

The values for the different external components are shown in Figure 5.17 [26]. The start-up functionality is generated by setting the PWM to a maximum duty cycle of 95% when there is no input applied to the Buck converter. At start up this will allow current to flow limited to the 5 A setting until the circuit is in steady state where it will operate at 50% duty cycle. The compensation is not added to stabilize the poles created by the output filter of the Buck converter because only steady state operation will be analyzed. Also, unlike most systems, the response time will not be determined by the compensation network but by the optocouplers propagation delay.

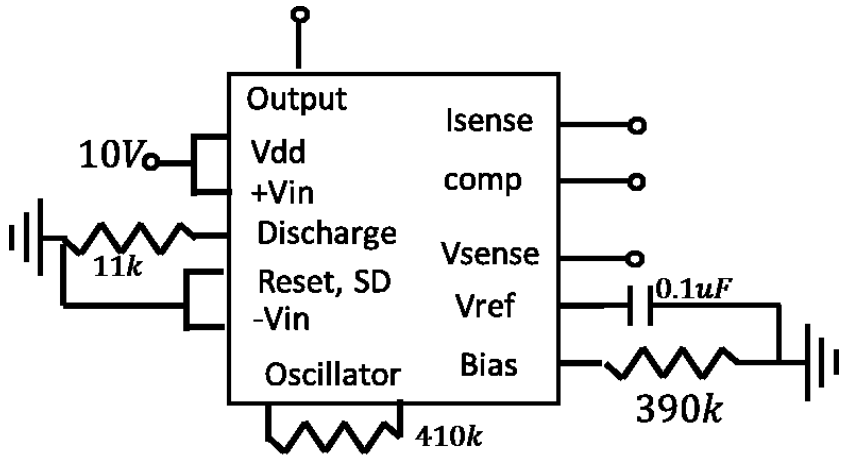


Figure 5.17 External components for HV9123 operation at 85 kHz and 95% maximum duty cycle [24]

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The output of the PWM IC is a PWM signal. This signal can only source ±10 mA and is a single square wave which needs to be converted into a separate on- and off-pulse as shown in Figure 5.18. These pulses are then buffered and sent to the digital transmission optocouplers to be sent to the high-side gate driver.

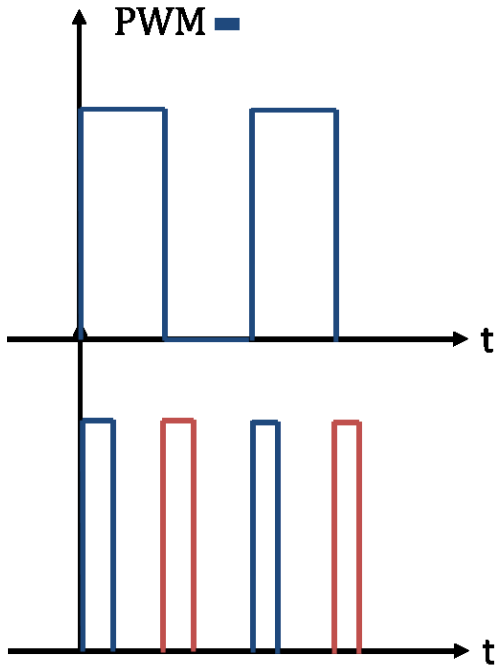


Figure 5.18 Converting PWM signal on top to two separate on- and off-pulses on the bottom

The pulse circuitry is best explained when focusing on one pulse. The design will focus on the on-pulse. First of all, the on-pulse needs to be an exact duration which depends on the rise time of the gate driven by the high-side gate driver. This precise pulse duration is created by a switched capacitor scheme and a comparator. Figure 5.19 shows this topology.

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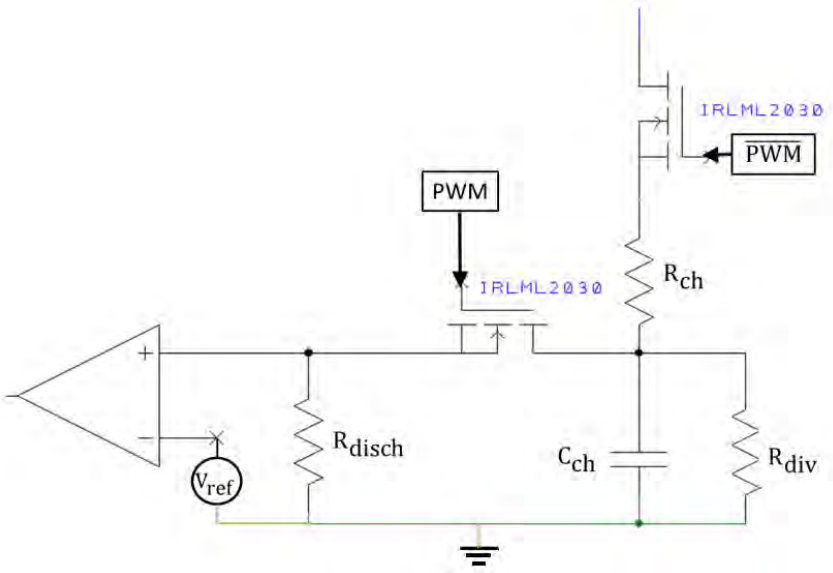


Figure 5.19 Pulse circuitry for on-pulse generation (off-pulse generation is the same with control signals from PWM inverted)

When the PWM signal is low the charging branch is on, causing the capacitor to charge to a final value set by R_{ch} and R_{div}. This value must be reached before the PWM signal goes high in a worst case scenario, which would be the minimum duty cycle of 5%. When the PWM signal goes high the charge switch turns off while the discharge switch is turned on and the capacitor discharges through R_{disch} from its peak value past the negative terminal reference value of V_{ref}. The amount of time that this takes depends on the design equation below.

$$V_{final}=V_{dd}*\frac{R_{div}}{R_{div}+R_{ch}} \quad \textbf{(5-30)}$$

$$t_{ch\text{-}V_{final}}=2.3*C_{ch}(R_{div}||R_{ch})<0.1*T_s \quad \textbf{(5-31)}$$

$$V(t_{pulse})=V_{ref}=V_{final}*e^{\frac{-t_{pulse}}{(R_{div}||R_{disch})C_{ch}}} \quad \textbf{(5-32)}$$

$$-(R_{div}||R_{disch})C_{ch}*\ln\left(\frac{V_{ref}}{V_{final}}\right)=t_{pulse} \quad \textbf{(5-33)}$$

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The value of V_{ref} is decided first to be 2.5 V and the final charge voltage for the capacitor will be 5 V. The desired t_{pulse} is the rise time of the MOSFET which will be around 100 ns. With the initial period used of 11 µs, the minimum charge time is 550 ns. The final values are chosen with the design equations above.

$$\frac{5}{10}=\frac{R_{div}}{R_{div}+R_{ch}} \quad \textbf{(5-34)}$$

$$550n=2.3*10n(50||50) \quad \textbf{(5-35)}$$

Because of all the capacitance in the pulse circuitry, if the charge capacitor is chosen less than 10 nF it will discharge too much when the discharge switch is turning on and there will be no pulse on the output of the comparator. This is shown in Figure 5.20 with experimental and simulated data. The capacitor in this experiment and simulation is below 1 nF.

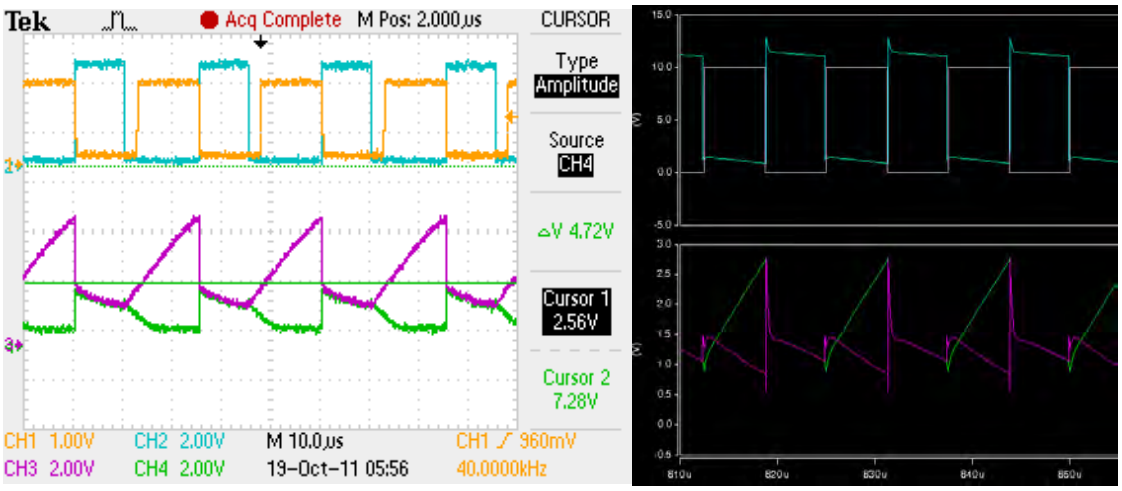


Figure 5.20 Cap discharge below Vref (2.5 V) due to parasitics eliminates pulses; (left) PWM signal (top), cap voltage (purple), Rdisch voltage (green); (right) PWM signals (top), cap voltage (green), Rdisch voltage (purple)

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With the capacitor chosen at 10 nF, the resistors are chosen to be 50 Ω. Now the discharge resistor can be determined to give the 100 ns pulse duration, which is determined as 30 Ω in the equation below.

$$-(50||30)10n* \ln\left(\frac{2.5}{5}\right)=130n \quad \textbf{(5-36)}$$

The waveforms of the pulse circuitry are shown in Figure 5.21. The output of the comparator is what will be sent to the digital transmission optocoupler.

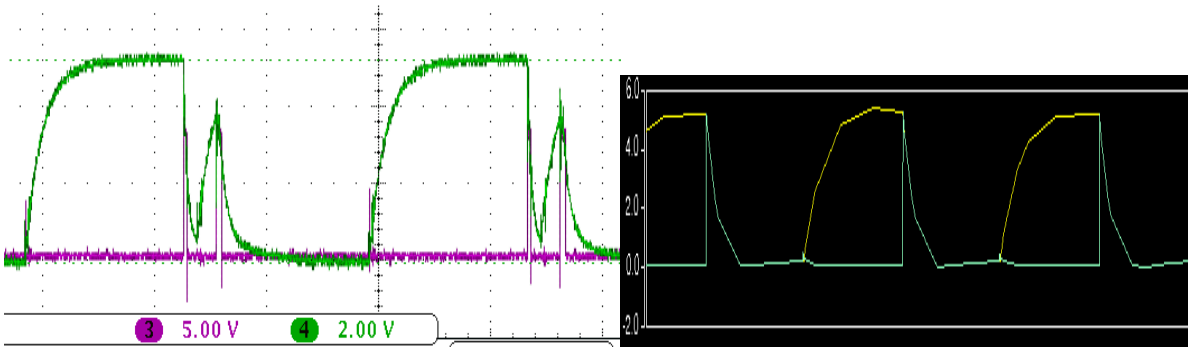


Figure 5.21 Pulse circuitry waveforms (experimental and simulated); (left) output pulse (purple), capacitor voltage (green); (right) capacitor voltage (yelow), Rdisch voltage (green)

5.1.6 Digital Transmission Optocoupler Selection

The selection of the digital transmission optocoupler is determined by the characteristics of the digital optocouplers presented in Chapter 4. The optocouplers must operate at the 10 V supply of the control circuitry unless and level shifter is used. Also, because the MAX15018A is chosen to relay the on- and off-pulses to control the half-bridge topology of the gate driver the digital optocouplers output voltage must be below 3.3 V to register an off-signal and above 6.7 V to register an on-signal to turn on the high-side MOSFET or low-side MOSFET of the gate driver [20]. The optocoupler to transmit the digital signals is chosen to be the LED and BJT pair. This is due to the ability to operate with a 10 V supply unlike the digital optocouplers with an amplifier output stage and the output voltage can swing from a

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minimum of 2.2 V at 70 °C to 10 V which is within the thresholds to control the gate driver correctly. The key parameters of pulse width and output voltage range for this circuitry was shown in Chapter 4. Pulse width is important because the energy recovery gate driver is shown to need very short turn-on and turn-off pulses to enable the energy recovery function, fully explained in the Background Chapter and Gate Driver Design Chapter. The pulse width from the input is maintained at the output if the rise and fall times of the output are fast enough to track the input's rise and fall times. The rise and fall times are a restricting parameter of the control signal optocouplers (also spoken as the minimum pulse widths). The rise and fall times and amplitude of the output are the restricting parameters for the control signal optocouplers. With the two key restricting parameters of the LED and BJT digital transmission scheme are determined to be the only applicable optocouplers from the previous chapter because their pulse width, amplitude, and rise and fall times are the best with outputs that are compatible with the thresholds needed by the gate driver inputs. However, the outputs obtained are inverted so a small inverter is used on the high-side before the control signals are sent to the gate driver inputs. To bias these circuits correctly, a buffer stage is needed to drive the LED on the input because the comparator cannot supply the correct amount of current. The buffer and optocoupler scheme is shown in Figure 5.22.

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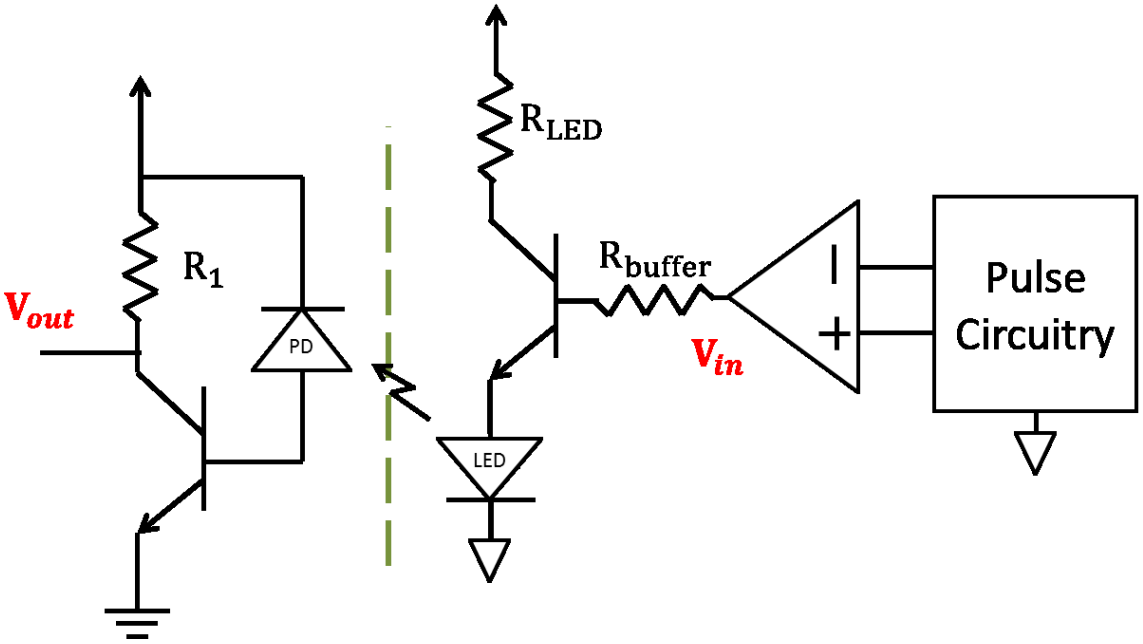


Figure 5.22 Buffer stage from pulse circuitry to digital transmission optocoupler

The comparator's current is buffered through an emitter follower that uses the design equation below to set the buffer resistor so that the proper current for the pulse is sent to the optocoupler. The important parameter is the LED current, which is equivalent to the emitter current.

$$I_{LED}=\beta\frac{(V_{in}-V_{BE}-V_{LED})}{R_{buffer}} \qquad \textbf{(5-37)}$$

With all of the components of the Buck converter designed, the next step is to validate the full system with a simulation and define the tests that determine the optocouplers used in this current-mode optically-controlled Buck converter.

5.2 Closed-Loop Buck Converter Simulation Verification

The Buck converter system validated with a simulation of the schematic shown in Figure 5.23. This simulation implements a simplified current-mode controlled buck converter. There is not any isolation modeled in this simulation because of the absence of a dynamic optocoupler model.

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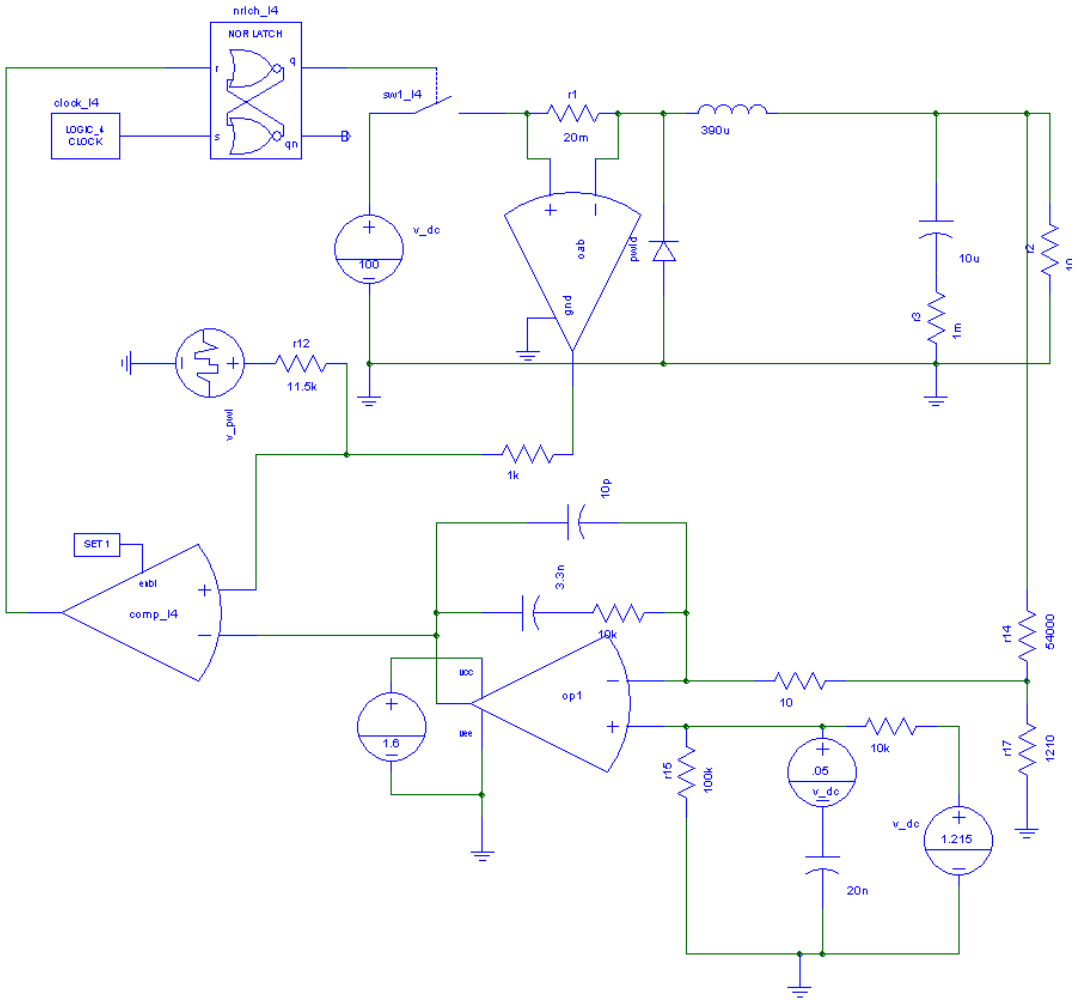


Figure 5.23 Schematic of current-mode Buck converter to validate the design above

This simulation takes into account the current and voltage sensing loop with a Buck converter operating with all of the open-loop parameters defined above (85 kHz, 100 Vin, 50 Vout, 5 A, and correct output filter). The current sensing scheme takes into account the sensing resistor, current sensing amplifier with correct gain, and slope compensation. The analogous voltage of the current sensing signal is then compared to an error voltage that is set to around 1 V (what the HV9123 scales the 4 V voltage sense pin voltage to) to allow for a nominal output voltage of 50 V at 5 A [24]. The compensation network has to be added so that this simulation will mirror the characteristics of the HV9123. The system is simulated over 5 ms with a soft-start of the entire circuit shown in Figure 5.24.

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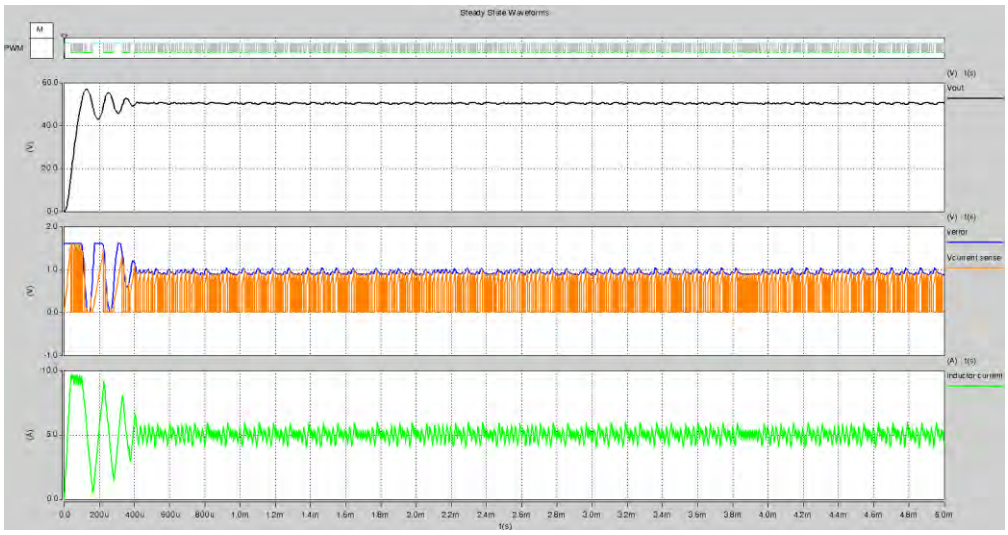


Figure 5.24 Full system simulation, output voltage (black), error voltage (blue), current sense (orange), inductor current (green)

Overall this simulation validates the design chosen above, albeit for oscillations in the inductor current. The output voltage is very stable and Figure 5.25 shows a zoomed in view of a very stable region of this simulation that represents what will be desired in the final design.

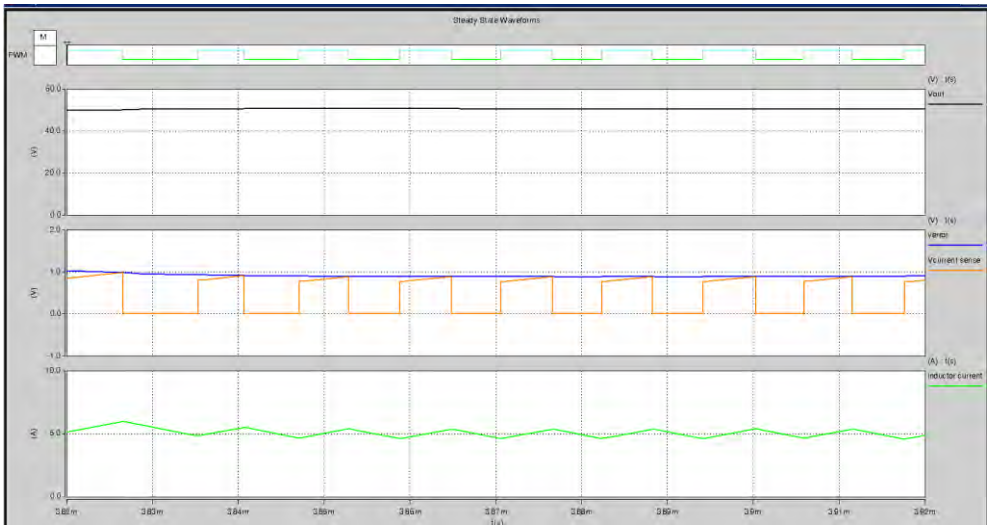


Figure 5.25-Waveforms zoomed in (current and voltage ripple well within design criteria), output voltage (black), error voltage (blue), current sense (orange), inductor current (green)

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5.3 Current-Mode Optically-Controlled Buck Converter

With all the full system components designed the current-mode optically-controlled Buck converter can be implemented and a PCB may be designed and populated. The first section will discuss the implementation and initial testing that is done to verify the design fulfills the results from the simulation presented in the Buck design section. Once the operation is verified the final experimentation can begin. The objective for these final experiments of the entire system is to determine the impact of the optocoupler feedback and control networks. Because the weakest link for the optocouplers is the propagation delay the impact on the full system is determined by increasing the frequency of operation of the Buck converter system until the optocouplers impede the proper operation. The respective topologies chosen have been analyzed in depth individually and the benchmark for the current optocoupler technologies is presented and discussed in the Conclusions Chapter to follow.

5.3.1 PCB Implementation of Current Mode Optically Controlled Buck Converter

The first step to testing the full system and determining how the optocouplers affect the operation is designing a PCB for the system. The PCB layout is designed to have all three isolated sections on one board with the optocouplers in between the Buck converter and high-side sensing section and the control circuitry section. Short routing tracks were integral because of the frequencies of the signals. The optimized layout is shown in Figure 5.26 with the sections labeled and the full schematic is shown in Figure 5.27.

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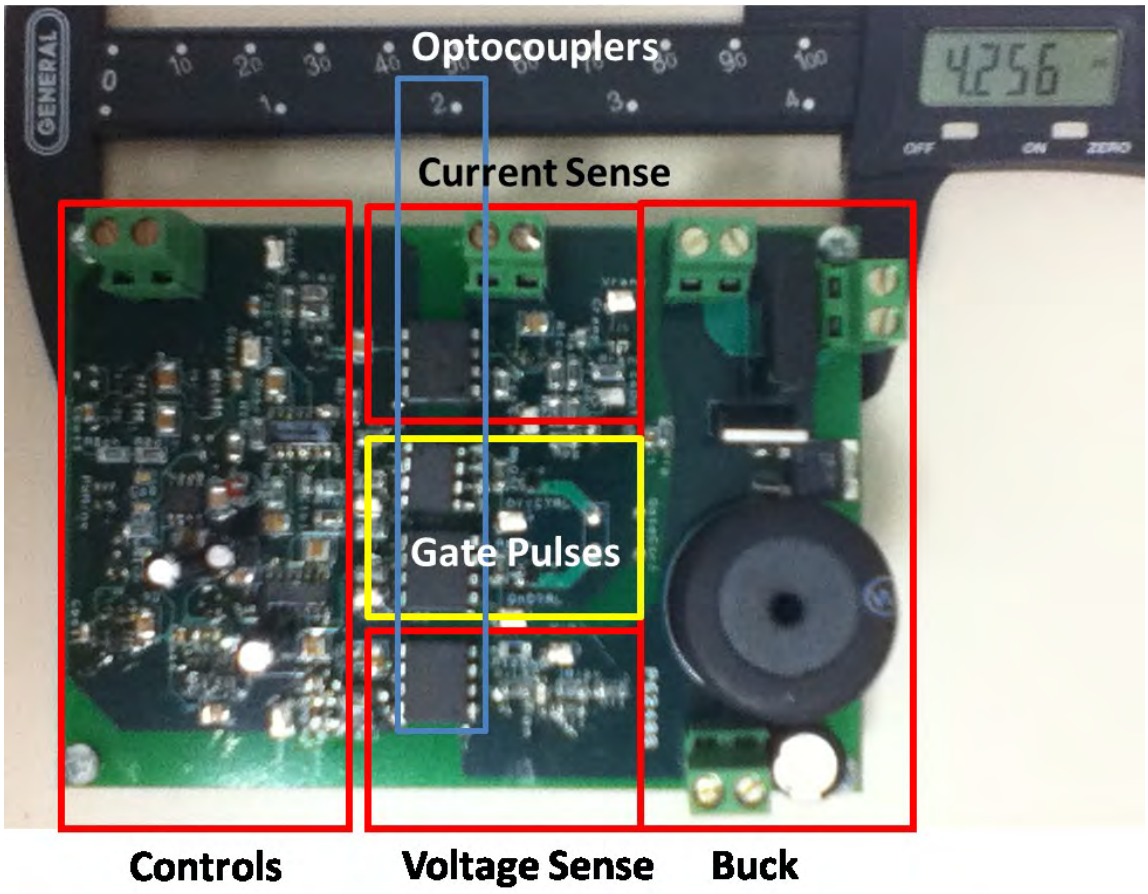


Figure 5.26 Full system PCB in the lab fully populated with sections marked

Once the system is designed a PCB, tests were conducted to verify the physically implemented design. The PCB needs to be verified at the initial values of 85 kHz switching and 100 V input voltage. The test setup is shown in Figure 5.28.

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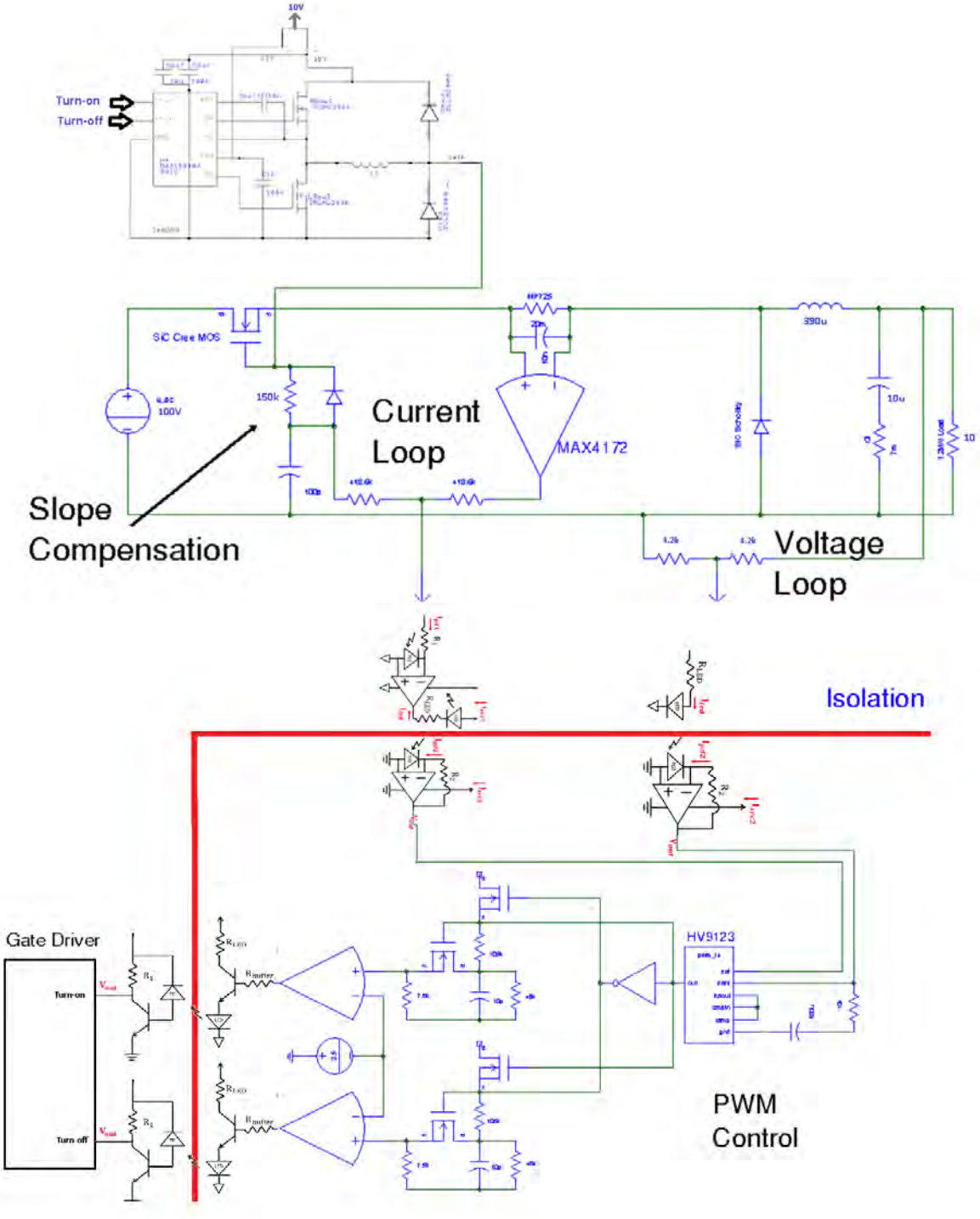


Figure 5.27 Full schematic

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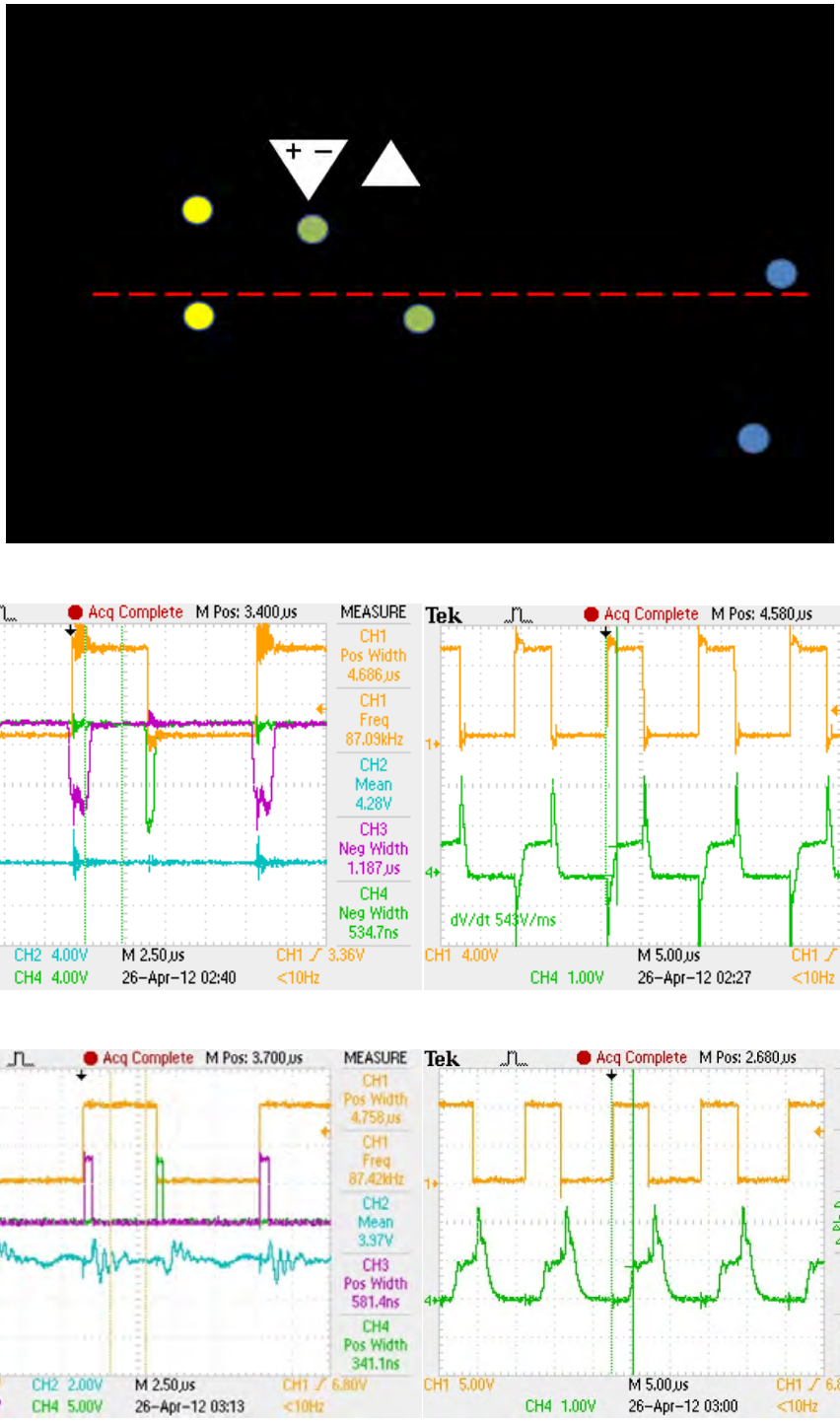


Figure 5.28 Row one: schematic shows the signals measured and their colors; row two: Gate voltage (yellow), on/off-pulses (green and purple), voltage sense (blue), current sense (green); row three: PWM output (Yellow), on/off-pulses (green and purple), voltage sense (blue), current sense (green)

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As the initial verification tests began, troubleshooting of different sections of the board took place. Many things like noise and parasitics affected the ideal design described in the Buck converter design section. There are important changes to the design that were decided upon during the verification phase. There were other troubleshooting difficulties, but they are skipped because the problem and solution do not add to or change the benchmark of the optocouplers or the final Buck converter design. The difference in the following troubleshooting discussion is that these changes affect the operation and benchmark of the current-mode optically-controlled Buck converter. The first changes have to do with the noise of the switching MOSFET. Figure 5.29 shows the noise on the gate and drain of the MOSFET while switching, this noise is reflected into the sensing network which causes issues.

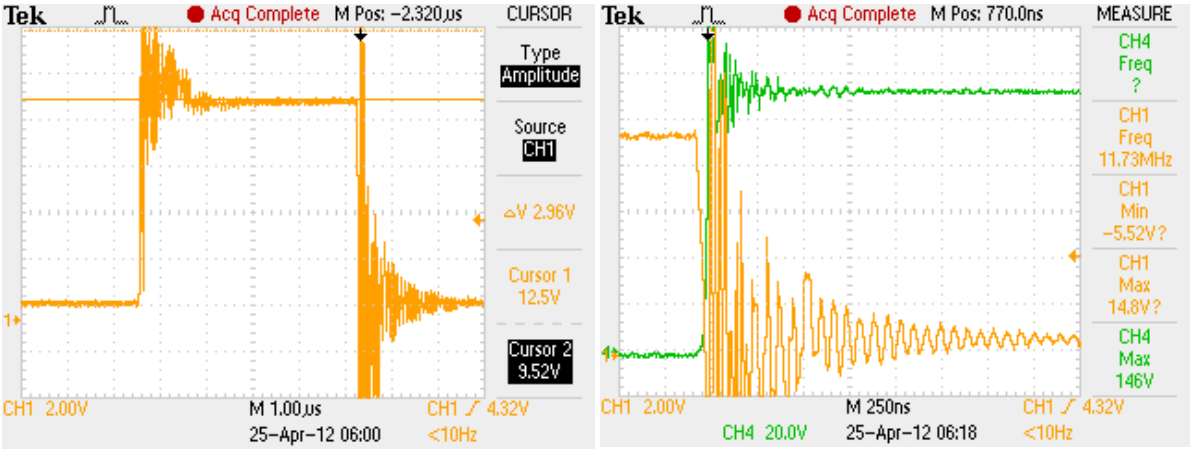


Figure 5.29 Oscillations present in gate (yellow) and drain (green)

The SiC MOSFET is switching 100 V at 85 kHz. The energy being switched is not the problem here. The problem is the rise and fall time of the MOSFET's gate voltage, which is only 8 ns. With any parasitics in the system that will cause a very large spike. The first step is to slow down the rise time by adding inductance into the gate driver path. Adding inductance decreases the resonance frequency, and as described in the gate driver chapter the turn-on time decreases. This is done to decrease the $\frac{di}{dt}$ which, due to inductance being the main component of the parasitics in the circuit, will decrease the

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voltage spikes. The original inductance was 22 nH, which is changed to 1 µH in which increases the rise time to 80 ns so that the change in current decreases. A lot of the noise is still present. Figure 5.30 shows that the noise is actually on the turn-off signal coming from the digital optocoupler that transmits this control signal.

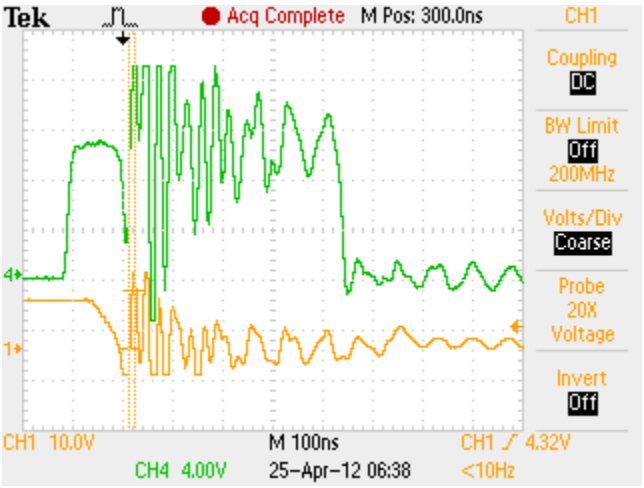


Figure 5.30 Noise in off-pulse (green) and gate voltage (yellow) (spike at 14V+)

The solution was to braid the signal line in the same ground line so that any noise from EMI would appear as common-mode noise and the potential difference would still be the same. The noise shows up in both signal and ground because the tightly braided lines will allow the two signals to share the same space and any electromagnetic signals will affect both wires. Figure 5.31 shows the gate and drain with a smaller and shorter duration noise. The rest of the noise is due to the pulse being on too long because of the limitations of the digital optocoupler. Because of the slow response times of the digital transmission optocoupler pulse width is added to the original signal which causes the energy recovery feature to be disrupted. This response time is further illustrated in the following sections.

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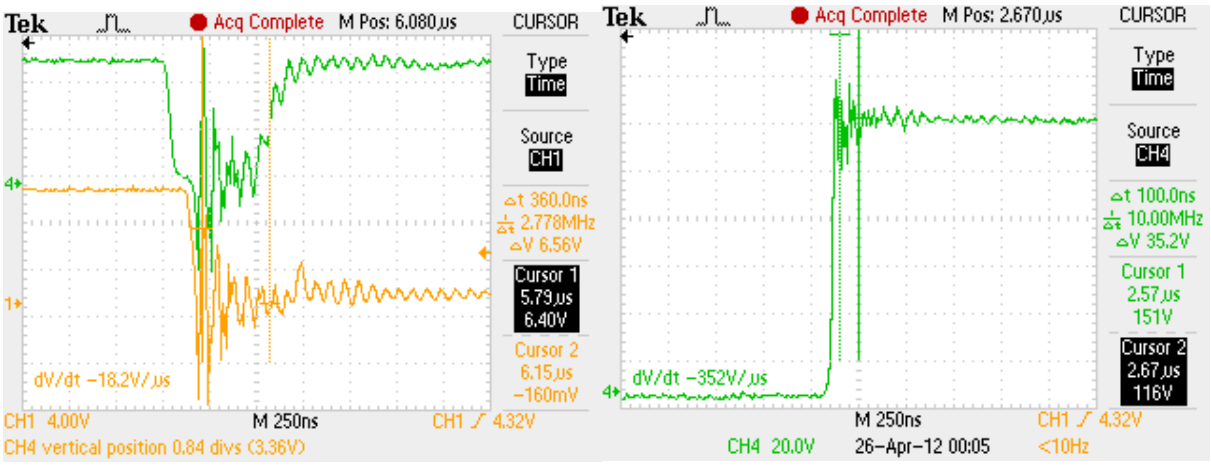


Figure 5.31 After ground wrapped control signal; (left) on-pulse (green), gate voltage (yellow) (spike reduced to 6 V); (right) drain voltage (green)

The next design changes have to do with the optocoupler application topologies. The first change is the resistors that set the gain in the circuitry. Initially the optimal test setup is used of 33 kΩ for both resistors, but the parasitics caused two problems -- an oscillation in the current sensing network and gain differences that needed to be compensated. The gains in the circuit were compensated by increasing the current sense analog transmission topology's R_2 to 43 kΩ and the voltage sense network's sampling resistors were changed to 3.9 kΩ and the LED resistor to 390 Ω. The LED resistor for the current sensing network was a different problem. There were oscillations at a high frequency present in the power supply which is shown in Figure 5.32.

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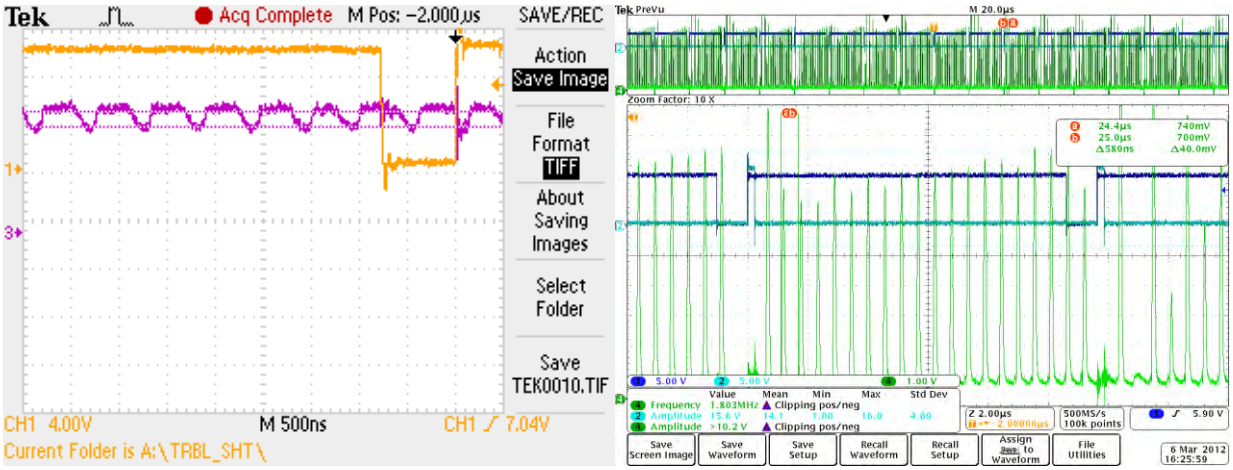


Figure 5.32 Oscillations showing in LED voltage of optocoupler (right-purple) and in output of analog transmission topology (right-green); yellow and blue are gate and PWM voltages, respectively

These were dampened by increasing the LED resistance to 900 Ω shown in Figure 5.33. The increased resistance increases the dampening of any ringing present in the circuit. It had to be increased because the ringing in the circuit needed to be dampened to not falsely trigger the Buck converter's switch. The trade-off is that the propagation delay of the optocoupler decreases as was shown in the application topology test. Figure 5.33 shows the current sensing in green working as predicted. The delay and turn-on spikes are due to the large noise present in the system when it is switching 100 V at 100 kHz and more. These need to be filtered out as best as possible to optimize the operation of the circuit.

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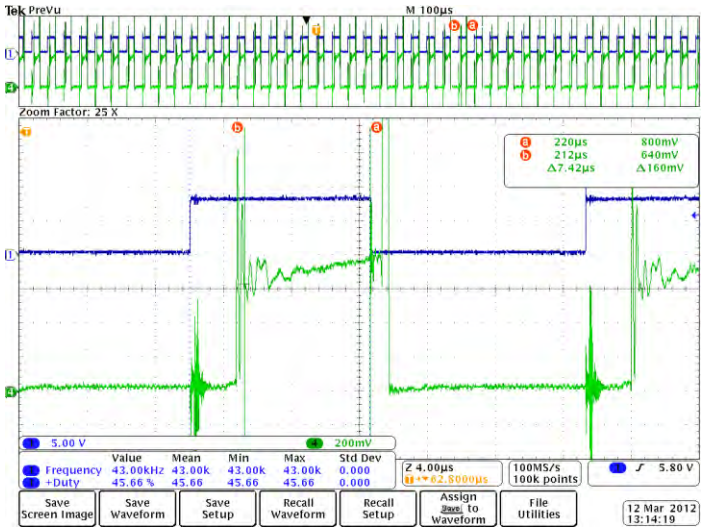


Figure 5.33 Current sense working (green), blue signal is PWM

The next step is the use of low pass filters at the current sensing op amp, voltage sensing input and output, and at the current sensing output. This changes the current signal from the figure above to Figure 5.34. The turn-on spikes are completely gone, while the turn-off spikes (larger due to energy stored in the Buck converter inductor being switched to a different branch of the circuit) were decreased to 2 V.

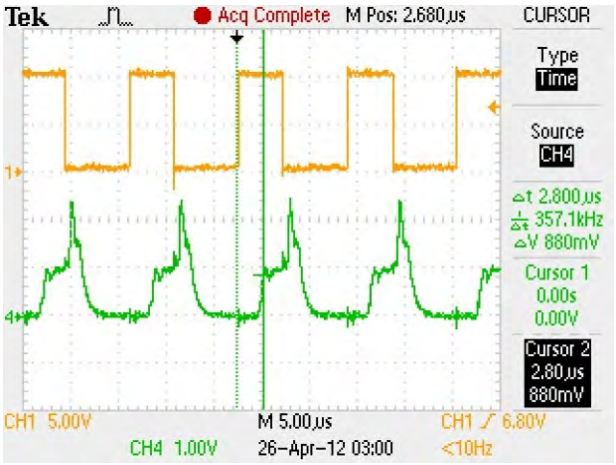


Figure 5.34 Oscillations gone, spike still exists at turn-off due to energy stored in inductor of Buck converter output filter

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5.3.2 Benchmark for Current Mode Optically Controlled Buck Converter

Now that the important design changes have been made the initial verification is complete. The initial operation of the Buck converter working at the initial frequency is shown previously. It works with a 100 V input and a 50 V output limited to 5 A. The final test can now be proposed. The system's operating frequency will be changed from 85 kHz to the maximum frequency that the optocouplers will allow. The change in the system will be recorded and a final benchmark can be concluded. The test setup measures many different parameters. Figure 5.35 highlights each system variable that is measured.

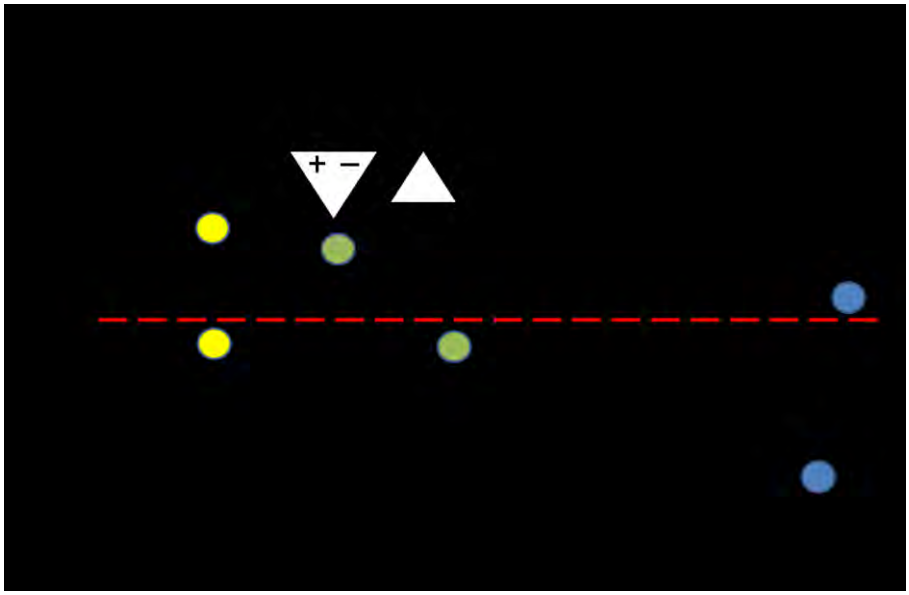
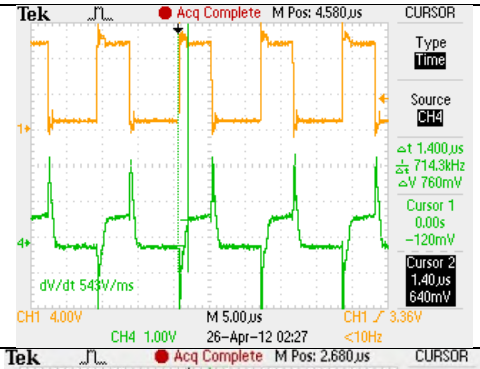
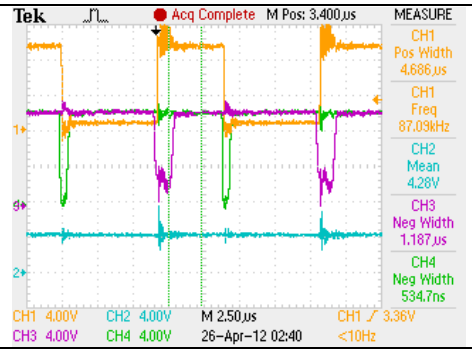
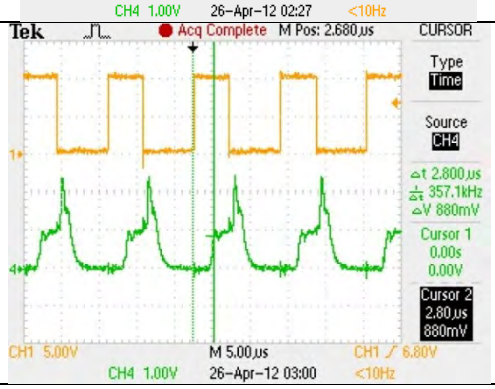
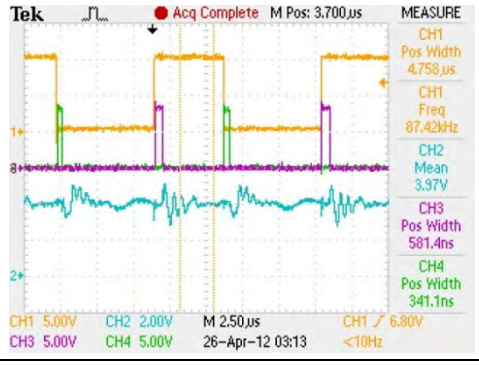
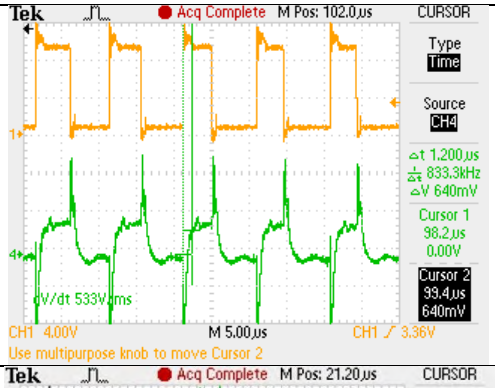
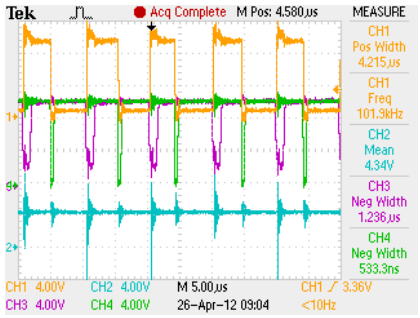
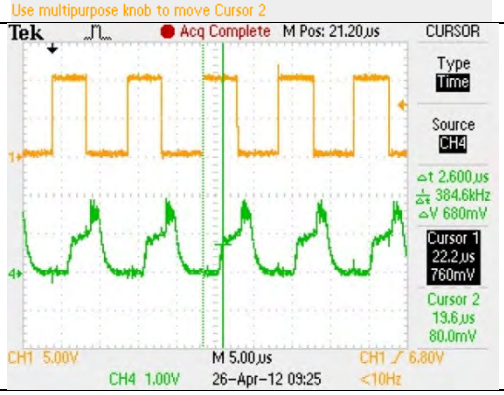
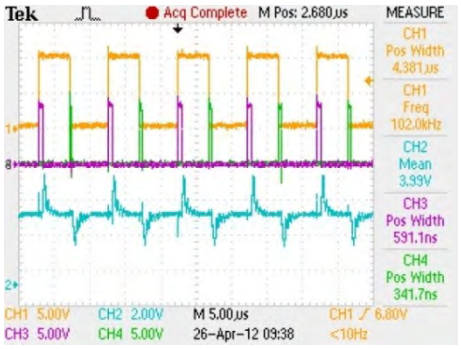


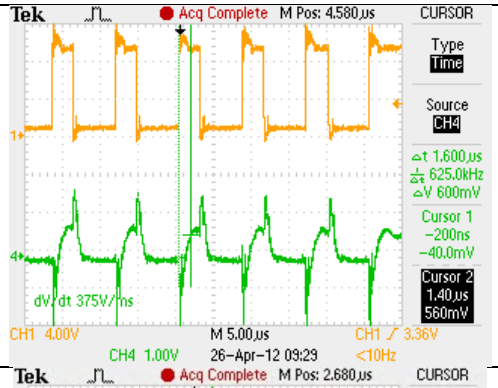
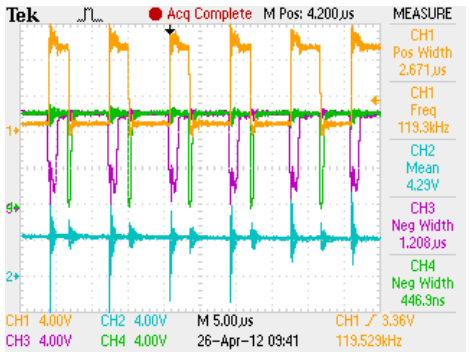
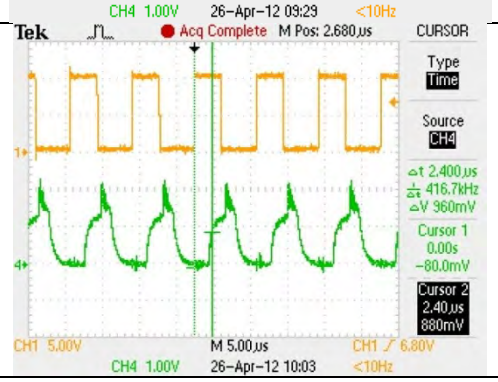
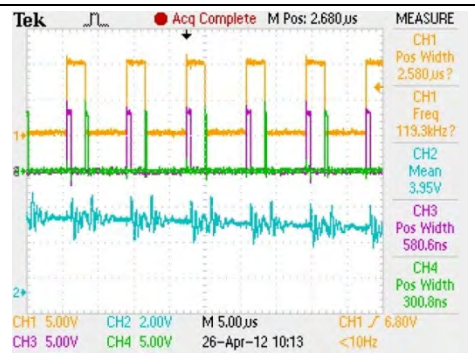
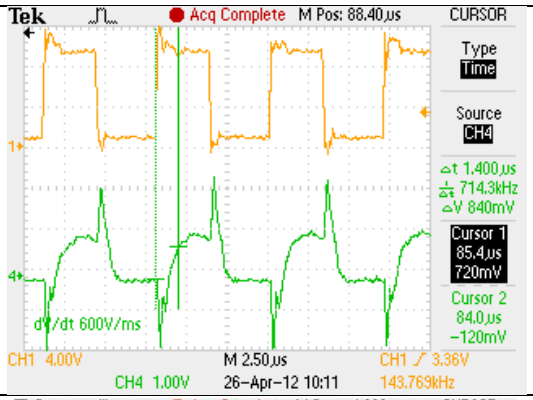
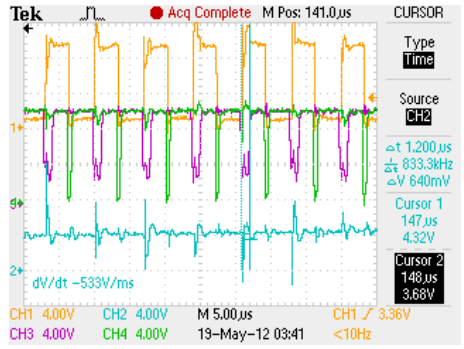
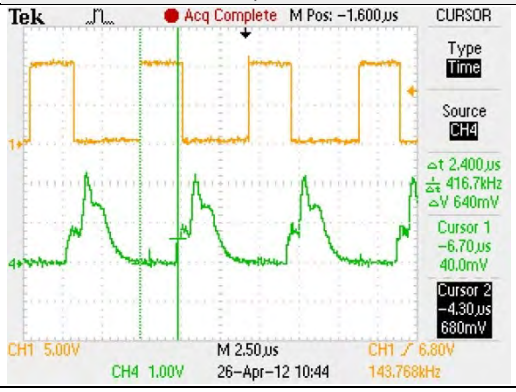
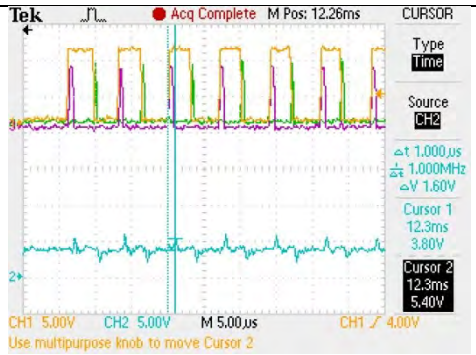
Figure 5.35 Measurements emphasized with colored circles where the dotted line represents the isolation barrier (note that the PWM and Gate signal also show the on- and off-pulses)

Table 5.3 shows the results from increasing the frequency until a maximum frequency was reached due to either the propagation delay of the analog transmission optocouplers or an overlap in the command signals because of the minimum pulse width of the digital optocouplers. The Conclusions Chapter will discuss these results specifically.

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Table 5.3 Results for Buck Converter Tests with Increasing Switching Frequencies

	85 kHz	
Power		
Control		
	100 kHz	
Power		
Control		

	120 kHz	
Power		
Control		
	140 kHz	
Power		 *Off-pulse width= 700ns
Control		 *Off-pulse width = 400ns

The propagation delay from the current sensing analog transmission circuitry is a total of 2.4 µs due to the noise present in the system and the increased propagation delay of the optocoupler topology. Also the digital pulses are as large as 1.2 µs on the output of the digital transmission optocoupler due to the minimum pulse widths of that circuitry. This is not the first failure mode in the circuit, but if the operating frequency was able to reach 250 kHz the digital propagation delay would impede correct operation of the Buck converter. The next chapter summarizes the experimental results from the Optocoupler Experimental Chapter to determine the benchmarks and the final implication of the optocoupler on the Buck converter system.

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6 CONCLUSIONS

The objective of this thesis is to determine the benchmark performance of the current optocoupler technologies and to design a real-world application for the optocoupler to operate in and display the benchmark within the context of a system. The information presented started with the specific concerns of this thesis. The first concern is the performance of commercially available optocouplers, and to create a benchmark of these optocouplers operating in the specific schemes defined to be analog and digital transmission. This benchmark is determined by experimenting with the two different roles that the optocouplers are applied in (analog and digital transmission) with respect to the important characteristics. These characteristics were defined as propagation delay, linearity, and temperature operation for the analog topologies, and propagation delay, minimum pulse width, and temperature operation, for the digital topologies. Different experiments were conducted in the Optocoupler Experimental Chapter to determine the characteristics of the optocoupler transmission topologies. Below, the final benchmark for the two different optocouplers schemes will be presented.

A parallel concern is to implement these optocoupler topologies that are defined, and test them to determine a benchmark in a specific power electronics system design. The design chosen was a current-mode controlled Buck converter. This system allows for the optocoupler to be shown off in two ways. First, is in the sensing networks that sense and transmit the key system variables (inductor current and output voltage) through the isolation barrier to the low voltage control of the system. The second part is to digitally transmit the control commands through the isolation barrier to the floating, high-voltage, gate driver to control the switch's state. This system determined and explored the limiting factors that the Buck converter had when the optocouplers were placed in the feedback and control path. This is a desired area of research because of the innovations sought in power electronics are

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increasing power density, operating temperature, and breakdown voltage, which cannot be achieved with current transformer isolation technologies.

6.1 Benchmarks

The experimental setup and results in the Optocoupler Chapter determined the benchmark for the two optocoupler schemes, digital and analog. This section will synthesize the results to draw conclusions on the final benchmark for each scheme. The benchmark will be defined in each subsection because they are different for each scheme since the information that is being transmitted has unique characteristics.

6.1.1 Analog Topology Benchmarks

The benchmark for the analog topologies is determined by several factors: propagation delay, linearity from input to output, operation over temperature, and power consumption. To conclude this thesis this benchmark needs to be determined from the results presented in an earlier chapter. Something that needs to be noted is the subjectivity of this benchmark. For this thesis some figures of merit outweigh others. Here there is an interest in finding the benchmark with respect to the fastest, most linear analog topology. It is seen from the trend presented in the Optocoupler Characterization Experiments chapter that the power consumption increases as the propagation delay is decreased. If the power consumption figure of merit outweighed the importance of the propagation delay then the final benchmark will look different, thus the subjectivity of this benchmark. The final benchmark that is presented below is a great starting point for any design implementing these optocoupler topologies, but it should not be interpreted as the ultimate performance of these devices, but rather, the optimum performance in which these devices should operate when optimizing for the key parameters that have been chosen.

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For the feedback analog topology using the chosen HCNR201 optocoupler the benchmark for the propagation delay for the analog optocouplers is shown right below 100 ns when the photodiode is biased to the maximum amount of about 60 µA and a voltage gain that is easily set by the two system resistors. This biasing corresponds to an input power consumption of 200 mW and an output consumption of 100 mW. This amount includes the power consumption of the op amp that is used in the design.

If the open-loop topology is used with the same optocoupler as in the feedback topology the propagation delay can be found to be below 280 ns but the transfer gain must be decreased to $0.6\ \frac{V}{V}$. The key here is LED current. Increasing this current by increasing the input voltage or decreasing the input LED resistance will decrease the propagation delay. A maximum of about 20 mA is achievable within the safe operating range of the optocoupler. At this point the propagation delay can be expected to be the same as the feedback topology, but it was shown that the output stage has to implement a larger feedback resistor than the feedback topology to have a comparable gain so the overall propagation delay is increased due to the op amp and overcoming the input threshold. The trade-off is a smaller power consumption of 65 mW on the output and zero on the input (excluding the input voltage biasing). In the linearity tests where the input is biased with a voltage that stays above the input threshold, the propagation delay is decreased to 100 ns or less when the smaller LED resistor is used – allowing for larger LED currents. This decrease in the propagation delay is due to the optocoupler operating in a properly biased regime. When the threshold has to be overcome the propagation delay is increased (as seen in the initial biasing test). The feedback analog topology does not have this problem because the input op amp forces the LED to be biased properly to allow the correct amount of current to flow through the input servo diode.

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It will be seen in the digital optocoupler topology benchmark that the propagation delay is much smaller than the analog topologies. The speed is affected by the material and packaging of the optocoupler and the input and output stage. The optocoupler material is held constant but the input and output stage is changed dramatically with respect to propagation delays. This is what hurts the propagation delay, or speed at which these devices can operate. The fundamental optocoupler structure that is within the analog topologies is capable of having the same propagation delays and rise and fall times as the digital topologies because it is the same technology, but to have any linearity there must be circuitry around. Also, the low natural gains have to be boosted with large op amp gains causing issues with noise injection. If future technologies like GaN can increase the CTR the high gain in the op amps could be decreased.

The linearity is an important part of the benchmark because if it is bad the optocoupler topology will distort the transmission of the analog data. The output of the analog feedback circuit with the fast propagation delay of around 100 ns is linear between ±5% of nominal gain (unity) while the input servo diode current is around 20 μA. There is no limit on the input voltage to this circuit as long as the input current is kept below about 60 μA. When the input is below the 20 μA region the output starts to decrease to 75% of the input. This is still a decent linearity when compared with the non-feedback topology. The linearity of the non-feedback topology is first seen in the biasing tests as the CTR changes across different LED currents. The CTR is relatively stable within a 5% range until the LED current is increased past the nominal range where the CTR quickly doubles. As seen in the section discussing the propagation delay benchmark, the propagation delay is decreased when operating the LED at this high current level. When a sinusoidal input is applied it can be seen that operating in the region where the CTR doubles from its nominal value allows for the output to be linear to a ±5% region of the CTR value. This happens when the LED is biased above 16 mA. If the 110 Ω R_{LED} is used the propagation delay will

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be around 100 ns, but the linear range is only 3 to 6 V. At 6 V the input current is up to around 50 mA, this is not a reasonable area to operate for long periods of time. With the 510 Ω R_{LED} the propagation delay decreases to around 200 ns but the input voltage range increases to an 18 V swing, from 7 V to 25 V. The CTR decreases all the way to 0.05% (an 83% decrease from the nominal gain in the linear region) at a slope of $0.1\frac{\%}{V}$ when the input bias is between 2.5 V to 7 V.

After defining the baseline performance of the propagation delay and linearity the operation over temperature must be identified to finalize the benchmark. For the feedback topology the temperature increases the propagation delay of the benchmark to 180 ns. The linearity is not changed due to temperature unless a larger R_{LED} is used. With a large R_{LED} the output voltage is cut off whenever the current through the LED causes the voltage across R_{LED} to cut-off the voltage across the LED, thus clamping the current even if the input voltage increases. The temperature affects the non-feedback topology by decreasing the overall CTR by about 8%. The linear range does not change because the CTR at each biasing point is shifted down. The propagation delay is generally increased with increased temperature, but not by as large as an amount as the feedback topology. Why is the effect of temperature on propagation delay different between the two topologies when, in both, only the optocoupler is heated? A possible reason is that in the feedback topology the optocoupler parameters change with temperature which effect the propagation delay of the input op amp because it is the feedback for that op amp, and in the non-feedback topology the changing parameters do not change the overall feedback of the op amp. Table 6.1 summarizes the benchmark for the different optocoupler topologies

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Table 6.1 Summary of Analog Transmission Optocoupler Benchmark

	Feedback	Effect of Temp	Non-feedback	Effect of Temp
Propagation delay	100 ns	Increased about 100 ns	200 ns (R_{LED} needs to be larger to allow for larger region of linearity)	Increases are only around 20-40 ns
Linearity (±5% of nominal gain)	2 to 6 V (20 µA-60 µA photodiode current)	None (big effect if large R_{LED} is chosen)	7 to 25 V (16 mA-45 mA LED current)	None
Linearity below biasing range	25% of nominal value	None	83% of nominal value	None
Input Power consumption	200 mW	Increased by at least 6-8% (less CTR)	n/a	n/a
Output Power consumption	100 mW	Same	65 mW	Same

A conclusion can be drawn that if a proper supply is available the feedback analog topology has the best baseline performance. Not only is the propagation delay faster overall even when the temperature increases, the linear operating region is stiffer. The biasing might look like a wider region in the non-feedback when the input voltage is focused on, but the feedback topology input voltage can be increased if the input biasing resistor is increased. The best part about the feedback topology is that out of the ±5% region the linearity only changes by ±25%. This still allows the circuit to be useful while the non-feedback topology becomes completely useless outside of the linear region.

6.1.2 Digital Topology Benchmarks

The digital topology benchmark is slightly different than the analog topologies'. Propagation delay and power consumption, along with temperature operation play a large role, but linearity is not needed since this is digital device. Minimum pulse width replaces this which will determine, along with propagation delay, the baud rate these devices can achieve. The minimum pulse width is determined by

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the minimum rise and fall time of the digital optocoupler output in response to an input change. It mostly has to do with proper biasing and output stage. A Schmitt trigger with hysteresis on the LED transistor pair could enhance the pulse width by decreasing the output voltage swing needed by the optocoupler output stage. This is done in the amplifier optocouplers and the effect can be seen to improve rise and fall times. The rails that the output must swing to for the LED and BJT pair optocoupler topology is to 10 V, the amplifier topologies only go to 5 V because that is the maximum operating power supply. The power consumption will be compared by simply doubling the amplifier topologies and the rise and fall times (ultimately the minimum pulse width) will be slightly compared by looking at slopes.

Because the output stage only needs to be turned on and off, it can be optimized to have extremely fast rise and fall times so the digital optocouplers have a propagation delay due only to the material of the optocoupler. The LED and BJT topology is not as optimized as a topology as the other ones so it will still have a good biasing range and propagation delay. The digital optocoupler temperature characteristics will determine the how the benchmark changes over increasing temperatures. Table 6.2 summarizes the benchmark for the different devices.

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Table 6.2 Summary of Digital Optocoupler Transmission Benchmark

	LED BJT Pair		LED Amplifier Pair	
	HCPL4505 (GaAsP)	**HCNW4505 (AlGaAs)**	**ACPL071L (GaAsP)**	**HCPL7723 (AlGaAs)**
Operating Point	V_{in}=10 V R_{LED}=100 Ω R_{out}=1.5 kΩ	V_{in}=10 V R_{LED}=400 Ω R_{out}=1.5 kΩ	V_{in}=4 V R_{LED}=110 Ω	V_{in}=2 V
Propagation Delay	40 ns	100 ns	28 ns	24 ns
Rise Time	120 ns (83 $\frac{V}{\mu s}$)	700 ns (14 $\frac{V}{\mu s}$)	8 ns (625 $\frac{V}{\mu s}$)	20 ns (250 $\frac{V}{\mu s}$)
Fall Time	580 ns (17 $\frac{V}{\mu s}$)	1700 ns (6 $\frac{V}{\mu s}$)	8 ns (625 $\frac{V}{\mu s}$)	44 ns (114 $\frac{V}{\mu s}$)
Minimum Pulse Width	740 ns	2500 ns	44 ns	88 ns
Max Data Transmission	1.35 MBd	0.4 MBd	22.7 MBd	11.3 MBd
Input Power Consumption	n/a	n/a	n/a	30 (60 mW)
Output Power Consumption	35 mW	58 mW	15 (30 mW)	65 (130 mW)
Effect of Temp	Decreases speed by 35% at 70 °C	n/a	Decreases speed by 15% at 70 °C	Increases fall time and unstable at 70 °C

The first thing seen above is the GaAsP optocouplers have better baseline performance than the other material used, AlGaAs, with its smaller rise and fall times, and correspondingly smaller minimum pulse widths and max data transmission. The amplifier outputs obviously create the benchmark of 22.7 MBd and 15 mW of power consumption. Even when the power is scaled it is less than the LED and BJT pair. Even in the temperature operation the speed only decreases by 15%. Another thing to note is the easy implementation of these devices. The output just needs a 5 V supply and the input needs one input resistor to bias the input LED at about 20 mA.

The next step is to determine the benchmark for the current-mode optically-controlled Buck converter. What will the optocouplers limiting factors like linearity and minimum pulse widths have on

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the overall system? The main factor for this is the maximum switching frequency allowed for the full system.

6.1.3 Current Mode Optically Controlled Buck Converter

The last section of the Current-mode optically controlled Buck converter chapter shows the waveforms of the experimental results that determine the maximum frequency of operation. As has been discussed and analyzed the maximum frequency is limited by the operation of the optocouplers. 140 kHz is the highest frequency that can be achieved. Although this frequency was easily accomplishable by the gate command circuitry with a 740 ns pulse width, the current sensing information has a much larger delay. There are two problems at play here. First of all noise injected in the circuit have caused a large propagation delay in the beginning due to a spike lasting 1 μs due to the switching MOSFET which the sensing circuitry and optocoupler transmission cannot respond too. As it has been stated before noise filtering was entered into the design at the point of measurement and then again at the output of the analog transmission circuitry, but this has not been good enough to filter noise over the very sensitive sensing circuitry. Also the optocoupler itself presents another 1 μs delay due to the propagation delay of the analog topology. This is larger than the benchmark set at 100 ns due to the introduction of a larger R_{LED} to dampen the oscillations in the circuitry at steady state.

The biggest lesson learned from implementing these optocouplers into a real circuit is their sensitivity. It can be seen the length at which the design process took to characterize the different optocouplers and determine how they can used stably in the Buck converter system compared to the poor results of a switching frequency of 140 kHz. A lot of this is due to the complexity of designing around the naturally low gains of the optocoupler. Because of these low natural gains, due to the small CTR parameter, the topologies have to introduce high gains with large resistors in the feedback of optocouplers. This has two main problems. One problem is that large resistors are very susceptible to

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EMI which generate voltage drops by inducing small amounts of current (tens of micro-amps) through the resistor. The other problem is that the biasing current is only tens of micro-amps so it is also very easy to distort. For the benchmark to be reached in a real system very good noise filtering needs to be applied. This would be very complex and possible future research into optocoupler analog applications.

6.2 Future Work

The future work can be broken down into two parts, research into other ways to implement optocouplers into power systems and ways to enhance the fundamental optocoupler and the circuits around them.

There are many other areas optocouplers can be implemented into power systems. One is in the actual gate control of MOSFET's in a half- or full-bridge topology. If enough gate voltage potential could be directly transmitted to the gates of the MOSFET's then there would not be a need for bootstrapping because the potential could be referenced to any node in the circuit, and unlike bootstrapping there would be isolation created as large as the withstanding voltage of the optocoupler. The area for research in this topic would be increasing rise and fall times because of how much that adds to the pulse width of a signal being transmitted. As seen in the benchmark conclusion, it can be upwards of 50% more pulse width.

This idea of transmitting information along with energy (charging the gate of a MOSFET) leads into a second area of research for implementing optocouplers into other areas of power systems, to create isolated power supplies in small footprints with high efficiency. Something not looked at in this thesis was the photovoltaic mode of operation for an optocoupler. This mode operates the output so that it supplies energy. This is the same concept as modern solar cells. The main problem for this topic of study is efficiency of energy transfer. Since CTR is so incredibly low the power on the output will be a factor of CTR less than the input. And in this case a BJT cannot be used to increase this CTR by a factor of

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β. There have been vast improvements in efficiency of commercial solar cells but to scale that down into the footprint of an optocoupler package is not a small task.

As stated earlier the dynamic characteristics of the optocoupler are not modeled in any simulation environment. This owes itself to the small uses the optocoupler has played thus far in the critical path of transmitting system variables to control a particular system. A simple static model with a current controlled current source can be used to simply model digital transmission, but for the analog transmission the CTR non-linearity and propagation delays present have large impacts on the overall system. For continued research on the subject of the optocoupler transmitting information on a critical path this needs to be remedied. Future work in this area could apply the dynamic characteristics derived by the experiments conducted in this thesis into a comprehensive model for the optocoupler.

Another area of future work is in the optocoupler material. GaN has been discussed multiple times in this thesis. There is obviously a need for optocouplers that can operate with more linearity and speed. GaN can be bring the improvements needed in increased CTR parameter in better matched and efficient LED and photodiode pairs and the rise and fall times needed to increase the overall baud rate. Something to continue researching is topologies to increase certain aspects of the key parameters presented in this thesis. With more circuitry can there be enhanced linearity and shorter propagation delays over temperature and biasing?

There is much more room in this area of research to innovate optocouplers enough so that they can replace the current transformer and increase power density by decreasing size, increase operating temperature, and increase switching speeds. This thesis has been a study into where the technology is at now and how it can be improved for future use.

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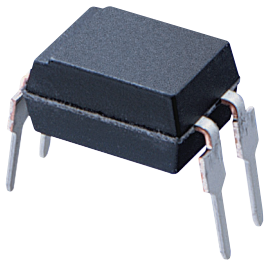
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PC817X Series

DIP 4pin General Purpose Photocoupler

*4-channel package type is also available.
(model No. **PC847X Series**)



■ Description

PC817X Series contains an IRED optically coupled to a phototransistor.

It is packaged in a 4pin DIP, available in wide-lead spacing option and SMT gullwing lead-form option.

Input-output isolation voltage(rms) is 5.0kV.

Collector-emitter voltage is 80V(*) and CTR is 50% to 600% at input current of 5mA.

■ Features

1. 4pin DIP package
2. Double transfer mold package (Ideal for Flow Soldering)
3. High collector-emitter voltage (V_{CEO}:80V(*))
4. Current transfer ratio (CTR : MIN. 50% at I_F=5 mA, V_{CE}=5V)
5. Several CTR ranks available
6. High isolation voltage between input and output ($V_{iso(rms)}$: 5.0 kV)

(*) Up to Date code "P7" (July 2002) V_{CEO} : 35V.
From the production Date code "J5" (May 1997) to "P7" (July 2002), however the products were screened by BV_{CEO}≥70V.

■ Agency approvals/Compliance

1. Recognized by UL1577 (Double protection isolation), file No. E64380 (as model No. **PC817**)
2. Package resin : UL flammability grade (94V-0)

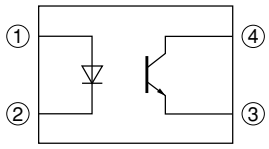
■ Applications

1. I/O isolation for MCUs (Micro Controller Units)
2. Noise suppression in switching circuits
3. Signal transmission between circuits of different potentials and impedances

Notice The content of data sheet is subject to change without prior notice.
In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that may occur in equipment using any SHARP devices shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest device specification sheets before using any SHARP device.

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■ Internal Connection Diagram

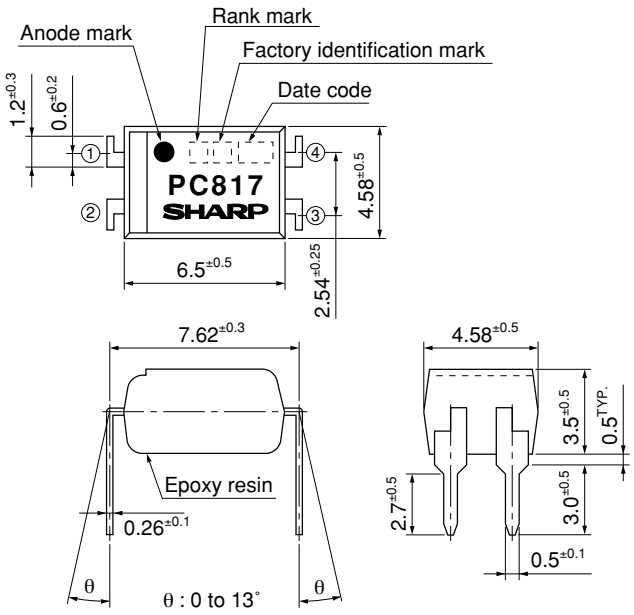


① Anode
② Cathode
③ Emitter
④ Collector

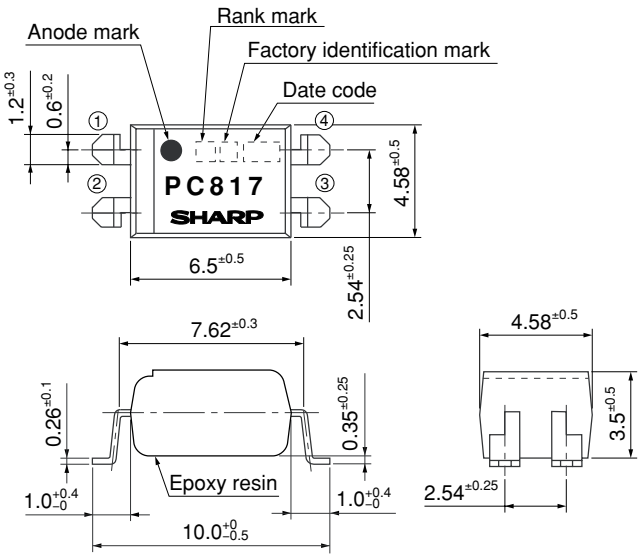
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(Unit : mm)

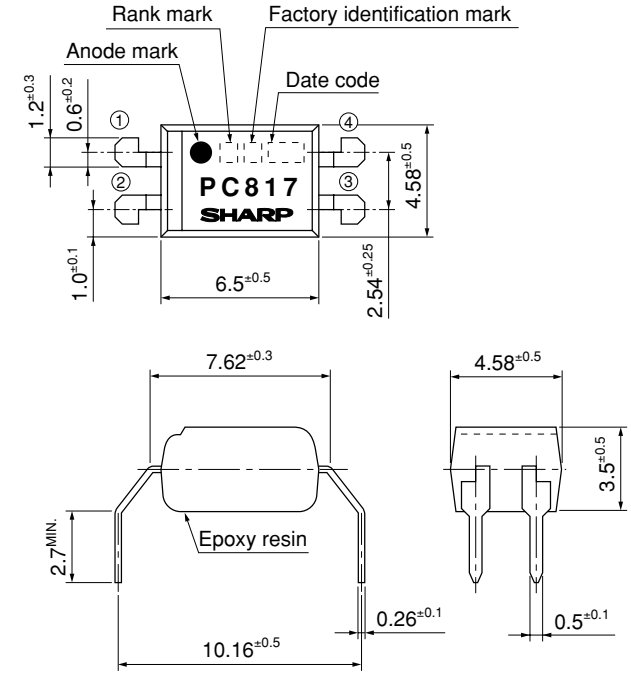
1. Through-Hole [ex. **PC817X**]



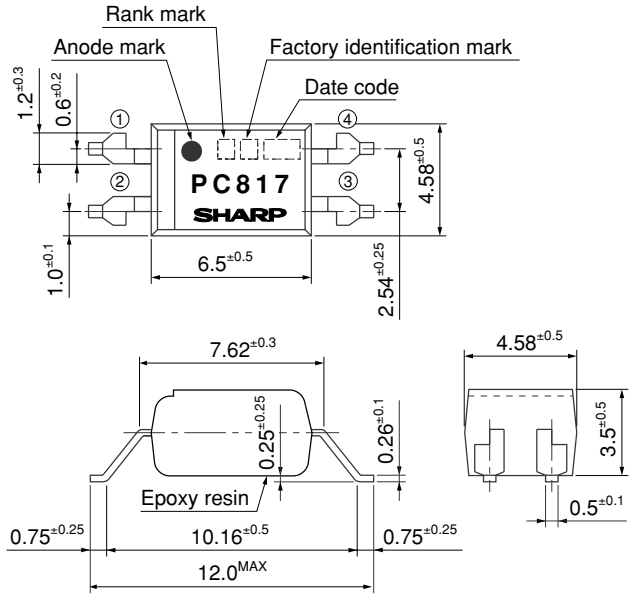
2. SMT Gullwing Lead-Form [ex. **PC817XI**]



3. Wide Through-Hole Lead-Form [ex. **PC817XF**]



4. Wide SMT Gullwing Lead-Form [ex. **PC817XFP**]



Product mass : approx. 0.21g

Date code (2 digit)

1st digit				2nd digit	
Year of production				Month of production	
A.D.	Mark	A.D	Mark	Month	Mark
1990	A	2002	P	January	1
1991	B	2003	R	February	2
1992	C	2004	S	March	3
1993	D	2005	T	April	4
1994	E	2006	U	May	5
1995	F	2007	V	June	6
1996	H	2008	W	July	7
1997	J	2009	X	August	8
1998	K	2010	A	September	9
1999	L	2011	B	October	O
2000	M	2012	C	November	N
2001	N	⋮	⋮	December	D

repeats in a 20 year cycle

Factory identification mark

Factory identification Mark	Country of origin
no mark	Japan
■	
◢	Indonesia
▽	Philippines
◥	China

* This factory marking is for identification purpose only.
Please contact the local SHARP sales representative to see the actural status of the production.

Rank mark

Refer to the Model Line-up table

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■ Absolute Maximum Ratings

(T_a=25˚C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	*1 Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
	Power dissipation	P	70	mW
Output	Collector-emitter voltage	V_{CEO}	*4 80	V
	Emitter-collector voltage	V_{ECO}	6	V
	Collector current	I_C	50	mA
	Collector power dissipation	P_C	150	mW
Total power dissipation		P_{tot}	200	mW
*2 Isolation voltage		$V_{iso\ (rms)}$	5.0	kV
Operating temperature		T_{opr}	−30 to +100	˚C
Storage temperature		T_{stg}	−55 to +125	˚C
*3 Soldering temperature		T_{sol}	260	˚C

*1 Pulse width≤100μs, Duty ratio : 0.001
*2 40 to 60%RH, AC for 1minute, f=60Hz
*3 For 10s
*4 Up to Date code "P7" (July 2002) V_{CEO} : 35V.

■ Electro-optical Characteristics

(T_a=25˚C)

	Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	I_F=20mA	–	1.2	1.4	V
	Peak forward voltage		V_{FM}	I_{FM}=0.5A	–	–	3.0	V
	Reverse current		I_R	V_R=4V	–	–	10	μA
	Terminal capacitance		C_t	V=0, f=1kHz	–	30	250	pF
Output	Collector dark current		I_{CEO}	V_{CE}=50V, I_F=0	–	–	100	nA
	Collector-emitter breakdown voltage		BV_{CEO}	I_C=0.1mA, I_F=0	*5 80	–	–	V
	Emitter-collector breakdown voltage		BV_{ECO}	I_E=10μA, I_F=0	6	–	–	V
Transfer characteristics	Collector current		I_C	I_F=5mA, V_{CE}=5V	2.5	–	30.0	mA
	Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_F=20mA, I_C=1mA	–	0.1	0.2	V
	Isolation resistance		R_{ISO}	DC500V, 40 to 60%RH	5×10^{10}	1×10^{11}	–	Ω
	Floating capacitance		C_f	V=0, f=1MHz	–	0.6	1.0	pF
	Cut-off frequency		f_c	V_{CE}=5V, I_C=2mA, R_L=100Ω, −3dB	–	80	–	kHz
	Response time	Rise time	t_r	V_{CE}=2V, I_C=2mA, R_L=100Ω	–	4	18	μs
		Fall time	t_f		–	3	18	μs

*5 From the production Date code "J5" (May 1997) to "P7" (July 2002), however the products were screened by BV_{CEO}≥70V.

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■ Model Line-up

Lead Form	Through-Hole	Wide Through-Hole	SMT Gullwing		Wide SMT Gullwing	Rank mark	I_C [mA] (I_F=5mA, V_{CE}=5V, T_a=25°C)
Package	Sleeve			Taping			
	100pcs/sleeve			2 000pcs/reel			
Model No.	**PC817X**	**PC817XF**	**PC817XI**	**PC817XP**	**PC817XFP**	with or without	2.5 to 30.0
	PC817X1	**PC817XF1**	**PC817XI1**	**PC817XP1**	–	A	4.0 to 8.0
	PC817X2	**PC817XF2**	**PC817XI2**	**PC817XP2**	–	B	6.5 to 13.0
	PC817X3	**PC817XF3**	**PC817XI3**	**PC817XP3**	–	C	10.0 to 20.0
	PC817X4	**PC817XF4**	**PC817XI4**	**PC817XP4**	–	D	15.0 to 30.0
	PC817X5	**PC817XF5**	**PC817XI5**	**PC817XP5**	–	A or B	4.0 to 13.0
	PC817X6	**PC817XF6**	**PC817XI6**	**PC817XP6**	–	B or C	6.5 to 20.0
	PC817X7	**PC817XF7**	**PC817XI7**	**PC817XP7**	–	C or D	10.0 to 30.0
	PC817X8	**PC817XF8**	**PC817XI8**	**PC817XP8**	–	A, B or C	4.0 to 20.0
	PC817X9	**PC817XF9**	**PC817XI9**	**PC817XP9**	–	B, C or D	6.5 to 30.0
	PC817X0	**PC817XF0**	**PC817XI0**	**PC817XP0**	–	A, B, C or D	4.0 to 30.0

Please contact a local SHARP sales representative to inquire about production status and Lead-Free options.

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Fig.1 Forward Current vs. Ambient Temperature

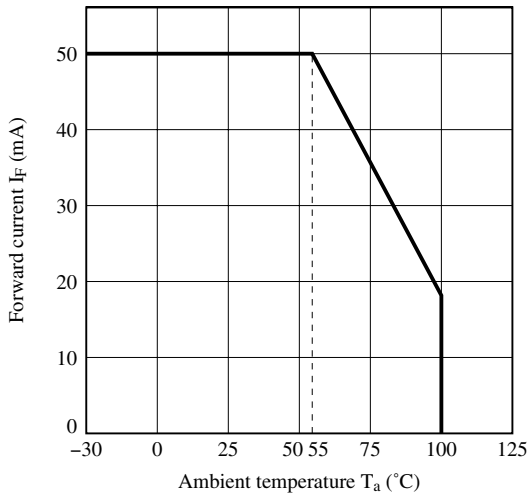


Fig.2 Diode Power Dissipation vs. Ambient Temperature

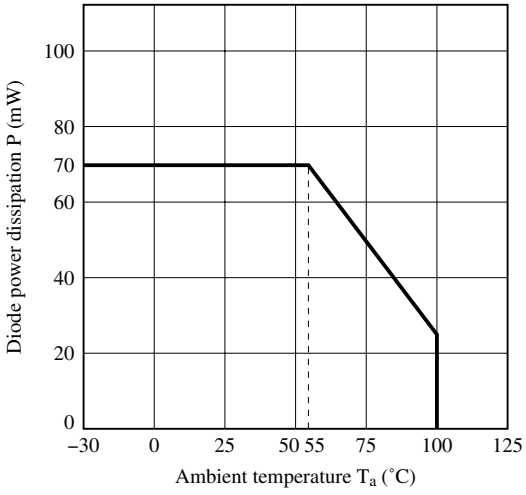


Fig.3 Collector Power Dissipation vs. Ambient Temperature

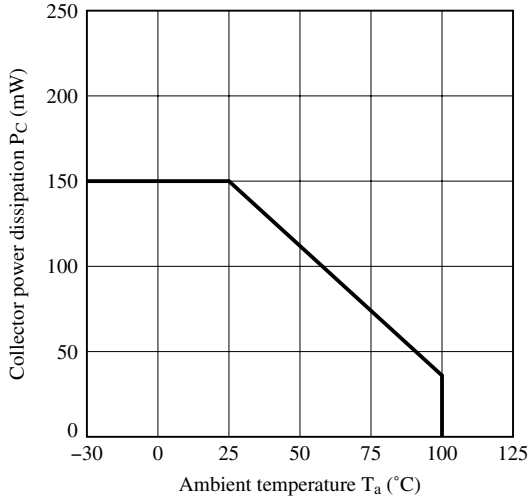


Fig.4 Total Power Dissipation vs. Ambient Temperature

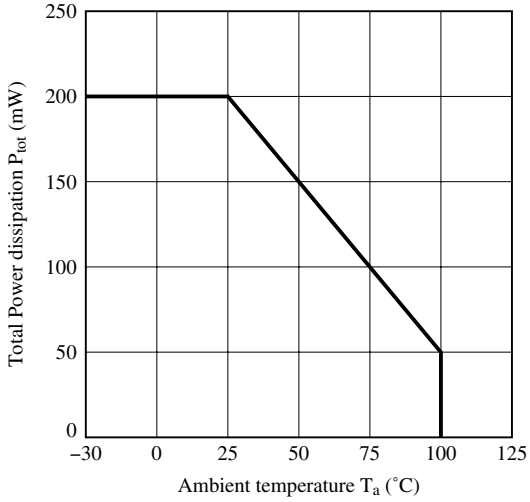


Fig.5 Peak Forward Current vs. Duty Ratio

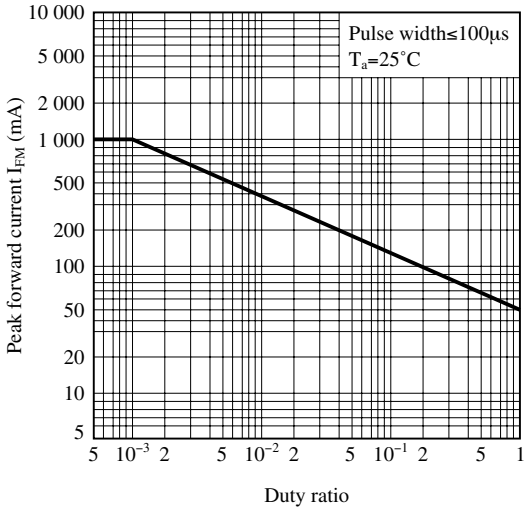


Fig.6 Current Transfer Ratio vs. Forward Current

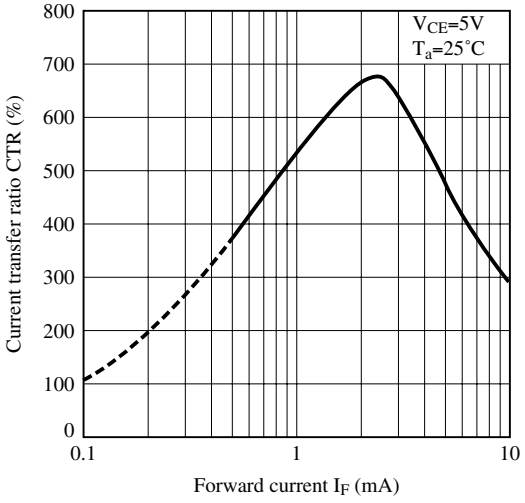


Fig.7 Forward Current vs. Forward Voltage

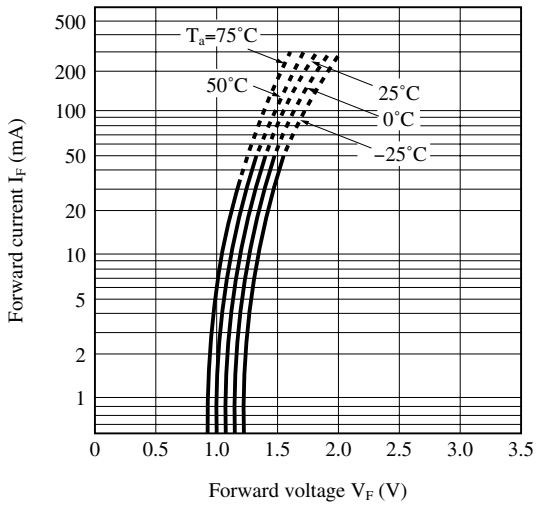


Fig.8 Collector Current vs. Collector-emitter Voltage

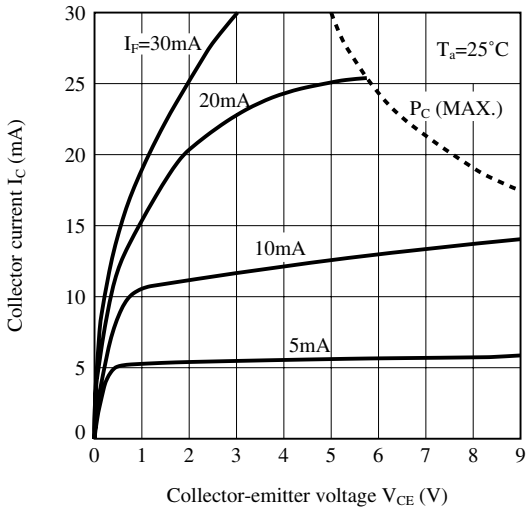


Fig.9 Relative Current Transfer Ratio vs. Ambient Temperature

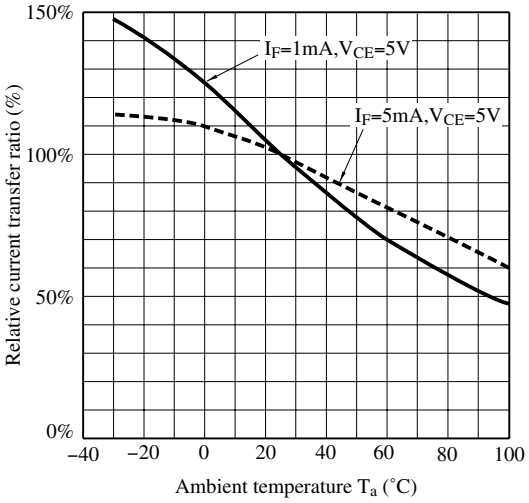


Fig.10 Collector - emitter Saturation Voltage vs. Ambient Temperature

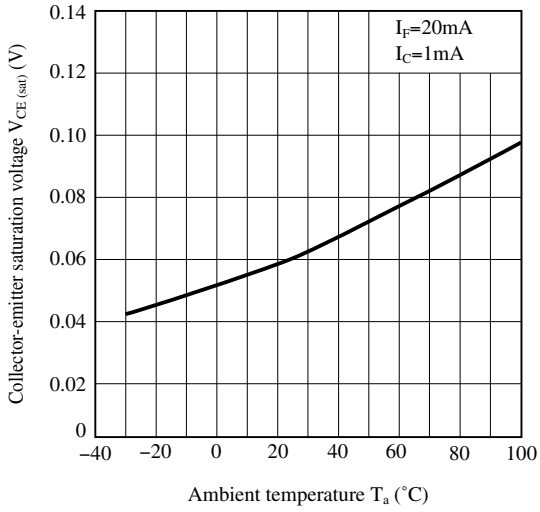


Fig.11 Collector Dark Current vs. Ambient Temperature

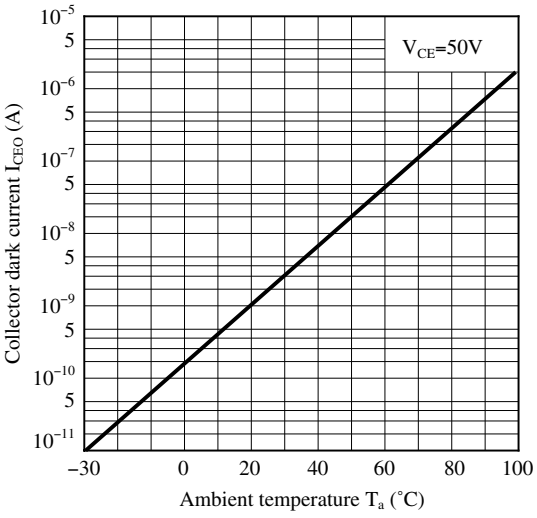


Fig.12 Collector-emitter Saturation Voltage vs. Forward Current

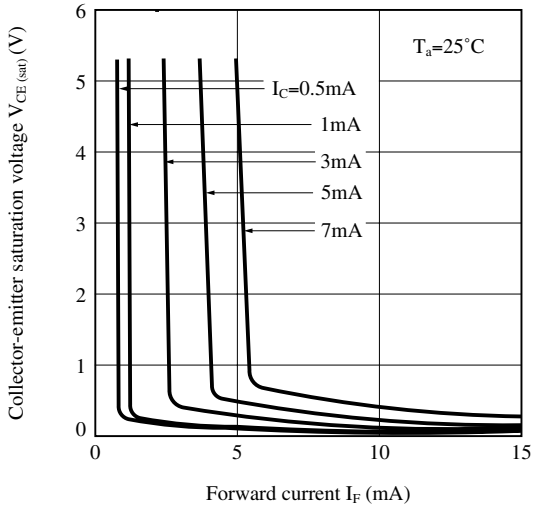


Fig.13 Response Time vs. Load Resistance

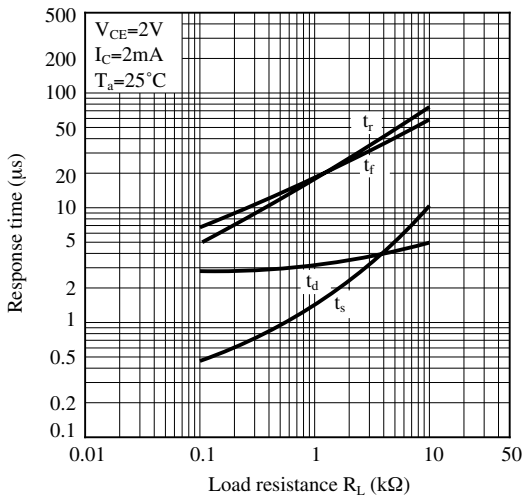
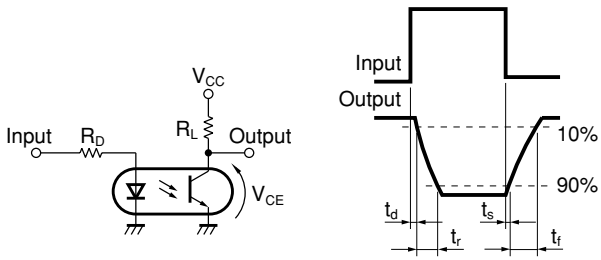


Fig.14 Test Circuit for Response Time



Please refer to the conditions in Fig.13.

Fig.15 Frequency Response

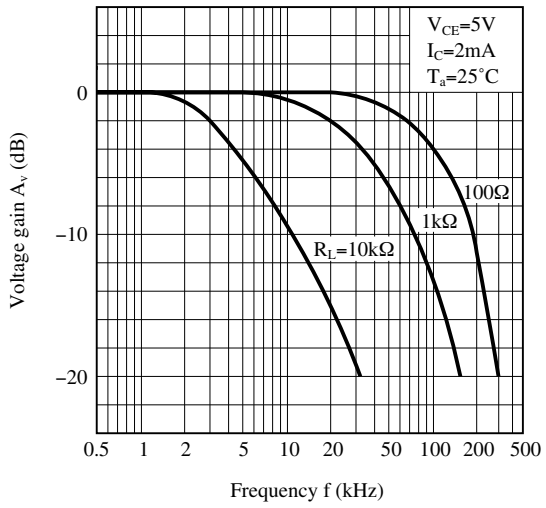
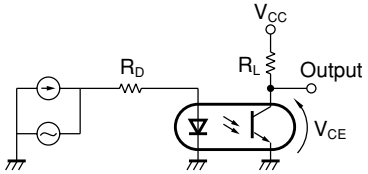


Fig.16 Test Circuit for Frequency Response



Please refer to the conditions in Fig.15.

Remarks : Please be aware that all data in the graph are just for reference and not for guarantee.

■ Design Considerations

● Design guide

While operating at I_F<1.0mA, CTR variation may increase.
Please make design considering this fact.

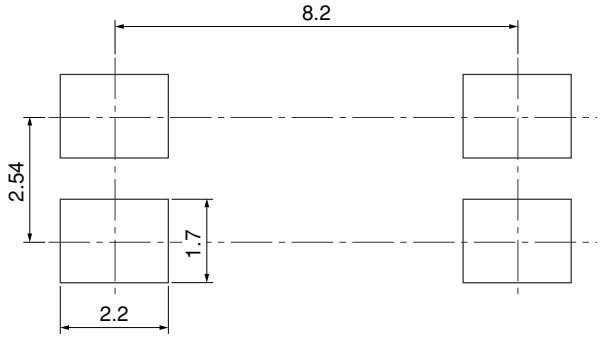
This product is not designed against irradiation and incorporates non-coherent IRED.

● Degradation

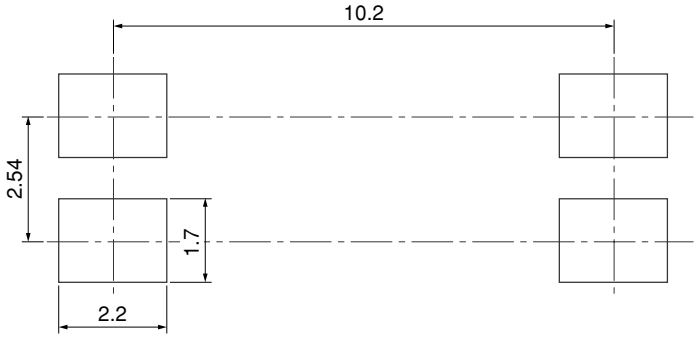
In general, the emission of the IRED used in photocouplers will degrade over time.
In the case of long term operation, please take the general IRED degradation (50% degradation over 5years) into the design consideration.

● Recommended Foot Print (reference)

SMT Gullwing Lead-form



Wide SMT Gullwing Lead-form



(Unit : mm)

☆ For additional design assistance, please review our corresponding Optoelectronic Application Notes.

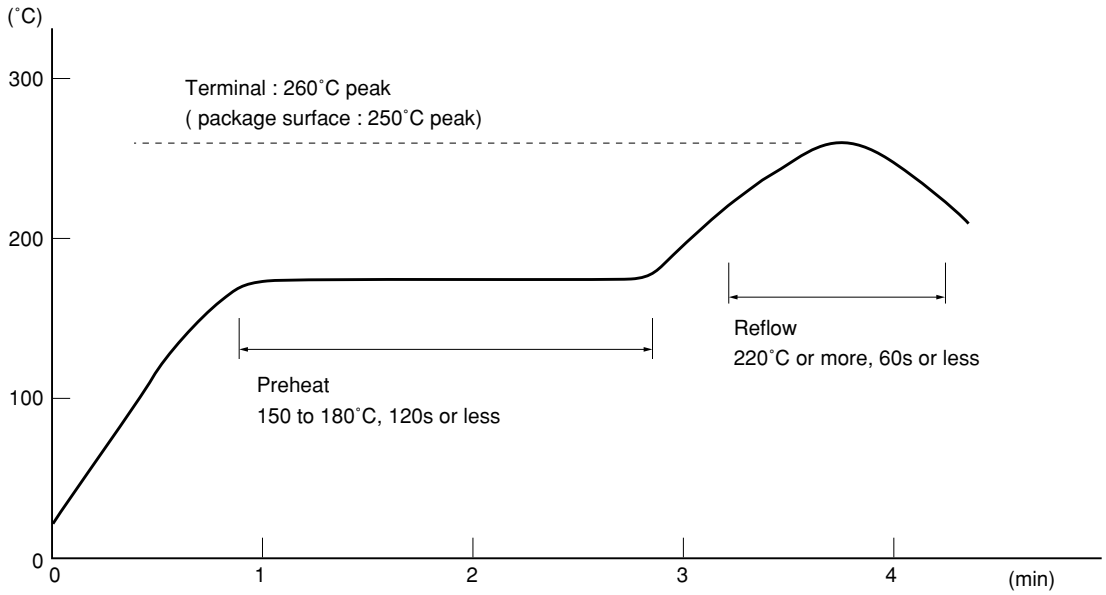
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■ Manufacturing Guidelines

● Soldering Method

Reflow Soldering:

Reflow soldering should follow the temperature profile shown below.
Soldering should not exceed the curve of temperature profile and time.
Please don't solder more than twice.



Flow Soldering :

Due to SHARP's double transfer mold construction submersion in flow solder bath is allowed under the below listed guidelines.

Flow soldering should be completed below 270˚C and within 10s.
Preheating is within the bounds of 100 to 150˚C and 30 to 80s.
Please don't solder more than twice.

Hand soldering

Hand soldering should be completed within 3s when the point of solder iron is below 400˚C.
Please don't solder more than twice.

Other notices

Please test the soldering method in actual condition and make sure the soldering works fine, since the impact on the junction between the device and PCB varies depending on the tooling and soldering conditions.

● Cleaning instructions

Solvent cleaning:

Solvent temperature should be 45˚C or below Immersion time should be 3minutes or less

Ultrasonic cleaning:

The impact on the device varies depending on the size of the cleaning bath, ultrasonic output, cleaning time, size of PCB and mounting method of the device.
Therefore, please make sure the device withstands the ultrasonic cleaning in actual conditions in advance of mass production.

Recommended solvent materials:

Ethyl alcohol, Methyl alcohol and Isopropyl alcohol
In case the other type of solvent materials are intended to be used, please make sure they work fine in actual using conditions since some materials may erode the packaging resin.

● Presence of ODC

This product shall not contain the following materials.
And they are not used in the production process for this device.
Regulation substances:CFCs, Halon, Carbon tetrachloride, 1.1.1-Trichloroethane (Methylchloroform)
Specific brominated flame retardants such as the PBBOs and PBBs are not used in this product at all.

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■ Package specification

● Sleeve package

1. Through-Hole or SMT Gullwing Lead-Form

Package materials

Sleeve : HIPS (with anti-static material)

Stopper : Styrene-Elastomer

Package method

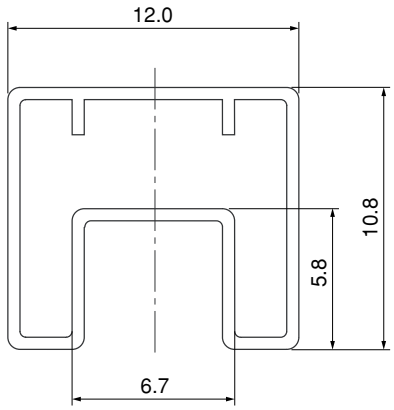
MAX. 100pcs of products shall be packaged in a sleeve.

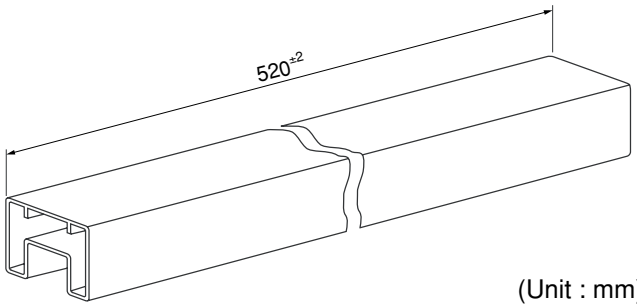
Both ends shall be closed by tabbed and tabless stoppers.

The product shall be arranged in the sleeve with its anode mark on the tabless stopper side.

MAX. 20 sleeves in one case.

Sleeve outline dimensions





(Unit : mm)

2. Wide Through-Hole Lead-Form or Wide SMT Gullwing Lead-Form

Package materials

Sleeve : HIPS (with anti-static material)

Stopper : Styrene-Elastomer

Package method

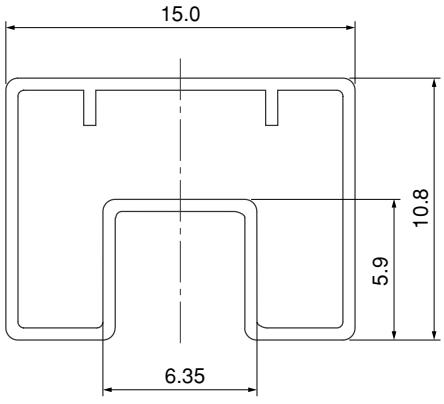
MAX. 100pcs of products shall be packaged in a sleeve.

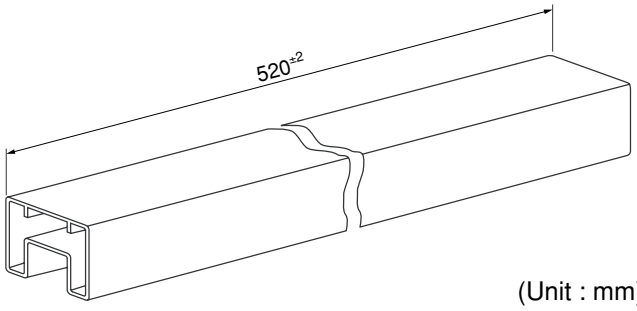
Both ends shall be closed by tabbed and tabless stoppers.

The product shall be arranged in the sleeve with its anode mark on the tabless stopper side.

MAX. 20 sleeves in one case.

Sleeve outline dimensions





(Unit : mm)

● Tape and Reel package

1. SMT Gullwing

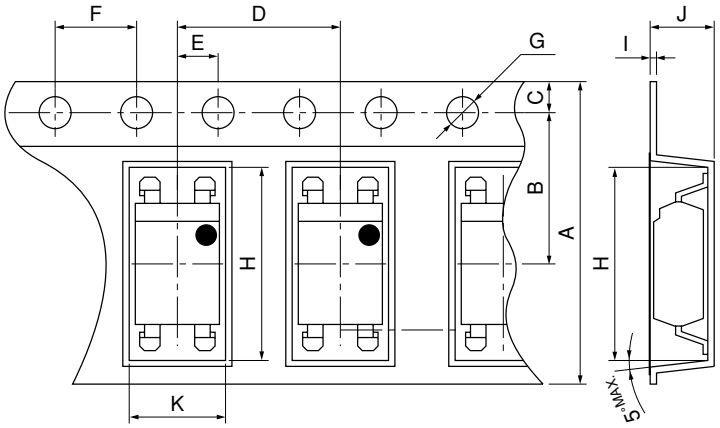
Package materials

Carrier tape : PS

Cover tape : PET (three layer system)

Reel : PS

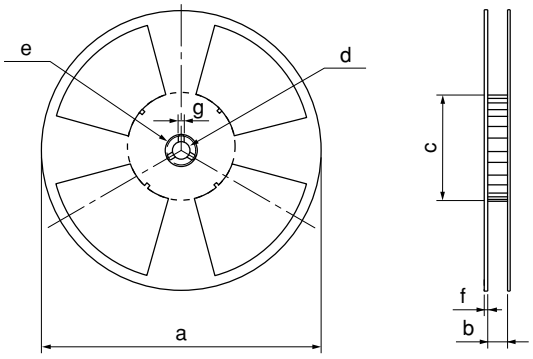
Carrier tape structure and Dimensions



Dimensions List (Unit : mm)

A	B	C	D	E	F	G
$16.0^{\pm0.3}$	$7.5^{\pm0.1}$	$1.75^{\pm0.1}$	$8.0^{\pm0.1}$	$2.0^{\pm0.1}$	$4.0^{\pm0.1}$	$\phi1.5^{+0.1}_{-0}$
H	I	J	K			
$10.4^{\pm0.1}$	$0.4^{\pm0.05}$	$4.2^{\pm0.1}$	$5.1^{\pm0.1}$			

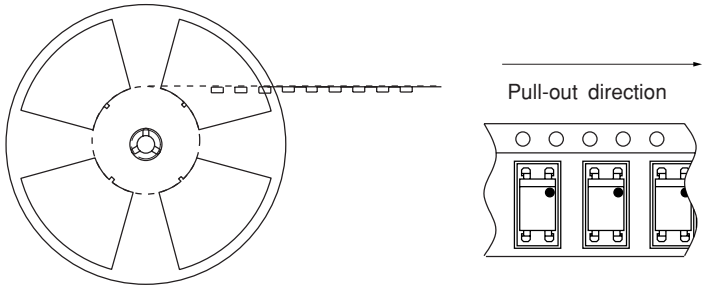
Reel structure and Dimensions



Dimensions List (Unit : mm)

a	b	c	d
330	$17.5^{\pm1.5}$	$100^{\pm1.0}$	$13^{\pm0.5}$
e	f	g	
$23^{\pm1.0}$	$2.0^{\pm0.5}$	$2.0^{\pm0.5}$	

Direction of product insertion



[Packing : 2 000pcs/reel]

2. Wide SMT Gullwing

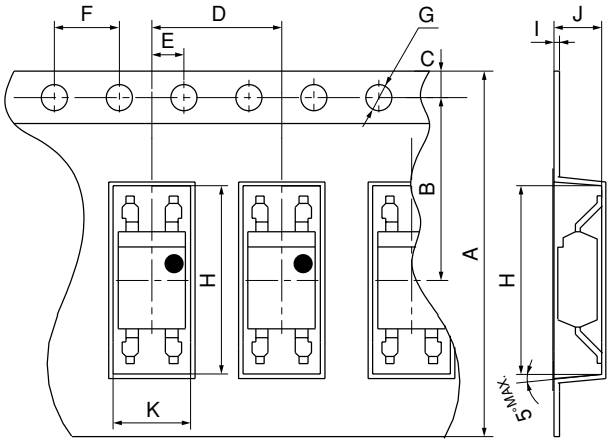
Package materials

Carrier tape : PS

Cover tape : PET (three layer system)

Reel : PS

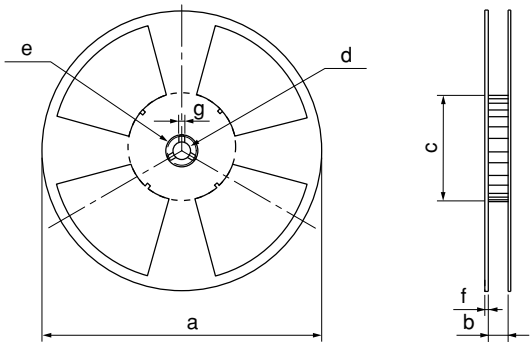
Carrier tape structure and Dimensions



Dimensions List (Unit : mm)

A	B	C	D	E	F	G
$24.0^{\pm0.3}$	$11.5^{\pm0.1}$	$1.75^{\pm0.1}$	$8.0^{\pm0.1}$	$2.0^{\pm0.1}$	$4.0^{\pm0.1}$	$\phi1.5^{+0.1}_{-0}$
H	I	J	K			
$12.4^{\pm0.1}$	$0.4^{\pm0.05}$	$4.1^{\pm0.1}$	$5.1^{\pm0.1}$			

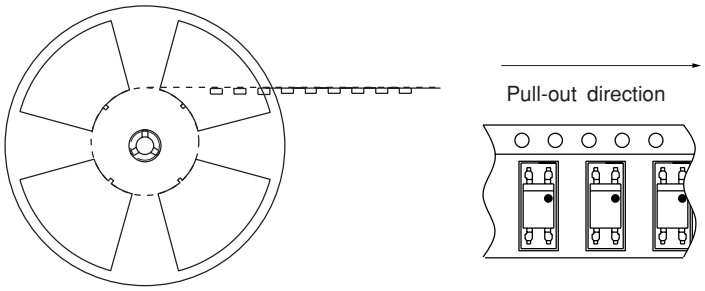
Reel structure and Dimensions



Dimensions List (Unit : mm)

a	b	c	d
330	$25.5^{\pm1.5}$	$100^{\pm1.0}$	$13^{\pm0.5}$
e	f	g	
$23^{\pm1.0}$	$2.0^{\pm0.5}$	$2.0^{\pm0.5}$	

Direction of product insertion



[Packing : 2 000pcs/reel]

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· The circuit application examples in this publication are provided to explain representative applications of SHARP devices and are not intended to guarantee any circuit design or license any intellectual property rights. SHARP takes no responsibility for any problems related to any intellectual property right of a third party resulting from the use of SHARP's devices.

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(i) The devices in this publication are designed for use in general electronic equipment designs such as:
--- Personal computers
--- Office automation equipment
--- Telecommunication equipment [terminal]
--- Test and measurement equipment
--- Industrial control
--- Audio visual equipment
--- Consumer electronics
(ii) Measures such as fail-safe function and redundant design should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that requires higher reliability such as:
--- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
--- Traffic signals
--- Gas leakage sensor breakers
--- Alarm equipment
--- Various safety devices, etc.
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--- Telecommunication equipment [trunk lines]
--- Nuclear power control equipment
--- Medical and other life support equipment (e.g., scuba).

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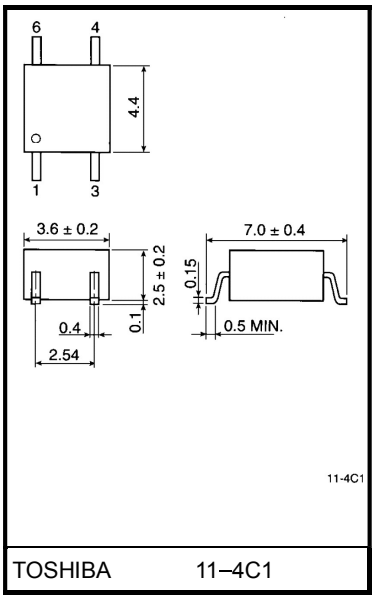
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TOSHIBA Photocoupler GaAℓAs Ired & Photo−Diode Array

TLP190B

Telecommunications
Programmable Controllers
MOS Gate Drivers
MOSFET Gate Drivers

Unit: mm



TOSHIBA 11−4C1

Weight: 0.09 g (typ.)

The TOSHIBA TLP190B mini-flat photocoupler is suitable for surface-mount assembly.
The TLP190B consists of a GaAℓAs light emitting diode optically coupled to a series connected photodiode array which is suitable for MOSFET gate drivers.

- Open voltage: 7.0V (min)
- Short current: 12.0 μA (min)
- Isolation voltage: 2500 Vrms (min)
- UL recognized: UL1577, file no. E67349

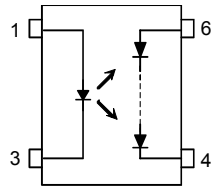
Short Current

Type Name	Classification	Short Current		Marking of Classification
		(min)	I_F	
TLP190B	C20	20 μA	10 mA	20
	Standard	12 μA		20, blank

Note: Application type name for certification test, please use standard product type name, i.e.

TLP190B(C20) : TLP190B

Pin Configuration (top view)



1. Anode
3. Cathode
4. Cathode
6. Anode

Start of commercial production
1990/11

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Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I_F	50	mA
	Forward current derating (Ta ≥ 25°C)	ΔI_F / °C	–0.5	mA / °C
	Pulse forward current (100μs pulse 100pps)	I_{FP}	1	A
	Reverse voltage	V_R	3	V
	Junction temperature	T_j	125	°C
Detector	Forward current	I_{FD}	50	μA
	Reverse voltage	V_{RD}	10	V
	Junction temperature	T_j	125	°C
Storage temperature range		T_{stg}	–55 to 125	°C
Operating temperature range		T_{opr}	–40 to 85	°C
Lead soldering temperature (10 s)		T_{sol}	260	°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) Note 1		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Device considered a two terminal device: Pins 1 and 3 shorted together and pins 4 and 6 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Forward current	I_F	—	20	25	mA
Operating temperature	T_{opr}	–25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Chic Electrics, Exhibit 1023
Shenzhen Chic Electrics v. Pilot

Individual Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
LED	Forward voltage	V_F	I_F = 10 mA	1.2	1.4	1.7	V
	Reverse current	I_R	V_R = 3 V	—	—	10	μA
	Capacitance	C_T	V = 0, f = 1 MHz	—	30	60	pF
Detector	Forward voltage	V_{FD}	I_{FD} = 10 μA	—	7	—	V
	Reverse current	I_{RD}	V_{RD} = 10 V	—	1	—	nA
	Capacitance (anode to cathode)	C_{TD}	V = 0, f = 1 MHz	—	—	—	pF

Coupled Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Open voltage	V_{OC}	I_F = 10 mA	7	8	—	V
Short current	I_{SC}	I_F = 10 mA	12	20	—	μA

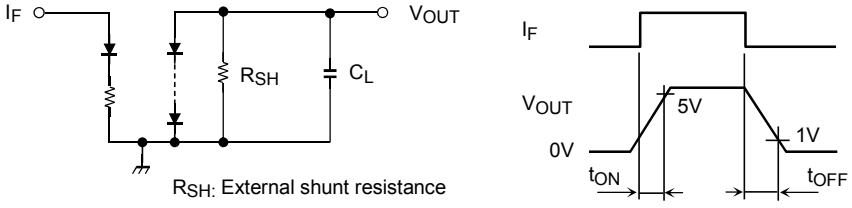
Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V_S = 0, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R_S	V_S = 500 V, R.H. ≤ 60%	5×10^{10}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	2500	—	—	Vrms
		AC, 1 second in oil	—	5000	—	
		DC, 1 minute in oil	—	5000	—	Vdc

Switching Characteristics (Ta = 25°C)

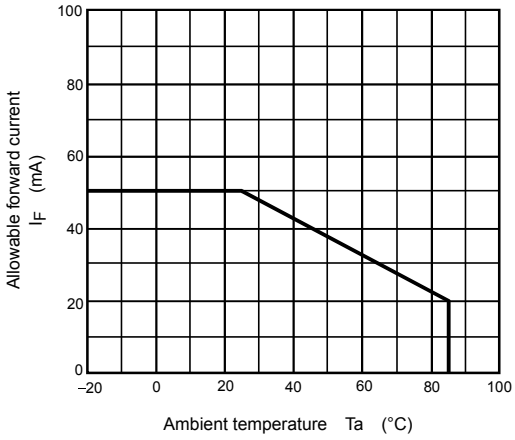
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Turn–on time	t_{ON}	I_F = 20 mA, R_{SH} = 510 kΩ	—	0.2	—	ms
Turn–off time	t_{OFF}	C_L = 1000pF (Fig. 1)	—	1	—	ms

Fig. 1 Switching time test circuit

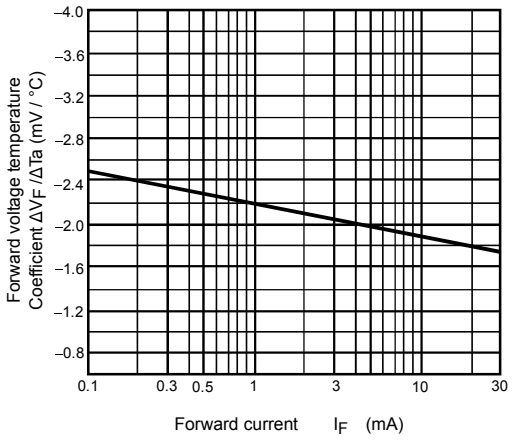


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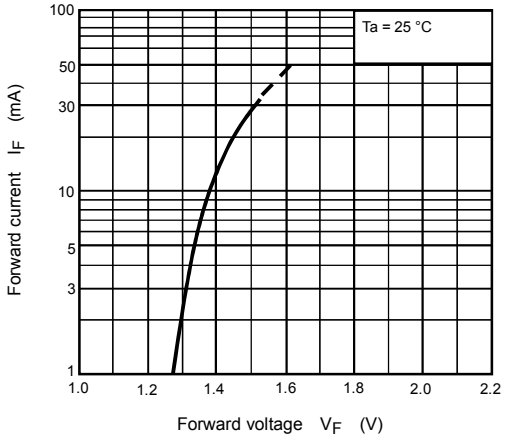
I_F – Ta



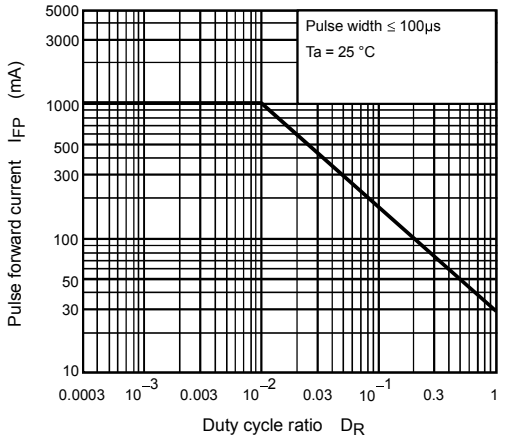
$\Delta V_F / \Delta Ta$ – I_F



I_F – V_F

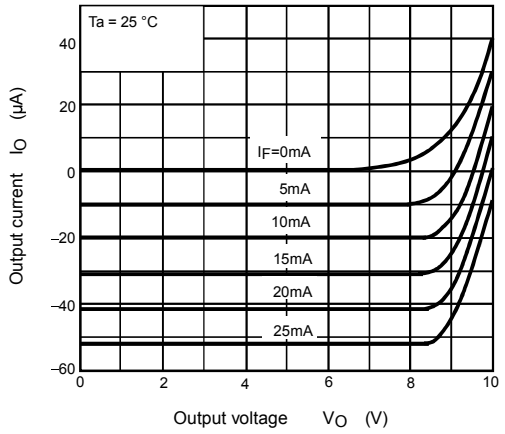


I_{FP} – D_R

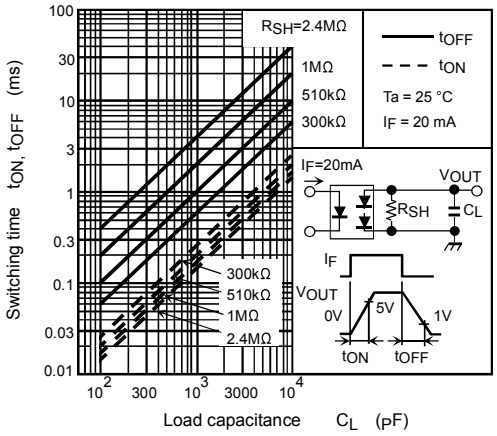


Chic Electrics, Exhibit 1023
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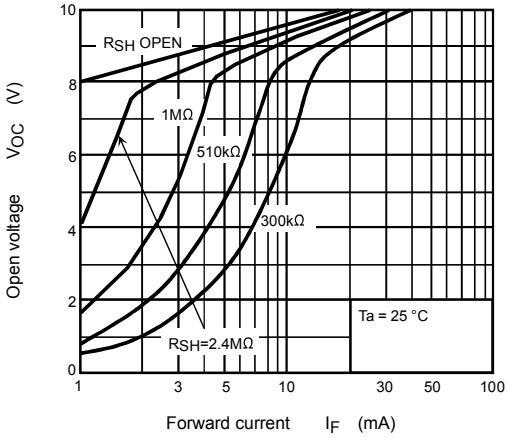
$I_O - V_O$



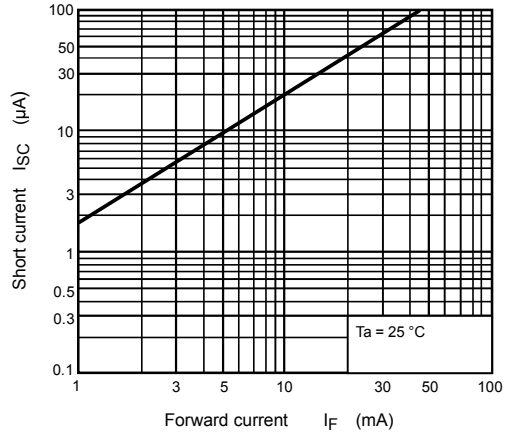
$t_{ON}, t_{OFF} - C_L$



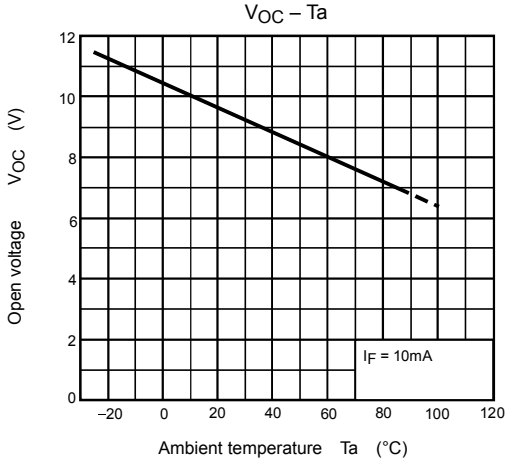
$V_{OC} - I_F$



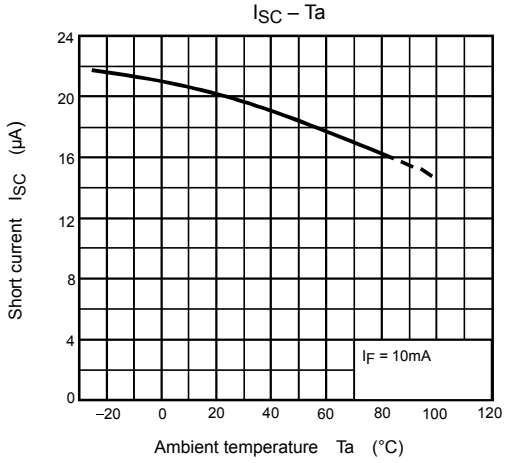
$I_{SC} - I_F$



$V_{OC} - Ta$



$I_{SC} - Ta$



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APPLICATION NOTE

AN1535
Rev 0.00
Jul 14, 2010

Prevent Reverse Charging of a Lithium Battery to Meet UL Safety Requirement

Introduction

Lithium batteries are commonly used in many applications with devices requiring backup power, such as Real Time Clock (RTC) and memory devices.

Whenever lithium batteries are not the single power source in a circuit, there is risk of fire or explosion if the battery is accidentally connected with an electrical power source that would charge the battery.

This application note provides information needed for connecting Lithium batteries in backup power switching circuits such that the circuit meets Underwriters Laboratories (UL) standards. Specifically, UL standard 60950-1 describes the guidelines for Lithium batteries.

Protection Circuit

Protection Circuit for Intersil's RTCs with Battery Switchover Feature

All Intersil's RTCs with a Battery Switchover feature, such as the ISL12026 series, have internal protection circuit to prevent reverse charging. Figure 1 shows the internal switchover circuitry illustrating the complementary control which disables one supply input while enabling the other. The two series MOSFET switches provide safe switching with redundancy. The is also a path from V_{DD} to V_{BAT} through a MOSFET (M1) used to pull-up the V_{BAT} switch gate, and two 200Ω resistors (R1 and R2). If the M1 gate is shorted, the current through resistors R1 and R2 limits the charging current to the Lithium battery (Up to 9.25mA for V_{DD} = 5.5V, V_{BAT} = 1.8V).

(A detailed schematic of the battery switchover control block is available upon request.

In order to meet full UL safety requirements, a series Schottky diode needs to be added to the V_{BAT} input for these products. The external diode is used to provide protection in the event that the internal MOSFET and series resisters should fail. Figure 2 shows the actual circuit with the external protection diode. (Note that a high value series resistor would provide similar protection, but would limit normal operating range.)

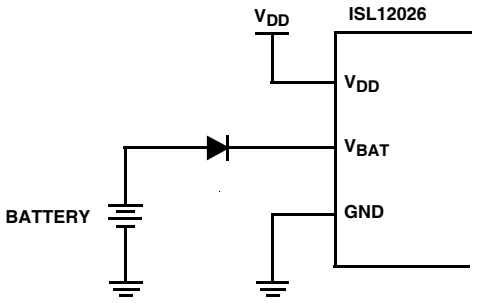


FIGURE 2. PROTECTION CIRCUIT WITH AN EXTERNAL DIODE)

Only use a silicon diode or Schottky diode having a low reverse current. A typical maximum reverse current of 1µA is recommended by UL. A few diodes that can be used that exhibit low reverse current include, but are not limited to, the BAS40, BAS70, and BAT54 diodes.

The reverse current can also be calculated for a specific battery. The maximum reverse current of the diode for a specific battery is given in Equation 1:

$$Ir = \frac{Ic}{T} 1 \times 10^{6} \quad \text{(EQ. 1)}$$

where Ir is the maximum reverse current in µA, Ic is the total allowable charging amount of a battery in mAh, and T is the total usage time in hour.

Ic is given in Equation 2:

$$Ic = Qxtp \quad \text{(EQ. 2)}$$

where Q is the nominal capacity of the battery in mAh and tp is the total allowable charging period in percent.

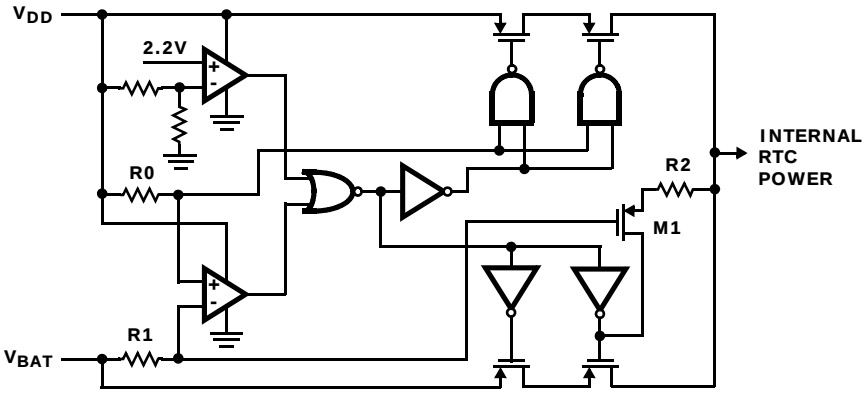


FIGURE 1. SIMPLIFIED BATTERY SWITCHOVER CIRCUIT

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For coin type battery, tp is 3%. For cylindrical battery, tp is 1%.

Example: A 1000mAh coin-type battery is to be used for five years.

With Equation 2, Ic is 30mAh (1000mAh x 3% (coin-type battery) = 30mAh).

With Equation 1, a diode with a reverse current of 0.7µA or less is required (30mAh ÷ usage period (5 years x 365 days x 24 hours) = 0.7µA).

Protection Circuit for Other Devices Without Internal Protection

For circuits that require a battery backup feature but either do not have a V_{BAT} pin or the V_{BAT} pin does not offer reverse charging protection, then a classic UL recommended three diode configuration is the best protection against reverse charging.

For example, the ISL12058 does not offer a battery switchover feature but an application requires it. The battery backup function can be added simply by connecting both main supply and backup battery to the V_{DD} pin. To have proper protection, a diode is placed in series with the main supply and two diodes are placed in series with the battery. The diode in series with the main supply is to block current from the battery into the main supply. Two diodes in series with the battery are to prevent reverse charging. The second diode is used to provide protection in the event that one should fail. Figure 3 shows the actual circuit with three diodes protection.

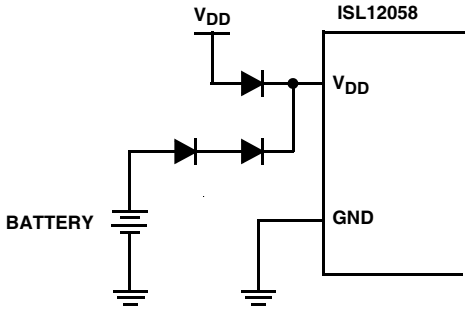


FIGURE 3. PROTECTION CIRCUIT WITH THREE DIODES

Testing

To insure the protection diodes are properly installed for the reverse charging protection, a simple test sequence is required after installation of the diodes.

A forced reverse charging test is done to insure the diodes are placed correctly to prevent reverse charging current to the battery. This is done by taking V_{DD} to 3.6V. The battery input is then forced to 1.8V and the charging current is check with an ampmeter capable of measuring current as low as 100nA to insure that it does not exceed the maximum reverse current of the protection diode. The test circuit is shown in Figure 4.

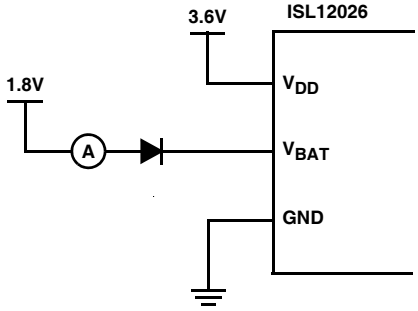


FIGURE 4. TEST CIRCUIT FOR REVERSE CHARGING PROTECTION

Conclusion

Lithium batteries are commonly used in a wide range of applications with devices requiring backup power, such as RTCs and memory devices. In order to meet UL standards for maximum charging (leakage) current, extra circuitry is required such as low leakage diodes even though a protected device has internal reverse charging protection. For a system with supplies other than the lithium battery, diode protection is not required but may be put in place to prevent any reverse charging from occurring.

Appendix

A) Intersil devices that require one diode in series (Figure 2 on page 1) with the V_{BAT} pin for UL requirements: ISL1208, ISL1209, ISL1218, ISL1219, ISL1220, ISL1221, ISL12020, ISL12020M, ISL12022, ISL12022M, ISL12024, ISL12025, ISL12026, ISL12027, ISL12028, ISL12029.

B) Intersil devices that require two diode in series (Figure 3) for UL requirements: ISL12057, ISL12058, ISL12059.

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