

Reference Point 3 Specification

Version 4.2

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FOREWORD

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1 Summary of Changes

Version	Approved by	Date	Comment
1.0	OBSAI Management Board	16/04/2004	Initial Release
2.0	OBSAI Management Board	11/10/2004	Second Release – incorporating remote head operation
3.0	OBSAI Management Board	01/08/2005	Third Release – incorporating WiMAX support
3.1	OBSAI Management Board	13/11/2006	Point Release – incorporating 4x line rate electrical specifications and related Type3 interconnect definition
4.0	OBSAI Management Board	3/7/2007	Fourth Release - incorporating LTE support
4.0.11	Release candidate	27/06/2008	Point Release – incorporating 8x (6144Mbps) line rate electrical specifications and related Type4&5 interconnect definitions Generic Packet Mode added
	with some corrections		LTE TDD specific channel bandwidths 1.6 and 3.2 do not exist any more and they were removed from Appendix F. Editorial corrections (cross-references corrected) Explicitly 100Ω resistance added to tables in ch5.
4.1	OBSAI Management Board	14/7/2008	Approved by Management Board
4.1.1	Draft	02/9/2009	Sections 4.2.8, 4.2.9, 4.3.3, 4.4.9.3, 4.4.9.4, 6.2.6, and 6.2.6.2 modified.

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4.1.2	Draft	06/10/2009	Sections 4.2.9 and 4.4.10.4 modified. Message multiplexing and de-multiplexing section moved from transport layer to data link layer, to Section 4.2.10. Sections 4.4.3 (Application level routing) and 6.2.7 (Multi-hop RTT) added.
4.1.3	Draft	04/11/2009	Sections 6.2.7 (Multi-Hop RTT), 4.4.7 (Message Format – Type Field), and 4.4.4 (Message Transmission Rules) modified.
4.1.4	Draft	09/11/2009	Sections 4.4.9.4, 6.2.6 and 6.2.7 modified.
4.1.5	Draft	12/01/2010	Corrections have been made to the following sections: 4.2.8, 4.3, 4.3.1, 6.2.5, 6.2.6, 6.2.6.2, and 6.2.7.
4.1.6	Draft	13/01/2010	The following sections have been modified: 5.1, 5.2.5, and Appendix A.
4.2	OBSAI Management Board	18/03/2010	Approved by Management Board

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2 Scope

This document specifies the Reference Point 3 characteristics. Chapter 3 defines the connectivity between RF and baseband modules. The protocol stack for data transfer is defined in Chapter 4, excluding the electrical characteristics, which are specified in Chapter 5. The protocol stack for data transfer between the base station and Remote RF units is defined in Chapter 6. Configuration and management of the protocol is detailed in Chapter 7.

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3 Reference Point 3 Architecture

OBSAI Reference Point 3 (RP3) interface exists between RF and BB modules of a base station. In this chapter, architecture or connectivity between RF and baseband modules is specified.

Architecture related parameters are defined in Section 3.1. In Section 3.2, interface of RF and baseband modules toward RP3 is defined. Topology of RP3 is specified in Section 3.3. Inter-cabinet connections are considered in Section 3.4.

3.1 Parameter Definitions

A set of parameters is used to define the architecture characteristics of RP3. In Table 1, the values of all of the parameters are specified.

Table 1: Architecture related RP3 parameters and their values.

Parameter	Value	Description
K	9	Maximum number of pairs of unidirectional links with differential signalling in every RF and baseband module.
K_{RF_in}	$0 \le K_{RF\_in} \le 9$	Number of incoming links with differential signalling that are implemented to a RF module.
K_{RF_out}	$0 \le K_{RF\_out} \le 9$	Number of outgoing links with differential signalling that are implemented to a RF module
K_{BB_in}	$0 \le K_{BB\_in} \le 9$	Number of incoming links with differential signalling that are implemented to a baseband module.
K_{BB_out}	$0 \le K_{BB\_out} \le 9$	Number of outgoing links with differential signalling that are implemented to a baseband module
P	36	Number of connector pins that are allocated to RP3 differential signals in every RF and baseband module

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Parameter	Value	Description
M	Integer, value equal to or greater than 1.	Number of RF modules in a base station.
N	Integer, value equal to or greater than 1.	Number of baseband modules in a base station.

3.2 Module Interface Toward RP3

Each OBSAI compliant RF module shall have maximum K (see Table 1) pairs of unidirectional links with differential signalling toward RP3 interface, i.e. 2*K links in total. A pair constitutes one incoming signal and one outgoing signal. Each RF module shall implement K_{RF_in} incoming links, where $0 \le K_{RF\_in} \le K$, and K_{RF_out} outgoing links, where $0 \le K_{RF\_out} \le K$. Among the implemented links with differential signalling, unused links shall be disabled for power conservation purposes. Each link requires 2 pins due to differential signalling that is used. In total, there exist P pins in each RF module that are allocated to differential signals to support RP3 interface. Each RF module shall always have the same pins of a connector allocated to RP3 signals. Refer to [6] for detailed pin definition.

The RF module may contain transmit functionality only, receiver functionality only, or both transmit and receive functionality.

Each OBSAI compliant baseband module shall have maximum K (see Table 1) pairs of unidirectional links with differential signalling toward RP3 interface, i.e. 2*K links in total. A pair constitutes one incoming signal and one outgoing signal. Each baseband module shall implement K_{BB_in} incoming links, where $0 \le K_{BB\_in} \le K$, and K_{BB_out} outgoing links, where $0 \le K_{BB\_out} \le K$. Among the implemented links with differential signalling, unused links shall be disabled for power conservation purposes. Each link requires 2 pins due to differential signalling that is used. In total, there exist P pins in each baseband module that are allocated for differential signals to support RP3 interface. Each baseband module shall always have the same pins of a connector allocated to RP3 signals. Refer to [5] for detailed pin definition.

Differential signalling is used at the lowest protocol layer at RP3 interface. On each link, bus protocol as specified in Chapter 4 shall be applied.

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Figure 1 illustrates RP3 interface of RF and baseband modules. A pair of unidirectional links with differential signalling is shown in the figure as a double-ended arrow.

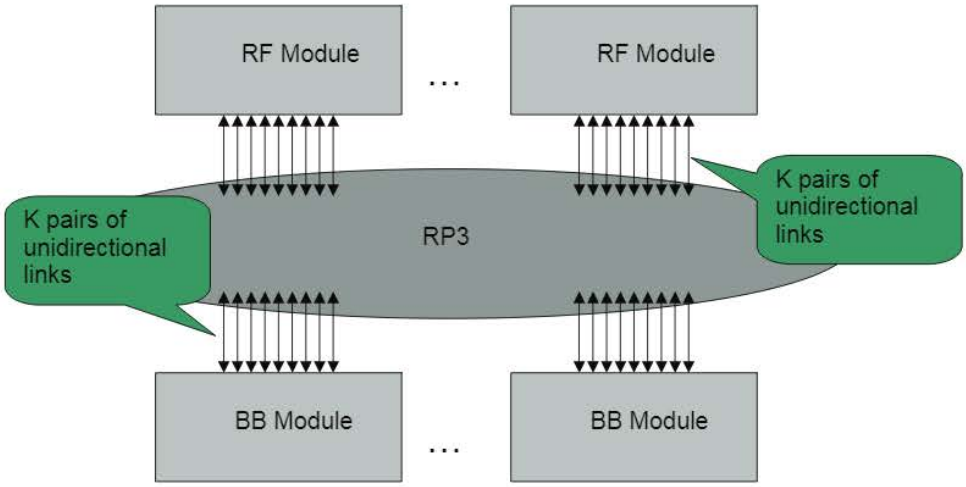


Figure 1: RP3 interface of RF and baseband modules. There exists a maximum of K pairs of unidirectional links toward RP3.

3.3 Topology

Topology specifies connectivity between RF and baseband modules. Two approaches are suggested (but not mandated): mesh and centralized combiner and distributor. They are explained in more detail below.

3.3.1 Mesh

Assuming *N* baseband and *M* RF modules in a base station, there exist in total *N*M* pairs of unidirectional links with differential signalling between baseband and RF modules in a full mesh. Each baseband module is connected to *M* RF modules while every RF module is connected to *N* baseband modules. Each pair of unidirectional links is implemented as two unidirectional differential signals in opposite directions for data and control transfer. Optionally, there may exist several parallel pairs of unidirectional links between any baseband and RF modules when very high data throughput is required. Connection between any pair of baseband and RF modules may also be missing if it is not required. When there does not exist any connection between a baseband module and an RF module, a partial mesh rather than full mesh is obtained.

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Each RF and baseband module has at maximum K pairs of unidirectional links. Therefore, K*K mesh at maximum can be supported but any combination, including asymmetrical combinations, up to this maximum is allowed.

Figure 2 illustrates a base station configuration with two baseband and three RF modules and a full mesh at RP3.

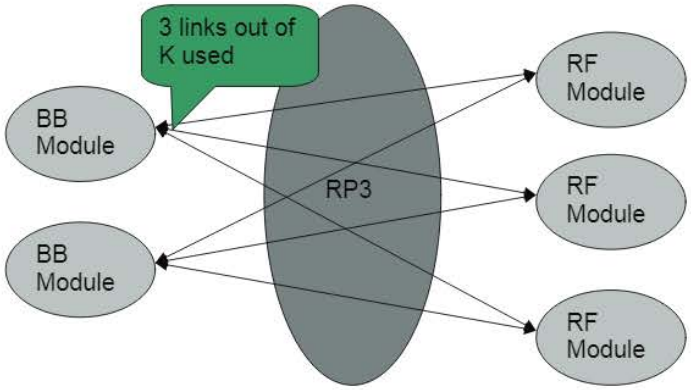


Figure 2: Full mesh connecting two baseband and three RF modules. Each baseband module is connected to every RF module and vice versa.

Figure 3 shows K-by-K full mesh.

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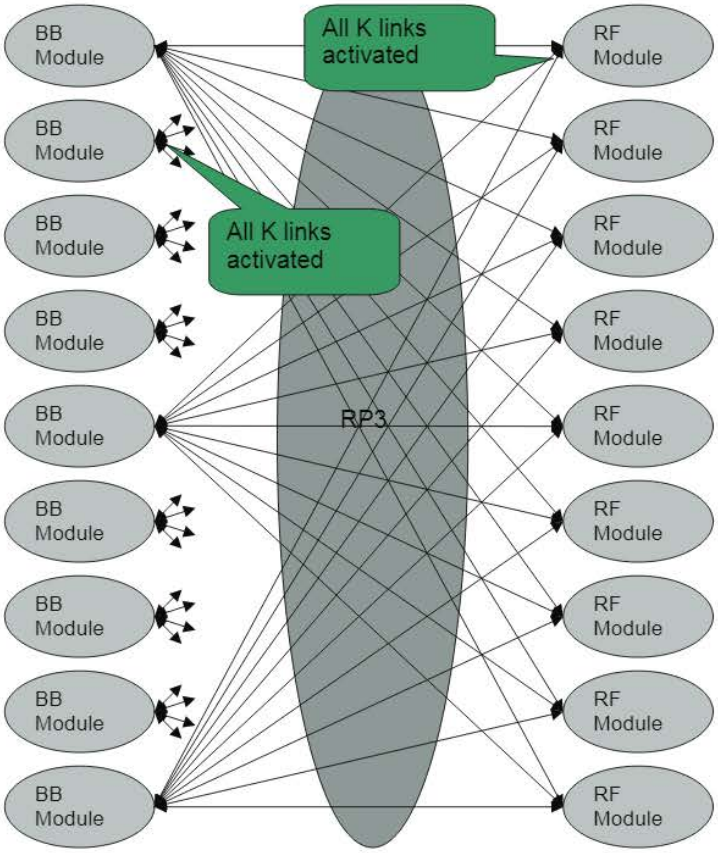


Figure 3: Full mesh connecting K baseband modules to K RF modules. All the connections are not drawn.

3.3.2 Centralized Combiner and Distributor

Assume *N* baseband and *M* RF modules in a base station maximum configuration. All links of both baseband and RF modules are connected to a centralized combiner and distributor (C/D) that is located in RP3. For each link, differential signalling is applied. In combining, input samples that are targeted to the same antenna and carrier at the same time instant are added together so that a single output sample stream is formed after which it is transmitted to the desired RF module(s). In distribution, RX sample stream from a RF module is distributed to all or to a subset of baseband modules. At maximum, K*(N+M) pairs of unidirectional links are connected to the combiner and distributor but any number of links below this maximum can be connected to combiner and distributor. For a given base station configuration, at maximum $\sum_{i=1}^{N} \mathrm{K}_{\mathrm{BB\_out}}[i] + \sum_{i=1}^{M} \mathrm{K}_{\mathrm{RF\_in}}[i]$ downlink

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unidirectional links and $\sum_{i=1}^{N} \mathrm{K}_{\mathrm{BB\_in}}[i] + \sum_{i=1}^{M} \mathrm{K}_{\mathrm{RF\_out}}[i]$ uplink unidirectional links are connected to the combiner and distributor. In these equations, $\mathrm{K}_{\mathrm{BB\_in}}[i]$ and $\mathrm{K}_{\mathrm{BB\_out}}[i]$ stand for number of incoming and outgoing links that are implemented to the i^{th} baseband module while $\mathrm{K}_{\mathrm{RF\_in}}[i]$ and $\mathrm{K}_{\mathrm{RF\_out}}[i]$ denote number of incoming and outgoing links that are implemented to the i^{th} RF module. Between any RF or baseband module and the centralized combiner and distributor, unused links shall be disabled for power conservation purposes.

In order to obtain better fault tolerance, a redundant combiner and distributor can be used. In full redundancy, all signals of every RF and baseband module are transferred through main and redundant combiner and distributor modules. Given maximum K pairs of unidirectional links per RF or baseband module, at maximum K-$\lfloor \mathrm{K}/2 \rfloor$ pairs of links from any module can be connected to main combiner and distributor and the remaining $\lfloor \mathrm{K}/2 \rfloor$ pairs of links can be connected to the redundant combiner and distributor, or vice versa, when redundancy is applied. $\lfloor \mathrm{X} \rfloor$ denotes the largest integer number equal to or less than X. Any number of links below this maximum can be connected to a combiner and distributor from a RF or baseband module. In load balancing redundancy, portion of the signals are transferred through the first combiner and distributor while rest of the signals are sent through the second combiner and distributor.

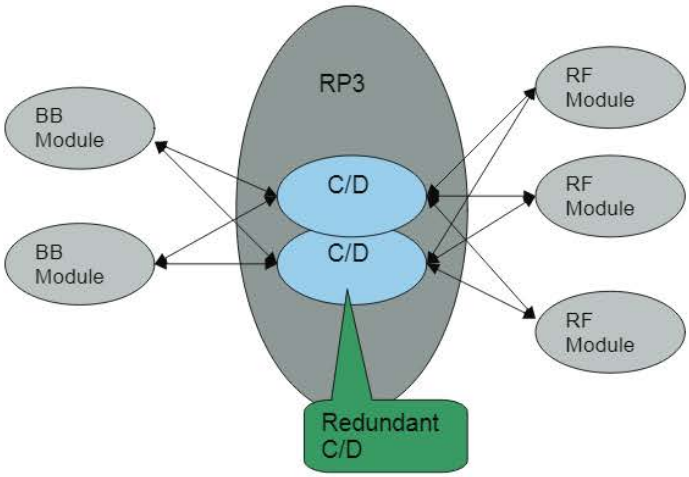


Figure 4: Centralized combiner and distributor (main and redundant) embedded into RP3 interface.

Figure 4 and Figure 5 illustrate centralized combiner and distributor topology with and without redundancy, respectively. Unlike in mesh

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approach, there now exist active component(s) in RP3. The same baseband and RF modules shall be used with mesh or centralized combiner and distributor topology.

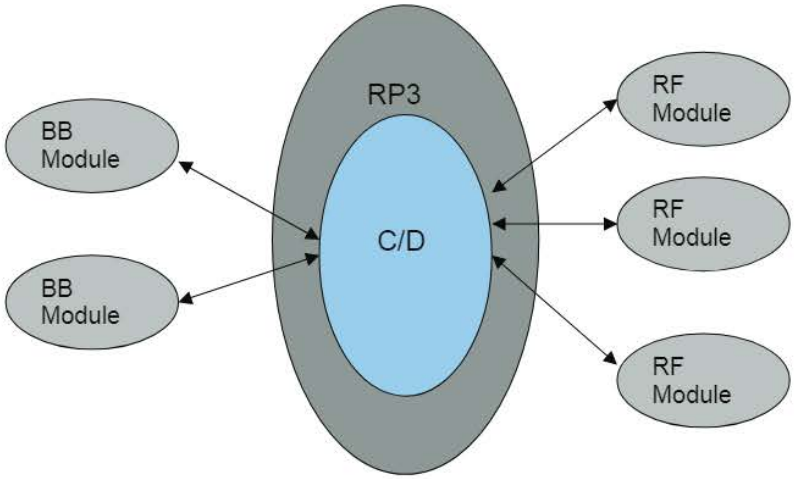


Figure 5: Centralized combiner and distributor embedded into RP3 interface. Redundant C/D is not applied.

3.4 Inter-Cabinet Connections

In very large configurations, a base station may be located in several cabinets and RF-baseband signal transfer between cabinets may be required. RP3 interface shall be used in inter-cabinet RF-baseband data transfers. Thus, differential signalling connections are used as well as the protocol stack defined in Chapter 4. Three topology options exist for inter-cabinet data transfers:

- Inter-cabinet mesh
- Links between bridge modules
- Links between centralized combiner and distributor modules

All these options are described in detail below. Two cabinet case is considered in this section. All the concepts presented can be generalized for X cabinet case where *X>2*.

3.4.1 Inter-Cabinet Mesh

Figure 6 illustrates the case where a full mesh exists between all baseband and RF modules in dual cabinet base station configuration.

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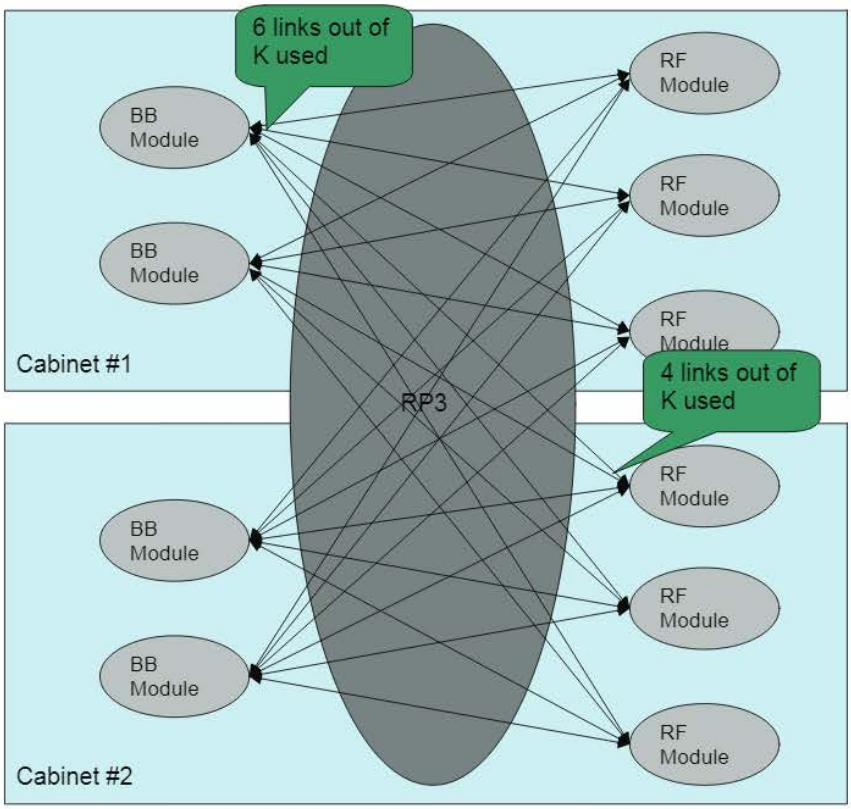


Figure 6: Full mesh between RF and baseband modules of two cabinets.

3.4.2 Connections between Bridge Modules

Figure 7 shows the second option for inter-cabinet communication. Now bridge modules are used that may simply forward data from cabinet to another. Bridge module is typically used in place of a baseband module and it can be used with intra-cabinet mesh or centralized combiner and distributor topologies.

Any baseband module of Cabinet #X can be connected to any RF module of Cabinet #Y when applying the bridge concept. Sufficient bandwidth in Baseband-to-RF links of Cabinet #X is assumed. In most simple implementation, bridge just forwards a set of differential signals from input to output. In a more advanced approach, bridge module is able to interchange data between links.

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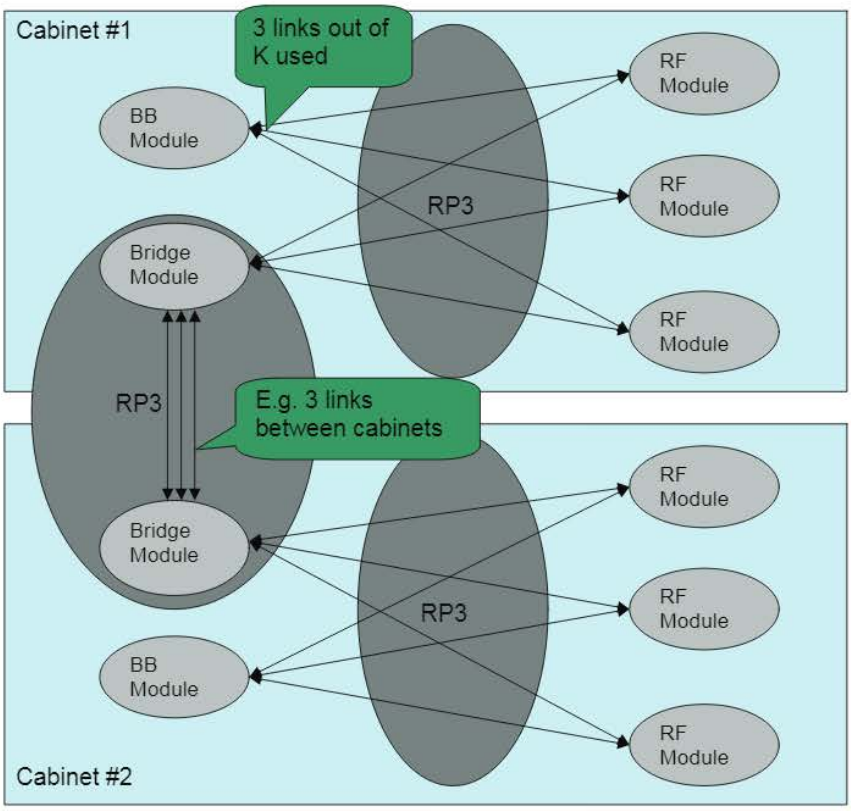


Figure 7: Bridge modules extending RP3 interface to two cabinets. Mesh topology is shown in intra-cabinet RF-baseband connections but also centralized combiner and distributor topology may be applied.

In order to obtain better fault tolerance, a redundant bridge module is typically used. Both the main and redundant bridge modules of the two cabinets shall be connected together.

3.4.3 Connections between Combiner and Distributor Modules

Figure 8 defines third option for inter-cabinet data transfer. When centralized combiner and distributor modules exist in RP3, these modules of different cabinets can be connected together. Both the main and redundant modules of the two cabinets shall be connected together.

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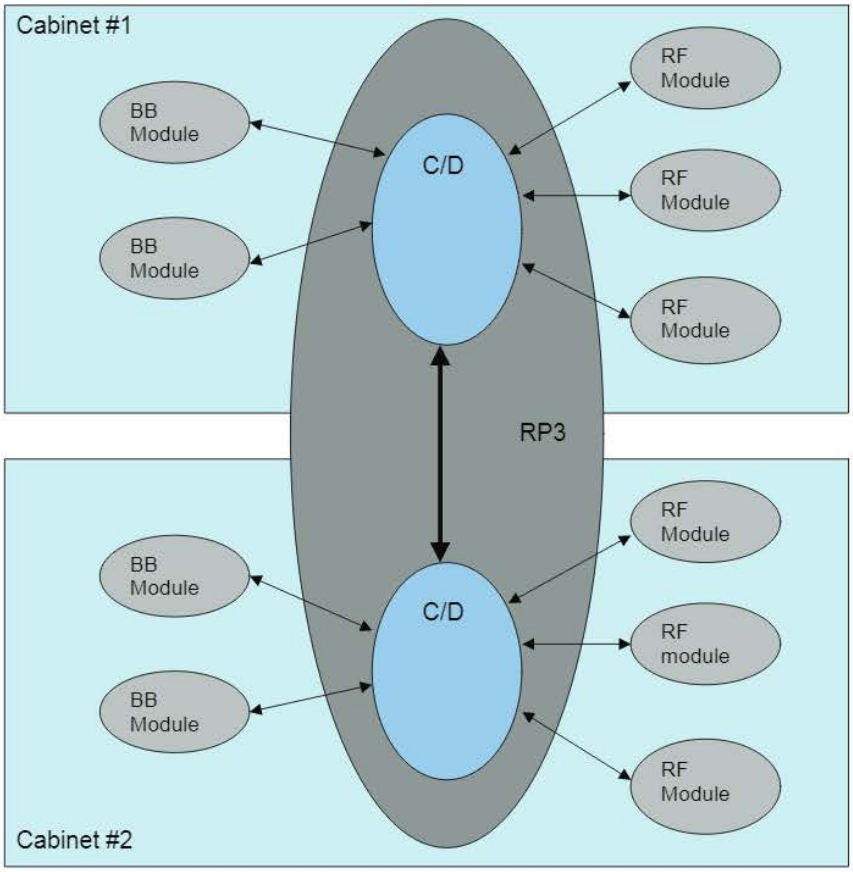


Figure 8: RP3 interface extended over two cabinets by connecting C/Ds together (redundant C/D not applied).

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4 Protocol Stack

The RP3 bus interface is a high-capacity, point-to-point serial interface bus for uplink and downlink telecom (user) data transfer and related control. The physical implementation of the bus is based on differential signalling technology. The protocol stack is based on a packet concept using a layered protocol with fixed length messages.

The bus protocol can be considered as a four-layer protocol consisting of

- **Application layer**, providing the mapping of different types of packets to the payload.
- **Transport layer**, responsible for the end-to-end delivery of the messages, which is simply routing of messages.
- **Data link layer,** responsible for framing of messages and message (link) synchronization
- **Physical layer**, responsible for coding, serialization, and transmission of data

This is illustrated below in Figure 9.

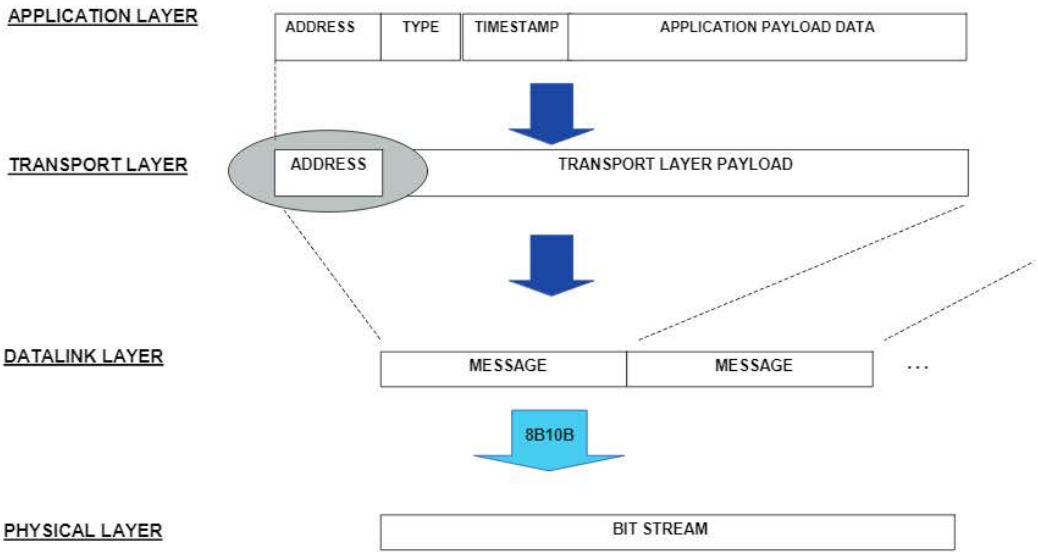


Figure 9: Layered structure of the bus protocol.

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4.1 Physical Layer

4.1.1 Electrical Signalling

Refer to Chapter 5 for a detailed specification on electrical characteristics of RP3 interface.

For conformance testing purposes, physical layer loopback shall be supported as illustrated in Figure ***10***.

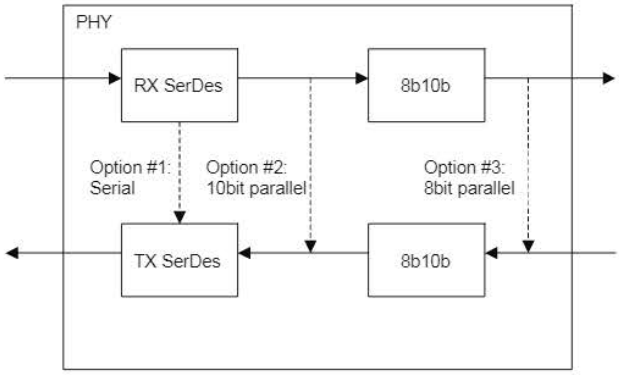


Figure 10: Illustration of possible physical layer loopback points.

4.1.2 Data Format and Line Coding

8b10b transmission code [1] shall be applied to all data that is transmitted over the RP3 bus. 8b10b transmission coding will provide a mechanism for serialization and clock recovery.

Figure ***11*** illustrates physical layer structure.

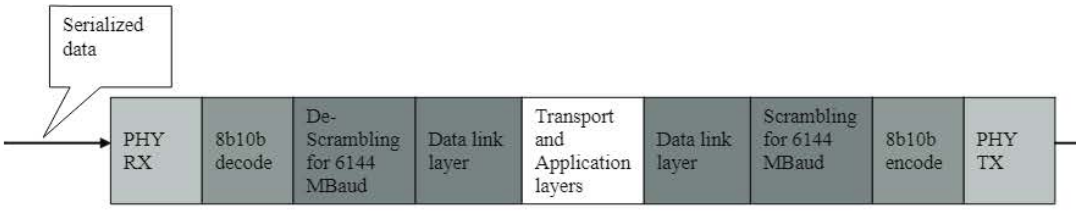


Figure 11: Illustration of Physical layer structure – data flow approach.

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Synchronization of physical layer receiver

In the Physical layer receiver, phase adjustments to the incoming signal are automatically done for each receiver port separately. Typically, phase adjustments are done when initialising the connection.

Line code violation detection

Physical layer, the 8b10b decoder, shall detect invalid line codes from the incoming serial bit stream. Each Line Code Violation (LCV), i.e. erroneously received byte, shall be indicated to Data link layer.

Physical layer, the 8b10b encoder, shall transmit K30.7 character to the link when Data link layer indicates that the byte to be transmitted contains an error.

4.1.3 Bus Clock

Physical layer of the bus is frequency and phase locked to a centralised BTS system clock [4]. In every bus node, byte clock for the bus is generated from BTS system clock and it equals to *Bus_line_Rate*/10 when bus line rate is expressed in baud units.

4.2 Data Link Layer

4.2.1 Message Overview

A fixed message format is used for all data that is transferred over the RP3 or RP3-01 (see Section 6) bus.

Figure *12* shows the message structure including partitioning of the message into bytes. In case of 6144Mbaud line rate, each byte of the message is scrambled and 8b10b encoded and then transmitted to a link. For other line rates, each byte of a message is first 8b10b encoded as shown in the figure and then transmitted to a link. 8b10b encoding is part of Physical layer functionality. The leftmost byte of the address field is first transmitted to the link while the rightmost byte of payload is last sent to the link. If data from other busses is transferred over the RP3 or RP3-01, it must be realigned such that Most Significant Bit (MSB) is transmitted first as defined in Figure 12.

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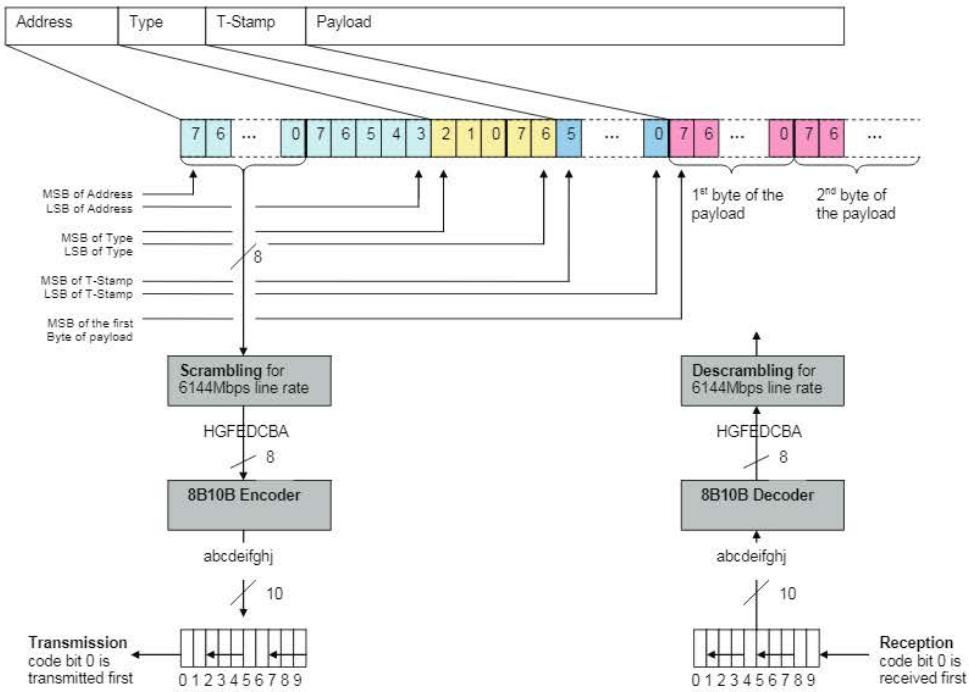


Figure 12: Message format of RP3 protocol stack.

Table 2 defines the size of each field of the message.

Table 2: Size of the message.

Field	Length (bits)
Address	13
Type	5
Time stamp (T-Stamp)	6
Payload	128
Total length	152 bits (=19 bytes)

4.2.2 Frame Structure

The protocol supports only fixed length messages of size 19 bytes as specified in Table 2.

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A block of data consisting of *M_MG* messages, 0<*M_MG*<65536, and *K_MG* IDLE bytes, 0<*K_MG*<*20,* is called a Message Group (MG). Consecutive Message Groups are transferred over a bus link. Master Frame length is fixed to 10 ms and it is composed of *i*N_MG,* where *0*<*N_MG*<*65536* and *i* ∈ {1, 2, 4, 8}, consecutive Message Groups for line rates *i*768*Mbps. Thus, any of the line rates 768 Mbps, 1536 Mbps, 3072, and 6144 Mbps can be applied. Parameters *M_MG* and *N_MG* must be selected such that $i*N\_MG*M\_MG < 2^{32}$ holds. Size of a Message Group equals to *M_MG*19+K_MG* bytes while Master Frame size in bytes is *i*N_MG*(M_MG*19+K_MG)*.

The *M_MG* message slots of a Message Group are divided into data and control slots. For a line rate *i*768* Mbps, the *i* last message slots of every i^{th} Message Group are control message slots while all other message slots are allocated for data message slots. In a Master Frame, there exist *i*N_MG* control message slots and Message Group with index *i-1,* where Message Group indices run from 0 to *i*N_MG-1,* is the first Message Group having control slots.

*K_MG i*dle codes K28.5 [1] exist at the end of each Message Group with one exception. Idle codes K28.7 are used to mark the end of a Master Frame, i.e. *K_MG* consecutive K28.7 codes exist at the end of last Message Group. A set of unique codes is used to mark the end of a Master Frame in order to facilitate reception.

There exists a large set of different Message Group and Master Frame definitions. Parameter set *M_MG*=21, *N_MG*=*i**1920, and *K_MG*=1 is recommended to be used for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards while parameter set *M_MG*=13, *N_MG*=*i**3072, and *K_MG*=3 is recommended for CDMA.

Figure 13 and Figure 14 Master Frames for WCDMA, GSM/EDGE, 802.16, LTE, and CDMA air interface standards for the 768 Mbps line rate (i=1).

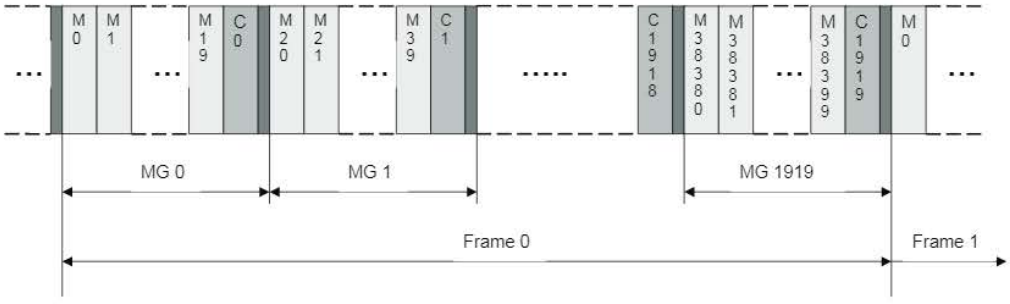


Figure 13: Master frame illustrating the sequence according to which WCDMA, GSM/EDGE, 802.16, and LTE messages are inserted to the bus (parameter set M_MG=21, N_MG=1920, K_MG=1, i = 1).

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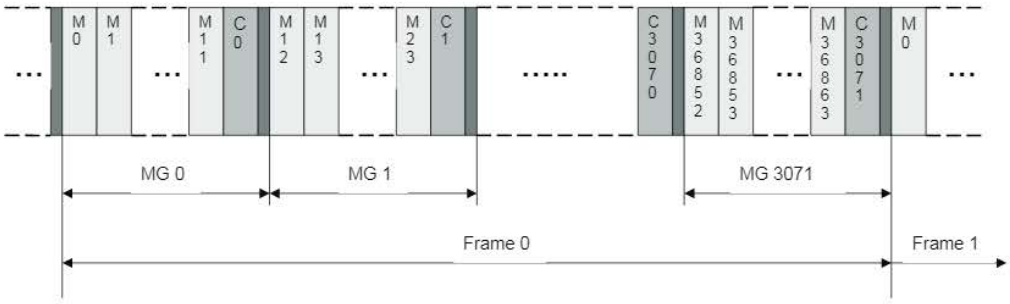


Figure 14: Master frame illustrating the sequence according to which CDMA messages are inserted to the bus (parameter set M_MG=13, N_MG=3072, K_MG=3, i =1).

Figure 15 illustrates Message Group structures for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards at all allowed line rates *i*768* Mbps, $i \in \{1, 2, 4, 8\}$.

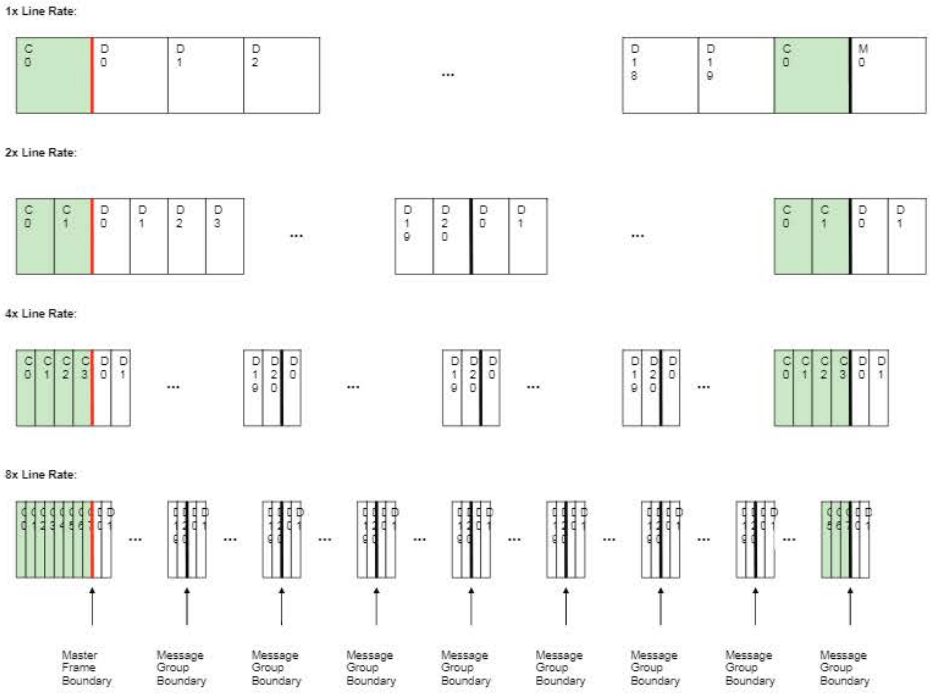


Figure 15: Message group structures for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards at 768 Mbps (1x), 1536 Mbps (2x), 3072 Mbps (4x), and 6144 Mbps (8x) line rates. Time span corresponding to a single message group at 768 Mbps line rate is shown.

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4.2.3 Bit Level Scrambling for 6144 Mbps (8x) Line Rate

Bit level scrambling shall be performed on 8x rate links to reduce cross talk between links as well as to reduce inter-Symbol interference (ISI). The RP3 transmitter shall apply a 7-degree polynomial to data bytes and the inverse operation shall be performed by the RP3 receiver. Scrambling only pertains to 6144 Mbps operation (8x link rate). Link rates {1x, 2x, 4x} are backward compatible with no scrambling applied.

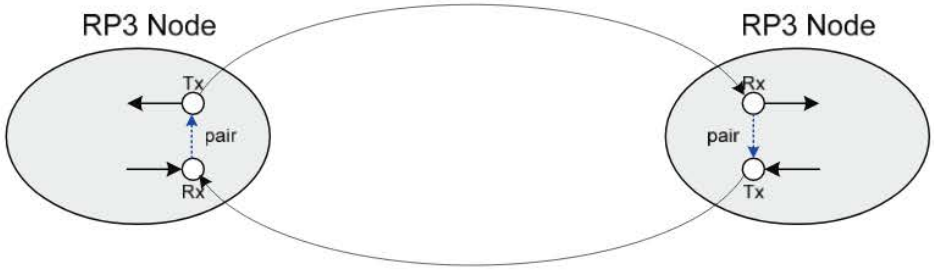


Figure 16: Scrambling Pattern Passed Between Two Adjacent RP3 Nodes.

Cross talk between transmitters through the local SERDES power supply is the main concern. With all transmitters having differing scrambling offsets, randomness between transmitting lanes is achieved. The assignment of unique scrambler offsets for receivers is optional as cross talk between receivers and transmitters is non-critical.

The RP3 transmitter is configured by higher layers, setting the starting value of the 7-degree polynomial scrambling code generator. Higher layers shall configure unique seed values for adjacent RP3 Tx links. The following table illustrates the available seed value to be used. These seed values represent nx7 position offsets (nx7 has been specifically chosen to give an odd offset between adjacent links). The RP3 receiver is a slave to the transmitter, receiving the seed value in a training sequence.

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Table 3: Scrambler Seed Values.

Nx7 Index	X^7	X^6	X^5	X^4	X^3	X^2	X^1
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
2	0	0	0	0	1	0	1
3	0	0	0	1	1	1	1
4	0	0	1	0	0	0	1
5	0	1	1	0	0	1	1
6	1	0	1	0	1	0	0
7	1	1	1	1	1	0	1
8	0	0	0	0	1	1	1
9	0	0	0	1	0	0	1
10	0	0	1	1	0	1	1
11	0	1	0	1	1	0	1
12	1	1	1	0	1	1	0
13	0	0	1	1	0	1	0
14	0	1	0	1	1	1	0
15	1	1	1	0	0	1	1
16	0	0	1	0	1	0	1
17	0	1	1	1	1	1	1

The scrambling shall follow the rules below:

The scrambling code generator increments by one bit position for each bit of every byte. In each bit position of the scrambling code generator a single scrambling bit is created which is XOR with each single bit of a data byte. The bits of a byte are processed in order from the MSB to the LSB corresponding to the order in which the scrambling bit sequence is generated. On every K28.5 or K28.7 character, the scrambling code generator is reset to the starting seed value.

The seed value and checking sequence is transmitted as training patterns from the RP3 transmitter to the receiver during the IDLE period of the transmit state machine. Only 8x rate links use these special patterns during the IDLE period. There are two sub-states in the IDLE state IDLE_REQ and IDLE_ACK; two different training patterns are transmitted in the two sub-states:

- IDLE_REQ: K28.5, byte0, …, byte15… repeat
- IDLE_ACK: K28.5, K28.5, byte0, …, byte15… repeat

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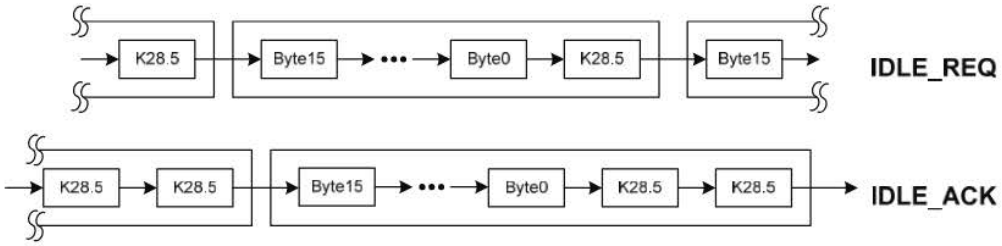


Figure 17: Scrambling Training Patterns.

In practice, the 16 byte training pattern is created by passing sixteen zero bytes (D.0.0) through the RP3 transmitter scrambler. The K28.5 preceding the training pattern resets the scrambler to the seed value. For seed discovery, the K28.5 resets the state of the de-scrambler to all zeros; this effectively disables the descrambler. The first 7 bits recovered of 16 byte sequence are the seed value which is extracted by the receiver for use as the initial value of the de-scrambler. The extra length of the training pattern helps guard against cross talk and ISI during the start-up protocol. After the seed value is extracted from the first training pattern, sixteen subsequent training patterns are checked. Successful de-scrambling of a training pattern results in the 16 bytes of zero (D0.0).

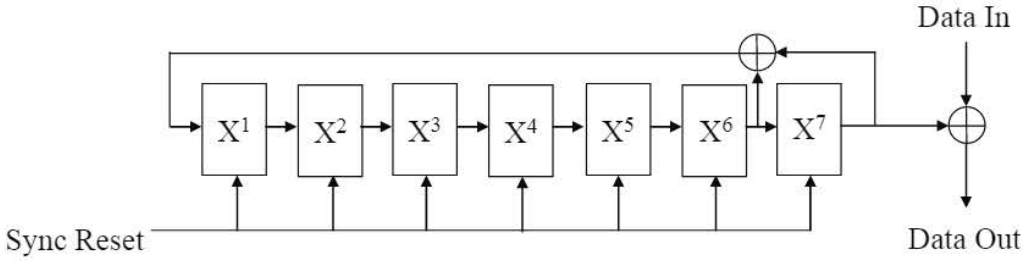


Figure 18: 7-Degree Polynomial Scrambler.

The scrambler shall be a 7-degree polynomial, linear feedback shift register (LFSR). The polynomial is $X^7 + X^6 + 1$. K28.5 or K28.7 characters reset the LFSR to the seed value. The bit pattern repeats every 127 bits.

The RP3 receivers are capable of differentiating IDLE_REQ from IDLE_ACK and capturing the scrambling code seed from either pattern. Random SERDES bit errors are infrequent but could corrupt the training sequence. The receiver verifies the seed value by checking16 consecutive training patterns after capturing the seed (failures re-start the training protocol). Each RP3 receiver has two different state conditions it can communicate to it's paired RP3 transmitter:

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- Scrambling code seed captured from adjacent node
- Acknowledge received from adjacent node

RP3 transmitters can transfer either IDLE_REQ or IDLE_ACK patterns in the IDLE state. The IDLE_REQ is transmitted while the paired receiver has yet to successfully capture the scrambler seed. After the seed is captured, IDLE_ACK is transmitted. Once both the seed is captured and IDLE_ACK is received by the RP3 receiver, the transmitter is enabled to leave the IDLE state.

When a receiver transitions back into the UNSYNC state for any reason, the paired transmitter is brought back into the IDLE state and begins the process of transmitting IDLE_REQ all over again. When a receiver receives IDLE_REQ, it's state is forced back into the UNSYNC state causing it to receive the scrambling seed value again.

The transmit IDLE_REQ & IDLE_ACK mechanism with associated conditional actions taken depending on the state received constitute a robust mechanism for training coordination between two nodes. Any order or delay of enabling the different RP3 transmitters and receivers in a chain are handled with this mechanism. Additionally retraining due to board hot swap or other disruptions is also handled by this mechanism.

A false byte alignment is indicated by the incoming 8b10b encoded bit stream when K28.7 character is followed by certain critical characters. Due to scrambling that is applied for 6144Mbps line rate, any character following K28.7 may cause false byte alignment. Therefore, K28.7 character should not be used for byte alignment or the achieved byte alignment should be locked before starting RP3 master frame transmission.

4.2.4 Counters

Master Frame is defined in Section 4.2.2. The Data link layer provides indices of current data and control message slots to upper layers which can then use these indices in the scheduling of message transmissions. Data message slot counter takes values from 0 up to *(i*(M_MG-1)*N_MG)-1* (refer to Section 4.2.2 for the definition of *N_MG* and *M_MG*) while control slot counter runs from 0 to *(i*N_MG)-1*. Both of these counters are 32 bits wide and they count message slots over a Master Frame duration. Both the data and control message slot counters are reset to zero in the beginning of the first data and control slots of the new master frame. As illustrated in Figure 19, the data message slot counter is reset to zero in the beginning of a Master Frame due to leading data message slot while the control slot counter is reset to zero in the beginning of the first control slot of the new master frame.

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Master frame timing denotes here the Δ corrected (see Section 4.2.5) Master Frame timing, i.e. Master Frame timing at a transmitter port. This refers to the fact that there exists latency in message transfer over the bus, i.e. the message is seen at slightly different times in separate bus nodes. Counter value *X* in the figure below identifies the same message slot of a Master Frame in each bus node.

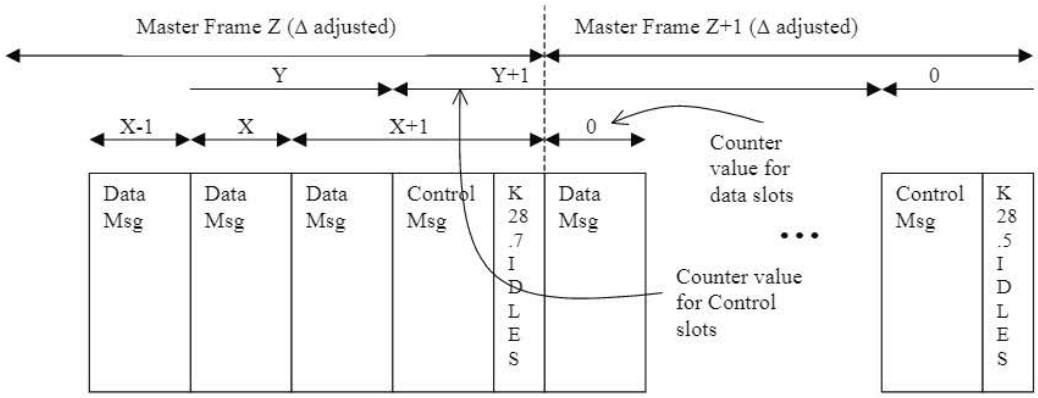


Figure 19: Timing of message slot counters for an example MG and MF definition.

For each bus transceiver (transmitter), message slot counters are activated (counting is started) after the offset parameter Δ (see Section 4.2.5) is available and the state of the transceiver is FRAME_TX (see Section 4.2.8).

4.2.5 Transmission of Frame Structure

Transmission time of Master Frame is synchronised to the RP3 bus frame clock at the output of each bus node. First byte of Master Frame is transmitted at offset Δ from the RP3 bus frame clock tick. In general, a common Δ value is used for uplink transmitter ports; another Δ value is used for all downlink transmitters. In some bus nodes, a specific parameter value is used for each transmitter port.

Parameter Δ fulfils the equation $\Delta = \Pi + D + B + P$, where *D* stands for processing delay of the receiver module and *B* indicates the maximum amount of buffering available at each Data link layer bus receiver while *P* denotes latency across the node; from receiver module to transmission module. Parameter Π is defined in Section 4.2.6 below. Note that the above equation only applies to bus nodes that forward received messages.

Offset values Δ are received at start-up by each bus node and their values are specified in byte-clock ticks. Alternatively, offset values Δ may be specified using two byte accuracy (even byte-clock ticks) which

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may be beneficial especially for higher RP3 line rates. Two's complement code numbers are used.

Offset value Δ of a transmitter is fixed at run time. Section 4.2.8 defines the process according to which the value of the parameter Δ can be changed. Figure 20 illustrates Master Frame transmission timing.

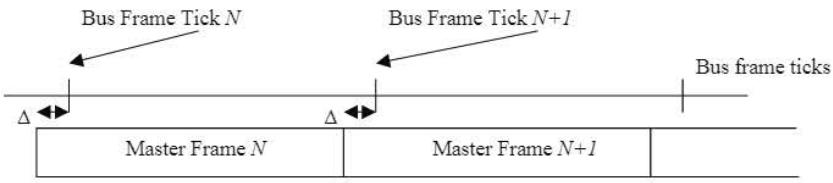


Figure 20: Master Frame is transmitted at an offset to the RP3 bus frame tick in each bus node.

After receiving the parameter Δ, Master Frame timing is valid at the second RP3 bus frame tick. This is due to the fact that Δ may take negative values.

4.2.6 Reception of Frame Structure

The purpose of Master Frame synchronisation is to minimise buffering need in bus nodes, i.e. to ensure that corresponding message slots are received at the same time at each bus node.

For each bus receiver, synchronisation block indicates the received Master Frame boundary (see Section 4.2.8). The synchronization block should contain buffering to compensate for variations of delay especially on long transmission media. An additional offset parameter Π is provided for each receiver that indicates earliest possible time instant when a Master Frame can be received. This time instant, called reference time, is equal to RP3 bus frame clock plus offset Π.

An exact value of Π is provided such that the end of the Master Frame shall be received at the reference time or at maximum MAX_OFFSET ns after the reference time. The default value of MAX_OFFSET equals to 52.08ns while value 104.17ns is optionally allowed (refer to Section 7.1.1 for MAX_OFFSET parameter definition). Target for bus configuration is to have the end of the Master Frame exactly MAX_OFFSET/2 ns after the reference time. This can be achieved when the entire RP3 bus (all parameters) is properly configured.

When initialising a bus link, received Master Frame boundary may not hit the allowed MAX_OFFSET ns wide time window. A false parameter

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value can cause this situation. Irrespective of the erroneous Π value, bus nodes can perform measurements of the received Master Frame boundary as defined in Section 4.2.9.

An error shall always be indicated to Application layer when received Master Frame boundary is detected outside the allowed MAX_OFFSET ns long window. No error is indicated if the Master Frame boundary is not detected at all. This functionality is optional in bus nodes that are located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes. When Master Frame boundary is detected outside the allowed window in any bus node, all following data and control messages are rejected by default. Thus, they are not forwarded to output port(s) and they are not summed together with other messages. However, in bus nodes that are located in Remote RF Units (see Chapter 6), transfer of messages is continued irrespective of the location of the Master Frame boundary. Message processing continues normally (assuming that receiver state has remained in FRAME_SYNC state; see Section 4.2.8) after detecting Master Frame boundary in the allowed window.

Value of parameter Π is fixed at run time. By default, the receiver state machine shall be resynchronised (see Section 4.2.8) when updating the value of the parameter Π. Advanced implementations of RP3 may be able to support run-time updating of parameter Π such that RP3 message transmission and reception is continued uninterruptedly.

Figure 21 illustrates run time (allowed) and measurement windows of received Master Frame.

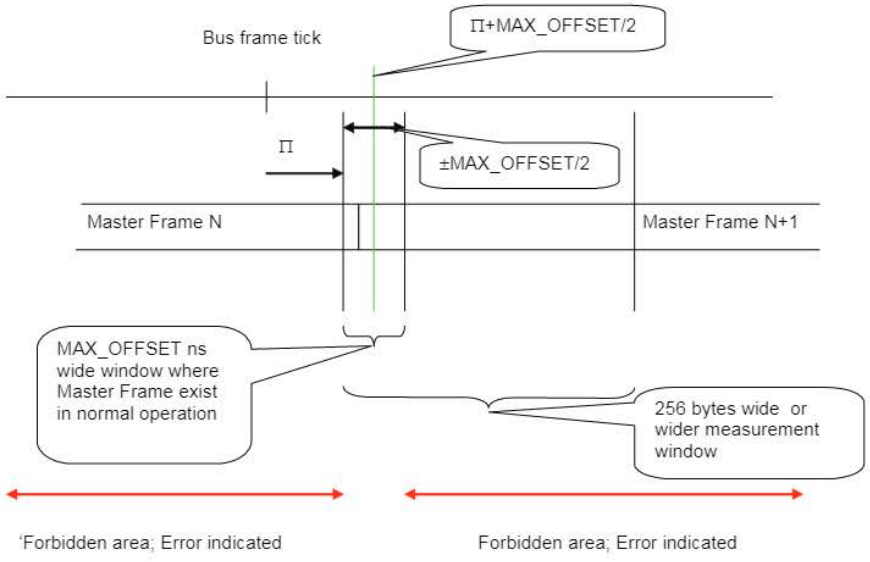


Figure 21: Run time and measurement windows of received Master Frame.

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Consider any bus node that has two or more receiver ports. Parameter Δ's at the transmitting nodes are defined so that difference in received Master Frame timing at any pair of ports is less than or equal to duration of MAX_OFFSET ns.

Figure 22 illustrates receive and transmit offsets of a Master Frame.

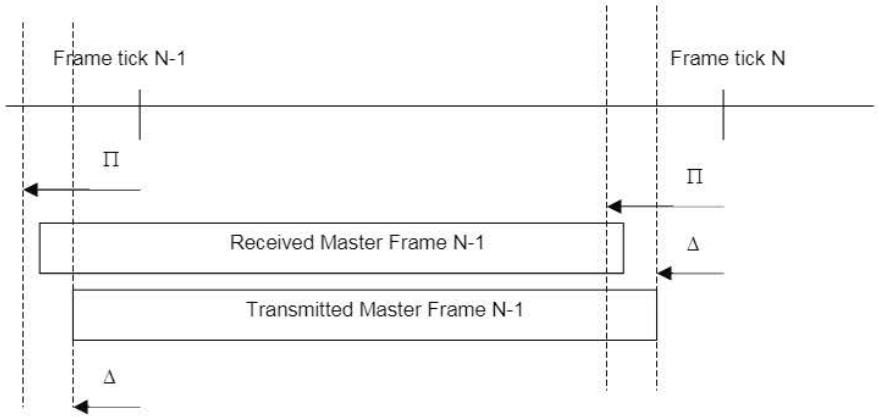


Figure 22: An example of Master Frame timings.

BTS Control and Clock block [2] is responsible of value assignment to parameters Δ and Π of all bus nodes. Figure 23 provides an example of Δ and Π value definition for a very simple intra-cabinet bus network. In the figure, there exists a bus network with three nodes. For clarity, downlink (DL) and uplink (UL) bus connections and corresponding parameter values have been drawn separately. The leftmost node exemplifies bus interface at baseband module while the rightmost node stands for bus endpoint at RF module. Combiner and distributor (C/D) node is at the middle.

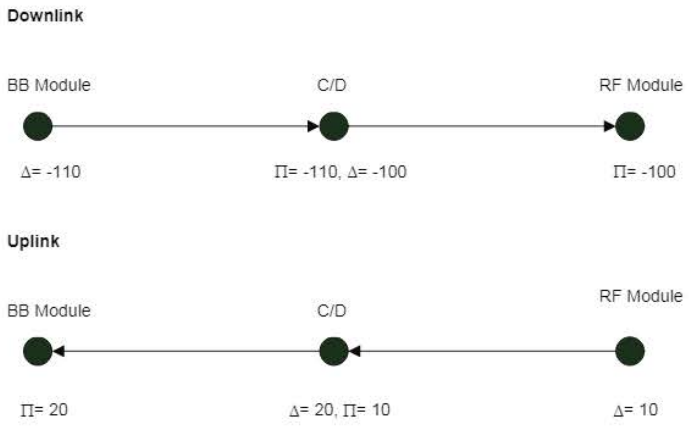


Figure 23: Example of Δ and Π assignments to a bus network.

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In this example, we assume that RP3 bus Master Frame and air interface frame are aligned in time. Therefore, negative Δ and Π values are applied in downlink direction in order to have the data early enough at RF module for transmission to the air (refer to timestamp definition in Section 4.4.8 and data mapping to Master Frame in Section 4.4.9 for related information). Capacity of the bus link and processing delay at RF determines the value of Π that shall be applied. Value of Π never equals to zero at RF bus node. Values of Δ and Π at C/D and baseband nodes are determined by taking into account delays over bus links as well as processing delay over C/D. For simplicity, we assume delay of 10 byte clock ticks over the C/D bus node.

In uplink direction, positive Δ and Π values are applied (refer to Sections 4.4.8 and 4.4.9 for related information). Processing delay at RF defines value of Δ at RF module. Other Δ and Π values are determined by delays over bus links and processing delay over C/D bus node.

4.2.7 Empty Message

When there is no message to transmit, i.e. no message has been received from transport layer for a given message slot, the Data link layer of the bus transmits an empty message. Data link layer at the receiver end will reject empty message and, therefore, these messages are invisible to upper protocol layers. Address '1111111111111' is reserved exclusively for the empty message. Figure 24 defines the empty message. Address field contains '1' bits while rest of the message contains don't care x bits. Don't care bits can be assigned to either '1' or '0' in message transmission.

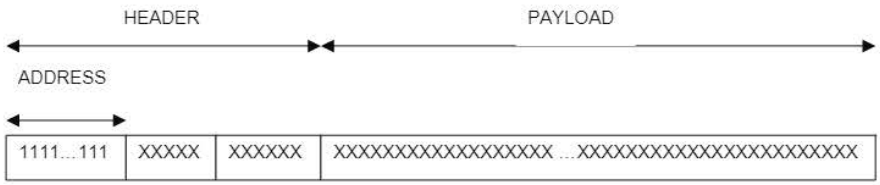


Figure 24: Empty message. The address field consists of thirteen '1' bits while rest of the message contains don't care x bits.

4.2.8 Synchronisation

Physical and Data link layers of the bus must be synchronised before actual data transfer can be started. The synchronisation algorithm can provide information to upper layers regarding the quality of a bus link.

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The frequency of byte errors as well as the status of the frame synchronisation shall be constantly monitored.

Data Link Layer Synchronisation

The synchronisation algorithm is described in the format of a set of finite state machines. Separate state machines exist for each transceiver. Separate state machines are provided for transmitter and receiver as shown in the following subsections.

Transmitter

There are three states in the transmitter state machine: OFF, IDLE, and FRAME_TX. On reset, the state machine enters the initial OFF state. In this state, transmission from the Physical layer macro to a bus link is disabled. Thus, nothing is transmitted to the bus.

The application layer controls the transition from OFF state to IDLE state. The state is changed when the Application layer sets parameter TRANSMITTER_EN equal to 1 and one of the following cases is true: (1) parameter LOS_ENABLE is set equal to 0 meaning that signal LOS (Loss of Signal) from receiver state machine does not have any impact on the transmitter state, or (2) LOS_ENABLE is equal to 1 (LOS has an impact) and LOS is equal to 0 (inactive).

In the IDLE state, the following functionality shall be implemented. In the case of the 768, 1536, and 3072Mbps line rates, the transmitter macro continuously transmits K28.5 IDLE based on which the receiver end can obtain sample (byte) synchronisation. Transmitter state machine always remains in state IDLE at least *t* micro seconds. Value of *t* is implementation specific and it is large enough to allow Phase Locked Loop (PLL) of the transmitter macro to settle and the interfacing receiver macro to obtain correct sample phase.

In the case of a 6144Mbps line rate, the IDLE state consists of two sub-states: IDLE_REQ and IDLE_ACK. When the transmitter enters the IDLE state, it immediately moves to IDLE_REQ state and starts transmitting the IDLE_REQ scrambling training pattern as defined in Section 4.2.3. When the associated RX state machine has captured the scrambling code seed, the transmitter enters IDLE_ACK state and starts transmitting IDLE_ACK sequence (see Section 4.2.3). When the associated RX state machine has received scrambling acknowledgement sequence, the transmitter remains in IDLE_ACK state and starts waiting for parameter Δ updating.

Transition from IDLE state to FRAME_TX state is done when Application layer updates (modifies) the value of parameter Δ. If the value of this parameter is not updated when the transmitter is in state IDLE, transition to state FRAME_TX is not done.

The value of the parameter Δ can only be provided in state IDLE. If there exists a need to change the value of Δ during base station run-

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time, the transmitter shall first be forced to the OFF state, then to IDLE after which the parameter Δ can be updated.

In the FRAME_TX state, transmission of the valid frame structure is performed (see Section 4.2.2). Valid messages from Application/Transport layer are transmitted as well as empty messages. Transmission of frame structure is activated within 20 ms after the updating of parameter Δ.

In Figure 25, all the state and state transitions are shown. As can be seen from the figure, HW reset or active LOS (Loss of Signal) from the receiver state machine shall force the state to OFF (transmission disabled). In the 6144 Mbps case, when IDLE_REQ received state is forced to IDLE_REQ, so receiving end can capture scrambling code again. Parameter ACK_T defines minimum number of IDLE_ACK codes transmitted, so that receiving end surely can detect ACK pattern.

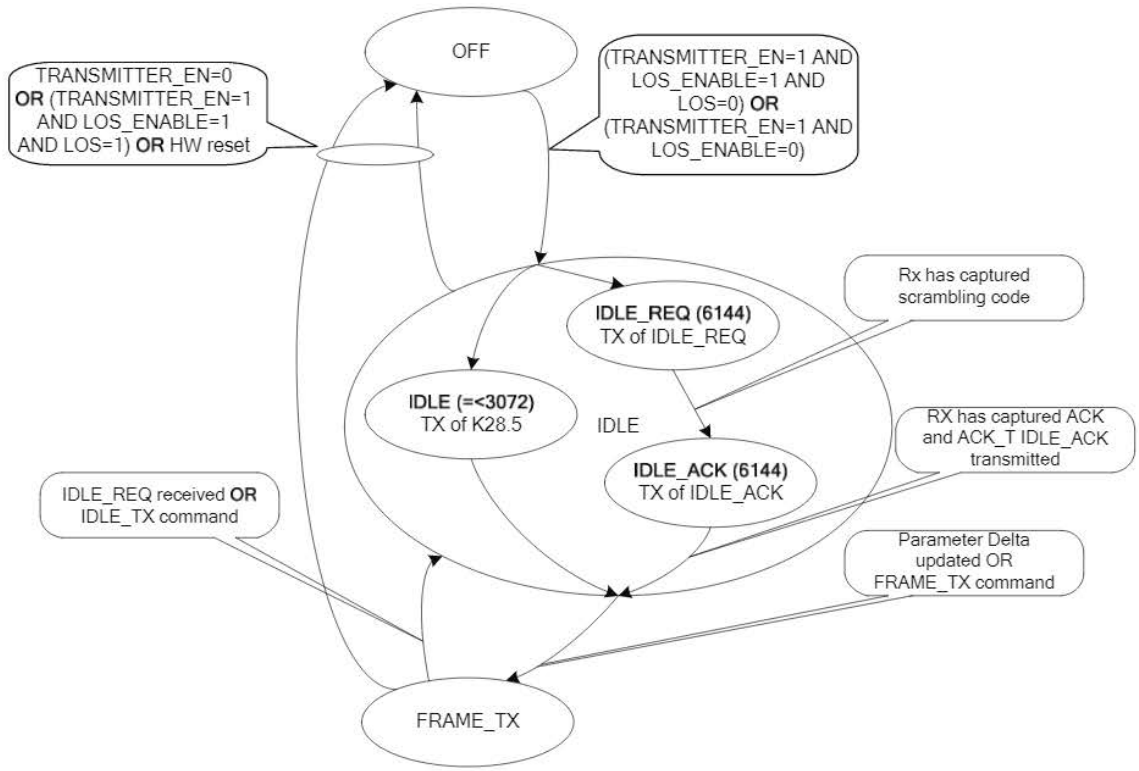


Figure 25: State diagram of the transmitter.

Receiver

In Figure 26, all the state and state transitions are shown.

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The receiver state machine consists of four states in the case of 768,1536, and 3070 Mbps line rates, while there exist six states for 6144 Mbps line rate. The four states applied for all line rates are as follows: UNSYNC, WAIT_FOR_K28.7_IDLES, WAIT_FOR_FRAME_SYNC_T, and FRAME_SYNC. Two of these states, namely WAIT_FOR_K28.7_IDLES and WAIT_FOR_FRAME_SYNC_T, can be considered to form a single logical state called SYNC. The meaning of states UNSYNC, SYNC, and FRAME_SYNC is as follows:

- UNSYNC: Bus link is down. Many byte errors are detected.
- SYNC: Bus link is working, i.e. connection exists.
- FRAME_SYNC: Normal operational mode. Frame structure is detected and messages are received.

Two additional states are applied for the 6144 Mbps line rate due to scrambling seed transfer from the transmitter to the receiver: WAIT_FOR_SEED and WAIT_FOR_ACK. These two states form a logical state called SCR_CAP (scrambling seed capture). It is expected, that the receiver can capture scrambling code both from IDLE_REQ and IDLE_ACK patterns. When in the state WAIT_FOR_K28.7_IDLES, IDLE_REQ is detected if every 17th byte of received data is a K28.5 and there are valid data bytes (no K-codes, no LCV errors) between K-codes. Contents of data bytes are not checked. This way it is possible to recognize IDLE_REQ, even if the scrambling code has been changed. Recognition of IDLE_REQ pattern in WAIT_FOR_K28.7_IDLES state triggers RX state transition to WAIT_FOR_SEED state, where the seed capture is made.

To reduce false recognition of IDLE_REQ, due to an errant K28.5, IDLE_REQ will not be detected in the WAIT_FOR_FRAME_SYNC_T and FRAME_SYNC states. If a scrambling code has been changed, many IDLE_REQs will be received. This will eventually cause FRAME_UNSYNC_T invalid message groups and force the transition to the WAIT_FOR_K28.7_IDLES state. IDLE_REQ will be detected in this state and cause a transition to the WAIT_FOR_SEED state.

The receiver state machine uses two separate criteria to determine the quality of a bus link; the first one monitors the signal quality by counting LCV errors and the second one monitors the validity of the received frame structure. Parameters BLOCK_SIZE, SYNC_T, UNSYNC_T, FRAME_SYNC_T and FRAME_UNSYNC_T control the transitions.

On reset, the state machine enters the UNSYNC state. State transition from the UNSYNC state to WAIT_FOR_K28.7_IDLES (768,1536, and 3070 Mbps line rate) or WAIT_FOR_SEED (6144 Mbps line rate) is done if SYNC_T consecutive valid blocks of bytes have been received. In each block, there exists BLOCK_SIZE bytes and a block is considered to be valid if all the bytes were received correctly (i.e. no

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8b10b decoding errors). Otherwise, the block is considered to be invalid.

In case of the 6144 Mbps line rate, a state transition from WAIT_FOR_SEED state to WAIT_FOR_ACK state is done when the scrambling seed is captured from the IDLE_REQ training pattern (or IDLE_ACK pattern) and verified over 16 sets of training patterns. Refer to Section 4.2.3 for the definition of the verification criterion. Transition from the WAIT_FOR_ACK state to the WAIT_FOR_K28.7_IDLES state is done when an acknowledgement of the seed capture has been received (IDLE_ACK pattern).

A transition from state WAIT_FOR_K28.7_IDLES back to UNSYNC is done if UNSYNC_T consecutive invalid byte blocks are received or in case of HW reset. Transition from state WAIT_FOR_K28.7_IDLES back to WAIT_FOR_SEED occurs if an IDLE_REQ pattern is detected.

A Master Frame boundary is indicated by a set of K28.7 IDLE bytes, i.e. it exists at the end of the block of *K_MG* consecutive K28.7 IDLEs. Transition from WAIT_FOR_K28.7_IDLES to WAIT_FOR_FRAME_SYNC_T is done when *K_MG* consecutive K28.7 IDLE bytes, i.e. a possible Master Frame boundary, is detected. In state WAIT_FOR_FRAME_SYNC_T as well as in state FRAME_SYNC, Master Frame timing is considered to be fixed (defined by the first set of received K28.7 IDLEs).

In WAIT_FOR_FRAME_SYNC_T state, validity of consecutive message groups is studied. When FRAME_SYNC_T consecutive valid message groups are received, FRAME_SYNC state is entered. If FRAME_UNSYNC_T consecutive invalid message groups are received, state WAIT_FOR_K28.7_IDLES is entered and search for a new set of K28.7 IDLE bytes is started immediately, unless the IDLE_REQ pattern is detected (6144 Mbps line rate), in which case the WAIT_FOR_SEED state will be entered.

State transition from FRAME_SYNC to WAIT_FOR_K28.7_IDLES is done when FRAME_UNSYNC_T consecutive invalid message groups are received and transition from FRAME_SYNC to UNSYNC is done when UNSYNC _T consecutive invalid blocks of bytes are received.

A valid message group is defined as a block of *M_MG*19+K_MG* bytes where the first *M_MG*19* bytes are of type data or an 8b10b decoding error occurs. IDLE codes K28.5 or K28.7 are not allowed. The last *K_MG* bytes must be either K28.5 or K28.7 IDLE bytes or an 8b10b decoding error. Furthermore, the order of the IDLE bytes matters. In the first *i*N_MG-1* Message Groups of a Master Frame, all IDLE bytes of the Message Group must equal to K28.5 while in the last Message Group of the Master Frame, *K_MG* IDLE codes shall equal to K28.7.

The receiver synchronization state machine has several outputs. Current state of the receiver will be available for Application layer. An interrupt shall be generated from each state change. Signal LOS (Loss

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of Signal) is active (has value 1) in state UNSYNC while it is inactive in other states. Synchronization block also indicates bytes that contain 8b10b decoding error as well as the location of the Master Frame boundary. In the case of a 6144 Mbps line rate, scramble seed capture and acknowledge training pattern received is also indicated.

Data Link layer shall forward messages to Transport layer only when in state FRAME_SYNC. This will prevent routing of false data from disconnected or otherwise malfunctioning receiver port.

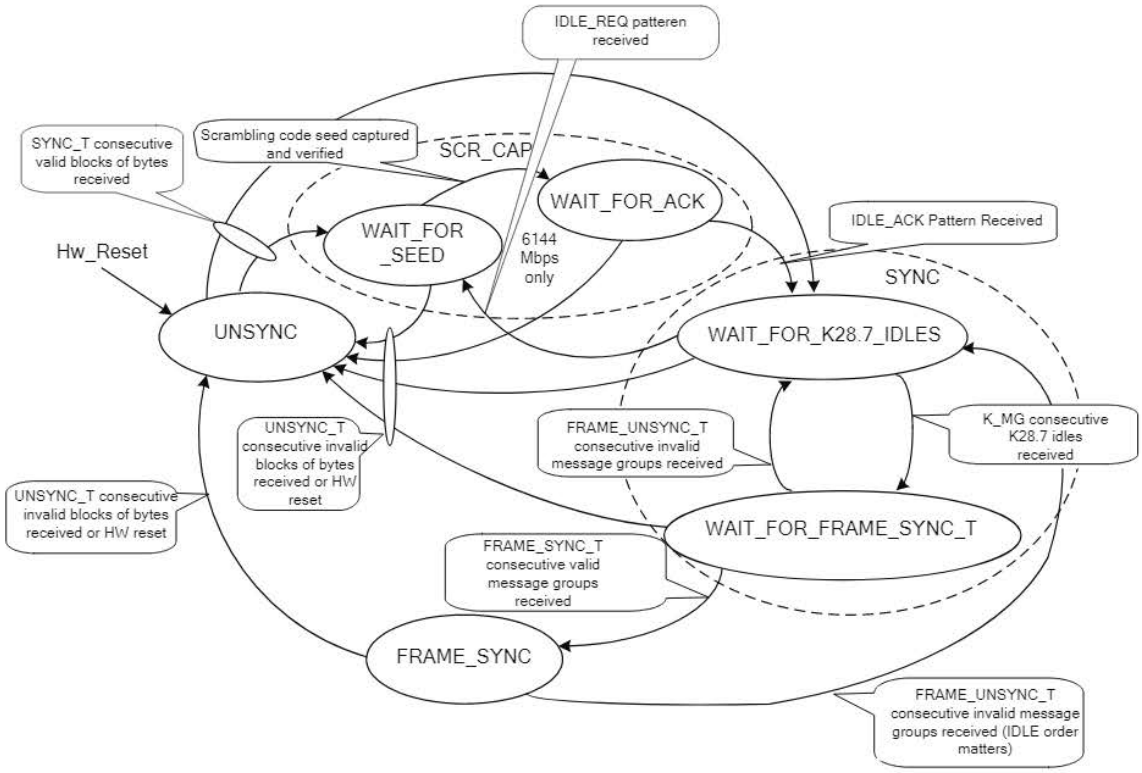


Figure 26: State diagram for the receiver.

Data Link layer shall forward messages to Transport layer only when in state FRAME_SYNC. This will prevent routing of false data from disconnected or otherwise malfunctioning receiver port.

4.2.9 Measurements

In this section, the measurements that are performed by the Data link layer are listed. Currently only timing offsets of received Master Frames with respect to baseband bus clock plus Π are measured (refer to Section 4.2.6). This measurement is optional in bus nodes that are

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located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes.

To support bus configuration and error recovery, each bus receiver can detect the received Master Frame within a time window that spans 0-255 bytes after the reference time. Window size of 256 bytes applies for old RP3 implementations. For implementations supporting OBSAI RP3 Specification, Version 4.2 or later, measurement window size that is equal to RP3 Master Frame Size shall be supported. The reference time stands for baseband bus frame clock tick plus offset Π. If the Master Frame offset is not detected during the time window, the measurement is saturated at the maximum counter value (default value is 255 in older implementations). The measurement is activated only in FRAME_SYNC mode (see Section 4.2.8) and the measurement is conducted once per Master Frame.

Table 4: Measurements performed by the Physical layer.

Measurement	Register width	Description
Received Master Frame offset	8 bits (default value in old implementations), positive integer (no sign bit). 32 bits in implementations supporting Version 4.2 or later.	Provided for each receiver separately. Master Frame offset from reference time, i.e. baseband bus frame clock tick plus Π. Value is given in byte-clock ticks. Measurement value is saturated at the maximum counter value if Master Frame boundary is not detected. Valid range of values for Master Frame boundary measurement is 0-MAX_OFFSET ns. Out of range error is indicated (see Section 4.2.6).

4.2.10 Message Multiplexer and Demultiplexer

Message multiplexer performs time interleaving of messages from *N*, *N*>1, input RP3 links to a single output RP3 link as illustrated in Figure 31. The multiplexer shall forward messages from the input links to the output link such that valid RP3 Message Group and Master Frame formats exist at the output link. The mapping algorithm used by the multiplexer shall remain the same for all time and it is set up at bus configuration time. The definition of the frame structure in Section 4.2.2 suggests the use of a round robin algorithm in message multiplexing.

The message multiplexer shall repeatedly perform a re-arrangement of messages from the input links to the output link over a time period that corresponds to the duration of a single message at 768Mbps line rate. Thus, messages from input links k, $0 \leq k < N$, with message slot indices $M_k * i + j_k$ shall be forwarded to messages slots $M_{out} * i + j_{out}$ at the

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output link, where the line rate of input link k equals to M_k * 768Mbps, the line rate of output link equals to M_{out} * 768Mbps, $M_k \in \{1, 2, 4, 8\}$, $j_k = \{0, \ldots, M_k - 1\}$, $M_{out} \in \{1, 2, 4, 8\}$, and $j_{out} = \{0, \ldots, M_{out} - 1\}$. Index i, $0 \le i < N\_MG * M\_MG$, runs over all message slots of a Master Frame at 768Mbps line rate. All or only a subset of the available input messages are forwarded to the output.

The order according to which messages are mapped from input links to output link can be defined in a format of a multiplexing table. This table, which is actually a vector, consist of M_{out} elements $E_0, \ldots, E_{Mout-1}$ each $E_{i_{out}} = (D, k, j_k)$ defining an input link and message slot from which the message is copied to the corresponding output message slot j_{out}. Parameter D is set equal to '1' when no input message is copied to that position, i.e. an empty message will be transmitted. Otherwise, D='0'.

Table 5 - Table 8 define the mandatory multiplexing algorithms for a set of multiplexing configurations using the format of multiplexing tables.

Table 5: Multiplexing table for the case where all messages from four 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	**Input position, i.e.** $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	0, 3, 0

Table 6: Multiplexing table for the case where all messages from two 1536Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	**Input position, i.e.** $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 1, 1

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Table 7: Multiplexing table for the case where all messages from one 1536Mbps link and two 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	**Input position, i.e.** $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 2, 0

Table 8: Multiplexing table for the case where all messages from two 768Mbps link are multiplexed to a single 1536Mbps link.

Output position (information only)	**Input position, i.e.** $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0

Table 9 illustrates a case where messages from three 768Mbps links are multiplexed into a 3072Mbps link.

Table 9: Multiplexing table for the case where all messages from three 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	**Input position, i.e.** $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	1, 0, 0

The message demultiplexer performs an inverse operation to the multiplexer, i.e. the output link in the above equations is considered as the input link and input links become output links.

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Figure 27: Illustration of message multiplexer.

4.3 Transport Layer

Transport layer consists of message router and summing units. Transport layer is responsible for the end-to-end delivery of messages. All routing of messages is performed at Transport layer. Based on the address of each message, bus nodes forward received messages to destination nodes. Local routing is applied, i.e. each bus node knows only its own output port(s) into which a message needs to be transmitted. Nodes do not have visibility to the entire message paths. These paths are defined by a bus control entity, Bus manager, when booting up the bus.

The address field, which is used to route the data to its destination point, occupies the first 13 bits of the message. The remaining part of the message, including type, timestamp, and payload, is passed transparently by the Transport Layer.

4.3.1 Overview of Transport Layer

In general, communication networks consist of bi-directional links (or unidirectional links in opposite directions) that connect nodes. In each node, the same routing algorithm is applied to all received messages. In an alternative approach, a bi-directional network is separated into two unidirectional networks that operate independently. When messages need to be transferred between these unidirectional networks, they must go across Application layer. Physical and Transport layers of the two networks operate independently. In a hybrid network concept, received messages in all bus nodes are divided into two groups and separate routing algorithms are applied to these groups. Messages may be classified, e.g., based on the direction of the received messages.

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The proposed bus protocol can be used in all above-mentioned network concepts. The hybrid approach is proposed with downlink and uplink networks, and separate routing tables are used for uplink and downlink messages.

Figure 28 illustrates Transport layer with a common message router for all received messages. External interfaces of Transport layer are shown including ports between Application and Transport layers as well as between Transport and Data link/Physical layers. All messages between protocol layers are transferred over these ports.

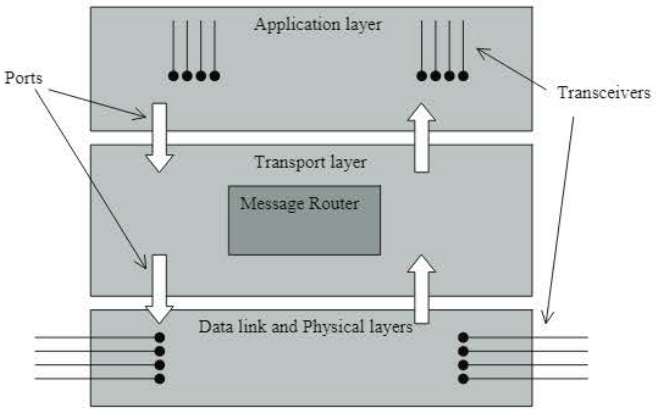


Figure 28: Transport layer with a common message router for all received messages.

When a bus node receives a message from another node, the message is first received by a transceiver at Physical and Data link layers. Then the message is sent to Transport layer, which determines the output transceiver with the help of a routing table. Assuming that transceiver at the Data link/Physical layer is targeted, the message is forwarded back to Data link layer for transmission to the next node. If the payload of the message is processed in the bus node, Transport layer will forward the message to Application layer based on the address of the message. Application layer may send the message back to the bus after processing.

Transport layer operates in a similar manner for all received messages whether they are received from Data link/Physical or from Application layers.

Figure 29 presents functional blocks of Transport layer where a dedicated message router is used for downlink and uplink messages. Application layer must indicate through parameters which transceivers, especially receiver ports of transceivers, are connected to downlink message router and which use the uplink router. Note that both message routers can forward messages to the transmitter port of any transceiver.

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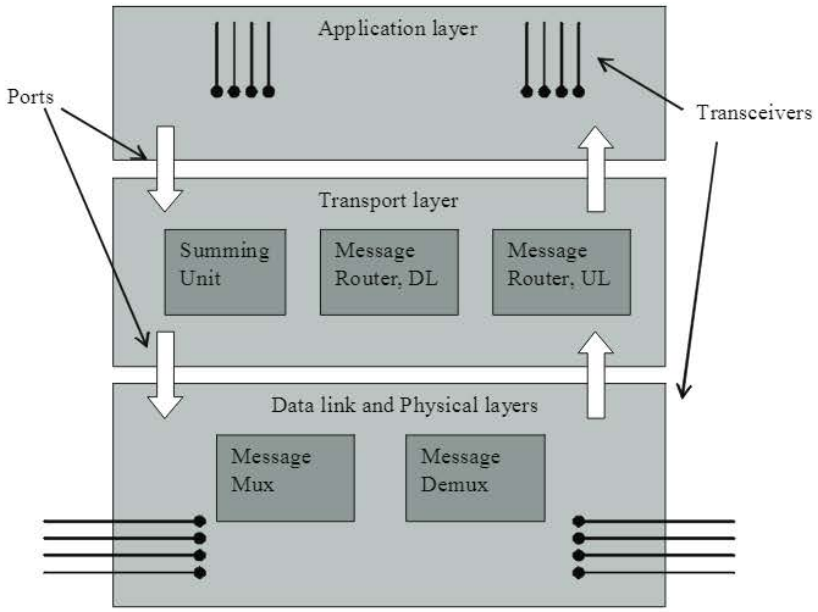


Figure 29: Transport layer with dedicated downlink and uplink message routers. Also summing unit is shown as well as message multiplexer and demultiplexer of the Data Link layer.

The summing unit, which is located in front of each transmitter port of a transceiver, adds together payloads of messages. Summing is performed when more than one message should be transmitted simultaneously to the output port.

Physical and Data link layers, as well as message router and summing unit at Transport layer, operate as fast as possible, i.e. messages are not buffered. Thus, message slot is never altered by these functional blocks. Message multiplexer and demultiplexer may perform line rate conversions due to which they may need to have buffers of length few messages.

In the following sections, all functional blocks of the transport layer are described in detail.

4.3.2 Message Format – Address Field

The address controls the routing of each message. In downlink direction, i.e. from baseband to RF, all message transfers are point-to-point, and the address identifies the target node. Both multicasting

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(point-to-multipoint) and point-to-point message transfers are applied in uplink direction, i.e. from RF to baseband. Uplink antenna sample data as well as some measurement results may require multicasting; all other message transmissions in uplink direction are typically point-to-point.

In networks where bus nodes apply the same routing algorithm to all received messages, each multicast address must be unique. This is undesirable because address space is consumed. When separate routing algorithms are applied for downlink and uplink messages, source node address of the message can be used as the multicast address. This concept shall be used.

The address field is divided into two sub-addresses, the node address and the sub-node address as illustrated in Figure 30.

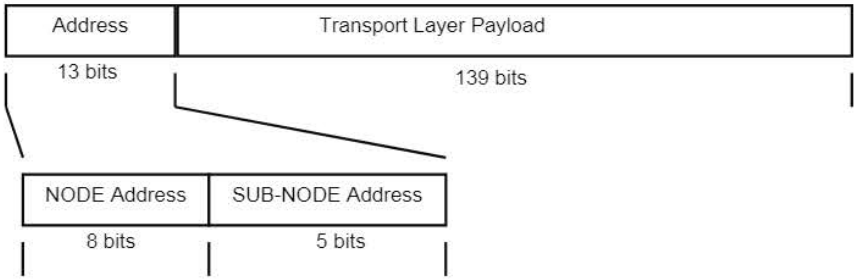


Figure 30: Address sub-fields.

Node and sub-node address fields are used in a hierarchical addressing scheme where the node field is used to uniquely address a specific bus node, i.e. baseband design block, and the sub-node address is used to identify the specific module within the design block. The node address size of 8 bits allows 256 baseband design blocks to be addressed, with up to 32 modules addressed with the 5 bits of sub-node address.

Node address does not necessarily stand for the address of a physical device such as ASIC (Application Specific Integrated Circuit). A device may have one or more node addresses and the nodes may have varying number of active sub-node addresses. For example, in an ASIC that holds both modulator (up conversion) and channelizer (down conversion) design blocks, the blocks typically have separate node addresses.

The general control block of a node, if applicable, is typically addressed using sub-node address 00000.

Reserved addresses

Address ‘00000000xxxxx’, where ‘x’ stands for either ‘0’ or ‘1’ bit, is reserved for initial booting of the bus network. Thus, node address ‘00000000’ can be used only as default boot up address. It cannot be assigned permanently to any node.

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Address '1111111111111' (1FFFh) is reserved for the empty message. Therefore, physical layer will delete all received messages with an all-ones address. However, addresses '1111111100000'-'1111111111110' (1FE0h-1FFEh) can be used, i.e. node address '11111111' (FFh) is valid.

4.3.3 Message Router

In RP3 implementations that are compliant with the RP3 Specification, Version 4.2 or later, the full 13 bit address is used for message routing. In implementations supporting older versions of the specification, the mechanism described below, i.e. address translation, may be used.

Figure 31 illustrates the functionality of the message router. The 13 bit input address of a message is first processed by a mapping unit which typically selects only a subset of the input bits. For example, the node address may only be selected. Refer to Section 7.1.3 for a description of the input parameters of the mapping unit. The transformed address is then used as an index to a routing table, which contains indices of the transceivers into which the message must be transmitted. Note that Message Router shall not change the content of any message. The transformed address is just a temporary parameter used by the router.

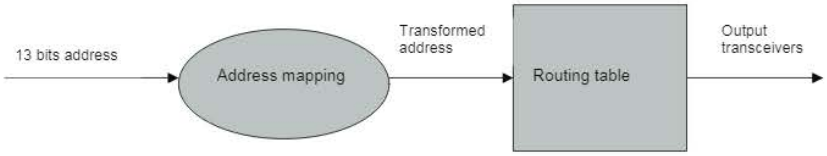


Figure 31: Functionality of message router.

An example of a routing table is given below. In the table, there is a bit vector (row) that corresponds to each transformed address. In the example, two bits wide transformed address is used. Length of the bit vector equals to the number of transceivers that exist in the node. Bit '1' means that the message must be forwarded to the corresponding transceiver while '0' prohibits message transmission. Least Significant Bit (LSB) of the bit vector stands for transceiver of Index 0.

As an example, consider a message with transformed address 10 (2 in decimal number). This message is transmitted by transceivers having indices 1 and 2.

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Table 10: An example of a table.

Transformed Address (input)	Transceivers (output)
00	(MSB) 000001 (LSB)
01	000010
10	000110
11	100001

4.3.4 Summing Unit

Summing unit is located in front of each transceiver, the transmitter port, and all transmitted messages pass through it. When a single message per message slot is to be transmitted, Summing unit forwards the message unaltered to the transceiver. In other words, summing unit will not examine the contents of the message. When two or more messages are targeted to the same message slot and transceiver, Summing unit generates a single output message from the input messages as follows. Header for the output message is copied from one of the input messages. Headers of the input messages should be equal, so any of the messages can be selected. An error is indicated to Application layer if the headers differ. Payload of the output message is a pointwise sum of the payloads of all input messages. In case of complex baseband IQ samples $x_i(n)$, where *i* denotes Index on the input message of a Summing unit and *n* stands for the time index of the samples, pointwise sum *y(n)* is equal to $y(n) = \sum_i x_i(n)$. Summing unit and the entire bus uses two's complement code numbers with sign extension. In the summing, saturating arithmetic is used in order to mitigate possible overflows.

As an example, consider two messages each containing four samples. Output message (4, 1, -1, 7) is obtained when performing pointwise sum of real valued messages (3, -1, 5, 4) and (1, 2, -6, 3). Only payload of messages is considered here.

Summing unit is typically activated only for WCDMA, CDMA, 802.16, and LTE data messages. Message collision occurs for example when baseband GSM/EDGE samples are added together. Summing unit detects message collisions by analysing headers of input messages. As an input parameter SUMMING_ALLOWED_FOR_TYPE (see Section 7.1.3), Summing unit receives a list of message types that may be added together. An error is indicated and message transmission is hindered when messages with improper type should be added together. Specifically, in case of message collision, Physical layer should send an

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empty message due to hindered message transmission but it is also acceptable to transmit one of the colliding input messages to the bus.

Summing unit performs also bit-by-bit comparison of all headers and checks that they are equal.

Only messages of type WCDMA/FDD, WCDMA/TDD, CDMA2000, 802.16, and LTE (see Table 12) may be summed together. Two or more messages of the same type can be added together. A message collision is reported in all other cases.

As an example, SUMMING_ALLOWED_FOR_TYPE = '00000000000000000000000001001100' enables summing of WCDMA/FDD, WCDMA/TDD, and CDMA2000 messages.

Figure 32 illustrates functionality of the Summing unit. In this example, three input messages are shown but *K* input messages need to be supported.

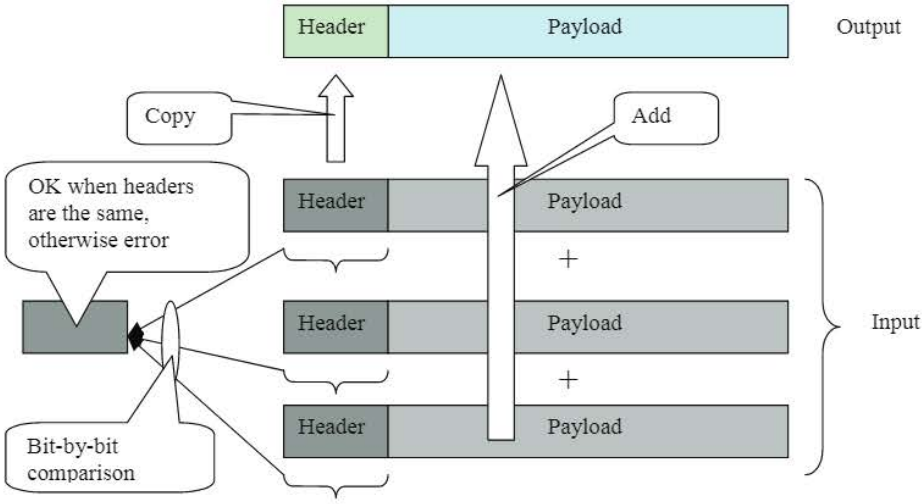


Figure 32: Functionality of Summing unit. Type check of input messages is not shown.

4.4 Application Layer

Application layer represents the user of the protocol and it maps different types of control and data into the payload. The application layer is also responsible for the insertion of the message header: address, type, and timestamp fields.

From bus protocol point of view, Application layer is divided into two parts: air interface applications and bus functions. Major portion of

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Application layer consist of air interface applications, which are isolated from the bus by "Bus Interface" part. The Bus Interface contains functions that prepare data for transmission over the bus. Also transmission and reception of messages is included. In this section, Bus Interface functionality is described.

4.4.1 Addressing

Application layer will generate message packets with the multicast or point-to-point address in the address field. Refer to Section 4.3.2 for details.

4.4.2 Paths

All data transfers over the bus are performed over paths. Path concept is introduced in order to decouple air interface applications from bus protocol and also to formalise bus configuration process.

A path consists of a set of bus links and message slots that are reserved for data transmission. Bus links connect the source and target nodes together and they are defined by the routing tables. Depending on the bandwidth needed for data communication, an appropriate number of message slots per Master Frame are reserved for the path. Bus manager will provide exact definitions of all paths through the bus. Paths are defined so that message collisions do not exist.

Paths are fixed, i.e. message transfer between any two nodes is always done over the same bus links using pre-specified message slots. Paths are defined before bus initialisation, i.e. message transfers over the bus are deterministic. In case of run-time BTS reconfiguration, paths may need to be modified, added or deleted. Transport layer supports run-time modification of routing tables with minimal corruption of messages. Bus nodes also support run-time modification of message transmission rules but this may be service affecting.

The path taken by a message is determined by the address in the message and the routing tables set up in the bus nodes by the Bus manager.

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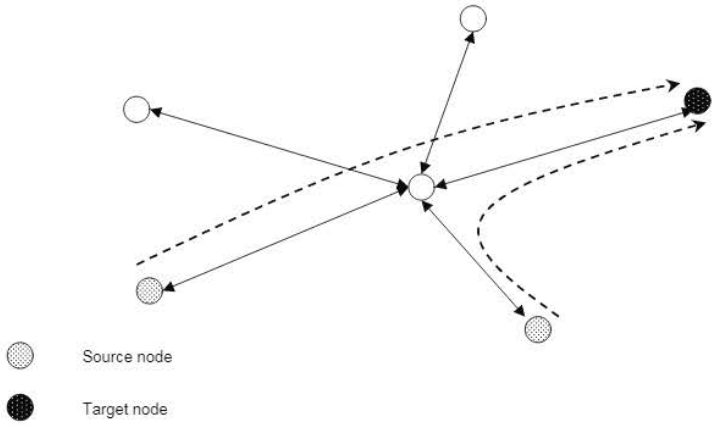


Figure 33: Arbitrary bus configuration with two paths. Message slots are not shown.

4.4.3 Routing

Data transmission between different networks (UL/DL for example) through Application layer is called application layer routing. In some configurations it is beneficial to use application layer routing to share same RP3 link for both UL and DL data.

Application layer routing stands for receiving a data stream, for example antenna carrier, from RP3 bus and transmitting it again to another RP3 link with a transmission rule. Application layer routing does not have any limitation regarding link timing.

4.4.4 Message Transmission Rules

For each path, Bus manager provides detailed rules for message transmission. Rules for paths utilizing data and control message slots are provided separately. As stated in Section 4.2.3, Data Link layer of the bus provides counter values for data and control message slots. Transmission of messages is done with respect to these counters.

There exist two layers of message transmission rules. The rules of the lower layer utilize modulo computation over message slot counters to define RP3 virtual links and their use is mandatory. The rules of the higher layer, which are optional, define paths within RP3 virtual links utilizing bit maps. When the higher layer rules are not used, RP3 virtual links equal to paths.

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At the lower layer, message slots for each RP3 virtual link are specified by the pair of numbers (*I* (Index), *M* (modulo)) such that equation $MessageSlotCounter \bmod M = I$ holds. In case of a path using data message slots, *MessageSlotCounter* runs from 0 up to *(i*(M_MG-1)*N_MG)-1* while it takes values from 0 up to *(i*N_MG)-1* in case of control message slots.

As an example, consider transmission of WCDMA data over RP3. For WCDMA, as well as for CDMA, message transmission rules of the lower layer are only used. Assume that a message transmission rule (1, 4) has been provided to a path which uses data message slots, i.e. the Index is equal to 1 while the modulo is 4. This rule states that the node can transmit messages to data message slots having indices 1, 5, 9, 13, 17, …

At the higher layer, Dual Bit Map concept is applied where two bit maps with maximum lengths of 80 bits (Bit Map 1) and 48 bits (Bit Map 2) are used. The actual lengths of the bit maps are indicated by parameters *Bit_Map_1_Size* and *Bit_Map_2_Size*. The first bit map *Bit_Map_1* is applied *Bit_Map_1_Mult* times after which the second bit map *Bit_Map_2* is used once. The procedure then repeats and reuses the first bit map *Bit_Map_1_Mult* times. A parameter *X* specifies the maximum number of antenna-carriers that fits into an RP3 virtual link. Refer to Table 11 for the definition of all parameters of the dual bit map method.

The Dual Bit Map algorithm is the following. Select *N* unique indices from 0 to *N-1* for each of the signals (antenna-carriers) that are being transmitted such that $N \leq X$ holds. Start reading the bit map, *Bit_Map_1*, from the MSB. If the bit equals 0, a message block of *X* consecutive message slots from the RP3 virtual channel are available for data transmission. Create an index *J* that increments from 0 to *X-1*. Send a data message from each of the signals (antenna-carriers) when *J* is equal to the index selected for each active signal. If the value of the bit is 1, a message block of *X+1* consecutive message slots from the RP3 virtual channel are available for data transmission and *J* increments from 0 to *X*. Any indices not used to transmit data messages can be used to transfer other messages, e.g. Ethernet or Empty messages. The algorithm continues by repeating the above procedure for the next bit of the *Bit_Map_1* word. To obtain the entire sequence of message blocks, *Bit_Map_1* is repeated *Bit_Map_1_Mult* times followed by the *Bit_Map_2* word when the *Bit_Map_2* size is non-zero.

Dual Bit Map algorithm is reset at RP3 Master Frame boundary.

Currently, parameters of the Dual Bit Map algorithm are defined only for 802.16, LTE and GSM/EDGE data in Appendix D, F and G. Use of these higher layer rules for 802.16 and LTE is mandatory in downlink direction when the Summing Unit (see Section 4.3.4) is activated for type 802.16 or LTE (see Table 12). In uplink direction, use of these rules is optional. Lower layer rules, i.e. the modulo rules, are mandatory

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both in downlink and uplink directions. Dual Bit Map rules are optional for GSM/EDGE.

Table 11: Definition of the parameters of the dual bit map concept.

Parameter	Definition
X	The maximum number of antenna-carriers that will fit into a given virtual RP3 link
Bit_Map_1_Mult	Number of times the first bit map is repeated
Bit_Map_1	Value of the first Bit Map in hexadecimal number. The Bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_1_Size	Size of the first Bit Map (number of bits)
Bit_Map_2	Value of the second Bit Map in hexadecimal number. The bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_2_Size	Size of the second Bit Map (number of Bits)

Figure 34 illustrates 802.16 data transmission into RP3 virtual link using the Dual Bit Map algorithm. Three OFDMA antenna-carriers with 8.75MHz channel bandwidth are mapped into RP3 link. In this example, we assume that the whole RP3 link with 1536 Mbps line rate is allocated for 802.16 data, i.e. the RP3 virtual channel is specified by parameters (0 (index), 1 (modulo)).

At node initialisation, the Bus manager will provide message transmission rules for the end nodes of the bus. Updated rules are provided during run-time if needed; for example, in case of BTS reconfiguration.

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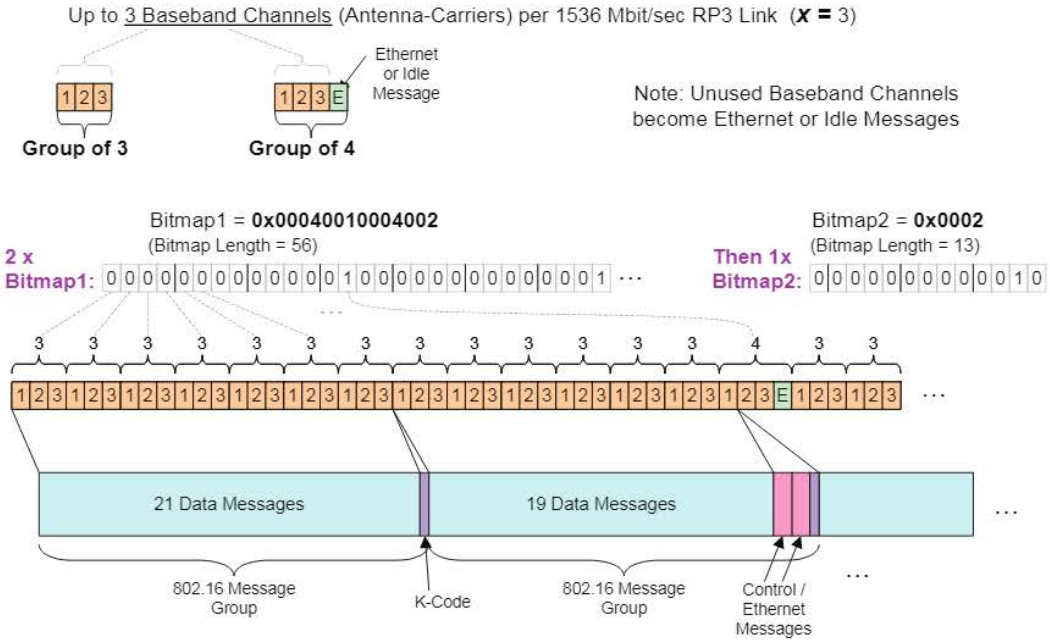


Figure 34: 802.16 data transmission into RP3 link using Dual Bit Map algorithm.

4.4.5 Bus Manager

Bus Manager is responsible for the configuration of the bus. Bus Manager is typically located at Control and Clock Module (CCM) and it is a function of the BTS Resource Manager. When the configuration for the BTS modules is known (the number of antennas and carriers etc), the Bus Manager configures the bus accordingly.

4.4.6 Buffering Requirements

Physical, Data link, and Transport layers of the bus perform minimal buffering, i.e. they process messages immediately when received. Buffers having size of few bytes exist at the Data link layer in order to compensate for propagation delays (see Sections 4.2.5 and 4.2.6).

At Application layer, messages need to be buffered because the bus will serialise messages and data. Consider e.g. WCDMA application where data from parallel sources, such as digitised samples from antennas, are transmitted over the bus in consecutive messages. Buffers are needed both in the transmitter and receiver ends in order to slice the continuous data stream into discrete messages and vice versa. At maximum, a double buffering scheme is used in WCDMA with four chips of data per buffer. The same double buffering concept can be

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used also for CDMA and LTE data. A buffer of size six messages is required for each 802.16 signal (antenna-carrier) in order to compensate the jitter caused by message transmission (refer to Section 4.4.4 for the definition of message transmission rules). In GSM/EDGE applications, entire time slot bursts are typically buffered at Application layer and, therefore, serialisation of data on the bus has minor impact.

4.4.7 Message Format – TYPE Field

Application layer is responsible for defining the type of the message. The TYPE field identifies the content of payload data. The following table presents the possible payload types.

Table 12: Content of type field.

Payload data type	Content of Type field
Control	00000
Measurement	00001
WCDMA/FDD	00010
WCDMA/TDD	00011
GSM/EDGE	00100
TETRA	00101
CDMA2000	00110
WLAN	00111
LOOPBACK	01000
Frame clock burst	01001
Ethernet	01010
RTT message	01011
802.16	01100
Virtual HW reset	01101
LTE	01110
Generic Packet	01111
Multi-hop RTT message	10000
Currently not in use	10001-11111

Most of the TYPE values presented above are self-explanatory. LOOPBACK messages are user defined application layer messages that may be used to monitor link integrity.

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4.4.8 Message Format – TIMESTAMP Field

The timestamp field relates the payload data to a specific time instant.

Consider a block of WCDMA or CDMA2000 antenna samples that exist in the payload of a message. In uplink direction, time stamp identifies the time instance when the last sample of the message was available at the output of the channelizer block (down converter, FIR filter). In downlink direction, time stamp defines the time instant when the first sample of the payload must be inserted into the modulator (up converter, FIR filter). Reference time is the WCDMA or CDMA2000 frame clock of the BTS.

The WCDMA time stamp is calculated as

$$TIMESTAMP = \lfloor CHIP\ NUMBER\ IN\ SLOT / 4 \rfloor MOD\ 64$$

where CHIP NUMBER IN SLOT stands for the chip Index of a WCDMA time slot and $\lfloor x \rfloor$ denotes the greatest integer not exceeding x. Thus, $\lfloor x \rfloor$ stands for the integer part or floor of x. All chips of an RP3 message shall have the same TIMESTAMP value as defined by the above equation.

In WCDMA, there exist 100 frames per second and each frame contains 15 time slots. Altogether, there exist 1500 time slots per second while every time slot consists of 2560 chips indicating that CHIP NUMBER IN SLOT takes values between 0 and 2559.

Computation of CDMA2000 time stamp is done analogously to WCDMA time stamp computation, i.e. $TIMESTAMP = \lfloor CHIP\ NUMBER\ IN\ SLOT / 4 \rfloor MOD\ 64$.

Time stamp computation for 802.16 and LTE applies modulo over I&Q sample index, i.e. TIMESTAMP = $\lfloor SAMPLE\ NUMBER\ IN\ AIR\ FRAME / 4 \rfloor MOD\ 64$.

For GSM/EDGE only in downlink direction, the MSB of the timestamp is used to identify the first packet in the timeslot, with a logic ‘1’ identifying the first, with subsequent packets set to a logic ‘0’. The remaining 5 LSBs of the timestamp represent a count reflecting the packet number with reference to the first packet in the timeslot. The count will wrap-around, but the MSB provides a unique identification of the first packet. Therefore, time stamps of messages containing first samples of a time slot are 100000, 000001, 000010, 000011, 000100, etc.

In the GSM/EDGE uplink direction, the same concept as that of the downlink direction is applied with one exception. The MSB is equal to ‘1’ during the four first messages of a time slot.

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4.4.9 Message Format – PAYLOAD Field

The payload represents the content of the message with the type field defining whether the payload contains control, measurement, antenna sample, or some other data. The payload size is fixed at 16 bytes and, from Physical and Transport layer point of view, is considered to be always full. It is the responsibility of Application layer to map data to the payload.

The following sections detail how Application layer maps data into the payload for the different data types. It is intended that data packets are only sent when there is sufficient data to fill them as defined in the following. The only exception is the last packet of the timeslot in GSM/EDGE mode where full amount of data may not be contained.

4.4.9.1 WCDMA Downlink Data Mapping

The WCDMA downlink data stream has a chip rate of 3.84 Mcps with an I&Q data format each of 16 bits giving 4 bytes per chip. This allows 4 consecutive chips of a single WCDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. Two's complement code is used to represent both I and Q sample values.

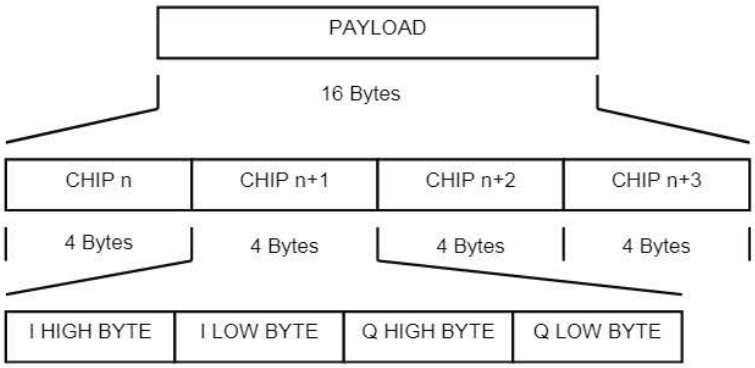


Figure 35: WCDMA DL Payload Mapping.

4.4.9.2 WCDMA Uplink Data Mapping

The WCDMA uplink data stream has a sample rate of 7.68 Msps (two times the chip rate), with an I&Q data format each of 8 bits giving 2 bytes per sample. This allows 8 consecutive samples (four chips) of a single WCDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. As in case of downlink data transfer, two's complement code is used and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

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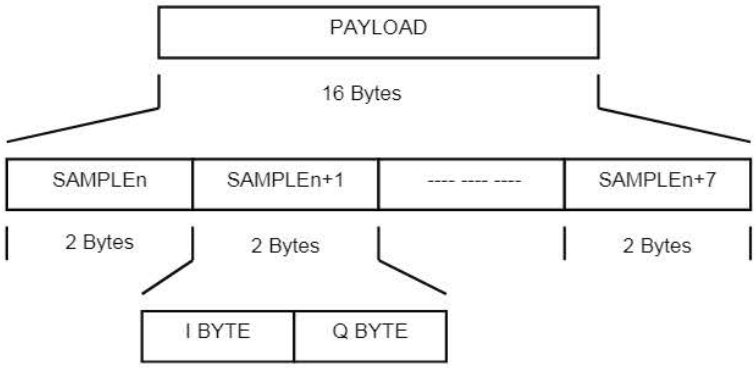


Figure 36: WCDMA UL Payload Mapping.

4.4.9.3 GSM/EDGE Uplink Data Mapping

The GSM/EDGE uplink data stream has a sample rate of 541.667Ksps or 650.000 Ksps (two times the symbol rate).

The GSM/EDGE uplink data stream I&Q data format is: 14 bits mantissa and a 4 bit shared exponent, giving 32 bits per sample.

A GSM/EDGE timeslot contains 156.25 or 187.5 symbols. Because of the fractional amount of samples per time slot, consecutive time slots have different amounts of samples to be transmitted. For a 156.25 symbol scenario, three out of every four timeslots will contain 156 symbols worth, with every 4th containing 157. At the 2x sample rate this equals to 312 or 314 samples per time slot. For 187.5 symbol scenario the respective numbers for every other time slot are 187 and 188 symbols, which mean at 2x over sampling ratio 374 and 376 samples per time slot. The samples are fully packed into payloads due to which the last message of a time slot has different number of samples.

The final packet will contain a Sample Count Indicator (SCI) allowing the number of valid bytes in the final message to be identified. See Table 13 for more details.

Table 13: Sample Count Indicator.

SCI	Sample count
000	312 samples per time slot
100	314 samples per time slot
001	374 samples per time slot
010	376 samples per time slot

In addition, other time slot related information may be contained within the final packet. All this information will be packed into the sample size,

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i.e. 32 bits, and will reside in the packet as if it were sample 315 or 377, as illustrated in the figure below.

When extracting the data, the receiver should assume that every timeslot has 315 or 377 samples within it. The baseband processing block should first read sample 315 or 377 to determine how many valid samples are within the buffer. Sample rate information is exchanged in upper protocol layers for example using RP3 control messages.

Figure 37 summarises GSM/EDGE/EGPRS2 uplink data mapping.

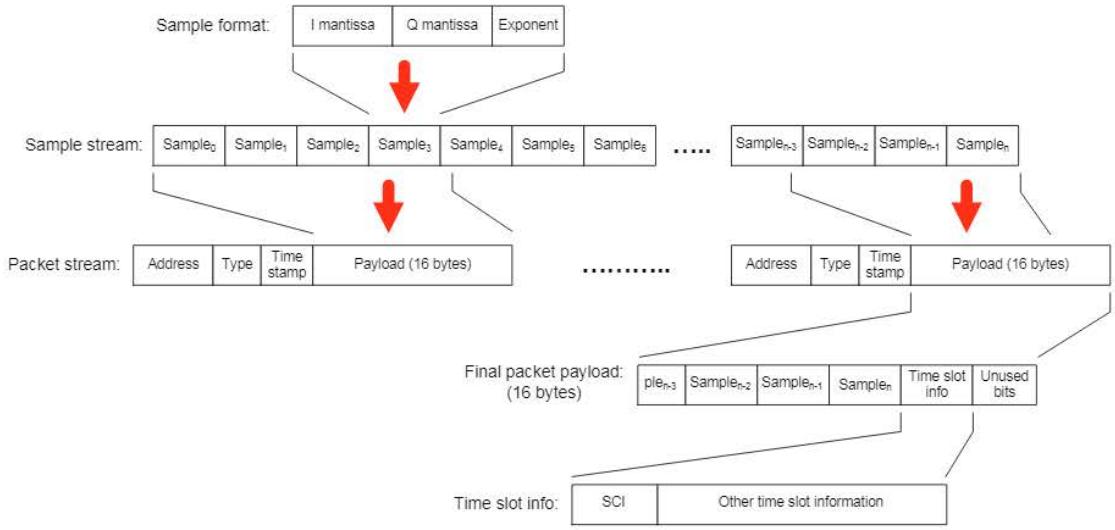


Figure 37: GSM/EDGE/EGPRS2 Uplink Payload Data Mapping

Detailed parameters for GSM/EDGE/EGPRS2 message transmission are provided in Appendix G.

4.4.9.4 GSM/EDGE Downlink Data Mapping

Two scenarios are supported in the GSM/EDGE downlink. The GSM/EDGE downlink data stream can be transmitted in either hard bits or as an up converted IQ data stream.

The hard bit data stream consists of 156.25 or 187.5 symbols per time slot. Integer number of symbols is achieved by using last symbol for 1.25 or 1.5 symbol periods, giving thus either 156 or 187 symbols to be transmitted per antenna carrier per time slot. For each symbol, 8 bits are used.

In the up converted IQ data option, one or more times over sampling is used for both symbol rates. Samples with two's complement code with 16 bit I and 16 bit Q are used.

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GSM time slot data may not fully occupy all the RP3 messages due to with pad bits are used. Unused payload bits at the end of the last RP3 message carrying GSM time slot data are filled with '1' bits.

In addition to the carrier data bits, it is necessary to send control data including carrier, power control, and phase/gain information.

In downlink, a time slot data to a modulator is partitioned in data messages, carrier control information messages, and power control information messages. The associated control is packed into control messages in order to protect the data by CRC check. Furthermore, in order to protect the control against bit errors, control messages can optionally sent twice over the bus. If CRC of the first associated control message indicates bit error, the receiver decodes the second, copy message. If control messages for a time slot have CRC failures and no correct message is received, Application layer is responsible for error handling.

Typically, respective channelizer (down converter) in the uplink direction needs also to have the associated control information. Therefore, after sending GSM/EDGE downlink data and control to modulator, baseband processing block sends frequency control and Gain Control messages to channelizer (down converter).

Detailed parameters for GSM/EDGE/EGPRS2 message transmission are provided in Appendix G.

4.4.9.5 CDMA2000 Downlink Data Mapping

The CDMA2000 downlink data stream has a chip rate of 1.2288 Mcps with an I&Q data format each of 16 bits giving 4 bytes per chip. This allows 4 consecutive chips of a single CDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. Two's complement code is used to represent both I and Q sample values.

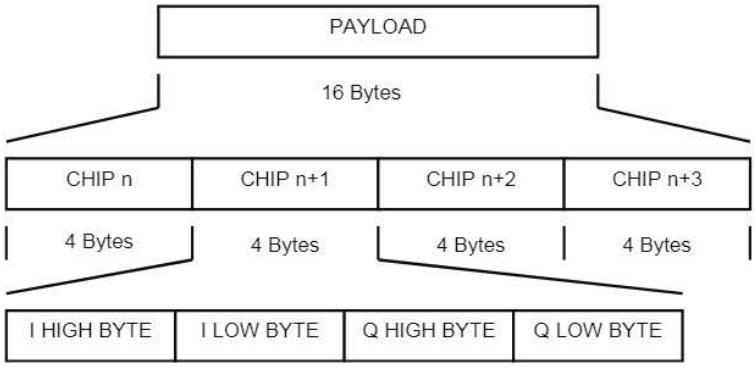


Figure 38: CDMA2000 DL Payload Mapping.

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4.4.9.6 CDMA2000 Uplink Data Mapping

The CDMA2000 uplink data stream has a sample rate of 2.4576 Msps (two times the chip rate), with an I&Q data format each of 8 bits giving 2 bytes per sample. This allows 8 consecutive samples (four chips) of a single CDMA2000 signal (antenna-carrier) to be mapped into the payload as illustrated below. As in case of downlink data transfer, two's complement code is used and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

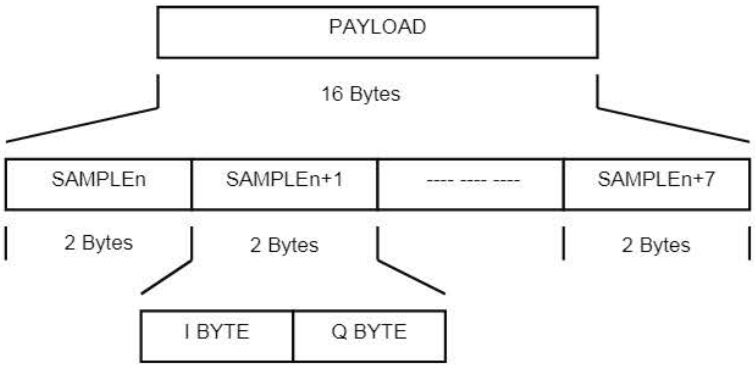


Figure 39: CDMA2000 UL Payload Mapping.

4.4.9.7 802.16 Downlink and Uplink Data Mapping

RP3 protocol supports data transfer of several 802.16 profiles, each with a specific sampling rate and multiple access method, as defined in Appendix D. For each profile, the same sampling rate is applied for both downlink and uplink data streams and no oversampling is applied, i.e. antenna-carrier data is transferred over RP3 link using sampling rates defined in Appendix D. Each I&Q sample consists of four bytes which allows four consecutive I&Q samples of a single 802.16 signal (antenna-carrier) to be mapped into the payload as illustrated below. Sixteen bit two's complement code is used for I and Q sample values and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

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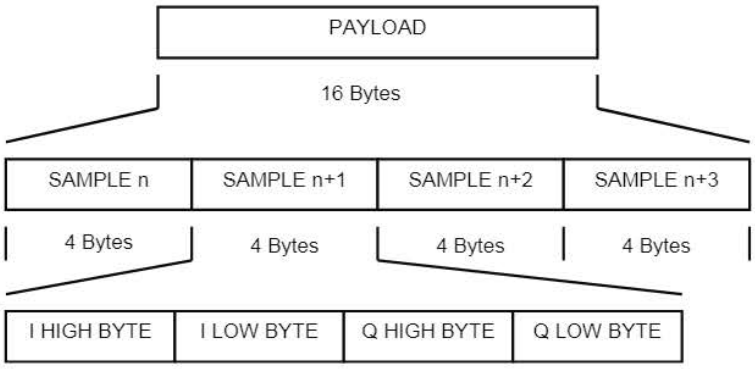


Figure 40: 802.16 downlink and uplink payload mapping.

4.4.9.8 LTE Downlink and Uplink Data Mapping

RP3 protocol supports data transfer of all LTE profiles, each with a specific sampling rate, as defined in Appendix F. For each profile, the same sampling rate is applied for both downlink and uplink data streams and no oversampling is applied, i.e. antenna-carrier data is transferred over RP3 link using sampling rates defined in Appendix F. Each I&Q sample consists of four bytes which allows four consecutive I&Q samples of a single LTE signal (antenna-carrier) to be mapped into the payload as illustrated below. Sixteen bit two's complement code is used for I and Q sample values and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

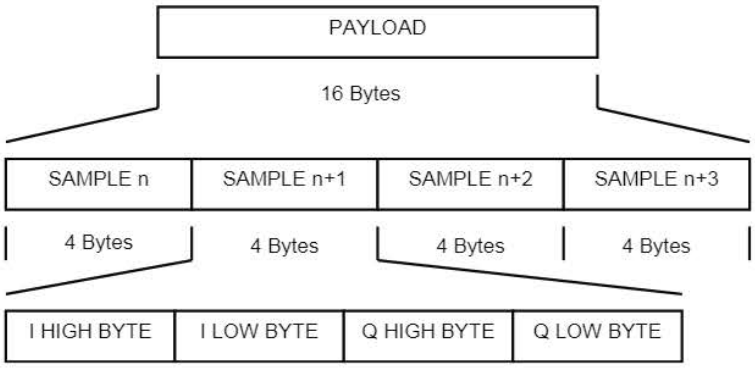


Figure 41: LTE downlink and uplink payload mapping.

4.4.10 Control and Measurement Data Mapping

Control and measurement messages, as identified by the CONTROL and MEASUREMENT type fields, use the payload to transport control and measurement information. A higher layer protocol is required within

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the payload to provide error detection. The following details two options for implementing the control and measurement signalling protocols.

4.4.10.1 Generic Control Message

Generic control message is illustrated in Table 14 and Figure 42 below, where the control message format consists of two payload fields: the message data and the 16 bit CRC. The timestamp field contains the value '000000' identifying this control message type.

The MSB of each message field is transmitted first (refer to Figure 12).



Figure 42: Generic control message.

Table 14: Content of generic control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000000
Data, 14 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

4.4.10.2 Control Message for Air Interface Synchronized Operations

Some control operations over the RP3/RP3-01 may need to be synchronized to a specific air interface frame. For these applications, a specific control message format is introduced as defined in Table 15 and Figure 43 below. The timestamp field contains the value '000001' identifying this control message type.

Table 15: Content of air interface synchronized control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000001

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Field	Value
Control subtype, 1 byte	Any content
Frame number, 1 byte	Least significant four bits of this byte are LSBs of air frame number. Four MSBs are set equal to '0000'.
Frame sample number, 3 bytes	Sample number within designated frame number to mark timing of control information.
Data, 9 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

A 24 bit sample counter, which counts samples over an air interface frame and resets at start of frame, is applied with the air interface synchronized control messages.

The MSB of each message field is transmitted first (refer to Figure 12).

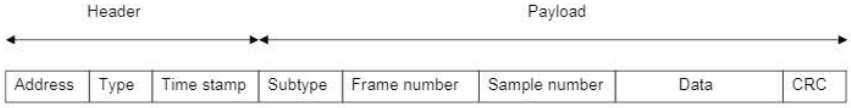


Figure 43: Air interface synchronized control message.

4.4.10.3 Generic Packet

The Generic Packet is a mechanism that allows multiple RP3 messages to represent a larger packet. Table 16 below defines the content of a RP3 message belonging to the Generic Packet.

Table 16: Content of the Generic Packet.

Field	Content
Address	Any valid address
Type	011111 (Generic Packet)
Time Stamp	See Table 17
Data, 16 bytes	A slice from a larger packet that is transferred over RP3

The time stamp field within the RP3 header is used to identify RP3 messages that belong to the same larger generic packet using two bits

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(MSBs) of the time stamp as Start Of Packet (SOP) and End Of Packet (EOP) indicators. The rest of the time stamp bits can optionally be used for packet identification for supporting up to 16 simultaneously transmitted generic packets to the same target address. The number of supported packet identifications can be chosen based on application. The four least significant bits of the time stamp field are set to zero if there does not exist need to support simultaneous packets to the same target address.

Table 17: Content of the time stamp field.

Time Stamp	Payload Content
10xxxx, where xxxx is set to 0000 (binary) or is optionally a binary number used for packet indication.	SOP: 16 first bytes of a Generic Packet + possible pad. The first byte of the Generic Packet is located immediately after RP3 header.
00xxxx, where xxxx is the same than for SOP	Next (second) RP3 message containing a part of the Generic Packet + possible pad.
…	
00xxxx, where xxxx is the same than for SOP	Nth RP3 message containing a part of the Generic Packet + possible pad.
11xxxx, where xxxx is the same than for SOP	EOP: The last RP3 message containing a slice from the Generic Packet + possible pad + CRC with packet identification xxxx.

A 16 bit CRC check sum, using the generator polynomial detailed in Section 4.4.10.4, is computed over the whole Generic Packet and possible pad bits and is then appended after the actual Generic Packet bits and pad. The Address, Type and Timestamp fields are excluded from the CRC. The content of the last RP3 message that has been allocated for Generic Packet + possible pad + CRC transfer is as defined in Table 18. The length of any Generic Packet + CRC is an integer multiple of 16 bytes, i.e. the last RP3 message transferring a portion of the Generic Packet is always full. Upper layer will provide pad bits when needed.

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Table 18: Payload of last message of Generic Packet.

Field	Value
Generic packet bits, 0 < *P* < 112 bits (14 bytes)	Content is arbitrary
–Possible pad, *Pad = P – 112* bits	'0' bits
Two last bytes (16 bits) of the payload	CRC check

Generic Packets with CRC failure shall be indicated to upper protocol layers and dropped by default. For every SOP there is exactly one legal EOP. If an EOP is received without a SOP, the error condition shall be indicated to upper protocol layers. If there is a SOP and then another SOP (without an EOP) the reception buffer may be flushed and the error condition shall be indicated to upper protocol layers.

If both Ethernet and Generic Packets are used in a system then the system should be designed in such a way as to prevent a burst of either Ethernet data or Generic Packets using all available control slots.

4.4.10.4 CRC Computation

For both control message options, the CRC is applied to the address, type, and timestamp fields of the message header as well as to the actual payload data. In total, 136 bits (17 bytes) are CRC protected. Generator polynomial $X^{16}+X^{12}+X^{5}+1$ is used with the high bit transmitted first. Initially, all CRC shift register elements are set equal to logical zero. Each control message enters the CRC shift register MSB first, i.e. leftmost bit of the message first (see Figure 43).

An example of CRC computation for a measurement message is provided enclosed. The first 17 bytes of the measurement message are the inputs to the CRC computation. The last two bytes shown in bold face is the CRC check sum. In the message header, Address equals to 0x01B0, Type to 0x01 (measurement), and Time Stamp to 0x00. The CRC equals to 0xAFD2.

Measurement message: (MSB) 0x0E, 0x00, 0x40, 0x50, 0x00, 0x00, 0xCC, 0x77, 0x0E, 0x0E, 0x0E, 0x0E, 0x11, 0x22, 0xFF, 0x88, 0x33, **0xAF, 0xD2**

4.4.10.5 Measurement Data Mapping

The RP3 interface facilitates the support and implementation of generic measurements and air interface synchronized measurements. Measurement messages use the same field format as the control messages with the Type field set to '00001' (Measurement). Thus, two options exist as defined in Section 4.4.10.1 and Section 4.4.10.2.

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5 Electrical Specifications

This sub-section defines the electrical specifications for the RP3 physical layer.

5.1 Overview

AC electrical specifications are given for both transmitter and receiver. They are specified for Baud Frequencies of 768, 1536, 3072, and 6144 MBaud.

The transmitter specification uses voltage swings that are capable of driving signals across RP3 compliant interconnect. Five RP3 compliant electrical interconnects are defined.

To ensure interoperability between components operating from different supply voltages or implemented in different technologies, AC coupling shall be used at the receiver input.

The overall performance requirement for BER shall be 10^{-15} for all electrical interconnects (TYPE 1, 2, 3, 4, and 5) and 10^{-12} for all optical interconnects.

5.1.1 Explanatory Note on Electrical Specifications

The parameters for the AC electrical specifications are guided by existing standards. For the line rates up to 3072 MBaud, the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [3] is used as a suitable basis to be modified for applications at the RP3-specific baud intervals described herein. For the 6144 MBaud line rate, the references are OIF-CEI-02.0 [14] Interoperability Agreement with its section 7 and related clauses and the Serial RapidIO v2 PHY specifications [15], which are also based on the OIF agreement, to be adapted to the specific needs in OBSAI.

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5.1.2 Compliance Interconnect

Five RP3 compliant interconnects are defined[1]:

- TYPE 1: A low loss interconnect definition specified in Section 5.4.1. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 2: A worst case, higher loss interconnect definition specified in Section 5.4.2. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 3: A low loss interconnect definition specified in Section 5.4.3. This interconnect shall be applied to 768, 1536, and 3072 Mbaud line rates.
- TYPE 4: A low loss interconnect definition specified in Section 5.4.4, targeting a PCB trace length from TX to RX of minimum 600 mm with 2 connectors. It shall be applied to 1536, 3072, and 6144 Mbaud line rates.
- TYPE 5, optional: A low loss interconnect definition specified in Section 5.4.4, targeting a PCB trace length from TX to RX of minimum 1000 mm with 2 connectors. It shall be applied to 1536, 3072, and 6144 Mbaud line rates.

Background information on all types interconnects is provided in Appendix E.

Note: The PCB trace length of TYPE4 and TYPE5 are difficult be be defined in length as the channels highly depend of many parameters such as PCB material, connector etc.

5.1.3 Equalization

With the use of high-speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, transmit and/or receive equalization may be used

At 6144 MBaud line rate, equalization is strongly recommended..

- For TYPE 4 interconnect a Linear Continuous Time equalizer may be used.

[1] Standard FR4 material was used as a reference when deriving the 3072 Mbaud channel model and this worst case model shall be applied both to backplane and front access cases.

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- For TYPE 5 interconnect also a Decision Feedback Equalizer (DFE) may be used.

5.2 Receiver Characteristics

The RP3 receiver electrical and timing characteristics are specified in the text and tables of this section. The RP3 receiver characteristics are summarized in Table 19, Table 20, Table 21, and Table 22.

Table 19: Receiver Characteristics – 768 MBaud

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss Differential Common mode	 10 6	 dB dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Jitter amplitude tolerance Minimum deterministic Minimum deterministic plus random Minimum total	 0.37 0.55 0.65	 UI p-p UI p-p UI p-p	Specifications include all but 10^{-15} of the jitter population.

Table 20: Receiver Characteristics – 1536 MBaud

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss Differential Common mode	 10 6	 dB dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Jitter amplitude tolerance Minimum deterministic Minimum deterministic plus random Minimum total	 0.37 0.55 0.65	 UI p-p UI p-p UI p-p	Specifications include all but 10^{-15} of the jitter population.

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Table 21: Receiver Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss Differential Common mode	 10 6	 dB dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Jitter amplitude tolerance Minimum deterministic Minimum deterministic plus random Minimum total	 0.37 0.55 0.65	 UI p-p UI p-p UI p-p	Specifications include all but 10^{-15} of the jitter population.

Table 22: Receiver Characteristics – 6144 MBaud

Parameter	Value	Units	Notes
Bit rate	6144	MBaud	+/- 100 ppm
Unit interval (nominal)	163	pS	
Input Differential Voltage	1200	mV	Max.
Receiver coupling	AC		
Return loss Differential Common mode	 8 6	 dB dB	Measured relative to 100 Ohm differential and 25 Ohm common mode, 100MHz to 4608 MHz
Input Common Mode Voltage	0 – 1800	mV	AC-coupling
Jitter amplitude tolerance Eye mask Bounded high probability Jitter Eye mask	 0.6 0.65 50	 UI p-p UI p-p mVp	At equalizer output. Specifications include all but 10^{-15} of the jitter population.

5.2.1 AC Coupling

The receiver shall be AC coupled to allow for maximum interoperability between components. AC coupling is considered part of the receiver for purposes of this specification unless explicitly stated otherwise.

5.2.2 Input Impedance

Receiver input impedance for up to 3072 MBaud shall result in a differential return loss better than 10 dB and a common mode return

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loss better than 6 dB from 100 MHz to (0.8 x Baud Frequency). Differential return loss at 6144MBaud shall be better than 8 dB and a common mode return loss better than 6 dB from 100 MHz to 3072 MHz. Receiver input impedance shall be measured at the module interface. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

5.2.3 Receiver Compliance Mask

The RP3 receiver shall comply with the eye mask specified in Figure 44 and Table 23.

The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a load as defined in Section 5.3.1.

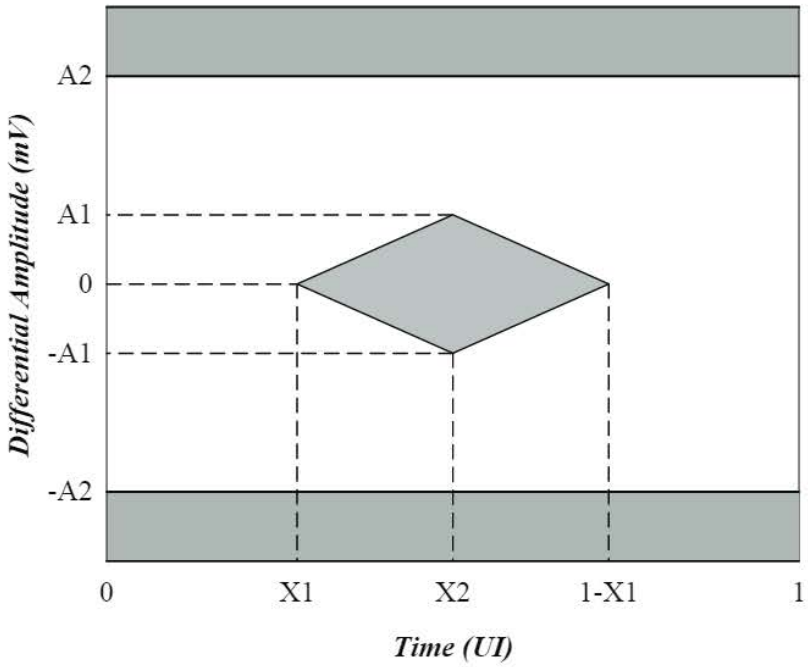


Figure 44: Receiver Compliance Mask

Note: The Receiver Compliance Mask with the values from Table 23 does not include the Sinusoidal Jitter SJ which is added in the Receiver Jitter Tolerance test, see 5.2.4.

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Table 23: Receiver Compliance Mask Parameters

Parameter	Value		Units
	≤ 3072	6144	MBaud
X1	0.275	0,3	UI
X2	0.5	0,5	UI
A1	100	50	mV
A2	800	600	mV

The jitter specifications include all but 10^{-15} of the jitter population.

5.2.4 Jitter Tolerance

The RP3 receiver shall tolerate a peak-to-peak total jitter amplitude of 0.65 UI. This total jitter is composed of three components: deterministic jitter, random jitter and an additional sinusoidal jitter. The jitter specifications include all but 10^{-15} of the jitter population.

Tolerance to deterministic jitter shall be at least 0.37 UI p-p. Tolerance to the sum of deterministic and random jitter shall be at least 0.55 UI p-p. The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 45 and the values of Table 24. This additional component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects.

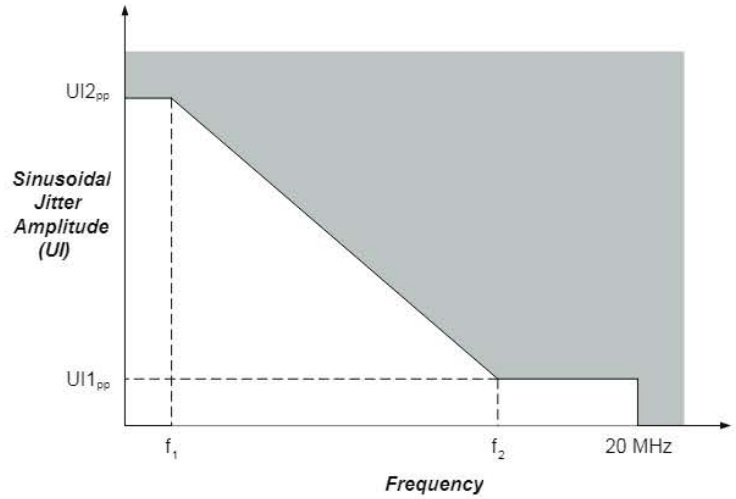


Figure 45: Sinusoidal Jitter Mask

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Table 24: Sinusoidal Jitter Mask Values

Baud Frequency (MBaud)	f_1 (kHz)	f_2 (kHz)	$UI1_{p-p}$	$UI2_{p-p}$
768	5.4	460.8	0.1	8.5
1536	10.9	921.6	0.1	8.5
3072	21.8	1843.2	0.1	8.5
6144	36.9	3686	0.05	5

5.2.5 Bit Error Ratio (BER) for Electrical Interconnects

For Type 1, 2, and 3 the receiver shall operate with a BER of 1×10^{-15} or better in the presence of an input signal as defined in Section 5.2.3.

For 6144Mbps line rate, noise and crosstalk may have a significant impact on BER. In the same way as in [14] and [15], to verify the receiver under test, the receiver shall meet a BER 10^{-12} with a stressed input eye mask. The stressed eye in such measurement includes sinusoidal, high probability Gaussian jitter as well as additive crosstalk. See also [16].

5.3 Transmitter Characteristics

The RP3 transmitter electrical and timing characteristics are specified in the text and tables of this section. The RP3 transmitter characteristics are summarized in: Table 25, Table 26, Table 27 and Table 28.

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1 *Table 25: Transmitter Characteristics – 768 MBaud*

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential amplitude Maximum Minimum	 1600 400	 mV_{p-p} mV_{p-p}	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter Maximum deterministic jitter ($J_{D)}$ Maximum total jitter (JT)	 0.17 0.35	 UI UI	Specifications include all but 10^{-15} of the jitter population.

2 *Table 26: Transmitter Characteristics – 1536 MBaud*

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential amplitude Maximum Minimum	 1600 400	 mV_{p-p} mV_{p-p}	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter Maximum deterministic jitter ($J_{D)}$ Maximum total jitter (JT)	 0.17 0.35	 UI UI	Specifications include all but 10^{-15} of the jitter population.

3

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Table 27: Transmitter Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential amplitude Maximum Minimum	 1600 400	 mV_{p-p} mV_{p-p}	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter Maximum deterministic jitter ($J_{D)}$ Maximum total jitter (JT)	 0.17 0.35	 UI UI	Specifications include all but 10^{-15} of the jitter population.

Table 28: Transmitter Characteristics – 6144 MBaud

Parameter	Value	Units	Notes
Bit rate	6144	MBaud	+/- 100 ppm
Unit interval (nominal)	163	pS	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential amplitude Maximum Minimum	 1200 800	 mV_{p-p} mV_{p-p}	
Absolute output voltage limits Maximum Minimum	 2.3 -0.4	 V V	
Differential output return loss		dB	See 5.3.3
Output Common Mode Voltage	100 – 1700	mV	
Output jitter Maximum deterministic jitter ($J_{D)}$ Maximum total jitter (JT)	 0.15 0.30	 UI UI	Specifications include all but 10^{-15} of the jitter population.

An RP3 Transmitter eye mask, to be satisfied with or without transmit equalization, is illustrated in Figure 46. This eye mask is provided

- for information only, not used for RP3 compliance testing in case of line rates up to 3072 MBaud

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- to be normative and used for compliance testing in case of 6144 MBaud line rate

The parameters are defined in Table 29.

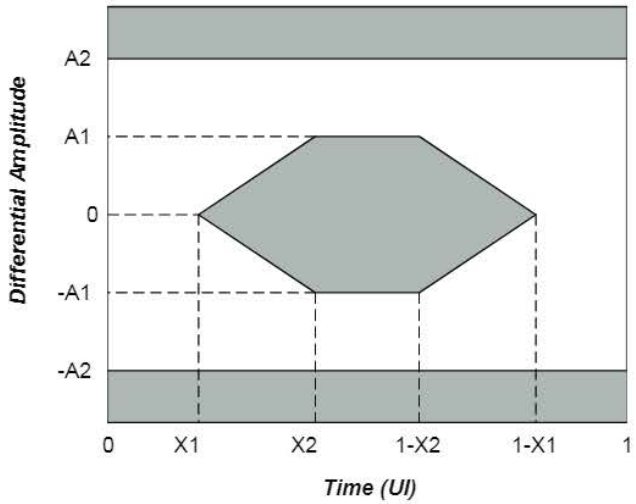


Figure 46: Transmitter Output Mask

Table 29: Transmitter output mask parameters

Parameter	Value		Unit
	≤ 3072	6144	MBaud
X1	0.175	0.15	UI
X2	0.39	0.4	UI
A1	200	400	mV
A2	800	600	mV

5.3.1 Load

The load is 100 Ohms +/- 5% differential up to (0.8 x Baud Frequency) unless otherwise noted.

5.3.2 Amplitude

For baud rates ≤ 3072 MBaud, the maximum transmitter differential amplitude shall be 1600 mV_{p-p}, including any transmit equalization. The minimum transmitter differential amplitude shall be 400 mV_{p-p}.

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For a baud rate of 6144 MBaud, the maximum transmitter differential amplitude shall be 1200 mV_{p-p}, including any transmit equalization. The minimum transmitter differential amplitude shall be 800 mV_{p-p}. To achieve the best far end eye opening, the amplitude should be programmable.

The minimum amplitude may not be suitable for transmission over a compliant channel. The absolute driver output voltage shall be between –0.4 V and 2.3 V with respect to ground. DC-referenced logic levels are not defined, as the receiver is AC coupled.

5.3.3 Output Impedance

For baud rates ≤ 3072 MBaud, the differential return loss, SDD22, of the transmitter shall be better than:

- *-10 dB for (Baud Frequency/10) < Freq (f) < 625 MHz*, and
- *-10 dB + 10log(f/625 MHz) dB for 625 MHz <= Freq(f) <= (Baud Frequency) MHz*

For baud rates ≤ 3072 (FFS) MBaud, the differential return loss, SDD22, of the transmitter shall be better than:

- *-8 dB for 100 MHz < f < 3072MHz*, and
- *-8 dB + 16.6*log10(f/3072 MHz) dB for 3072 MHz <= f <= 6144 MHz*

Differential return loss shall be measured at the module interface. The reference impedance for the differential return loss measurements is 100 Ohm resistive. The output impedance requirement applies to all valid output levels.

5.3.4 Transmitter Compliance

To measure compliance of an RP3 transmitter, the transmitter shall be connected to a compliance interconnect model. RP3 specifies five interconnect models for transmitter compliance testing, as introduced in 5.1.2:

In all cases, the RP3 transmitter shall be compliant if the signal presented to the RP3 receiver at the end of the compliance interconnect model (far-end) meets the minimum RP3 receiver compliance mask.

A compliant RP3 transmitter shall meet TYPE 1 and TYPE 2 compliance interconnect test cases, or TYPE 3, or Type4, or Type 5 compliance interconnect test case. In case of 6144 MBaud, Type 4 and

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Type 5, the "Statistical Eye" methodology shall be used for compliance testing as described in [2] (FFS) and [3].

5.4 Measurement and Test Requirements

This section defines the measurement and test requirements for an RP3 electrical interface. These measurement and test requirements are based upon those of the XAUI electrical interface as specified in Clause 47 of IEEE 802.3ae-2002 [3] for Type 1, 2 and 3 compliant interconnects. The measurement and test requirements for Type 4 and 5 compliant interconnects are based on the Rapid IO Part6: LP-Serial Physical Layer specification Rev.2.0 [15] or OIF-CEI-02.0 agreement [14] respectively.

Typical test instruments and their cabling are based on single ended 50 Ohm termination. In order to achieve the required 100 Ohm differential, as well as common mode 25 Ohm, resistive loads, in all measurements and tests related to electrical specifications, both lines of a differential transmission interconnect pair shall be terminated individually with 50 Ohm +/- 5% resistors to ground. Such a load shall maintain this accuracy in its resistive characteristics at least up to 0.8 x Baud Frequency. The requirements for the Type 4 and 5 compliant interconnect test and measurements are detailed in Chapter 10 of [15].

5.4.1 TYPE 1 Compliance Interconnect Definition

The TYPE 1 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 1 compliance interconnect shall be:

$$\textit{Differential Insertion Loss } (F) \leq (0.2629 \times \sqrt{F}) + (0.0034 \times F) + (12.76 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

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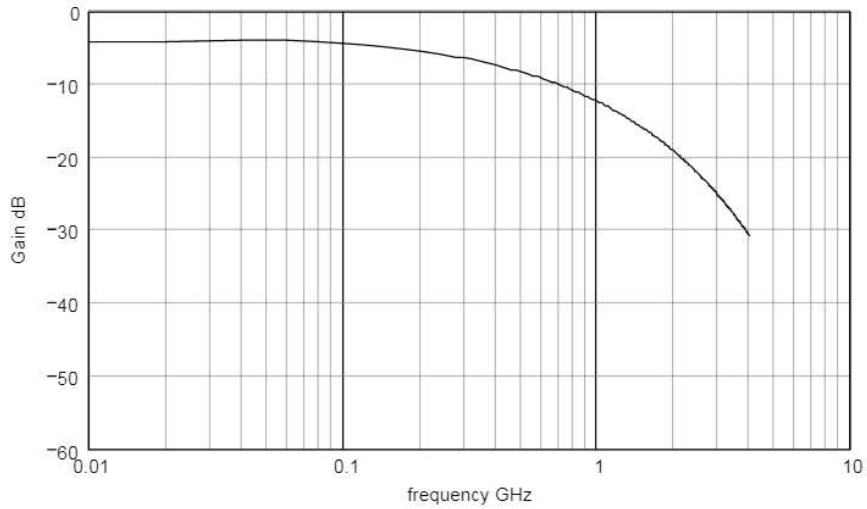


Figure 47: TYPE 1 Compliance Interconnect Differential Insertion Loss

5.4.2 TYPE 2 Compliance Interconnect Definition

The TYPE 2 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 2 compliance interconnect shall be:

$$\textit{Differential Insertion Loss } (F) \leq (0.1 \times \sqrt{F}) + (0.011 \times F) + (6 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

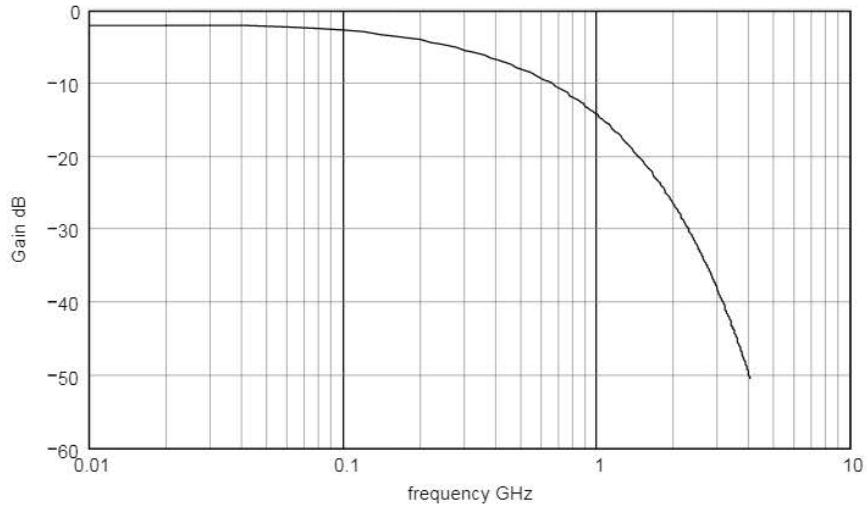


Figure 48: TYPE 2 Compliance Interconnect Differential Insertion Loss

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5.4.3 TYPE 3 Compliance Interconnect Definition

The TYPE 3 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768, 1536, and 3072 Mbaud line rates.

The worst case TYPE 3 channel differential Insertion Loss (transfer function) SDD21 shall meet Equation 1 where as the variable ***f*** (frequency) unit is in GHz. The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 return loss, therefore differential coupling effects may be neglected for insertion loss SDD21.

$$IL_{SDD\ 21}(dB) = \begin{cases} -10\sqrt{f/f_0} & ; \quad f < f_0 \\ -7(f - f_0)^{1.15} - 10 & ; \ f_0 \le f < 4.5GHz \end{cases}$$

$$f_0 = 1.5GHz$$

Equation 1: Differential Transfer Function (IL) Model

Figure 49 depicts the above TYPE 3 transfer function chart.

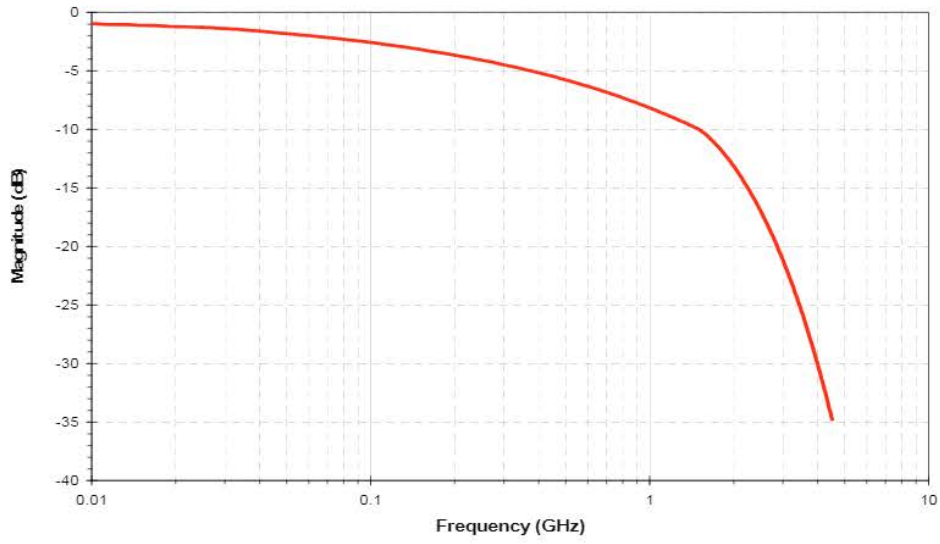


Figure 49: TYPE 3 Differential Transfer Function Chart

The worst case TYPE 3 channel differential return loss (RL) SDD11 shall meet Equation 2 where as the variable ***f*** (frequency) unit is in GHz.

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$$RL_{SDD11}(dB) = \begin{cases} -15 & ; \ f < 1GHz \\ 5(f) - 20 & ; \ 1 \le f < 3GHz \\ -5 & ; \ 3 \le f < 4.5GHz \end{cases}$$

Equation 2: Differential Return Loss Model

The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 insertion loss, therefore differential coupling effects may be neglected for return loss SDD11.

Figure 50 depicts the above TYPE 3 Return Loss chart.

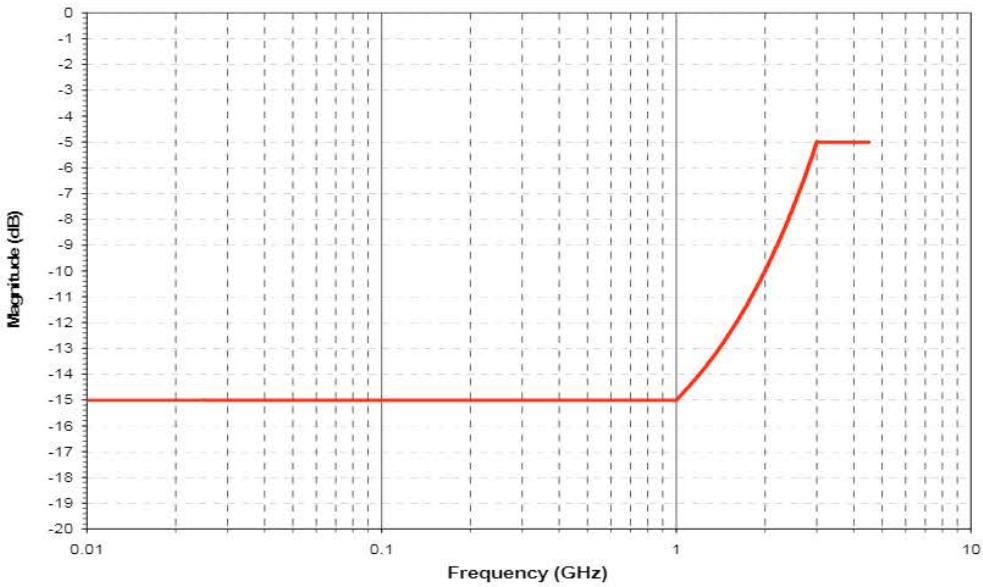


Figure 50: TYPE 3 Differential Return Loss Chart.

5.4.4 TYPE 4 and TYPE 5 Compliance Interconnect Definition

A serial link is comprised of a transmitter, a receiver, and a channel which connects them. Typically, two of these are normatively specified, and the third is informatively specified. In this specification, the transmitter and channel are normatively specified, while the receiver is informatively specified.

This specification follows the OIF inter-operability or compliance methodology and is based on using transmitter and receiver reference models, measured channel S-parameters, eye masks, and calculated "statistical eyes". These "statistical eyes" are determined by the reference models and measured channel S-parameters using publicly available StatEye MATLAB® scripts and form the basis for identifying

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compliant transmitters and channels. Compliant receivers are identified through a BER test.

Reference models are used extensively because at 6.144Gbaud data rates the incoming eye at the receiver may be closed. This prevents specifying receiver compliance through receiver eye masks as is typically done at lower data rates.

A compliant channel is determined using the appropriate transmitter and receiver reference model, measured S-parameters for the channel under consideration, and the StatEye script. A compliant channel is one that produces a receiver equalizer output "statistical eye" which meets a BER ≤ 10-15 using StatEye.

The reference model for the complete serial link as defined in [4] is shown in figure xxx.

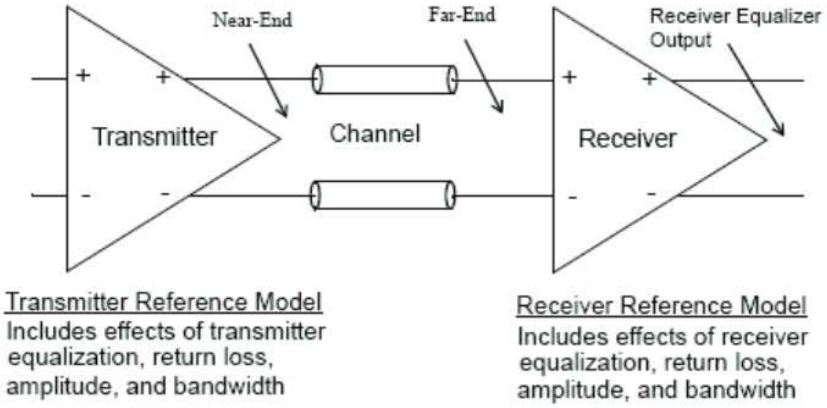


Figure 51: OIF reference model.

5.4.4.1 TYPE 4 and TYPE 5 Channel Compliancy

The following steps shall be made to identify which channels are to be considered compliant:
The forward channel and significant crosstalk channels shall be measured using a network analyzer 6.144 Mbaud

1. A single pre or post tap transmitter with <= 6dB of emphasis, with infinite precision accuracy.
2. A Tx edge rate filter: simple 40dB/dec low pass at 75% of baud rate, this is to emulate both Rx and Tx -3dB bandwidths at 3/4 baud rate.
3. A transmit amplitude of 800mVppd.

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4. Additional Uncorrelated Bounded High Probability Jitter of 0.15UIpp (emulating part of the Tx jitter).
5. Additional Uncorrelated Unbounded Gaussian Jitter of 0.15UIpp (emulating part of the Tx jitter).
6. The reference transmitter shall use the worst case transmitter return loss at the baud frequency. In order to construct the worse case transmitter return loss, the reference transmitter should be considered to be a parallel R and C, where R is the defined maximum allowed DC resistance of the interface and C is increased until the defined maximum Return Loss at the baud frequency is reached.
7.

   (a) TYPE 4
   The reference receiver uses a continuous-time equalizer with 1 zero and 1 pole in the region of baudrate/100 to baudrate. Additional parasitic zeros and poles must be considered part of the receiver vendor's device and The TYPE 4 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 6144 Mbaud line rates.be dealt with as they are for the reference receiver. Pole and Zero values have infinite precision accuracy. Maximum required gain/attenuation shall be less than or equal to 4dB.

   (b) TYPE 5
   The reference receiver uses a 5 tap DFE, with infinite precision accuracy.
8. The reference receiver shall use the worst case receiver return loss at the baud frequency. In order to construct the worse case receiver return loss, the reference receiver should be considered to be a parallel R and C, where R is the defined maximum allowed DC resistance of the interface and C is increased until the defined maximum Return Loss at the baud frequency is reached.

Table 30: Receiver Equalization Output Eye Mask

Parameter	Symbol	Max	Units
Eye mask	R_X1	0.30	UI
Eye mask	R_Y1	50	mV
Bounded High Probability Jitter	R_BHPJ	0.325	UI

9. Any parameters that have degrees of freedom (e.g. filter coefficients or sampling point) shall be optimized against the

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amplitude, at the zero phase offset, as generated by the Statistical Eye Output, e.g. by sweeping all degrees of freedom and selecting the parameters giving the maximum amplitude. A receiver return loss, as defined by the reference receiver, shall be used.

10. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Section 8.7.5, "Statistical Eye Methodology", and confirmed to be within the requirements of the equalized eye mask as specified in Table Table 30 at the required BER, 10^{-15}.

5.4.5 Eye Mask Measurements for TYPE 1, 2, and 3 Compliant Interconnects

For the purpose of eye mask measurements, the effect of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for mask measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae-2002 [3]. The RP3 link shall be active in both transmit and receive directions, and opposite ends of the link shall use synchronous clocks. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 1 x 10^{-15}. The eye pattern shall be measured with AC coupling and the compliance mask centered at 0 Volts differential. The left and right edges of the mask shall be aligned with the mean zero crossing points of the measured data eye as illustrated in Figure 52.

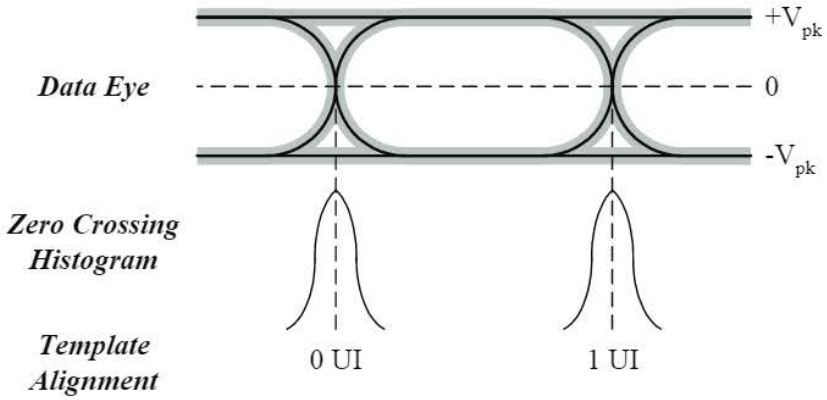


Figure 52: Eye Mask Alignment

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5.4.6 Transmit Jitter for TYPE 1, 2, and 3 Compliant Interconnects

Transmit jitter shall be measured at the driver output when terminated according to the definition in Section 5.4.

5.4.7 Jitter Tolerance

5.4.7.1 TYPE 1, 2, and 3 Compliant Interconnects

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 5.2.4 and then adjusting the signal amplitude until the data eye contacts the 4 points of the minimum eye opening of the receiver compliance mask specified in Figure 44 and Table 23. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye mask measurement requirements are defined in Section 5.4.5. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade rolloff below this. The required sinusoidal jitter specified in Section 5.2.4 is then added to the signal and the test load is replaced by the receiver being tested.

5.4.7.2 TYPE 4 and 5 Compliant Interconnects

For Type 4 and Type 5, the overall BER of 10^{-15} or better shall be confirmed with the StatEye calculation.

5.4.8 Noise and Crosstalk

In RapidIO Part 6: LP-Serial Physical Layer Specification Rev. 2.0 the input stressed eye includes sinusoidal, high probability, and Gaussian jitter as defined in the appropriate sections of this specification, along with any necessary additive crosstalk. Additive crosstalk is used to ensure that the receiver under test is adequately stressed if a low loss channel is used in the measurement. The additive input crosstalk signal is determined using the channel S-parameters, receiver reference model, and the StatEye script. It must be of an amplitude such that the resulting receiver equalizer output eye, given the channel, jitter, and crosstalk, is as close as feasible in amplitude when compared to the defined minimum amplitude used for channel compliance

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6 RP3-01 Interface for Remote RF Unit

There exist base station configurations where remote RF units are used. This chapter specifies an extension of the Reference Point 3 protocol for remote RF unit use.

Section 6.1 defines architecture for RP3-01 interface while protocol stack for data transfer is defined in Section 6.2.

6.1 Architecture

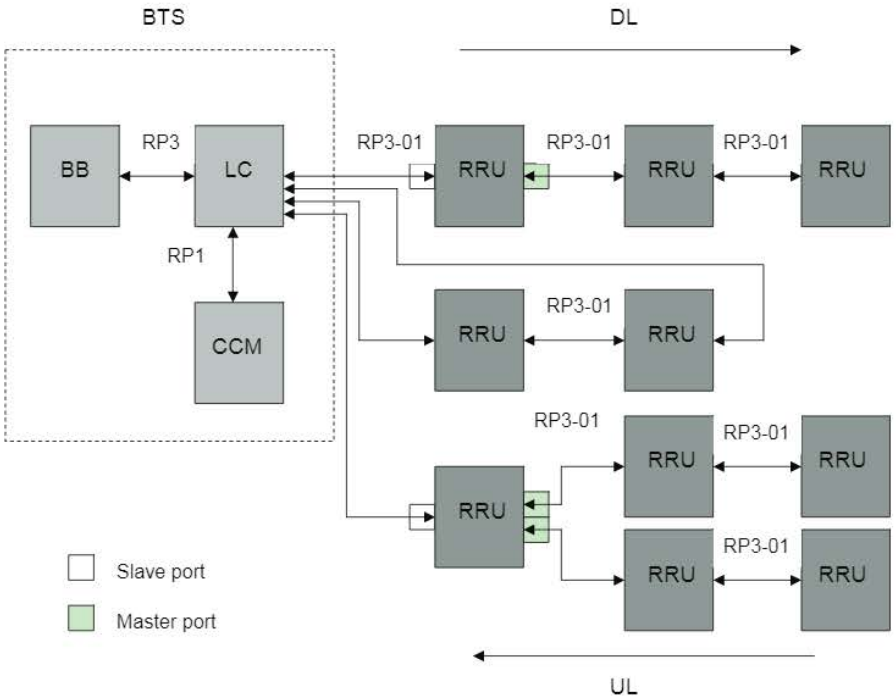


Figure 53: RP3-01 example architecture.
Base station with remote RF units (RRUs). RRUs in chain, ring, and tree-and-branch topologies. Examples of RP3-01 master and slave ports of RRUs are also shown.

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Figure 53 shows an example architecture of a BTS with remote RF units (RRUs). The figure provides a logical architecture and does not imply physical implementation of the BTS. The Local Converter (LC) may exist as a separate module or it may be integrated with other modules, such as the baseband module. For definitions of terms used in the figure and in the RP3-01 protocol description, refer to the Glossary.

The RP3-01 protocol shall support several RRU topologies, including point-to-point connection between a BTS and an RRU as well as chain, tree-and-branch and ring topologies.

Each RRU has one RP3-01 slave port and, optionally, one or more master ports. The slave port is connected toward the BTS either directly or through other RRU(s) while master port(s) connect to RRU(s) that are next in the chain. Slave and master ports are defined dynamically at BTS startup. The RP3-01 receiver first detecting transmission from the BTS, and its associated transmitter, are defined as the slave port while other ports are defined to be master ports.

Figure 54 provides an overview of RP3-01 protocol functionality at the LC and RRU for the case of a point-to-point topology. Section 6.2 defines in detail how RP1 and RP3 data is mapped into RP3-01 format. Basically, RP3-01 stands for an RP3 protocol where RP1 data is transferred in RP3 messages, between LCs and RRUs.

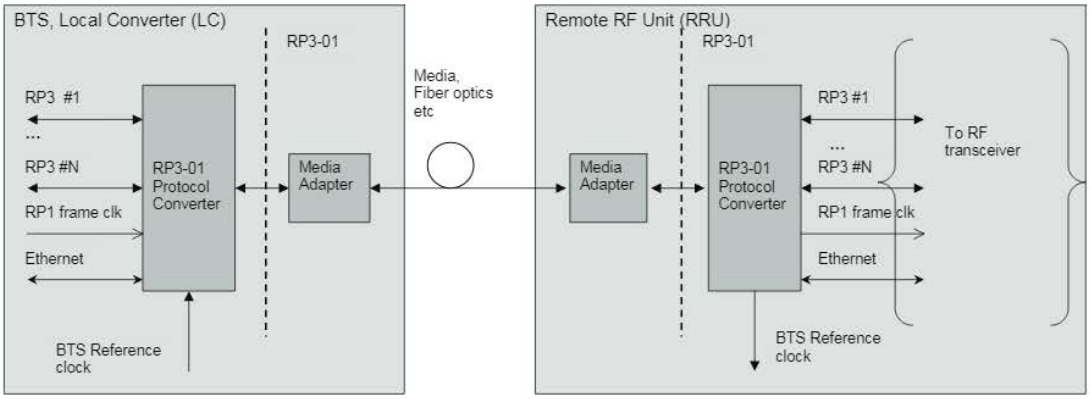


Figure 54: Logical model of OBSAI RP3-01 point-to-point interface.

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6.2 Protocol Stack

6.2.1 Physical Layer

6.2.1.1 Media Adapter and Media

The media adapters and media defined in Appendix A shall be used.

6.2.1.2 Line Rates

RP3-01 and RP3 line rates are the same, i.e. 768Mbps, 1536Mbps, 3072Mbps, or 6144Mbps line rate shall be used.

6.2.2 RP3-01 - Transfer of RP1 Data Over RP3

RP3-01 is an extension of the RP3 protocol specifically designed for data transfer between a BTS and one or more remote RF units. RP3-01 is equivalent to the RP3 protocol except for the fact that different physical layer technologies, suitable for supporting data transmission over long distances, are applied. In order to minimize the number of connections to RRUs, RP1 data is mapped into RP3 messages. RP1 data includes Ethernet and frame clock bursts.

In the RP3-01 protocol, bandwidth is allocated to all data transfers by defining message transmission rules (see Section 4.4.4). Separate transmission rules shall be given as needed to RP1 Ethernet, RP1 frame clock burst, RTT measurement, Virtual HW reset, loop back, RP3 data, and RP3 control messages. Typically, RP3 data and control messages are already scheduled at baseband and RF modules in downlink and uplink directions, respectively, using message transmission rules. RTT measurement, HW reset, and loop back are examples of RP3-01 link O&M messages. RP1 and RP3-01 link O&M data can be transmitted in any RP3 message slot, as illustrated by Figure 55.

6.2.3 RP1 Frame Clock Bursts

The Control and Clock Module (CCM) shall provide frame timing information for each air interface standard, independently, via periodic synchronization bursts, as shown in Figure 56 [4]. A dedicated link is used to transfer the frame timing information to modules that are located in a BTS cabinet. For a RRU, frame timing information is transferred over the RP3-01 protocol by mapping the information within the RP1 frame clock bursts, into RP3 messages, and then regenerating

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the RP1 frame clock burst at the RRU by applying the algorithm defined in this section.

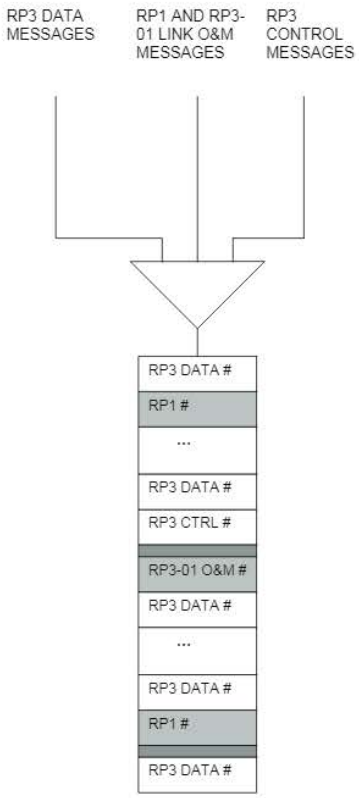


Figure 55: Examples of mapping RP1 and RP3-01 link O&M data into RP3 messages.

Start 1	Type 8	Type Specific Information 64	CRC 16	End 1

Figure 56: RP1 frame clock synchronization burst from CCM.

The LC is responsible for multiplexing RP1 frame clock synchronization bursts into RP3 messages and it performs the following functionality.

- A counter, called *c1,* is reset and started at the beginning of the RP3-01 Master Frame and this counter measures time as a multiple of 1/(*8**76.8)MHz. Thus 614.4MHz is the frequency of the reference clock.
- The RP1 Frame Clock Burst (FCB) from the CCM is received and processed.

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- The RP1 frame clock burst from the CCM is discarded if the CRC check fails
- Only the first RP1 frame clock burst after the beginning of the RP3-01 Master Frame is accepted
- If a new RP1 synchronization burst is received before the previous is transmitted as FCB message, the new RP1 burst is discarded and an interrupt is generated to upper layers

The CCM is responsible for alternating the transmission order of the RP1 frame clock burst for the different air interface standards, so that timing for each standard will be transferred to RRUs.

- The arrival time of the end bit of the RP1 frame clock burst, from the beginning of the RP3-01 Master Frame, is measured by the counter *c1* and stored into an RP3-01 frame clock synchronization message defined by Figure 57 and Table 31. Specifically, the arrival time of the end bit stands for the falling edge of the end bit as sampled by the raising edge of the system clock. System and System Frame Number (SFN) information from RP1 frame clock synchronization burst are also stored into the message. After the message has been constructed, including the header, the CRC check for the whole message is computed and added to end.
- RP3-01 frame clock synchronization message shall be transmitted to RRUs in an RP3 message. The RP3-01 FCB message shall be transmitted in a time window of 9ms, starting from the end of the RP1 synchronization burst.

RRUs are responsible for all of the computations that are required for frame time transfer. The algorithm described below is a general one and supports all air interface standards.

- Counter *c2* is reset to zero and started at the beginning of each RP3-01 Master Frame, except if the *c2* counter is serving a FCB (RP3 Frame Clock synchronization Burst) message. The *c2* counter measures time as a multiple of 1/(*8**76.8)MHz. Thus 614.4MHz is the frequency of the reference clock.
  - When FCB message is being served, c2 increments without reset at the MF boundary
  - If FCB message is being served by c2 counter when new FCB message is received from LC, then the new FCB message shall be discarded and an interrupt is generated to upper layer to indicate erroneous situation
- The RRU receives the RP3-01 frame clock synchronization message
- When RP3-01 FCB message type has been detected, the present c2 counter value is captured, without disturbing c2 counting. This captured c2 value is called FCB_message_rx_time

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- In case a new FCB message while an older message was being served by c2 counter, the count is not captured (erratic situation).

- The received message is discarded if the CRC check fails
- The RRU computes the buffering time B_{RRU} of the frame clock synchronization burst at the RRU, as follows
  - Find minimal positive integer value for parameter *k* such that

    $$k * SFN\_FRAME\_TIME \geq RP3-01\_MASTER\_FRAME\_TIME$$

    where *SFN_FRAME_TIME* equals to the length of the air interface frame and *RP3-01_MASTER_FRAME_TIME* is always equal to 10ms. As an example, assume that *SFN_FRAME_TIME* is equal to 10 ms (WCDMA case). Then *k* equals to 1.
  - The captured c2 value is compared to c1 value received in the FCB message
  - If FCB_message_rx_time > c1, then B_{RRU} is then computed using formula:

    $$B_{RRU} = k * SFN\_FRAME\_TIME + c1 * 1/(8 * 76.8MHz) - RP1\_FRAME\_CLOCK\_BURST\_TIME$$

    If FCB_message_rx_time < c1, then B_{RRU} is then computed using formula:

    $$B_{RRU} = k * SFN\_FRAME\_TIME - RP3-01\_MASTER\_FRAME + c1 * 1/(8 * 76.8MHz) - RP1\_FRAME\_CLOCK\_BURST\_TIME$$

    In the above equation, *RP1_FRAME_CLOCK_BURST_ TIME* stands for the time required to transmit an RP1 frame clock burst in RP1 interface. This equals to 90*1/3.84MHz= 23.4375us
- The RRU increments the System Frame Number (SFN) by *k*
- When the counter *c2* reaches B_{RRU}, the recomputed RP1 frame clock burst shall be sent to functional blocks within RRU.
  - The format of the recomputed RP1 frame clock burst is equal to that of the original burst received from the CCM (see Figure 56) but the value of the System Frame Number has been incremented by *k* and the CRC check value has been recomputed.
- The functional blocks of the RRU shall receive and decode SFN in exactly the same manner as in the case of a single cabinet BTS.

The content of an RP3-01 frame clock synchronization message is defined in detail in Table 31.

The MSB of each message field is transmitted first (refer to Figure 12).

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Figure 57: RP3-01 frame clock synchronization message.

Table 31: Content of RP3-01 frame clock synchronization message.

Field	Value
Address	Broadcast address (typically)
Type	Frame clock burst, 01001 in binary
Time stamp	000000
System, 8 bits	Refer to [4].
System Frame Number, 64 bits	Refer to [4].
c1 counter value, 26 bits	Positive integer number defining the arrival time of the RP1 frame clock burst from CCM with respect to RP3-01 Master Frame start as multiples of 1/(*8**76.8) MHz.
Reserved, 14 bits	All zeros
CRC, 16 bits	Refer to Section 4.4.10.4 for the definition of the CRC.

Figure 58 illustrates the timing of RP1 frame clock burst transmissions. As can be seen from the figure, the RRU obtains its frame timing from a "future" System Frame Number *p+k* not from the System Frame Number *p* that is used by all baseband and RF modules located in the BTS cabinet.

The propagation delay $\Delta_{LC\text{-}RRU}$ shown in Figure 58 may be large when an RRU is located far away from the BTS. The above algorithm does not take into account the impact of propagation delay in frame clock transfer. Propagation delay can be measured and removed from the frame clock timing. Section 6.2.6.2 specifies an algorithm for propagation delay measurement.

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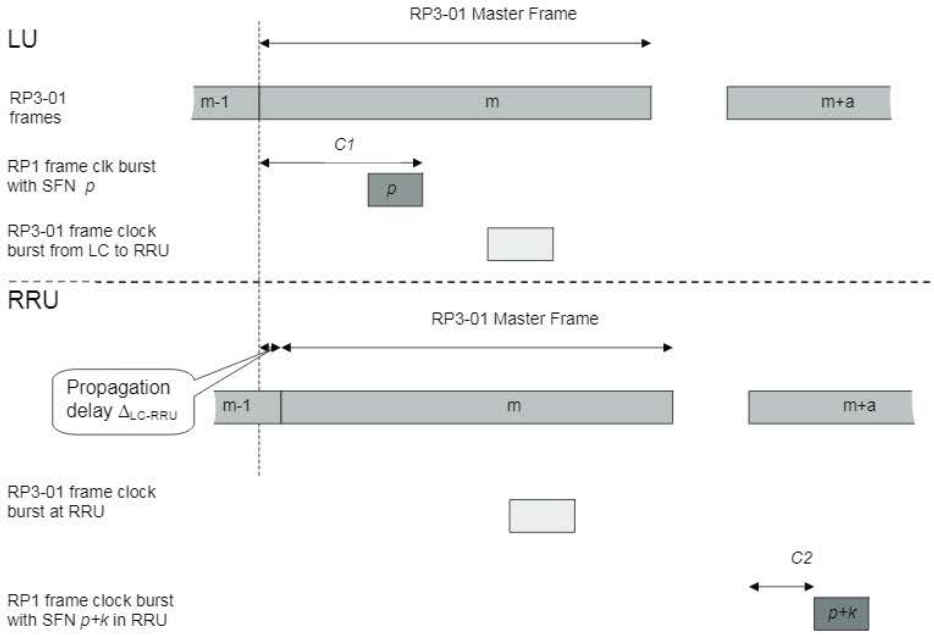


Figure 58: Timing principle in RP1 frame clock burst transfer.

6.2.4 Ethernet Transmission

Between any two RP3-01 nodes, whether in a BTS or an remote RF unit, a point-to-point Ethernet transfer is applied, as shown in Figure 59. Thus, only a single logical connection is allocated for Ethernet MAC messages between RP3-01 nodes. Where chain, ring, or tree-and-branch topologies are used for a number of remote RF units, the Ethernet switch in each RRU shall decide whether the MAC frame is consumed in that RRU or whether it will be forwarded to the next node.

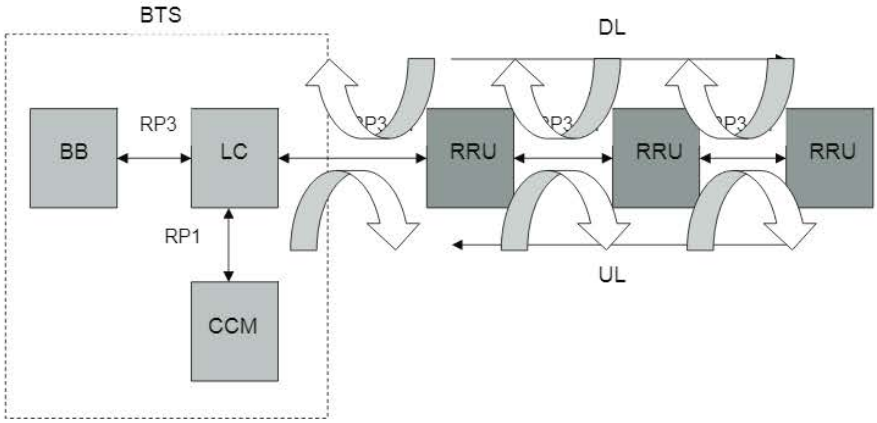


Figure 59: Ethernet frame transfer over RP3-01 network is done as a point-to-point transfer between a pair of nodes.

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The Ethernet throughput over each RP3-01 link is specifically allocated by message transmission rules, as defined in Section 6.2.2.

Ethernet MAC frames are mapped into RP3 messages and transferred over the RP3-01 protocol. At the input, there exist MAC frames as specified by 802.3-2002 [10]. A MAC frame consists of preamble, start frame delimiter, the addresses of the frame's source and destination, a length or type field, MAC client data, a field that contains padding if required, a frame check sequence, and an extension field, if required. Each MAC frame is sliced into consecutive RP3 messages and the time stamp field defines the beginning and end of each MAC frame, as indicated in Table 32.

Table 32: Content of the time stamp field of RP3 messages in relation to Ethernet MAC frame data of the payload.

Time Stamp	Payload Content
100000	16 first bytes of an Ethernet MAC frame. The first byte of the MAC frame is located immediately after RP3 header.
000000	Next (second) RP3 message containing a part of the MAC frame.
…	
000000	Nth RP3 message containing a part of the MAC frame.
1xxxxx	The last RP3 message containing a slice from the MAC frame and xxxxx, a binary number, indicates the number of bytes from the start of RP3 payload containing MAC frame data (counting started from the byte after the header).

Table 33 defines the content of RP3 messages when used for Ethernet data transfer. The 'Address' field contains the address of the next RP3-01 node, The 'type' field indicates that Ethernet MAC data is contained in the payload, and all bits of the payload contain MAC data, excluding the last RP3 message, which may be partially filled.

The bytes (octets) of an Ethernet MAC frame are transmitted over an RP3-01 link in the order specified by the 802.3 specification. The MSB of each 802.3 byte as defined in 802.3 specification is assigned to the MSB of each RP3 message payload byte.

At the receiver, MAC frames are reconstructed from the payload of RP3-01 Ethernet messages by concatenation according to the content of the 'type' and 'time stamp' fields. By monitoring the 'type' field, the receiver shall identify RP3 messages containing Ethernet data. The

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transmitter shall send only one MAC message at a time from which the 'time stamp' field can be used to identify the beginning and end of a MAC frame. A received MAC frame is discarded if an error is detected in 'time stamp' field processing. The RP3-01 protocol shall not check the validity of the MAC frame check or CRC fields.

Table 33: Content of RP3-01 Ethernet message.

Field	Content
Address	Target address of next RP3-01 node
Type	Ethernet, 01010 in binary
Time Stamp	See Table 32.
Payload	Slice from Ethernet MAC frame.

In Ethernet transfer over RP3-01, a flexible implementation methodology should be applied, in order to prepare for possible changes in the future.

In order to transfer Ethernet MAC frames over RP3-01, an Ethernet MAC Address must be established for each RRU. The RRU may use either a globally or locally unique MAC address. For a locally unique MAC address, OBSAI System Specification [2] describes the methodology to derive a locally unique MAC address based on module hardware position. However, the IDs described in that section are not normally available at the RRU. These IDs can be communicated from the BTS to the RRU through an initialization MAC frame.

Each RRU has an RP3-01 slave port and optionally one or more RP3-01 master ports. At startup, the RRU shall disable transmission on all RP3-01 master ports. An RRU's RP3-01 slave port at startup shall respond to only an RP3 node address of zero and shall not have an initial locally unique MAC address. It shall listen for an initialization MAC frame using the Ethernet transmission protocol over RP3-01 that contains a broadcast MAC address for the destination address. This initialization message shall contain all the IDs described in OBSAI System Specification. The RRU shall then use these IDs as described in that section to derive its permanent locally unique MAC address. If using a locally unique MAC address, the RRU shall use this permanent MAC address for any further Ethernet transmissions. The RRU shall be configured with a permanent RP3 node address using RP1 over RP3-01 at which time it shall stop using the zero RP3 node address. After MAC address and RP3 node address configuration, an RRU may be instructed over RP1 to enable its master port(s) one at a time to allow

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initialization and network discovery of any other RRUs in the RP3-01 chain as shown in the example architectures of Figure 53.

6.2.5 Line Rate Auto-Negotiation

There exists a set of allowed RP3-01 line rates as defined in Section 6.2.1.2 and each LC or RRU can support one or several of these line rates. Before communication over an RP3-01 link can be initiated, a common line rate needs to be negotiated between adjacent RP3-01 nodes, with a 'node' being either an LC or an RRU. If the common line rate is known and pre-configured, a search for a common line rate is not required. Auto-negotiation of the line rate shall be applied when the used line rate is not defined beforehand.

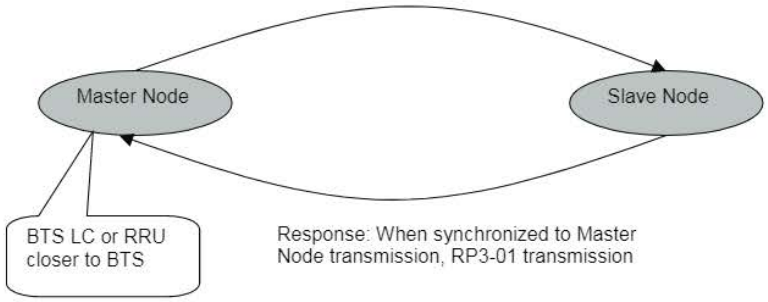


Figure 60: RP3-01 line rate auto-negotiation is done between a pair of nodes (LC and RRU or between adjacent RRUs).

Auto-negotiation of RP3-01 peer-to-peer links is considered in this section, as shown in Figure 60. For a chain, ring or tree-and-branch configuration of RRUs, the auto-negotiation algorithm is applied to each pair of RRUs at a time. The algorithm identifies a single line rate over each RP3-01 link, which is supported by both end nodes.

RP3-01 link synchronization is performed for a pair of RRUs. The Master node, which is the LC or RRU closest to the BTS, controls the auto-negotiation process.

The following assumptions are made:

- Master and slave nodes support all or a subset of allowed RP3-01 line rates.
- Allowed line rates include i*768 Mbps, where $i \in \{1, 2, 4, 8\}$, i.e. 768, 1536, 3072, and 6144 Mbps.

A set of parameters controls the operation of the algorithm and Application layer sets the value of these parameters. Table 34 lists the parameters of the auto-negotiation algorithm while Table 42 in Section 7.1.5 defines the parameters in detail. When setting parameter values for the RP3 receiver frame synchronization state machine (see Section

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4.2.8), the worst case RP3 frame synchronization time at the receiver shall not exceed TxTime.

Table 34: Parameters of line rate auto-negotiation algorithm.

Parameter	Description
MaxSynchronizationTime	Time limit for the line rate auto-negotiation algorithm.
MaxRxTime	Reception time at a given line rate.
TxTime	Transmission time at a given line rate.

Auto-negotiation algorithm for the Master node:

1. Set *Synchronization* = FALSE and start time out counter *TimeOutCounter*.
2. Select lowest RP3-01 line rate that is supported by the Master node
3. Attempt RP3-01 synchronization with the Slave node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) at the latest after TxTime.
    a. Start K28.5 transmission to the Slave Node and RP3 receiver synchronization state machine (refer to Section 4.2.8). In the case of 6144 Mbps line rate, start IDLE_REQ scrambling training pattern transmissions, and carry out IDLE_REQ/IDLE_ACK handshake process as defined in section 4.2.8.
    b. When Master's RP3 receiver state machine goes into state WAIT_FOR_K28.7_IDLES due to reception of K28.5 transmissions (completion of IDLE_REQ/IDLE_ACK scrambling handshake process for 6144 Mbps line rate) from the Slave node, start transmitting RP3 (RP3-01) frame format to the Slave node
    c. When Master's RP3 receiver state machine goes into state FRAME_SYNC, set *Synchronization* = TRUE (RP3-01 synchronization between Master and Slave nodes has been completed).
4. If *Synchronization* = FALSE and *TimeOutCounter* is less than MaxSynchronizationTime, change to next higher line rate (or go back to the lowest line rate if the highest line rate is being used) that is supported and goto Step 3.
5. End of Algorithm

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Auto-negotiation algorithm for the Slave node:

1. Set *RxSynchronization* = FALSE and start time out counter *TimeOutCounter*
2. Select lowest RP3-01 line rate that is supported by the Slave node
3. Attempt RP3-01 synchronization with the Master node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) latest after MaxRxTime
    a. Start RP3 receiver synchronization state machine (refer to Section 4.2.8 of RP3 Specification)
    b. When RP3 receiver synchronization state machine goes into state WAIT_FOR_K28.7_IDLES due to reception of K28.5 transmissions from the Master node, start K28.5 transmission back to Master Node. In the case of 6144 Mbps line rate, when the RP3 receiver synchronization state machine exits the UNSYNC state due to reception of IDLE_REQ pattern transmissions from the Master Node, start IDLE_REQ scrambling training pattern transmissions, and carry out IDLE_REQ/IDLE_ACK handshake process as defined in section 4.2.8.
    c. When RP3 receiver state machine goes into state FRAME_SYNC, start sending RP3 frame format to Master node and set *RxSynchronization* = TRUE.
4. If *RxSynchronization* = FALSE and *TimeOutCounter* is less than MaxSynchronizationTime, change to next higher line rate (or go back to the lowest line rate if the highest line rate is being used) that is supported and goto Step 3.
5. End of Algorithm

The Master node determines success or failure of the auto-negotiation procedure from the value of state parameter *Synchronization.* The Slave node is able to detect only the synchronization status of the downlink (from Master to Slave) RP3-01 link.

After RP3-01 link synchronization is achieved between the Master and the Slave, at some line rate common to both Master and Slave, RP1 Ethernet communication can be started over the interface and over other previously synchronized links. The Slave node can report the complete set of supported line rates using Ethernet messaging over the RP3-01 link.

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6.2.6 RTT Measurement and Internal Delays of a RRU

RRUs may be located far away from the BTS. In order to be able to configure the BTS, the propagation delay between the BTS and each RRU needs to be measured. In this section, Round Trip Time (RTT) measurement between a LU of a BTS and an RRU or between adjacent pairs of RRUs is defined. Internal delays of an RRU are also defined. Based on the knowledge of the RTT between adjacent RP3-01 nodes and the internal delays within the RRUs, the CCM can configure the BTS appropriately.

The reference point for the measurement shall be defined at the physical layer input / output electrical ports of the serial link (SerDes). These reference points shall apply to RRU internal delay measurements (Section 6.2.6.1) as well as to LU and RRU RTT measurements (Section 6.2.6.2).

Latency over an optical fiber is characterized by inaccuracy of the manufacturing process, temperature, strain, and dispersion. Local converter shall contain buffering and additional circuitry that shall be able to compensate dynamic delay variations over the fiber. This circuitry shall be located after receiver SerDes and before received master frame offset measurement.

Inaccuracy in the manufacturing process is a static parameter and does not require additional consideration in latency variation point of view.

Strain causes some delay change but its impact is difficult to estimate. During cable assembling, the target is to implement it without strain.

At maximum, 40km fiber lengths at maximum 100C temperature difference need to be supported in OBSAI. Temperature change causes latency variation of 0.0522 ps/m*C which stands for 2*40km*100C*0.0522 ps/m*C = 417 600 ps latency variation at maximum.

Dispersion depends on fiber, laser type, and wave length used. Maximum delay variation for Fiber-optic Backbone (FP)/1300 nm optical fiber equals to 6.4 ps/(nm*km) * 0.7 nm/K * 100K (temperature difference) * 80 km = 35840 ps. For Distributed FeedBack (DFB)/1550 nm fiber, delay variation is lower than that of Fiber Optic Backbone.

As a minimum, an OBSAI RP3 node at a Local Converter should be able to buffer delay variations of ± 453.44 ns which stands for ± 140 byte clock cycles at 307.2MHz byte clock rate. The requirement for an RP3 node is that it shall have a buffer of size 512 byte clock ticks to absorb delay variations.

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6.2.6.1 Internal Delays of an RRU

RRUs can be classified based on their support for different RP3-01 network topologies. A Class #1 RRU can only support point-to-point connection toward a BTS since they contain only a single RP3-01 transceiver while Class #2 RRUs can support chain and ring topologies due to dual RP3-01 transceiver support. Class #3 RRUs, having as a minimum three RP3-01 transceivers, can generate tree-and-branch topologies, i.e. it has a single RP3-01 transceiver, the RP3-01 slave port, toward the BTS and at least two RP3-01 transceivers, master ports, toward different RRUs.

Internal delays of Class #1, #2, and #3 RRUs are defined in Figure 61, Figure 62, and Figure 63, respectively. In a Class #3 RRU, all signal through-path propagation delays, in a given direction (transmit or receive) for a given RRU, are required to occupy the same number of RP3 byte clock cycles.

Each RRU shall report its internal delay values over the RP1 Ethernet connection which is available over RP3-01.

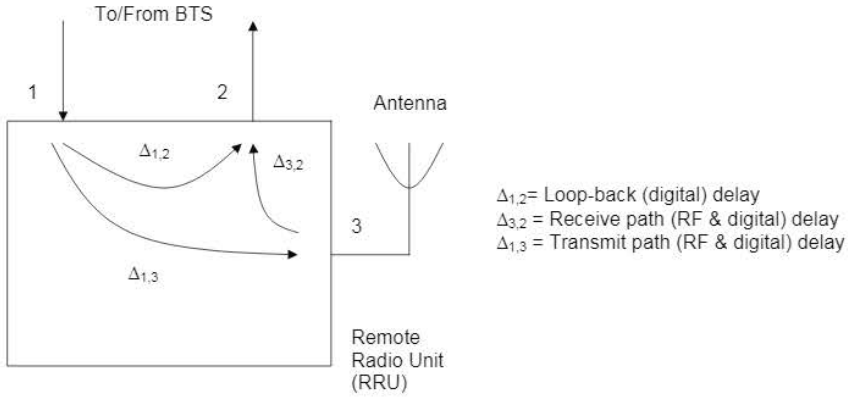


Figure 61: Internal delays of Class #1 RRU.

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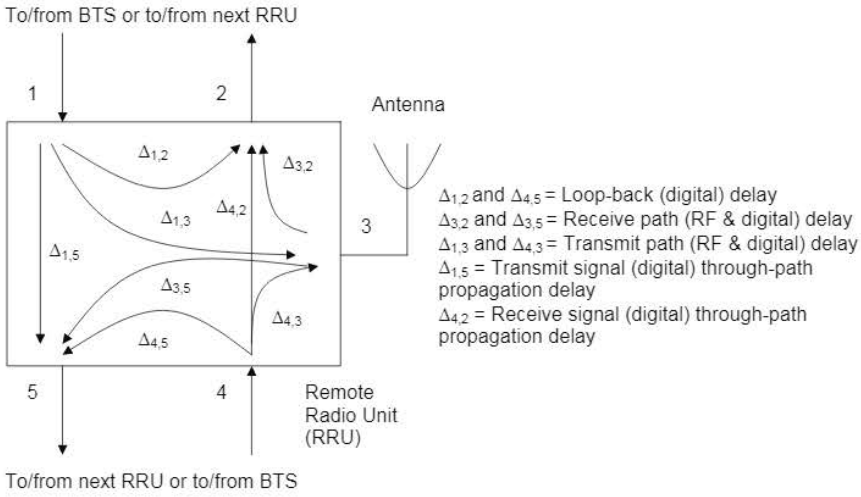


Figure 62: Internal delays of Class #2 RRU.

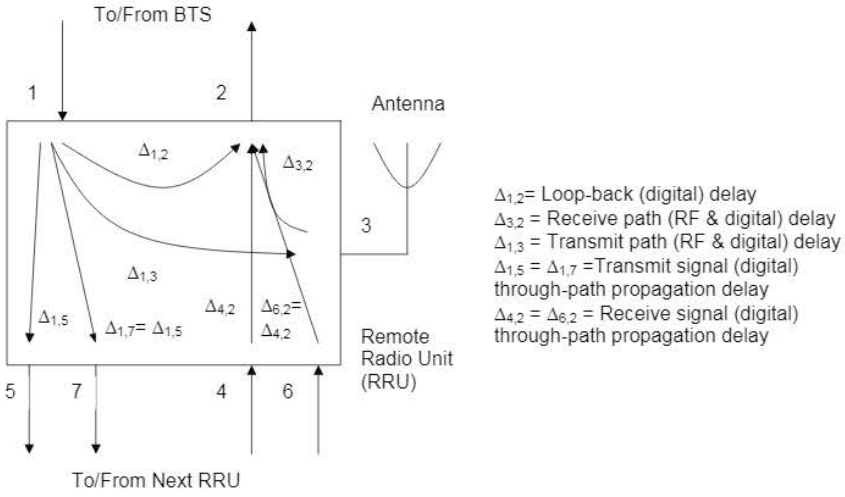


Figure 63: Internal delays of Class #3 RRU.

6.2.6.2 RTT Measurement Procedure

The RTT measurement procedure determines the two-way propagation delay over the media, e.g. fiber optics, between two adjacent RP3-01 nodes. In the case of chain, ring, or tree-and-branch topologies for the RRUs, RTT measurements are performed in a sequence for each adjacent pair of RP3-01 nodes.

The RTT measurement procedure is defined as follows: A Master RP3-01 node shall send the RTT measurement message defined in Figure 64 to a Slave RP3-01 node and measure the time *T* from message transmission to message reception. The Master node is either LC or

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RRU #n while the Slave node is RU #1 or RU #n+1, respectively, and *n>0.* The Slave node shall receive and send back the RTT measurement message to the Master node. Before transmission, the Slave node shall replace the address of the header by the return address of the payload and vice versa. Also buffering time $\Delta_{1,2}$ of the message at the Slave node will be stored into the message. Typically, the return address is equal to the RP3-01 node address of the Master node, so an 'address swap' procedure guarantees easy reception of the RTT message at the Master node.

All the time measurements are performed as a multiple of 1/(*8**76.8) MHz, i.e. 614.4MHz is the frequency of the reference clock.

Table 35 defines the content of different fields of the RTT message.

The MSB of each message field is transmitted first (refer to Figure 12).

Table 35: Content of an RTT Measurement message.

Field	Value
Address	Slave/Master RP3 node address (Slave address first, before address swap)
Type	01011 (RTT message)
Time stamp	000000
Return address, 13 first bits of the payload	Master/Slave RP3 node address (first Master address)
Reserved, 83 bits	All zeros
Buffering time $\Delta_{1,2}$, 16 bits	Positive integer number, buffering time will be measured using a reference clock at frequency (*8* *76.8)MHz.
CRC check, 16 bits	CRC check sum computed over the header and payload. Refer to Section 4.4.10.4 for the definition of the CRC.

The RTT between the Master and Slave nodes over fibre optics or other media is equal to $\Delta_{RTT} = T - \Delta_{1,2}$.

In the *ΔRTT* time calculation, the SERDES and PCS/Internal logic delays in both DL and UL paths shall be compensated in the measured *ΔRTT* and *Δ12* values.

In particular, at the LU (Local Unit) physical layer the internal logic / PCS / SERDES delays in both DL and UL paths between the reference measurement point as defined in Section 6.2.6 and the internal measurement point shall be removed from the measured ΔRTT value.

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At the RRU node physical layer, the internal logic / PCS / SERDES delays in both their DL and UL paths between the reference measurement point as defined in Section 6.2.6 and the internal measurement point shall be included in the measured *Δ12* value that will be reported into the RTT message reply.

The method described above accounts for situations in which the internal delays (internal logic/PCS/ SERDES) may not be approximated as symmetrical in their DL / UL components. In a RP3-01 optical link, the delay of O/E and E/O conversion and PCB differential traces may be accounted as propagation delay and included in the *ΔRTT* budget. This is an approximation assuming a fixed and symmetrical DL/UL delay contribution from the E/O and O/E conversion module and PCB traces provided they are having the same length.

The delay over the fibre is considered to be the same in downlink and uplink directions, i.e. one way delay over the fibre is equal to $\Delta_{RTT}/2$.



Figure 64: RTT Measurement message.

6.2.7 Multi-hop RTT

In a large RP3 network there can be several nodes connected to each other and the paths from baseband to last RF module can be several hops. In order to measure the delay over the whole network from one end (source) to another (target) at once, multi-hop RTT is defined as expansion to normal point-to-point RTT.

Multi-hop RTT is a measurement message that is routed through the RP3 network. Routing is based on the message header. The difference to a normal RTT message is that any node can initiate this measurement towards any node as the measurement request and response are separated with the time stamp. Table 36 defines the content of different fields of the multi-hop RTT message.

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Table 36: Content of an multi-hop RTT Measurement message.

Field	Value
Address	Target/Source RP3 node address (Target address first, before address swap)
Type	10000 (Multi-hop RTT message)
Time stamp	000000 (request), 000001 (response)
Return address, 13 first bits of the payload	Source/Target RP3 node address (first Source address)
Reserved, 67 bits	All zeros
Buffering time $\Delta_{1,2}$, 32 bits	Positive integer number, buffering time will be measured using a reference clock at frequency (*8* *76.8)MHz.
CRC check, 16 bits	CRC check sum computed over the header and payload. Refer to Section 4.4.10.4 for the definition of the CRC.

The target node of multi-hop RTT does not need to support more than one measurement simultaneously. If a collision occurs i.e. new measurement request arrive before the previous one is responded, the requesting party (source) needs to support time out. Time out counter shall support delays up to 32 bits operating at the nominal frequency of 614.4 MHz. The time out shall be programmed based on the need in the system configuration phase.

The target node of multi-hop RTT does not need to support more than one measurement simultaneously. When RTT target node is serving a RTT measurement, all new RTT measurement requests shall be rejected. Due to possible collisions, i.e. new measurement request arrive before the previous one is responded, the requesting party (source) need to support a time out mechanism. The time out counter shall support delays up to 32 bits operating at the nominal frequency of 614.4 MHz. The time out period shall be programmed based on the system topology during the system configuration phase. The time out period can be reduced for topologies with less hops. The maximum RTT message delay is expected to be in the region of 200us for a single hop or 51 ms for 255 hops (assuming each hop is 40km of fibre in each direction and the fibre delay is 5ns/m).

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6.2.8 Virtual HW Reset

A remote reset may need to be performed to a RRU in a case where the control processor of the RRU is halted. RRU may optionally support virtual HW reset functionality where the unit undergoes a boot sequence after receiving a specific virtual HW reset message. When receiving such a message, the following procedure shall be followed.

- CRC check is first performed. If the CRC check fails, the virtual HW message is rejected.
- The type field is checked. If it equals to 01101 (Virtual HW Reset), HW reset is performed for the RRU control processor.

Note that the virtual HW reset message may be received in either the data or control message slot. The virtual HW reset message is illustrated in Table 37 and Figure 65 below.

The MSB of each message field is transmitted first (refer to Figure 12).

Table 37: Content of virtual HW reset message.

Field	Value
Address	Address of the node that requires reset
Type	01101 (Virtual HW Reset)
Timestamp	000000
Payload data, 14 bytes	All zeros
CRC check, 16 bits	CRC check sum computed over the header and payload (see Section 4.4.10.4).



Figure 65: Virtual HW reset message.

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7 OAM&P

7.1 OAM&P Parameters

Operation of RP3 interface protocol is controlled through parameters. In this section, all parameters of the protocol are defined. Also error cases are considered.

7.1.1 External Parameters of Data Link Layer

In Table 38 external parameters of the Data link layer are listed. Application layer has access to all Data link layer parameters and input parameters are set by the Application layer.

Table 38: Input and output parameters of Data link layer.

Parameter	Input/ Output	Register width	Description
M_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of message slots in a Message Group (refer to Section 4.2.2 for details). 0< M_MG < 65536.
N_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of Message Groups in a Master Frame (refer to Section 4.2.2 for details). 0 < N_MG < 65536.
K_MG	Input	5 bits, positive number (no sign bit)	Specifies the number of IDLE bytes at the end of Message Group (refer to Section 4.2.2 for details). 0 < K_MG < 20.
DATA_MESSAGE_ SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in downlink direction. Takes values from 0 up to $i*(M\_MG-1)*N\_MG-1 < 2^{32}$ (refer to Section 4.2.2 for definition of *M_MG* and *N_MG*).

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Parameter	Input/ Output	Register width	Description
DATA_MESSAGE_ SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in uplink direction. Takes values from 0 up to $i*(M\_MG-1)*N\_MG-1 < 2^{32}$.
CONTROL_MESSAGE_ SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in downlink direction. Takes values from 0 up to *i*N_MG-1*.
CONTROL_MESSAGE_ SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in uplink direction. Takes values from 0 up to *i*N_MG-1*.
BLOCK_SIZE	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Defines the number of bytes within a block. (Reset value is 400)
SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid blocks of bytes which result in state WAIT_FOR_K28.7_IDLES. (Reset value is 255)
UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid blocks of bytes which result in state UNSYNC. (Reset value is 255)
FRAME_SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid Message Groups which result in state FRAME_SYNC. (Reset value is 1920)
FRAME_UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid Message Groups which result in state WAIT_FOR_K28.7_IDLES. (Reset value is 128)
TRANSMITTER_EN	Input	1 bit	For each transmitter separately. Value '1' enables transmission to the bus (if other conditions are also fulfilled) while value '0' disables transmission (see Section 4.2.8). (Reset value is '0').
LOS_ENABLE	Input	1 bit	For each transceiver separately. This parameter enables (value '1') or disables (value '0') the impact of signal LOS to transmitter state machine. See Section 4.2.8. (Reset value is '1')

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Parameter	Input/ Output	Register width	Description
DELTA (Δ)	Input	23 bits (16 bits allowed for ≤ 3072Mbps), two's complement code	In a general case, a common Δ value exists for all uplink bus transmitters of a node. Another common value exists typically for all downlink transmitters of a node. Link-specific Δ values are also allowed. Value of Δ is given in byte-clock ticks. When two byte accuracy is used for Δ, LSB of the register is ignored.
PI (Π)	Input	23 bits (16 bits allowed for ≤ 3072Mbps), two's complement code	In a general case, a common value exists for all uplink receivers of a bus node. A common value is typically used for all downlink receivers of a node. Receiver-specific Π values are also allowed. Value of Π is given in byte-clock ticks. When two byte accuracy is used for Π, LSB of the register is ignored.
MAX_OFFSET	Input	1 bit	Common value for a node. Defines the width of the allowed window for Master Frame boundary (see Section 4.2.6). MAX_OFFSET equals to 52.08 ns (the default value) for bit value '0' while MAX_OFFSET is equal to 104.17ns for '1'
SYNCHRONISATION_ STATUS	Output	4 bits	For each transceiver separately. Indicates the status of the transceiver (see Section 4.2.8). State encodings are the following. UNSYNC: 1000 WAIT_FOR_K28.7_ IDLES: 0100 WAIT_FOR_FRAME_ SYNC_T: 0010 FRAME_SYNC: 0001
SYNC_STATUS_CHANG E	Output	Interrupt	Application layer is interrupted always when a receiver state machine changes state.
Nx7	Input	5 bits	For each transmitter separately (applied only in case of 6144Mbps line rate). Specifies scrambler seed value (refer to Table 3). 0 ≤ Nx7 ≤ 17.

7.1.2 Error Cases at Data Link Layer

In Table 39, possible error cases at Data Link layer are defined.

In case of RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE, error recovery is left to Application layer.

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7.1.3 External Parameters of Transport Layer

In this section, parameters of the Transport layer are listed, see Table 40. Application layer has access to all parameters; input parameters are set by Application layer.

Table 39: Error cases at Data link layer.

Error	Register width	Description
RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE	1 bit	For each receiver port (transceiver) separately. This error is indicated when received Master Frame is detected outside the allowed MAX_OFFSET ns wide window (see Section 4.2.6). Value '0' indicates offset within the allowed range while '1' indicates out-of-range situation.

Table 40: Input and output parameters of Transport layer. All the parameters are defined for the whole node.

Parameter	Input/ Output	Register width	Description
RP3_ADDRESS	Input	13 bits	At least one address shall be supported per device based on which RP3 message reception is performed. The 8 bit wide node address shall be programmable while the 5 bit wide sub-node address may be hard-wired to the device. Note that in message transmission, Application layer may use several addresses when constructing and transmitting messages.
DL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that DL routing table is used to route messages that are received from the transceiver.
UL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that UL routing table is used to route messages that are received from the transceiver.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESS_DL	Input	4 bits	Specifies number of bits in a transformed address in downlink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESS_UL	Input	4 bits	Specifies number of bits in a transformed address in uplink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.

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Parameter	Input/ Output	Register width	Description
LSBs_MAPPING_OF_TRANSFORMED_ADDRESS_DL	Input	32 bits	Downlink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.
LSBs_MAPPING_OF_TRANSFORMED_ADDRESS_UL	Input	32 bits	Uplink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESS_DL	Input	20 bits	Downlink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESS_UL	Input	20 bits	Uplink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
DL_ROUTING_TABLE	Input	*A*T* bits	A table with *A* rows and *T* bits per row. *A* stands for $2^{DL\_TRANSFORMED\_ADDRESS\_RANGE}$, while *T* denotes total number of transceivers both at Application and Physical layers. The values of parameters *A* and *T* can be fixed and they take values in the range $0<A\leq 2^{13}$ and $0<T\leq 48$.
UL_ROUTING_TABLE	Input	*A'*T* bits	A table with *A'* rows and *T* bits per row. *A'* stands for $2^{UL\_TRANSFORMED\_ADDRESS\_RANGE}$, while *T* denotes total number of transceivers both at Application and Physical layers. The values of parameters *A'* and *T* can be fixed and they take values in the range $0<A'\leq 2^{13}$ and $0<T\leq 48$.

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Parameter	Input/ Output	Register width	Description
MULTIPLEXING_TABLE	Input	32 bits (4*8 bits)	For each multiplexer and demultiplexer separately. Vector containing four elements $E_{i_{out}} = (D, k, j_k)$. The first i elements of the vector are used for output (multiplexer)/input (demultiplexer) line rate i*768 Mbps. D exists in the MSB and values '0' and '1' are allowed, k field is three bits wide and may take values in the range of 0-7 (0x0-0x7 in hex), while j_k is located in the four least significant bits and it may take values in the range 0-15 (0x0-0xF in hex). See Section **Error! Reference source not found.** for the definition of $E_{i_{out}} = (D, k, j_k)$.
SUMMING_ALLOWED_FOR_TYPE	Input	32 bits	Value '1' in bit Index N indicates that messages of type N may be summed together. The least significant (rightmost) bit has Index 0 while MSB has Index 31. Refer to Table 12 for message type definitions and Section 4.3.4 for an example of SUMMING_ALLOWED_FOR_ TYPE parameter.

7.1.4 Error Cases at Transport Layer

In Table 41: Possible error cases at Transport layer. the possible error cases at the Transport layer are defined. Refer to RP3 compatible chip (ASIC) functional specifications for detailed descriptions on these error indicators.

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Table 41: Possible error cases at Transport layer.

Error	Register width	Description
DL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. There exists no output port corresponding to the address of the received message (all-zero bit vector exists for the address in the routing table (see Table 10)).
UL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specification. Operation is the same than in case of DL_ MESSAGE_REJECTED above. UL_MESSAGE_ REJECTED applies for UL direction.
MESSAGE_COLLISION	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. Refer to Section 4.3.4 for a definition of message collision.

7.1.5 Other External Parameters

In this section, parameters that may be applied at any protocol layer are listed, see Table 42: Other input and output parameters of bus node. Thus, the functionality corresponding to the parameters can be implemented at any protocol layer.

Physical layer shall be able to detect and report line code violations (see Section 4.1.2).

For each receiver port (link) separately, Loss Of Signal (LOS) defect reporting shall be supported. If N_LCV or more line code violations occur during period T_LCV, a LOS defect shall be reported. The LOS defect shall be removed when no LCVs occur in period T_LCV. LOS defect functionality can be implemented at any layer of the protocol stack.

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Table 42: Other input and output parameters of bus node.

Parameter	Input/ Output	Register width	Description
N_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Threshold value for Line Code Violation (LCV) defect reporting (see algorithm below). Reset value is 1.
T_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Parameter defining period for LCV defect monitoring. T_LCV specifies the period in number of received 8b10b line codes. Reset value is *N_MG*(M_MG*19+ K_MG)*..
LOS_DEFECT	Output	1 bit	For each receiver port separately. Value '1' indicates Loss Of Signal (LOS) while value '0' denotes normal operation (reset value)
MESSAGE_TX_RULE	Input	33 bits	There may exist several message transmission rules per a bus node. The MSB defines the message slot counter that is used in message transmission. '0' stands for data message slot counter while '1' refers to control slot counter. The following 16 bits contain the index *I* and the 16 least significant bits contain the modulo *M* (refer to Section 4.4.4 for the definition of *I* and *M*).
MAX_SYNCHRONIZATION_TIME	Input	32 bits, positive number	Common value for a node. Time limit for the line rate auto-negotiation algorithm (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 153600000 (5 seconds).
MAX_RX_TIME	Input	32 bits, positive number	Common value for a node. Reception time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 19660800 (0.64 seconds).
TX_TIME	Input	32 bits, positive number	Common value for a node. Transmission time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 6144000 (200 ms).

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Appendix A: Media Adapters and Media Options

Media adapters and media options for OBSAI RP3-01 interface are listed in this section. Phase distortion and latency are examples of important parameters that are associated with RP3-01 interface. These parameters are to be considered at base station system level and they are therefore out of the scope of RP3 specification.

A1: Fiber Optics

Table 43 lists the media options that shall be used.

Table 43: Options for optical cabling.

Type	Related Standard
50 μm Multimode	IEC 60793-2-10:2002, Type A1a [7]
62.5 μm Multimode	IEC 60793-2-10:2002, Type A1b [7]
Singlemode	IEC 60793-2-50:2002, Type B1 [8]

Table 44 proposes optical transceiver candidates for each line rate. OBSAI recommends to apply the Fibre channel or 10 Gbit Ethernet interface requirements to RP3-01.

Table 44: Optical interface recommendations for different RP3-01 line rates. This table is for information only.

Line Rate	50 μm Multimode Fiber	62.5 μm Multimode Fiber	Singlemode Fiber
768 Mbps	100-M5-SN-I in [9]	100-M6-SN-I in [9]	100-SM-LC-L in [9]
1536 Mbps	200-M5-SN-I in [9]	200-M6-SN-I in [9]	200-SM-LC-L in [9]
3072 Mbps	400-M5-SN-I in [9]	400-M6-SN-I in [9]	400-SM-LC-L in [9]
6144 Mbps	800-M5(E)-SN-I in [12]	800-M6(E)-SN-I in [12]	800-SM-LC-L in 12] 10GBASE-E in [19]

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OBSAI mandates the use of SFP (Small Form-factor Pluggable) transceivers for line rates up to 3072 Mbps and SFP+ [13] for 6144 Mbps line rate. Connector type is not recommended but the ORL (Optical Return Loss) of the used connector should fulfil PC (Physical Contact) requirement ORL<-30 dB for singlemode and TIA/EIA 568 requirement (ORL<-20 dB) for multimode applications. Super PC (ORL<-40 dB) is recommended for complex installations especially at 1550 nm wavelength.

A2: Other Media

Other technologies like wireless transmission or copper cable can be used as transport media. The requirements for the transmission parameters as specified in the OBSAI specifications shall be met.

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Appendix B: Multiplexing Examples (Informative)

Figure 66 provides an example of a Transport layer configuration. The message router and summing unit are defined here to operate at the lowest RP3 line rate used in the system. Demultiplexers are used to split high data rate RP3 links into several low rate links which may then be multiplexed back to high rate links after summing. RP3 line rates are configured or identified at BTS startup so multiplexer and demultiplexer blocks as well as router and summing blocks can be configured accordingly. For detailed information on message multiplexer, demultiplexer, and router operations, refer to Section 4.2.10.

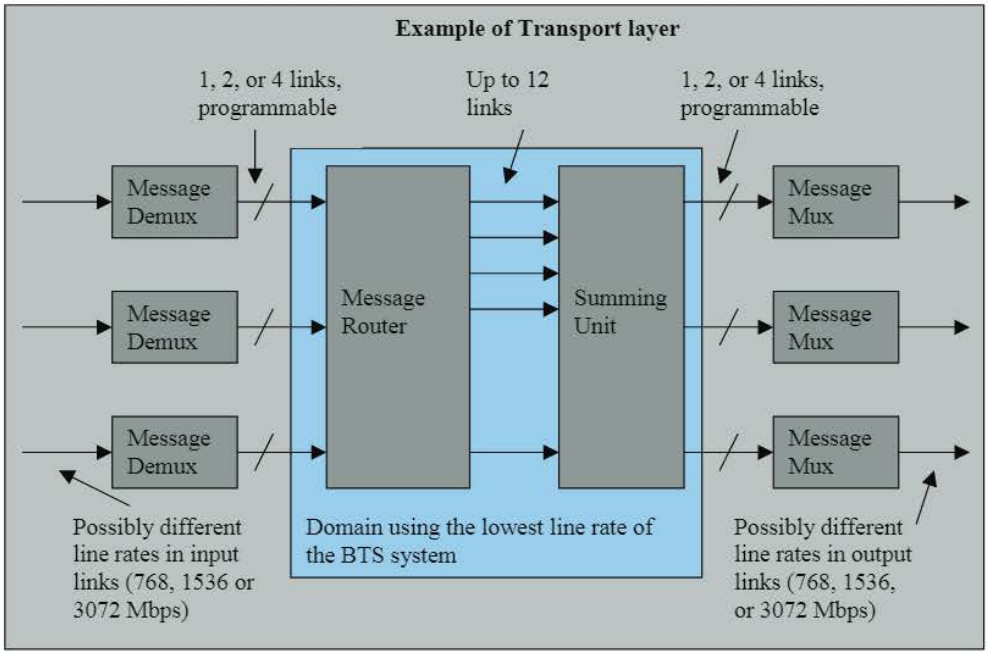


Figure 66: Example block diagram of Transport layer.

Figure 67 illustrates message multiplexing from four 50% full RP3 links into one 1536 Mbps. The concept presented in Figure 66 has been applied for this and other examples presented in this section.

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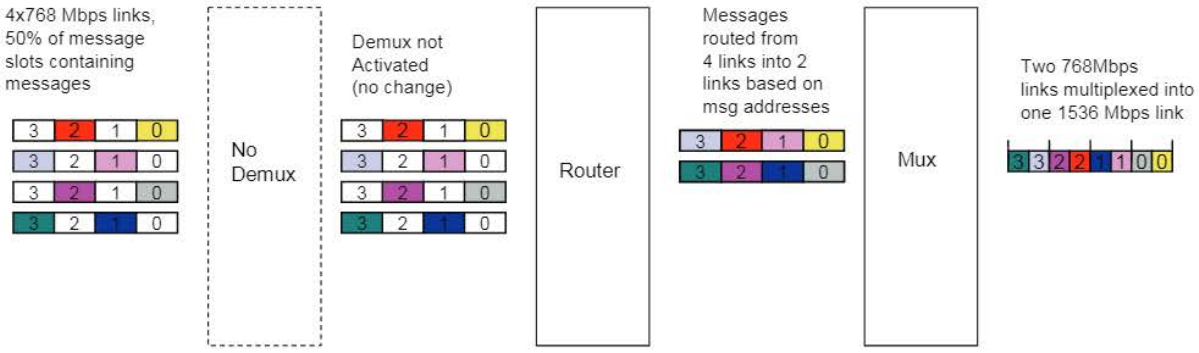


Figure 67: An example of message multiplexing from four 768 Mbps links into one 1536 Mbps link.

Figure 68 illustrates message interleaving from a single 768 Mbps RP3 link into a 3072 Mbps link. Such a case may be valid in the uplink direction when data from an RRU is interleaved to RP3-01 in a chain topology.

Illustrates e.g. data interleaving at an RRU to a chained fiber in UL direction

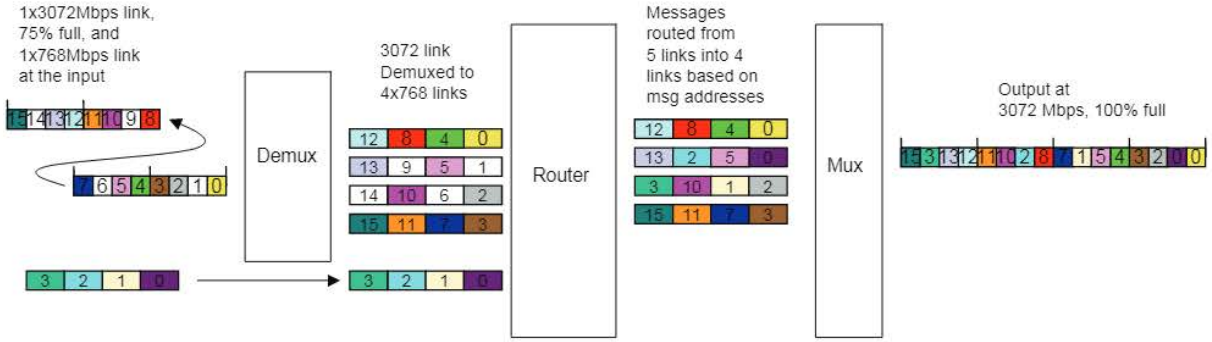


Figure 68: An example of message interleaving from one 768 Mbps link into one 3072 Mbps link.

Figure 69 and Figure 70 illustrate RP3 multiplexing in a possible BTS configuration where uplink data from several low capacity RRUs is forwarded to base band for processing. The configuration shown reduces the number of RP3 links at the base band modules.

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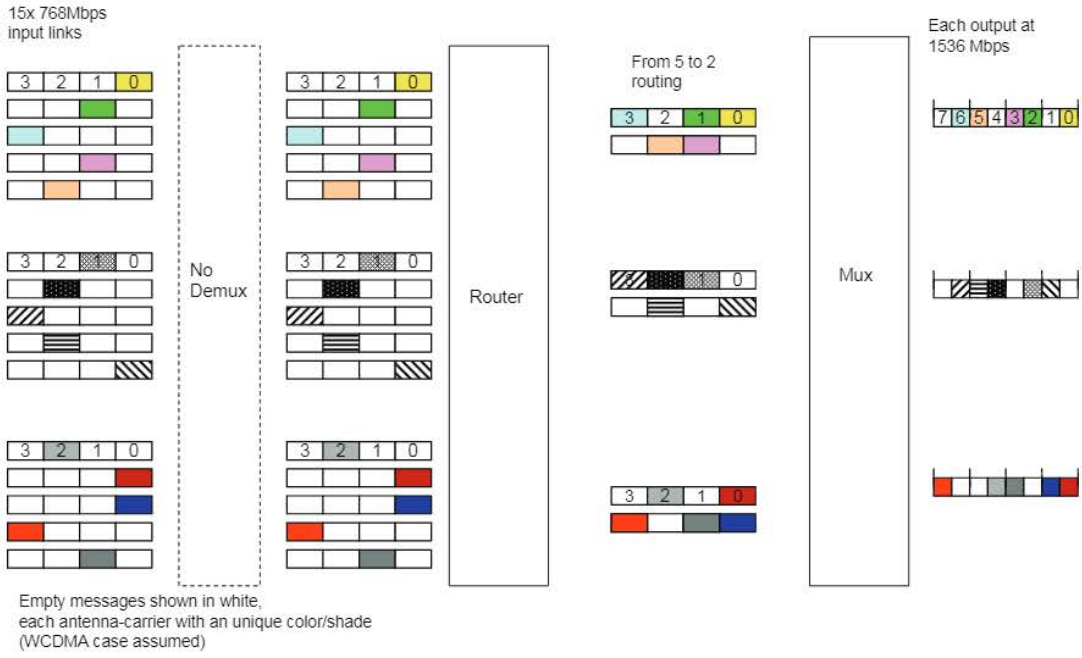


Figure 69: An example of message interleaving from fifteen 768 Mbps links into three 1536 Mbps link.

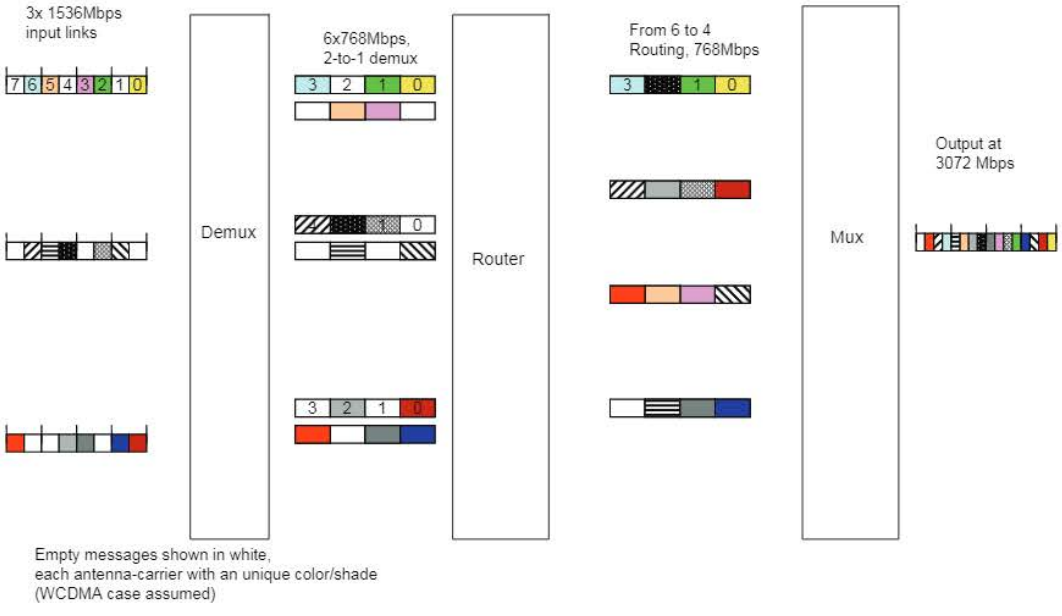


Figure 70: An example of message interleaving from three partly full 1536 Mbps links into one 3072 Mbps link.

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Appendix C: RP3 Bus Configuration Algorithm (Informative)

An example of the RP3 bus configuration is provided in this section for the base station configuration illustrated in Figure 71. We use a two sector WCDMA base station with a single TX antenna and two RX antennas per sector. There are two carriers per each antenna so a 2+2 configuration is illustrated. As can be seen from the figure, a base-station architecture with combiner and distributor is used but the configuration principles apply also to the mesh architecture. In this example, we split the 13 bit RP3 address into an 8 bit node address (MSBs) and a 5 bit sub-node address, where the node address identifies a module and the sub-node address specifies the antenna-carrier. RP3 links with a 768Mbps baud rate are assumed.

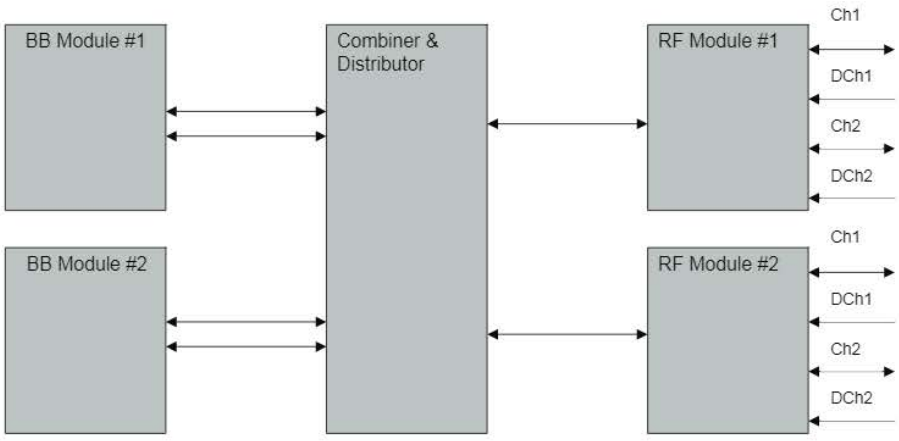


Figure 71: An example base station configuration.

Figure 72 illustrates data flows between the RF and BB modules. Each antenna-carrier is drawn separately to the figure and mapping of the antenna carriers to RP3 links is provided. Also node and sub-node addresses for different modules and antenna-carriers are provided. In this example, node addresses 1 and 2 have been allocated to BB

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modules while node addresses 16 and 32 (in decimal numbers) are applied to RF modules. Antennas-carriers in each RF module are numbered from 1 to 4.

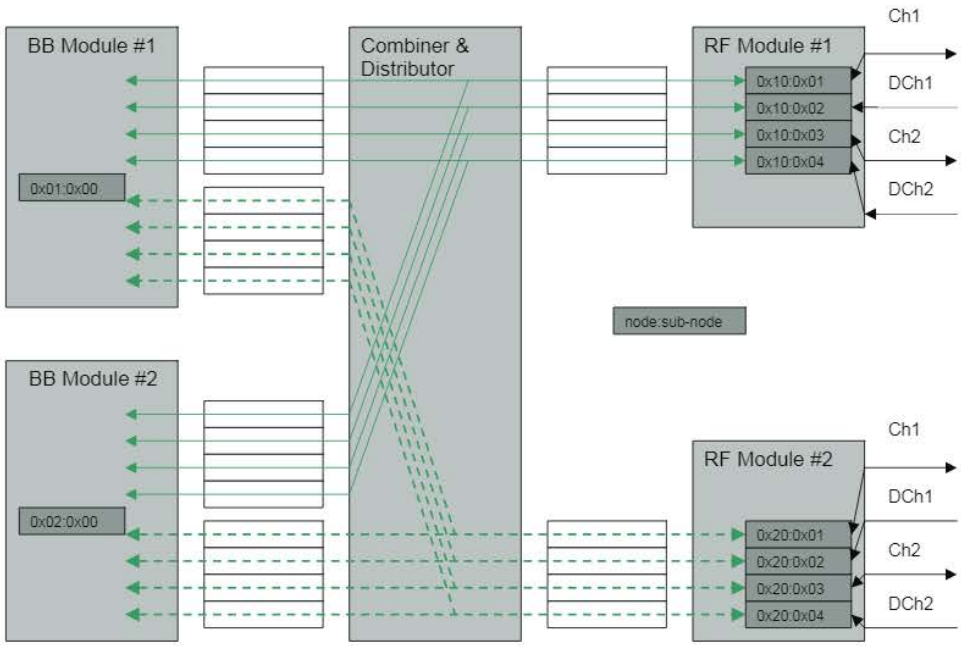


Figure 72: Data flows between BB and RF modules. Addresses of modules and antenna-carriers (or up/down converters at RF) are also shown.

Parameters for the message routing, multiplexing, and demultiplexing blocks of the combiner and distributor must be provided at base station start up. In this example, multiplexing and demultiplexing blocks are not used. Message routing tables are applied to the message routing between BB and RF modules. The routing tables define the output port or ports that correspond to each address. In the downlink direction, a point-to-point message transfer is typically applied so there exists a single output port index for each address in the downlink routing table. In uplink direction, the same message may be multicast to several BB modules for processing and because of this several output ports exist corresponding to an address in the uplink routing table.

In Figure 73, the port indices of the combiner distributor are shown, while downlink and uplink routing tables are provided in Table 45 and Table 46, respectively. In this example, we assume that the combiner distributor performs message routing based on the node address only.

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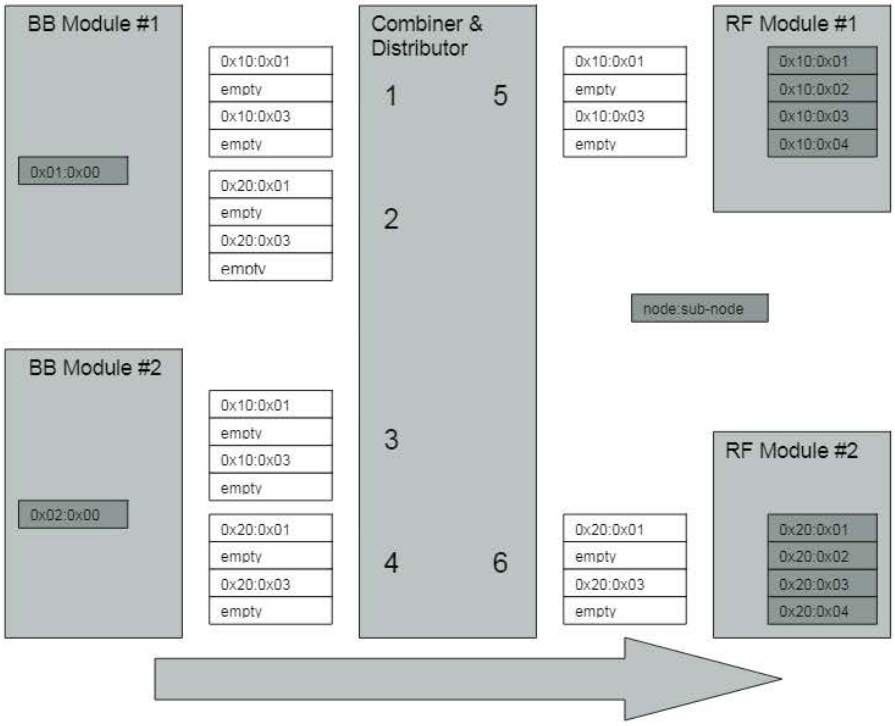


Figure 73: Index assignment to the ports of combiner distributor. Mapping of downlink messages to RP3 message slots is also shown.

Table 45: Downlink routing table.

Address Field (Target Address)	Output Port
0x10	5
0x20	6

Table 46: Uplink routing table.

Address Field (Source Address)	Output Ports
0x10	1, 3
0x20	2, 4

In addition to address assignment and the definition of routing tables, message transmission rules must also be defined in the BB and RF modules that form the end nodes of the bus. Table 47, Table 48, and Table 49 define the message transmission rules applied by the BB

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modules, RF module #1, and RF module #2, respectively. Figure 73 shows also how messages are mapped into the message slots of the RP3 links in the downlink direction, while Figure 74 illustrates the uplink case.

Table 47: Message transmission rules for BB modules #1 and #2.

Target	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x03	Link 1, 2 / 4
0x20: 0x01	Link 2, 0 / 4
0x20: 0x03	Link 2, 2 / 4

Table 48: Message transmission rules for RF module #1.

Source	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x02	Link 1, 1 / 4
0x10: 0x03	Link 1, 2 / 4
0x10: 0x04	Link 1, 3 / 4

Table 49: Message transmission rules for RF module #2.

Source	Link, Index/ modulo
0x20: 0x01	Link 1, 0 / 4
0x20: 0x02	Link 1, 1 / 4
0x20: 0x03	Link 1, 2 / 4
0x20: 0x04	Link 1, 3 / 4

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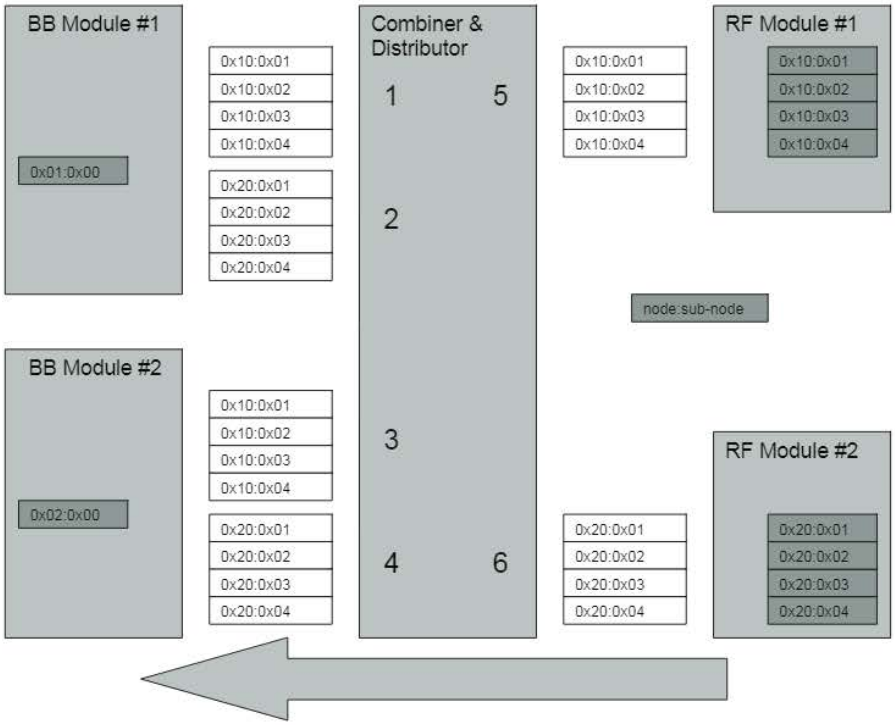


Figure 74: Mapping of uplink messages to RP3 message slots.

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Appendix D: Parameters for 802.16 Message Transmission

The parameters required for 802.16 data message transmission are provided in Table 50 for the currently supported 802.16 profiles, i.e.

Table 50: Parameters for supported 802.16 profiles in case of 768 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	10	1	0x5	3	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
2.5	144/125	2.88	5	1	0x2	3	0x0	0
3	86/75	3.44	4	1	0x2AA95552AAA	43	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	144/125	5.76	2	1	0x5	3	0x0	0
5.5	316/275	6.32	2	1	0x2A54A952A54A952A54AA	79	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
10	144/125	11.52	1	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	10	1	0x7FFFFFFD	35	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	28/25	5.6	2	1	0x6EEEEEED	35	0x0	0
5.5	28/25	6.16	2	1	0x0AAAAAAAAAAAAAAAAAAA	77	0x0	0
6	28/25	6.72	2	1	0x12	7	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
8.75	8/7	10	1	2	0xAAAD555AAAD555	56	0x1555	13
10	28/25	11.2	1	1	0x24A4A4A4A	35	0x0	0
14	8/7	16	0	0	0xFALSE	0	0x0	0
17.5	8/7	20	0	0	0xFALSE	0	0x0	0
20	28/25	22.4	0	0	0xFALSE	0	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	3	2	0x00040010004002	56	0x0002	13

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sampling rates (channel bandwidths) and OFDM/OFDMA multiple access methods. For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

Table 51: Parameters for supported 802.16 profiles in case of 1536 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	21	1	0x2	3	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
2.5	144/125	2.88	10	1	0x5	3	0x0	0
3	86/75	3.44	8	1	0x7FFDFFF7FFD	43	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	144/125	5.76	5	1	0x2	3	0x0	0
5.5	316/275	6.32	4	1	0x7EFDFBF7EFEFDFBF7EFD	79	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
10	144/125	11.52	2	1	0x5	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	21	1	0x7FFFBFFFD	35	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	28/25	5.6	5	1	0x2AAAAAAAA	35	0x0	0
5.5	28/25	6.16	4	1	0x1FFFFFFFFFFFFFFFFFFD	77	0x0	0
6	28/25	6.72	4	1	0x55	7	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
8.75	8/7	10	3	2	0x00040010004002	56	0x0002	13
10	28/25	11.2	2	1	0x6EEEEEED	35	0x0	0
14	8/7	16	1	1	0x1FFDFFD	25	0x0	0
17.5	8/7	20	1	2	0xAAAD555AAAD555	56	0x1555	13
20	28/25	22.4	1	1	0x24A4A4A4A	35	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	6	1	0x00408102040810204082	77	0x040810204082	48

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Table 52: Parameters for supported 802.16 profiles in case of 3072 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	42[1]	1	0x5	3	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
2.5	144/125	2.88	21	1	0x2	3	0x0	0
3	86/75	3.44	17	1	0x7EFDFBF7EFD	43	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	144/125	5.76	10	1	0x5	3	0x0	0
5.5	316/275	6.32	9	1	0x6EDDBBB76EEDDBBB76ED	79	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
10	144/125	11.52	5	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	43[1]	1	0x7F7FBFDFD	35	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	28/25	5.6	10	1	0x7FFFFFFFD	35	0x0	0
5.5	28/25	6.16	9	1	0x1FFFFFFFFF7FFFFFFFFD	77	0x0	0
6	28/25	6.72	9	1	0x02	7	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
8.75	8/7	10	6	1	0x00408102040810204082	77	0x040810204082	48
10	28/25	11.2	5	1	0x2AAAAAAAA	35	0x0	0
14	8/7	16	3	1	0x1F7DF7D	25	0x0	0
17.5	8/7	20	3	2	0x00040010004002	56	0x0002	13
20	28/25	22.4	2	1	0x6EEEEEEED	35	0x0	0
28	8/7	32	1	1	0x1FFDFFD	25	0x0	0
4.375	8/7	5	12	2	0x122448912244892	59	0x12	7

[1] RP3 sub-node address range limits the number of antenna-carriers per node to 32. The supported antenna-carrier range can be extended by using several node addresses for one physical node.

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Table 53: Parameters for supported 802.16 profiles in case of 6144 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	85	1	0x2	3	0x0	0
1.75	8/7	2	61	1	0x12A5A9	25	0x0	0
2.5	144/125	2.88	42	1	0x5	3	0x0	0
3	86/75	3.44	35	1	0x6EDDBB76EDB	43	0x0	0
3.5	8/7	4	30	1	0x1D76DDB	25	0x0	0
5	144/125	5.76	21	1	0x2	3	0x0	0
5.5	316/275	6.32	19	1	0x49554955495549554955	79	0x0	0
7	8/7	8	15	1	0x1249249	25	0x0	0
10	144/125	11.52	10	1	0x5	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	87	1	0x777777777	35	0x0	0
1.75	8/7	2	61	1	0x154AA54	25	0x0	0
3.5	8/7	4	30	1	0x1DB6DB7	25	0x0	0
5	28/25	5.6	21	1	0x7FF7FF7FF	35	0x0	0
5.5	28/25	6.16	19	1	0x1FFFFBFFFF7FFFEFFFFD	77	0x0	0
6	28/25	6.72	18	1	0x44	7	0x0	0
7	8/7	8	15	1	0x1494948	25	0x0	0
8.75	8/7	10	12	1	0x89122448912244	56	0x1224	13
10	28/25	11.2	10	1	0x7FFFDFFFF	35	0x0	0
14	8/7	16	7	1	0x1B6DDB6	25	0x0	0
17.5	8/7	20	6	1	0x81020408102040	56	0x1020	13
20	28/25	22.4	5	1	0x55554AAAA	35	0x0	0
28	8/7	32	3	1	0x1F7DF7D	25	0x0	0
4.375	8/7	5	24	1	0xADAAB6AADAAB6A	56	0x1AD5	13

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Appendix E: Background Information on Interconnects (Informative)

TYPE 1 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplane and cable while TYPE 2 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplanes. Figure 75 illustrates TYPE 1 and TYPE 2 interconnects.

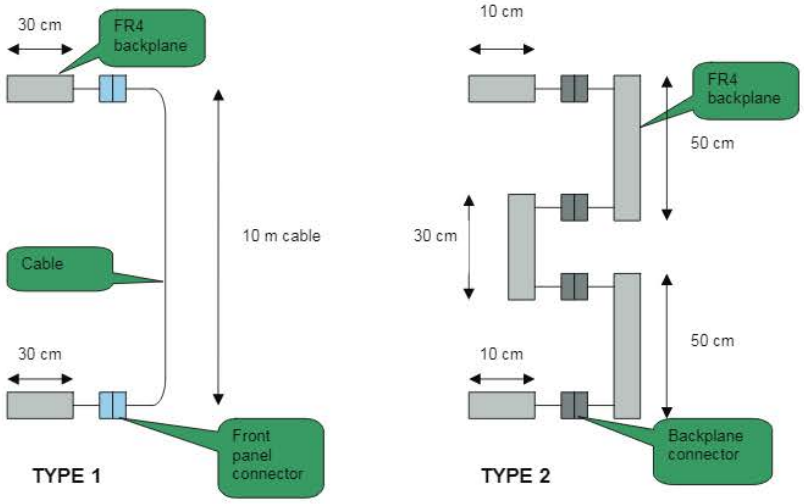


Figure 75: TYPE 1 and TYPE 2 Interconnects.

TYPE 3 Channel is defined as a serial interconnect at 768, 1536, or 3072MBaud data rate across backplane (PCB) made of commonly used FR4 materials or cable.

TYPE 4 and TYPE 5 Channels are defined as serial interconnect at 6144MBaud data rate across backplane or cable.

The backplane channels are defined as entirely passive links consists of two line cards interconnect across backplane through two backplane connectors as depicted in Figure 76 and meet the limitations as indicated in Table 54.

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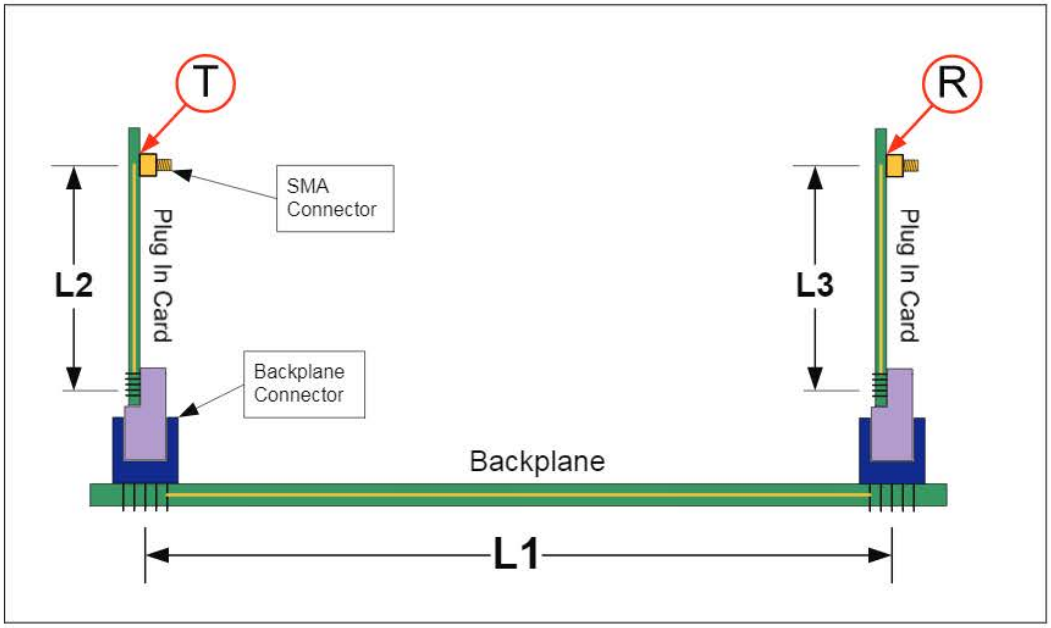


Figure 76: TYPE-3 Backplane Interconnect

Table 54: TYPE 3, 4, and 5 rear interconnect length specifications as indicated in Figure 76.

	Backplane Connector	L1 (Max.)	L2 (Max.)	L3 (Max.)
Type-3	OBSAI system Ref. Appendix B & C (HM 2mm 6 Row) Male & Female	800mm (31.5")	100mm (4")	100mm (4")
Type-4	High Speed / Controlled Impedance of any type	L1 + L2 + L3 ≤ 600mm (23.6")		
Type-5	High Speed / Controlled Impedance of any type	L1 + L2 + L3 ≤ 1000mm (39.4")		

Notes:

Connectors are excluded from the lengths calculation.

No more than two backplane connectors between point 'T' and 'R'

6 PTH's across the channel from 'T' to 'R' points

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The cable channel is defined as entirely passive link consists of two line cards interconnect across cable assembly terminated with front access connectors as depicted in Figure 77 and meet the following limitations.

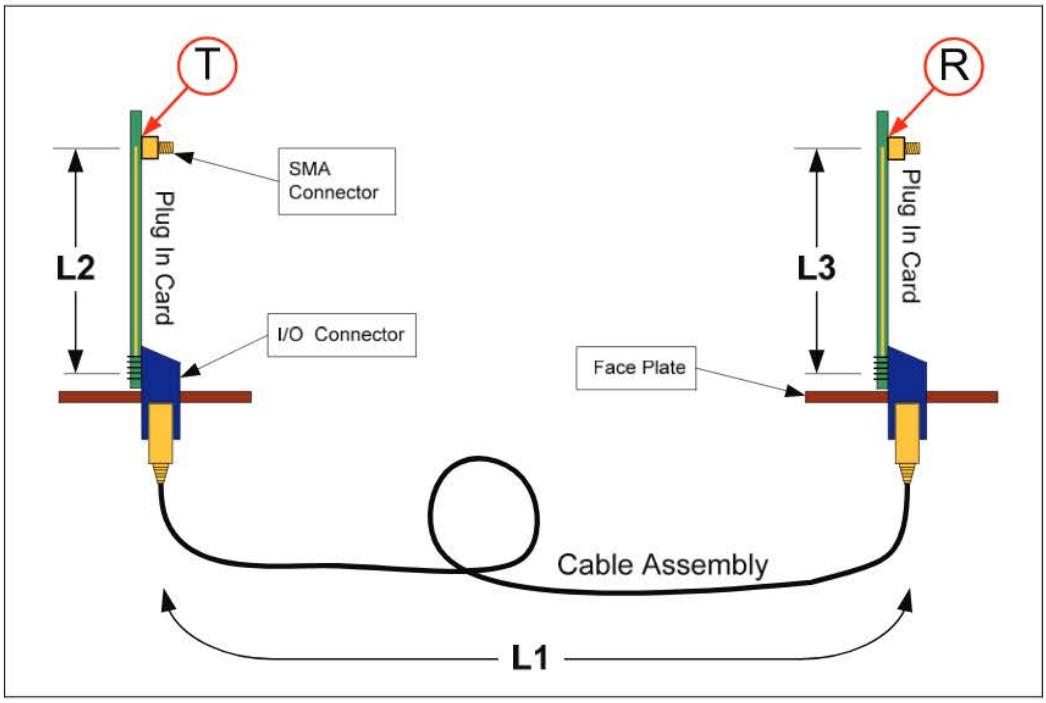


Figure 77: TYPE-3 Cable Interconnect

Table 55: TYPE 3, 4, and 5 front interconnect lengths specifications as indicated inFigure 77.

	Cable I/O Connector	L1 (Max.)	L2 (Max.)	L3 (Max.)
Type-3	OBSAI System Ref. Appendix F (Slim-I/O) Panel Mount Cable To Board	3000mm (9ft)	50mm (2")	50mm (2")
Type-4	High Speed / Controlled Impedance of any type	L1 + L2 + L3 ≤ TBD mm (TBD")		
Type-5	High Speed / Controlled Impedance of any type	L1 + L2 + L3 ≤ TBD mm (TBD")		

Notes:

No more than 4 PTH's across the channel from 'T' to 'R' points

PCB materials is made of commonly used standard FR4

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Cable diameter and conductors AWG shall be determined based on the requirements (refer to [11])

Insertion loss to Crosstalk Ratio

The ICR (Insertion loss to crosstalk ratio) is one of the informative channel parameters defined in the Annex 69B of the IEEE802.3ap for 1000BASE-KX @1.25GBd, 10GBASE-KX4 @3.125 GBd and 10GBASE-KR @10.3125GBd lane rates [17].

The ICR is recommended for informative analysis of the S-Parameter results..

Informative channel parameters in [17]:

- Fitted attenuation
- Insertion loss
- Insertion loss deviation
- Return loss
- Crosstalk
- Power sum differential near-end crosstalk (PSNEXT)
- Power sum differential far-end crosstalk (PSFEXT)
- Power sum differential crosstalk (PSXT)
- Insertion loss to crosstalk ratio (ICR)

Insertion loss to crosstalk ratio (*ICR*) is the ratio of the insertion loss, measured from TP1 to TP4 (T and R as defined in Appendix E of RP3 specification respectively), to the total crosstalk measured at TP4. *ICR* may be computed from *IL* and *PSXT* as shown in the following Equation:

$$ICR(f) = -IL(f) + PSXT(f)$$

The Type 4 and 5 interconnects should meet the limits of Type 10GBASE-KR. Detailed information and Equations for the analysis are available in [17].

$$ICR_{\min}(f) = 23.3 - 18.7\log_{10}\left(\frac{f}{5GHz}\right); \qquad \text{for } 100\text{MHz} \le \text{f} \le 5.15625\text{GHz}$$

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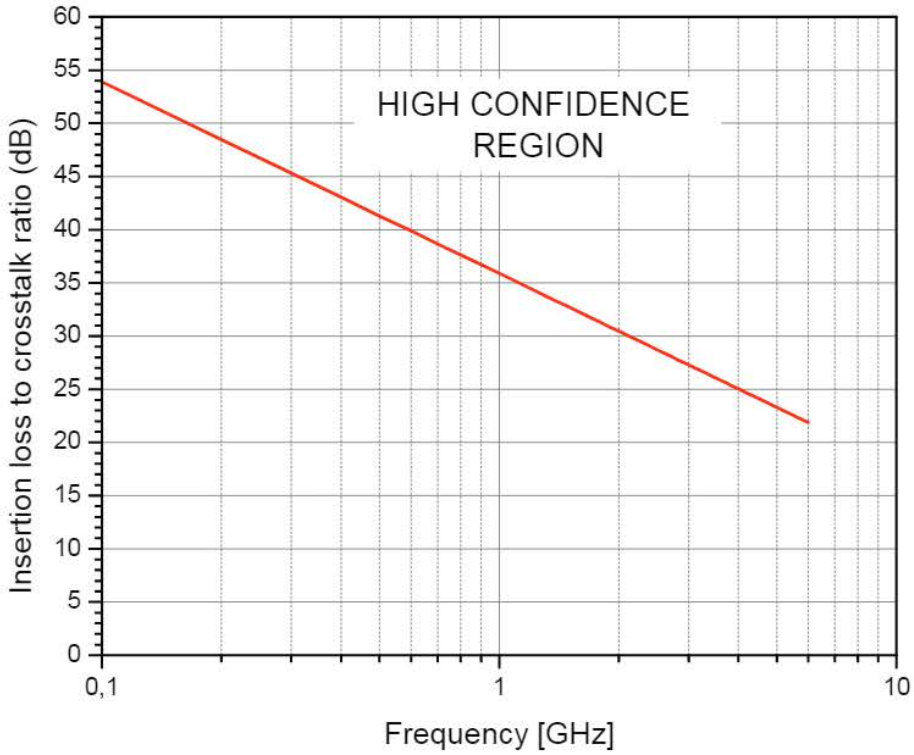


Figure 78: Insertion loss to crosstalk ratio limit

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Appendix F: Parameters for LTE Message Transmission

The parameters required for LTE data message transmission are provided in Table 56-Table 59 for the currently defined LTE profiles, i.e. sampling rates (channel bandwidths). For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters. Dual bit map rules are applicable only for the 15MHz channel bandwidth. For other channel bandwidths, antenna-carrier streams consume completely the bandwidth provided by the modulo transmission rules.

Table 56: Parameters for supported LTE profiles in case of 768 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	8	8	1	0x0	0	0x0	0
3.0	3.84	4	4	1	0x0	0	0x0	0
5	7.68	2	2	1	0x0	0	0x0	0
10	15.36	1	1	1	0x0	0	0x0	0
15	23.04	-	0	0	0xFALSE	0	0x0	0
20	30.72	-	0	0	0xFALSE	0	0x0	0

Table 57: Parameters for supported LTE profiles in case of 1536 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	16	16	1	0x0	0	0x0	0
3.0	3.84	8	8	1	0x0	0	0x0	0
5	7.68	4	4	1	0x0	0	0x0	0
10	15.36	2	2	1	0x0	0	0x0	0
15	23.04	1	1	1	0x1	3	0x0	0
20	30.72	1	1	1	0x0	0	0x0	0

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Table 58: Parameters for supported LTE profiles in case of 3072 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	32	32	1	0x0	0	0x0	0
3.0	3.84	16	16	1	0x0	0	0x0	0
5	7.68	8	8	1	0x0	0	0x0	0
10	15.36	4	4	1	0x0	0	0x0	0
15	23.04	1	2	1	0x3	3	0x0	0
20	30.72	2	2	1	0x0	0	0x0	0

Table 59: Parameters for supported LTE profiles in case of 6144 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	64	64	1	0x0	0	0x0	0
3.0	3.84	32	32	1	0x0	0	0x0	0
5	7.68	16	16	1	0x0	0	0x0	0
10	15.36	8	8	1	0x0	0	0x0	0
15	23.04	1	5	1	0x2	3	0x0	0
20	30.72	4	4	1	0x0	0	0x0	0

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Appendix G: Parameters for GSM/EDGE/EGPRS2 Message Transmission

G1: Uplink Transmission

The recommended parameters for GSM/EDGE/EGPRS2 uplink data message transmission are provided in Table 60-Table 63. For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

GSM/EDGE/EGPRS2 uplink data can also be transmitted using only low level modulo rules.

Table 60: Parameters for UL GSM/EDGE/EGPRS2 in case of 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	4	7	136	0	1	1	1
325.000	32	4	5	1	7BEFBDF7DF7BEFBD	63	F7DF7BEFBD	40
270.833	32	2	14	2	0000000000000002	68	0	1
325.000	32	2	11	1	5B6DB5B6DB5B6DB5	63	B6DB5B6DB5	40
270.833	32	1	28	2	0000000400000002	68	0	1
325.000	32	1	23	1	0491244912449124492	73	09124492	30

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Table 61: Parameters for UL GSM/EDGE/EGPRS2 in case of 1536 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	56	2	00008000400020002	68	0	1
325.000	32	1	46	1	2D6B5AD6B5AD6B5AD6B5	78	15AD6B5	25

Table 62: Parameters for UL GSM/EDGE/EGPRS2 in case of 3072 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	112	2	010080804040202	60	00202	17
325.000	32	1	93	2	0210842108422	49	02	5

Table 63: Parameters for UL GSM/EDGE/EGPRS2 in case of 6144 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	224	2	111088844442222	60	02222	17
325.000	32	1	188	2	2AA95552AAA5554AAAA	75	0AAA	13

G2: Downlink Transmission

Only modulo rules are required for GSM/EDGE/EGPRS2 downlink samples because there is no summing of downlink samples in BTS systems. Optional dual bit map parameters for GSM/EDGE/EGPRS2 downlink data message transmission are provided in Table 64-Table 68 for different sampling rates and different control messaging scenarios. Control messages can either be sent through the same channel as data or through control message slots. If hard bits are used, the same rules that are used for UL are recommended for symmetry and all DL timeslot messages are sent as a burst.

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For each case, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

Table 64: Parameters for DL GSM/EDGE in case of 156 symbols per time slot and 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversampling	0	4	14	11	0104208410821042	61	02	6
	3	4	13	3	0104104104104104 2	77	042	12
	6	4	12	16	244891244892	48	0492	13
156, 2x oversampling	0	4	7	7	0020040100200802	63	002	10
	3	4	6	3	3DF7DF7DF7DF7DF7DF7D	78	7BEFBEFBEFBD	47
	6	4	6	26	AD6B56B5AB5AD5	56	0	1
156, 4x oversampling	0	4	3	18	2AAAB55556AAAAD5555	74	15555555	29
	3	4	3	18	554AAA5552AA9554AAA	76	2AAAA	19
	6	4	3	7	25294A5294A5294A	63	1294A52A	30
156, no oversampling	0	2	28	11	092524A49292524A	61	0A	6
	3	2	26	3	49249249249249249 24A	80	2	3
	6	2	24	13	AD5AD5AD5AD5AD5	60	1	1
156, 2x oversampling	0	2	14	7	0421042108210842	63	022	10
	3	2	13	3	2DB6DB6DB6DB6DB6DB6D	78	5B6DB6DB6DB5	47
	6	2	13	32	010420821042	45	01042	17
156, 4x oversampling	0	2	7	24	00004000080002	56	00002	17
	3	2	6	27	7FF7FFBFFDFFD	51	3FD	10
	6	2	6	13	3BDEF7BDD	34	1DEF7BDD	29
156, no oversampling	0	1	56	15	6EDDBBB76ED	43	DDBB76ED	32
	3	1	52	3	DB6DB6DB6DDB6DB6DB6D	80	5	3
	6	1	49	10	0104104104104104 2	78	1	1
156, 2x oversampling	0	1	28	7	252525292929494A	63	12A	10
	3	1	27	3	12492492492492492 492	79	4924924924A	44
	6	1	26	32	0924A492924A	45	0924A	17
156, 4x oversampling	0	1	14	24	00804010080402	56	00202	17
	3	1	13	27	7DF7EFBEFDF7D	51	3BD	10
	6	1	13		56B56B5AB5AD5	51	AD5	12

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Table 65: Parameters for DL GSM/EDGE in case of 187 symbols per time slot and 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
187, no oversampling	0	4	11	1	1DDDD	17	0	0
	3	4	11	4	0000400020002	50	00002	17
	6	4	10	1	2A54AA	23	0	0
187, 2x oversampling	0	4	5	2	FEFF7FBFDFEFF7FBFD	72	7FBFD	19
	3	4	5	20	1B76EDBB76D	41	1B76ED	21
	6	4	5	4	1555AAAD555AAAD555	69	1555	13
187, 4x oversampling	0	4	2	2	FFFF7FFFDFFFF7FFFD	72	7FFFD	19
	3	4	2	1	1FEFFBFEFFBFEFFBFD	69	0	0
	6	4	2	20	1F7EFDFBF7D	41	1F7EFD	21
187, no oversampling	0	2	23	1	15555	17	0	0
	3	2	22	4	0040402020202	50	00202	17
	6	2	20	1	7EFEFD	23	0	0
187, 2x oversampling	0	2	11	2	1DEEF77BBDDEEF77BBDD	77	1DD	9
	3	2	11	15	0A52A52A52A52A	53	14A54A52A52A	46
	6	2	11	5	00040010004002	55	0002	14
187, 4x oversampling	0	2	5	2	FEFF7FBFDFEFF7FBFD	72	7FBFD	19
	3	2	5	1	1DEF7BDEF7BDEF7BDD	69	0	0
	6	2	5	20	1B76EDBB76D	41	1B76ED	21
187, no oversampling	0	1	47	1	00002	17	0	0
	3	1	44	3	088888444444222222	71	2	4
	6	1	41	1	6EEEED	23	0	0
187, 2x oversampling	0	1	23	3	55AAD56AB55	43	2AD56AB55	34
	3	1	22	17	7BEFBEFBEFBD	47	3DF7DF7DF7D	42
	6	1	22	5	02040810204082	55	0082	14
187, 4x oversampling	0	1	11	2	1DEEF77BBDDEEF77BBDD	77	1DD	9
	3	1	11	1	15AD6B5AD5AD6B5AD5	69	0	0
	6	1	11	15	0A52A52A52A52A	53	14A54A52A52A	46

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Table 66: Parameters for DL GSM/EDGE in case of 1536 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modu Lo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversampling	0	1	113	15	2A552A954AA	43	54A954AA	32
	3	1	105	3	4924949249492494924A	80	2	3
	6	1	98	10	124924924924924924A	75	2529294A	31
156, 2x oversampling	0	1	56	7	77777BBBBBDDDDD	59	3BBBBDDDDD	38
	3	1	54	4	B6DB6DB6DB6DB6DB5	68	16D	9
	6	1	52	32	1B76EDDBB76D	45	1B76D	17
156, 4x oversampling	0	1	28	19	042110844211084422	70	08844222	31
	3	1	27	39	6DB6EDB6D	35	36DB6D	22
	6	1	27	9	0410420821042	51	042	12
187, no oversampling	0	1	94	1	00202	17	0	0
	3	1	88	4	555554AAAAAA	48	0AAAAAA	25
	6	1	83	1	2AAAAA	23	0	0
187, 2x oversampling	0	1	47	2	010080804040202	60	00804040202	43
	3	1	45	16	2DB6DB6DB6DB5	50	16DB6DB6DB5	41
	6	1	44	5	12244892244892	55	0892	14
187, 4x oversampling	0	1	23	3	55AAD56AB55	43	2AD56AB55	34
	3	1	23	1	010841084108410842	69	0	0
	6	1	22	17	7BEFBEFBEFBD	47	3DF7DF7DF7D	42

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Table 67: Parameters for DL GSM/EDGE in case of 3072 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modu Lo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversampling	0	1	226	11	FEFF7F7FBFBFDFD	60	1FDFD	17
	3	1	210	3	DB76DDB76DDB76DDB76D	80	5	3
	6	1	196	10	DB6DB6DB6DB6DB6DB6D	76	16DB6D	21
156, 2x oversampling	0	1	113	7	55555AAAAB55555	59	2AAAAD5555	38
	3	1	109	4	24924924492492492	68	04A	9
	6	1	105	32	0A54A94A952A	45	0A52A	17
156, 4x oversampling	0	1	56	19	14A952A54A952A54AA	70	2A9552AA	31
	3	1	55	39	24A4A4A4A	35	124A4A	22
	6	1	54	6	2492524929249492A	71	0924A492924A	45
187, no oversampling	0	1	188	1	02222	17	0	0
	3	1	176	3	FFFFFDFFFFFDFFFFFD	72	1	1
	6	1	166	1	7FFFFD	23	0	0
187, 2x oversampling	0	1	94	2	111088844442222	60	08884442222	43
	3	1	91	11	1249244924922492492	75	2492	16
	6	1	88	6	56AD6AD6AD5	43	56AD6AD5	31
187, 4x oversampling	0	1	47	2	010080804040202	60	00804040202	43
	3	1	46	1	09494949494949494A	69	0	0
	6	1	45	16	2DB6DB6DB6DB5	50	16DB6DB6DB5	41

Table 68: Parameters for DL GSM/EDGE in case of 6144 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modu Lo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, 2x oversampling	0	1	227	7	000010000100002	59	0000080002	38
	3	1	218	5	2DB6D6DB6B6DB5	54	5B5	11
	6	1	210	32	1F7DFBEFDF7D	45	1EFBD	17
156, 4x oversampling	0	1	112	17	3F7EFDFBF7EFDFBF7EFD	78	7BEFBEFBD	35
	3	1	110	21	377777776EEEEEEED	66	1	1
	6	1	108	7	1B76DDBB6EDDB76D	61	DBB6EDDB76D	44
187, 2x oversampling	0	1	188	2	2AA95552AAA5554AAAA	75	0AAA	13
	3	1	182	11	5B6B6D6DB5B6B6DADB5	75	B5B5	16
	6	1	177	6	02082082082	43	02082082	31
187, 4x oversampling	0	1	94	2	111088844442222	60	08884442222	43
	3	1	92	1	1DDDDDDDDDDDDDDDDD	69	0	0
	6	1	91	11	1249244924922492492	75	2492	16

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Glossary

Abbreviations

BB	Baseband module
BTS	Base transceiver system
C/D	Combiner and distributor
CCM	Control and clock module
DL	Downlink direction from BTS to RRUs
HW	Hardware
LC	Local Converter that interfaces to RP3 and RP1 and combines them to RP3-01 and vice versa. Local Converter is referred to as Local cabinet in [2].
LSB	Least Significant Bit
LTE	Long Term Evolution
MSB	Most Significant Bit
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
RP3-01	Extension of RP3 protocol where RP1 data is mapped into RP3 messages
RRU	Remote RF unit. RRU is referred to as Remote cabinet in [2].
SFN	System frame number
UL	Uplink direction from RRUs to BTS

Definition of Terms

None listed.

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