

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner

v.

SONRAI MEMORY LIMITED
Patent Owner

Patent No. 6,874,014

DECLARATION OF DR. MARTIN WALKER

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I, Martin Walker, declare as follows:

I. INTRODUCTION

1. I have been retained by Apple Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 6,874,014 (“the ’014 patent”) (EX1001).

I have been asked to consider whether certain references disclose or suggest the limitations recited in claims 1, 3, 5, 7, 11-13, and 15 (“the challenged claims”) of the ’014 patent. My opinions are set forth below.

2. I am being compensated at my rate of \$650 per hour for the time I spend on this matter. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. In this section, I have summarized my educational background, career history, publications, and other relevant qualifications. My Curriculum Vitae, which states my qualifications more fully, is filed as a separate Exhibit (EX1003).

4. I received my Bachelor of Science degree in Electrical Engineering from the Massachusetts Institute of Technology in 1973. I received my Master of Science and Doctor of Philosophy degrees in Electrical Engineering in 1976 and 1979 from Stanford University.

5. Accordingly, I have over 40 years of experience with writing and analyzing computer software as well as computer system architecture.

6. Beginning in 1981, I developed computer software to aid in the development of integrated circuits. From 1983 to 1989, I was the founder and Chief Technical Officer at Analog Design Tools, Inc. Analog Design Tools' primary product was software used to design integrated circuits. I was responsible for all technical aspects of product definition and development, including the software design.

7. From 1990 to 1994, I was a founder and Executive Vice President of Symmetry Design Systems, which specialized in software product design and consulting for the electronic design marketplace.

8. In 1995, I founded a company called Frequency Technology (later called Sequence Design) that developed software for the design of advanced system-on-a-chip integrated circuits. As Chief Executive Officer, director, and Chief Scientist at Sequence, I was involved in overseeing the development of the company's products and technologies.

9. From 2000 to present, I have worked in the fields of market research and consulting in the fields of semiconductor (IC) design, including electronic design automation and field programmable gate arrays (FPGA) programming. Since that time, I have served as an expert in nearly 100 cases.

10. I am a named inventor on three patents in the fields of integrated circuit design: U.S. Patent Nos. 6,643,831, 6,381,730, and 5,901,063.

III. MATERIALS CONSIDERED AND SUMMARY OF OPINIONS

11. The opinions contained in this Declaration are based on the documents I reviewed and my professional judgment, as well as my education, experience, and/or knowledge regarding technologies relating to, among other things, networking technologies.

12. In forming my opinions expressed in this Declaration, I reviewed the following materials (and any other materials that I reference in this Declaration):

EX1001	U.S. Patent No. 6,874,014
EX1004	Prosecution History of U.S. Patent No. 6,874,014
EX1005	U.S. Patent Publication No. 2001/0044817 to Asano (" <i>Asano</i> ")
EX1006	U.S. Patent No. 6,542,991 to Joy et al. (" <i>Joy</i> ")
EX1007	U.S. Patent No. 7,143,401 to Babaian et al. (" <i>Babaian</i> ")
EX1008	Joch, "HOW-TO Chip Multiprocessing," Computerworld, November 27, 2000
EX1009	Olukotun et al., "The Case for a Single-Chip Multiprocessor," ACM SIGPLAN Notices, Vol. 31, Issue 9, Sept. 1996
EX1010	U.S. Patent No. 6,550,020 to Floyd
EX1011	Barroso et al., "Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing", Proc. 27th ACM Int'l Symp. Computer Architecture, 2000
EX1012	U.S. Patent No. 6,772,241 to George et al.
EX1013	U.S. Patent No. 6,526,462 to Elabd
EX1014	Hammond et al., "A Single-Chip Multiprocessor," Computer, vol. 30, no. 9, pp. 79–85, Sept. 1997
EX1015	U.S. Patent No. 6,178,503 to Madden et al.

EX1016	U.S. Patent No. 6,085,247 to Parsons, Jr. et al.
EX1017	U.S. Patent No. 6,247,109 to Kleinsorge et al.
EX1018	U.S. Patent No. 6,397,242 to Devine et al.

13. In support of my opinions, I have taken into account how a person of ordinary skill in the art (as defined below in Section IV) would have understood the claims and the specification of the '014 patent at the time of the alleged invention. My opinions take into account how a person of ordinary skill in the art would have understood the '014 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

14. As I discuss in detail below, it is my opinion that certain references disclose or suggest all the limitations recited in claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent.

IV. PERSON OF ORDINARY SKILL IN THE ART

15. I have been asked to consider the time of the alleged invention for the '014 patent to be the early 2001 time frame, including and up to May 29, 2001, which is the filing date of an application associated with the '014 patent. (EX1001, Cover). I may refer to this time frame in this declaration as the time of the alleged invention, the relevant time, or the time of the '014 patent.

16. Based on my knowledge and experience, I understand what a person of ordinary skill in the art would have known at the time of the alleged invention of the '014 patent. In my opinion, based on my review of the '014 patent, such a person

would have had an undergraduate degree in electrical engineering, computer engineering, computer science or a related field along with at least two years of work experience in the field of computer processor architecture. (*See, e.g.*, EX1001, 1:11–2:9 (discussing the background of the '014 patent), 2:12–44 (discussing the summary of the disclosure).) Alternatively, more education can supplement practical experience and vice versa.

17. My analysis of the '014 patent and my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it above, at the time of the alleged invention for that patent.

V. TECHNICAL BACKGROUND

18. In this section, I discuss the state of the art relevant to the subject matter of the '014 patent as would have been known, understood, and appreciated by a person of ordinary skill in the art prior to and at the time of the alleged invention for the '014 patent (e.g., early 2001 time frame, including and up to May 29, 2001, as I mentioned above in Section IV). I rely on and incorporate the understandings below regarding such known features and technologies to support my opinions regarding the knowledge of a person of ordinary skill in the art at the relevant timeframe and the motivations relating to how the prior art discloses and/or suggests the limitations of claims 1, 3, 5, 7, 11–13, and 15 of the '014 patent. In my opinion, the understandings regarding the technologies, processes, and features as I

discussed in this section (Section V) would have been in the mind of a person of ordinary skill in the art when contemplating the disclosures and/or suggestions in the prior art that I address below in Sections VII and IX and when considering combining features from that prior art in the manner that I explain below in that section.

A. Role of operating systems

19. It was generally known at the time of the alleged invention that an operating system is a computer program that provides an environment in which other computer programs can run:

Most people are generally familiar with computer operating systems. An operating system is the code or computer program that provides an environment in which other computer programs can run. The operating system manages the system resources, such as processing resources, memory allocation, and I/O devices, to enable other programs to easily take advantage of these resources. Some operating systems are multitasking, meaning they support concurrent operation of more than one task. A multitasking operating system divides the resources among various processes, giving each process access to memory, processing resources, and at least one execution thread.

(EX1016 (Parsons), 1:14–26).

20. Also, it was generally known that certain kinds of operating systems

provided an environment in which other *operating systems* could run. One example was a VMM, or Virtual Machine Monitor:

One solution that was the subject of intense research in the late 1960's and 1970's came to be known as the “virtual machine monitor” (VMM). See, for example, R. P. Goldberg, “Survey of virtual machine research,” IEEE Computer, Vol. 7, No. 6, 1974. During that time, moreover, IBM Corp. adopted a virtual machine monitor for use in its VM/370 system.

A virtual machine monitor is a thin piece of software that runs directly on top of the hardware and virtualizes all the resources of the machine. Since the exported interface is the same as the hardware interface of the machine, the operating system cannot determine the presence of the VMM. Consequently, when the hardware interface is compatible with the underlying hardware, the same operating system can run either on top of the virtual machine monitor or on top of the raw hardware.

(EX1018 (Devine), 1:37–52).

21. VMMs and similar “virtualization” OSes provided a means to run multiple standard OSes concurrently on a single CPU or a multiple-CPU processor:

FIGS. 7 and 8, as well as the description of the invention above, have assumed the presence of a single processor in the hardware **710**. This assumption has been made solely to simplify the discussion. The invention may also be used where the hardware **710** includes more than one processor.

(*Id.*, 25:2-6)

B. Configuring and operating systems with multiple processors

22. It was known at the time of the alleged invention to configure and operate a system, such as a microcomputer, with multiple processors to support additional and enhanced computing features. (EX1010 (Floyd), 1:16–27 (excerpted below); EX1012 (George), 1:19–25 (excerpted below); EX1017 (Kleinsorge), 1:34–65). Such a system was often referred to as a multiprocessor system, or just a multiprocessor.

... **By contrast, microcomputers designed for more demanding tasks (e.g., network servers) commonly include multiple CPUs.** While increasing the number of available processors augments computing power, coordinating the actions of the cooperating CPUs requires a concomitant increase in the complexity of the overall system architecture. ...

(EX1010 (Floyd), 1:20–27 (excerpted with emphasis added))¹.

Over the last few years, there have been many advances in computer system technology. These advances have lead to the development of computer systems having multiple processors to support additional and/or enhanced computing features. FIG. 1 illustrates, for example, one type of computer system that uses a co-processor in conjunction with a host CPU to perform

¹ Unless otherwise noted, all emphases are added.

complex mathematical operations.

(EX1012 (George), 1:19–25).

23. Because of the multiple processors in the multiprocessor system, these systems can execute applications more effectively because applications can be distributed among many processors instead of waiting to be executed by a single processor. *See, e.g.*, EX1010, 1:20–33 (excerpted above), *see also* EX1017, 1:41–46. For example:

Traditionally, computing speed has been addressed by using a “shared nothing” computing architecture where data, business logic, and graphic user interfaces are distinct tiers and have specific computing resources dedicated to each tier. Initially, a single central processing unit was used and the power and speed of such a computing system was increased by increasing the clock rate of the single central processing unit. More recently, computing systems have been developed which use several processors working as a team instead one massive processor working alone. **In this manner, a complex application can be distributed among many processors instead of waiting to be executed by a single processor.**

EX1017, 1:41–46.

C. Multiprocessor system running multiple operating systems concurrently

24. At the time of the alleged invention, it was well known that a

multiprocessor system could operate with either a single operating system (OS) or multiple OSs. Running a single OS on a multiprocessor was common:

“There are a number of ways to use a multiprocessor. Today, the most common use is to execute multiple processes in parallel to increase throughput in a multiprogramming environment under the control of a multiprocessor aware operating system. We note that there are a number of commercially available operating systems that have this capability (e.g. Silicon Graphics IRIX, Sun Solaris, Microsoft Windows NT).”

EX1009, 3.

25. However, it was also well known that a multiprocessor system could run multiple OSes concurrently. *See e.g.,* EX1012, 1:25–28 (discussing a multiprocessor system with a single OS), 2:41–47 (discussing a multiprocessor system with multiple operating systems), 2:55–61; EX1017, 1:46–65 (excerpted below). For example:

Such systems typically consist of several central processing units (CPUs) which are controlled by a single operating system. In a variant of a multiple processor system called “symmetric multiprocessing” or SMP, the applications are distributed equally across all processors. ... In another variant called “asymmetric multiprocessing” or AMP, one processor acts as a “master” and all of the other processors act as “slaves.” Therefore, all operations, including the operating system, must

pass through the master before being passed onto the slave processors. These multiprocessing architectures have the advantage that performance can be increased by adding additional processors, but suffer from the disadvantage that the software running on such systems must be carefully written to take advantage of the multiple processors and it is difficult to scale the software as the number of processors increases. Current commercial workloads do not scale well beyond 8-24 CPUs as a single SMP system, the exact number depending upon platform, operating system and application mix.

EX1017 (Kleinsorge), 1:46–65.

26. As an example of an AMP system, George (EX1012) discloses:

In one embodiment, the computer system may include a first processor coupled with a controller through a first bus and a second processor coupled with the controller through a second bus. **The second processor (e.g., a co-processor) operates with an operating system independent from the operating system of the first processor (e.g., a host processor).**

...

FIG. 2 illustrates one embodiment of a computer system having multiple processors running independent operating systems. Computer system 200 includes a processor 210, memory control hub (MCH) 220, an input/output control hub (ICH) 230, platform devices 240, co-processor 250, and buses 261-264. Buses 261-264 carry data and addresses to the various

components in computer system 200.

EX1012, 2:41–47, 2:55–61.

D. Sharing multiprocessor resources

27. In multiprocessor systems that execute multiple OSs, it was further known at the time of the alleged invention that such systems could be configured to share resources, such as one or more of its processors, between the different operating systems running simultaneously in the system. For example:

In accordance with the principles of the present invention, multiple instances of operating systems execute cooperatively in a single multiprocessor computer wherein all processors and resources are electrically connected together. The single physical machine with multiple physical processors and resources is adaptively subdivided by software into multiple partitions, each with the ability to run a distinct copy, or instance, of an operating system. Each of the partitions has access to its own physical resources plus resources designated as shared. In accordance with one embodiment, the partitioning of resources is performed by assigning resources within a configuration.

More particularly, software logically, and adaptively, partitions CPUs, memory, and I/O ports by assigning them together. An instance of an operating system may then be loaded on a partition. At different times, different operating system instances may be loaded on a given partition. This partitioning,

which a system manager directs, is a software function; no hardware boundaries are required. Each individual instance has the resources it needs to execute independently. **Resources, such as CPUs and memory, can be dynamically assigned to different partitions and used by instances of operating systems running within the machine by modifying the configuration.** The partitions themselves can also be changed without rebooting the system by modifying the configuration tree. The resulting adaptively-partitioned, multi-processing (APMP) system exhibits both scalability and high performance.

EX1017, 4:43–5:3.

E. Adoption of single-chip multiprocessors

28. It was known at the time of the alleged invention that multiple processors in a multiprocessor system, previously implemented on separate chips, could be advantageously combined on a single chip with sufficiently advanced chip manufacturing technology:

Due to recent advances in the manufacture of integrated circuits, however, multi-core microprocessor chips may soon be replacing single-core CPUs as the processor of choice for high-performance microcomputers. Multi-core microprocessors feature a single integrated circuit that includes two or more main processing cores, each of which may be utilized as if it was a separate central processing unit. Furthermore, in state-of-the-art multi-core processors, each of the main cores provides

computing power that equals or exceeds that of a conventional high-performance single core processor.

EX1010, 1:37–48.

29. Indeed, the concept of a single chip multiprocessor has been around since at least the 1990s:

Advances in IC processing allow for more microprocessor design options. The increasing gate density and cost of wires in advanced integrated circuit technologies require that we look for new ways to use their capabilities effectively. **This paper shows that in advanced technologies it is possible to implement a single-chip multiprocessor in the same area as a wide issue superscalar processor.** We find that for applications with little parallelism the performance of the two microarchitectures is comparable. **For applications with large amounts of parallelism at both the fine and coarse grained levels, the multiprocessor microarchitecture outperforms the superscalar architecture by a significant margin.** Single-chip multiprocessor architectures have the advantage in that they offer localized implementation of a high-clock rate processor for inherently sequential applications and low latency interprocessor communication for parallel applications.

EX1009, 1.

30. In addition, *Hammond* explains the same conclusion that for a given size of chip, a single-chip multiprocessor will outperform a wide-issue superscalar

uniprocessor. EX1014, 1, 4

31. It was also expected at the time of the alleged invention that such single chip multiprocessors (also known as multi-core microprocessor chips) would replace single-processor chips in computer systems. Indeed, *Floyd* discloses this change as I noted above. EX1010, 1:37–48.

32. Barroso also relatedly discloses that:

... The abundance of explicit thread-level parallelism in commercial workloads, along with advances in semiconductor integration density, **identify chip multiprocessing (CMP) as potentially the most promising approach for designing processors targeted at commercial servers.**

EX1011, 1.

The use of chip multiprocessing is inevitable in future microprocessor designs. Advances in semiconductor technology are enabling designs with several hundred million transistors in the near future. ... At the same time, **using the extra transistors to integrate multiple processors onto the same chip is quite promising, especially given the abundance of explicit thread-level parallelism in important commercial workloads.** At least a couple of next-generation processor designs subscribe to this philosophy by integrating two superscalar cores on a single die. **The key questions for designers of future processors will not be whether to use chip multiprocessing, but the appropriate trade-off between**

the number of cores and the power of each core, and how to best partition the memory hierarchy among the multiple cores.

Id., 11.

33. Indeed, it is was well known that in the year 2000, Sun Microsystems and IBM had already incorporated chip multiprocessors into its servers:

Early next year, top-echelon power users will find out if two heads are better than one. That's when Sun Microsystems Inc., IBM, Compaq Computer Corp., Hewlett-Packard Co. and others will **start to roll out high-end servers that take advantage of chip multiprocessing (CMP)**, a step forward from current systems that load up boxes with multiple discrete chip modules.

EX1008, 1.

The age for commercially viable CMP systems has arrived, thanks to continuing refinements in chip manufacturing techniques that let engineers pack circuits more densely. The extra die space opens up room for multiple chips - two in the initial systems but perhaps up to eight in later generations of CMP modules.

Id., 2.

34. It was also well known at the time of the alleged invention of the '014 patent that there were many recognized benefits in using a single chip

multiprocessor over a single processor chip. For example, each processor on a single chip multiprocessor could be used as if it was a separate processor. EX1010, 1:37–48. Furthermore, each of the processors in the single chip multiprocessor provides a computing power that equals or exceeds that of a conventional high-performance single core processor. *Id.*; *see also* EX1011, 1, 11. Also due to the number of processors on the single chip multiprocessor, a system can provide better execution of workloads. *See, e.g.*, EX1009, Abstract, 1; EX1011, 1, 11; EX1008, 1.

35. Likewise, it was well known that by putting multiple processors on a single chip, engineers could take advantage of shorter distances and faster bus speeds when shuttling data between the processors. EX1008, 1; *see also* EX1010, 1:48–60 (“Among the benefits provided by multi-core processors is an increase in physical processing core density within multiprocessor data processing systems, in that more processing cores may operate within a given amount of space, which leads to improvements in overall multiprocessor system performance”).

36. For example:

Our detailed simulation results show that while each Piranha processor core is substantially slower than an aggressive next-generation processor, **the integration of eight cores onto a single chip allows Piranha to outperform next-generation processors by up to 2.9 times (on a per chip basis) on important workloads such as OLTP** [on-line transaction

processing]. This performance advantage can approach a factor of five by using full-custom instead of ASIC logic.

EX1011, 1.

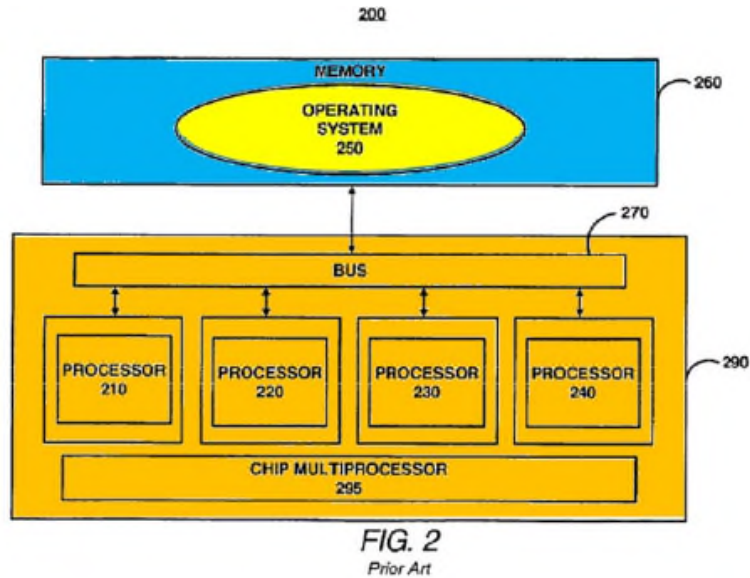
37. In another example:

Early tests are showing that two processors in a single module outperform multiple discrete processors by 50% or more. By putting two CPUs on a single piece of silicon, engineers can take advantage of shorter distances and faster bus speeds when shuttling data between the two CPU cores. The net performance result for IBM's version - called the Power4 processor - is the ability to process 100GB of data per second, or the equivalent of 20 full-length DVDs, says Joel Tendler, director of technology strategy at IBM's server group in Austin, Texas.

EX1008, 1.

VI. THE '014 PATENT

38. The '014 patent relates to “a multiprocessing chip utilizing multiple operating systems.” EX1001, 1:6-10. The '014 patent admits that multiprocessing systems with a multiprocessing chip were well-known, and it depicts a known prior art system in Figure 2 below. EX1001, 1:34-59; 1:41-42 (explaining that it was well-known in the art to use “multiple processors on a single die” to conserve space in a system).



EX1001, FIG. 2 (annotated).

39. The prior art multiprocessing system (200) includes a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted in orange). EX1001, 1:34-37. The processors 210-240 use a single operating system 250 (highlighted in yellow) stored in memory 260 (highlighted in blue). EX1001, 1:37-40. The processors “may communicate with the memory 260 via a bus 270.” EX1001, 1:40-41. The ’014 patent states that “schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together.” EX1001, 1:44-47; 1:60-63 (the ’014 patent acknowledges that it was known in the art that multiprocessor systems could “support[] multiple processors executing multiple operating systems”).

40. Unlike the prior art system with multiple processors and a single operating system, the ’014 patent discloses a “multiprocessing system” where

“multiple processors are connected to a memory storing *multiple* operating systems,” as illustrated in Figure 3 below. EX1001, 2:12-16 (emphasis added)².

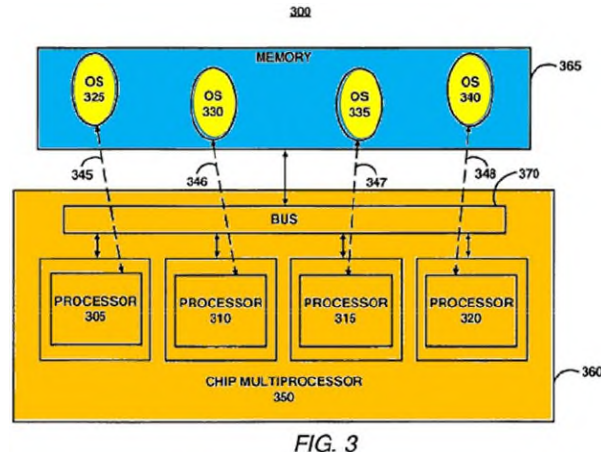


FIG. 3

EX1001, FIG. 3 (annotated), 2:54-55.

41. Like the prior-art system in FIG. 2 above, the computer system 300 in FIG. 3 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die (highlighted in orange). EX1001, 3:4-7. The multiprocessing system further includes multiple operating systems 325-340 (highlighted in yellow) stored in a memory 365 (highlighted in blue). EX1001, 3:10-11. The '014 patent explains that “[d]uring operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus 370.” EX1001, 3:11-14. The '014 patent also explains that “[e]ach processor may be ... capable of simultaneously executing

² Unless otherwise noted, all emphases are added.

multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.” EX1001, 3:47-51.

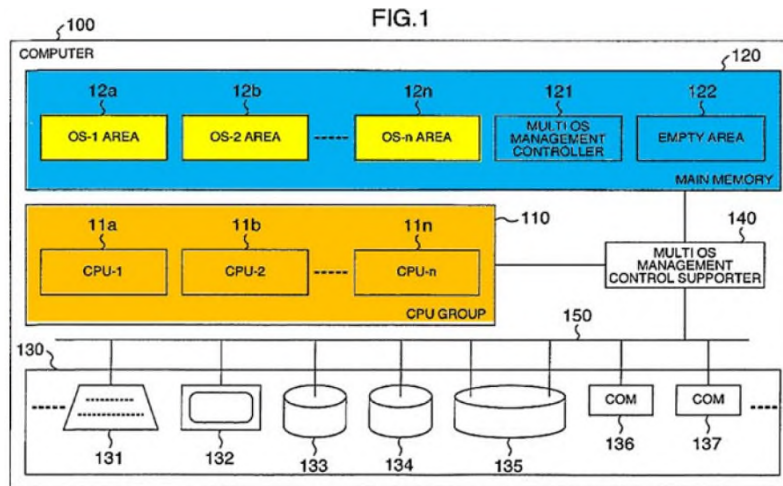
42. Claims 1, 3, 5, 7, 11–13, and 15 of the ’014 patent recite limitations relating to the features discussed above. However, as I discuss below in Sections VII and IX, it is my opinion that all of these features were well known in the art at the relevant time.

VII. OVERVIEW OF THE PRIOR ART³

A. Overview of Asano (EX1005)

43. Like the ’014 patent, Asano discloses a multiprocessing system 100 including multiple processors (e.g., 11a-11n) in a processor group 110 (highlighted in orange) where the multiple processors are connected to a memory (highlighted in blue) storing multiple operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1 (reproduced below); *see also* EX1005, ¶[0001] (“The present invention relates to a computer system and a method for controlling a computer system in which a plurality of operating systems (OS) operate on one computer”).

³ These summaries of the prior art references in Section VII are applicable to my analysis below in Section IX. Accordingly, I incorporate these summaries, which reflect how a person of ordinary skill in the art would have understood the references, into my analysis below where appropriate (*see, e.g.*, Section IX below).



EX1005, FIG. 1 (annotated).

44. The computer system 100 in Figure 1 includes a processor group 110 having multiple processors 11a-11n (highlighted in orange). EX1005, ¶[0031]. The multiprocessing system further includes multiple operating systems (highlighted in yellow), e.g., OS-1-OS-n, stored in a memory 120 (highlighted in blue). *Id.* Asano discloses that this multiprocessing system 100 can “execute a plurality of operating systems.” *Id.*

45. Asano further discloses that the processors are allocated either individually or in groups to the various operating systems. EX1005, ¶[0035]. For example, each processor may be allocated to a particular operating system at a predetermined time interval. *Id.*

B. Overview of Joy (EX1006)

46. Joy discloses multiple processors mounted on a single die. For example, Joy discloses a horizontal threaded processor architecture that “combines

multiple processors on a single integrated circuit die.” EX1006, 7:4-6. “The multiple processors are vertically threaded to form a processor with both vertical and horizontal threading, *augmenting executing efficiency and decreasing latency in a multiplicative fashion.*” EX1006, 7:6-9 (emphasis added); 2:17-32 (“To further increase system parallelism in some processor embodiments, multiple processor cores are formed in a single die.”). Joy further discloses that each of the vertical and horizontal threaded processors in the single integrated chip of Joy “advantageously accelerates context switching time from millisecond ranges to nanosecond ranges.” EX1006, 7:49-54. Joy explains that such fast context switching “is highly advantageous in all processing environments including embedded, desktop, and server applications, and the like.” EX1006, 7:52-54.

47. Figure 2C below illustrates the timing diagram for an exemplary single integrated circuit in Joy that includes two processors on the single die, where each processor can execute two or more threads simultaneously. EX1006, 7:9-15, 7:20-27, FIG. 2C; *see also* EX1006, 2:42-57 (Joy provides several exemplary configurations including “a ‘4C4T’ configuration” where a “four-processor multiprocessor is formed on a single die with each of the four processors being four-way vertically threaded.”); 2:34-42 (“For example two processor cores are combined ... in one system. In another example, four processor cores are combined A countless number of variations are possible. In some systems, each processor

core is a vertically-threaded pipeline.”). In particular, Figure 2C below illustrates a first processor executing a “first thread 252” and a “second thread 254” (highlighted red) in parallel with a second processor executing a “first thread 256” and a “second thread 258” (highlighted blue). EX1006, 7:10-27, FIG. 2C. Joy explains that by implementing “both vertical multithreading and horizontal multithreading,” the “processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time.” EX1006, 2:17-32; 7:52-54.

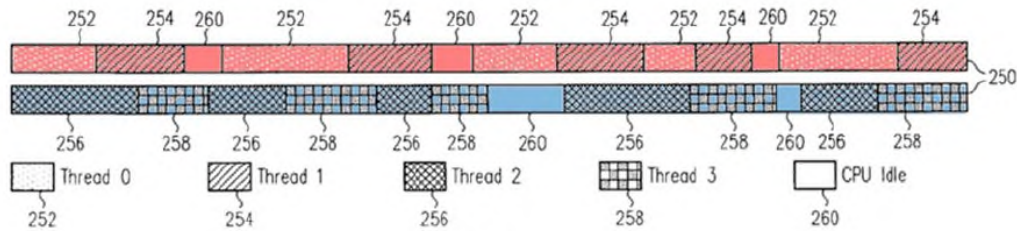


FIG. 2C

EX1006, FIG. 2C; 4:46-50 (FIG. 2C illustrates a timing diagram for the execution flow in a vertical and horizontal multithread processor).

C. Motivation to Combine Asano and Joy

48. As previously noted, Asano discloses a multiprocessing system 100 that includes multiple processors (e.g., 11a-11n) in a processor group 110 where the multiple processors are connected to a memory storing multiple operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1; see also EX1005, ¶[0001] (“The present invention relates to a computer system and a method for controlling a computer system in which a plurality of operating systems (OS) operate on one computer

....”). Asano discloses that each of the processors is allocated to execute an operating system from a plurality of operating systems, OS-1 to OS-n.

49. Asano discloses that at least two operating systems are simultaneously running on computing system 100. EX1005, ¶¶[0032]-[0033]. For example, Asano discloses that the computer system 100 includes a main memory 120 (“memory”). EX1005, ¶[0030]. The main memory 120 “includes main memory areas 12a to 12n” that are “allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n),” as shown in Figure 1 below. Figure 2, reproduced below, further illustrates one configuration of the system shown in Figure 1 where two operating systems, OS-1, OS-2 (highlighted yellow), are simultaneously running on the computer system 100. EX1005, ¶¶[0032]-[0033]. Thus, Asano teaches a computing system that includes multiple processors, where at least two processors are able to simultaneously execute a command, i.e., commands associated with executing an operating system. Asano does not limit the processor to any specific configuration or implementation, nor does it require a specific structure or arrangement. Thus, it is my opinion that a person of ordinary skill in the art seeking to implement a multi-processor system pursuant to the teachings of Asano would consider references disclosing the structure of such multi-processor systems, which includes Joy.

50. It is my opinion that Joy discloses precisely what is suggested by

Asano, multiple processors mounted on a single die. Moreover, because Joy discloses a flexible design (e.g., “[c]ountless other ‘nCkT’ structures and combinations may be implemented on one or more integrated circuit dies depending on the fabrication process employed and the applications envisioned for the process”), a person of ordinary skill in the art would immediately understand that the teachings of Joy regarding the fabrication process of multiple processors on a single die could be used in combination with the teachings of Asano regarding a multiprocessing system that simultaneously executes multiple operating systems.

51. As further discussed below, Joy teaches that it is advantageous to locate multiple processors on the same die, which leads to sped-up communications and reduced latency, for example. *See e.g.*, EX-2006, 7:31-39, 7:55-57. Thus, I believe that these known advantages would further motivate a POSITA to implement Asano’s processors on a single die.

D. Overview of Babaian

52. Babaian discloses multiple processors mounted on a single die. For example, Babaian discloses a single chip multiprocessor system. EX1007, 3:56-62 (“a *single chip* multiprocessor system with explicit parallelism architecture processors ...[with] multiprocessor parallel execution to help ensure a high level use of ILP [instruction-level parallelism]”) (excerpted), 4:8-18 (describing that the single chip multiprocessor system can be either tightly-coupled or weakly-coupled),

4:31-35 (describing the benefits associated with the single chip multiprocessor system that include “substantially increas[ing] the performance” in executing “program streams” and “data exchange”), 7:1-9 (Figure 7 illustrates an exemplary single-chip multiprocessor system 700 suited for parallel execution). The single-chip multiprocessor includes four processors 710-1 to 710-4 (highlighted orange) and optional specialized co-processors. EX1007, 7:1-9, FIG. 7. Because the processors (e.g., 710-1-4) are all contained in a single chip, a POSITA would have thus understood that the processors are mounted on a single die.

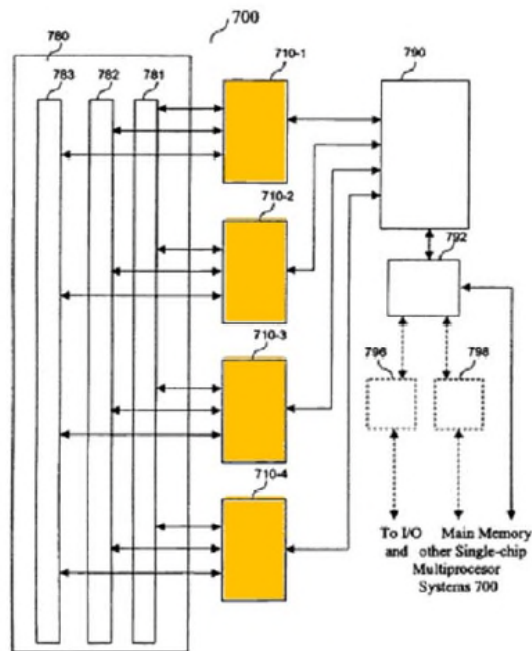


Fig. 7

EX1007, FIG. 7 (annotated); 4:56-58 (FIG. 7 illustrates a single-chip multiprocessor system).

53. Babaian further explains that such a configuration as shown above

allows for “flexible assignment of the idle processors for the execution of a program.” EX1007, 13:65-14:3; 3:14-17. For example, the system may “assign[] some Processors 710 for execution of a task, forming a working configuration.” EX1007, 13:46-48. Processor assignment is implemented by assigning numbers to each processor, e.g., processor 1-4. EX1007, 13:37-46. “For example, for parallel execution in two processors, Processors 710 with the physical numbers 1 and 3 can be assigned.” EX1007, 13:48-50. This processor numbering allows the single-chip multiprocessor to “simultaneously perform[] independent programs.” EX1007, 3:14-17.

E. Motivation to Combine Asano and Babaian

54. As previously noted, Asano teaches a computing system that includes multiple processors, where at least two processors are able to simultaneously execute a command, i.e., commands associated with executing an operating system. *See supra* Section, VII.A; *infra* Sections IX.A.1; IX.B.1. Asano does not limit the processors to any specific configuration or implementation, nor does it require a specific structure or arrangement. Thus, a person of ordinary skill in the art seeking to implement a multi-processor system pursuant to the teachings of Asano would consider references disclosing the structure of such multi-processor systems, which includes Babaian.

55. It is my opinion that Babaian discloses precisely what is suggested by

Asano, multiple processors mounted on a single die. *See supra* Section V.D; *infra* Section IX.B.1. Moreover, because Babaian discloses a flexible design (e.g., “[t]hose skilled in the art will realize that the Single-chip Multiprocessor System, retaining the essential features of the present invention, may have different implementations”), I believe that a person of ordinary skill in the art would immediately understand that the teachings of Babaian regarding the fabrication process of multiple processors on a single chip could be used in combination with the teachings of Asano regarding a multiprocessing system that simultaneously executes multiple operating systems.

VIII. CLAIM CONSTRUCTION

56. I have been asked to give the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history (Ex. 1004) of the ’014 patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

A. “simultaneously executing two or more operating systems”

57. As I understand, in the currently pending litigation, Petitioner and PO have agreed that “simultaneously executing two or more operating systems” should

be construed as “simultaneously executing two or more *independent* operating systems.”

58. Accordingly, for the purposes of my analysis, I have been asked to assume that “simultaneously executing two or more operating systems” should be construed as “simultaneously executing two or more *independent* operating systems.” I have applied this understanding in my analysis.

B. “multiple operating systems residing in a memory”

59. As I understand, in the currently pending litigation, Petitioner and PO have agreed that “multiple operations systems residing in a memory” should be construed as “multiple operating system residing in the same memory.”

60. Accordingly, I have been asked to analyze the challenged claims under both a plain and ordinary meaning construction and the agreed upon construction.

C. “multiple processors are connected to said memory via a bus”

61. As I understand, in the currently pending litigation, Petitioner and PO have agreed that “multiple processors are connected to said memory via a bus” in dependent claim 3 should be construed as “multiple processors are connected to said memory via the same bus.”

62. Accordingly, I have been asked to analyze the challenged claims under both a plain and ordinary meaning construction and the agreed upon construction.

D. “processor means” in claim 12

63. As I understand, in the currently pending litigation, Petitioner and PO have an agreed upon construction for “processor means.” The agreed-upon function is “executing a plurality of operating system means.” The agreed-upon structure is “chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360 as shown in Figure 3 and associated descriptions in the specification; or chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460 shown in Figure 4 and associated descriptions in the specification; and equivalents thereof.”

64. Accordingly, for the purposes of my analysis, I have been asked to apply the agreed upon construction for “processor means.”

E. “operating system means” in claim 12

65. For purposes of my analysis, I have been asked to apply plain and ordinary meaning to this limitation because it does not invoke means plus function.

F. “memory means” in claim 12

66. For purposes of my analysis, I have been asked to assume that the identified function of the “memory means” is “storing said plurality of operating system means,” where the corresponding structure is “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips

connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” EX1001, 3:15-20.

67. I have applied this understanding in my analysis

IX. THE PRIOR ART DISCLOSES ALL OF THE LIMITATIONS OF CLAIMS 1, 3, 5, 9, 11–13, AND 15 OF THE ’014 PATENT

A. Ground 1: Asano and Joy discloses and suggests the features of claims 1, 3, 5, 7, 11–13, and 15

68. In my opinion, the combination of Asano and Joy renders claims 1, 3, 5, 7, 11-13, and 15 obvious.

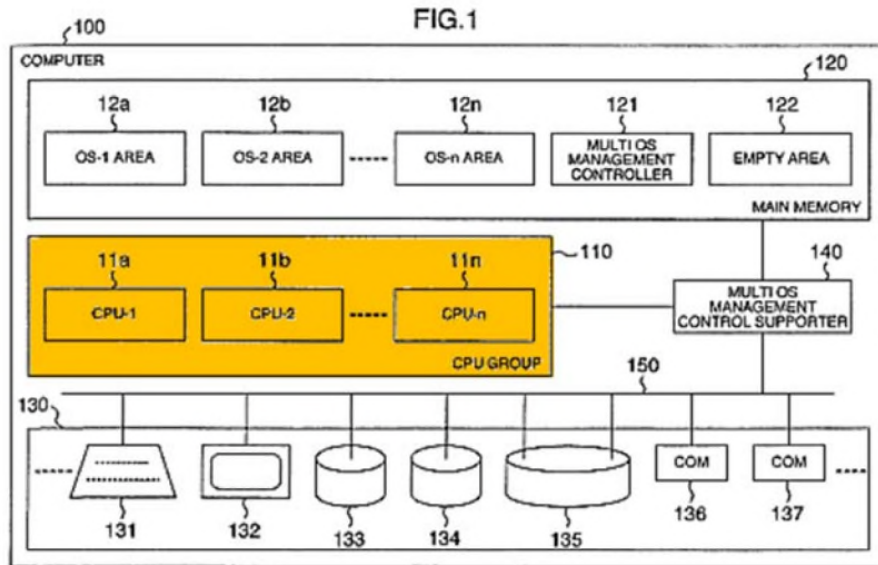
1. Claim 1

a) A multiprocessing system comprising

69. To the extent the preambles are limiting, it is my opinion that the Asano-Joy combination discloses the limitations therein.

70. For example, Asano discloses a computer system, as shown in Figure 1 below, that includes a processor group 110 (highlighted in orange) for executing a plurality of operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1; *see also* EX1005 ¶[0001] (“The present invention relates to a computer system ... in which a plurality of operating systems (OS) operate on one computer, and in particular, to a computer system ... in which computer resources can be efficiently used or operated in an operating state of a plurality of operating systems.”). “The processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b . . . , 11n.”

EX1005, ¶[0031]. A POSITA would have thus understood that Asano's computer system is a multiprocessing system as claimed because this system includes multiple processors (e.g., processors 11a-11n).



EX1005, FIG. 1 (annotated).

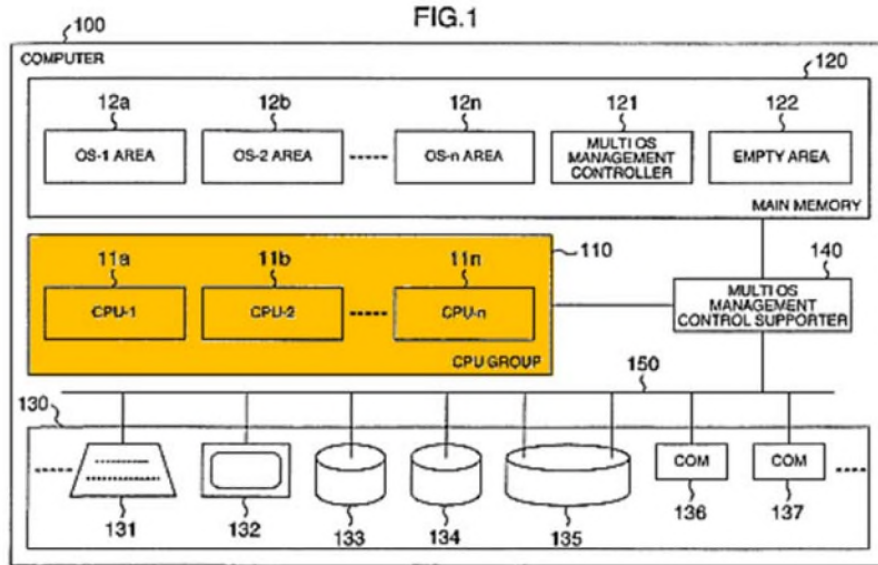
71. Thus, it is my opinion that the Asano-Joy combination discloses “[a] multiprocessing system,” as claimed.

b) multiple processors mounted on a single die

72. It is my opinion that the Asano-Joy combination discloses this limitation.

73. Asano discloses a computer system that includes a processor group 110 that includes multiple processors. EX1005 ¶[0030]-[0031]. For example, Asano discloses that the “processor group 110” (highlighted orange) “is a set of one or

more processors (CPUs)” that “includes processors 11a, 11b . . . , 11n.” EX1005 ¶[0031].



EX1005, FIG. 1 (annotated).

74. To the extent that Asano does not explicitly provide that the multiple processors are mounted on a single die, it is my opinion that Joy teaches doing so.

75. Specifically, Joy discloses multiple processors mounted on a single die. For example, Joy discloses a horizontal threaded processor architecture that “combines multiple processors on a single integrated circuit die.” EX1006, 7:4-6.

76. I believe a POSITA would have been motivated in light of Joy to configure the system in Asano so that its multiple processors are “mounted on a single die,” as claimed. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007).

77. A POSITA would have recognized that Joy and Asano disclose features in a similar technological field. *See supra* Section, V.C. For example, as discussed above, both Asano and Joy relate to multi-processor computing systems. EX1005, ¶[0031] (“The computer system 100 of the first embodiment includes a processor group 110 . . . The processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b, . . . 11n. ”); EX1006, 2:29-31 (“To further increase System parallelism in Some processor embodiments, multiple processor cores are formed in a single die.”); EX1006, 2:29-31 (explaining that Joy’s processor architecture is beneficial for computing applications that are “subject to frequent context switches” such as “disk server, network server, web server, telecommunications applications and the like”), EX1006, 14:64-67. Specifically, each system utilizes a computing system that includes multiple processors that are capable of simultaneously executing commands.

78. Additionally, Asano and Joy relate to improving computer systems for server applications. EX1005, ¶[0010] (“The computer system can be therefore developed as a server for a plurality of users.”), EX1005, ¶[0076] (“In general, when a computer of a multiprocessor environment is used as a server machine, a plurality of users access the server machine.”); EX1006, 7:51-54 (explaining that Joy’s processor architecture is beneficial for computing applications that are “subject to

frequent context switches” such as “disk server, network server, web server, telecommunications applications and the like”), EX1006, 14:64-67.

79. Joy discloses several benefits associated with using multiple processors on a single integrated circuit die that are applicable to any multiprocessing architecture, including Asano. For example, Joy discloses that “[h]orizontal multithreading or circuit chip multiprocessing *further increases on-chip parallelism by exploiting increasingly smaller processor core sizes*” (EX1006, 7:55-57) and “*further advantageously exploits processor speed and power improvements that inherently result from reduced circuit sizes* in the evolution of silicon processing” (EX1006, 7:36-39). “The combination of vertical multithreading and horizontal multithreading *also advantageously reduces communication latency among local (on-chip) multi-processor tasks by eliminating much signaling on high-latency communication lines between integrated circuit chips.*” EX1006, 7:31-36.

80. Joy’s teaching that processor speed and power improvements inherently result from reducing circuit sizes would further motivate a POSITA to arrange Asano’s processors on a single die. Likewise, Joy teaches that performance-reducing high-latency communication occurs between separate chips. EX1006, 7:31-36. This teaching likewise motivates a POSITA to arrange Asano’s processors on a single die so as to eliminate high-latency communication.

81. Accordingly, it is my opinion that a POSITA would have had reason to consider the teachings of Joy when implementing Asano's system.

82. Moreover, as I discuss below for claim limitation 1.d, Asano discloses that the processor group operates a plurality of operating systems where the system may allocate each processor to another operating system at a predetermined interval of time (e.g., switching between operating systems). *See infra* Section IX.A.1.d; *see also* EX1005 ¶¶[0030]-[0031], [0035]. A POSITA would have thus further recognized that implementing Joy's teachings regarding the multiple processors combined on a single integrated circuit die in Asano would have allowed the combined system to allocate (e.g., via context switching) each processor from an operating system to another operating system at nanosecond speeds. *See, e.g.,* EX1006, 7:49-54. A POSITA facing the wide range of needs created by developments in the technical field of Asano and Joy would have appreciated the benefits of using the multi-threaded, multiple processors mounted on a single die configuration as described in Joy with Asano's system. (*Id.*; *see also supra* Section IX.A.1.b.).

83. For instance, given Asano's system that allows each processor to be allocated to another operating system at a predetermined interval of time (EX1005 ¶[0035]), a POSITA would have appreciated that the benefits associated with using

one or more multiple processors on a single die as discussed by Joy would be similarly applicable to Asano.

84. In addition, it is my opinion that the benefits of having multiple processors on a single die in a multi-processor system (such as the system in Asano) were well known in the art before the '014 patent thereby motivating a POSITA to apply Joy's teachings regarding a single-die multiprocessor to Asano. For example:

- combining processors on a single piece of silicon “outperforms multiple discrete processors by 50% or more” (EX1008, 1) and allows engineers to “take advantage of shorter distances and faster bus speeds when shuttling data between” the processors (*Id.*);
- “[s]ingle-chip multiprocessor architectures have the advantage in that they offer localized implementation of a high-clock rate processor for inherently sequential applications and low latency interprocessor communication for parallel applications.” EX1009, Abstract;
- “[m]ulti-core microprocessors feature a single integrated circuit that includes two or more main processing cores, each of which may be utilized as if it was a separate central processing unit” (EX1010, 1:37-47) and “each of the main cores provides computing power that equals or exceeds that of a conventional high-performance single core processor” (*Id.*);

- “[a]mong the benefits provided by multi-core processors is an increase in physical processing core density within multiprocessor data processing systems, in that more processing cores may operate within a given amount of space, which leads to improvements in overall multiprocessor system performance” (EX1010, 1:48-60); and
- “[t]he key questions for designers of future processors will not be whether to use chip multiprocessing, but the appropriate trade-off between the number of cores and the power of each core” (EX1011, 292).⁴

85. Indeed, the '014 patent acknowledges using multiple processors mounted on a single die in a computer system as conventional and beneficial. For instance, the '014 patent describes a “conventional multiprocessing scheme (shown in FIG. 2) includes a computer system 200 having a chip multiprocessor 295” where “[t]he chip multiprocessor includes multiple processors 210-240 on a single die 290,” which saves space in the computer system. EX1001, 1:34-44, FIG. 2 (illustrating this conventional scheme). Thus, placing Asano’s multiple processors on a single die would have been a common-sense approach.

⁴ To show that claim 1 is obvious, Petitioner relies here on the teachings of Asano and Joy only. Exhibits 1008-1011 demonstrate what a POSITA would have known at the time of the alleged invention of the '014 patent regarding the benefits of having multiple processors on a single die. *Int’l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016).

86. Therefore, based on Joy's disclosure and the knowledge in the art, I believe it would have been obvious for the processor group 110 in the combined Asano-Joy system to be mounted on a single die.

87. Furthermore, using multiple processors mounted on a single die in the above combination would have been a straightforward application of basic computer design principles for designing a multi-processor system, as acknowledged by the '014 patent itself. EX1001, 1:34-42. Such knowledge, coupled with the disclosures/suggestions of Joy, would have motivated a POSITA to use multiple processors mounted on a single die in the Asano system to not only reduce the size of the computer system but also provide accelerated execution of threads based on fast context switching at nanosecond speeds as one benefit of the combination.

88. The combination of Asano with Joy would have involved the use of known technologies (e.g., computer chip architectures for computer systems), design concepts, and processes to obtain the foreseeable result of a computer system utilizing multiple processors mounted on a single die, which would provide fast context switching between executing threads originating from multiple operating systems.

89. A POSITA would have been skilled and knowledgeable to configure Asano's system to implement a system using multiple processors mounted on a

single die while considering any known design and related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. *Id.* For example, a POSITA would have been motivated based on such disclosures to configure Asano's system with CPU group 110 and its multiple processors (11a through 11n) on a single die. *Id.* Thus, a POSITA would have had a reasonable expectation of success in the above modification. *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) ("only a reasonable expectation of success, not a guarantee, is needed" in an obviousness analysis).

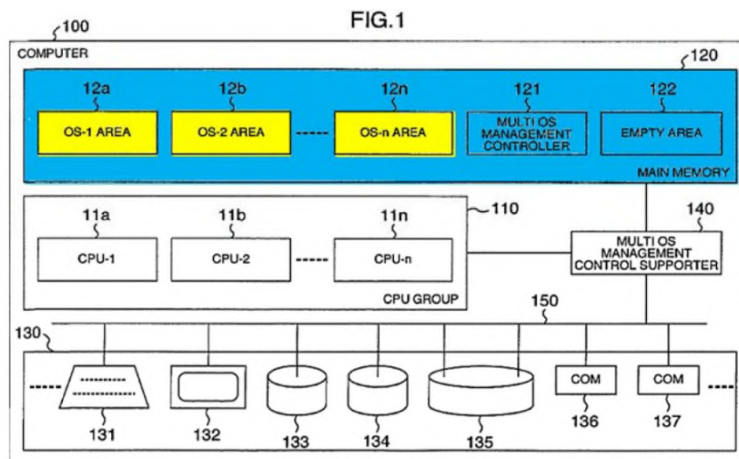
90. Accordingly, it is my opinion that the combination of Asano and Joy discloses and/or suggests "multiple processors mounted on a single die," as claimed.

c) multiple operating systems residing in a memory connected to multiple processors

91. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

92. For example, the combined Asano-Joy system includes multiple processors mounted on a single die ("said multiple processors"). *See supra* Section IX.A.1.b. As discussed below, the combined Asano- Joy system would have included multiple operating systems residing in a memory connected to the multiple processors.

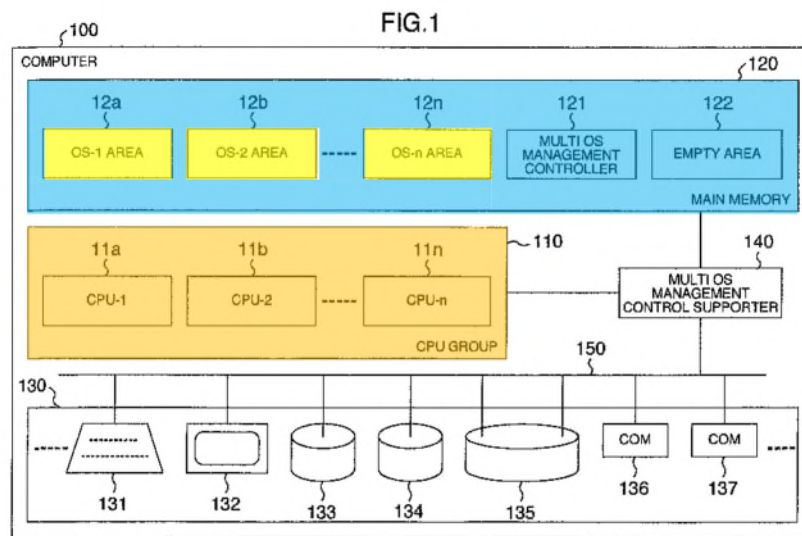
93. For example, Asano discloses that the computer system 100 includes a main memory 120 (“memory”). EX1005, ¶[0030]. The main memory 120 (highlighted blue) “includes main memory areas 12a to 12n” that are “allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n) [highlighted yellow],” as shown in Figure 1 below. EX1005, ¶[0031]. Thus, a POSITA would have understood that the multiple operating systems (e.g., OS-1 to OS-n) reside in memory 120, as claimed.



EX1005, FIG. 1 (annotated).

94. Asano further discloses that the memory 120 is connected to the multiple processors. For example, as illustrated in Figure 1 (below), the computer system 100 includes a bus 150 connecting the processor group 110 (highlighted orange), which includes multiple processors (e.g., CPU-1 to CPU-n), and the main memory 120 (highlighted blue). EX1005, ¶¶[0030]-[0031], FIG.1 (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120, an

external input/output device group 130, a multiple operating system (multi OS) management control supporter 140, and a bus 150 establishing connections between constituent components.”). The system further includes a multiple operating system management (multi-OS) control supporter 140 (EX1005, ¶[0031]) that “allocate[s] computer resources to the operating system.” EX1005, abstract.



EX1005, FIG. 1 (annotated).

95. It is my opinion that the manner in which Asano connects the memory to the multiple processors tracks that described in the '014 patent. For example, the '014 patent explains that each processor is connected with the memory “via a bus.” EX1001, 3:11-14). Asano’s memory and processors are connected in the same manner via bus 150. EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes

a processor group 110, a main memory 120... and a bus 150 establishing connections between the constituent components.”).

96. I believe a POSITA would have thus understood that the multiple operating systems residing in memory 120 are connected to the multiple processors in the processor group 110, as claimed.

97. Furthermore, it is my opinion that a POSITA would have understood that placing the multiple processors on a single chip (*see supra* Section IX.A.1.b) would not have detracted from or changed the connection between the processors and memory in Asano. Indeed, a POSITA would have recognized that in the combined Asano-Joy system, the processor group 110, which comprises multiple processors mounted on a single die, would be connected (e.g., via a bus) to the memory where the multiple operating systems reside.

98. Thus, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

99. Further, to the extent that the Board adopts the narrower agreed-upon construction (“multiple operating systems residing in the same memory”) rather than plain meaning, it is my opinion that the Asano-Joy combination still discloses and/or suggests this limitation.

100. As stated, and shown in Figure 1 above, main memory 120 (highlighted blue) “includes main memory areas 12a to 12n” that are “allocated respectively to

operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n) [highlighted yellow].” EX1005, ¶¶0031. Figure 1 clearly discloses each of the main memory areas 12a-12n that are allocated to the operating systems reside in the same memory – main memory 120. Furthermore, there is no teaching in Asano that would preclude the multiple operating systems from residing in the same memory.

101. Thus, under either construction, I believe that Asano-Joy discloses and/or suggests this limitation.

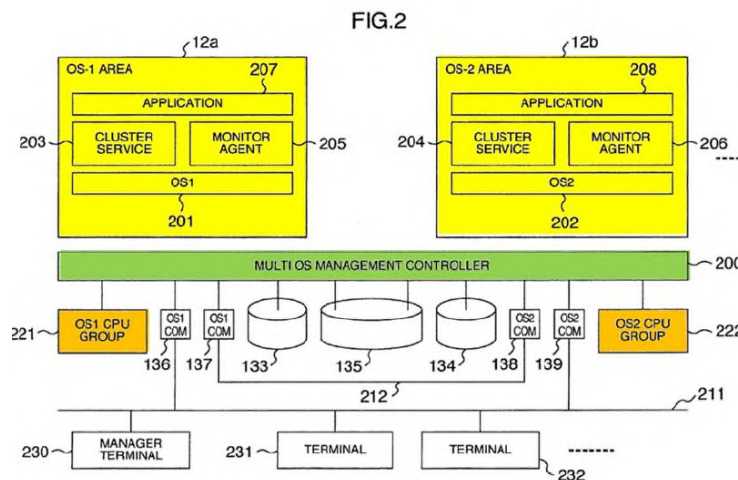
d) wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems

102. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

103. As explained above, the combined Asano-Joy system includes multiple processors mounted on a single die and multiple operating systems connected to these multiple processors. *See supra* Sections IX.A.1.b-c. Each of these processors in the combined Asano-Joy system executes an operating system from the multiple operating systems, whereby two or more of the processors are capable of simultaneously executing two or more of the operating systems.

104. Asano discloses that each of the processors is allocated to execute an operating system. For example, Asano discloses that the computer system 100

includes a processor group 110 that interacts with a multi-OS control supporter 140 to operate (“execute”) a plurality of operating systems, OS-1 to OS-n. *See supra* Section IX.A.1.c; EX1005 ¶¶[0030]-[0031]. Figure 2, reproduced below, further illustrates one configuration of the system shown in Figure 1 where two operating systems, OS-1, OS-2 (highlighted yellow), are simultaneously running on the computer system 100. EX1005, ¶¶[0032]-[0033].



EX1005, FIG. 2 (annotated); *see also* EX1005, ¶[0014] (“FIG. 2 is a block diagram schematically showing a system construction including a cluster configuration of operating systems running in a computer system”).

105. Regarding the configuration shown in Figure 2, Asano further discloses that processor group 110 is divided into two groups (CPU group 221 and 222 (highlighted orange)) via the multi-OS controller (highlighted green). EX1005, ¶¶[0032]-[0033]. These CPU groups are each allocated to run at least one operating system. EX1005, ¶[0032]; *see also* EX1005, ¶[0035]. A POSITA would have

understood that the allocation of the processors to the first and second operating systems would have resulted in processors executing the operating systems. EX1005 ¶[0001] (“a method for controlling a computer system in which a plurality of operating systems (OS) *operate* on one computer”); EX1005, ¶[0035] (explaining that each CPU within a given CPU group may be “allocated to another operating system at a predetermined interval of time”).

106. It is my opinion that Asano further discloses that the “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as claimed.

107. For example, Asano discloses a method of allocating the processors to simultaneously execute multiple operating systems where each CPU within a given CPU group “is allocated to another operating system at a predetermined interval of time.” EX1005, ¶[0035]. Asano further discloses that “the computer resources such as the CPU ... are updated to be allocated to a plurality of operating systems ... according to the states of the operating systems.” *Id.* A POSITA would have understood that this allocation of each of the processors to another operating system is a switching mechanism that provides each processor the capability to switch between multiple operating systems, which are simultaneously running in the system. The '014 patent describes a similar process, where “[e]ach processor may be ... capable of simultaneously executing multiple operating systems, for example,

by context switching, which may include rapidly switching between multiple operating systems.” EX1001, 3:46-51; EX1005, ¶[0035]

108. It is my opinion that Asano removes any question that multiple operating systems are executed simultaneously.

109. In one example, Asano describes that the system may “include[] two operating systems in which a first operating system operates as an active system and a second operating system operates as a standby system.” EX1005, ¶[0035]. Figure 3, reproduced below, illustrates an exemplary allocation of computer resources such that the system executes two operating systems simultaneously, (OS-1 and OS-2), on the processors (highlighted in yellow). EX1005, FIG. 3. Asano explains that in this exemplary allocation of computer resources, the system has allocated “95% of the CPU resources ... to the active OS-1 and 5% thereof are allocated to the standby OS-2.” EX1005, ¶[0036]-[0037].

FIG.3

300 COMPUTER STATE TABLE

310 COMPUTER RESOURCE ALLOCATION TABLE

311 COMPUTER RESOURCE NAME	312 ACTIVE COMPUTER RESOURCE SERVICE RATIO	313 STANDBY COMPUTER RESOURCE SERVICE RATIO
CPU	95%	5%
MAIN MEMORY		

320 OS STATE TABLE

321 OS NAME	322 STATE	323 ACTIVE,STANDBY	324 CPU
OS 1	OPERATING	ACTIVE	95%
OS 2	OPERATING	STANDBY	5%

EX1005, FIG. 3 (annotated). Thus, even in standby state, 5% of CPU resources is allocated to executing OS2. A POSITA would have understood that Asano contemplates achieving such division of CPU resources by having “each CPU . . . allocated to another operating system at a predetermined interval of time.” EX1004, ¶[0035].

110. Moreover, based on Asano’s teachings, I believe a POSITA would understand that any other allocation is possible, including one where the resource allocation between OS1 and OS2 is equal, for example. For example, Fig. 7 of Asano shows a computer resource update state table for operating systems OS1 through OSn while Fig. 8 shows a flow chart for updating the “processing procedure for each operating system to update computer resources.” EX1005, ¶¶[0053]-[0054]. The procedure includes comparing the current loads of multiple operating

systems and adjusting computing resources, indicating to a POSITA that the operating systems are executing simultaneously and generating differing loads on the computer resources. EX1005, ¶¶[0054]-[0063]. A POSITA would understand that any combination of workloads and resource allocations are possible between these simultaneously executing operating systems. For example, the Asano operating systems could split the resource allocation equally. In another example, one operating system could have a heavy load relative to others as illustrated in step 801 of Figure 8 and obtain additional resources at steps 808-810. *See id.*

111. Further, to the extent that the Board adopts the agreed-upon District Court construction of “simultaneously executing two or more operating systems” as “simultaneously executing two or more independent operating systems,” it is my opinion that Asano likewise teaches this limitation. In particular, Asano clearly shows that OS-1 and OS-2 are separate and distinct operating systems in Figure 1. Asano further explicitly discloses operating a plurality of OSs independent of each other. EX1005, claim 9 (“operating the operating systems independent of each other”). As another example, the dynamic computer resource update process discussed above demonstrates to a POSITA that each operating system is operating independently with different loads.

112. Thus, it is my opinion that Asano teaches this limitation under any construction.

113. For similar reasons, it is my opinion that the Asano-Joy combined system would have been configured such that each of the multiple processors in the single die executes an operating system from the multiple operating systems, and two or more of the multiple processors in the single die are capable of simultaneously executing two or more operating systems, as claimed. *See supra* Section IX.A.1.b. A POSITA would have understood that placing the multiple processors on a single chip (as discussed above in Section IX.A.1.b) would not have detracted from or changed the desirability of executing operating systems in this way, as taught in Asano. On the contrary, as explained above, Joy's multiple processors mounted on a single die enhances the ability (e.g., via context switching) for each processor to execute simultaneously two or more threads by switching at nanosecond speeds, thus further facilitating the simultaneous execution of multiple independent operating systems. *See supra* Section IX.A.1.b; EX1006, 7:9-14, 21-27, 45-54, FIG. 2C.

114. Accordingly, I believe that a POSITA would have understood that the system in the Asano-Joy combination includes both the software and hardware to allocate each processor to another operating system by rapidly switching each or some of the processors between multiple operating systems.

115. Thus, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

2. Claim 3

a) The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems

116. It is my opinion that Asano-Joy combination discloses and/or suggests this limitation.

117. As discussed for claim 1, Asano discloses that the multiple processors are connected to the memory to execute the operating systems. *See supra* Sections IX.A.1.c-d. Asano further discloses that the computer system 100 establishes connections between the processor group 110 and main memory 120 via a bus 150. EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120, an external input/output device group 130, a multi-OS control supporter 140, and *a bus 150 establishing connections between the constituent components.*”); *see also* EX1005, ¶[0031] (similar).

118. Accordingly, I believe a POSITA would have understood that the system in the Asano-Joy combination would have included a bus that connects the multiple processors mounted on a single die with the main memory 120 to execute instructions from the various operating systems and process data.

119. Thus, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

120. Further, to the extent that the Board adopts the agreed-upon District Court construction (“multiple processors are connected to said memory via the same bus”), it is my opinion that the Asano-Joy combination likewise discloses and/or suggests this limitation.

121. Asano teaches that the computer system 100 “includes a processor group 100, a main memory 120... and a bus 150 connecting the constituent components to each other as shown in Fig. 1.” EX1005, ¶0031], FIG.1. Accordingly, the same bus 150 connects the multiple processors CPU1-CPU_n to main memory 120. Furthermore, there is no teaching in Asano that would preclude the multiple processors from being connected to the memory via the same bus.

122. Accordingly, even under PO’s narrower interpretation, it is my opinion that the Asano-Joy combination still discloses and/or suggests this limitation.

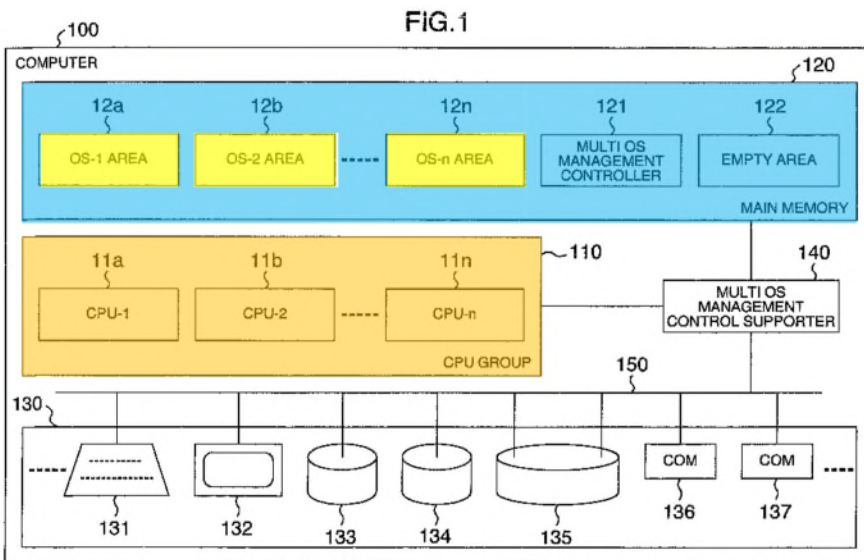
3. Claim 5

a) The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems

123. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

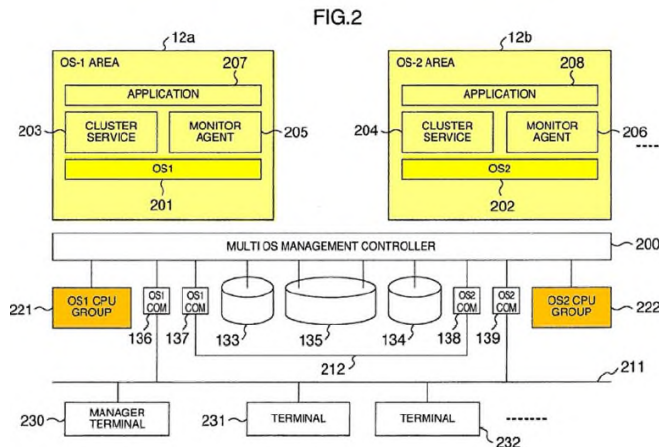
124. For example, Asano discloses a computer system, as shown in Figure 1 below, that includes a processor group 110 (highlighted orange) for executing a

plurality of operating systems and multiple separate operating system areas, OS-1 through OS-n area (highlighted yellow). *See supra* Section IX.A.1.a-d. Asano further explains that “the operating systems may differ from each other.” EX1005 ¶[0045] (“However, the operating systems may differ from each other. It is only necessary that each operating system can execute processing of the same applications.”). Accordingly, I believe a POSITA would have understood that the combined Asano-Joy system executes “distinct operating system[s]” because each operating system executed in the system is a separate operating system (e.g., each OS is located in separate areas in memory (OS-1 area to OS-n area)) and each of these operating systems may differ from each other.



EX1005, FIG. 1 (annotated).

125. Asano further describes that “each of said processors executes a distinct operating system of said multiple operating systems.” For example, regarding Figure 2 (below), Asano discloses an exemplary configuration when two operating systems (i.e., OS-1, OS-2), highlighted yellow, are running in the system. EX1005, ¶[0032]. Each operating system has a processor group allocated to it, which are highlighted in orange, i.e., “CPU group 221 allocated to OS-1 and the CPU Group 222 is allocated to OS-2.” EX1005, ¶[0030].



EX1005, FIG. 2 (annotated).

126. Asano further discloses and/or suggests a configuration where each of the processors in the processor group 110 is executing a distinct operating system from the multiple operating systems (e.g., OS1 (201) in 12a and OS2 (202) in 12b).

127. For example, Asano discloses that the processor group 110 may include one or more processors. EX1005, ¶[0031]. Asano further explains that each processor group (e.g., 11a in OS1 CPU group 221 and 11b in OS2 CPU group 222)

may be allocated to separate operating systems (e.g., OS1, OS2, respectively). EX1005, ¶[0035]. A POSITA would have thus understood Asano to teach that the processor group 110 could include two processors (e.g., 11-a and 11-b) and that the system assigns a single processor to each CPU group (e.g., OS1 CPU group 221 and OS2 CPU group 222). To this end, each of the processors, 11a and 11b, could be assigned to run distinct operating systems (OS-1 and OS-2, respectively)—i.e., in this scenario, each processor, 11-a and 11-b, executes a separate (“distinct”) operating system. EX1005, ¶[0035], FIG. 2. Accordingly, it is my opinion that Asano discloses the claimed “wherein each of said processors executes a distinct operating system of said multiple operating systems.”

128. At a minimum, it is my opinion that it would have been obvious to a POSITA to make use of two processors, with each processor executing a distinct operating system, in view of the teachings of Asano. Asano recognizes that processor group 110 may include one or more processors and specifically contemplates a processor 11-a and 11-b. EX1005, ¶[0031]. Moreover, Asano teaches the assignment of different processors to different operating systems. EX1005, ¶[0035]. I believe a POSITA would have recognized that, while Asano provides one example where two processors are assigned to each operating system (*Id.*), the number of processors assigned to a given operating system is a design choice, and, depending on the resources available (e.g., the number of processors

available), a single processor could be allocated to a given operating system instead. A POSITA would have recognized Asano to suggest exactly this by disclosing that “n” processors are available and that Asano’s process would have operated in the same way regardless of the number of processors assigned to an operating system. A POSITA also would have had a reasonable expectation of success in performing such an implementation.

129. Thus, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

4. Claim 7

a) A multiprocessing system comprising:

130. To the extent that the preamble of claim 7 is limiting, it is my opinion that Asano discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section IX.A.1.a; *infra* Section IX.A.6.b-d.

b) a plurality of processor groups mounted on a single die

131. This claim limitation 7.b varies from limitation 1.b in that it recites “groups” while claim limitation 1.b does not. *See supra* Section IX.A.1.b.

132. It is my opinion that the Asano-Joy combination discloses claim limitation 7.b for at least the same reasons discussed above from claim limitation 1.b because each of the processors in the processor group 221, which would have

been processors on a single die, are allocated into a plurality of groups.⁵ *See supra* Sections IX.A.1.b; *see also* EX1005, ¶[0035] (Asano discloses as an exemplary arrangement where CPU group 221 has been allocated “CPU-1 and CPU-2” and CPU group 222 has been allocated “CPU-3 and CPU-4 of the CPU group 110.”).

133. Thus, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

c) multiple operating systems residing in a memory connected to said groups

134. This claim limitation 7.c varies slightly from claim limitation 1.c in that it recites “groups” while claim limitation 1.c does not. *See supra* Section IX.A.1.c.

135. It is my opinion that the Asano-Joy combination discloses claim limitation 7.c for at least the same reasons discussed above from claim limitation 1.c. *See supra* Section IX.A.1.c.

136. Thus, I believe the Asano-Joy combination discloses and/or suggests this limitation.

⁵ '014 claim 8, which depends on claim 7, recites “wherein each of said groups includes multiple processors,” indicating that claim 7 is not limited to groups of multiple processors. EX1001, claim 8.

d) wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems

137. Claim limitation 7.d varies slightly from claim limitation 1.d in that it recites “groups” while claim limitation 1.d does not. *See supra* Section IX.A.1.d.

138. It is my opinion that the combined Asano-Joy system discloses limitation 7.d for at least the same reasons discussed above from claim limitation 1.d. *See supra* Sections IX.1.2.d.

139. Thus, I believe the Asano-Joy combination discloses and/or suggests this limitation.

5. Claim 11

a) The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems

140. Claim 11 varies slightly from claim 5 (“wherein each of said processors executes a distinct operating system of said multiple operating systems”) in that it recites “groups” while claim 5 does not. *See supra* Section IX.A.3.

141. It is my opinion that the combined Asano-Joy system discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section IX.A.3.

6. Claim 12

a) A multiprocessing apparatus comprising:

142. To the extent that the preamble of claim 7 is limiting, it is my opinion that the Asano- Joy combination discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section IX.A.1.a; *see infra* Section IX.A.10.b-d.

b) processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die

143. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitations 1.b, 1.d, and for the additional reasons provided below. *See supra* Sections IX.A.1.b, IX.A.1.d.

(1) operating system means

144. It is my opinion that the Asano-Joy combination discloses and/or suggests an “operating system means,” as claimed. *See supra* Section VIII.E (construction of “operating system means” as a conventional operating system, such as WINDOWS NT, UNIX, and the like, or equivalents thereof).

145. For example, Asano’s system includes operating systems, e.g., operating system 1 (OS-1) to operating system n (OS-n). *See supra* Section IX.A.1.c; EX1005, ¶¶[0031], [0045] (Asano disclose that “each operating system

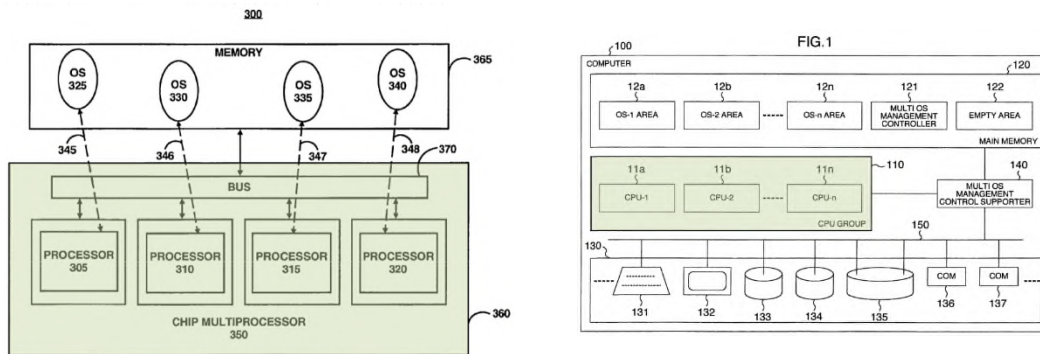
can execute processing of the same applications”), Abstract, FIG. 1. Thus, a POSITA would have understood that the operating systems in the combined Asano-Joy system are “operating system means,” as claimed because these operating systems support the Asano-Joy system with various functions, such as executing applications and processing of data, and thus acts like a conventional operating system. EX1005 ¶¶[0002] (“The technique is called ‘cluster system’ in which when an operating system running on a computer fails, another operating system receives processing of the failed operating system to continue the processing. In the system of the background art, at a failure of an operating system on a computer, programs running on the computer can be continuously executed.”), [0008], [0045].

(2) processor means

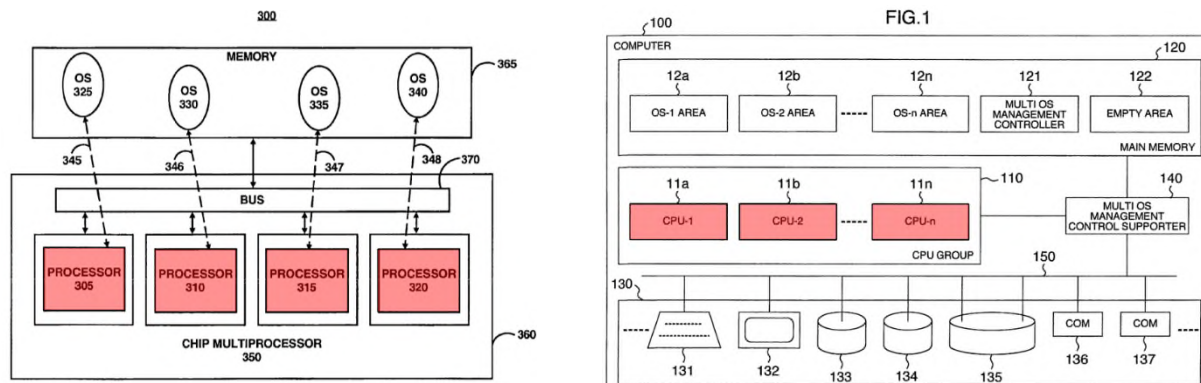
146. It is my opinion that the Asano-Joy combination discloses and/or suggests a “processor means,” as claimed. *See supra* Section VIII.D (construction of “processor means”). For example, the combined Asano-Joy system includes a processor group 110, which is a chip multiprocessor that consists of two or more processors (e.g., processors 11a, 11b . . . , 11n.). *See supra* Section IX.A.1.b; EX1005 ¶¶[0031]. I believe a POSITA would have thus understood that processor group 110 in the combined Asano-Joy system includes a plurality of processors mounted on a single die.

147. Further, to the extent the Board adopts the agreed-upon District Court construction, it is my opinion that the Asano-Joy combination still discloses this limitation.

148. With regard to the claimed structure, as shown below, the '014 Patent discloses chip multiprocessor 350 (left, green). Similarly, Asano discloses a chip multiprocessor (right, green).

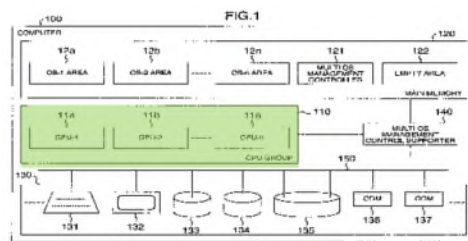
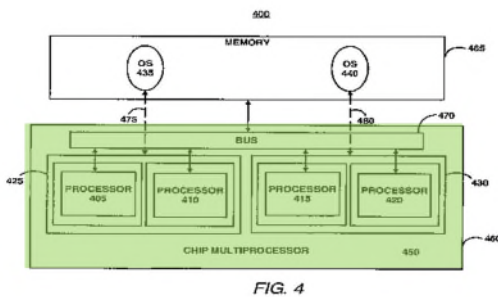


149. The '014 Patent discloses that chip multiprocessor 350 includes four processors 305-320 (left, red). Similarly, Asano discloses that CPU group 110 can include n number of CPUs, such as CPU-1 11a, CPU-2 11b, all the way up through CPU-n 11n (right, red).

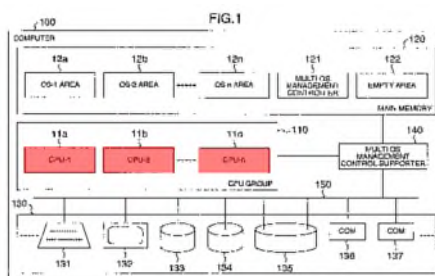
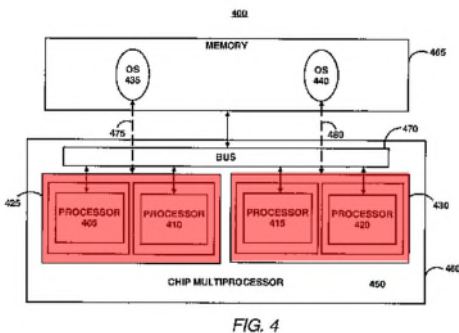


150. Further, as indicated in Section IX.A.1.b, it would be obvious to modify Asano's teachings with Joy to have CPU-1 through CPU-n be mounted on a single die.

151. As shown below, the '014 Patent discloses chip multiprocessor 450 (left, green). Similarly, Asano discloses a chip multiprocessor (right, green).



152. The '014 Patent discloses that chip multiprocessor 450 has multiple processors 405-420 (left, red). Similarly, Asano discloses that CPU group 110 can include *n* number of CPUs, such as CPU-1 11a, CPU-2 11b, all the way up through CPU-n 11n (right, red).



153. Further, as indicated in Section IX.A.1.b, it would be obvious to modify Asano's teachings with Joy to have CPU-1 through CPU-n be mounted on a single die.

154. Thus, to the extent “processor means” is construed under the agreed-upon construction, it is my opinion that the Asano-Joy combination still teaches this limitation.

155. Furthermore, as discussed above, the combined Asano-Joy system discloses that the processor group 110, which is a chip multiprocessor, executes a plurality of operating systems from the multiple operating systems (OS-1 through OS-n) thereby performing the claimed function. *See supra* Sections IX.A.1.a, IX.A.1.d; EX1005, ¶¶[0030]-[0031], FIGS. 1-2; *see also* EX1005, ¶[0001] (“The present invention relates to a computer system and a method for controlling *a computer system in which a plurality of operating systems (OS) operate on one computer*, and in particular, to a computer system and a method for controlling a computer system in which computer resources can be efficiently used or operated in an operating state of a plurality of operating systems”);

156. Accordingly, it is my opinion that the Asano-Joy combination discloses and/or suggests this limitation.

c) and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means

157. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.d. *See supra* Section IX.A.1.d;

d) memory means for storing said plurality of operating system means

158. It is my opinion that the Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.c and for the additional reasons explained below. *See supra* Section IX.A.1.c.

159. The Asano-Joy combination discloses and/or suggests a “memory means for storing said plurality of operating system means” as claimed. *See supra* Section VIII.F.

160. The '014 patent identifies as corresponding structure “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” *See supra* Section VIII.F. The Asano-Joy combination discloses and/or suggests this structure. For example, Asano’s system includes a main memory 120 that includes distinct areas, 12a to 12n, for storing operating systems (e.g., OS-1 through OS-n). *See supra* Section IX.A.1.c; EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120,”), ¶[0031] (“The main memory 120 includes main memory areas 12 a to 12 n independent of each other. The areas 12 a to 12 n are allocated respectively to operating systems, i.e., operating system 1 (OS-1) to

operating system n (OS-n). The main memory 120 further includes a main storage area 121 for the multiple operating system management controller and an empty area 122 to be reserved.”), ¶[0032] (“The external storage 133 is allocated to OS-1, the external device 134 is allocated to OS-2, the disk device 135 is shared between OS-1 and OS-2”).

161. It is my opinion that a POSITA would understand that “main memory 120” is a conventional computer memory and can be construed to include any of “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.”

162. To the extent the Asano’s main memory is not found to explicitly teach the sort of memory defined above in Section VIII.F, I believe it would have at a minimum been a mere obvious design choice to make use of such conventional memory. For example, the use of magnetic media, optical media, random access memory (RAM), and read-only memory (ROM) were well-known and conventional options for memory. *See, e.g.*, EX1015, 5:60-66 (explaining that operating systems are typically held in storage devices such as magnetic or optical disk drives); EX1016, 5:39-43 (explaining that operating systems may be stored in storage

devices such as a “hard disk, magnetic disk 48, optical disk 52, ROM 38, or RAM 40”).⁶

163. Further, should there be any doubt that main memory 120 can be construed in this manner, Joy explicitly discloses an “on-chip L2 cache SRAM 1124,” in its a single-chip dual-processor vertically-threaded processor 1100 design. The SRAM 1124 is “shared between the first vertical multithreading processor 1102 and the second vertical multithreading processor 1104.”

164. Thus, it is my opinion that the Asano-Joy combination discloses the corresponding structure.

165. Furthermore, as discussed above, the combined Asano-Joy system discloses that main memory 120 that includes distinct areas, 12a to 12n, for storing operating systems (e.g., OS-1 through OS-n) thereby disclosing the claimed function. *See supra* Section IX.A.1.c.

166. Accordingly, it is my opinion that the Asano-Joy combination discloses this limitation.

⁶ I rely on the teachings of Asano and Joy only for the limitations of claim 1. Exhibits 1015-1016 demonstrate what a POSITA would have known at the time of the alleged invention of the '014 patent regarding well-known and conventional types of memory useful for storing operating systems.

7. Claim 13

a) The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems

167. Claim 13 varies slightly from claim 3 (“wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems”) in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section IX.A.2. As I discuss above, the Asano-Joy combination discloses a “processor means” (*see supra* Section IX.A.6.b) and “memory means” (*see supra* Section IX.A.6.d).

168. Accordingly, it is my opinion that the combined Asano-Joy system discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section IX.A.2.

8. Claim 15

a) The apparatus of claim 12, wherein each of said processors of said processing means is operable to execute a distinct one of said plurality of operating system means

169. Claim 15 varies slightly from claim 5 in that it recites a “processor means” and “memory means” while claim 5 does not. *See supra* Section IX.A.3. As I discussed above, the combined Asano-Joy system discloses a “processor means.” *See supra* Section IX.A.6.b.

170. Accordingly, it is my opinion that the combined Asano-Joy system discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section IX.A.3.

B. Ground 2: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Asano and Babaian⁷

171. It is my opinion that the combination of Asano and Babaian renders claims 1, 3, 5, 7, 11-13, and 15 obvious.

1. Claim 1

a) Limitation 1.a

172. It is my opinion that Asano discloses this limitation. *See supra* Section IX.A.1.a.

b) Limitation 1.b

173. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

174. Asano discloses a computer system that includes a processor group that includes multiple processors, but Asano does not disclose “multiple processors mounted on a single die” as claimed. *See supra* Section IX.A.1.b.

⁷ The subheadings in Section IX.A provide the claim language for all corresponding claims and claim limitations in Section IX.B

175. To the extent that Asano does not explicitly provide that the multiple processors are mounted on a single die, I believe Babaian teaches doing so. Specifically, Babaian discloses multiple processor mounted on a single die. For example, Babaian discloses “a Single-chip Multiprocessor System 700 suited for parallel execution” that includes “four processors 710.” EX1007, 7:1-5.

176. Specifically, Babaian discloses multiple processors mounted on a single die. For example, Babaian discloses a horizontal threaded processor architecture that “combines multiple processors on a single integrated circuit die.” EX1006, 7:4-6.

177. It is my opinion that a POSITA would have been motivated in light of Babaian to configure the system in Asano (as discussed above for claim limitation 1.a) so that its multiple processors are “mounted on a single die,” as claimed. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. See KSR, 550 U.S. at 416-18. A POSITA would have recognized that Babaian and Asano disclose features in a similar technological field. Accordingly, I believe that a POSITA would have had reason to consider the teachings of Babaian when implementing Asano’s system, given that Babaian discloses the benefits of using multiple processors mounted on a single die in a computer system like the system disclosed in Asano.

178. Babaian discloses several advantages of using a single chip multiprocessor that are applicable to any multiprocessing architecture, including Asano. For example, Babaian explains that “[t]he single chip multiprocessor system substantially increases the performance due to parallel and macro-scheduled execution of a multitude of program streams, high performance and efficiently synchronized data exchange between the processors.” EX1007, 4:31-36. Babaian also explains that only a “few single-chip multiprocessor systems 700” are needed to provide a large multiprocessor system with “tens or hundreds of processors.” EX1007, 7:34-39.

179. Babaian’s teaching of performance improvements inherently result from parallel and macro-scheduled execution of a multitude of program streams inherently result from a single chip multiprocessor would further motivate a POSITA to arrange Asano’s processors on a single die. Likewise, Asano teaches that positioning multiple processors on a single die results in high performance and efficiently synchronized data exchange between the processors. EX1007, 4:32-35. This teaching likewise motivates a POSITA to arrange Asano’s processors on a single die so as to improve performance and efficiency of data exchange between processors.

180. Accordingly, it is my opinion that a POSITA would have had reason to consider the teachings of Babaian when implementing Asano’s system.

181. Further, as discussed below for claim limitation 1.d, Asano discloses that the processor group operates a plurality of operating systems where the system may allocate each processor to another operating system at a predetermined interval of time (e.g., switching between operating systems). *See infra* Section IX.B.1.d; *see also supra* Section IX.A.1.d; EX1005 ¶¶[0030]-[0031], [0035]. I believe that a POSITA would have thus recognized that implementing Babaian's teachings regarding the multi-processor on a single die configuration with the system in Asano would have allowed the combined system to allocate each processor quickly (via the flexible assignment of each processor) to another operating system. *See infra* Section IX.B.1.d; EX1005 ¶[0035] ("Each CPU is allocated to another operating system at a predetermined interval of time."); EX1007, 13:65-14:3. A POSITA facing the wide range of needs created by developments in the technical field of Asano and Babaian would have appreciated the benefits of using the single chip multiprocessor configuration as described in Babaian in Asano's system. Indeed, a POSITA would have appreciated that the benefits associated with assigning one or more multiple processors on a single die, as discussed by Babaian, would be similarly applicable to Asano. *See supra* Section IX.B.1.b(1); EX1007, 3:56-62, 4:8-36. For example, a POSITA would have immediately recognized that mounting multiple processors on a single die in the Asano multiprocessor system would have increased the system's performance substantially when executing programs,

improved the efficiency of data exchange between processors on the same die, and reduced the number of chips needed to implement a multiprocessor system. EX1007, 4:31-35.

182. In addition, the benefits of having multiple processors on a single die in a multi-processor system (such as the system in Asano) were well known in the art before the '014 patent thereby further motivating a POSITA to apply Babaian's teachings regarding a single chip multiprocessor to Asano. EX1007, 7:34-39; EX1008, 1; EX1009, Abstract; EX1010, 1:37-47; EX1011, 292.⁸ Thus, placing Asano's multiple processors on a single die would have been a common-sense approach.

183. Therefore, based on Babaian's disclosure and the knowledge in the art, I believe it would have been obvious for the processor group 110 in the combined Asano-Babaian system to be mounted on a single die. Furthermore, using multiple processors mounted on a single die in the above combination would have been a straightforward application of basic computer design principles for designing a multi-processor system, as acknowledged by the '014 patent itself. EX1001, 1:34-

⁸ To show that claim 1 is obvious, Petitioner relies here on the teachings of Asano and Babaian only in Section IX.B. EX1008-1011 demonstrate what a POSITA would have known at the time of the alleged invention of the '014 patent regarding the benefits of having multiple processors on a single die.

42. Such knowledge, coupled with the disclosures/suggestions of Babaian, would have motivated a POSITA to use multiple processors mounted on a single die in the Asano system to not only reduce the size of the computer system but also provide flexible assignment of the processors for the execution of multiple operating systems as one benefit of the combination.

184. The combination of Asano with Babaian would have involved the use of known technologies (e.g., computer chip architectures for computer systems), design concepts, and processes to obtain the foreseeable result of a computer system utilizing multiple processors mounted on a single die, which would provide fast switching between executing threads originating from multiple operating systems. A POSITA would have been skilled and knowledgeable to configure Asano's system to implement a system using multiple processors mounted on a single die while considering any known design and related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. For example, a POSITA would have been motivated based on such disclosures to configure Asano's system where the CPU group 110 includes multiple processors (11a through 11n) on a single die. Thus, a POSITA would have had a reasonable expectation of success in the above modification. *See Pfizer*, 480 F.3d at 1364.

185. Accordingly, it is my opinion that the combination of Asano and Babaian discloses and/or suggests this limitation.

c) Limitation 1.c

186. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

187. For example, Asano discloses that the computer system 100 includes multiple operating systems (e.g., OS-1 to OS-n) that reside in the main memory connected to the processor group that includes multiple processors. *See supra* Section IX.A.1.c. Accordingly, for reasons similar to those explained above, the Asano-Babaian combined system would have been further configured such that multiple operating systems reside in a memory, which is connected to the multiple processors mounted on a single die, as claimed. *See supra* Section IX.B.1.b.

188. Furthermore, I believe a POSITA would have understood that placing the multiple processors on a single chip would not have detracted from or changed the connection between the processors and memory in Asano.

189. Thus, it is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

d) Limitation 1.d

190. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

191. Asano discloses that each of the processors in the processor group is allocated to execute an operating system. *See supra* Section IX.A.1.d. Asano

further discloses that each processor in the group includes a switching mechanism that provides capability for the processor to switch between multiple operating systems, where the operating systems are simultaneously running in the system. *See supra* Section IX.A.1.d; EX1005 ¶[0035].

192. Accordingly, for reasons similar to those explained above regarding Asano's disclosures, I believe that the Asano-Babaian combined system would have been further configured such that each of the multiple processors in the single die executes an operating system from the multiple operating systems, and two or more of the multiple processors in the single die are capable of simultaneously executing two or more operating systems, as claimed. *See supra* Sections IX.A.1.d, IX.B.1.b.

193. Additionally, as explained above, Babaian's multiple processors mounted on a single die include the ability for each processor to be flexibly assigned for execution of a task. *See supra* Section IX.B.1.b; *see also* EX1007, 13:65-14:3. Accordingly, I believe a POSITA would have understood that the combined Asano-Babaian system includes both the software and hardware to allocate each processor to another operating system by flexible assignment of each of the processors between multiple operating systems.

194. Thus, it is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

2. Claim 3

195. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

196. Asano discloses that the multiple processors are connected to memory via a bus in order to execute the multiple operating systems. *See supra* Section IX.A.2. Accordingly, I believe a POSITA would have understood that the system in the Asano-Babaian combination would have included a bus that connects the multiple processors mounted on a single die with the main memory in order to execute instructions from the various operating systems and to process data.

3. Claim 5

197. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation.

198. For example, Asano discloses a configuration where each of the processors in the processor group executes a distinct operating system. *See supra* Section IX.A.3. Accordingly, I believe a POSITA would have understood that the system in the Asano-Babaian combination would have also included such a configuration.

4. Claim 7

a) Limitation 7.a

199. To the extent that the preamble of claim 7 is limiting, it is my opinion that the Asano-Babaian combination discloses the limitations of this preamble for at least the reasons as above for claim limitation 1.a. *See supra* Sections IX.B.1.a; *see infra* Section IX.B.6.b-d.

b) Limitation 7.b

200. This limitation 7.b varies from limitation 1.b in that it recites “groups” while limitation 1.b does not. *See supra* Section IX.B.1.b.

201. It is my opinion that the combined Asano- Babaian system discloses limitation 7.b for at least the same reasons discussed above from limitation 1.b because each of the processors in the processor group 221, which would have been processors on a single die, are allocated into a plurality of groups. *See supra* Sections IX.B.1.b, IX.B.5.

c) Limitation 7.c

202. This limitation 7.c varies from limitation 1.c in that it recites “groups” while limitation 1.c does not. *See supra* Section IX.B.1.c.

203. It is my opinion that the combined Asano-Babaian system discloses limitation 7.c for at least the same reasons discussed above from limitation 1.c. *See supra* Section IX.B.1.c.

d) Limitation 7.d

204. This limitation 7.d varies from limitation 1.d in that it recites “groups” while limitation 1.d does not. *See supra* Section IX.B.1.d.

205. It is my opinion that the combined Asano-Babaian system discloses limitation 7.d for at least the same reasons discussed above from limitation 1.d. *See supra* Sections IX.B.1.d, IX.B.5.

5. Claim 11

206. Claim 11 varies from claim 5 in that it recites “groups” while claim 5 does not. *See supra* Section IX.B.3.

207. It is my opinion that the combined Asano-Babaian system discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section IX.B.3.

6. Claim 12

a) Limitation 12.a

208. To the extent that the preamble of claim 12 is limiting, it is my opinion that the Asano-Babian combination discloses the limitations of this preamble for at least the reasons as above for limitation 1.a. *See supra* Section IX.B.1.a; *infra* Sections IX.B.10.b-d.

b) Limitation 12.b

209. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from

limitations 1.b, 1.d and limitation 12 in Ground 1. *See supra* Sections IX.A.6.b, IX.B.1.b, IX.B.1.d.

210. For example, for the same reasons as explained above for claim limitation 12 in Ground 1, the combined Asano-Babaian system would have included an operating system means (i.e., operating system 1 (OS-1) to operating system n (OS-n)). *See supra* Section IX.A.6.b.

211. Furthermore, as discussed above for claim limitation 12 in Ground 1, the combined Asano-Babaian system would have also included a processor means. *See supra* Section IX.A.6.b.

c) Limitation 12.c

212. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.d and claim limitation 12 from Ground 1. *See supra* Sections IX.A.6.c, IX.B.1.d.

d) Limitation 12.d

213. It is my opinion that the Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.c and claim limitation 12 from Ground 1. *See supra* Sections IX.A.6.d, IX.B.1.c.

7. Claim 13

214. Claim 13 varies from claim 3 in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section IX.B.2.

215. As discussed for limitations 12.b and 12.d, the combined Asano-Babaian system discloses a “processor means” (*see supra* Section IX.B.6.b) and “memory means” (*see supra* Section IX.B.6.d).

216. Accordingly, it is my opinion that the combined Asano-Babaian system discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section IX.B.2.

8. Claim 15

217. Claim 15 varies from claim 5 in that it recites a “processor means” and “memory means” while claim 5 does not. *See supra* Section IX.B.3.

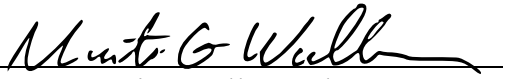
218. As discussed for claim limitation 12.b, the combined Asano-Babaian system discloses a “processor means.” *See supra* Section IX.B.6.b.

219. Accordingly, it is my opinion that the combined Asano-Babaian system discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section IX.B.3.

X. CONCLUSION

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 5 Apr 2023

By: 
Martin Walker, PhD.