

DOCKET NO.: 337722-000265

Filed on behalf of Apple Inc.

By: Joseph Wolfe, Reg. No. 73,173
James Heintz, Reg. No. 41,828

DLA Piper LLP (US)
1650 Market Street, Suite 5000
Philadelphia, PA 19103

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,

Petitioner

v.

SONRAI MEMORY LIMITED,

Patent Owner

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 6,874,014**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES	1
A.	Real Party-in-Interest	1
B.	Related Matters.....	1
C.	Counsel	2
D.	Service Information, Email, Hand Delivery, and Postal.....	2
III.	CERTIFICATION OF GROUNDS FOR STANDING	2
IV.	OVERVIEW OF CHALLENGE AND RELIEF REQUESTED.....	3
A.	Prior Art Patents and Printed Publications.....	3
B.	Grounds for Challenge	4
V.	OVERVIEW OF THE '014 PATENT AND THE PRIOR ART	4
A.	Summary of the Alleged Invention	4
B.	Level of Ordinary Skill in the Art.....	7
C.	Prosecution History	7
D.	Overview of Asano.....	8
E.	Overview of Joy	10
F.	Motivation to Combine Asano and Joy.....	12
G.	Overview of Babaian.....	14
H.	Motivation to Combine Asano and Babaian	16
VI.	CLAIM CONSTRUCTION	17
A.	"simultaneously executing two or more operating systems"	18
B.	"multiple operating systems residing in a memory"	18
C.	"multiple processors are connected to said memory via a bus".....	18
D.	"processor means" in claim 12.....	19
E.	"operating system means" in claim 12.....	19
F.	"memory means" in claim 12.....	20
VII.	SPECIFIC GROUNDS FOR PETITION	20
A.	Ground 1: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Asano and Joy.....	20

1.	Claim 1	21
2.	Claim 3	41
3.	Claim 5	43
4.	Claim 7	47
5.	Claim 11	49
6.	Claim 12	50
7.	Claim 13	58
8.	Claim 15	59
B.	Ground 2: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Asano and Babaian	59
1.	Claim 1	59
2.	Claim 3	68
3.	Claim 5	68
4.	Claim 7	69
5.	Claim 11	70
6.	Claim 12	70
7.	Claim 13	72
8.	Claim 15	72
VIII.	DISCRETIONARY DENIAL IS NOT APPROPRIATE	73
A.	<i>General Plastic</i> Denial is Inappropriate	73
B.	<i>Fintiv</i> Discretionary Denial is Inappropriate	73
1.	<i>Fintiv</i> Factor 1: Institution Will Enable a Stay	74
2.	<i>Fintiv</i> Factor 2: District Court Schedule	74
3.	<i>Fintiv</i> Factor 3: Parallel Proceeding Considerations	76
4.	<i>Fintiv</i> Factor 4: The Petition Raises Unique Issues	77
5.	<i>Fintiv</i> Factor 5: The Petition Will Enable Cancellation of Claims that Might Be Reasserted	77
6.	<i>Fintiv</i> Factor 6: Other Considerations Support Institution	78
IX.	CONCLUSION	79

I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for *inter partes* review of U.S. Patent No. 6,874,014 (“’014 patent”) (EX1001). The ’014 patent describes a chip architecture having multiple processors on a single die that utilizes multiple operating systems. As shown below, the system described in the ’014 patent was known in the prior art.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that Apple is the real party-in-interest, and further certifies that no other party exercised control or could exercise control over the filing of this petition or Apple’s participation in any proceeding instituted on this petition.

B. Related Matters

According to assignment records at the United States Patent and Trademark Office, the ’014 patent is currently owned by Sonrai Memory Limited (“Patent Owner” or “PO”).

The ’014 patent is asserted in the matter *Sonrai Memory Ltd. v. Apple Inc.*, 6:22-cv-00787 (WDTX).

The ’014 patent was the subject of a previously filed *inter partes review* – IPR 2021-01454 (hereinafter “’454 IPR”). EX1004, 52-69. In the ’454 IPR, prior

Petitioner requested institution of inter partes review of the '014 patent under the same grounds proposed in the present Petition. *Id.* On March 4, 2022, the Board issued their decision instituting *inter partes* review of all of the challenged claims of the '014 patent on all grounds asserted in the former Petition. *Id.* On October 12, 2022, the Board granted the joint Motion to Terminate the '454 IPR proceeding following a settlement agreement between the parties. Although the Board had instituted *inter partes* review of the challenged claims, the Board did not decide the merits of the proceedings.

C. Counsel

Lead Counsel: Joseph Wolfe (Reg. No. 73,173)

Backup Counsel: James Heintz (Reg. No. 41,828)

D. Service Information, Email, Hand Delivery, and Postal

Apple consents to electronic service at joseph.wolfe@us.dlapiper.com and DLA-Apple-Sonrai-IPR@us.dlapiper.com.

Petitioner can be reached at DLA Piper LLP (US), 1650 Market Street, Suite 5000, Philadelphia, PA 19103, Phone: 215-656-3359, Fax: 215-606-2059.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies pursuant to Rule 42.104(a) that the patent for which review is sought is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the

grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Pursuant to Rules 42.22(a)(1) and 42.104(1)-(2), Petitioner challenges claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent.

A. Prior Art Patents and Printed Publications

The '014 patent issued from U.S. Patent Application No. 09/865,605 (“’605 application”), filed on May 29, 2001. Petitioner applies prior art with a priority date earlier than the '605 application’s filing date, May 29, 2001 (“Critical Date”).

The following references are pertinent to the grounds of unpatentability:¹

1. U.S. Patent Application Publication 2001/0044817 (“Asano”), filed as Application No. 09/756,282 on January 9, 2001, and published on November 22, 2001, is prior art under at least 35 U.S.C. § 102(e).
2. U.S. Patent No. 6,542,991 (“Joy”), filed as Application No. 09/309,734 on May 11, 1999, and issued on April 1, 2003, is prior art under 35 U.S.C. § 102(e).

¹ Because the '014 patent issued from an application filed prior to enactment of the America Invents Act (“AIA”), the pre-AIA statutory framework applies.

3. U.S. Patent No. 7,143,401 (“Babaian”), filed as Application No. 09/789,850 on February 20, 2001, and published on November 15, 2001, is prior art under 35 U.S.C. § 102(e).

B. Grounds for Challenge

This Petition, supported by the declaration of Dr. Martin G. Walker (“Walker Decl.”) (EX1002), requests cancellation of claims 1, 3, 5, 7, 11-13, and 15 as being unpatentable under 35 U.S.C. § 103. *See* 35 U.S.C. § 314(a). The grounds for challenge include the following:

	Grounds	References	Challenged Claims
1.	§103	Asano in view of Joy	1, 3, 5, 7, 11-13, 15
2.	§103	Asano in view of Babaian	1, 3, 5, 7, 11-13, 15

V. OVERVIEW OF THE ’014 PATENT AND THE PRIOR ART

A. Summary of the Alleged Invention

The ’014 patent relates to “a multiprocessing chip utilizing multiple operating systems.” EX1001, 1:6-10; EX1002, ¶38. The ’014 patent admits that multiprocessing systems with a multiprocessing chip were well-known, and it depicts a known prior art system in Figure 2 below. EX1001, 1:34-59; 1:41-42 (explaining that it was well-known in the art to use “multiple processors on a single die” to conserve space in a system). EX1002, ¶38.

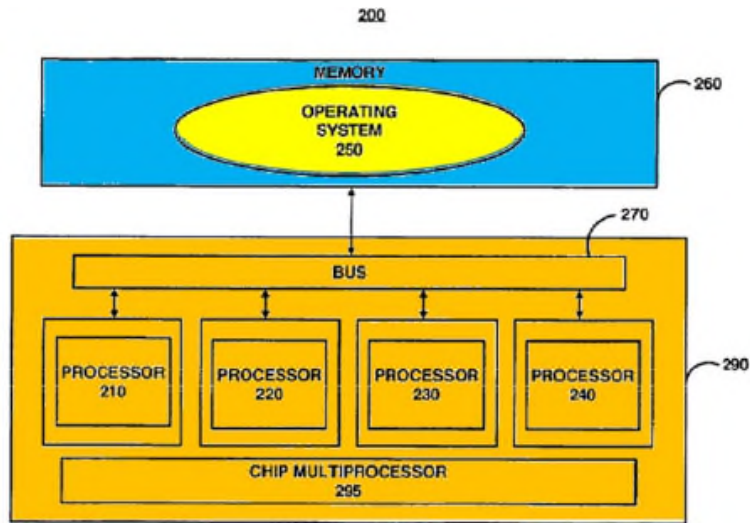


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated); EX1002, ¶38.

The prior art multiprocessing system (200) includes a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted in orange). EX1001, 1:34-37. The processors 210-240 use a single operating system 250 (highlighted in yellow) stored in memory 260 (highlighted in blue). EX1001, 1:37-40. The processors “may communicate with the memory 260 via a bus 270.” EX1001, 1:40-41. The ’014 patent states that “schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together.” EX1001, 1:44-47; 1:60-63 (the ’014 patent acknowledges that it was known in the art that multiprocessor systems could “support[] multiple processors executing multiple operating systems”); EX1002, ¶39.

Unlike the prior art system with multiple processors and a single operating

system, the '014 patent discloses a “multiprocessing system” where “multiple processors are connected to a memory storing **multiple** operating systems,” as illustrated in Figure 3 below. EX1001, 2:12-16 (emphasis added)². EX1002, ¶ 40.

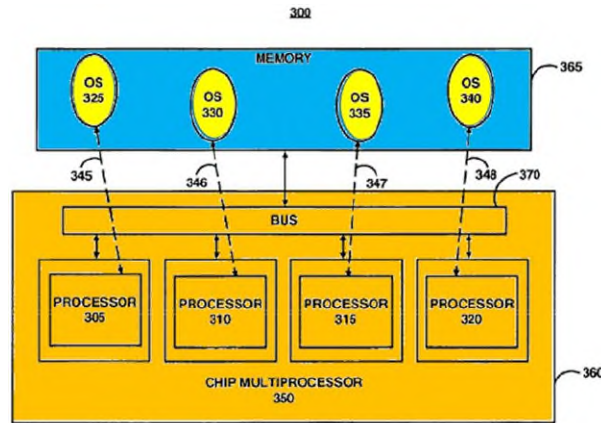


FIG. 3

EX1001, FIG. 3 (annotated), 2:54-55; EX1002, ¶40.

Like the prior-art system in FIG. 2 above, the computer system 300 in FIG. 3 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die (highlighted in orange). EX1001, 3:4-7. The multiprocessing system further includes multiple operating systems 325-340 (highlighted in yellow) stored in a memory 365 (highlighted in blue). EX1001, 3:10-11. The '014 patent explains that “[d]uring operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus

² Unless otherwise noted, all emphases are added.

370.” EX1001, 3:11-14. The ’014 patent also explains that “[e]ach processor may be ... capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.” EX1001, 3:47-51; EX1002, ¶41.

All the limitations in the challenged claims were known in the prior art and obvious. *See infra* Section VII; EX1002, ¶¶68-217; *see also* EX1002 ¶¶18-37 (technology background, citing Exhibits 1008-1018), ¶¶43-55 (discussing the prior art at issue in this petition), ¶¶68-217 (discussing prior art disclosures in view of each claim’s limitations).

B. Level of Ordinary Skill in the Art

A person having ordinary skill in the art (“POSITA”) for the ’014 patent would have had at least a bachelor’s degree in electrical engineering, computer science, computer engineering, or an equivalent, and at least two years of experience relating to the field of computer processor architecture. Additional education can remedy a deficiency in experience, and vice versa. EX1002, ¶¶15-17

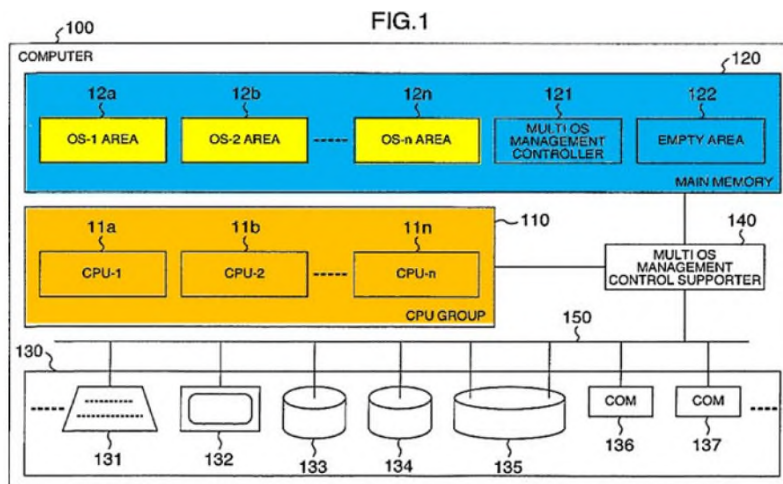
C. Prosecution History

During prosecution of the ’014 patent, the Examiner issued a first Office Action mailed April 16, 2004. In the first Office Action, the pending claims were rejected under 35 U.S.C. § 102 as being anticipated by Applicant Admitted Prior Art (“AAPA”). EX1004, 121-126. In response, Applicant argued over the rejection

without amending the claims. EX1004, 110-119. The Examiner issued a second Office Action mailed August 26, 2004. EX1004, 98-103. In the second Office Action, the pending claims were rejected as obvious over AAPA in view of US Patent No. 6,772,241 (“George”) (EX1012) and US Patent No. 6,526,462 (“Elabd”) (EX1013). *See id.* In distinguishing prior art, Applicant amended claim 1 to include the limitation “wherein . . . two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.” EX1004, 87-97 (PO amended claims 7 and 13 in a similar fashion). PO argued that the prior art of record did not disclose the “simultaneously executing” limitation. *Id.* Subsequently, the claims were allowed. EX1004, 77-80.

D. Overview of Asano

Asano discloses a multiprocessing system 100 including multiple processors (e.g., 11a-11n) in a processor group 110 (highlighted in orange) where the multiple processors are connected to a memory (highlighted in blue) storing multiple operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1 (reproduced below); *see also* EX1005, ¶[0001] (“The present invention relates to a computer system and a method for controlling a computer system in which a plurality of operating systems (OS) operate on one computer”); EX1002, ¶43.



EX1005, FIG. 1 (annotated); EX1002, ¶43.

The computer system 100 in Figure 1 includes a processor group 110 having multiple processors 11a-11n (highlighted in orange). EX1005, ¶[0031]. The multiprocessing system further includes multiple operating systems (highlighted in yellow), e.g., OS-1-OS-n, stored in a memory 120 (highlighted in blue). *Id.* Asano discloses that this multiprocessing system 100 can “execute a plurality of operating systems.” *Id.*; EX1002 ¶44.

Asano further discloses that the processors are allocated either individually or in groups to the various operating systems. EX1005, ¶[0035]. For example, each processor may be allocated to a particular operating system at a predetermined time interval. *Id.*; EX1002 ¶45.

E. Overview of Joy

Joy discloses multiple processors mounted on a single die. EX1002, ¶46. For example, Joy discloses a horizontal threaded processor architecture that “combines multiple processors on a single integrated circuit die.” EX1006, 7:4-6. “The multiple processors are vertically threaded to form a processor with both vertical and horizontal threading, *augmenting executing efficiency and decreasing latency in a multiplicative fashion.*” EX1006, 7:6-9 (emphasis added); 2:17-32 (“To further increase system parallelism in some processor embodiments, multiple processor cores are formed in a single die.”). Joy further discloses that each of the vertical and horizontal threaded processors in the single integrated chip of Joy “advantageously accelerates context switching time from millisecond ranges to nanosecond ranges.” EX1006, 7:49-54; EX1002, ¶46.. Joy explains that such fast context switching “is highly advantageous in all processing environments including embedded, desktop, and server applications, and the like.” EX1006, 7:52-54; EX1002 ¶46.

Figure 2C below illustrates the timing diagram for an exemplary single integrated circuit in Joy that includes two processors on the single die, where each processor can execute two or more threads simultaneously. EX1006, 7:9-15, 7:20-27, FIG. 2C; *see also* EX1006, 2:42-57 (Joy provides several exemplary configurations including “a ‘4C4T’ configuration” where a “four-processor

multiprocessor is formed on a single die with each of the four processors being four-way vertically threaded.”); 2:34-42 (“For example two processor cores are combined ... in one system. In another example, four processor cores are combined A countless number of variations are possible. In some systems, each processor core is a vertically-threaded pipeline.”). In particular, Figure 2C below illustrates a first processor executing a “first thread 252” and a “second thread 254” (highlighted red) in parallel with a second processor executing a “first thread 256” and a “second thread 258” (highlighted blue). EX1006, 7:10-27, FIG. 2C. Joy explains that by implementing “both vertical multithreading and horizontal multithreading,” the “processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time.” EX1006, 2:17-32; 7:52-54; EX1002, ¶47.

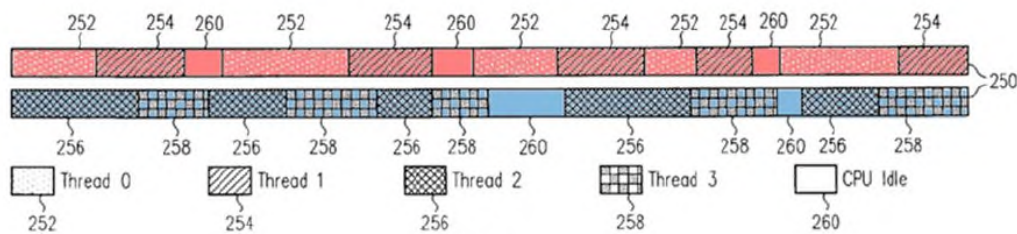


FIG. 2C

EX1006, FIG. 2C; 4:46-50 (FIG. 2C illustrates a timing diagram for the execution flow in a vertical and horizontal multithread processor); EX1002, ¶47.

F. Motivation to Combine Asano and Joy

As previously noted, Asano discloses a multiprocessing system 100 that includes multiple processors (e.g., 11a-11n) in a processor group 110 where the multiple processors are connected to a memory storing multiple operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1; see also EX1005, ¶[0001] (“The present invention relates to a computer system and a method for controlling a computer system in which a plurality of operating systems (OS) operate on one computer”). Asano discloses that each of the processors is allocated to execute an operating system from a plurality of operating systems, OS-1 to OS-n. EX1002, ¶48.

Asano discloses that at least two operating systems are simultaneously running on computing system 100. EX1005, ¶¶[0032]-[0033]. For example, Asano discloses that the computer system 100 includes a main memory 120 (“memory”). EX1005, ¶[0030]. The main memory 120 “includes main memory areas 12a to 12n” that are “allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n),” as shown in Figure 1 below. Figure 2, reproduced below, further illustrates one configuration of the system shown in Figure 1 where two operating systems, OS-1, OS-2 (highlighted yellow), are simultaneously running on the computer system 100. EX1005, ¶¶[0032]-[0033]. Thus, Asano teaches a computing system that includes multiple

processors, where at least two processors are able to simultaneously execute a command, i.e., commands associated with executing an operating system. Asano does not limit the processor to any specific configuration or implementation, nor does it require a specific structure or arrangement. Thus, a person of ordinary skill in the art seeking to implement a multi-processor system pursuant to the teachings of Asano would consider references disclosing the structure of such multi-processor systems, which includes Joy. EX1002 ¶49.

Joy discloses precisely what is suggested by Asano, multiple processors mounted on a single die. Moreover, because Joy discloses a flexible design (e.g., “[c]ountless other ‘nCkT’ structures and combinations may be implemented on one or more integrated circuit dies depending on the fabrication process employed and the applications envisioned for the process”), a person of ordinary skill in the art would immediately understand that the teachings of Joy regarding the fabrication process of multiple processors on a single die could be used in combination with the teachings of Asano regarding a multiprocessing system that simultaneously executes multiple operating systems. EX1002 ¶50.

As further discussed below, Joy teaches that it is advantageous to locate multiple processors on the same die, which leads to sped-up communications and reduced latency, for example. *See e.g.*, EX2006, 7:31-39, 7:55-57; EX1002, ¶51.

These known advantages would further motivate a POSITA to implement Asano's processors on a single die. EX1002 ¶51.

G. Overview of Babaian

Babaian discloses multiple processors mounted on a single die. EX1002, ¶52. For example, Babaian discloses a single chip multiprocessor system. EX1007, 3:56-62 (“a ***single chip*** multiprocessor system with explicit parallelism architecture processors ...[with] multiprocessor parallel execution to help ensure a high level use of ILP [instruction-level parallelism]”) (excerpted), 4:8-18 (describing that the single chip multiprocessor system can be either tightly-coupled or weakly-coupled), 4:31-35 (describing the benefits associated with the single chip multiprocessor system that include “substantially increas[ing] the performance” in executing “program streams” and “data exchange”), 7:1-9 (Figure 7 illustrates an exemplary single-chip multiprocessor system 700 suited for parallel execution). The single-chip multiprocessor includes four processors 710-1 to 710-4 (highlighted orange) and optional specialized co-processors. EX1007, 7:1-9, FIG. 7. Because the processors (e.g., 710-1-4) are all contained in a single chip, a POSITA would have thus understood that the processors are mounted on a single die. EX1002, ¶52.

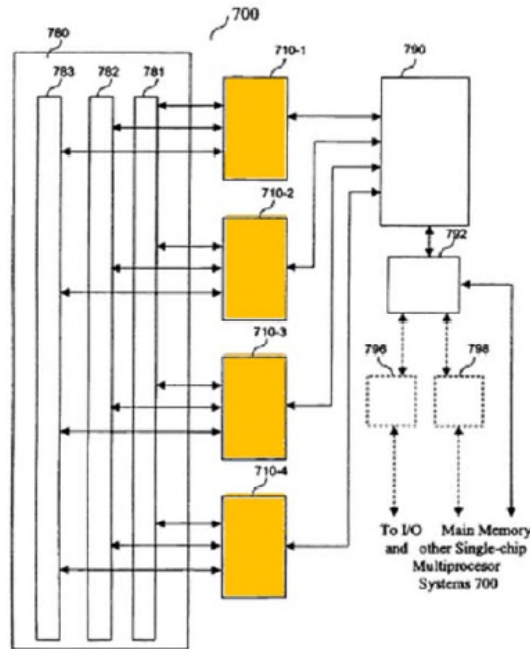


Fig. 7

EX1007, FIG. 7 (annotated); 4:56-58; EX1002, ¶52 (FIG. 7 illustrates a single-chip multiprocessor system).

Babaian further explains that such a configuration as shown above allows for “flexible assignment of the idle processors for the execution of a program.”

EX1007, 13:65-14:3; 3:14-17. For example, the system may “assign[] some Processors 710 for execution of a task, forming a working configuration.”

EX1007, 13:46-48. Processor assignment is implemented by assigning numbers to each processor, e.g., processor 1-4. EX1007, 13:37-46. “For example, for parallel execution in two processors, Processors 710 with the physical numbers 1 and 3 can be assigned.” EX1007, 13:48-50. This processor numbering allows the single-chip

multiprocessor to “simultaneously perform[] independent programs.” EX1007, 3:14-17; EX1002, ¶53.

H. Motivation to Combine Asano and Babaian

As previously noted, Asano teaches a computing system that includes multiple processors, where at least two processors are able to simultaneously execute a command, i.e., commands associated with executing an operating system. *See supra* Section, V.D; *infra* Sections VII.A.1; VII.B.1. Asano does not limit the processors to any specific configuration or implementation, nor does it require a specific structure or arrangement. Thus, a person of ordinary skill in the art seeking to implement a multi-processor system pursuant to the teachings of Asano would consider references disclosing the structure of such multi-processor systems, which includes Babaian. EX1002, ¶54.

Babaian discloses precisely what is suggested by Asano, multiple processors mounted on a single die. *See supra* Section V.G; *infra* Section VII.B.1. Moreover, because Babaian discloses a flexible design (e.g., “[t]hose skilled in the art will realize that the Single-chip Multiprocessor System, retaining the essential features of the present invention, may have different implementations”), a person of ordinary skill in the art would immediately understand that the teachings of Babaian regarding the fabrication process of multiple processors on a single chip could be used in combination with the teachings of Asano regarding a

multiprocessing system that simultaneously executes multiple operating systems.

EX1002, ¶55.

VI. CLAIM CONSTRUCTION

Claims subject to *inter partes* review are to be “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-16 (Fed. Circ. 2005). The Board, however, only construes the claims when necessary to resolve the controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper no. 11 at 16 (Aug. 14, 2015). Aside from the terms addressed below, Petitioner submits that no express constructions of any of the terms are necessary and that the challenged claims should be interpreted according to their plain and ordinary meaning. EX1002, ¶56-67.³

³ Petitioner reserves all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §§ 101 or 112, in district court as relevant to those proceedings. *See, e.g., Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11-13 (November 10, 2020). A comparison of the claims to any accused products in litigation may raise controversies that are not presented here given the similarities between the references and the patent.

A. "simultaneously executing two or more operating systems"

In the currently pending litigation, Petitioner and PO have agreed that "simultaneously executing two or more operating systems" should be construed as "simultaneously executing two or more *independent* operating systems." The Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language.

B. "multiple operating systems residing in a memory"

In the currently pending litigation, Petitioner and PO have agreed that "multiple operations systems residing in a memory" should be construed as "multiple operating system residing in the same memory." The Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language.

C. "multiple processors are connected to said memory via a bus"

In the currently pending litigation, Petitioner and PO have agreed that "multiple processors are connected to said memory via a bus" in dependent claim 3 should be construed as "multiple processors are connected to said memory via the same bus." The Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language.

D. “processor means” in claim 12

In the currently pending litigation, Petitioner and PO have an agreed upon construction for “processor means.” The agreed-upon function is “executing a plurality of operating system means.” The agreed-upon structure is “chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360 as shown in Figure 3 and associated descriptions in the specification; or chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460 shown in Figure 4 and associated descriptions in the specification; and equivalents thereof.” The function and corresponding structure are substantially similar to those proposed by petitioner in the ’454 IPR.

E. “operating system means” in claim 12

The “operating system means” phrase does not recite “means for” language. Instead, the “operator system means” only recites “means.” Accordingly, “operating system means” does not invoke 35 U.S.C. § 112 ¶6. EX1001, 4:66, Claim 12. Further, this term is not subject to any claim construction dispute in the current litigation. EX1002, ¶65.

Therefore, no construction aside from plain and ordinary meaning is required.

F. “memory means” in claim 12

The “memory means” phrase recites “means for” language, which invokes 35 U.S.C. § 112 ¶6. EX1001, 5:1, Claim 12. The identified function of the “memory means” is “storing said plurality of operating system means.” EX1001, 5:1-2, Claim 12. The ’014 patent identifies as corresponding structure “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” EX1001, 3:15-20; EX1002, ¶66.

Thus, the claimed “memory means” should be construed as SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; or equivalents thereof. EX1002, ¶66.

VII. SPECIFIC GROUNDS FOR PETITION

Pursuant to Rule 42.104(b)(4)-(5), the following sections, detail the grounds of unpatentability, the limitations of the challenged claims of the ’014 patent, and how these claims are obvious in view of the prior art.

A. Ground 1: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Asano and Joy

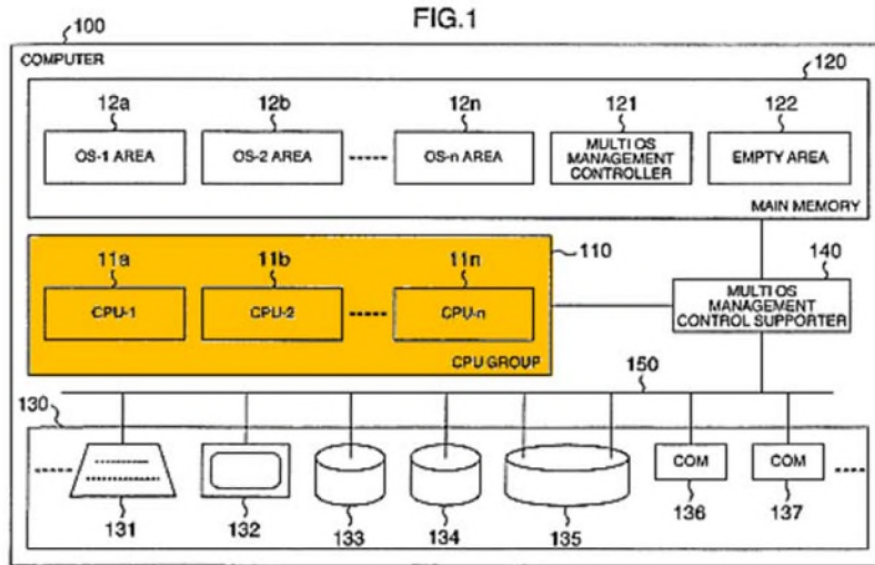
Both Asano and Joy were not considered during prosecution of the ’014 patent and are highly relevant to claims 1, 3, 5, 7, 11-13, and 15 of the ’014 patent.

1. Claim 1

a. A multiprocessing system comprising

To the extent the preambles are limiting, the Asano-Joy combination discloses the limitations therein. EX1002, ¶69.

For example, Asano discloses a computer system, as shown in Figure 1 below, that includes a processor group 110 (highlighted in orange) for executing a plurality of operating systems. EX1005, ¶¶[0030]-[0031], FIG. 1; *see also* EX1005 ¶[0001] (“The present invention relates to a computer system ... in which a plurality of operating systems (OS) operate on one computer, and in particular, to a computer system ... in which computer resources can be efficiently used or operated in an operating state of a plurality of operating systems.”). “The processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b . . . , 11n.” EX1005, ¶[0031]. A POSITA would have thus understood that Asano’s computer system is a multiprocessing system as claimed because this system includes multiple processors (e.g., processors 11a-11n). EX1002, ¶70.



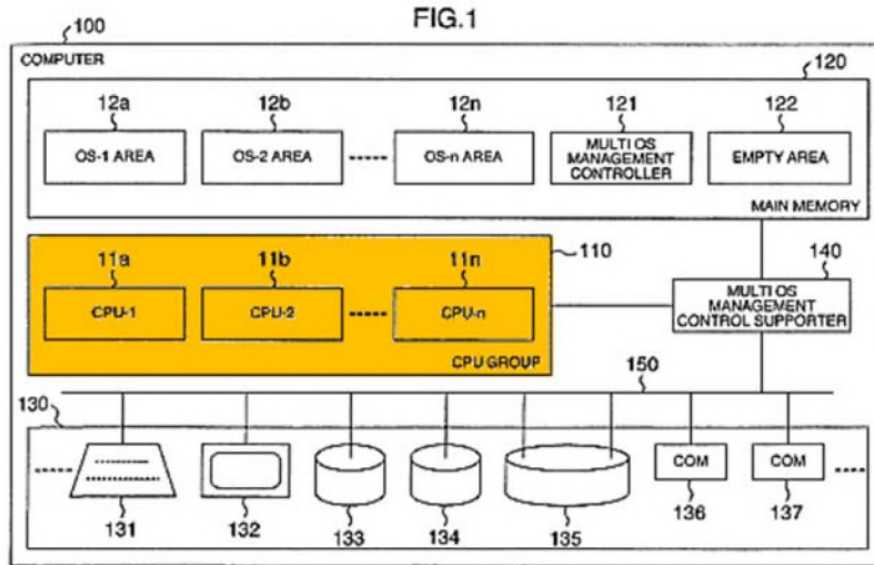
EX1005, FIG. 1 (annotated); EX1002, ¶70.

Thus, Asano discloses “[a] multiprocessing system,” as claimed. EX1002, ¶71.

b. multiple processors mounted on a single die

The Asano-Joy combination discloses this limitation. EX1002, ¶72.

Asano discloses a computer system that includes a processor group 110 that includes multiple processors. EX1005 ¶¶[0030]-[0031]. For example, Asano discloses that the “processor group 110” (highlighted orange) “is a set of one or more processors (CPUs)” that “includes processors 11a, 11b . . . , 11n.” EX1005 ¶[0031]; EX1002, ¶73.



EX1005, FIG. 1 (annotated); EX1002, ¶73.

To the extent that Asano does not explicitly provide that the multiple processors are mounted on a single die, Joy teaches doing so. EX1002, ¶74.

Specifically, Joy discloses multiple processors mounted on a single die. For example, Joy discloses a horizontal threaded processor architecture that “combines multiple processors on a single integrated circuit die.” EX1006, 7:4-6; EX1002, ¶75.

A POSITA would have been motivated in light of Joy to configure the system in Asano so that its multiple processors are “mounted on a single die,” as claimed. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable

results. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). EX1002 ¶76.

A POSITA would have recognized that Joy and Asano disclose features in a similar technological field. *See supra* Section, V.F. For example, as discussed above, both Asano and Joy relate to multi-processor computing systems. EX1005, ¶[0031] (“The computer system 100 of the first embodiment includes a processor group 110 . . . The processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b, . . . 11n. ”); EX1006, 2:29-31 (“To further increase System parallelism in Some processor embodiments, multiple processor cores are formed in a single die.”); EX1006, 2:29-31 (explaining that Joy’s processor architecture is beneficial for computing applications that are “subject to frequent context switches” such as “disk server, network server, web server, telecommunications applications and the like”), EX1006, 14:64-67; EX1002, ¶77. Specifically, each system utilizes a computing system that includes multiple processors that are capable of simultaneously executing commands. EX1002, ¶77.

Additionally, Asano and Joy relate to improving computer systems for server applications. EX1005, ¶[0010] (“The computer system can be therefore developed as a server for a plurality of users.”), EX1005, ¶[0076] (“In general, when a computer of a multiprocessor environment is used as a server machine, a plurality of users access the server machine.”); EX1006, 7:51-54 (explaining that

Joy's processor architecture is beneficial for computing applications that are "subject to frequent context switches" such as "disk server, network server, web server, telecommunications applications and the like"), EX1006, 14:64-67; EX1002, ¶78.

Joy discloses several benefits associated with using multiple processors on a single integrated circuit die that are applicable to any multiprocessing architecture, including Asano. For example, Joy discloses that "[h]orizontal multithreading or circuit chip multiprocessing *further increases on-chip parallelism by exploiting increasingly smaller processor core sizes*" (EX1006, 7:55-57) and "*further advantageously exploits processor speed and power improvements that inherently result from reduced circuit sizes* in the evolution of silicon processing" (EX1006, 7:36-39). "The combination of vertical multithreading and horizontal multithreading *also advantageously reduces communication latency among local (on-chip) multi-processor tasks by eliminating much signaling on high-latency communication lines between integrated circuit chips.*" EX1006, 7:31-36; EX1002, ¶79.

Joy's teaching that processor speed and power improvements inherently result from reducing circuit sizes would further motivate a POSITA to arrange Asano's processors on a single die. EX1002, ¶80. Likewise, Joy teaches that performance-reducing high-latency communication occurs between separate chips.

EX1006, 7:31-36. This teaching likewise motivates a POSITA to arrange Asano's processors on a single die so as to eliminate high-latency communication. EX1002, ¶80.

Accordingly, a POSITA would have had reason to consider the teachings of Joy when implementing Asano's system. EX1002 ¶81.

Moreover, as discussed below for claim limitation 1.d, Asano discloses that the processor group operates a plurality of operating systems where the system may allocate each processor to another operating system at a predetermined interval of time (e.g., switching between operating systems). *See infra* Section VII.A.1.d; *see also* EX1005 ¶¶[0030]-[0031], [0035]. A POSITA would have thus further recognized that implementing Joy's teachings regarding the multiple processors combined on a single integrated circuit die in Asano would have allowed the combined system to allocate (e.g., via context switching) each processor from an operating system to another operating system at nanosecond speeds. *See, e.g.*, EX1006, 7:49-54. A POSITA facing the wide range of needs created by developments in the technical field of Asano and Joy would have appreciated the benefits of using the multi-threaded, multiple processors mounted on a single die configuration as described in Joy with Asano's system. (*Id.*; *see also supra* Section VII.A.1.b.). EX1002, ¶82.

For instance, given Asano's system that allows each processor to be allocated to another operating system at a predetermined interval of time (EX1005 ¶[0035]), a POSITA would have appreciated that the benefits associated with using one or more multiple processors on a single die as discussed by Joy would be similarly applicable to Asano. EX1002, ¶83.

In addition, the benefits of having multiple processors on a single die in a multi-processor system (such as the system in Asano) were well known in the art before the '014 patent thereby further motivating a POSITA to apply Joy's teachings regarding a single-die multiprocessor to Asano. EX1002, ¶ 84. For example:

- combining processors on a single piece of silicon “outperforms multiple discrete processors by 50% or more” (EX1008, 1) and allows engineers to “take advantage of shorter distances and faster bus speeds when shuttling data between” the processors (*Id.*);
- “[s]ingle-chip multiprocessor architectures have the advantage in that they offer localized implementation of a high-clock rate processor for inherently sequential applications and low latency interprocessor communication for parallel applications.” EX1009, Abstract;
- “[m]ulti-core microprocessors feature a single integrated circuit that includes two or more main processing cores, each of which may be utilized as if it

was a separate central processing unit” (EX1010, 1:37-47) and “each of the main cores provides computing power that equals or exceeds that of a conventional high-performance single core processor” (*Id.*);

- “[a]mong the benefits provided by multi-core processors is an increase in physical processing core density within multiprocessor data processing systems, in that more processing cores may operate within a given amount of space, which leads to improvements in overall multiprocessor system performance” (EX1010, 1:48-60); and
- “[t]he key questions for designers of future processors will not be whether to use chip multiprocessing, but the appropriate trade-off between the number of cores and the power of each core” (EX1011, 292).⁴

EX1002, ¶84.

Indeed, the ’014 patent acknowledges using multiple processors mounted on a single die in a computer system as conventional and beneficial. EX1002, ¶85.

For instance, the ’014 patent describes a “conventional multiprocessing scheme

⁴ To show that claim 1 is obvious, Petitioner relies here on the teachings of Asano and Joy only. Exhibits 1008-1011 demonstrate what a POSITA would have known at the time of the alleged invention of the ’014 patent regarding the benefits of having multiple processors on a single die. *Int’l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016).

(shown in FIG. 2) includes a computer system 200 having a chip multiprocessor 295” where “[t]he chip multiprocessor includes multiple processors 210-240 on a single die 290,” which saves space in the computer system. EX1001, 1:34-44, FIG. 2 (illustrating this conventional scheme). Thus, placing Asano’s multiple processors on a single die would have been a common-sense approach. EX1002, ¶85.

Therefore, based on Joy’s disclosure and the knowledge in the art, it would have been obvious for the processor group 110 in the combined Asano-Joy system to be mounted on a single die. EX1002, ¶86.

Furthermore, using multiple processors mounted on a single die in the above combination would have been a straightforward application of basic computer design principles for designing a multi-processor system, as acknowledged by the ’014 patent itself. EX1001, 1:34-42. Such knowledge, coupled with the disclosures/suggestions of Joy, would have motivated a POSITA to use multiple processors mounted on a single die in the Asano system to not only reduce the size of the computer system but also provide accelerated execution of threads based on fast context switching at nanosecond speeds as one benefit of the combination. EX1002 ¶87.

The combination of Asano with Joy would have involved the use of known technologies (e.g., computer chip architectures for computer systems), design

concepts, and processes to obtain the foreseeable result of a computer system utilizing multiple processors mounted on a single die, which would provide fast context switching between executing threads originating from multiple operating systems. EX1002, ¶88.

A POSITA would have been skilled and knowledgeable to configure Asano's system to implement a system using multiple processors mounted on a single die while considering any known design and related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. *Id.* For example, a POSITA would have been motivated based on such disclosures to configure Asano's system with CPU group 110 and its multiple processors (11a through 11n) on a single die. *Id.* Thus, a POSITA would have had a reasonable expectation of success in the above modification. *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) ("only a reasonable expectation of success, not a guarantee, is needed" in an obviousness analysis); EX1002, ¶89.

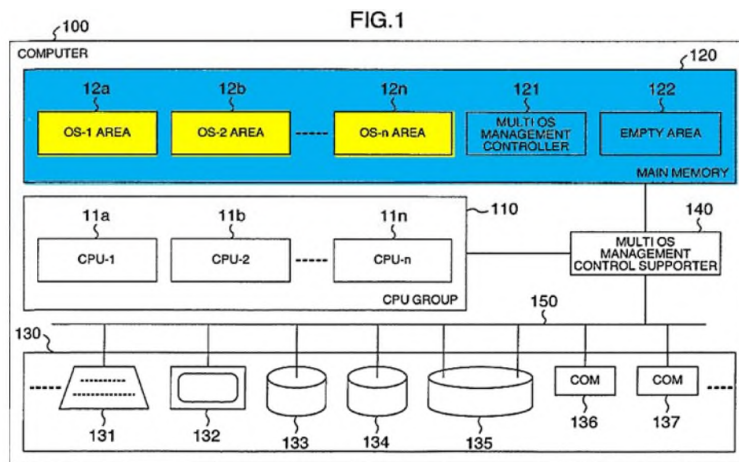
Accordingly, the combination of Asano and Joy discloses and/or suggests "multiple processors mounted on a single die," as claimed. EX1002, ¶90.

c. multiple operating systems residing in a memory connected to multiple processors

The Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶91.

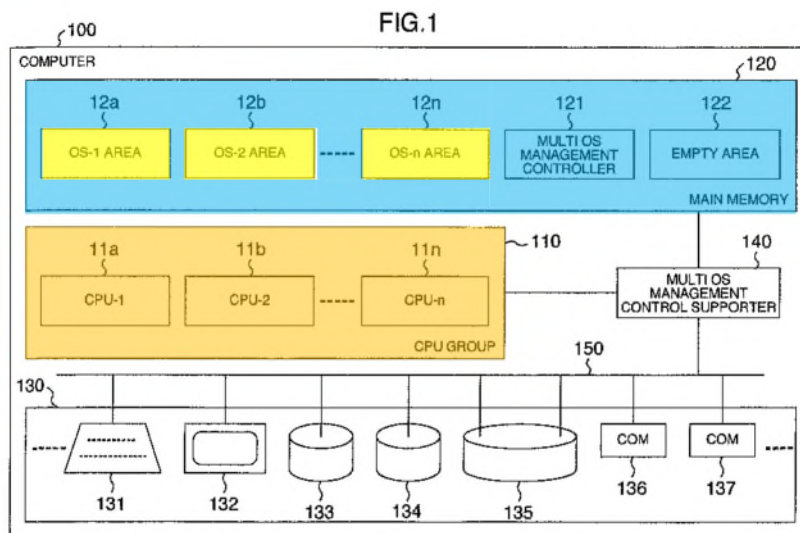
For example, the combined Asano-Joy system includes multiple processors mounted on a single die (“said multiple processors”). *See supra* Section VII.A.1.b. As discussed below, the combined Asano- Joy system would have included multiple operating systems residing in a memory connected to the multiple processors. EX1002, ¶92.

For example, Asano discloses that the computer system 100 includes a main memory 120 (“memory”). EX1005, ¶[0030]. The main memory 120 (highlighted blue) “includes main memory areas 12a to 12n” that are “allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n) [highlighted yellow],” as shown in Figure 1 below. EX1005, ¶[0031]. Thus, a POSITA would have understood that the multiple operating systems (e.g., OS-1 to OS-n) reside in memory 120, as claimed. EX1002, ¶93.



EX1005, FIG. 1 (annotated); EX1002, ¶93.

Asano further discloses that the memory 120 is connected to the multiple processors. For example, as illustrated in Figure 1 (below), the computer system 100 includes a bus 150 connecting the processor group 110 (highlighted orange), which includes multiple processors (e.g., CPU-1 to CPU-n), and the main memory 120 (highlighted blue). EX1005, ¶¶[0030]-[0031], FIG.1 (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120, an external input/output device group 130, a multiple operating system (multi OS) management control supporter 140, and a bus 150 establishing connections between constituent components.”). The system further includes a multiple operating system management (multi-OS) control supporter 140 (EX1005, ¶[0031]) that “allocate[s] computer resources to the operating system.” EX1005, abstract; EX1002, ¶94.



EX1005, FIG. 1 (annotated); EX1002, ¶94.

The manner in which Asano connects the memory to the multiple processors tracks that described in the '014 patent. For example, the '014 patent explains that each processor is connected with the memory “via a bus.” EX1001, 3:11-14.

Asano’s memory and processors are connected in the same manner via bus 150.

EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120... and a bus 150 establishing connections between the constituent components.”), EX1002 ¶95.

A POSITA would have thus understood that the multiple operating systems residing in memory 120 are connected to the multiple processors in the processor group 110, as claimed. EX1002, ¶96.

Furthermore, a POSITA would have understood that placing the multiple processors on a single chip (*see supra* Section VII.A.1.b) would not have detracted from or changed the connection between the processors and memory in Asano.

Indeed, a POSITA would have recognized that in the combined Asano-Joy system, the processor group 110, which comprises multiple processors mounted on a single die, would be connected (e.g., via a bus) to the memory where the multiple operating systems reside. EX1002, ¶97.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶98.

Further, to the extent that the Board adopts the narrower agreed-upon District Court construction (“multiple operating systems residing in the same memory”) rather than plain meaning, the Asano-Joy combination still discloses and/or suggests this limitation. EX1002, ¶99.

As stated, and shown in Figure 1 above, main memory 120 (highlighted blue) “includes main memory areas 12a to 12n” that are “allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n) [highlighted yellow].” EX1005, ¶[0031. Figure 1 clearly discloses each of the main memory areas 12a-12n that are allocated to the operating systems reside in the same memory – main memory 120. Furthermore, there is no teaching in Asano that would preclude the multiple operating systems from residing in the same memory. EX1002, ¶100.

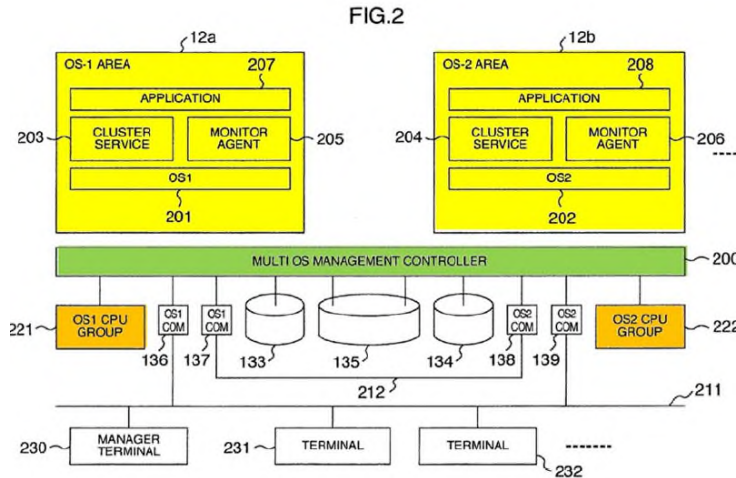
Thus, Asano-Joy still discloses and/or suggests this limitation. EX1002, ¶101.

- d. wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems**

The Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶102.

As explained above, the combined Asano-Joy system includes multiple processors mounted on a single die and multiple operating systems connected to these multiple processors. *See supra* Sections VII.A.1.b-c. Each of these processors in the combined Asano-Joy system executes an operating system from the multiple operating systems, whereby two or more of the processors are capable of simultaneously executing two or more of the operating systems. EX1002, ¶103.

Asano discloses that each of the processors is allocated to execute an operating system. For example, Asano discloses that the computer system 100 includes a processor group 110 that interacts with a multi-OS control supporter 140 to operate (“execute”) a plurality of operating systems, OS-1 to OS-n. *See supra* Section VII.A.1.c; EX1005 ¶¶[0030]-[0031]. Figure 2, reproduced below, further illustrates one configuration of the system shown in Figure 1 where two operating systems, OS-1, OS-2 (highlighted yellow), are simultaneously running on the computer system 100. EX1005, ¶¶[0032]-[0033]; EX1002, ¶104.



EX1005, FIG. 2 (annotated); *see also* EX1005, ¶[0014] (“FIG. 2 is a block diagram schematically showing a system construction including a cluster configuration of operating systems running in a computer system”); EX1002, ¶104.

Regarding the configuration shown in Figure 2, Asano further discloses that processor group 110 is divided into two groups (CPU group 221 and 222 (highlighted orange)) via the multi-OS controller (highlighted green). EX1005, ¶¶[0032]-[0033]. These CPU groups are each allocated to run at least one operating system. EX1005, ¶[0032]; *see also* EX1005, ¶[0035]. A POSITA would have understood that the allocation of the processors to the first and second operating systems would have resulted in processors executing the operating systems. EX1002, ¶105; *see also* EX1005 ¶[0001] (“a method for controlling a computer system in which a plurality of operating systems (OS) *operate* on one computer”); EX1005, ¶[0035] (explaining that each CPU within a given CPU

group may be “allocated to another operating system at a predetermined interval of time”). EX1002, ¶105.

Asano further discloses that the “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as claimed. EX1002, ¶106.

For example, Asano discloses a method of allocating the processors to simultaneously execute multiple operating systems where each CPU within a given CPU group “is allocated to another operating system at a predetermined interval of time.” EX1005, ¶[0035]. Asano further discloses that “the computer resources such as the CPU ... are updated to be allocated to a plurality of operating systems ... according to the states of the operating systems.” *Id.* A POSITA would have understood that this allocation of each of the processors to another operating system is a switching mechanism that provides each processor the capability to switch between multiple operating systems, which are simultaneously running in the system. The ’014 patent describes a similar process, where “[e]ach processor may be ... capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.” EX1001, 3:46-51; EX1005, ¶[0035]; EX1002, ¶107.

Asano removes any question that multiple operating systems are executed simultaneously. EX1002, ¶108.

In one example, Asano describes that the system may “include[] two operating systems in which a first operating system operates as an active system and a second operating system operates as a standby system.” EX1005, ¶[0035]. Figure 3, reproduced below, illustrates an exemplary allocation of computer resources such that the system executes two operating systems simultaneously, (OS-1 and OS-2), on the processors (highlighted in yellow). EX1005, FIG. 3. Asano explains that in this exemplary allocation of computer resources, the system has allocated “95% of the CPU resources ... to the active OS-1 and 5% thereof are allocated to the standby OS-2.” EX1005, ¶[0036]-[0037]; EX1002, ¶109.

FIG.3

300 COMPUTER STATE TABLE

310 COMPUTER RESOURCE ALLOCATION TABLE

311 COMPUTER RESOURCE NAME	312 ACTIVE COMPUTER RESOURCE SERVICE RATIO	313 STANDBY COMPUTER RESOURCE SERVICE RATIO
CPU	95%	5%
MAIN MEMORY		

320 OS STATE TABLE

321 OS NAME	322 STATE	323 ACTIVE,STANDBY	324 CPU
OS 1	OPERATING	ACTIVE	95%
OS 2	OPERATING	STANDBY	5%

EX1005, FIG. 3 (annotated). Thus, even in standby state, 5% of CPU resources is allocated to executing OS2. A POSITA would have understood that Asano contemplates achieving such division of CPU resources by having “each CPU . . .

allocated to another operating system at a predetermined interval of time.”

EX1004, ¶[0035]; EX1002, ¶109.

Moreover, based on Asano’s teachings a POSITA would understand that any other allocation is possible, including one where the resource allocation between OS1 and OS2 is equal, for example. EX1002, ¶110. For example, Fig. 7 of Asano shows a computer resource update state table for operating systems OS1 through OSn while Fig. 8 shows a flow chart for updating the “processing procedure for each operating system to update computer resources.” EX1005, ¶¶[0053]-[0054]. The procedure includes comparing the current loads of multiple operating systems and adjusting computing resources, indicating to a POSITA that the operating systems are executing simultaneously and generating differing loads on the computer resources. EX1005, ¶¶[0054]-[0063]; EX1002, ¶110.

Further, to the extent that the Board adopts the agreed-upon District Court construction of “simultaneously executing two or more operating systems” as “simultaneously executing two or more independent operating systems,” Asano likewise teaches this limitation. In particular, Asano clearly shows that OS-1 and OS-2 are separate and distinct operating systems in Figure 1. Asano further explicitly discloses operating a plurality of OSs independent of each other. EX1005, claim 9 (“operating the operating systems independent of each other”). As another example, the dynamic computer resource update process discussed

above demonstrates to a POSITA that each operating system is operating independently with different loads. EX1002, ¶111.

Thus, Asano teaches this limitation under any construction. EX1002, ¶112.

For similar reasons, the Asano-Joy combined system would have been configured such that each of the multiple processors in the single die executes an operating system from the multiple operating systems, and two or more of the multiple processors in the single die are capable of simultaneously executing two or more operating systems, as claimed. *See supra* Section VII.A.1.b. A POSITA would have understood that placing the multiple processors on a single chip (as discussed above in Section VII.A.1.b) would not have detracted from or changed the desirability of executing operating systems in this way, as taught in Asano. On the contrary, as explained above, Joy's multiple processors mounted on a single die enhances the ability (e.g., via context switching) for each processor to execute simultaneously two or more threads by switching at nanosecond speeds, thus further facilitating the simultaneous execution of multiple independent operating systems. *See supra* Section VII.A.1.b; EX1006, 7:9-14, 21-27, 45-54, FIG. 2C; EX1002, ¶113.

Accordingly, a POSITA would have understood that the system in the Asano-Joy combination includes both the software and hardware to allocate each

processor to another operating system by rapidly switching each or some of the processors between multiple operating systems. EX1002, ¶114.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶115.

2. Claim 3

a. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems

The Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶116.

As discussed for claim 1, Asano discloses that the multiple processors are connected to the memory to execute the operating systems. *See supra* Sections VII.A.1.c-d. Asano further discloses that the computer system 100 establishes connections between the processor group 110 and main memory 120 via a bus 150. EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120, an external input/output device group 130, a multi-OS control supporter 140, and *a bus 150 establishing connections between the constituent components.*”); *see also* EX1005, ¶[0031] (similar); EX1002, ¶117.

Accordingly, a POSITA would have understood that the system in the Asano-Joy combination would have included a bus that connects the multiple

processors mounted on a single die with the main memory 120 to execute instructions from the various operating systems and process data. EX1002, ¶118.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶119.

Further, to the extent that the Board adopts the agreed-upon District Court construction (“multiple processors are connected to said memory via the same bus”), the Asano-Joy combination likewise discloses and/or suggests this limitation. EX1002, ¶120.

Asano teaches that the computer system 100 “includes a processor group 100, a main memory 120... and a bus 150 connecting the constituent components to each other as shown in Fig. 1.” EX1005, ¶0031], FIG.1. Accordingly, the same bus 150 connects the multiple processors CPU1-CPU_n to main memory 120. Furthermore, there is no teaching in Asano that would preclude the multiple processors from being connected to the memory via the same bus. EX1002, ¶121.

Accordingly, even under PO’s narrower interpretation, the Asano-Joy combination still discloses and/or suggests this limitation. EX1002, ¶122.

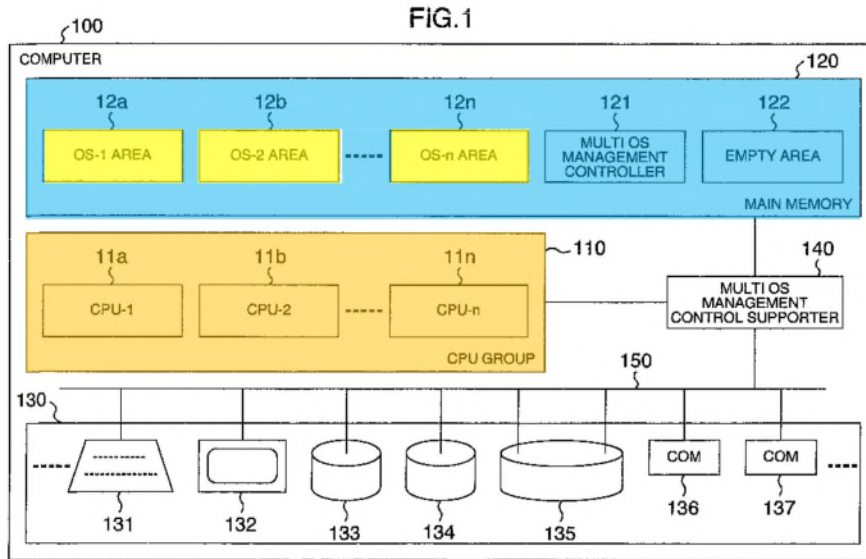
3. Claim 5

- a. **The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems**

The Asano-Joy combination discloses and/or suggests this limitation.

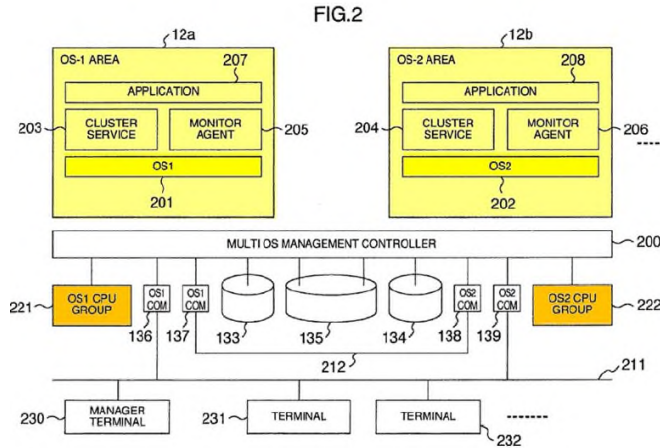
EX1002, ¶123.

For example, Asano discloses a computer system, as shown in Figure 1 below, that includes a processor group 110 (highlighted orange) for executing a plurality of operating systems and multiple separate operating system areas, OS-1 through OS-n area (highlighted yellow). *See supra* Section VII.A.1.a-d. Asano further explains that “the operating systems may differ from each other.” EX1005 ¶[0045] (“However, the operating systems may differ from each other. It is only necessary that each operating system can execute processing of the same applications.”). Accordingly, a POSITA would have understood that the combined Asano-Joy system executes “distinct operating system[s]” because each operating system executed in the system is a separate operating system (e.g., each OS is located in separate areas in memory (OS-1 area to OS-n area)) and each of these operating systems may differ from each other. EX1002, ¶124.



EX1005, FIG. 1 (annotated); EX1002, ¶124.

Asano further describes that “each of said processors executes a distinct operating system of said multiple operating systems.” EX1002, ¶125. For example, regarding Figure 2 (below), Asano discloses an exemplary configuration when two operating systems (i.e., OS-1, OS-2), highlighted yellow, are running in the system. EX1005, ¶[0032]. Each operating system has a processor group allocated to it, which are highlighted in orange, i.e., “CPU group 221 allocated to OS-1 and the CPU Group 222 is allocated to OS-2.” EX1005, ¶[0030]; EX1002 ¶125.



EX1005, FIG. 2 (annotated); EX1002, ¶125.

Asano further discloses and/or suggests a configuration where each of the processors in the processor group 110 is executing a distinct operating system from the multiple operating systems (e.g., OS1 (201) in 12a and OS2 (202) in 12b).

EX1002, ¶126.

For example, Asano discloses that the processor group 110 may include one or more processors. EX1005, ¶[0031]. Asano further explains that each processor group (e.g., 11a in OS1 CPU group 221 and 11b in OS2 CPU group 222) may be allocated to separate operating systems (e.g., OS1, OS2, respectively). EX1005, ¶[0035]. A POSITA would have thus understood Asano to teach that the processor group 110 could include two processors (e.g., 11-a and 11-b) and that the system assigns a single processor to each CPU group (e.g., OS1 CPU group 221 and OS2 CPU group 222). EX1002, ¶127. To this end, each of the processors, 11a and 11b, could be assigned to run distinct operating systems (OS-1 and OS-2,

respectively)—i.e., in this scenario, each processor, 11-a and 11-b, executes a separate (“distinct”) operating system. EX1005, ¶[0035], FIG. 2. Accordingly, Asano discloses the claimed “wherein each of said processors executes a distinct operating system of said multiple operating systems.” EX1002, ¶127.

At a minimum, it would have been obvious to a POSITA to make use of two processors, with each processor executing a distinct operating system, in view of the teachings of Asano. EX1002, ¶128. Asano recognizes that processor group 110 may include one or more processors and specifically contemplates a processor 11-a and 11-b. EX1005, ¶[0031]. Moreover, Asano teaches the assignment of different processors to different operating systems. EX1005, ¶[0035]. A POSITA would have recognized that, while Asano provides one example where two processors are assigned to each operating system (*Id.*), the number of processors assigned to a given operating system is a design choice, and, depending on the resources available (e.g., the number of processors available), a single processor could be allocated to a given operating system instead. EX1002, ¶128. A POSITA would have recognized Asano to suggest exactly this by disclosing that “n” processors are available and that Asano’s process would have operated in the same way regardless of the number of processors assigned to an operating system. EX1002, ¶128. A POSITA also would have had a reasonable expectation of success in performing such an implementation. EX1002, ¶128.

Thus, the Asano-Joy combination discloses and/or suggests this limitation.
EX1002, ¶129.

4. Claim 7

a. A multiprocessing system comprising:

To the extent that the preamble of claim 7 is limiting, Asano discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section VII.A.1.a; *infra* Section VII.A.6.b-d; EX1002, ¶130.

b. a plurality of processor groups mounted on a single die

This claim limitation 7.b varies from limitation 1.b in that it recites “groups” while claim limitation 1.b does not. *See supra* Section VII.A.1.b; EX1002, ¶131.

The Asano-Joy combination discloses claim limitation 7.b for at least the same reasons discussed above from claim limitation 1.b because each of the processors in the processor group 221, which would have been processors on a single die, are allocated into a plurality of groups.⁵ *See supra* Sections VII.A.1.b;

⁵ '014 claim 8, which depends on claim 7, recites “wherein each of said groups includes multiple processors,” indicating that claim 7 is not limited to groups of multiple processors. EX1001, claim 8.

see also EX1005, ¶[0035] (Asano discloses as an exemplary arrangement where CPU group 221 has been allocated “CPU-1 and CPU-2” and CPU group 222 has been allocated “CPU-3 and CPU-4 of the CPU group 110.”); EX1002, ¶132.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶133.

c. multiple operating systems residing in a memory connected to said groups

This claim limitation 7.c varies slightly from claim limitation 1.c in that it recites “groups” while claim limitation 1.c does not. *See supra* Section VII.A.1.c; EX1002, ¶134.

The Asano-Joy combination discloses claim limitation 7.c for at least the same reasons discussed above from claim limitation 1.c. *See supra* Section VII.A.1.c; EX1002, ¶135.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶136.

- d. wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems**

Claim limitation 7.d varies slightly from claim limitation 1.d in that it recites “groups” while claim limitation 1.d does not. *See supra* Section VII.A.1.d; EX1002, ¶137.

The combined Asano-Joy system discloses limitation 7.d for at least the same reasons discussed above from claim limitation 1.d. *See supra* Sections VII.1.2.d; EX1002, ¶138.

Thus, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶139.

5. Claim 11

- a. The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems**

Claim 11 varies slightly from claim 5 (“wherein each of said processors executes a distinct operating system of said multiple operating systems”) in that it recites “groups” while claim 5 does not. *See supra* Section VII.A.3; EX1002, ¶140.

The combined Asano-Joy system discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section VII.A.3; EX1002, ¶141.

6. Claim 12

a. A multiprocessing apparatus comprising:

To the extent that the preamble of claim 7 is limiting, the Asano- Joy combination discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section VII.A.1.a; *see infra* Section VII.A.10.b-d; EX1002, ¶142.

b. processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die

The Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitations 1.b, 1.d, and for the additional reasons provided below. *See supra* Sections VII.A.1.b, VII.A.1.d; EX1002, ¶143.

(1) operating system means

The Asano-Joy combination discloses and/or suggests an “operating system means,” as claimed. EX1002, ¶144; *see also supra* Section VI.E (construction of “operating system means” as a conventional operating system, such as WINDOWS NT, UNIX, and the like, or equivalents thereof).

For example, Asano’s system includes operating systems, e.g., operating system 1 (OS-1) to operating system n (OS-n). *See supra* Section VII.A.1.c; EX1005, ¶¶[0031], [0045] (Asano disclose that “each operating system can

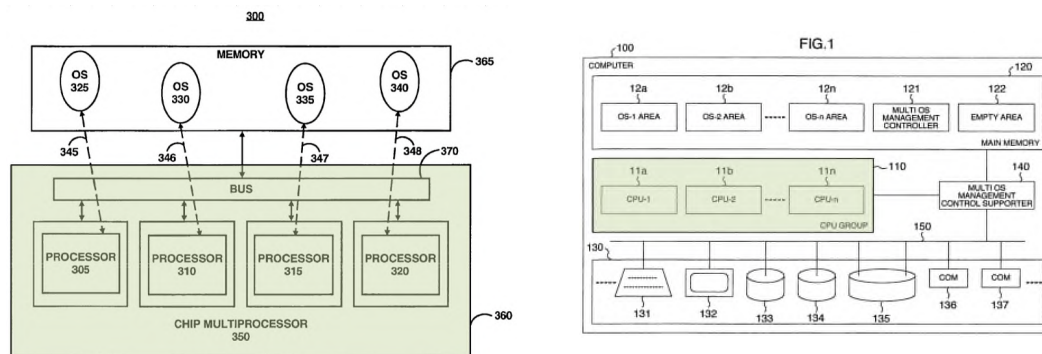
execute processing of the same applications”), Abstract, FIG. 1. Thus, a POSITA would have understood that the operating systems in the combined Asano-Joy system are “operating system means,” as claimed because these operating systems support the Asano-Joy system with various functions, such as executing applications and processing of data, and thus acts like a conventional operating system. EX1002, ¶145; *see also* EX1005 ¶¶[0002] (“The technique is called ‘cluster system’ in which when an operating system running on a computer fails, another operating system receives processing of the failed operating system to continue the processing. In the system of the background art, at a failure of an operating system on a computer, programs running on the computer can be continuously executed.”), EX1005, ¶¶[0008], [0045].

(2) processor means

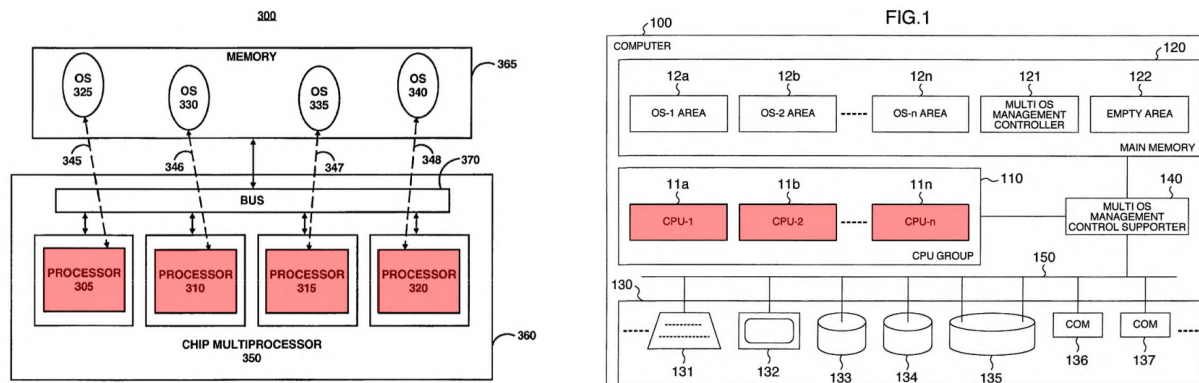
The Asano-Joy combination discloses and/or suggests a “processor means,” as claimed. EX1002, ¶146; *see also supra* Section VI.D (construction of “processor means”). For example, the combined Asano-Joy system includes a processor group 110, which is a chip multiprocessor that consists of two or more processors (e.g., processors 11a, 11b . . . , 11n.). *See supra* Section VII.A.1.b; EX1005 ¶[0031]. A POSITA would have thus understood that processor group 110 in the combined Asano-Joy system includes a plurality of processors mounted on a single die. EX1002, ¶146.

Further, to the extent the Board adopts the agreed-upon District Court construction, the Asano-Joy combination still discloses this limitation. EX1002, ¶147.

With regard to the claimed structure, as shown below, the '014 Patent discloses chip multiprocessor 350 (left, green). Similarly, Asano discloses a chip multiprocessor (right, green). EX1002, ¶148.

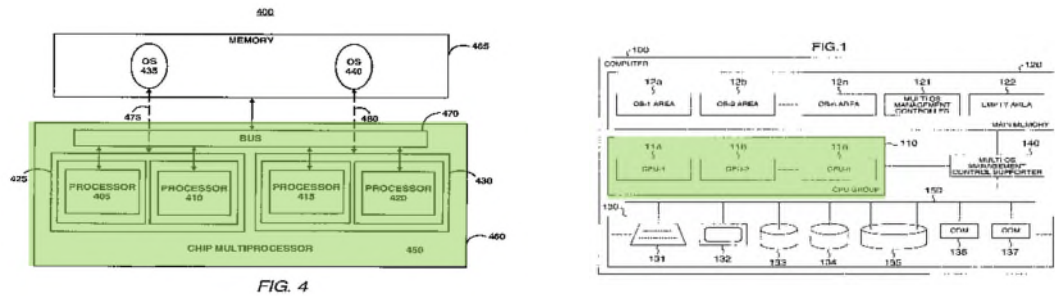


The '014 Patent discloses that chip multiprocessor 350 includes four processors 305-320 (left, red). Similarly, Asano discloses that CPU group 110 can include n number of CPUs, such as CPU-1 11a, CPU-2 11b, all the way up through CPU- n 11n (right, red). EX1002, ¶149.

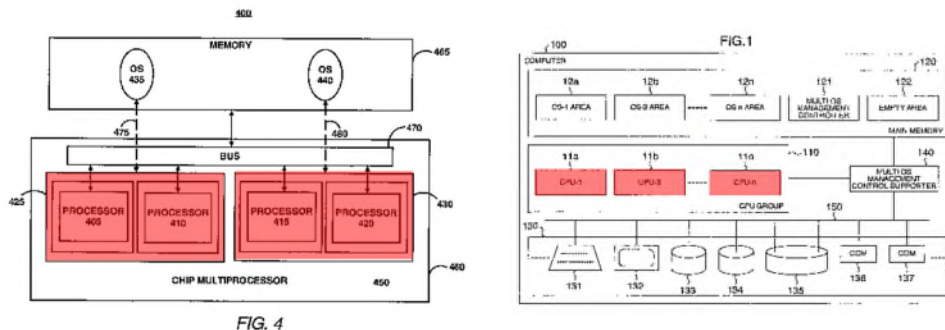


Further, as indicated in Section VII.A.1.b, it would be obvious to modify Asano's teachings with Joy to have CPU-1 through CPU-n be mounted on a single die. EX1002, ¶150.

As shown below, the '014 Patent discloses chip multiprocessor 450 (left, green). Similarly, Asano discloses a chip multiprocessor (right, green). EX1002, ¶151.



The '014 Patent discloses that chip multiprocessor 450 has multiple processors 405-420 (left, red). Similarly, Asano discloses that CPU group 110 can include *n* number of CPUs, such as CPU-1 11a, CPU-2 11b, all the way up through CPU-n 11n (right, red). EX1002, ¶152.



Further, as indicated in Section VII.A.1.b, it would be obvious to modify Asano's teachings with Joy to have CPU-1 through CPU-n be mounted on a single die. EX1002, ¶153.

Thus, to the extent "processor means" is construed under the agreed-upon construction, Asano-Joy still teaches this limitation. EX1002, ¶154.

Furthermore, as discussed above, the combined Asano-Joy system discloses that the processor group 110, which is a chip multiprocessor, executes a plurality of operating systems from the multiple operating systems (OS-1 through OS-n) thereby performing the claimed function. *See supra* Sections VII.A.1.a, VII.A.1.d; EX1005, ¶¶[0030]-[0031], FIGS. 1-2; *see also* EX1005, ¶[0001] ("The present invention relates to a computer system and a method for controlling *a computer system in which a plurality of operating systems (OS) operate on one computer*, and in particular, to a computer system and a method for controlling a computer system in which computer resources can be efficiently used or operated in an operating state of a plurality of operating systems"); EX1002, ¶155.

Accordingly, the Asano-Joy combination discloses and/or suggests this limitation. EX1002, ¶156.

- c. and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means**

The Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.d. *See supra* Section VII.A.1.d; EX1002, ¶157.

- d. memory means for storing said plurality of operating system means**

The Asano-Joy combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.c and for the additional reasons explained below. *See supra* Section VII.A.1.c; EX1002, ¶158.

The Asano-Joy combination discloses and/or suggests a “memory means for storing said plurality of operating system means” as claimed. EX1002, ¶159; *see also supra* Section VI.F.

The '014 patent identifies as corresponding structure “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” *See supra* Section VI.F. The Asano-Joy combination discloses and/or suggests this structure. For example, Asano’s system includes a main memory 120 that includes distinct areas, 12a to 12n, for storing operating systems (e.g., OS-1 through OS-n). *See supra* Section

VII.A.1.c; EX1005 ¶[0030] (“In FIG. 1, a computer system 100 includes a processor group 110, a main memory 120,”), ¶[0031] (“The main memory 120 includes main memory areas 12 a to 12 n independent of each other. The areas 12 a to 12 n are allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n). The main memory 120 further includes a main storage area 121 for the multiple operating system management controller and an empty area 122 to be reserved.”), ¶[0032] (“The external storage 133 is allocated to OS-1, the external device 134 is allocated to OS-2, the disk device 135 is shared between OS-1 and OS-2”). EX1002, ¶160.

A POSITA would understand that “main memory 120” is a conventional computer memory and can be construed to include any of “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” EX1002, ¶161.

To the extent the Asano’s main memory is not found to explicitly teach the sort of memory defined above in Section VI.F, it would have at a minimum been a mere obvious design choice to make use of such conventional memory. EX1002 ¶162. For example, the use of magnetic media, optical media, random access memory (RAM), and read-only memory (ROM) were well-known and conventional options for memory. *See, e.g.*, EX1015, 5:60-66 (explaining that

operating systems are typically held in storage devices such as magnetic or optical disk drives); EX1016, 5:39-43 (explaining that operating systems may be stored in storage devices such as a “hard disk, magnetic disk 48, optical disk 52, ROM 38, or RAM 40”); EX1002, ¶162.⁶

Further, should there be any doubt that main memory 120 can be construed in this manner, Joy explicitly discloses an “on-chip L2 cache SRAM 1124,” in its a single-chip dual-processor vertically-threaded processor 1100 design. The SRAM 1124 is “shared between the first vertical multithreading processor 1102 and the second vertical multithreading processor 1104.” EX1002, ¶163.

Thus, the Asano-Joy combination discloses the corresponding structure. EX1002, ¶164.

Furthermore, as discussed above, the combined Asano-Joy system discloses that main memory 120 that includes distinct areas, 12a to 12n, for storing operating

⁶ Petitioner relies on the teachings of Asano and Joy only for the limitations of claim 1. Exhibits 1015-1016 demonstrate what a POSITA would have known at the time of the alleged invention of the '014 patent regarding well-known and conventional types of memory useful for storing operating systems.

systems (e.g., OS-1 through OS-n) thereby disclosing the claimed function. *See supra* Section VII.A.1.c; EX1002, ¶165.

Accordingly, the Asano-Joy combination discloses this limitation. EX1002, ¶166.

7. Claim 13

a. The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems

Claim 13 varies slightly from claim 3 (“wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems”) in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section VII.A.2. The Asano-Joy combination discloses a “processor means” (*see supra* Section VII.A.6.b) and “memory means” (*see supra* Section VII.A.6.d). EX1002, ¶167.

Accordingly, the combined Asano-Joy system discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section VII.A.2; EX1002, ¶168.

8. Claim 15

- a. The apparatus of claim 12, wherein each of said processors of said processing means is operable to execute a distinct one of said plurality of operating system means**

Claim 15 varies slightly from claim 5 in that it recites a “processor means” and “memory means” while claim 5 does not. *See supra* Section VII.A.3. As discussed above, the combined Asano-Joy system discloses a “processor means.” *See supra* Section VII.A.6.b; EX1002, ¶169.

Accordingly, the combined Asano-Joy system discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section VII.A.3; EX1002, ¶170.

B. Ground 2: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Asano and Babaian⁷

1. Claim 1

a. Limitation 1.a

Asano discloses this limitation. *See supra* Section VII.A.1.a; EX1002, ¶172.

⁷ The subheadings in Section VII.A provide the claim language for all corresponding claims and claim limitations in Section VII.B

b. Limitation 1.b

The Asano-Babaian combination discloses and/or suggests this limitation. EX1002, ¶173.

Asano discloses a computer system that includes a processor group that includes multiple processors, but Asano does not disclose “multiple processors mounted on a single die” as claimed. *See supra* Section VII.A.1.b; EX1002, ¶174.

To the extent that Asano does not explicitly provide that the multiple processors are mounted on a single die, Babaian teaches doing so. Specifically, Babaian discloses multiple processor mounted on a single die. For example, Babaian discloses “a Single-chip Multiprocessor System 700 suited for parallel execution” that includes “four processors 710.” EX1007, 7:1-5; EX1002, ¶175.

Specifically, Babaian discloses multiple processors mounted on a single die. For example, Babaian discloses a horizontal threaded processor architecture that “combines multiple processors on a single integrated circuit die.” EX1006, 7:4-6; EX1002, ¶176.

A POSITA would have been motivated in light of Babaian to configure the system in Asano (as discussed above for claim limitation 1.a) so that its multiple processors are “mounted on a single die,” as claimed. EX1002, ¶177. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. See

KSR, 550 U.S. at 416-18. A POSITA would have recognized that Babaian and Asano disclose features in a similar technological field. EX1002, ¶177.

Accordingly, a POSITA would have had reason to consider the teachings of Babaian when implementing Asano's system, given that Babaian discloses the benefits of using multiple processors mounted on a single die in a computer system like the system disclosed in Asano. EX1002, ¶177.

Babaian discloses several advantages of using a single chip multiprocessor that are applicable to any multiprocessing architecture, including Asano. EX1002, ¶178. For example, Babaian explains that "[t]he single chip multiprocessor system substantially increases the performance due to parallel and macro-scheduled execution of a multitude of program streams, high performance and efficiently synchronized data exchange between the processors." EX1007, 4:31-36. Babaian also explains that only a "few single-chip multiprocessor systems 700" are needed to provide a large multiprocessor system with "tens or hundreds of processors." EX1007, 7:34-39' EX1002, ¶178.

Babaian's teaching of performance improvements inherently result from parallel and macro-scheduled execution of a multitude of program streams inherently result from a single chip multiprocessor would further motivate a POSITA to arrange Asano's processors on a single die. EX1002, ¶179. Likewise,

Asano teaches that positioning multiple processors on a single die results in high performance and efficiently synchronized data exchange between the processors. EX1007, 4:32-35. This teaching likewise motivates a POSITA to arrange Asano's processors on a single die so as to improve performance and efficiency of data exchange between processors. EX1002, ¶179.

Accordingly, a POSITA would have had reason to consider the teachings of Babaian when implementing Asano's system. EX1002, ¶180.

Further, as discussed below for claim limitation 1.d, Asano discloses that the processor group operates a plurality of operating systems where the system may allocate each processor to another operating system at a predetermined interval of time (e.g., switching between operating systems). *See infra* Section VII.B.1.d; *see also supra* Section VII.A.1.d; EX1005 ¶¶[0030]-[0031], [0035]. A POSITA would have thus recognized that implementing Babaian's teachings regarding the multi-processor on a single die configuration with the system in Asano would have allowed the combined system to allocate each processor quickly (via the flexible assignment of each processor) to another operating system. EX1002, ¶181; *see also infra* Section VII.B.1.d; EX1005 ¶[0035] ("Each CPU is allocated to another operating system at a predetermined interval of time."); EX1007, 13:65-14:3. A POSITA facing the wide range of needs created by developments in the technical field of Asano and Babaian would have appreciated the benefits of using the single

chip multiprocessor configuration as described in Babaian in Asano's system. Indeed, a POSITA would have appreciated that the benefits associated with assigning one or more multiple processors on a single die, as discussed by Babaian, would be similarly applicable to Asano. EX1002, ¶181; *see also supra* Section VII.B.1.b; EX1007, 3:56-62, 4:8-36. For example, a POSITA would have immediately recognized that mounting multiple processors on a single die in the Asano multiprocessor system would have increased the system's performance substantially when executing programs, improved the efficiency of data exchange between processors on the same die, and reduced the number of chips needed to implement a multiprocessor system. EX1002, ¶181; EX1007, 4:31-35.

In addition, the benefits of having multiple processors on a single die in a multi-processor system (such as the system in Asano) were well known in the art before the '014 patent thereby further motivating a POSITA to apply Babaian's teachings regarding a single chip multiprocessor to Asano. EX1002, ¶182; EX1007, 7:34-39; EX1008, 1; EX1009, Abstract; EX1010, 1:37-47; EX1011,

292.⁸ Thus, placing Asano's multiple processors on a single die would have been a common-sense approach. EX1002, ¶182.

Therefore, based on Babaian's disclosure and the knowledge in the art, it would have been obvious for the processor group 110 in the combined Asano-Babaian system to be mounted on a single die. EX1002, ¶183. Furthermore, using multiple processors mounted on a single die in the above combination would have been a straightforward application of basic computer design principles for designing a multi-processor system, as acknowledged by the '014 patent itself. EX1001, 1:34-42. Such knowledge, coupled with the disclosures/suggestions of Babaian, would have motivated a POSITA to use multiple processors mounted on a single die in the Asano system to not only reduce the size of the computer system but also provide flexible assignment of the processors for the execution of multiple operating systems as one benefit of the combination. EX1002, ¶183.

⁸ To show that claim 1 is obvious, Petitioner relies here on the teachings of Asano and Babaian only in Section VII.B. EX1008-1011 demonstrate what a POSITA would have known at the time of the alleged invention of the '014 patent regarding the benefits of having multiple processors on a single die.

The combination of Asano with Babaian would have involved the use of known technologies (e.g., computer chip architectures for computer systems), design concepts, and processes to obtain the foreseeable result of a computer system utilizing multiple processors mounted on a single die, which would provide fast switching between executing threads originating from multiple operating systems. EX1002, ¶184. A POSITA would have been skilled and knowledgeable to configure Asano's system to implement a system using multiple processors mounted on a single die while considering any known design and related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. EX1002, ¶184. For example, a POSITA would have been motivated based on such disclosures to configure Asano's system where the CPU group 110 includes multiple processors (11a through 11n) on a single die. EX1002, ¶184. Thus, a POSITA would have had a reasonable expectation of success in the above modification. *See Pfizer*, 480 F.3d at 1364; EX1002, ¶184.

Accordingly, the combination of Asano and Babaian discloses and/or suggests this limitation. EX1002, ¶185.

c. Limitation 1.c

The Asano-Babaian combination discloses and/or suggests this limitation. EX1002, ¶186.

For example, Asano discloses that the computer system 100 includes multiple operating systems (e.g., OS-1 to OS-n) that reside in the main memory connected to the processor group that includes multiple processors. *See supra* Section VII.A.1.c. Accordingly, for reasons similar to those explained above, the Asano-Babaian combined system would have been further configured such that multiple operating systems reside in a memory, which is connected to the multiple processors mounted on a single die, as claimed. EX1002, ¶187; *see supra* Section VII.B.1.b.

Furthermore, a POSITA would have understood that placing the multiple processors on a single chip would not have detracted from or changed the connection between the processors and memory in Asano. EX1002, ¶188.

Thus, the Asano-Babaian combination discloses and/or suggests this limitation. EX1002, ¶189.

d. Limitation 1.d

The Asano-Babaian combination discloses and/or suggests this limitation. EX1002, ¶190.

Asano discloses that each of the processors in the processor group is allocated to execute an operating system. *See supra* Section VII.A.1.d. Asano further discloses that each processor in the group includes a switching mechanism that provides capability for the processor to switch between multiple operating

systems, where the operating systems are simultaneously running in the system.

See supra Section VII.A.1.d; EX1005 ¶[0035]; EX1002, ¶191.

Accordingly, for reasons similar to those explained above regarding Asano's disclosures, the Asano-Babaian combined system would have been further configured such that each of the multiple processors in the single die executes an operating system from the multiple operating systems, and two or more of the multiple processors in the single die are capable of simultaneously executing two or more operating systems, as claimed. *See supra* Sections VII.A.1.d, VII.B.1.b; EX1002, ¶192.

Additionally, as explained above, Babaian's multiple processors mounted on a single die include the ability for each processor to be flexibly assigned for execution of a task. *See supra* Section VII.B.1.b; *see also* EX1007, 13:65-14:3. Accordingly, a POSITA would have understood that the combined Asano-Babaian system includes both the software and hardware to allocate each processor to another operating system by flexible assignment of each of the processors between multiple operating systems. EX1002, ¶193.

Thus, the Asano-Babaian combination discloses and/or suggests this limitation. EX1002, ¶194.

2. Claim 3

The Asano-Babaian combination discloses and/or suggests this limitation.
EX1002, ¶195.

Asano discloses that the multiple processors are connected to memory via a bus in order to execute the multiple operating systems. *See supra* Section VII.A.2. Accordingly, a POSITA would have understood that the system in the Asano-Babaian combination would have included a bus that connects the multiple processors mounted on a single die with the main memory in order to execute instructions from the various operating systems and to process data. EX1002, ¶196.

3. Claim 5

The Asano-Babaian combination discloses and/or suggests this limitation.
EX1002, ¶197.

For example, Asano discloses a configuration where each of the processors in the processor group executes a distinct operating system. *See supra* Section VII.A.3. Accordingly, a POSITA would have understood that the system in the Asano-Babaian combination would have also included such a configuration.
EX1002, ¶198.

4. Claim 7

a. Limitation 7.a

To the extent that the preamble of claim 7 is limiting, the Asano-Babaian combination discloses the limitations of this preamble for at least the reasons as above for claim limitation 1.a. *See supra* Sections VII.B.1.a; *see infra* Section VII.B.6.b-d; EX1002, ¶199.

b. Limitation 7.b

This limitation 7.b varies from limitation 1.b in that it recites “groups” while limitation 1.b does not. *See supra* Section VII.B.1.b; EX1002, ¶200.

The combined Asano- Babaian system discloses limitation 7.b for at least the same reasons discussed above from limitation 1.b because each of the processors in the processor group 221, which would have been processors on a single die, are allocated into a plurality of groups. *See supra* Sections VII.B.1.b, VII.B.5; EX1002, ¶201.

c. Limitation 7.c

This limitation 7.c varies from limitation 1.c in that it recites “groups” while limitation 1.c does not. *See supra* Section VII.B.1.c; EX1002, ¶202.

The combined Asano-Babaian system discloses limitation 7.c for at least the same reasons discussed above from limitation 1.c. *See supra* Section VII.B.1.c; EX1002, ¶203.

d. Limitation 7.d

This limitation 7.d varies from limitation 1.d in that it recites “groups” while limitation 1.d does not. *See supra* Section VII.B.1.d; EX1002, ¶204.

The combined Asano-Babaian system discloses limitation 7.d for at least the same reasons discussed above from limitation 1.d. *See supra* Sections VII.B.1.d, VII.B.5; EX1002, ¶205.

5. Claim 11

Claim 11 varies from claim 5 in that it recites “groups” while claim 5 does not. *See supra* Section VII.B.3; EX1002, ¶206.

The combined Asano-Babaian system discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section VII.B.3; EX1002, ¶207.

6. Claim 12

a. Limitation 12.a

To the extent that the preamble of claim 12 is limiting, *Asano* discloses the limitations of this preamble for at least the reasons as above for limitation 1.a. (*See supra* Section VII.B.1.a; *infra* Sections VII.B.10.b-d; EX1002, ¶208.

b. Limitation 12.b

The Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from limitations 1.b, 1.d and limitation 12 in Ground 1. *See supra* Sections VII.A.6.b, VII.B.1.b, VII.B.1.d; EX1002, ¶209.

For example, for the same reasons as explained above for claim limitation 12 in Ground 1, the combined Asano-Babaian system would have included an operating system means (i.e., operating system 1 (OS-1) to operating system n (OS-n)). *See supra* Section VII.A.6.b; EX1002, ¶210.

Furthermore, as discussed above for claim limitation 12 in Ground 1, the combined Asano-Babaian system would have also included a processor means . *See supra* Section VII.A.6.b; EX1002, ¶211.

c. Limitation 12.c

The Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.d and claim limitation 12 from Ground 1. *See supra* Sections VII.A.6.c, VII.B.1.d; EX1002, ¶212.

d. Limitation 12.d

The Asano-Babaian combination discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.c and claim

limitation 12 from Ground 1. *See supra* Sections VII.A.6.d, VII.B.1.c; EX1002, ¶213.

7. Claim 13

Claim 13 varies from claim 3 in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section VII.B.2; EX1002, ¶214.

As discussed for limitations 12.b and 12.d, the combined Asano-Babaian system discloses a “processor means” (*see supra* Section VII.B.6.b) and “memory means” (*see supra* Section VII.B.6.d). EX1002, ¶215.

Accordingly, the combined Asano-Babaian system discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section VII.B.2; EX1002, ¶216.

8. Claim 15

Claim 15 varies from claim 5 in that it recites a “processor means” and “memory means” while claim 5 does not. *See supra* Section VII.B.3; EX1002, ¶217.

As discussed for claim limitation 12.b, the combined Asano-Babaian system discloses a “processor means.” *See supra* Section VII.B.6.b; EX1002, ¶218.

Accordingly, the combined Asano-Babaian system discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section VII.B.3; EX1002, ¶219.

VIII. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. *General Plastic* Denial is Inappropriate

The Board has previously instituted *inter partes* review of the '014 patent; however, the Board never issued a final written decision because the parties to the instituted *inter partes* review filing a joint motion to terminate the proceedings. As such, the '014 patent has not previously been substantively challenged in a post-grant proceeding. Further, the prior art in this Petition was not previously before the Examiner during prosecution of the '014 patent, such that the combinations of references presented in the grounds herein have not previously been presented to the Office. Accordingly, the *General Plastic* factors weigh against discretionary denial.

B. *Fintiv* Discretionary Denial is Inappropriate

The *Fintiv* factors (enumerated below) weigh against discretionary denial. IPR2020-00019, Paper 11, 5-6 (PTAB Mar. 20, 2020) (precedential). Recent board decisions applying these factors confirm discretionary denial is not warranted here. *Apple Inc. v. Maxell, Ltd.*, IPR2020-00204, Paper 11 at 11-20 (PTAB Jun. 19, 2020); *Sand Revolution II, LLC v. Cont'l Intermodal Group-Trucking LLC*,

IPR2019-01393, Paper 24 at 6-14 (PTAB Jun. 16, 2020); *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper 10 at 5-22 (PTAB Jun. 15, 2020).

1. *Fintiv* Factor 1: Institution Will Enable a Stay

The litigation based in the Western District of Texas is early on. Institution will enable the Board to resolve the issue of validity, and a finding of invalidity will relieve the Western District of Texas of the need to continue with the companion litigation for the '014 patent. Apple has acted expeditiously in filing this Petition, and the opportunity for such simplification increases the likelihood that the court will grant a stay in view of IPR institution. *Sand Revolution II LLC v. Continental Intermodal Group–Trucking LLC*, IPR2019-01393, Paper 24, 7 (June 16, 2020); *see also Dish Network LLC v. Broadband iTV, Inc.*, IPR2020- 01359, Paper 15 (Feb. 12, 2021) (“It would be improper to speculate, at this stage, what the Texas court might do regarding a motion to stay....”).

2. *Fintiv* Factor 2: District Court Schedule

If the Board institutes trial, the statutory deadline for a final written decision will be in approximately June/July 2024, depending on the timing of the Notice of Filing Date Accorded. District court trial dates in contrast shift, even in normal times. *Mylan Pharma. Inc. v. Sanofi-Aventis Deutschland GMBH*, IPR2018-01680, Paper 22 at 17 (PTAB Apr. 3, 2019).

The court has tentatively set trial for April 8, 2024. *See* EX1019. There is no guarantee trial will commence on April 8, 2024. Further, “a court’s general ability to set a fast-paced schedule is not particularly relevant,” especially where “the forum [W.D.Tex.] itself has not historically resolved cases so quickly.” *In re Apple Inc.*, 979 F.3d 1332, 1344 (Fed. Cir. 2020); *see also Dish Network LLC v. Broadband iTV, Inc.*, IPR2020-01280, Paper 17, 13-16 (PTAB Feb. 4, 2021). Indeed, the Federal Circuit found error in reliance on the case’s scheduled trial date. *In re Apple Inc.*, 979 F.3d at 345. It is thus improper to conclude that the district court trial will proceed according to the current schedule. *See also Sand Revolution*, IPR2019-01393, Paper 24 at 8-9 (“it is unclear that the court in the related district court litigation will adhere to any currently scheduled jury trial date or, if it is changed, when such a trial will be held”). The coronavirus pandemic has added additional uncertainty to the tentative trial date.

Further, a recent study analyzing discretionary denials issued between May and October 2020 found that, out of 55 discretionary denials during that period, only seven cited a trial date that proved accurate. EX1021. And in four of those instances, the cited date was correct because trial had already occurred when the Board denied institution. *Id.* (citations omitted). The study notes that, when evaluating future trial dates, the Board was incorrect 94% of the time. *Id.* Indeed, in the seminal *NHK* and *Fintiv* cases, after the Board denied institution, the

associated trial dates were delayed after expected final written decision dates. *See Mylan Pharmaceuticals Inc. v. Sanofi-Aventis Deutschland GmbH*, IPR2018-01680, Paper 22 at 17, n. 6 (PTAB Apr. 3, 2019) (“In the district court case running parallel to *NHK Spring*, the court ultimately moved the trial date back six months, illustrating the uncertainty associated with litigation schedules.”); *Fintiv, Inc. v. Apple Inc.*, 6:21-CV-00926-ADA, Dkt. 412, Order (EX1022) (resetting *Fintiv* trial to January 10, 2022, nearly **one year and two months after the initial trial date** set in the initial scheduling order, and eight months after a FWD would have issued if the Board had instituted in *Apple Inc. v. Fintiv*, IPR2020-00019). Further, even after the cited order in *Fintiv, Inc. v. Apple Inc.* was issued, the trial continued to be delayed time and time again.

In contrast, and despite the pandemic, the Board has adhered to the one-year statutory deadline for final decisions prescribed by 35 U.S.C. § 316(a)(11). *Sand Revolution*, IPR2019-01393, Paper 24 at 8-10. Overall, this factor does not support discretionary denial. *See id.*

3. *Fintiv* Factor 3: Parallel Proceeding Considerations

The court in the underlying litigation has not yet issued any substantive order related to the challenged patent. In the underlying litigation, the District Court held the claim construction hearing and issued an order construing terms on April 6, 2023. Most notable from this hearing – none of the terms at issue

involved the '014 patent. Further, virtually no substantive discovery has taken place.⁹

Moreover, any investment in the district court proceeding is a result of Patent Owner's strategic choice of forum in the Western District of Texas. Almost no other court would be as far along in the trial calendar where, as here, a petition was filed approximately three (3) months before the one-year statutory bar date. Overall, this factor weighs against discretionary denial.

4. *Fintiv* Factor 4: The Petition Raises Unique Issues

To eliminate any potential overlap of issues, Petitioner concedes that if the Board institutes IPR, Petitioner will not assert invalidity of the challenged claims in the district court litigation using the grounds asserted in this petition. This stipulation weighs against discretionary denial. *See Sand Revolution*, IPR2019-01393, Paper 24 at 11-12; *Maxell*, IPR2020-00204, Paper 11 at 15-16.

5. *Fintiv* Factor 5: The Petition Will Enable Cancellation of Claims that Might Be Reasserted

Apple's petition is potentially helpful to future defendants. Apple's status as both Petitioner and Defendant therefore is, at worst, a neutral factor. Institution

⁹ Some venue-specific discovery has occurred.

would serve overall efficiency, enabling the Board to determine invalidity of claims that Patent Owner might otherwise later assert against others.

Further, members of the Board have noted that *Fintiv* addresses only the scenario in which the petitioner is unrelated to a defendant in a parallel proceeding, finding this should weigh against denying institution, but that *Fintiv* “says nothing about situations in which the petitioner is the same as, or is related to, the district court defendant.” *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020-00122, Paper 15, at *10-11 (PTAB May 15, 2020) (APJ Crumbley, dissenting) (noting that disfavoring a “defendant in the district court” is “contrary to the goal of providing district court litigants an alternative venue to resolve questions of patentability”).

6. *Fintiv* Factor 6: Other Considerations Support Institution

While this patent has been previously challenged in a PTAB post-issuance proceeding by another party (*see supra* Section II.B), the PTAB never had the opportunity to decide the merits of the case despite instituting inter partes review, because the parties agreed to terminate the proceedings. Further, the Patent Office did not consider the prior art references asserted in this petition, Asano, Joy, and Babaian, during prosecution of the '014 patent application. And the strength of Petitioner’s patentability challenges on the preliminary record favor institution. *See Maxell*, IPR2020-00204, Paper 11 at 19 (considering such a circumstance).

In summary, the *Fintiv* factors altogether weigh against discretionary denial.

IX. CONCLUSION

For the foregoing reasons, Petitioner requests *inter partes* review of claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent.

Dated: April 12, 2023

Respectfully Submitted,

/Joseph W. Wolfe/

Joseph W. Wolfe

Registration No. 73,173

James Heintz

Registration No. 41,828

Table of Exhibits for U.S. Patent 6,874,014 Petition for *Inter Partes* Review

Exhibit	Description
1001	U.S. Patent No. 6,874,014
1002	Declaration of Dr. Martin G. Walker
1003	Curriculum Vitae of Dr. Martin G. Walker
1004	Prosecution History of U.S. Patent No. 6,874,014
1005	U.S. Patent Publication No. 2001/0044817 to Asano (“Asano”)
1006	U.S. Patent No. 6,542,991 to Joy et al. (“Joy”)
1007	U.S. Patent No. 7,143,401 to Babaian et al. (“Babaian”)
1008	Joch, “HOW-TO Chip Multiprocessing,” Computerworld, November 27, 2000
1009	Olukotun et al., “The Case for a Single-Chip Multiprocessor,” ACM SIGPLAN Notices, Vol. 31, Issue 9, Sept. 1996
1010	U.S. Patent No. 6,550,020 to Floyd et al. (“Floyd”)
1011	Barroso et al., “Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing”, Proc. 27th ACM Int’l Symp. Computer Architecture, 2000
1012	U.S. Patent No. 6,772,241 to George et al.
1013	U.S. Patent No. 6,526,462 to Elabd
1014	Hammond et al., “A Single-Chip Multiprocessor,” Computer, vol. 30, no. 9, pp. 79-85, Sept. 1997
1015	U.S. Patent No. 6,178,503 to Madden et al.
1016	U.S. Patent No. 6,085,247 to Parsons, Jr. et al.

1017	U.S. Patent No. 6,247,109 to Kleinsorge et al.
1018	U.S. Patent No. 6,397,242 to Devine et al.
1019	<i>Sonrai Memory Ltd. v. Apple Inc.</i> , Case No. 6:22-cv-00787-ADA, Dkt. 22, Agreed Scheduling Order.
1020	Thom Tillis letter to Andrew Hirschfeld dated November 2, 2021.
1021	“How reliable are trial dates relied on by the PTAB in the Fintiv analysis?”, Andrew Dufresne et al., 1600ptab.com (October 29, 2021).
1022	<i>Fintiv, Inc. v. Apple Inc.</i> , 6:21-CV-00926-ADA, Dkt. 41 2, Order.

CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,771 words, which is less than the 14,000 allowed under 37 CFR §42.24(a)(i).

Dated: April 12, 2023

Respectfully Submitted,

/Joseph Wolfe/
Joseph Wolfe
Attorney for Petitioner
Reg. No. 73,173

DLA Piper LLP (US)
One Liberty Place
1650 Market Street
Philadelphia, PA 19103
215-656-3300

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that, on April 12, 2023, a true and correct copy of the foregoing materials were served on Patent Owner electronically, by agreement, by emailing a copy to the following attorneys for the Patent Owner:

- Petition for *Inter Partes* Review of U.S. Patent No. 6,874,014 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 6,874,014 (EX1001 – EX1022)
- Power of Attorney
- Word Count Certification under 37 C.F.R. § 42.24(d)
- Appendix of claim listing

Brett Cooper
Drew B. Hollander
Jonathan Randy Yim
BC Law Group, P.C.
200 Madison Avenue, 24th Floor
New York, NY 10016

Seth Raymond Hasenour
BC Law Group, P.C.
607 Terrell Hill Dr., Suite Unit B
Austin, TX 78704
Sonrai_Counsel@b-clg.com

/Joseph W. Wolfe/
Joseph W. Wolfe
Reg. No. 73,173

APPENDIX

1. A multiprocessing system comprising:
multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,
wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.
2. The system of claim 1, wherein at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously.
3. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.
4. The system of claim 1, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.
5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.
6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups,
wherein each of said groups executes an operating system of said multiple
operating systems, and two or more of said plurality of processor groups are
capable of simultaneously executing two or more operating systems of said
multiple operating systems.

8. The system of claim 7, wherein each of said groups includes multiple
processors.

9. The system of claim 8, wherein said multiple processors in each of said
groups are connected to said memory via a bus to execute said multiple operating
systems.

10. The system of claim 8, wherein said multiple processors in each of said
groups are directly connected to said memory to execute said multiple operating
systems.

11. The system of claim 7, wherein each of said groups executes a distinct
operating system of said multiple operating systems.

12. A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means,
wherein said processor means includes a plurality of processors mounted on a

single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means; and

memory means for storing said plurality of operating system means.

13. The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

14. The apparatus of claim 12, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

15. The apparatus of claim 12, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

16. The apparatus of claim 12, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

17. The apparatus of claim 16, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

18. The apparatus of claim 16, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

19. The apparatus of claim 12, wherein at least one of said plurality of processors is operable to simultaneously execute two or more of said plurality of operating system means.