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Law Offices of James E. Eakin
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Menlo Park, CA 94026

FILING RECEIPT

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Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
** **SMALL ENTITY** **
Title

NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM

INVENTORS

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Sasa Trajkovic, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems employing Distributed Antenna Systems (DAS). More specifically, the present invention relates to a DAS which is part of a distributed wireless network

base station in which all radio-related functions that provide network coverage and/or capacity for a given area are contained in a small single unit that can be deployed in a location remote from the remaining distributed wireless network base station unit or units which are not performing radio-related functions. Multi-mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA, UMTS and WiMAX standards with advanced software configurability are features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multiple operators and multi-frequency bands per operator within a single DAS to reduce the costs associated with radio network equipment and radio network deployment.

BACKGROUND OF THE INVENTION

[002] Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users requires end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G and other advanced network capabilities. Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting these higher bandwidth requirements are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must deal with the limited availability of new spectrum,

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leverage existing spectrum, and ensure operation of all desired wireless technology standards. The processes of scarce resource optimization while ensuring a future-proof implementation must both take place at the same time during the transition phase, which usually spans many years and thus can encompass numerous future developments. Distributed open base station architecture concepts have evolved in parallel with the evolution of the various technology standards to provide a flexible, lower-cost, and more scalable modular environment for managing the radio access evolution. Such advanced base station architectures can generally be appreciated from Figure 1 [PRIOR ART], which shows an architecture for a prior art Distributed Wireless Network Base Station. In Figure 1, 100 is a depiction of a Distributed Wireless Network Base Station. The Base Transceiver Station (BTS) or Digital Access Unit (DAU) 101 coordinates the communication between the Remote Radio Head Units 102, 103 and the Base Station Controller (BSC). The BTS communicates with multiple Remote Radio Heads via optical fiber. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI), and the IR Interface standards introduced publicly-defined interfaces separating the Base Transceiver Station (BTS) or Digital Access Unit and the remote radio head unit (RRU) parts of a base station by employing optical fiber transport.

[003] The RRU concept constitutes a fundamental part of an advanced state-of-the-art base station architecture. RRU-based system implementation is driven by the need to achieve consistent reductions in both Capital Expenses (CAPEX) and Operating Expenses (OPEX), and enable a more optimized, energy-efficient, and greener base deployment. An existing application employs an architecture where a 2G/3G/4G base station is connected to RRUs over

multiple optical fibers. Either CPRI, OBSAI or IR Interfaces may be used to carry RF data to the RRUs to cover a sectorized radio network coverage area corresponding to a radio cell site. A typical implementation for a three-sector cell employs three RRU's. The RRU incorporates a large number of digital interfacing and processing functions. However, commercially available RRU's are power inefficient, costly and inflexible. Their poor DC-to-RF power conversion insures that they will need to have a large mechanical housing to help dissipate the heat generated. The demands from wireless service providers for future RRU's also includes greater flexibility in the RRU platform, which is not presently available. As standards evolve, there will be a need for multi-band RRUs that can accommodate two or more operators using a single wideband power amplifier. Co-locating multiple operators in one DAS system would reduce the infrastructure costs and centralize the Remote Monitoring Function of multiple Operators on the Network. To accommodate multiple operators and multiple bands per operator would require a very high optical data rate to the RRUs which is not achievable with prior art designs.

SUMMARY OF THE INVENTION

[004] The present invention substantially overcomes the limitations of the prior art discussed above. Accordingly, it is an object of the present invention to provide a high performance, cost-effective DAS system, architecture and method for an RRU-based approach which enables each of multiple operators to use multi-frequency bands. The present disclosure enables a RRU to be field reconfigurable, as presented in US Patent application US 61/172,642 (DW-1016P), filed 4/24/2009, entitled Remotely Reconfigurable Power Amplifier

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System and Method, US Patent application US 12/108,502 (DW-1011U), filed 4/23/2008, entitled Digital Hybrid Mode Power Amplifier System, US Patent application SN 61/288,838 (DW-1018P), filed 12/21/2009, entitled Multi-band Wideband Power Amplifier Digital Predistortion System, US Patent application SN 61/288,840 (DW-1019P), filed 12/21/2009, entitled Remote Radio Head Unit with Wideband Power Amplifier and Method, US Patent application SN 61/288,844 (DW-1020P), filed 12/21/2009, entitled Modulation Agnostic Digital Hybrid Mode Power Amplifier System, and US Patent application SN 61/288,847 (DW-1021P), filed 12/21/2009, entitled High Efficiency Remotely Reconfigurable Remote Radio Head Unit System and Method for Wireless Communications, all of which are incorporated herein by reference. In addition, the system and method of the present invention supports multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands, and multi-channels. To achieve the above objects, the present invention maximizes the data rate to the Remote Radio Head Unit in a cost effective architecture. Figures 2 and 3 depict a low power RRU and high power RRU. The RRUs depicted in Figures 2 and 3 can be extended to a multi-band and multi-channel configuration. Multi-band implies more than two frequency bands and multi-channel implies more than one output to an antenna system. Various embodiments of the invention are disclosed.

[005] An embodiment of the present invention utilizes a RRU Access Module. The objective of the access module is to de-multiplex and multiplex high speed data to achieve aggregate data rates sufficient for operation of a plurality of RRU Band Modules which are geographically distributed. An alternative embodiment of the present invention utilizes the physical separation of the RRU Band Modules from the RRU Access Module using an optical fiber cable,

Ethernet cables, RF cable and any other form of connection between the modules. In an alternative embodiment, a Remote Radio Unit comprised of one or more RRU Band Modules may be collocated with the antenna or antennas. In a further alternative embodiment, the RRU Access Module can also supply DC power on the interconnection cabling. In other aspects of the invention, control and measurement algorithms are implemented to permit improved network deployment, network management, and optimization.

[006] Applications of the present invention are suitable to be employed with all wireless base-stations, remote radio heads, distributed base stations, distributed antenna systems, access points, repeaters, distributed repeaters, optical repeaters, digital repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

[007] Appendix I is a glossary of terms used herein, including acronyms.

THE FIGURES

[008] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[009] Figure 1 [PRIOR ART] is a block diagram showing the basic structure of a prior art Distributed Wireless Base Station system.

[0010] Figure 2 is a block diagram showing a multi-channel High Power Remote Radio Head Unit according to one embodiment of the present invention.

[0011] Figure 3 is a block diagram multi-channel High Power Remote Radio Head Unit according to one embodiment of the present invention.

[0012] Figure 4 is a block diagram of a Remote Radio Head Unit high level system of the present invention.

[0013] Figure 5 is a block diagram of the Remote Radio Head Unit Access Module of the present invention.

[0014] Figure 6 is a Remote Radio Head Unit Band Module according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention is a novel Distributed Antenna System that utilizes a high speed Remote Radio Head Unit Access Module interconnected with Remote Radio Head Unit Band Module.

[0016] An embodiment of a Remote Radio Head Unit in accordance with the invention is shown in Figure 2. Fiber 1, indicated at 200A, is a high speed fiber cable that transports data between the BTS and the Remote Radio Head Unit. Fiber 2, indicated at 200B, is used to daisy chain other remote radio head units which are thereby interconnected to the BTS or DAU. The software-defined digital platform 216 performs baseband signal processing, typically in an FPGA or equivalent. Building block 203 is a Serializer/Deserializer. The deserializer portion extracts the serial input bit stream from the optical fiber 201 and converts it into a parallel bit stream. The serializer portion performs the inverse operation for sending data from the Remote Radio Head Unit to the BTS. In an embodiment, the two distinct bit streams communicate with the BTS using

different optical wavelengths over one fiber, although multiple fibers can be used in alternative arrangements. The deframer 204 deciphers the structure of the incoming bit stream and sends the deframed data to the Crest Factor Reduction Algorithm 209. The Crest Factor Reduction block 209 reduces the Peak-to-Average Ratio of the incoming signal so as to improve the Power amplifier DC-to-RF conversion efficiency. The waveform is then presented to the Digital Predistorter block 208. The digital predistorter compensates for the nonlinearities of the Power Amplifier 221 in an adaptive feedback loop. Digital Upconverter 210 filters and digitally translates the deframed signal to an IF frequency. The Framer 204 takes the data from the two digital downconverters 206, 207 and packs it into a Frame for transmission to the BTS over the optical fiber 201. Elements 211 and 212 are Analog to Digital converters that are used to translate the two analog receive signals into digital signals. The receiver comprises a diversity branch which contains a downconverter 217 and a Band Pass Filter 223. The main branch has a receiver path comprised of a duplexer 224 and a downconverter 218.

[0017] The power amplifier has an output coupler for extracting a replica of the output signal in the feedback path. The feedback signal is frequency-translated by downconverter 219 to either an IF frequency or baseband and presented to an Analog to Digital converter 213. This feedback signal is used in an adaptive loop for performing Digital Predistortion to compensate for any nonlinearities created by the power amplifier.

[0018] The Ethernet cable is used to locally communicate with the Remote Radio Head Unit. Switch 226 is used to allow easy access to either the FPGA or the CPU. DC power converters 228 and 229 are used to obtain the desired DC voltages for the Remote Radio Head Unit. Either an external voltage can be

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connected directly into the RRU or the DC power may be supplied through the Ethernet cable.

[0019] Although the description of the instant embodiment is directed to an application where a second optical fiber connection provides a capability for daisy chaining to other Remote Radio Head Units, an alternative embodiment provides multiple optical fiber connections to support a modified "hybrid star" configuration for appropriate applications which dictate this particular optical transport network configuration.

[0020] Figure 3 depicts a remote radio head unit. In at least some designs, this architecture offers benefits when the RF output power is relatively low. In the embodiment shown in Figure 3, digital predistrortion and crest factor reduction are not employed as was the case in Figure 2. Even though this topology shows a non-diversity configuration, a diversity receive branch can be added along with an additional transmitter path for development of a Multiple Input Multiple Output (MIMO) Remote Radio Head Unit.

[0021] The Remote Radio Head Unit high level system is shown in Figure 4. It comprises a Remote Radio Head Unit Access Module 400 which communicates directly with the BTS or DAU. The function of the Remote Radio Head Unit Access Module 400 is to route the high speed data (at any desired speed, e.g., such as 10 Gbps as illustrated in Fig. 4) (the "Data Speed") to the multiple Remote Radio Head Unit Band Modules and allows for local communications with them via Ethernet. A backplane 401 is used to interconnect the Remote Radio Head Unit Access Module 400 with the various Remote Radio Head Unit Band Modules 402,403,404,405 at any speed lower than the Data Speed (e.g., less than or equal to 3Gbps as illustrated in Fig. 4). The output ports of the Remote Radio Head Unit Band Modules are combined

and sent to an antenna for transmission. An alternative embodiment is described as follows. Although the description of instant embodiment is directed to applications for up to four Remote Radio Head Unit Band Modules, an alternative embodiment involves feeding a much larger quantity of Remote Radio Head Unit Band Modules with signals of various bandwidths at various frequency bands covering multiple octaves of frequency range, to support a wide range of applications including location-based services, mobile internet, public safety communications, private enterprise telecommunications and broadband, and other wireless applications. The system can in theory support an infinite quantity of RRUs. Also, the Remote Radio Head Unit Band Modules may be set up remotely to have RF power values selected based on the specific desired applications as well as location-specific radio signal propagation factors. A further alternative embodiment leverages the flexibility of the architecture shown in Figure 4 to provide a capability known as Flexible Simulcast. With Flexible Simulcast, the amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular RRU or group of RRUs by each RRU Access Module can be set via software control to meet desired capacity and throughput objectives or wireless subscriber needs.

[0022] The detailed topology of the Remote Radio Head Unit Access Module is shown in Figure 5. It comprises a Small form Factor Pluggable optic transceiver (SFP) 500 which operates on two distinct wavelengths, one for communicating from the BTS to the Remote Radio Head Unit Access Module and the other for communicating in the opposite direction. The SFP contains a Laser Diode for converting the electronic signal to a digital optical signal and an Optical detector for converting the digital optical signal into an electronic signal.

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A multiplexer/demultiplexer 501 converts the high speed data to multiple lower speed data paths for delivery to a FPGA 502. The multiplexer/demultiplexer 501 performs the opposite function when data is being sent back to the BTS or DAU. The framer/deframer 503 routes the data to the appropriate Remote Radio Head Unit Band Modules. An additional multiplexer/demultiplexer 506 allows for further expansion of lower speed Remote Radio Head Units. The number of Remote Radio Head units is only limited by the capability of the FPGA. Local communication with the Remote Radio Head Unit's Access Module's FPGA or the individual Remote Radio Head Unit Band Modules is via an Ethernet connection 508. Although the description of this embodiment is mainly directed to an application where a BTS and/or DAU (or multiple BTS and/or multiple DAU) feeds the Remote Radio Head Unit Access Module, an alternative embodiment is described as follows. The alternative embodiment is one where the digital optical signals fed to the Remote Radio Head Unit Access Module may be generated by an RF-to-Digital interface which receives RF signals by means of one or more antennas directed to one or more base stations located at some distance from the Remote Radio Head Unit Access Module. A further alternative embodiment is one where the signals fed to the Remote Radio Head Unit Access Module may be generated in a combination of ways; some may be generated by an RF-to-Digital interface and some may be generated by a BTS and/or DAU. Some neutral host applications gain an advantage with regard to cost-effectiveness from employing this further alternative embodiment. Although the optical signals fed to the Remote Radio Head Unit Access Module described in the preferred and alternative embodiments are digital; the optical signals are not limited to digital, and can be analog or a combination of analog and digital. A further alternative embodiment employs transport on one or multiple optical wavelengths fed to the Remote Radio Head Unit Access Module.

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[0023] The Remote Radio Head Unit Band Module is shown in Figure 6. It comprises a Software Defined Digital (SDD) section 610 and an RF section 622. An alternative embodiment employs a Remote Antenna Unit comprising a broadband antenna with RRU Band Module Combiner and multiple plug-in module slots, into which multiple RRU Band Modules intended for operation in different frequency bands are inserted. To provide an overall compact unit with low visual impact, this embodiment employs RRU Band Modules which each have a physically small form factor. One example of a suitably small form factor for the RRU Band Module is the PCMCIA module format. A further alternative embodiment employs RRU Band Modules where each has an integral antenna, and the embodiment does not require a common antenna shared by multiple RRU Band Modules.

[0024] In summary, the Neutral Host Distributed Antenna System (NHDAS) of the present invention enables the use of remote radio heads for multi-operator multi-band configurations , which subsequently saves hardware resources and reduces costs. The NHDAS system is also reconfigurable and remotely field-programmable since the algorithms can be adjusted like software in the digital processor at any time.

[0025] Moreover, the NHDAS system is flexible with regard to being able to support various modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, LTE and wireless LAN systems. This means that the NHDAS system is capable of supporting multi-modulation schemes, multi-bands and multi-operators.

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[0026] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

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What is Claimed is:

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ABSTRACT

A remote radio head unit (RRU) system for achieving high data rate communications in a Distributed Antenna System is disclosed. The Distributed Antenna System is configured as a Neutral Host enabling multiple operators to exist on one DAS system. The present disclosure enables a remote radio head unit to be field reconfigurable and support multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

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APPENDIX I

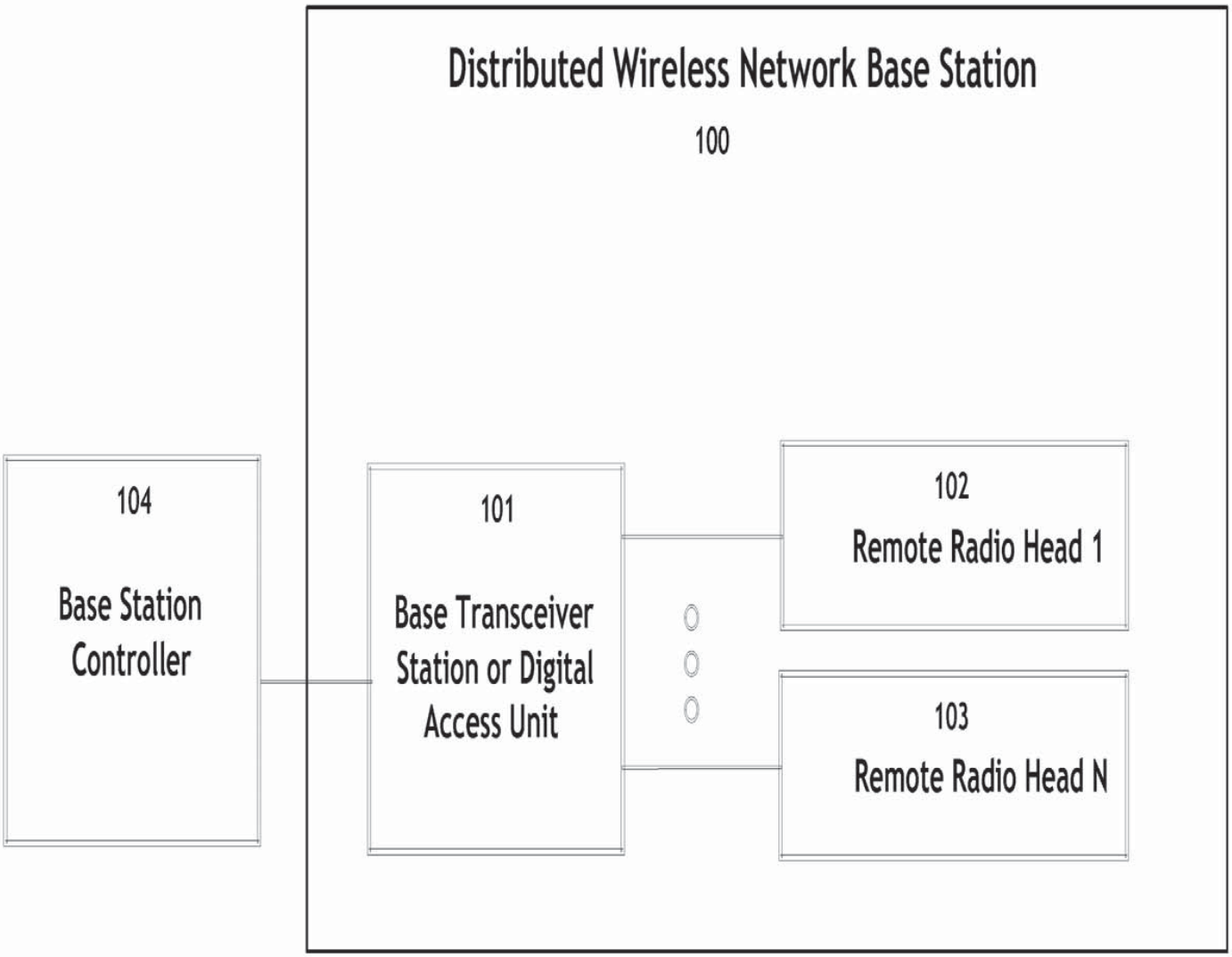
Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing

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PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRH	Remote Radio Head
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Figure 1: PRIOR ART



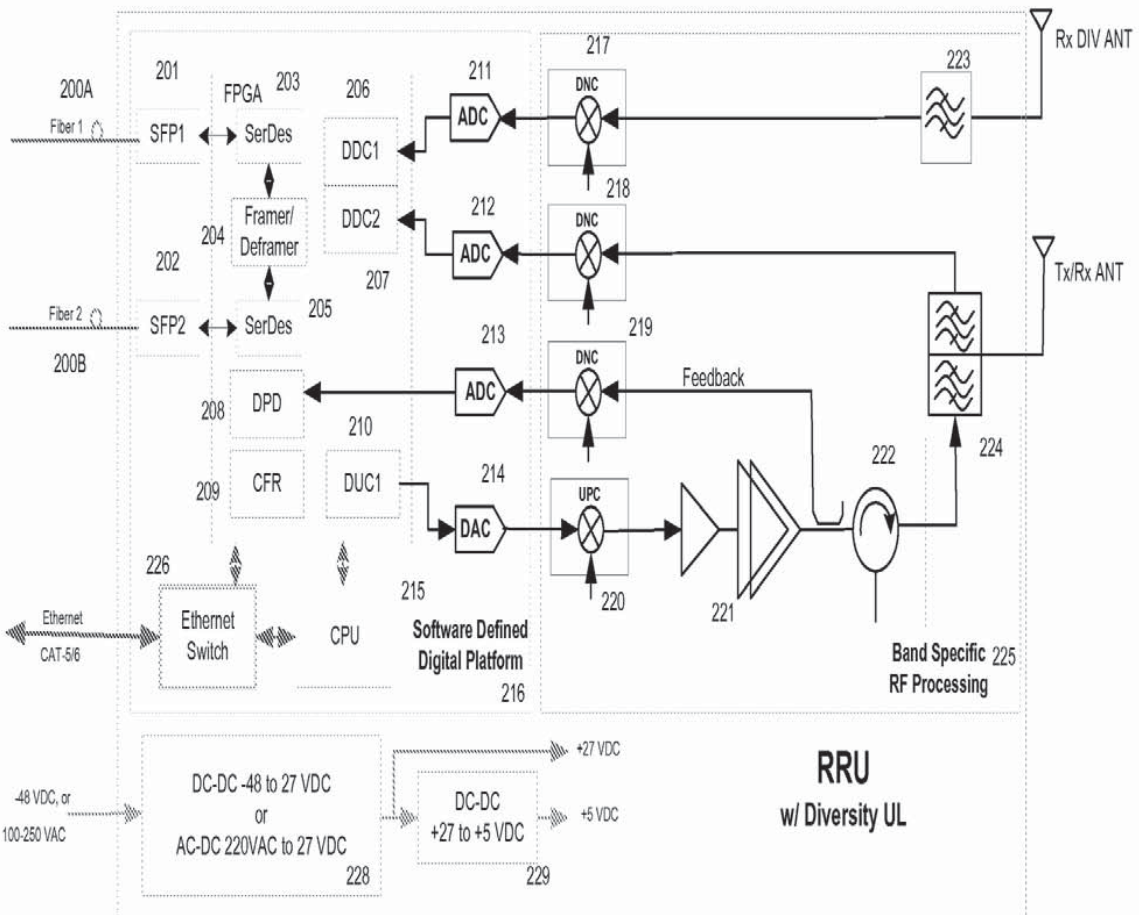


Figure 2. Remote Radio Head Unit

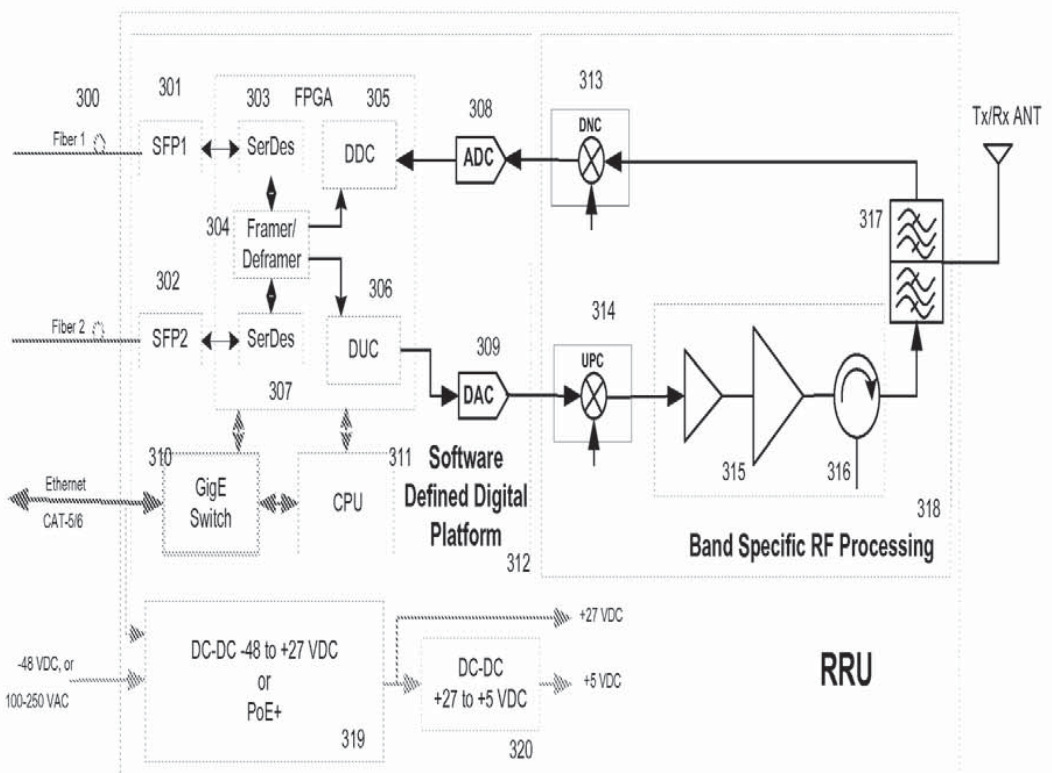


Figure 3. Remote Radio Head Unit

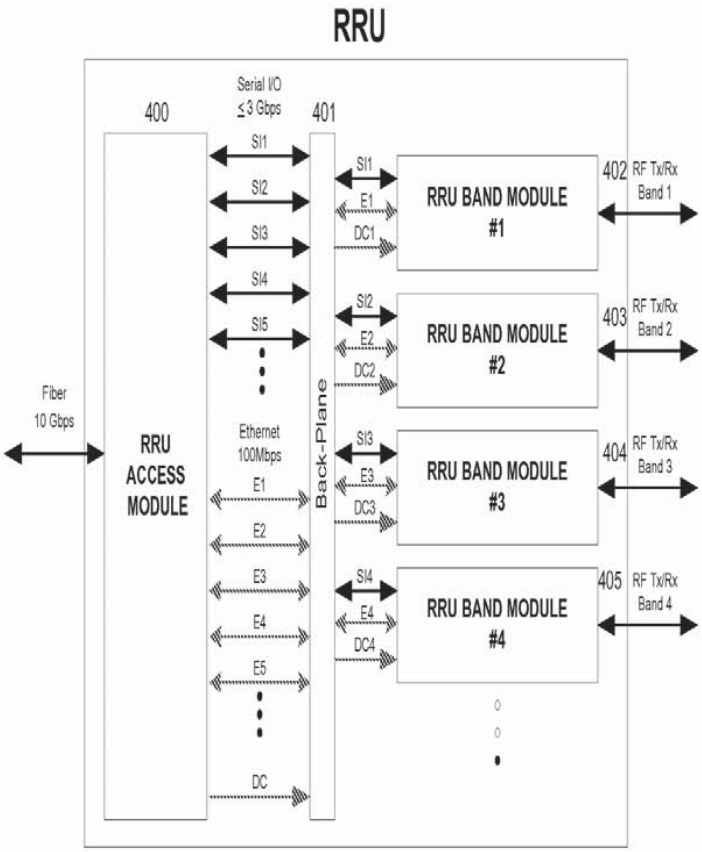


Figure 4. Remote Radio Head Unit High Level System

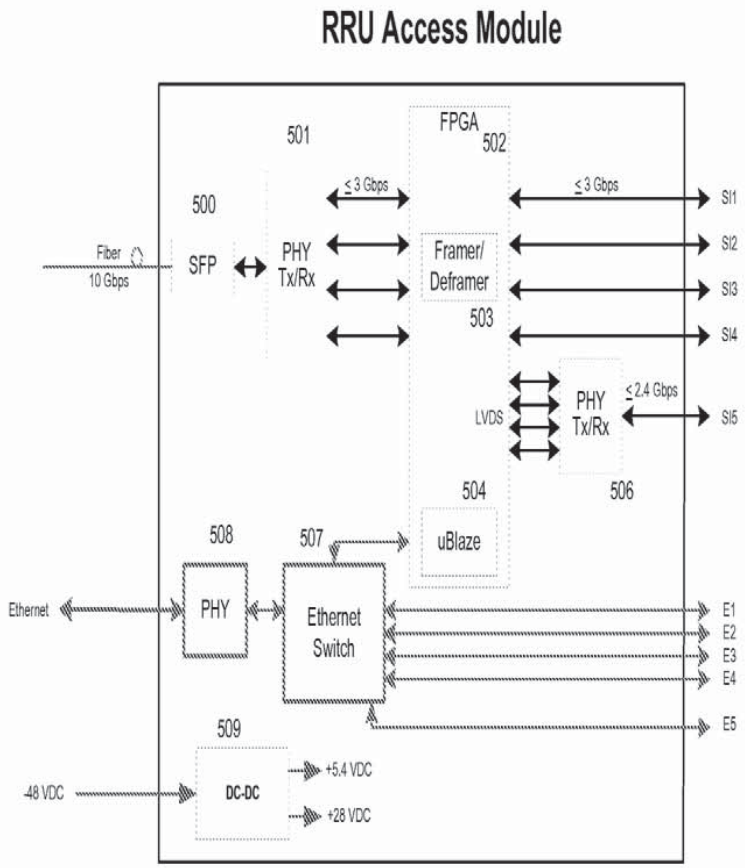


Figure 5. Remote Radio Head Unit Access Module

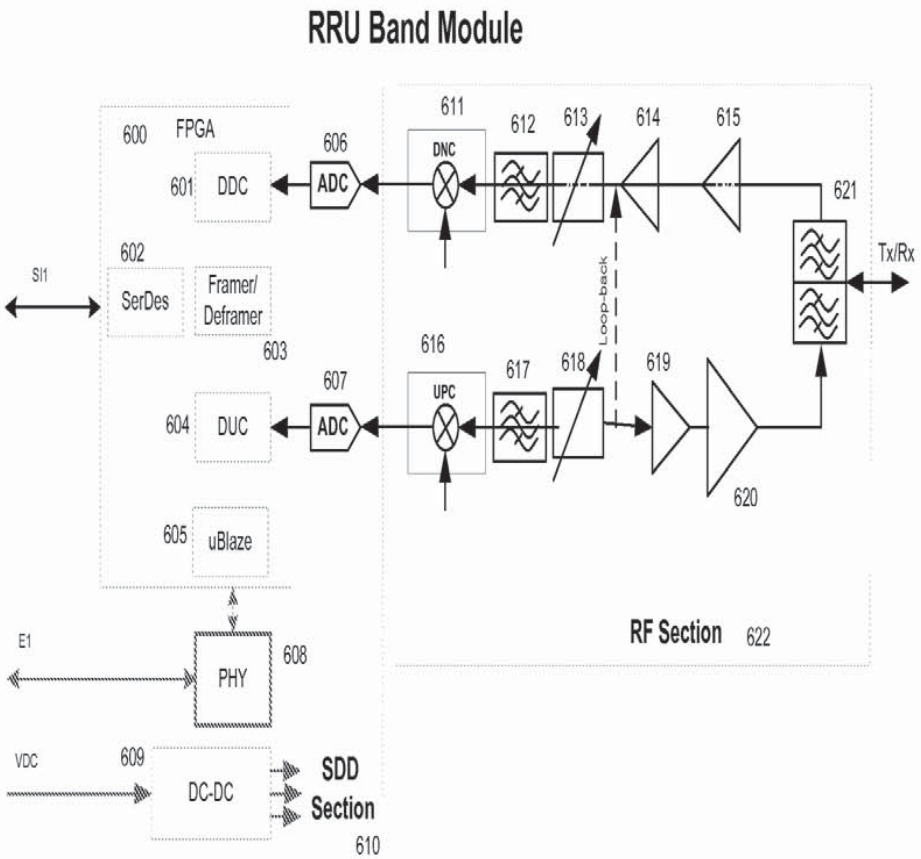


Figure 6. Remote Radio Head Unit Band Module

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PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS

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Ying Xiao, Citizen of China

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

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US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit. Multi-mode radios capable of operating according to GSM, HSPA, LTE, and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multi-frequency bands within a single RRU to economize the cost of radio network deployment.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G. Wireless and mobile technology standards are

evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years. Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution, Figure 6. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept constitutes a fundamental part of a state-of-the-art base station architecture. However, RRUs to-date are power inefficient, costly and inflexible. Their poor DC to RF power conversion insures that they will have a large mechanical housing. The RRU demands from the service providers are also for greater flexibility in the RRU platform. As standards evolve, there is a need for a software upgradable RRU. Today RRUs lack the flexibility and performance that is required by service providers. The RRU performance limitations are driven in part by the poor power efficiency of the RF amplifiers. Thus there has been a need for an efficient, flexible RRU architecture that is field reconfigurable.

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SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems in the prior art, and it is an object of the present invention to provide a high performance and cost effective method of multi-frequency bands RRU systems enabled by high linearity and high efficiency power amplifiers for wideband communication system applications. The present disclosure enables a RRU to be field reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels.

[002] To achieve the above objects, according to the present invention, the technique is generally based on the method of adaptive digital predistortion to linearize RF power amplifiers. Various embodiments of the invention are disclosed, including single band, dual band, and multi-band RRU's. Another embodiment is a multi-band multi-channel RRU. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[003] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations,

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distributed antenna systems, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram showing the basic form of a Remote Radio head unit system.

[007] Figure 2 is a block diagram showing a multi-channel Remote Radio Head Unit according to one embodiment of the present invention.

[007] Figure 3 is a block diagram showing polynomial based predistortion in a Remote Radio head system of the present invention.

[008] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a remote radio head unit system of the present invention.

[009] Figure 5 illustrates an analog modulator compensation block.

[0010] Figure 6 depicts schematically a variety of potential installation schemes for an RRU-based system architecture.

[0011] Figure 7 depicts a three-sector arrangement of an RRU system architecture comprising optical links to a base station server.

[0012] Figure 8 shows in block diagram form various DSP-based functions including crest factor reduction and digital predistortion.

[0013] Figure **9** is a Digital Hybrid Module with either an RF input signal or a baseband modulated signal or an optical interface according to another embodiment of the present invention.

[0014] Figure **10** is a Dual Channel Remote Radio head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present invention.

[0015] Figure **11** is an alternative Dual Channel Remote Radio Head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present

[0016] Figure **12** is an 8 channel Dual Band Remote Radio Head block diagram showing a digital hybrid module with an optical interface, and further comprises a calibration algorithm for insuring that each power amplifier output is time-aligned, phase-aligned and amplitude-aligned with respect to each other.

GLOSSARY

Acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector

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AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter

MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
SERDES	Serializer/Deserializer
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network.

DETAILED DESCRIPTION OF THE INVENTION

[001] The present invention is a novel RRU **s**ystem that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

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[002] Figure 1 is a high level block diagram showing the basic system architecture of what is sometimes referred to as a Remote Radio Head Unit, or RRU, which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention operates as a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a Remote Radio head Unit (RRU) hereinafter.

[003] Figure 2 illustrates in schematic block diagram form an embodiment of an eight channel (or n channel) RRU in which an input signal 200 is provided. Depending on the implementation, the input signal can take the form of an RF modulated signal, a baseband signal, or an optical signal. The input signal 200 is fed to a plurality of channels, where each channel includes a digital predistortion (DPD) controller, indicated at 201, 211 and 271, respectively. The DPD can be implemented in an FPGA in at least some embodiments. For each channel, the DPD outputs are fed to

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associated PA's 202, 212 and 272, respectively, and the PA outputs 203, 213 and 273 are fed back to that channel's DPD's.

[004] Figure 3 illustrates a polynomial-based digital predistorter function in the RRU system of the present invention. The PD in the present invention generally utilizes an adaptive LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3, and in embodiments disclosed from Figures 9-12 discussed hereinafter, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the RRU system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistorter algorithm based on the error between the reference input signal and the amplified power output signal.

[005] Figure 4 shows in block diagram form additional details of an embodiment including a DPD in accordance with the present invention and is discussed in greater detail hereinafter. In general, the input 400 is provided to the DPD 401. The output of the DPD is fed to a DAC 402 and thence to the PA 403. A feedback signal from the output of the PA is received by ADC 406, and the digital form is supplied to alignment logic 405, after which the aligned signal is provided to DPD estimator logic 404, which also receives an

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input from the output of the DPD 401. The output of the DPD estimator is then fed back to the DPD 401.

[006] Figure 5 illustrates an analog modulator compensation block. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11 , g12 , g21 , g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to an AQM's in-phase and quadrature ports, discussed hereinafter in connection with Figure 9.

[007] Figure 6 illustrates a plurality of possible implementations of an RRU-based system architecture, in with a base station server 600 is connected to, for example, a tower-mounted RRU 605, a rooftop-mounted RRU 610, and/or a wall-mounted RRU 615.

[008] Figure 7 illustrates an embodiment of a three-sector implementation of an RRU-based system architecture, in which a base station server 700 is optically linked to a plurality of RRU's 710 to provide adequate coverage for a site.

[009] Figure 8 illustrates in simplified form an embodiment of the DSP functionality of some implementations of the present invention. An input signal is fed to an interface 800, which can take several forms including OBSAI, CPRI or IR. The incoming signal is fed to a digital up-converter (DUC) 805 and then to CFR/DPD logic 810, such as an FPGA. The output of

the CFR/DPD logic 810 is then supplied to a DAC 815. The DAC provides an output signal to the analog RF portion 820 of the system, which in turn provides a feedback signal to a ADC 825, and back through the DSP block in the form of inputs to the CFR/DPD and a DDC 830. The DDC outputs a signal to the interface 800, which in turn can provide an output.

[0010] Figure 9 is a block diagram showing a more sophisticated embodiment of a RRU system, where like elements are indicated with like numerals. The embodiment of Figure 9 applies crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in US patent application SN 61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0011] Figure 9 is a block diagram showing a RRU system according to one embodiment of the present invention (the "FIG. 9. System"). RRU systems consist of three primary blocks: power amplifiers, baseband processing and an optical interface. The optical interface contains an optical to electrical interface for the transmit/receive mode. The optical interface 901,

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shown in Figure 9, is coupled to a FPGA. The FPGA 902 performs the functions of SERDES/Framer/De-Framer/Control and Management. This FPGA 902 interfaces with another FPGA 903 that performs the following Digital Signal Processing tasks: Crest Factor Reduction/ Digital Upconversion/Digital Downconversion and Digital Predistortion. Another embodiment will be to integrate 902 with 903 in a single FPGA. The Serializer/De-serializer (SERDES) module converts the high speed serial bit stream from the optical to electrical receiver to a parallel bit stream. The De-Framer decodes the parallel bit stream and extracts the In-phase and Quadrature (I/Q) modulation and delivers this to the digital signal processing module 903. The Control and Management module extracts the control signals from the parallel bit stream and performs tasks based on the requested information. The received I/Q data from the optical interface is frequency translated to an Intermediate Frequency in the Digital Upconverter Module (DUC). This composite signal then undergoes Crest Factor Reduction (CFR) in order to reduce the peak to average power ratio. The resultant signal is then applied to a Digital Predistorter in order to compensate for the distortion in the Power Amplifier module 905. The RRU operates in a receive mode as well as a transmit mode. The RRU receives the signal from the output duplexer and passes this signal to the Rx path or paths, depending on the number of channels. The received signal is frequency translated to an Intermediate Frequency (IF) in the receiver (Rx1 and Rx2 in Figure 10). The IF signal is further downconverted using a Digital Downconverter (DDC) module and demodulated into the In-phase and quadrature components. The recovered I/Q signal is then sent to the Framer module/ SERDES and prepared for transmission over the optical interface.

[0012] The FIG. 9. System has a multi-mode of RF or multi-carrier digital signal or optical at the input, and an RF signal at the output 910. The multi-mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode") or optical input (the "Optical-in Mode"). The FIG. 9. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 915, a power amplifier module 960, a receiver 965 and a feedback path 925.

[0013] The FPGA-based Digital part comprises either one of two digital processors 902,903 (e.g. FPGA), digital-to-analog converters 935 (DACs), analog-to-digital converters 940 (ADCs), and a phase-locked loop (PLL) 945. Since the FIG. 9 System has a multi-input mode, the digital processor has three paths of signal processing. For the baseband signal input path, the digital processor has implemented a digital up-converter (DUC), CFR, and a PD. For the optical input path, SERDES, Framer/ Deframer, digital up-converter (DUC), CFR, and PD are implemented. For the RF input path, analog downconverter, DUC, CFR and PD are implemented.

[0014] The Baseband-in Mode of FIG. 9 contains the I-Q signals. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

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[0015] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a wideband feedback which requires a very high speed ADC. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DACs . As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals 935, respectively. The gate bias voltage 950 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 935 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. The PLL 945 sweeps the local oscillation signal for the feedback part in order to translate the RF output signal to baseband, for processing in the Digital Module.

[0016] The power amplifier part comprises an AQM for real and complex signals (such as depicted in the embodiments shown in Figure 9) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental RRU system. One such Doherty power amplifier

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technique is presented in commonly assigned U.S. Provisional Patent Application SN 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0017] The feedback portion comprises a directional coupler, a mixer, a low pass filter (LPF), gain amplifiers and, and a band pass filter (BPF),. Depending upon the embodiment, these analog components can be mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the LPF, the gain amplifier, and the BPF which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the DET 970 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, which shows a polynomial-based predistortion algorithm and from Figure 4, which shows the primary adaptive predistorter blocks which can be used in some embodiments of the invention.

[0018] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a

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small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 907, hence maximizing the RRU system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC in the FPGA-based Digital portion and an extra UPC in the power amplifier part. The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0019] FIG. 9. is a block diagram showing a RRU system implemented with AQM according to another embodiment of the present invention (the "FIG. 9 System"). The digital processor of FIG. 9 System has implemented a CFR, a PD, and an analog quadrature modulator corrector (AQMC).

[0020] FIG. 9. is a block diagram showing a RRU system implemented with AQM and AQM-based Clipping Error Restoration Path according to another embodiment of th_e present invention (the "FIG. 9 System"). The Clipping Error Restoration Path in FIG. 9 System has two DACs in the FPGA-based Digital part and an AQM in lieu of the UPC in the power amplifier part.

[0021] Figure 10 is a block diagram showing a dual channel RRU implemented with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as $occu_{rs}$ in a $_{T}$ime

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Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. An additional switch is used for calibrating the Digital Predistorter for each power amplifier. Another embodiment of the RRU is extending its applications to multi-frequency bands. In an embodiment, a multi-frequency band (ie. 2 or more bands) implementation comprises adding additional channelized power amplifiers in parallel. The output of the additional power amplifiers will be combined in an N by 1 duplexer and fed to a single antenna, although multiple antenna can also be utilized in some embodiments. Another embodiment of the multi-frequency band RRU combines two or more frequency bands in one or more of the power amplifiers.

Figure 11 is a block diagram showing another embodiment of the dual channel RRU. In this embodiment the Rx switch is placed on the third port of the circulator, thereby reducing the insertion loss between the PA output and the duplexer.

Figure 12 is a block diagram showing an embodiment of an 8 channel RRU. In this embodiment, the feedback path consists of a receiver chain plus a wideband capture chain. The receiver chain is required when the RRU is switched to a receive mode. The wideband capture chain is required for capturing the wideband distortion of the power amplifier. In addition a channel calibration algorithm is required in order to insure that each power amplifier output is time, phase and amplitude aligned to each other.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA).

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Figure 1 shows the block diagram of linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The primary DPD blocks are shown in Figure 4.

Delay Estimation Algorithm:

The DPD estimator compares $x(n)$ and its corresponding feedback signal $y(n-\Delta d)$ to find the DPD coefficients, where Δd is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $x(n)$, and feedback data, $y(n)$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign\big(y(i+m+1) - y(i+m)\big)$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $C(m)$ is the feedback path delay..

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is

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necessary. To simplify the design, only a half-sample delay is considered in this design. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel. The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

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$$e^{jo,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{jhe}$$

Magnitude correction:

As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

The choice of N will depend on the accuracy desired.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^j$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

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where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2} q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = {k_a k_b}/{k_a'}$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2} q_{i-1}^* & \overline{d(1)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_1^{1/2}} & 0 \\ \overline{q_1^*} & \overline{e_a^*(1)\gamma^{\frac{1}{2}}(1)} \\ \overline{h_1 \Phi_1^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(1)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

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$$\overline{\Phi^{*}_{Z}}[w_i - \bar{w}] = \bar{q}_i$$

In the iterative process, a block of data (in this design, there is 4096 data in one block) is stored in memory, and the algorithm uses all the data in memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data are processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficient as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

Channel Calibration Algorithm

The 8 channel RRU in Figure 12 has 16 distinct power amplifiers. Half the power amplifiers are designed for one band and the other for a second band . The bands are hereafter referred to as band A and band B, they occupy two distinct frequencies. The 8 channel RRU uses 8 antennas and both bands will coexist on each antenna. In order to maximize performance, each power amplifier's output signal needs to be time, phase and amplitude aligned with respect to each other. The antenna calibration algorithms consist of three distinct approaches: 1) A Pilot Tone is injected into each PA 2) a Reference Modulated signal is transmit through each PA 3) the Real Time I/Q data is used as the reference signal . The Pilot Tone approach requires the injection of a single carrier IF tone that will be tracked in either the feedback calibration path or the individual PA's receiver. Each transmitter

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path for band A will be time, phase and amplitude aligned with respect to each other, similarly for band B. The Reference Modulated approach will utilize a stored complex modulated signal which will be transmitted through each of the band A PAs, similarly for the band B PAs. The transmitters will then be time, phase and amplitude aligned with respect to each other. Either the feedback calibration path or the individual receivers can be used for obtaining the PA output signals. The Real Time approach will operate on the real-time transmitted signals. This approach will utilize the DPD time alignment, phase and magnitude offset information to synchronize each PA output with respect to each other.

[0022] In summary, the RRU system of the present invention could enhance the performance for the efficiency and linearity more effectively since the RRU system is able to implement CFR, DPD and adaptation algorithm in one digital processor, which subsequently saves hardware resources and processing time. The high power efficiency of RF power amplifiers inside the RRU means that less thermal dissipation mechanism such as heat sink is needed; therefore, significantly reducing the size and volume of the mechanical housing. This smaller RRU can then enable service provider to deploy the RRU in areas where heavy or large RRU could not be deployed, such as pole tops, top of street lights, etc. due to lack of real estate, or weight limitation, wind factor, type of safety issues. The RRU system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime.

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[0023] **M**oreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. The multi-frequency bands benefits mean that mobile operators can deploy fewer RRUs to cover more frequency bands for more mobile subscribers; hence significantly reducing CAPEX and OPEX. Other benefits of the RRU system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0024] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A remote radio head unit (RRU) system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier inside the RRU. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are monitored by a wideband feedback path and controlled by the adaptation algorithm in a digital module. Therefore, the present invention could compensate the nonlinearities as well as memory effects of the power amplifier systems and also improve performances, in terms of power added efficiency, adjacent channel leakage ratio and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

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FIG. 1. Remote Radio Head Unit

Figure 2
8 Channel RRU

Figure 3. Polynomial based digital predistorter function

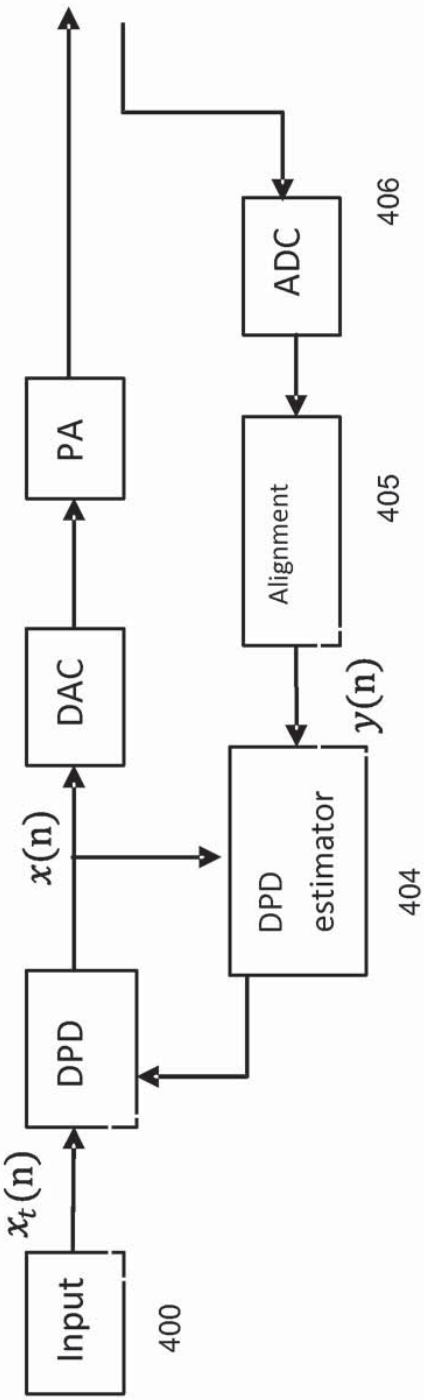


FIG. 4. Digital Predistortion Block Diagram

Figure 5 Analog Quadrature Modulator Compensation Block

Wall Mount
RRU 615
Rooftop
Mount RRU
610
Tower Mount
RRU 605
Base Station
Server 600

Figure 6

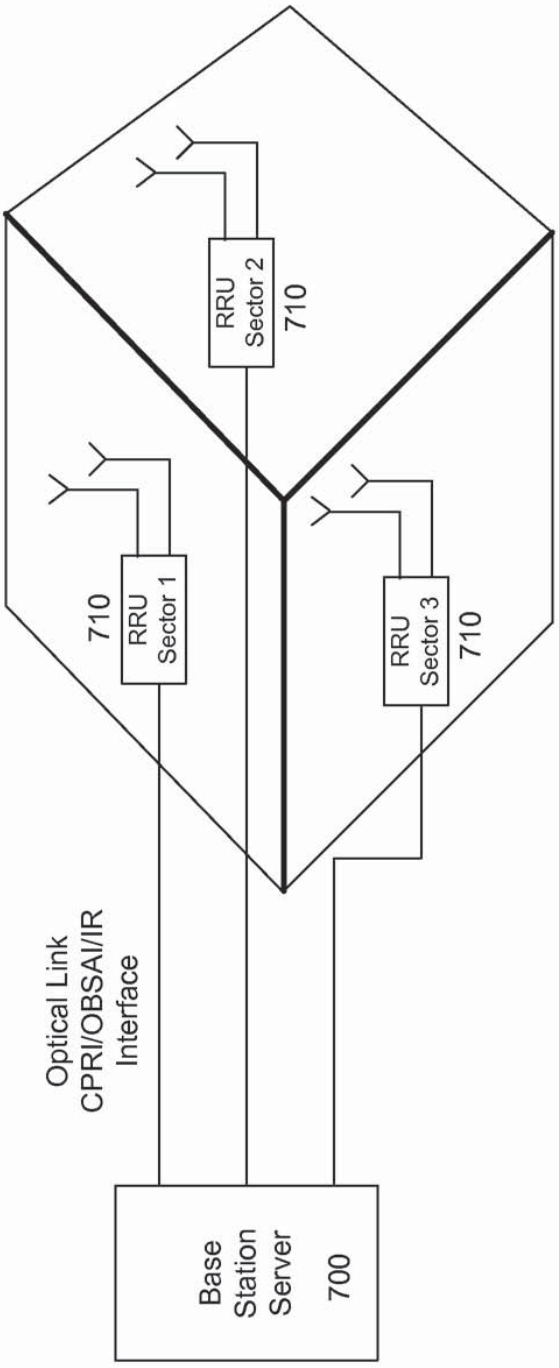

RRU
Sector 2
710
710
RRU
Sector 1
RRU
Sector 3
710
Optical Link
CPRI/OBSAI/IR
Interface
Base
Station
Server
700

Figure 7

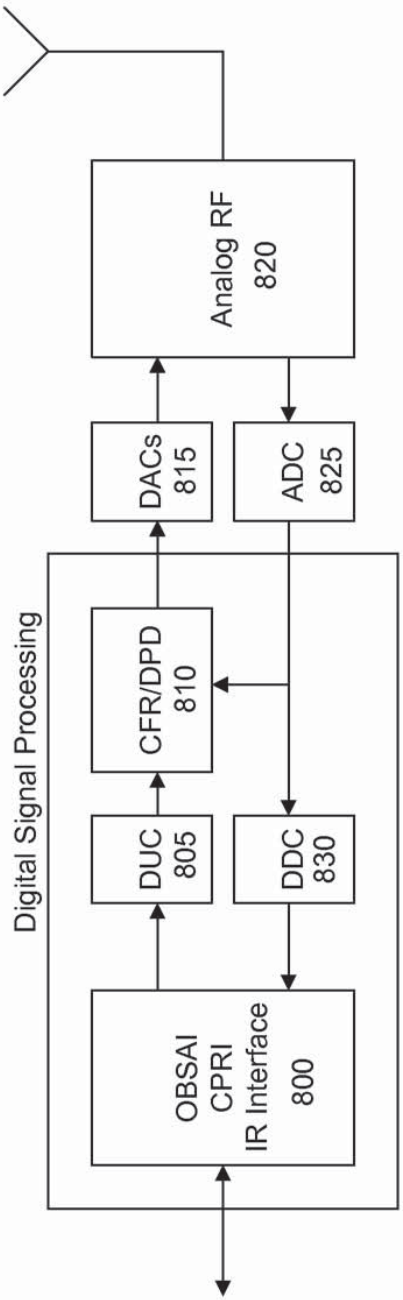

Digital Signal Processing
OBSAI
CPRI
IR Interface
800
DUC
805
CFR/DPD
810
DACs
815
DDC
830
ADC
825
Analog RF
820

Figure 8

Figure 9 Digital Hybrid Module

Figure 10 Dual Channel Remote Radio Head

Figure 11 Dual Channel Remote Radio Head

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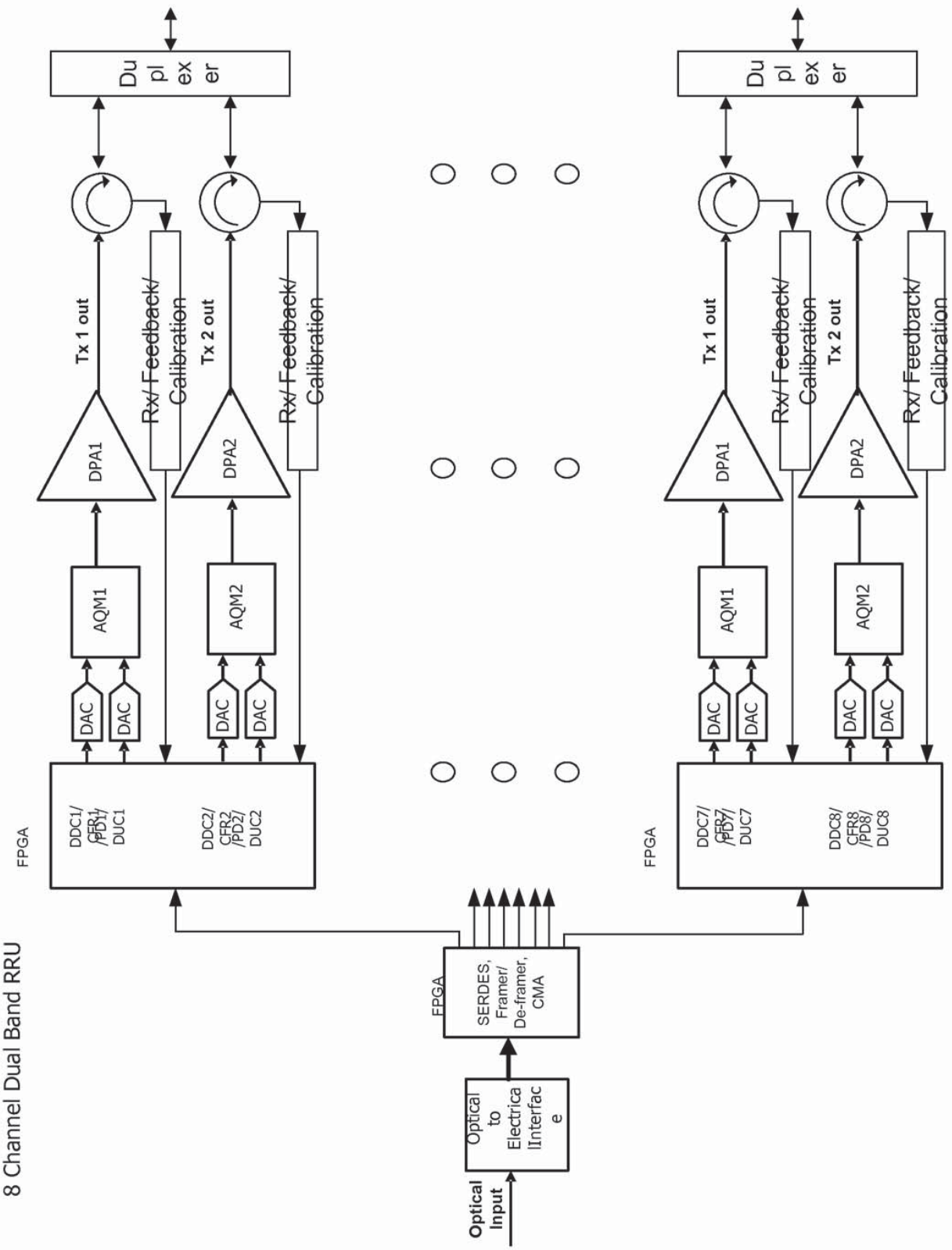


Figure 12
8 Channel Dual Band RRU

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM

INVENTORS

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Kyoung-Joon Cho, Citizen of Korea
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SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

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US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[002] A wideband mobile communication system using complex modulation techniques, such as wideband code division access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. Conventional digital predistortion (DPD) techniques have an operational bandwidth limitation.

[003] Conventional DSP-based DPD schemes utilize FPGAs, DSPs or microprocessors to compute, calculate and correct the PA's nonlinearities: they perform fast tracking and adjustments of signals in the PA system. However, conventional DSP-based DPD schemes are challenged by variations of the linearity performance of the power amplifier over wide bandwidths due to the environment changing such as temperature and the

asymmetric distortions of the output signal of the PA resulting from memory effects. Conventional DPD algorithms are based on a wideband feedback signal, they require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. Multi-frequency band, or simply multi-band, applications can have their operating frequencies spaced significantly apart. Conventional DPD architectures use an ADC sampling rate that is greater than twice the nonlinear distortion bandwidth of the input signal. This sampling rate is typically more than double a factor of five times the operating bandwidth of the complex modulated signal. The factor of five accounts for the spectral re-growth attributed to the nonlinear distortion created by the power amplifier. This restriction on sampling rate, limits the feasibility of the conventional predistortion architectures to single band applications. Higher sampling rate ADCs have lower resolution, consume more power and are more expensive.

SUMMARY OF THE INVENTION

[004] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers, and multi-channels.

[005] To achieve the above objects, according to the present invention, the technique is based on the method of adaptive digital predistortion to linearize a RF power amplifier. The present invention is based on using distinct signals from different frequencies (Multi-Band Signals). These Multi-Band Signals will experience distortion by the power amplifier and create nonlinear distortion centered on each carrier that is approximately five times their individual bandwidths. The feedback signal from the power amplifier's are down converted to an intermediate frequency (IF) that insures that the fundamental carrier bandwidths will not be aliased onto each other after sampling in the ADC. The present invention can accommodate aliasing of the nonlinear distortion of the individual carriers.

[006] Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction (CFR), DPD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator (AQM) compensation structure is also utilized to enhance performance.

[007] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called an adaptive DPD algorithm, which is implemented in the digital domain and taught in the applications incorporated herein by reference and attached as an Appendix.

Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless

devices, and other wireless communication systems such as microwave and satellite communications.

THE FIGURES

[008] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[009] Figure 1 is a block diagram showing the basic form of a digital predistortion power amplifier system.

[0010] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0011] Figure 3 is a block diagram showing polynomial based predistorter of the present invention.

[0012] Figure 4 is a block diagram of the digital predistortion Direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0013] Figure 5 is a block diagram of the digital predistortion In-direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0014] Figure 6 is a depiction of the frequency domain signals present in the aliased digital predistortion system.

[0015] Figure 7 is an embodiment of the Quadrature Modulator compensation block architecture.

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Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DPD	Digital Predistortion
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude

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FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

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[0016] The present invention is a novel multi-band predistortion system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers that operate simultaneously over multiple, distinct frequency bands.

[0017] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the DPD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system, as further discussed in the applications incorporated by reference. The present invention is a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101.

[0018] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD, Figure 2. The coefficients of the DPD are adapted by a synchronizing the wideband captured, aliased output Multi-BandSignal *ya[n]* from the feedback path (Sampled Feedback Aliased Signal) with the reference Multi-Band Signal *x[n]* (Input Signal). The DPD algorithm performs the synchronization and compensation. The synchronization aligns the reference signal with the aliased feedback signal in the alignment block. In one embodiment of the DPD algorithm, the reference signal and the aliased Sampled Feedback Aliased Signal *ya[n]* are used in the Direct Learning adaptive algorithm. In another embodiment of the DPD algorithm, the aliased predistorted signal *za[n]* (Predistorted Output Aliased Signal) and the Sampled Feedback Aliased Signal *ya[n]* are used in an Indirect Learning adaptive algorithm.

[0019] Some embodiments apply crest factor reduction (CFR) prior to the DPD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is typically used, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems,

incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0020] In all embodiments, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD. The coefficients of the DPD are adapted by synchronizing the wideband captured output signal from the feedback path with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal via a DAC. The DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals, respectively.

[0021] FIG 3. is a block diagram showing a predistortion (PD) part in the DPD system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the PD system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306.

The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows the block diagram of a digitally predistorted PA system. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4 and Figure 5. The coefficients are obtained using the QR RLS adaptive algorithm in the DPD estimator block.

Figure 4 shows one embodiment of the multi-band digital predistorter. The Direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the aliased sampled Multi-Band Signal *xa[n]* (Sampled Input Aliased Signal) as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

Figure 5 shows another embodiment of the multi-band digital predistorter. The in-direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the Predistorted Output Aliased

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Signal *za[n]* as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

A depiction of the spectrum domain plots are shown in Figure 6. The reference Input Signal *x[n]* shows two distinct bands centered at frequencies F_a and F_b. The operating bandwidth of the individual carriers is small in comparison to the frequency spacing between the carriers. The nonlinearities in the power amplifier will cause spectral re-growth as shown in the analog feedback Multi-Band Signal *y(t)* (Analog Feedback Signal). The Analog Feedback Signal is down converted to an intermediate frequency Fi which is selected to be in the 1st Nyquist zone as shown in Figure 6. The choice of frequency Fi is dependent on the ADC sampling rate used, the operating bandwidth of the carriers and the frequency separation (F_a - F_b) between the carriers. The ADC sampling rate is typically the limiting factor in the choice of Fi. For a two carrier system F_a is positioned in the 1st Nyquist zone and F_b is positioned in the 2nd Nyquist zone in at least some embodiments. The choice of Fi limits how close Fa and Fb can be separated together.

Sampling on the Analog Feedback Signal *y(t)* generates images as shown in the spectrum for the Sampled Feedback Aliased Signal *ya[n]*. The nonlinear distortion from the individual carriers are allowed to alias onto each other as long as the aliased part of the signal does not adversely impact the original Multi-Band signal. A Direct Learning algorithm uses the difference between *xa[n]* and *ya[n]* to minimize the resultant error signal. The QR RLS algorithm uses this error to adapt the predistorter coefficients in the DPD estimator. The In-Direct learning algorithm first models the power amplifier using the Predistorted Output Aliased Signal *za[n]* and the Sampled Feedback Aliased

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Signal *ya[n]*. The modelled power amplifier coefficients are then used to calculate the predistorter coefficients.

[0022] FIG. 7. is a block diagram showing the analog quadrature modulator compensation structure. The analog quadrature modulator will translate the baseband signal ouput from the DACs to an RF frequency. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12 , g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12 , g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

[0023] In summary, the multi-band wideband power amplifier predistortion system of the present invention can significantly reduce the feedback ADC sampling rate requirements. This will enable multi-band wideband applications and reduce the power consumption and cost. The system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime, as discussed in greater detail in the applications incorporated by reference and attached as an Appendix.

[0024] Moreover, the multi-band wideband DPD system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that

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the DPD system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DPD system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0025] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

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ABSTRACT

A high performance and cost effective method of RF-digital hybrid mode power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications is disclosed. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels.

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RF
Modulated signal or
Baseband signal or
Optical signal
100
Digital
Predistortion
Controller 101
(e.g. FPGA)
Main
PA
102
RF PA output
103
Feedback signal 105

Figure 1

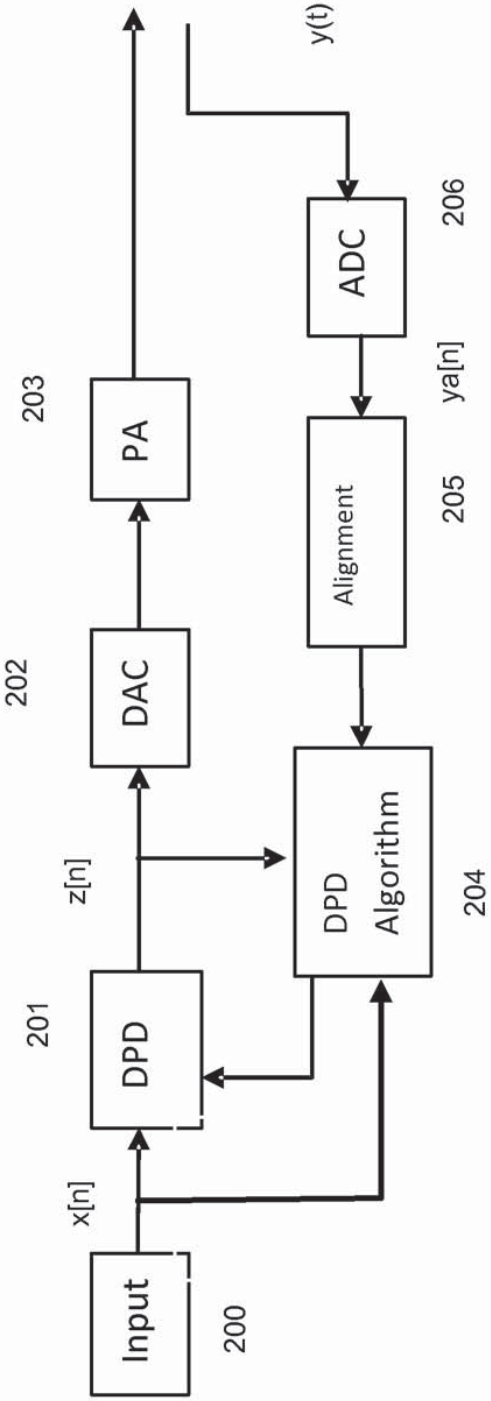


FIG. 2. Digital Predistortion Block Diagram

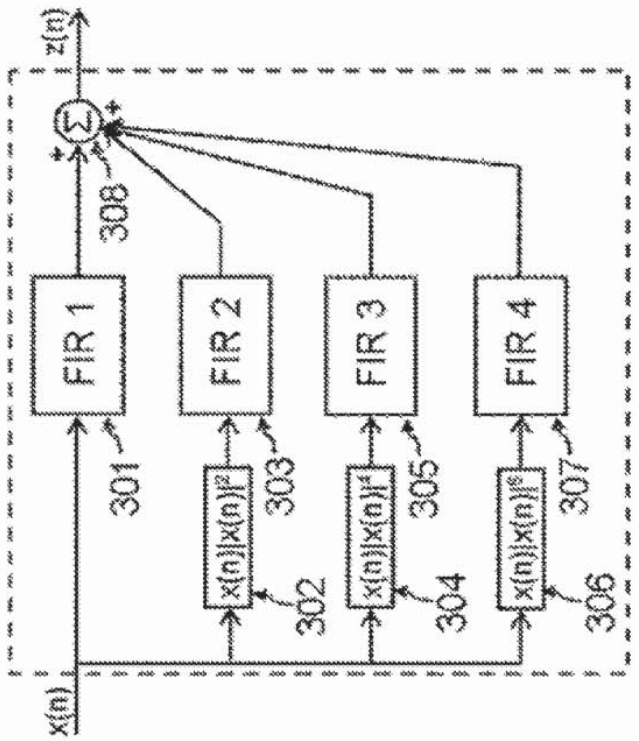


FIG. 3. Polynomial based Predistorter

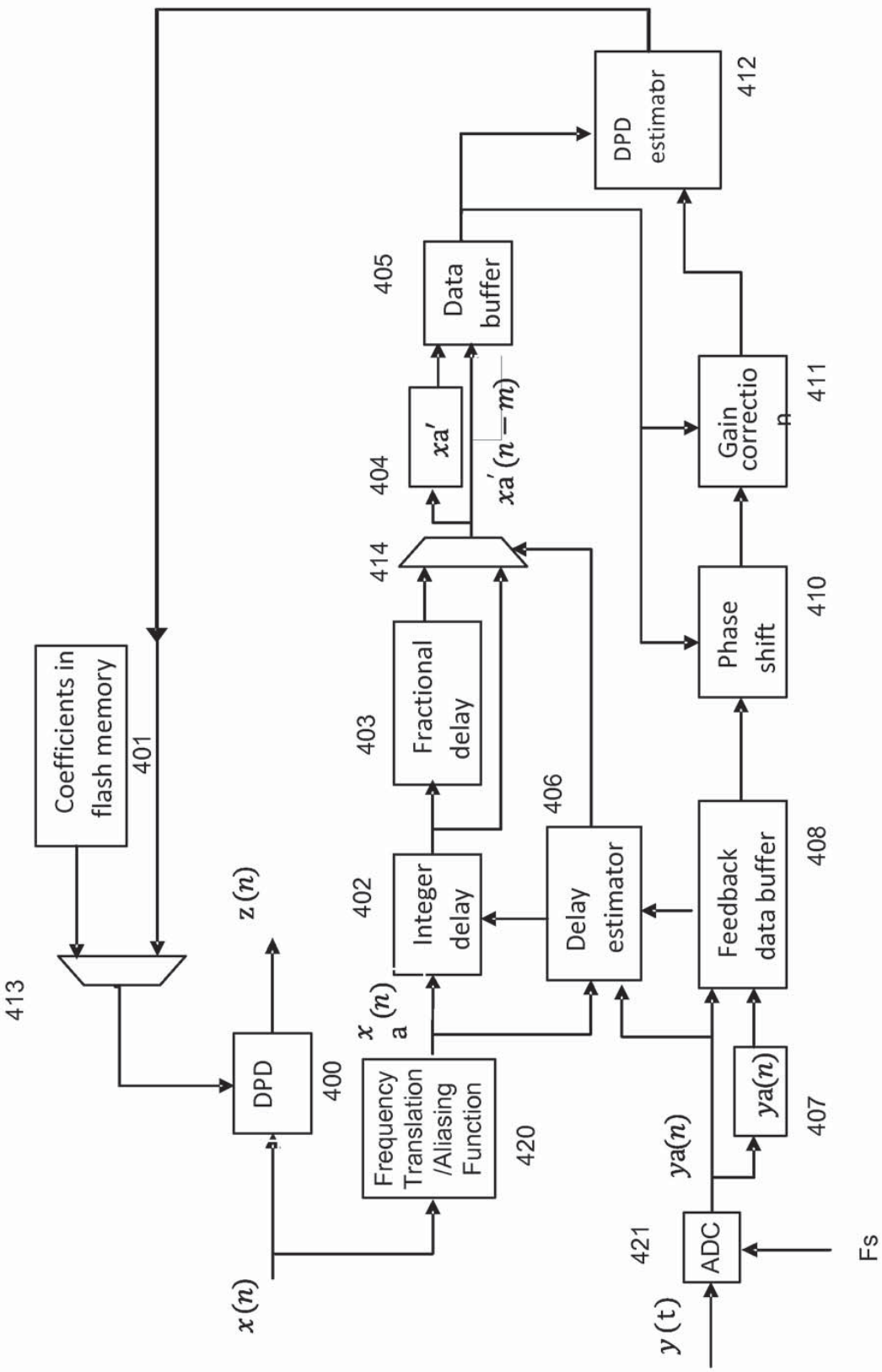


FIG. 4. Digital Predistortion Direct Learning Algorithm

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FIG. 5. Digital Predistortion Indirect Learning Algorithm

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Input Signal
x[n]
Fb
Fa
Sampled Input Signal
xa[n]
Aliased Image Fa
Fs
Aliased Image Fb
Fs/2
Predistorter Output after Aliasing
za[n]
Fs
Fs/2
Analog Feedback Signal
y(t)
Fb
Fi
Fa
Sampled Feedback Signal
ya[n]
Aliased Image Fa
Fs
2nd Nyquist Zone
Aliased Image Fb
Fs/2
1st Nyquist Zone

Figure 6

Figure 7: Analog Quadrature Modulator Compensation Block

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

REMOTE RADIO HEAD UNIT WITH WIDEBAND POWER AMPLIFIER AND METHOD

INVENTORS

Chengxun Wang, Citizen of People's Republic of China

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SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications, attached as Appendices:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER

SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective solutions to expand network capacity and evolution towards 4G and beyond.

Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years.

Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept is a fundamental part of a state-of-the-art base station architecture. 2G/3G/4G base stations are typically connected to RRUs over optical fibers. Either CPRI, OBSAI or IR Interfaces may be used to carry data to the RRH to cover a three-sector cell. The RRU incorporates a large number of digital interfacing and processing functions. Traditionally, a multi-channel RRU means that multiple antennas are used, typically with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as occurs in a Time Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. To extent the prior art architecture to multiple bands (i.e., two or more bands) implementation would consist of adding additional channelized power

amplifiers in parallel. The output of the additional power amplifiers is typically combined in an N by 1 duplexer and fed to a single antenna.

While conventional RRU architecture offers some benefits, RRUs to date are power- inefficient, costly and inflexible. Further, their poor DC-to-RF power conversion insures that they will have a large mechanical housing. In addition, current RRU designs are inflexible. As standards evolve, there is a need for multi-band RRUs that can accommodate two or more operating channels using a single wideband power amplifier. This creates an isolation problem at the individual receivers because the wideband power amplifier is always turned on. Isolation between the wideband transmitter and receivers is a problem with any modulation standard (HSPA+, WiMAX, LTE, etc.) when multi-band RRUs are developed using a single power amplifier This is a common problem for all communication systems that utilize a wideband power amplifier in a multi-band scenario.

SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective technique for implementing RRU systems that service multi-frequency bands. Further, the present disclosure enables a RRU to be field-reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels. The present invention also serves multi-frequency bands within a single RRU to economize the cost of radio network deployment. In particular, the present invention resolves an isolation issue for a RRU with fewer power amplifiers than the number of operating frequency bands. Multi-

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mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks.

[002] The present invention achieves the above objects using techniques generally based on methods and techniques for maximizing the isolation between the transmitted signal (Tx Signal) and the received signal (Rx Signal). The Tx Signal may comprise noise generated at the output of the power amplifier or it may comprise an unwanted transmitter band leaking into the receiver. With the use of the present invention, conventional RRU's can be extended to a multi-band and multi-channel configuration. Multi-band means that more than one frequency bands are used in the RRU and multi-channel means that more than one output antenna is used. Various embodiments of the invention are disclosed.

[003] An embodiment of the present invention utilizes duplexers, switches and circulators to maximize the isolation between the transmitter and receiver. Another embodiment of the present invention utilizes an Interference Cancellation System (ICS) together with duplexers, switches and circulators.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations, distributed antenna systems, access points, repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram of a TD-SCDMA dual-band single PA configuration in a remote radio head unit system in accordance with the present invention.

[007] Figure 2 is a block diagram of the TD-SCDMA dual-band single PA with a Interference Cancellation System (ICS) configuration in a remote radio head unit system in accordance with the present invention.

[008] Figure 3 is a FDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[009] Figure 4 is an Interference Cancellation System using Power Detection.

[0010] Figure 5 is a TDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[0011] Figure 6 is an Interference Cancellation System using Correlation.

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter

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AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications

I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

The present invention is a novel RRU system that utilizes a wideband power amplifier. The present invention is a hybrid system of digital and

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analog modules. The interplay of the digital and analog modules of the hybrid system eliminates interference between the wideband power amplifier output and the receiver's inputs.. The present invention, therefore, achieves higher Transmitter (Tx) to Receiver (Rx) isolation when using wideband power amplifiers with multiple frequency bands .

Referring first to Figure 1, an embodiment of some aspects of the invention is shown in block diagram form. Figure 1 depicts the analog section of a dual channel RRU. In this embodiment a single wideband power amplifier 404 is used. The two distinct frequency band signals are combined in a duplexer 403 and input to the wideband power amplifier 404. The output of the wideband power amplifier 404 is sent to a diplexer 405 in order to separate the two frequency band signals. This configuration enables the individual transmitter frequency bands to be independently turned-off. The Tx switches 405 and 407 are placed in the signal path after the diplexer 405. The signals are then passed through circulators 411 and 412 and a duplexer 413 in order to gain further isolation between the Tx signals and the Rx signals. The Rx switches 408 and 410 are placed on the third port of the circulator. Alternatively, two or more frequency bands can be combined in one power amplifier using the same architecture as in Figure 1.

Figure 2 illustrates a further alternative embodiment of the dual-band single wideband power amplifier RRU analog section. In the embodiment of Figure 2, an interference cancellation system (ICS) 520 is utilized to improve the isolation between the transmitter and receivers. The interference cancellation system generates a replicate of the unwanted feedback signal but in anti-phase so as to eliminate the interference. The interference

cancellation system comprises five primary blocks: Delay, variable attenuator, variable phase shifter, Down Converter (DNC) and DSP controller, alternative arrangements of which are shown in Figures 4 and 6, discussed hereinafter. The ICS receives incoming signals through links 506 and 507. The anti-phase output of the ICS is combined with the signals from switches Rx1 and Rx2, indicated at 510 and 511, respectively, by the use of adders 551 and 552, and the resulting signal provides the inputs to the LNA's 515 and 516. The ICS is an adaptive control system which continuously adjusts the variable attenuator as well as the variable phase shifter so as to maintain good interference cancellation. Alternatively, an embodiment of the ICS can comprise a fixed attenuator and phase shifter setting, eliminating the need for DSP control, although in at least some cases this results in inferior performance compared to the adaptive ICS system of Figure 2. The remaining elements of Figure 2 correspond to those shown in Figure 1, and are indicated by the same numerals except that the most significant digit has been changed from "4" to "5".

Figure 3 shows another embodiment of the analog section of a dual-band single wideband power amplifier RRU in Frequency Division Duplex (FDD) mode. This embodiment is modulation agnostic for FDD standard systems, and elements 601-604 operate analogously to elements 401-404 of Figure 1. The triplexer 608 separates the transmitter bands from the receiver bands. FDD systems use different transmit and receive frequencies for each channel. The function of the triplexer 608 is to pass the output of power amplifier 604 to the antenna while isolating the receivers from the transmitter output. The ICS 609 system is utilized for increasing the isolation between

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the transmitter output and the receiver inputs as with Figure 2, and receives the output of PA 604 through link 605. The output of the ICS 609 is combined with the appropriate triplexer outputs through adders 610 and 611, and the links 605 feeding the LNA's 612 and 613.

Figure 4 is a depiction of one embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. Coupler 605 is used to sample the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 710. This separates the two frequencies into distinct sections. The delay block 701 time-aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 702 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 703 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 707 or Microprocessor is used to control the attenuator and phase shifter. A power detection based adaptive algorithm in the DSP continuously monitors the signal at the Down Converter (DNC) 708 output and minimizes the level of the interference based on the detected power level . The power level of the interference is measured at the receiver while that band is in the transmit mode of operation. The second band is similarly processed using elements 704, 705 and 706.

Figure 5 shows an embodiment of the analog section of a dual-band single wideband power amplifier RRU in Time Division Duplex (TDD) mode.

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This embodiment is modulation agnostic for TDD standard systems. The output of wideband power amplifier 804 feeds a circulator 807. The circulator provides some isolation between the transmitted signals and the receiver inputs. A multi-band filter 820 is placed between the circulator and the output antenna in order to attenuate out-of-band emissions. The third port of the circulator 807 is delivered to a diplexer 808, which separates the two distinct operating bands. TDD mode requires the transmitter and receiver to operate using the same frequency band at distinct times. In order to provide isolation between the transmitter and receiver, switches 821, 822 are used. The switches can provide some isolation but additional isolation may be required depending on the system specifications. The ICS 809 can provide additional isolation between the transmitter output and the receiver inputs in the manner described above.

Figure 6 is a depiction of another embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 910. This separates the two frequencies into distinct sections. The delay block 901 time aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 902 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 903 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 907 or Microprocessor is used to control the attenuator and

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phase shifter. A correlation-based adaptive algorithm in the DSP is used to minimize the level of interference. The DSP correlates the two signals by controlling the output of switch 911 and the output of switch 912 after the signals have been translated to baseband using the two Downconverters 920 and 909. The switches 911 and 912 alternate between the two channels. The objective of the algorithm is to minimize the correlation between the sampled power amplifier output and the interference at the receiver. The computed correlation coefficient is used as the error function in an adaptive algorithm such as a Least Mean Squared (LMS) algorithm.

[001] From the foregoing teachings, those skilled in the art will appreciate that the RRU system of the present invention enables the use of single wideband power amplifier for multi-band operation , which consequently saves hardware resources and reduces costs. The RRU system is also reconfigurable and field-programmable since the algorithms can be adjusted like software in the digital processor at anytime.

[002] Moreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-frequency bands and multi-channels.

[003] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such

substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

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ABSTRACT

A remote radio head unit (RRU) system for multiple operating frequency bands, multi-channels, driven by a single or more wide band power amplifiers. More specifically, the present invention enables multiple-bands RRU to use fewer power amplifers in order to reduce size and cost of the multi-band RRU. The present invention is based on the method of using duplexers and/or interference cancellation system technique to increase the isolation between the transmitter signal and receiver signal of the RRU.

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Figure 1: Dual Band TD-SCDMA RRU

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Figure 2: Dual Band TD-SCDMA RRU with Interference Cancellation System

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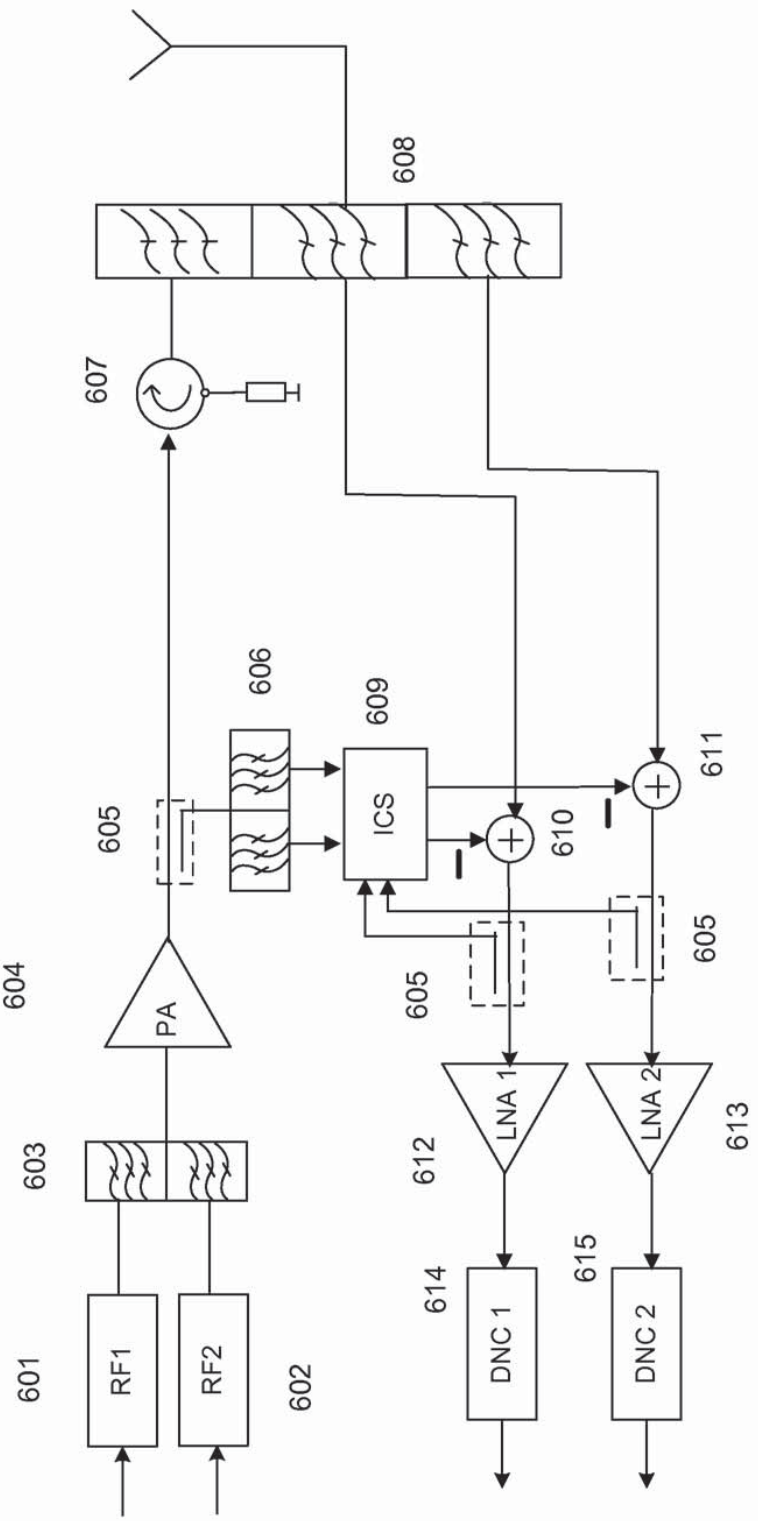


Figure 3: FDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

Figure 4: Dual-Band Interference Cancellation System using power detection

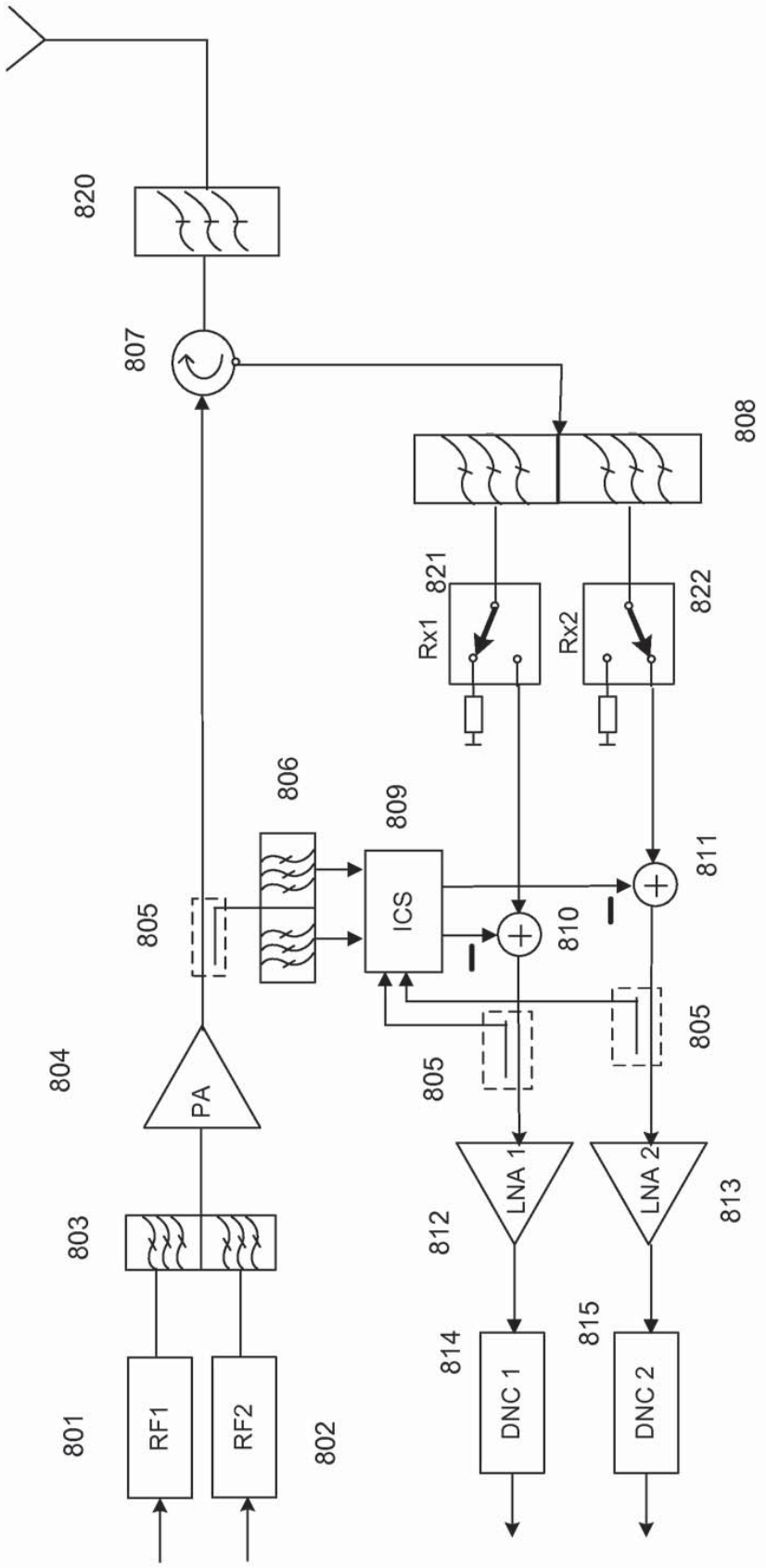


Figure 5: TDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

Figure 6: Dual-Band Interference Cancellation System using Correlation

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD

INVENTORS

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Ying Xiao, Citizen of Canada

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SPECIFICATION

RELATED APPLICATIONS

[001] This application claims the benefit of the following applications:

[002] US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

[003] US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

[004] US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

[005] US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

[006] US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

[007] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

[008] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

[009] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

[0010] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

[0011] All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[0012] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[0013] A wideband mobile communication system using complex modulation techniques, such as wideband code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. The conventional feedforward linear power amplifier (FFLPA) has been widely utilized due to its excellent linearity performance in spite of poor power efficiency.

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[0014] Conventional FFLPAs are mainly based on the principle of error subtraction and power-matching with dedicated hardware circuitries to realize non-linear corrections to PA. These approaches must use an auxiliary PA and complicated hardware circuitries to match exactly the transmitted power-balance, time-delay and errors generated by the main PA. After a perfect matching is obtained, the non-linear distortion errors from the main PA can then be canceled by those distortion errors from the auxiliary PA. Due to the complexities of the nonlinear predistortion circuits, which among other things involve many variables and parameters, FFLPAs require significant fine tuning and other calibration efforts. In addition, such traditional FFLPA schemes are also vulnerable to fluctuating environmental conditions, such as temperature and humidity changes, since perfect alignment of the main PA's signal and that of the auxiliary PA are vital. As a result, traditional predistortion schemes are costly to implement and are limited in their predistortion accuracy and stability in a commercial wireless system environment.

[0015] In order to overcome the FFLPA's poor efficiency, digital baseband predistortion (PD) has been demonstrated due to the recent advances in digital signal processing (DSP) technology. In addition, Doherty power amplifiers (DPA) have also been applied to these linearization systems to improve power efficiency. However, there is still a demand for higher performance of the power amplifier such as more linearity and better efficiency with less expensive architecture.

[0016] Conventional DSP-based PD schemes utilize digital microprocessors to compute, calculate and correct the PA's nonlinearities, typically by performing fast tracking and adjustments of signals in the PA system. However, conventional DSP-based PD schemes are challenged by

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variations of the linearity performance of the amplifier due to changes in the environment such as temperature and the asymmetric distortions of the output signal of the PA resulting from memory effects. All of these variations and distortions have to be compensated for. Conventional PD algorithms are based on a wideband feedback signal, and require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. In addition, time-synchronizations are typically required to capture an error signal between a reference signal and a distorted signal. This time-matching process may result in small synchronization errors which can further affect conventional PD schemes' linearization performance. Amplitude and phase synchronization is also required in order to align the reference signal and the distorted signal.

[0017] Moreover, conventional PD schemes necessitate coded in-phase (I) and quadrature (Q) channel signals in the baseband as the required ideal or reference signals. As a result, conventional PD schemes are often standard or modulation specific and must be closely tailored to each baseband system. Therefore, in order to deploy conventional PD schemes into base-stations, the PD engines must be embedded into the baseband architecture of base-stations. This embedment is a practical implementation challenge since it is frequently inconvenient or impossible to modify the baseband architectures of existing base-stations or base-station designs. Once the PD scheme is set up for a specific base-station design, it is often not reconfigurable and hence not upgradeable to future changes in standards or modulations. Furthermore, since traditional PD approaches require baseband I-Q signal sources to operate, they are inapplicable to certain RF systems that

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do not possess any baseband I-Q signal sources, such as repeater and indoor signal coverage sub-systems.

SUMMARY OF THE INVENTION

[0018] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for wideband communication system applications. The present disclosure provides a field-reconfigurable power amplifier system that supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. In multi-channel configurations of the present invention there can be more than one PA for multiple bands.

[0019] To achieve the above objects, the present invention is generally based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[0020] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

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[0021] Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

[0022] A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are sampled in a feedback path and controlled by the adaptation algorithm in a digital module. Therefore, in an embodiment, the present invention is capable of compensating for the nonlinearities as well as memory effects of power amplifier systems and also improves performance, in terms of power added efficiency, adjacent channel leakage ratio (ACLR) and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

THE FIGURES

[0023] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

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[0024] Figure 1 is a block diagram showing the basic form of a digital hybrid mode power amplifier system.

[0025] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0026] Figure 3 is a block diagram showing polynomial-based predistortion in a digital hybrid mode power amplifier system of the present invention.

[0027] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a digital hybrid mode power amplifier system of the present invention.

[0028] Figure 5 is a delay estimation block diagram of the present invention.

[0029] Figure 6 is a block diagram of a fractional delay for the present invention.

[0030] Figure 7 is a block diagram showing a digital hybrid mode power amplifier system implemented with a down converter (DNC) and UPC-based clipping error restoration path according to another embodiment of the present invention..

[0031] Figure 8 is a block diagram showing a digital hybrid mode power amplifier system implemented with a DNC and an analog quadrature modulator (AQM) according to another embodiment of the present invention.

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Figure 9 is a block diagram showing an embodiment of the analog quadrature modulator compensation structure.

GLOSSARY

The acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter

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EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access

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WLAN Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0032] The present invention is a novel RF-out PA system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[0033] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention is a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a digital hybrid mode power amplifier (DHMPA) system hereinafter.

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Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows in block diagram form an embodiment of a linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3), and complies with the formula:

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4.

[0034] FIG 3. is a block diagram showing a predistortion (PD) part in the DHMPA system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 and in embodiments disclosed in FIG. 7 and FIG. 8, discussed below, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the DHMPA system in FIG. 3 has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

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Delay Estimation Algorithm:

The DPD estimator compares $x(n)$ and its corresponding feedback signal $y(n - \Delta d)$ to find the DPD coefficients, where Δd is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $x(n)$, and feedback data, $y(n)$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign(y(i+m+1) - y(i+m))$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $C(m)$ is the feedback path delay. The delay estimation block is shown in Figure 5.

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is necessary. To simplify the design, only a half-sample delay is considered in this design, as shown in Figure 6. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel. The interpolation function for fractional delay is

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$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{j\theta o,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{j\theta o}$$

Magnitude correction:

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As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

In this design, N is chosen to be 4096. The choice of N will depend on the desired accuracy.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^{j}$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

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$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = {k_a k_b}/{k_a'}$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & \overline{d(1)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_1^{1/2}} & 0 \\ \overline{q_1^*} & \overline{e_a^*(1)\gamma^{\frac{1}{2}}(1)} \\ \overline{h_1 \Phi_1^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(1)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{\frac{*}{2}}}[w_i - \overline{w}] = \overline{q_1}$$

In the iterative process, a block of data (in this design, there are 4096 data in one block) is stored in memory, and the algorithm uses all the data in

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memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data is processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficients as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

[0035] Figures 7 and 8 are block diagrams showing more sophisticated embodiments of DHMPA system, where like elements are indicated with like numerals and elements not numbered in Figure 8 have the same reference numerals as shown in Figure 7. The embodiments of Figures 7and 8 apply crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is

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included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0036] Figure 7 is a block diagram showing a DHMPA system implemented with DQM in accordance with an embodiment of the present invention (the "FIG. 7. System"). The system shown in Figure 7 has a dual mode of RF-in 700 and/or multi-carrier digital signal 705 at the input, and an RF signal at the output 710. The dual mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode"). The FIG. 7. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 715, a power amplifier module 760 and a feedback path 725.

[0037] The FPGA-based Digital part comprises a digital processor 715 (e.g. FPGA), digital-to-analog converters 735 (DACs), analog-to-digital converters 740 (ADCs), and a phase-locked loop (PLL) 745. Since the FIG. 7 System has a dual input mode, the digital processor has two paths of signal processing. For the RF signal input path, the digital processor has implemented a digital quadrature demodulator (DQDM), a CFR, a PD, and a digital quadrature modulator (DQM). For the baseband digital input path, a digital up-converter (DUC), CFR, PD, and a DQM are implemented.

[0038] The RF-in Mode of the FIG. 7. System has implemented a down converter (DNC) 750 prior to the FPGA-based Digital part and an ADC 740 prior to the FPGA. An analog down converted signal is provided to the FPGA-based Digital module and converted to a digital signal by the ADC 740. The digitally converted signal is demodulated by the DQDM to generate both real and imaginary signals and then PAPR of the signal is reduced by CFR. The peak reduced signal is predistorted to linearize the amplifier and is

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passed through a DQM to generate the real signal and then converted to an intermediate frequency (IF) analog signal by a DAC in the FPGA-based Digital part. However, it is not required in all embodiments to implement DQDM and DQM in the FPGA. If, as shown in Figures 7 and 8, a digital modulator will not be used, then two DAC's 801 behind the FPGA feeding AQM module 800 can be used to generate real and imaginary signals, respectively (the "AQM Implementation").

[0039] The Baseband-in Mode of FIG. 7. works slightly different from the RF-in Mode. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. From this point onwards, the Baseband-in Mode and RF-in Mode proceeds identically. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0040] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a synchronizing the wideband captured output signal from the feedback path 725 with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. . The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DAC 740 as shown. As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. Alternatively, if the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to

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generate real and imaginary signals, respectively. The gate bias voltage 753 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 535 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. .

[0041] The power amplifier part comprises a UPC for a real signal (such as illustrated in the embodiment shown in Figures 7), or an AQM for real and complex signals (such as the embodiment of a DHMPA system depicted in Figure 8) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental DHMPA system. One such Doherty power amplifier technique is presented in commonly assigned U.S. Provisional Patent Application S.N. 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference, together with U.S. Patent Application S.N. 12/603,419, filed 10/21/2009, entitled N-Way Doherty Distributed Power Amplifier with Power Tracking. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0042] The feedback portion comprises a directional coupler, a mixer, a gain amplifier, a band pass filter (BPF), and a Digital to Analog Converter (DAC). Depending upon the embodiment, these analog components can be

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mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the the gain amplifier, and the BPF (e.g., surface acoustic wave filter) which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the digital PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the detector 580 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, discussed above, which shows a polynomial-based predistortion algorithm and from Figure 4, also discussed above, which shows the block diagram of the digital predistorter synchronization algorithm which can be used in some embodiments of the invention.

[0043] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 790, hence maximizing the DHMPA system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC 735 in the FPGA-

based Digital portion and an extra UPC 720 in the power amplifier part (see FIG. 7. & 8.). The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0044] Referring again to Figure 7, the RF input signal is first down-converted to baseband digital signals, and then digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz). If the system of Figure 7 has a Baseband-in Mode, then the digital data streams from multi-channels are digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz) directly as they enter the digital processor. The CFR then reduces the PAPR. The peak-reduced signal is predistorted to linearize the DPA and is passing through two DACs for real and imaginary signals and finally through an AQM.

[0045] FIG. 9. is a block diagram showing an embodiment of the analog quadrature modulator compensation structure. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12, g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2. The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

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[0046] The configuration of the power amplifier part and the feedback part of the system shown in FIG. 8 are the same as for the system shown in FIG. 7.

[0047] In FIG. 8 System, the DNC frequency translates the RF signal into a low IF signal. The IF signal is then presented to the ADC whereupon it is digitally down-converted to baseband followed by CFR and predistortion (PD). The output of the PD is a baseband signal which will then be digitally upconverted to an IF frequency and presented to the DAC. The output of the DAC is then further frequency translated to a RF frequency through the up-converter (UPC.) The configuration of the power amplifier part and the feedback part of FIG. 8 System are the same as for the FIG. 7 System.

[0048] In summary, the DHMPA system of the present invention enhances efficiency and linearity relative to the prior art since the DHMPA system is able to implement CFR, DPD and adaptation algorithms in one digital processor, which consequently saves hardware resources and processing time. The DHMPA system is also reconfigurable and field-programmable since the algorithms and power-efficiency-enhancing features can be adjusted like software in the digital processor at anytime.

[0049] Furthermore, since the DHMPA system accepts RF modulated signal as input, it is not necessary to use coded I and Q channel signals in the baseband. Therefore, the performance of wireless base-station systems can be enhanced simply by replacing the existing PA modules with the DHMPA. The result is that the present invention provides a "plug and play" PA system solution such that the structure of existing base-station systems does not

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need to be modified or rebuilt for a new set of signal channels in order to benefit from high efficiency and high linearity PA system performance.

[0050] Moreover, the DHMPA system is agnostic to modulation schemes such as quadrature phase shift keying (QPSK), quadrature amplitude modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM), etc. in code division multiple access (CDMA), global system for wireless communications (GSM), WCDMA, CDMA2000, and wireless LAN systems. This means that the DHMPA system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DHMPA system of the present invention include correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0051] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

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FIG. 1. Basic Digital Hybrid Mode Power Amplifier System

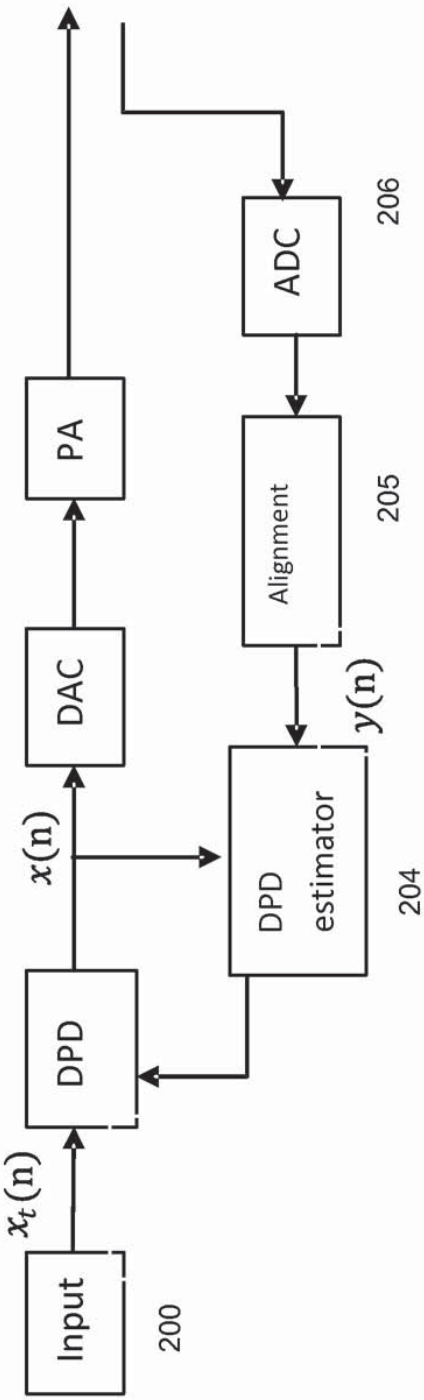


FIG. 2. Digital Predistortion Block Diagram

FIG. 3. Polynomial based PD in an embodiment of Digital Hybrid Mode Predistortion PA System

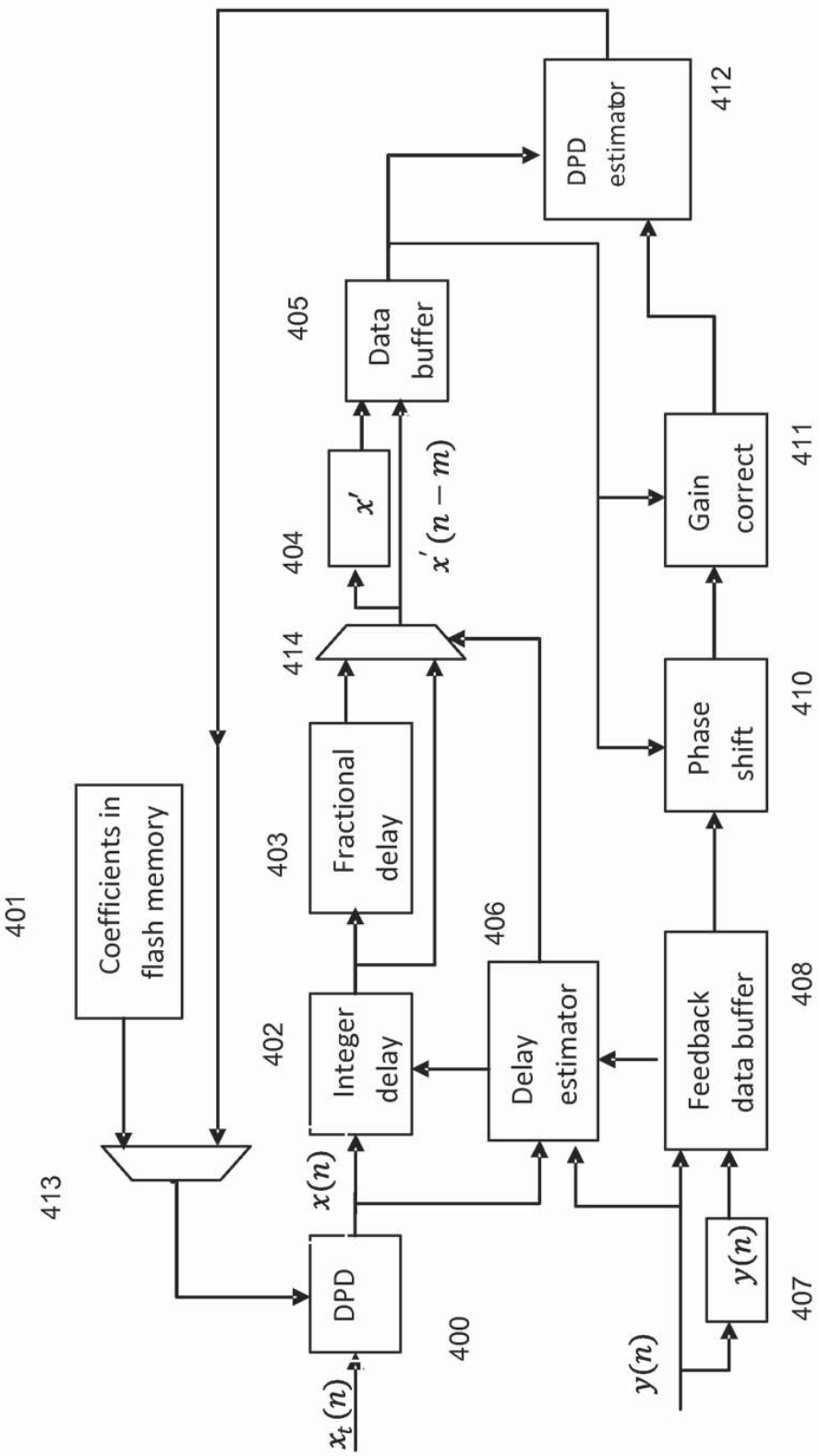


FIG. 4. Digital Predistortion Algorithm

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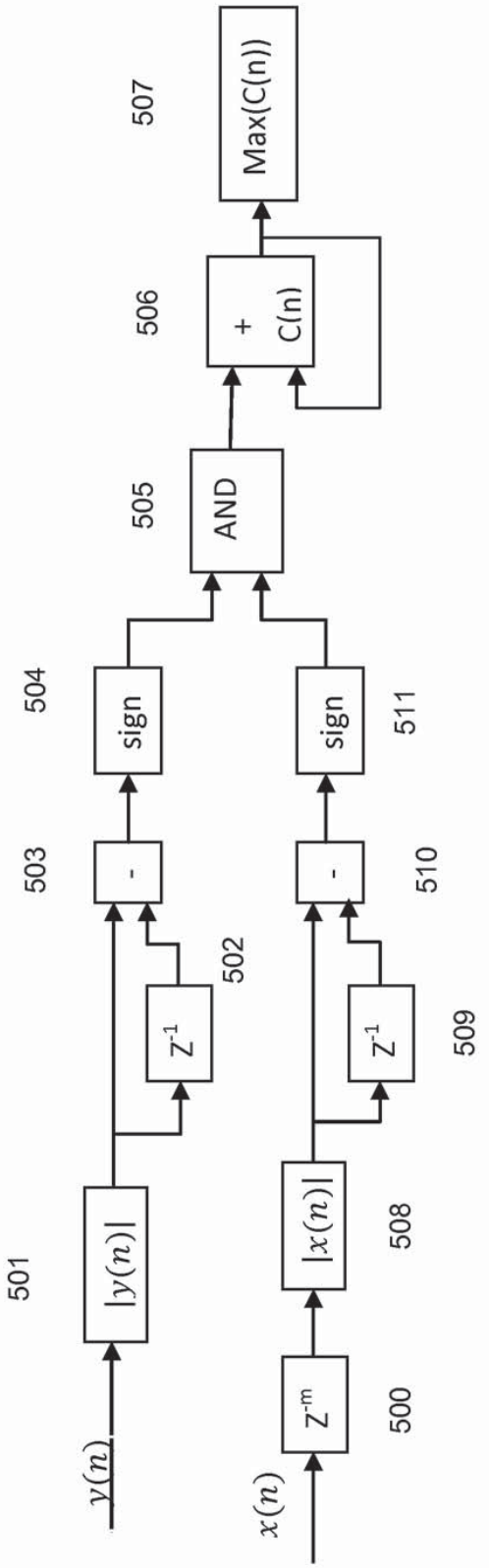


FIG. 5. Delay Estimation Block

Figure 6 Fractional Delay Block

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FIG. 7. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input

FIG. 8. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input, with Feedback Calibration

Figure 9 Analog Quadrature Modulator Compensation Block

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	DW-1022P
	Application Number	
Title of Invention	NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	DW-1022P
	Application Number	
Title of Invention	NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM	

Citizenship under 37 CFR 1.41(b) [i]	CA		
Mailing Address of Applicant:			
Address 1	4238 Southwood Street		
Address 2			
City	Burnaby	**State/Province**	BC
Postal Code	V5J 2E9	**Country**[i]	CA

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	54412		
Email Address	jee@jeelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM		
Attorney Docket Number	DW-1022P	**Small Entity Status Claimed**	☒
Application Type	Provisional		
Subject Matter			
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

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CommScope Exhibit 1022

PTO/SB/14 (11-08)
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Customer Number	54412

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			(•) Yes ( ) No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. [X]			
Organization Name	Dali Systems Co. Ltd.		
Mailing Address Information:			
Address 1	Offices of Maples Corporate Services Limited		
Address 2	PO Box 309, Ugland House South Church Street		
City	George Town Grand Cayman	**State/Province**	
Country [i]	KY	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

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Title of Invention	NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM	

Signature	/James E. Eakin/			Date (YYYY-MM-DD)	2010-08-17
First Name	James E.	Last Name	Eakin	Registration Number	27874

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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