

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DECLARATION OF DR. PETER KENINGTON

- i -

DECLARATION OF DR. PETER KENINGTON

I, Peter Kenington, Ph.D., currently residing in Devauden, United Kingdom, declare as follows.

A. Background

1. This declaration involves my knowledge related to the OBSAI standards publications. The statements made herein are based on my own knowledge and opinions. I am being compensated for my time in connection with this matter at a rate of £250 per hour.
2. I have a Ph.D. in Communications Engineering from the University of Bristol and a Bachelor's of Engineering in Electrical and Electronic Engineering also from the University of Bristol. I have been lecturing, leading research, or working in the field of communications engineering since at least 1990.

B. OBSAI

3. The Open Base Station Architecture Initiative ("OBSAI") is a trade organization consisting of more than 130 component, module and base station vendors. The aim of OBSAI was to create an open set of specifications for the internal modules required in a base-station, encompassing both interface and mechanical aspects. The OBSAI project was well known in the industry and hundreds of engineers representing the participating vendors were involved in generating the OBSAI standards.

4. I became involved with OBSAI as RP3 Project Coordinator in December 2002. Within two years I became the OBSAI Technical Chair, a position I have held since June of 2004. In my position as Technical Chair I personally worked with many engineers in developing the OBSAI specification documents. My name is listed as OBSAI Technical Chair on multiple specification documents published by OBSAI.

5. Attached hereto at Tab A is a true and correct copy of OBSAI BTS System Reference Document V2.0, which was released in April of 2006.

6. Attached hereto at Tab B is a true and correct copy of OBSAI Reference Point 3 (RP3) Specification V3.1, which was released in November of 2006.

7. Attached hereto at Tab C is a true and correct copy of OBSAI Reference Point 3 (RP3) Specification V4.1, which was released in July of 2008.

8. As Technical Chair of OBSAI, I was involved in developing, writing, finalizing, and releasing the specification documents shown at Tabs A-C.

9. OBSAI published its specifications to the public by making them available for public download from the OBSAI website (www.obsai.com). For example, a true and correct copy of a portion of the website from 2020 showing a list of specification documents available for free download is shown at Tab D.

10. The two specification documents shown at Tabs A and B were published and made available to the public on the OBSAI website in or prior to December 2006.

11. Attached hereto at Tab E is a true and correct copy of an article I wrote which was published in the December 2006 issue of the trade magazine, *European Communications*. The article is entitled, "Open Base Station Architecture." In the article I described the OBSAI project, and I also noted that the specification documents generated by OBSAI were available to the public for free download from OBSAI's website at www.obsai.com. The following is a quote from the article that published in December of 2006:

OBSAI's specifications are compatible with all of the major current and emerging air interface standards...and are available for public download free of charge (from www.obsai.com).

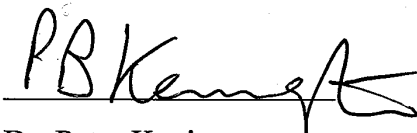
The OBSAI specification documents available for public download in December 2006 free of charge included the specification documents shown at Tabs A and B.

12. Likewise, the specification document shown at Tab C was published and made available to the public on the OBSAI website within a few weeks after its release date in 2008.

13. Attached hereto at Tab F is a true and correct copy of a portion of the OBSAI website from May 2007 that shows under the heading "Public Documents" that users were able to "Download Specifications." The URL for this page was http://www.obsai.com/obsai/documents/public_documents. This portion of the OBSAI website was retrieved from web.archive.org (i.e., "The Wayback Machine") at https://web.archive.org/web/20070525150857/http://www.obsai.com/obsai/documents/public_documents.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on 15th July, 2022


Dr. Peter Kenington

TAB A



OPEN BASE STATION ARCHITECTURE INITIATIVE

**BTS SYSTEM REFERENCE DOCUMENT
Version 2.0**

FOREWORD

OBSAI description and specification documents are developed within the Technical Working Group of the Open Base Station Architecture Initiative Special Interest Group (OBSAI SIG). Members of the OBSAI TWG serve voluntarily and without compensation. The description and specifications developed within OBSAI represent a consensus of the broad expertise on the subject within the OBSAI SIG.

The OBSAI SIG uses the following terminology in the specifications:

- "shall" expresses a provision that is binding
- "should" and "may" expresses non-mandatory provisions
- "will" expresses a declaration of purpose on the part of the OBSAI SIG. It may be necessary to use "will" in cases where the simple future tense is required

Use of an OBSAI reference or specification document is wholly voluntary. The existence of an OBSAI Specification does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the OBSAI Specification. Furthermore, the viewpoint expressed at the time a specification is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the specification. Every OBSAI Specification is subjected to review in accordance with the Open Base Station Architecture Initiative Rules and Procedures.

Implementation of all or part of an OBSAI Specification may require licenses under third party intellectual property rights, including without limitation, patent rights (such a third party may or may not be an OBSAI Member). The Promoters of the OBSAI Specification are not responsible and shall not be held responsible in any manner for identifying or failing to identify any or all such third party intellectual property rights.

The information in this document is subject to change without notice and describes only the product defined in the introduction of this documentation. This document is intended for the use of OBSAI Member's customers only for the purposes of the agreement under which the document is submitted, and no part of it may be reproduced or transmitted in any form or means without the prior written permission of OBSAI Management Board. The document has been prepared for use by professional and properly trained personnel, and the customer assumes full responsibility when using it. OBSAI Management Board, Marketing Working Group and Technical Working Group welcome customer comments as part of the process of continuous development and improvement of the documentation.

The information or statements given in this document concerning the suitability, capacity, or performance of the mentioned hardware or software products cannot be considered binding but shall be defined in the agreement made between OBSAI members. However, the OBSAI Management Board, Marketing Working Group or Technical Working Group have made all reasonable efforts to ensure that the instructions contained in the document are adequate and free of material errors and omissions.

OBSAI liability for any errors in the document is limited to the documentary correction of errors. OBSAI WILL NOT BE RESPONSIBLE IN ANY EVENT FOR ERRORS IN THIS DOCUMENT OR FOR ANY DAMAGES, INCIDENTAL OR CONSEQUENTIAL (INCLUDING MONETARY LOSSES), that might arise from the use of this document or the information in it.

This document and the product it describes are considered protected by copyright according to the applicable laws. OBSAI logo is a registered trademark of Open Base Station Architecture Initiative Special Interest Group. Other product names mentioned in this document may be trademarks of their respective companies, and they are mentioned for identification purposes only. Copyright © Open Base Station Architecture Initiative Special Interest Group. All rights reserved. Users are cautioned to check to determine that they have the latest edition of any OBSAI Specification.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of OBSAI, the OBSAI TWG will initiate action to prepare appropriate responses. Since OBSAI Specifications represent a consensus of OBSAI Member's interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason OBSAI and the members of its Technical Working Groups are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on specifications and requests for interpretations should be addressed to:

Peter Kenington
Chairman, OBSAI Technical Working Group
Linear Communications Consultants Ltd.
Email: pbk@linearcomms.com

Contents

1	Summary of changes	13
2	Scope.....	15
3	Reference Architecture	16
3.1	Open Architecture Objectives	16
3.2	Architecture Overview.....	16
3.3	Architecture Configurations	18
3.4	Block Functional Specifications	19
3.4.1	Transport Block (TB).....	20
3.4.2	Control and Clock Block (CCB).....	23
3.4.3	Baseband Block.....	25
3.4.4	RF Block	42
3.4.5	General Purpose Block.....	46
3.4.6	Power System Unit (PSU) Block.....	48
3.5	OAM&P Principles and Architecture	48
3.5.1	Overview of OAM&P support.....	49
3.5.2	OAM&P Implementation Concept.....	50
3.5.3	OAM&P BTS Information Model	52
3.6	Addressing Principles	53
3.6.1	MAC Address Assignment.....	53
3.6.2	IP Address Assignment	55
3.6.3	IPv6 Address Assignment.....	55
3.6.4	IPv4 Address Assignment.....	56
3.6.5	Addressing Of Software Resources.....	56
3.7	Synchronization	57
3.8	BTS Start-up and Hot Insertion/Removal Principles	58
3.8.1	Concepts and Definitions.....	59
3.8.2	Principles for DA-based Implementation.....	60
3.8.3	Principles for DA-less Implementation	62
3.9	Redundancy and Availability Criteria	66
3.9.1	N+1 Redundancy.....	66
3.9.2	RP1 and RP2 Ethernet Redundancy Principles.....	66

3.10	Mechanical and Dimensioning Requirements.....	68
3.10.1	Overview.....	68
3.10.2	Sealed Module Common Features (Excluding RF Modules)	71
3.10.3	Unsealed Module Common Features	76
3.10.4	RF Module Common Features.....	80
3.10.5	Rear Transition Module	80
3.11	Backplane	80
3.11.1	Data Connections	81
3.11.2	Power Connections.....	82
3.12	Module Power Interface.....	84
3.12.1	Module Supply Voltage.....	84
3.12.2	Module Supply Protection.....	85
4	Glossary	86
4.1	Abbreviations.....	86
4.2	Definition of Terms.....	89
5	References	92
5.1	American National Standards Institute (ANSI).....	92
5.2	TIA/EIA	92
5.3	Telcordia.....	93
5.4	Underwriters Laboratory (UL)	93
5.5	Government.....	93
5.6	ITU.....	93
5.7	IEEE	93
5.8	IETF.....	94
5.9	3 rd Generation Partnership Project (3GPP).....	94
5.10	Other.....	95
Appendix A.	Design Recommendations	97
A.1.	Environmental Conditions.....	97
A.1.1.	Operating Temperature And Humidity	97
A.1.2.	Storage Temperature And Humidity	97
A.1.3.	Altitude Requirements	97
A.2.	Design and Construction Criteria.....	98
A.2.1.	Maintainability Criteria	98

A.2.2. Safety and Fail-safe Operation	99
Appendix B. Specification for HARD-Metric Vertical Male Connector.....	100
B.1. Scope	100
B.2. General Description	100
B.3. Electrical Specification.....	101
B.4. Mechanical Specification	102
B.5. Environmental Requirement	102
B.5.1. Environment Specification For Operation	103
B.5.2. Environment Specification For Transportation.....	105
B.6. Coding	105
B.6.1. Coding 0	105
B.6.2. Coding 1	105
B.6.3. Coding 2	106
B.6.4. Coding 3	106
B.7. PCB Layout	107
B.8. Specification Drawings	108
B.8.1. Male Connector	108
B.8.2. Male Connector With Endwall.....	110
B.9. Male Connector With Guidance.....	111
B.9.1. Available Pin Type(s)/Length(s).....	112
B.9.2. Coding Pin	113
B.9.3. Guide Pin.....	114
B.10. Reference Documents	115
Appendix C. Hard-Metric 2MM 6-Row Daughterboard Receptacle	116
C.1. Summary of changes.....	116
C.2. Scope	117
C.3. General Description	117
C.4. Electrical Specification.....	118
C.5. Mechanical Specification	118
C.6. Environmental Requirement	119
C.6.1. Environment specification for operation.....	120
C.6.2. Environment Specification For Transportation.....	122
C.7. Coding	122

C.7.1. Coding 0	122
C.7.2. Coding 1	122
C.7.3. Coding 2	122
C.7.4. Coding 3	123
C.8. PCB Layout	123
C.9. Specification Drawings	126
C.9.1. Female PIHR Connector.....	126
C.9.2. Female PIHR Connector With Guidance	127
C.9.3. Female Press-fit Connector	128
C.9.4. Female Press-Fit Connector With Guidance	129
C.10. Reference Documents	130

Appendix D. HARD-Metric Right Angled Male Power Connector Specification
131

D.1. Summary of changes.....	131
D.2. Scope	131
D.3. General Description	132
D.4. Electrical Specification.....	132
D.5. Mechanical Specification	133
D.6. Environmental Requirement	133
D.6.1. Environment Specification For Operation	133
D.6.2. Environment Specification For Transportation.....	135
D.7. Pin Types and Contact Loading.....	136
D.7.1. Pin Types.....	136
D.7.2. Contact Loading.....	136
D.8. PCB Layout	138
D.9. Specification Drawings	139
D.9.1. Male Pressfit Connector	139
D.9.2. Male PIHR Connector.....	141
D.10. Reference Documents	143

Appendix E. HARD-Metric Straight Female Power Connector Specification**144**

E.1. Summary of changes.....	144
E.2. Scope	144
E.3. General Description	145
E.4. Electrical Specification.....	145

E.5. Mechanical Specification	146
E.6. Environmental Requirement	146
E.6.1. Environment Specification For Operation	146
E.6.2. Environment Specification For Transportation	147
E.7. PCB Layout	149
E.8. Specification Drawings	150
E.9. Reference Documents	151

List of Figures

Figure 3.2-1	BTS Reference Architecture.....	17
Figure 3.3-1	BTS Module Configuration Options.....	19
Figure 3.4-1	Example of Implementation of Module in Proprietary Block	47
Figure 3.5-1	Network Management Hierarchy	49
Figure 3.5-2	OAM&P BTS Internal Interface Architecture	51
Figure 3.5-3	OAM&P BTS Internal Interface Architecture for Indirect Interface.....	52
Figure 3.5-4	OBSAI Management Protocol Stack	53
Figure 3.6-1	IEEE 802 based global MAC address	54
Figure 3.6-2	MAC address based on HW position	54
Figure 3.6-3	IPv6 address interface ID.....	56
Figure 3.7-1	Synchronization Hierarchy	58
Figure 3.10-1	Sealed Module Perspective Views	70
Figure 3.10-2	Unsealed Module Perspective View.....	70
Figure 3.10-3	Module Depth Reference Dimension	71
Figure 3.10-4	Sealed Module Dimensions, Side View.....	72
Figure 3.10-5	Sealed Module Dimensions, Top View.....	73
Figure 3.10-6	Sealed Module Dimensions, Front View.....	74
Figure 3.10-7	Sealed Module Dimensions, Rear View	75
Figure 3.10-8	Unsealed Module Dimensions, Side View.....	77
Figure 3.10-9	Unsealed Module Dimensions, Top View.....	77
Figure 3.10-10	Unsealed Module Dimensions, Top Detail	77
Figure 3.10-11	Unsealed Module Dimensions, Front View.....	79
Figure 3.10-12	ESD Strip Schematic and Dimensions	80
Figure B-1	2mm Straight Male Connector 144 Pin with Guide and Coding Block	100
Figure B-2.	Male Connector With Guidance And Coding 1	105
Figure B-3.	Male Connector With Guidance And Coding 2	106
Figure B-4.	Male Connector With Guidance And Coding 3	106

Figure B-5.	Lay Out Drawing For 144 Pin Male Press-Fit Connector With Guidance	107
Figure B-6.	Layout Drawing For 144 Pin Male Press-Fit Connector Without Guidance	107
Figure B-7.	Male Connector	108
Figure B-8.	Male Connector With Endwall	110
Figure C-9.	Male Connector With Guidance	111
Figure B-10.	Available Pin Length(S)	112
Figure B-11.	Coding Pin	113
Figure B-12.	Guide Pin	114
Figure C-1.	2mm Right Angle Female, 144pin Version With Guide And Coding Block	117
Figure C-2.	Female Connector With Guidance And Coding 1	122
Figure C-3.	Female Connector With Guidance And Coding 2	123
Figure C-4.	Female Connector With Guidance And Coding 3	123
Figure C-5.	Board Layout For 144 Pin Female Press-Fit Connector With Guidance	124
Figure C-6.	Board Layout For 144 Pin Female Press-Fit Connector Without Guidance	124
Figure C-7.	Layout Drawing For 144 Pin Female PIHR Connector With Guidance	125
Figure C-8.	Board Layout For 144 Pin Female PIHR Connector Without Guidance	125
Figure C-9.	Female PIHR Connector Without Guidance	126
Figure C-10.	Female PIHR Connector With Guidance	127
Figure C-11.	Female Press-Fit Connector Without Guidance	128
Figure C-12.	Female Press-Fit Connector With Guidance	129
Figure D-1	Right Angle Male, 4-Pin	132
Figure D-2.	Pin Lengths For Male Connector	136
Figure D-3.	OBSAI Sequenced Preferred	136
Figure D-4.	OBSAI Non-Sequenced Alternative	137
Figure D-5.	Board Layout For Male Connector Press-Fit / PIHR, 4-Pin	138

Figure D-6a.	Male Connector Pressfit, 4-Pin	139
Figure D-6b.	Male Connector Pressfit, 4-Pin	140
Figure D-6c.	Male Connector Pressfit, 4-Pin	140
Figure D-7a.	Male Connector PIHR, 4-Pin	141
Figure D-7b.	Male Connector PIHR, 4-Pin	142
Figure D-7c.	Male Connector PIHR, 4-Pin.....	142
Figure E-1.	Straight Female Connector, 4-Pin.....	145
Figure E-2.	Board Layout For Female Connector Press-Fit, 4-Pin	149
Figure E-3.	Female Connector Press-Fit, 4-Pin.....	150

List of Tables

Table 3.3-1	Base Transceiver Station Configuration Options.....	19
Table 3.4-2	WiMAX Profiles for Initial Certification .. Error! Bookmark not defined.	
Table 3.4-3	WirelessMAN OFDM Symbol Parameters Error! Bookmark not defined.	
Table 3.4-4	Mandatory Channel Coding.....	38
Table 3.4-5	Data Rates Achieved at Various Bandwidths	39
Table 3.4-6	Summary of Radio Profile Characteristics for 3G Standards.....	43
Table 3.11-1	Sequenced Connector Pin Characteristics For P1	83
Table 3.11-2	Sequenced Connector Pin Characteristics For P2	83
Table 3.11-3	Non-Sequenced Connector Pin Characteristics For P2.....	83
Table 3.12-1	-48 VDC Supply Voltage Requirements	84
Table 3.12-2	+24 VDC Supply Voltage Requirements	85
Table 3.3-1	Base Transceiver Station Configuration Options.....	19
Table 3.4-1	Mandatory Channel Coding.....	38
Table 3.11-1	Sequenced Connector Pin Characteristics For P1	83
Table 3.11-2	Sequenced Connector Pin Characteristics For P2	83
Table 3.11-3	Non-Sequenced Connector Pin Characteristics For P2.....	83
Table 3.12-1	-48 VDC Supply Voltage Requirements	84
Table 3.12-2	+24 VDC Supply Voltage Requirements	85

1 Summary of changes

Version	Changed Item	Date
0.01	Document started	10/19/02
1.0	Document released to MB	10/17/03
1.1	Changes to mechanics & dimensioning	05/01/04
1.1	Inserted revised appendices B&C	5/10/04
1.1	Added configuration options	5/15/04
1.1	Added new architecture figure with RP4 and added RP4 description	5/15/04
1.1	Addressing principles added	5/20/04
1.1	Appendix D, E added	6/26/04
1.1	Replaced "shall" with "should" in Appendix A	7/8/04
1.1	Fixed formatting errors in Appendix D, E. Fixed dimensioning errors on p108/109. Removed highlight from text pp43, 44.	11/10/04
1.1	Moved text in Section 3.11 to 3.4.6, Power Interface	12/14/04
1.2	Changed references of PM to GPM. Changed section 3.4.6 to refer to system power only. Redrew figures in section 3.6.1.1 and 3.6.1.2. Added back (edited) section 3.11 about module power requirements.	1/16/05
1.2	Complete revision of 3.8: Start-up Principles	3/7/05
2.0	Added IEEE802.16 / WiMAX references to Sections 2.0, 3.2, 3.3	10/1/05
2.0	Added section 3.4.3.4 for IEEE802.16/WiMAX functional support	10/1/05
2.0	Removed references to RP4 as an OBSAI interface	12/20/05
2.0	Replace "Proprietary Module" with "General Purpose Module" in section 3.4.5	12/20/05
2.0	Changed references to lub and Abis interfaces to "Network Interface" as appropriate	12/20/05

Version	Changed Item	Date
2.0	Updated baseband and RF module descriptions in WiMAX section	27-Apr-06
	Approved by Management Board	

2 Scope

The OBSAI family of specifications provides the architecture, function descriptions and minimum requirements for integration of a set of common modules into a base transceiver station (BTS). As a minimum, the BTS will have the capability to be configured from a set of common modules in order to support one or more current or future wireless network access standards as described herein. The technical requirements contained in the OBSAI family of specifications form an interface specification to ensure compatibility and interoperability among and between the set of common modules. The requirements do not address the quality or reliability of service of the access standards, nor do they cover measurement procedures.

This document describes the following:

- Reference architecture and common functional blocks
- Functions performed by each module in the common set of modules
- Relationships between modules and functions
- Module form, fit and dimensioning
- Physical and logical interfaces between the modules for the transport of signaling and user data between modules
- System growth and expansion capabilities
- Supported network interfaces such as Iub for 3GPP and Abis interface for 3GPP2
- Supported external interfaces to User Equipment (UE).
- Configurability to support different access technologies such as GSM/EDGE, CDMA2000, WCDMA or IEEE802.16/WiMAX.
- Interchangeability criteria
- Redundancy provisions for different access technologies
- Operation, administration, management and provisioning (OAM&P) criteria
- Safety and fail-safe operation

This approach to writing the set of compatibility specifications is intended to provide the BTS integrator with sufficient flexibility to respond to differences in access technologies, configurations, reliability, capacity, etc. Furthermore, it defines the architecture with the flexibility to integrate future capabilities that cannot be defined at this time.

3 Reference Architecture

3.1 Open Architecture Objectives

The general principles guiding the definition of the architecture and interfaces for the open base transceiver station (BTS) are the following:

- Define an open, standardized internal modular structure of wireless base stations.
- Define a set of standard BTS modules with specified form, fit and function such that BTS vendors can acquire and integrate modules from multiple vendors in an OEM fashion.
- Define open, standards-based digital interfaces between BTS modules based on a logical model of the entity controlled through the interfaces.
- Define open, standards-based interfaces to assure interoperability and compatibility between BTS modules.
- Define an open, standardized interface for exchange of clock and synchronization signals that meet the timing, frequency stability, phase noise and jitter constraints of supported air interfaces.
- Define a set of standard OAM&P principles for integration of multiple modules from multiple vendors into a functioning base station.
- Define the internal modular structure for the base station to allow scalability for small to large capacity configurations.
- Define the internal modular structure for the base station to support concurrent operation with different air interface standards.

3.2 Architecture Overview

Figure 3.2-1 shows the reference architecture for the OBSAI base transceiver station (BTS) reference architecture. The architecture elements consist of the following:

- Functional blocks consisting of the Transport Block, Control and Clock Block, Baseband Block and RF Block. A block represents a logical grouping of a set of functions and attributes. A block may consist of one or more modules, each of which represents a physical implementation of a subset of the block functions.

- External network interface. Examples are: (Iub) to the Radio Network Controller (RNC) for 3GPP systems, (Abis) to the Base Station Controller (BSC) for 3GPP2 systems, R6 to ASN GW (centralized GW) or R3 to CSN (distributed GW) for 802.16/WiMAX system.
- External radio interface. Examples are Uu or Um to the User Equipment (UE) for 3GPP systems (i.e., GSM or WCDMA), Um for 3GPP2 systems (i.e., CDMA) or R1 for IEEE802.16/WiMAX.
- Internal interfaces between BTS functional blocks designated as Reference Point 1 (RP1), Reference Point 2 (RP2), Reference Point 3 (RP3). RP1 includes control data and clock signals to all blocks. RP2 provides transport for user data between Transport Block and Baseband Block. RP3 provides transport for air interface data between Baseband Block and RF Block. RP4 provides the DC power interface between the internal modules and DC power sources.

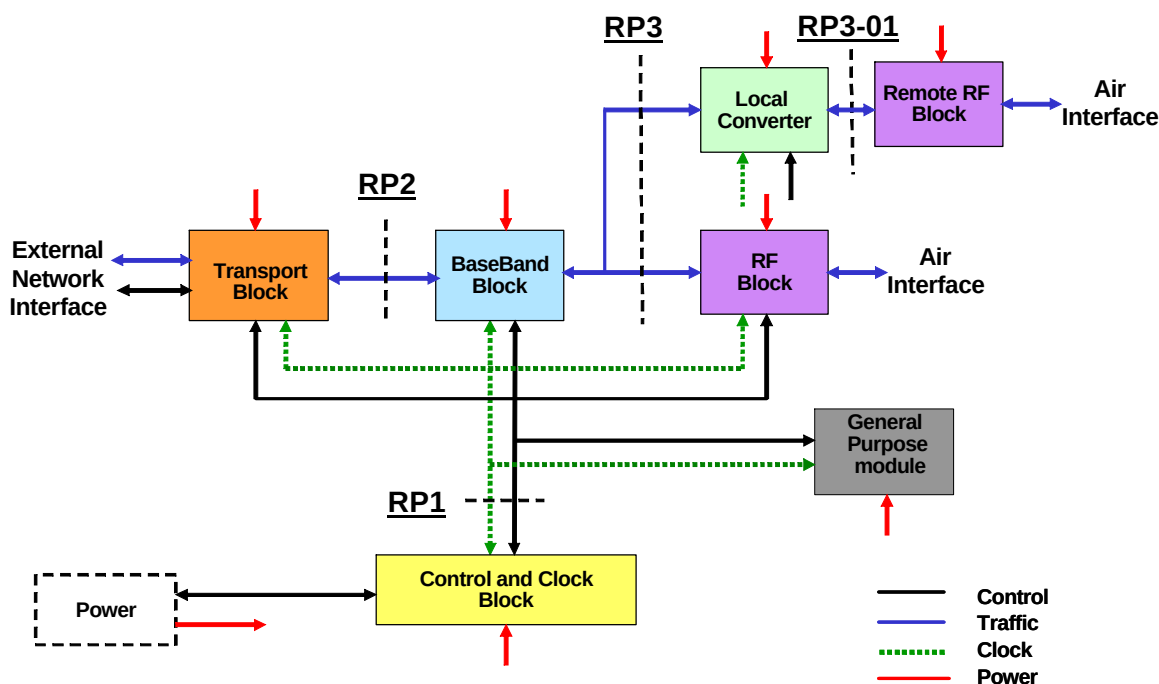


Figure 3.2-1 BTS Reference Architecture

External Network Interfaces. The external network interface to the RNC, BSC or ASN-GW provided by the Transport Block shall transport user data and control data over a suitable communications path such as T1, E1, DS3, OC1, OC3, Ethernet, or DSL. For 3GPP systems, the logical interface is designated by the Iub described in 3GPP Series 25.4xx specifications. GSM/EDGE specifications are given in Series 3GPP/04.xxx and 05.xxx for air interface and 08.xxx for transport

interface. For 3GPP2 systems the logical interface is specified by the Abis interface in TIA/EIA IS-828-A specifications.

The external interface to the UE transports user data and signaling data over the air interface. For 3GPP systems, the logical interface to UE is specified by the Uu described in 3GPP Series 26.4xx specifications. For 3GPP2 systems the logical interface to UE is specified by the Um described in IS-2000 specifications. For IEEE802.16/WiMAX the interface to the Access Terminal is specified in the IEEE802.16 -2004 and IEEE802.16e specifications.

Block Structure. Each block in the reference architecture of Figure 3.2-1 represents a logical separation of BTS functions in protocol processing. A block may consist of one or more modules that execute a subset of block functions. A module represents a physical realization of block functions.

Reference Point Function Reference Point 1 (RP1) interchanges control, performance, status, alarm and provisioning data between the Control and Clock block and other BTS blocks with the protocol specified in the OBSAI RP1 Specification document. RP1 also defines an open, standardized interface for exchange of clock and synchronization signals that meet the timing, frequency stability, phase noise and jitter constraints of supported air interfaces. The interface employs a common clock rate for generation of system clock signals for all blocks and modules within each block.

Reference Point 2 (RP2) interchanges user data packets between the Transport Block and the Baseband Block with the protocol specified in the OBSAI RP2 Specification document.

Reference Point 3 (RP3) interchanges formatted air interface user and signaling data user between the Baseband Block and the RF Block with the protocol specified in the OBSAI Reference Point 3 Specification.

3.3 Architecture Configurations

Table 3.3-1 and Figure 3.3-1 illustrates different configurability options supportable for the reference point interfaces for GSM/EDGE, CDMA2000, WCDMA and IEEE802.16/WiMAX. Based on the configuration option ranges, the following maximum constraints apply: (a) 31 RP1 ports per TM; (b) 9 RP3 ports per BBM; (c) 12 RP3 ports per RFM. Not all possible combinations listed in Table 3.3-1 are allowable, however.

Table 3.3-1 Base Transceiver Station Configuration Options

		GSM/EDGE	WCDMA	CDMA	WiMAX
Frequency band(s)		800,900,1800, 1900	1800,1900, 2100	800,1900, 2100	2.5, 3.5, 5.8 GHz
Number of carriers/sec		1.....16	1...4	1....15	1...15
Number of sectors		1-6	1-6	1-6	1-6
Transport Modules		1-2	1-2	1-2	1-2
Control & Clock Modules		1-2	1-2	1-2	1-2
Baseband Modules		1-12	1-6	1-12	1-12
RF Modules		1-9	1-9	1-9	1-9
Antennas /sector	Regular	2-4	2-4	2-4	2-4
	Smart Antenna	4-8	4-8	4-8	4-8

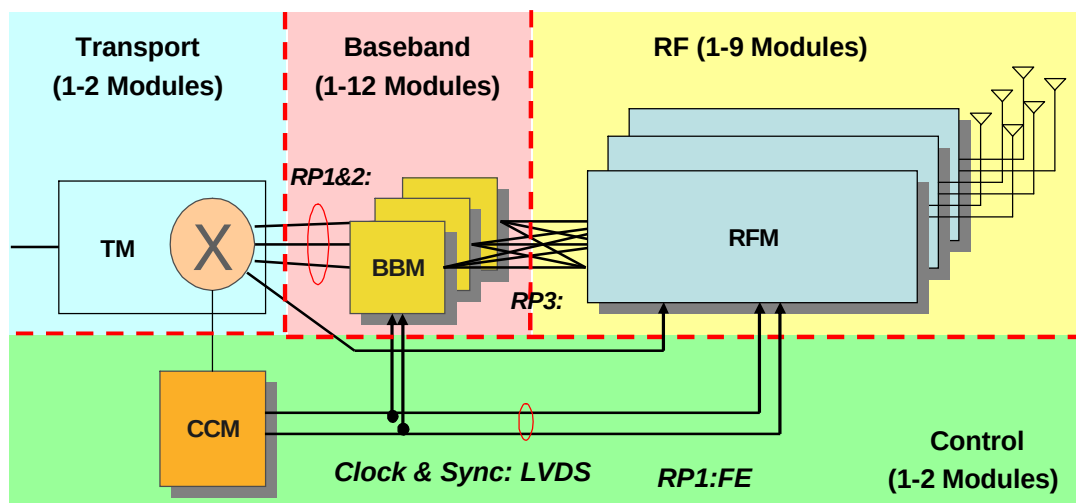


Figure 3.3-1 BTS Module Configuration Options

3.4 Block Functional Specifications

The OBSAI incorporates the following BTS functional blocks:

- Transport Block (TB)
- Control and Clock Block (CCB)
- Baseband Block (BB)

- RF Block (RFB)
- Optional General Purpose Block

Each block consists of one or more modules based on access technology, configuration and reliability implementations.

3.4.1 Transport Block (TB)

The Transport Block consists of one or more modules that perform the functions described below. The Transport Block shall provide the capability for concurrent operation of two or more air interface standards as described herein. Each module shall provide one or more Network Interface(s) at the front panel. The OBSAI BTS shall have the capability to add a Transport Block module without powering down the BTS. Redundancy requirements of the Transport Block are defined in Section 3.9.

3.4.1.1 Transport Function List

The following lists the functions performed by the Transport Block:

- External Network Interface Functions
- Internal Networking Functions
- QoS Functions
- Network Interface Protocol Termination
- Synchronization Functions
- OAM&P Functions
- Security Functions

3.4.1.2 Transport Function Descriptions

3.4.1.2.1 External Network Interface

The Transport Block interfaces to external systems (RNC / BSC / ASN-GW or CSN) via the Network Interface and to BTS internal functional blocks via interfaces defined by the OBSAI Reference Point 1 Specification and the OBSAI RP2 Specification. The Transport Block shall perform interworking function between external network interface and the RP1 and RP2 interfaces. The types of Network Interfaces supportable by the Transport Block consist of, but shall not be limited to, the following:

- ATM / IMA over (Nx) E1 / T1 / J1
- IP over PPP / MP over (Nx) E1 / T1 / J1
- IP over PPP / MP over (Nx) ATM over E1 / T1 / J1
- IP over ATM / IMA over (Nx) E1 / T1 / J1
- ATM over E3 / T3
- IP over PPP over E3 / T3
- IP over ATM over E3 / T3

- ATM over SDH STM-1 / SONET OC-3
- IP over ATM SDH STM-1 / SONET OC-3
- IP over ATM SDH STM-1 / SONET OC-3
- ATM over HDSL / SDSL / SHDSL / VDSL
- IP over ATM over HDSL / SDSL / SHDSL / VDSL
- IP over Ethernet 10Base-T/100Base-T/1000Base-T

The Transport Block shall support multiple Network Interfaces to enable various RAN / BSS topologies (e.g. star, chain, and ring) without the need for other equipment. Depending on the transport technology, this function refers to ATM multiplexing / cross-connection / switching or IP routing. The number and type of those Network Interfaces is not specified.

Upper protocol layers (Radio Network Layer, RNL) may be RAN / BSS vendor proprietary or defined by standardization bodies dedicated to the specification of RAN / BSS network interface functions (e.g. 3GPP Iub NBAP and FP, 3GPP2 Abis). The Transport Block shall support only Transport Network Layer (TNL) functions. It shall not perform any RNL related tasks. In particular the Transport Block shall not terminate any RNL related protocols. All RNL traffic (User Plane, Control Plane and Management Plane) is passed transparently through the Transport Block, but shall be handled according to associated QoS attributes.

In case the Network Interface is ATM based, the Transport Block shall terminate the ATM and AAL layers and support an ATM-IP-Interworking Function (AIWF). The AIWF shall be linked to the TNL Resource Management Function located at the Control and Clock Block.

Depending on the Network Interface, the following protocol terminations shall apply:

- If the Transport Block supports low-capacity Network Interfaces (e.g. E1 / T1 / J1), the Transport Block shall support inverse multiplexing techniques:
- If the Transport Block supports PPP Multilink Protocol (MP), the Transport Block shall use [RFC 1990]
- If the Transport Block supports Inverse Multiplexing for ATM (IMA), the Transport Block shall use [af-phy-0086.001]
- If the Transport Block supports Multi-Class Extension to Multi-Link PPP (MCMP), the Transport Block shall use [RFC 2686]
- If the Transport Block supports Differentiated UBR (DiffUBR), the Transport Block shall use [af-tm-add]
- If the Transport Block supports IP header compression techniques, the Transport Block shall use [RFC 2507], [RFC 2508] and [RFC 2509] (PPP mapping).
- If the Transport Block supports IP packet scheduling and prioritization using the principles of Differentiated Services

(DiffServ), the Transport Block shall use [RFC 2474], [RFC 2475], [RFC 3086], [RFC 2597], [RFC 2598] and [RFC 3140].

3.4.1.2.2 Internal Networking Functions

The Transport Block shall convey following types of information between the Network Interface and the RP1 and RP2 Interfaces:

- User Plane data (U-Plane) via RP2
- Control Plane data (C-Plane) via RP1
- Management Plane data (M-Plane) via RP1

If the Network Interface is IP based (depending on RAN / BSS standard version), the Transport Block shall act as an IP router between those interfaces.

RP1 and RP2 interfaces to the Transport Block shall use a single transport infrastructure built upon well-known LAN technologies, namely Ethernet and IP. Detailed characteristics of the RP1 and RP2 Interfaces are defined by the OBSAI Reference Point 1 Specification and OBSAI Reference Point 2 Specification.

The Transport Block shall support communication between other BTS blocks via RP1. The Ethernet switching function shall be part of the Transport Block. For details, refer to the OBSAI Reference Point 1 Specification.

Addressing principles for RP1 and RP2 are defined in the OBSAI Reference Point 1 Specification and the OBSAI Reference Point 2 Specification.

3.4.1.2.3 QoS Functions

The Transport Block shall maintain Quality-of-Service on the TNL based on the requirements set by the RNL. This function shall implement the established throughput, delay, delay variation and drop rate limits. It shall include packet fragmenting and reassembly. It may include multiple-link-multiplexing/demultiplexing if necessary to meet throughput and delay requirements. It may also include congestion management, prioritization and resource reservation.

The latency (delay) introduced by the Transport Block (Network Interface to RP1 and RP2 Interfaces and Network Interface to Network Interface) shall not exceed 1ms.

Ethernet switching shall be supported between modules interfaced to RP1 and RP2 Interfaces. The delay between any two Ethernet-switched interfaces shall not exceed 100μs.

3.4.1.2.4 Synchronization Functions

The Transport Block shall provide synchronization information, such as clock signal and Synchronization Status Messages (SSM) extracted

from ingress Network Interface(s), for further processing at the Control and Clock Block to derive synchronization and clock signals when synchronous backhaul links are used.

In addition, the Transport Block shall be able to synchronize the egress Network Interface(s) based on the following:

- A clock signal recovered from a selected ingress Network Interface
- A clock signal received from the Control and Clock Block
- A free-running clock

3.4.1.2.5 OAM&P Functions

The Transport Block shall conform to the BTS system level OAM&P architecture which is defined in Section 3.5. Additional details specific to this block are available in the OBSAI Transport Module Specifications.

3.4.1.2.6 Security Functions

The Transport Block may provide Security functions for OAM&P messages, control plane (C-Plane) messages and user plane (U-Plane) messages communicated over network interfaces. If supported, the Transport Block shall terminate a secure tunnel using IPSec techniques where the payload information can be routed further to its destination (e.g. the Control and Clock Block).

These functions include the following:

- Access control
- Connectionless integrity
- Data origin authentication
- Rejection of replayed packets
- Confidentiality (encryption)

3.4.2 Control and Clock Block (CCB)

The Control and Clock Block is the primary control processor for the BTS. The CCB shall control BTS resources, supervise all BTS activities, monitor BTS status and report BTS status and performance data.

The Control and Clock Block shall consist of one or more modules that perform the functions described below. The CCB shall provide the capability for concurrent operation of two or more air interface standards as described herein. The OBSAI BTS shall have the capability to add a Control and Clock Block module (CCM) without powering down the BTS.

If the processing capacity of the Control and Clock Block is scalable or if the processing functions are capable of load sharing, the BTS shall be capable of adding or removing a second CCM without powering down the BTS.

Redundancy requirements of the Control and Clock Block are defined in Section 3.9

3.4.2.1 Control and Clock Block Function List

The following lists the functions performed by the Control and Clock Block:

- Congestion Control
- Admission Control
- BTS Level OAM&P Functions
- BTS Configuration Management and Control
- Radio Resource Management
- Multi-vendor Configurations
- RF Scheduling
- Network Interface (NI) Signaling Termination
- System Clock Generation and Distribution

3.4.2.2 Control and Clock Block Function Description

3.4.2.2.1 Congestion Control

The congestion control function in the CCB determines and reports the occurrence of Transport Block, Baseband Block or RF Block resource overload thresholds conditions in the BTS. The congestion control function determines corrective action needed to restore the system to a stable state.

3.4.2.2.2 Admission Control

The purpose of the admission control is to admit or deny new users, new radio access bearers or new radio links (for example, due to handover). The admission control should avoid overload situations and base its decisions on interference and resource measurements. The admission control is employed at, for example, initial UE access, RAB assignment/reconfiguration and at handover. These cases may give different results depending on priority and call loading.

The Serving RNC performs admission Control towards the network interface.

3.4.2.2.3 BTS Level OAM&P Functions

The Control and Clock Block shall conform to the BTS system level OAM&P architecture described in Section 3.5. Additional details

specific to this block are available in the “Control and Clock Module Specifications”.

3.4.2.2.4 Radio Resource Management

The Resource Management function shall allocate and de-allocate the BTS radio resources. This includes the following:

- Call admission control
- Transmit power allocation
- Channel element allocation/deallocation
- Walsh code allocation
- Data call admission control
- Radio channel rate setting
- Service mode setting
- Test channel elements
- Take channel elements out of service and return them to service
- Paging channel processing
- Processing of request and release messages for fundamental, supplemental, and control channels

3.4.2.2.5 Multi-Vendor Configurations

The Control and Clock Block shall provide the high-level interface to other BTS modules from various vendors. This function performs any interoperation function needed to allow the Control and Clock Module to communicate with Transport Modules, Baseband Modules and RF Modules from different vendors.

3.4.2.2.6 RF Scheduling

The Control and Clock Block shall perform RF scheduling functions.

3.4.2.2.7 Network Interface Signaling Termination

The Signaling Termination function terminates the backhaul signaling protocols.

3.4.2.2.8 System Clock Generation and Distribution

The System Clock Generation and Distribution function shall generate the clock signals needed by the BTS for each supported air interface and shall distribute the respective signals to the appropriate modules. This function shall perform clock monitoring, clock selection and clock switchover.

3.4.3 Baseband Block

The Baseband Block shall consist of one or more modules that perform baseband processing for the air interfaces that include, but are not limited to, those described below. The Baseband Block shall provide

the capability for concurrent operation of two or more of the following air interface standards:

- 800 (GSM, CDMA2000)
- 900 (GSM)
- 1800 (GSM – Europe)
- 1800 (CDMA Korea)
- 1900 (GSM, WCDMA, CDMA2000)
- 2100 (WCDMA)
- 2300 (WiMAX)
- 2500 (WiMAX)
- 3500/3600 (WiMAX)
- 5800 (WiMAX – Unlicensed)

The OBSAI BTS shall have the capability to add or remove a Baseband module (BBM) without powering down the BTS.

Redundancy requirements of the Baseband Block are defined in Section 3.9.

3.4.3.1 Baseband block – GSM/EDGE Systems

For GSM systems the Baseband Block shall provide the common and dedicated channel functions in accordance with the GSM requirements of 3GPP. GSM/EDGE baseband algorithms are applied to logical and physical channels. Logical channels can be divided into traffic and signaling channels as described in 3GPP TS 05.01. A physical channel is defined as a sequence of TDMA (Time Division Multiple Access) frames at specific carrier, a time slot number (modulo 8) and a frequency hopping sequence.

3.4.3.1.1 GSM Function List

The following lists the functions performed by the Baseband Block when configured to support GSM/EDGE:

- Channel encoding/decoding
- Interleaving/de-interleaving
- Bit detection
- Frequency hopping
- Ciphering/deciphering
- DL diversity transmission (MIMO, etc.)
- UL diversity reception, IRC reception, SA reception
- Protocol frame processing

3.4.3.1.2 Channel Encoding/Decoding

This function performs GSM channel coding and decoding in accordance with 3GPP TS 05.03. Each logical channel has its own

coding and interleaving scheme. The following sequence and order of operations is used:

- Information bits are coded with a systematic block code building words of information and parity bits
- These information and parity bits are encoded with a convolutional code
- Convolutionally encoded bits are then reordered and interleaved
- Block codes include Cyclic, Fire, and Reed Solomon codes. Block interleaving is used.

3.4.3.1.3 Bit Detection

Bit detection generates soft bits for channel decoding from user equipment (UE) uplink transmission. Intersymbol interference and other time varying channel disturbances must be taken care of by the bit detector. In the literature, there exist several algorithms for bit detection. Examples of bit detectors include adaptive linear and decision-feedback equalizers are given by Proakis.

3.4.3.1.4 Frequency Hopping

This function performs frequency hopping in accordance with 3GPP TS 05.02. In frequency hopping, time slots are sent according to a sequence of frequencies that are derived from an algorithm. The frequency hopping occurs between time slots and, therefore, an entire time slot is transmitted and received on a fixed frequency.

3.4.3.1.5 Ciphering/Deciphering

This function performs ciphering and deciphering in accordance with 3GPP TS 03.20. Data flow on the radio path is obtained by bit per bit binary addition of the user data flow and a ciphering bit stream, generated by algorithm A5. Ciphering is performed for channel encoded and interleaved data.

3.4.3.1.6 DL Diversity Transmission (MIMO, etc.)

The BB Block provides the capability to support modules that support diversity transmission from antenna configurations such as adaptive antenna arrays, orthogonal transmitter arrays, or Multiple Input, Multiple Output (MIMO) arrays.

3.4.3.1.7 UL Diversity Reception

Receiver performance can be improved by increasing the number of receiver antennas. Signals from different antennas can be combined using e.g. maximal ratio or interference rejection combining algorithms.

3.4.3.1.8 Frame Protocol Processing

This GSM BB Block function performs TRAU frame protocol processing in accordance with 3GPP GSM specifications. For down-link traffic, the GSM BB module shall receive TRAU frames embedded in IP packets from the Transport Block via from RP2 and shall extract the TRAU frame from the IP packets. For the uplink direction, speech samples or raw data is processed at the baseband and framed according to the 3GPP specification as TRAU frames. The TRAU frames shall be embedded in IP packets and communicated to the Transport Block across RP2.

3.4.3.1.9 Messages To/From RP1

The GSM Baseband Block shall interface to the Control and Clock Block through Reference Point 1 (RP1) for the exchange of control, signaling, OAM&P and clock data in accordance with the requirements of the OBSAI Reference Point 1 Specification.

3.4.3.1.10 Messages To/From RP2

The GSM Baseband Block shall interface to the Transport Block through RP2 for the exchange of user data in accordance with the requirements of the OBSAI Reference Point 2 Specification.

3.4.3.1.11 Messages To/From RP3

The GSM Baseband block shall provide the capability to interface to the RF Block through RP3 for the exchange of over-the-air user and signaling data. Downlink/uplink messages with data and fast control information are sent from baseband/RF unit to RF/Transport Block.

3.4.3.2 Baseband Block - WCDMA Systems

For WCDMA systems the Baseband Block shall provide the common and dedicated channel functions in accordance with the WCDMA requirements of 3GPP TS 25.xx. There exist a number of common and dedicated transport channels as described in 3GPP TS 25.211. A physical channel is defined by a specific carrier frequency, scrambling code, channelization code, start and stop time (duration) and, on the uplink, relative phase (0 or $\pi/2$).

3.4.3.2.1 WCDMA Function List

The following lists the functions performed by modules of the Baseband Block when configured to support WCDMA:

- Channel encoding/decoding
- Interleaving
- Rate matching
- Multiplexing/demultiplexing

- Spreading
- Power weighting & summing of physical channels
- RAKE reception
- MUD alternative
- Interference cancellation
- Interference Rejection CancellationFrame protocol processing
- Messages to/from RP1
- Messages to/from RP2
- Messages to/from RP3
- Higher layer processing (L2 and L3)
- CRC

3.4.3.2.2 Channel Encoding/Decoding

This function performs channel coding and decoding in accordance with 3GPP TS 25.212. Convolutional and Turbo encoding is applied to downlink data. Code rates 1/2 and 1/3 are used in convolutional encoding while code rate 1/3 is always applied in Turbo encoding. The coding scheme is selected according to transport channel type.

Decoding of convolution and Turbo encoded data is performed in uplink direction. Viterbi decoding may be applied to convolutionally encoded data while MAP (Maximum A Posteriori), log-MAP, max log-MAP or relevant algorithm may be used in Turbo decoding.

3.4.3.2.3 Interleaving

This function performs interleaving and deinterleaving accordance with 3GPP TS 25.212 for both in downlink and uplink directions. 1st and 2nd interleavers are block interleavers with inter-column permutations in accordance with 3GPP TS 25.212. 1st interleaver is applied to transport channel data and 2nd interleaver processes physical channel data.

3.4.3.2.4 Rate Matching

This function performs rate matching in accordance with 3GPP TS 25.212. Rate matching means that data bits are repeated or punctured based rate-matching attributes that are assigned by higher protocol layers. In the uplink direction, rate matching is used to match the total data rate of transport channels to that available in physical channels. In the downlink direction, data transmission is interrupted if the number of bits is lower than the maximum supported by physical channels.

3.4.3.2.5 Multiplexing/Demultiplexing

This function performs multiplexing and demultiplexing in accordance with 3GPP TS 25.212. In the downlink direction, transport channels are mapped to physical channels by concatenating radio frames (10 ms duration) of transport channels and then splitting the data to available

physical channels. The reverse operation, i.e. demultiplexing, is done in uplink direction.

3.4.3.2.6 Spreading

This function performs spreading in accordance with 3GPP TS 25.213. In the downlink direction, physical channel data bits are first serial-to-parallel converted to I and Q branches after which channelization operation is applied to every I and Q bit. Channelization transfers a bit to a number of chips increasing the bandwidth of the signal. Used spreading factor (SF) determines how many chips will be created. The same channelization code is applied to I and Q bits and the result is considered as a complex stream of samples which is then multiplied by a complex scrambling code. In the uplink direction, different channelization codes are applied to I and Q bit sequences.

3.4.3.2.7 Power Weighting & Summing Of Physical Channels

This function performs power weighting and physical channel summing functions. After spreading, physical channels are multiplied by a weight that defines the transmission power of the channel. A complex weight coefficient may be used to cover transmission antenna diversity and smart antenna cases. A closed loop power control algorithm influences the weight used in downlink. After spreading and weighting, channels that are targeted to the same antenna and carrier frequency are summed together in order to obtain data compression.

3.4.3.2.8 RAKE Reception

This function performs RAKE reception. In a RAKE receiver, decorrelators or fingers are allocated to multipath components of one or several receiver antennas. Channel impulse response measurements are used to detect these multipaths components. For each decorrelator output, a channel estimate is computed from known pilot symbols after which output symbols of the decorrelators are combined. In maximal ratio combining, output symbols are multiplied by the respective complex conjugates of channel estimates after which the results are added together.

3.4.3.2.9 Multi-user Detection Alternative (option)

The WCDMA BB modules may perform a multi-user detection function. Multi-user Detection (MUD) RAKE simultaneously demodulates several uplink transmissions from user equipments in the presence of multi-user interference. Instead of considering the multi-user interference as white Gaussian noise, MUD RAKE receiver attempts to exploit the structure of multiaccess interference. Several MUD algorithms have been presented since the earliest reference (see Verdu).

3.4.3.2.10 Interference Cancellation RAKE Reception (option)

The WCDMA BB modules may perform an interference cancellation function. An Interference Cancellation (IC) RAKE receiver is an example of MUD algorithm. In IC RAKE, interference of other known WCDMA code channels is subtracted away from a received signal before RAKE reception. In practice, this will result in a receiver structure where there exist several RAKE receivers for each channel and signal is regenerated between these receiver stages. Both successive and parallel interference cancellation algorithms are applied.

3.4.3.2.11 Interference Rejection Cancellation RAKE Reception (option)

The WCDMA BB modules may perform an interference rejection function. In Interference Rejection Cancellation (IRC) RAKE receiver, spatial processing over several receiver antenna elements is applied in order to reject interference from few isolated interferers. By increasing the number of receiver antennas, performance of IRC RAKE is improved.

3.4.3.2.12 Frame Protocol Processing

This function performs frame protocol processing in accordance with 3GPP 25.212 specifications. Frame Protocol (FP) packets to/from transport are carried from/to baseband unit using UDP/IP. Processing includes timing, CRC calculations, bit framing and other specified tasks.

3.4.3.2.13 Messages To/From RP1

The WCDMA Baseband Block shall interface to the Control and Clock Block through Reference Point 1 (RP1) for the exchange of control, signaling, OAM&P and clock data in accordance with the requirements in the OBSAI Reference Point 1 Specification.

3.4.3.2.14 Messages To/From RP2

The WCDMA Baseband Block shall interface to the Transport Block through RP2 for the exchange of user data. User data is carried from/to the Transport Block by IP/UDP.

Network interface Frame Protocol (FP) is terminated in baseband processing block. When ATM/AAL2 is used for carrying FP data blocks, then transport is terminating AAL2 and converting the FP packets to IP/UDP.

Dedicated Node B Application Protocol (DNBAP) may be terminated in Transport Block or it may be terminated in Control and Clock Block depending on implementation.

3.4.3.2.15 Messages To/From RP3

WCDMA BB modules in the BB Block shall provide the capability to interface to the RF Block through RP3 for the exchange of over-the-air user and signaling data. Downlink/uplink messages with data and fast control information are sent from baseband/RF unit to RF/Transport Block.

3.4.3.2.16 Higher Layer Processing (L2 and L3)

This function terminates protocol functions above Layer 1 (L1), such as Macro Diversity Combining (MDC), Media Access Control-High Speed Downlink Shared Channel (MAC-hs), MAC-e, Radio Link Control (RLC)-MAC, and PDCP.

3.4.3.2.17 Cyclic Redundancy Check (CRC)

This function performs error detection functions by means of Cyclic Redundancy Check (CRC) in accordance with 3GPP TS 25.212.

3.4.3.3 Baseband Block - CDMA2000 (3GPP2) Systems

The RF Block shall consist of one or more plug-in modules. The OBSAI BTS shall have the capability to add a Baseband Block module without powering down the BTS.

3.4.3.3.1 CDMA2000 (3GPP2) Function List

The following lists the functions performed by modules in the Baseband Block when configured to support 3GPP2 CDMA2000:

- Scrambling
- Channel encoding/decoding
- Interleaving/de-interleaving
- Multiplexing/demultiplexing:
- Mapping of transport channels to physical channels
- Spreading
- Modulation
- Power weighting & combining of physical channels
- RAKE reception with despreading, channel estimation and maximal ratio combining
- Baseband combining/distribution
- Multi-user detection (MUD)
- Packing/unpacking
- Frame protocol processing
- Messages to/from RP1
- Messages to/from RP2
- Messages to/from RP3
- Power control
- Smart antenna signal processing

- Diversity signal processing

3.4.3.3.2 Scrambling

This function provides scrambling of user data by means of user-addressed long code. In Radio Configuration 3-9, the data scrambling is accomplished by operating on groups of 2M modulation symbols with modulo-2 addition of the modulation symbols and the binary value of the long code PN chip. In Radio Configuration 10, the interleaved symbols is accomplished by exclusive-ORing a scrambling sequence with the symbols out of the interleaver (packet data scrambling).

3.4.3.3.3 Channel Encoding/Decoding

This function provides an error correction capability into the frame to combat the channel transmission errors by adding redundancy in a controlled manner. Two types of the channel codes are specified in CDMA2000: convolutional code and turbo code.

Convolutional Code. A convolutional code is generated by passing the information sequence to be transmitted through a linear finite-state shift register. A code symbol can be considered as the convolution of the input data sequence with the impulse response of a generator function. In general, the shift register consists of K stages, where K is called the constraint length of the code. In CDMA2000, K=9 is used and code rate is 1/2, 1/3, or 1/4.

Turbo Code. The fundamental turbo code encoder is built using two identical recursive systematic convolutional (RSC) codes with parallel concatenation. Its decoding is based on passing the extrinsic information in iterative fashion between two maximum a posteriori (MAP) decoders for RSC codes. A code symbol is based on the outputs of two recursive convolutional codes (constituent codes) of the Turbo code.

3.4.3.3.4 Interleaving

This function is the process of permuting a sequence of symbols, and allows an effective method for dealing with burst error channel for the coded data in such a way that the channel with burst error is transformed into a channel having independent errors. In CDMA2000, Spreading Rate 1 uses bit-reversal order/forward-backward bit-reversal order block interleavers and the interleaver with symbol separation, subblock interleaving and symbol grouping (Radio Configuration 10) and Spreading Rate 3 demultiplexes its input symbols into three blocks with N/3 symbols each before interleaving.

3.4.3.3.5 Multiplexing/Demultiplexing

This function combines one or more data blocks into a multiplex protocol data unit (MuxPDU) and combines one or more MuxPDUs into

a Physical layer SDU for transmission by the Physical layer. This function separates the information contained in physical layer SDU and directs the information to the correct entity (e.g., Upper Layer Signaling, Data Service instances, or Voice Service)

3.4.3.3.6 Spreading

This function modulates each bit of the data with an N-chip spreading code uniquely assigned to that user data channel. The spreading signal is comprised of symbols that are defined by a spreading sequence that is known to both the transmitter and receiver.

Orthogonal Spreading. The function provides orthogonality between user channels with Walsh code spreading sequences. .

Quadrature Spreading. The function modulates the I and Q components of QPSK carrier modulation with orthogonal spreading codes to uniquely identify the signals transmitted on the same carrier frequency by different sectors. The spreading sequence is a quadrature sequence of length 2^{15} for Spreading Rate 1 and each carrier of Spreading Rate 3. This sequence is called the pilot PN sequence.

3.4.3.3.7 Modulation

This function is used to transmit discrete units of information called symbols, and the information may be contained in the amplitude (e.g., on-off keying), the phase (e.g., phase-shift keying), or the amplitude and phase (e.g., quadrature-amplitude modulation) of the signal. In CDMA2000, BPSK, QPSK, OQPSK, 8-PSK and 16-QAM are used

3.4.3.3.8 Power Weighting And Combining of Physical Channels

This function divides composite RF power and assigns it to the pilot, sync, paging, and traffic channels. Walsh functions are used for channelization. Each Walsh function is assigned to each channel and combined signal is transmitted.

3.4.3.3.9 RAKE Reception With Despreading, Channel Estimation And Maximal Ratio Combining

This function allows the reception of the spread spectrum signal over a frequency-selective channel. The received signal is passed through a delay line receiver. The signal at each tap is despread with the replica of the time-delayed spreading sequence. Fading coefficient for each channel is estimated through channel estimation process. Each despread signal is then multiplied by corresponding fading coefficient and combined for demodulation. This is called the maximal ratio combining.

3.4.3.3.10 Baseband Combining/Distribution

This function allows the BB combiner to combine/distribute the same carrier/sector/path signals from/to different channel cards with channel pooling.

3.4.3.3.11 Multi-user Detection (MUD) (option)

The CDMA2000 BB modules in the BB Block may provide the multi-user detection function. This function improves the performance of spread-spectrum and antenna array systems by exploiting the structure of the multiple access interference (MAI) when demodulating the signals of a user.

3.4.3.3.12 Packing/Unpacking

This function is one way of implementing multi-user detection. It can be classified as a serial or a parallel cancellation with respect to the number of signals involved in each cancellation stage. In addition, it can be classified as a partial or a full cancellation with respect to the extent of the cancellation.

3.4.3.3.13 Frame Protocol Processing

This function defines the processing of the frame based on the protocol that is used to form the frame. Frame Protocol (FP) packets to/from transport are carried from/to baseband unit using UDP/IP. Processing is done according to the air interface standard. Processing includes timing, CRC calculations, bit framing and other specified tasks.

3.4.3.3.14 Messages To/From RP1

The cdma2000 Baseband Block shall interface to the Control and Clock Block through Reference Point 1 (RP1) for the exchange of control, signaling, OAM&P and clock data in accordance with the requirements in the RP1 Specification document.

3.4.3.3.15 Messages To/From RP2

The cdma2000 Baseband Block shall interface to the Transport Block through RP2 for the exchange of user data. User data is carried from/to the Transport Block by IP/UDP.

3.4.3.3.16 Messages To/From RP3

The cdma2000 Baseband block shall provide the capability to interface to the RF Block through RP3 for the exchange of over-the-air user and signaling data. Downlink/uplink messages with data and fast control information are sent from baseband/RF unit to RF/Transport Block. The OBSAI RP2 Specification will define the protocol used on RP2 for the exchange of user data.

3.4.3.3.17 Power Control

This function forces all users to transmit the minimum amount of power needed to achieve acceptable signal quality at BTS.

3.4.3.3.18 Smart Antenna Signal Processing (option)

This function provides the spatial signal processing that employs an array of antennas. When an array of antennas is able to change its antenna pattern dynamically to adjust to noise, interference, and multipath, it is called adaptive antenna. When the receiver selects the beam among a number of fixed beams at an antenna site, it is called switched beam systems. Smart antenna systems can include both adaptive antenna and switched beam systems.

3.4.3.3.19 Diversity Signal Processing

This function is used to reduce the effects of fading and improve the reliability of the communication without increasing either the transmitter's power or the channel bandwidth by combining the multipath signals. The OBSAI BTS shall support transmit diversity methods which include, but are not limited to, the following:

- Orthogonal Transmit Diversity per 3GPP2 CDMA2000
- Space Time Spreading per 3GPP2 CDMA2000
- Phase Sweep TX Diversity (PSTD)
- Time Delay TX Diversity (TDTD)

The OBSAI BTS shall support receive diversity methods which include, but are not limited to, the following:

- Maximum ratio combining
- MMSE

3.4.3.4 Baseband Block - WiMAX (IEEE802.16) Systems

For IEEE802.16/WiMAX systems, the Baseband Block shall provide all necessary baseband functionality in accordance with the requirements of IEEE802.16-2004 and IEEE802.16e standards.

WirelessMAN-OFDM and WirelessMAN-OFDMA are both supported in the OBSAI specifications.

- MAC
- Randomization/De-randomization
- FEC (Channel encoding/decoding)
- Interleaving/deinterleaving
- Modulation/de-modulation
- CINR (Carrier-to-Interference Noise Ratio) [or at RF, FFS]
- Baseband beam forming algorithms (Optional)
- MIMO (Optional)

- Frame construction/de-construction
- Pre-IFFT Peak Power Reduction (FFS)
- IFFT/FFT
- Cyclic Prefix addition/removal
- TDD switch control
- Time and frequency synchronization
- Equalization
- Messages to/from RP1
- Messages to/from RP2
- Messages to/from RP3
- Power control

3.4.3.4.1 MAC

The standard describes a medium access control (MAC) that controls access of the basestation (BS) and subscriber stations (SS) to the air through a rich set of features. It provides a connection-oriented service to upper layers of the protocol stack. Connections have QoS characteristics that are granted and maintained by the MAC. The on-air timing is based on consecutive frames that are divided into slots. The size of frames and the size of individual slots within the frames can be varied on a frame-by-frame basis, under the control of a scheduler in the BS.

The QoS parameters can be varied by the SS making requests to the BS to change them while a connection is maintained. QoS service in the 802.16 MAC service takes one of four forms: (a) constant bit rate grant, (b) real time polling, (c) nonreal-time polling, and (d) best effort. Through the use of flexible PHY modulation and coding options, flexible frame and slot allocations, flexible QoS mechanisms, packing, fragmentation and ARQ, the 802.16 standard can be used to deliver broadband voice and data into cells that may have a wide range of properties. This includes a wide range of population densities, a wide range of cell radii and a wide range of propagation environments. Convergence sublayers at the top of the MAC enable Ethernet, ATM, TDM voice and IP (Internet Protocol) services to be offered over 802.16.

3.4.3.4.2 Randomization/De-randomization

Data randomization shall be performed on each burst of data on the downlink and uplink in accordance with IEEE802.16 standard. The randomization is performed on each allocation (downlink or uplink), which means that for each allocation of a data block (subchannels on the frequency domain and OFDM symbols on the time domain) the randomizer shall be used independently.

3.4.3.4.3 FEC (Channel encoding/decoding)

Convolutional or turbo-encoding of data is performed in the downlink. Decoding of convolution and Turbo-encoded data is performed in uplink direction. Viterbi decoding may be applied to convolutionally encoded data while MAP (Maximum A Posteriori), log-MAP, max log-MAP or relevant algorithm may be used in Turbo decoding. Reed-Solomon and convolutional coding are mandatory forward-error correction techniques that must be used when implementing the WirelessMAN OFDM PHY. Table 3.4-1 lists the corresponding rate set along with the modulation types.

Table 3.4-1 Mandatory Channel Coding

Modulation	Code Rate
QPSK	1/2
QPSK	3/4
16 QAM	1/2
16 QAM	3/4
64 QAM	3/4
64 QAM	2/3

Note: The code rates mentioned in this table are the overall code rates achieved by Reed-Solomon and convolutional coding.

Table 3.4-2 shows the data rates achieved for various bandwidths and combination of modulation types and coding rates. A guard time value of 1/32 is used. The rates here consider the effect of PHY overhead but MAC overhead and preamble overhead are not included.

Table 3.4-2 Data Rates Achieved at Various Bandwidths

BW	Code Rate					
	QPSK 1/2	QPSK 3/4	16QAM 1/2	16QAM 3/4	64QAM 2/3	64QAM 3/4
1.75	1.04	2.18	2.91	4.36	5.94	6.55
3.5	2.08	4.37	5.82	8.73	11.88	13.09
7.0	4.15	8.73	11.64	17.45	23.75	26.18
10	8.31	12.47	16.63	24.94	33.25	37.40
20	16.62	24.92	33.25	49.87	66.49	74.81

3.4.3.4.4 Interleaving/deinterleaving

The IEEE802.16/WiMAX BB module shall perform interleaving of encoded data bits in accordance with IEEE802.16 specification. All encoded data bits shall be interleaved by a block interleaver with a block size corresponding to the number of coded bits per the allocated subchannels per OFDM symbol. The interleaver is defined by a two step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second permutation insures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of lowly reliable bits.

3.4.3.4.5 Modulation/de-modulation

Conversion of wanted data to I & Q baseband signals capable of being transmitted by OFDM or OFDMA carriers by the RF module (and vice-versa for the receive side).

3.4.3.4.6 CINR (Carrier-to-Interference Noise Ratio) [or at RF, FFS]

The baseband module can carry out an assessment of the signal quality of the received signal (or signals) by assessing the ratio of the composite carrier to the received interference and noise.

3.4.3.4.7 Baseband beam forming algorithms (Optional)

When an adaptive antenna system is employed, which utilises baseband beamforming techniques, the signal processing required to form and update the beams is performed in the baseband module. Similarly if fixed or switched beamforming is employed, this is undertaken in the baseband module.

3.4.3.4.8 MIMO (Optional)

The IEEE802.16/WiMAX BB module may provide spatial signal processing that employs an array of antennas such as MIMO, space-division multi-access (SDMA), Alamouti, etc. The multiple-antenna coding algorithm shall be performed in accordance with IEEE802.16 specification.

3.4.3.4.9 Frame construction/de-construction

The IEEE802.16/WiMAX BB modules shall perform on-air framing in accordance with IEEE802.16 standard. WirelessMAN OFDM PHY frame durations are 2 (for OFDMA), 2.5, 4, 5, 8, 10, 12.5 and 20 msec. In the case of an FDD system, uplink and downlink subframes shall be time-aligned on separate uplink and downlink channels. In the case of a TDD system, each frame shall be divided up into a downlink subframe and an uplink subframe. In both TDD and FDD modes, the length of the frame can vary per frame. In TDD mode, the division point between uplink and downlink can also vary per frame, allowing asymmetric allocation of on air time between uplink and downlink if required. The downlink frame format includes a preamble, a down-link slot location directory, an uplink slot location directory.

3.4.3.4.10 Pre-IFFT Peak Power Reduction (FFS)

In OFDM and OFDMA systems, it is possible to apply peak power reduction techniques at two points in the overall system: prior to the IFFT (which falls within the baseband module) and in the form of more conventional crest factor reduction (which falls within the RF module).

3.4.3.4.11 IFFT/FFT

The IFFT and FFT algorithms are used to convert to/from time and frequency domains when forming or decoding the multiple carriers in an OFDM or OFDMA system.

3.4.3.4.12 Cyclic Prefix addition/removal

A cyclic prefix is employed to provide a synchronisation capability for the WiMAX system.

3.4.3.4.13 TDD switch control

The baseband module provides a control signal to the RF module to indicate when the system should be in transmit mode and when it should be in receive mode.

3.4.3.4.14 Time and frequency synchronization

The baseband module must provide frequency synchronisation with the received signal and extract the frame timing of that signal.

3.4.3.4.15 Equalization

Channel equalization of the received signal is provided by the baseband module.

3.4.3.4.16 Messages to/from RP1

The IEEE802.16/WiMAX Baseband Block shall interface to the Control and Clock Block through Reference Point 1 (RP1) for the exchange of control, signaling, OAM&P and clock data in accordance with the requirements in the OBSAI Reference Point 1 Specification.

3.4.3.4.17 Messages to/from RP2

The IEEE802.16/WiMAX Baseband Block shall interface to the Transport Block through RP2 for the exchange of user data. User data is carried from/to the Transport Block by IP/UDP. WiMAX R6 interface is aligned with OBSAI RP2 interface. WiMAX user data transfer over RP2 using IP/GRE protocol should be considered because this protocol is used in R6.

The interface Frame Protocol (FP) is terminated in baseband processing block. When ATM/AAL2 is used for carrying FP data blocks, then transport is terminating AAL2 and converting the FP packets to IP/UDP.

3.4.3.4.18 Messages to/from RP3

IEEE802.16/WiMAX BB modules in the BB Block shall provide the capability to interface to the RF Block through RP3 for the exchange of over-the-air user and signaling data. Downlink/uplink messages with data and fast control information are sent from baseband/RF unit to RF/baseband Block.

3.4.3.4.19 Power control

The baseband module can control the power of the OFDM or OFDMA modulated signals, with the capability to assign each an individual power level.

3.4.3.4.20 Interference Rejection Cancellation (option)

The IEEE802.16/WiMAX BB modules may perform an interference rejection function. In Interference Rejection Cancellation (IRC) receiver, spatial processing over several receiver antenna elements is applied in order to reject interference from few isolated interferers.

3.4.3.5 Baseband Block OAM&P Functions

The Baseband Block shall conform to the BTS system level OAM&P architecture described in Section 3.4. Additional details specific to this block are available in the "Baseband Module Specifications".

The functional split between BB and RF Modules need to be defined in more detail. In RP3 work, FFT/iFFT and CP addition/removal have been assumed to be located at the BB Module.

3.4.4 RF Block

The RF Block shall consist of one or more modules that perform the RF functions described below for the air interfaces that include, but are not limited to, those listed below. The RF Block shall provide the capability for concurrent operation of two or more of the air interfaces summarized in Table 3.4-3 below. In order to ensure global implementation, the IEEE 802.16 standard has been defined with a variable channel bandwidth. The channel bandwidth can be an integer multiple of 1.25 MHz, 1.5 MHz, and 1.75 MHz with a maximum of 20 MHz. This large choice of possible bandwidths is being narrowed down to a few possibilities by the WiMax Forum, whose primary task is to ensure interoperability between implementations of the 802.16d standard by different vendors.

The OBSAI BTS shall have the capability to add or remove a RM module in the RF Block without powering down the BTS.

Redundancy requirements of the RF Block are defined in Section 3.9.

Table 3.4-3 Summary of Radio Profile Characteristics for 3G Standards

Standard	Frequency Range (MHz)		Bandwidth (MHz)	Modulation
GSM	T-GSM 380	380.2 - 389.8 / 390.2 - 399.8	0.200	0.3 GMSK, 1 bit/symbol EGPRS only: 3 δ /8 rotating 8PSK 3 bits/symbol
	T-GSM 410:	410.2 - 419.8 / 420.2 - 429.8		
	GSM 450	450.4 - 457.6 / 460.4 - 467.6		
	GSM 480	478.8 - 486 / 488.8 - 496		
	GSM 750	747 - 762 / 777 - 792		
	GSM 850	:824 - 849 / 869 - 894		
	P-GSM 900:	890 - 915 / 935 - 960		
	E-GSM 900	880 - 915 / 925 - 960		
	R-GSM 900	876 - 915 / 921 - 960		
	T-GSM 900	870.4 - 876 / 915.4 - 921		
	DCS 1800	1710 - 1785 / 1805 - 1880		
	PCS 1900	1850 - 1910 / 1930 - 1990		
3GPP W-CDMA	Band I	1920 - 1980 / 2110 - 2170	5	HPSK with RRC filter (a = 0.22), 1 bit/symbol (UL) QPSK with RRC filter (a = 0.22), 2 bits/symbol (DL)
	Band II	1850 - 1910 / 1930 - 1990		
	Band III	1710 - 1785 / 1805 - 1880		
	Band IV	1710 - 1755 / 2110 to 2155		
	Band V	824 - 849 / 869 to 894		
	Band VI	830 - 840 / 875 - 885		
3GPP HSDPA / HSUP	Band VII:	2500 - 2570 / 2620 - 2690	5	HPSK with RRC filter (a = 0.22), 1 bit/symbol (UL) QPSK with RRC filter (a = 0.22), 2 bits/symbol (DL)
	Band VIII	880 - 915 / 925 - 960		
	Band II	1850 - 1910 / 1930 - 1990		
	Band III	1710 - 1785 / 1805 - 1880		
3GPP2 CDMA	NMT 450	411 to 483 / 421-493	1.25	Chebychev low pass (FIR) QPSK/HPSK, 2 bits/symbol (UL) QPSK, 2 bits/symbol (DL)
	Band 0	824-849 / 869 - 894		
	Band 1	1850 - 1910 / 1930 - 1990		
	Band 2	872 - 915 / 917 - 960		
	Band 3	887 - 924 / 832 - 870		
	Band 4	1750 - 1780 / 1840 - 1870		
	Band 5	411 - 420 / 421 - 430		
		450 - 460 / 460 - 470 479 - 483.5 / 489 - 493.5		
	Band 6	1920 - 1980 / 2110 to 2170		
WiMAX	Fixed access: 3400-3600 (except US) Unlicensed bands Mobile access: 2300-2400 (Korea) 2500-2690 (US, Mexico, Brazil) 3600 (US - Future)		Fixed access: 1.25 to 28 MHz Mobile access: 1.25, 5, 10, 20 MHz	Fixed access: OFDM with BPSK, QPSK, 16QAM, 64QAM Mobile access: OFDMA with BPSK, QPSK, 16QAM, 64QAM

3.4.4.1 RF Block Function List

The following lists the functions performed by the RF Block:

- D/A & A/D conversion
- Up/down conversion

- Carrier selection
- Linear power amplification
- Antenna interface
- Transmit / receive RF filtering
- RF combining
- Transmit / receive RF filtering
- Diversity transmit
- Diversity receive (duplexing, etc.)
- Low noise amplification
- Peak power reduction
- OAM&P Functions
- Implementing detailed control of air interface timings
- Calibration of parallel transmit/receive channels (Optional. FFS; part of the calibration could be done at BB)

3.4.4.1.1 D/A & A/D Conversion

For the forward direction, the RF Block performs the function that converts the digital signals received from the Baseband Block into the analog format for transmission on the RF carrier. For the reverse direction, the RF Block performs the function that converts the received analog signals into the digital format for communications to the Baseband Block.

3.4.4.1.2 Up/Down Conversion

For the forward direction, the RF Block performs the function that translates and upconverts the digital signals received from the Baseband Block to the assigned carrier frequency. For the reverse direction, the RF Block downconverts and translates the received RF signals on the assigned carrier frequency into the digital format for communications to the Baseband Block.

3.4.4.1.3 Carrier Selection

This function allows the operator to select or change the carrier frequency for any module in the RF Block. For FDD operation, the carrier selection sets both transmit and receive frequencies.

3.4.4.1.4 Linearized Power Amplification

This function allows a linearized power amplifier (LPA) to amplify the transmitted signal preserving the original wave shape of the input signal at the output.

3.4.4.1.5 Antenna Interface

This function allows the RF module to send or receive RF signals through antennas. The RF modules in the RF Block shall provide a 50-ohm antenna interface.

3.4.4.1.6 RF Combining

The OBSAI BTS shall combine the outputs of RF amplifiers to drive one common antenna.

3.4.4.1.7 Transmit / Receive RF Filtering

This function rejects the local feed-through of out-of-band signals in the transmit path and the unwanted mixing image in the transmitted signal.

3.4.4.1.8 Diversity Transmit

The OBSAI BTS shall provide the capability for transmit diversity for each carrier and each sector. This function allows the base station system to transmit TX signals through polarization antenna or multiple antennas.

3.4.4.1.9 Diversity Receive

The OBSAI BTS shall provide the capability to receive RX signals through polarization antenna or multiple antennas.

3.4.4.1.10 Low Noise Amplification

This function amplifies input signal at the front-end using an amplifier with very low noise figure.

3.4.4.1.11 Peak Power Reduction

The OBSAI BTS shall provide crest factor reduction for CDMA2000, WCDMA, and OFDMA (Orthogonal Frequency Division Multiple Access) signals. This function reduces the peak power of original baseband signal for increasing the efficiency and reducing the back-off margin of power amplifier.

3.4.4.1.12 RF Block OAM&P Function

The RF Block shall conform to the BTS system level OAM&P architecture described in Section 3.5. Additional details specific to this block will be available in the OBSAI RF Block Specifications.

3.4.4.1.13 Control of Air Interface Timings

For the forward direction, the RF block aligns samples, which are received from the baseband block, with the air interface frame clock.

3.4.4.1.14 Calibration of Parallel Transmit/Receive Channels

The OBSAI BTS may optionally support smart antenna technologies. RF block supports calibration of parallel transmit and receive channels removing (minimizing) delay, phase, and amplitude differences between the channels.

3.4.5 General Purpose Block

The OBSAI BTS may have the capability to add a General Purpose (GP) module for functions not explicitly covered by the functions of the Transport Block, Control and Clock Block, Baseband Block, or RF Block. Examples of functions that might belong to a General Purpose Module include various types of network interfaces, GPS timing receiver, external alarm collection unit, etc.

The possible set of interfaces that a non-standard module may require is unknown; therefore, all interfaces for such a module cannot be standardized. However, a General Purpose Module shall meet the requirements for RP1 interface, mechanical dimensions, power and signal connectors. A General Purpose Module may interface to other modules via front panel connection, or on a backplane through use of Proprietary Reserved signal pins.

3.4.5.1 Example: Network Interface Module

An example of how a General Purpose Module might be used to implement various types of network interfaces is shown in Figure 3.4-1 below. In this example, the module in the Transport Block consists of a Router&Switch sub-module. One or more Network Interface sub-modules are implemented as modules in the General Purpose Block.

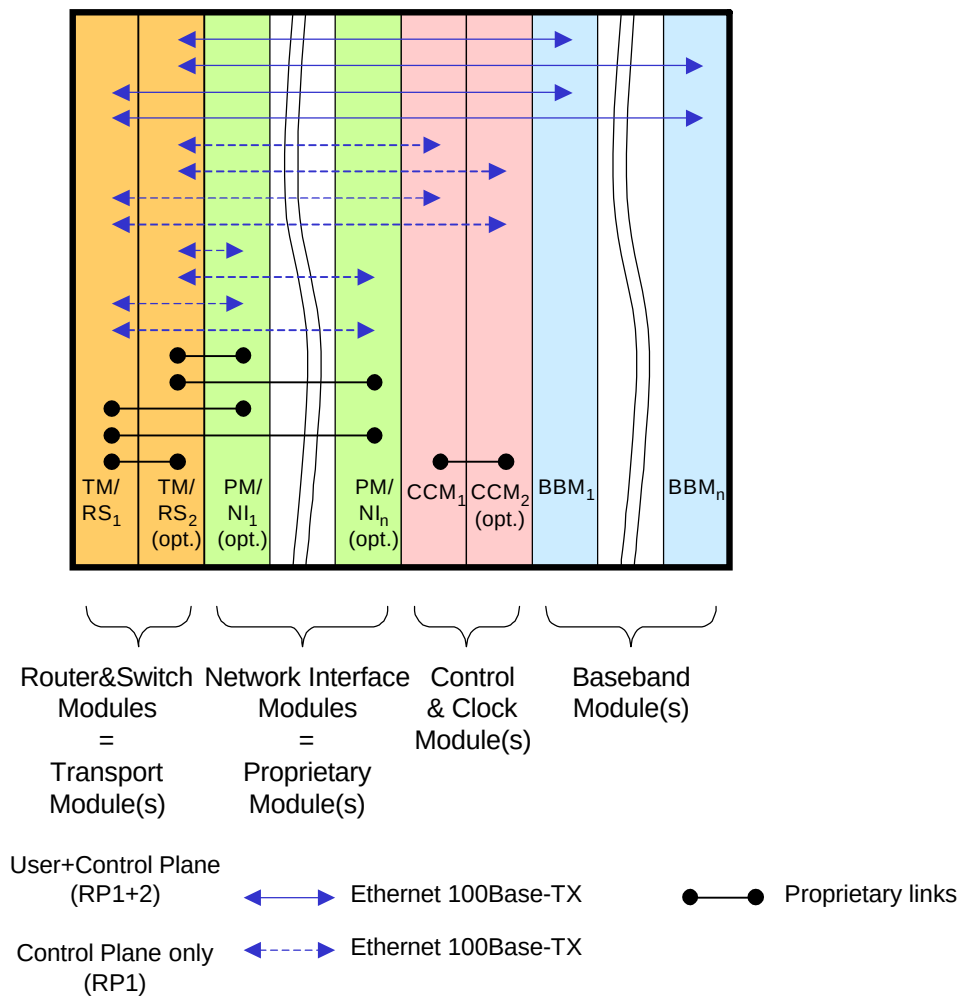


Figure 3.4-1 Example of Implementation of Module in General purpose Block

3.4.5.2 Example: External I/O Interface Module

A General Purpose Module may also be used to provide the capability for an operator to interface with external equipment or instrumentation for controlling site equipment or for collection of alarms.

3.4.5.3 Example: Extension Module

While one function of the Transport Block is to distribute the RP1 and RP2 Ethernet network to all modules in first shelf, and one function of the Control and Clock Block is to distribute timing references to all modules in that same shelf, some BTS designs require the Ethernet network as well as timing references in additional shelves as well. For this reason, the Extension Module concept was created.

The Extension Module is responsible for taking an Ethernet link from the TM, and timing reference from the CM, and providing Ethernet

connectivity as well as the timing reference to all other cards in the shelf in which the EM resides.

The number of Ethernet and timing reference ports that the Extension Module must support varies greatly from one BTS design to another. For this reason, the Extension Module will not be standardized as a part of the OBSAI specifications. It is intended that the Extension Module be designed in such a way as to interoperate with the TM and CM as described in their respective specifications.

The TM specifications include a requirement to provide enough Ethernet ports to support all of the modules that will reside in the first shelf, plus one additional port to support to an Extension Module. Likewise, the CM specifications include a requirement to provide enough Synchronization Bus ports to support all of the modules that will reside in the first shelf, plus one additional port to support an Extension Module.

The Extension module should provide enough Ethernet ports and Synchronization Bus ports to support all of the modules that are located in the shelf in which it resides plus one additional port to support another EM in another shelf. Delays in switching/routing and clock distribution should be minimized.

3.4.6 Power System Unit (PSU) Block

The system Power Module is responsible for delivering power to all operating modules of the BTS through the respective backplane of each shelf. Modules and backplanes shall provide DC isolation between the power domain and the BTS logic-common domain. DC output of the Power Module shall be isolated from chassis and earth ground, with provision for connecting the DC power return to earth ground. All conduits of the power domain shall observe the mutual creepage clearance distances between the conduits and logic-common and associated signals.

3.4.6.1 Supply Voltage

The BTS shall operate with either –48 VDC or +24 VDC nominal power.

3.5 OAM&P Principles and Architecture

The high level concepts of OAM&P functionality of the OBSAI BTS are described in this section with the scope limited to the discussion of:

- System level OAM&P implementation concepts
- Minimal BTS information model

- Protocol for internal interfaces

Refer to the OBSAI Reference Point 1 Specification, the OBSAI Reference Point 2 Specification and the OBSAI Reference Point 3 Specification for requirements related to that interface.

3.5.1 Overview of OAM&P support

OAM&P support is limited to internal functions and interfaces of the OBSAI BTS. This is shown in Figure 3.5-1. It is assumed that the ultimate responsibility of interoperating with external third party and legacy EMS/NMS lies with the BTS system integrator.

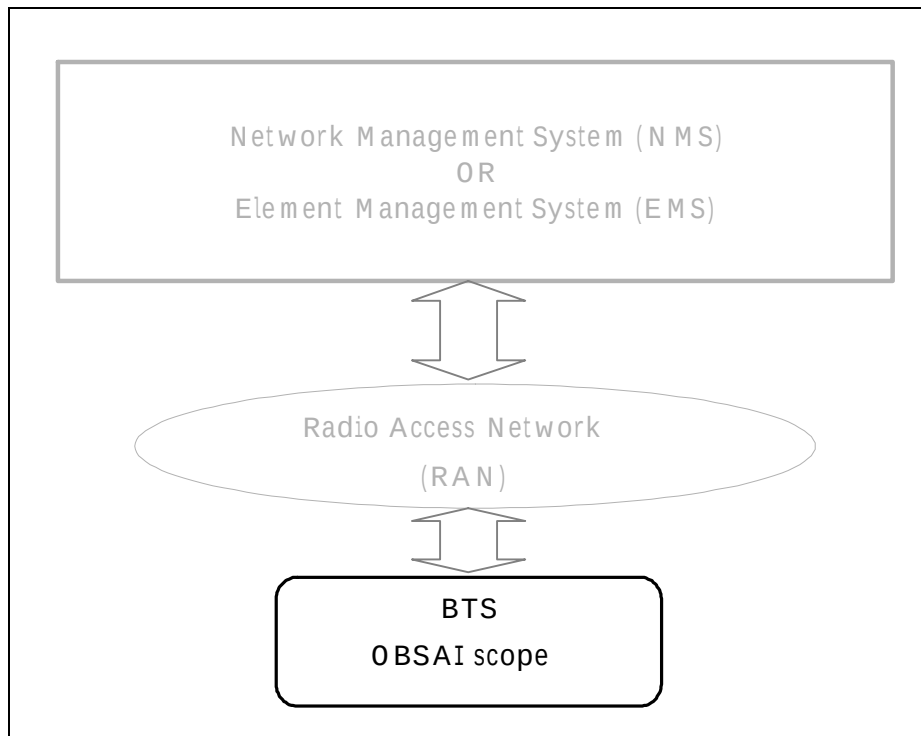


Figure 3.5-1 Network Management Hierarchy

The following basic capabilities shall be supported by the OBSAI BTS:

- Configuration management functions for enabling deployment of OBSAI BTS modules.
- Fault Management capabilities for monitoring the health of OBSAI BTS modules.
- Performance management functions for collecting performance metrics of OBSAI BTS modules.
- Software management functions related to installing, and updating software.

Section 3.5.3.1 provides an overview of the protocol stack for both internal and external interfaces.

3.5.2 OAM&P Implementation Concept

The OBSAI OAM&P support internal to the BTS shall be XML-based. The XML-based protocol enables network management via a web interface that also allows easy plug-in to legacy EMS/NMS.

The vendor modules shall support the proposed common BTS information model specific to the module as outlined in the OBSAI Reference Point 1 Specification. Module agent software shall reside on the local hardware (for example, the BBM module agent shall reside on the BBM). The communication between the module agents (BBM, RFM, TM and GPM) and the BTS master agent on the Control and Clock Block shall be via both direct and indirect interface as described in sections 3.5.2.1.1 and 3.5.2.1.2 respectively.

An external EMS/NMS shall be able to interface directly with the BTS master agent, which shall provide a conduit for managing the information pertaining to the other modules. A direct interface from an external EMS/NMS to the module agents shall not be supported.

The module vendors shall be responsible for providing module agent software. The system integrator shall have the additional responsibility of providing the management software that resides on an external EMS/NMS.

3.5.2.1 Internal Interface

The module agents in the OAM&P architecture shall have the capability to use a direct interface with the BTS master agent. A combination of direct and indirect interfaces with the BTS master agent is also possible as described below.

3.5.2.1.1 Direct Interface

If the direct interface option is chosen, then the module agents shall communicate directly with the BTS master agent as shown in Figure 3.5-2. The direct interface shall be XML-based as specified in the OBSAI Reference Point 1 Specification.

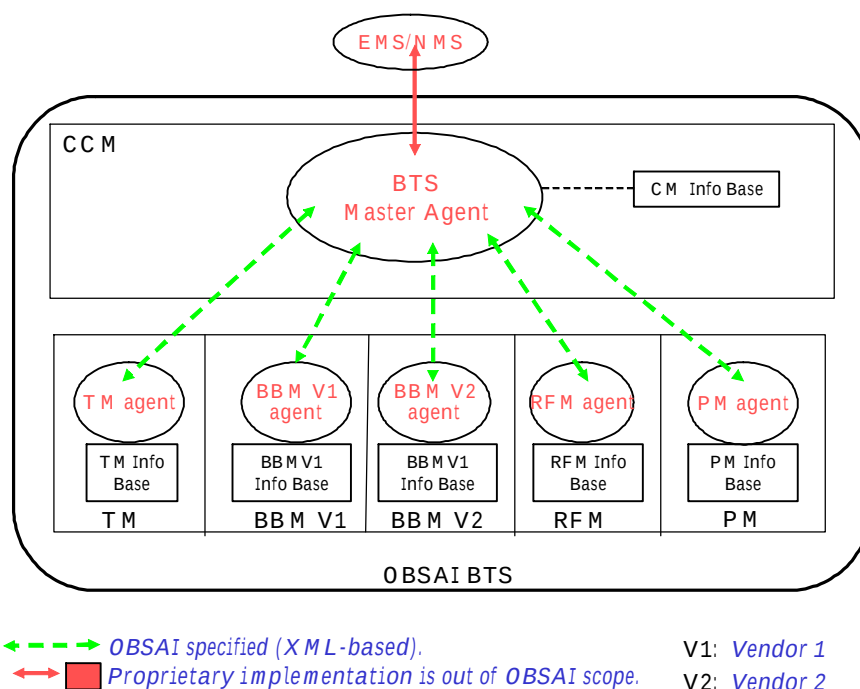


Figure 3.5-2 OAM&P BTS Internal Interface Architecture

3.5.2.1.2 Indirect Interface

In this option, each module agent shall communicate with the BTS master agent via a module proxy as shown in Figure 3.5-3. The module proxies shall be provided by the vendor of that module. The proxies shall reside on the CCM. The interface between the module agent and its proxy is not specified within OBSAI and may be XML-based or proprietary. The interface between the module proxies and the BTS master agent shall be XML-based as specified in the OBSAI Reference Point 1 Specification.

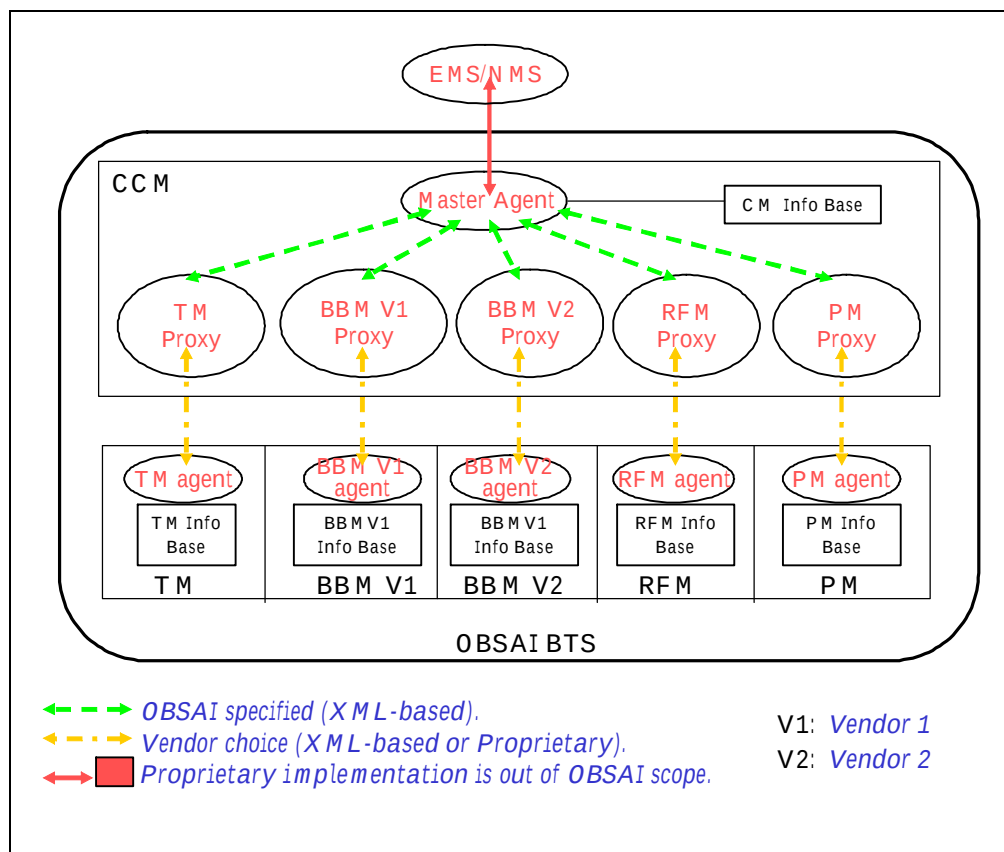


Figure 3.5-3 OAM&P BTS Internal Interface Architecture for Indirect Interface

3.5.3 OAM&P BTS Information Model

The OBSAI information model shall be logically distributed within an OBSAI BTS. This distribution is regardless of the chosen internal agent interface. The distribution of each module's information model aligns with common abstraction trends in the industry. Elements within each module's information model shall be accessed by the BTS master agent only via the module agent and/or the module proxy. Refer the OBSAI Reference Point 1 Specification for details pertaining to the OBSAI information model.

3.5.3.1 Protocol Stack

This protocol stack for the management of OBSAI BTS is shown in Figure 3.5-4.

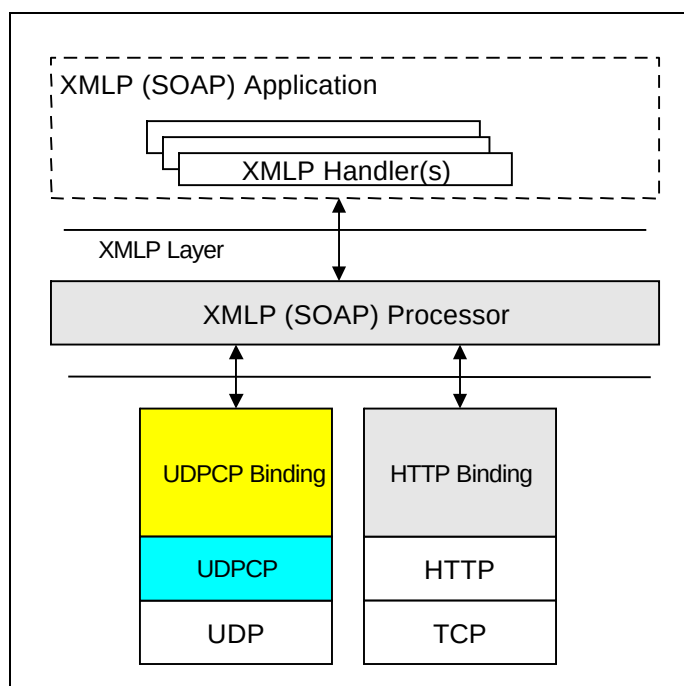


Figure 3.5-4 OBSAI Management Protocol Stack

3.6 Addressing Principles

The Addressing Principles section provides means for addressing HW and SW resources of OBSAI modules. When a module is powered up one of the first steps for the module is to create its own physical and logical addressing information to be able to initiate communication with other modules.

Ethernet MAC addresses shall be either globally or locally unique as described in section 3.6.1.

IPv6 addresses shall be created using IPv6 Stateless Address auto-configuration mechanism. For IPv4 addresses the DHCP “Dynamic Host Configuration Protocol” shall be used. These methods are described in section 3.6.2.

When a module has assigned both MAC and IP-addresses the SW resources can be addressed as described in section 3.6.3.

3.6.1 MAC Address Assignment

This section describes how 48-bit Ethernet MAC addresses are allocated. All MAC addresses shall be according to [IEEE Std 802.3]. It shall be possible to use both global and locally unique addresses.

These MAC addresses can be used both for physical MAC and logical MAC (shared virtual) purposes as mentioned in section 3.9.2.

3.6.1.1 Globally Unique MAC Address Allocation

The global MAC addresses shall have the “u” bit set to 0. This prevents overlapping with locally unique MAC addresses.

The first 24 bits of the MAC address will be reserved for company identification as assigned from IANA and shown as “c” in Figure 3.6-1. The last 24 bits are the manufacturer selected extension identifier bits, shown as “m” in Figure 3.6-1 below.



Figure 3.6-1 IEEE 802 based global MAC address

3.6.1.2 Locally Unique MAC Address Allocation

MAC Address Based On Module HW Position:

If this method is used, the MAC address shall be created as shown in Figure 3.6-2 below:



Figure 3.6-2 MAC address based on HW position

When MAC addresses are based on HW position, the “x” bit shall be set to 0. “u” is the universal/local bit and shall be set to 1, indicating local scope. “g” is the group/individual bit and shall be set to 0, indicating an individual address. The bit positions labeled “Res” are reserved bits. These reserved bits shall be set to 0. The OBSAI defined bits are described below:

- Local Cabinet ID (LCID): 3 bits. These bits are reserved for Local Cabinet identification. If Local Cabinet identification is not required, this field shall be set to 0.

- Remote Cabinet ID (RCID): 7 bits. These bits are used for identification of Remote Cabinets. All modules inside a Local Cabinet shall set this field to 0. This allows up to 127 individual RCs to be addressable from each local cabinet using the remaining unreserved RCID values. The RCID value is a logical address. However, it can be physically associated with the RC it addresses via a centralized mapping table. This allows the RCID addressing scheme to flexibly support both existing and future RC network topologies. The address generation function resident in the local cabinet shall arbitrarily assign the RCID value when an unconfigured RC boots up. The location of the address generation function in the local cabinet is not specified by OBSAI and is implementation specific.
- Subrack ID (SRID): 3 bits. These bits shall be used to identify the module subrack. *(Note: The term Subrack ID is used interchangeably with Shelf Address in OBSAI documents)*
- Slot ID: 5 bits. These bits shall be used to identify the module slot position. *(Note: The term Slot ID is used interchangeably with Module Address in OBSAI documents)*
- IF ID: 4 bits. These bits shall be used to identify one of “n” possible processor interfaces within the module.

MAC Address Based On Other Methods:

Other methods may be used when module HW position information is not available. In these cases, it is the BTS Integrator's responsibility to ensure uniqueness of these addresses. “x” bit shall be set to 1. “u” is the universal/local bit and shall be set to 1, indicating local scope. “g” is the group/individual bit and shall be set to 0, indicating an individual address. The remaining bits are not defined by OBSAI.

3.6.2 IP Address Assignment

Following sections present means for auto-configuration of IP addresses.

3.6.3 IPv6 Address Assignment

The IPv6 address shall be created using stateless address auto-configuration as described in [RFC 3513], which is based on 48-bit MAC address.

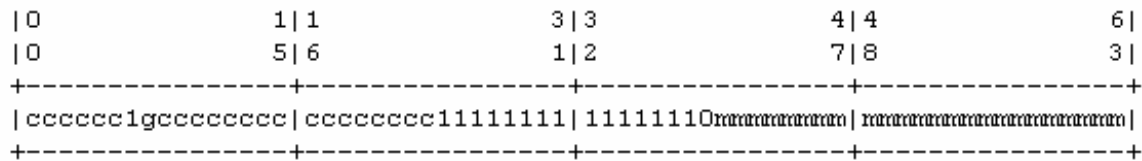


Figure 3.6-3 IPv6 address interface ID

3.6.4 IPv4 Address Assignment

The Dynamic Host Configuration Protocol (DHCP), specified in [RFC 2131] and [RFC 2132] shall be used to assign IPv4 addresses. The BTS integrator is responsible for ensuring the presence of a single active DHCP server.

3.6.5 Addressing Of Software Resources

Service Location Protocol (SLP) shall be used for resolving addresses of services provided by BTS modules. SLP is described in detail in [RFC 2608], [RFC 2609], [RFC 2614] and [RFC 3111]. The SLP specifications allow implementation with or without a Directory Agent (DA). Both methods shall be supported, but not simultaneously. The usage of DA shall be configurable to enable modules to decide whether to perform DA discovery or not. Optionally it shall be possible to use a fallback mechanism to change the selected method in case of a problem. The SLP uses URLs for addressing software resources. URL includes the name of the service, transport protocol used, the address of the service including port information. Attributes may also be provided. The format is as follows:

URL= Service:Name:protocol://IP-address:port;Attributes;

Examples of Directory Agent service and Master Agent service are illustrated below:

URL= Service:DirectoryAgent:UDP://192.168.100.1:427;

URL= Service:MasterAgent:SOAP://10.10.142.2:90;

3.6.5.1 SLP Exceptions

SLP was originally developed for use in enterprise office networks. Using the SLP in OBSAI BTS environment requires the following parameters to be redefined as follows.

3.6.5.1.1 Service Lifetime.

According to the [RFC 2608], the service lifetime can be set from 0 to approximately 18 hours (values 0 to 0xffff). In OBSAI specification the value 0 in service lifetime shall indicate infinite service registration.

3.6.5.1.2 Service Deregistration

According to the [RFC 2608], the Service Deregistration message is set to be optional. When the service lifetime is set to be infinite, Service Deregistration message is mandatory.

3.7 Synchronization

Figure 3.7-1 illustrates the synchronization hierarchy of the clock and frequency functions provided by the synchronization plane. The synchronization plane shall perform the following functions:

- Interface to one or more time and frequency sources
- Generate and distribute a common system clock and time reference signal
- Provide the capability for concurrent operation with multiple air interfaces.

The BTS shall have the capability to interface to one or more of the following input reference clock and timing sources:

- GPS based clock and time reference
- Atomic clock locked terrestrial transmission
- 10 MHz external reference such as from a rubidium clock
- 2.048 MHz external reference (typical reference in E1/T1 interface clocking)
- External core network interface

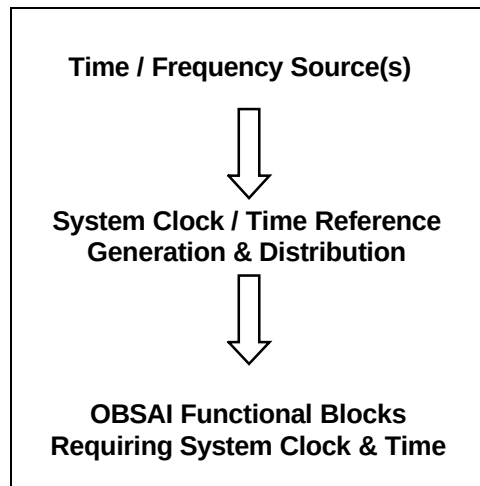


Figure 3.7-1 Synchronization Hierarchy

The BTS shall have the capability to derive time and frequency reference signaling from the input reference clock and timing source, generate internal system clock and time reference signaling required for OBSAI functional blocks, and distribute the system clock and time reference signals to OBSAI Functional Blocks. The OBSAI BTS shall use a common System Clock for synchronizing all frequencies used by Functional Blocks and system modules. The OBSAI BTS shall use one clock network to deliver clock signaling, frame timing, and time stamp for each of the air interface systems independently. The common system clock shall support concurrent operation of WCDMA, CDMA2000 and GSM/EDGE on the same BTS.

3.8 BTS Start-up and Hot Insertion/Removal Principles

This section describes the typical sequence of events that occur when a module/resource is inserted in or removed from an OBSAI BTS. The purpose of this section is to illustrate the possible occurrence of events and the use of OBSAI specified messages to manage the events. Additionally, the principles described here are not intended to include exception cases like timeouts, lost messages etc. These details are design considerations that are out of scope of this section.

The principles discussed are applicable to both a deployed BTS and a new BTS. The typical Start-up Sequence overview is shown in Figure 3.8-2.

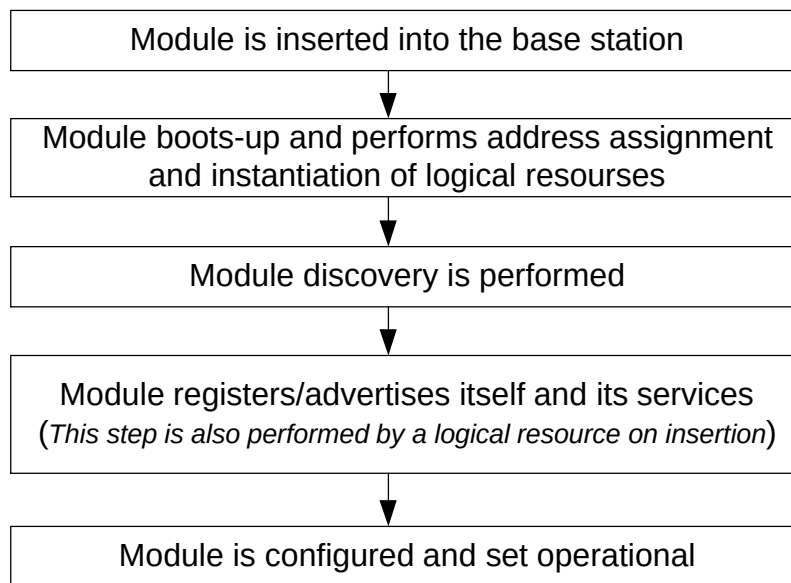


Figure 3.8-2 Start-up Sequence overview

In the case of a module insertion or removal, the entire start-up/removal sequence may be executed. In the case of a resource insertion or removal, service registration/removal may be performed (if applicable). Section 3.8.2 describes the sequence of events for a Directory Agent (DA) based implementation. Section 3.8.3 describes the typical sequence of events for a DA-less implementation.

The described principles use the following OBSAI specifications and guidelines (refer OBSAI System Reference Document and RP1 Specifications):

- OBSAI OAM&P Interface Specifications
- OBSAI HW and SW Addressing Principles
- Service Location Protocol Specifications (RFC 2608)

It is assumed that all physical module properties are described in a Module Property File (MPF) provided by the module vendor. The file format is not specified but it is recommended that it be in XML-format.

3.8.1 Concepts and Definitions

Auto Detection: Service provided by CCM and other modules to monitor for Module Ready Indication messages at configured intervals sent by other modules and CCM respectively. The details of the Module Ready Indication Message are provided in the OBSAI OAM&P CM Interface Specification.

Module/Resource Removal: Physical removal or failure related unavailability of a module/resource.

Start-up: Sequence of events that occur within a module when it or the entire BTS is restarted.

3.8.2 Principles for DA-based Implementation

Typical CCM Start-up scenario (after boot-up and address generation) for DA-based implementation is illustrated in section 3.8.2.1. Module Start-up scenario is illustrated in section 3.8.2.2. Module Removal scenario is described in section 3.8.2.3.

3.8.2.1 CCM Start-up

The following sequence diagram applies to the case of the Active CCM:

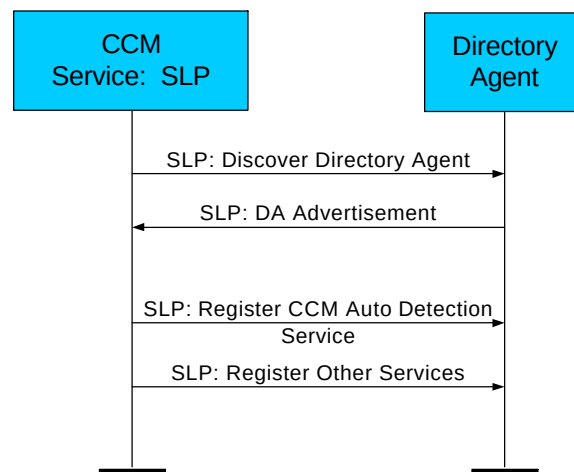


Figure 3.8-2 CCM Start-up (DA-based)

3.8.2.2 Module Start-up (except CCM)

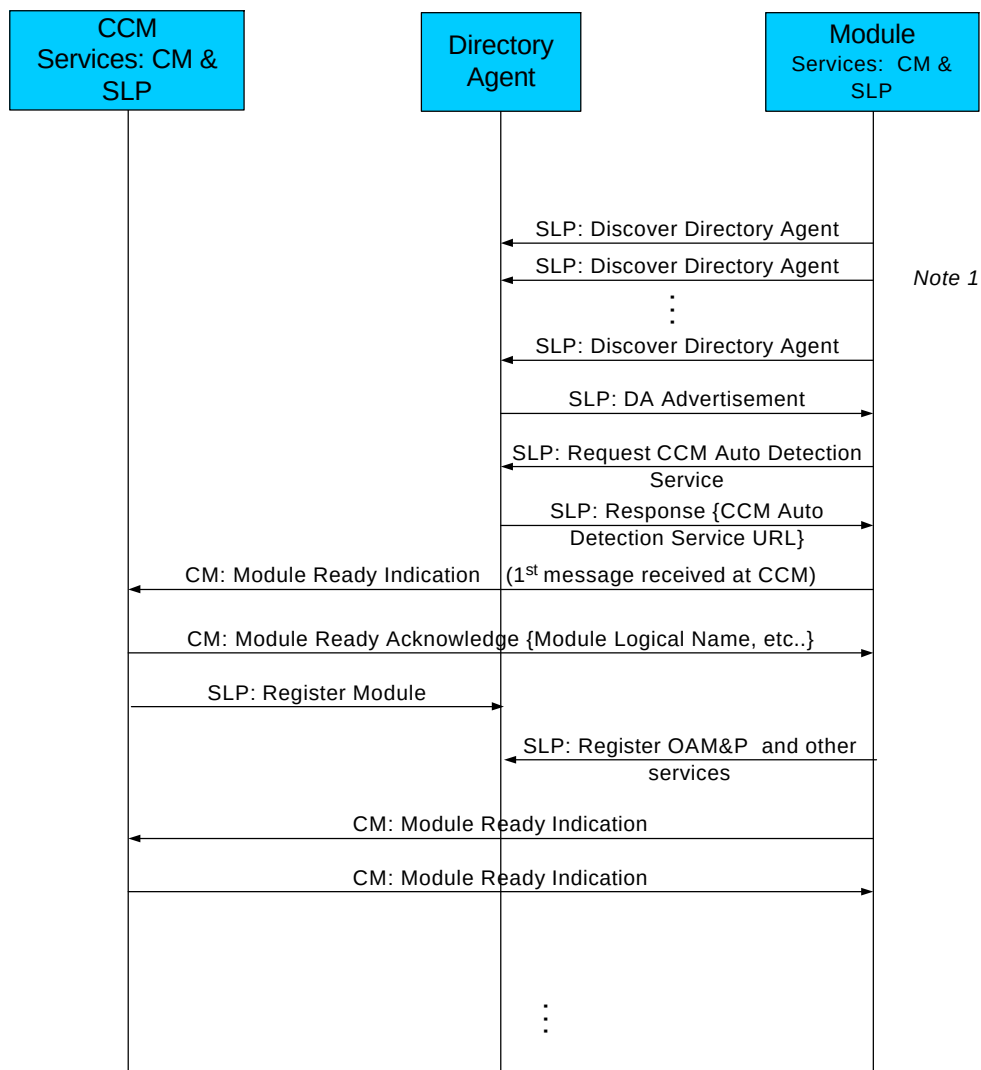


Figure 3.8.2.23.8-3 Module Start-up (except CCM)

Note 1: The discover Directory Agent message shall be repeated until a response is received.

3.8.2.3 Module/Resource Removal

This section illustrates the detection of ungraceful removal of a module/resource. It is assumed that module/resource de-registers its services when it is removed gracefully.

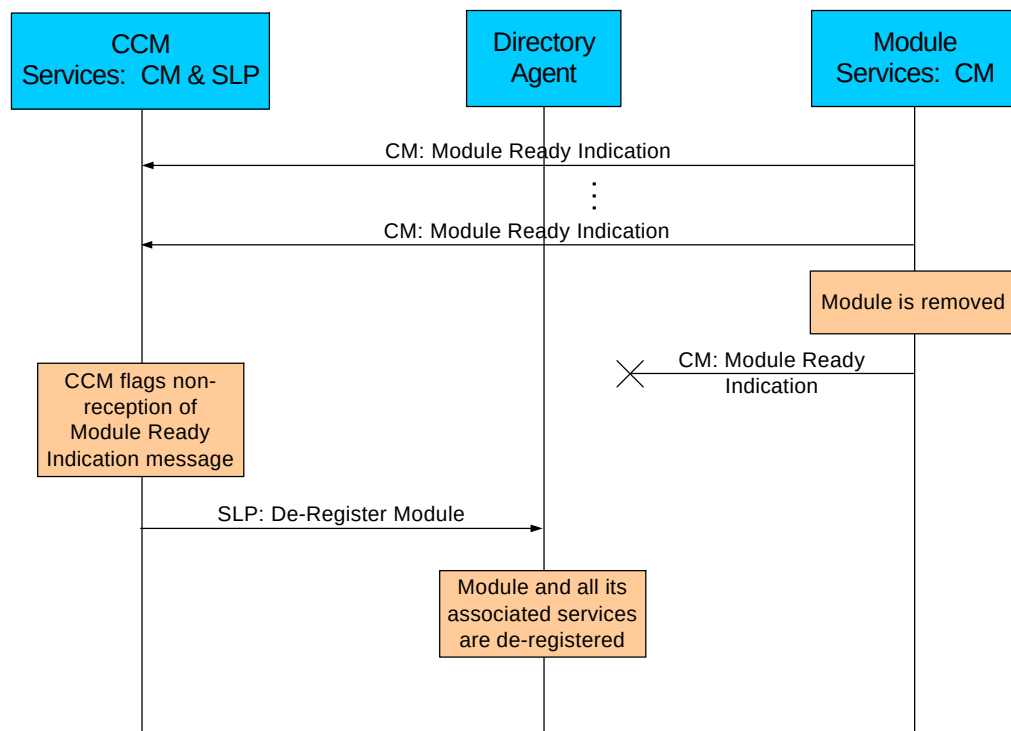


Figure 3.8-4 Module Start-up (except CCM)

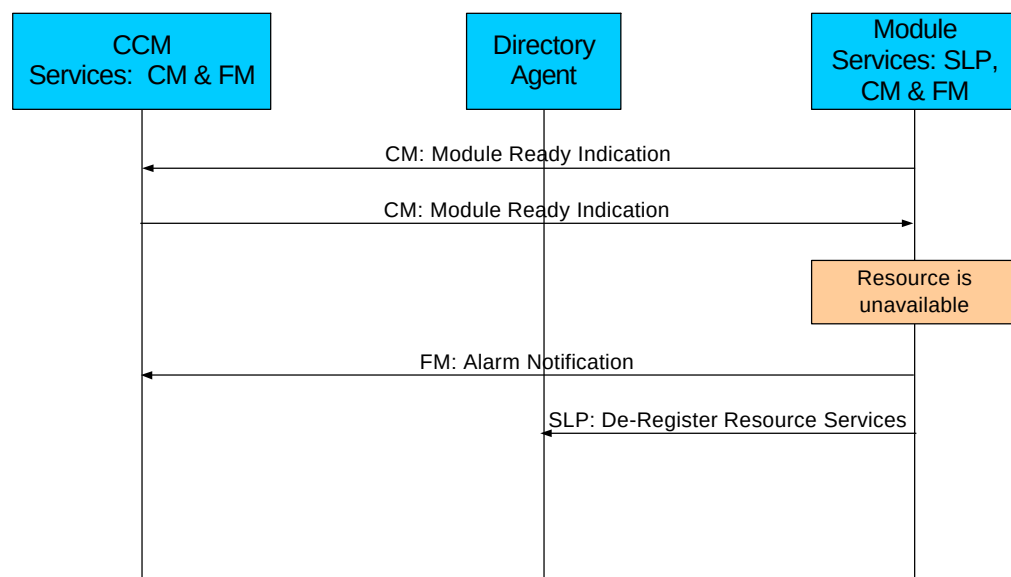


Figure 3.8-5 Module Start-up (except CCM)

3.8.3 Principles for DA-less Implementation

Typical hot insertion scenario (after boot-up and address generation) for DA-less implementation is illustrated in section 3.8.3.2 and the corresponding hot removal scenario is illustrated in section 3.8.3.3.

3.8.3.1 CCM Start-up

The following sequence diagram applies to the case of the Active CCM. The CCM shall advertise its auto-detection services when it is restarted.

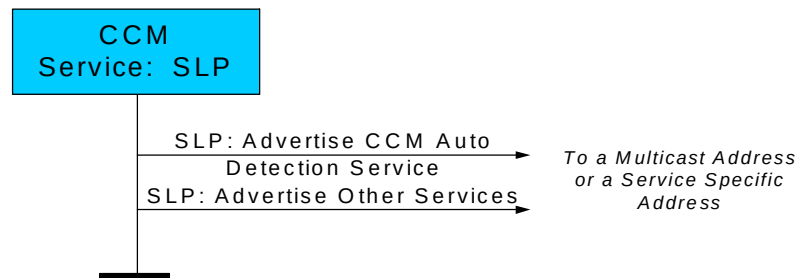


Figure 3.8-6 CCM Start-up (DA-less Implementation)

3.8.3.2 Module Start-up (except CCM)

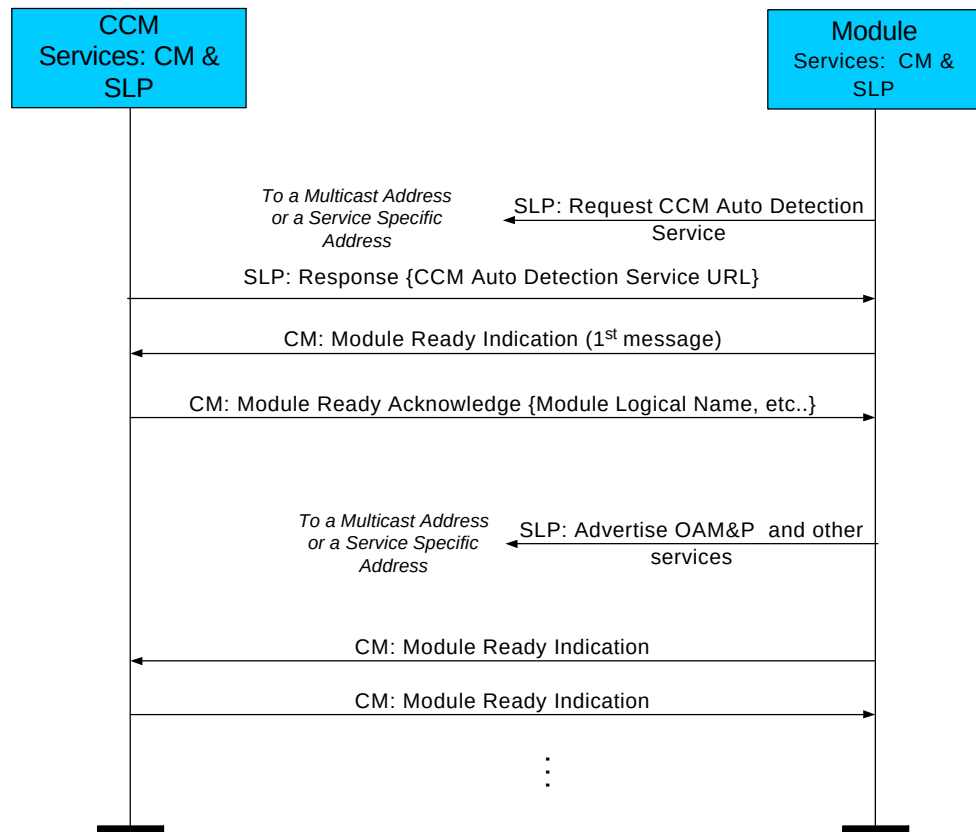


Figure 3.8-7 Module Start-up (except CCM)

3.8.3.3 Module Removal

This section illustrates the detection of ungraceful removal of a module/resource

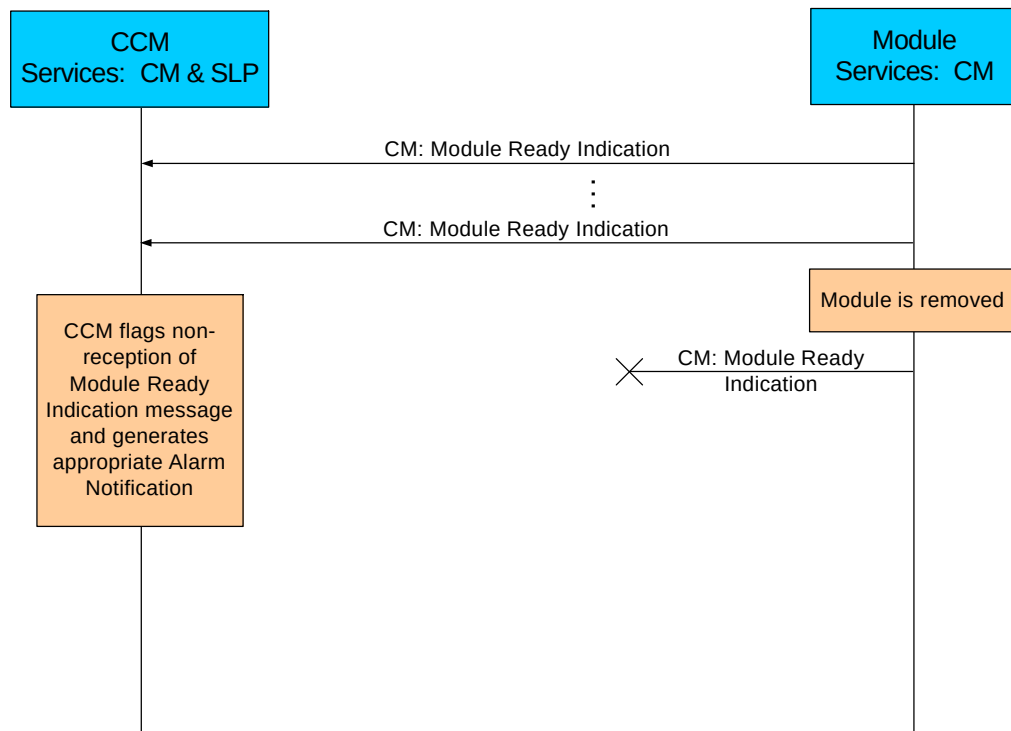


Figure 3.8-8 Module Start-up (except CCM)

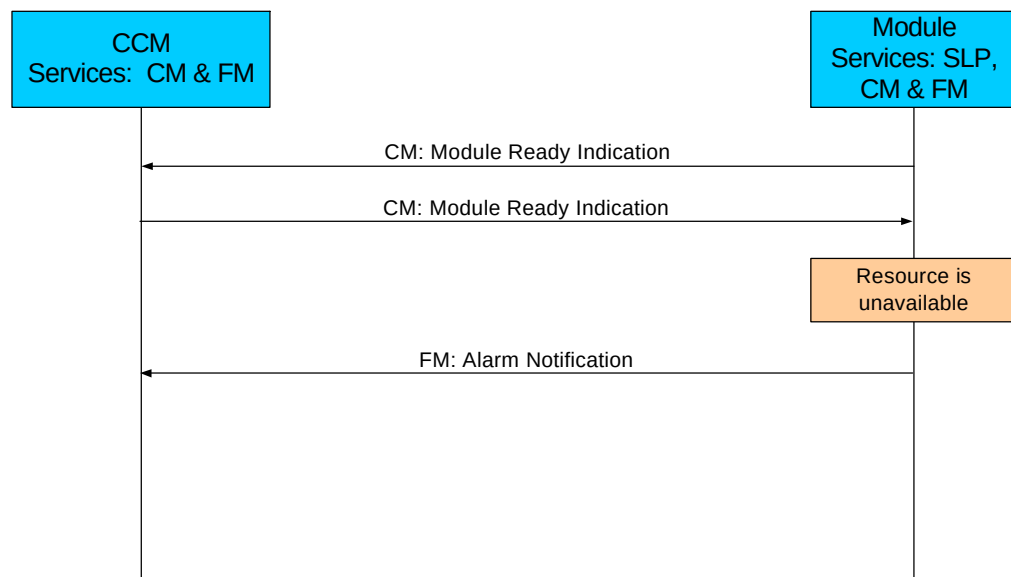


Figure 3.8-9 Module Start-up (except CCM)

3.9 Redundancy and Availability Criteria

The OBSAI architecture supports base stations with an availability of up to 99.999%. The actual availability of each BTS is determined to a large extent by the BTS integrator and the modules that are designed into the BTS. The BTS integrator determines the requirement for BTS availability on a case-by-case basis. Use of module redundancy to achieve high availability is not a requirement- it is optional. However, if redundancy is used it shall adhere these specifications.

3.9.1 N+1 Redundancy

To support a capability for an availability of 99.999%, the OBSAI BTS shall be configurable to support the following redundancy options:

- The Transport Block shall support 1:1 redundancy.
- The Control and Clock Block shall support 1:1 redundancy.
- The Baseband Block shall support 1:N redundancy for up to nine (9) modules.
- The RF Block shall support 1:N redundancy for up to 9 modules.

3.9.2 RP1 and RP2 Ethernet Redundancy Principles

3.9.2.1 Overview

Since the TM and the CCM are both critical to the operation of the base station, they have the most rigorous requirements during a switchover. During a switchover of one of these modules, no calls that are currently in progress may be dropped. Any calls in the process of being established may be blocked. If redundancy is required on the CCM and TM, then 1+1 redundancy shall be used.

A failure in any other module (BBM, RFM, GPM, or others) might only affect a portion of the active calls. The requirement for the number of calls that may be dropped during a switchover in one of these modules is not specified. If redundancy is required on the BBM, RFM, and GPM modules, then N+1 redundancy shall be used.

As specified in the OBSAI RP2 Specification, the RP1 and RP2 Ethernet network shall be implemented as a dual star with a TM at the center of each. Each node on the RP1 and RP2 Ethernet network shall contain two independent Ethernet interfaces, one for connection to each star. The TM modules shall be in an Active/Standby relationship and the inactive TM shall not switch any packets from one port to another.

3.9.2.2 1+1 Redundancy

Between the active and standby instances of 1+1 redundant modules, certain information must be synchronized to allow a rapid switchover in case of a failure. These specifications will not dictate what information gets synchronized, or how it gets synchronized. The CCM and the TM interfaces shall contain dedicated proprietary buses that can be used to facilitate this synchronization of information. The respective module interface specifications will contain electrical signaling specifications for these busses, but the message formats and content shall be left unspecified.

All notifications of switches in activity (to other modules on the Ethernet fabric) shall occur across RP1. No other out-of-band signals shall be used to indicate to other modules that a switch has occurred, or which module is currently active.

Any communication between modules of the same 1+1 redundant set that occurs during the fault detection, fault isolation, activity switch negotiation phases will be left unspecified. Only information that traverses RP1 between modules of different types, such as change in in activity notification from failover, will be specified.

Faults in 1+1 redundant modules cause one of two types of failures: node failures or fabric failures. Nodes are all modules, other than the TM, which use the RP1 and RP2 Ethernet fabric for communication. Fabric failures are caused by faults in the interconnection between modules, or faults in the TM itself.

3.9.2.3 Node Failures

1+1 redundant nodes share a common virtual IP address and a common virtual MAC address that all other modules in the OBSAI BTS use to communicate with the currently active module.

Each 1+1 redundant node shall also have a unique physical IP and physical MAC address that can be used to communicate directly with any individual node.

Other nodes on the network shall map the services performed by the 1+1 redundant nodes to the virtual IP address shared by them. Other nodes on the network shall map the shared virtual IP address with the shared MAC address.

Upon failure of an active module, its inactive mate shall adopt the commonly shared IP and MAC addresses and shall immediately issue a gratuitous ARP. Using the information contained in this gratuitous ARP, the TM shall adjust its port mappings to associate the newly active module to the shared MAC address. All other nodes in the

system will not need to take any further action to resume communication with the services provided by the 1+1 redundant set.

3.9.2.4 Fabric Failures

Upon failure of a TM or of the RP1 and RP2 Ethernet network interconnection between modules, the secondary TM shall become active and the secondary Ethernet star network shall become active. At that time, both the primary TM and the primary Ethernet star will become inactive. The TM modules themselves will negotiate this switch in activity. At the time of the TM switchover, a “break before make” connection should be made in the activation/deactivation of the Ethernet stars. All other modules (nodes) in the network shall be notified about this switchover. Further flows of notifications will ensure reach ability of any active module from any other active module over the active Ethernet star network.

3.10 Mechanical and Dimensioning Requirements

3.10.1 Overview

An OBSAI platform is made up of one or more linked shelves. These may be divided based on module type and other factors such as size, cooling, or cabling requirements. For example, a platform could have an “RF shelf” supporting large-pitch high-power RF modules, and a “baseband shelf” with all other modules at smaller pitch.

The basic mechanical elements of an OBSAI shelf are:

- Plug-in modules containing specific electronic functions along with front and rear interface connectors. Each module shall have a faceplate with two extractor handles, and rear backplane connectors. It may also include covers on component side 2 and/or component side 1. Both sealed and unsealed (open) modules shall be supported.
- Backplane providing connections between modules as well as power distribution and grounding.
- Subrack supporting the backplane as well as providing module alignment and support.
- Optional Rear Transition Module (RTM) allowing board-specific interface connection from the rear. The RTM, if used, shall have a faceplate and two extractor handles. It may also include covers on component side 2 and/or component side 1.

This section defines dimensioning for modules, card guides, and backplane connectors pertinent to the BB, TM, CCM & GPM and is subject to change. Dimensions and connectors for the RFM are defined separately in the RFM Specification.

3.10.1.1 Nomenclature

3.10.1.1.1 Orientation

The position and orientation of OBSAI modules is not defined by this document. However, for clarity within this document, the orientation of modules within a subrack will be assumed in a vertical orientation. When viewed from the front, component side 1 faces right, and component side 2 faces left. The top edge of the front board is closest to the power connector.

If the physical implementation of a shelf is oriented horizontally, when viewed from the front, the component side 1 faces upwards and component side 2 faces downwards.

3.10.1.1.2 Backplane Connectors

Module backplane connectors may vary based on module type or application. Figures in this section depict modules with two data connectors and two power connectors. They are illustrative only.

3.10.1.2 Sealed Modules

Sealed modules shall be fully enclosed. They require a gasketed interface to backplane assemblies and shall provide ingress protection to IP54. Additional backplane connectors and rear-transition modules (RTM) are possible, and are not defined by this document. Sealed modules shall fit within the defined sealed module envelope and shall follow the module guide restrictions.

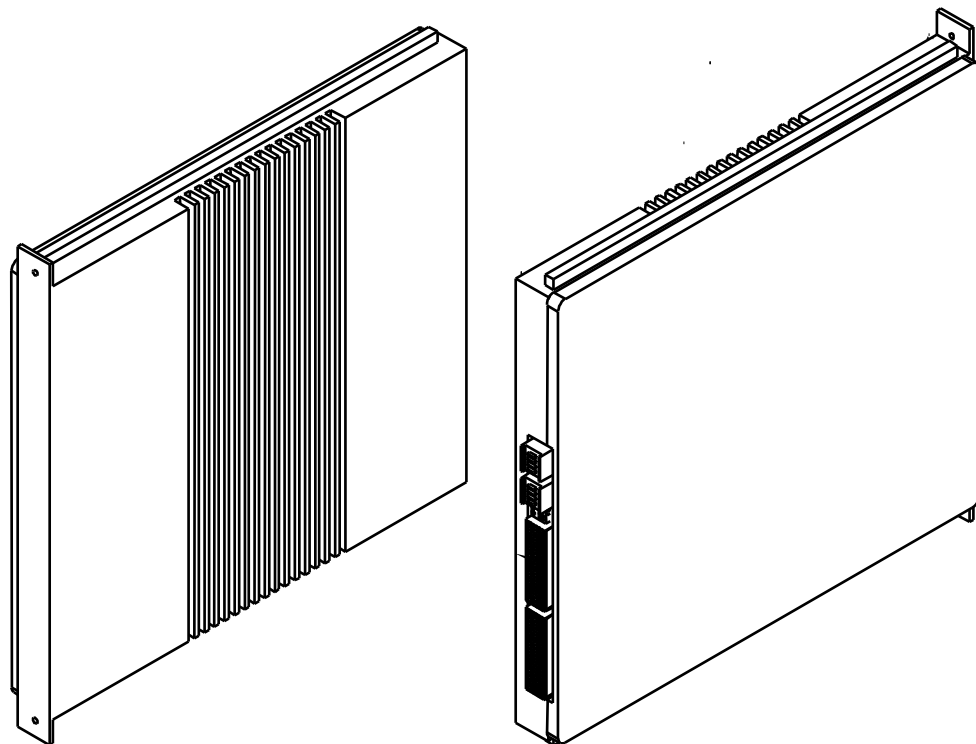
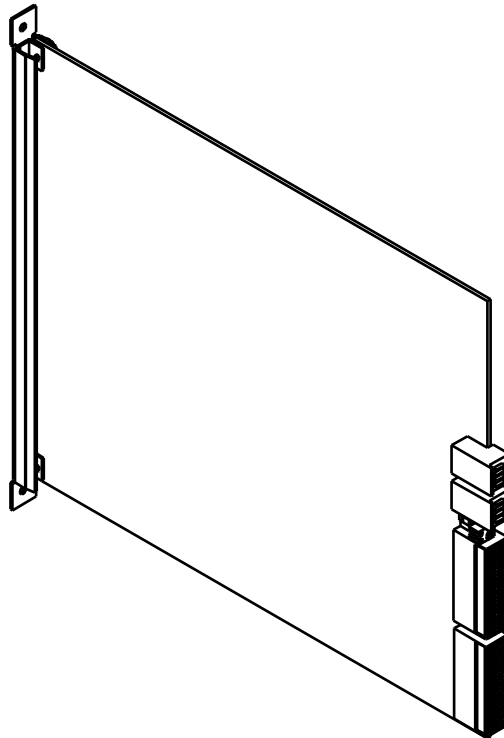


Figure 3.10-1 Sealed Module Perspective Views**3.10.1.3 Unsealed Modules**

There are no enclosure requirements for unsealed modules. Additional backplane connectors and rear-transition modules (RTM) are possible, and are not defined by this document. Unsealed modules shall fit within the defined module envelope and shall follow the module guide restrictions.

**Figure 3.10-2 Unsealed Module Perspective View****3.10.1.4 Module Reference Dimensions**

Sealed and Unsealed modules are designed for a nominal depth from the inside of the faceplate to the backplane surface of 295.6 mm. Both modules also have the same backplane connector positions, relative to the module centerline.

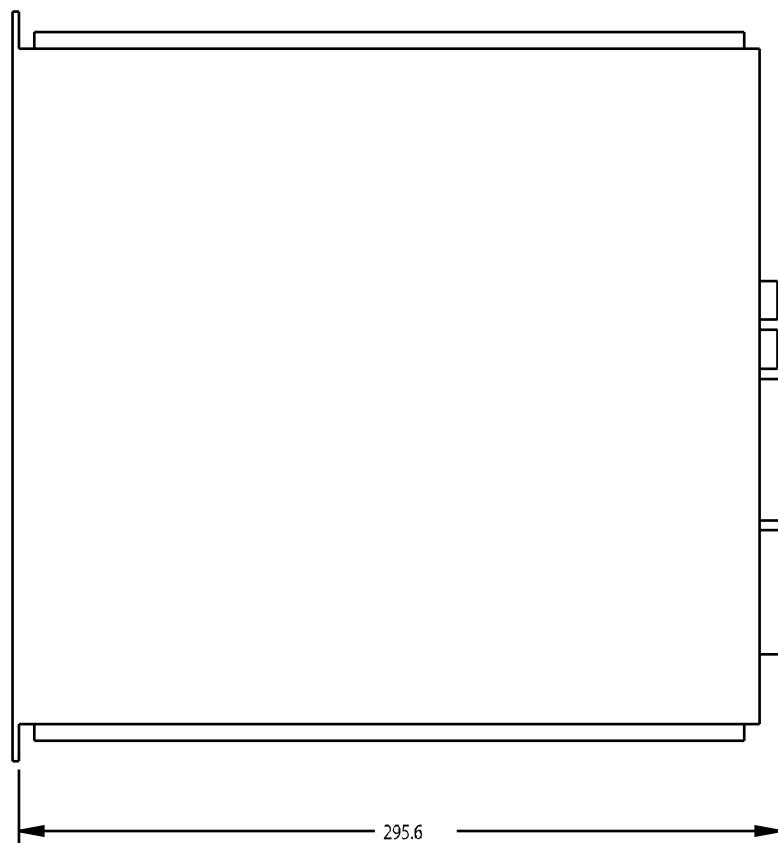


Figure 3.10-3 Module Depth Reference Dimension

3.10.2 Sealed Module Common Features (Excluding RF Modules)

The section applies to Control and Clock Block modules, Baseband Block modules, Transport Block modules and General Purpose Modules.

3.10.2.1 Dimensions

The nominal height of sealed modules shall be 275.00 mm including guide rail. The nominal depth from the inside of the faceplate to the backplane surface shall be 295.6 mm. The lower faceplate mounting position shall be the datum for locating the faceplate, connectors, and alignment pins. The chassis will provide two metallic module guides connected to shelf ground. This module guide may be a maximum of 3 mm in height. Sealed modules shall have 6.0 mm wide rails that are part of the enclosure, and fits into the guide.

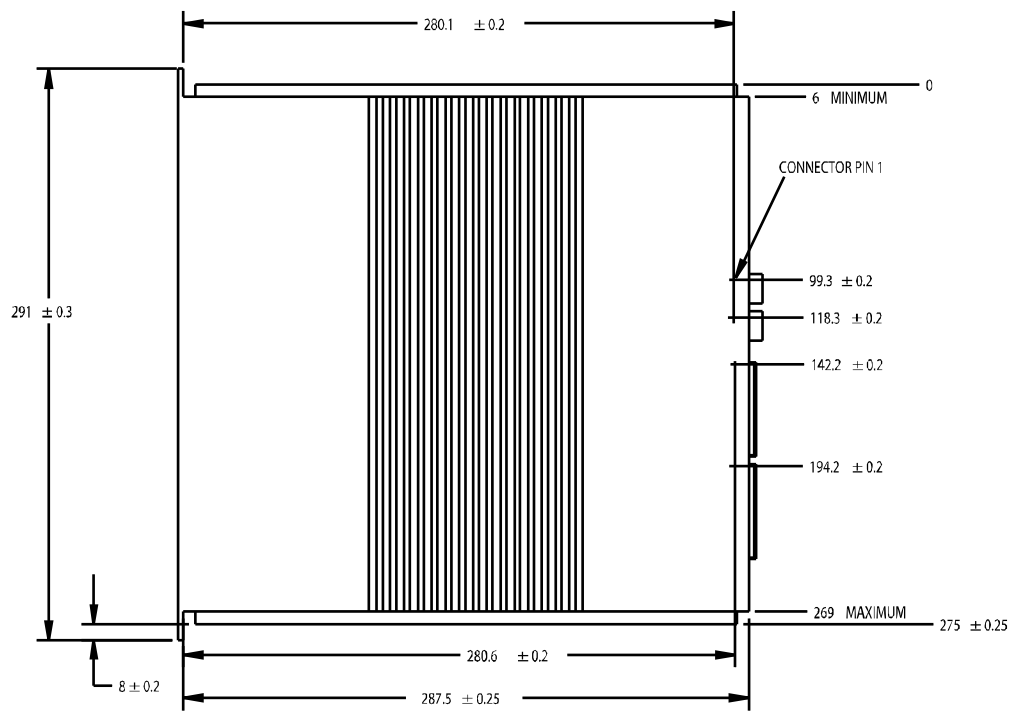


Figure 3.10-4 Sealed Module Dimensions, Side View

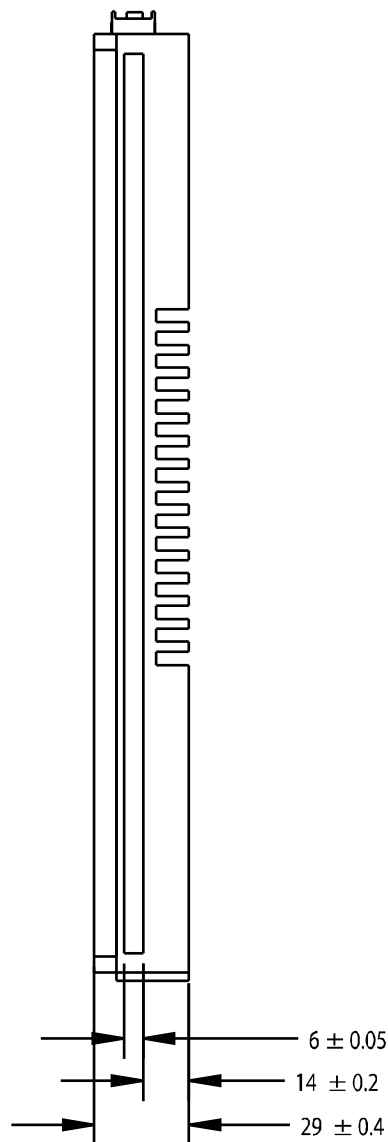


Figure 3.10-5 Sealed Module Dimensions, Top View

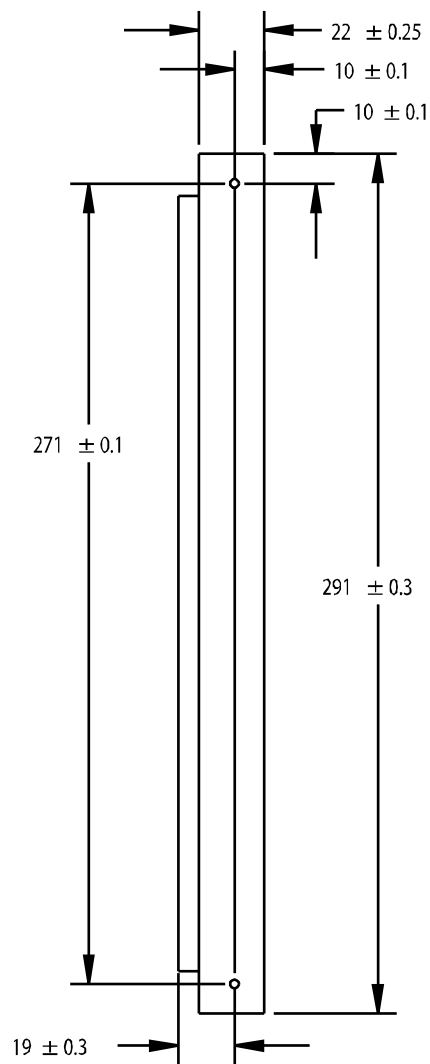


Figure 3.10-6 Sealed Module Dimensions, Front View

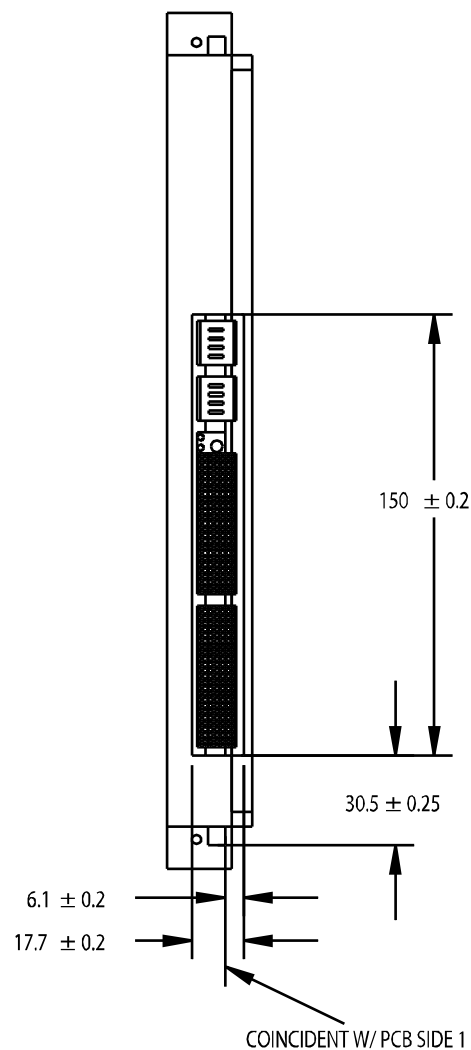


Figure 3.10-7 Sealed Module Dimensions, Rear View

3.10.2.2 PCB Thickness

The thickness of a PCB that is within the enclosure of a sealed module and is not defined.

3.10.2.3 Module Pitch

All sealed module dimensions are based on a module-to-module pitch of 30.48 mm (1.2 inch). Modules wider than this should be larger by even multiples of 15.24 mm.

3.10.2.4 Component Height Limits

Maximum component height in sealed modules is dependent on the method of module construction, and is not defined in this specification. All components shall remain within the specified envelope.

3.10.2.5 Faceplate

The front and optional RTM faceplates provide for module fastening, extraction and insertion, and can be a location for external interfaces. They shall include two extractor handles, and retention screws. The faceplate metal thickness shall be between 1.0 mm and 3.0 mm.

The front faceplate shall have two captive retentions screws. These screws shall be M3, with a #2 Phillips head.

3.10.2.6 Electrostatic Discharge (Sealed Module)

Each sealed module shall provide a conductive path from the guide rails to all exposed metallic surfaces of the enclosure. When a module is inserted into a Subrack, it contacts the card guide, which is connected to shelf ground. This provides a discharge path before the backplane connectors engage and when the front board comes to rest after being completely installed. The module logic ground shall have a direct, low-resistance connection to the module enclosure and faceplate (chassis ground).

3.10.2.7 Module Enclosure

Modules shall be covered and sealed as needed. Envelope limits for component sides 1 and 2 shall not be exceeded.

3.10.3 Unsealed Module Common Features

The section applies to Control and Clock Block modules, Baseband Block modules, Transport Block modules and General Purpose Modules.

3.10.3.1 Dimensions

The nominal PCB height for unsealed modules shall be 233.35 mm. The nominal depth from the inside of the faceplate to the backplane surface shall be 295.6 mm. The lower faceplate mounting position shall be the datum for locating the faceplate, connectors, and alignment pins. The chassis will provide two metallic module guides connected to shelf ground. This module guide may be a maximum of 3 mm in height. Unsealed modules shall have a 2 mm thick printed circuit board that fit into the guide. An additional clearance of 1.5 mm is defined on unsealed modules between any traces and any metallic guide rail. This component keep-out area also contains circuitry to provide electrostatic discharge (ESD) protection.

The component keepout areas located on the top and bottom edges of the PCB shall be 4.5mm to allow for the guides and clearance requirements.

Note: The unsealed module dimensions and connector positions allow the same PCB to be used as part of a sealed module.

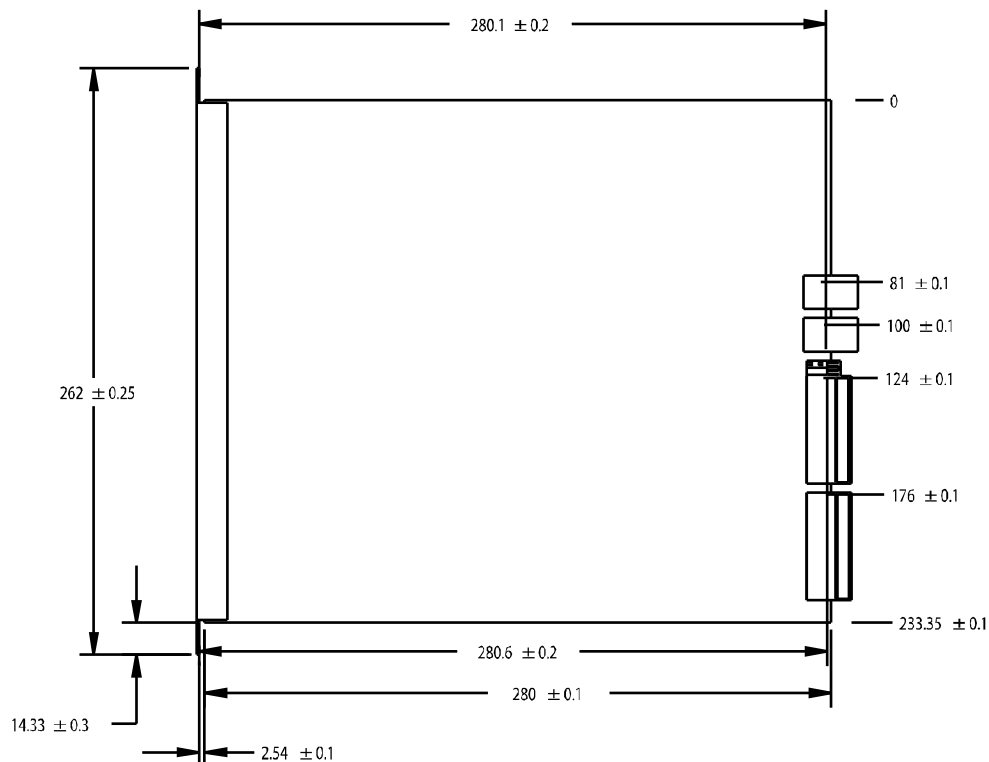


Figure 3.10-8 Unsealed Module Dimensions, Side View

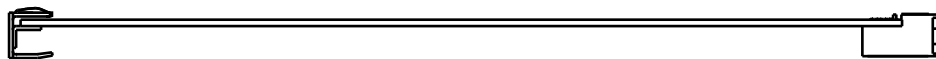


Figure 3.10-9 Unsealed Module Dimensions, Top View

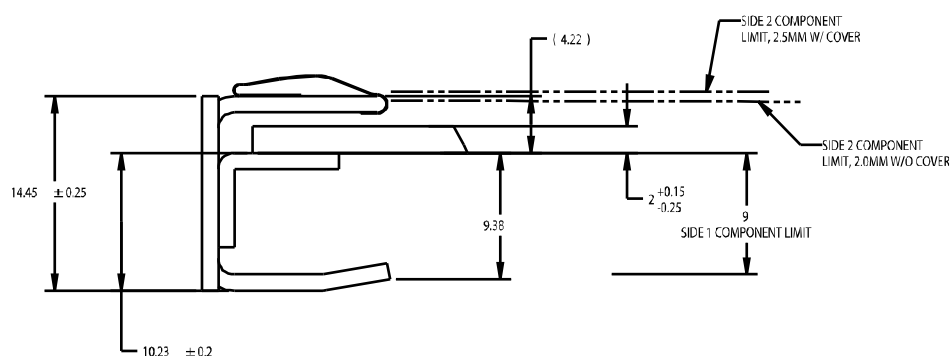


Figure 3.10-10 Unsealed Module Dimensions, Top Detail

3.10.3.2 PCB Thickness

The PCB thickness of unsealed modules, or exposed PCB edges, shall be 2.0 +0.15/-0.25mm.

3.10.3.3 Module Pitch

All unsealed module dimensions are based on a module-to-module pitch of 15.24 mm (0.6 inch). Modules wider than this should be larger by even multiples of 15.24 mm.

3.10.3.4 Component Height Limits

Component bodies in unsealed modules shall not extend beyond the defined module envelope. These limits provide for electrical and mechanical clearance between adjacent modules and shelf components.

Side 2 component height will be dependent on the space required for an optional cover (including insulation requirements for a conductive cover), and will take into account PCB warp and bow.

3.10.3.5 Faceplate

The front and optional RTM faceplates provide for module fastening, extraction and insertion, and can be a location for external I/O interfaces. They shall include a component side 2 EMC gasket, two extractor handles, and retention screws. The faceplate metal thickness shall be between 1.0 mm and 3.0 mm.

The front faceplate shall have two captive retentions screws. These screws shall be M3, with a #2 Phillips head.



Figure 3.10-11 Unsealed Module Dimensions, Front View

3.10.3.6 Electrostatic Discharge (Unsealed Module)

Each unsealed module shall provide a two-segment discharge strip located on Component Side 1 along the bottom edge of the PCB. A discharge strip shall not be used along the top edge of the PCB. This strip shall withstand 250 insertion/extraction cycles and be dimensioned as shown. When a front board is inserted into a subrack, it contacts to the ESD clip, which is connected to chassis ground. The ESD strip is divided into two segments to achieve a "controlled discharge." The ESD strip provides a discharge path before the backplane connectors engage and when the front board comes to rest after being completely installed. Segment 1 shall be connected to the face plate through a 10 MOhm $\pm$ 20% resistance to discharge any built up static charge from the front board or user. The resistor is used to limit the amount of discharge current. The 10 Mohm discharge resistor shall have a minimum voltage rating of 2 kV, and be rated for at least ¼ Watt dissipation. Segment 2 provides a discharge path from the face plate to shelf ground when the entire system is assembled. It shall make a

gas-tight connection directly to the face plate. The module logic ground shall have a direct, low-resistance connection to the module faceplate (chassis ground).

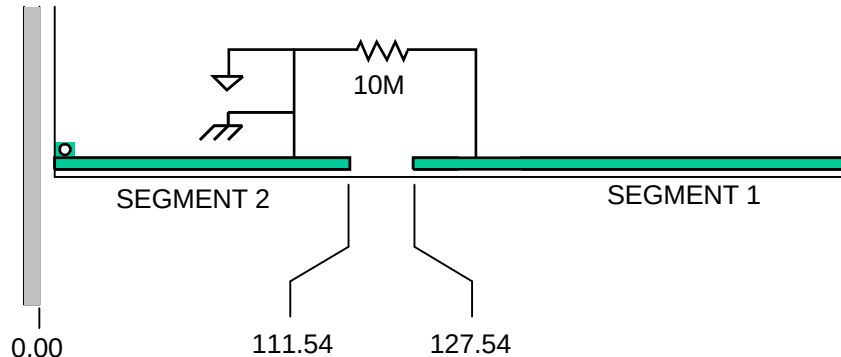


Figure 3.10-12 ESD Strip Schematic and Dimensions

3.10.3.7 Optional Module Cover

Modules may be covered or sealed as needed. Envelope limits for component sides 1 and 2 shall not be exceeded.

3.10.4 RF Module Common Features

RF module common features are to be provided in a later version of this document.

3.10.5 Rear Transition Module

Optional rear transition modules (RTM) allow vendor-specific connection to a front module from the rear of the shelf. Each RTM is on the same plane as the associated front module. It must follow the same component side 1 and 2 envelope limits as the front module. The function and connections of the RTM are vendor defined.

3.11 Backplane

OBSAI specifications focus on modules and their interfaces. The actual BTS design is beyond the scope of OBSAI. For the sake of clarity, however, guidelines are given where appropriate. In that sense, OBSAI does not specify a BTS backplane as such. Backplane interface specifications (electrical characteristics and pin assignments) are part of respective Module Interface Specifications.

3.11.1 Data Connections

This subsection defines categories of electrical signals at the backplane interface (except power interface):

- **Common Signals.** Common Signals are common to all modules and shall be supported. Common Signals are assigned to fixed pin positions at the Data Connector(s) which are present at all modules. Examples are:
 - Shelf ID
 - Slot ID
 - RP1 System Clock Input (redundant)
 - RP1/2 Ethernet Port (redundant)
 - Non-connect (e.g. - Debug Port(s), Production Test Port(s), Programming Port(s))
- **Module Type Specific Signals.** Module Type Specific Signals are common to a certain module type (TM, CCM, BBM, RFM) and shall be supported. Module Type Specific Signals shall be assigned to fixed pin positions at the Data Connector(s). Examples are:
 - Transport Module
- Ethernet Fabric Ports (fan-out)
- Reference Clock Output
 - Control and Clock Module
- System Clock Outputs (fan-out)
- Reference Clock Inputs
- **Module Type Unspecified Signals.** Module Type Unspecified Signals are optional. Their functional and electrical characteristics are not specified. If present, Module Type Unspecified Signals shall be assigned to a range of pin positions at the Data Connector(s). The range of pin positions shall be fixed for a certain module type, but may differ between module types. Examples are:
 - Redundancy Control Port(s)
 - Link(s) to General Purpose Module(s)
- **Unspecified Signals.** Unspecified Signals are optional. Their functional and electrical characteristics are not specified. If present, Unspecified Signals shall be assigned to one or more unspecified connectors. Examples are:
 - Link(s) to General Purpose Module(s)
 - Support for RTM

Refer to Appendices B and C for the data connector specifications.

3.11.2 Power Connections

A single power bus is connected to the modules through a four-pin power connector P1, and an optional P2.

3.11.2.1 Connector Mating Sequence And Short Pins

The plug-in modules and backplane shall provide a sequenced mating such that pins will connect in three groups. There is no mating sequence requirement within a group. Upon module insertion, the mating sequence shall be:

Enclosure contact with chassis ground at the card guides.

- Logic/chassis ground. This is a long pin within the power connector.
- Power supply signals and digital signals. These are medium length pins.
- Power enable (PWR_ENA). This is a short pin within the power connector tied (on the backplane) to the PWR_NEG pin.

3.11.2.2 Power Connector Types

Power connector P1 shall be equipped with an OBSAI sequenced connector. This connector has three pin lengths, and provides the mating sequence described in the previous section.

Table 3.11-1 Sequenced Connector Pin Characteristics For P1

P1	Pin Length	Signal
1	Medium	PWR_POS
2	Short	PWR_ENA
3	Medium	PWR_NEG
4	Long	GND

Power connector P2, if installed, can be equipped with an OBSAI sequenced or non-sequenced connector. If a sequenced connector is installed, only the two medium length pins can be used to deliver power to the module.

Table 3.11-2 Sequenced Connector Pin Characteristics For P2

P2	Pin Length	Signal
1	Medium	PWR_POS
2	Short	NC
3	Medium	PWR_NEG
4	Long	NC

If a non-sequenced connector is installed, all four medium length pins can be used to deliver power to the module.

Table 3.11-3 Non-Sequenced Connector Pin Characteristics For P2

P2	Pin Length	Signal
1	Medium	PWR_POS
2	Medium	PWR_POS
3	Medium	PWR_NEG
4	Medium	PWR_NEG

Refer to Appendices D and E for the power connector specifications.

3.12 Module Power Interface

The shelf backplane is responsible for delivering power to all of the operating modules through their respective power connector(s). Modules and backplanes shall provide DC isolation between the power domain and the shelf logic-common and chassis domains. All conduits of the power domain shall observe the mutual creepage clearance distances between the conduits and logic-common and associated signals.

3.12.1 Module Supply Voltage

A module shall operate within either –48 VDC nominal or +24 VDC nominal (or both) power as defined below.

3.12.1.1 Nominal –48 Volt Requirement

The table below lists the requirements for -48 VDC supply power:

Table 3.12-1 -48 VDC Supply Voltage Requirements

Nominal operating voltage	-48 VDC
Maximum input voltage	-58 VDC
Maximum operating voltage	-58 VDC
Minimum operating voltage	-39.5 VDC
Minimum input voltage	0 VDC

3.12.1.2 Nominal +24 Volt Requirement

The table below lists the requirements for +24 VDC supply power:

Table 3.12-2 +24 VDC Supply Voltage Requirements

Nominal operating voltage	+24 VDC
Maximum input voltage	+57 VDC
Maximum operating voltage	+32 VDC
Minimum operating voltage	+19.2 VDC
Minimum input voltage	0 VDC

3.12.2 Module Supply Protection

Modules shall use circuit interruptors such as fuses in series with the power bus to ensure that the current on individual power connector pins does not exceed 23 amps (derated to 21 amps in the case of all four pins carrying current). Current limiter values should be appropriate for the maximum operational current of the module.

Modules shall include protection from damage caused by a supply voltage polarity reversal.

4 Glossary

4.1 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ABBREVIATION	DESIGNATION
AAL	ATM Adaptation Layer
AAL2	ATM Adaptation Layer type 2
AAL5	ATM Adaptation Layer type 5
ADDs	Application Data Delivery Service
AMPS	Advanced Mobile Phone System
ANSI	American National Standards Institute
ARFCN	Absolute Radio Frequency Channel Number
ATM	Asynchronous Transfer Mode
BS	Base Station
BSAP	Base Station Application Part
BSC	Base Station Controller
BSMAP	Base Station Management Application Part
BSS	Base Station Subsystem
BTS	Base Transceiver System
CANID	Current Access Network Identifiers
CBC	Cell Broadcast Centre
CBS	Cell Broadcast Service
CC	Call Control
CDG	CDMA Development Group
CDMA	Code Division Multiple Access
CID	Connection Identifier (used with reference to AAL2)
CM	Connection Management
CN	Core Network
CPCH	Common Packet Channel
CRNC	Controlling Radio Network Controller
DCCH	Dedicated Control Channel

ABBREVIATION	DESIGNATION
DCH	Dedicated Channel
DL	Downlink
DS	Direct Spread
DS0	Digital Signal Level 0
DS1	Digital Signal Level 1
DS-41	An operational mode in which the BS and MS operate with the direct spread (DS) radio layers of the UMTS system defined by 3GPP, and the upper layers defined in IS-2000 that conform to and interoperate with ANSI-41 based networks.
DTX	Discontinuous Transmission
EDGE	Enhanced Data rates for Global Evolution
EIA	Electronics Industry Association
EIB	Erase Indicator Bit
ESN	Electronic Serial Number
EVRC	Enhanced Variable Rate Codec
FACH	Forward Access Channel
FCH	Fundamental Channel
FER	Frame Error Rate
FFS	For Further Study
FQI	Frame Quality Indicator
FSN	Frame Sequence Number
GERAN	GSM EDGE Radio Access Network
GSM	Global System for Mobile Communications
GTP	GPRS Tunneling Protocol
IEI	Information Element Identifier
IETF	Internet Engineering Task Force
IMSI	International Mobile Subscriber Identity
IOS	Interoperability Specification
IP	Internet Protocol
IPv4	Internet Protocol, version 4
IPv6	Internet Protocol, version 6
ISDN	Integrated Services Digital Network
ISLP	Intersystem Link Protocol
ITU	International Telecommunications Union
IWF	Interworking Function
kb	kilo bits
LAC	Location Area Code

ABBREVIATION	DESIGNATION
LI	Length Indicator
LSB	Least Significant Bit
MAC	Medium Access Control
MIN	Mobile Identification Number
MIP	Mobile IP
MM	Mobility Management
MS	Mobile Station
MSB	Most Significant Bit
MSC	Mobile Switching Center
N-AMPS	Narrow band AMPS
NAS	Non Access Stratum
NBAP	Node B Application Part
NEBS	Network Equipment-Building System
NID	Network Identification
NNSF	NAS Node Selection Function
OAM&P	Operations, Administration, Maintenance, and Provisioning
OTD	Orthogonal Transmit Diversity
PCF	Packet Control Function
PCH	Paging Channel
PDE	Position Determining Entity
PDSN	Packet Data Serving Node
PIN	Personal Identification Number
PLD	Position Location Data
PLMN	Public Land Mobile Network
PMC	Packet Mode Channel
PN	Pilot Number
PPP	Point to Point Protocol
PSTN	Public Switched Telephone Network
QCELP	Q Code Excited Linear Prediction
QOF	Quasi Orthogonal Function
QoS	Quality of Service
RAB	Radio Access Bearer
RACH	Random Access Channel
RANAP	Radio Access Network Application Part
RANDC	Random Confirmation
RANDSSD	Random SSD

ABBREVIATION	DESIGNATION
RC	Radio Configuration
RF	Radio Frequency
RFC	Remote Feature Control
RLP	Radio Link Protocol
RNC	Radio Network Controller
RNL	Radio Network Layer
RNS	Radio Network Subsystem
SCH	Supplemental Channel
SDB	Short Data Burst
SDU	Selection/Distribution Unit
SID	System Identification
SLR	Source Local Reference
SME	Signaling Message Encryption
SOCI	Service Option Connection Identifier
SRNC	Serving Radio Network Controller
SRNC-ID	Source Radio Network Controller Identifier
SSD	Shared Secret Data
STP	Signal Transfer Point
TCP	Transmission Control Protocol
TIA	Telecommunications Industry Association
TNL	Transport Network Layer
TSB	Telecommunications Systems Bulletin
TTI	Transmission Time Interval
UDI	Unrestricted Digital Information
UDP	User Datagram Protocol
UE	User Equipment
UL	Underwriters Laboratory
UMTS	Universal Mobile Telecommunication System
USIM	UMTS Subscriber Identity Module
UTRAN	Universal Terrestrial Radio Access Network

4.2 Definition of Terms

For the purposes of the present document, the following terms and definitions apply:

Abis: designation of the interface between the Base Transceiver System (BTS) and the Base Station Controller (BSC) for IS-2000. TIA/EIA-828-A provides the specifications for this interface.

ALCAP: generic name in 3GPP systems for the transport signaling protocols used to set-up and tear-down transport bearers

Cell: Radio Network object that can be uniquely identified by a User Equipment from a (cell) identification that is broadcasted over a geographical area from one radio node.

Controlling RNC: role an RNC can take with respect to a specific set of Node B's. There is only one Controlling RNC for any Node B. The Controlling RNC has the overall control of the logical resources of its node B's.

Globally unique MAC: A MAC address that has 24 first bits (Company_ID) assigned from IEEE. Last 24 bits shall be unique and handled within Company.

Network Interface: interface between the RNC and the Node B for 3GPP (e.g. Iub).

Locally unique MAC: A MAC address that has different scope than in Global IEEE addresses. The "u" bit is indicating local scope.

Logical MAC: A MAC address that is shared between two or more physical interfaces. Is usable e.g. in redundancy purposes. Called also "shared dynamic" in this document.

Logical Model: Logical Model defines an abstract view of a network or network element by means of information objects representing network element, aggregations of network elements, the topological relationship between the elements, endpoints of connections (termination points), and transport entities (such as connections) that transport information between two or more termination points

The information objects defined in the Logical Model are used, among others, by connection management functions. In this way, a physical implementation independent management is achieved.

Node B: logical node in the OBSAI System responsible for radio transmission / reception in one or more cells to/from the UE. The logical node terminates the network interface (Iub) towards the RNC.

Physical MAC: A MAC address that is assigned to an physical interface.

Radio Link: "radio link" is a logical association between a single User Equipment and a single UTRAN access point. Its physical realization comprises one or more radio bearer transmissions.

Radio Link Set: set of one or more Radio Links that has a common generation of Transmit Power Control (TPC) commands in the DL

Radio Resources: resources that constitute the radio interface in OBSAI, e.g. frequencies, scrambling codes, spreading factors, power for common and dedicated channels

Radio Node B Application Part: Radio Network Signaling over the network interface (Iub)

Radio Network Controller: logical node in the RNS in charge of controlling the use and the integrity of the radio resources

Radio Network Subsystem: RNS can be either a full UTRAN or only a part of a UTRAN. An RNS offers the allocation and release of specific radio resources to establish means of connection in between an UE and the UTRAN. A Radio Network Subsystem contains one RNC and is responsible for the resources and transmission/reception in a set of cells.

Universal Terrestrial Radio Access Network: UTRAN is a conceptual term identifying that part of the network which consists of RNCs and Node Bs between Iu and Uu.

Unique MAC: A MAC address needs to be unique within a BTS LAN.

User Equipment: Mobile Equipment with one or several UMTS Subscriber Identity Module(s). A device allowing a user access to network services via the Uu interface.

UTRAN Access Point: conceptual point within the UTRAN performing radio transmission and reception. A UTRAN access point is associated with one specific cell, i.e. there exists one UTRAN access point for each cell. It is the UTRAN-side end point of a radio link.

Uu: Radio interface between UTRAN and the User Equipment

5 References

5.1 American National Standards Institute (ANSI)

ANSI T1.102 - 1993, Digital Hierarchy - Electrical Interfaces.

ANSI T1.403 - 1995 Network to Customer Installation - DS1 Metallic Interface.

5.2 TIA/EIA

TIA/EIA/IS-2000.1-A, Introduction to cdma2000 Standards for Spread Spectrum Systems, March, 2000.

TIA/EIA/IS-2000.2-A, Physical Layer Standard for cdma2000 Spread Spectrum Systems, March, 2000.

TIA/EIA/IS-2000.3-A, Medium Access Control (MAC) Standard for cdma2000 Spread Spectrum Systems, March, 2000.

TIA/EIA/IS-2000.4-A, Signaling Link Access Control (LAC) Standard for cdma2000 Spread Spectrum Systems, March, 2000.

TIA/EIA/IS-2000.5-A, Upper Layer (Layer 3) Signaling Standard for cdma2000 Spread Spectrum Systems, March, 2000.

TIA/EIA/IS-2000.6-A, Analog Signaling Standard for cdma2000 Spread Spectrum Systems, March, 2000.

TIA/EIA-95-B, Mobile Station-Base Station Compatibility Standard for Wideband Spread Spectrum Cellular Systems, February, 1999.

TIA/EIA-41-D, Cellular Radio Telecommunications Intersystem Operations, February 1996.

TIA/EIA-97-C, Recommended Minimum Performance Standard for Base Stations Supporting Dual-Mode Spread Spectrum Cellular Mobile Stations, September, 1999.

TIA/EIA/IS-733-1, High Rate Speech Service Option 17 for Wideband Spread Spectrum Communications Systems Addendum 1, September 1999

TIA/EIA IS-828, BTS-BSC Inter-operability (Abis Interface), version 2, July 2001.

5.3 Telcordia

Telcordia Technologies Generic Requirements GR-63-CORE: Network Equipment-Building System (NEBS) Requirements: Physical Protection, Issue 1, October 1995.

Telcordia Technologies Generic Requirements GR-487-CORE: Generic Requirements for Electronic Equipment Cabinets, Issue 2, March 2000.

Telcordia Technologies Generic Requirements GR-1089-CORE: Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Communications Equipment, Issue 2, December 1997, with Rev 1, February 1999.

5.4 Underwriters Laboratory (UL)

UL 60950 (formerly UL1950), third edition: Standard for Safety for Information Technology Equipment, 1995.

5.5 Government

Code of Federal Regulations Title 47: Telecommunications, Revised October 1, 1999.

5.6 ITU

ITU Recommendation G.703 Physical/Electrical Characteristics of Hierarchical Digital Interfaces.

5.7 IEEE

[IEEE Std 802.3] IEEE 802.3, 2000 Edition (ISO/IEC 8802-3: 2000 (E)), IEEE Standard for Information technology--Telecommunications and information exchange between systems--Local and metropolitan area networks--Specific requirements--Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

[IEEE Std 802.16d] IEEE802.16-2004: Air Interface for Fixed Broadband Wireless Access Systems

[IEEE Std 802.16e] IEEE P802.16e/D12, "Draft IEEE Standard for Local and metropolitan area networks. Part 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems Amendment for

Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands," October 2005

5.8 IETF

RFC 768: "User Datagram Protocol", (8/1980)

RFC 791 (1981): "Internet Protocol".

[RFC2131] Dynamic Host Configuration Protocol

[RFC2132] DHCP options and BOOTP Vendor Extensions

RFC 2460: "Internet Protocol, Version 6 (Ipv6) Specification".

RFC 2474: "Definition of the Differentiated Services Field (DS Field) in the IPv4 and IPv6 Headers " December 1998

RFC 2570, Introduction to SNMPv3 (April 1999)

RFC 2571, An Architecture for Describing SNMP Management Frameworks (May 1999)

RFC 2572, Message Processing and Dispatching (May1999)

RFC 2573, SNMP Applications (April 1999)

RFC 2574, User-based Security Model (April 1999)

RFC 2575, View-based Access Control Model (April 1999)

RFC 2576, (PROPOSED STANDARD), Coexistence between SNMP Version 1, Version 2, and Version 3 (March 2000)

[RFC2608] Service Location Protocol, version 2

[RFC2609] Service Templates and Service: Schemes

[RFC2614] An API for service location

[RFC3111] Service Location Protocol Modifications for IPv6

[RFC3513] IPv6 Addressing Architecture

5.9 3rd Generation Partnership Project (3GPP)

3GPP TR 25.990: "Vocabulary".

3GPP TS 05.01: "GERAN, Physical Layer on the Radio Path, General Description"

3GPP TS 05.02: "GSM/EDGE, Radio Access Network, Multiplexing and Multiple Access on the Radio Path"

3GPP TS 05.03" "GERAN, Channel Coding"

3GPP TS 23.003: "Numbering, Addressing and Identification".

3GPP TS 23.101: "General UMTS Architecture".

3GPP TS 23.110: "UMTS Access Stratum Services and Functions".

3GPP TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD)".

3GPP TS 25.212: "Radio Access Network, Multiplexing and Channel Coding (FDD)"

3GPP TS 25.213: "Radio Access Network, Spreading and Modulation"

3GPP TS 25.331: "RRC Protocol Specification".

3GPP TS 25.402: "Synchronisation in UTRAN, Stage 2".

3GPP TS 25.414: "UTRAN Iu Interface Data Transport & Transport Signalling".

3GPP TS 25.424: "UTRAN Iur Interface Data Transport & Transport Signaling for Common Transport Channel Data Streams".

3GPP TS 25.426: "UTRAN Iur and Iub Interface Data Transport & Transport Signaling for DCH Data Streams".

3GPP TS 25.434: "UTRAN Iub Interface Data Transport & Transport Signaling for Common Transport Channel Data Streams".

3GPP TS 23.236: "Intra-domain connection of Radio Access Network (RAN) nodes to multiple Core Network (CN) nodes".

3GPP TS 25.442: "UTRAN Implementation Specific O&M Transport".

3GPP TR 43.930: "Iur-g interface; Stage 2".

5.10 Other

"Information technology – Open Systems Interconnection – Network service definition", X.213, ISO/IEC 8348.

"Information technology – Open Systems Interconnection – Network service definition Amendment 1: Addition of the Internet protocol address format identifier", X.213/Amd.1, ISO/IEC 8348.

R.E. Blahut, Theory and Practice of Error Control codes, Addison-Wesley, Reading, 1983.

S. Lin and D.J. Costello, Jr., Error Control Coding: Fundamentals and Applications, Prentice-Hall, Englewood Cliffs, N.J., 1983.

S. Verdu, "Optimum Sequence Detection of Asynchronous Multiple-Access Communications," Abs. IEEE Int. Symp. Information Theory, St. Jovite, Canada, p. 80, Sept. 1983.

J.G. Proakis, Digital Communications, McGraw-Hill, New York, 1995.

[WiMAX Profiles] WiMAX Forum™ Regulatory Working Group, *Initial Certification Profiles and the European regulatory framework – September, 2004*

Appendix A. Design Recommendations

Appendix A provides recommended minimum or essential requirements that are not controlled by performance characteristics, interface requirements, or specified referenced documents. They include appropriate design standards, requirements governing the use or selection of materials, parts and processes, interchangeability requirements, environmental conditions, electromagnetic compatibility, reliability, reparability, and safety requirements.

A.1. Environmental Conditions

A.1.1. Operating Temperature And Humidity

The BTS should not sustain any damage or deterioration of functional performance during its operating life when operated in an ambient temperature, external to the cabinet housing, of -40°C with no solar load to +52°C with maximum solar load of 720 W/m² and maximum power dissipation and a relative humidity of 5% to 95%. With ambient temperatures above 84°F, the relative humidity may be limited to that corresponding to a specific humidity of 0.024 pounds of water per pound of dry air.

A.1.2. Storage Temperature And Humidity

The OBSAI BTS should meet all functional criteria after being stored in ambient temperatures of -40°C to +70°C with a relative humidity of 5% to 95%. With ambient temperatures above 84°F, the relative humidity may be limited to that corresponding to a specific humidity of 0.024 pounds of water per pound of dry air.

A.1.3. Altitude Requirements

The OBSAI BTS should meet all functional criteria after being installed at altitudes from 200 feet below mean sea level to 13,000 feet above mean sea level. For high altitude operation, the temperature requirement is derated at 1°C per 1000 feet above sea level in accordance with Telcordia guidelines.

A.2. Design and Construction Criteria

This section provides the minimum or essential requirements that are not controlled by performance characteristics, interface requirements, or specified referenced documents. They should include appropriate design standards, requirements governing the use or selection of materials, parts and processes, interchangeability requirements, environmental conditions, electromagnetic compatibility, reliability, reparability, and safety requirements.

A.2.1. Maintainability Criteria

The BTS should allow field access, such as a door, for the removal of a faulty module or CCA. Module insertion or extraction while power is on should not damage any module. Insertion or extraction of a module should not disrupt operation of the BTS.

A.2.1.1. Field Upgrades

The BTS should support the following hardware upgrades in the field.

- Insert or remove baseband modules
- Increase from 1 to TBD carriers
- Insert or remove RF modules
- Insert or remove backhaul interface(s)

A.2.1.2. Mean Time To Repair (MTTR)

Mean-time-to-repair (MTTR) should apply to replacement of a failed field replaceable unit (FRU) and should include the following operations by field personnel:

- Time for fault detection and isolation to one or more FRUs
- Disassembly of mounting fixtures (if any)
- Interchange of the failed FRU
- Reassembly of mounting fixtures
- Alignment and checkout of the replaced FRU

At the field (on-site) level, the BTS should have a MTTR of no greater than thirty minutes and a Maximum Time To Repair (MTTRMAX) no greater than sixty minutes at the 95th percentile. MTTR does not include the time required to travel to the BTS site.

A.2.1.3. Maintenance Access

Maintenance procedures must ensure that access to the equipment during a maintenance action should not cause BTS equipment to overheat and should not allow excessive moisture and dirt intrusion.

Maintenance procedures must ensure that access to the equipment during a maintenance action should not cause OBSAI BTS modules to overheat and should not allow excessive moisture and dirt intrusion.

A.2.2. Safety and Fail-safe Operation

The BTS and the internal modules should comply with the requirements of Underwriters Laboratory (UL), 60950, 3rd Edition.

Appendix B. Specification for HARD-Metric Vertical Male Connector

B.1. Scope

Specification for:	Hard metric 2mm, straight male, 144 pin. electrical connector with or without guide and coding block and with or without endwall.
Other parts:	Guide and coding pin.

B.2. General Description

Type:	Data
Connection method:	Press-fit (PCB thickness $\geq 1,4$ mm)
Shape:	Straight male
Number of poles:	6 x 24

Male connector will be loaded with hm 2mm standard pins acc. to IEC 61076-4-101. Pin type(s) used for this connector are described in chapter 9.4.

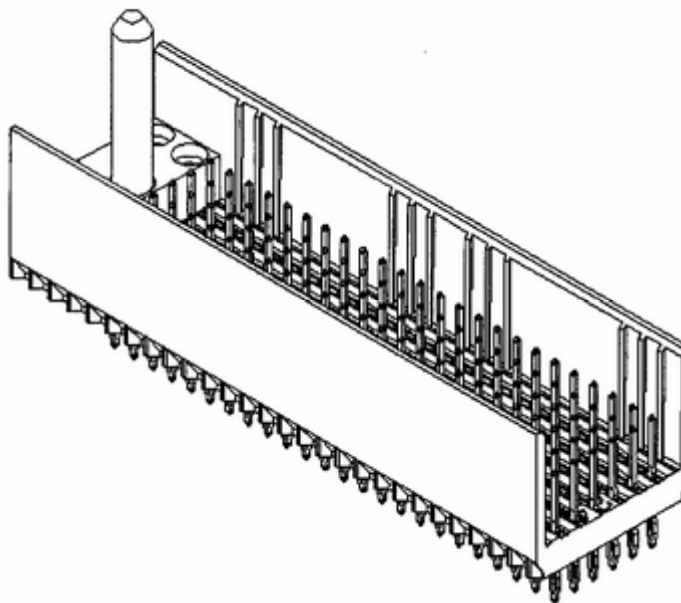


Figure B-1 2mm Straight Male Connector 144 Pin with Guide and Coding Block

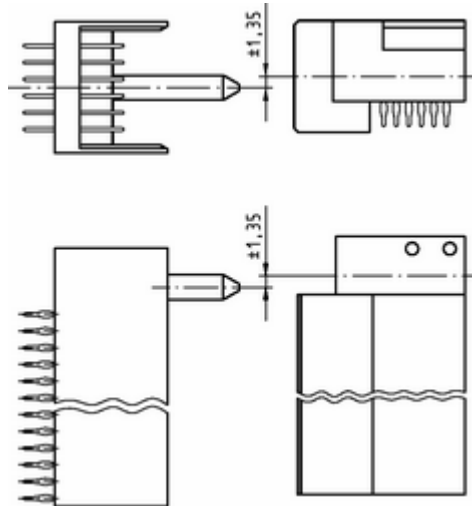
B.3. Electrical Specification

Operational temperature range:	45...+85 °C
Signaling rate:	DC ... 1.536 Gbps
Max. Voltage (U):	< 60 VDC
Creepage distance:	> 0,8 mm
Clearance distance:	> 0,8 mm
Max. Current (I):	0,6 A at max. +35°C temperature rise
Contact resistance (Ohm):	Row a < 0,015 O on mated pair Row f < 0,035 O on mated pair
Insulation resistance:	> 1000 MO
Voltage proof:	750 V (RMS)

B.4. Mechanical Specification

All mechanical dimensions are described in drawings in chapter 9.

Allowed misalignment:	= $\pm 1,35$ mm with guide
-----------------------	----------------------------



Contact range / wipe:	According to IEC 61076-4-101
Basic material of the body:	PC, PCT, PBT or similar. No high temp material required. Connector plastics shall be UL listed with V0.
Contact material:	Phosphor Bronze
Press-fit pin plating:	Tin lead (0,5 ... 3 μm) over nickel (min. 2,0 μm) and press-in zone acc. to IEC 60352-5 (01/02) . ROHS compatible pins are required in the future.
Weight (g):	< 30 g 144 pin
Durability:	≥ 250 mating cycles (IEC 61076-4-101, performance level 2)

B.5. Environmental Requirement

Following values are list of conditions where connector will be used. Connector manufacturer does not have to test connector according

these conditions. However this information must be taken account in connector design.

These requirements come from system requirements and might be extended by a connector environmental test specification in a separate document.

B.5.1. Environment Specification For Operation

Climatic conditions:

Temperature range	-45...+85°C
Relative humidity range	5...100% (ETS 300 019-1-4:1992, class 4.1)
Absolute humidity range	0,26...29g/m
Rate of temperature change	0,5°C/min
Air pressure range	70...106 kPa (ETS 300019-1-1:1991)

Mechanical conditions:

Sinusoidal vibration:

Displacement	3,5mm peak between 5...9Hz
Acceleration	2m/s (~0,2g)
Frequency range	62...500Hz
Sweeps	5 sweep cycles for 3 direction increasing frequency (1dB/octave, logarithmic)

Shocks:

Shock spectrum	Half Sine
Duration	11ms
Acceleration	100m/s ² (10 g)
Number	3 (may be extended for ~10 shocks)
Direction	6 axis (+X, +Y, +Z, -X, -Y, -Z) (total 6 x 3)

Bump shocks:

Acceleration amplitude	400m/s (40g)
Pulse duration	6ms / pulse

Number	500 bumps in each of 6 directions
--------	-----------------------------------

Random:

ASD (14)	0,96m2/s3 or – 3dB/oct
Direction	3 (X, Y, Z)
Frequency	5 – 20 – 800Hz
Duration	3 * 10 min

Earthquake:

Earthquake (zone 4 tests) GR-63-CORE	
--------------------------------------	--

B.5.2. Environment Specification For Transportation

Climatic and mechanical conditions for units, modules and components:

ETS 300 019-1-2: 1994 (testing methods) class 2.3.

ETS 300 019-1-2: 1992 (requirements) class 2.3.

B.6. Coding

Four types of coding are in use.

B.6.1. Coding 0

The connector does not contain any code pins.

B.6.2. Coding 1

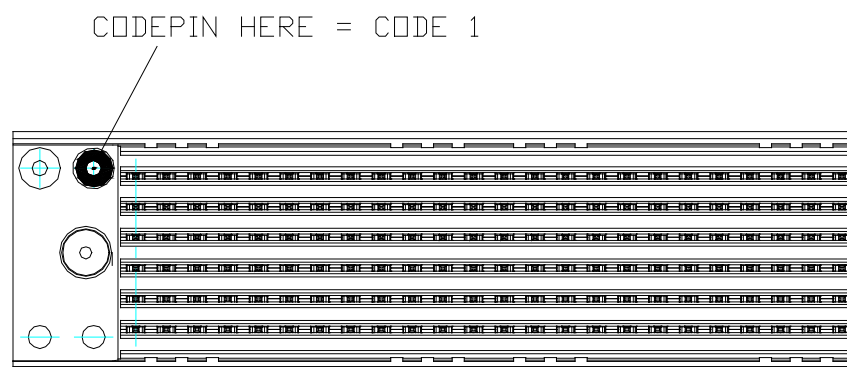


Figure B-2. Male Connector With Guidance And Coding 1

B.6.3. Coding 2

CODE PIN HERE = CODE 2

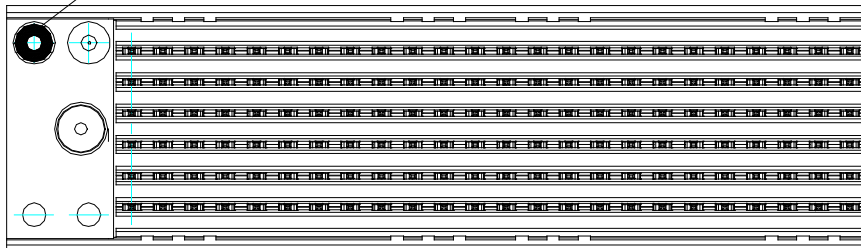


Figure B-3. Male Connector With Guidance And Coding 2

B.6.4. Coding 3

CODE PINS HERE = CODE 3

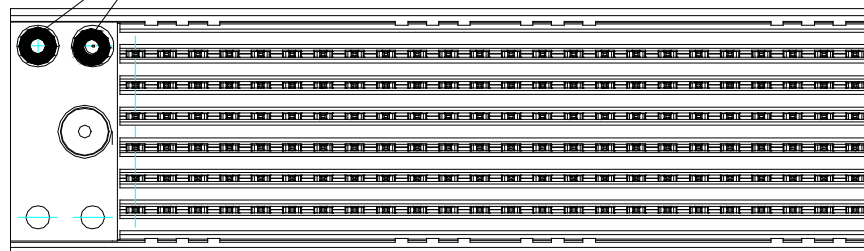


Figure B-4. Male Connector With Guidance And Coding 3

B.7. PCB Layout

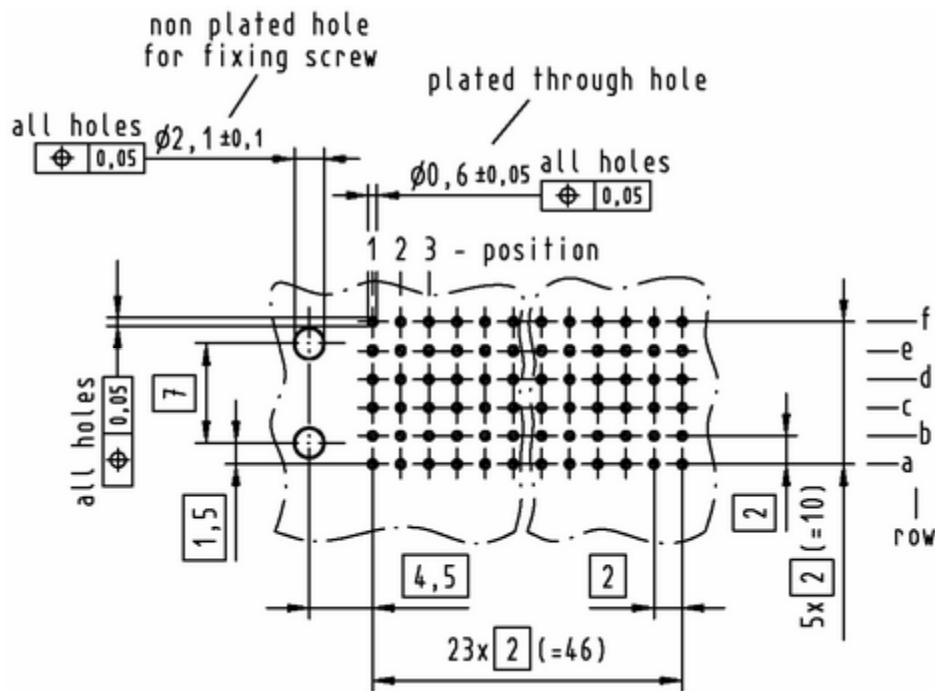


Figure B-5. Lay Out Drawing For 144 Pin Male Press-Fit Connector With Guidance

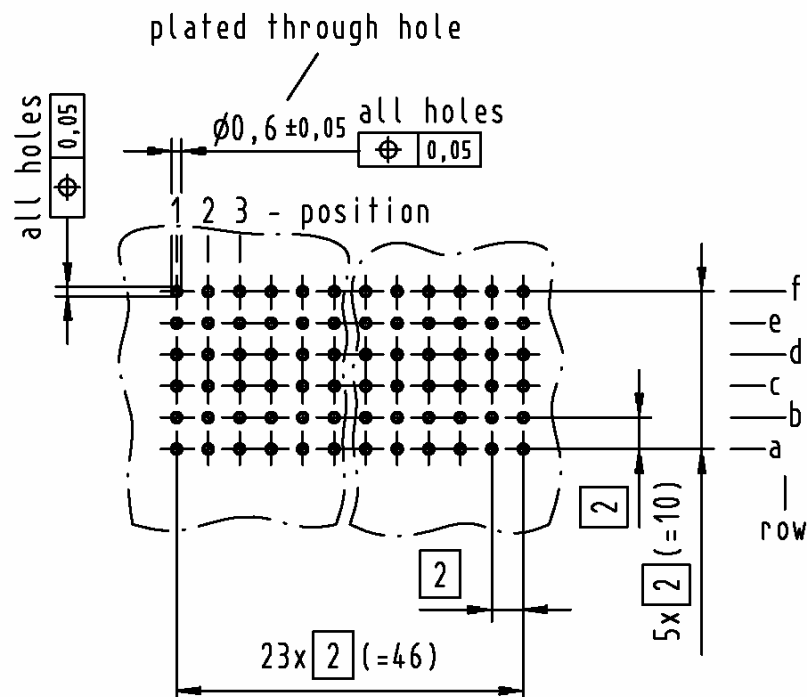


Figure B-6. Layout Drawing For 144 Pin Male Press-Fit Connector Without

Guidance

B.8. Specification Drawings

B.8.1. Male Connector

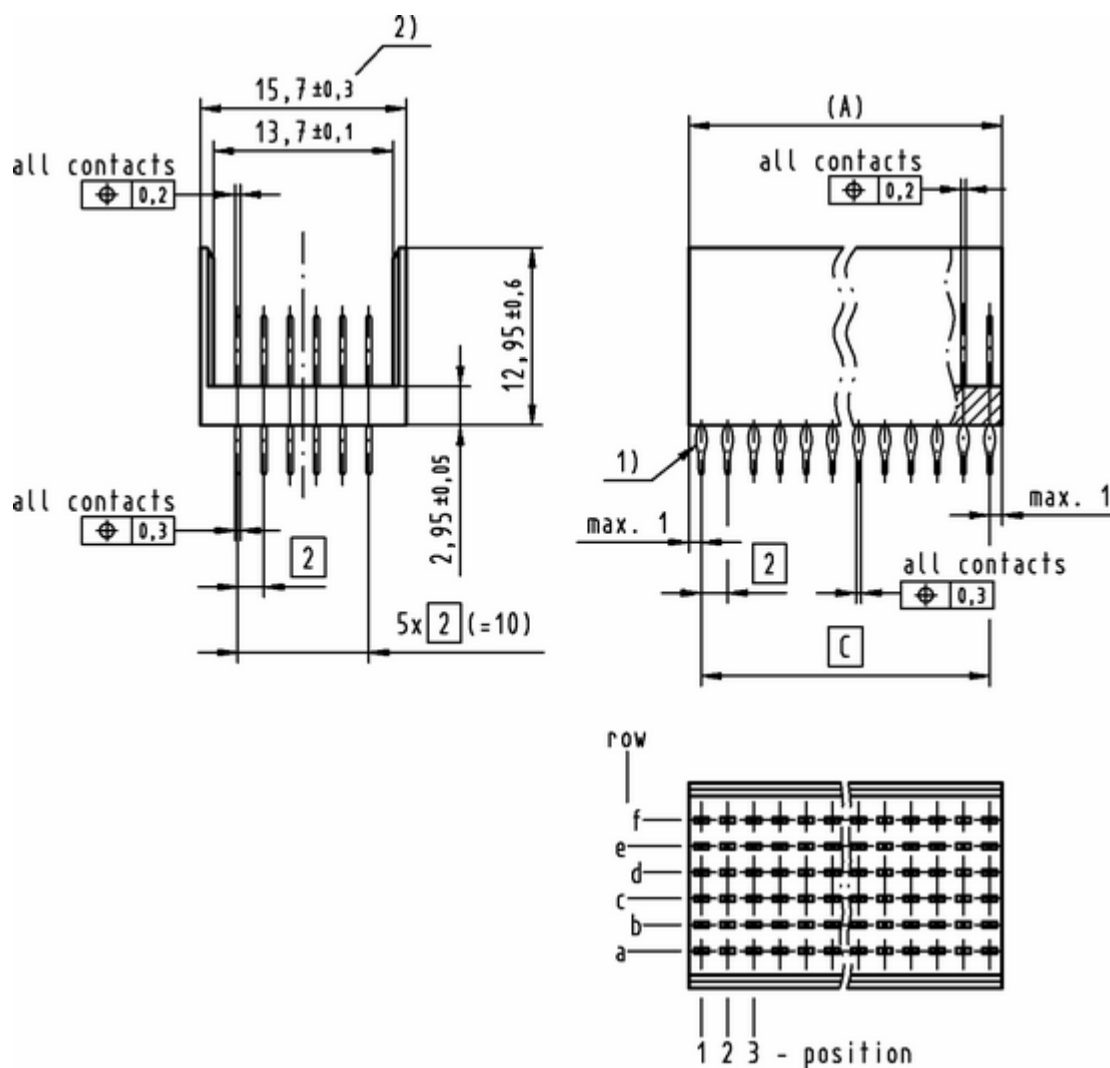


Figure B-7. Male Connector

- 1) Press-fit section acc. to IEC 60352-5
- 2) Dimension for slot distance 15,24 mm : $14,9 \pm 0,1$

A (mm)	C (mm)
max 48	$23 \times 2 = 46$

B.8.2. Male Connector With Endwall

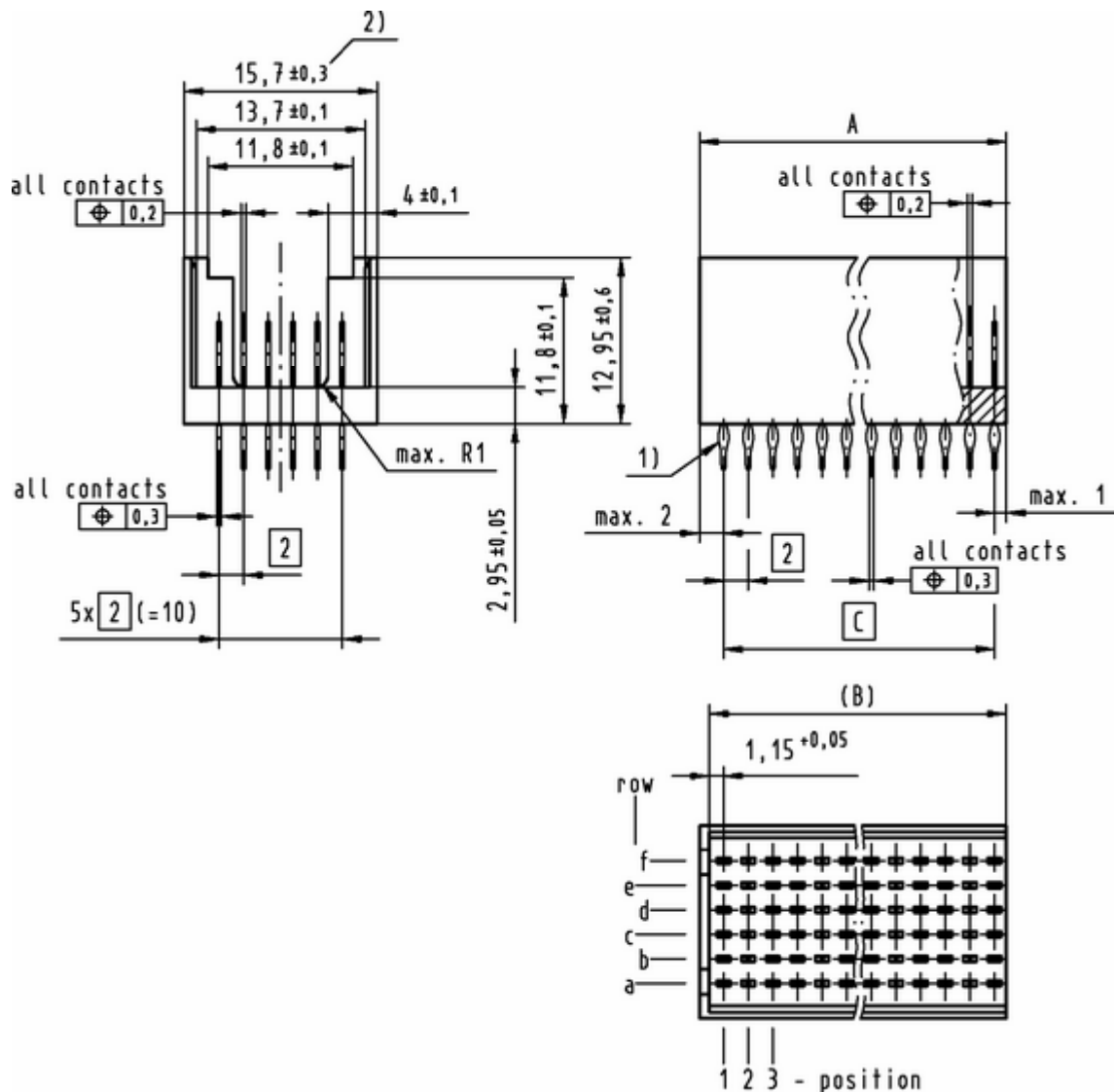


Figure B-8. Male Connector With Endwall

- 1) Press-fit section acc. to IEC 60352-5
- 2) Dimension for slot distance 15,24 mm : $14,9 \pm 0,1$

A (mm)	B (mm)	C (mm)
max 49	48	$23 \times 2 = 46$

B.9. Male Connector With Guidance

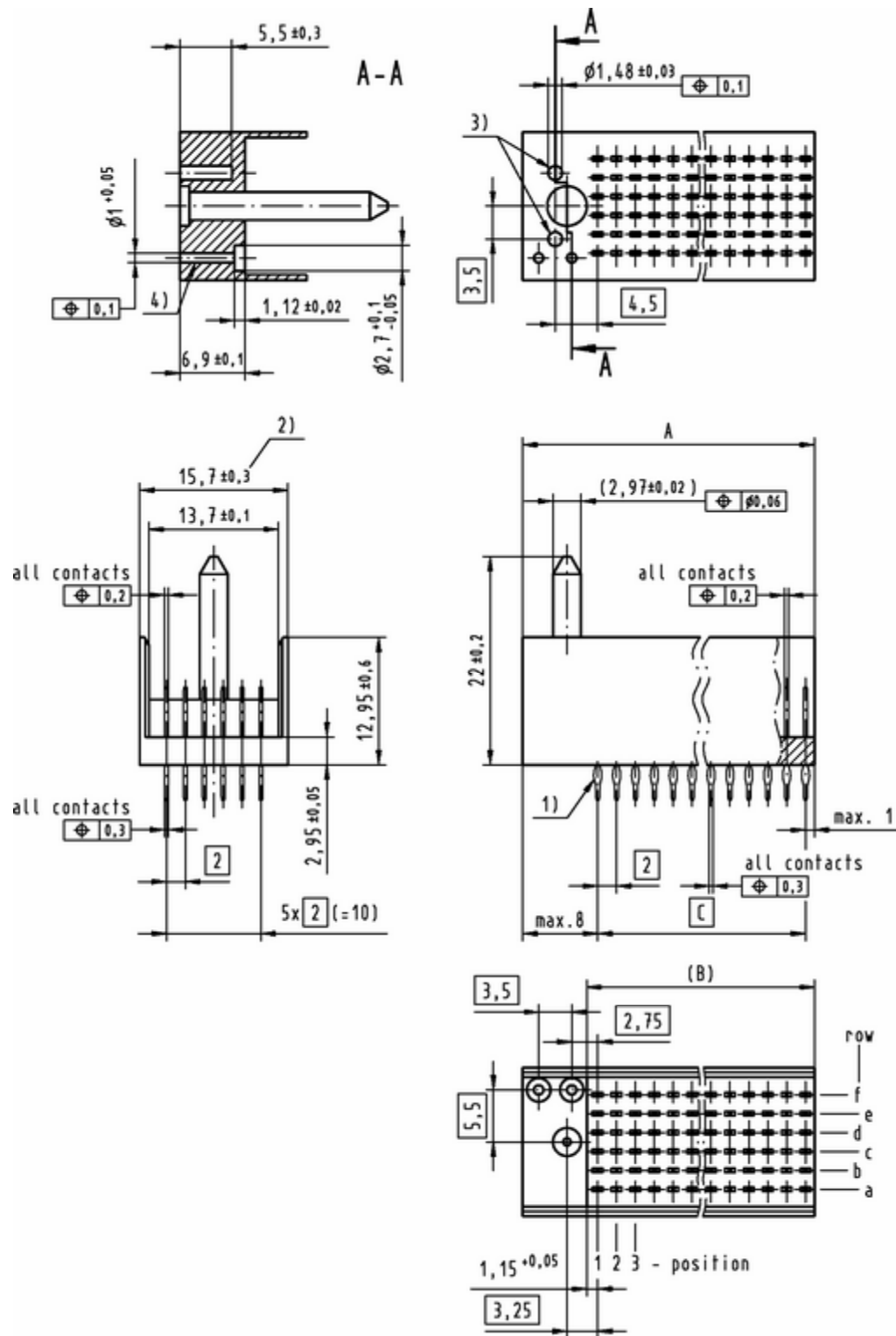


Figure C-9. Male Connector With Guidance

- 1) Press-fit section acc. to IEC 60352-5
- 2) Dimension for slot distance 15,24 mm : $14,9 \pm 0,1$
- 3) Hole for fixing screw
- 4) Hole for coding pin

A (mm)	B (mm)	C (mm)
max 55	48	$23 \times 2 = 46$

B.9.1. Available Pin Type(s)/Length(s)

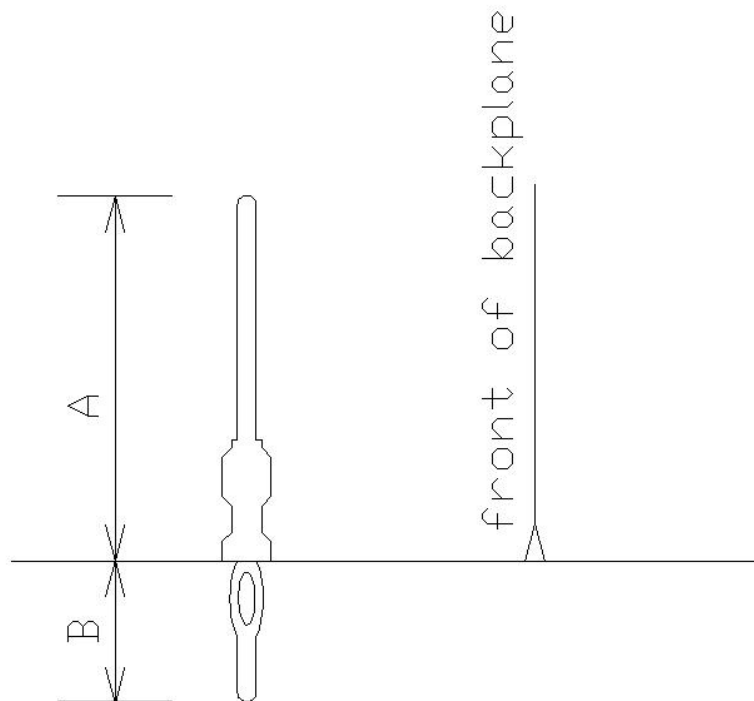


Figure B-10. Available Pin Length(S)

A (mm)	B (mm)
$9,7 \pm 0,2$	$3,7 \pm 0,2$

B.9.2. Coding Pin

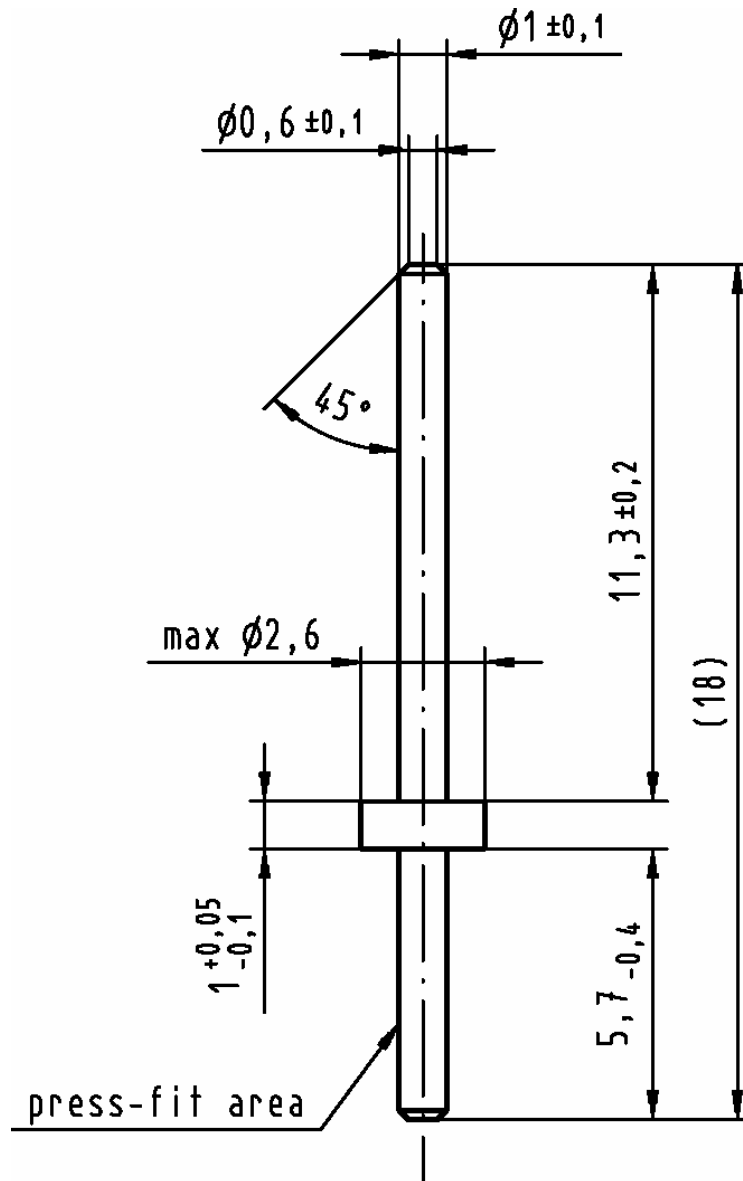


Figure B-11. Coding Pin

Required tensile strength for Coding pin material : $R_m \geq 450\text{N/mm}^2$

B.9.3. Guide Pin

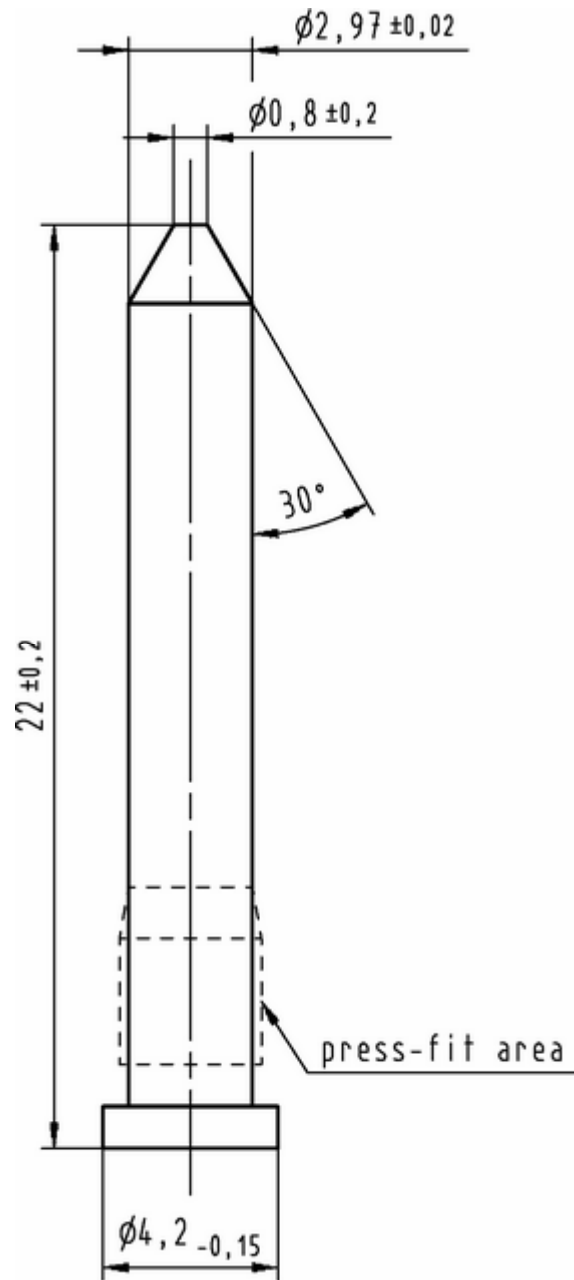


Figure B-12. Guide Pin

Required tensile strength for Guide pin material: $R_m \geq 450 \text{ N/mm}^2$

B.10. Reference Documents

MIL- STD- 883, method 2003,3

ETS 300 019-1-4:1992, class 4.1

ETS 300019-1-1:1991

ETS 300 019-1-2

IEC 512-3, 5b

ISO 9001

Earthquake (zone 4 tests) GR-63-CORE

IEC 61076-4-101

IEC 60352-5 (01/02)

Appendix C. Hard-Metric 2MM 6-Row Daughterboard Receptacle

C.1. Summary of changes

Version	Approved by	Date
0.0.1	Document started	Sep. 05, 2003
0.02	TWG	Mar. 10, 2004

C.2. Scope

Specification for	Hard metric 2mm female right angle receptacle, 144 pins electrical connector. With or without guide and coding block.
-------------------	---

C.3. General Description

Type:	Data
Connection method:	Pin in hole reflow (PCB thickness min 1,45mm, max. 2,15mm) or pressfit (PCB thickness 1,4 – 2,4mm)
Shape:	Right angle female
Number of poles:	6 x 24

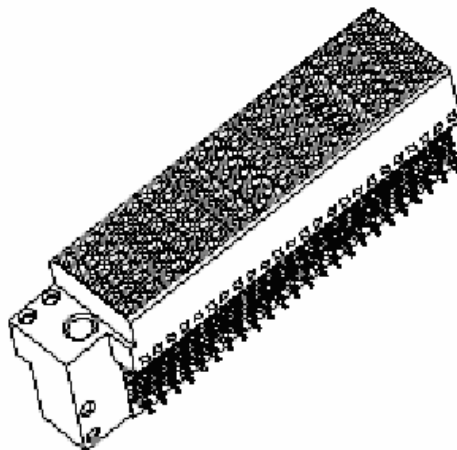


Figure C-1. 2mm Right Angle Female, 144pin Version With Guide And Coding Block

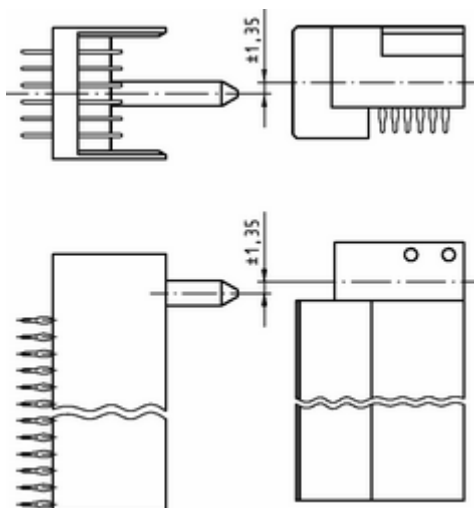
C.4. Electrical Specification

Operational temperature range:	45...+85 °C
Signaling rate:	DC ... 1.536 Gbps
Max. Voltage (U):	< 60 VDC
Creepage distance:	> 0,6 mm
Clearance distance:	> 0,6 mm
Max. Current (I):	0,6 A at max. +35°C temperature rise
Contact resistance (Ohm):	Row a < 0,015 O on mated pair Row f < 0,035 O on mated pair
Insulation resistance:	> 1000 MO
Voltage proof:	750 V (RMS)

C.5. Mechanical Specification

All mechanical dimensions are described in drawings in chapter 9.

Allowed misalignment:	= ±1,35 mm with guide
-----------------------	-----------------------



Contact range / wipe:	According to IEC 61076-4-101
Basic material of the	PIHR connector housing material must be

body:	suitable for lead free reflow process. On pressfit connectors no high temperature material is required. Connector plastics shall be UL listed with V0.
Contact material:	Phosphor Bronze
Press-fit pin plating:	Tin lead (0,5 ... 3 µm) over nickel (min. 2,0 µm) and press-in zone acc. to IEC 60352-5 (01/02) . ROHS compatible pins are required in the future.
Weight (g):	< 30 g 144 pin
Durability:	≥ 250 mating cycles (IEC 61076-4-101, performance level 2)
Solderability	PIHR connector must be suitable for lead free reflow process

C.6. Environmental Requirement

Following values are list of conditions where connector will be used. Connector manufacturer does not have to test connector according these conditions. However this information must be taken account in connector design.

These requirements come from system requirements and might be extended by a connector environmental test specification in a separate document.

C.6.1. Environment specification for operation

Climatic conditions:

Temperature range	-45...+85°C
Relative humidity range	5...100% (ETS 300 019-1-4:1992, class 4.1)
Absolute humidity range	0,26...29g/m
Rate of temperature change	0,5°C/min
Air pressure range	70...106 kPa (ETS 300019-1-1:1991)

Mechanical conditions:

Sinusoidal vibration:

Displacement	3,5mm peak between 5...9Hz
Acceleration	2m/s (~0,2g)
Frequency range	62...500Hz
Sweeps	5 sweep cycles for 3 direction increasing frequency (1dB/octave, logarithmic)

Shocks:

Shock spectrum	Half Sine
Duration	11ms
Acceleration	100m/s ² (10 g)
Number	3 (may be extended for ~10 shocks)
Direction	6 axis (+X, +Y, +Z, -X, -Y, -Z) (total 6 x 3)

Bump shocks:

Acceleration amplitude	400m/s (40g)
Pulse duration	6ms / pulse
Number	500 bumps in each of 6 directions

Random:

ASD (14)	0,96m ² /s ³ or – 3dB/oct
Direction	3 (X, Y, Z)

Frequency	5 – 20 – 800Hz
Duration	3 * 10 min

Earthquake:

Earthquake (zone 4 tests) GR-63-CORE	
--------------------------------------	--

C.6.2. Environment Specification For Transportation

Climatic and mechanical conditions for units, modules and components:

ETS 300 019-1-2: 1994 (testing methods) class 2.3.

ETS 300 019-1-2: 1992 (requirements) class 2.3.

C.7. Coding

Four types of coding are in use.

C.7.1. Coding 0

There are no coding holes in the guide and coding block of the connector.

C.7.2. Coding 1

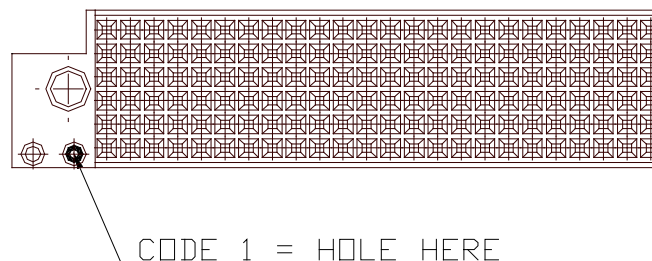


Figure C-2. Female Connector With Guidance And Coding 1

C.7.3. Coding 2

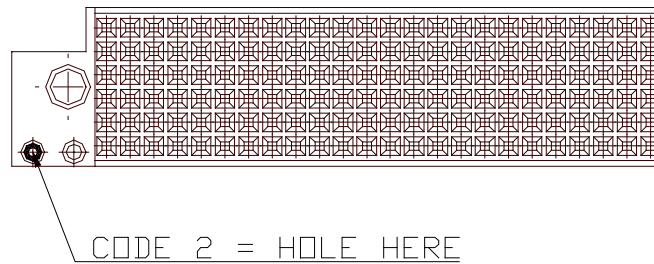


Figure C-3. Female Connector With Guidance And Coding 2

C.7.4. Coding 3

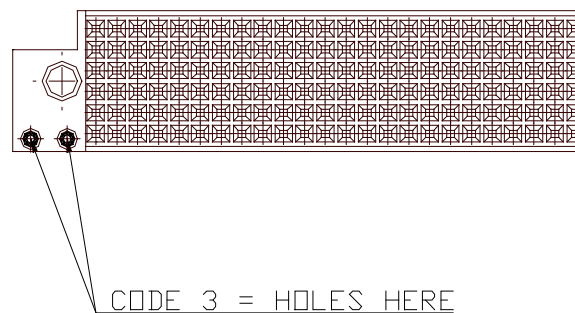


Figure C-4. Female Connector With Guidance And Coding 3

C.8. PCB Layout

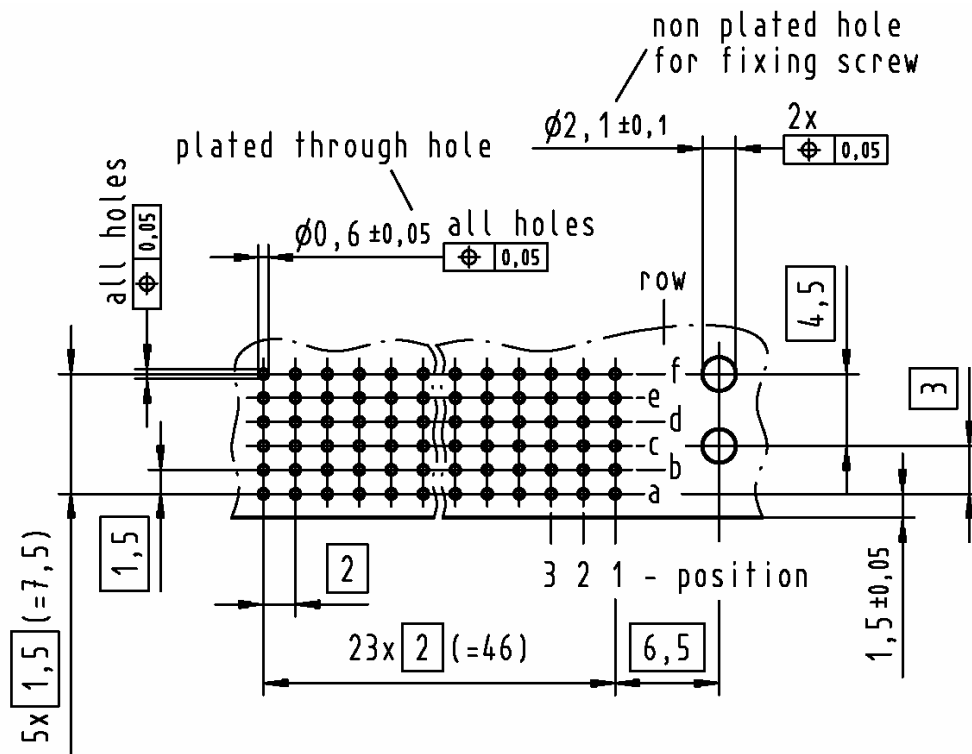


Figure C-5. Board Layout For 144 Pin Female Press-Fit Connector With Guidance

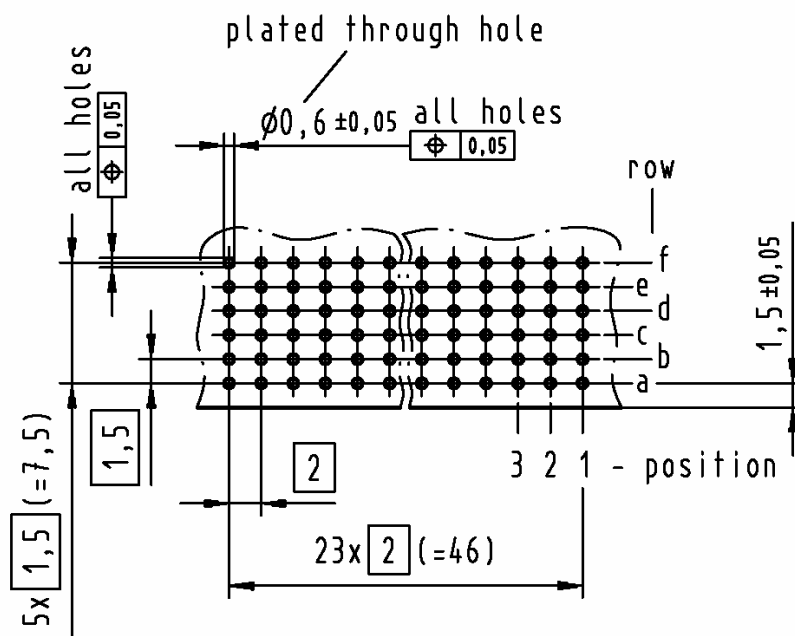


Figure C-6. Board Layout For 144 Pin Female Press-Fit Connector Without Guidance

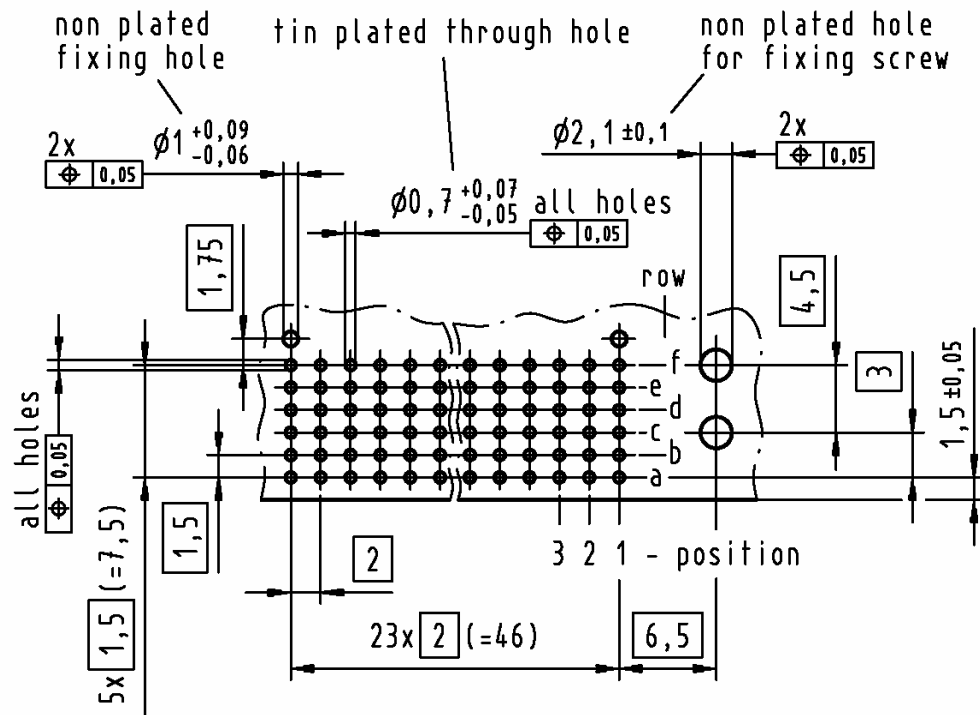


Figure C-7. Layout Drawing For 144 Pin Female PIHR Connector With Guidance

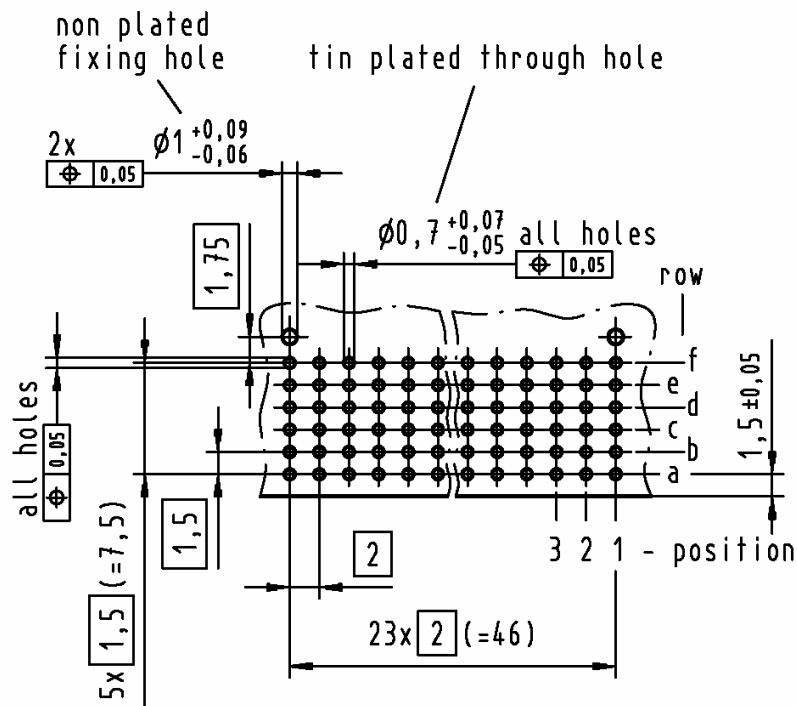


Figure C-8. Board Layout For 144 Pin Female PIHR Connector Without Guidance

C.9. Specification Drawings

C.9.1. Female PIHR Connector

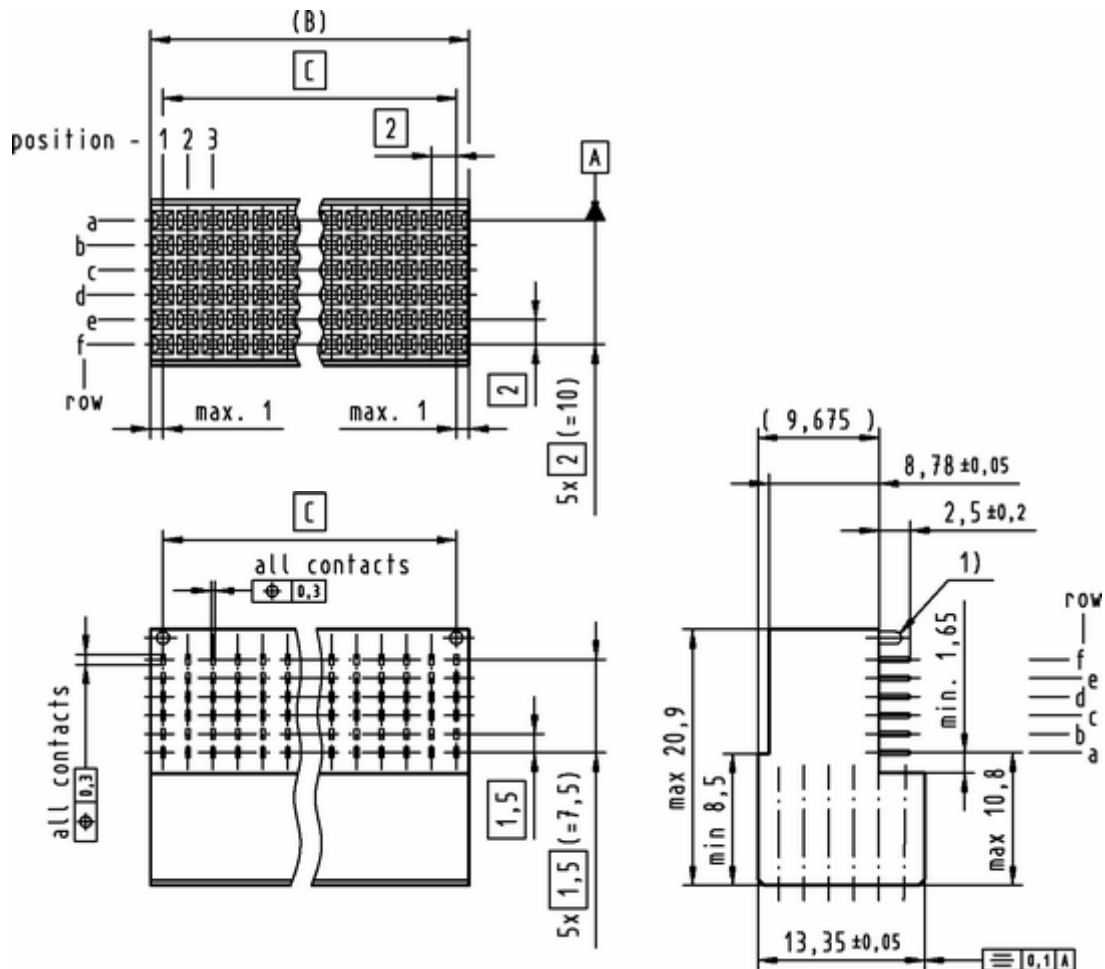


Figure C-9. Female PIHR Connector Without Guidance

1) Forces for locking-pin (if used): insertion force: max 8N; retention force: min 0,5N

Remark: A locking mechanism is necessary to hold the connector in its position for reflow soldering. Whether this mechanism is a plastic peg as shown or something else is not relevant.

Connector Type	B (mm)	C (mm)
144 pin	max 48	23 x 2 = 46

C.9.2. Female PIHR Connector With Guidance

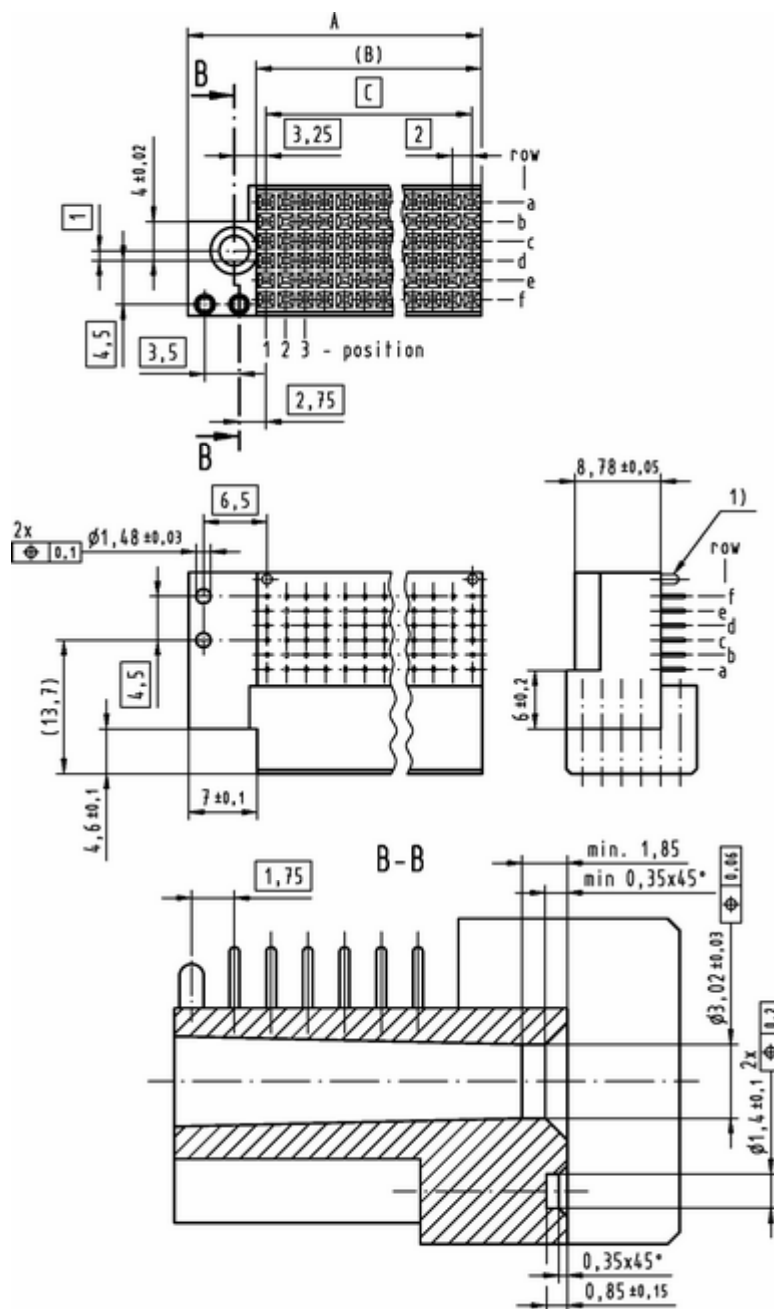


Figure C-10. Female PIHR Connector With Guidance

1) Forces for locking-pin (if used): insertion force: max 8N; retention force: min 0,5N

Connector Type	A (mm)	B (mm)	C (mm)
144 pin with guidance	max 55	max 48	23 x 2 = 46

C.9.3. Female Press-fit Connector

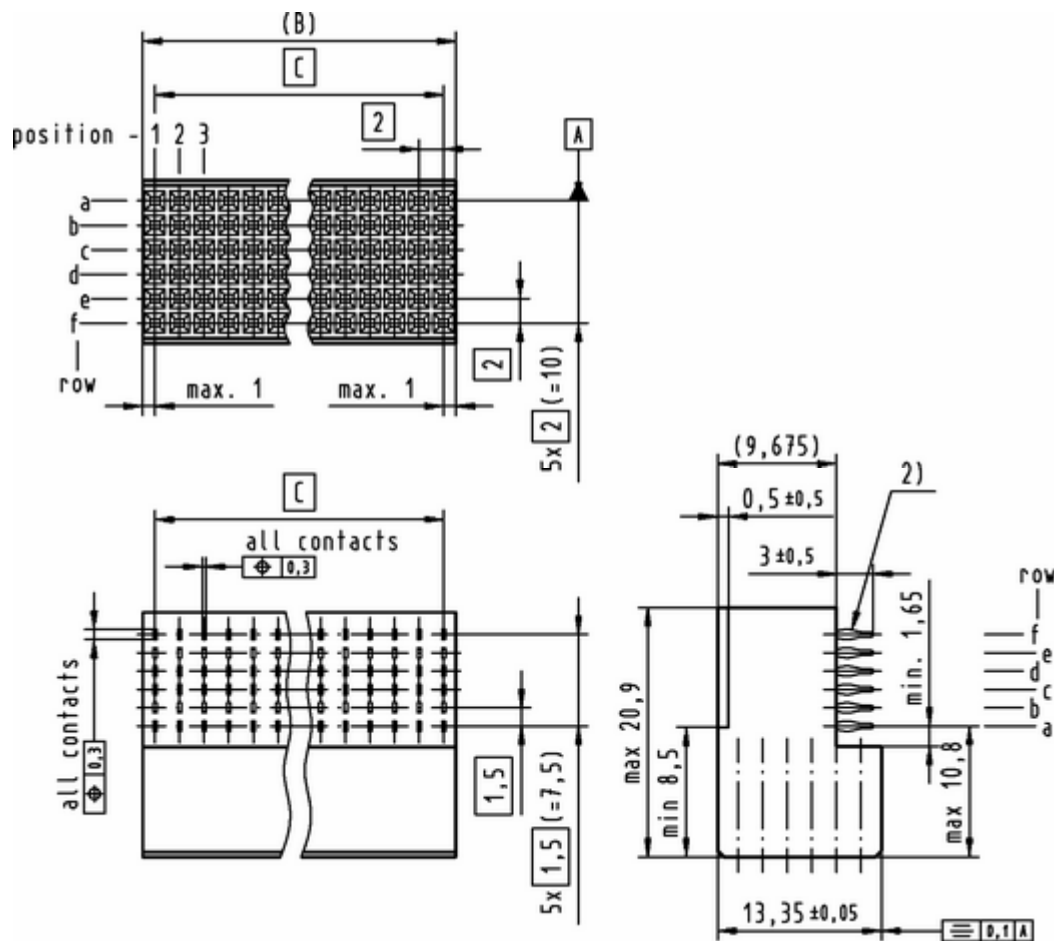


Figure C-11. Female Press-Fit Connector Without Guidance

2) Press-fit section acc. to IEC 60352-5

Connector Type	B (mm)	C (mm)
144 pin	max 48	23 x 2 = 46

C.9.4. Female Press-Fit Connector With Guidance

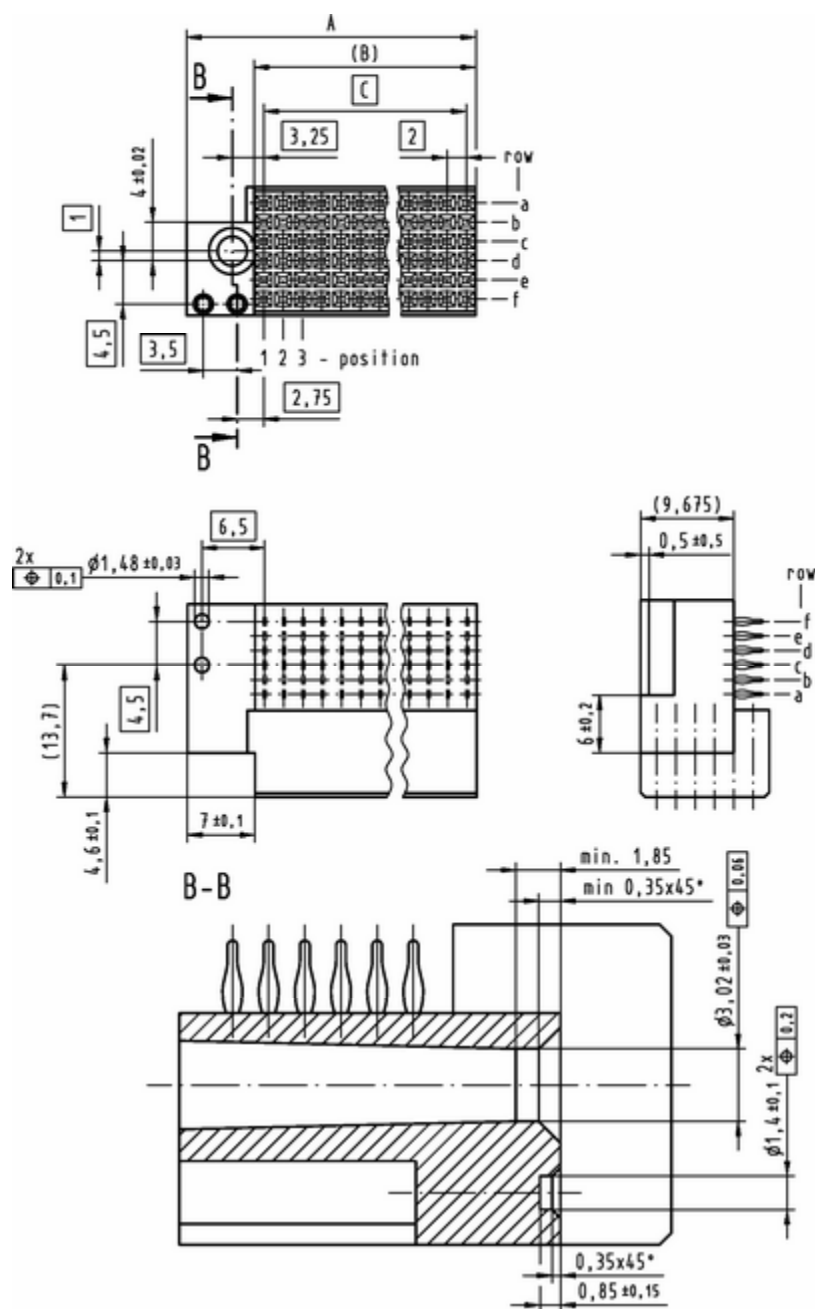


Figure C-12. Female Press-Fit Connector With Guidance

2) Press-fit section acc. to IEC 60352-5

Connector Type	A (mm)	B (mm)	C (mm)
144 pin with guidance	max 55	max 48	23 x 2 = 46

C.10. Reference Documents

MIL- STD- 883, method 2003,3

ETS 300 019-1-4:1992, class 4.1

ETS 300019-1-1:1991

ETS 300 019-1-2

IEC 512-3, 5b

ISO 9001

Earthquake (zone 4 tests) GR-63-CORE

IEC 61076-4-101

IEC 60352-5 (01/02)

Appendix D. HARD-Metric Right Angled Male Power Connector Specification

D.1. Summary of changes

Version	Approved by	Date
0.01		Jan.29, 2004
0.02		Feb.04, 2004
0.03		Mar.03, 2004
0.04		Mar.09, 2004

D.2. Scope

Specification for Hard metric, right angled male.
 4 pin electrical power connector.

D.3. General Description

- Type: Power
- Connection method: Pin in hole reflow or press-fit
(PCB thickness min 1,45 mm x
, max. 2,15mm)
- Shape: Right angled male.
- Number of poles: 4

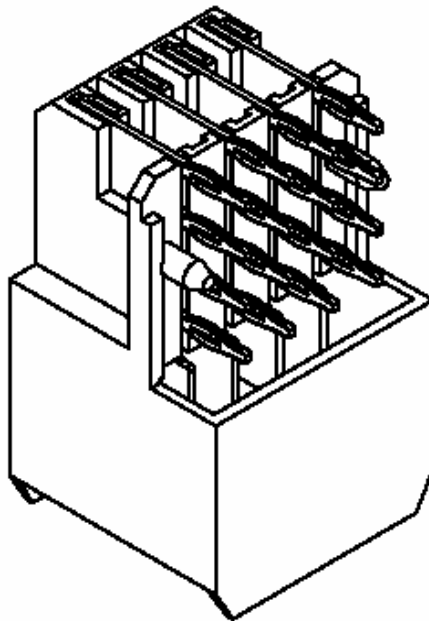


Figure D-1 Right Angle Male, 4-Pin

D.4. Electrical Specification

- Operational temperature range: -45...+85 °C
- Max. Voltage (U): < 60 VDC
- Creepage distance: > 1,2 mm
- Clearance distance: > 1,0 mm
- Maximum current (I): 23A at 80% derating and 70°C
environmental temperature
According to IEC 60512-3 test
5b, with two pins loaded.
- Contact resistance (Ohm): < 0,003 O on mated pair
- Insulation resistance: > 1000 M O

- Voltage proof: 1500 V (RMS)

D.5. Mechanical Specification

- All mechanical dimensions are described in drawings in Section E.9.
- Allowed misalignment: = $\pm 1,0$ mm
- Contact range / wipe: According to IEC 61076-4-101
- Basic material of the body: PIHR connector housing material must be suitable for lead free reflow process. On pressfit connectors no high temperature material is required. Connector plastics shall be UL listed with V0
- Contact Copper alloy
- Solder pin (PIHR): acc. to IEC 60068-2-58
- Press-fit pin: press-in zone acc. to IEC 60352-5 (01/02) .
- Weight (g): < 10g
- Durability: ≥ 250 mating cycles (IEC 61076-4-101, performance level 2)
- Solderability PIHR connector must be suitable for lead free reflow process

PIHR connector must have min 0,5mm stand off to PCB surface. Connector must be compatible with ROHS requirements.

D.6. Environmental Requirement

Following values are a list of conditions where the connector will be used. Connector manufacturer does not have to test the connector according to these conditions. However this information must be taken into account in connector design.

These requirements come from system requirements and might be extended by a connector environmental test specification in a separate document.

D.6.1. Environment Specification For Operation

Climatic conditions:

- Temperature range -45...+85°C.
- Relative humidity range 5...100% (ETS 300 019-1-4:1992, class 4.1).

- Absolute humidity range 0,26...29g/m³.
- Rate of temperature change 0,5°C/min.
- Air pressure range 70...106 kPa (ETS 300019-1-1:1991).

Mechanical conditions:

1. Sinusoidal vibration:

- Displacement 3,5mm peak between 5...9 Hz
- Acceleration 2m/s^2 (~0.2g)
- Frequency range 62...500 Hz
- Sweeps 5 sweep cycles for 3 direction increasing frequency (1dB/octave, logarithmic)

2. Shocks:

- | | |
|----------------|---|
| Shock spectrum | Half Sine |
| Duration | 11ms |
| Acceleration | 100 m/s ² (10 g) |
| • Number | 3 (may be extended for ~10 shocks) |
| • Direction | 6 axis (+X, +Y, +Z, -X, -Y, -Z) (total 6 x 3) |

3. Bump shocks:

- Acceleration amplitude 400 m/s² (40 g)
- Pulse duration 6 ms/ pulse
- Number 500 bumps in each of 6 directions.

4. Random:

- ASD (14) $0,96\text{ m}^2/\text{s}^3$ or – 3 dB/oct
- Direction 3 (X, Y, Z)
- Frequency 5 – 20 – 800 Hz.
- Duration 3 * 10 min

5. Earthquake:

- Earthquake (zone 4 tests) GR-63-CORE

D.6.2. Environment Specification For Transportation

Climatic and mechanical conditions for units, modules and components:

- ETS 300 019-1-2: 1994 (testing methods) class 2.3.
- ETS 300 019-1-2: 1992 (requirements) class 2.3.

D.7. Pin Types and Contact Loading

D.7.1. Pin Types

Type -

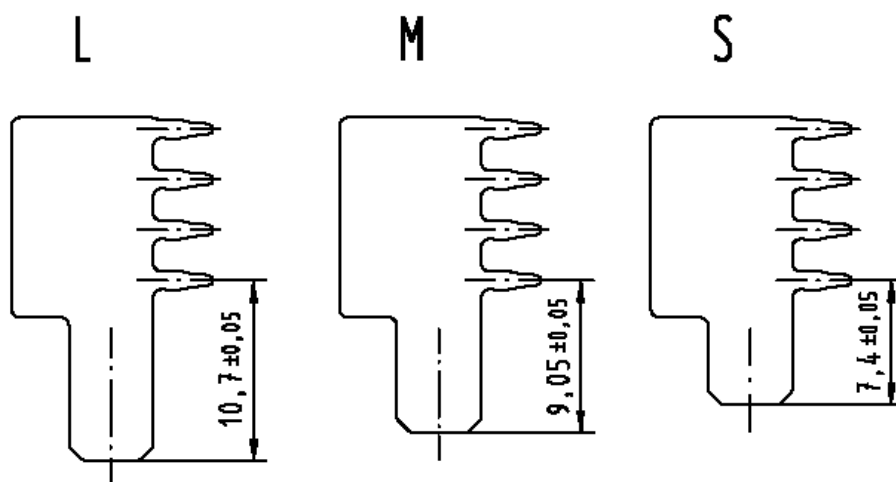


Figure D-2. Pin Lengths For Male Connector

D.7.2. Contact Loading

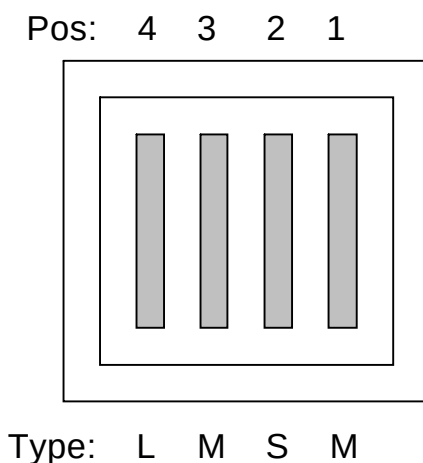


Figure D-3. OBSAI Sequenced Preferred

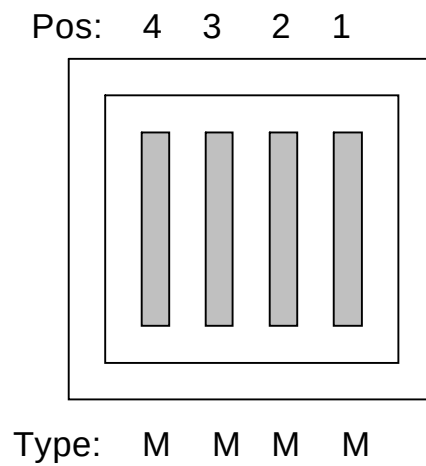


Figure D-4. OBSAI Non-Sequenced Alternative

D.8. PCB Layout

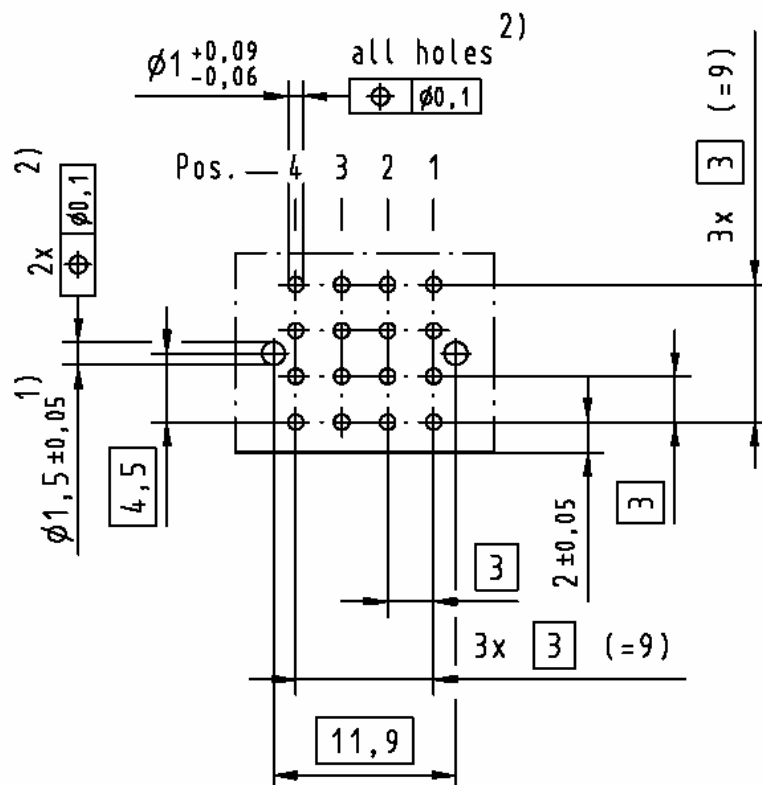


Figure D-5. Board Layout For Male Connector Press-Fit / PIHR, 4-Pin

1. Non-metallized drillings
2. Recommendation per IEC 326-3 for automatic component insertion is "extra fine" Tolerance given in Table 5 ($\phi 0,05$).

D.9. Specification Drawings

D.9.1. Male Pressfit Connector

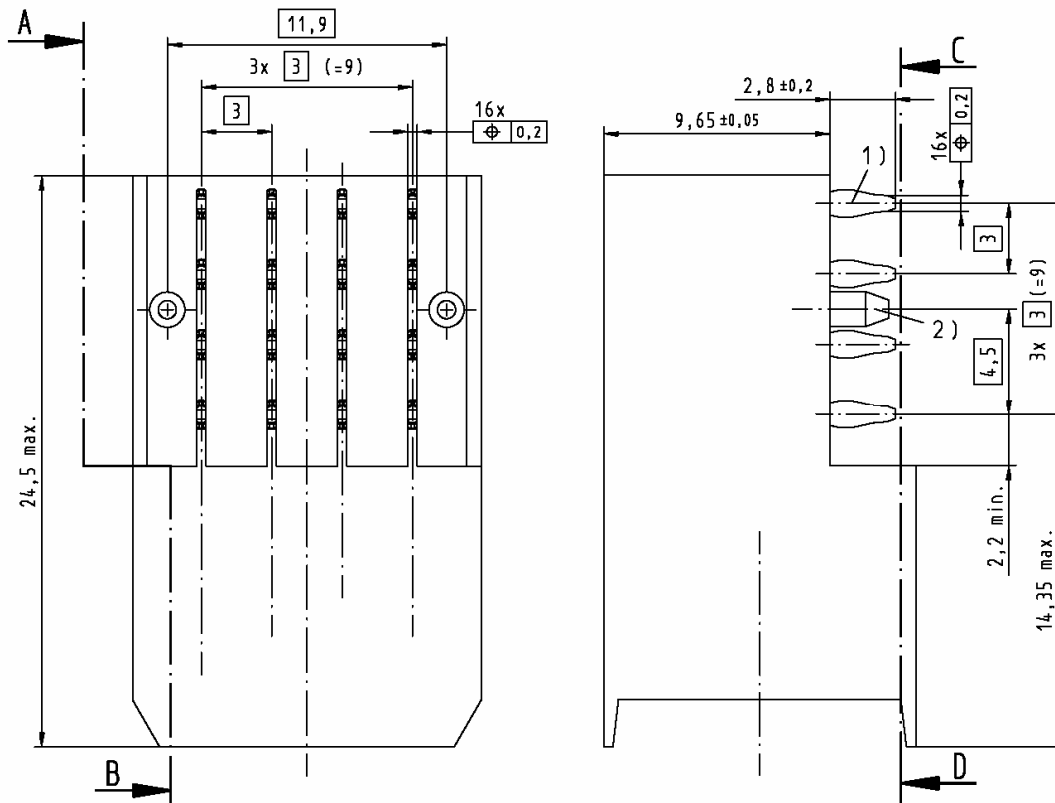


Figure D-6a. Male Connector Pressfit, 4-Pin

- 1) Press-fit section acc. to IEC 60352-5
- 2) Location peg

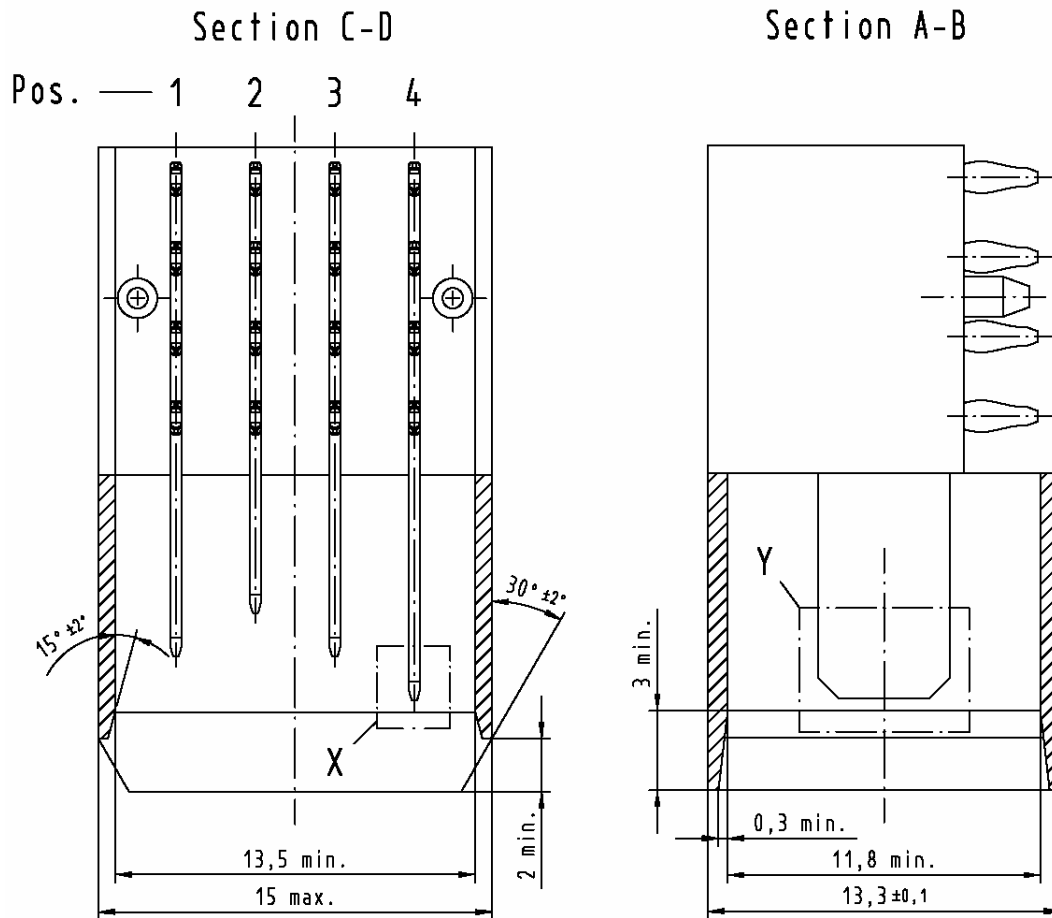


Figure D-6b. Male Connector Pressfit, 4-Pin

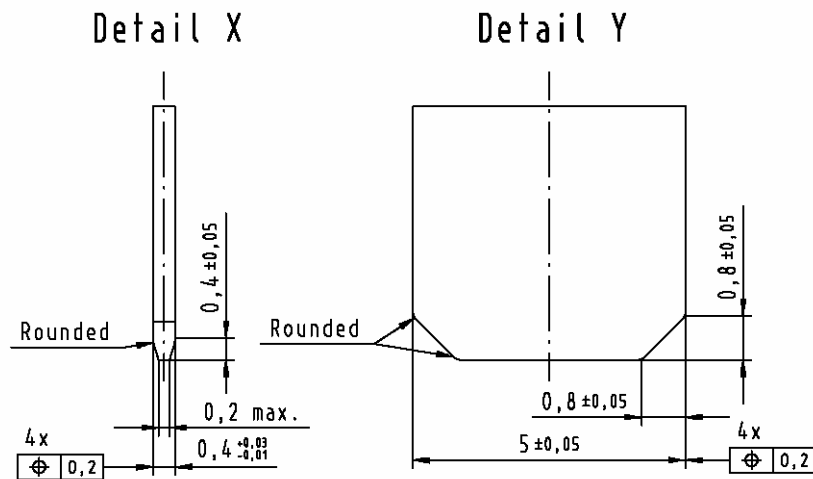


Figure D-6c. Male Connector Pressfit, 4-Pin

D.9.2. Male PIHR Connector

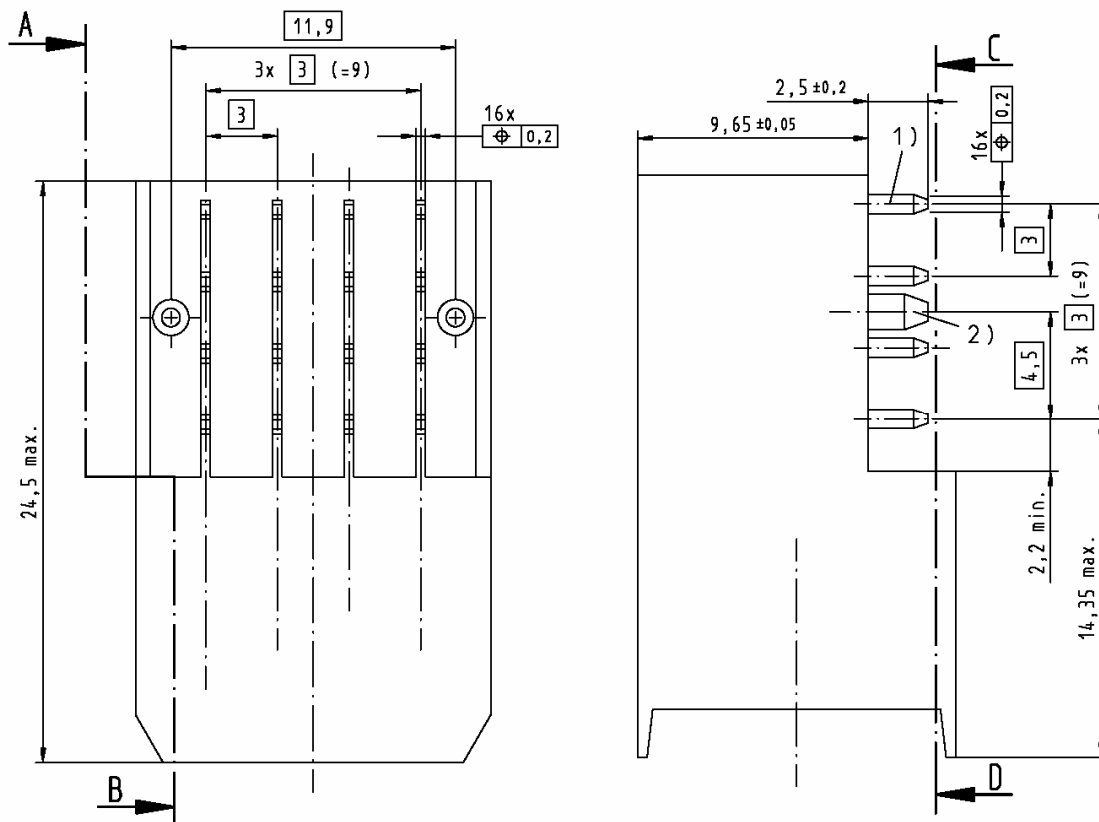


Figure D-7a. Male Connector PIHR, 4-Pin

1) Solder Pin acc. to IEC 60068-2-58

2) Location / locking pin

- Forces for locking-pin:
- Remark:

insertion force: max 8N
retention force: min 0,5N
A locking mechanism is necessary to hold the connector in its position for reflow soldering. Whether this mechanism is a plastic peg as shown or something else is not relevant.

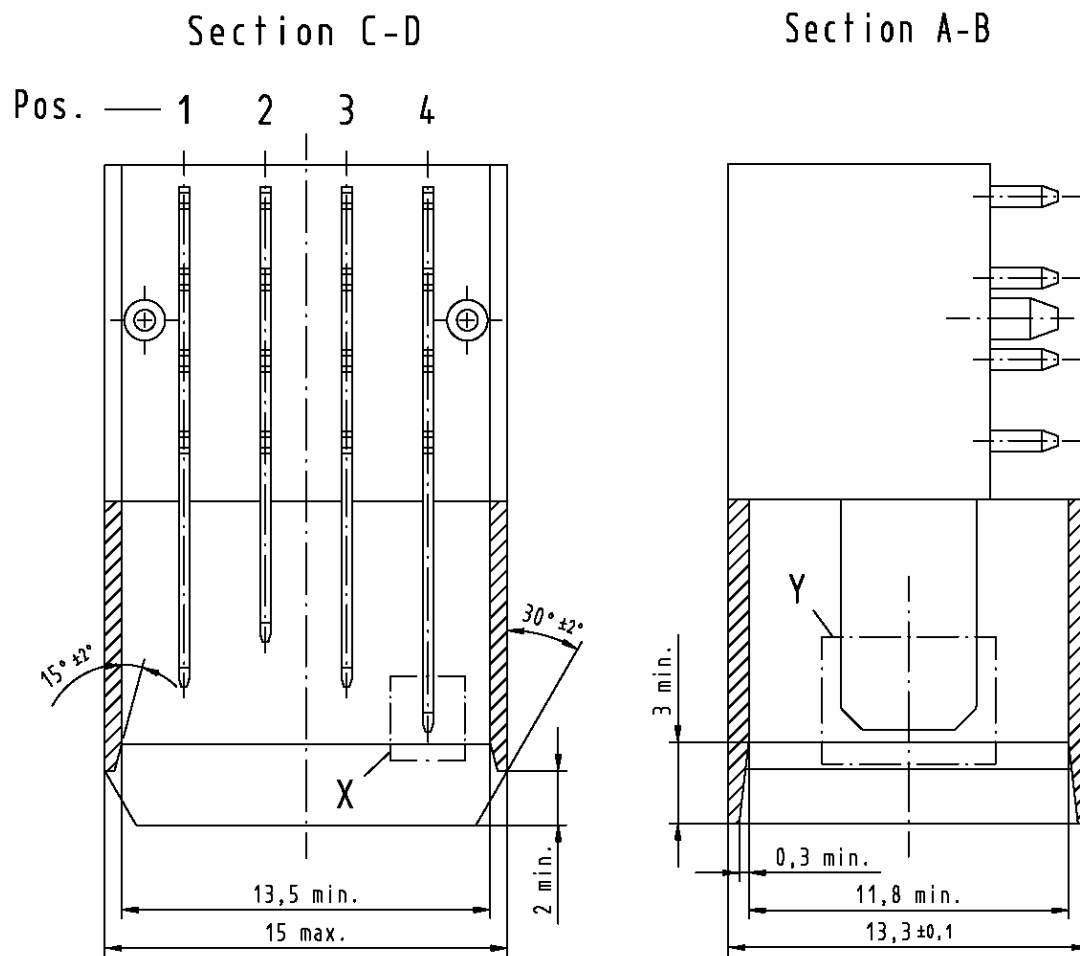


Figure D-7b. Male Connector PIHR, 4-Pin

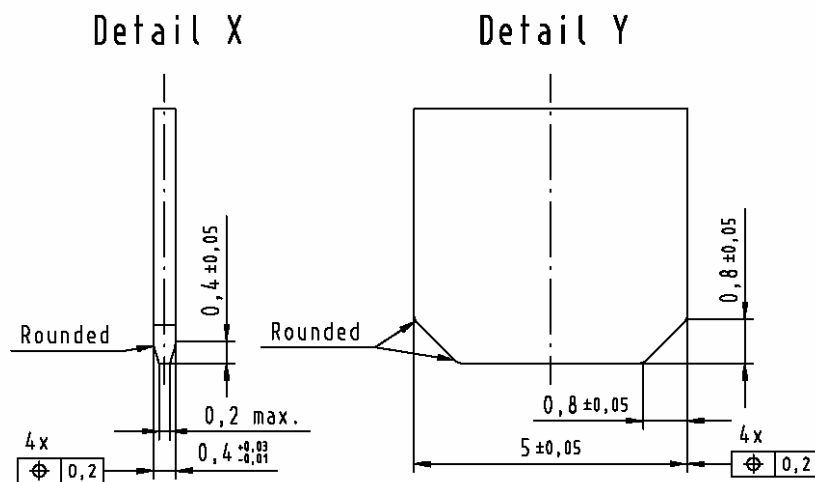


Figure D-7c. Male Connector PIHR, 4-Pin

D.10. Reference Documents

MIL- STD- 883, method 2003,3

ETS 300 019-1-4:1992, class 4.1

ETS 300019-1-1:1991

ETS 300 019-1-2

IEC 60512-3, 5b

ISO 9001

Earthquake (zone 4 tests) GR-63-CORE

IEC 61076-4-101

IEC 60352-5 (01/02)

IEC 60068-2-58

IEC 326-3

Appendix E. HARD-Metric Straight Female Power Connector Specification

E.1. Summary of changes

Version	Approved by	Date
0.01		Jan.29, 2004
0.02		Mar.03, 2004
0.03		Mar.09, 2004

E.2. Scope

Specification for Hard Metric, straight female.
4 pin electrical power connector.

E.3. General Description

- | | |
|----------------------|---|
| • Type: | Power |
| • Connection method: | Press-fit (PCB thickness $\geq 1,4$ mm) |
| • Shape: | Straight female |
| • Number of poles | 4 |

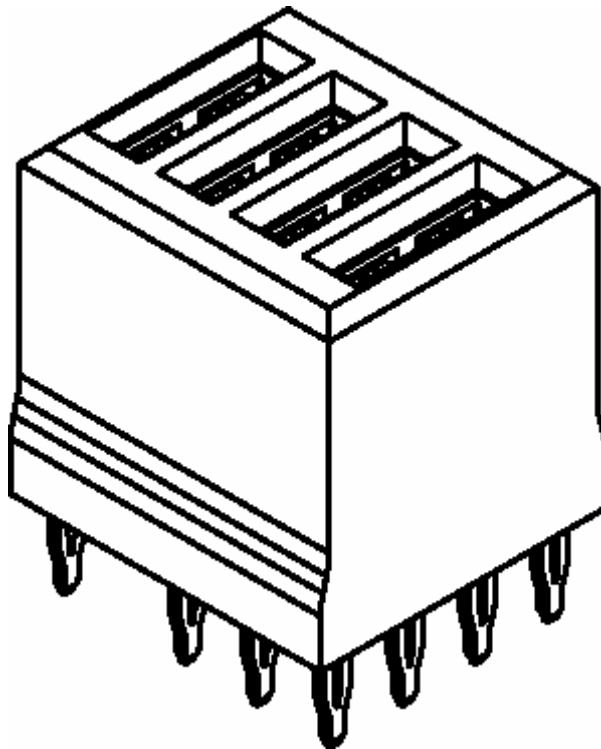


Figure E-1. Straight Female Connector, 4-Pin

E.4. Electrical Specification

- | | |
|----------------------------------|---|
| • Operational temperature range: | -45...+85 °C |
| • Max. Voltage (U): | < 60 VDC |
| • Creepage distance: | > 1,2 mm |
| • Clearance distance: | > 1,0 mm |
| • Max. Current (I): | 23 A at 80% derating and 70°C environmental temperature. Acc. to IEC 60512-3 test 5b. With two pins loaded. |

- Contact resistance (Ohm): < 0,003 O on mated pair
- Insulation resistance: > 1000 M O
- Voltage proof: 1500 V (RMS)

E.5. Mechanical Specification

- All mechanical dimensions are described in drawings in Section E.8.
- Allowed misalignment: = $\pm 1,0$ mm
- Contact range / wipe: According to IEC 61076-4-101
- Basic material of the body: PC, PCT, PBT or similar. No high temp material required.
- Connector plastics: Shall be UL listed with V0.
- Contact material: Copper alloy
- Press-fit pin: press-in zone acc. to IEC 60352-5 (01/02)
- Weight (g): <10 g .
- Durability: ≥ 250 mating cycles (IEC 61076-4-101, performance level 2).

Connector must be compatible with ROHS requirements.

E.6. Environmental Requirement

Following values are a list of conditions where the connector will be used. Connector manufacturer does not have to test the connector according to these conditions. However this information must be taken into account in connector design. These requirements come from system requirements and might be extended by a connector environmental test specification in a separate document.

E.6.1. Environment Specification For Operation

Climatic conditions:

- Temperature range -45...+85°C.
- Relative humidity range 5...100% (ETS 300 019-1-4:1992, class 4.1).
- Absolute humidity range 0,26...29g/m³ .
- Rate of temperature change 0,5°C/min.
- Air pressure range 70...106 kPa (ETS 300019-1-1:1991).

Mechanical conditions:

- 1) Sinusoidal vibration:
 - Displacement 3,5mm peak between 5...9 Hz
 - Acceleration 2m/s^2 ($\sim 0.2g$)
 - Frequency range 62...500 Hz
 - Sweeps 5 sweep cycles for 3 direction increasing frequency (1dB/octave, logarithmic)
- 2) Shocks:
 - Shock spectrum Half Sine
 - Duration 11ms
 - Acceleration 100 m/s^2 (10 g)
 - Number 3 (may be extended for ~ 10 shocks)
 - Direction 6 axis (+X, +Y, +Z, -X, -Y, -Z) (total 6 x 3)
- 3) Bump shocks:
 - Acceleration amplitude 400 m/s^2 (40 g)
 - Pulse duration 6 ms/ pulse
 - Number 500 bumps in each of 6 directions.
- 4) Random:
 - ASD (14) $0,96\text{ m}^2/\text{s}^3$ or -3 dB/oct
 - Direction 3 (X, Y, Z)
 - Frequency 5 – 20 – 800 Hz.
 - Duration $3 * 10\text{ min}$
- 5) Earthquake:
 - Earthquake (zone 4 tests) GR-63-CORE

E.6.2. Environment Specification For Transportation

Climatic and mechanical conditions for units, modules and components:

- ETS 300 019-1-2: 1994 (testing methods) class 2.3.
- ETS 300 019-1-2: 1992 (requirements) class 2.3.

E.7. PCB Layout

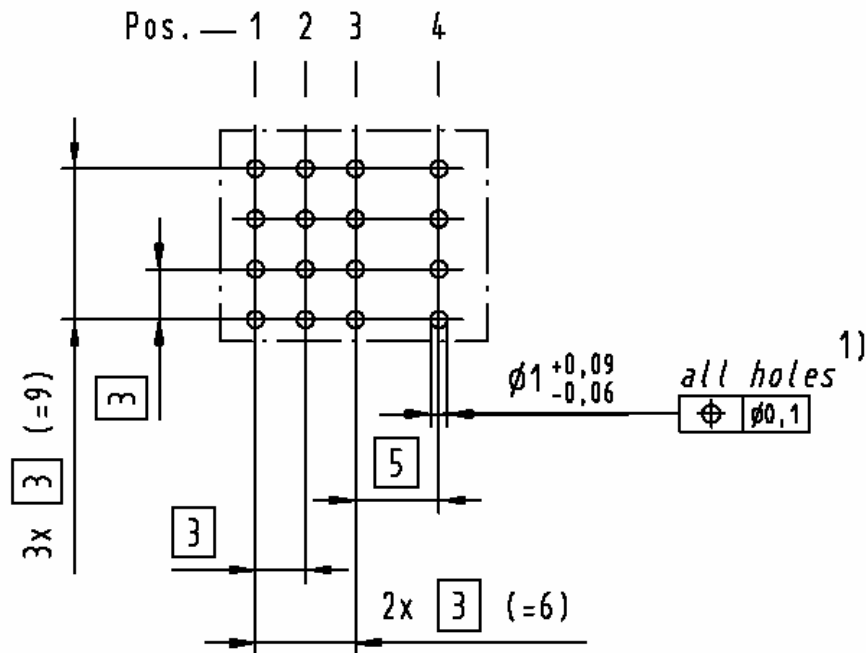


Figure E-2. Board Layout For Female Connector Press-Fit, 4-Pin

- 1) Recommendation per IEC 326-3 for automatic component insertion is "extra fine" Tolerance given in Table 5 ($\phi 0,05$).

E.8. Specification Drawings

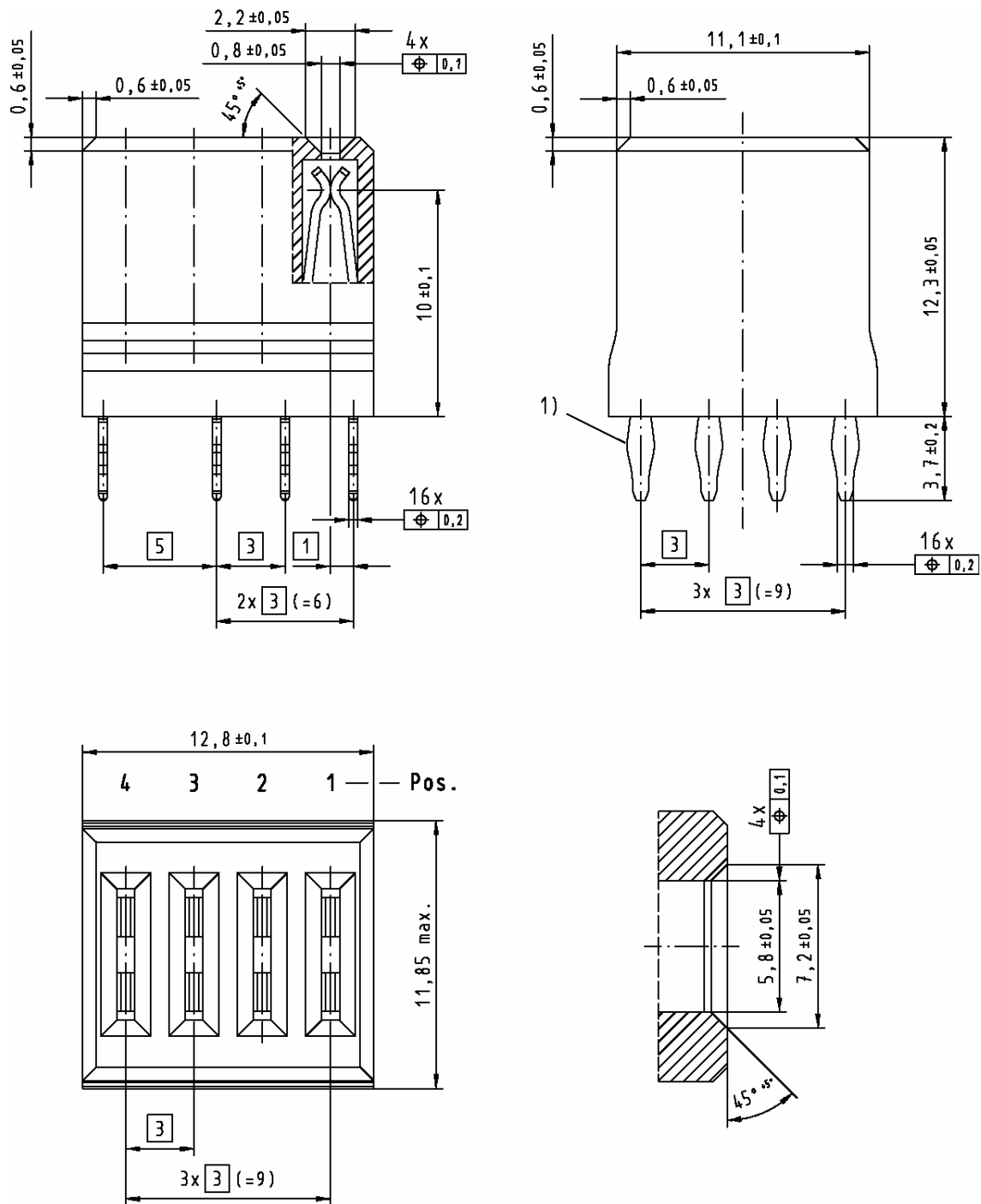


Figure E-3. Female Connector Press-Fit, 4-Pin

1) Press-fit section acc. to IEC 60352-5

E.9. Reference Documents

- MIL- STD- 883, method 2003,3
- ETS 300 019-1-4:1992, class 4.1
- ETS 300019-1-1:1991
- ETS 300 019-1-2
- IEC 60512-3, 5b
- ISO 9001
- Earthquake (zone 4 tests) GR-63-CORE
- IEC 61076-4-101
- IEC 60352-5 (01/02)
- IEC 326-3

TAB B



Reference Point 3 Specification

Version 3.1

Contents

1	Summary of Changes	12
2	Scope	13
3	Reference Point 3 Architecture	14
3.1	Parameter Definitions.....	14
3.2	Module Interface Toward RP3	15
3.3	Topology	16
3.3.1	Mesh	16
3.3.2	Centralized Combiner and Distributor	18
3.4	Inter-Cabinet Connections	20
3.4.1	Inter-Cabinet Mesh	20
3.4.2	Connections between Bridge Modules.....	21
3.4.3	Connections between Combiner and Distributor Modules	22
4	Protocol Stack	24
4.1	Physical Layer.....	25
4.1.1	Electrical Signalling.....	25
4.1.2	Data Format and Line Coding	25
4.1.3	Bus Clock.....	26
4.2	Data Link Layer	26
4.2.1	Message Overview	26
4.2.2	Frame Structure	27
4.2.3	Counters	29
4.2.4	Transmission of Frame Structure.....	30
4.2.5	Reception of Frame Structure	31
4.2.6	Empty Message	34
4.2.7	Synchronisation	34
4.2.8	Measurements	38
4.3	Transport Layer.....	39
4.3.1	Overview of Transport Layer.....	39
4.3.2	Message Format – Address Field	42
4.3.3	Message Router.....	43
4.3.4	Message Multiplexer and Demultiplexer	44

4.3.5	Summing Unit	46
4.4	Application Layer.....	48
4.4.1	Addressing	48
4.4.2	Paths.....	49
4.4.3	Message Transmission Rules	50
4.4.4	Bus Manager.....	52
4.4.5	Buffering Requirements	52
4.4.6	Message Format – TYPE Field	53
4.4.7	Message Format – TIMESTAMP Field	53
4.4.8	Message Format – PAYLOAD Field	54
4.4.9	Control and Measurement Data Mapping	60
5	Electrical Specifications	63
5.1	Overview	63
5.1.1	Explanatory Note on Electrical Specifications.....	63
5.1.2	Equalization	63
5.1.3	Compliance Interconnect	64
5.2	Receiver Characteristics	64
5.2.1	AC Coupling.....	64
5.2.2	Input Impedance	66
5.2.3	Receiver Compliance Mask	66
5.2.4	Jitter Tolerance	67
5.2.5	Bit Error Ratio (BER).....	67
5.3	Transmitter Characteristics	68
5.3.1	Load	70
5.3.2	Amplitude	70
5.3.3	Output Impedance	70
5.3.4	Transmitter Compliance	71
5.4	Measurement and Test Requirements	71
5.4.1	TYPE 1 Compliance Interconnect Definition	71
5.4.2	TYPE 2 Compliance Interconnect Definition	72
5.4.3	TYPE 3 Compliance Interconnect Definition	73
5.4.4	Eye Mask Measurements	75
5.4.5	Transmit Jitter	76
5.4.6	Jitter Tolerance	76

6	RP3-01 Interface for Remote RF Unit.....	77
6.1	Architecture.....	77
6.2	Protocol Stack.....	79
6.2.1	Physical Layer.....	79
6.2.2	RP3-01 - Transfer of RP1 Data Over RP3.....	79
6.2.3	RP1 Frame Clock Bursts	79
6.2.4	Ethernet Transmission	84
6.2.5	Line Rate Auto-Negotiation.....	87
6.2.6	RTT Measurement and Internal Delays of a RRU.....	89
6.2.7	Virtual HW Reset	92
7	OAM&P.....	94
7.1	OAM&P Parameters.....	94
7.1.1	External Parameters of Data Link Layer	94
7.1.2	Error Cases at Data Link Layer.....	96
7.1.3	External Parameters of Transport Layer	96
7.1.4	Error Cases at Transport Layer.....	99
7.1.5	Other External Parameters	99
	Appendix A: Media Adapter and Media Options – Fibre Optics	101
	Appendix B: Multiplexing Examples (Informative)	102
	Appendix C: RP3 Bus Configuration Algorithm (Informative).....	105
	Appendix D: Parameters for 802.16 Message Transmission.....	110
	Appendix E: Background Information on TYPE 1 – 3 Interconnects (Informative).....	113
	Glossary	115
	References	116

List of Figures

Figure 1: RP3 interface of RF and baseband modules. There exists maximum K pairs of unidirectional links toward RP3.	16
Figure 2: Full mesh connecting two baseband and three RF modules. Each baseband module is connected to every RF module and vice versa.	17
Figure 3: Full mesh connecting K baseband modules to K RF modules. All the connections are not drawn.	18
Figure 4: Centralized combiner and distributor (main and redundant) embedded into RP3 interface.....	19
Figure 5: Centralized combiner and distributor embedded into RP3 interface. Redundant C/D is not applied.	20
Figure 6: Full mesh between RF and baseband modules of two cabinets.	21
Figure 7: Bridge modules extending RP3 interface to two cabinets. Mesh topology is shown in intra-cabinet RF-baseband connections but also centralized combiner and distributor topology may be applied.	22
Figure 8: RP3 interface extended over two cabinets by connecting C/Ds together (redundant C/D not applied).	23
Figure 9: Layered structure of the bus protocol.	24
Figure 10: Illustration of Physical layer structure – data flow approach.....	25
Figure 11: Message format of RP3 protocol stack.....	26
Figure 12: Master frame illustrating the sequence according to which WCDMA, GSM/EDGE, and 802.16 messages are inserted to the bus (parameter set M_MG=21, N_MG=1920, K_MG=1, i = 1).....	28
Figure 13: Master frame illustrating the sequence according to which CDMA messages are inserted to the bus (parameter set M_MG=13, N_MG=3072, K_MG=3, i =1).....	28
Figure 14: Message Group structures for WCDMA, GSM/EDGE, and 802.16 air interface standards at 768 Mbps (1x), 1536Mbps (2x), and 3072Mbps (4x) line rates. Time span corresponding to a single message group at 768Mbps line rate is shown.	29
Figure 15: Timing of message slot counters for an example MG and MF definition. .	30
Figure 16: Master Frame is transmitted at an offset to the RP3 bus frame tick in each bus node.	31
Figure 17: Run time and measurement windows of received Master Frame.....	32
Figure 18: An example of Master Frame timings (downlink direction).	33
Figure 19: Example of Δ and Π assignments to a bus network.	33
Figure 20: Empty message. The address field consists of thirteen ‘1’ bits while rest of the message contains don’t care x bits.	34

Figure 21: State diagram of the transmitter.	36
Figure 22: State diagram for the receiver.	38
Figure 23: Transport layer with a common message router for all received messages.	40
Figure 24: Transport layer with dedicated downlink and uplink message routers. Also message multiplexer, demultiplexer, and summing unit is shown.	41
Figure 25: Address sub-fields.	42
Figure 26: Functionality of message router.	43
Figure 27: Illustration of message multiplexer.	46
Figure 28: Functionality of Summing unit. Type check of input messages is not shown.	48
Figure 29: Arbitrary bus configuration with two paths. Message slots are not shown.	49
Figure 30: Illustration of 802.16 data transmission into RP3 link using Dual Bit Map algorithm.	52
Figure 31: WCDMA DL Payload Mapping.	55
Figure 32: WCDMA UL Payload Mapping.	56
Figure 33: GSM/EDGE UL Payload Mapping.	57
Figure 34: GSM/EDGE downlink burst for a modulator block.	58
Figure 35: GSM/EDGE associated control information for a channelizer block.	58
Figure 36: CDMA2000 DL Payload Mapping.	59
Figure 37: CDMA2000 UL Payload Mapping.	59
Figure 38: 802.16 downlink and uplink payload mapping.	60
Figure 39: Generic control message.	60
Figure 40: Air interface synchronized control message.	62
Figure 41: Receiver Compliance Mask.	66
Figure 42: Sinusoidal Jitter Mask.	67
Figure 43: Example Transmitter Output Mask (For Information Only)	70
Figure 44: TYPE 1 Compliance Interconnect Differential Insertion Loss.	72
Figure 45: TYPE 2 Compliance Interconnect Differential Insertion Loss.	73
Figure 46: TYPE 3 Differential Transfer Function Chart.	74
Figure 47: TYPE 3 Differential Return Loss Chart.	75
Figure 48: Eye Mask Alignment.	76
Figure 49: RP3-01 example architecture. Base station with remote RF units (RRUs). RRUs in chain, ring, and tree-and-branch topologies. Examples of RP3-01 master and slave ports of RRUs are also shown.	77

Figure 50: Logical model of OBSAI RP3-01 point-to-point interface.....	78
Figure 51: Examples of mapping RP1 and RP3-01 link O&M data into RP3 messages.....	80
Figure 52: RP1 frame clock synchronization burst from CCM.....	80
Figure 53: RP3-01 frame clock synchronization message.	83
Figure 54: Timing principle in RP1 frame clock burst transfer.	84
Figure 55: Ethernet frame transfer over RP3-01 network is done as a point-to-point transfer between a pair of nodes.....	84
Figure 56: RP3-01 line rate auto-negotiation is done between a pair of nodes (LC and RRU or between adjacent RRUs).	87
Figure 57: Internal delays of Class #1 RRU.	90
Figure 58: Internal delays of Class #2 RRU.	90
Figure 59: Internal delays of Class #3 RRU.	91
Figure 60: RTT Measurement message.....	92
Figure 61: Virtual HW reset message.....	93
Figure 62: Example block diagram of Transport layer.....	102
Figure 63: An example of message multiplexing from four 768 Mbps links into one 1536 Mbps link.	103
Figure 64: An example of message interleaving from one 768 Mbps link into one 3072 Mbps link.	103
Figure 65: An example of message interleaving from fifteen 768 Mbps links into three 1536 Mbps link.	104
Figure 66: An example of message interleaving from three partly full 1536 Mbps 'links into one 3072 Mbps link.	104
Figure 67: An example base station configuration.....	105
Figure 68: Data flows between BB and RF modules. Addresses of modules and antenna-carriers (or up/down converters at RF) are also shown.....	106
Figure 69: Index assignment to the ports of combiner distributor. Mapping of downlink messages to RP3 message slots is also shown.....	107
Figure 70: Mapping of uplink messages to RP3 message slots.	109
Figure 71: TYPE 1 and TYPE 2 Interconnects.	113
Figure 72: TYPE-3 Backplane Interconnect	114
Figure 73: TYPE-3 Cable Interconnect.....	114

List of Tables

1		
2		
3	Table 1: Architecture related RP3 parameters and their values.	14
4	Table 2: Size of the message.	27
5	Table 3: Measurements performed by the Physical layer.	39
6	Table 4: An example of a table.	44
7	Table 5: Multiplexing table for the case where all messages from four	
8	768Mbps links are multiplexed to a single 3072Mbps link.	45
9	Table 6: Multiplexing table for the case where all messages from two	
10	1536Mbps links are multiplexed to a single 3072Mbps link.	45
11	Table 7: Multiplexing table for the case where all messages from one 1536Mbps	
12	link and two 768Mbps links are multiplexed to a single 3072Mbps link.	45
13	Table 8: Multiplexing table for the case where all messages from two	
14	768Mbps link are multiplexed to a single 1536Mbps link.	45
15	Table 9: Multiplexing table for the case where all messages from three	
16	768Mbps links are multiplexed to a single 3072Mbps link.	46
17	Table 10: Definition of the parameters of the dual bit map concept.	51
18	Table 11: Content of type field.	53
19	Table 12: Content of generic control message.	60
20	Table 13: Content of air interface synchronized control message.	61
21	Table 14: Receiver Characteristics – 768 Mbaud.	65
22	Table 15: Receiver Characteristics – 1536 Mbaud.	65
23	Table 16: Receiver Characteristics – 3072 Mbaud.	65
24	Table 17: Receiver Compliance Mask Parameters.	67
25	Table 18: Sinusoidal Jitter Mask Values.	68
26	Table 19: Transmitter Characteristics – 768 Mbaud.	68
27	Table 20: Transmitter Characteristics – 1536 Mbaud.	69
28	Table 21: Transmitter Characteristics – 3072 Mbaud.	69
29	Table 22: Content of RP3-01 frame clock synchronization message.	83
30	Table 23: Content of the time stamp field of RP3 messages in relation to	
31	Ethernet MAC frame data of the payload.	85
32	Table 24: Content of RP3-01 Ethernet message.	86
33	Table 25: Parameters of line rate auto-negotiation algorithm.	88
34	Table 26: Content of an RTT Measurement message.	92
35	Table 27: Content of virtual HW reset message.	93
36	Table 28: Input and output parameters of Data link layer.	94

1	Table 29: Error cases at Data link layer.	97
2	Table 30: Input and output parameters of Transport layer. All the parameters are	
3	defined for the whole node.	97
4	Table 31: Possible error cases at Transport layer.	99
5	Table 32: Other input and output parameters of bus node.	100
6	Table 33: Options for optical cabling.	101
7	Table 34: Optical interface recommendations for different RP3-01 line rates.	
8	This table is for information only.	101
9	Table 35: Downlink routing table.	107
10	Table 36: Uplink routing table.	107
11	Table 37: Message transmission rules for BB modules #1 and #2.	108
12	Table 38: Message transmission rules for RF module #1.	108
13	Table 39: Message transmission rules for RF module #2.	109
14	Table 40: Parameters for supported 802.16 profiles in case of 768 Mbps	
15	virtual RP3 link.	110
16	Table 41: Parameters for supported 802.16 profiles in case of 1536 Mbps	
17	virtual RP3 link.	111
18	Table 42: Parameters for supported 802.16 profiles in case of 3072 Mbps	
19	virtual RP3 link.	112

FOREWORD

OBSAI description and specification documents are developed within the Technical Working Group of the Open Base Station Architecture Initiative Special Interest Group (OBSAI SIG). Members of the OBSAI TWG serve voluntarily and without compensation. The description and specifications developed within OBSAI represent a consensus of the broad expertise on the subject within the OBSAI SIG.

The OBSAI SIG uses the following terminology in the specifications:

- “shall” expresses a provision that is binding
- “should” and “may” expresses non-mandatory provisions
- “will” expresses a declaration of purpose on the part of the OBSAI SIG. It may be necessary to use “will” in cases where the simple future tense is required

Use of an OBSAI reference or specification document is wholly voluntary. The existence of an OBSAI Specification does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the OBSAI Specification. Furthermore, the viewpoint expressed at the time a specification is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the specification. Every OBSAI Specification is subjected to review in accordance with the Open Base Station Architecture Initiative Rules And Procedures.

Implementation of all or part of an OBSAI Specification may require licenses under third party intellectual property rights, including without limitation, patent rights (such a third party may or may not be an OBSAI Member). The Promoters of the OBSAI Specification are not responsible and shall not be held responsible in any manner for identifying or failing to identify any or all such third party intellectual property rights.

The information in this document is subject to change without notice and describes only the product defined in the introduction of this documentation. This document is intended for the use of OBSAI Member’s customers only for the purposes of the agreement under which the document is submitted, and no part of it may be reproduced or transmitted in any form or means without the prior written permission of OBSAI Management Board. The document has been prepared for use by professional and properly trained personnel, and the customer assumes full responsibility when using it. OBSAI Management Board, Marketing Working Group and Technical Working Group welcome

customer comments as part of the process of continuous development and improvement of the documentation.

The information or statements given in this document concerning the suitability, capacity, or performance of the mentioned hardware or software products cannot be considered binding but shall be defined in the agreement made between OBSAI members. However, the OBSAI Management Board, Marketing Working Group or Technical Working Group have made all reasonable efforts to ensure that the instructions contained in the document are adequate and free of material errors and omissions.

OBSAI liability for any errors in the document is limited to the documentary correction of errors. OBSAI WILL NOT BE RESPONSIBLE IN ANY EVENT FOR ERRORS IN THIS DOCUMENT OR FOR ANY DAMAGES, INCIDENTAL OR CONSEQUENTIAL (INCLUDING MONETARY LOSSES), that might arise from the use of this document or the information in it.

This document and the product it describes are considered protected by copyright according to the applicable laws. OBSAI logo is a registered trademark of Open Base Station Architecture Initiative Special Interest Group. Other product names mentioned in this document may be trademarks of their respective companies, and they are mentioned for identification purposes only. Copyright © Open Base Station Architecture Initiative Special Interest Group. All rights reserved. Users are cautioned to check to determine that they have the latest edition of any OBSAI Specification.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of OBSAI, the OBSAI TWG will initiate action to prepare appropriate responses. Since OBSAI Specifications represent a consensus of OBSAI Member's interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason OBSAI and the members of its Technical Working Groups are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on specifications and requests for interpretations should be addressed to:

Peter Kenington

Chairman, OBSAI Technical Working Group

Linear Communications Consultants Ltd.

Email: pbk@linearcomms.com

1 Summary of Changes

Version	Approved by	Date	Comment
1.0	OBSAI Management Board	16/04/2004	Initial Release
2.0	OBSAI Management Board	11/10/2004	Second Release – incorporating remote head operation
3.0	OBSAI Management Board	01/08/2005	Third Release – incorporating WiMAX support
3.1	OBSAI Management Board	13/11/2006	Point Release – incorporating 4x line rate electrical specifications and related Type3 interconnect definition

2 Scope

This document specifies the Reference Point 3 characteristics. Chapter 3 defines the connectivity between RF and baseband modules. The protocol stack for data transfer is defined in Chapter 4, excluding the electrical characteristics, which are specified in Chapter 5. The protocol stack for data transfer between the base station and Remote RF units is defined in Chapter 6. Configuration and management of the protocol is detailed in Chapter 7.

3 Reference Point 3 Architecture

OBSAI Reference Point 3 (RP3) interface exists between RF and BB modules of a base station. In this chapter, architecture or connectivity between RF and baseband modules is specified.

Architecture related parameters are defined in Section 3.1. In Section 3.2, interface of RF and baseband modules toward RP3 is defined. Topology of RP3 is specified in Section 3.3. Inter-cabinet connections are considered in Section 3.4.

3.1 Parameter Definitions

A set of parameters is used to define the architecture characteristics of RP3. In Table 1, the values of all of the parameters are specified.

Table 1: Architecture related RP3 parameters and their values.

Parameter	Value	Description
K	9	Maximum number of pairs of unidirectional links with differential signalling in every RF and baseband module.
K_{RF_in}	$0 \leq K_{RF_in} \leq 9$	Number of incoming links with differential signalling that are implemented to a RF module.
K_{RF_out}	$0 \leq K_{RF_out} \leq 9$	Number of outgoing links with differential signalling that are implemented to a RF module
K_{BB_in}	$0 \leq K_{BB_in} \leq 9$	Number of incoming links with differential signalling that are implemented to a baseband module.
K_{BB_out}	$0 \leq K_{BB_out} \leq 9$	Number of outgoing links with differential signalling that are implemented to a baseband module

Parameter	Value	Description
P	36	Number of connector pins that are allocated to RP3 differential signals in every RF and baseband module
M	Integer, value equal to or greater than 1.	Number of RF modules in a base station.
N	Integer, value equal to or greater than 1.	Number of baseband modules in a base station.

1

2 3.2 Module Interface Toward RP3

3 Each OBSAI compliant RF module shall have maximum K (see Table 1)
4 pairs of unidirectional links with differential signalling toward RP3
5 interface, i.e. $2 \cdot K$ links in total. A pair constitutes one incoming signal
6 and one outgoing signal. Each RF module shall implement K_{RF_in}
7 incoming links, where $0 \leq K_{RF_in} \leq K$, and K_{RF_out} outgoing links, where
8 $0 \leq K_{RF_out} \leq K$. Among the implemented links with differential
9 signalling, unused links shall be disabled for power conservation
10 purposes. Each link requires 2 pins due to differential signalling that is
11 used. In total, there exist P pins in each RF module that are allocated
12 to differential signals to support RP3 interface. Each RF module shall
13 always have the same pins of a connector allocated to RP3 signals.
14 Refer to [6] for detailed pin definition.

15 The RF module may contain transmit functionality only, receiver
16 functionality only, or both transmit and receive functionality.

17 Each OBSAI compliant baseband module shall have maximum K (see
18 Table 1) pairs of unidirectional links with differential signalling toward
19 RP3 interface, i.e. $2 \cdot K$ links in total. A pair constitutes one incoming
20 signal and one outgoing signal. Each baseband module shall implement
21 K_{BB_in} incoming links, where $0 \leq K_{BB_in} \leq K$, and K_{BB_out} outgoing links,
22 where $0 \leq K_{BB_out} \leq K$. Among the implemented links with differential
23 signalling, unused links shall be disabled for power conservation
24 purposes. Each link requires 2 pins due to differential signalling that is
25 used. In total, there exist P pins in each baseband module that are
26 allocated for differential signals to support RP3 interface. Each
27 baseband module shall always have the same pins of a connector
28 allocated to RP3 signals. Refer to [5] for detailed pin definition.

Differential signalling is used at the lowest protocol layer at RP3 interface. On each link, bus protocol as specified in Chapter 4 shall be applied.

Figure 1 illustrates RP3 interface of RF and baseband modules. A pair of unidirectional links with differential signalling is shown in the figure as a double-headed arrow.

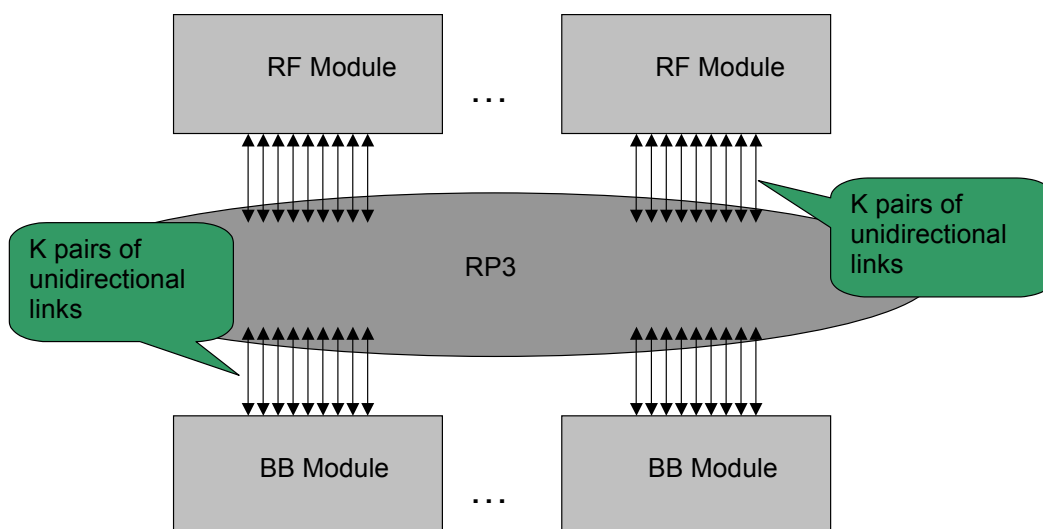


Figure 1: RP3 interface of RF and baseband modules. There exists maximum K pairs of unidirectional links toward RP3.

3.3 Topology

Topology specifies connectivity between RF and baseband modules. Two approaches are suggested (but not mandated): mesh and centralized combiner and distributor. They are explained in more detail below.

3.3.1 Mesh

Assuming N baseband and M RF modules in a base station, there exist in total $N \times M$ pairs of unidirectional links with differential signalling between baseband and RF modules in a full mesh. Each baseband module is connected to M RF modules while every RF module is connected to N baseband modules. Each pair of unidirectional links is implemented as two unidirectional differential signals in opposite directions for data and control transfer. Optionally, there may exist several parallel pairs of unidirectional links between any baseband and RF modules when very high data throughput is required. Connection

between any pair of baseband and RF modules may also be missing if it is not required. When there does not exist any connection between a baseband module and an RF module, a partial mesh rather than full mesh is obtained.

Each RF and baseband module has at maximum K pairs of unidirectional links. Therefore, $K \times K$ mesh at maximum can be supported but any combination, including asymmetrical combinations, up to this maximum is allowed.

Figure 2 illustrates a base station configuration with two baseband and three RF modules and a full mesh at RP3.

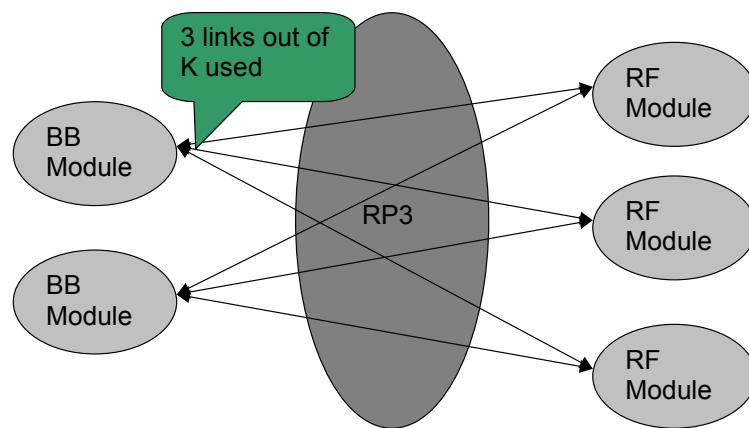


Figure 2: Full mesh connecting two baseband and three RF modules. Each baseband module is connected to every RF module and vice versa.

Figure 3 shows K-by-K full mesh.

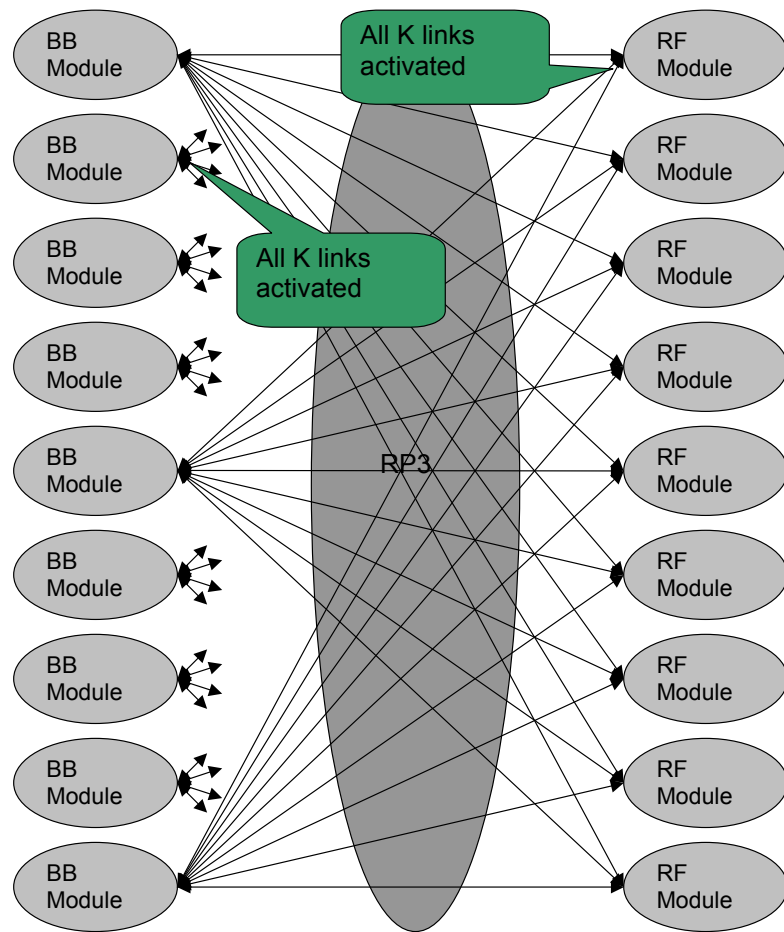


Figure 3: Full mesh connecting K baseband modules to K RF modules. All the connections are not drawn.

3.3.2 Centralized Combiner and Distributor

Assume N baseband and M RF modules in a base station maximum configuration. All links of both baseband and RF modules are connected to a centralized combiner and distributor (C/D) that is located in RP3. For each link, differential signalling is applied. In combining, input samples that are targeted to the same antenna and carrier at the same time instant are added together so that a single output sample stream is formed after which it is transmitted to the desired RF module(s). In distribution, RX sample stream from a RF module is distributed to all or to a subset of baseband modules. At maximum, $K \cdot (N+M)$ pairs of unidirectional links are connected to the combiner and distributor but any number of links below this maximum can be connected to combiner and distributor. For a given base station

configuration, at maximum $\sum_{i=1}^N K_{\text{BB_out}}[i] + \sum_{i=1}^M K_{\text{RF_in}}[i]$ downlink

unidirectional links and $\sum_{i=1}^N K_{BB_in}[i] + \sum_{i=1}^M K_{RF_out}[i]$ uplink unidirectional links are connected to the combiner and distributor. In these equations, $K_{BB_in}[i]$ and $K_{BB_out}[i]$ stand for number of incoming and outgoing links that are implemented to the i^{th} baseband module while $K_{RF_in}[i]$ and $K_{RF_out}[i]$ denote number of incoming and outgoing links that are implemented to the i^{th} RF module. Between any RF or baseband module and the centralized combiner and distributor, unused links shall be disabled for power conservation purposes.

In order to obtain better fault tolerance, a redundant combiner and distributor can be used. In full redundancy, all signals of every RF and baseband module are transferred through main and redundant combiner and distributor modules. Given maximum K pairs of unidirectional links per RF or baseband module, at maximum $K - \lfloor K/2 \rfloor$ pairs of links from any module can be connected to main combiner and distributor and the remaining $\lfloor K/2 \rfloor$ pairs of links can be connected to the redundant combiner and distributor, or vice versa, when redundancy is applied. $\lfloor X \rfloor$ denotes the largest integer number equal to or less than X . Any number of links below this maximum can be connected to a combiner and distributor from a RF or baseband module. In load balancing redundancy, portion of the signals are transferred through the first combiner and distributor while rest of the signals are sent through the second combiner and distributor.

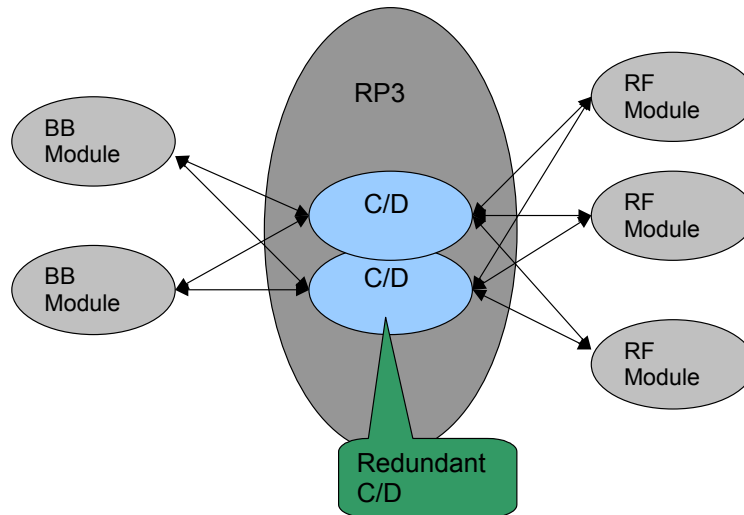


Figure 4: Centralized combiner and distributor (main and redundant) embedded into RP3 interface.

Figure 4 and Figure 5 illustrate centralized combiner and distributor topology with and without redundancy, respectively. Unlike in mesh

approach, there now exist active component(s) in RP3. The same baseband and RF modules shall be used with mesh or centralized combiner and distributor topology.

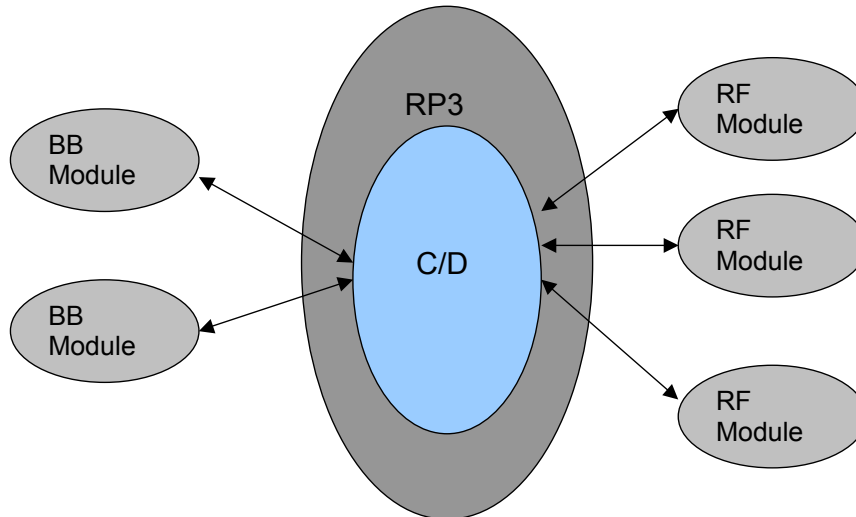


Figure 5: Centralized combiner and distributor embedded into RP3 interface. Redundant C/D is not applied.

3.4 Inter-Cabinet Connections

In very large configurations, a base station may be located in several cabinets and RF-baseband signal transfer between cabinets may be required. RP3 interface shall be used in inter-cabinet RF-baseband data transfers. Thus, differential signalling connections are used as well as the protocol stack defined in Chapter 4. Three topology options exist for inter-cabinet data transfers:

- Inter-cabinet mesh
- Links between bridge modules
- Links between centralized combiner and distributor modules

All these options are described in detail below. Two cabinet case is considered in this section. All the concepts presented can be generalized for X cabinet case where $X > 2$.

3.4.1 Inter-Cabinet Mesh

Figure 6 illustrates the case where a full mesh exists between all baseband and RF modules in dual cabinet base station configuration.

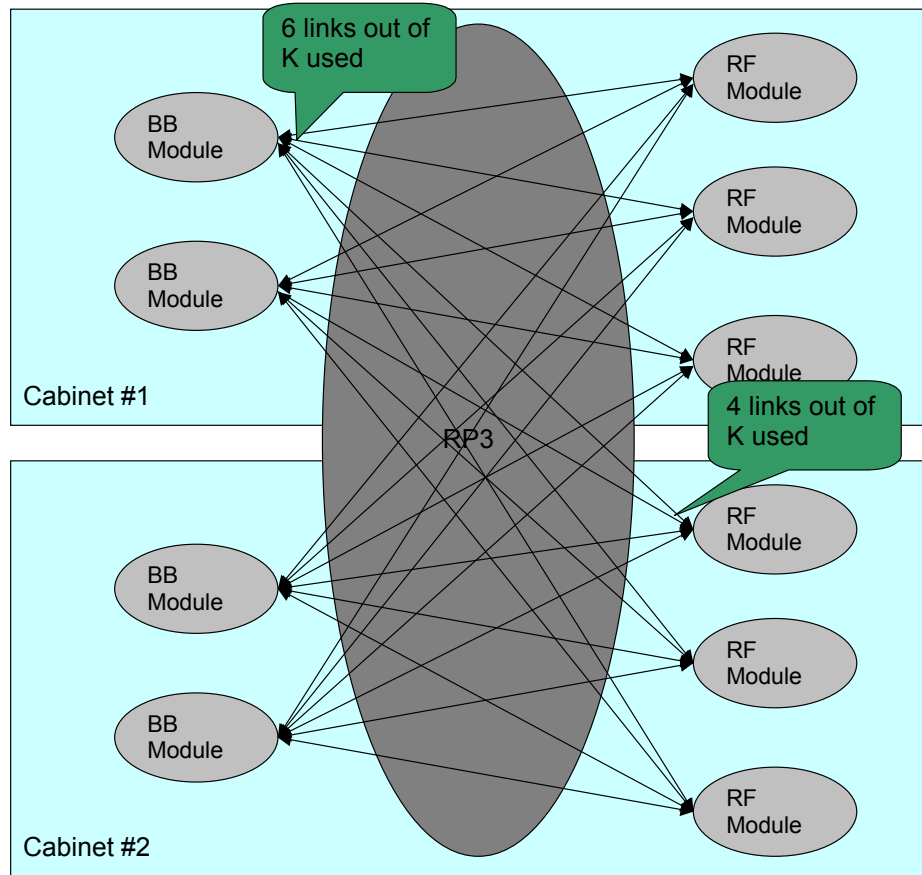


Figure 6: Full mesh between RF and baseband modules of two cabinets.

3.4.2 Connections between Bridge Modules

Figure 7 shows the second option for inter-cabinet communication. Now bridge modules are used that may simply forward data from cabinet to another. Bridge module is typically used in place of a baseband module and it can be used with intra-cabinet mesh or centralized combiner and distributor topologies.

Any baseband module of Cabinet #X can be connected to any RF module of Cabinet #Y when applying the bridge concept. Sufficient bandwidth in Baseband-to-RF links of Cabinet #X is assumed. In most simple implementation, bridge just forwards a set of differential signals from input to output. In a more advanced approach, bridge module is able to interchange data between links.

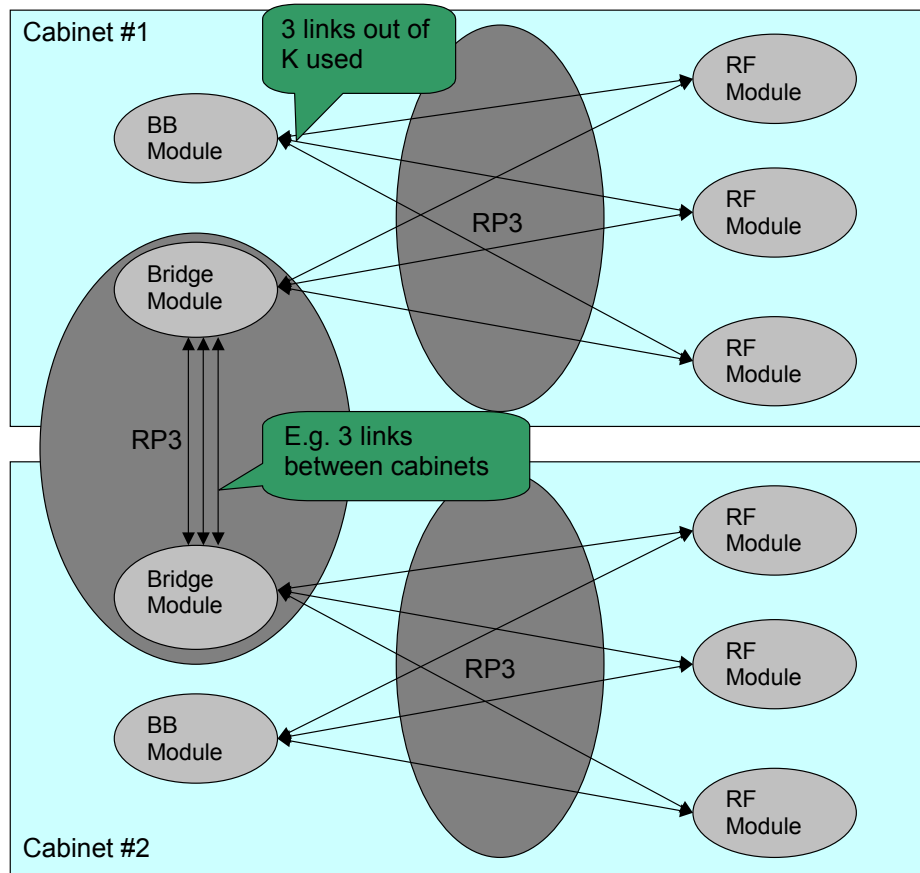


Figure 7: Bridge modules extending RP3 interface to two cabinets. Mesh topology is shown in intra-cabinet RF-baseband connections but also centralized combiner and distributor topology may be applied.

In order to obtain better fault tolerance, a redundant bridge module is typically used. Both the main and redundant bridge modules of the two cabinets shall be connected together.

3.4.3 Connections between Combiner and Distributor Modules

Figure 8 defines third option for inter-cabinet data transfer. When centralized combiner and distributor modules exist in RP3, these modules of different cabinets can be connected together. Both the main and redundant modules of the two cabinets shall be connected together.

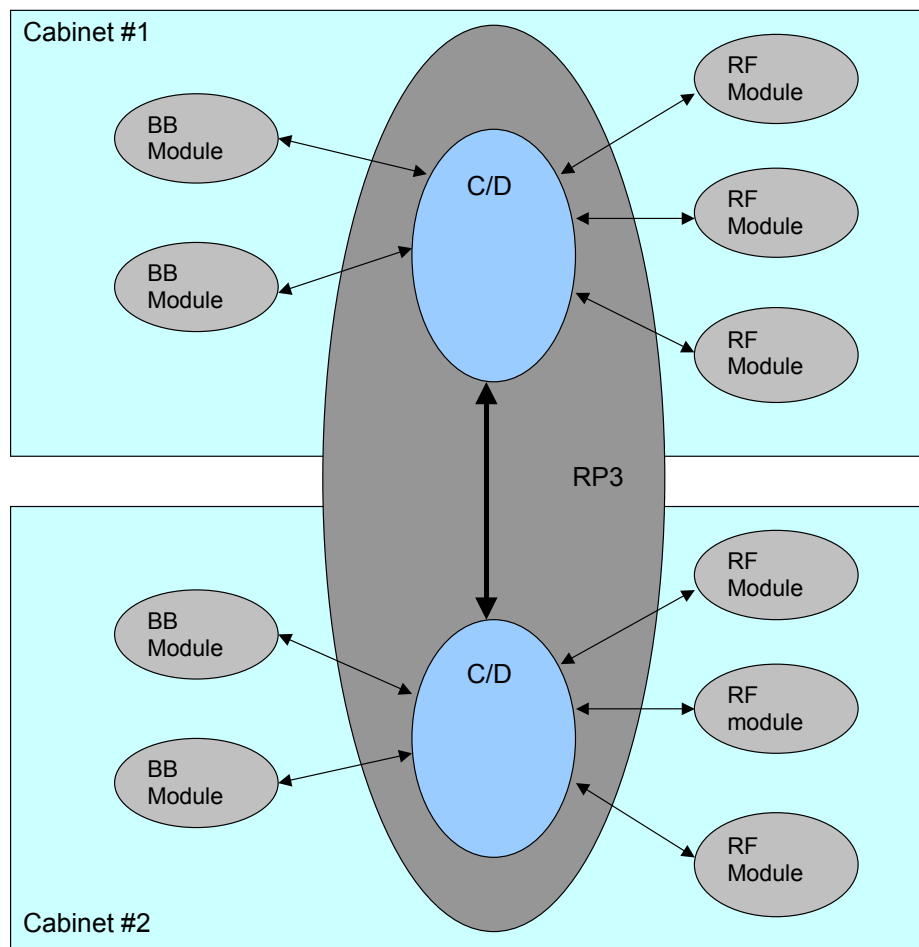


Figure 8: RP3 interface extended over two cabinets by connecting C/Ds together (redundant C/D not applied).

4 Protocol Stack

The RP3 bus interface is a high-capacity, point-to-point serial interface bus for uplink and downlink telecom (user) data transfer and related control. The physical implementation of the bus is based on differential signalling technology. The protocol stack is based on a packet concept using a layered protocol with fixed length messages.

The bus protocol can be considered as a four-layer protocol consisting of

- **Application layer**, providing the mapping of different types of packets to the payload.
- **Transport layer**, responsible for the end-to-end delivery of the messages, which is simply routing of messages.
- **Data link layer**, responsible for framing of messages and message (link) synchronization
- **Physical layer**, responsible for coding, serialization, and transmission of data

This is illustrated below in Figure 9.

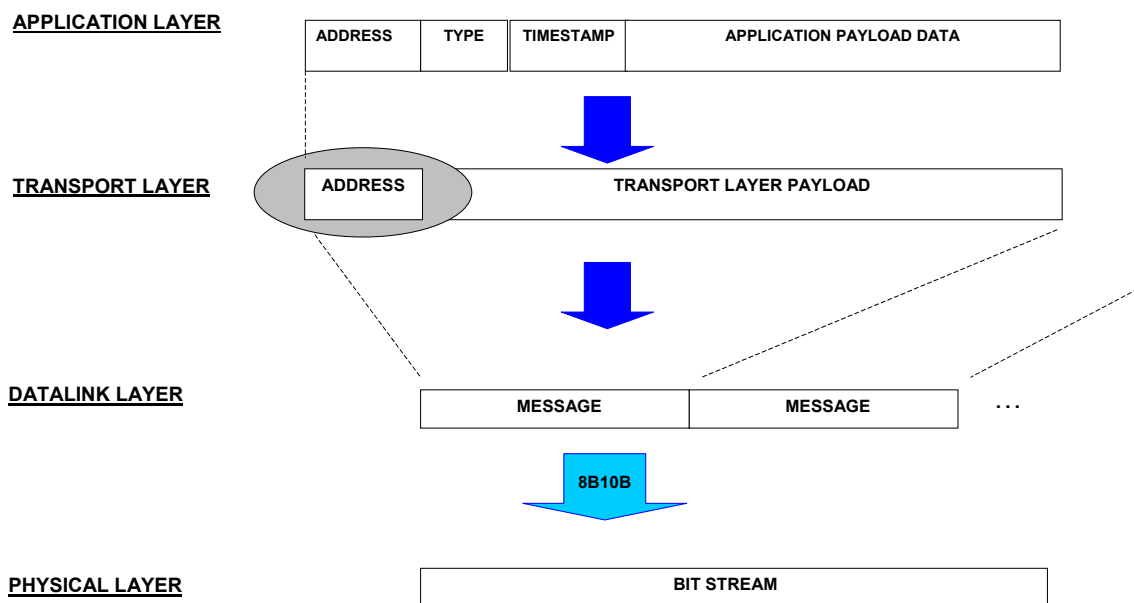


Figure 9: Layered structure of the bus protocol.

4.1 Physical Layer

4.1.1 Electrical Signalling

Refer to Chapter 5 for a detailed specification on electrical characteristics of RP3 interface.

4.1.2 Data Format and Line Coding

8b10b transmission code [1] shall be applied to all data that is transmitted over the RP3 bus. 8b10b transmission coding will provide a mechanism for serialization and clock recovery. Figure 10 illustrates physical layer structure.

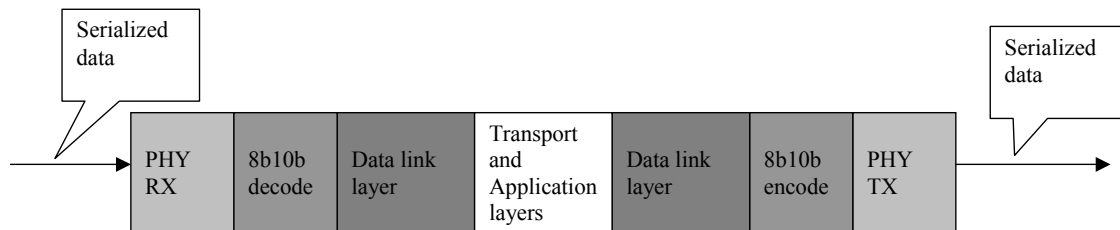


Figure 10: Illustration of Physical layer structure – data flow approach.

Synchronization of physical layer receiver

In the Physical layer receiver, phase adjustments to the incoming signal are automatically done for each receiver port separately. Typically, phase adjustments are done when initialising the connection.

Line code violation detection

Physical layer, the 8b10b decoder, shall detect invalid line codes from the incoming serial bit stream. Each Line Code Violation (LCV), i.e. erroneously received byte, shall be indicated to Data link layer.

Physical layer, the 8b10b encoder, shall transmit K30.7 character to the link when Data link layer indicates that the byte to be transmitted contains an error.

4.1.3 Bus Clock

Physical layer of the bus is frequency and phase locked to a centralised BTS system clock [4]. In every bus node, byte clock for the bus is generated from BTS system clock and it equals to $Bus_line_Rate/10$ when bus line rate is expressed in baud units.

4.2 Data Link Layer

4.2.1 Message Overview

A fixed message format is used for all data that is transferred over the RP3 or RP3-01 (see Section 6) bus. Figure 11 shows the message structure including partitioning of the message into bytes. Each byte of a message is first 8b10b encoded as shown in the figure and then transmitted to a link. 8b10b encoding is part of Physical layer functionality. The leftmost byte of the address field is first transmitted to the link while the rightmost byte of payload is last sent to the link. If data from other busses is transferred over the RP3 or RP3-01, it must be realigned such that MSB is transmitted first as defined in Figure 11.

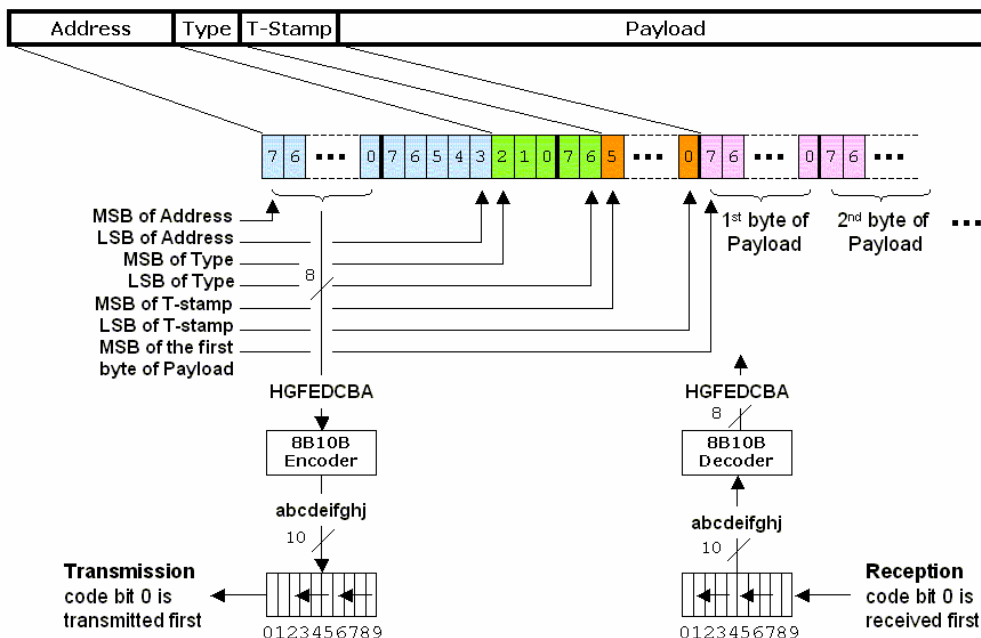


Figure 11: Message format of RP3 protocol stack.

Table 2 defines the size of each field of the message.

Table 2: Size of the message.

Field	Length (bits)
Address	13
Type	5
Time stamp (T-Stamp)	6
Payload	128
Total length	152 bits (=19 bytes)

4.2.2 Frame Structure

The protocol supports only fixed length messages of size 19 bytes as specified in Table 2.

A block of data consisting of M_MG messages, $0 < M_MG < 65536$, and K_MG IDLE bytes, $0 < K_MG < 20$, is called a Message Group (MG). Consecutive Message Groups are transferred over a bus link. Master Frame length is fixed to 10 ms and it is composed of $i*N_MG$, where $0 < N_MG < 65536$ and $i \in \{1, 2, 4\}$, consecutive Message Groups for line rates $i*768$ Mbps. Thus, any of the line rates 768 Mbps, 1536 Mbps, and 3072 Mbps can be applied. Parameters M_MG and N_MG must be selected such that $i*N_MG*M_MG < 2^{32}$ holds. Size of a Message Group equals to $M_MG*19+K_MG$ bytes while Master Frame size in bytes is $i*N_MG*(M_MG*19+K_MG)$.

The M_MG message slots of a Message Group are divided into data and control slots. For a line rate $i*768$ Mbps, the i last message slots of every i^{th} Message Group are control message slots while all other message slots are allocated for data message slots. In a Master Frame, there exist $i*N_MG$ control message slots and Message Group with index $i-1$, where Message Group indices run from 0 to $i*N_MG-1$, is the first Message Group having control slots.

K_MG idle codes K28.5 [1] exist at the end of each Message Group with one exception. Idle codes K28.7 are used to mark the end of a Master Frame, i.e. K_MG consecutive K28.7 codes exist at the end of last Message Group. A set of unique codes is used to mark the end of a Master Frame in order to facilitate reception.

There exists a large set of different Message Group and Master Frame definitions. Parameter set $M_MG=21$, $N_MG=i*1920$, and $K_MG=1$ is recommended to be used for WCDMA, GSM/EDGE, and 802.16 air interface standards while parameter set $M_MG=13$, $N_MG=i*3072$, and $K_MG=3$ is recommended for CDMA.

Figure 12 and Figure 13 Master Frames for WCDMA, GSM/EDGE, 802.16, and CDMA air interface standards for the 768 Mbps line rate ($i=1$).

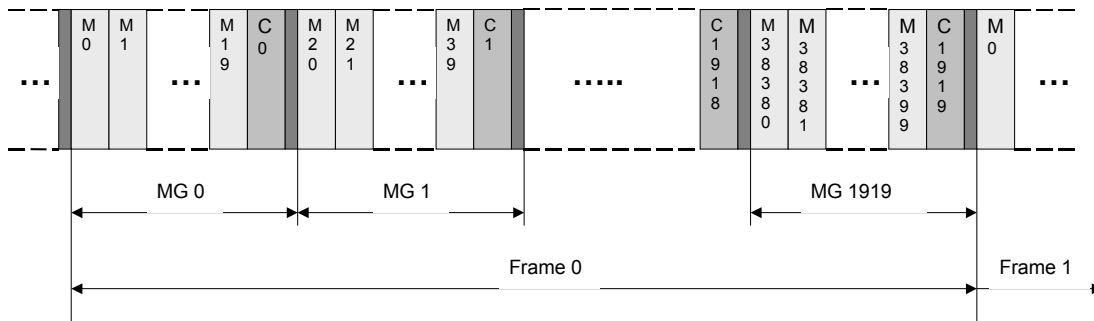


Figure 12: Master frame illustrating the sequence according to which WCDMA, GSM/EDGE, and 802.16 messages are inserted to the bus (parameter set $M_MG=21$, $N_MG=1920$, $K_MG=1$, $i=1$).

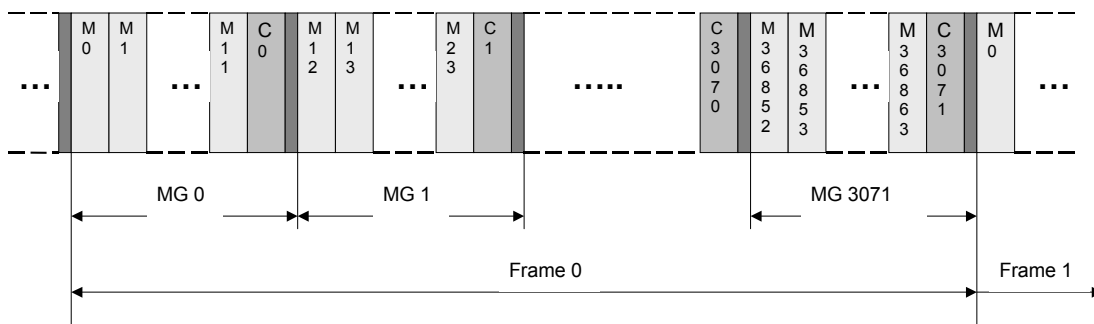


Figure 13: Master frame illustrating the sequence according to which CDMA messages are inserted to the bus (parameter set $M_MG=13$, $N_MG=3072$, $K_MG=3$, $i=1$).

Figure 14 illustrates Message Group structures for WCDMA, GSM/EDGE, and 802.16 air interface standards at all allowed line rates $i \cdot 768$ Mbps, $i \in \{1, 2, 4\}$.

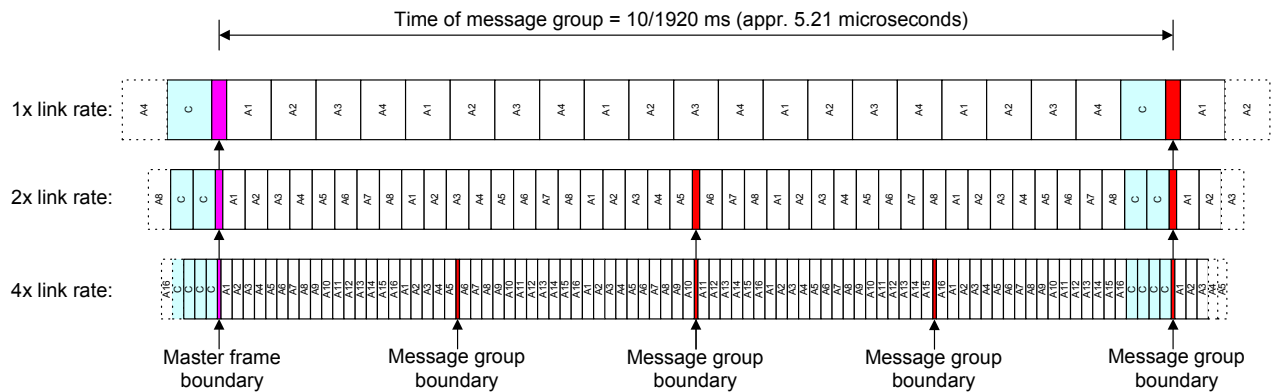


Figure 14: Message Group structures for WCDMA, GSM/EDGE, and 802.16 air interface standards at 768 Mbps (1x), 1536Mbps (2x), and 3072Mbps (4x) line rates. Time span corresponding to a single message group at 768Mbps line rate is shown.

4.2.3 Counters

Master Frame is defined in Section 4.2.2. The Data link layer provides indices of current data and control message slots to upper layers which can then use these indices in the scheduling of message transmissions. Data message slot counter takes values from 0 up to $(i*(M_MG-1)*N_MG)-1$ (refer to Section 4.2.2 for the definition of N_MG and M_MG) while control slot counter runs from 0 to $(i*N_MG)-1$. Both of these counters are 32 bits wide and they count message slots over a Master Frame duration. Both the data and control message slot counters are reset to zero in the beginning of the first data and control slots of the new master frame. As illustrated in Figure 15, the data message slot counter is reset to zero in the beginning of a Master Frame due to leading data message slot while the control slot counter is reset to zero in the beginning of the first control slot of the new master frame.

Master frame timing denotes here the Δ corrected (see Section 4.2.4) Master Frame timing, i.e. Master Frame timing at a transmitter port. This refers to the fact that there exists latency in message transfer over the bus, i.e. the message is seen at slightly different times in separate bus nodes. Counter value X in the figure below identifies the same message slot of a Master Frame in each bus node.

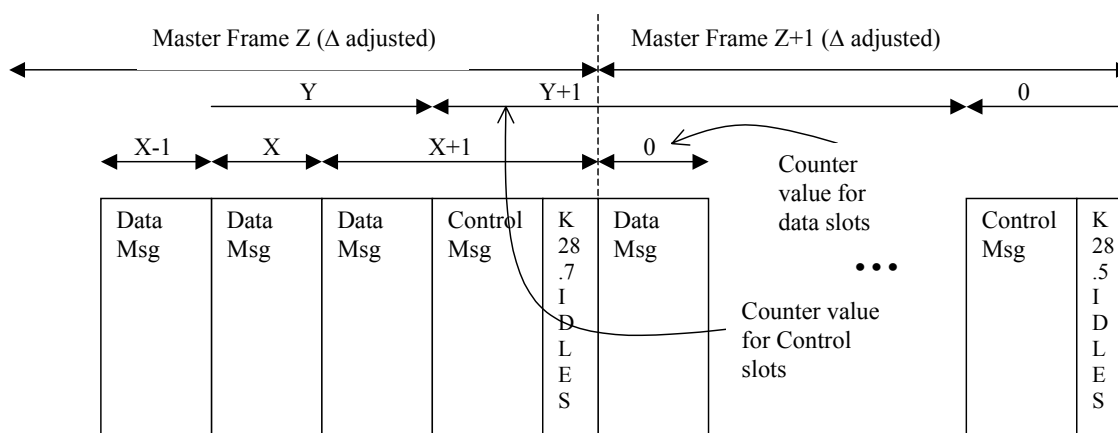


Figure 15: Timing of message slot counters for an example MG and MF definition.

For each bus transceiver (transmitter), message slot counters are activated (counting is started) after the offset parameter Δ (see Section 4.2.4) is available and the state of the transceiver is FRAME_TX (see Section 4.2.7).

4.2.4 Transmission of Frame Structure

Transmission time of Master Frame is synchronised to the RP3 bus frame clock at the output of each bus node. First byte of Master Frame is transmitted at offset Δ from the RP3 bus frame clock tick. In general, a common Δ value is used for uplink transmitter ports; another Δ value is used for all downlink transmitters. In some bus nodes, a specific parameter value is used for each transmitter port.

Parameter Δ fulfils the equation $\Delta = \Pi + D + B + P$, where D stands for processing delay of the receiver module and B indicates the maximum amount of buffering available at each Data link layer bus receiver while P denotes latency across the node; from receiver module to transmission module. Parameter Π is defined in Section 4.2.5 below. Note that the above equation only applies to bus nodes that forward received messages.

Offset values Δ are received at start-up by each bus node and their values are specified in byte-clock ticks. 16-bit two's complement code numbers are used.

Offset value Δ of a transmitter is fixed at run time. Section 4.2.7 defines the process according to which the value of the parameter Δ can be changed.

Figure 16 illustrates Master Frame transmission timing.

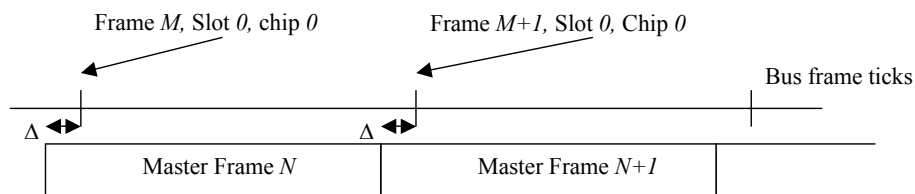


Figure 16: Master Frame is transmitted at an offset to the RP3 bus frame tick in each bus node.

After receiving the parameter Δ , Master Frame timing is valid at the second RP3 bus frame tick. This is due to the fact that Δ may take negative values. In downlink, Δ has negative values while positive values are used in uplink direction.

4.2.5 Reception of Frame Structure

The purpose of Master Frame synchronisation is to minimise buffering need in bus nodes, i.e. to ensure that corresponding message slots are received at the same time at each bus node.

For each bus receiver, synchronisation block indicates the received Master Frame boundary (see Section 4.2.7). An additional offset parameter Π is provided for each receiver that indicates earliest possible time instant when a Master Frame can be received. This time instant, called reference time, is equal to RP3 bus frame clock plus offset Π .

An exact value of Π is provided such that the end of the Master Frame shall be received at the reference time or at maximum MAX_OFFSET byte ticks after the reference time. The default value of MAX_OFFSET equals to four while value eight is optionally allowed (refer to Section 7.1.1 for MAX_OFFSET parameter definition). Target for bus configuration is to have the end of the Master Frame exactly MAX_OFFSET/2 byte clock ticks after the reference time. This can be achieved when the entire RP3 bus (all parameters) is properly configured.

When initialising a bus link, received Master Frame boundary may not hit the allowed MAX_OFFSET+1 bytes wide time window. A false parameter value can cause this situation. Irrespective of the erroneous Π value, bus nodes can perform measurements of the received Master Frame boundary as defined in Section 4.2.8.

An error shall always be indicated to Application layer when received Master Frame boundary is detected outside the allowed MAX_OFFSET+1 byte ticks long window. No error is indicated if the Master Frame boundary is not detected at all. This functionality is

optional in bus nodes that are located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes. When Master Frame boundary is detected outside the allowed window in any bus node, all following data and control messages are rejected by default. Thus, they are not forwarded to output port(s) and they are not summed together with other messages. However, in bus nodes that are located in Remote RF Units (see Chapter 6), transfer of messages is continued irrespective of the location of the Master Frame boundary. Message processing continues normally (assuming that receiver state has remained in FRAME_SYNC state; see Section 4.2.7) after detecting Master Frame boundary in the allowed window.

Value of parameter Π is fixed at run time. By default, the receiver state machine shall be resynchronised (see Section 4.2.7) when updating the value of the parameter Π . Advanced implementations of RP3 may be able to support run-time updating of parameter Π such that RP3 message transmission and reception is continued uninterrupted. In downlink direction, Π will typically take negative values while it has positive values in uplink direction.

Figure 17 illustrates run time (allowed) and measurement windows of received Master Frame.

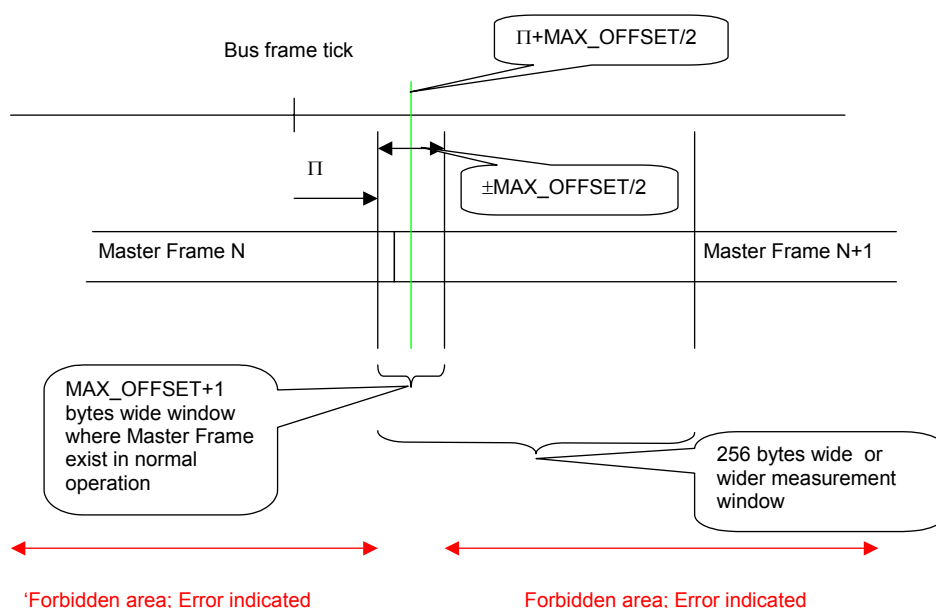


Figure 17: Run time and measurement windows of received Master Frame.

Consider any bus node that has two or more receiver ports. Parameter Δ 's at the transmitting nodes are defined so that difference in received

Master Frame timing at any pair of ports is less than or equal to duration of MAX_OFFSET bus bytes.

Figure 18 illustrates receive and transmit offsets of a Master Frame.

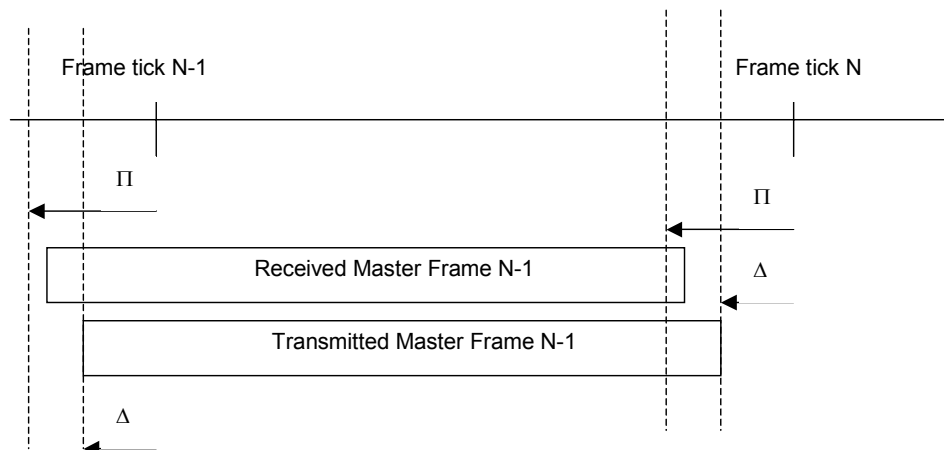


Figure 18: An example of Master Frame timings (downlink direction).

BTS Control and Clock block [2] is responsible of value assignment to parameters Δ and Π of all bus nodes. Figure 19 provides an example of Δ and Π value definition for a very simple intra-cabinet bus network. In the figure, there exists a bus network with three nodes. For clarity, downlink (DL) and uplink (UL) bus connections and corresponding parameter values have been drawn separately. The leftmost node exemplifies bus interface at baseband module while the rightmost node stands for bus endpoint at RF module. Combiner and distributor (C/D) node is at the middle.

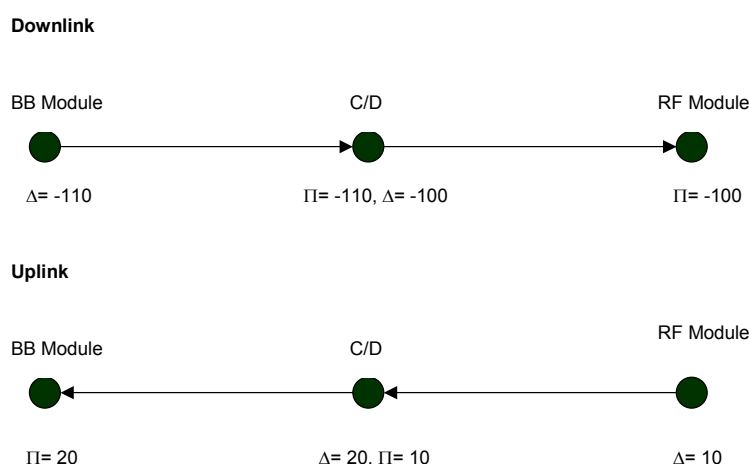


Figure 19: Example of Δ and Π assignments to a bus network.

Negative Δ and Π values are applied in downlink direction in order to have the data early enough at RF module for transmission to the air (refer to timestamp definition in Section 4.4.7 and data mapping to Master Frame in Section 4.4.8 for related information). Capacity of the bus link and processing delay at RF determines the value of Π that shall be applied. Value of Π never equals to zero at RF bus node. Values of Δ and Π at C/D and baseband nodes are determined by taking into account delays over bus links as well as processing delay over C/D. For simplicity, we assume delay of 10 byte clock ticks over the C/D bus node.

In uplink direction, positive Δ and Π values are applied (refer to Sections 4.4.7 and 4.4.8 for related information). Processing delay at RF defines value of Δ at RF module. Other Δ and Π values are determined by delays over bus links and processing delay over C/D bus node.

4.2.6 Empty Message

When there is no message to transmit, i.e. no message has been received from transport layer for a given message slot, the Data link layer of the bus transmits an empty message. Data link layer at the receiver end will reject empty message and, therefore, these messages are invisible to upper protocol layers. Address '111111111111' is reserved exclusively for the empty message. Figure 20 defines the empty message. Address field contains '1' bits while rest of the message contains don't care x bits. Don't care bits can be assigned to either '1' or '0' in message transmission.

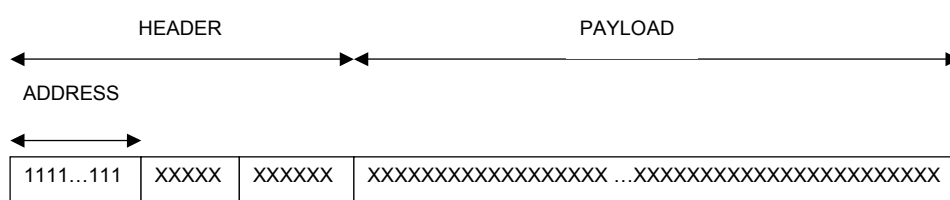


Figure 20: Empty message. The address field consists of thirteen '1' bits while rest of the message contains don't care x bits.

4.2.7 Synchronisation

Physical and Data link layers of the bus must be synchronised before actual data transfer can be started. Synchronisation algorithm can provide information to upper layers regarding the quality of a bus link.

Frequency of byte errors as well as status of frame synchronisation is constantly monitored.

Data Link Layer Synchronisation

The synchronisation algorithm is described in the format of finite state machines. Separate state machines exist for each transceiver.

Separate state machines are provided for transmitter and receiver as shown in the following subsections.

Transmitter

There are three states in the transmitter state machine: OFF, IDLE, and FRAME_TX. On reset, the state machine enters the initial OFF state. In this state, transmission from the Physical layer macro to a bus link is disabled. Thus, nothing is transmitted to the bus.

Application layer controls the transition from OFF state to IDLE state. State is changed when Application layer sets parameter TRANSMITTER_EN equal to 1 and one of the following cases is true: (1) parameter LOS_ENABLE is set equal to 0 meaning that signal LOS (Loss of Signal) from receiver state machine does not have any impact on the transmitter state, or (2) LOS_ENABLE is equal to 1 (LOS has an impact) and LOS is equal to 0 (inactive).

In IDLE state, the transmitter macro continuously transmits K28.5 IDLE based on which the receiver end can obtain sample (byte) synchronisation. Transmitter state machine always remains in state IDLE at least t micro seconds. Value of t is implementation specific and it is large enough to allow Phase Locked Loop (PLL) of the transmitter macro to settle and the interfacing receiver macro to obtain correct sample phase.

Transition from IDLE state to FRAME_TX state is done when Application layer updates (modifies) the value of parameter Δ . If the value of this parameter is not updated when the transmitter is in state IDLE, transition to state FRAME_TX is not done.

The value of the parameter Δ can only be provided in state IDLE. If there exist a need to change the value of Δ during base station run-time, the transmitter shall first be forced to OFF state, then to IDLE after which the parameter Δ can be updated.

In FRAME_TX state, transmission of the valid frame structure is performed (see Section 4.2.2). Valid messages from Application/Transport layer are transmitted as well as empty messages. Transmission of frame structure is activated within 20 ms after the updating of parameter Δ .

In Figure 21, all the states and state transitions are shown. As can be seen from the figure, HW reset or active LOS (Loss of Signal) from receiver state machine may force the state to OFF (transmission disabled).

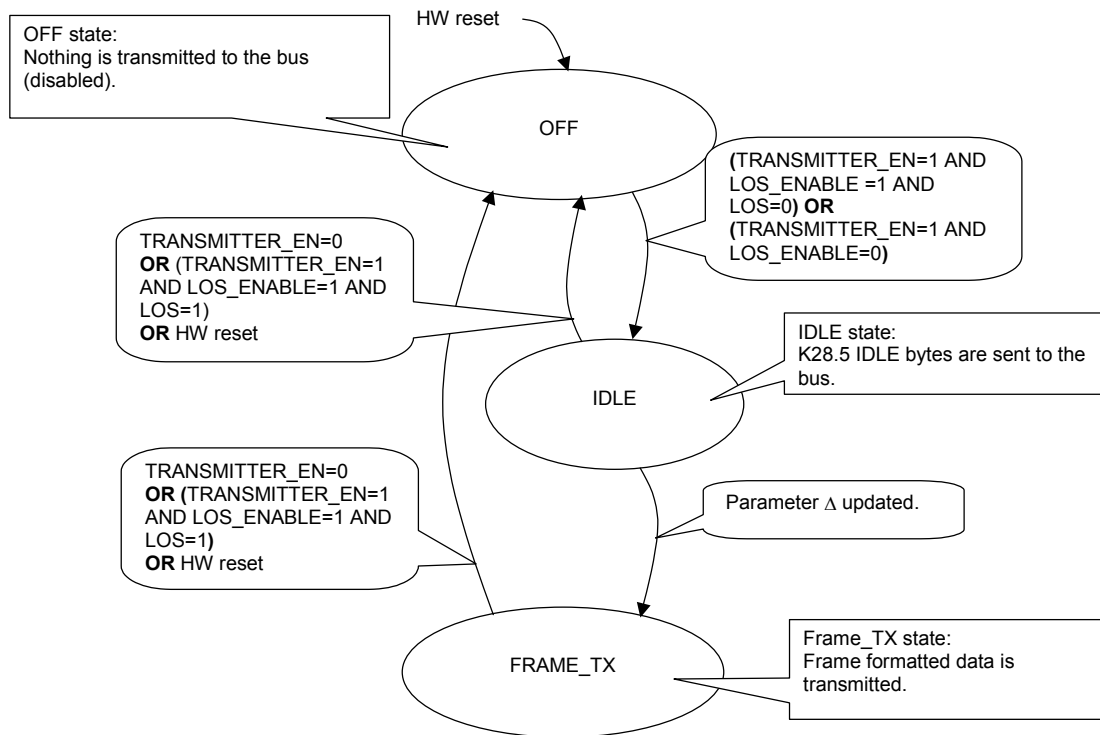


Figure 21: State diagram of the transmitter.

Receiver

As can be seen from Figure 22, receiver state machine consists of four states: UNSYNC, WAIT_FOR_K28.7_IDLES, WAIT_FOR_FRAME_SYNC_T, and FRAME_SYNC. Two of these states, namely WAIT_FOR_K28.7_IDLES and WAIT_FOR_FRAME_SYNC_T, can be considered to form a single logical state called SYNC. The meaning of states UNSYNC, SYNC, and FRAME_SYNC is as follows:

- UNSYNC: Bus link is down. A lot of byte errors are detected.
- SYNC: Bus link is working, i.e. connection exists.
- FRAME_SYNC: Normal operational mode. Frame structure is detected and messages are received.

The receiver state machine uses two separate criteria to determine the quality of a bus link; the first one monitors the byte error rate of the link while the second one monitors the validity of the received frame structure (refer to Section 4.2.2 for a definition of the frame structure). Parameters BLOCK_SIZE, SYNC_T, UNSYNC_T, FRAME_SYNC_T, FRAME_UNSYNC_T control the state transitions.

On reset, the state machine enters the state UNSYNC. State transition to WAIT_FOR_K28.7_IDLES is done if SYNC_T consecutive blocks of bytes have been properly received. In each block, there exists BLOCK_SIZE bytes and a block is considered to be valid if all the bytes were received correctly (no 8b10b decoding errors). Otherwise, the block is considered to be invalid.

Transition from state WAIT_FOR_K28.7_IDLES back to UNSYNC is done if UNSYNC_T consecutive invalid byte blocks are received or in case of HW reset.

Master Frame boundary is indicated by a set of K28.7 IDLE bytes, i.e. it exists at the end of the block of K_MG consecutive K28.7 IDLES.

Transition from WAIT_FOR_K28.7_IDLES to WAIT_FOR_FRAME_SYNC_T is done when K_MG (refer to Section 4.2.2 for a definition of K_MG) consecutive K28.7 idle bytes, i.e. a possible Master Frame boundary, is detected. In state WAIT_FOR_FRAME_SYNC_T as well as in state FRAME_SYNC, Master Frame timing is considered to be fixed (defined by the first set of received K28.7 IDLES).

In WAIT_FOR_FRAME_SYNC_T state, validity of consecutive message groups (see Section 4.2.2) is studied. When FRAME_SYNC_T consecutive valid message groups are received, FRAME_SYNC state is entered. If FRAME_UNSYNC_T consecutive invalid message groups are received, state WAIT_FOR_K28.7_IDLES is entered and search for new set of K28.7 IDLES is started immediately.

State transition from FRAME_SYNC to WAIT_FOR_K28.7_IDLES is done when FRAME_UNSYNC_T consecutive invalid message groups are received and transition from FRAME_SYNC to UNSYNC is done when UNSYNC_T consecutive invalid blocks of bytes are received.

A valid message group stands for a block of $M_MG*19+K_MG$ bytes where the first M_MG*19 bytes are of type data or 8b10b decoding error. Idle codes K28.5 or K28.7 are not allowed. The last K_MG bytes must be either K28.5 or K28.7 idle bytes or a 8b10b decoding errors. Furthermore, the order of the idle bytes matters. In the first $i*N_MG-1$ Message Groups of a Master Frame, all K_MG idle bytes of the Message Group must equal to K28.5 while in the last Message Group of the Master Frame, K_MG idle codes shall equal to K28.7.

Receiver synchronisation state machine has several outputs. Current state of the receiver will be available for Application layer. An interrupt is generated from each state change. Signal LOS (Loss of Signal) is active (has value 1) in state UNSYNC while it is inactive in other states. Synchronisation block indicates also bytes that contain 8b10b decoding error as well as the location of the Master Frame boundary.

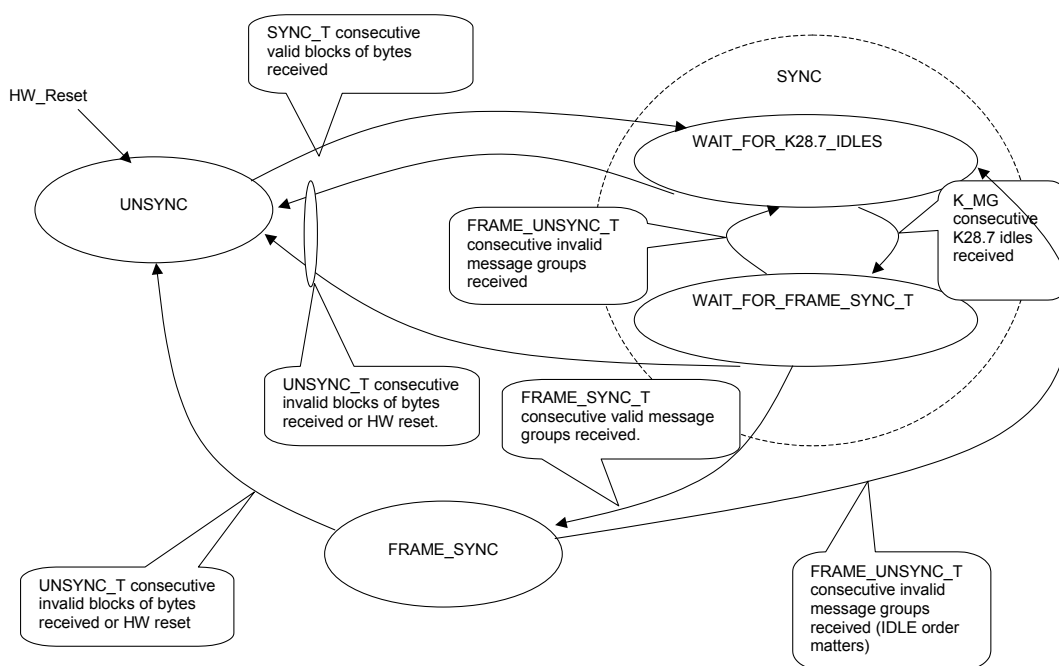


Figure 22: State diagram for the receiver.

Data Link layer shall forward messages to Transport layer only when in state FRAME_SYNC. This will prevent routing of false data from disconnected or otherwise malfunctioning receiver port.

4.2.8 Measurements

In this section, the measurements that are performed by the Data link layer are listed. Currently only timing offsets of received Master Frames with respect to baseband bus clock plus Π are measured (refer to Section 4.2.5). This measurement is optional in bus nodes that are located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes.

To support bus configuration and error recovery, each bus receiver can detect the received Master Frame within a time window that spans 0-255 bytes after the reference time. Also larger measurement windows are allowed. The reference time stands for baseband bus frame clock tick plus offset Π . If the Master Frame offset is not detected during the time window, the measurement is saturated at the maximum counter value (default value is 255). The measurement is activated only in FRAME_SYNC mode (see Section 4.2.7) and the measurement is conducted once per Master Frame.

1

Table 3: Measurements performed by the Physical layer.

Measurement	Register width	Description
Received Master Frame offset	8 bits (default value), positive integer (no sign bit). Wider registers, e.g. time windows, are allowed.	Provided for each receiver separately. Master Frame offset from reference time, i.e. baseband bus frame clock tick plus Π . Value is given in byte-clock ticks. Measurement value is saturated at the maximum counter value (255 is the default value) if Master Frame boundary is not detected. Valid range of values for Master Frame boundary measurement is 0-MAX_OFFSET. Out of range error is indicated (see Section 4.2.5).

2 4.3 Transport Layer

3 Transport layer consists of message router, multiplexer, demultiplexer
4 and summing units. Transport layer is responsible for the end-to-end
5 delivery of messages. All routing of messages is performed at Transport
6 layer. Based on the address of each message, bus nodes forward
7 received messages to destination nodes. Local routing is applied, i.e.
8 each bus node knows only its own output port(s) into which a message
9 needs to be transmitted. Nodes do not have visibility to the entire
10 message paths. These paths are defined by a bus control entity, Bus
11 manager, when booting up the bus.

12 The address field, which is used to route the data to its destination
13 point, occupies the first 13 bits of the message. The remaining part of
14 the message, including type, timestamp, and payload, is passed
15 transparently by the Transport Layer.

16 4.3.1 Overview of Transport Layer

17 In general, communication networks consist of bi-directional links (or
18 unidirectional links in opposite directions) that connect nodes. In each
19 node, the same routing algorithm is applied to all received messages. In
20 an alternative approach, a bi-directional network is separated into two
21 unidirectional networks that operate independently. When messages
22 need to be transferred between these unidirectional networks, they
23 must go across Application layer. Physical and Transport layers of the
24 two networks operate independently. In a hybrid network concept,
25 received messages in all bus nodes are divided into two groups and
26 separate routing algorithms are applied to these groups. Messages may
27 be classified, e.g., based on the direction of the received messages.

The proposed bus protocol can be used in all above-mentioned network concepts. The hybrid approach is proposed with downlink and uplink networks, and separate routing tables are used for uplink and downlink messages.

Figure 23 illustrates Transport layer with a common message router for all received messages. External interfaces of Transport layer are shown including ports between Application and Transport layers as well as between Transport and Data link/Physical layers. All messages between protocol layers are transferred over these ports.

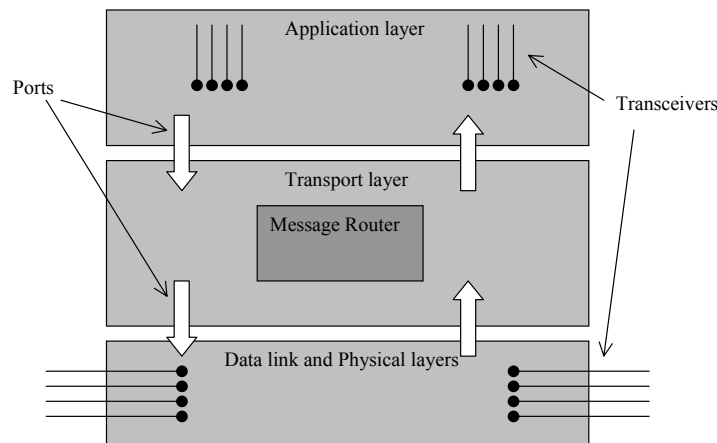


Figure 23: Transport layer with a common message router for all received messages.

When a bus node receives a message from another node, the message is first received by a transceiver at Physical and Data link layers. Then the message is sent to Transport layer, which determines the output transceiver with the help of a routing table. Assuming that transceiver at the Data link/Physical layer is targeted, the message is forwarded back to Data link layer for transmission to the next node. If the payload of the message is processed in the bus node, Transport layer will forward the message to Application layer based on the address of the message. Application layer may send the message back to the bus after processing.

Transport layer operates in a similar manner for all received messages whether they are received from Data link/Physical or from Application layers.

Figure 24 presents functional blocks of Transport layer where a dedicated message router is used for downlink and uplink messages. Application layer must indicate through parameters which transceivers, especially receiver ports of transceivers, are connected to downlink message router and which use the uplink router. Note that both message routers can forward messages to the transmitter port of any transceiver.

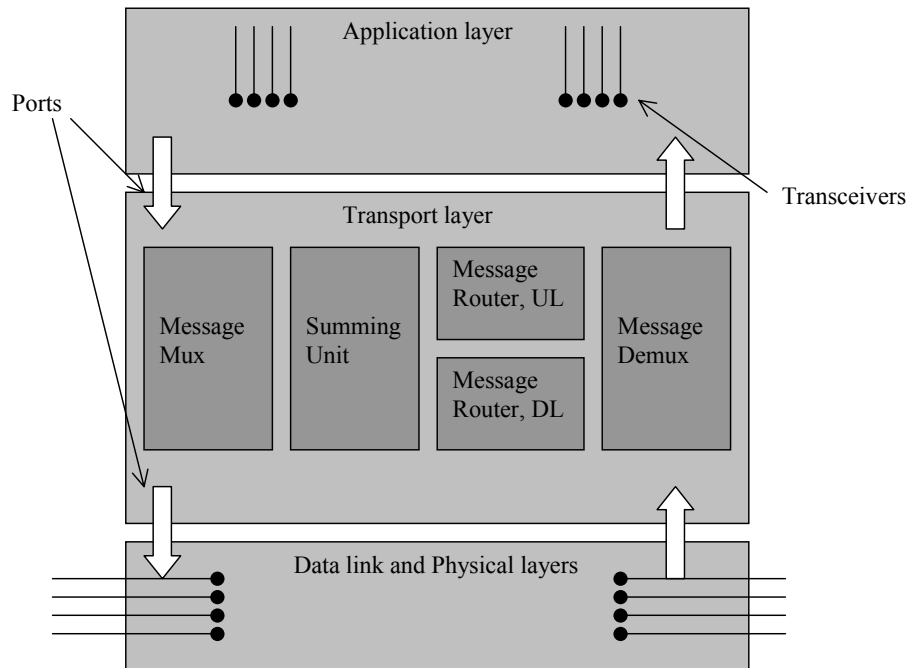


Figure 24: Transport layer with dedicated downlink and uplink message routers. Also message multiplexer, demultiplexer, and summing unit is shown.

Message multiplexer performs parallel to serial conversion of messages, i.e. it time interleaves messages from two or more input RP3 links into an output RP3 link. Message demultiplexer performs the opposite operation to message multiplexer.

The summing unit, which is located in front of each transmitter port of a transceiver, adds together payloads of messages. Summing is performed when more than one message should be transmitted simultaneously to the output port.

Physical and Data link layers, as well as message router and summing unit at Transport layer, operate as fast as possible, i.e. messages are not buffered. Thus, message slot is never altered by these functional blocks. Message multiplexer and demultiplexer may perform line rate conversions due to which they may need to have buffers of length few messages.

In the following sections, all functional blocks of the transport layer are described in detail.

4.3.2 Message Format – Address Field

The address controls the routing of each message. In downlink direction, i.e. from baseband to RF, all message transfers are point-to-point, and the address identifies the target node. Both multicasting (point-to-multipoint) and point-to-point message transfers are applied in uplink direction, i.e. from RF to baseband. Uplink antenna sample data as well as some measurement results may require multicasting; all other message transmissions in uplink direction are typically point-to-point.

In networks where bus nodes apply the same routing algorithm to all received messages, each multicast address must be unique. This is undesirable because address space is consumed. When separate routing algorithms are applied for downlink and uplink messages, source node address of the message can be used as the multicast address. This concept shall be used.

The address field is divided into two sub-addresses, the node address and the sub-node address as illustrated in Figure 25.

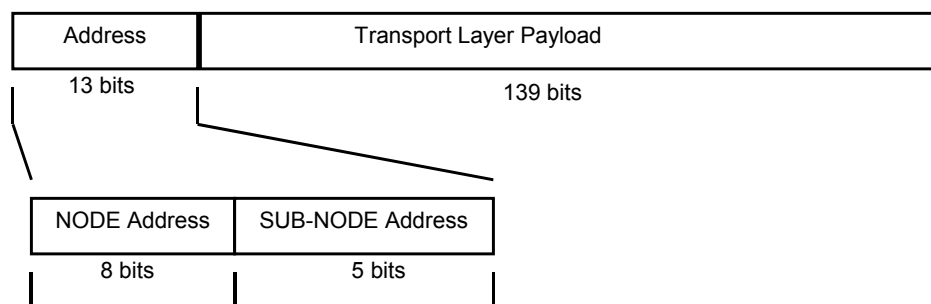


Figure 25: Address sub-fields.

Node and sub-node address fields are used in a hierarchical addressing scheme where the node field is used to uniquely address a specific bus node, i.e. baseband design block, and the sub-node address is used to identify the specific module within the design block. The node address size of 8 bits allows 256 baseband design blocks to be addressed, with up to 32 modules addressed with the 5 bits of sub-node address.

Node address does not necessarily stand for the address of a physical device such as ASIC (Application Specific Integrated Circuit). A device may have one or more node addresses and the nodes may have varying number of active sub-node addresses. For example, in an ASIC that holds both modulator (up conversion) and channelizer (down conversion) design blocks, the blocks typically have separate node addresses.

The general control block of a node, if applicable, is typically addressed using sub-node address 00000.

Reserved addresses

Address '00000000xxxxx', where 'x' stands for either '0' or '1' bit, is reserved for initial booting of the bus network. Thus, node address '00000000' can be used only as default boot up address. It cannot be assigned permanently to any node.

Address '111111111111' (1FFFh) is reserved for the empty message. Therefore, physical layer will delete all received messages with an all-ones address. However, addresses '1111111100000'-'1111111111110' (1FE0h-1FFEh) can be used, i.e. node address '11111111' (FFh) is valid.

4.3.3 Message Router

Figure 26 illustrates the functionality of the message router. The 13 bit input address of a message is first processed by a mapping unit which typically selects only a subset of the input bits. For example, the node address may only be selected. Refer to Section 7.1.3 for a description of the input parameters of the mapping unit. The transformed address is then used as an index to a routing table, which contains indices of the transceivers into which the message must be transmitted. Note that Message Router shall not change the content of any message. The transformed address is just a temporary parameter used by the router.

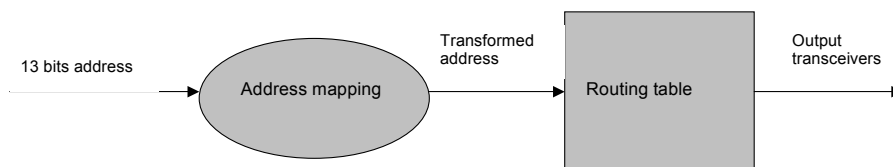


Figure 26: Functionality of message router.

An example of a routing table is given below. In the table, there is a bit vector (row) that corresponds to each transformed address. In the example, two bits wide transformed address is used. Length of the bit vector equals to the number of transceivers that exist in the node. Bit '1' means that the message must be forwarded to the corresponding transceiver while '0' prohibits message transmission. Least Significant Bit (LSB) of the bit vector stands for transceiver of Index 0.

As an example, consider a message with transformed address 10 (2 in decimal number). This message is transmitted by transceivers having indices 1 and 2.

Table 4: An example of a table.

Transformed Address (input)	Transceivers (output)
00	(MSB) 000001 (LSB)
01	000010
10	000110
11	100001

4.3.4 Message Multiplexer and Demultiplexer

Message multiplexer performs time interleaving of messages from N , $N > 1$, input RP3 links to a single output RP3 link as illustrated in Figure 27. The multiplexer shall forward messages from the input links to the output link such that valid RP3 Message Group and Master Frame formats exist at the output link. The mapping algorithm used by the multiplexer shall remain the same for all time and it is set up at bus configuration time. The definition of the frame structure in Section 4.2.2 suggests the use of a round robin algorithm in message multiplexing.

The message multiplexer shall repeatedly perform a re-arrangement of messages from the input links to the output link over a time period that corresponds to the duration of a single message at 768Mbps line rate. Thus, messages from input links k , $0 \leq k < N$, with message slot indices $M_k * i + j_k$ shall be forwarded to messages slots $M_{out} * i + j_{out}$ at the output link, where the line rate of input link k equals to $M_k * 768\text{Mbps}$, the line rate of output link equals to $M_{out} * 768\text{Mbps}$, $M_k \in \{1, 2, 4\}$, $j_k = \{0, \dots, M_k - 1\}$, $M_{out} \in \{1, 2, 4\}$, and $j_{out} = \{0, \dots, M_{out} - 1\}$. Index i , $0 \leq i < N_MG * M_MG$, runs over all message slots of a Master Frame at 768Mbps line rate. All or only a subset of the available input messages are forwarded to the output.

The order according to which messages are mapped from input links to output link can be defined in a format of a multiplexing table. This table, which is actually a vector, consist of M_{out} elements $E_0, \dots, E_{M_{out}-1}$ each $E_{i_{out}} = (D, k, j_k)$ defining an input link and message slot from which the message is copied to the corresponding output message slot j_{out} . Parameter D is set equal to '1' when no input message is copied to that position, i.e. an empty message will be transmitted. Otherwise, $D = '0'$.

Table 5 - Table 8 define mandatory multiplexing algorithms for a set of multiplexing configurations using the format of multiplexing tables.

1 *Table 5: Multiplexing table for the case where all messages from four*
2 *768Mbps links are multiplexed to a single 3072Mbps link.*

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	0, 3, 0

3 *Table 6: Multiplexing table for the case where all messages from two*
4 *1536Mbps links are multiplexed to a single 3072Mbps link.*

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 1, 1

5 *Table 7: Multiplexing table for the case where all messages from one*
6 *1536Mbps link and two 768Mbps links are multiplexed to a single*
7 *3072Mbps link.*

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 2, 0

8 *Table 8: Multiplexing table for the case where all messages from two 768Mbps*
9 *link are multiplexed to a single 1536Mbps link.*

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0

Table 9 illustrates a case where messages from three 768Mbps links are multiplexed into a 3072Mbps link.

Table 9: Multiplexing table for the case where all messages from three 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	1, 0, 0

The message demultiplexer performs an inverse operation to the multiplexer, i.e. the output link in the above equations is considered as the input link and input links become output links.



Figure 27: Illustration of message multiplexer.

4.3.5 Summing Unit

Summing unit is located in front of each transceiver, the transmitter port, and all transmitted messages pass through it. When a single message per message slot is to be transmitted, Summing unit forwards the message unaltered to the transceiver. In other words, summing unit will not examine the contents of the message. When two or more messages are targeted to the same message slot and transceiver, Summing unit generates a single output message from the input messages as follows. Header for the output message is copied from one of the input messages. Headers of the input messages should be equal, so any of the messages can be selected. An error is indicated to

and the entire bus uses two's complement code numbers with sign extension. In the summing, saturating arithmetic is used in order to mitigate possible overflows.

As an example, consider two messages each containing four samples. Output message (4, 1, -1, 7) is obtained when performing pointwise sum of real valued messages (3, -1, 5, 4) and (1, 2, -6, 3). Only payload of messages is considered here.

Summing unit is typically activated only for WCDMA, CDMA, and 802.16 data messages. Message collision occurs for example when baseband GSM/EDGE samples are added together. Summing unit detects message collisions by analysing headers of input messages. As an input parameter SUMMING_ALLOWED_FOR_TYPE (see Section 7.1.3), Summing unit receives a list of message types that may be added together. An error is indicated and message transmission is hindered when messages with improper type should be added together. Specifically, in case of message collision, Physical layer should send an empty message due to hindered message transmission but it is also acceptable to transmit one of the colliding input messages to the bus.

Summing unit performs also bit-by-bit comparison of all headers and checks that they are equal.

Only messages of type WCDMA/FDD, WCDMA/TDD, CDMA2000, and 802.16 (see Table 11) may be summed together. Two or more messages of the same type can be added together. A message collision is reported in all other cases.

As an example, SUMMING_ALLOWED_FOR_TYPE = '0000000000000000000000001001100' enables summing of WCDMA/FDD, WCDMA/TDD, and CDMA2000 messages.

Figure 28 illustrates functionality of the Summing unit. In this example, three input messages are shown but K input messages need to be supported.

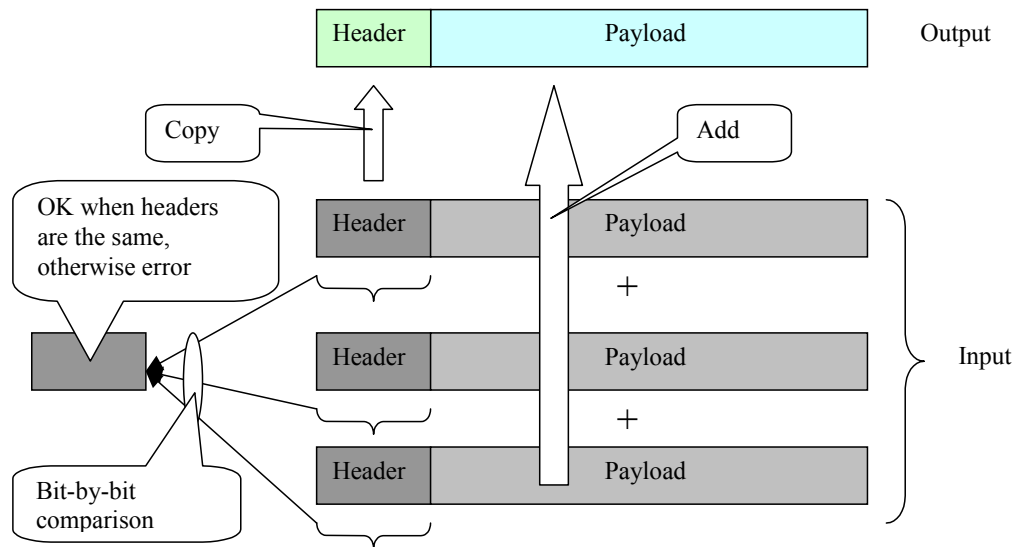


Figure 28: Functionality of Summing unit. Type check of input messages is not shown.

4.4 Application Layer

Application layer represents the user of the protocol and it maps different types of control and data into the payload. The application layer is also responsible for the insertion of the message header: address, type, and timestamp fields.

From bus protocol point of view, Application layer is divided into two parts: air interface applications and bus functions. Major portion of Application layer consist of air interface applications, which are isolated from the bus by "Bus Interface" part. The Bus Interface contains functions that prepare data for transmission over the bus. Also transmission and reception of messages is included. In this section, Bus Interface functionality is described.

4.4.1 Addressing

Application layer will generate message packets with the multicast or point-to-point address in the address field. Refer to Section 4.3.2 for details.

4.4.2 Paths

All data transfers over the bus are performed over paths. Path concept is introduced in order to decouple air interface applications from bus protocol and also to formalise bus configuration process.

A path consists of a set of bus links and message slots that are reserved for data transmission. Bus links connect the source and target nodes together and they are defined by the routing tables. Depending on the bandwidth needed for data communication, an appropriate number of message slots per Master Frame are reserved for the path. Bus manager will provide exact definitions of all paths through the bus. Paths are defined so that message collisions do not exist.

Paths are fixed, i.e. message transfer between any two nodes is always done over the same bus links using pre-specified message slots. Paths are defined before bus initialisation, i.e. message transfers over the bus are deterministic. In case of run-time BTS reconfiguration, paths may need to be modified, added or deleted. Transport layer supports run-time modification of routing tables with minimal corruption of messages. Bus nodes also support run-time modification of message transmission rules but this may be service affecting.

The path taken by a message is determined by the address in the message and the routing tables set up in the bus nodes by the Bus manager.

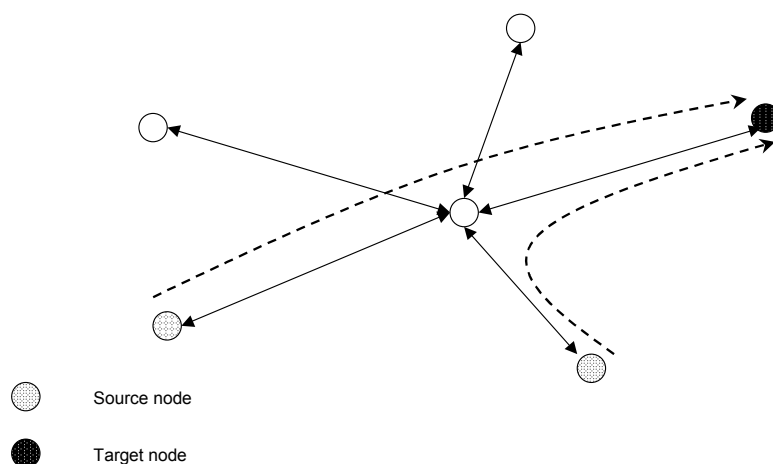


Figure 29: Arbitrary bus configuration with two paths. Message slots are not shown.

4.4.3 Message Transmission Rules

For each path, Bus manager provides detailed rules for message transmission. Rules for paths utilizing data and control message slots are provided separately. As stated in Section 4.2.3, Data Link layer of the bus provides counter values for data and control message slots. Transmission of messages is done with respect to these counters.

There exist two layers of message transmission rules. The rules of the lower layer utilize modulo computation over message slot counters to define RP3 virtual links and their use is mandatory. The rules of the higher layer, which are optional, define paths within RP3 virtual links utilizing bit maps. When the higher layer rules are not used, RP3 virtual links equal to paths.

At the lower layer, message slots for each RP3 virtual link are specified by the pair of numbers (I (Index), M (modulo)) such that equation $MessageSlotCounter \text{ modulo } M = I$ holds. In case of a path using data message slots, $MessageSlotCounter$ runs from 0 up to $(i*(M_MG-1)*N_MG)-1$ while it takes values from 0 up to $(i*N_MG)-1$ in case of control message slots.

As an example, consider transmission of WCDMA data over RP3. For WCDMA, as well as for CDMA, message transmission rules of the lower layer are only used. Assume that a message transmission rule (1, 4) has been provided to a path which uses data message slots, i.e. the Index is equal to 1 while the modulo is 4. This rule states that the node can transmit messages to data message slots having indices 1, 5, 9, 13, 17, ...

At the higher layer, Dual Bit Map concept is applied where two bit maps with maximum lengths of 80 bits (Bit Map 1) and 48 bits (Bit Map 2) are used. The actual lengths of the bit maps are indicated by parameters $Bit_Map_1_Size$ and $Bit_Map_2_Size$. The first bit map Bit_Map_1 is applied $Bit_Map_1_Mult$ times after which the second bit map Bit_Map_2 is used once. The procedure then repeats and reuses the first bit map $Bit_Map_1_Mult$ times. A parameter X specifies the number of antenna-carriers that fits into an RP3 virtual link. Refer to Table 10 for the definition of all parameters of the dual bit map method.

The Dual Bit Map algorithm is the following. Select a unique index J for all the X signals (antenna-carriers) that are being transmitted such that $0 < J \leq X$ holds. Start reading the bit map, Bit_Map_1 , from the most significant bit. If the bit equals to 0, X consecutive message slots from the RP3 virtual channel are available for data transmission. Send one message worth of data from each of the X signals (antenna-carriers) in the order specified by indices J . If the value of the bit is 1, $X+1$ consecutive message slots from the RP3 virtual channel are available for data transmission from which X first ones are used for the X antenna-carriers, message mapping done in the order indicated by indices J , while the last slot of the message block is used to transfer

other messages, e.g. Ethernet or Empty messages. The algorithm continues by repeating the above procedure for the next bit of the bit map.

Currently, parameters of the Dual Bit Map algorithm are defined only for 802.16 data in Appendix 0. Use of these higher layer rules for 802.16 is mandatory in downlink direction when the Summing Unit (see Section 4.3.5) is activated for type 802.16 (see Table 11). In uplink direction, use of these rules is optional. Lower layer rules, i.e. the modulo rules, are mandatory both in downlink and uplink directions.

Table 10: Definition of the parameters of the dual bit map concept.

Parameter	Definition
X	The maximum number of antenna-carriers that will fit into a given virtual RP3 link
Bit_Map_1_Mult	Number of times the first bit map is repeated
Bit_Map_1	Value of the first Bit Map in hexadecimal number. The Bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_1_Size	Size of the first Bit Map (number of bits)
Bit_Map_2	Value of the second Bit Map in hexadecimal number. The bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_2_Size	Size of the second Bit Map (number of Bits)

Figure 30 illustrates 802.16 data transmission into RP3 virtual link using the Dual Bit Map algorithm. Three OFDMA antenna-carriers with 8.75MHz channel bandwidth are mapped into RP3 link. In this example, we assume that the whole RP3 link with 1536 Mbps line rate is allocated for 802.16 data, i.e. the RP3 virtual channel is specified by parameters (0 (index), 1 (modulo)).

At node initialisation, the Bus manager will provide message transmission rules for the end nodes of the bus. Updated rules are provided during run-time if needed; for example, in case of BTS reconfiguration.

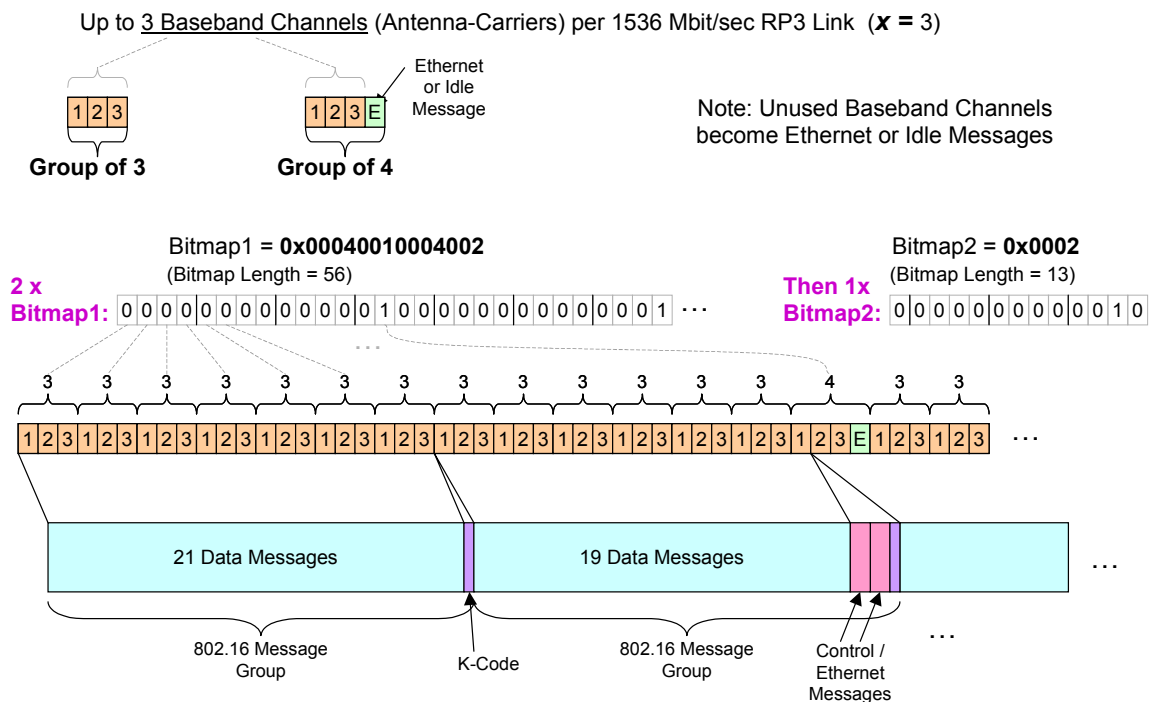


Figure 30: Illustration of 802.16 data transmission into RP3 link using Dual Bit Map algorithm.

4.4.4 Bus Manager

Bus Manager is responsible for the configuration of the bus. Bus Manager is typically located at Control and Clock Module (CCM) and it is a function of the BTS Resource Manager. When the configuration for the BTS modules is known (the number of antennas and carriers etc), the Bus Manager configures the bus accordingly.

4.4.5 Buffering Requirements

Physical, Data link, and Transport layers of the bus perform minimal buffering, i.e. they process messages immediately when received. Buffers having size of few bytes exist at the Data link layer in order to compensate for propagation delays (see Sections 4.2.4 and 4.2.5).

At Application layer, messages need to be buffered because the bus will serialise messages and data. Consider e.g. WCDMA application where data from parallel sources, such as digitised samples from antennas, are transmitted over the bus in consecutive messages. Buffers are needed both in the transmitter and receiver ends in order to slice the continuous data stream into discrete messages and vice versa. At maximum, a double buffering scheme is used in WCDMA with four chips of data per buffer. The same double buffering concept is used

also for CDMA data. A buffer of size six messages is required for each 802.16 signal (antenna-carrier) in order to compensate the jitter caused by message transmission (refer to Section 4.4.3 for the definition of message transmission rules). In GSM/EDGE applications, entire time slot bursts are typically buffered at Application layer and, therefore, serialisation of data on the bus has minor impact.

4.4.6 Message Format – TYPE Field

Application layer is responsible for defining the type of the message. The TYPE field identifies the content of payload data. The following table presents the possible payload types.

Table 11: Content of type field.

Payload data type	Content of Type field
Control	00000
Measurement	00001
WCDMA/FDD	00010
WCDMA/TDD	00011
GSM/EDGE	00100
TETRA	00101
CDMA2000	00110
WLAN	00111
LOOPBACK	01000
Frame clock burst	01001
Ethernet	01010
RTT message	01011
802.16	01100
Virtual HW reset	01101
Currently not in use	01110-11111

Most of the TYPE values presented above are self-explanatory. LOOPBACK messages are used to monitor link integrity.

4.4.7 Message Format – TIMESTAMP Field

The timestamp field relates the payload data to a specific time instant.

Consider a block of WCDMA or CDMA2000 antenna samples that exist in the payload of a message. In uplink direction, time stamp identifies the time instance when the last sample of the message was available at the output of the channelizer block (down converter, FIR filter). In downlink direction, time stamp defines the time instant when the first sample of the payload must be inserted into the modulator (up converter, FIR filter). Reference time is the WCDMA or CDMA2000 frame clock of the BTS.

The WCDMA time stamp is calculated as

$$TIMESTAMP = (CHIP\ NUMBER\ IN\ SLOT / 4) \text{ MOD } 64$$

where CHIP NUMBER IN SLOT stands for the chip Index of a WCDMA time slot. In UL and DL directions, CHIP NUMBER denotes the time Index of the last and first chip (sample) of the message, respectively.

In WCDMA, there exist 100 frames per second and each frame contains 15 time slots. Altogether, there exist 1500 time slots per second while every time slot consists of 2560 chips indicating that CHIP NUMBER IN SLOT takes values between 0 and 2559.

Computation of CDMA2000 time stamp is done analogously to WCDMA time stamp computation, i.e. $TIMESTAMP = (CHIP\ NUMBER\ IN\ SLOT / 4) \text{ MOD } 64$.

Time stamp computation for 802.16 applies modulo over I&Q sample index, i.e. $TIMESTAMP = (SAMPLE\ NUMBER\ IN\ FRAME / 4) \text{ MOD } 64$. For GSM/EDGE in downlink direction, the most significant bit of the timestamp is used to identify the first packet in the timeslot, with a logic '1' identifying the first, with subsequent packets set to a logic '0'. The remaining 5 LSBs of the timestamp represent a count reflecting the packet number with reference to the first packet in the timeslot. The count will wrap-around, but the MSB provides a unique identification of the first packet. Therefore, time stamps of messages containing first samples of a time slot are 100000, 000001, 000010, 000011, 000100, etc.

In the GSM/EDGE uplink direction, the same concept as that of the downlink direction is applied with one exception. The MSB is equal to '1' during the four first messages of a time slot.

4.4.8 Message Format – PAYLOAD Field

The payload represents the content of the message with the type field defining whether the payload contains control, measurement, antenna sample, or some other data. The payload size is fixed at 16 bytes and, from Physical and Transport layer point of view, is considered to be always full. It is the responsibility of Application layer to map data to the payload.

The following sections detail how Application layer maps data into the payload for the different data types. It is intended that data packets are only sent when there is sufficient data to fill them as defined in the following. The only exception is the last packet of the timeslot in GSM/EDGE mode where full amount of data may not be contained.

4.4.8.1 WCDMA Downlink Data Mapping

The WCDMA downlink data stream has a chip rate of 3.84 Mcps with an I&Q data format each of 16 bits giving 4 bytes per chip. This allows 4 consecutive chips of a single WCDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. Two's complement code is used to represent both I and Q sample values.

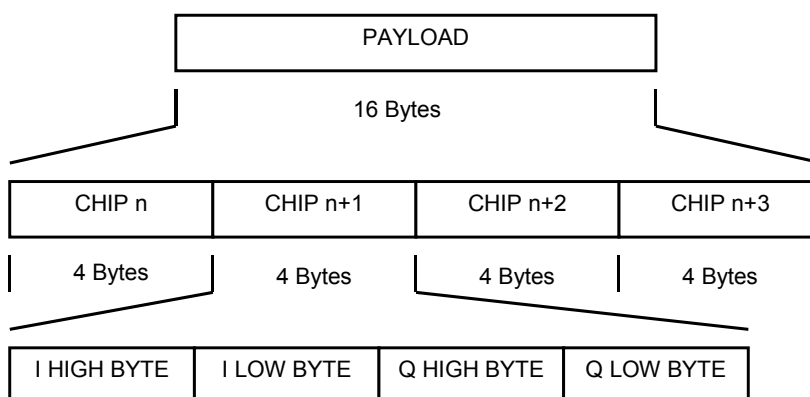


Figure 31: WCDMA DL Payload Mapping.

In case of WCDMA, the first chip of a radio frame (chip Index is 0) is always mapped to the first data message of a Master Frame (refer to Section 4.2.2 for a recommended WCDMA Master Frame definition). The first available data message slot of a Master Frame for a given WCDMA signal is defined by index I of message transmission rule (I, X) (see Section 4.4.3).

4.4.8.2 WCDMA Uplink Data Mapping

The WCDMA uplink data stream has a sample rate of 7.68 Msps (two times the chip rate), with an I&Q data format each of 8 bits giving 2 bytes per sample. This allows 8 consecutive samples (four chips) of a single WCDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. As in case of downlink data transfer, two's complement code is used and the most significant bit of a sample (both I and Q) is transmitted first (refer to Figure 11).

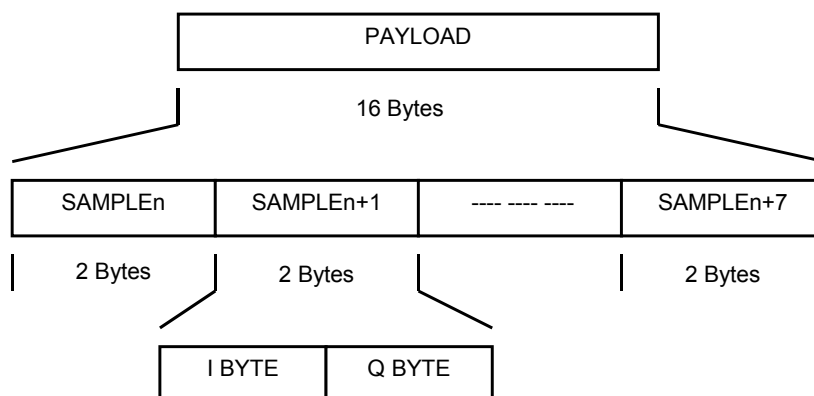


Figure 32: WCDMA UL Payload Mapping.

The first chip of a radio frame is always mapped to the first data message of a Master frame from the corresponding WCDMA frame.

4.4.8.3 GSM/EDGE Uplink Data Mapping

The GSM/EDGE uplink data stream has a sample rate of 541.667Ksps (two times the symbol rate), with an I&Q data format each of 12 bits mantissa and a 4 bit shared exponent, giving 28 bits per sample.

A GSM/EDGE timeslot contains 156.25 symbols. Three out of every four timeslots will contain 156 symbols worth, with every 4th containing 157. Given the 2x sample rate, this equals to 312 or 314 samples. The samples are 28 bits long and are fully packed into payloads due to which 69 messages are required to send a timeslot worth of data. The final packet will be partially filled containing either 4 bytes or 11 bytes worth of data.

The final packet will contain a Sample Count Indicator (SCI) (one bit) allowing the number of valid bytes in the final message to be identified. Bit value '0' indicates 312 samples per burst while '1' denotes 314. In addition, other time slot related information may be contained within the final packet. All this information will be packed into 28 bits and will reside in the packet as if it were sample 315, as illustrated in the figure below.

When extracting the data, the receiver should assume that every timeslot has 315 samples within it. The baseband processing block should first read sample 315 to determine how many valid samples are within the buffer.

Figure 33 summarises GSM/EDGE uplink data mapping.

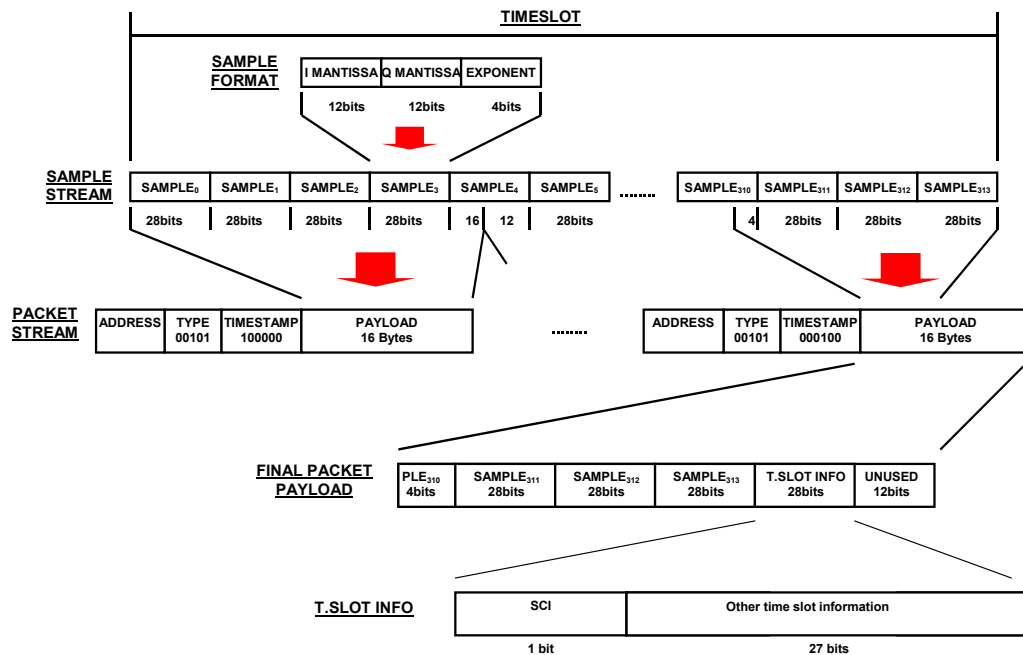


Figure 33: GSM/EDGE UL Payload Mapping.

4.4.8.4 GSM/EDGE Downlink Data Mapping

GSM/EDGE downlink data is transmitted to the RF as hard bits where it is modulated by the modulator (up converter) design block. Baseband processing block will transmit 468 data bits per timeslot per carrier per TX antenna. The 468 bits are derived from 3×156 , with the final symbol transmitted for 1.25 symbol periods giving the 156.25 symbols per timeslot.

In addition to the raw data bits, it is necessary to send carrier, power control, and phase/gain information.

In downlink, a time slot data burst to a modulator is partitioned into 8 physical layer messages: 4 messages for the burst data, 1 (original) + 1 (copy) messages for carrier control information and 1 (original) + 1 (copy) messages for power control information. The associated control is packed into control messages in order to protect the data by CRC check. Furthermore, in order to protect the control against bit errors, control messages are sent twice over the bus. If CRC of the first associated control message indicates bit error, the receiver decodes the second, copy message. If both messages have CRC failures, Application layer is responsible for error handling.

Typically, respective channelizer (down converter) in the uplink direction needs also to have the associated control information. Therefore, after sending GSM/EDGE downlink burst to modulator, baseband processing block sends 1 (original) + 1 (copy) frequency control and 1 (original) + 1 (copy) Gain Control messages to channelizer (down converter).

Figure 34 and Figure 35 illustrate transmission of a GSM/EDGE burst.

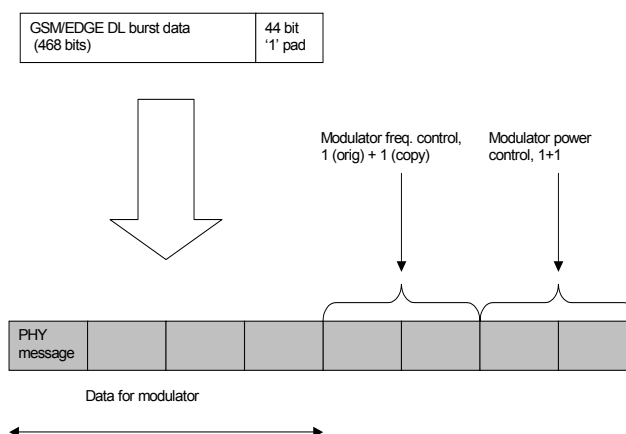


Figure 34: GSM/EDGE downlink burst for a modulator block.

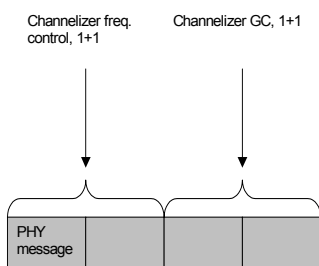


Figure 35: GSM/EDGE associated control information for a channelizer block.

4.4.8.5 CDMA2000 Downlink Data Mapping

The CDMA2000 downlink data stream has a chip rate of 1.2288 Mcps with an I&Q data format each of 16 bits giving 4 bytes per chip. This allows 4 consecutive chips of a single CDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. Two's complement code is used to represent both I and Q sample values.

In case of CDMA2000, the first chip of a radio frame (chip Index is 0) is always mapped to the first data message of a Master Frame (refer to Section 4.2.2 for a recommended CDMA Master Frame definition). The first available data message slot of a Master Frame for a given CDMA signal is defined by index I of message transmission rule (I, X) (see Section 4.4.3).

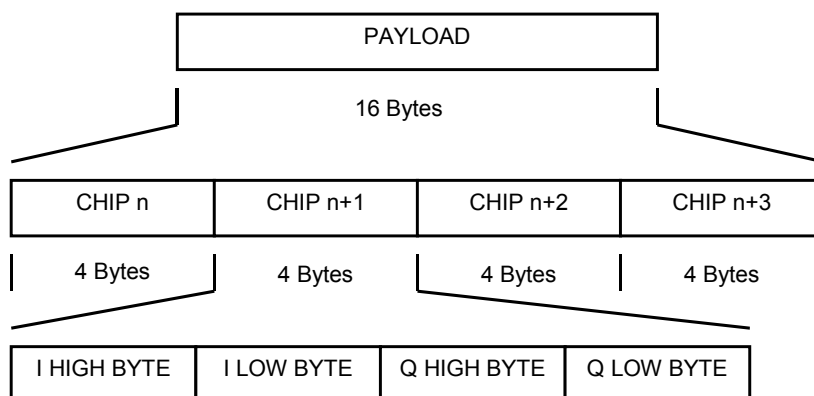


Figure 36: CDMA2000 DL Payload Mapping.

4.4.8.6 CDMA2000 Uplink Data Mapping

The CDMA2000 uplink data stream has a sample rate of 2.4576 Msps (two times the chip rate), with an I&Q data format each of 8 bits giving 2 bytes per sample. This allows 8 consecutive samples (four chips) of a single CDMA2000 signal (antenna-carrier) to be mapped into the payload as illustrated below. As in case of downlink data transfer, two's complement code is used and the most significant bit of a sample (both I and Q) is transmitted first (refer to Figure 11).

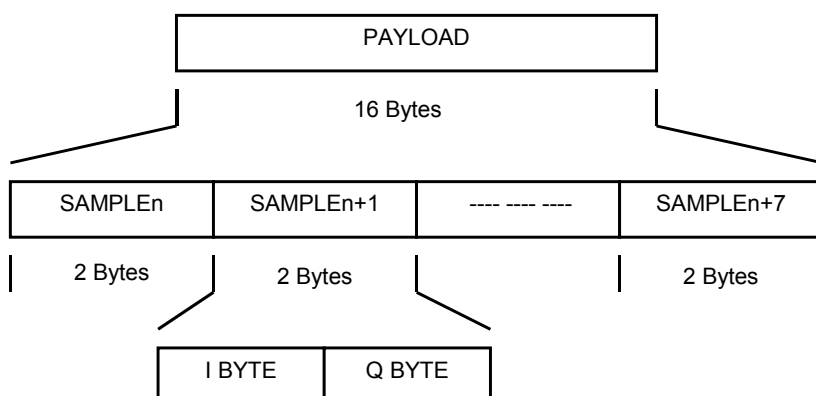


Figure 37: CDMA2000 UL Payload Mapping.

The first chip of a radio frame is always mapped to the first data message of a Master frame from the corresponding CDMA2000 frame.

4.4.8.7 802.16 Downlink and Uplink Data Mapping

RP3 protocol supports data transfer of several 802.16 profiles, each with a specific sampling rate and multiple access method, as defined in Appendix D. For each profile, the same sampling rate is applied for both downlink and uplink data streams and no oversampling is applied, i.e. antenna-carrier data is transferred over RP3 link using symbol rates defined in Appendix D. Each I&Q sample consists of four bytes which allows four consecutive I&Q samples of a single 802.16 signal

(antenna-carrier) to be mapped into the payload as illustrated below. Sixteen bit two's complement code is used for I and Q sample values and the most significant bit of a sample (both I and Q) is transmitted first (refer to Figure 11).

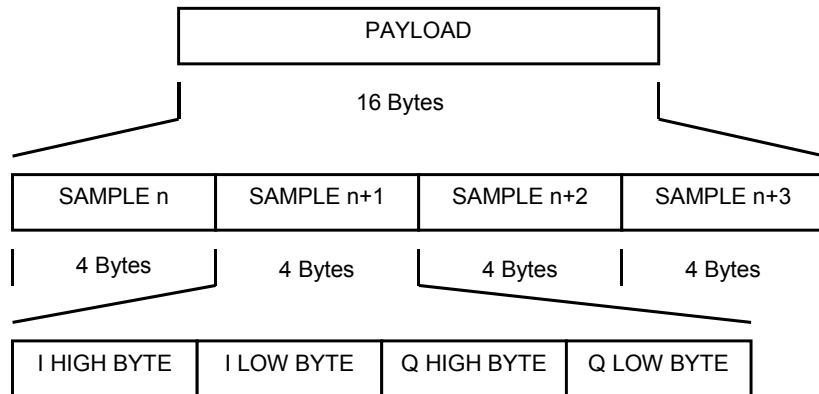


Figure 38: 802.16 downlink and uplink payload mapping.

4.4.9 Control and Measurement Data Mapping

Control and measurement messages, as identified by the CONTROL and MEASUREMENT type fields, use the payload to transport control and measurement information. A higher layer protocol is required within the payload to provide error detection. The following details two options for implementing the control and measurement signalling protocols.

4.4.9.1 Generic Control Message

Generic control message is illustrated in Table 12 and Figure 39 below, where the control message format consists of two payload fields: the message data and the 16 bit CRC. The timestamp field contains the value '000000' identifying this control message type.

The most significant bit of each message field is transmitted first (refer to Figure 11).

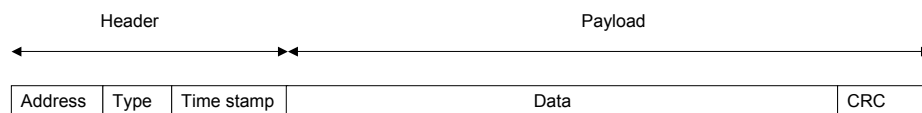


Figure 39: Generic control message.

Table 12: Content of generic control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000000
Data, 14 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

4.4.9.2 Control Message for Air Interface Synchronized Operations

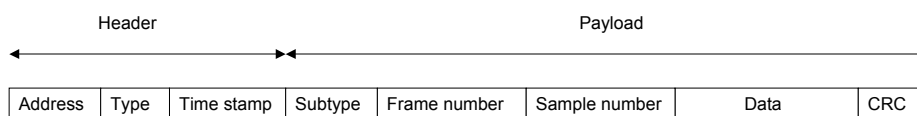
Some control operations over the RP3/RP3-01 may need to be synchronized to a specific air interface frame. For these applications, a specific control message format is introduced as defined in Table 13 and Figure 40 below. The timestamp field contains the value '000001' identifying this control message type.

Table 13: Content of air interface synchronized control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000001
Control subtype, 1 byte	Any content
Frame number, 1 byte	Least significant four bits of this byte are least significant bits of air frame number. Four most significant bits are set equal to '0000'.
Frame sample number, 3 bytes	Sample number within designated frame number to mark timing of control information.
Data, 9 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

A 24 bit sample counter, which counts samples over an air interface frame and resets at start of frame, is applied with the air interface synchronized control messages.

- 1 The most significant bit of each message field is transmitted first
2 (refer to Figure 11).



3
4 *Figure 40: Air interface synchronized control message.*

5

6 **4.4.9.3 CRC Computation**

7 For both control message options defined above, the CRC is applied to
8 the address, type, and timestamp fields of the message header as well
9 as to the actual payload data. In total, 136 bits (17 bytes) are CRC
10 protected. Generator polynomial $X^{16}+X^{12}+X^5+1$ is used with the high bit
11 transmitted first. Initially, all CRC shift register elements are set equal to
12 logical zero. Each control message enters the CRC shift register MSB
13 first, i.e. leftmost bit of the message first (see Figure 40).

14 **4.4.9.4 Measurement Data Mapping**

15 The RP3 interface facilitates the support and implementation of generic
16 measurements and air interface synchronized measurements.
17 Measurement messages use the same field format as the control
18 messages with the Type field set to '00001' (Measurement). Thus, two
19 options exist as defined in Section 4.4.9.1 and Section 4.4.9.2.

5 Electrical Specifications

This sub-section defines the electrical specifications for the RP3 physical layer.

5.1 Overview

AC electrical specifications are given for both transmitter and receiver. A single transmitter and a single receiver are specified for Baud Frequencies of 768, 1536, and 3072 MBaud.

The transmitter specification uses voltage swings that are capable of driving signals across RP3 compliant interconnect. Three RP3 compliant interconnects are defined.

To ensure interoperability between components operating from different supply voltages or implemented in different technologies, AC coupling must be used at the receiver input.

5.1.1 Explanatory Note on Electrical Specifications

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [3]. The goal of this standard is that electrical designs for RP3 can reuse electrical designs for XAUI, suitably modified for applications at the RP3-specific baud intervals described herein.

For RP3 compliance testing, a receiver compliance mask and three compliant interconnects are defined. A transmit compliance mask is not defined. Transmit compliance is verified by connecting a transmitter to a compliant interconnect and measuring the signal at the end of the channel. If the measured signal meets the minimum receiver compliance mask, the transmitter is deemed compliant.

5.1.2 Equalization

With the use of high-speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This

loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, transmit and/or receive equalization can be used.

5.1.3 Compliance Interconnect

Three RP3 compliant interconnects are defined¹:

- TYPE 1: A low loss interconnect definition specified in Section 5.4.1. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 2: A worst case, higher loss interconnect definition specified in Section 5.4.2. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 3: A low loss interconnect definition specified in Section 5.4.3. This interconnect shall be applied to 768, 1536, and 3072 Mbaud line rates.

Background information on TYPE1, TYPE2, and TYPE 3 interconnects is provided in Appendix E.

5.2 Receiver Characteristics

The RP3 receiver electrical and timing characteristics are specified in the text and tables of this section. The RP3 receiver characteristics are summarized in Table 14, Table 15, and Table 16.

5.2.1 AC Coupling

The receiver shall be AC coupled to allow for maximum interoperability between components. AC coupling is considered part of the receiver for purposes of this specification unless explicitly stated otherwise.

¹ Standard FR4 material was used as a reference when deriving the 3072 Mbaud channel model and this worst case model shall be applied both to backplane and front access cases.

Reference Point 3 Specification

1

Table 14: Receiver Characteristics – 768 MBaud

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10^{-15} of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

2

Table 15: Receiver Characteristics – 1536 MBaud

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10^{-15} of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

3

Table 16: Receiver Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10^{-15} of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

5.2.2 Input Impedance

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8 x Baud Frequency). Receiver input impedance shall be measured at the module interface. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

5.2.3 Receiver Compliance Mask

The RP3 receiver shall comply with the eye mask specified in Table 17 and Figure 41.

The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a load as defined in Section 5.3.1.

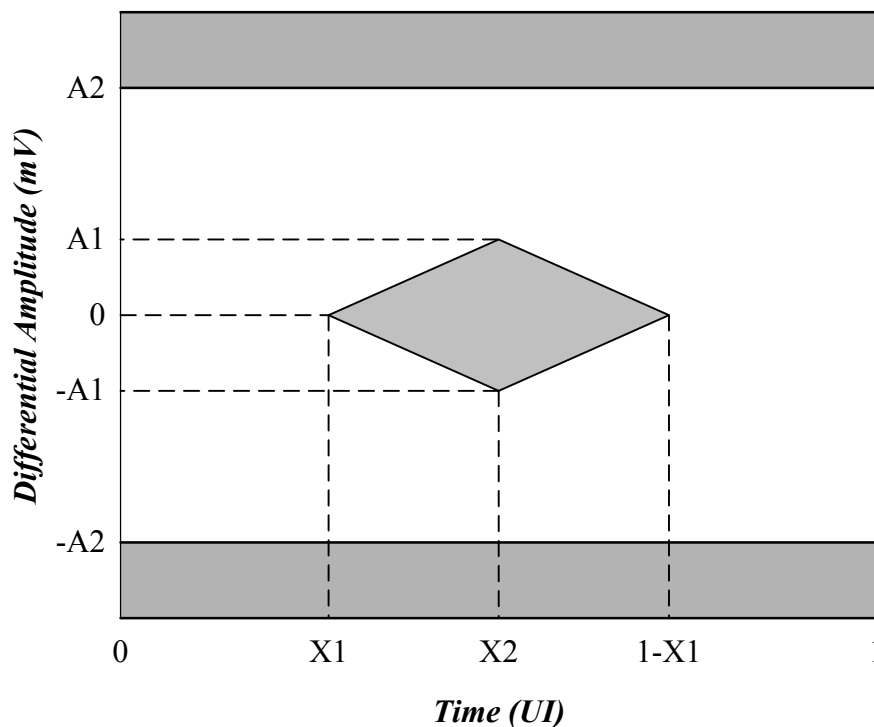


Figure 41: Receiver Compliance Mask

Note: The Receiver Compliance Mask with the values from Table 17 does not include the Sinusoidal Jitter SJ. SJ is added in the Receiver Jitter Tolerance test.

Table 17: Receiver Compliance Mask Parameters

Parameter	Value	Units
X1	0.275	UI
X2	0.5	UI
A1	100	mV
A2	800	mV

5.2.4 Jitter Tolerance

The RP3 receiver shall have a peak-to-peak total jitter amplitude tolerance of 0.65 UI. This total jitter is composed of three components: deterministic jitter, random jitter and an additional sinusoidal jitter. The jitter specifications include all but 10^{-15} of the jitter population.

Tolerance to deterministic jitter shall be at least 0.37 UI p-p. Tolerance to the sum of deterministic and random jitter shall be at least 0.55 UI p-p. The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 42 and the values of Table 18. This additional component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects.

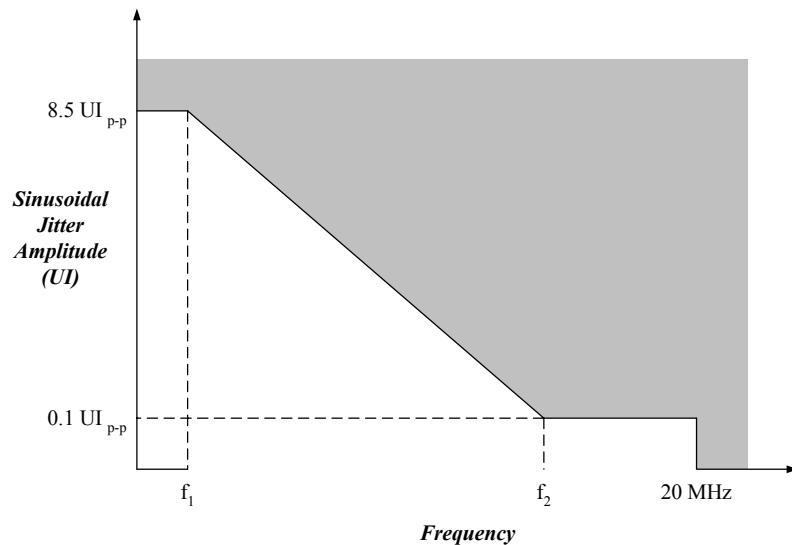


Figure 42: Sinusoidal Jitter Mask

5.2.5 Bit Error Ratio (BER)

The receiver shall operate with a BER of better than 1×10^{-15} in the presence of an input signal as defined in Section 5.2.3.

1 *Table 18: Sinusoidal Jitter Mask Values*

Baud Frequency (MBaud)	f_1 (kHz)	f_2 (kHz)
768	5.4	460.8
1536	10.9	921.6
3072	21.8	1843.2

2 **5.3 Transmitter Characteristics**

3 The RP3 transmitter electrical and timing characteristics are specified in
 4 the text and tables of this section. The RP3 transmitter characteristics
 5 are summarized in Table 19, Table 20 and Table 21.

6 *Table 19: Transmitter Characteristics – 768 MBaud*

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10^{-15} of the jitter population.
Maximum deterministic jitter (J_D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

7

1

Table 20: Transmitter Characteristics – 1536 MBaud

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

2

3

Table 21: Transmitter Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

4

5

6

7

An example RP3 Transmitter eye mask, where transmit equalization is not used, is illustrated in Figure 43. This example eye mask is provided for information only and should not be used for RP3 compliance testing.

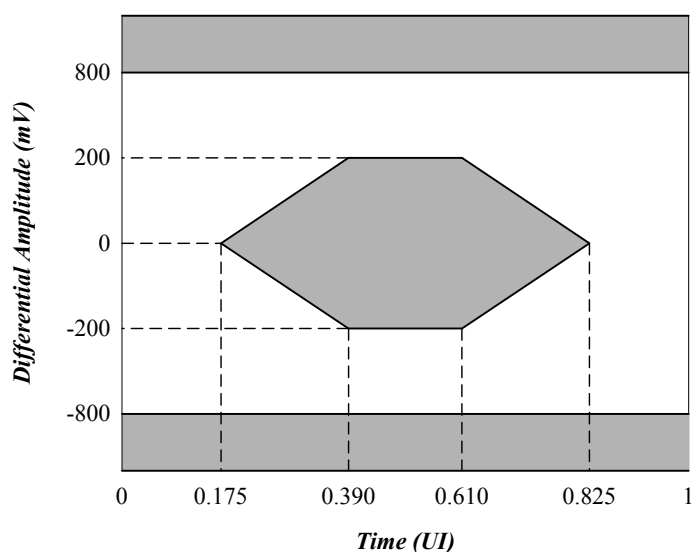


Figure 43: Example Transmitter Output Mask (For Information Only)

5.3.1 Load

The load is 100 Ohms +/- 5% differential up to (0.8 x Baud Frequency) unless otherwise noted.

5.3.2 Amplitude

The maximum transmitter differential amplitude shall be 1600 mV_{p-p}, including any transmit equalization. The minimum transmitter differential amplitude shall be 400 mV_{p-p}. This minimum value is not suitable for transmission over high loss interconnect. DC-referenced logic levels are not defined, as the receiver is AC coupled. Absolute driver output voltage shall be between -0.4 V and 2.3 V with respect to ground.

5.3.3 Output Impedance

The differential return loss, SDD11, of the transmitter shall be better than:

- -10 dB for $(\text{Baud Frequency}/10) < \text{Freq}(f) < 625 \text{ MHz}$, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \leq \text{Freq}(f) \leq (\text{Baud Frequency}) \text{ MHz}$

Differential return loss shall be measured at the module interface. The reference impedance for the differential return loss measurements is

1 100 Ohm resistive. The output impedance requirement applies to all
2 valid output levels.

3 **5.3.4 Transmitter Compliance**

4 To measure compliance of an RP3 transmitter, the transmitter shall be
5 connected to a compliance interconnect model. RP3 specifies three
6 interconnect models for transmitter compliance testing:

- 7 • TYPE 1: A low loss interconnect model as specified in Section
8 5.4.1.
- 9 • TYPE 2: A worst case, higher loss interconnect model as
10 specified in Section 5.4.2.
- 11 • TYPE 3: A low loss interconnect model as specified in Section
12 5.4.3.

13 In all cases, the RP3 transmitter shall be compliant if the signal
14 presented to the RP3 receiver at the end of the compliance interconnect
15 model meets the minimum RP3 receiver compliance mask.

16 A compliant RP3 transmitter shall meet TYPE 1 and TYPE 2
17 compliance interconnect test cases or TYPE 3 compliance interconnect
18 test case.

19 **5.4 Measurement and Test Requirements**

20 This section defines the measurement and test requirements for an
21 RP3 electrical interface. These measurement and test requirements are
22 based upon those of the XAUI electrical interface as specified in Clause
23 47 of IEEE 802.3ae-2002 [3].

24 Typical test instruments and their cabling are based on single ended 50
25 Ohm termination. In order to achieve the required 100 Ohm differential,
26 as well as common mode 25 Ohm, resistive loads, in all measurements
27 and tests related to electrical specifications, both lines of a differential
28 transmission interconnect pair shall be terminated individually with 50
29 Ohm +/- 5% resistors to ground. Such a load shall maintain this
30 accuracy in its resistive characteristics at least up to 0.8 x Baud
31 Frequency.

32 **5.4.1 TYPE 1 Compliance Interconnect Definition**

33 The TYPE 1 interconnect definition shall be used to validate the
34 compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 1 compliance interconnect shall be:

$$\text{Differential Insertion Loss (F)} \leq (0.2629 \times \sqrt{F}) + (0.0034 \times F) + (12.76 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

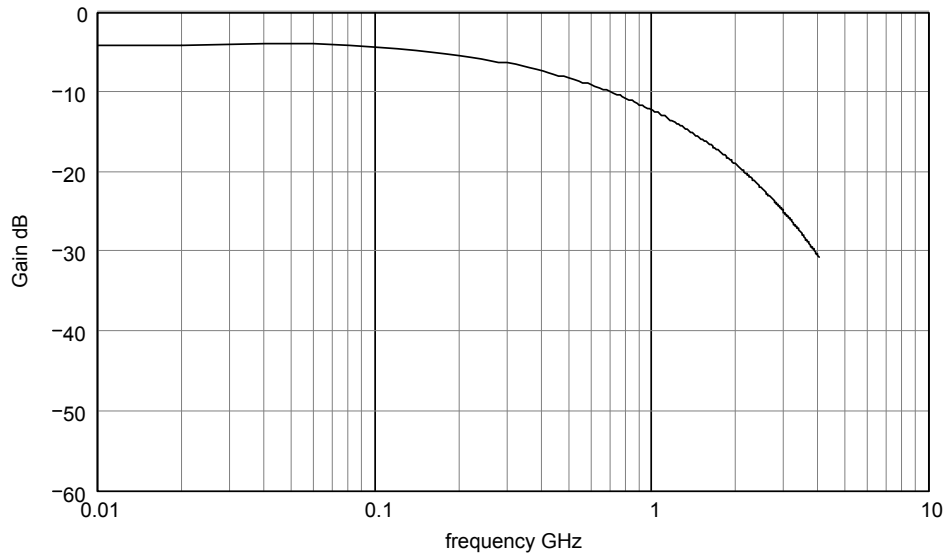


Figure 44: TYPE 1 Compliance Interconnect Differential Insertion Loss

5.4.2 TYPE 2 Compliance Interconnect Definition

The TYPE 2 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 2 compliance interconnect shall be:

$$\text{Differential Insertion Loss (F)} \leq (0.1 \times \sqrt{F}) + (0.011 \times F) + (6 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

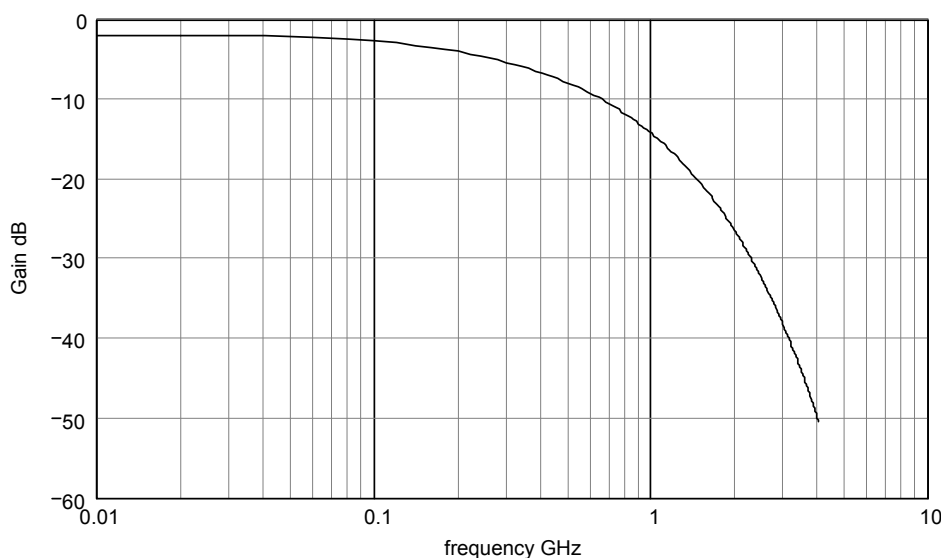


Figure 45: TYPE 2 Compliance Interconnect Differential Insertion Loss

5.4.3 TYPE 3 Compliance Interconnect Definition

The TYPE 3 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768, 1536, and 3072 Mbaud line rates.

The worst case TYPE 3 channel differential Insertion Loss (transfer function) SDD21 shall meet Equation 1 where as the variable f (frequency) unit is in GHz. The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 return loss, therefore differential coupling effects may be neglected for insertion loss SDD21.

$$IL_{SDD\ 21}(dB) = \begin{cases} -10 \sqrt{f/f_0} & ; f < f_0 \\ -7(f - f_0)^{1.15} - 10 & ; f_0 \leq f < 4.5\text{GHz} \end{cases}$$

$$f_0 = 1.5\text{GHz}$$

Equation 1: Differential Transfer Function (IL) Model

Figure 46 depicts the above TYPE 3 transfer function chart.

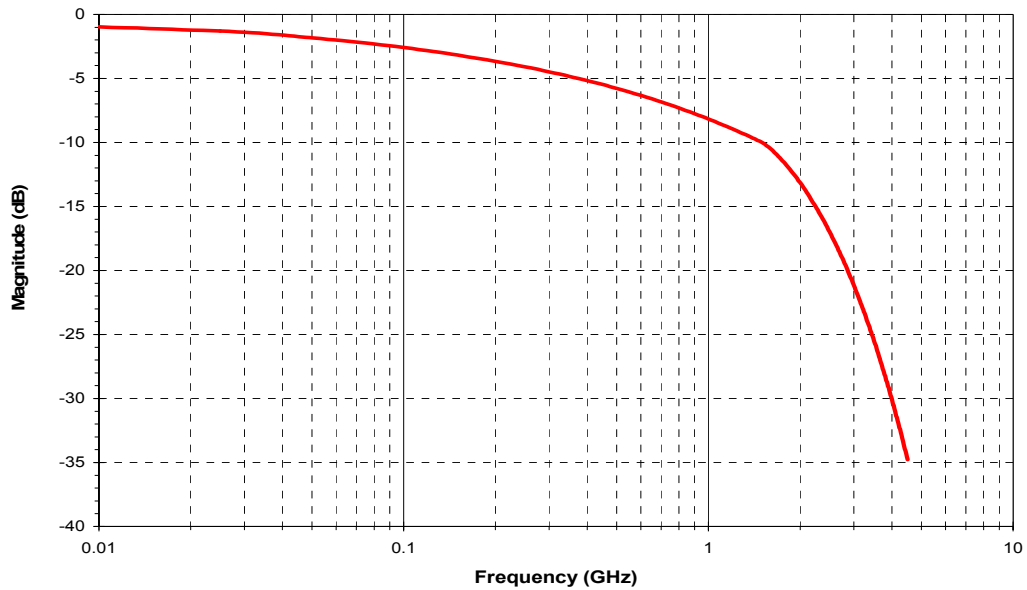


Figure 46: TYPE 3 Differential Transfer Function Chart

The worst case TYPE 3 channel differential return loss (RL) SDD11 shall meet Equation 2 where as the variable f (frequency) unit is in GHz.

$$RL_{SDD11}(dB) = \begin{cases} -15 & ; f < 1GHz \\ 5(f) - 20 & ; 1 \leq f < 3GHz \\ -5 & ; 3 \leq f < 4.5GHz \end{cases}$$

Equation 2: Differential Return Loss Model

The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 insertion loss, therefore differential coupling effects may be neglected for return loss SDD11.

Figure 47 depicts the above TYPE 3 Return Loss chart.

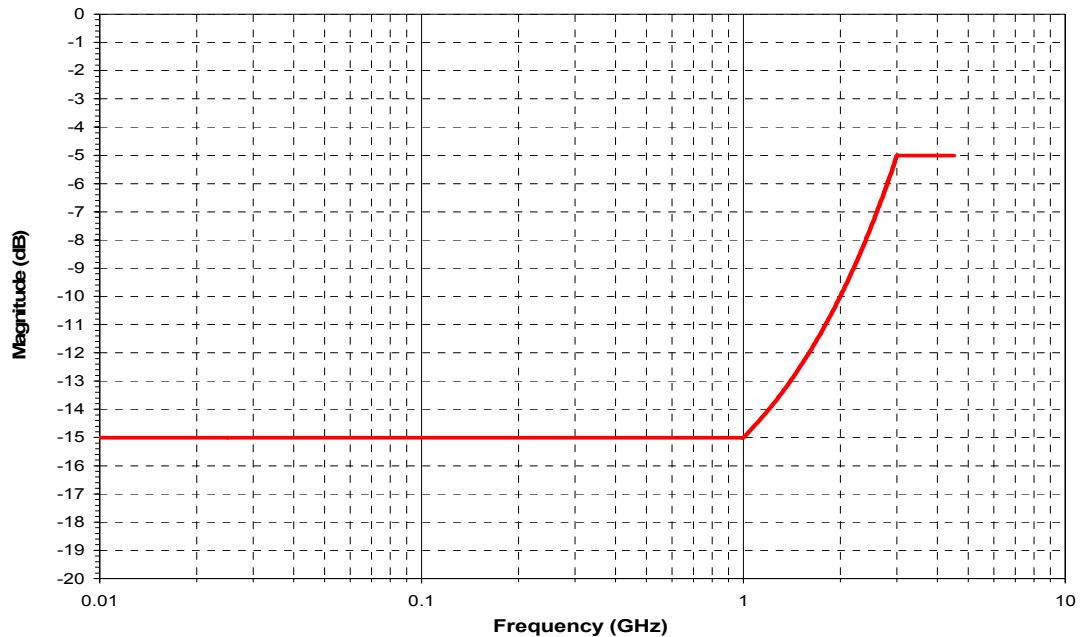


Figure 47: TYPE 3 Differential Return Loss Chart.

5.4.4 Eye Mask Measurements

For the purpose of eye mask measurements, the effect of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for mask measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae-2002 [3]. The RP3 link shall be active in both transmit and receive directions, and opposite ends of the link shall use synchronous clocks. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 1×10^{-15} . The eye pattern shall be measured with AC coupling and the compliance mask centered at 0 Volts differential. The left and right edges of the mask shall be aligned with the mean zero crossing points of the measured data eye as illustrated in Figure 48.

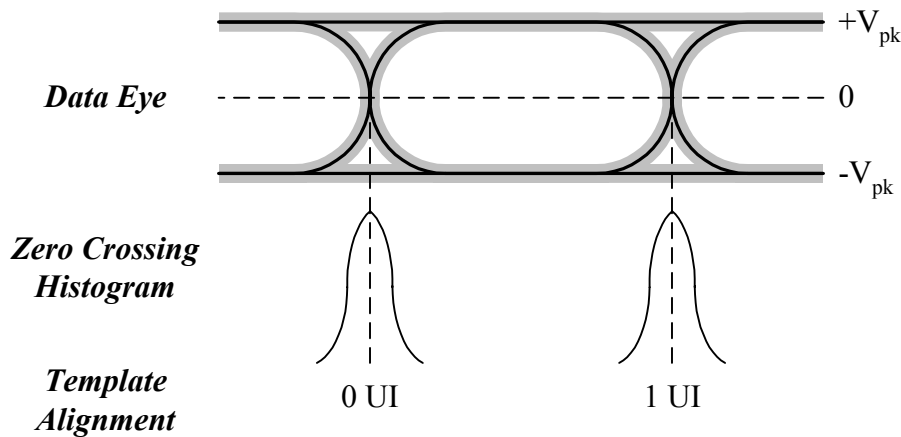


Figure 48: Eye Mask Alignment

5.4.5 Transmit Jitter

Transmit jitter shall be measured at the driver output when terminated according to the definition in Section 5.4.

5.4.6 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 5.2.4 and then adjusting the signal amplitude until the data eye contacts the 4 points of the minimum eye opening of the receiver compliance mask specified in Figure 41 and Table 17. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye mask measurement requirements are defined in Section 5.4.4. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade rolloff below this. The required sinusoidal jitter specified in Section 5.2.4 is then added to the signal and the test load is replaced by the receiver being tested.

6 RP3-01 Interface for Remote RF Unit

There exist base station configurations where remote RF units are used. This chapter specifies an extension of the Reference Point 3 protocol for remote RF unit use.

Section 6.1 defines architecture for RP3-01 interface while protocol stack for data transfer is defined in Section 6.2.

6.1 Architecture

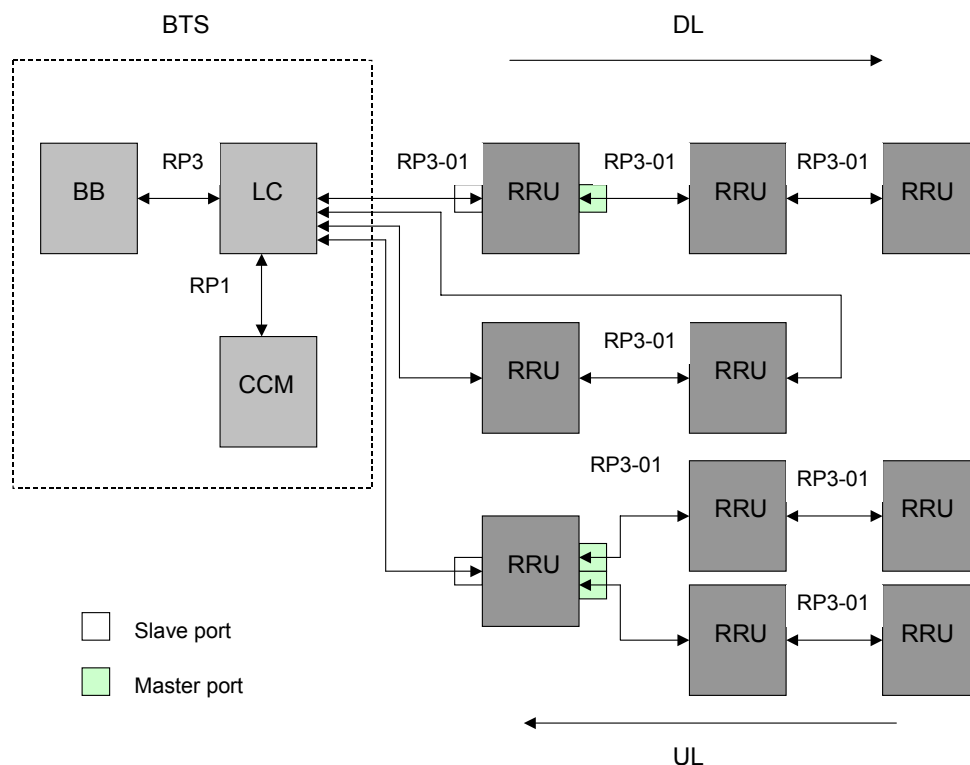


Figure 49: RP3-01 example architecture. Base station with remote RF units (RRUs). RRUs in chain, ring, and tree-and-branch topologies. Examples of RP3-01 master and slave ports of RRUs are also shown.

Figure 49 shows an example architecture of a BTS with remote RF units (RRUs). The figure provides a logical architecture and does not

imply physical implementation of the BTS. The Local Converter (LC) may exist as a separate module or it may be integrated with other modules, such as the baseband module. For definitions of terms used in the figure and in the RP3-01 protocol description, refer to the Glossary.

The RP3-01 protocol shall support several RRU topologies, including point-to-point connection between a BTS and an RRU as well as chain, tree-and-branch and ring topologies.

Each RRU has one RP3-01 slave port and, optionally, one or more master ports. The slave port is connected toward the BTS either directly or through other RRU(s) while master port(s) connect to RRU(s) that are next in the chain. Slave and master ports are defined dynamically at BTS startup. The RP3-01 receiver first detecting transmission from the BTS, and its associated transmitter, are defined as the slave port while other ports are defined to be master ports.

Figure 50 provides an overview of RP3-01 protocol functionality at the LC and RRU for the case of a point-to-point topology. Section 6.2 defines in detail how RP1 and RP3 data is mapped into RP3-01 format. Basically, RP3-01 stands for an RP3 protocol where RP1 data is transferred in RP3 messages, between LCs and RRUs.

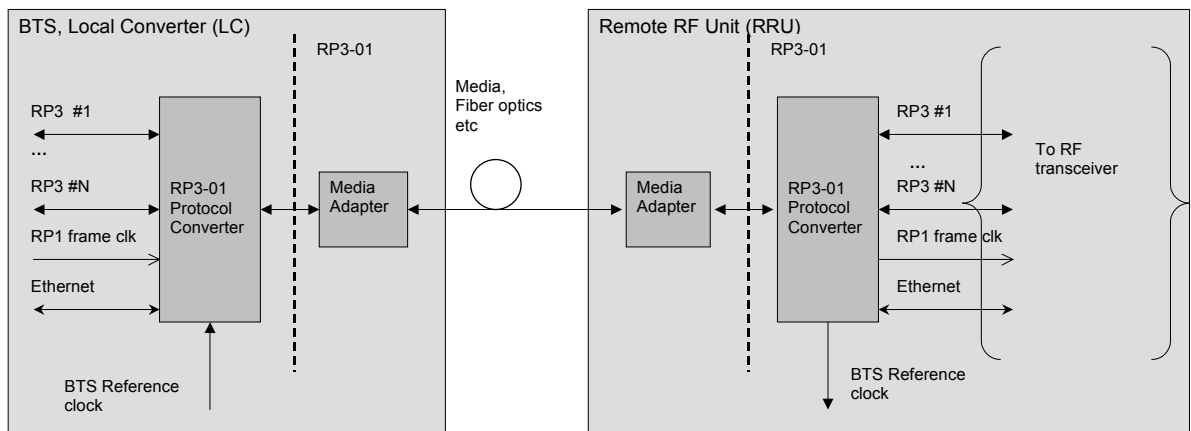


Figure 50: Logical model of OBSAI RP3-01 point-to-point interface.

6.2 Protocol Stack

6.2.1 Physical Layer

6.2.1.1 Media Adapter and Media

The media adapters and media defined in Appendix A shall be used.

6.2.1.2 Line Rates

RP3-01 and RP3 line rates are the same, i.e. 768Mbps, 1536Mbps, or 3072Mbps line rate shall be used.

6.2.2 RP3-01 - Transfer of RP1 Data Over RP3

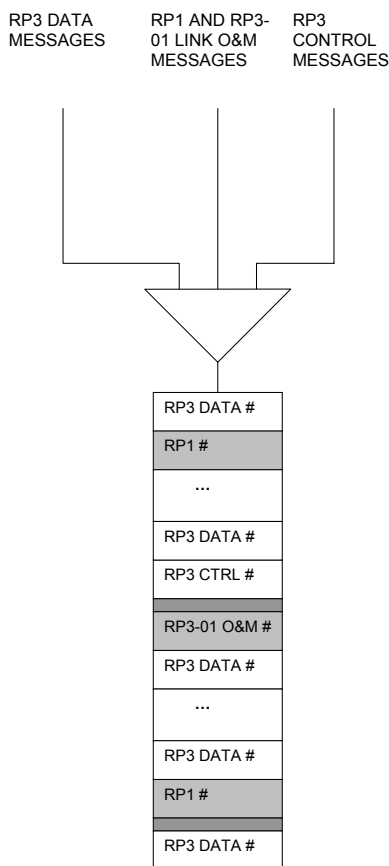
RP3-01 is an extension of the RP3 protocol specifically designed for data transfer between a BTS and one or more remote RF units. RP3-01 is equivalent to the RP3 protocol except for the fact that different physical layer technologies, suitable for supporting data transmission over long distances, are applied. In order to minimize the number of connections to RRUs, RP1 data is mapped into RP3 messages. RP1 data includes Ethernet and frame clock bursts.

In the RP3-01 protocol, bandwidth is allocated to all data transfers by defining message transmission rules (see Section 4.4.3). Separate transmission rules shall be given as needed to RP1 Ethernet, RP1 frame clock burst, RTT measurement, Virtual HW reset, loop back, RP3 data, and RP3 control messages. Typically, RP3 data and control messages are already scheduled at baseband and RF modules in downlink and uplink directions, respectively, using message transmission rules. RTT measurement, HW reset, and loop back are examples of RP3-01 link O&M messages. RP1 and RP3-01 link O&M data can be transmitted in any RP3 message slot, as illustrated by Figure 51.

6.2.3 RP1 Frame Clock Bursts

The Control and Clock Module (CCM) shall provide frame timing information for each air interface standard, independently, via periodic synchronization bursts, as shown in Figure 52 [4]. A dedicated link is used to transfer the frame timing information to modules that are located in a BTS cabinet. For a RRU, frame timing information is transferred over the RP3-01 protocol by mapping the information within the RP1 frame clock bursts, into RP3 messages, and then regenerating

1 the RP1 frame clock burst at the RRU by applying the algorithm defined
2 in this section.



3
4 *Figure 51: Examples of mapping RP1 and RP3-01 link O&M data into*
5 *RP3 messages.*

Start 1	Type 8	Type Specific Information 64	CRC 16	End 1
------------	-----------	---------------------------------	-----------	----------

6
7 *Figure 52: RP1 frame clock synchronization burst from CCM.*

8 **The LC** is responsible for multiplexing RP1 frame clock synchronization
9 bursts into RP3 messages and it performs the following functionality.

- 10
- 11 • A counter, called *c1*, is reset and started at the beginning of the
12 RP3-01 Master Frame and this counter measures time as a multiple
13 of $1/(8*76.8)$ MHz. Thus 614.4MHz is the frequency of the reference
clock.
 - 14 • The RP1 Frame Clock Burst (FCB) from the CCM is received and
15 processed.

- The RP1 frame clock burst from the CCM is discarded if the CRC check fails
- Only the first RP1 frame clock burst after the beginning of the RP3-01 Master Frame is accepted
- If a new RP1 synchronization burst is received before the previous is transmitted as FCB message, the new RP1 burst is discarded and an interrupt is generated to upper layers

The CCM is responsible for alternating the transmission order of the RP1 frame clock burst for the different air interface standards, so that timing for each standard will be transferred to RRUs.

- The arrival time of the end bit of the RP1 frame clock burst, from the beginning of the RP3-01 Master Frame, is measured by the counter *c1* and stored into an RP3-01 frame clock synchronization message defined by Figure 53 and Table 22. System and System Frame Number (SFN) information from RP1 frame clock synchronization burst are also stored into the message. After the message has been constructed, including the header, the CRC check for the whole message is computed and added to end.
- RP3-01 frame clock synchronization message shall be transmitted to RRUs in an RP3 message. The RP3-01 FCB message shall be transmitted in a time window of 9ms, starting from the end of the RP1 synchronization burst.

RRUs are responsible for all of the computations that are required for frame time transfer. The algorithm described below is a general one and supports all air interface standards.

- Counter *c2* is reset to zero and started at the beginning of each RP3-01 Master Frame, except if the *c2* counter is serving a FCB (RP3 Frame Clock synchronization Burst) message. The *c2* counter measures time as a multiple of $1/(8*76.8)$ MHz. Thus 614.4MHz is the frequency of the reference clock.
 - When FCB message is being served, *c2* increments without reset at the MF boundary
 - If FCB message is being served by *c2* counter when new FCB message is received from LC, then the new FCB message shall be discarded and an interrupt is generated to upper layer to indicate erroneous situation
- The RRU receives the RP3-01 frame clock synchronization message
- When RP3-01 FCB message type has been detected, the present *c2* counter value is captured, without disturbing *c2* counting. This captured *c2* value is called FCB_message_rx_time

- In case a new FCB message while an older message was being served by c2 counter, the count is not captured (erratic situation).
 - The received message is discarded if the CRC check fails
 - The RRU computes the buffering time B_{RRU} of the frame clock synchronization burst at the RRU, as follows
 - Find minimal positive integer value for parameter k such that

$$k * SFN_FRAME_TIME \geq RP3-01_MASTER_FRAME_TIME$$
 where SFN_FRAME_TIME equals to the length of the air interface frame and $RP3-01_MASTER_FRAME_TIME$ is always equal to 10ms. As an example, assume that SFN_FRAME_TIME is equal to 10 ms (WCDMA case). Then k equals to 1.
 - The captured c2 value is compared to c1 value received in the FCB message
 - If $FCB_message_rx_time > c1$, then B_{RRU} is then computed using formula:

$$B_{RRU} = k * SFN_FRAME_TIME + c1 * 1 / (8 * 76.8MHz) - RP1_FRAME_CLOCK_BURST_TIME$$
 If $FCB_message_rx_time < c1$, then B_{RRU} is then computed using formula:

$$B_{RRU} = k * SFN_FRAME_TIME - RP3-01_MASTER_FRAME_TIME + c1 * 1 / (8 * 76.8MHz) - RP1_FRAME_CLOCK_BURST_TIME$$
 In the above equation, $RP1_FRAME_CLOCK_BURST_TIME$ stands for the time required to transmit an RP1 frame clock burst in RP1 interface. This equals to $90 * 1 / 3.84MHz = 23.4375us$
 - The RRU increments the System Frame Number (SFN) by k
 - When the counter $c2$ reaches B_{RRU} , the recomputed RP1 frame clock burst shall be sent to functional blocks within RRU.
 - The format of the recomputed RP1 frame clock burst is equal to that of the original burst received from the CCM (see Figure 52) but the value of the System Frame Number has been incremented by k and the CRC check value has been recomputed.
 - The functional blocks of the RRU shall receive and decode SFN in exactly the same manner as in the case of a single cabinet BTS.
- The content of an RP3-01 frame clock synchronization message is defined in detail in Table 22.
- The most significant bit of each message field is transmitted first (refer to Figure 11).

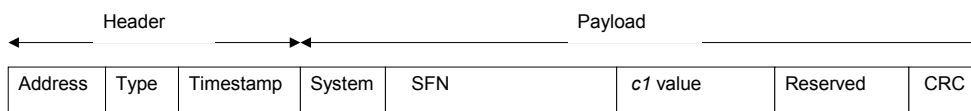


Figure 53: RP3-01 frame clock synchronization message.

Table 22: Content of RP3-01 frame clock synchronization message.

Field	Value
Address	Broadcast address (typically)
Type	Frame clock burst, 01001 in binary
Time stamp	000000
System, 8 bits	Refer to [4].
System Frame Number, 64 bits	Refer to [4].
c1 counter value, 26 bits	Positive integer number defining the arrival time of the RP1 frame clock burst from CCM with respect to RP3-01 Master Frame start as multiples of $1/(8*76.8)$ MHz.
Reserved, 14 bits	All zeros
CRC, 16 bits	Refer to Section 4.4.9.3 for the definition of the CRC.

Figure 54 illustrates the timing of RP1 frame clock burst transmissions. As can be seen from the figure, the RRU obtains its frame timing from a “future” System Frame Number $p+k$ not from the System Frame Number p that is used by all baseband and RF modules located in the BTS cabinet.

The propagation delay Δ_{LC-RRU} shown in Figure 54 may be large when an RRU is located far away from the BTS. The above algorithm does not take into account the impact of propagation delay in frame clock transfer. Propagation delay can be measured and removed from the frame clock timing. Section 6.2.6.2 specifies an algorithm for propagation delay measurement.

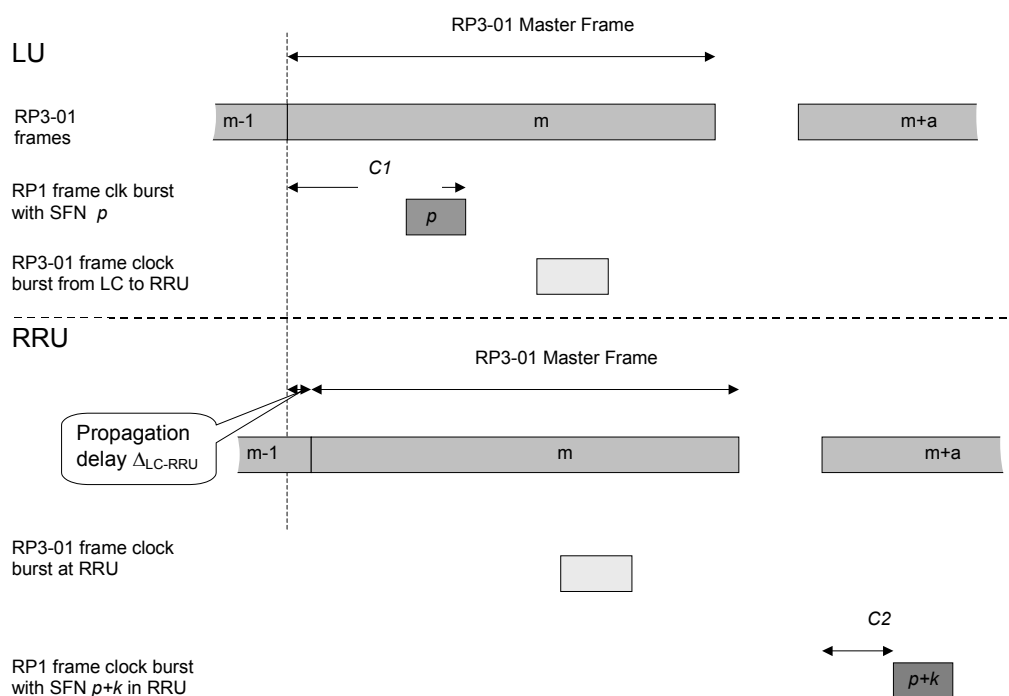


Figure 54: Timing principle in RP1 frame clock burst transfer.

6.2.4 Ethernet Transmission

Between any two RP3-01 nodes, whether in a BTS or an remote RF unit, a point-to-point Ethernet transfer is applied, as shown in Figure 55. Thus, only a single logical connection is allocated for Ethernet MAC messages between RP3-01 nodes. Where chain, ring, or tree-and-branch topologies are used for a number of remote RF units, the Ethernet switch in each RRU shall decide whether the MAC frame is consumed in that RRU or whether it will be forwarded to the next node.

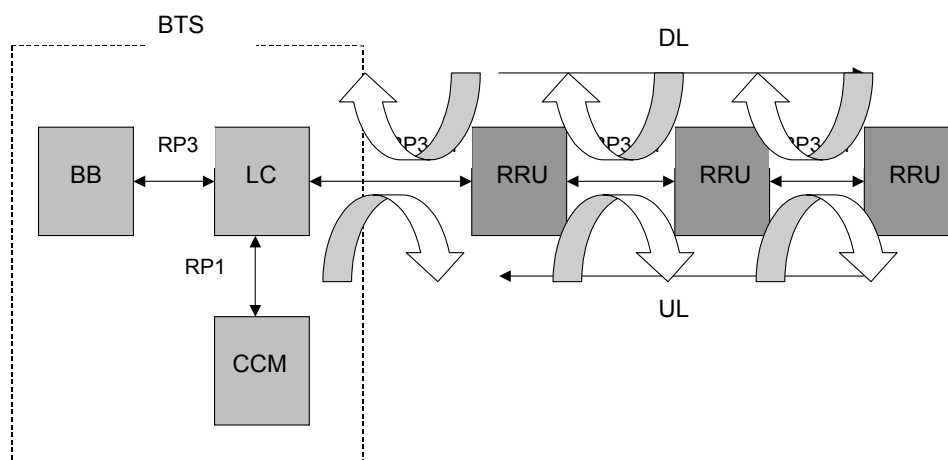


Figure 55: Ethernet frame transfer over RP3-01 network is done as a point-to-point transfer between a pair of nodes.

The Ethernet throughput over each RP3-01 link is specifically allocated by message transmission rules, as defined in Section 6.2.2.

Ethernet MAC frames are mapped into RP3 messages and transferred over the RP3-01 protocol. At the input, there exist MAC frames as specified by 802.3-2002 [10]. A MAC frame consists of preamble, start frame delimiter, the addresses of the frame's source and destination, a length or type field, MAC client data, a field that contains padding if required, a frame check sequence, and an extension field, if required. Each MAC frame is sliced into consecutive RP3 messages and the time stamp field defines the beginning and end of each MAC frame, as indicated in Table 23.

Table 23: Content of the time stamp field of RP3 messages in relation to Ethernet MAC frame data of the payload.

Time Stamp	Payload Content
100000	16 first bytes of an Ethernet MAC frame. The first byte of the MAC frame is located immediately after RP3 header.
000000	Next (second) RP3 message containing a part of the MAC frame.
...	
000000	Nth RP3 message containing a part of the MAC frame.
1xxxxx	The last RP3 message containing a slice from the MAC frame and xxxxx, a binary number, indicates the number of bytes from the start of RP3 payload containing MAC frame data (counting started from the byte after the header).

Table 24 defines the content of RP3 messages when used for Ethernet data transfer. The 'Address' field contains the address of the next RP3-01 node, The 'type' field indicates that Ethernet MAC data is contained in the payload, and all bits of the payload contain MAC data, excluding the last RP3 message, which may be partially filled.

The most significant bit of each message field is transmitted first (refer to Figure 11).

At the receiver, MAC frames are reconstructed from the payload of RP3-01 Ethernet messages by concatenation according to the content of the 'type' and 'time stamp' fields. By monitoring the 'type' field, the receiver shall identify RP3 messages containing Ethernet data. The transmitter shall send only one MAC message at a time from which the

'time stamp' field can be used to identify the beginning and end of a MAC frame. A received MAC frame is discarded if an error is detected in 'time stamp' field processing. The RP3-01 protocol shall not check the validity of the MAC frame check or CRC fields.

Table 24: Content of RP3-01 Ethernet message.

Field	Content
Address	Target address of next RP3-01 node
Type	Ethernet, 01010 in binary
Time Stamp	See Table 23.
Payload	Slice from Ethernet MAC frame.

In Ethernet transfer over RP3-01, a flexible implementation methodology should be applied, in order to prepare for possible changes in the future.

In order to transfer Ethernet MAC frames over RP3-01, an Ethernet MAC Address must be established for each RRU. The RRU may use either a globally or locally unique MAC address. For a locally unique MAC address, OBSAI System Specification [2] describes the methodology to derive a locally unique MAC address based on module hardware position. However, the IDs described in that section are not normally available at the RRU. These IDs can be communicated from the BTS to the RRU through an initialization MAC frame.

Each RRU has an RP3-01 slave port and optionally one or more RP3-01 master ports. At startup, the RRU shall disable transmission on all RP3-01 master ports. An RRU's RP3-01 slave port at startup shall respond to only an RP3 node address of zero and shall not have an initial locally unique MAC address. It shall listen for an initialization MAC frame using the Ethernet transmission protocol over RP3-01 that contains a broadcast MAC address for the destination address. This initialization message shall contain all the IDs described in OBSAI System Specification. The RRU shall then use these IDs as described in that section to derive its permanent locally unique MAC address. If using a locally unique MAC address, the RRU shall use this permanent MAC address for any further Ethernet transmissions. The RRU shall be configured with a permanent RP3 node address using RP1 over RP3-01 at which time it shall stop using the zero RP3 node address. After MAC address and RP3 node address configuration, an RRU may be instructed over RP1 to enable its master port(s) one at a time to allow initialization and network discovery of any other RRUs in the RP3-01 chain as shown in the example architectures of Figure 49.

6.2.5 Line Rate Auto-Negotiation

There exists a set of allowed RP3-01 line rates as defined in Section 6.2.1.2 and each LC or RRU can support one or several of these line rates. Before communication over an RP3-01 link can be initiated, a common line rate needs to be negotiated between adjacent RP3-01 nodes, with a 'node' being either an LC or an RRU. If the common line rate is known and pre-configured, a search for a common line rate is not required. Auto-negotiation of the line rate shall be applied when the used line rate is not defined beforehand.

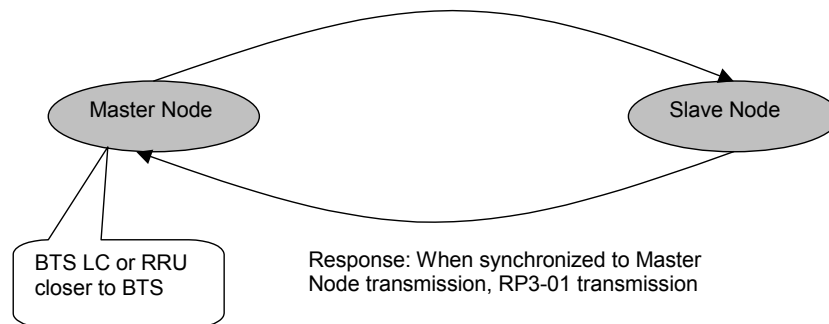


Figure 56: RP3-01 line rate auto-negotiation is done between a pair of nodes (LC and RRU or between adjacent RRUs).

Auto-negotiation of RP3-01 peer-to-peer links is considered in this section, as shown in Figure 56. For a chain, ring or tree-and-branch configuration of RRUs, the auto-negotiation algorithm is applied to each pair of RRUs at a time. The algorithm identifies a single line rate over each RP3-01 link, which is supported by both end nodes.

RP3-01 link synchronization is performed for a pair of RRUs. The Master node, which is the LC or RRU closest to the BTS, controls the auto-negotiation process.

The following assumptions are made:

- Master and slave nodes support all or a subset of allowed RP3-01 line rates.
- Allowed line rates include $i \times 768$ Mbps, where $i \in \{1, 2, 4\}$, i.e. 768, 1536, and 3072 Mbps.

A set of parameters controls the operation of the algorithm and Application layer sets the value of these parameters. Table 25 lists the parameters of the auto-negotiation algorithm while Table 32 in Section 7.1.5 defines the parameters in detail. When setting parameter values for the RP3 receiver frame synchronization state machine (see Section 4.2.7), the worst case RP3 frame synchronization time at the receiver shall not exceed TxTime.

Table 25: Parameters of line rate auto-negotiation algorithm.

Parameter	Description
MaxSynchronizationTime	Time limit for the line rate auto-negotiation algorithm.
MaxRxTime	Reception time at a given line rate.
TxTime	Transmission time at a given line rate.

Auto-negotiation algorithm for the Master node:

1. Set *Synchronization* = FALSE and start time out counter *TimeOutCounter*.
2. Select lowest RP3-01 line rate that is supported by the Master node
3. Attempt RP3-01 synchronization with the Slave node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) at the latest after TxTime.
 - a. Start K28.5 transmission to the Slave Node and RP3 receiver synchronization state machine (refer to Section 4.2.7).
 - b. When Master's RP3 receiver state machine goes into state WAIT_FOR_K28.7_IDLEES due to reception of K28.5 transmissions from the Slave node, start transmitting RP3 (RP3-01) frame format to the Slave node
 - c. When Master's RP3 receiver state machine goes into state FRAME_SYNC, set *Synchronization* = TRUE (RP3-01 synchronization between Master and Slave nodes has been completed).
4. If *Synchronization* = FALSE and *TimeOutCounter* is less than MaxSynchronizationTime, change to next higher line rate (or go back to the lowest line rate if the highest line rate is being used) that is supported and goto Step 3.
5. End of Algorithm

Auto-negotiation algorithm for the Slave node:

1. Set *RxSynchronization* = FALSE and start time out counter *TimeOutCounter*
2. Select lowest RP3-01 line rate that is supported by the Slave node
3. Attempt RP3-01 synchronization with the Master node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) latest after MaxRxTime

- 1 a. Start RP3 receiver synchronization state machine (refer to
- 2 Section 4.2.7 of RP3 Specification)
- 3 b. When RP3 receiver synchronization state machine goes
- 4 into state WAIT_FOR_K28.7_IDLEES due to reception of
- 5 K28.5 transmissions from the Master node, start K28.5
- 6 transmission back to Master Node.
- 7 c. When RP3 receiver state machine goes into state
- 8 FRAME_SYNC, start sending RP3 frame format to Master
- 9 node and set *RxSynchronization* = TRUE.
- 10 4. If *RxSynchronization* = FALSE and *TimeOutCounter* is less than
- 11 MaxSynchronizationTime, change to next higher line rate (or go
- 12 back to the lowest line rate if the highest line rate is being used)
- 13 that is supported and goto Step 3.
- 14 5. End of Algorithm
- 15 The Master node determines success or failure of the auto-negotiation
- 16 procedure from the value of state parameter *Synchronization*. The
- 17 Slave node is able to detect only the synchronization status of the
- 18 downlink (from Master to Slave) RP3-01 link.
- 19 After RP3-01 link synchronization is achieved between the Master and
- 20 the Slave, at some line rate common to both Master and Slave, RP1
- 21 Ethernet communication can be started over the interface and over
- 22 other previously synchronized links. The Slave node can report the
- 23 complete set of supported line rates using Ethernet messaging over the
- 24 RP3-01 link.

25 **6.2.6 RTT Measurement and Internal Delays of a RRU**

26 RRUs may be located far away from the BTS. In order to be able to

27 configure the BTS, the propagation delay between the BTS and each

28 RRU needs to be measured. In this section, Round Trip Time (RTT)

29 measurement between a LC of a BTS and an RRU or between adjacent

30 pairs of RRUs is defined. Internal delays of an RRU are also defined.

31 Based on the knowledge of the RTT between adjacent RP3-01 nodes

32 and the internal delays within the RRUs, the CCM can configure the

33 BTS appropriately.

34 **6.2.6.1 Internal Delays of an RRU**

35 RRUs can be classified based on their support for different RP3-01

36 network topologies. A Class #1 RRU can only support point-to-point

37 connection toward a BTS since they contain only a single RP3-01

38 transceiver while Class #2 RRUs can support chain and ring topologies

39 due to dual RP3-01 transceiver support. Class #3 RRUs, having as a

40 minimum three RP3-01 transceivers, can generate tree-and-branch

topologies, i.e. it has a single RP3-01 transceiver, the RP3-01 slave port, toward the BTS and at least two RP3-01 transceivers, master ports, toward different RRUs.

Internal delays of Class #1, #2, and #3 RRUs are defined in Figure 57, Figure 58, and Figure 59, respectively. In a Class #3 RRU, all signal through-path propagation delays, in a given direction (transmit or receive) for a given RRU, are required to occupy the same number of RP3 byte clock cycles.

Each RRU shall report its internal delay values over the RP1 Ethernet connection which is available over RP3-01.

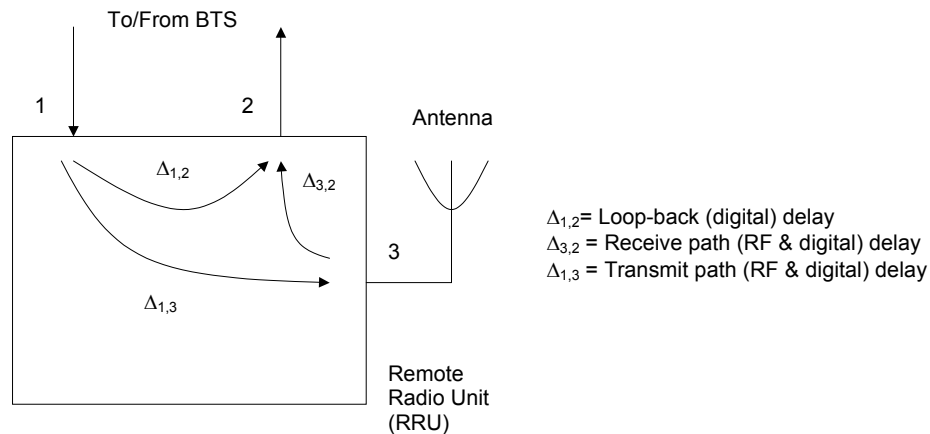


Figure 57: Internal delays of Class #1 RRU.

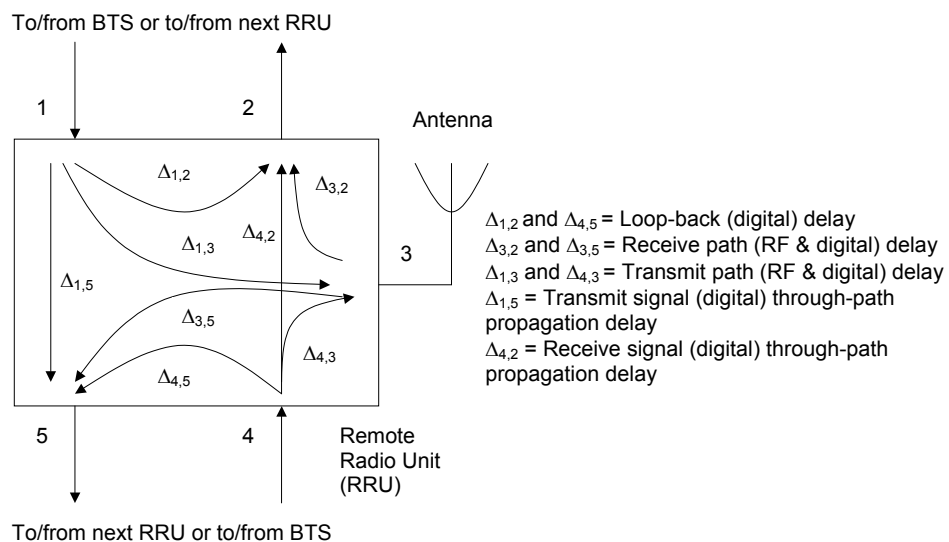


Figure 58: Internal delays of Class #2 RRU.

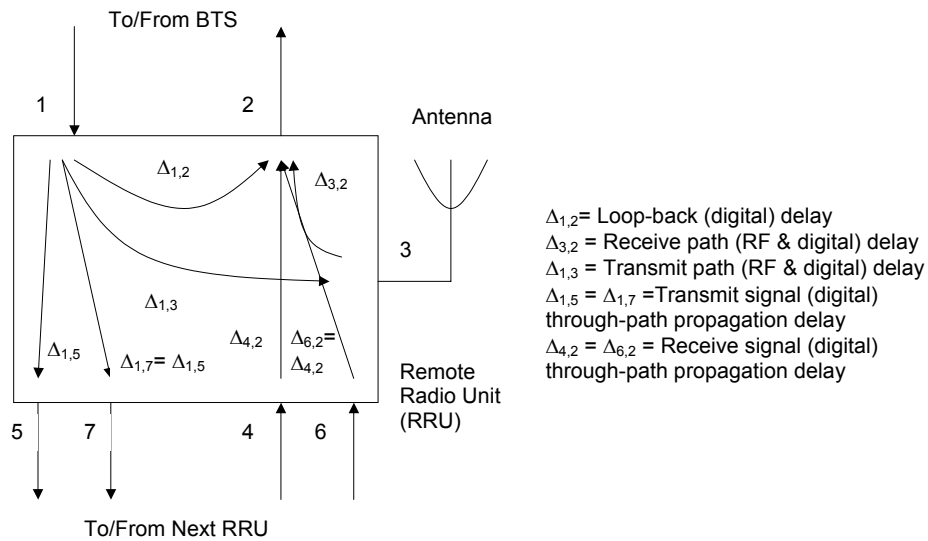


Figure 59: Internal delays of Class #3 RRU.

6.2.6.2 RTT Measurement Procedure

The RTT measurement procedure determines the two way propagation delay over the media, e.g. fiber optics, between two adjacent RP3-01 nodes. In the case of chain, ring, or tree-and-branch topologies for the RRU's, RTT measurements are performed in a sequence for each adjacent pair of RP3-01 nodes.

The RTT measurement procedure is defined as follows: A Master RP3-01 node shall send the RTT measurement message defined in Figure 60 to a Slave RP3-01 node and measure the time T from message transmission to message reception. The Master node is either LC or RRU # n while the Slave node is RU #1 or RU # $n+1$, respectively, and $n > 0$. The Slave node shall receive and send back the RTT measurement message to the Master node. Before transmission, the Slave node shall replace the address of the header by the return address of the payload and vice versa. Also buffering time $\Delta_{1,2}$ of the message at the Slave node will be stored into the message. Typically, the return address is equal to the RP3-01 node address of the Master node, so an 'address swap' procedure guarantees easy reception of the RTT message at the Master node.

All the time measurements are performed as a multiple of $1/(8*76.8)$ MHz, i.e. 614.4MHz is the frequency of the reference clock.

Table 26 defines the content of different fields of the RTT message.

The most significant bit of each message field is transmitted first (refer to Figure 11).

Table 26: Content of an RTT Measurement message.

Field	Value
Address	Slave/Master RP3 node address (Slave address first, before address swap)
Type	01011 (RTT message)
Time stamp	000000
Return address, 13 first bits of the payload	Master/Slave RP3 node address (first Master address)
Reserved, 83 bits	All zeros
Buffering time $\Delta_{1,2}$, 16 bits	Positive integer number, buffering time will be measured using a reference clock at frequency $(8 * 76.8)$ MHz.
CRC check, 16 bits	CRC check sum computed over the header and payload. Refer to Section 4.4.9.3 for the definition of the CRC.

The RTT between the Master and Slave nodes over fibre optics or other media is equal to $\Delta_{RTT} = T - \Delta_{1,2}$. The delay over the fibre is considered to be the same in downlink and uplink directions, i.e. one way delay over the fibre is equal to $\Delta_{RTT} / 2$.

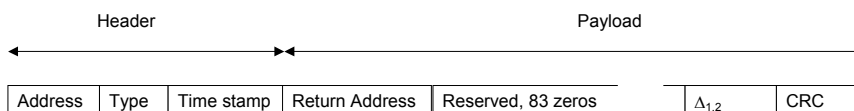


Figure 60: RTT Measurement message.

6.2.7 Virtual HW Reset

A remote reset may need to be performed to a RRU in a case where the control processor of the RRU is halted. RRU may optionally support virtual HW reset functionality where the unit undergoes a boot sequence after receiving a specific virtual HW reset message. When receiving such a message, the following procedure shall be followed.

- CRC check is first performed. If the CRC check fails, the virtual HW message is rejected.
- The type field is checked. If it equals to 01101 (Virtual HW Reset), HW reset is performed for the RRU control processor.

Note that the virtual HW reset message may be received in either the data or control message slot. The virtual HW reset message is illustrated in Table 27 and Figure 61 below.

The most significant bit of each message field is transmitted first (refer to Figure 11).

Table 27: Content of virtual HW reset message.

Field	Value
Address	Address of the node that requires reset
Type	01101 (Virtual HW Reset)
Timestamp	000000
Payload data, 14 bytes	All zeros
CRC check, 16 bits	CRC check sum computed over the header and payload (see Section 4.4.9.3).

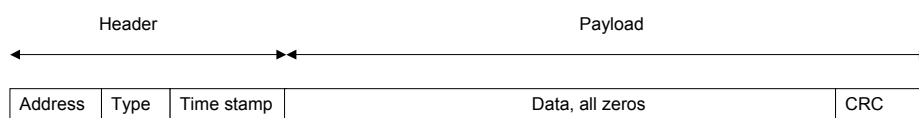


Figure 61: Virtual HW reset message.

7 OAM&P

7.1 OAM&P Parameters

Operation of RP3 interface protocol is controlled through parameters. In this section, all parameters of the protocol are defined. Also error cases are considered.

7.1.1 External Parameters of Data Link Layer

In Table 28 external parameters of the Data link layer are listed. Application layer has access to all Data link layer parameters and input parameters are set by the Application layer.

Table 28: Input and output parameters of Data link layer.

Parameter	Input/Output	Register width	Description
M_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of message slots in a Message Group (refer to Section 4.2.2 for details). $0 < M_MG < 65536$.
N_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of Message Groups in a Master Frame (refer to Section 4.2.2 for details). $0 < N_MG < 65536$.
K_MG	Input	5 bits, positive number (no sign bit)	Specifies the number of IDLE bytes at the end of Message Group (refer to Section 4.2.2 for details). $0 < K_MG < 20$.
DATA_MESSAGE_SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in downlink direction. Takes values from 0 up to $i*(M_MG-1)*N_MG-1 < 2^{32}$ (refer to Section 4.2.2 for definition of M_MG and N_MG).

Reference Point 3 Specification

Parameter	Input/Output	Register width	Description
DATA_MESSAGE_SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in uplink direction. Takes values from 0 up to $i*(M_MG-1)*N_MG-1 < 2^{32}$.
CONTROL_MESSAGE_SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in downlink direction. Takes values from 0 up to $i*N_MG-1$.
CONTROL_MESSAGE_SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in uplink direction. Takes values from 0 up to $i*N_MG-1$.
BLOCK_SIZE	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Defines the number of bytes within a block. (Reset value is 400)
SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid blocks of bytes which result in state WAIT_FOR_K28.7_IDLE. (Reset value is 255)
UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid blocks of bytes which result in state UNSYNC. (Reset value is 255)
FRAME_SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid Message Groups which result in state FRAME_SYNC. (Reset value is 1920)
FRAME_UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid Message Groups which result in state WAIT_FOR_K28.7_IDLE. (Reset value is 128)
TRANSMITTER_EN	Input	1 bit	For each transmitter separately. Value '1' enables transmission to the bus (if other conditions are also fulfilled) while value '0' disables transmission (see Section 4.2.7). (Reset value is '0').
LOS_ENABLE	Input	1 bit	For each transceiver separately. This parameter enables (value '1') or disables (value '0') the impact of signal LOS to transmitter state machine. See Section 4.2.7. (Reset value is '1')

Parameter	Input/Output	Register width	Description
DELTA (Δ)	Input	16 bits, two's complement code	In a general case, a common Δ value exists for all uplink bus transmitters of a node. Another common value exists typically for all downlink transmitters of a node. Link-specific Δ values are also allowed. Value of Δ is given in byte-clock ticks.
PI (Π)	Input	16 bits, two's complement code	In a general case, a common value exists for all uplink receivers of a bus node. A common value is typically used for all downlink receivers of a node. Receiver-specific Π values are also allowed. Value of Π is given in byte-clock ticks.
MAX_OFFSET	Input	1 bit	Common value for a node. Defines the width of the allowed window for Master Frame boundary (see Section 4.2.5). MAX_OFFSET equals to 4 (the default value) for bit value '0' while MAX_OFFSET is equal to 8 for '1'
SYNCHRONISATION_STATUS	Output	4 bits	For each transceiver separately. Indicates the status of the transceiver (see Section 4.2.7). State encodings are the following. UNSYNC: 1000 WAIT_FOR_K28.7_IDLES: 0100 WAIT_FOR_FRAME_SYNC_T: 0010 FRAME_SYNC: 0001
SYNC_STATUS_CHANGE	Output	Interrupt	Application layer is interrupted always when a receiver state machine changes state.

1

2 7.1.2 Error Cases at Data Link Layer

3 In Table 29, possible error cases at Data Link layer are defined.
4 In case of RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE,
5 error recovery is left to Application layer.

6 7.1.3 External Parameters of Transport Layer

7 In this section, parameters of the Transport layer are listed, see Table
8 30. Application layer has access to all parameters; input parameters are
9 set by Application layer.

10

1 *Table 29: Error cases at Data link layer.*

Error	Register width	Description
RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE	1 bit	For each receiver port (transceiver) separately. This error is indicated when received Master Frame is detected outside the allowed MAX_OFFSET+1 wide window (see Section 4.2.5). Value '0' indicates offset within the allowed range while '1' indicates out-of-range situation.

2

3 *Table 30: Input and output parameters of Transport layer. All the parameters*
4 *are defined for the whole node.*

Parameter	Input/Output	Register width	Description
RP3_ADDRESS	Input	13 bits	At least one address shall be supported per device based on which RP3 message reception is performed. The 8 bit wide node address shall be programmable while the 5 bit wide sub-node address may be hard-wired to the device. Note that in message transmission, Application layer may use several addresses when constructing and transmitting messages.
DL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that DL routing table is used to route messages that are received from the transceiver.
UL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that UL routing table is used to route messages that are received from the transceiver.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESSES_DL	Input	4 bits	Specifies number of bits in a transformed address in downlink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESSES_UL	Input	4 bits	Specifies number of bits in a transformed address in uplink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.
LSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_DL	Input	32 bits	Downlink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.

Parameter	Input/Output	Register width	Description
LSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_UL	Input	32 bits	Uplink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_DL	Input	20 bits	Downlink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_UL	Input	20 bits	Uplink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
DL_ROUTING_TABLE	Input	$A \cdot T$ bits	A table with A rows and T bits per row. A stands for $2^{DL_TRANSFORMED_ADDRESS_RANGE}$, while T denotes total number of transceivers both at Application and Physical layers. The values of parameters A and T can be fixed and they take values in the range $0 < A \leq 2^{13}$ and $0 < T \leq 48$.
UL_ROUTING_TABLE	Input	$A' \cdot T$ bits	A table with A' rows and T bits per row. A' stands for $2^{UL_TRANSFORMED_ADDRESS_RANGE}$, while T denotes total number of transceivers both at Application and Physical layers. The values of parameters A' and T can be fixed and they take values in the range $0 < A' \leq 2^{13}$ and $0 < T \leq 48$.
MULTIPLEXING_TABLE	Input	32 bits (4*8 bits)	For each multiplexer and demultiplexer separately. Vector containing four elements $E_{i_{out}} = (D, k, j_k)$. The first i elements of the vector are used for output (multiplexer)/input (demultiplexer) line rate $i \cdot 768$ Mbps. D exists in the most significant bit and values '0' and '1' are allowed, k field is three bits wide and may take values in the range of 0-7 (0x0-0x7 in hex), while j_k is located in the four least significant bits and it may take values in the range 0-15 (0x0-0xF in hex). See Section 4.3.4 for the definition of $E_{i_{out}} = (D, k, j_k)$.
SUMMING_ALLOWED_FOR_TYPE	Input	32 bits	Value '1' in bit Index N indicates that messages of type N may be summed together. The least significant (rightmost) bit has Index 0 while most significant bit has Index 31. Refer to Table 11 for message type definitions and Section 4.3.5 for an example of SUMMING_ALLOWED_FOR_TYPE parameter.

7.1.4 Error Cases at Transport Layer

In Table 31: Possible error cases at Transport layer. the possible error cases at Transport layer are defined. Refer to RP3 compatible chip (ASIC) functional specifications for detailed descriptions on these error indicators.

Table 31: Possible error cases at Transport layer.

Error	Register width	Description
DL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. There exists no output port corresponding to the address of the received message (all-zero bit vector exists for the address in the routing table (see Table 4)).
UL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specification. Operation is the same than in case of DL_MESSAGE_REJECTED above. UL_MESSAGE_REJECTED applies for UL direction.
MESSAGE_COLLISION	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. Refer to Section 4.3.5 for a definition of message collision.

7.1.5 Other External Parameters

In this section, parameters that may be applied at any protocol layer are listed, see Table 32: Other input and output parameters of bus node. Thus, the functionality corresponding to the parameters can be implemented at any protocol layer.

Physical layer shall be able to detect and report line code violations (see Section 4.1.2).

For each receiver port (link) separately, Loss Of Signal (LOS) defect reporting shall be supported. If N_LCV or more line code violations occur during period T_LCV, a LOS defect shall be reported. The LOS defect shall be removed when no LCVs occur in period T_LCV. LOS

defect functionality can be implemented at any layer of the protocol stack.

Table 32: Other input and output parameters of bus node.

Parameter	Input/Output	Register width	Description
N_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Threshold value for Line Code Violation (LCV) defect reporting (see algorithm below). Reset value is 1.
T_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Parameter defining period for LCV defect monitoring. T_LCV specifies the period in number of received 8b10b line codes. Reset value is $N_MG \cdot (M_MG \cdot 19 + K_MG)$.
LOS_DEFECT	Output	1 bit	For each receiver port separately. Value '1' indicates Loss Of Signal (LOS) while value '0' denotes normal operation (reset value)
MESSAGE_TX_RULE	Input	33 bits	There may exist several message transmission rules per a bus node. The most significant bit defines the message slot counter that is used in message transmission. '0' stands for data message slot counter while '1' refers to control slot counter. The following 16 bits contain the index I and the 16 least significant bits contain the modulo M (refer to Section 4.4.3 for the definition of I and M).
MAX_SYNCHRONIZATION_TIME	Input	32 bits, positive number	Common value for a node. Time limit for the line rate auto-negotiation algorithm (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 153600000 (5 seconds).
MAX_RX_TIME	Input	32 bits, positive number	Common value for a node. Reception time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 19660800 (0.64 seconds).
TX_TIME	Input	32 bits, positive number	Common value for a node. Transmission time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 6144000 (200 ms).

Appendix A: Media Adapter and Media Options – Fibre Optics

Table 33 lists the media options that shall be used.

Table 33: Options for optical cabling.

Type	Related Standard
50 µm Multimode	IEC 60793-2-10:2002, Type A1a [7]
62.5 µm Multimode	IEC 60793-2-10:2002, Type A1b [7]
Singlemode	IEC 60793-2-50:2002, Type B1 [8]

Table 34 proposes optical transceiver candidates for each line rate. OBSAI recommends to apply Fiber channel interface requirements to RP3-01 as specified by Subclauses 6.2 and 6.3 of [9].

Table 34: Optical interface recommendations for different RP3-01 line rates. This table is for information only.

Line Rate	50 µm Multimode Fiber	62.5 µm Multimode Fiber	Singlemode Fiber
768 Mbps	100-M5-SN-I in [9]	100-M6-SN-I in [9]	100-SM-LC-L in [9]
1536 Mbps	200-M5-SN-I in [9]	200-M6-SN-I in [9]	200-SM-LC-L in [9]
3072 Mbps	400-M5-SN-I in [9]	400-M6-SN-I in [9]	400-SM-LC-L in [9]

OBSAI mandates the use of SFP (Small Form-factor Pluggable) transceivers. Connector type is not recommended but the ORL (Optical Return Loss) of the used connector should fulfil PC (Physical Contact) requirement ORL<-30 dB for singlemode and TIA/EIA 568 requirement (ORL<-20 dB) for multimode applications. Super PC (ORL<-40 dB) is recommended for complex installations especially at 1550 nm wavelength.

Appendix B: Multiplexing Examples (Informative)

Figure 62 provides an example of a Transport layer configuration. The message router and summing unit are defined here to operate at the lowest RP3 line rate used in the system. Demultiplexers are used to split high data rate RP3 links into several low rate links which may then be multiplexed back to high rate links after summing. RP3 line rates are configured or identified at BTS startup so multiplexer and demultiplexer blocks as well as router and summing blocks can be configured accordingly. For detailed information on message multiplexer, demultiplexer, and router operations, refer to Section 4.3.

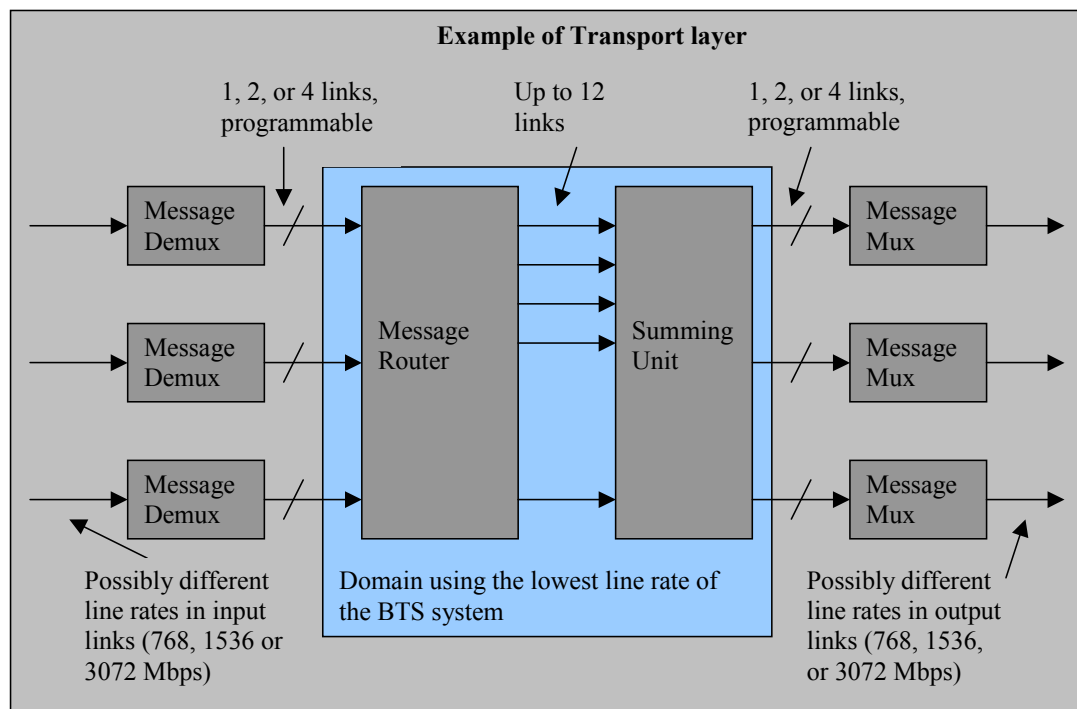
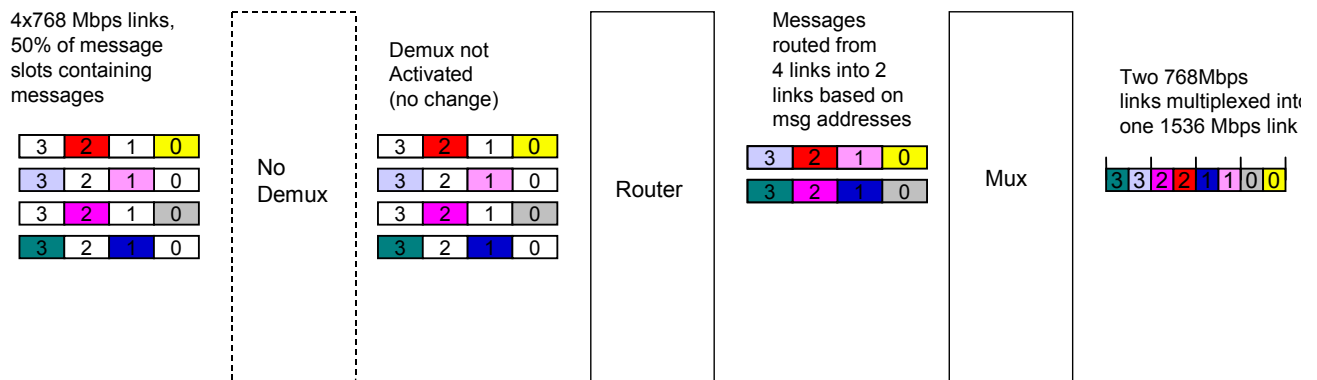


Figure 62: Example block diagram of Transport layer.

Figure 63 illustrates message multiplexing from four 50% full RP3 links into one 1536 Mbps. The concept presented in Figure 62 has been applied for this and other examples presented in this section.

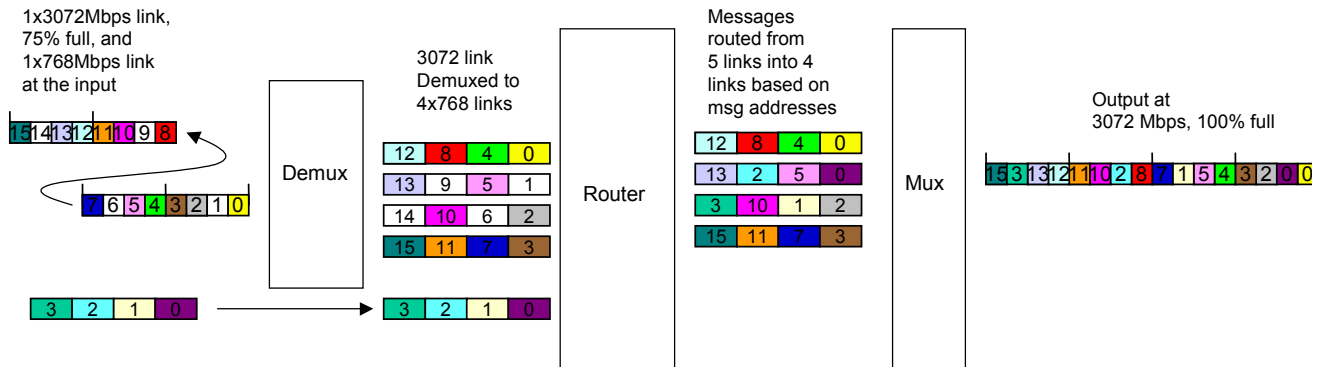


Empty messages shown in white,
each antenna-carrier with an unique color
(WCDMA case assumed)

Figure 63: An example of message multiplexing from four 768 Mbps links into one 1536 Mbps link.

Figure 64 illustrates message interleaving from a single 768 Mbps RP3 link into a 3072 Mbps link. Such a case may be valid in the uplink direction when data from an RRU is interleaved to RP3-01 in a chain topology.

Illustrates e.g. data interleaving at an RRU to a chained fiber in UL direction



Empty messages shown in white,
each antenna-carrier with an unique color
(WCDMA case assumed)

Figure 64: An example of message interleaving from one 768 Mbps link into one 3072 Mbps link.

Figure 65 and Figure 66 illustrate RP3 multiplexing in a possible BTS configuration where uplink data from several low capacity RRUs is forwarded to base band for processing. The configuration shown reduces the number of RP3 links at the base band modules.

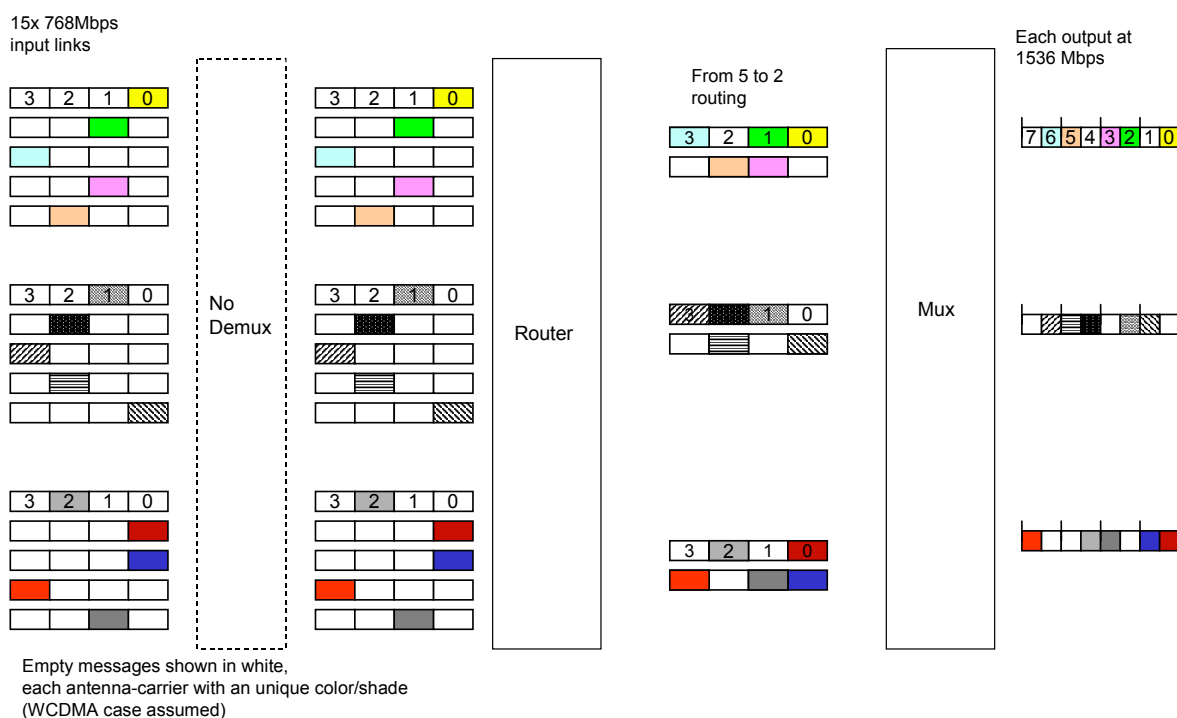


Figure 65: An example of message interleaving from fifteen 768 Mbps links into three 1536 Mbps link.

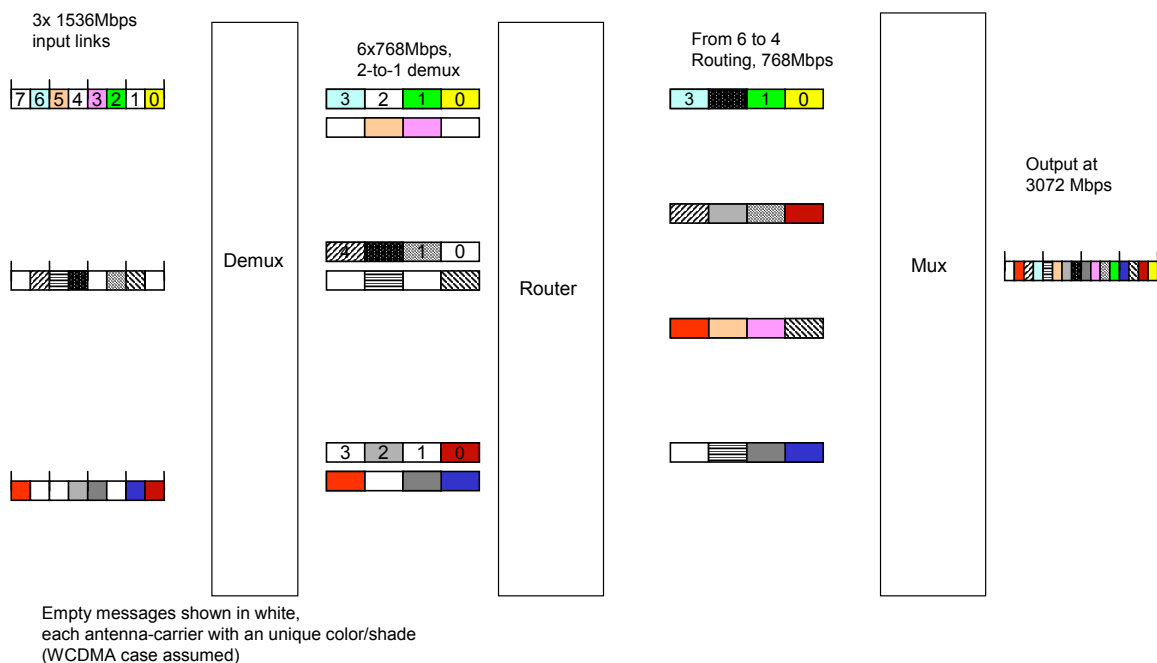


Figure 66: An example of message interleaving from three partly full 1536 Mbps links into one 3072 Mbps link.

Appendix C: RP3 Bus Configuration Algorithm (Informative)

An example of the RP3 bus configuration is provided in this section for the base station configuration illustrated in Figure 67. We use a two sector WCDMA base station with a single TX antenna and two RX antennas per sector. There are two carriers per each antenna so a 2+2 configuration is illustrated. As can be seen from the figure, a base-station architecture with combiner and distributor is used but the configuration principles apply also to the mesh architecture. In this example, we split the 13 bit RP3 address into an 8 bit node address (MSB) and a 5 bit sub-node address, where the node address identifies a module and the sub-node address specifies the antenna-carrier. RP3 links with a 768Mbps baud rate are assumed.

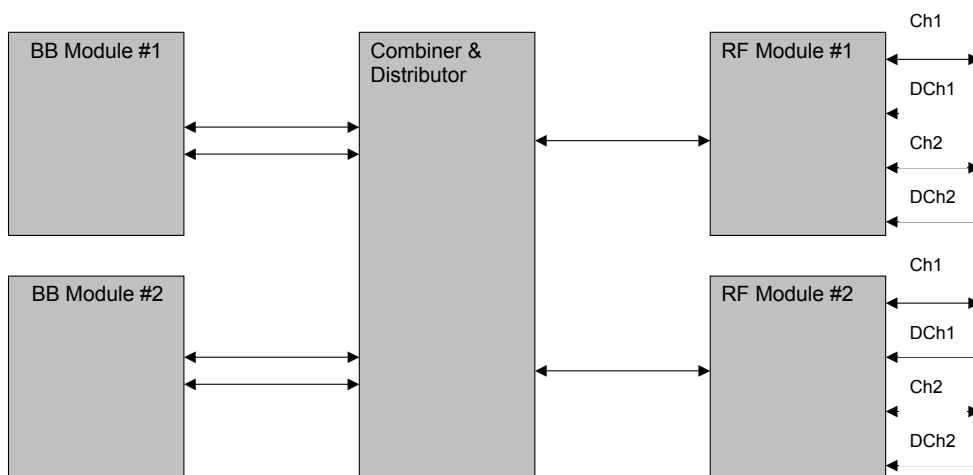


Figure 67: An example base station configuration.

Figure 68 illustrates data flows between the RF and BB modules. Each antenna-carrier is drawn separately to the figure and mapping of the antenna carriers to RP3 links is provided. Also node and sub-node addresses for different modules and antenna-carriers are provided. In this example, node addresses 1 and 2 have been allocated to BB

modules while node addresses 16 and 32 (in decimal numbers) are applied to RF modules. Antennas-carriers in each RF module are numbered from 1 to 4.

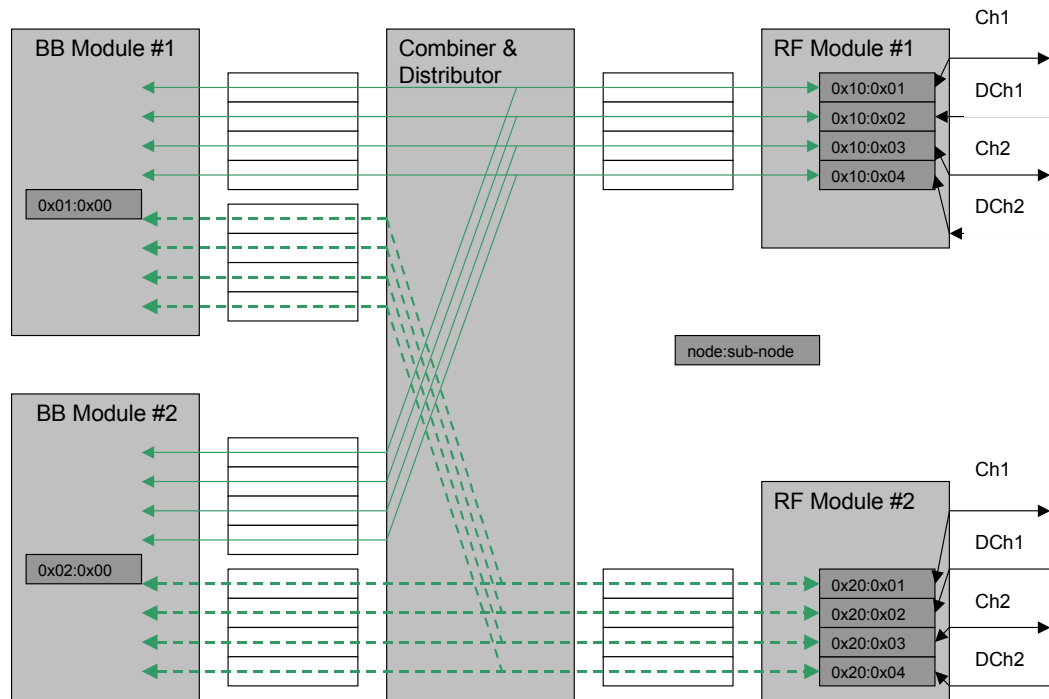


Figure 68: Data flows between BB and RF modules. Addresses of modules and antenna-carriers (or up/down converters at RF) are also shown.

Parameters for the message routing, multiplexing, and demultiplexing blocks of the combiner and distributor must be provided at base station start up. In this example, multiplexing and demultiplexing blocks are not used. Message routing tables are applied to the message routing between BB and RF modules. The routing tables define the output port or ports that correspond to each address. In the downlink direction, a point-to-point message transfer is typically applied so there exists a single output port index for each address in the downlink routing table. In uplink direction, the same message may be multicast to several BB modules for processing and because of this several output ports exist corresponding to an address in the uplink routing table.

In Figure 69, the port indices of the combiner distributor are shown, while downlink and uplink routing tables are provided in Table 35 and Table 36, respectively. In this example, we assume that the combiner distributor performs message routing based on the node address only.

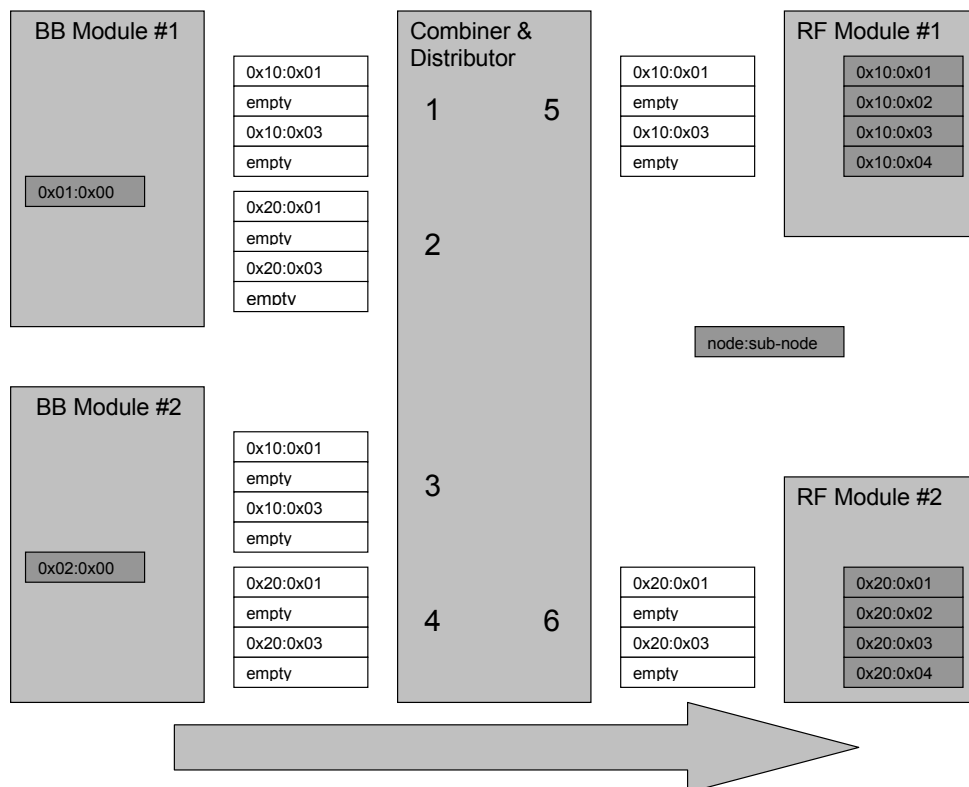


Figure 69: Index assignment to the ports of combiner distributor. Mapping of downlink messages to RP3 message slots is also shown.

Table 35: Downlink routing table.

Address Field (Target Address)	Output Port
0x10	5
0x20	6

Table 36: Uplink routing table.

Address Field (Source Address)	Output Ports
0x10	1, 3
0x20	2, 4

In addition to address assignment and the definition of routing tables, message transmission rules must also be defined in the BB and RF modules that form the end nodes of the bus. Table 37, Table 38, and

Table 39 define the message transmission rules applied by the BB modules, RF module #1, and RF module #2, respectively. Figure 69 shows also how messages are mapped into the message slots of the RP3 links in the downlink direction, while Figure 70 illustrates the uplink case.

Table 37: Message transmission rules for BB modules #1 and #2.

Target	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x03	Link 1, 2 / 4
0x20: 0x01	Link 2, 0 / 4
0x20: 0x03	Link 2, 2 / 4

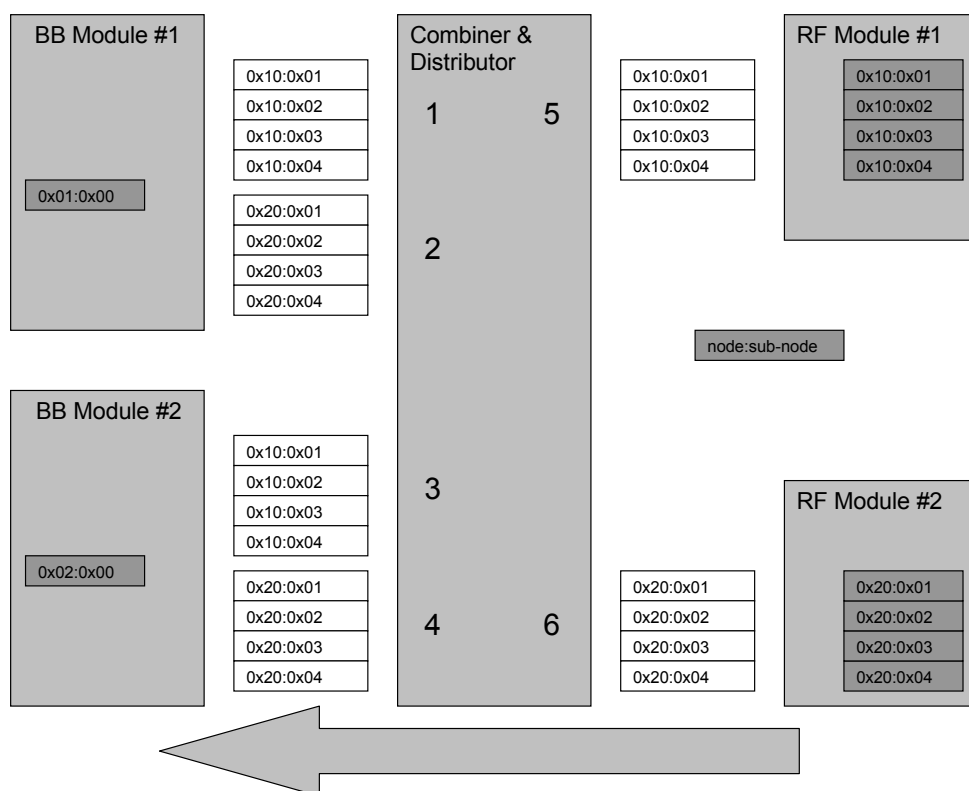
Table 38: Message transmission rules for RF module #1.

Source	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x02	Link 1, 1 / 4
0x10: 0x03	Link 1, 2 / 4
0x10: 0x04	Link 1, 3 / 4

1

Table 39: Message transmission rules for RF module #2.

Source	Link, Index/ modulo
0x20: 0x01	Link 1, 0 / 4
0x20: 0x02	Link 1, 1 / 4
0x20: 0x03	Link 1, 2 / 4
0x20: 0x04	Link 1, 3 / 4



2

3

Figure 70: Mapping of uplink messages to RP3 message slots.

Appendix D: Parameters for 802.16 Message Transmission

The parameters required for 802.16 data message transmission are provided in Table 40 for currently supported 802.16 profiles, i.e.

Table 40: Parameters for supported 802.16 profiles in case of 768 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	10	1	0x5	3	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
2.5	144/125	2.88	5	1	0x2	3	0x0	0
3	86/75	3.44	4	1	0x2AA95552AAA	43	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	144/125	5.76	2	1	0x5	3	0x0	0
5.5	316/275	6.32	2	1	0x2A54A952A54A952A54AA	79	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
10	144/125	11.52	1	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	10	1	0x7FFFFFFFD	35	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	28/25	5.6	2	1	0x6EEEEEEED	35	0x0	0
5.5	28/25	6.16	2	1	0x0AAAAAAAAAAAAAAAAAAAAA	77	0x0	0
6	28/25	6.72	2	1	0x12	7	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
8.75	8/7	10	1	2	0xAAAD555AAD555	56	0x1555	13
10	28/25	11.2	1	1	0x24A4A4A4A	35	0x0	0
14	8/7	16	0	0	0xFALSE	0	0x0	0
17.5	8/7	20	0	0	0xFALSE	0	0x0	0
20	28/25	22.4	0	0	0xFALSE	0	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	3	2	0x00040010004002	56	0x0002	13

sampling rates (channel bandwidths) and OFDM/OFDMA multiple access methods. For each profile, the values of six different parameters are defined. Refer to Table 10 for the description of these parameters.

Table 41: Parameters for supported 802.16 profiles in case of 1536 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	21	1	0x2	3	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
2.5	144/125	2.88	10	1	0x5	3	0x0	0
3	86/75	3.44	8	1	0x7FFDFFF7FFD	43	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	144/125	5.76	5	1	0x2	3	0x0	0
5.5	316/275	6.32	4	1	0x7EFD7BF7E7EFD7BF7EFD	79	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
10	144/125	11.52	2	1	0x5	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	21	1	0x7FFFBFFFD	35	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	28/25	5.6	5	1	0x2AAAAAAAA	35	0x0	0
5.5	28/25	6.16	4	1	0x1FFFFFFFFFFFFFFFFFFD	77	0x0	0
6	28/25	6.72	4	1	0x55	7	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
8.75	8/7	10	3	2	0x00040010004002	56	0x0002	13
10	28/25	11.2	2	1	0x6EEEEEEED	35	0x0	0
14	8/7	16	1	1	0x1FFDFFD	25	0x0	0
17.5	8/7	20	1	2	0xAAAD555AAD555	56	0x1555	13
20	28/25	22.4	1	1	0x24A4A4A4A	35	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	6	1	0x00408102040810204082	77	0x040810204082	48

Table 42: Parameters for supported 802.16 profiles in case of 3072 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	42	1	0x5	3	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
2.5	144/125	2.88	21	1	0x2	3	0x0	0
3	86/75	3.44	17	1	0x7EFD7BF7EFD	43	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	144/125	5.76	10	1	0x5	3	0x0	0
5.5	316/275	6.32	9	1	0x6EDDBBB76EEDDBBB76ED	79	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
10	144/125	11.52	5	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	43	1	0x7F7FBFD7D	35	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	28/25	5.6	10	1	0x7FFFFFFFD	35	0x0	0
5.5	28/25	6.16	9	1	0x1FFFFFFFFF7FFFFFFFFFD	77	0x0	0
6	28/25	6.72	9	1	0x02	7	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
8.75	8/7	10	6	1	0x00408102040810204082	77	0x040810204082	48
10	28/25	11.2	5	1	0x2AAAAAAAA	35	0x0	0
14	8/7	16	3	1	0x1F7DF7D	25	0x0	0
17.5	8/7	20	3	2	0x00040010004002	56	0x0002	13
20	28/25	22.4	2	1	0x6EEEEEEED	35	0x0	0
28	8/7	32	1	1	0x1FFDFFD	25	0x0	0
4.375	8/7	5	12	2	0x122448912244892	59	0x12	7

Appendix E: Background Information on TYPE 1 – 3 Interconnects (Informative)

TYPE 1 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplane and cable while TYPE 2 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplanes. Figure 71 illustrates TYPE 1 and TYPE 2 interconnects.

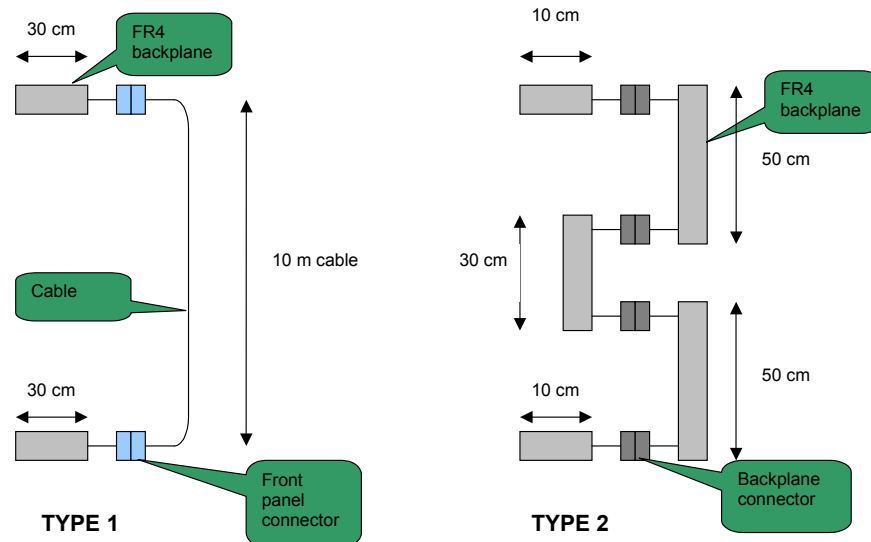


Figure 71: TYPE 1 and TYPE 2 Interconnects.

TYPE 3 Channel is defined as a serial interconnect at 768, 1536, or 3072Mbaud data rate across backplane or cable.

The backplane channel is defined as entirely passive link consists of two line cards interconnect across backplane through two OBSAI – RP3 backplane connectors as depicted in Figure 72 and meet the following limitations:

- Line Card maximum trace length is 100mm (4")
- Backplane maximum trace length is 800mm (31.5")
- 6 PTH's across the channel from Tx to Rx points

- 1 • Two OBSAI RP3 backplane connectors
- 2 • PCB materials is made of commonly used standard FR4

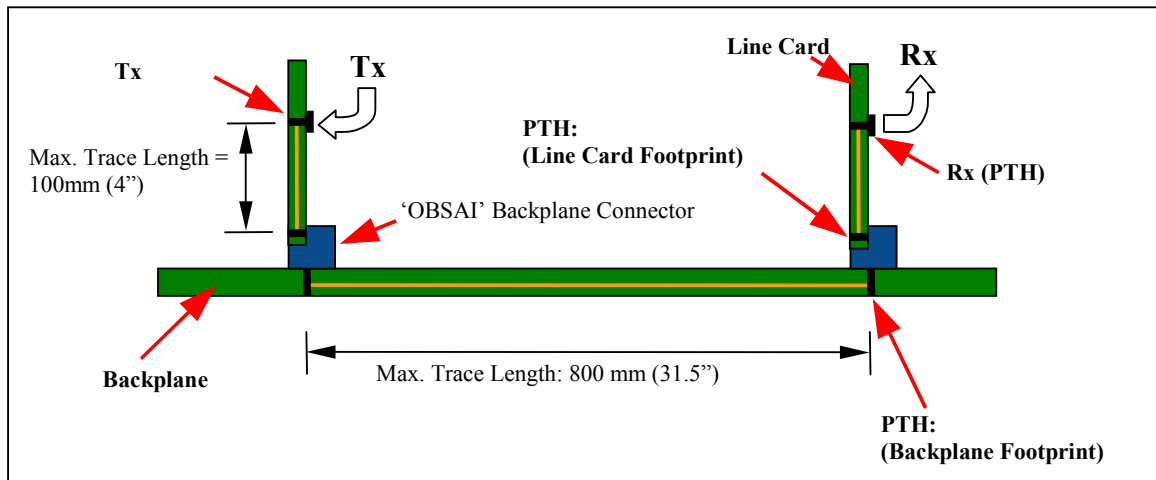


Figure 72: TYPE-3 Backplane Interconnect

The cable channel is defined as entirely passive link consists of two line cards interconnect across cable assembly terminated with OBSAI – RP3 front access connectors (Slim-I/O) as depicted in Figure 73 and meet the following limitations:

- Line Card maximum trace length is 50mm (2")
- Cable Assembly maximum length is 3m (9ft)
- 4 PTH's across the channel from Tx to Rx points
- Two OBSAI RP3 front access panel connectors (aka Slim-I/O)
- PCB materials is made of commonly used standard FR4
- Cable diameter and conductors AWG shall be determined based on the requirements (refer [11])

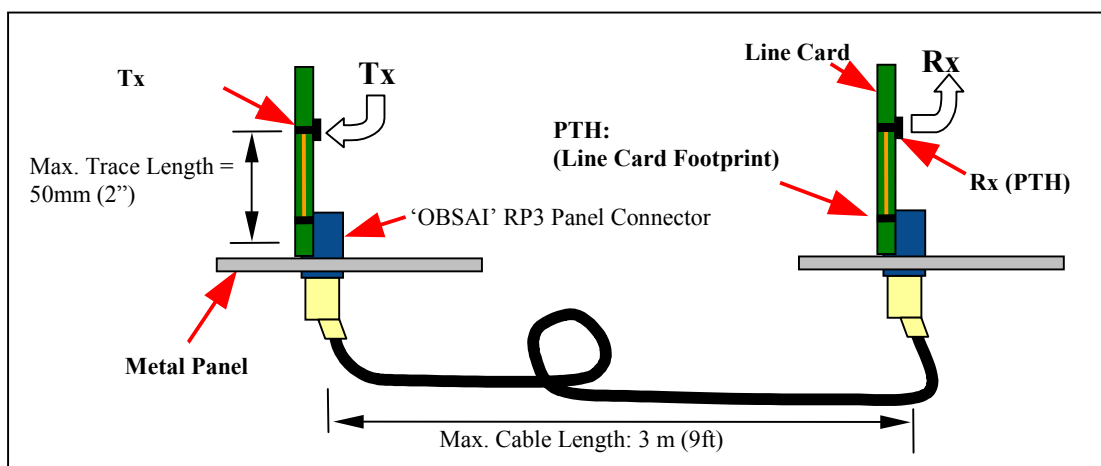


Figure 73: TYPE-3 Cable Interconnect

1 Glossary

2 Abbreviations

BB	Baseband module
BTS	Base transceiver system
C/D	Combiner and distributor
CCM	Control and clock module
DL	Downlink direction from BTS to RRUs
HW	Hardware
LC	Local Converter that interfaces to RP3 and RP1 and combines them to RP3-01 and vice versa. Local Converter is referred to as Local cabinet in [2].
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
RP3-01	Extension of RP3 protocol where RP1 data is mapped into RP3 messages
RRU	Remote RF unit. RRU is referred to as Remote cabinet in [2].
SFN	System frame number
UL	Uplink direction from RRUs to BTS

3

4 Definition of Terms

5 None listed.

References

- [1] A.X. Widmer and P.A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM Journal of Research and Development, vol. 27, no. 5, pp. 440-451, Sept. 1983.
- [2] Open Base Station Architecture Initiative, BTS System Reference Document.
- [3] IEEE 802.3ae Standard for Information Technology – Local & Metropolitan Area Networks – Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications-- Media Access Control (MAC) Parameters, Physical Layer, and Management Parameters for 10 Gb/s Operation
- [4] Open Base Station Architecture Initiative, Reference Point 1 Specification, Section 8.4.
- [5] Open Base Station Architecture Initiative, Baseband Module Specification.
- [6] Open Base Station Architecture Initiative, RF Module Specification.
- [7] IEC 60793-2-10 (2002-3) Part 2-10: Product specifications sectional specification for category A1 multimode fibres, March 2002
- [8] IEC 60793-2-50 (2002-1) Part 2-50: Product specifications sectional specification for class B single-mode fibres, January 2002
- [9] INCINTS 352 – Fibre Channel 1998 Physical Interface (FC-PI'98), 1998.
- [10] IEEE 802.3 Standard for Information Technology – Telecommunication and Information Exchange Between Systems – Local and Metropolitan Area Networks – Specific Requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
- [11] Open Base Station Architecture Initiative, BTS System Reference Document, Appendix F.

TAB C



Reference Point 3 Specification

Version 4.1

Contents

1	Summary of Changes	13
2	Scope	14
3	Reference Point 3 Architecture	15
3.1	Parameter Definitions.....	15
3.2	Module Interface Toward RP3	16
3.3	Topology	17
3.3.1	Mesh	17
3.3.2	Centralized Combiner and Distributor	19
3.4	Inter-Cabinet Connections	21
3.4.1	Inter-Cabinet Mesh	21
3.4.2	Connections between Bridge Modules.....	22
3.4.3	Connections between Combiner and Distributor Modules	23
4	Protocol Stack	25
4.1	Physical Layer.....	26
4.1.1	Electrical Signalling.....	26
4.1.2	Data Format and Line Coding.....	26
4.1.3	Bus Clock.....	27
4.2	Data Link Layer.....	27
4.2.1	Message Overview	27
4.2.2	Frame Structure	28
4.2.3	Bit Level Scrambling for 6144 Mbps (8x) Line Rate	31
4.2.4	Counters	34
4.2.5	Transmission of Frame Structure.....	35
4.2.6	Reception of Frame Structure.....	36
4.2.7	Empty Message	39
4.2.8	Synchronisation	39
4.2.9	Measurements	44
4.3	Transport Layer.....	44
4.3.1	Overview of Transport Layer.....	45
4.3.2	Message Format – Address Field	48
4.3.3	Message Router.....	49

4.3.4	Message Multiplexer and Demultiplexer	50
4.3.5	Summing Unit	52
4.4	Application Layer.....	54
4.4.1	Addressing	54
4.4.2	Paths.....	55
4.4.3	Message Transmission Rules	56
4.4.4	Bus Manager.....	58
4.4.5	Buffering Requirements	58
4.4.6	Message Format – TYPE Field	59
4.4.7	Message Format – TIMESTAMP Field	60
4.4.8	Message Format – PAYLOAD Field	61
4.4.9	Control and Measurement Data Mapping	66
5	Electrical Specifications	71
5.1	Overview	71
5.1.1	Explanatory Note on Electrical Specifications	71
5.1.2	Compliance Interconnect	72
5.1.3	Equalization	72
5.2	Receiver Characteristics	73
5.2.1	AC Coupling.....	74
5.2.2	Input Impedance	74
5.2.3	Receiver Compliance Mask	75
5.2.4	Jitter Tolerance	76
5.2.5	Bit Error Ratio (BER).....	77
5.3	Transmitter Characteristics	77
5.3.1	Load	80
5.3.2	Amplitude	80
5.3.3	Output Impedance	81
5.3.4	Transmitter Compliance	81
5.4	Measurement and Test Requirements	82
5.4.1	TYPE 1 Compliance Interconnect Definition	82
5.4.2	TYPE 2 Compliance Interconnect Definition	83
5.4.3	TYPE 3 Compliance Interconnect Definition	84
5.4.4	TYPE 4 and TYPE 5 Compliance Interconnect Definition	85

5.4.5	Eye Mask Measurements for TYPE 1, 2, and 3 Compliant Interconnects	88
5.4.6	Transmit Jitter for TYPE 1, 2, and 3 Compliant Interconnects	89
5.4.7	Jitter Tolerance	89
5.4.8	Noise and Crosstalk	89
6	RP3-01 Interface for Remote RF Unit.....	90
6.1	Architecture	90
6.2	Protocol Stack	92
6.2.1	Physical Layer	92
6.2.2	RP3-01 - Transfer of RP1 Data Over RP3	92
6.2.3	RP1 Frame Clock Bursts	92
6.2.4	Ethernet Transmission	97
6.2.5	Line Rate Auto-Negotiation	100
6.2.6	RTT Measurement and Internal Delays of a RRU	102
6.2.7	Virtual HW Reset	105
7	OAM&P.....	107
7.1	OAM&P Parameters	107
7.1.1	External Parameters of Data Link Layer	107
7.1.2	Error Cases at Data Link Layer	109
7.1.3	External Parameters of Transport Layer	110
7.1.4	Error Cases at Transport Layer	112
7.1.5	Other External Parameters	113
	Appendix A: Media Adapters and Media Options.....	115
	Appendix B: Multiplexing Examples (Informative)	117
	Appendix C: RP3 Bus Configuration Algorithm (Informative).....	120
	Appendix D: Parameters for 802.16 Message Transmission.....	125
	Appendix E: Background Information on Interconnects (Informative).....	129
	Appendix F: Parameters for LTE Message Transmission	134
	Appendix G: Parameters for GSM/EDGE/EGPRS2 Message Transmission....	136
	Glossary	142
	References	143

List of Figures

Figure 1: RP3 interface of RF and baseband modules. There exists a maximum of K pairs of unidirectional links toward RP3.....	17
Figure 2: Full mesh connecting two baseband and three RF modules. Each baseband module is connected to every RF module and vice versa.	18
Figure 3: Full mesh connecting K baseband modules to K RF modules. All the connections are not drawn.	19
Figure 4: Centralized combiner and distributor (main and redundant) embedded into RP3 interface.	20
Figure 5: Centralized combiner and distributor embedded into RP3 interface. Redundant C/D is not applied.	21
Figure 6: Full mesh between RF and baseband modules of two cabinets.	22
Figure 7: Bridge modules extending RP3 interface to two cabinets. Mesh topology is shown in intra-cabinet RF-baseband connections but also centralized combiner and distributor topology may be applied.....	23
Figure 8: RP3 interface extended over two cabinets by connecting C/Ds together (redundant C/D not applied).	24
Figure 9: Layered structure of the bus protocol.	25
Figure 10: Illustration of possible physical layer loopback points.	26
Figure 11: Illustration of Physical layer structure – data flow approach.....	26
Figure 12: Message format of RP3 protocol stack.....	28
Figure 13: Master frame illustrating the sequence according to which WCDMA, GSM/EDGE, 802.16, and LTE messages are inserted to the bus (parameter set $M_MG=21$, $N_MG=1920$, $K_MG=1$, $i = 1$).....	29
Figure 14: Master frame illustrating the sequence according to which CDMA messages are inserted to the bus (parameter set $M_MG=13$, $N_MG=3072$, $K_MG=3$, $i=1$).....	30
Figure 15: Message group structures for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards at 768 Mbps (1x), 1536 Mbps (2x), 3072 Mbps (4x), and 6144 Mbps (8x) line rates. Time span corresponding to a single message group at 768 Mbps line rate is shown.	30
Figure 16: Scrambling Pattern Passed Between Two Adjacent RP3 Nodes.	31
Figure 17: Scrambling Training Patterns.	33
Figure 18: 7-Degree Polynomial Scrambler.....	33
Figure 19: Timing of message slot counters for an example MG and MF definition. .	35
Figure 20: Master Frame is transmitted at an offset to the RP3 bus frame tick in each bus node.	36
Figure 21: Run time and measurement windows of received Master Frame.....	37

Figure 22: An example of Master Frame timings.....	38
Figure 23: Example of Δ and II assignments to a bus network.	38
Figure 24: Empty message. The address field consists of thirteen '1' bits while rest of the message contains don't care x bits.	39
Figure 25: State diagram of the transmitter.	41
Figure 26: State diagram for the receiver.	43
Figure 27: Transport layer with a common message router for all received messages.	46
Figure 28: Transport layer with dedicated downlink and uplink message routers. Also message multiplexer, demultiplexer, and summing unit is shown.	47
Figure 29: Address sub-fields.	48
Figure 30: Functionality of message router.	49
Figure 31: Illustration of message multiplexer.	52
Figure 32: Functionality of Summing unit. Type check of input messages is not shown.	54
Figure 33: Arbitrary bus configuration with two paths. Message slots are not shown.	55
Figure 34: 802.16 data transmission into RP3 link using Dual Bit Map algorithm.....	58
Figure 35: WCDMA DL Payload Mapping.	61
Figure 36: WCDMA UL Payload Mapping.	62
Figure 37: GSM/EDGE/EGPRS2 Uplink Payload Data Mapping	63
Figure 38: CDMA2000 DL Payload Mapping.....	64
Figure 39: CDMA2000 UL Payload Mapping.....	65
Figure 40: 802.16 downlink and uplink payload mapping.	65
Figure 41: LTE downlink and uplink payload mapping.	66
Figure 42: Generic control message.	66
Figure 43: Air interface synchronized control message.....	68
Figure 44: Receiver Compliance Mask.....	75
Figure 45: Sinusoidal Jitter Mask	76
Figure 46: Transmitter Output Mask.....	80
Figure 47: TYPE 1 Compliance Interconnect Differential Insertion Loss	83
Figure 48: TYPE 2 Compliance Interconnect Differential Insertion Loss	83
Figure 49: TYPE 3 Differential Transfer Function Chart.....	84
Figure 50: TYPE 3 Differential Return Loss Chart.....	85
Figure 51: OIF reference model.	86

<i>Figure 52: Eye Mask Alignment.....</i>	<i>88</i>
<i>Figure 53: RP3-01 example architecture.....</i>	<i>90</i>
<i>Figure 54: Logical model of OBSAI RP3-01 point-to-point interface.....</i>	<i>91</i>
<i>Figure 55: Examples of mapping RP1 and RP3-01 link O&M data into RP3 messages.....</i>	<i>93</i>
<i>Figure 56: RP1 frame clock synchronization burst from CCM.....</i>	<i>93</i>
<i>Figure 57: RP3-01 frame clock synchronization message.....</i>	<i>96</i>
<i>Figure 58: Timing principle in RP1 frame clock burst transfer.....</i>	<i>97</i>
<i>Figure 59: Ethernet frame transfer over RP3-01 network is done as a point-to-point transfer between a pair of nodes.....</i>	<i>97</i>
<i>Figure 60: RP3-01 line rate auto-negotiation is done between a pair of nodes (LC and RRU or between adjacent RRUs).....</i>	<i>100</i>
<i>Figure 61: Internal delays of Class #1 RRU.....</i>	<i>103</i>
<i>Figure 62: Internal delays of Class #2 RRU.....</i>	<i>103</i>
<i>Figure 63: Internal delays of Class #3 RRU.....</i>	<i>104</i>
<i>Figure 64: RTT Measurement message.....</i>	<i>105</i>
<i>Figure 65: Virtual HW reset message.....</i>	<i>106</i>
<i>Figure 66: Example block diagram of Transport layer.....</i>	<i>117</i>
<i>Figure 67: An example of message multiplexing from four 768 Mbps links into one 1536 Mbps link.....</i>	<i>118</i>
<i>Figure 68: An example of message interleaving from one 768 Mbps link into one 3072 Mbps link.....</i>	<i>118</i>
<i>Figure 69: An example of message interleaving from fifteen 768 Mbps links into three 1536 Mbps link.....</i>	<i>119</i>
<i>Figure 70: An example of message interleaving from three partly full 1536 Mbps links into one 3072 Mbps link.....</i>	<i>119</i>
<i>Figure 71: An example base station configuration.....</i>	<i>120</i>
<i>Figure 72: Data flows between BB and RF modules. Addresses of modules and antenna-carriers (or up/down converters at RF) are also shown.....</i>	<i>121</i>
<i>Figure 73: Index assignment to the ports of combiner distributor. Mapping of downlink messages to RP3 message slots is also shown.....</i>	<i>122</i>
<i>Figure 74: Mapping of uplink messages to RP3 message slots.....</i>	<i>124</i>
<i>Figure 75: TYPE 1 and TYPE 2 Interconnects.....</i>	<i>129</i>
<i>Figure 76: TYPE-3 Backplane Interconnect.....</i>	<i>130</i>
<i>Figure 77: TYPE-3 Cable Interconnect.....</i>	<i>131</i>
<i>Figure 78: Insertion loss to crosstalk ratio limit.....</i>	<i>133</i>

List of Tables

1		
2		
3	Table 1: Architecture related RP3 parameters and their values.....	15
4	Table 2: Size of the message.....	28
5	Table 3: Scrambler Seed Values.....	32
6	Table 4: Measurements performed by the Physical layer.....	44
7	Table 5: An example of a table.....	50
8	Table 6: Multiplexing table for the case where all messages from four 768Mbps links	
9	are multiplexed to a single 3072Mbps link.....	51
10	Table 7: Multiplexing table for the case where all messages from two 1536Mbps links	
11	are multiplexed to a single 3072Mbps link.....	51
12	Table 8: Multiplexing table for the case where all messages from one 1536Mbps link	
13	and two 768Mbps links are multiplexed to a single 3072Mbps link.	51
14	Table 9: Multiplexing table for the case where all messages from two 768Mbps link	
15	are multiplexed to a single 1536Mbps link.....	51
16	Table 10: Multiplexing table for the case where all messages from three 768Mbps	
17	links are multiplexed to a single 3072Mbps link.	52
18	Table 11: Definition of the parameters of the dual bit map concept.....	57
19	Table 12: Content of type field.....	59
20	Table 13: Sample Count Indicator.....	62
21	Table 14: Content of generic control message.....	67
22	Table 15: Content of air interface synchronized control message.....	67
23	Table 16: Content of the Generic Packet.	68
24	Table 17: Content of the time stamp field.....	69
25	Table 18: Payload of last message of Generic Packet.....	69
26	Table 19: Receiver Characteristics – 768 MBaud	73
27	Table 20: Receiver Characteristics – 1536 MBaud	73
28	Table 21: Receiver Characteristics – 3072 MBaud	74
29	Table 22: Receiver Characteristics – 6144 MBaud	74
30	Table 23: Receiver Compliance Mask Parameters	76
31	Table 24: Sinusoidal Jitter Mask Values.....	77
32	Table 25: Transmitter Characteristics – 768 MBaud	78
33	Table 26: Transmitter Characteristics – 1536 MBaud	78
34	Table 27: Transmitter Characteristics – 3072 MBaud	79
35	Table 28: Transmitter Characteristics – 6144 MBaud	79

1	Table 29: Transmitter output mask parameters.....	80
2	Table 30: Receiver Equalization Output Eye Mask	87
3	Table 31: Content of RP3-01 frame clock synchronization message.	96
4	Table 32: Content of the time stamp field of RP3 messages in relation to Ethernet	
5	MAC frame data of the payload.....	98
6	Table 33: Content of RP3-01 Ethernet message.....	99
7	Table 34: Parameters of line rate auto-negotiation algorithm.	101
8	Table 35: Content of an RTT Measurement message.....	105
9	Table 36: Content of virtual HW reset message.....	106
10	Table 37: Input and output parameters of Data link layer.....	107
11	Table 38: Error cases at Data link layer.	110
12	Table 39: Input and output parameters of Transport layer. All the parameters are	
13	defined for the whole node.	110
14	Table 40: Possible error cases at Transport layer.	113
15	Table 41: Other input and output parameters of bus node.	114
16	Table 42: Options for optical cabling.	115
17	Table 43: Optical interface recommendations for different RP3-01 line rates. This	
18	table is for information only.	115
19	Table 44: Downlink routing table.	122
20	Table 45: Uplink routing table.....	122
21	Table 46: Message transmission rules for BB modules #1 and #2.....	123
22	Table 47: Message transmission rules for RF module #1.	123
23	Table 48: Message transmission rules for RF module #2.	123
24	Table 49: Parameters for supported 802.16 profiles in case of 768 Mbps virtual RP3	
25	link.....	125
26	Table 50: Parameters for supported 802.16 profiles in case of 1536 Mbps virtual RP3	
27	link.....	126
28	Table 51: Parameters for supported 802.16 profiles in case of 3072 Mbps virtual RP3	
29	link.....	127
30	Table 52: Parameters for supported 802.16 profiles in case of 6144 Mbps virtual RP3	
31	link.....	128
32	Table 53: TYPE 3, 4, and 5 rear interconnect length specifications as indicated in	
33	Figure 76.	130
34	Table 54: TYPE 3, 4, and 5 front interconnect lengths specifications as indicated	
35	inFigure 77.	131
36	Table 55: Parameters for supported LTE profiles in case of 768 Mbps virtual RP3	
37	link.....	134

1	Table 56: Parameters for supported LTE profiles in case of 1536 Mbps virtual RP3	
2	link.....	134
3	Table 57: Parameters for supported LTE profiles in case of 3072 Mbps virtual RP3	
4	link.....	135
5	Table 58: Parameters for supported LTE profiles in case of 6144 Mbps virtual RP3	
6	link.....	135
7	Table 59: Parameters for UL GSM/EDGE/EGPRS2 in case of 768 Mbps virtual RP3	
8	link.....	136
9	Table 60: Parameters for UL GSM/EDGE/EGPRS2 in case of 1536 Mbps virtual RP3	
10	link.....	137
11	Table 61: Parameters for UL GSM/EDGE/EGPRS2 in case of 3072 Mbps virtual RP3	
12	link.....	137
13	Table 62: Parameters for UL GSM/EDGE/EGPRS2 in case of 6144 Mbps virtual RP3	
14	link.....	137
15	Table 63: Parameters for DL GSM/EDGE in case of 156 symbols per time slot and	
16	768 Mbps virtual RP3 link.....	138
17	Table 64: Parameters for DL GSM/EDGE in case of 187 symbols per time slot and	
18	768 Mbps virtual RP3 link.....	139
19	Table 65: Parameters for DL GSM/EDGE in case of 1536 Mbps virtual RP3 link. ..	140
20	Table 66: Parameters for DL GSM/EDGE in case of 3072 Mbps virtual RP3 link. ..	141
21	Table 67: Parameters for DL GSM/EDGE in case of 6144 Mbps virtual RP3 link. ..	141
22		

FOREWORD

OBSAI description and specification documents are developed within the Technical Working Group of the Open Base Station Architecture Initiative Special Interest Group (OBSAI SIG). Members of the OBSAI TWG serve voluntarily and without compensation. The description and specifications developed within OBSAI represent a consensus of the broad expertise on the subject within the OBSAI SIG.

The OBSAI SIG uses the following terminology in the specifications:

- “shall” expresses a provision that is binding
- “should” and “may” expresses non-mandatory provisions
- “will” expresses a declaration of purpose on the part of the OBSAI SIG. It may be necessary to use “will” in cases where the simple future tense is required

Use of an OBSAI reference or specification document is wholly voluntary. The existence of an OBSAI Specification does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the OBSAI Specification. Furthermore, the viewpoint expressed at the time a specification is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the specification. Every OBSAI Specification is subjected to review in accordance with the Open Base Station Architecture Initiative Rules And Procedures.

Implementation of all or part of an OBSAI Specification may require licenses under third party intellectual property rights, including without limitation, patent rights (such a third party may or may not be an OBSAI Member). The Promoters of the OBSAI Specification are not responsible and shall not be held responsible in any manner for identifying or failing to identify any or all such third party intellectual property rights.

The information in this document is subject to change without notice and describes only the product defined in the introduction of this documentation. This document is intended for the use of OBSAI Member’s customers only for the purposes of the agreement under which the document is submitted, and no part of it may be reproduced or transmitted in any form or means without the prior written permission of OBSAI Management Board. The document has been prepared for use by professional and properly trained personnel, and the customer assumes full responsibility when using it. OBSAI Management Board, Marketing Working Group and Technical Working Group welcome

customer comments as part of the process of continuous development and improvement of the documentation.

The information or statements given in this document concerning the suitability, capacity, or performance of the mentioned hardware or software products cannot be considered binding but shall be defined in the agreement made between OBSAI members. However, the OBSAI Management Board, Marketing Working Group or Technical Working Group have made all reasonable efforts to ensure that the instructions contained in the document are adequate and free of material errors and omissions.

OBSAI liability for any errors in the document is limited to the documentary correction of errors. OBSAI WILL NOT BE RESPONSIBLE IN ANY EVENT FOR ERRORS IN THIS DOCUMENT OR FOR ANY DAMAGES, INCIDENTAL OR CONSEQUENTIAL (INCLUDING MONETARY LOSSES), that might arise from the use of this document or the information in it.

This document and the product it describes are considered protected by copyright according to the applicable laws. OBSAI logo is a registered trademark of Open Base Station Architecture Initiative Special Interest Group. Other product names mentioned in this document may be trademarks of their respective companies, and they are mentioned for identification purposes only. Copyright © Open Base Station Architecture Initiative Special Interest Group. All rights reserved. Users are cautioned to check to determine that they have the latest edition of any OBSAI Specification.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of OBSAI, the OBSAI TWG will initiate action to prepare appropriate responses. Since OBSAI Specifications represent a consensus of OBSAI Member's interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason OBSAI and the members of its Technical Working Groups are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on specifications and requests for interpretations should be addressed to:

Peter Kenington

Chairman, OBSAI Technical Working Group

Linear Communications Consultants Ltd.

Email: pbk@linearcomms.com

1 Summary of Changes

Version	Approved by	Date	Comment
1.0	OBSAI Management Board	16/04/2004	Initial Release
2.0	OBSAI Management Board	11/10/2004	Second Release – incorporating remote head operation
3.0	OBSAI Management Board	01/08/2005	Third Release – incorporating WiMAX support
3.1	OBSAI Management Board	13/11/2006	Point Release – incorporating 4x line rate electrical specifications and related Type3 interconnect definition
4.0	OBSAI Management Board	3/7/2007	Fourth Release - incorporating LTE support
4.0.11	Release candidate	27/06/2008	Point Release – incorporating 8x (6144Mbps) line rate electrical specifications and related Type4&5 interconnect definitions Generic Packet Mode added
	with some corrections		LTE TDD specific channel bandwidths 1.6 and 3.2 do not exist any more and they were removed from Appendix F. Editorial corrections (cross-references corrected) Explicitly 100Ω resistance added to tables in ch5.
4.1	OBSAI Management Board	14/7/2008	Approved by Management Board

1 2 **Scope**

2 This document specifies the Reference Point 3 characteristics. Chapter
3 3 defines the connectivity between RF and baseband modules. The
4 protocol stack for data transfer is defined in Chapter 4, excluding the
5 electrical characteristics, which are specified in Chapter 5. The protocol
6 stack for data transfer between the base station and Remote RF units is
7 defined in Chapter 6. Configuration and management of the protocol is
8 detailed in Chapter 7.

3 Reference Point 3 Architecture

OBSAI Reference Point 3 (RP3) interface exists between RF and BB modules of a base station. In this chapter, architecture or connectivity between RF and baseband modules is specified.

Architecture related parameters are defined in Section 3.1. In Section 3.2, interface of RF and baseband modules toward RP3 is defined. Topology of RP3 is specified in Section 3.3. Inter-cabinet connections are considered in Section 3.4.

3.1 Parameter Definitions

A set of parameters is used to define the architecture characteristics of RP3. In Table 1, the values of all of the parameters are specified.

Table 1: Architecture related RP3 parameters and their values.

Parameter	Value	Description
K	9	Maximum number of pairs of unidirectional links with differential signalling in every RF and baseband module.
K_{RF_in}	$0 \leq K_{RF_in} \leq 9$	Number of incoming links with differential signalling that are implemented to a RF module.
K_{RF_out}	$0 \leq K_{RF_out} \leq 9$	Number of outgoing links with differential signalling that are implemented to a RF module
K_{BB_in}	$0 \leq K_{BB_in} \leq 9$	Number of incoming links with differential signalling that are implemented to a baseband module.
K_{BB_out}	$0 \leq K_{BB_out} \leq 9$	Number of outgoing links with differential signalling that are implemented to a baseband module
P	36	Number of connector pins that are allocated to RP3 differential signals in every RF and baseband module

Parameter	Value	Description
M	Integer, value equal to or greater than 1.	Number of RF modules in a base station.
N	Integer, value equal to or greater than 1.	Number of baseband modules in a base station.

3.2 Module Interface Toward RP3

Each OBSAI compliant RF module shall have maximum K (see Table 1) pairs of unidirectional links with differential signalling toward RP3 interface, i.e. $2 \times K$ links in total. A pair constitutes one incoming signal and one outgoing signal. Each RF module shall implement K_{RF_in} incoming links, where $0 \leq K_{RF_in} \leq K$, and K_{RF_out} outgoing links, where $0 \leq K_{RF_out} \leq K$. Among the implemented links with differential signalling, unused links shall be disabled for power conservation purposes. Each link requires 2 pins due to differential signalling that is used. In total, there exist P pins in each RF module that are allocated to differential signals to support RP3 interface. Each RF module shall always have the same pins of a connector allocated to RP3 signals. Refer to [6] for detailed pin definition.

The RF module may contain transmit functionality only, receiver functionality only, or both transmit and receive functionality.

Each OBSAI compliant baseband module shall have maximum K (see Table 1) pairs of unidirectional links with differential signalling toward RP3 interface, i.e. $2 \times K$ links in total. A pair constitutes one incoming signal and one outgoing signal. Each baseband module shall implement K_{BB_in} incoming links, where $0 \leq K_{BB_in} \leq K$, and K_{BB_out} outgoing links, where $0 \leq K_{BB_out} \leq K$. Among the implemented links with differential signalling, unused links shall be disabled for power conservation purposes. Each link requires 2 pins due to differential signalling that is used. In total, there exist P pins in each baseband module that are allocated for differential signals to support RP3 interface. Each baseband module shall always have the same pins of a connector allocated to RP3 signals. Refer to [5] for detailed pin definition.

Differential signalling is used at the lowest protocol layer at RP3 interface. On each link, bus protocol as specified in Chapter 4 shall be applied.

Figure 1 illustrates RP3 interface of RF and baseband modules. A pair of unidirectional links with differential signalling is shown in the figure as a double-ended arrow.

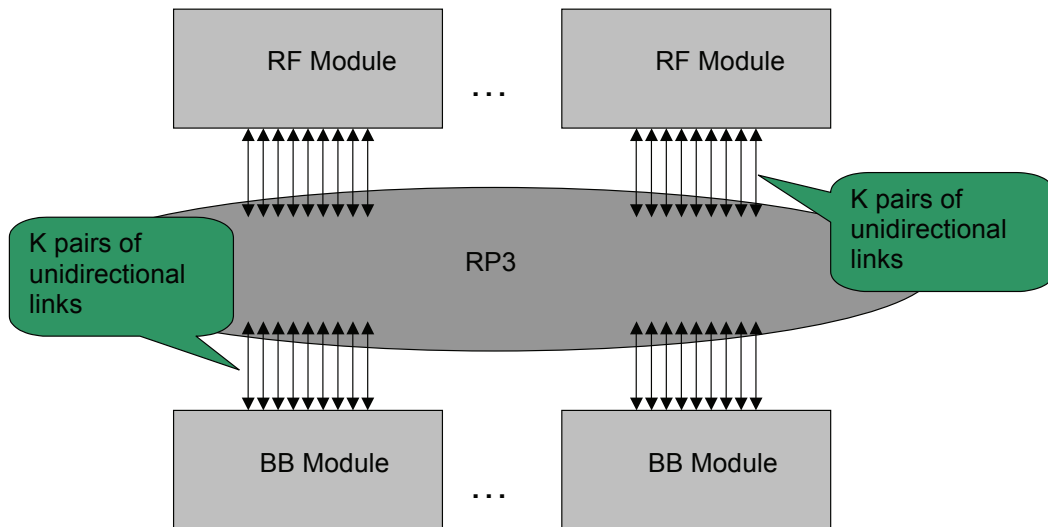


Figure 1: RP3 interface of RF and baseband modules. There exists a maximum of K pairs of unidirectional links toward RP3.

3.3 Topology

Topology specifies connectivity between RF and baseband modules. Two approaches are suggested (but not mandated): mesh and centralized combiner and distributor. They are explained in more detail below.

3.3.1 Mesh

Assuming N baseband and M RF modules in a base station, there exist in total $N \times M$ pairs of unidirectional links with differential signalling between baseband and RF modules in a full mesh. Each baseband module is connected to M RF modules while every RF module is connected to N baseband modules. Each pair of unidirectional links is implemented as two unidirectional differential signals in opposite directions for data and control transfer. Optionally, there may exist several parallel pairs of unidirectional links between any baseband and RF modules when very high data throughput is required. Connection between any pair of baseband and RF modules may also be missing if it is not required. When there does not exist any connection between a baseband module and an RF module, a partial mesh rather than full mesh is obtained.

Each RF and baseband module has at maximum K pairs of unidirectional links. Therefore, K*K mesh at maximum can be supported but any combination, including asymmetrical combinations, up to this maximum is allowed.

Figure 2 illustrates a base station configuration with two baseband and three RF modules and a full mesh at RP3.

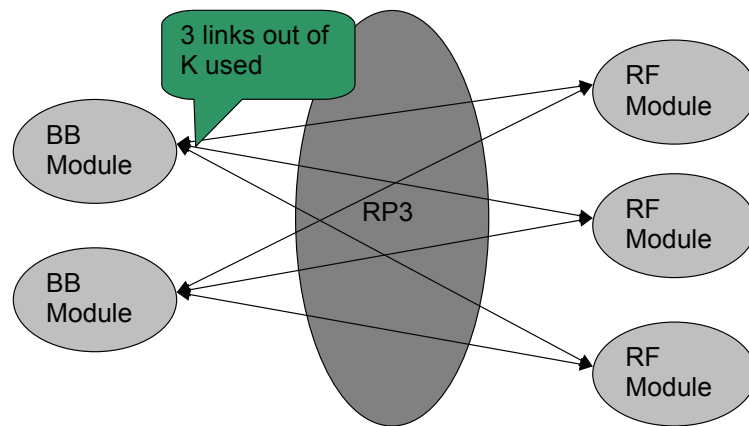


Figure 2: Full mesh connecting two baseband and three RF modules. Each baseband module is connected to every RF module and vice versa.

Figure 3 shows K-by-K full mesh.

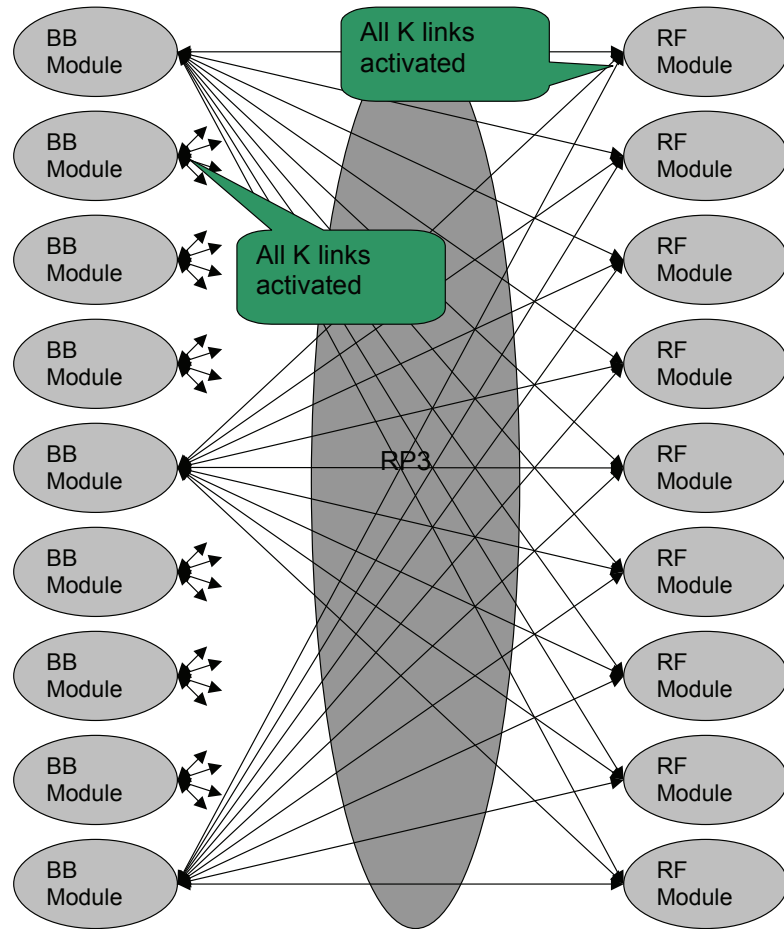


Figure 3: Full mesh connecting K baseband modules to K RF modules. All the connections are not drawn.

3.3.2 Centralized Combiner and Distributor

Assume N baseband and M RF modules in a base station maximum configuration. All links of both baseband and RF modules are connected to a centralized combiner and distributor (C/D) that is located in RP3. For each link, differential signalling is applied. In combining, input samples that are targeted to the same antenna and carrier at the same time instant are added together so that a single output sample stream is formed after which it is transmitted to the desired RF module(s). In distribution, RX sample stream from a RF module is distributed to all or to a subset of baseband modules. At maximum, $K \cdot (N+M)$ pairs of unidirectional links are connected to the combiner and distributor but any number of links below this maximum can be connected to combiner and distributor. For a given base station

configuration, at maximum $\sum_{i=1}^N K_{\text{BB_out}}[i] + \sum_{i=1}^M K_{\text{RF_in}}[i]$ downlink

unidirectional links and $\sum_{i=1}^N K_{BB_in}[i] + \sum_{i=1}^M K_{RF_out}[i]$ uplink unidirectional links are connected to the combiner and distributor. In these equations, $K_{BB_in}[i]$ and $K_{BB_out}[i]$ stand for number of incoming and outgoing links that are implemented to the i^{th} baseband module while $K_{RF_in}[i]$ and $K_{RF_out}[i]$ denote number of incoming and outgoing links that are implemented to the i^{th} RF module. Between any RF or baseband module and the centralized combiner and distributor, unused links shall be disabled for power conservation purposes.

In order to obtain better fault tolerance, a redundant combiner and distributor can be used. In full redundancy, all signals of every RF and baseband module are transferred through main and redundant combiner and distributor modules. Given maximum K pairs of unidirectional links per RF or baseband module, at maximum $K - \lfloor K/2 \rfloor$ pairs of links from any module can be connected to main combiner and distributor and the remaining $\lfloor K/2 \rfloor$ pairs of links can be connected to the redundant combiner and distributor, or vice versa, when redundancy is applied. $\lfloor X \rfloor$ denotes the largest integer number equal to or less than X . Any number of links below this maximum can be connected to a combiner and distributor from a RF or baseband module. In load balancing redundancy, portion of the signals are transferred through the first combiner and distributor while rest of the signals are sent through the second combiner and distributor.

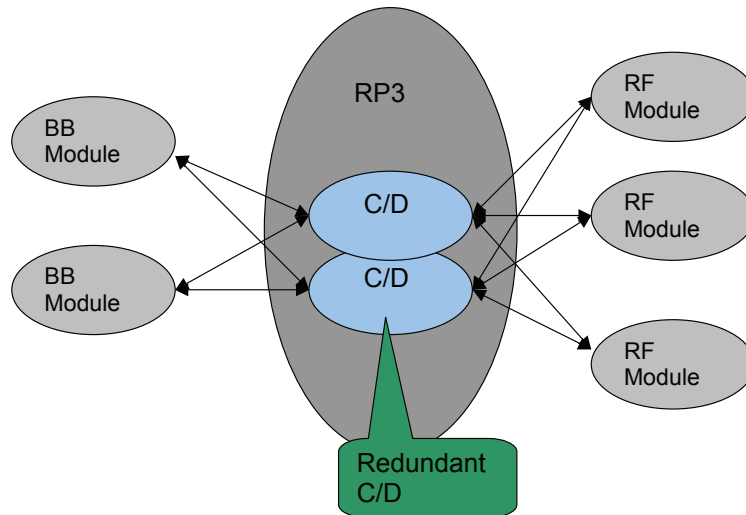


Figure 4: Centralized combiner and distributor (main and redundant) embedded into RP3 interface.

Figure 4 and Figure 5 illustrate centralized combiner and distributor topology with and without redundancy, respectively. Unlike in mesh

approach, there now exist active component(s) in RP3. The same baseband and RF modules shall be used with mesh or centralized combiner and distributor topology.

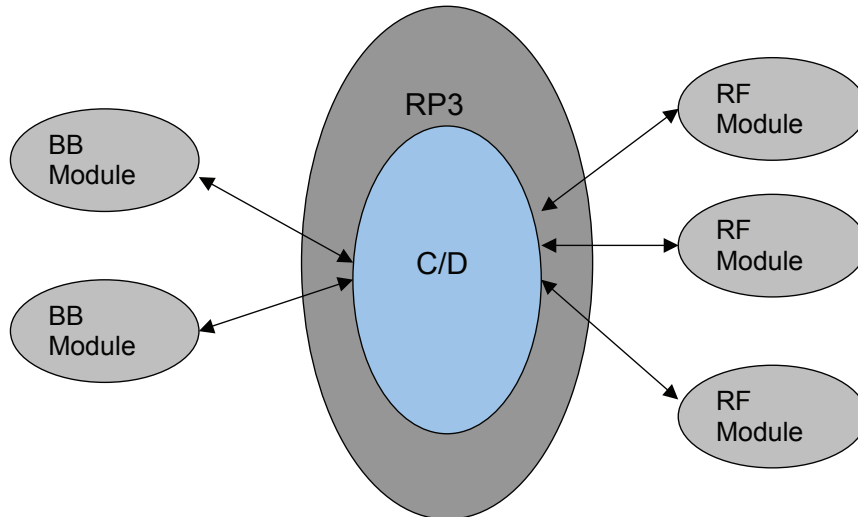


Figure 5: Centralized combiner and distributor embedded into RP3 interface. Redundant C/D is not applied.

3.4 Inter-Cabinet Connections

In very large configurations, a base station may be located in several cabinets and RF-baseband signal transfer between cabinets may be required. RP3 interface shall be used in inter-cabinet RF-baseband data transfers. Thus, differential signalling connections are used as well as the protocol stack defined in Chapter 4. Three topology options exist for inter-cabinet data transfers:

- Inter-cabinet mesh
- Links between bridge modules
- Links between centralized combiner and distributor modules

All these options are described in detail below. Two cabinet case is considered in this section. All the concepts presented can be generalized for X cabinet case where $X > 2$.

3.4.1 Inter-Cabinet Mesh

Figure 6 illustrates the case where a full mesh exists between all baseband and RF modules in dual cabinet base station configuration.

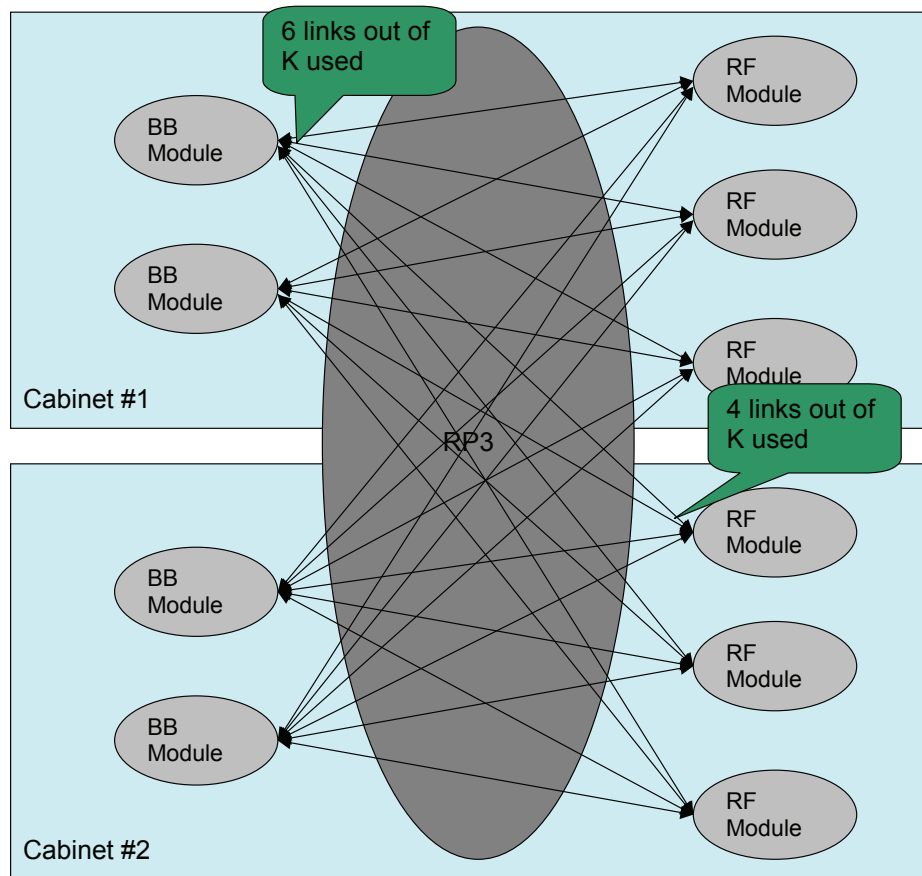


Figure 6: Full mesh between RF and baseband modules of two cabinets.

3.4.2 Connections between Bridge Modules

Figure 7 shows the second option for inter-cabinet communication. Now bridge modules are used that may simply forward data from cabinet to another. Bridge module is typically used in place of a baseband module and it can be used with intra-cabinet mesh or centralized combiner and distributor topologies.

Any baseband module of Cabinet #X can be connected to any RF module of Cabinet #Y when applying the bridge concept. Sufficient bandwidth in Baseband-to-RF links of Cabinet #X is assumed. In most simple implementation, bridge just forwards a set of differential signals from input to output. In a more advanced approach, bridge module is able to interchange data between links.

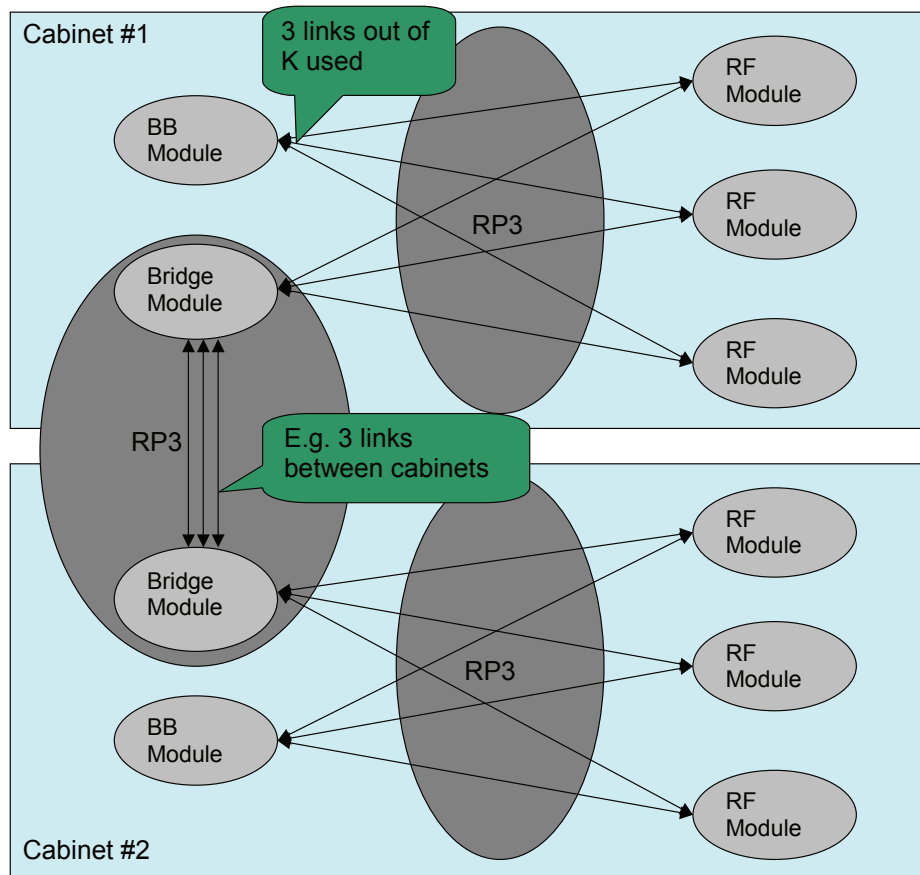


Figure 7: Bridge modules extending RP3 interface to two cabinets. Mesh topology is shown in intra-cabinet RF-baseband connections but also centralized combiner and distributor topology may be applied.

In order to obtain better fault tolerance, a redundant bridge module is typically used. Both the main and redundant bridge modules of the two cabinets shall be connected together.

3.4.3 Connections between Combiner and Distributor Modules

Figure 8 defines third option for inter-cabinet data transfer. When centralized combiner and distributor modules exist in RP3, these modules of different cabinets can be connected together. Both the main and redundant modules of the two cabinets shall be connected together.

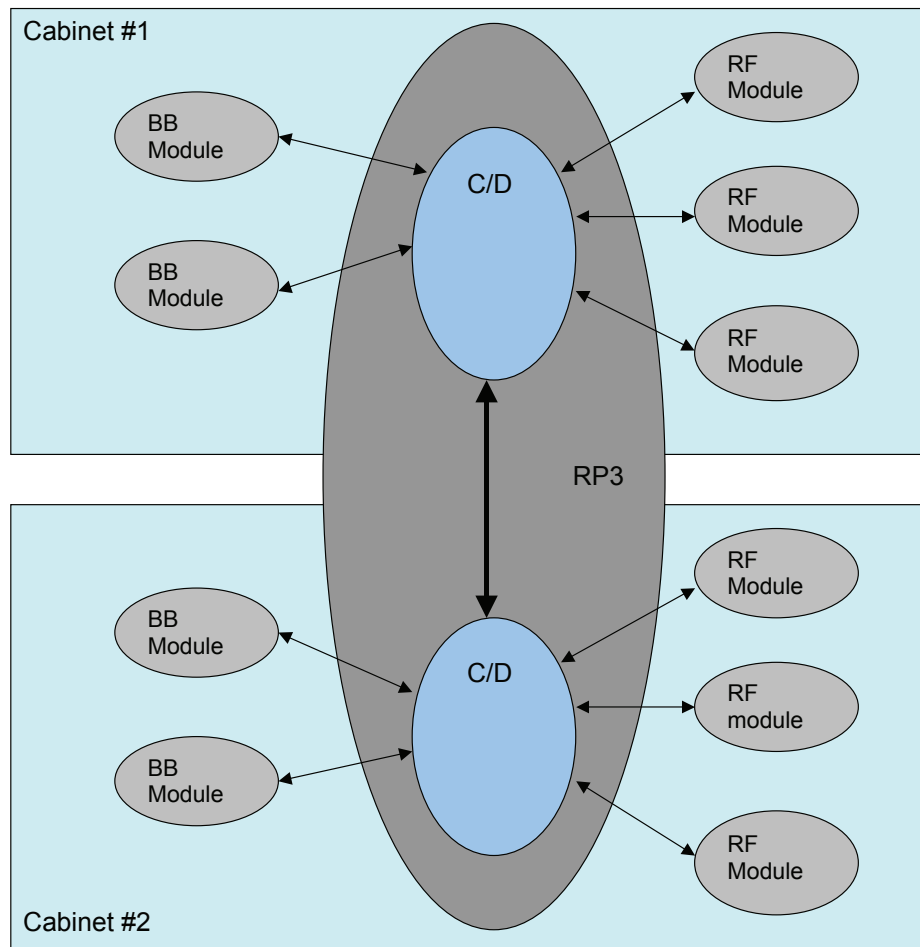


Figure 8: RP3 interface extended over two cabinets by connecting C/Ds together (redundant C/D not applied).

4 Protocol Stack

The RP3 bus interface is a high-capacity, point-to-point serial interface bus for uplink and downlink telecom (user) data transfer and related control. The physical implementation of the bus is based on differential signalling technology. The protocol stack is based on a packet concept using a layered protocol with fixed length messages.

The bus protocol can be considered as a four-layer protocol consisting of

- **Application layer**, providing the mapping of different types of packets to the payload.
- **Transport layer**, responsible for the end-to-end delivery of the messages, which is simply routing of messages.
- **Data link layer**, responsible for framing of messages and message (link) synchronization
- **Physical layer**, responsible for coding, serialization, and transmission of data

This is illustrated below in Figure 9.

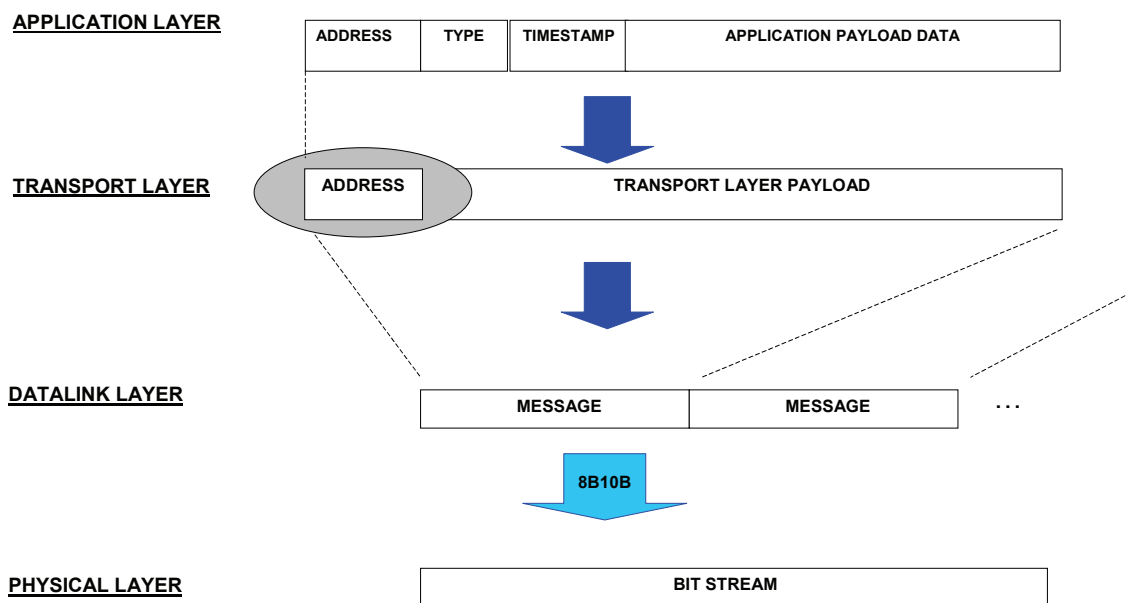


Figure 9: Layered structure of the bus protocol.

4.1 Physical Layer

4.1.1 Electrical Signalling

Refer to Chapter 5 for a detailed specification on electrical characteristics of RP3 interface.

For conformance testing purposes, physical layer loopback shall be supported as illustrated in Figure 10.

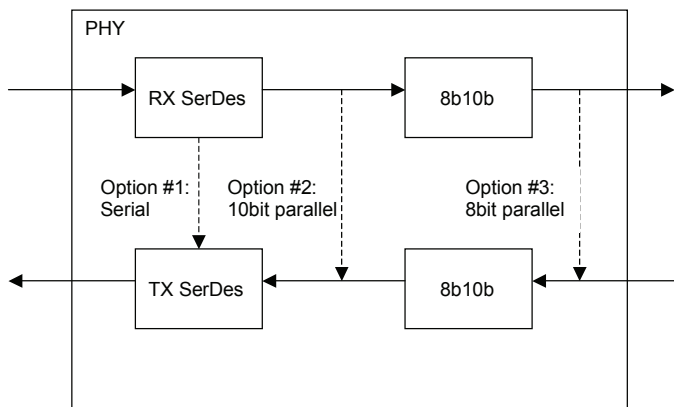


Figure 10: Illustration of possible physical layer loopback points.

4.1.2 Data Format and Line Coding

8b10b transmission code [1] shall be applied to all data that is transmitted over the RP3 bus. 8b10b transmission coding will provide a mechanism for serialization and clock recovery.

Figure 11 illustrates physical layer structure.

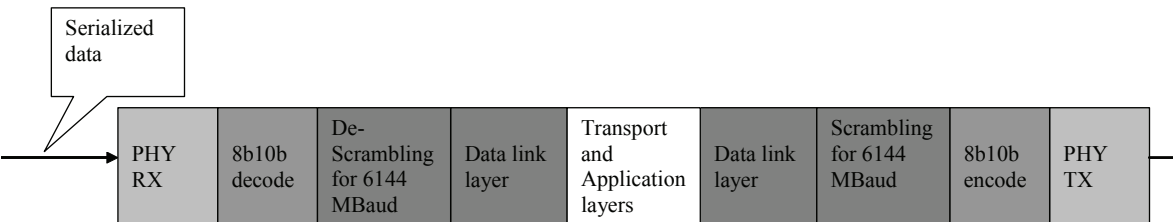


Figure 11: Illustration of Physical layer structure – data flow approach.

Synchronization of physical layer receiver

In the Physical layer receiver, phase adjustments to the incoming signal are automatically done for each receiver port separately. Typically, phase adjustments are done when initialising the connection.

Line code violation detection

Physical layer, the 8b10b decoder, shall detect invalid line codes from the incoming serial bit stream. Each Line Code Violation (LCV), i.e. erroneously received byte, shall be indicated to Data link layer.

Physical layer, the 8b10b encoder, shall transmit K30.7 character to the link when Data link layer indicates that the byte to be transmitted contains an error.

4.1.3 Bus Clock

Physical layer of the bus is frequency and phase locked to a centralised BTS system clock [4]. In every bus node, byte clock for the bus is generated from BTS system clock and it equals to *Bus_line_Rate*/10 when bus line rate is expressed in baud units.

4.2 Data Link Layer

4.2.1 Message Overview

A fixed message format is used for all data that is transferred over the RP3 or RP3-01 (see Section 6) bus.

Figure 12 shows the message structure including partitioning of the message into bytes. In case of 6144Mbaud line rate, each byte of the message is scrambled and 8b10b encoded and then transmitted to a link. For other line rates, each byte of a message is first 8b10b encoded as shown in the figure and then transmitted to a link. 8b10b encoding is part of Physical layer functionality. The leftmost byte of the address field is first transmitted to the link while the rightmost byte of payload is last sent to the link. If data from other busses is transferred over the RP3 or RP3-01, it must be realigned such that Most Significant Bit (MSB) is transmitted first as defined in Figure 12.

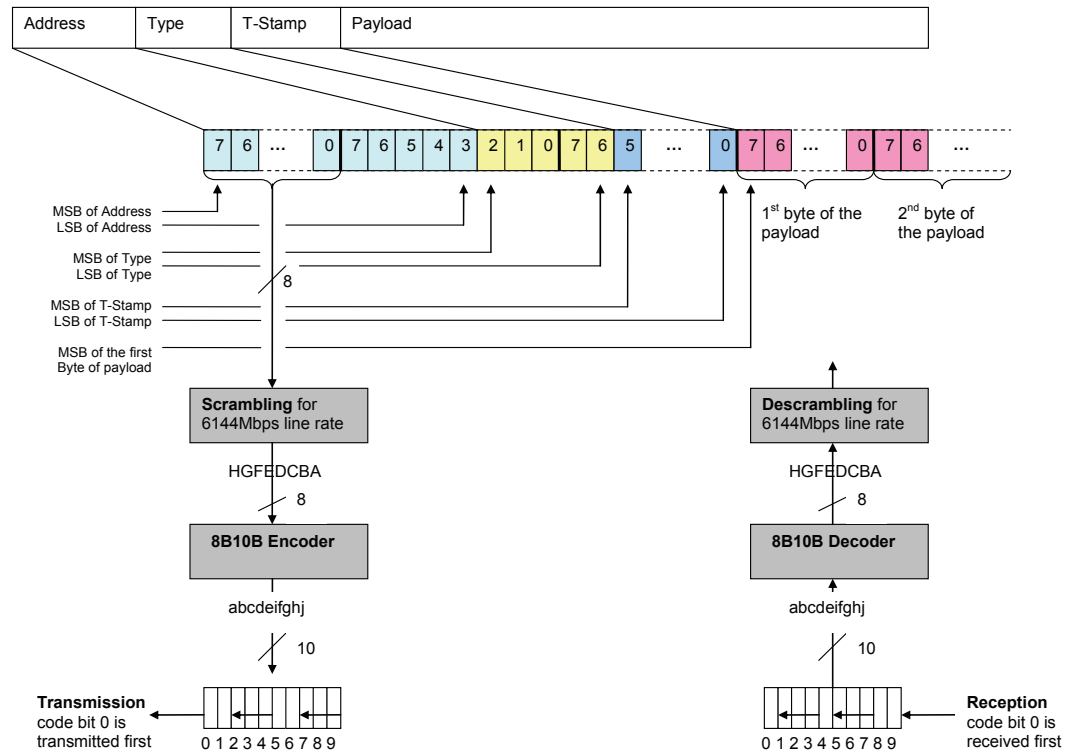


Figure 12: Message format of RP3 protocol stack.

Table 2 defines the size of each field of the message.

Table 2: Size of the message.

Field	Length (bits)
Address	13
Type	5
Time stamp (T-Stamp)	6
Payload	128
Total length	152 bits (=19 bytes)

A block of data consisting of M_MG messages, $0 < M_MG < 65536$, and K_MG IDLE bytes, $0 < K_MG < 20$, is called a Message Group (MG). Consecutive Message Groups are transferred over a bus link. Master Frame length is fixed to 10 ms and it is composed of $i * N_MG$, where $0 < N_MG < 65536$ and $i \in \{1, 2, 4, 8\}$, consecutive Message Groups for line rates $i * 768$ Mbps. Thus, any of the line rates 768 Mbps, 1536 Mbps, 3072, and 6144 Mbps can be applied. Parameters M_MG and N_MG must be selected such that $i * N_MG * M_MG < 2^{32}$ holds. Size of a Message Group equals to $M_MG * 19 + K_MG$ bytes while Master Frame size in bytes is $i * N_MG * (M_MG * 19 + K_MG)$.

The M_MG message slots of a Message Group are divided into data and control slots. For a line rate $i * 768$ Mbps, the i last message slots of every i^{th} Message Group are control message slots while all other message slots are allocated for data message slots. In a Master Frame, there exist $i * N_MG$ control message slots and Message Group with index $i - 1$, where Message Group indices run from 0 to $i * N_MG - 1$, is the first Message Group having control slots.

K_MG idle codes K28.5 [1] exist at the end of each Message Group with one exception. Idle codes K28.7 are used to mark the end of a Master Frame, i.e. K_MG consecutive K28.7 codes exist at the end of last Message Group. A set of unique codes is used to mark the end of a Master Frame in order to facilitate reception.

There exists a large set of different Message Group and Master Frame definitions. Parameter set $M_MG=21$, $N_MG=i*1920$, and $K_MG=1$ is recommended to be used for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards while parameter set $M_MG=13$, $N_MG=i*3072$, and $K_MG=3$ is recommended for CDMA.

Figure 13 and Figure 14 Master Frames for WCDMA, GSM/EDGE, 802.16, LTE, and CDMA air interface standards for the 768 Mbps line rate ($i=1$).

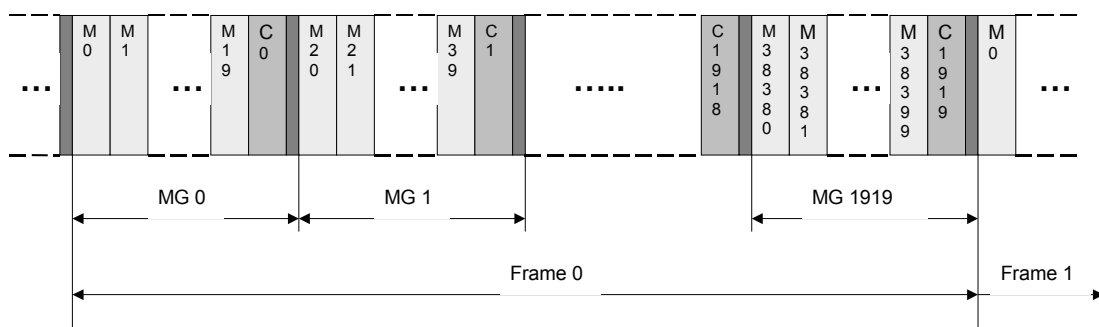


Figure 13: Master frame illustrating the sequence according to which WCDMA, GSM/EDGE, 802.16, and LTE messages are inserted to the bus (parameter set $M_MG=21$, $N_MG=1920$, $K_MG=1$, $i = 1$).

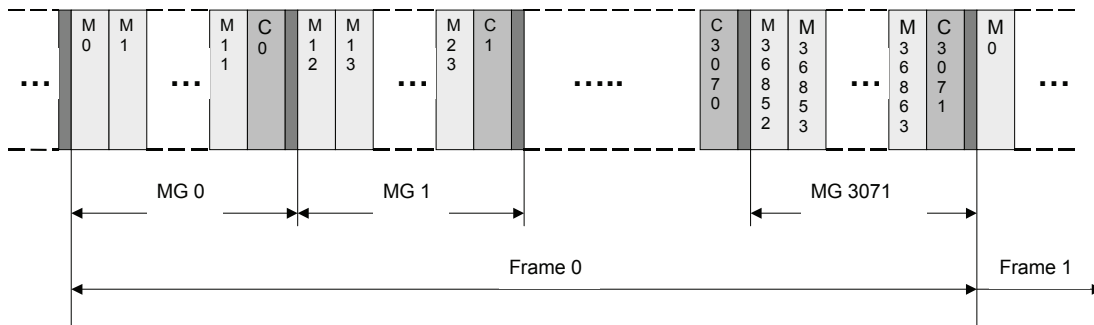


Figure 14: Master frame illustrating the sequence according to which CDMA messages are inserted to the bus (parameter set $M_MG=13$, $N_MG=3072$, $K_MG=3$, $i=1$).

Figure 15 illustrates Message Group structures for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards at all allowed line rates $i \cdot 768$ Mbps, $i \in \{1, 2, 4, 8\}$.

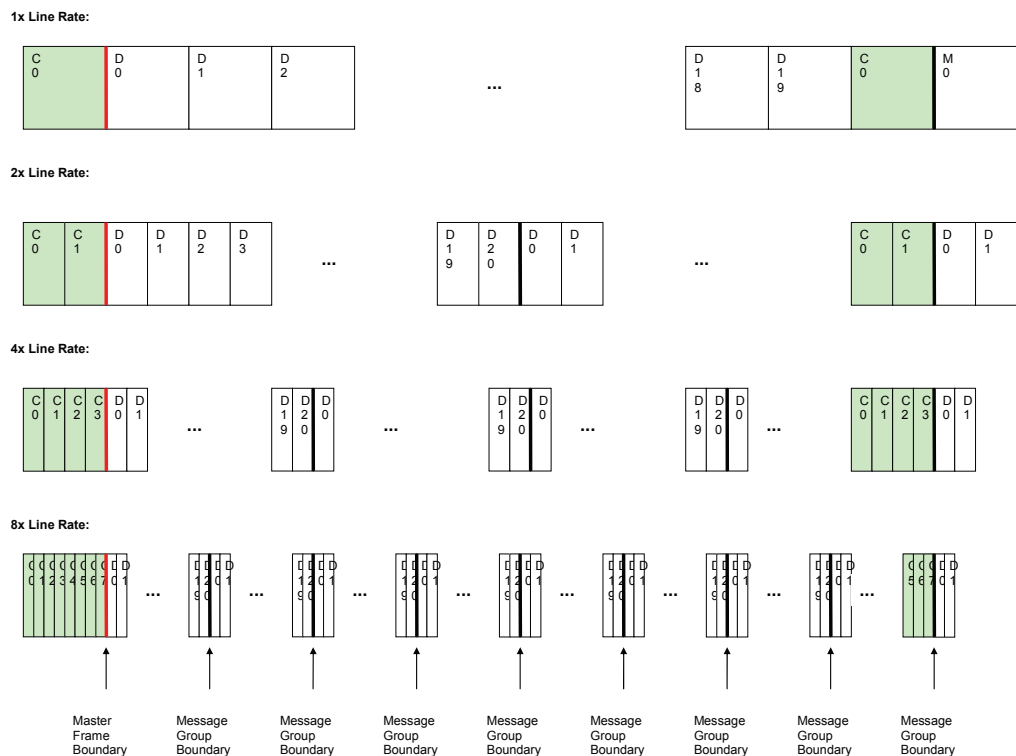


Figure 15: Message group structures for WCDMA, GSM/EDGE, 802.16, and LTE air interface standards at 768 Mbps (1x), 1536 Mbps (2x), 3072 Mbps (4x), and 6144 Mbps (8x) line rates. Time span corresponding to a single message group at 768 Mbps line rate is shown.

4.2.3 Bit Level Scrambling for 6144 Mbps (8x) Line Rate

Bit level scrambling shall be performed on 8x rate links to reduce cross talk between links as well as to reduce inter-Symbol interference (ISI). The RP3 transmitter shall apply a 7-degree polynomial to data bytes and the inverse operation shall be performed by the RP3 receiver. Scrambling only pertains to 6144 Mbps operation (8x link rate). Link rates {1x, 2x, 4x} are backward compatible with no scrambling applied.

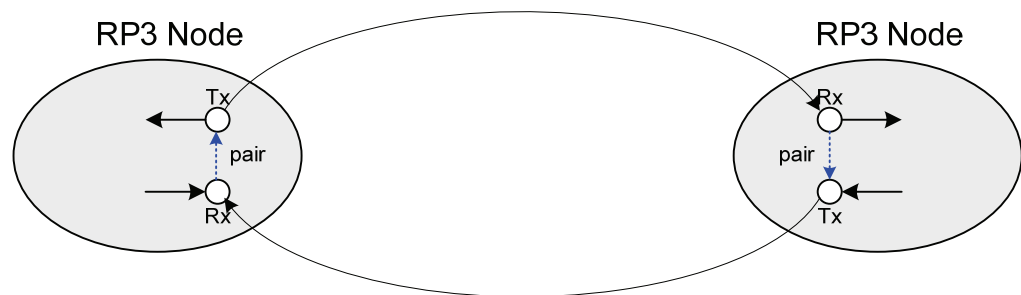


Figure 16: Scrambling Pattern Passed Between Two Adjacent RP3 Nodes.

Cross talk between transmitters through the local SERDES power supply is the main concern. With all transmitters having differing scrambling offsets, randomness between transmitting lanes is achieved. The assignment of unique scrambler offsets for receivers is optional as cross talk between receivers and transmitters is non-critical.

The RP3 transmitter is configured by higher layers, setting the starting value of the 7-degree polynomial scrambling code generator. Higher layers shall configure unique seed values for adjacent RP3 Tx links. The following table illustrates the available seed value to be used. These seed values represent nx7 position offsets (nx7 has been specifically chosen to give an odd offset between adjacent links). The RP3 receiver is a slave to the transmitter, receiving the seed value in a training sequence.

Table 3: Scrambler Seed Values.

Nx7 Index	X ⁷	X ⁶	X ⁵	X ⁴	X ³	X ²	X ¹
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
2	0	0	0	0	1	0	1
3	0	0	0	1	1	1	1
4	0	0	1	0	0	0	1
5	0	1	1	0	0	1	1
6	1	0	1	0	1	0	0
7	1	1	1	1	1	0	1
8	0	0	0	0	1	1	1
9	0	0	0	1	0	0	1
10	0	0	1	1	0	1	1
11	0	1	0	1	1	0	1
12	1	1	1	0	1	1	0
13	0	0	1	1	0	1	0
14	0	1	0	1	1	1	0
15	1	1	1	0	0	1	1
16	0	0	1	0	1	0	1
17	0	1	1	1	1	1	1

The scrambling shall follow the rules below:

The scrambling code generator increments by one bit position for each bit of every byte. In each bit position of the scrambling code generator a single scrambling bit is created which is XOR with each single bit of a data byte. The bits of a byte are processed in order from the MSB to the LSB corresponding to the order in which the scrambling bit sequence is generated. On every K28.5 or K28.7 character, the scrambling code generator is reset to the starting seed value.

The seed value and checking sequence is transmitted as training patterns from the RP3 transmitter to the receiver during the IDLE period of the transmit state machine. Only 8x rate links use these special patterns during the IDLE period. There are two sub-states in the IDLE state IDLE_REQ and IDLE_ACK; two different training patterns are transmitted in the two sub-states:

- IDLE_REQ: K28.5, byte0, ..., byte15... repeat
- IDLE_ACK: K28.5, K28.5, byte0, ..., byte15... repeat

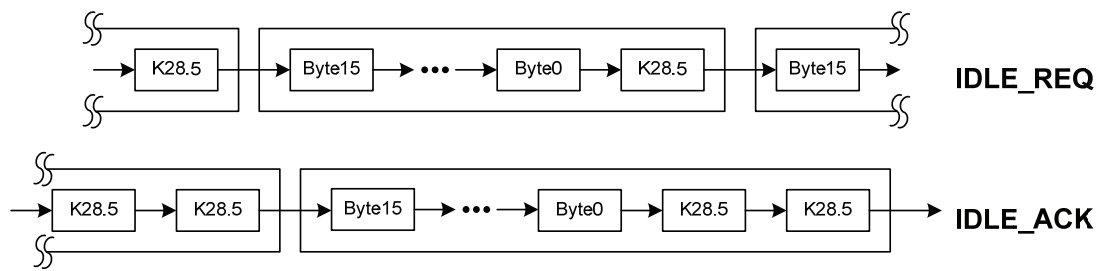


Figure 17: Scrambling Training Patterns.

In practice, the 16 byte training pattern is created by passing sixteen zero bytes (D.0.0) through the RP3 transmitter scrambler. The K28.5 preceding the training pattern resets the scrambler to the seed value. For seed discovery, the K28.5 resets the state of the de-scrambler to all zeros; this effectively disables the descrambler. The first 7 bits recovered of 16 byte sequence are the seed value which is extracted by the receiver for use as the initial value of the de-scrambler. The extra length of the training pattern helps guard against cross talk and ISI during the start-up protocol. After the seed value is extracted from the first training pattern, sixteen subsequent training patterns are checked. Successful de-scrambling of a training pattern results in the 16 bytes of zero (D0.0).

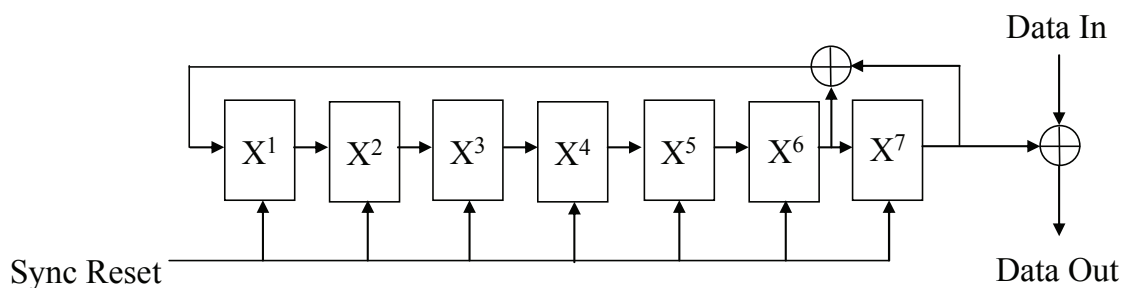


Figure 18: 7-Degree Polynomial Scrambler.

The scrambler shall be a 7-degree polynomial, linear feedback shift register (LFSR). The polynomial is $X^7 + X^6 + 1$. K28.5 or K28.7 characters reset the LFSR to the seed value. The bit pattern repeats every 127 bits.

The RP3 receivers are capable of differentiating IDLE_REQ from IDLE_ACK and capturing the scrambling code seed from either pattern. Random SERDES bit errors are infrequent but could corrupt the training sequence. The receiver verifies the seed value by checking 16 consecutive training patterns after capturing the seed (failures re-start the training protocol). Each RP3 receiver has two different state conditions it can communicate to it's paired RP3 transmitter:

- Scrambling code seed captured from adjacent node
- Acknowledge received from adjacent node

RP3 transmitters can transfer either IDLE_REQ or IDLE_ACK patterns in the IDLE state. The IDLE_REQ is transmitted while the paired receiver has yet to successfully capture the scrambler seed. After the seed is captured, IDLE_ACK is transmitted. Once both the seed is captured and IDLE_ACK is received by the RP3 receiver, the transmitter is enabled to leave the IDLE state.

When a receiver transitions back into the UNSYNC state for any reason, the paired transmitter is brought back into the IDLE state and begins the process of transmitting IDLE_REQ all over again. When a receiver receives IDLE_REQ, it's state is forced back into the UNSYNC state causing it to receive the scrambling seed value again.

The transmit IDLE_REC & IDLE_ACK mechanism with associated conditional actions taken depending on the state received constitute a robust mechanism for training coordination between two nodes. Any order or delay of enabling the different RP3 transmitters and receivers in a chain are handled with this mechanism. Additionally retraining due to board hot swap or other disruptions is also handled by this mechanism.

A false byte alignment is indicated by the incoming 8b10b encoded bit stream when K28.7 character is followed by certain critical characters. Due to scrambling that is applied for 6144Mbps line rate, any character following K28.7 may cause false byte alignment. Therefore, K28.7 character should not be used for byte alignment or the achieved byte alignment should be locked before starting RP3 master frame transmission.

4.2.4 Counters

Master Frame is defined in Section 4.2.2. The Data link layer provides indices of current data and control message slots to upper layers which can then use these indices in the scheduling of message transmissions. Data message slot counter takes values from 0 up to $(i*(M_MG-1)*N_MG)-1$ (refer to Section 4.2.2 for the definition of N_MG and M_MG) while control slot counter runs from 0 to $(i*N_MG)-1$. Both of these counters are 32 bits wide and they count message slots over a Master Frame duration. Both the data and control message slot counters are reset to zero in the beginning of the first data and control slots of the new master frame. As illustrated in Figure 19, the data message slot counter is reset to zero in the beginning of a Master Frame due to leading data message slot while the control slot counter is reset to zero in the beginning of the first control slot of the new master frame.

Master frame timing denotes here the Δ corrected (see Section 4.2.5) Master Frame timing, i.e. Master Frame timing at a transmitter port. This refers to the fact that there exists latency in message transfer over the bus, i.e. the message is seen at slightly different times in separate bus nodes. Counter value X in the figure below identifies the same message slot of a Master Frame in each bus node.

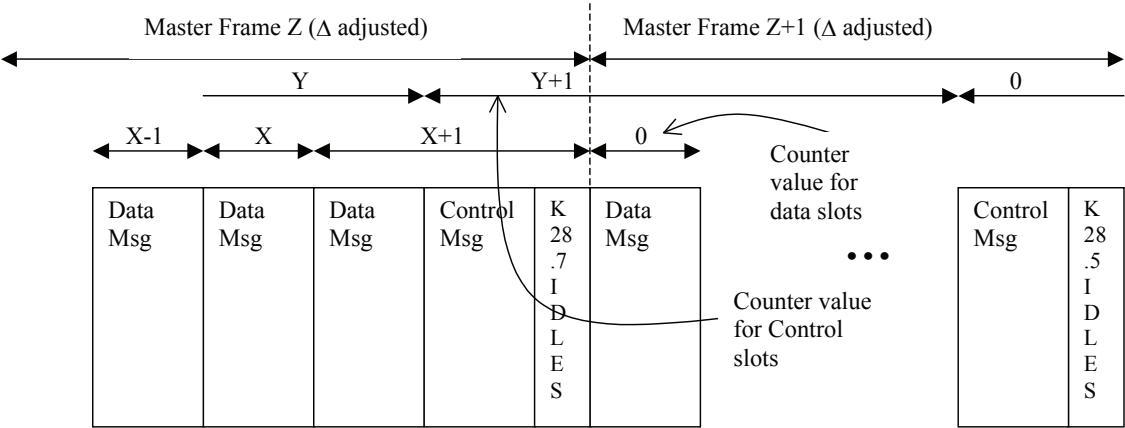


Figure 19: Timing of message slot counters for an example MG and MF definition.

For each bus transceiver (transmitter), message slot counters are activated (counting is started) after the offset parameter Δ (see Section 4.2.5) is available and the state of the transceiver is FRAME_TX (see Section 4.2.8).

4.2.5 Transmission of Frame Structure

Transmission time of Master Frame is synchronised to the RP3 bus frame clock at the output of each bus node. First byte of Master Frame is transmitted at offset Δ from the RP3 bus frame clock tick. In general, a common Δ value is used for uplink transmitter ports; another Δ value is used for all downlink transmitters. In some bus nodes, a specific parameter value is used for each transmitter port.

Parameter Δ fulfils the equation $\Delta = \Pi + D + B + P$, where D stands for processing delay of the receiver module and B indicates the maximum amount of buffering available at each Data link layer bus receiver while P denotes latency across the node; from receiver module to transmission module. Parameter Π is defined in Section 4.2.6 below. Note that the above equation only applies to bus nodes that forward received messages.

Offset values Δ are received at start-up by each bus node and their values are specified in byte-clock ticks. Alternatively, offset values Δ may be specified using two byte accuracy (even byte-clock ticks) which

may be beneficial especially for higher RP3 line rates. Two's complement code numbers are used.

Offset value Δ of a transmitter is fixed at run time. Section 4.2.8 defines the process according to which the value of the parameter Δ can be changed. Figure 20 illustrates Master Frame transmission timing.

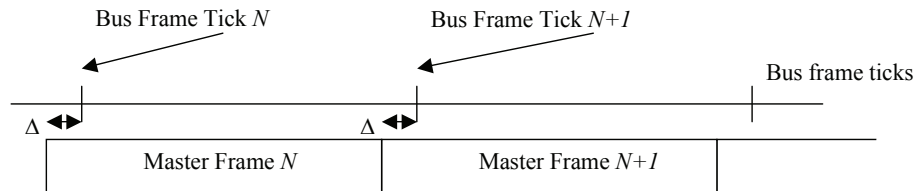


Figure 20: Master Frame is transmitted at an offset to the RP3 bus frame tick in each bus node.

After receiving the parameter Δ , Master Frame timing is valid at the second RP3 bus frame tick. This is due to the fact that Δ may take negative values.

4.2.6 Reception of Frame Structure

The purpose of Master Frame synchronisation is to minimise buffering need in bus nodes, i.e. to ensure that corresponding message slots are received at the same time at each bus node.

For each bus receiver, synchronisation block indicates the received Master Frame boundary (see Section 4.2.8). The synchronization block should contain buffering to compensate for variations of delay especially on long transmission media. An additional offset parameter Π is provided for each receiver that indicates earliest possible time instant when a Master Frame can be received. This time instant, called reference time, is equal to RP3 bus frame clock plus offset Π .

An exact value of Π is provided such that the end of the Master Frame shall be received at the reference time or at maximum MAX_OFFSET ns after the reference time. The default value of MAX_OFFSET equals to 52.08ns while value 104.17ns is optionally allowed (refer to Section 7.1.1 for MAX_OFFSET parameter definition). Target for bus configuration is to have the end of the Master Frame exactly $\text{MAX_OFFSET}/2$ ns after the reference time. This can be achieved when the entire RP3 bus (all parameters) is properly configured.

When initialising a bus link, received Master Frame boundary may not hit the allowed MAX_OFFSET ns wide time window. A false parameter

value can cause this situation. Irrespective of the erroneous Π value, bus nodes can perform measurements of the received Master Frame boundary as defined in Section 4.2.9.

An error shall always be indicated to Application layer when received Master Frame boundary is detected outside the allowed MAX_OFFSET ns long window. No error is indicated if the Master Frame boundary is not detected at all. This functionality is optional in bus nodes that are located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes. When Master Frame boundary is detected outside the allowed window in any bus node, all following data and control messages are rejected by default. Thus, they are not forwarded to output port(s) and they are not summed together with other messages. However, in bus nodes that are located in Remote RF Units (see Chapter 6), transfer of messages is continued irrespective of the location of the Master Frame boundary. Message processing continues normally (assuming that receiver state has remained in FRAME_SYNC state; see Section 4.2.8) after detecting Master Frame boundary in the allowed window.

Value of parameter Π is fixed at run time. By default, the receiver state machine shall be resynchronised (see Section 4.2.8) when updating the value of the parameter Π . Advanced implementations of RP3 may be able to support run-time updating of parameter Π such that RP3 message transmission and reception is continued uninterrupted.

Figure 21 illustrates run time (allowed) and measurement windows of received Master Frame.

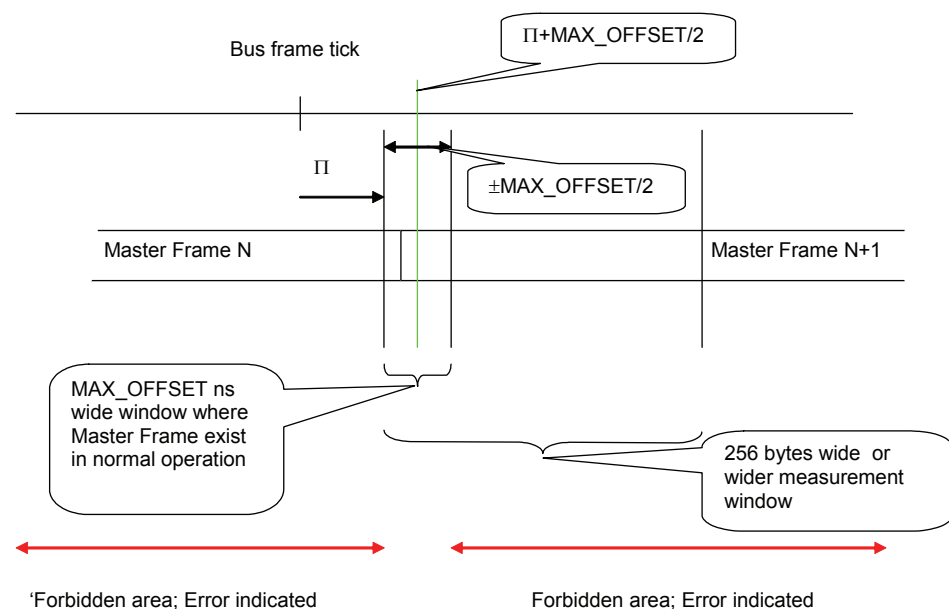


Figure 21: Run time and measurement windows of received Master Frame.

Consider any bus node that has two or more receiver ports. Parameter Δ 's at the transmitting nodes are defined so that difference in received Master Frame timing at any pair of ports is less than or equal to duration of MAX_OFFSET ns.

Figure 22 illustrates receive and transmit offsets of a Master Frame.

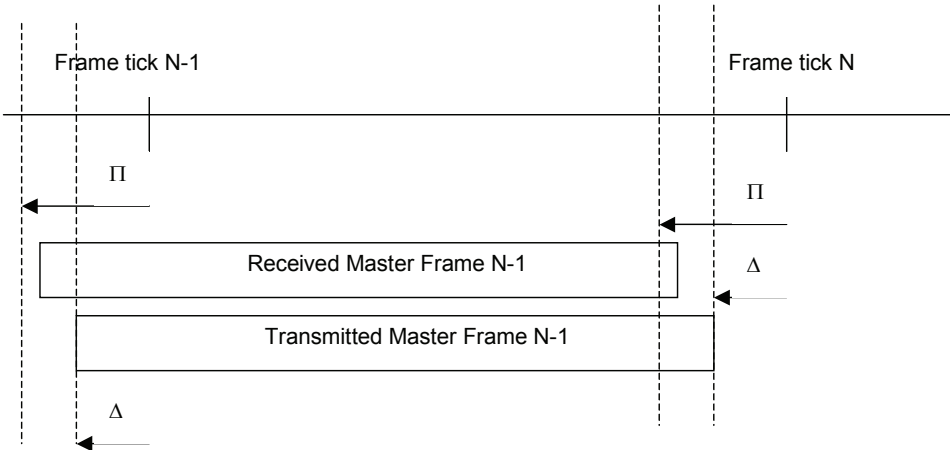


Figure 22: An example of Master Frame timings.

BTS Control and Clock block [2] is responsible of value assignment to parameters Δ and Π of all bus nodes. Figure 23 provides an example of Δ and Π value definition for a very simple intra-cabinet bus network. In the figure, there exists a bus network with three nodes. For clarity, downlink (DL) and uplink (UL) bus connections and corresponding parameter values have been drawn separately. The leftmost node exemplifies bus interface at baseband module while the rightmost node stands for bus endpoint at RF module. Combiner and distributor (C/D) node is at the middle.

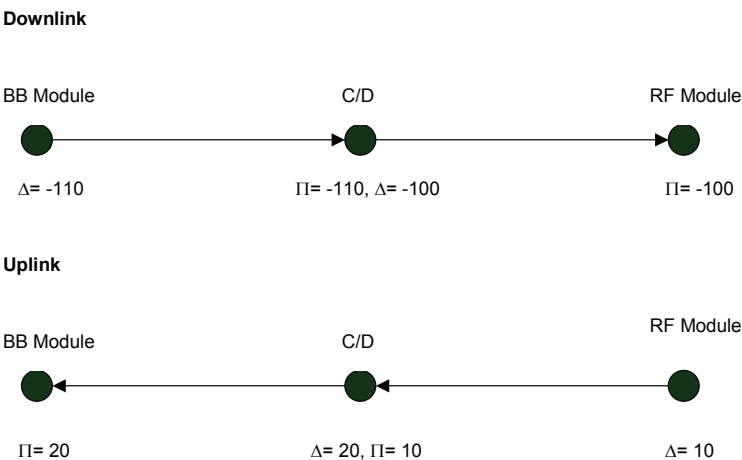


Figure 23: Example of Δ and Π assignments to a bus network.

In this example, we assume that RP3 bus Master Frame and air interface frame are aligned in time. Therefore, negative Δ and Π values are applied in downlink direction in order to have the data early enough at RF module for transmission to the air (refer to timestamp definition in Section 4.4.7 and data mapping to Master Frame in Section 4.4.8 for related information). Capacity of the bus link and processing delay at RF determines the value of Π that shall be applied. Value of Π never equals to zero at RF bus node. Values of Δ and Π at C/D and baseband nodes are determined by taking into account delays over bus links as well as processing delay over C/D. For simplicity, we assume delay of 10 byte clock ticks over the C/D bus node.

In uplink direction, positive Δ and Π values are applied (refer to Sections 4.4.7 and 4.4.8 for related information). Processing delay at RF defines value of Δ at RF module. Other Δ and Π values are determined by delays over bus links and processing delay over C/D bus node.

4.2.7 Empty Message

When there is no message to transmit, i.e. no message has been received from transport layer for a given message slot, the Data link layer of the bus transmits an empty message. Data link layer at the receiver end will reject empty message and, therefore, these messages are invisible to upper protocol layers. Address '1111111111111' is reserved exclusively for the empty message. Figure 24 defines the empty message. Address field contains '1' bits while rest of the message contains don't care x bits. Don't care bits can be assigned to either '1' or '0' in message transmission.

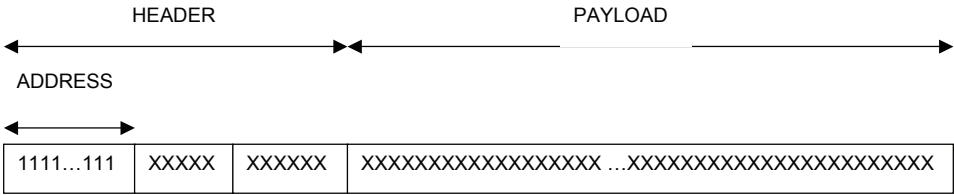


Figure 24: Empty message. The address field consists of thirteen '1' bits while rest of the message contains don't care x bits.

4.2.8 Synchronisation

Physical and Data link layers of the bus must be synchronised before actual data transfer can be started. Synchronisation algorithm can provide information to upper layers regarding the quality of a bus link.

Frequency of byte errors as well as status of frame synchronisation shall be constantly monitored.

Data Link Layer Synchronisation

The synchronisation algorithm is described in the format of finite state machines. Separate state machines exist for each transceiver. Separate state machines are provided for transmitter and receiver as shown in the following subsections.

Transmitter

There are three states in the transmitter state machine: OFF, IDLE, and FRAME_TX. On reset, the state machine enters the initial OFF state. In this state, transmission from the Physical layer macro to a bus link is disabled. Thus, nothing is transmitted to the bus.

Application layer controls the transition from OFF state to IDLE state. State is changed when Application layer sets parameter TRANSMITTER_EN equal to 1 and one of the following cases is true: (1) parameter LOS_ENABLE is set equal to 0 meaning that signal LOS (Loss of Signal) from receiver state machine does not have any impact on the transmitter state, or (2) LOS_ENABLE is equal to 1 (LOS has an impact) and LOS is equal to 0 (inactive).

In IDLE state, the following functionality shall be implemented. In case of 768, 1536, and 3072Mbps line rate, the transmitter macro continuously transmits K28.5 IDLE based on which the receiver end can obtain sample (byte) synchronisation. Transmitter state machine always remains in state IDLE at least t micro seconds. Value of t is implementation specific and it is large enough to allow Phase Locked Loop (PLL) of the transmitter macro to settle and the interfacing receiver macro to obtain correct sample phase.

In case of 6144Mbps line rate, the IDLE state consists of two sub-states: IDLE_REQ and IDLE_ACK. When the transmitter enters the IDLE state, it immediately moves to IDLE_REQ state and starts transmitting the IDLE_REQ scrambling training pattern as defined in Section 4.2.3. When the associated RX state machine has captured the scrambling code seed, the transmitter enters IDLE_ACK state and starts transmitting IDLE_ACK sequence (see Section 4.2.3). When the associated RX state machine has received scrambling acknowledgement sequence, the transmitter remains in IDLE_ACK state and starts waiting for parameter Δ updating (or alternatively moves to a third sub-state where it waits for delta updating (FFS)).

Transition from IDLE state to FRAME_TX state is done when Application layer updates (modifies) the value of parameter Δ . If the value of this parameter is not updated when the transmitter is in state IDLE, transition to state FRAME_TX is not done.

The value of the parameter Δ can only be provided in state IDLE. If there exist a need to change the value of Δ during base station run-

time, the transmitter shall first be forced to OFF state, then to IDLE after which the parameter Δ can be updated.

In FRAME_TX state, transmission of the valid frame structure is performed (see Section 4.2.2). Valid messages from Application/Transport layer are transmitted as well as empty messages. Transmission of frame structure is activated within 20 ms after the updating of parameter Δ .

In Figure 25, all the states and state transitions are shown. As can be seen from the figure, HW reset or active LOS (Loss of Signal) from receiver state machine shall force the state to OFF (transmission disabled).

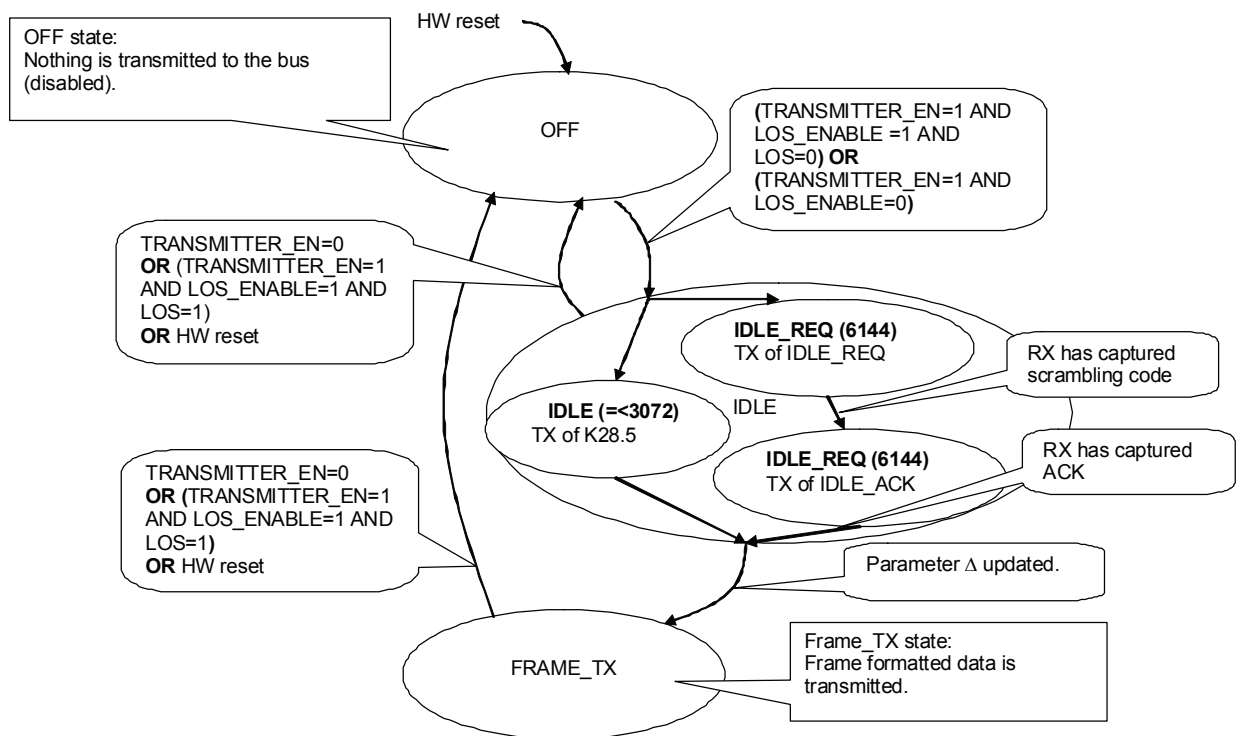


Figure 25: State diagram of the transmitter.

Receiver

As can be seen from Figure 26, receiver state machine consists of four states in case of 768, 1536, and 3072 Mbps line rate while there exist six states for 6144 Mbps line rate. The four states applied for 768 – 3072 Mbps line rates are the following: UNSYNC, WAIT_FOR_K28.7_IDLES, WAIT_FOR_FRAME_SYNC_T, and FRAME_SYNC. Two of these states, namely WAIT_FOR_K28.7_IDLES and WAIT_FOR_FRAME_SYNC_T, can be considered to form a single logical state called SYNC. The meaning of states UNSYNC, SYNC, and FRAME_SYNC is as follows:

- UNSYNC: Bus link is down. A lot of byte errors are detected.
- SYNC: Bus link is working, i.e. connection exists.
- FRAME_SYNC: Normal operational mode. Frame structure is detected and messages are received.

Two additional states are applied for the 6144Mbps line rate due to scrambling seed transfer from the transmitter to the receiver: IDLE_REC and IDLE_ACK.

On reset, the state machine enters the state UNSYNC. In case of 6144 Mbps line rate, state transition to IDLE_REC state is done when the scrambling seed is captured from the IDLE_REC training pattern (see Section 4.2.3). Transition to IDLE_ACK state is done when the acknowledgement of the seed capture has been received.

The remaining part of the receiver state machine uses two separate criteria to determine the quality of a bus link; the first one monitors the byte error rate of the link while the second one monitors the validity of the received frame structure (refer to Section 4.2.2 for a definition of the frame structure). Parameters BLOCK_SIZE, SYNC_T, UNSYNC_T, FRAME_SYNC_T, FRAME_UNSYNC_T control the state transitions.

State transition from UNSYNC state (768, 1536, or 3072Mbps line rate) or IDLE_ACK state (6144Mbps line rate) to WAIT_FOR_K28.7_IDLES is done if SYNC_T consecutive blocks of bytes have been properly received. In each block, there exists BLOCK_SIZE bytes and a block is considered to be valid if all the bytes were received correctly (no 8b10b decoding errors). Otherwise, the block is considered to be invalid.

Transition from state WAIT_FOR_K28.7_IDLES back to UNSYNC is done if UNSYNC_T consecutive invalid byte blocks are received or in case of HW reset.

Master Frame boundary is indicated by a set of K28.7 IDLE bytes, i.e. it exists at the end of the block of K_MG consecutive K28.7 IDLES. Transition from WAIT_FOR_K28.7_IDLES to WAIT_FOR_FRAME_SYNC_T is done when K_MG (refer to Section 4.2.2 for a definition of K_MG) consecutive K28.7 idle bytes, i.e. a possible Master Frame boundary, is detected. In state WAIT_FOR_FRAME_SYNC_T as well as in state FRAME_SYNC, Master Frame timing is considered to be fixed (defined by the first set of received K28.7 IDLES).

In WAIT_FOR_FRAME_SYNC_T state, validity of consecutive message groups (see Section 4.2.2) is studied. When FRAME_SYNC_T consecutive valid message groups are received, FRAME_SYNC state is entered. If FRAME_UNSYNC_T consecutive invalid message groups are received, state WAIT_FOR_K28.7_IDLES is entered and search for new set of K28.7 IDLES is started immediately.

State transition from FRAME_SYNC to WAIT_FOR_K28.7_IDLES is done when FRAME_UNSYNC_T consecutive invalid message groups are received and transition from FRAME_SYNC to UNSYNC is done when UNSYNC_T consecutive invalid blocks of bytes are received.

A valid message group stands for a block of $M_MG*19+K_MG$ bytes where the first M_MG*19 bytes are of type data or 8b10b decoding error. Idle codes K28.5 or K28.7 are not allowed. The last K_MG bytes must be either K28.5 or K28.7 idle bytes or 8b10b decoding errors. Furthermore, the order of the idle bytes matters. In the first $i*N_MG-1$ Message Groups of a Master Frame, all K_MG idle bytes of the Message Group must equal to K28.5 while in the last Message Group of the Master Frame, K_MG idle codes shall equal to K28.7.

Receiver synchronisation state machine has several outputs. Current state of the receiver will be available for Application layer. An interrupt is generated from each state change. Signal LOS (Loss of Signal) is active (has value 1) in state UNSYNC while it is inactive in other states. Synchronisation block indicates also bytes that contain 8b10b decoding error as well as the location of the Master Frame boundary.

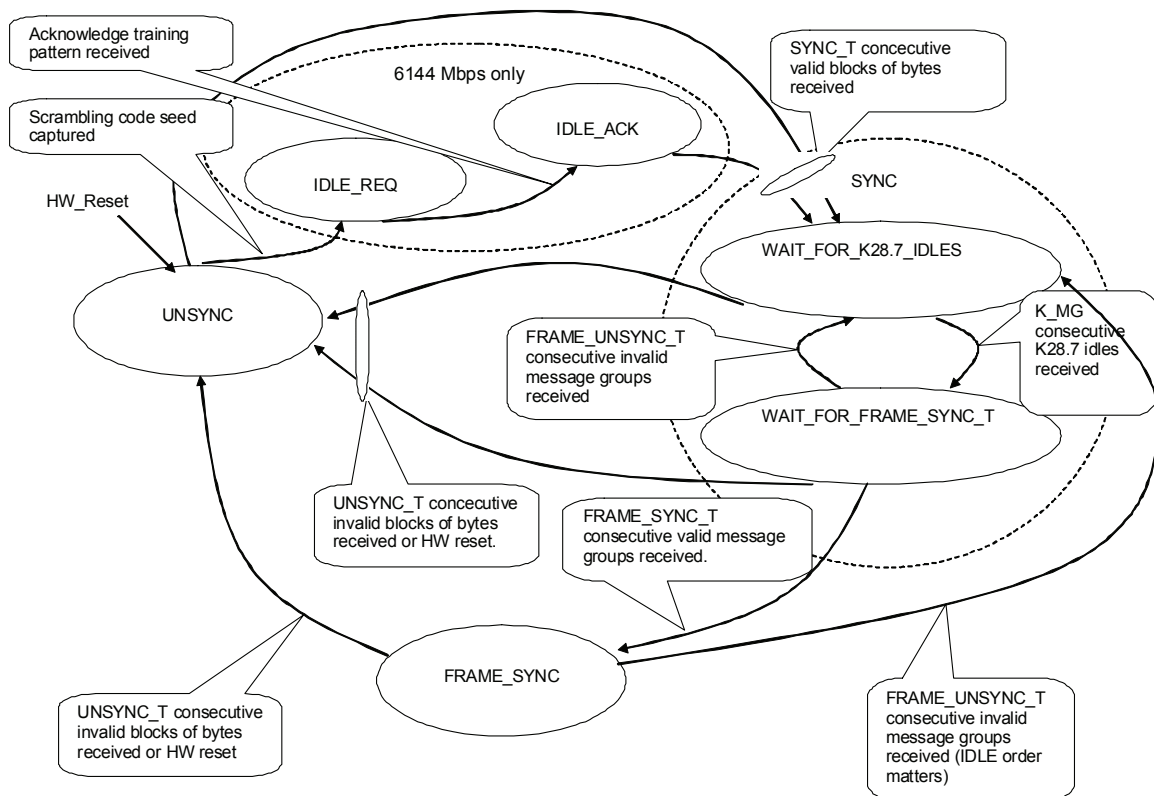


Figure 26: State diagram for the receiver.

Data Link layer shall forward messages to Transport layer only when in state FRAME_SYNC. This will prevent routing of false data from disconnected or otherwise malfunctioning receiver port.

4.2.9 Measurements

In this section, the measurements that are performed by the Data link layer are listed. Currently only timing offsets of received Master Frames with respect to baseband bus clock plus Π are measured (refer to Section 4.2.6). This measurement is optional in bus nodes that are located in Remote RF Units (see Chapter 6) while it is mandatory in other nodes.

To support bus configuration and error recovery, each bus receiver can detect the received Master Frame within a time window that spans 0-255 bytes after the reference time. Also larger measurement windows are allowed. The reference time stands for baseband bus frame clock tick plus offset Π . If the Master Frame offset is not detected during the time window, the measurement is saturated at the maximum counter value (default value is 255). The measurement is activated only in FRAME_SYNC mode (see Section 4.2.8) and the measurement is conducted once per Master Frame.

Table 4: Measurements performed by the Physical layer.

Measurement	Register width	Description
Received Master Frame offset	8 bits (default value), positive integer (no sign bit). Wider registers, e.g. time windows, are allowed.	Provided for each receiver separately. Master Frame offset from reference time, i.e. baseband bus frame clock tick plus Π . Value is given in byte-clock ticks. Measurement value is saturated at the maximum counter value (255 is the default value) if Master Frame boundary is not detected. Valid range of values for Master Frame boundary measurement is 0-MAX_OFFSET ns. Out of range error is indicated (see Section 4.2.6).

4.3 Transport Layer

Transport layer consists of message router, multiplexer, demultiplexer and summing units. Transport layer is responsible for the end-to-end delivery of messages. All routing of messages is performed at Transport layer. Based on the address of each message, bus nodes forward

received messages to destination nodes. Local routing is applied, i.e. each bus node knows only its own output port(s) into which a message needs to be transmitted. Nodes do not have visibility to the entire message paths. These paths are defined by a bus control entity, Bus manager, when booting up the bus.

The address field, which is used to route the data to its destination point, occupies the first 13 bits of the message. The remaining part of the message, including type, timestamp, and payload, is passed transparently by the Transport Layer.

4.3.1 Overview of Transport Layer

In general, communication networks consist of bi-directional links (or unidirectional links in opposite directions) that connect nodes. In each node, the same routing algorithm is applied to all received messages. In an alternative approach, a bi-directional network is separated into two unidirectional networks that operate independently. When messages need to be transferred between these unidirectional networks, they must go across Application layer. Physical and Transport layers of the two networks operate independently. In a hybrid network concept, received messages in all bus nodes are divided into two groups and separate routing algorithms are applied to these groups. Messages may be classified, e.g., based on the direction of the received messages.

The proposed bus protocol can be used in all above-mentioned network concepts. The hybrid approach is proposed with downlink and uplink networks, and separate routing tables are used for uplink and downlink messages.

Figure 27 illustrates Transport layer with a common message router for all received messages. External interfaces of Transport layer are shown including ports between Application and Transport layers as well as between Transport and Data link/Physical layers. All messages between protocol layers are transferred over these ports.

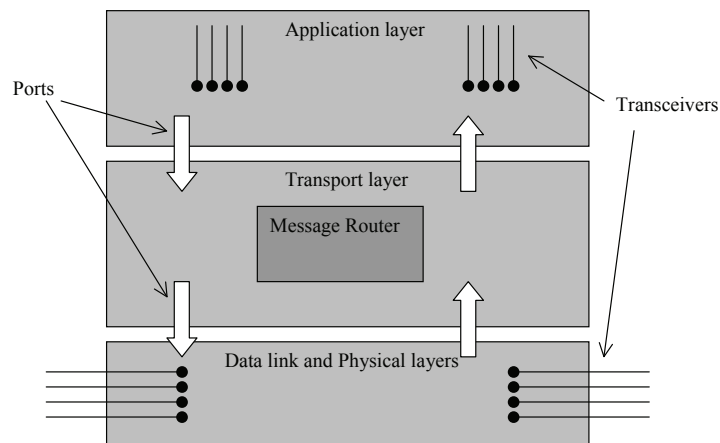


Figure 27: Transport layer with a common message router for all received messages.

When a bus node receives a message from another node, the message is first received by a transceiver at Physical and Data link layers. Then the message is sent to Transport layer, which determines the output transceiver with the help of a routing table. Assuming that transceiver at the Data link/Physical layer is targeted, the message is forwarded back to Data link layer for transmission to the next node. If the payload of the message is processed in the bus node, Transport layer will forward the message to Application layer based on the address of the message. Application layer may send the message back to the bus after processing.

Transport layer operates in a similar manner for all received messages whether they are received from Data link/Physical or from Application layers.

Figure 28 presents functional blocks of Transport layer where a dedicated message router is used for downlink and uplink messages. Application layer must indicate through parameters which transceivers, especially receiver ports of transceivers, are connected to downlink message router and which use the uplink router. Note that both message routers can forward messages to the transmitter port of any transceiver.

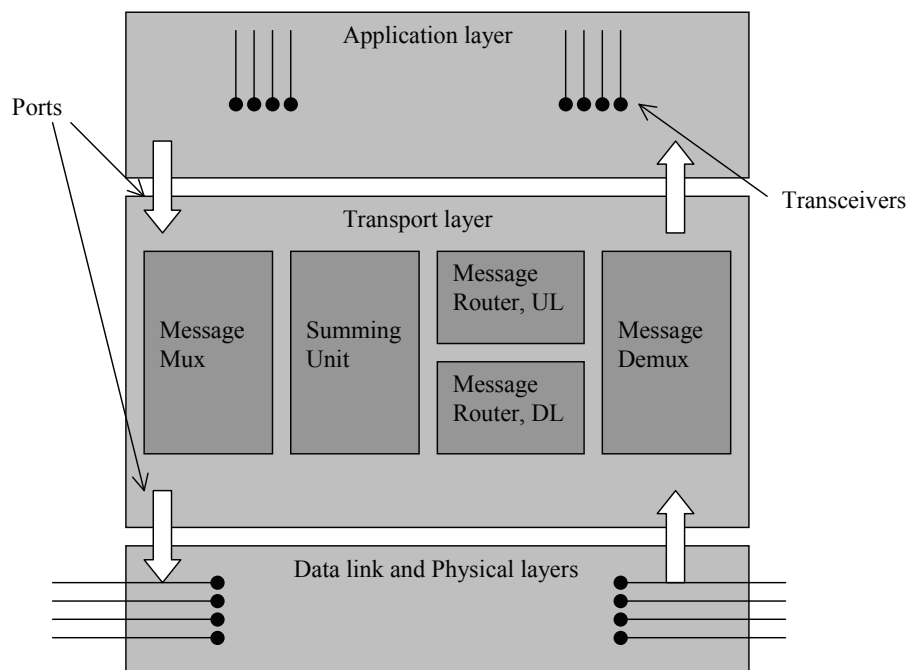


Figure 28: Transport layer with dedicated downlink and uplink message routers. Also message multiplexer, demultiplexer, and summing unit is shown.

Message multiplexer performs parallel to serial conversion of messages, i.e. it time interleaves messages from two or more input RP3 links into an output RP3 link. Message demultiplexer performs the opposite operation to message multiplexer.

The summing unit, which is located in front of each transmitter port of a transceiver, adds together payloads of messages. Summing is performed when more than one message should be transmitted simultaneously to the output port.

Physical and Data link layers, as well as message router and summing unit at Transport layer, operate as fast as possible, i.e. messages are not buffered. Thus, message slot is never altered by these functional blocks. Message multiplexer and demultiplexer may perform line rate conversions due to which they may need to have buffers of length few messages.

In the following sections, all functional blocks of the transport layer are described in detail.

4.3.2 Message Format – Address Field

The address controls the routing of each message. In downlink direction, i.e. from baseband to RF, all message transfers are point-to-point, and the address identifies the target node. Both multicasting (point-to-multipoint) and point-to-point message transfers are applied in uplink direction, i.e. from RF to baseband. Uplink antenna sample data as well as some measurement results may require multicasting; all other message transmissions in uplink direction are typically point-to-point.

In networks where bus nodes apply the same routing algorithm to all received messages, each multicast address must be unique. This is undesirable because address space is consumed. When separate routing algorithms are applied for downlink and uplink messages, source node address of the message can be used as the multicast address. This concept shall be used.

The address field is divided into two sub-addresses, the node address and the sub-node address as illustrated in Figure 29.

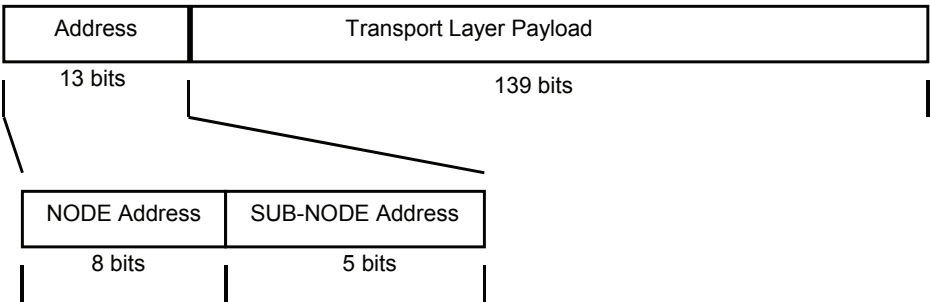


Figure 29: Address sub-fields.

Node and sub-node address fields are used in a hierarchical addressing scheme where the node field is used to uniquely address a specific bus node, i.e. baseband design block, and the sub-node address is used to identify the specific module within the design block. The node address size of 8 bits allows 256 baseband design blocks to be addressed, with up to 32 modules addressed with the 5 bits of sub-node address.

Node address does not necessarily stand for the address of a physical device such as ASIC (Application Specific Integrated Circuit). A device may have one or more node addresses and the nodes may have varying number of active sub-node addresses. For example, in an ASIC that holds both modulator (up conversion) and channelizer (down conversion) design blocks, the blocks typically have separate node addresses.

The general control block of a node, if applicable, is typically addressed using sub-node address 00000.

Reserved addresses

Address '00000000xxxxx', where 'x' stands for either '0' or '1' bit, is reserved for initial booting of the bus network. Thus, node address '00000000' can be used only as default boot up address. It cannot be assigned permanently to any node.

Address '111111111111' (1FFFh) is reserved for the empty message. Therefore, physical layer will delete all received messages with an all-ones address. However, addresses '1111111100000'-'1111111111110' (1FE0h-1FFEh) can be used, i.e. node address '11111111' (FFh) is valid.

4.3.3 Message Router

Figure 30 illustrates the functionality of the message router. The 13 bit input address of a message is first processed by a mapping unit which typically selects only a subset of the input bits. For example, the node address may only be selected. Refer to Section 7.1.3 for a description of the input parameters of the mapping unit. The transformed address is then used as an index to a routing table, which contains indices of the transceivers into which the message must be transmitted. Note that Message Router shall not change the content of any message. The transformed address is just a temporary parameter used by the router.

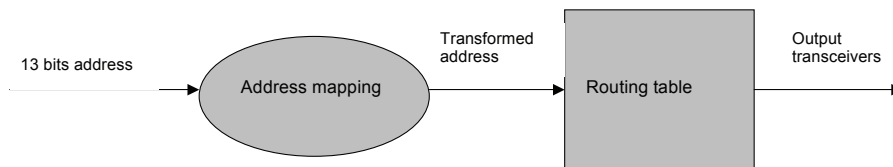


Figure 30: Functionality of message router.

An example of a routing table is given below. In the table, there is a bit vector (row) that corresponds to each transformed address. In the example, two bits wide transformed address is used. Length of the bit vector equals to the number of transceivers that exist in the node. Bit '1' means that the message must be forwarded to the corresponding transceiver while '0' prohibits message transmission. Least Significant Bit (LSB) of the bit vector stands for transceiver of Index 0.

As an example, consider a message with transformed address 10 (2 in decimal number). This message is transmitted by transceivers having indices 1 and 2.

Table 5: An example of a table.

Transformed Address (input)	Transceivers (output)
00	(MSB) 000001 (LSB)
01	000010
10	000110
11	100001

4.3.4 Message Multiplexer and Demultiplexer

Message multiplexer performs time interleaving of messages from N , $N > 1$, input RP3 links to a single output RP3 link as illustrated in Figure 31. The multiplexer shall forward messages from the input links to the output link such that valid RP3 Message Group and Master Frame formats exist at the output link. The mapping algorithm used by the multiplexer shall remain the same for all time and it is set up at bus configuration time. The definition of the frame structure in Section 4.2.2 suggests the use of a round robin algorithm in message multiplexing.

The message multiplexer shall repeatedly perform a re-arrangement of messages from the input links to the output link over a time period that corresponds to the duration of a single message at 768Mbps line rate. Thus, messages from input links k , $0 \leq k < N$, with message slot indices $M_k * i + j_k$ shall be forwarded to messages slots $M_{out} * i + j_{out}$ at the output link, where the line rate of input link k equals to $M_k * 768\text{Mbps}$, the line rate of output link equals to $M_{out} * 768\text{Mbps}$, $M_k \in \{1, 2, 4, 8\}$, $j_k = \{0, \dots, M_k - 1\}$, $M_{out} \in \{1, 2, 4, 8\}$, and $j_{out} = \{0, \dots, M_{out} - 1\}$. Index i , $0 \leq i < N_MG * M_MG$, runs over all message slots of a Master Frame at 768Mbps line rate. All or only a subset of the available input messages are forwarded to the output.

The order according to which messages are mapped from input links to output link can be defined in a format of a multiplexing table. This table, which is actually a vector, consist of M_{out} elements $E_0, \dots, E_{M_{out}-1}$ each $E_{i_{out}} = (D, k, j_k)$ defining an input link and message slot from which the message is copied to the corresponding output message slot j_{out} . Parameter D is set equal to '1' when no input message is copied to that position, i.e. an empty message will be transmitted. Otherwise, $D = '0'$.

Table 6 - Table 9 define mandatory multiplexing algorithms for a set of multiplexing configurations using the format of multiplexing tables.

Table 6: Multiplexing table for the case where all messages from four 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	0, 3, 0

Table 7: Multiplexing table for the case where all messages from two 1536Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 1, 1

Table 8: Multiplexing table for the case where all messages from one 1536Mbps link and two 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 0, 1
3	0, 2, 0

Table 9: Multiplexing table for the case where all messages from two 768Mbps link are multiplexed to a single 1536Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0

Table 10 illustrates a case where messages from three 768Mbps links are multiplexed into a 3072Mbps link.

Table 10: Multiplexing table for the case where all messages from three 768Mbps links are multiplexed to a single 3072Mbps link.

Output position (information only)	Input position, i.e. $E_{i_{out}} = (D, k, j_k)$
0	0, 0, 0
1	0, 1, 0
2	0, 2, 0
3	1, 0, 0

The message demultiplexer performs an inverse operation to the multiplexer, i.e. the output link in the above equations is considered as the input link and input links become output links.



Figure 31: Illustration of message multiplexer.

4.3.5 Summing Unit

Summing unit is located in front of each transceiver, the transmitter port, and all transmitted messages pass through it. When a single message per message slot is to be transmitted, Summing unit forwards the message unaltered to the transceiver. In other words, summing unit will not examine the contents of the message. When two or more messages are targeted to the same message slot and transceiver, Summing unit generates a single output message from the input messages as follows. Header for the output message is copied from one of the input messages. Headers of the input messages should be equal, so any of the messages can be selected. An error is indicated to Application layer if the headers differ. Payload of the output message is a pointwise sum of the payloads of all input messages. In case of complex baseband IQ samples $x_i(n)$, where i denotes Index on the

input message of a Summing unit and n stands for the time index of the samples, pointwise sum $y(n)$ is equal to $y(n) = \sum_i x_i(n)$. Summing unit

and the entire bus uses two's complement code numbers with sign extension. In the summing, saturating arithmetic is used in order to mitigate possible overflows.

As an example, consider two messages each containing four samples. Output message (4, 1, -1, 7) is obtained when performing pointwise sum of real valued messages (3, -1, 5, 4) and (1, 2, -6, 3). Only payload of messages is considered here.

Summing unit is typically activated only for WCDMA, CDMA, 802.16, and LTE data messages. Message collision occurs for example when baseband GSM/EDGE samples are added together. Summing unit detects message collisions by analysing headers of input messages. As an input parameter SUMMING_ALLOWED_FOR_TYPE (see Section 7.1.3), Summing unit receives a list of message types that may be added together. An error is indicated and message transmission is hindered when messages with improper type should be added together. Specifically, in case of message collision, Physical layer should send an empty message due to hindered message transmission but it is also acceptable to transmit one of the colliding input messages to the bus.

Summing unit performs also bit-by-bit comparison of all headers and checks that they are equal.

Only messages of type WCDMA/FDD, WCDMA/TDD, CDMA2000, 802.16, and LTE (see Table 12) may be summed together. Two or more messages of the same type can be added together. A message collision is reported in all other cases.

As an example, SUMMING_ALLOWED_FOR_TYPE = '0000000000000000000000001001100' enables summing of WCDMA/FDD, WCDMA/TDD, and CDMA2000 messages.

Figure 32 illustrates functionality of the Summing unit. In this example, three input messages are shown but K input messages need to be supported.

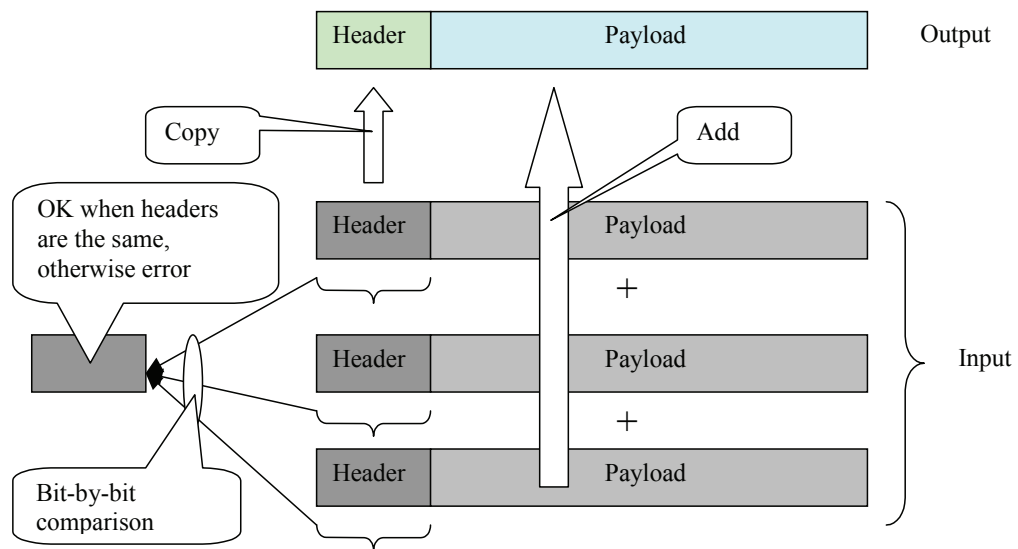


Figure 32: Functionality of Summing unit. Type check of input messages is not shown.

4.4 Application Layer

Application layer represents the user of the protocol and it maps different types of control and data into the payload. The application layer is also responsible for the insertion of the message header: address, type, and timestamp fields.

From bus protocol point of view, Application layer is divided into two parts: air interface applications and bus functions. Major portion of Application layer consist of air interface applications, which are isolated from the bus by "Bus Interface" part. The Bus Interface contains functions that prepare data for transmission over the bus. Also transmission and reception of messages is included. In this section, Bus Interface functionality is described.

4.4.1 Addressing

Application layer will generate message packets with the multicast or point-to-point address in the address field. Refer to Section 4.3.2 for details.

4.4.2 Paths

All data transfers over the bus are performed over paths. Path concept is introduced in order to decouple air interface applications from bus protocol and also to formalise bus configuration process.

A path consists of a set of bus links and message slots that are reserved for data transmission. Bus links connect the source and target nodes together and they are defined by the routing tables. Depending on the bandwidth needed for data communication, an appropriate number of message slots per Master Frame are reserved for the path. Bus manager will provide exact definitions of all paths through the bus. Paths are defined so that message collisions do not exist.

Paths are fixed, i.e. message transfer between any two nodes is always done over the same bus links using pre-specified message slots. Paths are defined before bus initialisation, i.e. message transfers over the bus are deterministic. In case of run-time BTS reconfiguration, paths may need to be modified, added or deleted. Transport layer supports run-time modification of routing tables with minimal corruption of messages. Bus nodes also support run-time modification of message transmission rules but this may be service affecting.

The path taken by a message is determined by the address in the message and the routing tables set up in the bus nodes by the Bus manager.

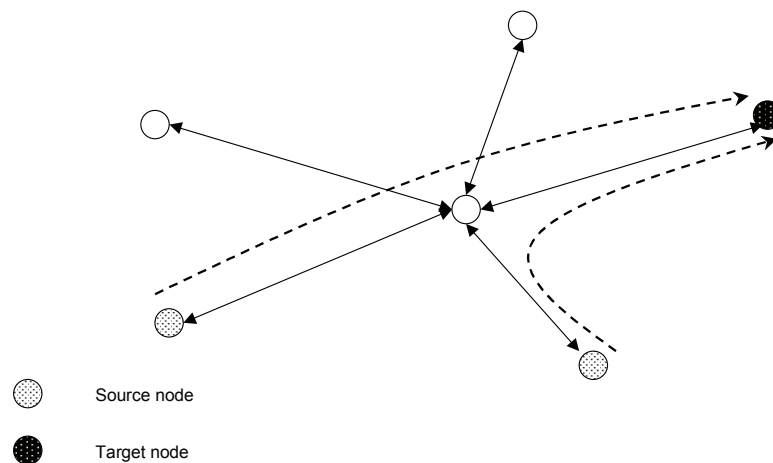


Figure 33: Arbitrary bus configuration with two paths. Message slots are not shown.

4.4.3 Message Transmission Rules

For each path, Bus manager provides detailed rules for message transmission. Rules for paths utilizing data and control message slots are provided separately. As stated in Section 4.2.3, Data Link layer of the bus provides counter values for data and control message slots. Transmission of messages is done with respect to these counters.

There exist two layers of message transmission rules. The rules of the lower layer utilize modulo computation over message slot counters to define RP3 virtual links and their use is mandatory. The rules of the higher layer, which are optional, define paths within RP3 virtual links utilizing bit maps. When the higher layer rules are not used, RP3 virtual links equal to paths.

At the lower layer, message slots for each RP3 virtual link are specified by the pair of numbers (I (Index), M (modulo)) such that equation $MessageSlotCounter \text{ modulo } M = I$ holds. In case of a path using data message slots, $MessageSlotCounter$ runs from 0 up to $(i*(M_MG-1)*N_MG)-1$ while it takes values from 0 up to $(i*N_MG)-1$ in case of control message slots.

As an example, consider transmission of WCDMA data over RP3. For WCDMA, as well as for CDMA, message transmission rules of the lower layer are only used. Assume that a message transmission rule (1, 4) has been provided to a path which uses data message slots, i.e. the Index is equal to 1 while the modulo is 4. This rule states that the node can transmit messages to data message slots having indices 1, 5, 9, 13, 17, ...

At the higher layer, Dual Bit Map concept is applied where two bit maps with maximum lengths of 80 bits (Bit Map 1) and 48 bits (Bit Map 2) are used. The actual lengths of the bit maps are indicated by parameters $Bit_Map_1_Size$ and $Bit_Map_2_Size$. The first bit map Bit_Map_1 is applied $Bit_Map_1_Mult$ times after which the second bit map Bit_Map_2 is used once. The procedure then repeats and reuses the first bit map $Bit_Map_1_Mult$ times. A parameter X specifies the maximum number of antenna-carriers that fits into an RP3 virtual link. Refer to Table 11 for the definition of all parameters of the dual bit map method.

The Dual Bit Map algorithm is the following. Select N unique indices from 0 to $N-1$ for each of the signals (antenna-carriers) that are being transmitted such that $N \leq X$ holds. Start reading the bit map, Bit_Map_1 , from the MSB. If the bit equals 0, a message block of X consecutive message slots from the RP3 virtual channel are available for data transmission. Create an index J that increments from 0 to $X-1$. Send a data message from each of the signals (antenna-carriers) when J is equal to the index selected for each active signal. If the value of the bit is 1, a message block of $X+1$ consecutive message slots from the RP3 virtual channel are available for data transmission and J increments

from 0 to X. Any indices not used to transmit data messages can be used to transfer other messages, e.g. Ethernet or Empty messages. The algorithm continues by repeating the above procedure for the next bit of the *Bit_Map_1* word. To obtain the entire sequence of message blocks, *Bit_Map_1* is repeated *Bit_Map_1_Mult* times followed by the *Bit_Map_2* word when the *Bit_Map_2* size is non-zero.

Currently, parameters of the Dual Bit Map algorithm are defined only for 802.16, LTE and GSM/EDGE data in Appendix D, F and G. Use of these higher layer rules for 802.16 and LTE is mandatory in downlink direction when the Summing Unit (see Section 4.3.5) is activated for type 802.16 or LTE (see Table 12). In uplink direction, use of these rules is optional. Lower layer rules, i.e. the modulo rules, are mandatory both in downlink and uplink directions. Dual Bit Map rules are optional for GSM/EDGE.

Table 11: Definition of the parameters of the dual bit map concept.

Parameter	Definition
X	The maximum number of antenna-carriers that will fit into a given virtual RP3 link
Bit_Map_1_Mult	Number of times the first bit map is repeated
Bit_Map_1	Value of the first Bit Map in hexadecimal number. The Bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_1_Size	Size of the first Bit Map (number of bits)
Bit_Map_2	Value of the second Bit Map in hexadecimal number. The bit Map is read starting from the leftmost (MSB) bit.
Bit_Map_2_Size	Size of the second Bit Map (number of Bits)

Figure 34 illustrates 802.16 data transmission into RP3 virtual link using the Dual Bit Map algorithm. Three OFDMA antenna-carriers with 8.75MHz channel bandwidth are mapped into RP3 link. In this example, we assume that the whole RP3 link with 1536 Mbps line rate is allocated for 802.16 data, i.e. the RP3 virtual channel is specified by parameters (0 (index), 1 (modulo)).

At node initialisation, the Bus manager will provide message transmission rules for the end nodes of the bus. Updated rules are provided during run-time if needed; for example, in case of BTS reconfiguration.

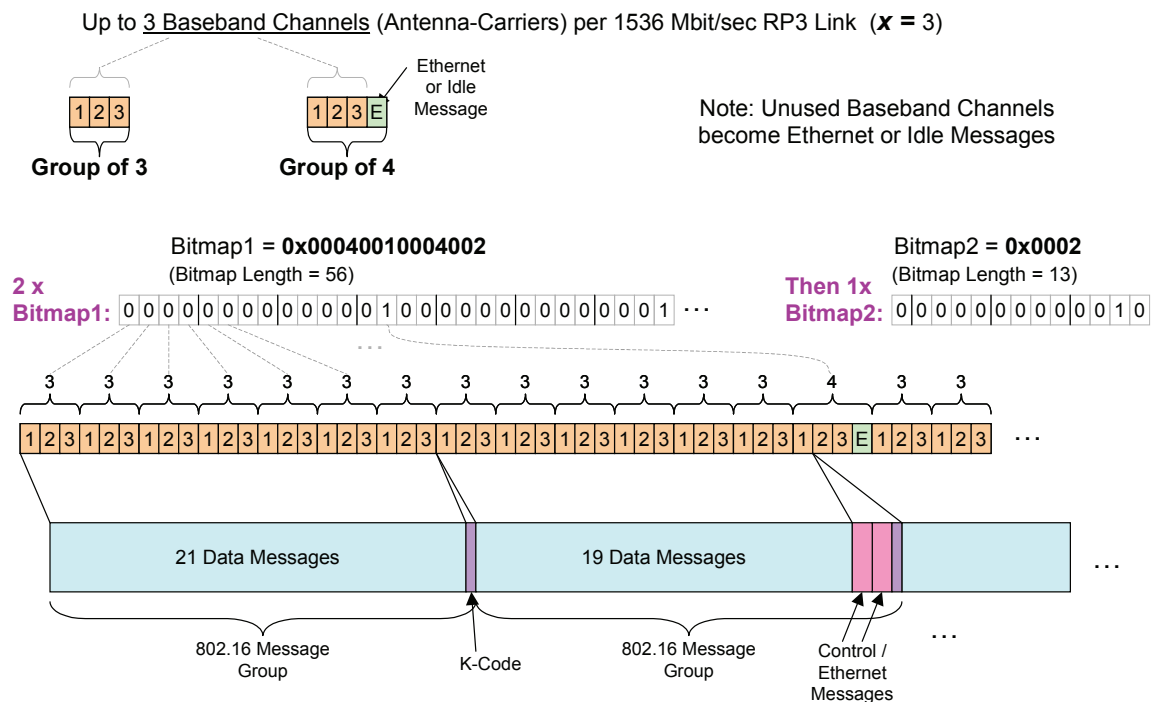


Figure 34: 802.16 data transmission into RP3 link using Dual Bit Map algorithm.

4.4.4 Bus Manager

Bus Manager is responsible for the configuration of the bus. Bus Manager is typically located at Control and Clock Module (CCM) and it is a function of the BTS Resource Manager. When the configuration for the BTS modules is known (the number of antennas and carriers etc), the Bus Manager configures the bus accordingly.

4.4.5 Buffering Requirements

Physical, Data link, and Transport layers of the bus perform minimal buffering, i.e. they process messages immediately when received. Buffers having size of few bytes exist at the Data link layer in order to compensate for propagation delays (see Sections 4.2.5 and 4.2.6).

At Application layer, messages need to be buffered because the bus will serialise messages and data. Consider e.g. WCDMA application where data from parallel sources, such as digitised samples from antennas, are transmitted over the bus in consecutive messages. Buffers are needed both in the transmitter and receiver ends in order to slice the continuous data stream into discrete messages and vice versa. At maximum, a double buffering scheme is used in WCDMA with four chips of data per buffer. The same double buffering concept can be

used also for CDMA and LTE data. A buffer of size six messages is required for each 802.16 signal (antenna-carrier) in order to compensate the jitter caused by message transmission (refer to Section 4.4.3 for the definition of message transmission rules). In GSM/EDGE applications, entire time slot bursts are typically buffered at Application layer and, therefore, serialisation of data on the bus has minor impact.

4.4.6 Message Format – TYPE Field

Application layer is responsible for defining the type of the message. The TYPE field identifies the content of payload data. The following table presents the possible payload types.

Table 12: Content of type field.

Payload data type	Content of Type field
Control	00000
Measurement	00001
WCDMA/FDD	00010
WCDMA/TDD	00011
GSM/EDGE	00100
TETRA	00101
CDMA2000	00110
WLAN	00111
LOOPBACK	01000
Frame clock burst	01001
Ethernet	01010
RTT message	01011
802.16	01100
Virtual HW reset	01101
LTE	01110
Generic Packet	01111
Currently not in use	10000-11111

Most of the TYPE values presented above are self-explanatory. LOOPBACK messages are user defined application layer messages that may be used to monitor link integrity.

4.4.7 Message Format – TIMESTAMP Field

The timestamp field relates the payload data to a specific time instant.

Consider a block of WCDMA or CDMA2000 antenna samples that exist in the payload of a message. In uplink direction, time stamp identifies the time instance when the last sample of the message was available at the output of the channelizer block (down converter, FIR filter). In downlink direction, time stamp defines the time instant when the first sample of the payload must be inserted into the modulator (up converter, FIR filter). Reference time is the WCDMA or CDMA2000 frame clock of the BTS.

The WCDMA time stamp is calculated as

$$TIMESTAMP = \lfloor CHIP\ NUMBER\ IN\ SLOT / 4 \rfloor MOD\ 64$$

where CHIP NUMBER IN SLOT stands for the chip Index of a WCDMA time slot and $\lfloor x \rfloor$ denotes the greatest integer not exceeding x . Thus, $\lfloor x \rfloor$ stands for the integer part or floor of x . All chips of an RP3 message shall have the same TIMESTAMP value as defined by the above equation.

In WCDMA, there exist 100 frames per second and each frame contains 15 time slots. Altogether, there exist 1500 time slots per second while every time slot consists of 2560 chips indicating that CHIP NUMBER IN SLOT takes values between 0 and 2559.

Computation of CDMA2000 time stamp is done analogously to WCDMA time stamp computation, i.e. $TIMESTAMP = \lfloor CHIP\ NUMBER\ IN\ SLOT / 4 \rfloor MOD\ 64$.

Time stamp computation for 802.16 and LTE applies modulo over I&Q sample index, i.e. $TIMESTAMP = \lfloor SAMPLE\ NUMBER\ IN\ AIR\ FRAME / 4 \rfloor MOD\ 64$.

For GSM/EDGE only in downlink direction, the MSB of the timestamp is used to identify the first packet in the timeslot, with a logic '1' identifying the first, with subsequent packets set to a logic '0'. The remaining 5 LSBs of the timestamp represent a count reflecting the packet number with reference to the first packet in the timeslot. The count will wrap-around, but the MSB provides a unique identification of the first packet. Therefore, time stamps of messages containing first samples of a time slot are 100000, 000001, 000010, 000011, 000100, etc.

In the GSM/EDGE uplink direction, the same concept as that of the downlink direction is applied with one exception. The MSB is equal to '1' during the four first messages of a time slot.

1
2
3
4
5
6
7
8
9
0
1
2

3
4
5
6
7
8

9
0
1
2
3
4
5
6
7
8
9

The following sections detail how Application layer maps data into the payload for the different data types. It is intended that data packets are only sent when there is sufficient data to fill them as defined in the following. The only exception is the last packet of the timeslot in GSM/EDGE mode where full amount of data may not be contained.

4.4.8.1

The diagram illustrates a 16-byte payload structure. At the top, a box labeled "PAYLOAD" is shown with a dimension of "16 Bytes" below it. This payload is divided into four equal segments, each labeled "CHIP n", "CHIP n+1", "CHIP n+2", and "CHIP n+3". Each chip segment is further divided into four sub-segments: "I HIGH BYTE", "I LOW BYTE", "Q HIGH BYTE", and "Q LOW BYTE". The total width of the diagram is 16 bytes, and the total height is 16 bytes.

PAYLOAD			
16 Bytes			
CHIP n	CHIP n+1	CHIP n+2	CHIP n+3
4 Bytes	4 Bytes	4 Bytes	4 Bytes
I HIGH BYTE	I LOW BYTE	Q HIGH BYTE	Q LOW BYTE

Figure 35: WCDMA DL Payload Mapping.

4.4.8.2

(both I and Q) is transmitted first (refer to Figure 12).

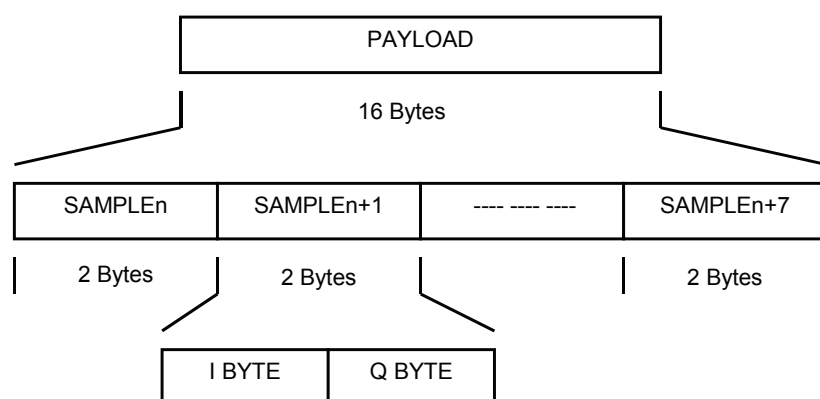


Figure 36: WCDMA UL Payload Mapping.

4.4.8.3 GSM/EDGE Uplink Data Mapping

The GSM/EDGE uplink data stream has a sample rate of 541.667Ksps or 650.000 Ksps (two times the symbol rate).

The GSM/EDGE uplink data stream I&Q data format is 14 bits mantissa and a 4 bit shared exponent, giving 32 bits per sample.

A GSM/EDGE timeslot contains 156.25 or 187.5 symbols. Because of the fractional amount of samples per time slot, consecutive time slots have different amount of samples to be transmitted. For 156.25 symbol scenario three out of every four timeslots will contain 156 symbols worth, with every 4th containing 157. At the 2x sample rate this equals to 312 or 314 samples per time slot. For 187.5 symbol scenario the respective numbers for every other time slot are 187 and 188 symbols, which mean at 2x over sampling ratio 374 and 376 samples per time slot. The samples are fully packed into payloads due to which the last message of a time slot has different number of samples.

The final packet will contain a Sample Count Indicator (SCI) allowing the number of valid bytes in the final message to be identified. See Table 13 for more details.

Table 13: Sample Count Indicator.

SCI	Sample count
000	312 samples per time slot
100	314 samples per time slot
001	374 samples per time slot
010	376 samples per time slot

In addition, other time slot related information may be contained within the final packet. All this information will be packed into the sample size,

i.e. 32 bits, and will reside in the packet as if it were sample 315 or 377, as illustrated in the figure below.

When extracting the data, the receiver should assume that every timeslot has 315 or 377 samples within it. The baseband processing block should first read sample 315 or 377 to determine how many valid samples are within the buffer. Sample rate information is exchanged in upper protocol layers for example using RP3 control messages.

Figure 37 summarises GSM/EDGE/EGPRS2 uplink data mapping.

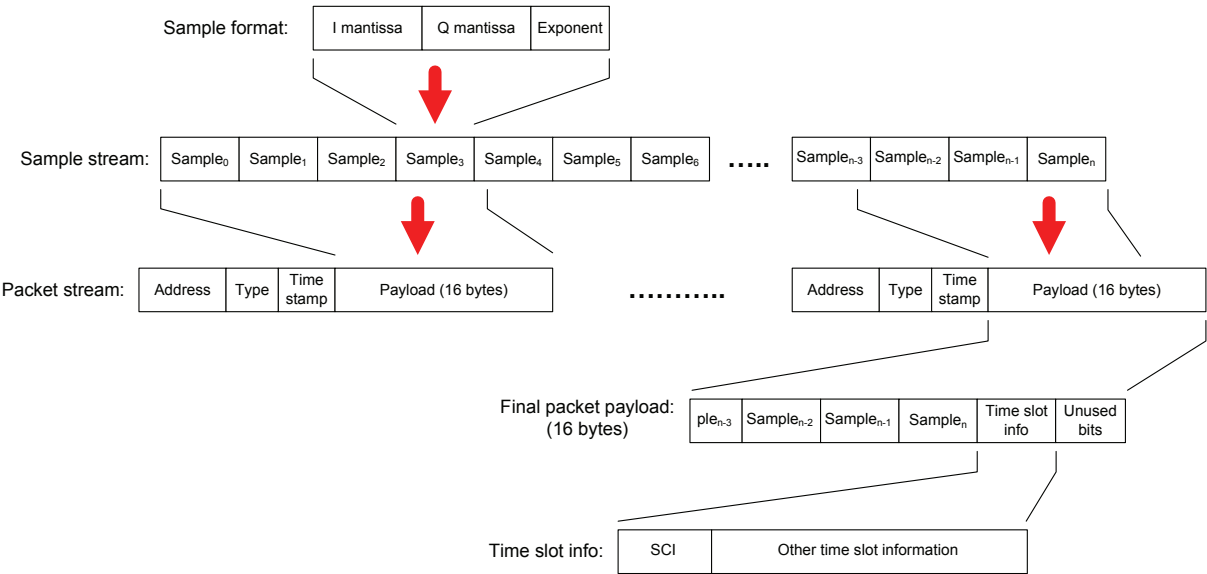


Figure 37: GSM/EDGE/EGPRS2 Uplink Payload Data Mapping

Detailed parameters for GSM/EDGE/EGPRS2 message transmission are provided in Appendix G.

4.4.8.4 GSM/EDGE Downlink Data Mapping

Two scenarios are supported in GSM/EDGE downlink. The GSM/EDGE downlink data stream can be transmitted in either in hard bits or up converted IQ data stream.

Hard bit data stream consists of 156.25 or 187.5 symbols per time slot. Integer number of symbols is achieved by using last symbol for 1.25 or 1.5 symbol periods, giving thus either 156 or 187 symbols to be transmitted per antenna carrier per time slot. For each symbol, 8 bits are used.

In up converted IQ data option, one or more times over sampling is used for both symbol rates. Samples with two's complement code with 16 bit I and 16 bit Q are used.

In addition to the carrier data bits, it is necessary to send control data including carrier, power control, and phase/gain information.

In downlink, a time slot data to a modulator is partitioned in data messages, carrier control information messages, and power control information messages. The associated control is packed into control messages in order to protect the data by CRC check. Furthermore, in order to protect the control against bit errors, control messages can optionally sent twice over the bus. If CRC of the first associated control message indicates bit error, the receiver decodes the second, copy message. If control messages for a time slot have CRC failures and no correct message is received, Application layer is responsible for error handling.

Typically, respective channelizer (down converter) in the uplink direction needs also to have the associated control information. Therefore, after sending GSM/EDGE downlink data and control to modulator, baseband processing block sends frequency control and Gain Control messages to channelizer (down converter).

Detailed parameters for GSM/EDGE/EGPRS2 message transmission are provided in Appendix G.

4.4.8.5 CDMA2000 Downlink Data Mapping

The CDMA2000 downlink data stream has a chip rate of 1.2288 Mcps with an I&Q data format each of 16 bits giving 4 bytes per chip. This allows 4 consecutive chips of a single CDMA signal (antenna-carrier) to be mapped into the payload as illustrated below. Two's complement code is used to represent both I and Q sample values.

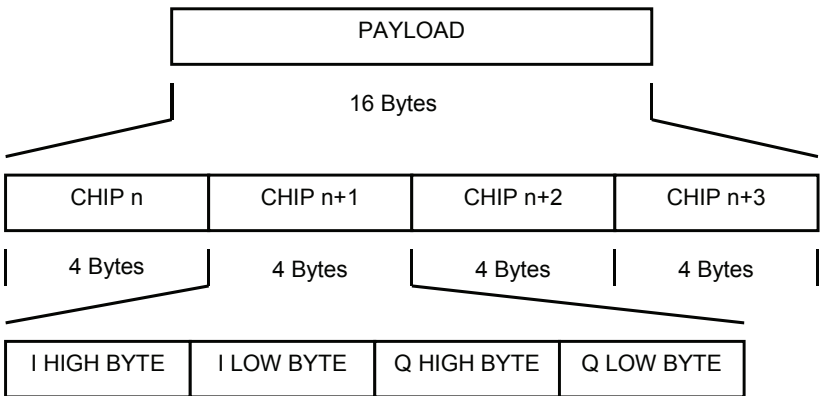


Figure 38: CDMA2000 DL Payload Mapping.

4.4.8.6 CDMA2000 Uplink Data Mapping

The CDMA2000 uplink data stream has a sample rate of 2.4576 Msps (two times the chip rate), with an I&Q data format each of 8 bits giving 2 bytes per sample. This allows 8 consecutive samples (four chips) of a single CDMA2000 signal (antenna-carrier) to be mapped into the payload as illustrated below. As in case of downlink data transfer, two's

complement code is used and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

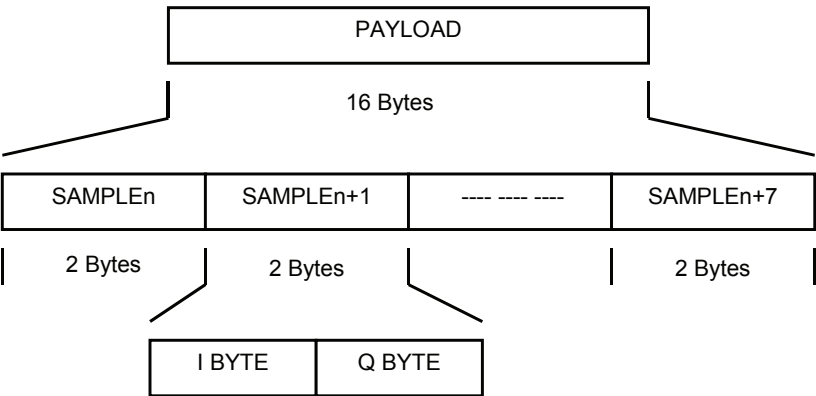


Figure 39: CDMA2000 UL Payload Mapping.

4.4.8.7 802.16 Downlink and Uplink Data Mapping

RP3 protocol supports data transfer of several 802.16 profiles, each with a specific sampling rate and multiple access method, as defined in Appendix D. For each profile, the same sampling rate is applied for both downlink and uplink data streams and no oversampling is applied, i.e. antenna-carrier data is transferred over RP3 link using sampling rates defined in Appendix D. Each I&Q sample consists of four bytes which allows four consecutive I&Q samples of a single 802.16 signal (antenna-carrier) to be mapped into the payload as illustrated below. Sixteen bit two's complement code is used for I and Q sample values and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

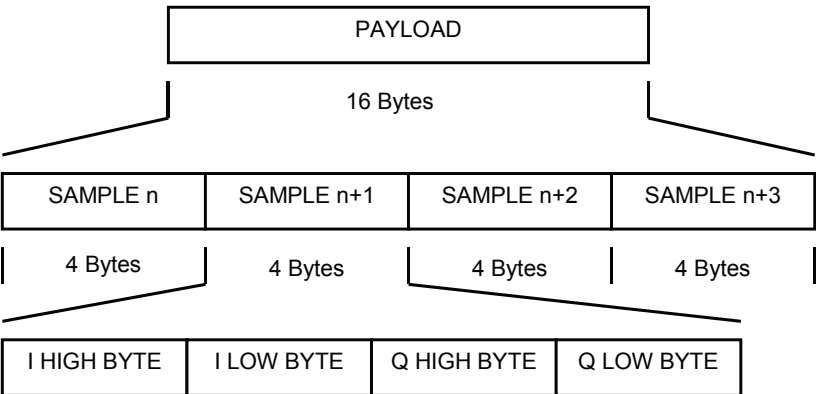


Figure 40: 802.16 downlink and uplink payload mapping.

4.4.8.8 LTE Downlink and Uplink Data Mapping

RP3 protocol supports data transfer of all LTE profiles, each with a specific sampling rate, as defined in Appendix F. For each profile, the same sampling rate is applied for both downlink and uplink data

streams and no oversampling is applied, i.e. antenna-carrier data is transferred over RP3 link using sampling rates defined in Appendix F. Each I&Q sample consists of four bytes which allows four consecutive I&Q samples of a single LTE signal (antenna-carrier) to be mapped into the payload as illustrated below. Sixteen bit two's complement code is used for I and Q sample values and the MSB of a sample (both I and Q) is transmitted first (refer to Figure 12).

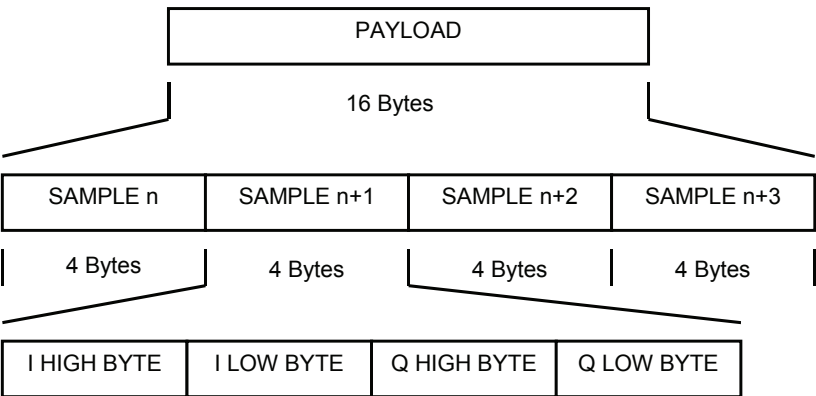


Figure 41: LTE downlink and uplink payload mapping.

4.4.9 Control and Measurement Data Mapping

Control and measurement messages, as identified by the CONTROL and MEASUREMENT type fields, use the payload to transport control and measurement information. A higher layer protocol is required within the payload to provide error detection. The following details two options for implementing the control and measurement signalling protocols.

4.4.9.1 Generic Control Message

Generic control message is illustrated in Table 14 and Figure 42 below, where the control message format consists of two payload fields: the message data and the 16 bit CRC. The timestamp field contains the value '000000' identifying this control message type.

The MSB of each message field is transmitted first (refer to Figure 12).

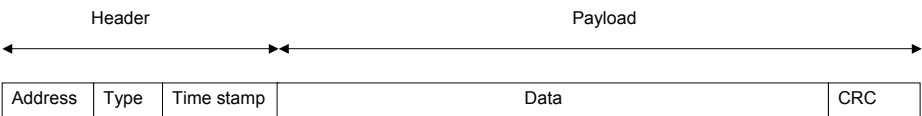


Figure 42: Generic control message.

Table 14: Content of generic control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000000
Data, 14 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

4.4.9.2 Control Message for Air Interface Synchronized Operations

Some control operations over the RP3/RP3-01 may need to be synchronized to a specific air interface frame. For these applications, a specific control message format is introduced as defined in Table 15 and Figure 43 below. The timestamp field contains the value '000001' identifying this control message type.

Table 15: Content of air interface synchronized control message.

Field	Value
Address	Any valid address
Type	00000 (control)
Timestamp	000001
Control subtype, 1 byte	Any content
Frame number, 1 byte	Least significant four bits of this byte are LSBs of air frame number. Four MSBs are set equal to '0000'.
Frame sample number, 3 bytes	Sample number within designated frame number to mark timing of control information.
Data, 9 bytes	Any content
CRC check, 16 bits	CRC check sum computed over the header and payload

A 24 bit sample counter, which counts samples over an air interface frame and resets at start of frame, is applied with the air interface synchronized control messages.

The MSB of each message field is transmitted first (refer to Figure 12).

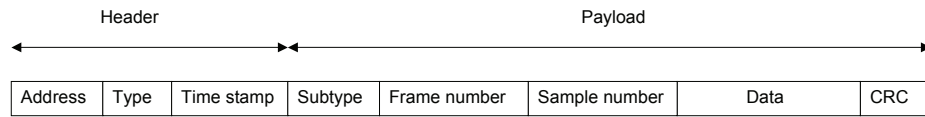


Figure 43: Air interface synchronized control message.

4.4.9.3 Generic Packet

The Generic Packet is a mechanism that allows multiple RP3 messages to represent a larger packet. Table 16 below defines the content of a RP3 message belonging to the Generic Packet.

Table 16: Content of the Generic Packet.

Field	Content
Address	Any valid address
Type	011111 (Generic Packet)
Time Stamp	See Table 17
Data, 16 bytes	A slice from a larger packet that is transferred over RP3

The time stamp field within the RP3 header is used to identify RP3 messages that belong to the same larger generic packet using two bits (MSBs) of the time stamp as Start Of Packet (SOP) and End Of Packet (EOP) indicators. The rest of the time stamp bits can optionally be used for packet identification for supporting up to 16 simultaneously transmitted generic packets to the same target address. The number of supported packet identifications can be chosen based on application. The four least significant bits of the time stamp field are set to zero if there does not exist need to support simultaneous packets to the same target address.

Table 17: Content of the time stamp field.

Time Stamp	Payload Content
10xxxx, where xxxx is set to 0000 (binary) or is optionally a binary number used for packet indication.	SOP: 16 first bytes of a Generic Packet + possible pad + CRC. The first byte of the Generic Packet is located immediately after RP3 header.
00xxxx, where xxxx is the same than for SOP	Next (second) RP3 message containing a part of the Generic Packet + possible pad + CRC.
...	
00xxxx, where xxxx is the same than for SOP	Nth RP3 message containing a part of the Generic Packet + possible pad + CRC.
11xxxx, where xxxx is the same than for SOP	EOP: The last RP3 message containing a slice from the Generic Packet + possible pad + CRC with packet identification xxxx.

A 16 bit CRC check sum is computed over the whole Generic Packet and possible pad bits and is then appended after the actual Generic Packet bits and pad. The content of the last RP3 message that has been allocated for Generic Packet + possible pad + CRC transfer is as defined in Table 18. The length of any Generic Packet + CRC is an integer multiple of 16 bytes, i.e. the last RP3 message transferring a portion of the Generic Packet is always full. Upper layer will provide pad bits when needed.

Table 18: Payload of last message of Generic Packet.

Field	Value
Generic packet bits, $0 < P < 112$ bits (14 bytes)	Content is arbitrary
–Possible pad, $Pad = P - 112$ bits	'0' bits
Two last bytes (16 bits) of the payload	CRC check

Generic Packets with CRC failure shall be indicated to upper protocol layers and dropped by default. For every SOP there is exactly one legal EOP. If an EOP is received without a SOP, the error condition shall be indicated to upper protocol layers. If there is a SOP and then another SOP (without an EOP) the reception buffer may be flushed and the error condition shall be indicated to upper protocol layers.

4.4.9.4 CRC Computation

For both control message options and for the Generic Packet defined above, the CRC is applied to the address, type, and timestamp fields of the message header as well as to the actual payload data. In total, 136 bits (17 bytes) are CRC protected. Generator polynomial $X^{16}+X^{12}+X^5+1$ is used with the high bit transmitted first. Initially, all CRC shift register elements are set equal to logical zero. Each control message enters the CRC shift register MSB first, i.e. leftmost bit of the message first (see Figure 43).

4.4.9.5 Measurement Data Mapping

The RP3 interface facilitates the support and implementation of generic measurements and air interface synchronized measurements. Measurement messages use the same field format as the control messages with the Type field set to '00001' (Measurement). Thus, two options exist as defined in Section 4.4.9.1 and Section 4.4.9.2.

5 Electrical Specifications

This sub-section defines the electrical specifications for the RP3 physical layer.

5.1 Overview

AC electrical specifications are given for both transmitter and receiver. They are specified for Baud Frequencies of 768, 1536, 3072, and 6144 MBaud.

The transmitter specification uses voltage swings that are capable of driving signals across RP3 compliant interconnect. Five RP3 compliant interconnects are defined.

To ensure interoperability between components operating from different supply voltages or implemented in different technologies, AC coupling shall be used at the receiver input.

The overall performance requirement for BER shall be 10^{-15} for all Types of interconnect.

5.1.1 Explanatory Note on Electrical Specifications

The parameters for the AC electrical specifications are guided by existing standards. For the line rates up to 3072 MBaud, the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 [3] is used as a suitable basis to be modified for applications at the RP3-specific baud intervals described herein. For the 6144 MBaud line rate, the references are OIF-CEI-02.0 [14] Interoperability Agreement with its section 7 and related clauses and the Serial RapidIO v2 PHY specifications [15], which are also based on the OIF agreement, to be adapted to the specific needs in OBSAI.

5.1.2 Compliance Interconnect

Five RP3 compliant interconnects are defined¹:

- TYPE 1: A low loss interconnect definition specified in Section 5.4.1. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 2: A worst case, higher loss interconnect definition specified in Section 5.4.2. This interconnect shall be applied to 768 and 1536 Mbaud line rates.
- TYPE 3: A low loss interconnect definition specified in Section 5.4.3. This interconnect shall be applied to 768, 1536, and 3072 Mbaud line rates.
- TYPE 4: A low loss interconnect definition specified in Section 5.4.4, targeting a PCB trace length from TX to RX of minimum 600 mm with 2 connectors. It shall be applied to 1536, 3072, and 6144 Mbaud line rates.
- TYPE 5, optional: A low loss interconnect definition specified in Section 5.4.4, targeting a PCB trace length from TX to RX of minimum 1000 mm with 2 connectors. It shall be applied to 1536, 3072, and 6144 Mbaud line rates.

Background information on all types interconnects is provided in Appendix E.

Note: The PCB trace length of TYPE4 and TYPE5 are difficult to be defined in length as the channels highly depend of many parameters such as PCB material, connector etc.

5.1.3 Equalization

With the use of high-speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, transmit and/or receive equalization may be used

At 6144 MBaud line rate, equalization is strongly recommended..

- For TYPE 4 interconnect a Linear Continuous Time equalizer may be used.

¹ Standard FR4 material was used as a reference when deriving the 3072 Mbaud channel model and this worst case model shall be applied both to backplane and front access cases.

- For TYPE 5 interconnect also a Decision Feedback Equalizer (DFE) may be used.

5.2 Receiver Characteristics

The RP3 receiver electrical and timing characteristics are specified in the text and tables of this section. The RP3 receiver characteristics are summarized in Table 19, Table 20, Table 21, and Table 22.

Table 19: Receiver Characteristics – 768 MBaud

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10^{-15} of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

Table 20: Receiver Characteristics – 1536 MBaud

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10^{-15} of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

1

Table 21: Receiver Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Input Differential Voltage	1600	mV	Max.
Receiver coupling	AC		
Return loss			
Differential	10	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode
Common mode	6	dB	
Jitter amplitude tolerance			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Minimum deterministic	0.37	UI p-p	
Minimum deterministic plus random	0.55	UI p-p	
Minimum total	0.65	UI p-p	

2

Table 22: Receiver Characteristics – 6144 MBaud

Parameter	Value	Units	Notes
Bit rate	6144	MBaud	+/- 100 ppm
Unit interval (nominal)	163	pS	
Input Differential Voltage	1200	mV	Max.
Receiver coupling	AC		
Return loss			
Differential	8	dB	Measured relative to 100 Ohm differential and 25 Ohm common mode, 100MHz to 4608 MHz
Common mode	6	dB	
Input Common Mode Voltage	0 – 1800	mV	AC-coupling
Jitter amplitude tolerance			At equalizer output. Specifications include all but 10 ⁻¹⁵ of the jitter population.
Eye mask	0.6	UI p-p	
Bounded high probability Jitter	0.65	UI p-p	
Eye mask	50	mVp	

3 5.2.1 AC Coupling

4 The receiver shall be AC coupled to allow for maximum interoperability
5 between components. AC coupling is considered part of the receiver for
6 purposes of this specification unless explicitly stated otherwise.

7 5.2.2 Input Impedance

8 Receiver input impedance for up to 3072 MBaud shall result in a
9 differential return loss better than 10 dB and a common mode return

loss better than 6 dB from 100 MHz to (0.8 x Baud Frequency).
Differential return loss at 6144MBaud shall be better than 8 dB and a
common mode return loss better than 6 dB from 100 MHz to 3072 MHz.
Receiver input impedance shall be measured at the module interface.
AC coupling components are included in this requirement. The
reference impedance for return loss measurements is 100 Ohm
resistive for differential return loss and 25 Ohm resistive for common
mode.

5.2.3 Receiver Compliance Mask

The RP3 receiver shall comply with the eye mask specified in Figure 44
and Table 23.

The eye pattern of the receiver test signal is measured at the input pins
of the receiving device with the device replaced with a load as defined
in Section 5.3.1.

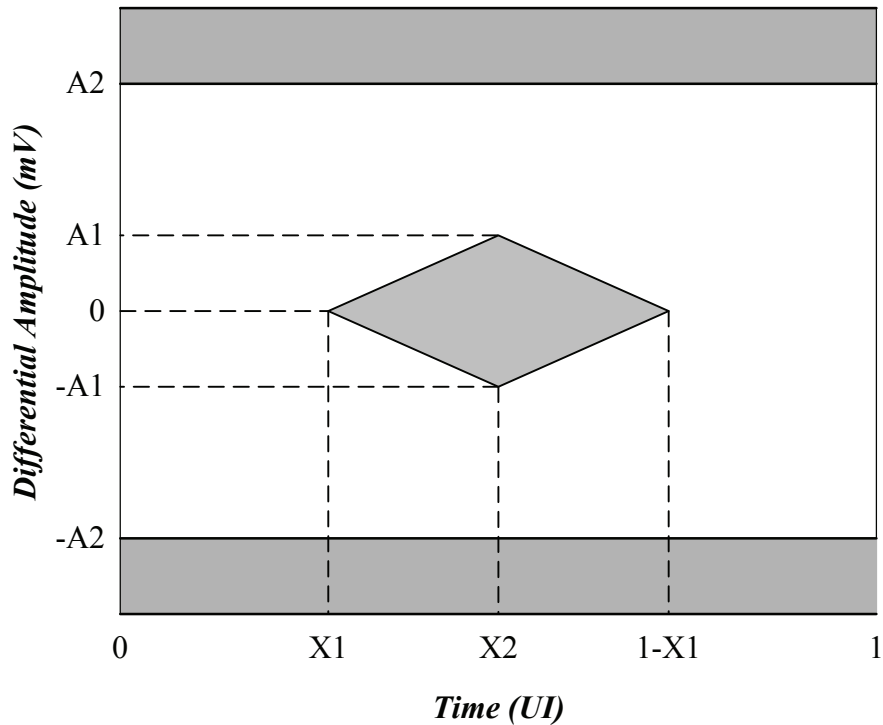


Figure 44: Receiver Compliance Mask

Note: The Receiver Compliance Mask with the values from Table 23
does not include the Sinusoidal Jitter SJ which is added in the Receiver
Jitter Tolerance test, see 5.2.4.

Table 23: Receiver Compliance Mask Parameters

Parameter	Value		Units
	≤ 3072	6144	
X1	0.275	0,3	UI
X2	0.5	0,5	UI
A1	100	50	mV
A2	800	600	mV

The jitter specifications include all but 10^{-15} of the jitter population.

5.2.4 Jitter Tolerance

The RP3 receiver shall tolerate a peak-to-peak total jitter amplitude of 0.65 UI. This total jitter is composed of three components: deterministic jitter, random jitter and an additional sinusoidal jitter. The jitter specifications include all but 10^{-15} of the jitter population.

Tolerance to deterministic jitter shall be at least 0.37 UI p-p. Tolerance to the sum of deterministic and random jitter shall be at least 0.55 UI p-p. The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 45 and the values of Table 24. This additional component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects.

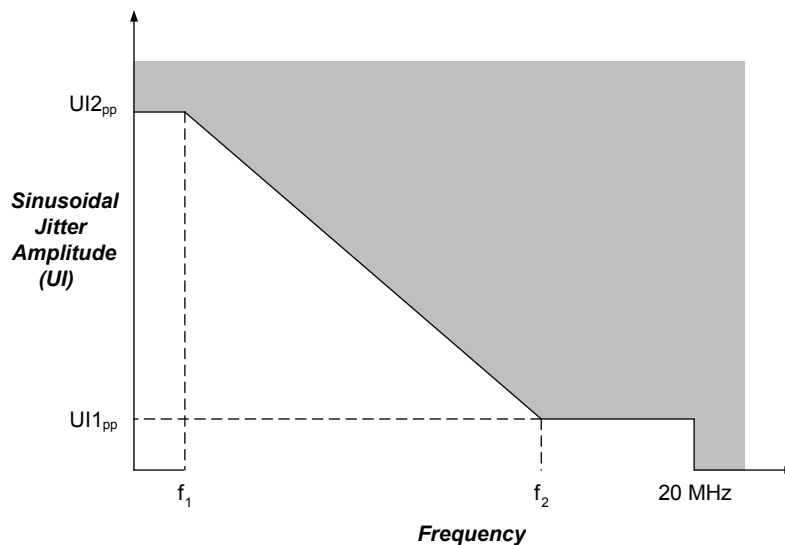


Figure 45: Sinusoidal Jitter Mask

Table 24: Sinusoidal Jitter Mask Values

Baud Frequency (MBaud)	f ₁ (kHz)	f ₂ (kHz)	UI1 _{p-p}	UI2 _{p-p}
768	5.4	460.8	0.1	8.5
1536	10.9	921.6	0.1	8.5
3072	21.8	1843.2	0.1	8.5
6144	36.9	3686	0.05	5

5.2.5 Bit Error Ratio (BER)

For Type 1, 2, and 3 the receiver shall operate with a BER of 1×10^{-15} or better in the presence of an input signal as defined in Section 5.2.3.

For 6144Mbps line rate, noise and crosstalk may have a significant impact on BER. In the same way as in [14] and [15], to verify the receiver under test, the receiver shall meet a BER 10^{-12} with a stressed input eye mask. The stressed eye in such measurement includes sinusoidal, high probability Gaussian jitter as well as additive crosstalk. See also [16].

5.3 Transmitter Characteristics

The RP3 transmitter electrical and timing characteristics are specified in the text and tables of this section. The RP3 transmitter characteristics are summarized in Table 25, Table 26, Table 27 and Table 28.

1

Table 25: Transmitter Characteristics – 768 MBaud

Parameter	Value	Units	Notes
Bit rate	768	MBaud	+/- 100 ppm
Unit interval (nominal)	1302	pS	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

2

Table 26: Transmitter Characteristics – 1536 MBaud

Parameter	Value	Units	Notes
Bit rate	1536	MBaud	+/- 100 ppm
Unit interval (nominal)	651	pS	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

3

1

Table 27: Transmitter Characteristics – 3072 MBaud

Parameter	Value	Units	Notes
Bit rate	3072	MBaud	+/- 100 ppm
Unit interval (nominal)	326	pS	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential amplitude			
Maximum	1600	mV _{p-p}	
Minimum	400	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss	See Equation in Section 5.3.3		
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.17	UI	
Maximum total jitter (JT)	0.35	UI	

2

Table 28: Transmitter Characteristics – 6144 MBaud

Parameter	Value	Units	Notes
Bit rate	6144	MBaud	+/- 100 ppm
Unit interval (nominal)	163	pS	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential amplitude			
Maximum	1200	mV _{p-p}	
Minimum	800	mV _{p-p}	
Absolute output voltage limits			
Maximum	2.3	V	
Minimum	-0.4	V	
Differential output return loss		dB	See 5.3.3
Output Common Mode Voltage	100 – 1700	mV	
Output jitter			Specifications include all but 10 ⁻¹⁵ of the jitter population.
Maximum deterministic jitter (J _D)	0.15	UI	
Maximum total jitter (JT)	0.30	UI	

3

4

5

6

7

A RP3 Transmitter eye mask, to be satisfied with or without transmit equalization, is illustrated in Figure 46. This eye mask is provided

- for information only, not used for RP3 compliance testing in case of line rates up to 3072 MBaud

- to be normative and used for compliance testing in case of 6144 MBaud line rate

The parameters are defined in Table 29.

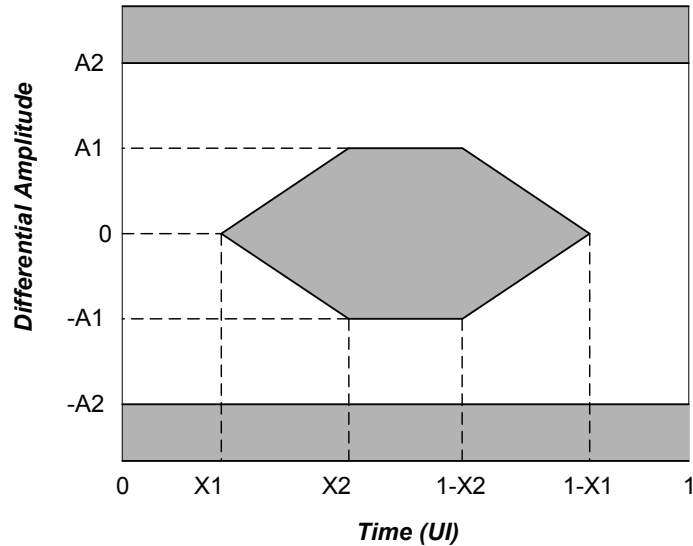


Figure 46: Transmitter Output Mask

Table 29: Transmitter output mask parameters

Parameter	Value		Unit
	≤ 3072	6144	MBaud
X1	0.175	0.15	UI
X2	0.39	0.4	UI
A1	200	400	mV
A2	800	600	mV

5.3.1 Load

The load is 100 Ohms +/- 5% differential up to (0.8 x Baud Frequency) unless otherwise noted.

5.3.2 Amplitude

For baud rates ≤ 3072 MBaud, the maximum transmitter differential amplitude shall be 1600 mV_{p-p}, including any transmit equalization. The minimum transmitter differential amplitude shall be 400 mV_{p-p}.

For a baud rate of 6144 MBaud, the maximum transmitter differential amplitude shall be 1200 mV_{p-p}, including any transmit equalization. The minimum transmitter differential amplitude shall be 800 mV_{p-p}. To achieve the best far end eye opening, the amplitude should be programmable.

The minimum amplitude may not be suitable for transmission over a compliant channel. The absolute driver output voltage shall be between -0.4 V and 2.3 V with respect to ground. DC-referenced logic levels are not defined, as the receiver is AC coupled.

5.3.3 Output Impedance

For baud rates ≤ 3072 MBaud, the differential return loss, SDD22, of the transmitter shall be better than:

- -10 dB for $(\text{Baud Frequency}/10) < \text{Freq}(f) < 625 \text{ MHz}$, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \leq \text{Freq}(f) \leq (\text{Baud Frequency}) \text{ MHz}$

For baud rates ≤ 3072 (FFS) MBaud, the differential return loss, SDD22, of the transmitter shall be better than:

- -8 dB for $100 \text{ MHz} < f < 3072 \text{ MHz}$, and
- $-8 \text{ dB} + 16.6 * \log_{10}(f/3072 \text{ MHz}) \text{ dB}$ for $3072 \text{ MHz} \leq f \leq 6144 \text{ MHz}$

Differential return loss shall be measured at the module interface. The reference impedance for the differential return loss measurements is 100 Ohm resistive. The output impedance requirement applies to all valid output levels.

5.3.4 Transmitter Compliance

To measure compliance of an RP3 transmitter, the transmitter shall be connected to a compliance interconnect model. RP3 specifies five interconnect models for transmitter compliance testing, as introduced in 5.1.2:

In all cases, the RP3 transmitter shall be compliant if the signal presented to the RP3 receiver at the end of the compliance interconnect model (far-end) meets the minimum RP3 receiver compliance mask.

A compliant RP3 transmitter shall meet TYPE 1 and TYPE 2 compliance interconnect test cases, or TYPE 3, or Type4, or Type 5 compliance interconnect test case. In case of 6144 MBaud, Type 4 and

Type 5, the “Statistical Eye” methodology shall be used for compliance testing as described in [2] (FFS) and [3].

5.4 Measurement and Test Requirements

This section defines the measurement and test requirements for an RP3 electrical interface. These measurement and test requirements are based upon those of the XAUI electrical interface as specified in Clause 47 of IEEE 802.3ae-2002 [3] for Type 1, 2 and 3 compliant interconnects. The measurement and test requirements for Type 4 and 5 compliant interconnects are based on the Rapid IO Part6: LP-Serial Physical Layer specification Rev.2.0 [15] or OIF-CEI-02.0 agreement [14] respectively.

Typical test instruments and their cabling are based on single ended 50 Ohm termination. In order to achieve the required 100 Ohm differential, as well as common mode 25 Ohm, resistive loads, in all measurements and tests related to electrical specifications, both lines of a differential transmission interconnect pair shall be terminated individually with 50 Ohm +/- 5% resistors to ground. Such a load shall maintain this accuracy in its resistive characteristics at least up to 0.8 x Baud Frequency. The requirements for the Type 4 and 5 compliant interconnect test and measurements are detailed in Chapter 10 of [15].

5.4.1 TYPE 1 Compliance Interconnect Definition

The TYPE 1 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 1 compliance interconnect shall be:

$$\text{Differential Insertion Loss (F)} \leq (0.2629 \times \sqrt{F}) + (0.0034 \times F) + (12.76 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

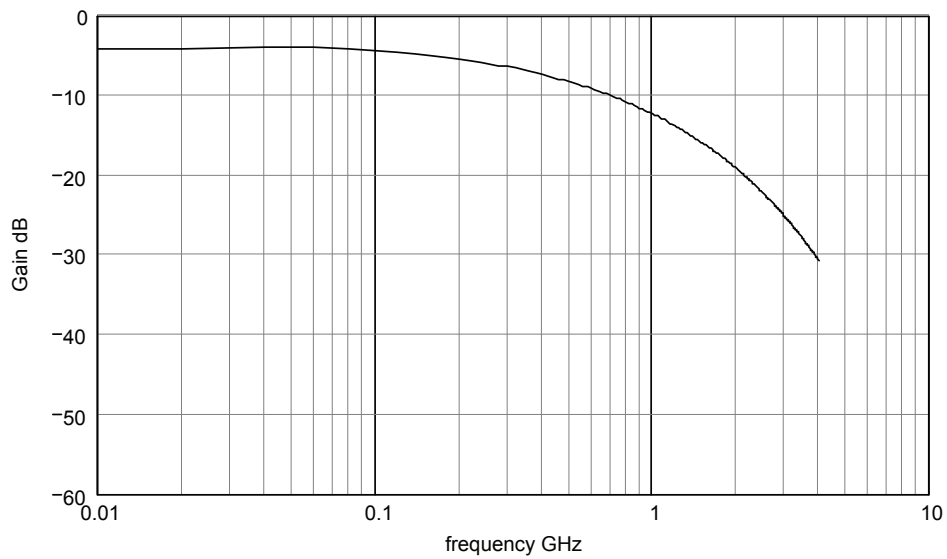


Figure 47: TYPE 1 Compliance Interconnect Differential Insertion Loss

5.4.2 TYPE 2 Compliance Interconnect Definition

The TYPE 2 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768 and 1536 Mbaud line rates.

The differential insertion loss, in dB with F in MHz, of the TYPE 2 compliance interconnect shall be:

$$\text{Differential Insertion Loss (F)} \leq (0.1 \times \sqrt{F}) + (0.011 \times F) + (6 / \sqrt{F})$$

for all frequencies from 100 MHz to 2000 MHz.

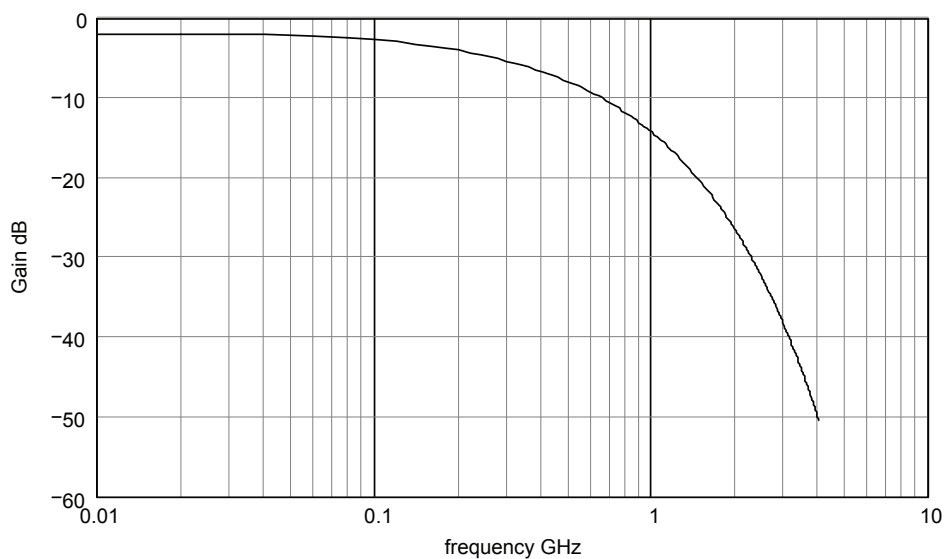


Figure 48: TYPE 2 Compliance Interconnect Differential Insertion Loss

5.4.3 TYPE 3 Compliance Interconnect Definition

The TYPE 3 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 768, 1536, and 3072 Mbaud line rates.

The worst case TYPE 3 channel differential Insertion Loss (transfer function) SDD21 shall meet Equation 1 where as the variable f (frequency) unit is in GHz. The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 return loss, therefore differential coupling effects may be neglected for insertion loss SDD21.

$$IL_{SDD\ 21}(dB) = \begin{cases} -10 \sqrt{f/f_0} & ; f < f_0 \\ -7(f - f_0)^{1.15} - 10 & ; f_0 \leq f < 4.5GHz \end{cases}$$

$$f_0 = 1.5GHz$$

Equation 1: Differential Transfer Function (IL) Model

Figure 49 depicts the above TYPE 3 transfer function chart.

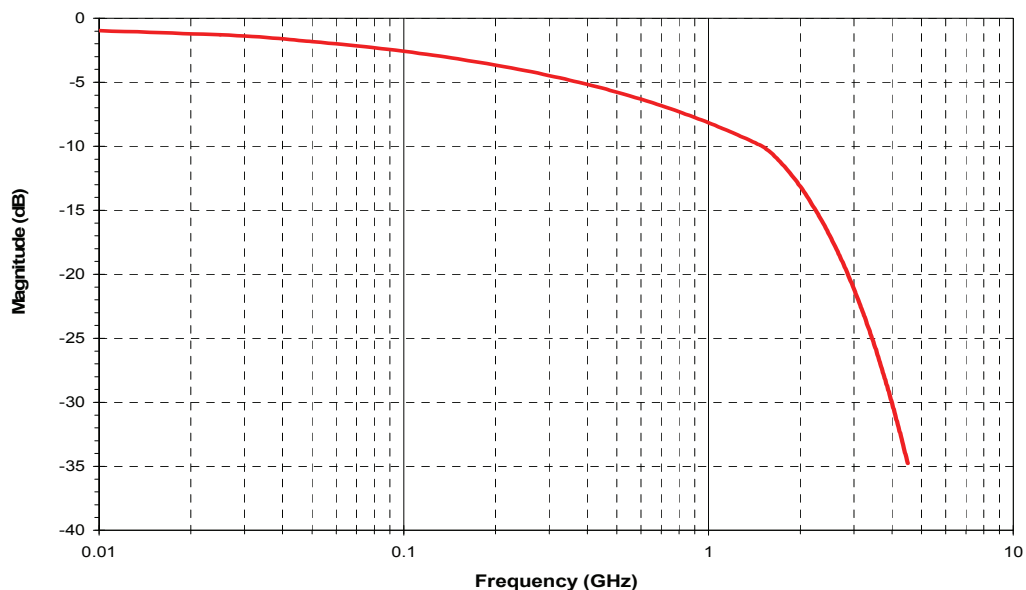


Figure 49: TYPE 3 Differential Transfer Function Chart

The worst case TYPE 3 channel differential return loss (RL) SDD11 shall meet Equation 2 where as the variable f (frequency) unit is in GHz.

$$RL_{SDD11}(dB) = \begin{cases} -15 & ; f < 1GHz \\ 5(f) - 20 & ; 1 \leq f < 3GHz \\ -5 & ; 3 \leq f < 4.5GHz \end{cases}$$

Equation 2: Differential Return Loss Model

The equation specified in terms of two ports mixed mode S-Parameters assuming the channel meets TYPE 3 insertion loss, therefore differential coupling effects may be neglected for return loss SDD11.

Figure 50 depicts the above TYPE 3 Return Loss chart.

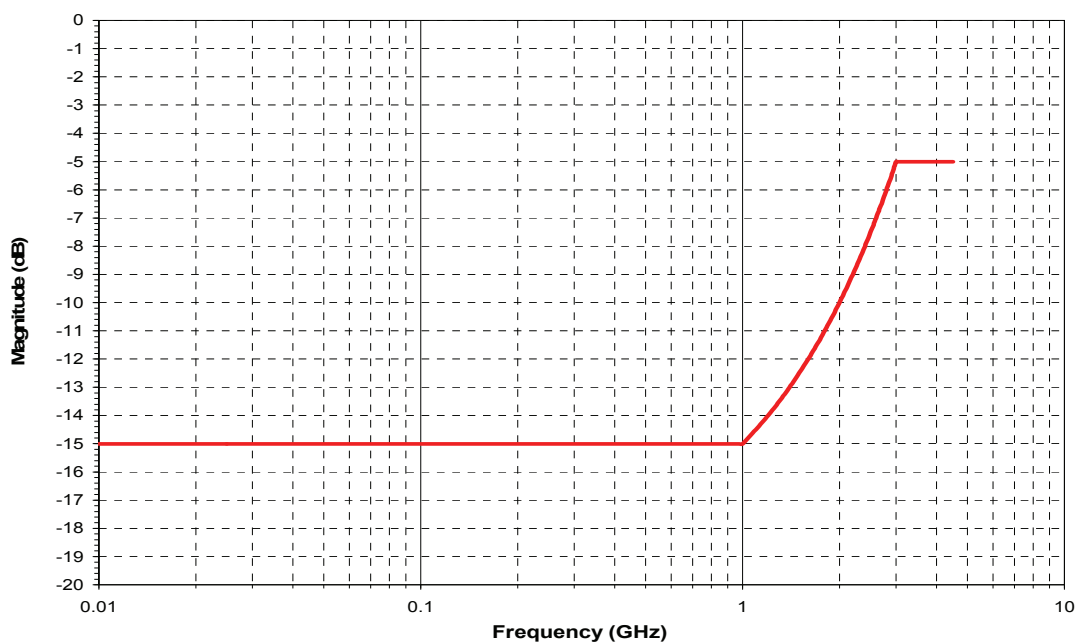


Figure 50: TYPE 3 Differential Return Loss Chart.

5.4.4 TYPE 4 and TYPE 5 Compliance Interconnect Definition

A serial link is comprised of a transmitter, a receiver, and a channel which connects them. Typically, two of these are normatively specified, and the third is informatively specified. In this specification, the transmitter and channel are normatively specified, while the receiver is informatively specified.

This specification follows the OIF inter-operability or compliance methodology and is based on using transmitter and receiver reference models, measured channel S-parameters, eye masks, and calculated “statistical eyes”. These “statistical eyes” are determined by the reference models and measured channel S-parameters using publicly available StatEye MATLAB® scripts and form the basis for identifying

compliant transmitters and channels. Compliant receivers are identified through a BER test.

Reference models are used extensively because at 6.144Gbaud data rates the incoming eye at the receiver may be closed. This prevents specifying receiver compliance through receiver eye masks as is typically done at lower data rates.

A compliant channel is determined using the appropriate transmitter and receiver reference model, measured S-parameters for the channel under consideration, and the StatEye script. A compliant channel is one that produces a receiver equalizer output “statistical eye” which meets a $BER \leq 10^{-15}$ using StatEye.

The reference model for the complete serial link as defined in [4] is shown in figure xxx.

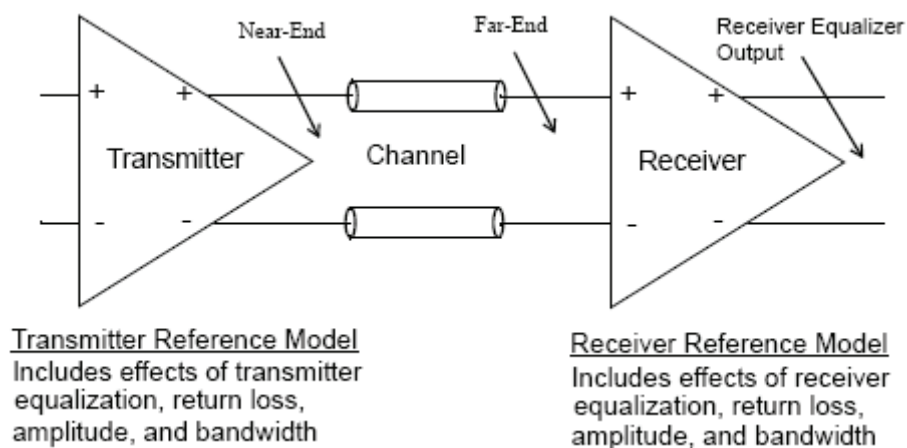


Figure 51: OIF reference model.

5.4.4.1 TYPE 4 and TYPE 5 Channel Compliancy

The following steps shall be made to identify which channels are to be considered compliant:

The forward channel and significant crosstalk channels shall be measured using a network analyzer 6.144 Mbaud

1. A single pre or post tap transmitter with ≤ 6 dB of emphasis, with infinite precision accuracy.
2. A Tx edge rate filter: simple 40dB/dec low pass at 75% of baud rate, this is to emulate both Rx and Tx -3dB bandwidths at 3/4 baud rate.
3. A transmit amplitude of 800mVppd.

4. Additional Uncorrelated Bounded High Probability Jitter of 0.15UIpp (emulating part of the Tx jitter).
5. Additional Uncorrelated Unbounded Gaussian Jitter of 0.15UIpp (emulating part of the Tx jitter).
6. The reference transmitter shall use the worst case transmitter return loss at the baud frequency. In order to construct the worse case transmitter return loss, the reference transmitter should be considered to be a parallel R and C, where R is the defined maximum allowed DC resistance of the interface and C is increased until the defined maximum Return Loss at the baud frequency is reached.
7.
 - (a) TYPE 4
The reference receiver uses a continuous-time equalizer with 1 zero and 1 pole in the region of baudrate/100 to baudrate. Additional parasitic zeros and poles must be considered part of the receiver vendor's device and The TYPE 4 interconnect definition shall be used to validate the compliance of an RP3 transmitter for 6144 Mbaud line rates. be dealt with as they are for the reference receiver. Pole and Zero values have infinite precision accuracy. Maximum required gain/attenuation shall be less than or equal to 4dB.
 - (b) TYPE 5
The reference receiver uses a 5 tap DFE, with infinite precision accuracy.
8. The reference receiver shall use the worst case receiver return loss at the baud frequency. In order to construct the worse case receiver return loss, the reference receiver should be considered to be a parallel R and C, where R is the defined maximum allowed DC resistance of the interface and C is increased until the defined maximum Return Loss at the baud frequency is reached.

Table 30: Receiver Equalization Output Eye Mask

Parameter	Symbol	Max	Units
Eye mask	R_X1	0.30	UI
Eye mask	R_Y1	50	mV
Bounded High Probability Jitter	R_BHPJ	0.325	UI

9. Any parameters that have degrees of freedom (e.g. filter coefficients or sampling point) shall be optimized against the

amplitude, at the zero phase offset, as generated by the Statistical Eye Output, e.g. by sweeping all degrees of freedom and selecting the parameters giving the maximum amplitude. A receiver return loss, as defined by the reference receiver, shall be used.

10. The opening of the eye shall be calculated using Statistical Eye Analysis methods, as per Section 8.7.5, "Statistical Eye Methodology", and confirmed to be within the requirements of the equalized eye mask as specified in Table 10-12 at the required BER, 10-12.

5.4.5 Eye Mask Measurements for TYPE 1, 2, and 3 Compliant Interconnects

For the purpose of eye mask measurements, the effect of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for mask measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae-2002 [3]. The RP3 link shall be active in both transmit and receive directions, and opposite ends of the link shall use synchronous clocks. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 1×10^{-15} . The eye pattern shall be measured with AC coupling and the compliance mask centered at 0 Volts differential. The left and right edges of the mask shall be aligned with the mean zero crossing points of the measured data eye as illustrated in Figure 52.

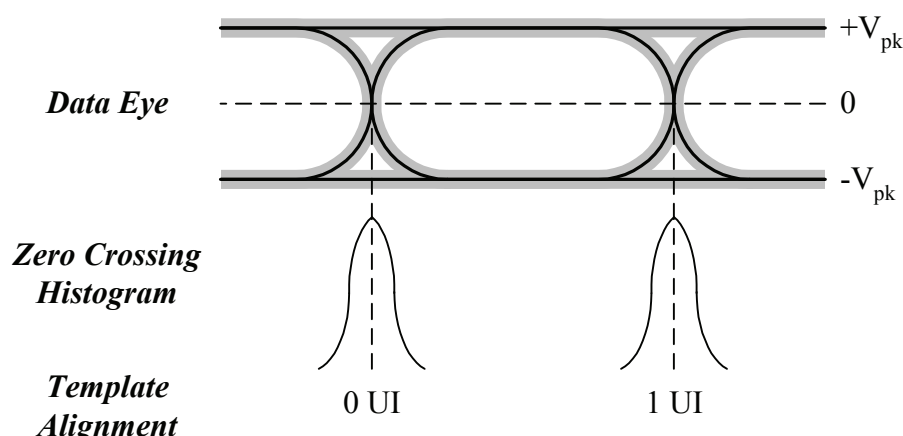


Figure 52: Eye Mask Alignment

5.4.6 Transmit Jitter for TYPE 1, 2, and 3 Compliant Interconnects

Transmit jitter shall be measured at the driver output when terminated according to the definition in Section 5.4.

5.4.7 Jitter Tolerance

5.4.7.1 TYPE 1, 2, and 3 Compliant Interconnects

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 5.2.4 and then adjusting the signal amplitude until the data eye contacts the 4 points of the minimum eye opening of the receiver compliance mask specified in Figure 44 and Table 23. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye mask measurement requirements are defined in Section 5.4.5. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade rolloff below this. The required sinusoidal jitter specified in Section 5.2.4 is then added to the signal and the test load is replaced by the receiver being tested.

5.4.7.2 TYPE 4 and 5 Compliant Interconnects

For Type 4 and Type 5, the overall BER of 10^{-15} or better shall be confirmed with the StatEye calculation.

5.4.8 Noise and Crosstalk

In RapidIO Part 6: LP-Serial Physical Layer Specification Rev. 2.0 the input stressed eye includes sinusoidal, high probability, and Gaussian jitter as defined in the appropriate sections of this specification, along with any necessary additive crosstalk. Additive crosstalk is used to ensure that the receiver under test is adequately stressed if a low loss channel is used in the measurement. The additive input crosstalk signal is determined using the channel S-parameters, receiver reference model, and the StatEye script. It must be of an amplitude such that the resulting receiver equalizer output eye, given the channel, jitter, and crosstalk, is as close as feasible in amplitude when compared to the defined minimum amplitude used for channel compliance

6 RP3-01 Interface for Remote RF Unit

There exist base station configurations where remote RF units are used. This chapter specifies an extension of the Reference Point 3 protocol for remote RF unit use.

Section 6.1 defines architecture for RP3-01 interface while protocol stack for data transfer is defined in Section 6.2.

6.1 Architecture

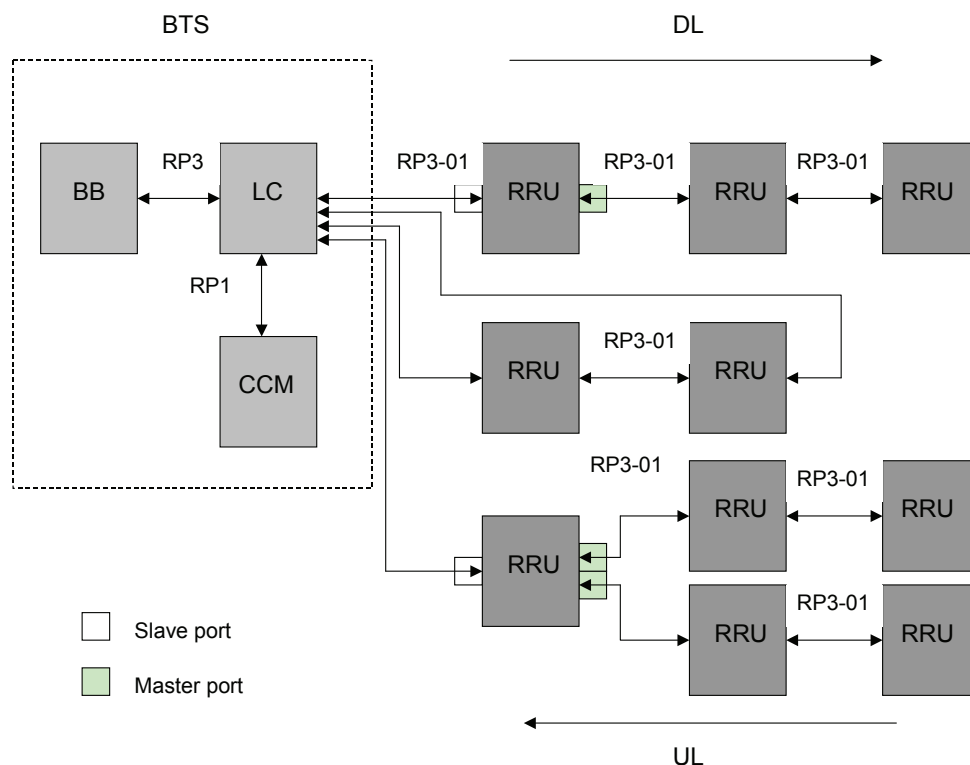


Figure 53: RP3-01 example architecture. Base station with remote RF units (RRUs). RRUs in chain, ring, and tree-and-branch topologies. Examples of RP3-01 master and slave ports of RRUs are also shown.

Figure 53 shows an example architecture of a BTS with remote RF units (RRUs). The figure provides a logical architecture and does not imply physical implementation of the BTS. The Local Converter (LC) may exist as a separate module or it may be integrated with other modules, such as the baseband module. For definitions of terms used in the figure and in the RP3-01 protocol description, refer to the Glossary.

The RP3-01 protocol shall support several RRU topologies, including point-to-point connection between a BTS and an RRU as well as chain, tree-and-branch and ring topologies.

Each RRU has one RP3-01 slave port and, optionally, one or more master ports. The slave port is connected toward the BTS either directly or through other RRU(s) while master port(s) connect to RRU(s) that are next in the chain. Slave and master ports are defined dynamically at BTS startup. The RP3-01 receiver first detecting transmission from the BTS, and its associated transmitter, are defined as the slave port while other ports are defined to be master ports.

Figure 54 provides an overview of RP3-01 protocol functionality at the LC and RRU for the case of a point-to-point topology. Section 6.2 defines in detail how RP1 and RP3 data is mapped into RP3-01 format. Basically, RP3-01 stands for an RP3 protocol where RP1 data is transferred in RP3 messages, between LCs and RRUs.

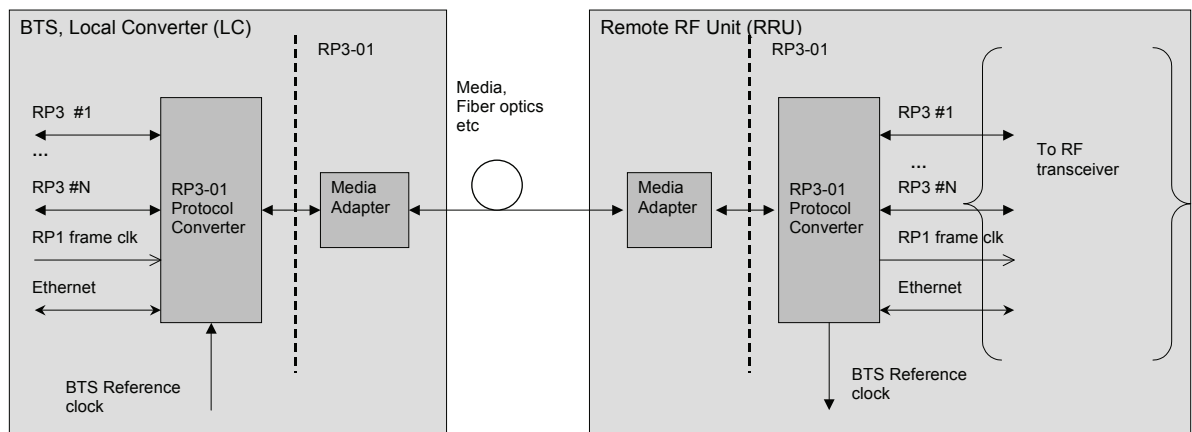


Figure 54: Logical model of OBSAI RP3-01 point-to-point interface.

6.2 Protocol Stack

6.2.1 Physical Layer

6.2.1.1 Media Adapter and Media

The media adapters and media defined in Appendix A shall be used.

6.2.1.2 Line Rates

RP3-01 and RP3 line rates are the same, i.e. 768Mbps, 1536Mbps, 3072Mbps, or 6144Mbps line rate shall be used.

6.2.2 RP3-01 - Transfer of RP1 Data Over RP3

RP3-01 is an extension of the RP3 protocol specifically designed for data transfer between a BTS and one or more remote RF units. RP3-01 is equivalent to the RP3 protocol except for the fact that different physical layer technologies, suitable for supporting data transmission over long distances, are applied. In order to minimize the number of connections to RRUs, RP1 data is mapped into RP3 messages. RP1 data includes Ethernet and frame clock bursts.

In the RP3-01 protocol, bandwidth is allocated to all data transfers by defining message transmission rules (see Section 4.4.3). Separate transmission rules shall be given as needed to RP1 Ethernet, RP1 frame clock burst, RTT measurement, Virtual HW reset, loop back, RP3 data, and RP3 control messages. Typically, RP3 data and control messages are already scheduled at baseband and RF modules in downlink and uplink directions, respectively, using message transmission rules. RTT measurement, HW reset, and loop back are examples of RP3-01 link O&M messages. RP1 and RP3-01 link O&M data can be transmitted in any RP3 message slot, as illustrated by Figure 55.

6.2.3 RP1 Frame Clock Bursts

The Control and Clock Module (CCM) shall provide frame timing information for each air interface standard, independently, via periodic synchronization bursts, as shown in Figure 56 [4]. A dedicated link is used to transfer the frame timing information to modules that are located in a BTS cabinet. For a RRU, frame timing information is transferred over the RP3-01 protocol by mapping the information within the RP1 frame clock bursts, into RP3 messages, and then regenerating

the RP1 frame clock burst at the RRU by applying the algorithm defined in this section.

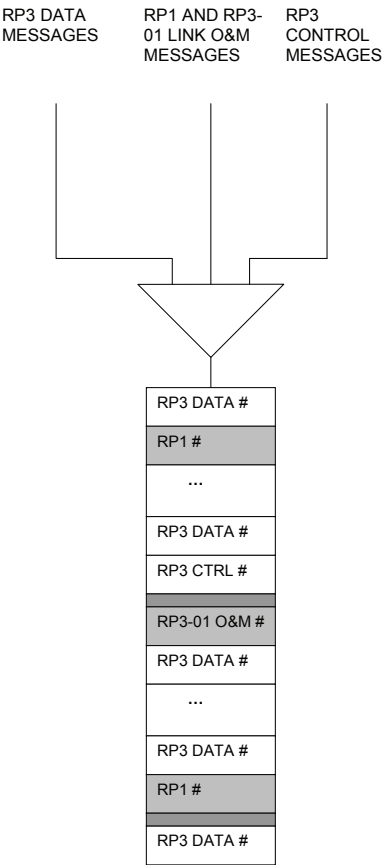


Figure 55: Examples of mapping RP1 and RP3-01 link O&M data into RP3 messages.

Start 1	Type 8	Type Specific Information 64	CRC 16	End 1
------------	-----------	---------------------------------	-----------	----------

Figure 56: RP1 frame clock synchronization burst from CCM.

The LC is responsible for multiplexing RP1 frame clock synchronization bursts into RP3 messages and it performs the following functionality.

- A counter, called *c1*, is reset and started at the beginning of the RP3-01 Master Frame and this counter measures time as a multiple of 1/(8*76.8)MHz. Thus 614.4MHz is the frequency of the reference clock.
- The RP1 Frame Clock Burst (FCB) from the CCM is received and processed.

- The RP1 frame clock burst from the CCM is discarded if the CRC check fails
- Only the first RP1 frame clock burst after the beginning of the RP3-01 Master Frame is accepted
- If a new RP1 synchronization burst is received before the previous is transmitted as FCB message, the new RP1 burst is discarded and an interrupt is generated to upper layers

The CCM is responsible for alternating the transmission order of the RP1 frame clock burst for the different air interface standards, so that timing for each standard will be transferred to RRUs.

- The arrival time of the end bit of the RP1 frame clock burst, from the beginning of the RP3-01 Master Frame, is measured by the counter *c1* and stored into an RP3-01 frame clock synchronization message defined by Figure 57 and Table 31. Specifically, the arrival time of the end bit stands for the falling edge of the end bit as sampled by the raising edge of the system clock. System and System Frame Number (SFN) information from RP1 frame clock synchronization burst are also stored into the message. After the message has been constructed, including the header, the CRC check for the whole message is computed and added to end.
- RP3-01 frame clock synchronization message shall be transmitted to RRUs in an RP3 message. The RP3-01 FCB message shall be transmitted in a time window of 9ms, starting from the end of the RP1 synchronization burst.

RRUs are responsible for all of the computations that are required for frame time transfer. The algorithm described below is a general one and supports all air interface standards.

- Counter *c2* is reset to zero and started at the beginning of each RP3-01 Master Frame, except if the *c2* counter is serving a FCB (RP3 Frame Clock synchronization Burst) message. The *c2* counter measures time as a multiple of $1/(8*76.8)$ MHz. Thus 614.4MHz is the frequency of the reference clock.
 - When FCB message is being served, *c2* increments without reset at the MF boundary
 - If FCB message is being served by *c2* counter when new FCB message is received from LC, then the new FCB message shall be discarded and an interrupt is generated to upper layer to indicate erroneous situation
- The RRU receives the RP3-01 frame clock synchronization message
- When RP3-01 FCB message type has been detected, the present *c2* counter value is captured, without disturbing *c2* counting. This captured *c2* value is called FCB_message_rx_time

- In case a new FCB message while an older message was being served by c2 counter, the count is not captured (erratic situation).
- The received message is discarded if the CRC check fails
- The RRU computes the buffering time B_{RRU} of the frame clock synchronization burst at the RRU, as follows
 - Find minimal positive integer value for parameter k such that

$$k * SFN_FRAME_TIME \geq RP3-01_MASTER_FRAME_TIME$$
 where SFN_FRAME_TIME equals to the length of the air interface frame and $RP3-01_MASTER_FRAME_TIME$ is always equal to 10ms. As an example, assume that SFN_FRAME_TIME is equal to 10 ms (WCDMA case). Then k equals to 1.
 - The captured c2 value is compared to c1 value received in the FCB message
 - If $FCB_message_rx_time > c1$, then B_{RRU} is then computed using formula:

$$B_{RRU} = k * SFN_FRAME_TIME + c1 * 1 / (8 * 76.8MHz) - RP1_FRAME_CLOCK_BURST_TIME$$
 If $FCB_message_rx_time < c1$, then B_{RRU} is then computed using formula:

$$B_{RRU} = k * SFN_FRAME_TIME - RP3-01_MASTER_FRAME_TIME + c1 * 1 / (8 * 76.8MHz) - RP1_FRAME_CLOCK_BURST_TIME$$
 In the above equation, $RP1_FRAME_CLOCK_BURST_TIME$ stands for the time required to transmit an RP1 frame clock burst in RP1 interface. This equals to $90 * 1 / 3.84MHz = 23.4375us$
- The RRU increments the System Frame Number (SFN) by k
- When the counter $c2$ reaches B_{RRU} , the recomputed RP1 frame clock burst shall be sent to functional blocks within RRU.
 - The format of the recomputed RP1 frame clock burst is equal to that of the original burst received from the CCM (see Figure 56) but the value of the System Frame Number has been incremented by k and the CRC check value has been recomputed.
- The functional blocks of the RRU shall receive and decode SFN in exactly the same manner as in the case of a single cabinet BTS.

The content of an RP3-01 frame clock synchronization message is defined in detail in Table 31.

The MSB of each message field is transmitted first (refer to Figure 12).

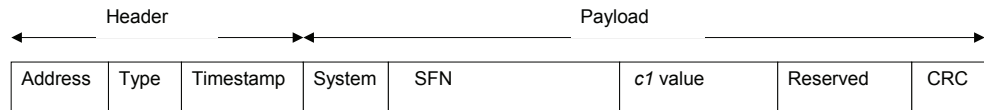


Figure 57: RP3-01 frame clock synchronization message.

Table 31: Content of RP3-01 frame clock synchronization message.

Field	Value
Address	Broadcast address (typically)
Type	Frame clock burst, 01001 in binary
Time stamp	000000
System, 8 bits	Refer to [4].
System Frame Number, 64 bits	Refer to [4].
c1 counter value, 26 bits	Positive integer number defining the arrival time of the RP1 frame clock burst from CCM with respect to RP3-01 Master Frame start as multiples of $1/(8*76.8)$ MHz.
Reserved, 14 bits	All zeros
CRC, 16 bits	Refer to Section 4.4.9.4 for the definition of the CRC.

Figure 58 illustrates the timing of RP1 frame clock burst transmissions. As can be seen from the figure, the RRU obtains its frame timing from a “future” System Frame Number $p+k$ not from the System Frame Number p that is used by all baseband and RF modules located in the BTS cabinet.

The propagation delay Δ_{LC-RRU} shown in Figure 58 may be large when an RRU is located far away from the BTS. The above algorithm does not take into account the impact of propagation delay in frame clock transfer. Propagation delay can be measured and removed from the frame clock timing. Section 6.2.6.2 specifies an algorithm for propagation delay measurement.

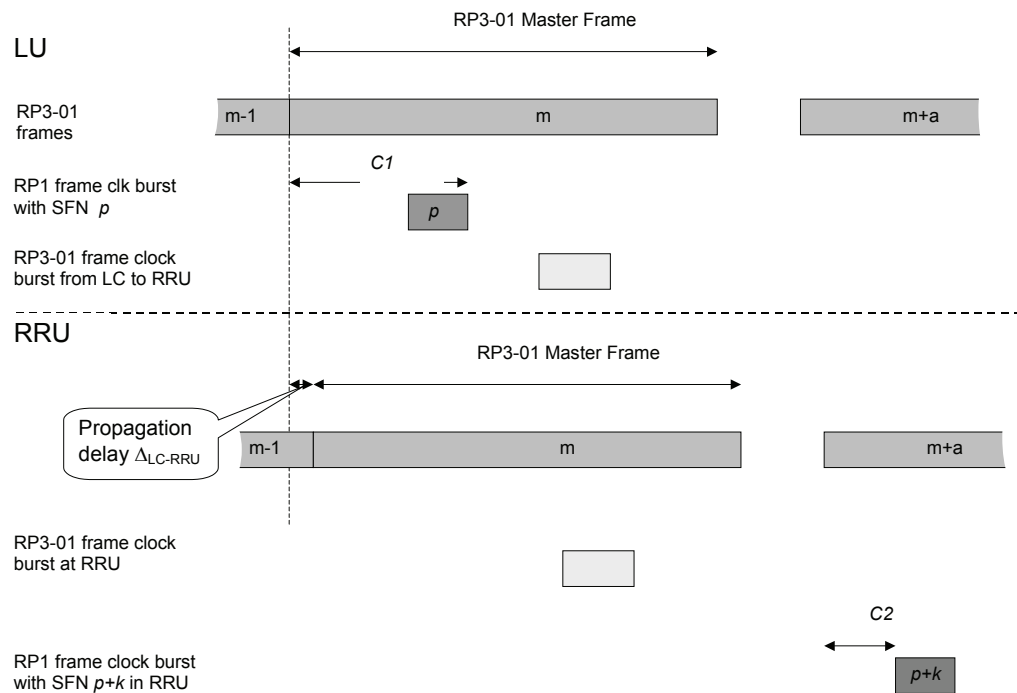


Figure 58: Timing principle in RP1 frame clock burst transfer.

6.2.4 Ethernet Transmission

Between any two RP3-01 nodes, whether in a BTS or an remote RF unit, a point-to-point Ethernet transfer is applied, as shown in Figure 59. Thus, only a single logical connection is allocated for Ethernet MAC messages between RP3-01 nodes. Where chain, ring, or tree-and-branch topologies are used for a number of remote RF units, the Ethernet switch in each RRU shall decide whether the MAC frame is consumed in that RRU or whether it will be forwarded to the next node.

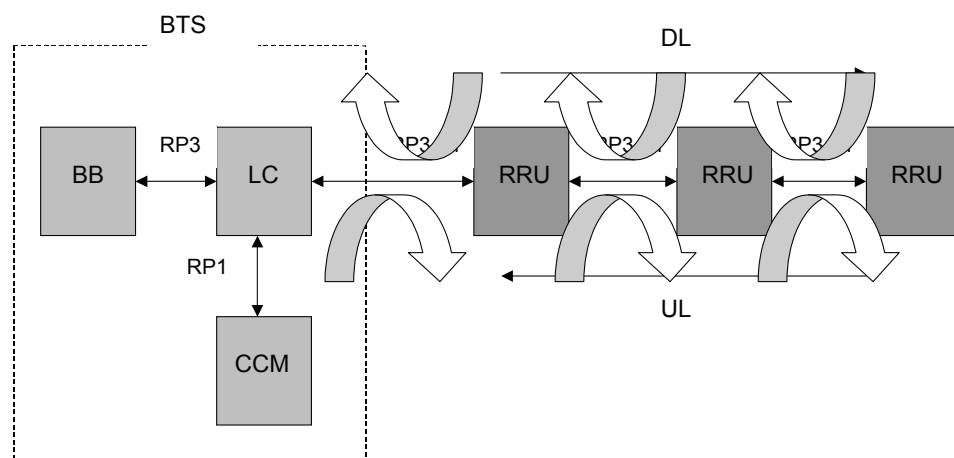


Figure 59: Ethernet frame transfer over RP3-01 network is done as a point-to-point transfer between a pair of nodes.

The Ethernet throughput over each RP3-01 link is specifically allocated by message transmission rules, as defined in Section 6.2.2.

Ethernet MAC frames are mapped into RP3 messages and transferred over the RP3-01 protocol. At the input, there exist MAC frames as specified by 802.3-2002 [10]. A MAC frame consists of preamble, start frame delimiter, the addresses of the frame's source and destination, a length or type field, MAC client data, a field that contains padding if required, a frame check sequence, and an extension field, if required. Each MAC frame is sliced into consecutive RP3 messages and the time stamp field defines the beginning and end of each MAC frame, as indicated in Table 32.

Table 32: Content of the time stamp field of RP3 messages in relation to Ethernet MAC frame data of the payload.

Time Stamp	Payload Content
100000	16 first bytes of an Ethernet MAC frame. The first byte of the MAC frame is located immediately after RP3 header.
000000	Next (second) RP3 message containing a part of the MAC frame.
...	
000000	Nth RP3 message containing a part of the MAC frame.
1xxxxx	The last RP3 message containing a slice from the MAC frame and xxxxx, a binary number, indicates the number of bytes from the start of RP3 payload containing MAC frame data (counting started from the byte after the header).

Table 33 defines the content of RP3 messages when used for Ethernet data transfer. The 'Address' field contains the address of the next RP3-01 node, The 'type' field indicates that Ethernet MAC data is contained in the payload, and all bits of the payload contain MAC data, excluding the last RP3 message, which may be partially filled.

The bytes (octets) of an Ethernet MAC frame are transmitted over an RP3-01 link in the order specified by the 802.3 specification. The MSB of each 802.3 byte as defined in 802.3 specification is assigned to the MSB of each RP3 message payload byte.

At the receiver, MAC frames are reconstructed from the payload of RP3-01 Ethernet messages by concatenation according to the content of the 'type' and 'time stamp' fields. By monitoring the 'type' field, the receiver shall identify RP3 messages containing Ethernet data. The

transmitter shall send only one MAC message at a time from which the 'time stamp' field can be used to identify the beginning and end of a MAC frame. A received MAC frame is discarded if an error is detected in 'time stamp' field processing. The RP3-01 protocol shall not check the validity of the MAC frame check or CRC fields.

Table 33: Content of RP3-01 Ethernet message.

Field	Content
Address	Target address of next RP3-01 node
Type	Ethernet, 01010 in binary
Time Stamp	See Table 32.
Payload	Slice from Ethernet MAC frame.

In Ethernet transfer over RP3-01, a flexible implementation methodology should be applied, in order to prepare for possible changes in the future.

In order to transfer Ethernet MAC frames over RP3-01, an Ethernet MAC Address must be established for each RRU. The RRU may use either a globally or locally unique MAC address. For a locally unique MAC address, OBSAI System Specification [2] describes the methodology to derive a locally unique MAC address based on module hardware position. However, the IDs described in that section are not normally available at the RRU. These IDs can be communicated from the BTS to the RRU through an initialization MAC frame.

Each RRU has an RP3-01 slave port and optionally one or more RP3-01 master ports. At startup, the RRU shall disable transmission on all RP3-01 master ports. An RRU's RP3-01 slave port at startup shall respond to only an RP3 node address of zero and shall not have an initial locally unique MAC address. It shall listen for an initialization MAC frame using the Ethernet transmission protocol over RP3-01 that contains a broadcast MAC address for the destination address. This initialization message shall contain all the IDs described in OBSAI System Specification. The RRU shall then use these IDs as described in that section to derive its permanent locally unique MAC address. If using a locally unique MAC address, the RRU shall use this permanent MAC address for any further Ethernet transmissions. The RRU shall be configured with a permanent RP3 node address using RP1 over RP3-01 at which time it shall stop using the zero RP3 node address. After MAC address and RP3 node address configuration, an RRU may be instructed over RP1 to enable its master port(s) one at a time to allow

initialization and network discovery of any other RRUs in the RP3-01 chain as shown in the example architectures of Figure 53.

6.2.5 Line Rate Auto-Negotiation

There exists a set of allowed RP3-01 line rates as defined in Section 6.2.1.2 and each LC or RRU can support one or several of these line rates. Before communication over an RP3-01 link can be initiated, a common line rate needs to be negotiated between adjacent RP3-01 nodes, with a 'node' being either an LC or an RRU. If the common line rate is known and pre-configured, a search for a common line rate is not required. Auto-negotiation of the line rate shall be applied when the used line rate is not defined beforehand.

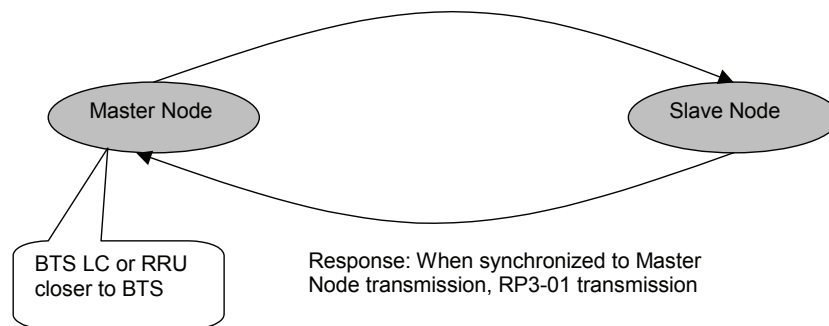


Figure 60: RP3-01 line rate auto-negotiation is done between a pair of nodes (LC and RRU or between adjacent RRUs).

Auto-negotiation of RP3-01 peer-to-peer links is considered in this section, as shown in Figure 60. For a chain, ring or tree-and-branch configuration of RRUs, the auto-negotiation algorithm is applied to each pair of RRUs at a time. The algorithm identifies a single line rate over each RP3-01 link, which is supported by both end nodes.

RP3-01 link synchronization is performed for a pair of RRUs. The Master node, which is the LC or RRU closest to the BTS, controls the auto-negotiation process.

The following assumptions are made:

- Master and slave nodes support all or a subset of allowed RP3-01 line rates.
- Allowed line rates include $i \times 768$ Mbps, where $i \in \{1, 2, 4, 8\}$, i.e. 768, 1536, 3072, and 6144 Mbps.

A set of parameters controls the operation of the algorithm and Application layer sets the value of these parameters. Table 34 lists the parameters of the auto-negotiation algorithm while Table 41 in Section 7.1.5 defines the parameters in detail. When setting parameter values for the RP3 receiver frame synchronization state machine (see Section

4.2.7), the worst case RP3 frame synchronization time at the receiver shall not exceed TxTime.

Table 34: Parameters of line rate auto-negotiation algorithm.

Parameter	Description
MaxSynchronizationTime	Time limit for the line rate auto-negotiation algorithm.
MaxRxTime	Reception time at a given line rate.
TxTime	Transmission time at a given line rate.

Auto-negotiation algorithm for the Master node:

1. Set *Synchronization* = FALSE and start time out counter *TimeOutCounter*.
2. Select lowest RP3-01 line rate that is supported by the Master node
3. Attempt RP3-01 synchronization with the Slave node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) at the latest after TxTime.
 - a. Start K28.5 transmission to the Slave Node and RP3 receiver synchronization state machine (refer to Section 4.2.7).
 - b. When Master's RP3 receiver state machine goes into state WAIT_FOR_K28.7_IDLES due to reception of K28.5 transmissions from the Slave node, start transmitting RP3 (RP3-01) frame format to the Slave node
 - c. When Master's RP3 receiver state machine goes into state FRAME_SYNC, set *Synchronization* = TRUE (RP3-01 synchronization between Master and Slave nodes has been completed).
4. If *Synchronization* = FALSE and *TimeOutCounter* is less than MaxSynchronizationTime, change to next higher line rate (or go back to the lowest line rate if the highest line rate is being used) that is supported and goto Step 3.
5. End of Algorithm

Auto-negotiation algorithm for the Slave node:

1. Set *RxSynchronization* = FALSE and start time out counter *TimeOutCounter*
2. Select lowest RP3-01 line rate that is supported by the Slave node

3. Attempt RP3-01 synchronization with the Master node by applying steps 3.a-3.c. Goto Step 4 (stop synchronization attempt) latest after *MaxRxTime*
 - a. Start RP3 receiver synchronization state machine (refer to Section 4.2.7 of RP3 Specification)
 - b. When RP3 receiver synchronization state machine goes into state *WAIT_FOR_K28.7_IDLES* due to reception of K28.5 transmissions from the Master node, start K28.5 transmission back to Master Node.
 - c. When RP3 receiver state machine goes into state *FRAME_SYNC*, start sending RP3 frame format to Master node and set *RxSynchronization* = TRUE.
4. If *RxSynchronization* = FALSE and *TimeOutCounter* is less than *MaxSynchronizationTime*, change to next higher line rate (or go back to the lowest line rate if the highest line rate is being used) that is supported and goto Step 3.
5. End of Algorithm

The Master node determines success or failure of the auto-negotiation procedure from the value of state parameter *Synchronization*. The Slave node is able to detect only the synchronization status of the downlink (from Master to Slave) RP3-01 link.

After RP3-01 link synchronization is achieved between the Master and the Slave, at some line rate common to both Master and Slave, RP1 Ethernet communication can be started over the interface and over other previously synchronized links. The Slave node can report the complete set of supported line rates using Ethernet messaging over the RP3-01 link.

6.2.6 RTT Measurement and Internal Delays of a RRU

RRUs may be located far away from the BTS. In order to be able to configure the BTS, the propagation delay between the BTS and each RRU needs to be measured. In this section, Round Trip Time (RTT) measurement between a LC of a BTS and an RRU or between adjacent pairs of RRUs is defined. Internal delays of an RRU are also defined. Based on the knowledge of the RTT between adjacent RP3-01 nodes and the internal delays within the RRUs, the CCM can configure the BTS appropriately.

6.2.6.1 Internal Delays of an RRU

RRUs can be classified based on their support for different RP3-01 network topologies. A Class #1 RRU can only support point-to-point connection toward a BTS since they contain only a single RP3-01

transceiver while Class #2 RRUs can support chain and ring topologies due to dual RP3-01 transceiver support. Class #3 RRUs, having as a minimum three RP3-01 transceivers, can generate tree-and-branch topologies, i.e. it has a single RP3-01 transceiver, the RP3-01 slave port, toward the BTS and at least two RP3-01 transceivers, master ports, toward different RRUs.

Internal delays of Class #1, #2, and #3 RRUs are defined in Figure 61, Figure 62, and Figure 63, respectively. In a Class #3 RRU, all signal through-path propagation delays, in a given direction (transmit or receive) for a given RRU, are required to occupy the same number of RP3 byte clock cycles.

Each RRU shall report its internal delay values over the RP1 Ethernet connection which is available over RP3-01.

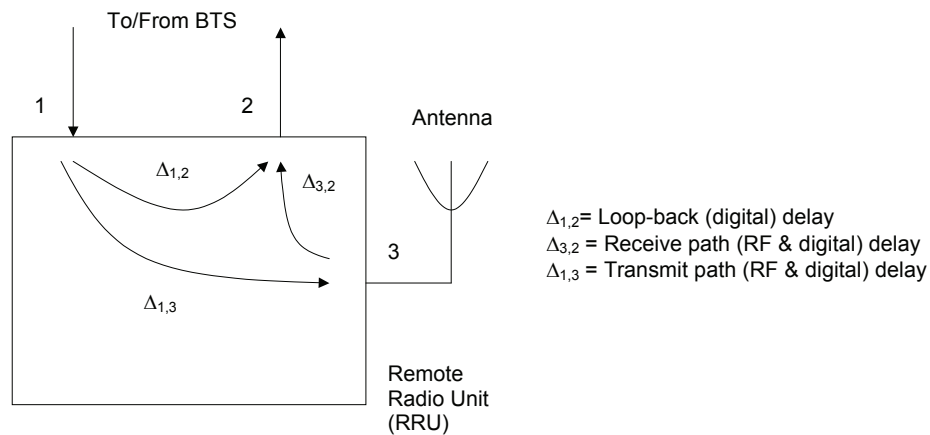


Figure 61: Internal delays of Class #1 RRU.

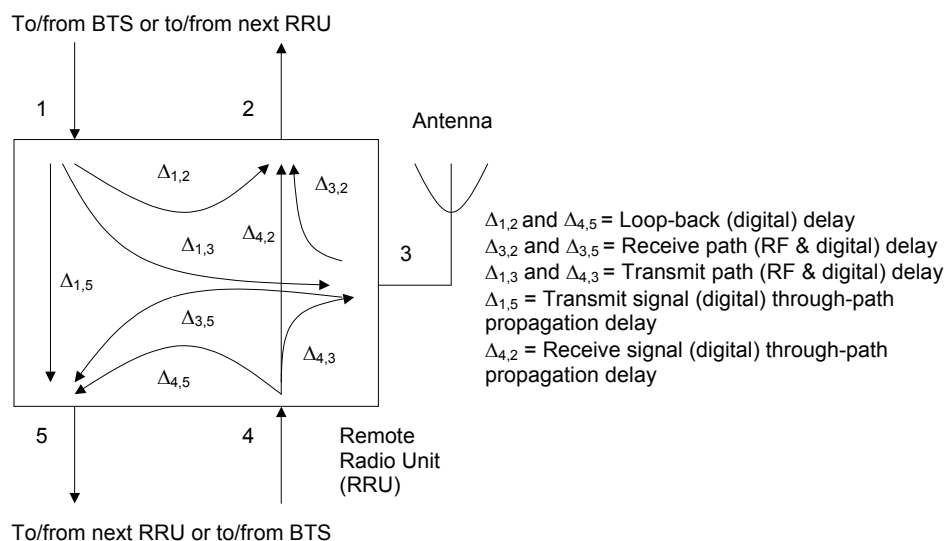


Figure 62: Internal delays of Class #2 RRU.

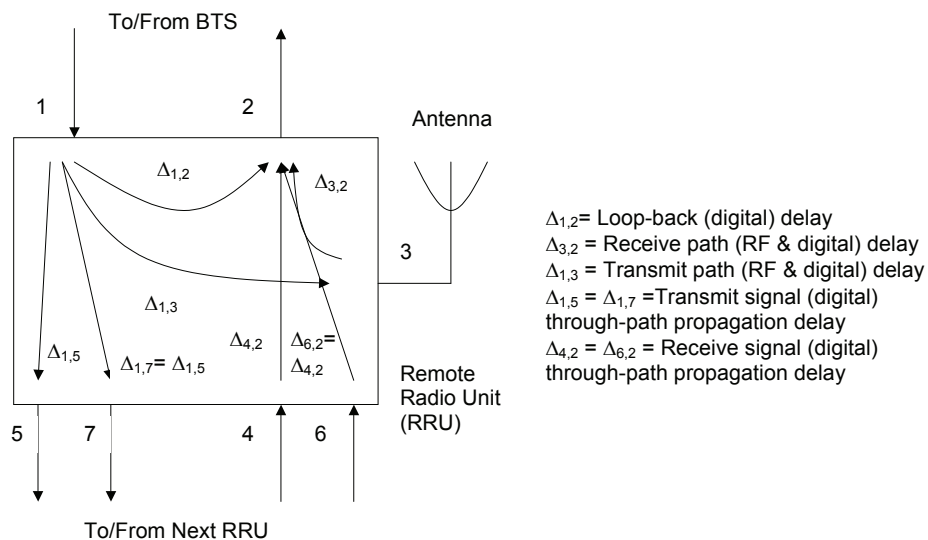


Figure 63: Internal delays of Class #3 RRU.

6.2.6.2 RTT Measurement Procedure

The RTT measurement procedure determines the two way propagation delay over the media, e.g. fiber optics, between two adjacent RP3-01 nodes. In the case of chain, ring, or tree-and-branch topologies for the RRU's, RTT measurements are performed in a sequence for each adjacent pair of RP3-01 nodes.

The RTT measurement procedure is defined as follows: A Master RP3-01 node shall send the RTT measurement message defined in Figure 64 to a Slave RP3-01 node and measure the time T from message transmission to message reception. The Master node is either LC or RRU # n while the Slave node is RU #1 or RU # $n+1$, respectively, and $n > 0$. The Slave node shall receive and send back the RTT measurement message to the Master node. Before transmission, the Slave node shall replace the address of the header by the return address of the payload and vice versa. Also buffering time $\Delta_{1,2}$ of the message at the Slave node will be stored into the message. Typically, the return address is equal to the RP3-01 node address of the Master node, so an 'address swap' procedure guarantees easy reception of the RTT message at the Master node.

All the time measurements are performed as a multiple of $1/(8 \times 76.8)$ MHz, i.e. 614.4MHz is the frequency of the reference clock.

Table 35 defines the content of different fields of the RTT message.

The MSB of each message field is transmitted first (refer to Figure 12).

Table 35: Content of an RTT Measurement message.

Field	Value
Address	Slave/Master RP3 node address (Slave address first, before address swap)
Type	01011 (RTT message)
Time stamp	000000
Return address, 13 first bits of the payload	Master/Slave RP3 node address (first Master address)
Reserved, 83 bits	All zeros
Buffering time $\Delta_{1,2}$, 16 bits	Positive integer number, buffering time will be measured using a reference clock at frequency (8 * 76.8)MHz.
CRC check, 16 bits	CRC check sum computed over the header and payload. Refer to Section 4.4.9.4 for the definition of the CRC.

The RTT between the Master and Slave nodes over fibre optics or other media is equal to $\Delta_{RTT} = T - \Delta_{1,2}$. The delay over the fibre is considered to be the same in downlink and uplink directions, i.e. one way delay over the fibre is equal to $\Delta_{RTT} / 2$.

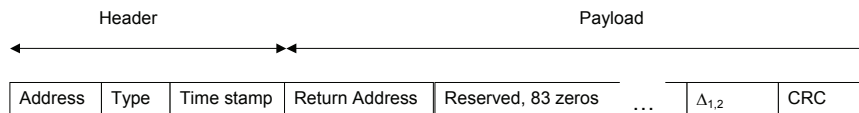


Figure 64: RTT Measurement message.

6.2.7 Virtual HW Reset

A remote reset may need to be performed to a RRU in a case where the control processor of the RRU is halted. RRU may optionally support virtual HW reset functionality where the unit undergoes a boot sequence after receiving a specific virtual HW reset message. When receiving such a message, the following procedure shall be followed.

- CRC check is first performed. If the CRC check fails, the virtual HW message is rejected.
- The type field is checked. If it equals to 01101 (Virtual HW Reset), HW reset is performed for the RRU control processor.

Note that the virtual HW reset message may be received in either the data or control message slot. The virtual HW reset message is illustrated in Table 36 and Figure 65 below.

The MSB of each message field is transmitted first (refer to Figure 12).

Table 36: Content of virtual HW reset message.

Field	Value
Address	Address of the node that requires reset
Type	01101 (Virtual HW Reset)
Timestamp	000000
Payload data, 14 bytes	All zeros
CRC check, 16 bits	CRC check sum computed over the header and payload (see Section 4.4.9.4).

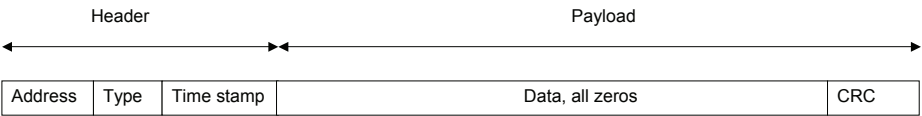


Figure 65: Virtual HW reset message.

7 OAM&P

7.1 OAM&P Parameters

Operation of RP3 interface protocol is controlled through parameters. In this section, all parameters of the protocol are defined. Also error cases are considered.

7.1.1 External Parameters of Data Link Layer

In Table 37 external parameters of the Data link layer are listed. Application layer has access to all Data link layer parameters and input parameters are set by the Application layer.

Table 37: Input and output parameters of Data link layer.

Parameter	Input/ Output	Register width	Description
M_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of message slots in a Message Group (refer to Section 4.2.2 for details). $0 < M_MG < 65536$.
N_MG	Input	16 bits, positive number (no sign bit)	Specifies the number of Message Groups in a Master Frame (refer to Section 4.2.2 for details). $0 < N_MG < 65536$.
K_MG	Input	5 bits, positive number (no sign bit)	Specifies the number of IDLE bytes at the end of Message Group (refer to Section 4.2.2 for details). $0 < K_MG < 20$.
DATA_MESSAGE_SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in downlink direction. Takes values from 0 up to $i*(M_MG-1)*N_MG-1 < 2^{32}$ (refer to Section 4.2.2 for definition of M_MG and N_MG).

Parameter	Input/ Output	Register width	Description
DATA_MESSAGE_SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts data message slots over Master Frame duration in uplink direction. Takes values from 0 up to $i*(M_MG-1)*N_MG-1 < 2^{32}$.
CONTROL_MESSAGE_SLOT_COUNTER_DL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in downlink direction. Takes values from 0 up to $i*N_MG-1$.
CONTROL_MESSAGE_SLOT_COUNTER_UL	Output	32 bits, positive number (no sign bit)	Counts control message slots over Master Frame duration in uplink direction. Takes values from 0 up to $i*N_MG-1$.
BLOCK_SIZE	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Defines the number of bytes within a block. (Reset value is 400)
SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid blocks of bytes which result in state WAIT_FOR_K28.7_IDLE. (Reset value is 255)
UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid blocks of bytes which result in state UNSYNC. (Reset value is 255)
FRAME_SYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive valid Message Groups which result in state FRAME_SYNC. (Reset value is 1920)
FRAME_UNSYNC_T	Input	16 bits, positive number (zero not allowed)	Common value for a node. Synchronisation. Threshold value for consecutive invalid Message Groups which result in state WAIT_FOR_K28.7_IDLE. (Reset value is 128)
TRANSMITTER_EN	Input	1 bit	For each transmitter separately. Value '1' enables transmission to the bus (if other conditions are also fulfilled) while value '0' disables transmission (see Section 4.2.8). (Reset value is '0').
LOS_ENABLE	Input	1 bit	For each transceiver separately. This parameter enables (value '1') or disables (value '0') the impact of signal LOS to transmitter state machine. See Section 4.2.8. (Reset value is '1')

Parameter	Input/ Output	Register width	Description
DELTA (Δ)	Input	23 bits (16 bits allowed for $\leq 3072\text{Mbps}$), two's complement code	In a general case, a common Δ value exists for all uplink bus transmitters of a node. Another common value exists typically for all downlink transmitters of a node. Link-specific Δ values are also allowed. Value of Δ is given in byte-clock ticks. When two byte accuracy is used for Δ , LSB of the register is ignored.
PI (Π)	Input	23 bits (16 bits allowed for $\leq 3072\text{Mbps}$), two's complement code	In a general case, a common value exists for all uplink receivers of a bus node. A common value is typically used for all downlink receivers of a node. Receiver-specific Π values are also allowed. Value of Π is given in byte-clock ticks. When two byte accuracy is used for Π , LSB of the register is ignored.
MAX_OFFSET	Input	1 bit	Common value for a node. Defines the width of the allowed window for Master Frame boundary (see Section 4.2.6). MAX_OFFSET equals to 52.08 ns (the default value) for bit value '0' while MAX_OFFSET is equal to 104.17ns for '1'
SYNCHRONISATION_STATUS	Output	4 bits	For each transceiver separately. Indicates the status of the transceiver (see Section 4.2.8). State encodings are the following. UNSYNC: 1000 WAIT_FOR_K28.7_IDLES: 0100 WAIT_FOR_FRAME_SYNC_T: 0010 FRAME_SYNC: 0001
SYNC_STATUS_CHANGE	Output	Interrupt	Application layer is interrupted always when a receiver state machine changes state.
Nx7	Input	5 bits	For each transmitter separately (applied only in case of 6144Mbps line rate). Specifies scrambler seed value (refer to Table 3). $0 \leq Nx7 \leq 17$.

1

2 7.1.2 Error Cases at Data Link Layer

3 In Table 38, possible error cases at Data Link layer are defined.

4 In case of RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE,
5 error recovery is left to Application layer.

7.1.3 External Parameters of Transport Layer

In this section, parameters of the Transport layer are listed, see Table 39. Application layer has access to all parameters; input parameters are set by Application layer.

Table 38: Error cases at Data link layer.

Error	Register width	Description
RX_MASTER_FRAME_BOUNDARY_OUT_OF_RANGE	1 bit	For each receiver port (transceiver) separately. This error is indicated when received Master Frame is detected outside the allowed MAX_OFFSET ns wide window (see Section 4.2.6). Value '0' indicates offset within the allowed range while '1' indicates out-of-range situation.

Table 39: Input and output parameters of Transport layer. All the parameters are defined for the whole node.

Parameter	Input/Output	Register width	Description
RP3_ADDRESS	Input	13 bits	At least one address shall be supported per device based on which RP3 message reception is performed. The 8 bit wide node address shall be programmable while the 5 bit wide sub-node address may be hard-wired to the device. Note that in message transmission, Application layer may use several addresses when constructing and transmitting messages.
DL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that DL routing table is used to route messages that are received from the transceiver.
UL_TRANSCEIVERS	Input	1 bit	For each transceiver separately. Value '1' indicates that UL routing table is used to route messages that are received from the transceiver.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESSES_DL	Input	4 bits	Specifies number of bits in a transformed address in downlink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.
NUMBER_OF_BITS_IN_TRANSFORMED_ADDRESSES_UL	Input	4 bits	Specifies number of bits in a transformed address in uplink direction (see Section 4.3.3). Valid values are 1-13. Reset value is 8.

Parameter	Input/ Output	Register width	Description
LSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_DL	Input	32 bits	Downlink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.
LSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_UL	Input	32 bits	Uplink direction. Contains eight groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which stands for bit Index 0 (LSB) in the transformed address. Four MSBs contain the Index of the input address bit that is copied to bit location 7 in transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_DL	Input	20 bits	Downlink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
MSBs_MAPPING_OF_TRANSFORMED_ADDRESSES_UL	Input	20 bits	Uplink direction. Contains five groups of four bits. Four LSBs contain the bit Index of the 13 bit input address which is copied to bit Index 8 in the transformed address.
DL_ROUTING_TABLE	Input	$A \cdot T$ bits	A table with A rows and T bits per row. A stands for $2^{DL_TRANSFORMED_ADDRESS_RANGE}$, while T denotes total number of transceivers both at Application and Physical layers. The values of parameters A and T can be fixed and they take values in the range $0 < A \leq 2^{13}$ and $0 < T \leq 48$.
UL_ROUTING_TABLE	Input	$A' \cdot T$ bits	A table with A' rows and T bits per row. A' stands for $2^{UL_TRANSFORMED_ADDRESS_RANGE}$, while T denotes total number of transceivers both at Application and Physical layers. The values of parameters A' and T can be fixed and they take values in the range $0 < A' \leq 2^{13}$ and $0 < T \leq 48$.

Parameter	Input/ Output	Register width	Description
MULTIPLEXING_TABLE	Input	32 bits (4*8 bits)	For each multiplexer and demultiplexer separately. Vector containing four elements $E_{i_{out}} = (D, k, j_k)$. The first i elements of the vector are used for output (multiplexer)/input (demultiplexer) line rate $i \times 768$ Mbps. D exists in the MSB and values '0' and '1' are allowed, k field is three bits wide and may take values in the range of 0-7 (0x0-0x7 in hex), while j_k is located in the four least significant bits and it may take values in the range 0-15 (0x0-0xF in hex). See Section 4.3.4 for the definition of $E_{i_{out}} = (D, k, j_k)$.
SUMMING_ALLOWED_FOR_TYPE	Input	32 bits	Value '1' in bit Index N indicates that messages of type N may be summed together. The least significant (rightmost) bit has Index 0 while MSB has Index 31. Refer to Table 12 for message type definitions and Section 4.3.5 for an example of SUMMING_ALLOWED_FOR_TYPE parameter.

1

2 7.1.4 Error Cases at Transport Layer

3 In Table 40: Possible error cases at Transport layer. the possible error
4 cases at the Transport layer are defined. Refer to RP3 compatible chip
5 (ASIC) functional specifications for detailed descriptions on these error
6 indicators.

1

Table 40: Possible error cases at Transport layer.

Error	Register width	Description
DL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. There exists no output port corresponding to the address of the received message (all-zero bit vector exists for the address in the routing table (see Table 5)).
UL_MESSAGE_REJECTED	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specification. Operation is the same than in case of DL_MESSAGE_REJECTED above. UL_MESSAGE_REJECTED applies for UL direction.
MESSAGE_COLLISION	64 bits	Node (chip)-specific diagnostic information. Specified in detail in chip functional specifications. Refer to Section 4.3.5 for a definition of message collision.

2

3 7.1.5 Other External Parameters

4 In this section, parameters that may be applied at any protocol layer are
5 listed, see Table 41: Other input and output parameters of bus node.
6 Thus, the functionality corresponding to the parameters can be
7 implemented at any protocol layer.

8 Physical layer shall be able to detect and report line code violations
9 (see Section 4.1.2).

10 For each receiver port (link) separately, Loss Of Signal (LOS) defect
11 reporting shall be supported. If N_LCV or more line code violations
12 occur during period T_LCV, a LOS defect shall be reported. The LOS
13 defect shall be removed when no LCVs occur in period T_LCV. LOS
14 defect functionality can be implemented at any layer of the protocol
15 stack.

Table 41: Other input and output parameters of bus node.

Parameter	Input/ Output	Register width	Description
N_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Threshold value for Line Code Violation (LCV) defect reporting (see algorithm below). Reset value is 1.
T_LCV	Input	32 bits, positive number	Value applies for all receiver ports of a bus node. Parameter defining period for LCV defect monitoring. T_LCV specifies the period in number of received 8b10b line codes. Reset value is $N_MG \cdot (M_MG \cdot 19 + K_MG) ..$
LOS_DEFECT	Output	1 bit	For each receiver port separately. Value '1' indicates Loss Of Signal (LOS) while value '0' denotes normal operation (reset value)
MESSAGE_TX_RULE	Input	33 bits	There may exist several message transmission rules per a bus node. The MSB defines the message slot counter that is used in message transmission. '0' stands for data message slot counter while '1' refers to control slot counter. The following 16 bits contain the index I and the 16 least significant bits contain the modulo M (refer to Section 4.4.3 for the definition of I and M).
MAX_SYNCHRONIZATION_TIME	Input	32 bits, positive number	Common value for a node. Time limit for the line rate auto-negotiation algorithm (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 153600000 (5 seconds).
MAX_RX_TIME	Input	32 bits, positive number	Common value for a node. Reception time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 19660800 (0.64 seconds).
TX_TIME	Input	32 bits, positive number	Common value for a node. Transmission time at a given line rate (see Section 6.2.5). Value given as multiples of BTS reference clock ticks (1/30.72 MHz). Reset value is 6144000 (200 ms).

Appendix A: Media Adapters and Media Options

Media adapters and media options for OBSAI RP3-01 interface are listed in this section. Phase distortion and latency are examples of important parameters that are associated with RP3-01 interface. These parameters are to be considered at base station system level and they are therefore out of the scope of RP3 specification.

A1: Fiber Optics

Table 42 lists the media options that shall be used.

Table 42: Options for optical cabling.

Type	Related Standard
50 μm Multimode	IEC 60793-2-10:2002, Type A1a [7]
62.5 μm Multimode	IEC 60793-2-10:2002, Type A1b [7]
Singlemode	IEC 60793-2-50:2002, Type B1 [8]

Table 43 proposes optical transceiver candidates for each line rate. OBSAI recommends to apply the Fibre channel interface requirements to RP3-01.

Table 43: Optical interface recommendations for different RP3-01 line rates. This table is for information only.

Line Rate	50 μm Multimode Fiber	62.5 μm Multimode Fiber	Singlemode Fiber
768 Mbps	100-M5-SN-I in [9]	100-M6-SN-I in [9]	100-SM-LC-L in [9]
1536 Mbps	200-M5-SN-I in [9]	200-M6-SN-I in [9]	200-SM-LC-L in [9]
3072 Mbps	400-M5-SN-I in [9]	400-M6-SN-I in [9]	400-SM-LC-L in [9]
6144 Mbps	800-M5(E)-SN-I in [12]	800-M6(E)-SN-I in [12]	800-SM-LC-L in [12]

OBSAI mandates the use of SFP (Small Form-factor Pluggable) transceivers for line rates up to 3072 Mbps and SFP+ [13] for 6144 Mbps line rate. Connector type is not recommended but the ORL (Optical Return Loss) of the used connector should fulfil PC (Physical Contact) requirement ORL<-30 dB for singlemode and TIA/EIA 568 requirement (ORL<-20 dB) for multimode applications. Super PC (ORL<-40 dB) is recommended for complex installations especially at 1550 nm wavelength.

A2: Other Media

Other technologies like wireless transmission or copper cable can be used as transport media. The requirements for the transmission parameters as specified in the OBSAI specifications shall be met.

Appendix B: Multiplexing Examples (Informative)

Figure 66 provides an example of a Transport layer configuration. The message router and summing unit are defined here to operate at the lowest RP3 line rate used in the system. Demultiplexers are used to split high data rate RP3 links into several low rate links which may then be multiplexed back to high rate links after summing. RP3 line rates are configured or identified at BTS startup so multiplexer and demultiplexer blocks as well as router and summing blocks can be configured accordingly. For detailed information on message multiplexer, demultiplexer, and router operations, refer to Section 4.3.

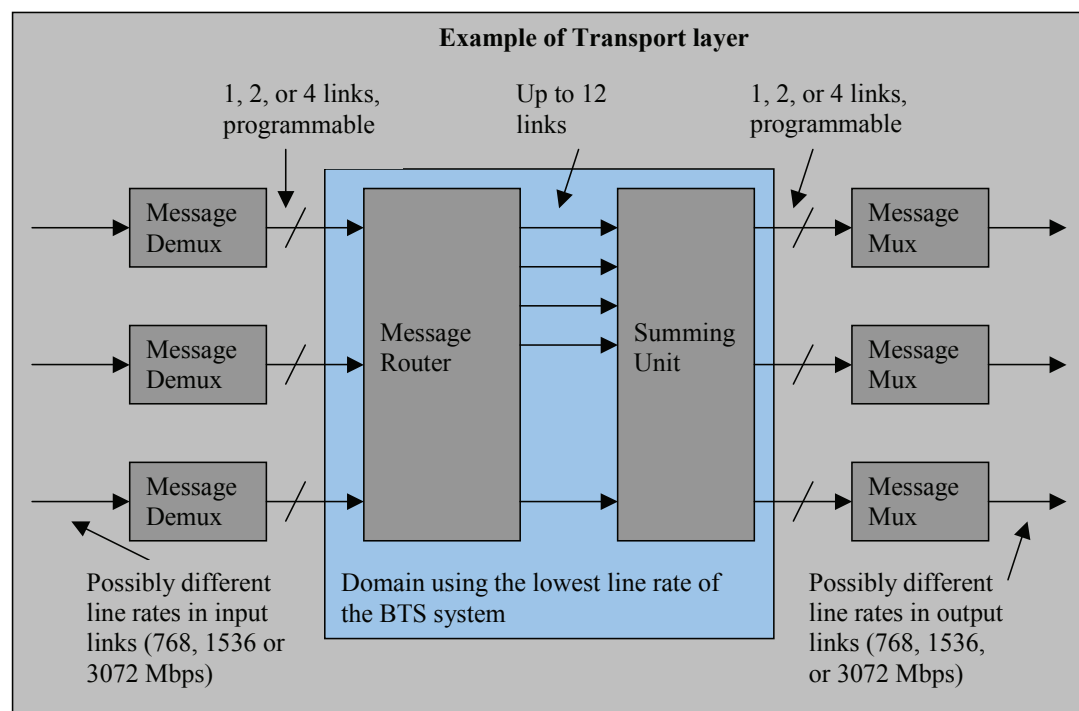
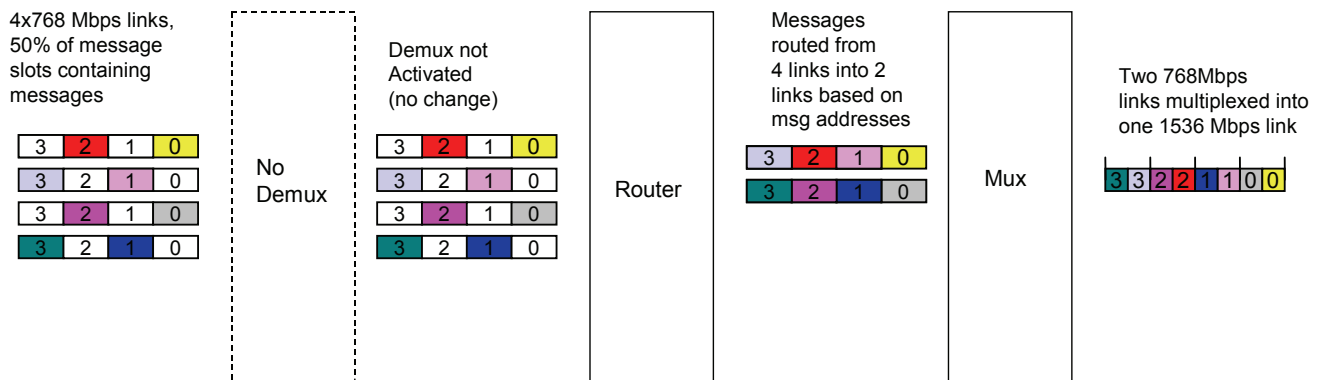


Figure 66: Example block diagram of Transport layer.

Figure 67 illustrates message multiplexing from four 50% full RP3 links into one 1536 Mbps. The concept presented in Figure 66 has been applied for this and other examples presented in this section.

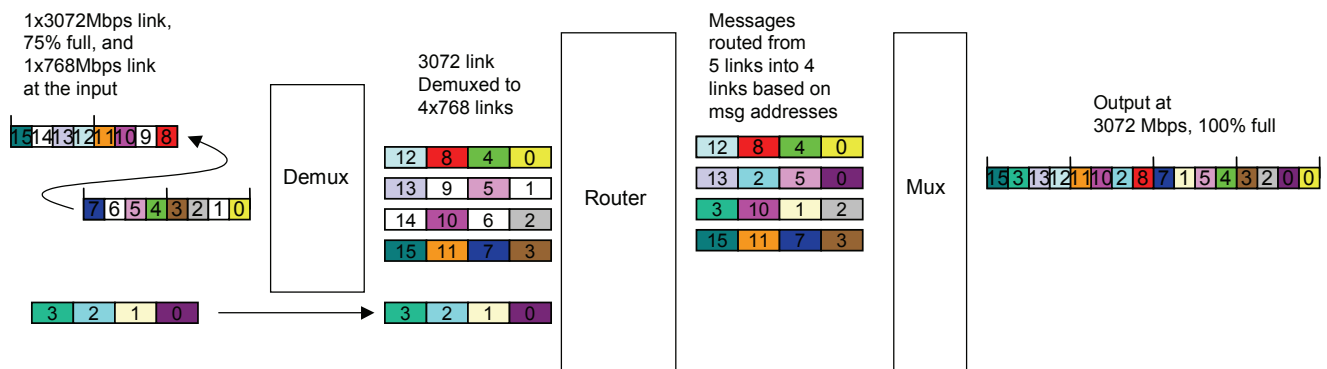


Empty messages shown in white,
each antenna-carrier with an unique color
(WCDMA case assumed)

Figure 67: An example of message multiplexing from four 768 Mbps links into one 1536 Mbps link.

Figure 68 illustrates message interleaving from a single 768 Mbps RP3 link into a 3072 Mbps link. Such a case may be valid in the uplink direction when data from an RRU is interleaved to RP3-01 in a chain topology.

Illustrates e.g. data interleaving at an RRU to a chained fiber in UL direction



Empty messages shown in white,
each antenna-carrier with an unique color
(WCDMA case assumed)

Figure 68: An example of message interleaving from one 768 Mbps link into one 3072 Mbps link.

Figure 69 and Figure 70 illustrate RP3 multiplexing in a possible BTS configuration where uplink data from several low capacity RRUs is forwarded to base band for processing. The configuration shown reduces the number of RP3 links at the base band modules.

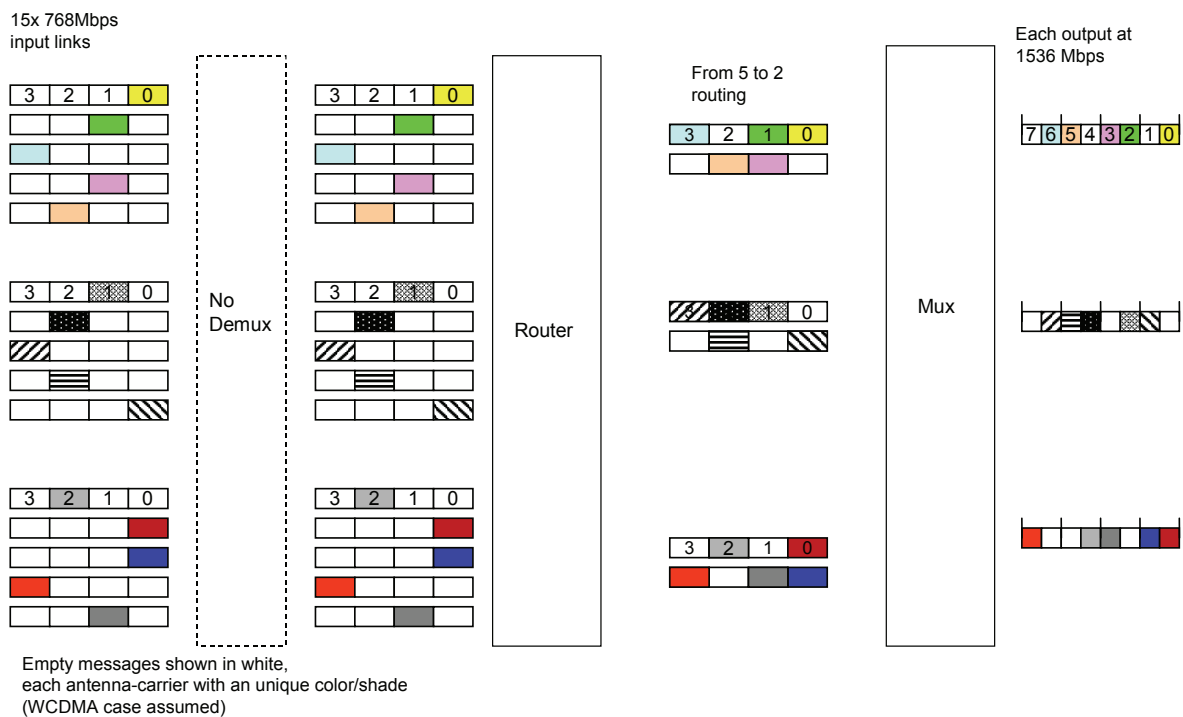


Figure 69: An example of message interleaving from fifteen 768 Mbps links into three 1536 Mbps link.

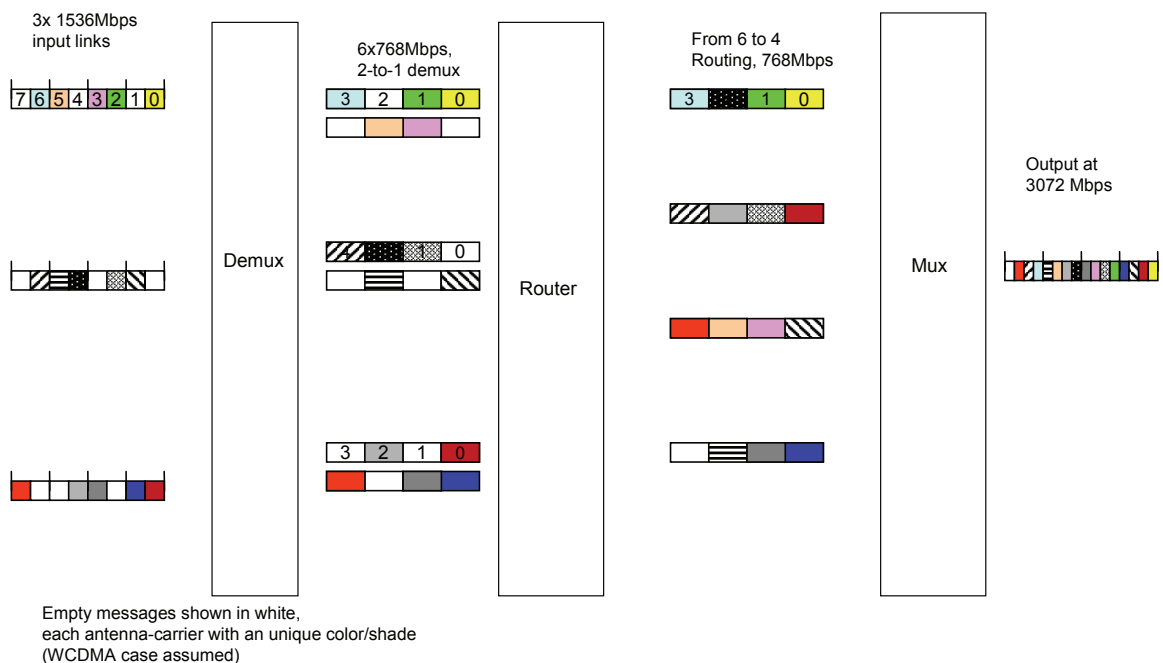


Figure 70: An example of message interleaving from three partly full 1536 Mbps links into one 3072 Mbps link.

Appendix C: RP3 Bus Configuration Algorithm (Informative)

An example of the RP3 bus configuration is provided in this section for the base station configuration illustrated in Figure 71. We use a two sector WCDMA base station with a single TX antenna and two RX antennas per sector. There are two carriers per each antenna so a 2+2 configuration is illustrated. As can be seen from the figure, a base-station architecture with combiner and distributor is used but the configuration principles apply also to the mesh architecture. In this example, we split the 13 bit RP3 address into an 8 bit node address (MSBs) and a 5 bit sub-node address, where the node address identifies a module and the sub-node address specifies the antenna-carrier. RP3 links with a 768Mbps baud rate are assumed.

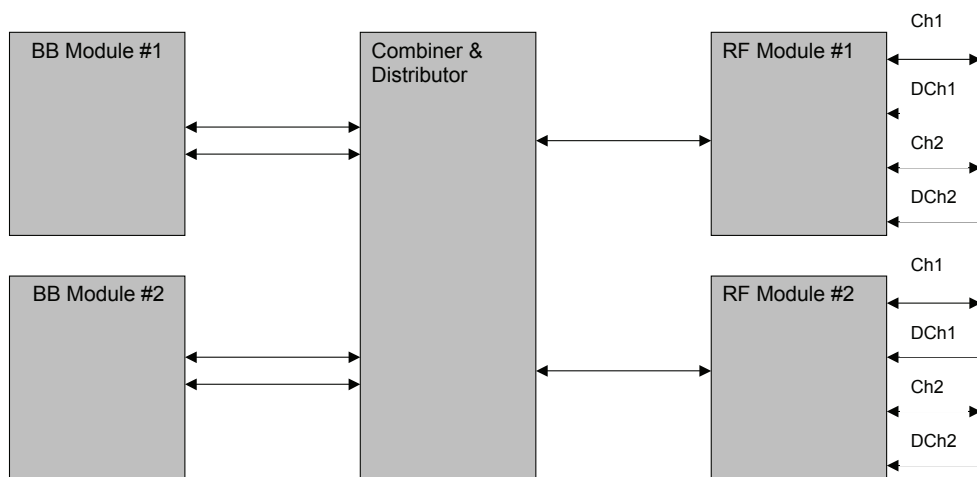


Figure 71: An example base station configuration.

Figure 72 illustrates data flows between the RF and BB modules. Each antenna-carrier is drawn separately to the figure and mapping of the antenna carriers to RP3 links is provided. Also node and sub-node addresses for different modules and antenna-carriers are provided. In this example, node addresses 1 and 2 have been allocated to BB

modules while node addresses 16 and 32 (in decimal numbers) are applied to RF modules. Antennas-carriers in each RF module are numbered from 1 to 4.

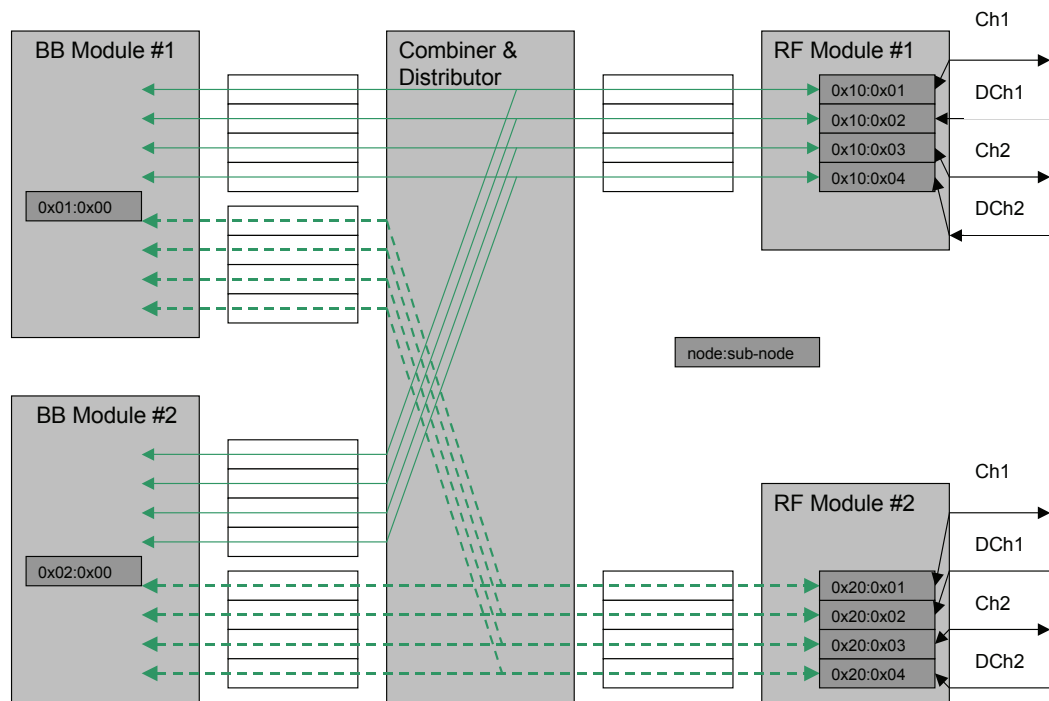


Figure 72: Data flows between BB and RF modules. Addresses of modules and antenna-carriers (or up/down converters at RF) are also shown.

Parameters for the message routing, multiplexing, and demultiplexing blocks of the combiner and distributor must be provided at base station start up. In this example, multiplexing and demultiplexing blocks are not used. Message routing tables are applied to the message routing between BB and RF modules. The routing tables define the output port or ports that correspond to each address. In the downlink direction, a point-to-point message transfer is typically applied so there exists a single output port index for each address in the downlink routing table. In uplink direction, the same message may be multicast to several BB modules for processing and because of this several output ports exist corresponding to an address in the uplink routing table.

In Figure 73, the port indices of the combiner distributor are shown, while downlink and uplink routing tables are provided in Table 44 and Table 45, respectively. In this example, we assume that the combiner distributor performs message routing based on the node address only.

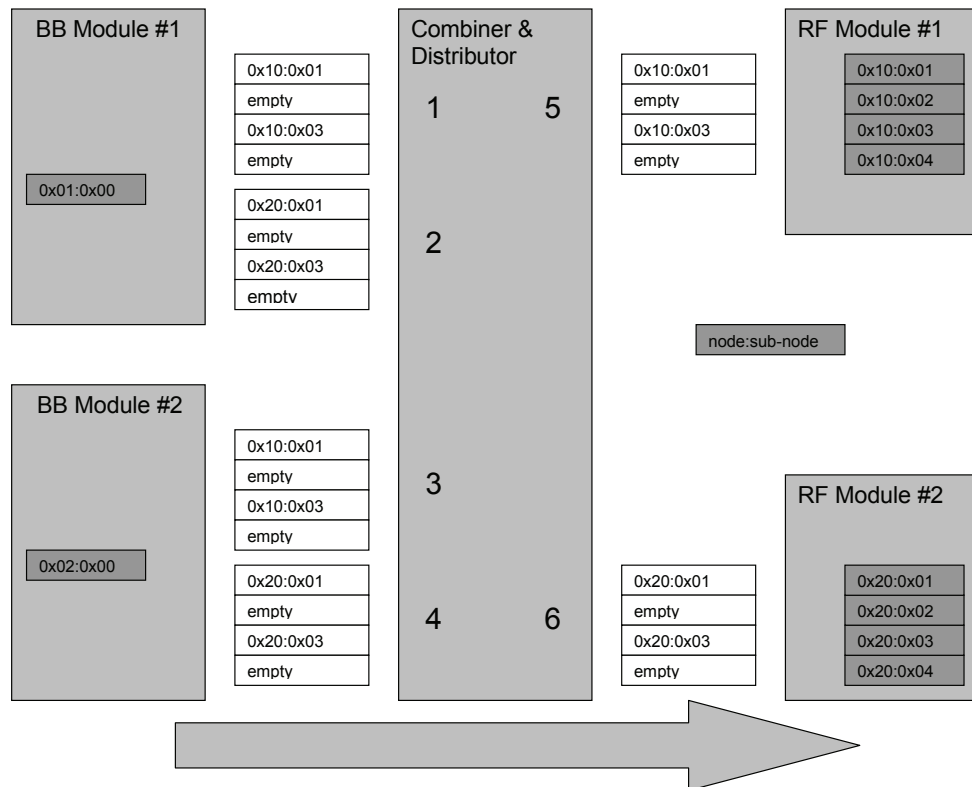


Figure 73: Index assignment to the ports of combiner distributor. Mapping of downlink messages to RP3 message slots is also shown.

Table 44: Downlink routing table.

Address Field (Target Address)	Output Port
0x10	5
0x20	6

Table 45: Uplink routing table.

Address Field (Source Address)	Output Ports
0x10	1, 3
0x20	2, 4

In addition to address assignment and the definition of routing tables, message transmission rules must also be defined in the BB and RF modules that form the end nodes of the bus. Table 46, Table 47, and Table 48 define the message transmission rules applied by the BB

modules, RF module #1, and RF module #2, respectively. Figure 73 shows also how messages are mapped into the message slots of the RP3 links in the downlink direction, while Figure 74 illustrates the uplink case.

Table 46: Message transmission rules for BB modules #1 and #2.

Target	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x03	Link 1, 2 / 4
0x20: 0x01	Link 2, 0 / 4
0x20: 0x03	Link 2, 2 / 4

Table 47: Message transmission rules for RF module #1.

Source	Link, Index/ modulo
0x10: 0x01	Link 1, 0 / 4
0x10: 0x02	Link 1, 1 / 4
0x10: 0x03	Link 1, 2 / 4
0x10: 0x04	Link 1, 3 / 4

Table 48: Message transmission rules for RF module #2.

Source	Link, Index/ modulo
0x20: 0x01	Link 1, 0 / 4
0x20: 0x02	Link 1, 1 / 4
0x20: 0x03	Link 1, 2 / 4
0x20: 0x04	Link 1, 3 / 4

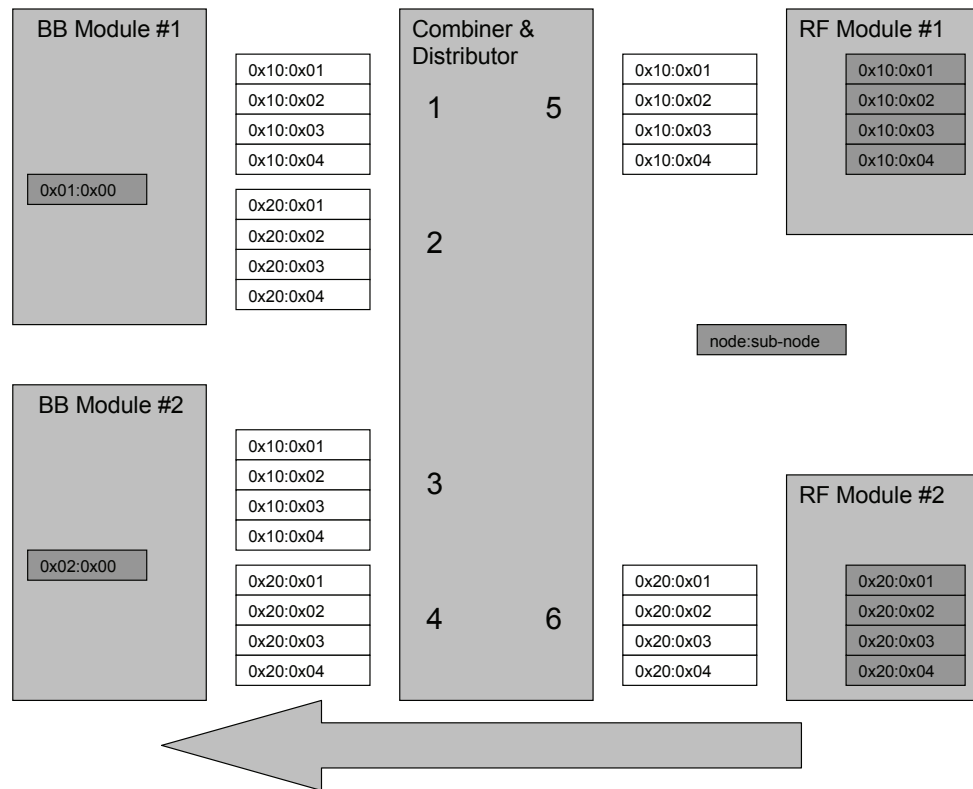


Figure 74: Mapping of uplink messages to RP3 message slots.

Appendix D: Parameters for 802.16 Message Transmission

The parameters required for 802.16 data message transmission are provided in Table 49 for the currently supported 802.16 profiles, i.e.

Table 49: Parameters for supported 802.16 profiles in case of 768 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	10	1	0x5	3	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
2.5	144/125	2.88	5	1	0x2	3	0x0	0
3	86/75	3.44	4	1	0x2AA95552AAA	43	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	144/125	5.76	2	1	0x5	3	0x0	0
5.5	316/275	6.32	2	1	0x2A54A952A54A952A54AA	79	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
10	144/125	11.52	1	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	10	1	0x7FFFFFFFD	35	0x0	0
1.75	8/7	2	7	1	0x1B6DB6D	25	0x0	0
3.5	8/7	4	3	1	0x1F7DF7D	25	0x0	0
5	28/25	5.6	2	1	0x6EEEEEEED	35	0x0	0
5.5	28/25	6.16	2	1	0x0AAAAAAAAAAAAAAAAAAAAA	77	0x0	0
6	28/25	6.72	2	1	0x12	7	0x0	0
7	8/7	8	1	1	0x1FFDFFD	25	0x0	0
8.75	8/7	10	1	2	0xAAAD555AAD555	56	0x1555	13
10	28/25	11.2	1	1	0x24A4A4A4A	35	0x0	0
14	8/7	16	0	0	0xFALSE	0	0x0	0
17.5	8/7	20	0	0	0xFALSE	0	0x0	0
20	28/25	22.4	0	0	0xFALSE	0	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	3	2	0x00040010004002	56	0x0002	13

sampling rates (channel bandwidths) and OFDM/OFDMA multiple access methods. For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

Table 50: Parameters for supported 802.16 profiles in case of 1536 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	21	1	0x2	3	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
2.5	144/125	2.88	10	1	0x5	3	0x0	0
3	86/75	3.44	8	1	0x7FFDFFF7FFD	43	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	144/125	5.76	5	1	0x2	3	0x0	0
5.5	316/275	6.32	4	1	0x7EFD7BF7EFE7DFBF7EFD	79	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
10	144/125	11.52	2	1	0x5	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	21	1	0x7FFFBFFFFD	35	0x0	0
1.75	8/7	2	15	1	0x092524A	25	0x0	0
3.5	8/7	4	7	1	0x1B6DB6D	25	0x0	0
5	28/25	5.6	5	1	0x2AAAAAAAAA	35	0x0	0
5.5	28/25	6.16	4	1	0x1FFFFFFFFFFFFFFFFFFFFD	77	0x0	0
6	28/25	6.72	4	1	0x55	7	0x0	0
7	8/7	8	3	1	0x1F7DF7D	25	0x0	0
8.75	8/7	10	3	2	0x00040010004002	56	0x0002	13
10	28/25	11.2	2	1	0x6EEEEEEED	35	0x0	0
14	8/7	16	1	1	0x1FFDFFD	25	0x0	0
17.5	8/7	20	1	2	0xAAAD555AAAD555	56	0x1555	13
20	28/25	22.4	1	1	0x24A4A4A4A	35	0x0	0
28	8/7	32	0	0	0xFALSE	0	0x0	0
4.375	8/7	5	6	1	0x00408102040810204082	77	0x040810204082	48

1
2

Table 51: Parameters for supported 802.16 profiles in case of 3072 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	42 ¹	1	0x5	3	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
2.5	144/125	2.88	21	1	0x2	3	0x0	0
3	86/75	3.44	17	1	0x7EFD7BF7EFD	43	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	144/125	5.76	10	1	0x5	3	0x0	0
5.5	316/275	6.32	9	1	0x6EDDBBB76EEDDBBB76ED	79	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
10	144/125	11.52	5	1	0x2	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	43 ¹	1	0x7F7FBFD7D	35	0x0	0
1.75	8/7	2	30	1	0x1BB76ED	25	0x0	0
3.5	8/7	4	15	1	0x092524A	25	0x0	0
5	28/25	5.6	10	1	0x7FFFFFFFD	35	0x0	0
5.5	28/25	6.16	9	1	0x1FFFFFFFFF7FFFFFFFFFD	77	0x0	0
6	28/25	6.72	9	1	0x02	7	0x0	0
7	8/7	8	7	1	0x1B6DB6D	25	0x0	0
8.75	8/7	10	6	1	0x00408102040810204082	77	0x040810204082	48
10	28/25	11.2	5	1	0x2AAAAAAAA	35	0x0	0
14	8/7	16	3	1	0x1F7DF7D	25	0x0	0
17.5	8/7	20	3	2	0x00040010004002	56	0x0002	13
20	28/25	22.4	2	1	0x6EEEEEEED	35	0x0	0
28	8/7	32	1	1	0x1FFDFFD	25	0x0	0
4.375	8/7	5	12	2	0x122448912244892	59	0x12	7

3

¹ RP3 sub-node address range limits the number of antenna-carriers per node to 32. The supported antenna-carrier range can be extended by using several node addresses for one physical node.

1
2

Table 52: Parameters for supported 802.16 profiles in case of 6144 Mbps virtual RP3 link.

802.16 OFDM Sample Rates			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	144/125	1.44	85	1	0x2	3	0x0	0
1.75	8/7	2	61	1	0x12A5A9	25	0x0	0
2.5	144/125	2.88	42	1	0x5	3	0x0	0
3	86/75	3.44	35	1	0x6EDDBB76EDB	43	0x0	0
3.5	8/7	4	30	1	0x1D76DDB	25	0x0	0
5	144/125	5.76	21	1	0x2	3	0x0	0
5.5	316/275	6.32	19	1	0x49554955495549554955	79	0x0	0
7	8/7	8	15	1	0x1249249	25	0x0	0
10	144/125	11.52	10	1	0x5	3	0x0	0
802.16 OFDMA Sample Rates			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate Mult.	Samp. Rate	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.25	28/25	1.4	87	1	0x77777777	35	0x0	0
1.75	8/7	2	61	1	0x154AA54	25	0x0	0
3.5	8/7	4	30	1	0x1DB6DB7	25	0x0	0
5	28/25	5.6	21	1	0x7FF7FF7FF	35	0x0	0
5.5	28/25	6.16	19	1	0x1FFFFBFFFF7FFFEFFFD	77	0x0	0
6	28/25	6.72	18	1	0x44	7	0x0	0
7	8/7	8	15	1	0x1494948	25	0x0	0
8.75	8/7	10	12	1	0x89122448912244	56	0x1224	13
10	28/25	11.2	10	1	0x7FFFDFFFF	35	0x0	0
14	8/7	16	7	1	0x1B6DDB6	25	0x0	0
17.5	8/7	20	6	1	0x81020408102040	56	0x1020	13
20	28/25	22.4	5	1	0x55554AAAA	35	0x0	0
28	8/7	32	3	1	0x1F7DF7D	25	0x0	0
4.375	8/7	5	24	1	0xADAAB6AADAAB6A	56	0x1AD5	13

3
4

Appendix E: Background Information on Interconnects (Informative)

TYPE 1 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplane and cable while TYPE 2 channel is defined as a serial interconnect at 768 or 1536 Mbaud data rate across backplanes. Figure 75 illustrates TYPE 1 and TYPE 2 interconnects.

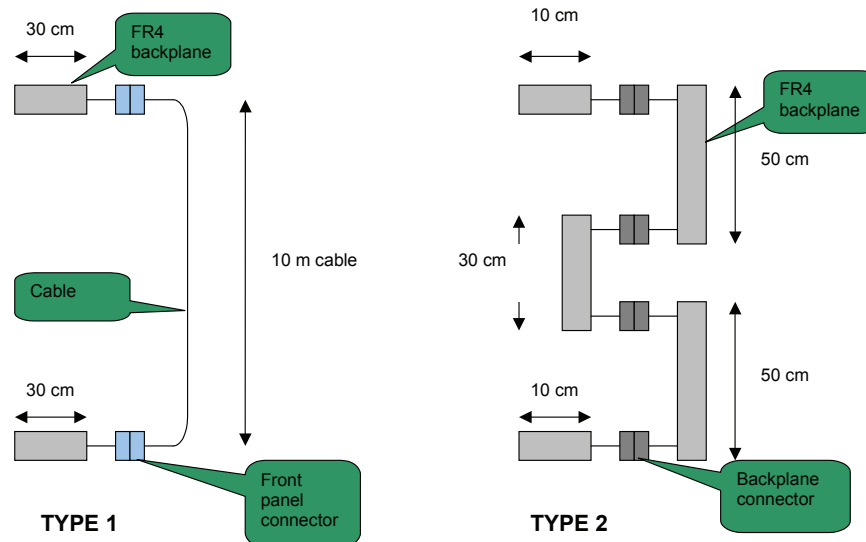


Figure 75: TYPE 1 and TYPE 2 Interconnects.

TYPE 3 Channel is defined as a serial interconnect at 768, 1536, or 3072Mbaud data rate across backplane (PCB) made of commonly used FR4 materials or cable.

TYPE 4 and TYPE 5 Channels are defined as serial interconnect at 6144Mbaud data rate across backplane or cable.

The backplane channels are defined as entirely passive links consists of two line cards interconnect across backplane through two backplane connectors as depicted in Figure 76 and meet the limitations as indicated in .

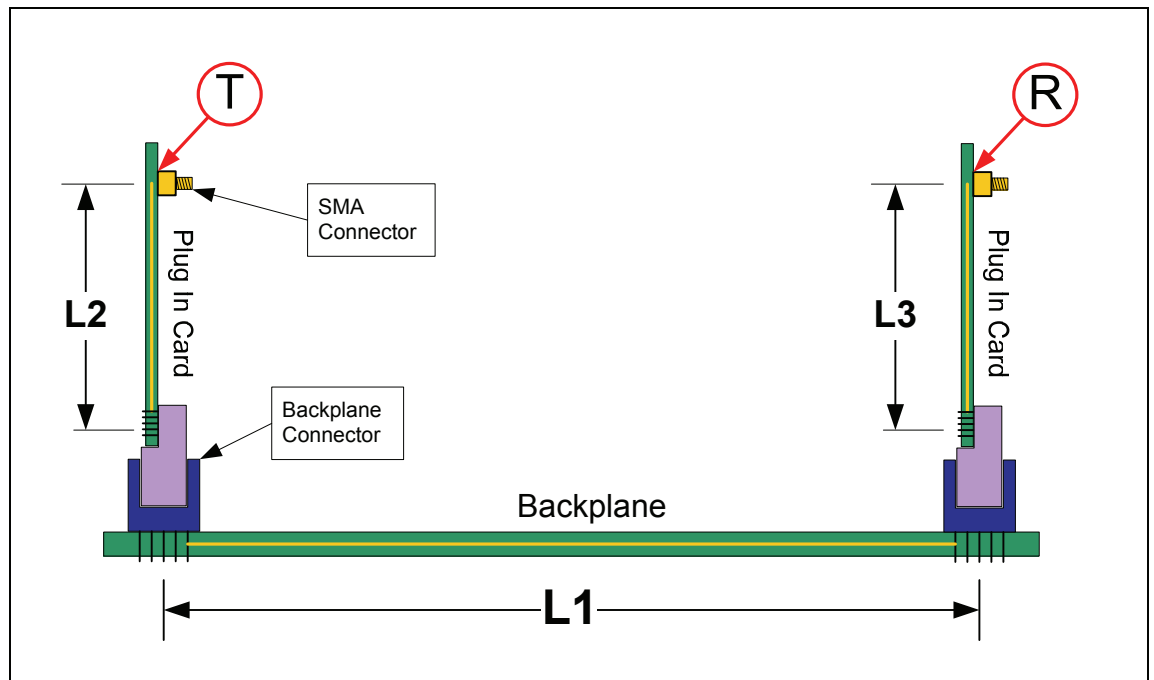


Figure 76: TYPE-3 Backplane Interconnect

Table 53: TYPE 3, 4, and 5 rear interconnect length specifications as indicated in Figure 76.

	Backplane Connector	L1 (Max.)	L2 (Max.)	L3 (Max.)
Type-3	OBSAI system Ref. Appendix B & C (HM 2mm 6 Row) Male & Female	800mm (31.5")	100mm (4")	100mm (4")
Type-4	High Speed / Controlled Impedance of any type	$L1 + L2 + L3 \leq 600\text{mm (23.6")}$		
Type-5	High Speed / Controlled Impedance of any type	$L1 + L2 + L3 \leq 1000\text{mm (39.4")}$		

Notes:

Connectors are excluded from the lengths calculation.

No more than two backplane connectors between point 'T' and 'R'

6 PTH's across the channel from 'T' to 'R' points

The cable channel is defined as entirely passive link consists of two line cards interconnect across cable assembly terminated with front access connectors as depicted in Figure 77 and meet the following limitations.

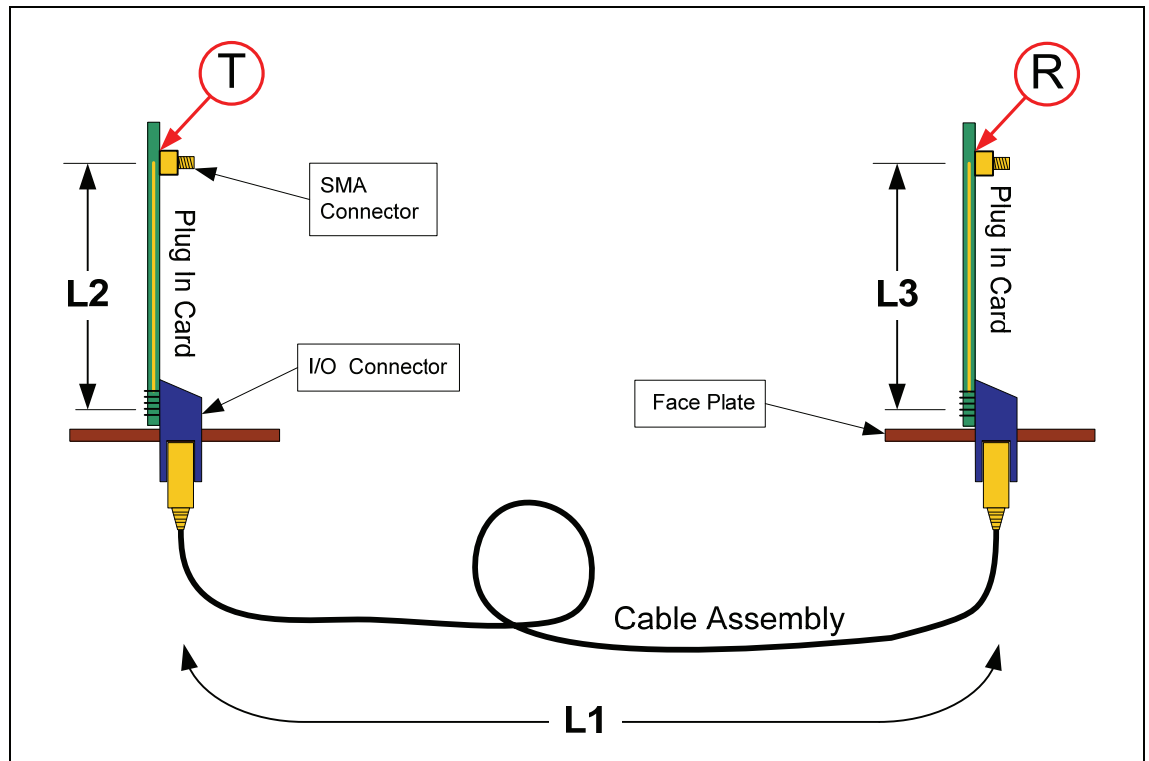


Figure 77: TYPE-3 Cable Interconnect

Table 54: TYPE 3, 4, and 5 front interconnect lengths specifications as indicated in Figure 77.

	Cable I/O Connector	L1 (Max.)	L2 (Max.)	L3 (Max.)
Type-3	OBSAI System Ref. Appendix F (Slim-I/O) Panel Mount Cable To Board	3000mm (9ft)	50mm (2")	50mm (2")
Type-4	High Speed / Controlled Impedance of any type	$L1 + L2 + L3 \leq \text{TBD mm (TBD")}$		
Type-5	High Speed / Controlled Impedance of any type	$L1 + L2 + L3 \leq \text{TBD mm (TBD")}$		

Notes:

No more than 4 PTH's across the channel from 'T' to 'R' points

PCB materials is made of commonly used standard FR4

Cable diameter and conductors AWG shall be determined based on the requirements (refer to [11])

Insertion loss to Crosstalk Ratio

The ICR (Insertion loss to crosstalk ratio) is one of the informative channel parameters defined in the Annex 69B of the IEEE802.3ap for 1000BASE-KX @1.25GBd, 10GBASE-KX4 @3.125 GBd and 10GBASE-KR @10.3125GBd lane rates [17].

The ICR is recommended for informative analysis of the S-Parameter results..

Informative channel parameters in [17]:

- Fitted attenuation
- Insertion loss
- Insertion loss deviation
- Return loss
- Crosstalk
- Power sum differential near-end crosstalk (PSNEXT)
- Power sum differential far-end crosstalk (PSFEXT)
- Power sum differential crosstalk (PSXT)
- Insertion loss to crosstalk ratio (ICR)

Insertion loss to crosstalk ratio (*ICR*) is the ratio of the insertion loss, measured from TP1 to TP4 (T and R as defined in Appendix E of RP3 specification respectively), to the total crosstalk measured at TP4. *ICR* may be computed from *IL* and *PSXT* as shown in the following Equation:

$$ICR(f) = -IL(f) + PSXT(f)$$

The Type 4 and 5 interconnects should meet the limits of Type 10GBASE-KR. Detailed information and Equations for the analysis are available in [17].

$$ICR_{\min}(f) = 23.3 - 18.7 \log_{10} \left(\frac{f}{5GHz} \right); \quad \text{for } 100MHz \leq f \leq 5.15625GHz$$

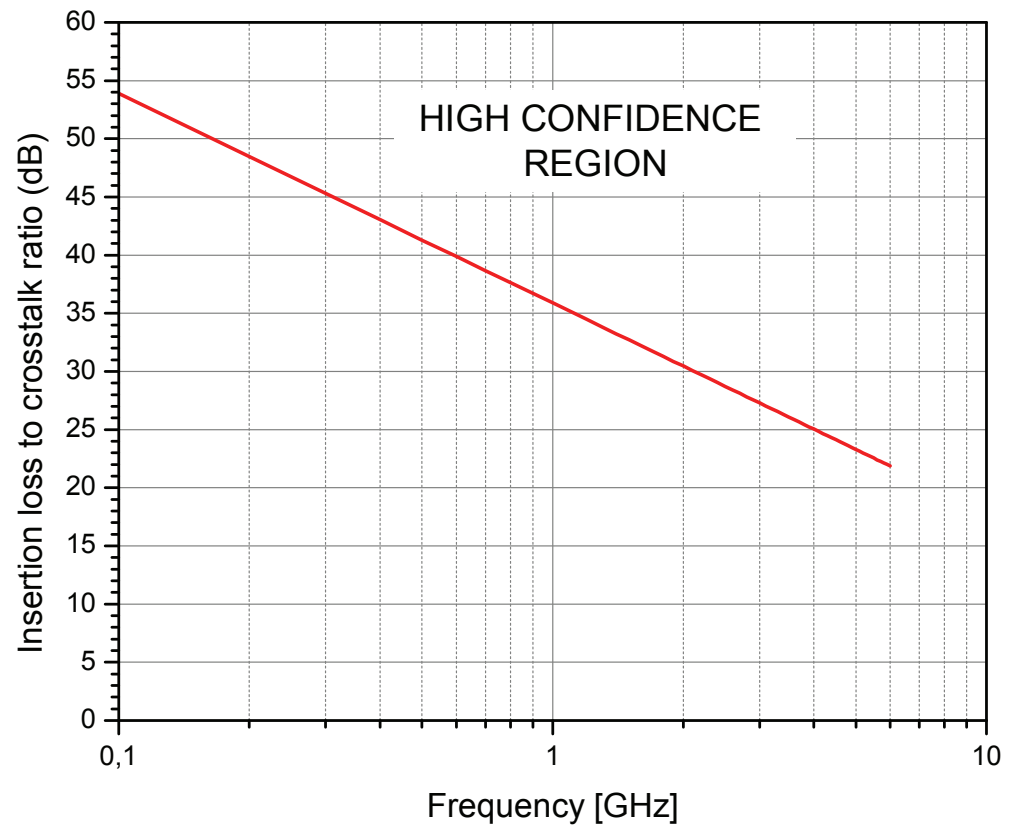


Figure 78: Insertion loss to crosstalk ratio limit

Appendix F: Parameters for LTE Message Transmission

The parameters required for LTE data message transmission are provided in Table 55-Table 58 for the currently defined LTE profiles, i.e. sampling rates (channel bandwidths). For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters. Dual bit map rules are applicable only for the 15MHz channel bandwidth. For other channel bandwidths, antenna-carrier streams consume completely the bandwidth provided by the modulo transmission rules.

Table 55: Parameters for supported LTE profiles in case of 768 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Mo du lo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	8	8	1	0x0	0	0x0	0
3.0	3.84	4	4	1	0x0	0	0x0	0
5	7.68	2	2	1	0x0	0	0x0	0
10	15.36	1	1	1	0x0	0	0x0	0
15	23.04	-	0	0	0xFALSE	0	0x0	0
20	30.72	-	0	0	0xFALSE	0	0x0	0

Table 56: Parameters for supported LTE profiles in case of 1536 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Mo du lo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	16	16	1	0x0	0	0x0	0
3.0	3.84	8	8	1	0x0	0	0x0	0
5	7.68	4	4	1	0x0	0	0x0	0
10	15.36	2	2	1	0x0	0	0x0	0
15	23.04	1	1	1	0x1	3	0x0	0
20	30.72	1	1	1	0x0	0	0x0	0

Table 57: Parameters for supported LTE profiles in case of 3072 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	32	32	1	0x0	0	0x0	0
3.0	3.84	16	16	1	0x0	0	0x0	0
5	7.68	8	8	1	0x0	0	0x0	0
10	15.36	4	4	1	0x0	0	0x0	0
15	23.04	1	2	1	0x3	3	0x0	0
20	30.72	2	2	1	0x0	0	0x0	0

Table 58: Parameters for supported LTE profiles in case of 6144 Mbps virtual RP3 link.

LTE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Chan Band width	Samp. Rate	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
1.4	1.92	64	64	1	0x0	0	0x0	0
3.0	3.84	32	32	1	0x0	0	0x0	0
5	7.68	16	16	1	0x0	0	0x0	0
10	15.36	8	8	1	0x0	0	0x0	0
15	23.04	1	5	1	0x2	3	0x0	0
20	30.72	4	4	1	0x0	0	0x0	0

Appendix G: Parameters for GSM/EDGE/EGPRS2 Message Transmission

G1: Uplink Transmission

The recommended parameters for GSM/EDGE/EGPRS2 uplink data message transmission are provided in Table 59-Table 62. For each profile, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

GSM/EDGE/EGPRS2 uplink data can also be transmitted using only low level modulo rules.

Table 59: Parameters for UL GSM/EDGE/EGPRS2 in case of 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	4	7	136	0	1	1	1
325.000	32	4	5	1	7BEFBDF7DF7BEFBD	63	F7DF7BEFBD	40
270.833	32	2	14	2	00000000000000002	68	0	1
325.000	32	2	11	1	5B6DB5B6DB5B6DB5	63	B6DB5B6DB5	40
270.833	32	1	28	2	00000000400000002	68	0	1
325.000	32	1	23	1	0491244912449124492	73	09124492	30

Table 60: Parameters for UL GSM/EDGE/EGPRS2 in case of 1536 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	56	2	00008000400020002	68	0	1
325.000	32	1	46	1	2D6B5AD6B5AD6B5AD6B5	78	15AD6B5	25

Table 61: Parameters for UL GSM/EDGE/EGPRS2 in case of 3072 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	112	2	010080804040202	60	00202	17
325.000	32	1	93	2	0210842108422	49	02	5

Table 62: Parameters for UL GSM/EDGE/EGPRS2 in case of 6144 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Sample rate (Ksps)	Samp. size	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
270.833	32	1	224	2	111088844442222	60	02222	17
325.000	32	1	188	2	2AA95552AAA5554AAAA	75	0AAA	13

G2: Downlink Transmission

Only modulo rules are required for GSM/EDGE/EGPRS2 downlink samples because there is no summing of downlink samples in BTS systems. Optional dual bit map parameters for GSM/EDGE/EGPRS2 downlink data message transmission are provided in Table 63-Table 67 for different sampling rates and different control messaging scenarios. Control messages can either be sent through the same channel as data or through control message slots. If hard bits are used, the same rules that are used for UL are recommended for symmetry and all DL timeslot messages are sent as a burst.

For each case, the values of six different parameters are defined. Refer to Table 11 for the description of these parameters.

Table 63: Parameters for DL GSM/EDGE in case of 156 symbols per time slot and 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Contr ol messa ges per time slot	Mo du Lo	X	Bit Ma p 1 Mu lt.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversamp ling	0	4	14	11	0104208410821042	61	02	6
	3	4	13	3	01041041041041041042	77	042	12
	6	4	12	16	244891244892	48	0492	13
156, 2x oversamp ling	0	4	7	7	0020040100200802	63	002	10
	3	4	6	3	3DF7DF7DF7DF7DF7D	78	7BEFBEBEFBD	47
	6	4	6	26	AD6B56B5AB5AD5	56	0	1
156, 4x oversamp ling	0	4	3	18	2AAAB55556AAAAD5555	74	15555555	29
	3	4	3	18	554AAA5552AA9554AAA	76	2AAAA	19
	6	4	3	7	25294A5294A5294A	63	1294A52A	30
156, no oversamp ling	0	2	28	11	092524A49292524A	61	0A	6
	3	2	26	3	4924924924924924A	80	2	3
	6	2	24	13	AD5AD5AD5AD5AD5	60	1	1
156, 2x oversamp ling	0	2	14	7	0421042108210842	63	022	10
	3	2	13	3	2DB6DB6DB6DB6DB6D	78	5B6DB6DB6DB5	47
	6	2	13	32	010420821042	45	01042	17
156, 4x oversamp ling	0	2	7	24	00004000080002	56	00002	17
	3	2	6	27	7FF7FFBFFDFFD	51	3FD	10
	6	2	6	13	3BDEF7BDD	34	1DEF7BDD	29
156, no oversamp ling	0	1	56	15	6EDDBBB76ED	43	DDBB76ED	32
	3	1	52	3	DB6DB6DB6DDB6DB6DB6D	80	5	3
	6	1	49	10	01041041041041041042	78	1	1
156, 2x oversamp ling	0	1	28	7	252525292929494A	63	12A	10
	3	1	27	3	12492492492492492492	79	4924924924A	44
	6	1	26	32	0924A492924A	45	0924A	17
156, 4x oversamp ling	0	1	14	24	00804010080402	56	00202	17
	3	1	13	27	7DF7EFBEFDF7D	51	3BD	10
	6	1	13		56B56B5AB5AD5	51	AD5	12

1
2

Table 64: Parameters for DL GSM/EDGE in case of 187 symbols per time slot and 768 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 768 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
187, no oversampling	0	4	11	1	1DDDD	17	0	0
	3	4	11	4	0000400020002	50	00002	17
	6	4	10	1	2A54AA	23	0	0
187, 2x oversampling	0	4	5	2	FEFF7FBFDFF7FBFD	72	7FBFD	19
	3	4	5	20	1B76EDBB76D	41	1B76ED	21
	6	4	5	4	1555AAAD555AAAD555	69	1555	13
187, 4x oversampling	0	4	2	2	FFFF7FFFDF7FFFDF	72	7FFFDF	19
	3	4	2	1	1FEFFBFEFFBFEFFBFD	69	0	0
	6	4	2	20	1F7EFD7BF7D	41	1F7EFD	21
187, no oversampling	0	2	23	1	15555	17	0	0
	3	2	22	4	0040402020202	50	00202	17
	6	2	20	1	7EFEFD	23	0	0
187, 2x oversampling	0	2	11	2	1DEEF77BBDDEEF77BBDD	77	1DD	9
	3	2	11	15	0A52A52A52A52A	53	14A54A52A52A	46
	6	2	11	5	00040010004002	55	0002	14
187, 4x oversampling	0	2	5	2	FEFF7FBFDFF7FBFD	72	7FBFD	19
	3	2	5	1	1DEF7BDEF7BDEF7BDD	69	0	0
	6	2	5	20	1B76EDBB76D	41	1B76ED	21
187, no oversampling	0	1	47	1	00002	17	0	0
	3	1	44	3	08888844444422222	71	2	4
	6	1	41	1	6EEEEED	23	0	0
187, 2x oversampling	0	1	23	3	55AAD56AB55	43	2AD56AB55	34
	3	1	22	17	7BEFBEFBEFBD	47	3DF7DF7DF7D	42
	6	1	22	5	02040810204082	55	0082	14
187, 4x oversampling	0	1	11	2	1DEEF77BBDDEEF77BBDD	77	1DD	9
	3	1	11	1	15AD6B5AD5AD6B5AD5	69	0	0
	6	1	11	15	0A52A52A52A52A	53	14A54A52A52A	46

3

1
2

Table 65: Parameters for DL GSM/EDGE in case of 1536 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 1536 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversampling	0	1	113	15	2A552A954AA	43	54A954AA	32
	3	1	105	3	4924949249492494924A	80	2	3
	6	1	98	10	124924924924924924A	75	2529294A	31
156, 2x oversampling	0	1	56	7	77777BBBBBDDDDDD	59	3BBBBDDDDDD	38
	3	1	54	4	B6DB6DB6DB6DB6DB5	68	16D	9
	6	1	52	32	1B76EDDBB76D	45	1B76D	17
156, 4x oversampling	0	1	28	19	042110844211084422	70	08844222	31
	3	1	27	39	6DB6EDB6D	35	36DB6D	22
	6	1	27	9	0410420821042	51	042	12
187, no oversampling	0	1	94	1	00202	17	0	0
	3	1	88	4	555554AAAAAA	48	0AAAAAA	25
	6	1	83	1	2AAAAA	23	0	0
187, 2x oversampling	0	1	47	2	010080804040202	60	00804040202	43
	3	1	45	16	2DB6DB6DB6DB5	50	16DB6DB6DB5	41
	6	1	44	5	12244892244892	55	0892	14
187, 4x oversampling	0	1	23	3	55AAD56AB55	43	2AD56AB55	34
	3	1	23	1	010841084108410842	69	0	0
	6	1	22	17	7BEFBEFBEFBD	47	3DF7DF7DF7D	42

3

Table 66: Parameters for DL GSM/EDGE in case of 3072 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 3072 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, no oversampling	0	1	226	11	FEFF7F7FBFBFDFD	60	1FDFD	17
	3	1	210	3	DB76DDB76DDB76DDB76D	80	5	3
	6	1	196	10	DB6DB6DB6DB6DB6DB6D	76	16DB6D	21
156, 2x oversampling	0	1	113	7	55555AAAAB55555	59	2AAAAD5555	38
	3	1	109	4	24924924492492492	68	04A	9
	6	1	105	32	0A54A94A952A	45	0A52A	17
156, 4x oversampling	0	1	56	19	14A952A54A952A54AA	70	2A9552AA	31
	3	1	55	39	24A4A4A4A	35	124A4A	22
	6	1	54	6	24925249292494924A	71	0924A492924A	45
187, no oversampling	0	1	188	1	02222	17	0	0
	3	1	176	3	FFFFFDFFFFFDFFFFFD	72	1	1
	6	1	166	1	7FFFFD	23	0	0
187, 2x oversampling	0	1	94	2	111088844442222	60	08884442222	43
	3	1	91	11	1249244924922492492	75	2492	16
	6	1	88	6	56AD6AD6AD5	43	56AD6AD5	31
187, 4x oversampling	0	1	47	2	010080804040202	60	00804040202	43
	3	1	46	1	09494949494949494A	69	0	0
	6	1	45	16	2DB6DB6DB6DB5	50	16DB6DB6DB5	41

Table 67: Parameters for DL GSM/EDGE in case of 6144 Mbps virtual RP3 link.

GSM/EDGE Sample Rates & Modulo Rule			Dual Bitmap Parameters for 6144 Mbps virtual RP3 link					
Sample rate (samples per time slot)	Control messages per time slot	Modulo	X	Bit Map 1 Mult.	Bit Map 1	Bit Map 1 Size	Bit Map 2	Bit Map 2 Size
156, 2x oversampling	0	1	227	7	000010000100002	59	0000080002	38
	3	1	218	5	2DB6D6DB6B6DB5	54	5B5	11
	6	1	210	32	1F7DFBEFDF7D	45	1EFBD	17
156, 4x oversampling	0	1	112	17	3F7EFDFBF7EFDFBF7EFD	78	7BEFBEFBD	35
	3	1	110	21	377777776EEEEEEED	66	1	1
	6	1	108	7	1B76DDBB6EDDB76D	61	DBB6EDDB76D	44
187, 2x oversampling	0	1	188	2	2AA95552AAA5554AAAA	75	0AAA	13
	3	1	182	11	5B6B6D6DB5B6B6DADB5	75	B5B5	16
	6	1	177	6	02082082082	43	02082082	31
187, 4x oversampling	0	1	94	2	111088844442222	60	08884442222	43
	3	1	92	1	1DDDDDDDDDDDDDDDDDD	69	0	0
	6	1	91	11	1249244924922492492	75	2492	16

Glossary

Abbreviations

BB	Baseband module
BTS	Base transceiver system
C/D	Combiner and distributor
CCM	Control and clock module
DL	Downlink direction from BTS to RRUs
HW	Hardware
LC	Local Converter that interfaces to RP3 and RP1 and combines them to RP3-01 and vice versa. Local Converter is referred to as Local cabinet in [2].
LSB	Least Significant Bit
LTE	Long Term Evolution
MSB	Most Significant Bit
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
RP3-01	Extension of RP3 protocol where RP1 data is mapped into RP3 messages
RRU	Remote RF unit. RRU is referred to as Remote cabinet in [2].
SFN	System frame number
UL	Uplink direction from RRUs to BTS

Definition of Terms

None listed.

References

- [1] A.X. Widmer and P.A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM Journal of Research and Development, vol. 27, no. 5, pp. 440-451, Sept. 1983.
- [2] Open Base Station Architecture Initiative, BTS System Reference Document.
- [3] IEEE 802.3ae Standard for Information Technology – Local & Metropolitan Area Networks – Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications-- Media Access Control (MAC) Parameters, Physical Layer, and Management Parameters for 10 Gb/s Operation
- [4] Open Base Station Architecture Initiative, Reference Point 1 Specification, Section 8.4.
- [5] Open Base Station Architecture Initiative, Baseband Module Specification.
- [6] Open Base Station Architecture Initiative, RF Module Specification.
- [7] IEC 60793-2-10 (2002-3) Part 2-10: Product specifications sectional specification for category A1 multimode fibres, March 2002
- [8] IEC 60793-2-50 (2002-1) Part 2-50: Product specifications sectional specification for class B single-mode fibres, January 2002
- [9] INCINTS 352 – Fibre Channel 1998 Physical Interface (FC-PI'98), 1998.
- [10] IEEE 802.3 Standard for Information Technology – Telecommunication and Information Exchange Between Systems – Local and Metropolitan Area Networks – Specific Requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
- [11] Open Base Station Architecture Initiative, BTS System Reference Document, Appendix F.
- [12] Fibre Channel, Physical Interface-4 (FC-PI-4)
- [13] SFF-8431, SFP+
- [14] Implementation Agreement OIF-CEI-02.0
- [15] RapidIO Part6: LP-Serial Physical Layer Specification Rev. 2
- [16] Open Base Station Architecture Initiative, Appendix G Conformance Test Cases for RP3 Interface.

- | | | |
|---|------|---|
| 1 | [17] | StatEye development forum, |
| 2 | | http://www.stateye.org/developmentForum/doku.php |
| 3 | [18] | IEEE 802.3ap Standard for Information Technology – Telecommunication |
| 4 | | and Information Exchange Between Systems – Local and Metropolitan |
| 5 | | Area Networks, Annex 69B. |

TAB D



About

Documents

Members of OBSAI

Specifications

OBSAI System Spec V2.0

[OBSAI_System_Spec_V2.0.pdf](#) 1.74 MB

System Spec Appendix F V1.0

[Appendix F Panel Mount IO Cable to Board Connector_V1_0.pdf](#)
888.46 kB

OBSAI System Ref Doc v2.0

[OBSAI_System_Spec_V2.0.pdf](#) 2.89 MB

OBSAI System Spec Appendix B

[OBSAI_SystemSpecAppendixB.pdf](#) 399.38 kB

OBSAI System Spec Appendix C

[OBSAI_SystemSpecAppendixC.pdf](#) 235.48 kB

RP Specifications

RP1_v2.1

[RP1_Spec_v2_1.pdf](#) 1,019.33 kB

RP2_v2.1

[RP2_V2_1.pdf](#) 358.14 kB

RP3_V4.2

[RP3_Specification_V4.2.pdf](#) 1.61 MB

RP4_v1.1

[RP4_V1.1.PDF](#) 57.22 kB

Module Specifications

TM Specification v1.0

[TM_Specification_v1.0.pdf](#) 149.22 kB

GPM Specification v1.0

[GPM_Specification_V1.0.PDF](#) 111.84 kB

CCM Specification v1.0

[CCM_Specification_v1.0.pdf](#) 132.78 kB

BBM_spec_v1.0

[BBM_spec_v1.0.pdf](#)

TAB E

Open base station architecture

Analysis

19 December 2006

So, what's the correlation between Charles Darwin's theory of evolution and base station antennas, you may ask. Peter Kenington makes the connection...

In 1859, when Charles Darwin first published "On the Origin of Species...", there is little doubt that he did not have wireless base-stations in mind. In reality, however, many of his ideas are equally applicable to this area of evolution, as they are to evolution in the natural world. One of the key elements that have enabled this to happen is the now widely accepted set of open specifications, set out by the Open Base Station Architecture Initiative (OBSAI), covering the interfaces between the main modules within a base station.

Darwin's key insight was in noticing that, in the natural world, the survival of a species is based upon its ability to adapt to environmental change and to competition from rival species that are also evolving. The key to survival is in finding a niche, be it large or small, within the ecosystem of our planet. Niches exist at all levels within the food chain, from that of a simple, low functionality existence (e.g. single-celled creatures, bacteria etc.) through to something of much higher 'performance' (e.g. tigers, dolphins and man). The same situation exists in the base-station arena, where simple, low cost pico and femto BTSs are beginning to emerge to fulfil low cost, short-range coverage requirements. These complement larger, more sophisticated designs for high-capacity, multi-carrier macro cells. In both cases, the key to survival rests in achieving acceptable or superior levels of performance, for the lowest possible ownership cost.

The natural world and the world of base-stations have one major difference from an evolutionary perspective, and that is that base-stations can now immediately take advantage of the latest innovation (in RF or baseband) through the designing in or substitution of a new RF, baseband, transport, clock/control or power supply module. The internal interface specifications, pioneered by OBSAI, enable this process for a BTS (Base-station Transceiver System). In the case of the natural world, however, the adoption of a new form of jaw, leg muscle etc. from another species would either take very many generations or prove to be impossible. This is, in many respects, how things used to be in the base-station world: if a particular OEM included a useful innovation in its new generation BTS product, at best, this would be copied by its rivals in a subsequent generation of BTS.

The adoption of the OBSAI standards represents a significant short-cut in this process, since innovations which are included in module products placed on the open market, can become a part of many manufacturers' products quite quickly. This potentially reduces the hardware development burden within the OEMs and allows them greater freedom to concentrate on developing aspects of their products, which will provide true differentiation from their competitors. Many of these areas fall within the domain of software and this will increasingly dominate in future BTS generations. It is this area more than most that will lead to the survival of the 'fittest' – which in a BTS context translates to the most innovative.

The OBSAI organisation consists of more than 130 component, module and base station vendors. Its aim is to create an open set of specifications for the internal modules required in a base-station, encompassing both interface and mechanical aspects. A good analogy in the PC industry is that of the PCI bus/card specifications. Many more unit-level options will become available in the future, as the technology develops to integrate modules into combined units. This will open up new location possibilities for base-stations due to the availability of smaller and more versatile architectures that are easier to site.

Revolution in evolution

The last 20 years or so has seen a revolution in the PC industry, in cost, yes, but also in capability and this has been brought about, in a large part, by the PCI bus. Most PC manufacturers offer a huge range of models, but these generally fall into a very small number of 'families' – often just one. PC manufacturers have achieved the seemingly impossible, in being able to offer a huge range of choice to their customers whilst employing a modest cost base for their organization. This has been achieved through minimizing inventory and design engineering services, through the use of standard packaging and 'modules' (e.g. graphics cards, DVD-drives, memory cards, motherboards etc.). These modules can then be selected appropriately to generate a large product offering appropriate for all tastes and budgets. Their success rests, in a large part, on them being able to provide the customer with exactly what he or she wants. This is a level of service that it has not, in the past, been economic to provide in the base-station area.

Changed landscape

OBSAI's announcement, in June 2006, that it had released a full set of interface, hardware and test specifications for the internal interfaces within a base-station has changed the landscape for the mobile radio base-station. OBSAI's specifications are compatible with all of the major current and emerging air interface standards, including GSM, GSM/EDGE, WCDMA, CDMA2000 and WiMAX and are available for public download free of charge (from www.obsai.com). These specifications allow module vendors to manufacture modules that are capable of operating

in any OBSAI-compatible BTS, thereby reducing substantially the development effort and costs involved in the introduction of a new range of BTS products. They also enable a more PC-like model to be adopted in the design and construction of a BTS product – i.e. the selection of modules from a range of vendors at a range of capability levels and costs, such that the overall BTS closely matches the operator's requirements. Embracing this model will be a route, and a key, to survival in the emerging BTS marketplace.

A head in the clouds

The changes in the market landscape, in terms of planning restrictions, health concerns, acoustic noise objections (from cooling fan noise) and many other issues are making it increasingly difficult for operators to erect new cell sites. New BTS architectures are therefore emerging to try and address these problems; here again, the survivors will be those that adopt these new architectures and can make them work for their customers. These issues have given birth to the remote RF head – a new form of BTS deployment that is fully supported by the OBSAI specifications. This architecture places the active RF electronics remotely from the rest of the BTS and its associated backhaul. The remote RF head itself houses all of the radio-related functions (transmitter RF, receiver RF, filtering etc.). This is then connected to the remainder of the BTS via fibre-optic cable. The above arrangement allows main elements of the BTS (the digital and network interface modules) to be housed in a low-cost internal location, such as a basement. The RF head can then be situated on the roof of the building or on an outside wall. Another option is to site the remote RF head at the top of an antenna mast, with the remainder of the BTS being located at the base of the mast in a suitable hut or other enclosure.

Cheap hotels bring comfort

This principle can be extended to multiple remote RF heads, whilst still maintaining a single, central, location for the other aspects of their associated base-stations. This concept is usually referred to as a BTS hotel. The remote RF heads themselves can be located a substantial distance from the main BTS hotel site, due to the very low losses associated with the fibre optic cables used to connect them to the remainder of the BTS.

One of the main advantages of the BTS hotel architecture lies in its ability to provide cost-effective BTS redundancy. It is typically not economically viable to provide 100 per cent redundancy within a traditional BTS. However, in the case of a BTS hotel, N+1 redundancy can be used (i.e. the provision of one redundant BTS covering a number of active BTS systems within the BTS hotel location).

Significant disadvantage

The significant disadvantage with the BTS hotel architecture is, however, in the cost of the fibre optic links that run between the BTS hotel and its remote units. Installing new fibre – if there is none in existence already – involves significant civil works and is therefore extremely expensive. There are, however a number of examples of various types of BTS hotel in operation today, covering applications in city centers, at airports and for major sporting events. So, natural selection has been a part of the evolution of the earth's species for billions of years and has proved to be a successful method of ensuring that the best-adapted species are available to maintain our ecosystem. In the world of base-station engineering, the same principles apply – however the timescales are dramatically shorter. The open specifications provided by OBSAI shine a powerful light on the future evolutionary path for the BTS – it will be interesting to see who is the fittest and, hence, survives this new dawn.

Peter Kenington is the Managing Director of Linear Communications Consultants and the Technical Chair of OBSAI. Email: pbk@linearcomms.com

TAB F

http://www.obsai.com/obsai/documents/public_documents

Go

APR MAY SEP

25

2006 2007 2008

About this capture

4 captures

25 May 2007 - 5 Apr 2010



Public Documents

Public documents are stored here.

Links for Supplementary Material

This area is for documents endorsed by OBSAI but which do not form a part of the OBSAI specifications.

[View list](#)

Download Specifications

This area is for downloadable specifications

[View list](#)

Not logged in

Login

Password

[Join OBSAI?](#)

[Forgot your password?](#)

Latest News

[Invitation to OBSAI Meeting, May 22-24.](#)

The meeting will be held in Nokia White Plains office, NY, USA and is hosted by Nokia Siemens Networks.

[Read more...](#)

[Wimax World Europe](#)

Austria,
Vienna
May
29-31,
2007



[Read more...](#)

[Elektrobit Introduces Base Station Interface Tester for Verification of OBSAI RP3 and RP3-01 Interfaces](#)

Elektrobit Introduces...

[Read more...](#)