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PROVISIONAL APPLICATION

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FOR

Daisy-Chained Ring of Remote Units for a Distributed Antenna System

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SPECIFICATION

Related Applications

[001] This is a continuation-in-part and claims the benefit of U.S. patent application S.N. 12/767,669, entitled "Remotely Reconfigurable Power Amplifier System and Method," filed April 26, 2010, and through it U.S. Pat. Appn. S.N. 61/172,642, filed on April 24, 2009, and further claims the benefit of U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010, and the benefit of U.S. Provisional Application S.N. 61/382,836, entitled "Remotely Reconfigurable Distributed Antenna System and Methods," filed September 14, 2010, all of which are hereby incorporated by reference in their entirety for all purposes, and attached hereto as Appendices.

FIELD OF THE INVENTION

[002] The present invention generally relates to wireless communication systems employing Distributed Antenna Systems (DAS) as part of a distributed wireless network. More specifically, the present invention relates to a DAS utilizing one or more remotely monitored and controlled digital access units configured to assign particular packet transmissions to selected ones of a plurality of remote units, which can in some embodiments be configured in a daisy-chained rings.

BACKGROUND OF THE INVENTION

[003] Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates.

Mobility and an increased level of multimedia content for end users requires end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. One of the most difficult challenges faced by network operators is maximizing the capacity of their DAS networks while ensuring cost-effective DAS deployments and at the same time providing a very high degree of DAS remote unit availability.

[004] In order to provide DAS network capacity which is high enough to meet short-term needs of network subscribers in specific locations yet also avoid costly and inefficient deployment of radio resources, DAS network planners prefer to employ DAS architectures and solutions which provide a high degree of dynamic flexibility. Therefore, it would be advantageous for wireless network operators to employ a DAS solution which has a high degree of flexibility to implement dynamic rearrangements based on ever-changing network conditions and subscriber needs. Also, the more future-proof a DAS deployment can be, generally the lower its life cycle cost.

[005] DAS network planners and system integrators employ a wide range of innovative approaches for helping to ensure that a particular DAS deployment is as cost-effective as possible. The types of costs considered by network planners and integrators include DAS deployment or DAS installation cost, as well as operational costs including maintenance costs, emergency restoration costs and network re-arrangement costs. Rearrangement costs are particularly significant for indoor DAS applications, due to frequent changes in building use and facility needs changes. Therefore, it would be advantageous to employ DAS systems and methods which are based on as few DAS transport facilities as possible to minimize

installation and/or lease costs and have self-healing capabilities to avoid the need for costly emergency restoration services.

[006] In order to obtain a high degree of DAS remote unit availability, two primary conditions must be satisfied. First, the DAS remote unit itself must be inherently reliable. Second, the transport media e.g., optical fiber, must be very reliable. It is well known that electronic and/or optical connections themselves are a significant root cause of failure or reduced availability in a DAS network. Companies who maintain outdoor DAS networks have reported that a failure of outside plant optical fiber facilities is not as rare as would be desirable. Therefore, it would be advantageous to employ systems and methods which offer higher redundancy and/or self-healing features in the event of failure of a transport media connection.

SUMMARY OF THE INVENTION

[007] The present invention substantially achieves the advantages and benefits discussed above and overcomes the limitations of the prior art discussed above by providing a distributed antenna system responsive to one or more base stations and having at least one but in some embodiments a plurality of Digital Access Units ("DAU's"), each operating to control the packet traffic of an associated plurality of Digital Remote Units ("DRU's"). In embodiments employing multiple DAU's, the DAU's can be daisy-chained linearly or in a ring configuration. Likewise, depending upon the implementation, the DRU's associated with a given DAU can be configured in either a linear or ring Daisy chain configuration.

[008] The data received from the base stations is down-converted, digitized and converted to baseband with the DAU. The data streams are then I/Q mapped and framed and independently serialized, such that multiple data streams are available in parallel from the DAU. In at least some embodiments, the DAU communicates with the associated DRU's via an optical transport arrangement. It will be appreciated by those skilled in the art that, using the present invention, it is possible to configure a distributed antenna system having *n* base stations, each providing *m* RF outputs for transmission by one or more associated DAU's to *o* DRU's, where the only limits are imposed by the technical performance specifications of the particular DAS, such as delay.

[009] By the use of a ring configuration for connecting, in at least some embodiments, the DRU's and/or the DAU's, fault tolerance is built into the system, with resulting high availability. In single DAU embodiments, each DRU is accessible through two paths, and therefore remains available even in the event of a line break. In multi-DAU embodiments, where the DAU's are linearly daisy-chained, each DRU is accessible from multiple DRU's such that even some DAU failures will not prevent system operation. In embodiments employing a ring connection for the DAU's, multiple paths exist to each DAU, and thus provide an additional level of fault tolerance as well as dynamic load balancing and resource management as discussed in greater detail hereinafter.

[0010] Thus, the configuration of the advanced system architecture of the present invention provides a high degree of flexibility to manage, control, enhance and facilitate the radio resource efficiency, usage, availability, and overall performance of the distributed wireless network. The present

invention enables specialized applications and enhancements including Flexible Simulcast, automatic traffic load-balancing, network and radio resource optimization, network calibration, autonomous/assisted commissioning, carrier pooling, automatic frequency selection, radio frequency carrier placement, traffic monitoring, traffic tagging, and indoor location determination using pilot beacons. The present invention can also serve multiple operators, multi-mode radios (modulation-independent) and multi-frequency bands per operator to increase the efficiency and traffic capacity of the operators' wireless networks.

[0011] Further the present invention provides a high degree of dynamic flexibility, supports dynamic re-arrangements, and provides a low life cycle cost. This advanced system architecture enables deployment of DAS networks using fewer DAS transport facilities to reduce costs, while providing self-healing features. The present invention also offers redundancy and enhanced system availability.

[0012] It is an object of the present invention to provide Flexible Simulcast capabilities, as disclosed in U.S. Provisional Application S.N. 61/382,836, entitled "Remotely Reconfigurable Distributed Antenna System and Methods," filed September 14, 2010, incorporated herein by reference and attached as Appendix A, in a high-availability ring configuration using, for example, optical fiber transport. As discussed above, the ring configuration insures that a break in any optical fiber cable will not shut down the daisy-chained network, because the downlink and uplink signals can be rerouted around the cable break to the respective DRUs.

[0013] It is a further object of the present invention to balance the bidirectional data rate on the optical fibers so as to increase the maximum achievable data rate during operation on the ring network of DRUs.

[0014] It is a further object of the present invention to provide higher transport network capacity in the event the data transport is asymmetrical between the downlink and uplink, as is typically the case for mobile broadband networks.

[0015] It is a further object of the present invention to provide an adaptive and automatic control for optimizing the transport media capacity on the ring.

[0016] It is a further object of the present invention to provide a method of summing co-channel users' uplink signals in the DRU daisy chain.

[0017] Applications of the present invention are suitable to be employed with distributed base stations, distributed antenna systems, distributed repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

[0018] Appendix I is a glossary of terms used herein, including acronyms.

THE FIGURES

[0019] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0020] Figure 1 is a block diagram according to one embodiment of the invention showing the basic structure and an example of a unidirectional,

channelized downlink transport, one ring scenario based on having one DAU and four DRUs.

[0021] Figure 2 is a block diagram in accordance with an embodiment of the invention showing the basic structure and an example of a unidirectional, channelized uplink transport, one ring scenario based on having one DAU and four DRUs.

[0022] Figure 3 is a block diagram in accordance with an embodiment of the invention showing the basic structure and an example of a unidirectional, channelized uplink transport, two ring scenario based on having one DAU and eight DRUs.

[0023] Figure 4 is a block diagram in accordance with an embodiment of the invention showing the basic structure and an example of a unidirectional channelized uplink or downlink transport. This example of a five ring scenario comprises two DAUs and twenty DRUs.

[0024] Figure 5 illustrates an embodiment of a cellular network system employing multiple DRUs according to the present invention.

[0025] Figure 6 illustrates an embodiment of a multi-band system employing six different services operating in different frequency channels with multiple DRUs according to the present invention.

[0026] Figure 7 illustrates in block diagram form the interaction between the DAU embedded software control module and the DRU embedded software control module.

[0027] Figure 8 illustrates in block diagram form an embodiment of a DAS according to an aspect of the invention, including daisy-chained DAU's.

DETAILED DESCRIPTION OF THE INVENTION

[0028] The present invention is a novel Reconfigurable Distributed Antenna System that provides a high degree of flexibility to manage, control, re-configure, enhance and facilitate the radio resource efficiency, usage and overall performance of the distributed wireless network. Figure 1 illustrates an embodiment of the Distributed Antenna System 100 in accordance with the present invention. The system employs a Digital Access Unit functionality 105 (hereinafter "DAU"). The DAU 105 serves as an interface between associated base stations (BTS) 110A-B and a plurality of digital remote units (DRU) 125A-n, although only four DRU's are shown in Figure 1. In the present description, "DRU" will be used interchangeably with Remote Radio Head Unit, or "RRU", because of the similarity of the functions discussed herein, although those skilled in the art will recognize that a DRU communicates with a DAU, whereas an RRU communicates with a base station. In addition, those skilled in the art will recognize that a DAU is monitored and controlled by a remote network operations center ("NOC"), as indicated at bidirectional link 115 in Figure 1. Such links are typically Ethernet connections or external modems, but can be any form of link suitable for remote monitoring and control. The NOC has the capability to remotely configure the DAU parameter settings which in turn configures the DRU's parameter settings. The NOC can request information from the DAUs. The DAUs can subsequently request information from the DRUs. The information requested includes but is not limited to uplink power, downlink power, optical error rate, gain settings, active carriers, etc.

[0029] For the downlink (DL) path, RF input signals 120A through 120*n* are received at the DAU 105 from one or more base station units (BTS) indicated at 110A through 110p. The RF input signals are separately down-converted, digitized, and converted to baseband (using a Digital Down-Converter) by the DAU. Data streams are then I/Q mapped and framed and specific parallel data streams are then independently serialized and translated to optical signals using pluggable SFP modules, again by the DAU 105. The independently serialized, parallel data streams are then delivered to different DRU's 125A-125*k*, typically over optical fiber cable arranged, in at least some embodiments, in a ring configuration indicated at connection pairs 140A-145A, or, in other embodiments, a daisy chain configuration. In addition, each DAU can support a plurality of rings with associated DRU's, where the additional rings are indicated by fiber optic pairs up through 140*o*-145*o*. . It will be appreciated by those skilled in the art that the number of RF inputs, DAU's and DRU's and rings is limited only by network performance factors, such as delay. In addition, as discussed in connection with Figure 4 herein, the DAS can be further extended by using a ring or daisy-chain of DAU's, each of which supports an arrangement of DRU's and rings as shown in Figure 1.

[0030] One function of the DAU 105 is to determine the direction in which downlinked channels are propagated around the ring. As just one example, the embodiment shown in Figure 1 is configured to have downlink channels A, B, C and D propagate in a first direction, for example clockwise, and channels E, F, G, and H propagate in the counter direction, although it will be understood that the number of channels propagating in each direction need not be equal, nor adjacent, nor sequential. Likewise, the number of channels received at each DRU is assigned by the DAU and need not be equal,

adjacent or sequential, but instead will typically be any configuration that optimizes network utilization.

[0031] Referring next to Figure 2, an embodiment of an uplink (UL) path in accordance with the invention can be better appreciated. Channels received at the antenna associated with each DRU are converted into optical signals by each DRU 125A-125*k*. Optical signals received from the DRU's are de-serialized and de-framed by the DAU 105, and are also up-converted digitally using a Digital Up-Converter implemented within the DAU 105. Each data stream is then independently converted to the analog domain and up-converted to the appropriate RF frequency band, still within the DAU 105 in the illustrated implementation, although this functionality can be separate. The RF signals are then delivered to the appropriate one of a plurality of BTS' 110A-110*p*. As with the arrangement shown in Figure 1, the direction of propagation of each channel is controlled by the DAU, with some channels propagating in a clockwise direction and others in a counterclockwise direction. Also as discussed in connection with Figure 1, while adjacent channels are shown as propagating in the same direction in Figure 2, this is not required and any channel can be selected to propagate in either direction.

[0032] Referring again to Figure 1, it will be appreciated by those skilled in the art that, in some implementations of a DAS, more than one carrier can exist in each channel, and, as such, a DRU may receive a channel comprising a signal containing two or more carriers, or a wireless operator may have more than one RF carrier per channel allocated to a single base station. This is referred to as a "composite signal". The manner in which a composite downlink signal is managed by the present invention can be better understood with reference to Figure 1. In such instances, the DAU will

receive a composite downlink input signal 130 from, e.g., a first base station 110A belonging to one wireless operator, enters the DAU 105 at the RF input port 120A. Composite signal 130 comprises carriers A-D. A second composite downlink input signal from e.g., a *p*th base station 110*p* belonging to the same wireless operator enters DAU1 at the DAU1 RF input port 120*n*. Composite signal 135 comprises carriers E-H. The functionality of the DAU 105, and DRU's 125A-125*k*, respectively, are explained in detail in U.S. Provisional Application S.N. 61/374,593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010, incorporated herein by reference and attached hereto as Appendix B.

[0033] One optical output of DAU 105 is fed to DRU 125A, via bidirectional optical cable 140A. A second optical output of DAU 105 is fed via bidirectional optical cable 145A to DRU3. Similarly, bidirectional optical cables 150, 155 and 160 connect DRU's 125A-n in a ring configuration, such that DRU 125A connects to DRU 125B via cable 150A, DRU 125B connects to DRU 125n via cable 150B, and DRU 125*k* connects to DRU 125C, or the *k*th-1 DRU, via cable 150*m*. This connection facilitates networking of DAU 105, which means that all of Carriers A-H are available within DAU 105 to transport data to DRU's 125A-*k* depending on software settings within the networked DAU system. Depending upon the embodiment, the software settings within DRU 125A are configured either manually or automatically, such that carriers A-H are present in the downlink output signal 155A at the antenna port of DRU 125A. The presence of all eight carriers means that DRU 125A is potentially able to access the full capacity of both base stations feeding DAU 105. A possible application for DRU125A is a cafeteria in an

enterprise building during the lunch hour where a large number of wireless subscribers are gathered.

[0034] DRU 125B is fed by a second optical port of DRU 125A via bidirectional optical cable 150A. The optical cable 150A performs the function of daisy chaining DRU 125A with DRU125B. As with DRU 125A, the software settings within DRU 125B are configured either manually or automatically such that Carriers A, C, D and F are present in downlink output signal 155B at the antenna port of DRU 125B. The capacity of DRU 125B is set to a much lower value than DRU 125A by virtue of its specific channel settings as controlled by DAU 105. The individual Digital Remote Units have integrated frequency selective DUCs and DDCs with gain control for each carrier. The DAU's can remotely turn on and off the individual carriers via the gain control parameters.

[0035] In a similar manner as described previously for DRU 125A, the software settings within DRU 125C are configured either manually or automatically such that Carriers B and F are present in downlink output signal 155C at the antenna port of DRU 125C. Compared to the downlink signal 155B at the antenna port of DRU 125B, the capacity of DRU 125C, which is also configured via its software settings, is much less than the capacity of DRU 125B. DRU 125n is fed by the optical cable 150m connected to the second optical port of the nth-1 DRU, shown for simplicity in Figure 1 as DRU 125C. The software settings within DRU 125n are configured either manually or automatically such that carriers A, D, E and H are present in downlink output signal 155D at the antenna port of DRU 125n. Typically, the capacity of DRU 125n is set to a much lower value than DRU 125A, however, the relative capacity settings of each of DRU's 125A-n can be adjusted dynamically to meet the capacity needs within the coverage

zones determined by the physical positions of antennas connected to those DRU's. As noted above, the ring connection is completed by interconnecting DRU 125B and DRU 125n through optical cable 150B. The ring configuration insures that any optical cable breaks will not shut down the daisy chained network. The downlink and uplink signals will be rerouted around the cable break to the respective DRUs.

[0036] The present invention facilitates conversion and transport of several discrete relatively narrow RF bandwidths. This approach allows conversion of only those multiple specific relatively narrow bandwidths which carry useful or specific information. This approach also allows more efficient use of the available optical fiber transport bandwidth for neutral host applications, and allows transport of more individual operators' band segments over the optical fiber. As disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 together with U.S. Provisional Application S.N. 61/382,836, entitled "Remotely Reconfigurable Distributed Antenna System and Methods", filed September 14, 2010, both assigned to the assignee of the present invention, and also referring to Figure 1 of the instant patent application, Digital Up Converters located within the DRU can be dynamically reconfigured as the result of commands from the NOC to transport from the DAU input to any specific DRU output any specific narrow frequency band or bands, RF carriers or RF channels which are available at the respective RF input port of either DAU. This capability is illustrated in Figure 1 where only specific frequency bands or RF carriers appear at the output of a given DRU. More specifically, through commands received from the NOC, the FPGA's in the

DAU and one or more of the associated DRU's can be reprogrammed or reconfigured to convert and transport only the desired narrow bandwidths.

[0037] A related capability of the present invention is that not only can the Digital Up Converters located within each DRU be configured to transport any specific narrow frequency band from the DAU input to any specific DRU output, but also the Digital Up Converters within each DRU can be configured to transport any specific time slot or time slots of each carrier from the DAU input to any specific DRU output. The carriers and time slots are monitored by the DAU by filtering the signals and performing power detection of the individual time slots, which information can be conveyed to the NOC as desired. Then, as with the Digital Up Converters, the Field Programmable Gate Arrays (FPGA) in the DAU or DRU can be dynamically reconfigured by commands received from the NOC in a manner analogous to software programmability. The DAU detects which carriers and corresponding time slots are active. This information is relayed to the individual DRUs via the management control and monitoring protocol software. This information is then used, as appropriate, by the DRUs for turning off and on individual carriers and their corresponding time slots.

[0038] Data transport between the Base Station and the subscribers is typically asymmetrical, whereby the downlink data rate is higher than the uplink rate. The ring network configuration of Daisy Chained DRUs can exploit this data rate asymmetry to maximize the data transport on the optical fibers 150A-150*m*.

[0039] The present invention balances the bidirectional data rate on the optical fibers so as to increase the maximum achievable data rate on the ring network of DRUs. The individual downlink channels are transmitted in a

unidirectional sense along the ring network. Referring to Figure 1, downlink channels A, B, C, and D are transmitted in a clockwise sense around the ring of DRU's 125A-*k*. On the other hand, downlink channels E, F, G and H are transmitted in a counterclockwise sense around the ring of DRU's. Referring to Figure 2, the uplink channels J, K, L and M are transmitted in a counterclockwise sense whereas uplink channels N, O, P and Q are transmitted in a clockwise sense around the ring of DRUs. If the downlink and uplink data rates were the same, there would be no advantage in the transport mechanism. However, if the data transport is asymmetrical between the downlink and uplink then a significant advantage can be gained. For example, for a factor of two difference between the downlink and uplink data rates, a 4/3 factor increase in data transport can be achieved. The larger the asymmetry between the downlink and uplink data rates, the larger will be the increase in data transport using the unidirectional channel transport mechanism around the ring.

[0040] Referring again to Figure 1, a further embodiment in accordance with another aspect of the present invention may be better understood. In the event that there is a significant change in asymmetry between the downlink and uplink data rates and/or if there is a change in channel complement at the BTS, the Management Control module [discussed in connection with Figure 7 herein] which is typically comprised within each DAU is able to automatically and adaptively re-allocate data transport resources on the clockwise direction of the ring and on the counter-clockwise direction of the ring to maximize the overall transport capacity. As stated previously, the larger the degree of asymmetry between uplink and downlink data rates for a particular DAU, the higher the increase in data transport using the

unidirectional channel transport mechanism around the ring. If there is more than one DAU present, in an embodiment one DAU is designated a Master DAU by the NOC, and the Management Control module located in the Master DAU makes decisions to optimize the overall transport capacity. In the event the master DAU fails, the NOC can designate another DAU as master. Alternatively, any suitable failover algorithm can be implemented.

[0041] Referring to Figure 3, an alternative embodiment of the present invention wherein a single DAU controls a plurality of rings, each comprising a plurality of daisy-chained DRU's, can be better understood. In Figure 3, two daisy-chained rings, indicated at 300 and 305, are shown although the number of rings could be greater and is determined mainly as a matter of design preference up to limits imposed by network performance. The rings each link a plurality of DRU's 310A-*n* and 315A-*m*, to a single DAU 320. The directional flow of the data transport is shown as the dashed lines 325 and dotted lines 330. The downlink channels available from the plurality of DRU's are divided into two subsets which flow in opposite directions around the two daisy-chained rings. The uplink channels are transported in a similar fashion. The channels are grouped into the two subsets so as to maximize the data transport to and from the DRUs. The DAU in turn communicates with one or more BTS's via RF Ports 335A-*p*.

[0042] Heuristic algorithms may be used to allocate RF channel data in a Dual-ring DAS. For Figure 3, there are two fibre rings R1, R2 (clockwise and counter clockwise) and a set T of $n \geqslant 2$ independent RF channels K*i*, $1 \leqslant i \leqslant n$ (including uplink and downlink). A channel K*i* requires a bandwidth of b(K*i*) to transport on a fibre ring. A time-bounded algorithm exists which obtains a schedule having the optimal bandwidth allocation (i.e. the maximum

aggregate bandwidth of each ring is as small as possible). A large number of advanced heuristic algorithms have been developed to solve such scheduling optimization problems. Some examples are genetic algorithm, evolutionary algorithm, greedy search, Tabu search, harmony search, simulated annealing, ant colony optimization, etc. For purposes of simplicity and clarity, a simple heuristic algorithm for two rings is described here, although the number of rings is not limited to two.

[0043] The algorithm begins by sorting the channels K*i* decreasingly by bandwidth b(K*i*). Then it schedules the channel in such a way that each channel is assigned to the ring which has the smaller aggregate bandwidth. The formal description of the algorithm follows.

[0044] Input: T = set of *n* independent channels K*i* with required bandwidth b(K*i*), $1 \leqslant i \leqslant n$.

[0045] Output: L_1, L_2 and D_1, D_2. L*j* is the set of channels schedule on ring R*j* , and D_j is the maximum aggregate bandwidth of ring R*j*, D*j* = ($\sum$b(J), JϵL_j), $1 \leqslant j \leqslant 2$.

[0046] ALGORITHM (T, L, D)

[0047] Step 1 (initialize K*i* and D_1, D_2) Sort K*i* such that b(K*i*) $\leqslant$ b(Ki_{+1}), $1 \leqslant i \leqslant n-1$. $D_1 \leftarrow 0$, $D_2 \leftarrow 0$.

[0048] Step 2 (Schedule a channel)

[0049] For *i* =1 to *n,* step 1 do

[0050] If $D_1 \leqslant D_2$, then [assign K*i* onto L_1, $D_1 \leftarrow D_1$ + b(K*i*)] .

[0051] else [assign K*i* onto L_2, $D_2 \leftarrow D_2$ + b(K*i*)] .

[0052] Referring next to Figure 4, a still further an alternative embodiment of the present invention may be understood. The arrangement illustrated in Figure 1 comprised downlink signals from two separate base stations belonging to the same wireless operator entering the DAU 105 at input ports 110A and 110p, respectively. In the embodiment of Figure 4, a first composite signal enters a first DAU 400 at that DAU's RF input port from a base station 405, and a second composite downlink input signal from, e.g., a second base station 410 belonging to a different wireless operator enters DAU 415 at that second DAU's RF input port. DAU 400 directly supports two rings 420 and 425, DAU 415 directly supports two rings 430 and 435, and a ring 440 is shared between DAU 400 and DAU 405. Each of the rings comprises daisy-chained DRU's generally indicated at 445 and connected via, for example, fiber optic links, as discussed in connection with Figure 1. It will be noted that channels A are transported in the opposite sense as channels B. The downlink channels in subset A are transported counterclockwise around each ring, whereas the channels in subset B are transported in a clockwise sense around each ring. In this embodiment, signals belonging to both the first operator and the second operator are converted and transported to the DRU's 445 on ring 440 because DAU 400 and DAU 405 are daisy-chained through the fiber optic cable 440. This embodiment provides an example of a neutral host wireless system, where multiple wireless operators share a common infrastructure comprised of DAU 400, DAU 415, and DRU's 445. All the previously mentioned features and advantages accrue to each of the two wireless operators. It will further be appreciated that, while Figure 4 illustrates only two DAU's linked in daisy-chain style, it is possible to daisy chain a larger plurality of DAU's, and the

daisy-chained DAU's can also be configured in a ring configuration similar to the manner in which the DRU's are connected. This arranged is illustrated in Figure 8, below.

[0053] As disclosed in U.S. Provisional Application S.N. 61/374,593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 and again referring to Figure 1 of the instant patent application, the Digital Up Converters present in the DRU's of the present invention can be programmed to process various signal formats and modulation types including FDMA, CDMA, TDMA, OFDMA and others. Also, the Digital Up Converters present in the respective DRUs can be programmed to operate with signals to be transmitted within various frequency bands subject to the capabilities and limitations of the system architecture disclosed in U.S. Provisional Application S.N. 61/374593, mentioned above. In one embodiment of the present invention where a wideband CDMA signal is present within, e.g., the bandwidth corresponding to a first carrier at the input port to DAU 105, the transmitted signal at the antenna ports of DRU 125A, DRU 125B and DRU*k* will be a wideband CDMA signal which is virtually identical to the signal present within the bandwidth corresponding to that first carrier at the input port to DAU 105.

[0054] As disclosed in U.S. Provisional Application S.N. 61/374,593, again identified above, and also referring to Figure 1 of the instant patent application, it is to be understood that the Digital Up Converters present in the respective DRUs can be programmed to transmit any desired composite signal format to each of the respective DRU antenna ports. As an example, the Digital Up Converters present in DRU 125A and DRU 125B can be dynamically software-reconfigured as described previously so that the signal

present at the antenna port of DRU 125A would correspond to the spectral profile shown in Figure 1 as 155A and also that the signal present at the antenna port of DRU 125B would correspond to the spectral profile shown in Figure 1 as 155B. The application for such a dynamic re-arrangement of DRU capacity would be e.g., if a company meeting were suddenly convened in the area of the enterprise corresponding to the coverage area of DRU 125B.

[0055] Referring again to Figure 2, another embodiment of the Distributed Antenna System of the present invention can be better understood. As disclosed in the aforementioned U.S. Provisional Application S.N. 61/374,593, and also as shown in Figure 2, the optical ring transport mechanism can be implemented with regard to uplink signals. As discussed previously with regard to downlink signals and by referring to Figure 1, the uplink system shown in Figure 2 is mainly comprised of DAU 105, together with DRU's 125A-125k. In a manner similar to the downlink operation explained by referring to Figure 1, the operation of the uplink system shown in Figure 2 can be understood as follows.

[0056] The Digital Down Converters present in each of DRU's 125A-*k* are dynamically software-configured as described previously so that uplink signals of the appropriate desired signal format(s) present at the receive antenna ports of the respective DRU's 125A-125k are selected based on the desired uplink band(s) to be processed and filtered, converted and transported to the appropriate uplink output port of DAU 105. The DAU and DRUs frame the individual data packets corresponding to their respective radio signature using the Common Public Interface Standard (CPRI). Other Interface standards are applicable provided they uniquely identify data

packets with respective DRUs. Header information is transmitted along with the data packet which indentifies the DRU and DAU that corresponds to the individual data packet.

[0057] In one example for the embodiment shown in Figure 2, DRU's 125A and 125C are configured to receive uplink signals within the Channel K bandwidth, whereas DRU 125B and DRU 125*n* are both configured to reject uplink signals within the Channel K bandwidth. When DRU 125C receives a strong enough signal at its receive antenna port within the Channel K bandwidth to be properly filtered and processed, the Digital Down Converters within DRU 125C facilitate processing and conversion. Similarly, when DRU 125A receives a strong enough signal at its receive antenna port within the Channel K bandwidth to be properly filtered and processed, the Digital Down Converters within DRU 125A facilitate processing and conversion. The signals from DRU 125A and DRU 125C are combined based on the active signal combining algorithm, and are fed to the base station connected to the uplink output port of DAU 105. The term simulcast is frequently used to describe the operation of DRU125A and DRU 125C with regard to uplink and downlink signals within Channel K bandwidth. The term Flexible Simulcast refers to the fact that the present invention supports dynamic and/or manual rearrangement of which specific DRU are involved in the signal combining process for each Channel bandwidth.

[0058] Referring still to Figure 2, the Digital Down Converters present in DRU 125A are configured to receive and process signals within Channel J-Q bandwidths. The Digital Down Converters present in DRU 125B are configured to receive and process signals within Channel J, L, M and O bandwidths. The Digital Down Converters present in DRU 125C are

configured to receive and process signals within Channel K and O bandwidths. The Digital Down Converters present in DRU 125*n* are configured to receive and process signals within Channel J, M, N and Q bandwidths. The respective high-speed digital signals resulting from processing performed within each of the four DRU are routed to the DAU. As described previously, the uplink signals from the four DRUs are combined within the respective DAU corresponding to each base station.

[0059] In summary, the Reconfigurable Distributed Antenna System of the present invention described herein efficiently conserves resources and reduces costs. The reconfigurable system is adaptive or manually field-programmable, since the algorithms can be adjusted like software in the digital processor at any time.

[0060] Referring next to Figure 5, a alternative embodiment of the present invention may be better understood. Each DRU has a coverage radius that can be adjusted based on the power transmission from that particular remote unit. The DAU controls the various DRU's transmission power and can optimize the overall coverage zone. In the illustrated embodiment, DAU 502, again under the control of a NOC (not shown), is associated with a base station 501 and in turn interfaces with three DRU's 503, 504 and 505. A user 506 with a mobile device is provided relatively uniform coverage throughout the area covered by the three DRU's.

[0061] Referring next to Figure 6, a still further alternative embodiment may be better appreciated. The input frequency bands 605-630 (here denoted as six frequency bands at 700, 800, 850, 1900, 2100 and 2600 MHz) are input into the DAU 600 from the BTS's (not shown). The DAU includes, among other functionalities discussed herein, an RF IN portion for each band, and a

digital distribution matrix for distributing the frequency bands to a plurality of DRU's, indicated as DRU1-DRU60, daisy-chained along three separate rings 635, 640 and 645 for achieving the desired coverage. The frequency bands are transported to either all or a subset of DRUs. The particular number of frequency bands, DAU's, DRU's and rings is exemplary only, and can, in practice, be any number appropriate to the performance capabilities and needs of the network.

[0062] Referring next to Figure 7, the software embedded in the DAU and DRU, which controls the operation of keys functions of these devices, can be better understood. In particular, the DAU embedded software control module 700 comprises a DAU Management Control Module 705 and a DAU monitoring module 710. The DAU Management Control Module 705 communicates with the NOC 715, and also the DAU monitoring module 710. One such key function is determining and/or setting the appropriate amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular DRU or group of DRUs to meet desired capacity and throughput objectives. As noted previously, the NOC 715 monitors the DAS operation and sends commands to the DAU's for configuring various functions of the DRU's as well as the DAU, in at least some embodiments.

[0063] The DAU Monitoring module, in addition to other functions, detects which carriers and corresponding time slots are active for each DRU. The DAU Management Control module communicates with the DRU Embedded Software Control module 720 over a fiber optic link control channel via a control protocol. In an embodiment, the control protocol comprises headers together with packets of data, such that both control information and data are transmitted to the DRU's together as a message. DRU functions or features

that the header would control in the DRU are typically implementation specific and can include, among other things, measuring uplink and downlink power, measuring gain of uplink and downlink, and monitoring alarms in the DRU.

[0064] In turn, the DRU Management Control module 725 within the DRU Embedded Software Control Module sets the individual parameters of all the DRU Digital Up-Converters 730 to enable or disable specific radio resources from being transmitted by a particular DRU or group of DRUs, and also sets the individual parameters of all the DRU Digital Down-Converters 735 to enable or disable specific radio resources from being transmitted by a particular DRU or group of DRUs. In addition, the DRU Embedded Software Control Module comprises a DRU Pilot Beacon Control Module 740, which communicates with a DRU Pilot Beacon 745.

[0065] Referring next to Figure 8, an embodiment of a daisy-chained configuration of DAU's is illustrated, together with a daisy-chained configuration of DRU's. In an embodiment, a plurality of base stations 800A-800*n* are each associated with one of DAU's 805A-*n*. The DAU's are daisy-chained, and each DAU communicates with one or more daisy-chains 810A-810*m* of DRU's which may or may not be arranged in a ring configuration. It will be appreciated that the DAU's can also be configured in a ring configuration, as discussed above.

[0066] An algorithm operating within the DAU Monitoring module which detects which carriers and corresponding time slots for each carrier are active for each DRU provides information to the DAU Management Control module to help identify when, e.g., a particular downlink carrier is loaded by a percentage greater than a predetermined threshold whose value is

communicated to the DAU Management Control module by the DAU's Remote Monitoring and Control function 715. If that occurs, the DAU Management Control module can adaptively modify the system configuration to begin to deploy, typically although not necessarily slowly, additional radio resources (such as RF carriers, CDMA codes or TDMA time slots) for use by a particular DRU which need those radio resources within its coverage area. At the same time, usually the DAU Management Control module adaptively modifies the system configuration to begin to remove, again typically slowly, certain radio resources (such as RF carriers, CDMA codes or TDMA time slots) for use by a particular DRU where that DRU no longer needs those radio resources within its coverage area.

[0067] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

What is Claimed is: [TBD]

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ABSTRACT

The present disclosure is a novel utility of a software defined radio (SDR) based Distributed Antenna System (DAS) that is field reconfigurable and support multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands and multi-channels. More specifically, the present invention relates to a DAS utilizing one or more Daisy-Chained Rings of Remote Units. The present invention enables a high degree of flexibility to manage, control, enhance, facilitate the usage and performance of a distributed wireless network such as Flexible Simulcast, automatic traffic load-balancing, network and radio resource optimization, network calibration, autonomous/assisted commissioning, carrier pooling, automatic frequency selection, frequency carrier placement, traffic monitoring, traffic tagging, pilot beacon, etc. As a result, a DAS in accordance with the present invention can increase the efficiency and traffic capacity of the operators' wireless network.

APPENDIX I

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
BTS	Base Transceiver System or Base Station
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DAU	Digital Access Unit
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration

EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
PN	Pseudo-Noise
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRH	Remote Radio Head
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System

UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

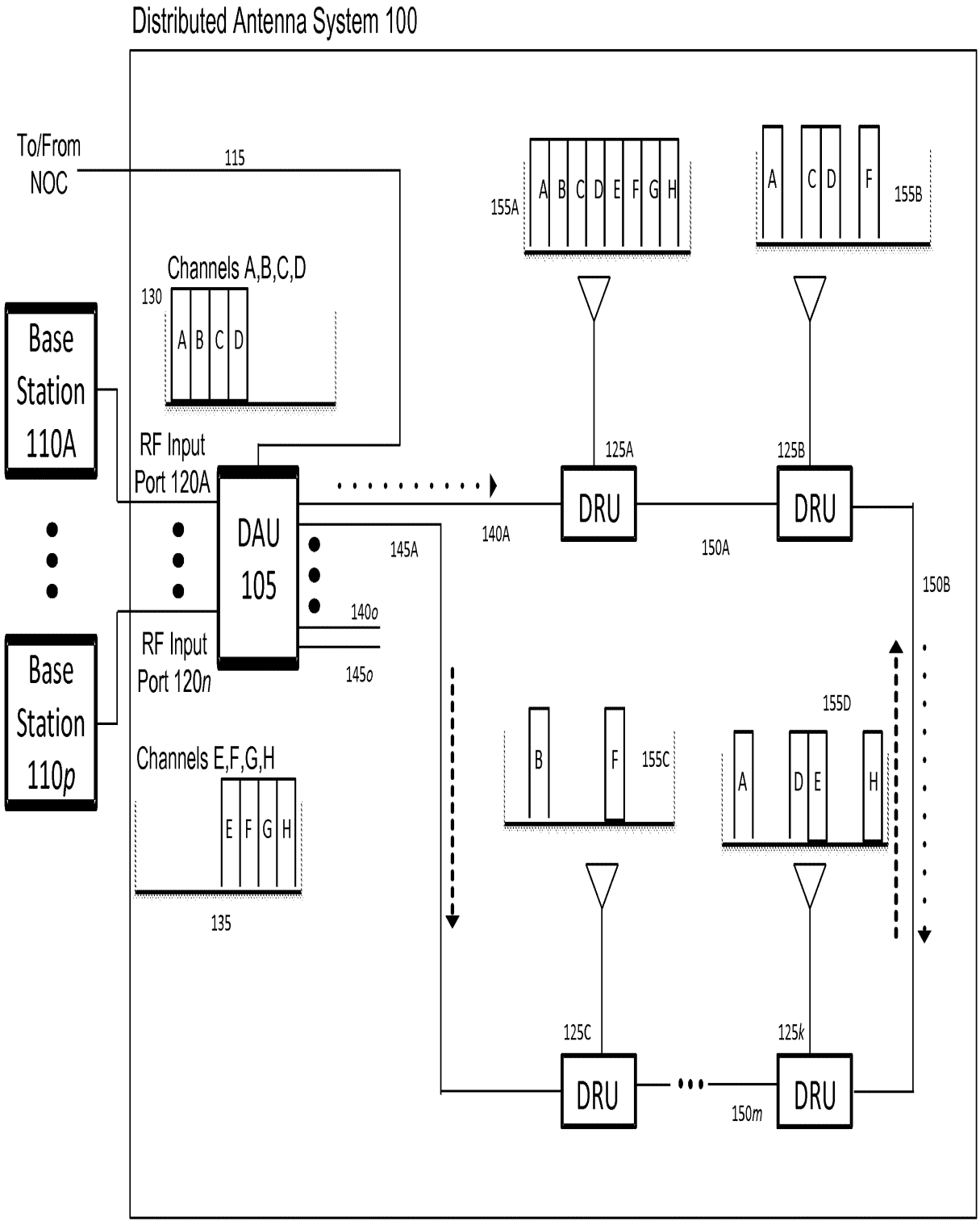


Figure 1: Example of Uni-directional Channels for Downlink

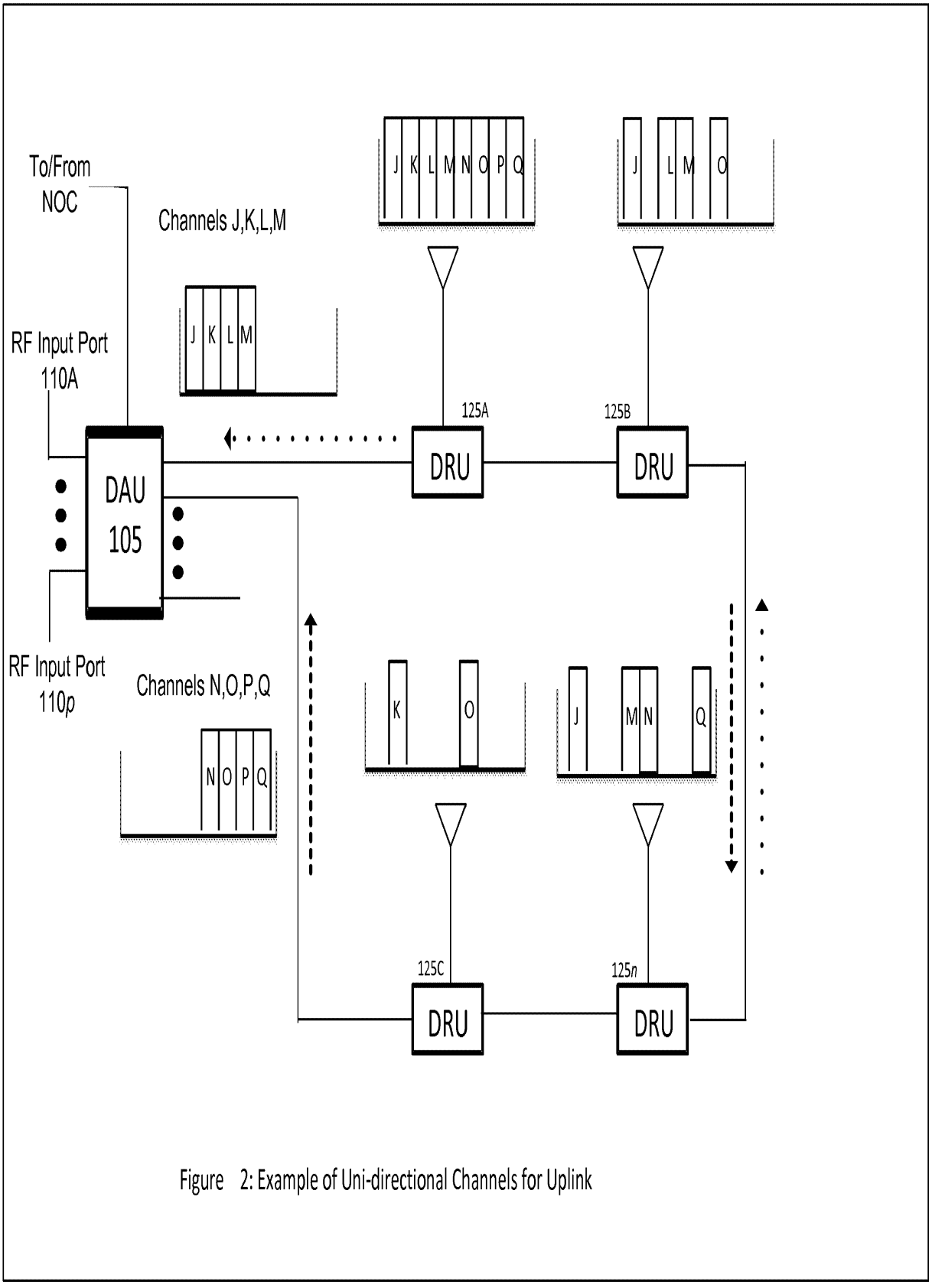


Figure 2: Example of Uni-directional Channels for Uplink

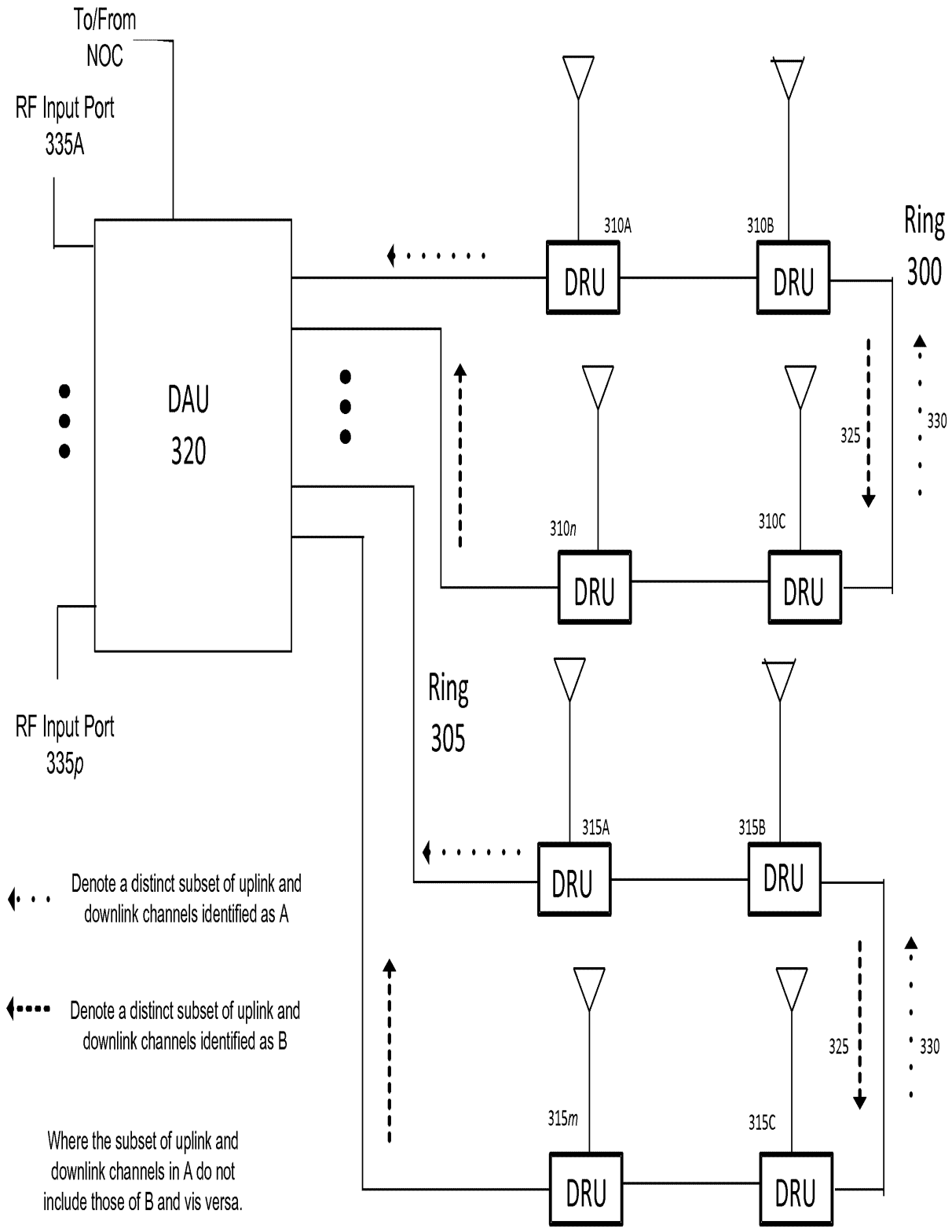


Figure 3: Example of Daisy Chain Ring Network for Uplink

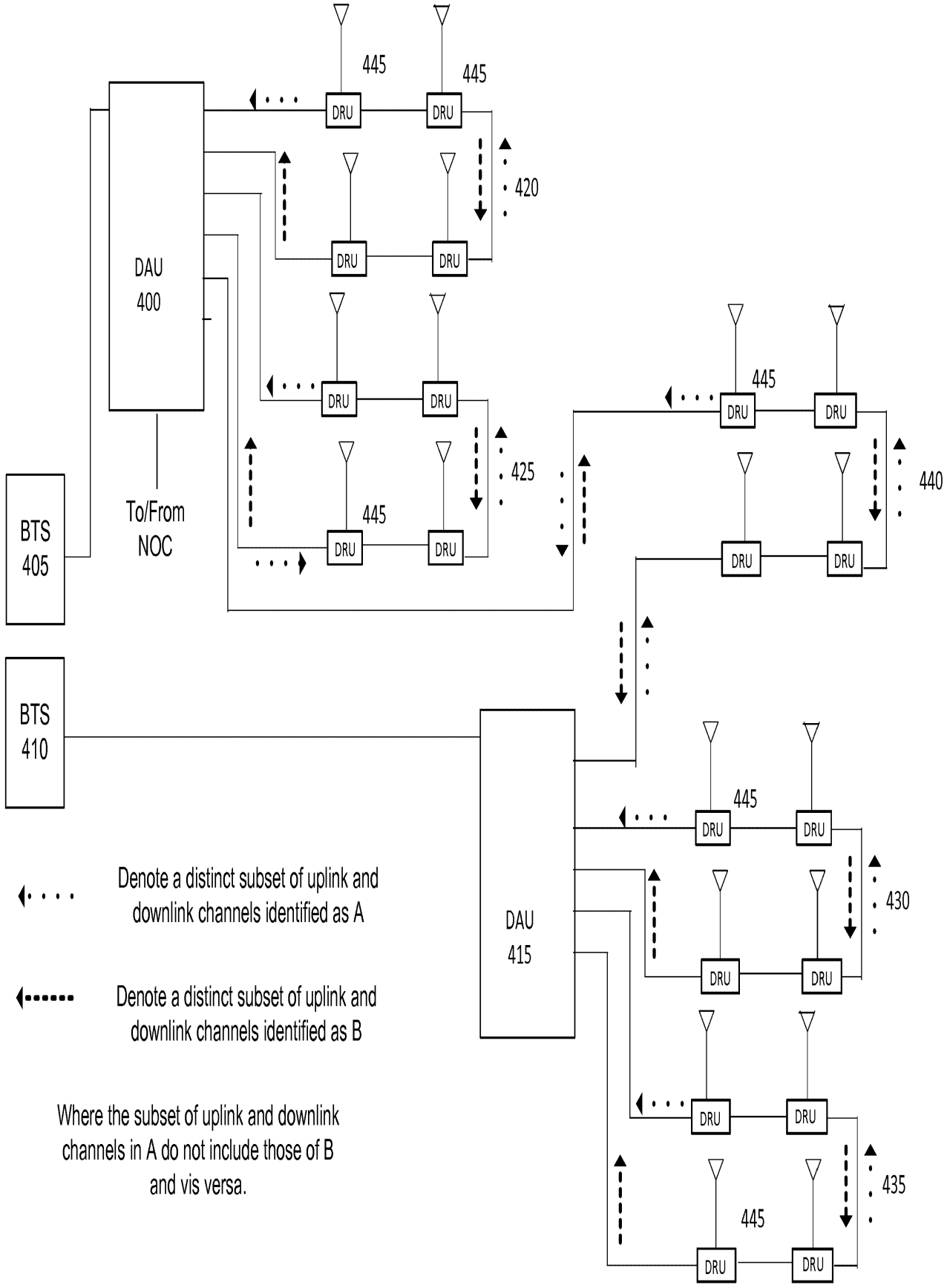


Figure 4: Example of Daisy Chain Ring Network for Uplink or Downlink

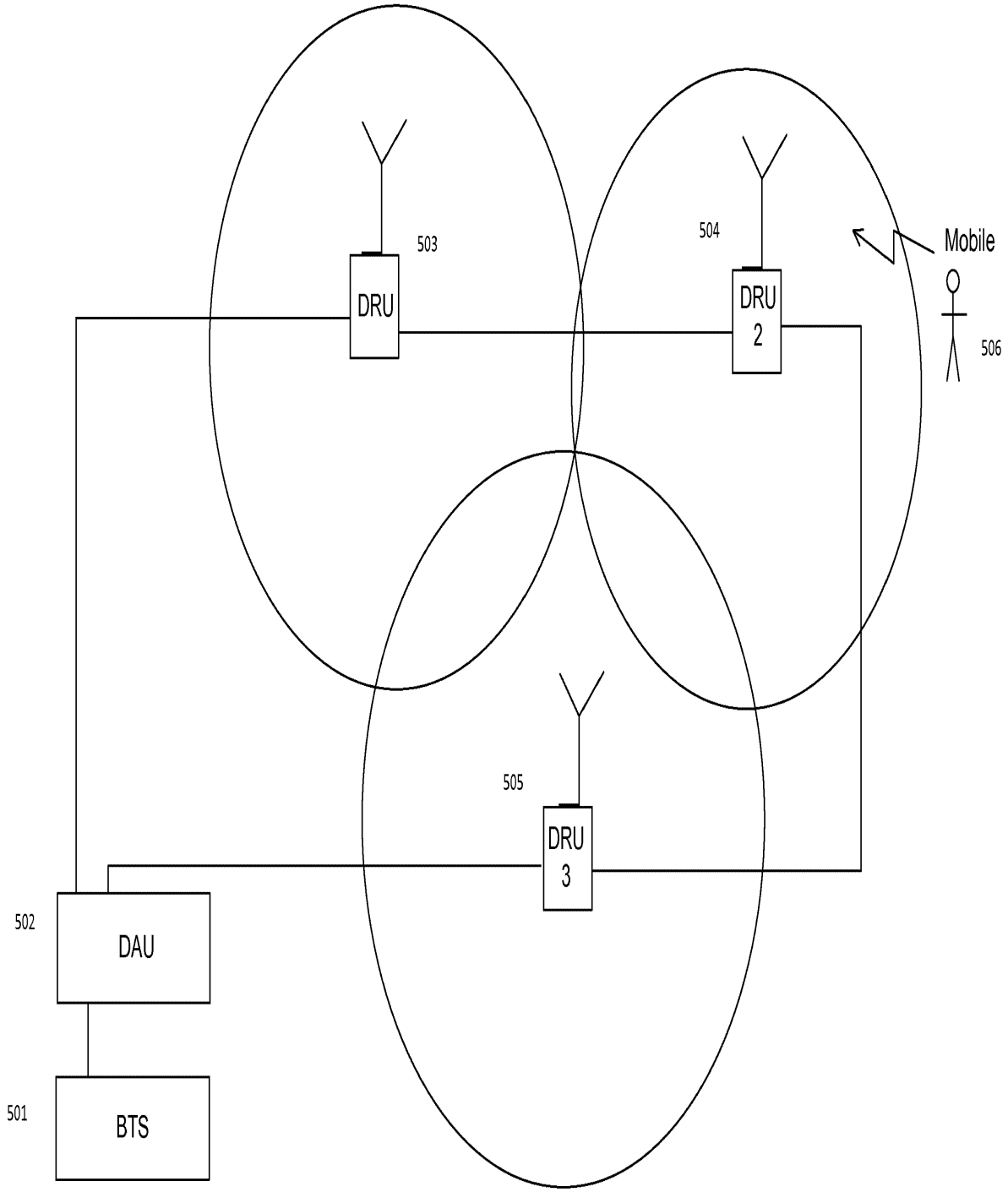


Figure 5 Daisy Chain Example of DAS

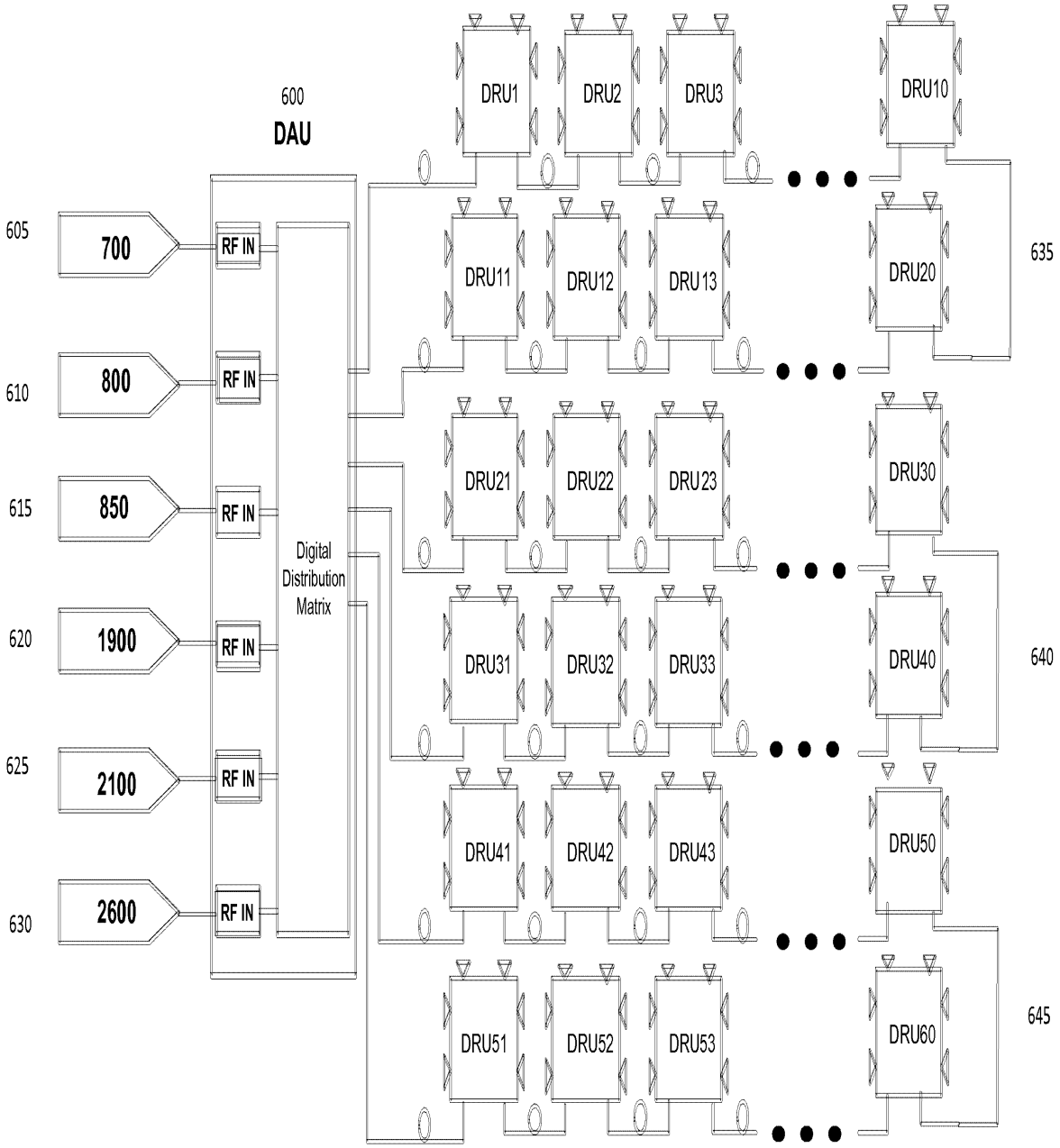


Figure 6. An embodiment of a multi-band system illustrating one DAU supporting up to six different services operating at different frequency bands, with three optical rings of DRU's 1-60.

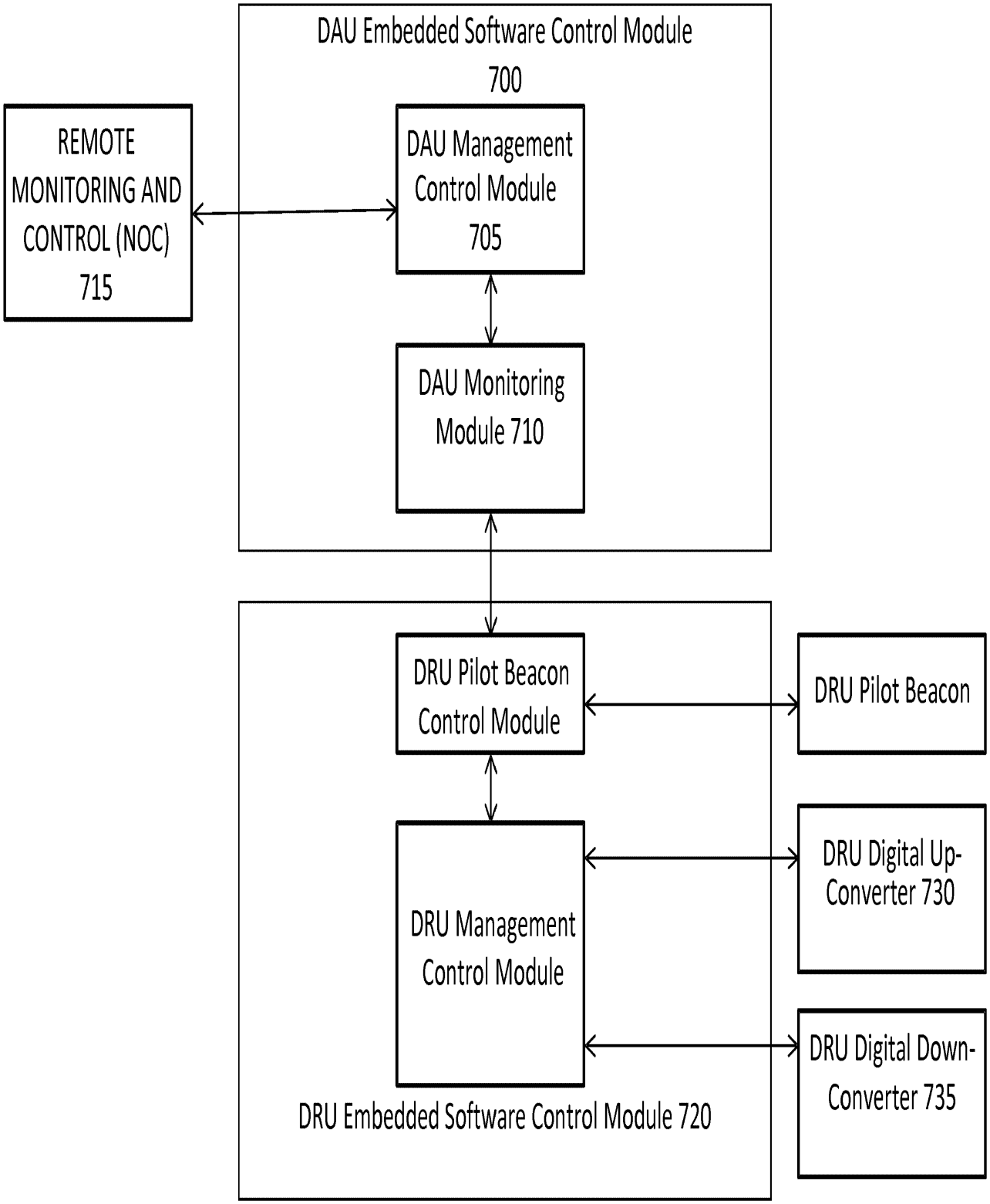


Figure 7: Embedded Software Control Modules

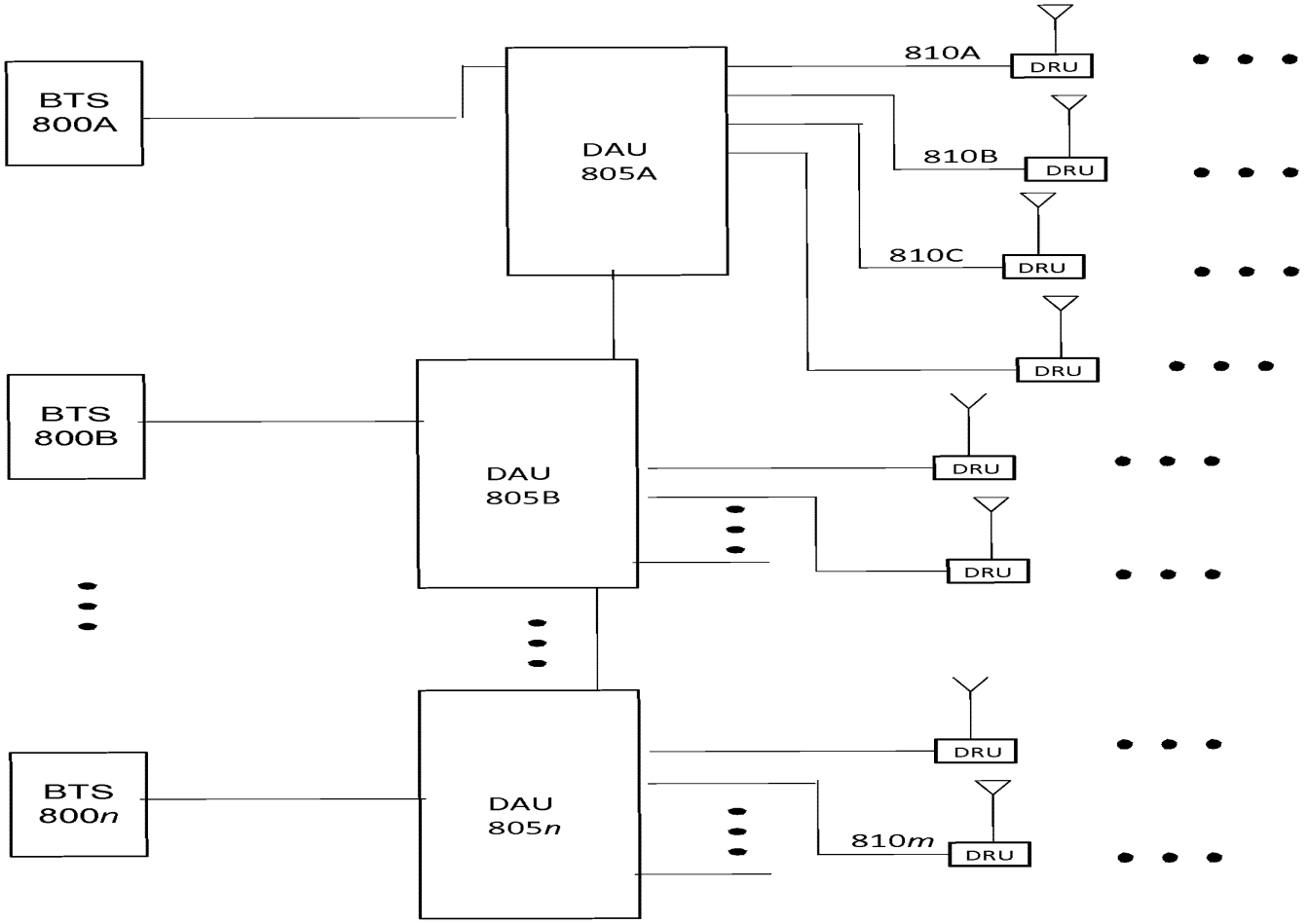


Figure 8 Daisy Chained DAUs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

REMOTELY RECONFIGURABLE DISTRIBUTED ANTENNA SYSTEM AND METHODS

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SPECIFICATION

RELATED APPLICATIONS

[001] This is a continuation-in-part and claims the benefit of U.S. patent application S.N. 12/767,669, entitled "Remotely Reconfigurable Power Amplifier System and Method," filed April 26, 2010, and through its U.S. Pat. Appn. S.N.

US61/172,642, filed on April 24, 2009, and further claims the benefit of U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010, all of which are hereby incorporated by reference in their entirety for all purposes, and attached hereto as Appendices.

FIELD OF THE INVENTION

[002] The present invention generally relates to wireless communication systems employing Distributed Antenna Systems (DAS) as part of a distributed wireless network. More specifically, the present invention relates to a DAS utilizing software defined radio (SDR).

BACKGROUND OF THE INVENTION

[003] Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users requires end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. One of the most difficult challenges faced by network operators is caused by the physical movement of subscribers from one location to another, and particularly when wireless subscribers congregate in large numbers at one location. A notable example is a business enterprise facility during lunchtime, when a large number of wireless subscribers visit a cafeteria location in the building. At that time, a large number of subscribers have moved away from their offices and usual work areas. It's likely that during lunchtime there are many locations throughout the

facility where there are very few subscribers. If the indoor wireless network resources were properly sized during the design process for subscriber loading as it is during normal working hours when subscribers are in their normal work areas, it is very likely that the lunchtime scenario will present some unexpected challenges with regard to available wireless capacity and data throughput.

[004] To accommodate this variation in subscriber loading, there are several candidate prior art approaches.

[005] One approach is to deploy many low-power high-capacity base stations throughout the facility. The quantity of base stations is determined based on the coverage of each base station and the total space to be covered. Each of these base stations is provisioned with enough radio resources, i.e., capacity and broadband data throughput to accommodate the maximum subscriber loading which occurs during the course of the workday and work week. Although this approach typically yields a high quality of service, the notable disadvantage of this approach is that during a major part of the time many of the base stations' capacity is being wasted. Since a typical indoor wireless network deployment involves capital and operational costs which are assessed on a per-subscriber basis for each base station, the typically high total life cycle cost for a given enterprise facility is far from optimal.

[006] A second candidate approach involves deployment of a DAS along with a centralized group of base stations dedicated to the DAS. A conventional DAS deployment falls into one of two categories. The first type of DAS is "fixed", where the system configuration doesn't change based on time of day or other information about usage. The remote units associated with the DAS are set up during the design process so that a particular block of base station radio resources is thought to be enough to serve each small group of DAS remote

units. A notable disadvantage of this approach is that most enterprises seem to undergo frequent re-arrangements and re-organizations of various groups within the enterprise. Therefore, it's highly likely that the initial setup will need to be changed from time to time, requiring deployment of additional staff and contract resources with appropriate levels of expertise regarding wireless networks.

[007] The second type of DAS is equipped with a type of network switch which allows the location and quantity of DAS remote units associated with any particular centralized base station to be changed manually. Although this approach would seem to allow dynamic reconfiguration based on the needs of the enterprise or based on time of day, it frequently requires deployment of additional staff resources for real-time management of the network. Another issue is that it's not always correct or best to make the same DAS remote unit configuration changes back and forth on each day of the week at the same times of day. Frequently it is difficult or impractical for an enterprise IT manager to monitor the subscriber loading on each base station. And it is almost certain that the enterprise IT manager has no practical way to determine the loading at a given time of day for each DAS remote unit; they can only guess.

[008] Another major limitation of prior art DAS deployments is related to their installation, commissioning and optimization process. Some challenging issues which must be overcome include selecting remote unit antenna locations to ensure proper coverage while minimizing downlink interference from outdoor macro cell sites, minimizing uplink interference to outdoor macro cell sites, and ensuring proper intra-system handovers while indoors and while moving from outdoors to indoors (and vice-versa). The process of performing such deployment optimization is frequently characterized as trial-and-error and as such, the results may not be consistent with a high quality of service.

[009] A major limitation of prior art DAS equipment employing digital transmission links such as optical fiber or wired Ethernet is the fact that the prior-art RF-to-digital conversion techniques utilize an approach whereby the system converts a single broad RF bandwidth of e.g., 10 to 25 MHz to digital. Therefore all the signals, whether weak or strong, desired or undesired, contained within that broad bandwidth are converted to digital, whether those signals are desired or not. This approach frequently leads to inefficiencies within the DAS which limit the DAS network capacity. It would be preferable to employ an alternative approach yielding greater efficiencies and improved flexibility, particularly for neutral host applications.

[0010] In 2008 the FCC further clarified its E-911 requirements with regard to Phase 2 accuracy for mobile wireless networks. The information required in Phase 2 is the mobile phone number and the physical location, within a few dozen yards, from which the call was made. The Canadian government is reportedly considering enacting similar requirements. Also the FCC is eager to see US mobile network operators provide positioning services with enhanced accuracy for E-911 for indoor subscribers. There is a reported effort within the FCC to try to mandate Phase 2 accuracy indoors, within the next 2 years.

[0011] Many wireless networks employ mobile and fixed broadband wireless terminals which employ GPS-based E-911 location services. It has been demonstrated that GPS signals from satellites outdoors don't propagate well into the indoor space. Therefore an alternative, more robust E-911 location determination approach is required for indoors, particularly if the FCC requirements are changed to be more stringent.

[0012] Several US operators have expressed concern about how they can practically and cost-effectively obtain these enhanced location accuracy capabilities. Operators are very eager to identify a cost-effective approach which can be deployed indoors for enhanced location accuracy.

[0013] One proposed approach toward indoor location accuracy enhancement for CDMA networks would employ a separate unit known as a CDMA Pilot Beacon. A notable disadvantage of this approach for an indoor DAS application is that since the CDMA Pilot Beacon unit is a separate and dedicated device and not integrated within the DAS, it would likely be costly to deploy. The Pilot Beacon approach for CDMA networks employs a Pilot Beacon with a unique PN code (in that area) which effectively divides a particular CDMA network coverage area (e.g., indoors) into multiple small zones (which each correspond to the coverage area of a low-power Pilot Beacon). Each Pilot Beacon's location, PN code and RF Power level are known by the network. Each Pilot Beacon must be synchronized to the CDMA network, via GPS or local base station connection. A variable delay setting permits each Pilot Beacon to have the appropriate system timing to permit triangulation and/or Cell ID position determination. One optional but potentially costly enhancement to this approach would employ a Wireless Modem for each Pilot Beacon to provide remote Alarms, Control and Monitoring of each CDMA Pilot Beacon. No known solution for indoor location accuracy enhancement has been publicly proposed for WCDMA networks.

[0014] One candidate technically-proven approach toward indoor location accuracy enhancement for GSM networks would employ a separate unit known as a Location Measurement Unit or LMU. A notable disadvantage of this approach for an indoor DAS application is that, since the LMU is a separate and

dedicated device and not integrated within the DAS, it is costly to deploy. Each LMU requires a backhaul facility to a central server which analyzes the LMU measurements. The LMU backhaul cost adds to the total cost of deploying the enhanced accuracy E-911 solution for GSM networks. Despite the availability of the already technically-proven LMU approach, it has not been widely deployed in conjunction with indoor DAS.

[0015] Based on the prior art approaches described herein, it is apparent that a highly efficient, easily deployed and dynamically reconfigurable wireless network is not achievable with prior art systems and capabilities.

SUMMARY OF THE INVENTION

[0016] The present invention substantially overcomes the limitations of the prior art discussed above. The advanced system architecture of the present invention provides a high degree of flexibility to manage, control, enhance and facilitate radio resource efficiency, usage and overall performance of the distributed wireless network. This advanced system architecture enables specialized applications and enhancements including flexible simulcast, automatic traffic load-balancing, network and radio resource optimization, network calibration, autonomous/assisted commissioning, carrier pooling, automatic frequency selection, radio frequency carrier placement, traffic monitoring, traffic tagging, and indoor location determination using pilot beacons. The present invention can also serve multiple operators, multi-mode radios (modulation-independent) and multi-frequency bands per operator to increase the efficiency and traffic capacity of the operators' wireless networks.

[0017] Accordingly, it is an object of the present invention to provide a capability for Flexible Simulcast. With Flexible Simulcast, the amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular RRU or group of RRUs by each RRU Access Module can be set via software control as described hereinafter to meet desired capacity and throughput objectives or wireless subscriber needs. To achieve these and other objects, an aspect of the present invention employs software-programmable frequency selective Digital Up-Converters (DUCs) and Digital Down-Converters (DDCs). A software-defined Remote Radio Head architecture is used for cost-effective optimization of the radio performance. Frequency selective DDCs and DUCs at the Remote Radio Head enable a high signal to noise ratio (SNR) which maximize the throughput data rate. An embodiment shown in Figure 1 depicts abasic structure and provides an example of a Flexible Simulcast downlink transport scenario. Figure 2 depicts an embodiment of a basic structure of a Flexible Simulcast uplink transport scenario.

[0018] It is a further object of the present invention to facilitate conversion and transport of several discrete relatively narrow RF bandwidths. In another aspect of the invention, an embodiment converts only that plurality of specific, relatively narrow bandwidths that carry useful information. Thus, this aspect of the present invention allows more efficient use of the available optical fiber transport bandwidth for neutral host applications, and facilitates transport of more operators' band segments over the optical fiber. To achieve the above result, the present invention utilizes frequency-selective filtering at the Remote Radio Head which enhances the system performance. In some embodiments of this aspect of the invention, noise reduction via frequency- selective filtering at the Remote Radio Head is utilized for maximizing the SNR and consequently

maximizing the data throughput. It is a further object of the present invention to provide CDMA and WCDMA indoor location accuracy enhancement. In an aspect of the present invention, an embodiment provides enhanced location accuracy performance by employing pilot beacons. Figure 3 depicts a typical indoor system employing multiple Remote Radio Head Units (RRUs) and a central Digital Access Unit (DAU). The Remote Radio Heads have a unique beacon that is distinct and identifies that particular indoor cell. The mobile user will use the beacon information to assist in the localization to a particular cell. .

[0019] It is a further object of the present invention to enhance GSM and LTE indoor location accuracy.. In another aspect, an embodiment of the present invention provides localization of a user based on the radio signature of the mobile device. Figure 4 depicts a typical indoor system employing multiple Remote Radio Head Units (RRUs) and a central Digital Access Unit (DAU). In accordance with the invention, each Remote Radio Head provides unique header information on data received by that Remote Radio Head. The system of the invention uses this header information in conjunction with the mobile user's radio signature to localize the user to a particular cell.

It is a further object of the present invention to re-route local traffic to Internet VOIP, Wi-Fi or WiMAX. In this aspect of the invention, an embodiment determines the radio signatures of the individual users within a DAU or Island of DAUs and uses this information to identify if the users are located within the coverage area associated with a specific DAU or Island of DAUs. The DAUs track the radio signatures of all the active users within its network and record a running data base containing information pertaining to them. One embodiment of the present invention is for the Network Operations Center (NOC) to inform the DAU that, e.g., two specific users are collocated within the same DAU or Island

of DAUs, as depicted in Figure 6. The DAUs then reroute the users to Internet VOIP, Wi-Fi or WiMAX as appropriate. Another embodiment of the present invention is to determine the Internet Protocol (IP) addresses of the individual users' Wi-Fi connections. If the individual users' IP addresses are within the same DAU or Island of DAUs, the data call for these users is rerouted over the internal network.

[0020] Applications of the present invention are suitable to be employed with distributed base stations, distributed antenna systems, distributed repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

[0021] Appendix I is a glossary of terms used herein, including acronyms.

THE FIGURES

[0022] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0023] Figure 1 is a block diagram according to one embodiment of the invention showing the basic structure and an example of a Flexible Simulcast downlink transport scenario based on having 2 DAU and 4 DRU.

[0024] Figure 2 is a block diagram in accordance with an embodiment of the invention showing the basic structure and an example of a Flexible Simulcast uplink transport scenario based on having 2 DAU and 4 DRU.

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[0025] Figure 3 shows an embodiment of an indoor system employing multiple Remote Radio Head Units (RRUs) and a central Digital Access Unit (DAU).

[0026] Figure 4 shows an embodiment of an indoor system in accordance with the invention which employs multiple Remote Radio Head Units (RRUs) and a central Digital Access Unit (DAU).

[0027] Figure 5 illustrates an embodiment of a cellular network system employing multiple Remote Radio Heads according to the present invention.

[0028] Figure 6 is a depiction of local connectivity according to one embodiment of the present invention.

[0029] Figure 7 illustrates an embodiment of the basic structure of the embedded software control modules which manage key functions of the DAU and RRU, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

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[0030] The present invention is a novel Reconfigurable Distributed Antenna System that provides a high degree of flexibility to manage, control, re-configure, enhance and facilitate the radio resource efficiency, usage and overall performance of the distributed wireless network. An embodiment of the Reconfigurable Distributed Antenna System in accordance with the present invention is shown in Figure 1. The Flexible Simulcast System 100 can be used to explain the operation of Flexible Simulcast with regard to downlink signals. The system employs a Digital Access Unit functionality (hereinafter “DAU”). The DAU serves as an interface to the base station (BTS). The DAU is (at one

end) connected to the BTS, and on the other side connected to multiple RRUs. For the downlink (DL) path, RF signals received from the BTS are separately down-converted, digitized, and converted to baseband (using a Digital Down-Converter). Data streams are then I/Q mapped and framed. Specific parallel data streams are then independently serialized and translated to optical signals using pluggable SFP modules, and delivered to different RRUs over optical fiber cable. For the uplink (UL) path optical signals received from RRUs are de-serialized, deframed, and up-converted digitally using a Digital Up-Converter. Data streams are then independently converted to the analog domain and up-converted to the appropriate RF frequency band. The RF signal is then delivered to the BTS. An embodiment of the system is mainly comprised of DAU1 indicated at 101, RRU1 indicated at 103, RRU2 indicated at 104, DAU2 indicated at 102, RRU3 indicated at 105, and RRU4 indicated at 106. A composite downlink input signal 107 from, e.g., a base station belonging to one wireless operator enters DAU1 at the DAU1 RF input port. Composite signal 107 is comprised of Carriers 1-4. A second composite downlink input signal from e.g., a second base station belonging to the same wireless operator enters DAU2 at the DAU2 RF input port. Composite signal 108 is comprised of Carriers 5-8. The functionality of DAU1, DAU2, RRU1, RRU2, RRU3 and RRU4 are explained in detail by U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 and attached hereto as an appendix. One optical output of DAU1 is fed to RRU1. A second optical output of DAU1 is fed via bidirectional optical cable 113 to DAU2. This connection facilitates networking of DAU1 and DAU2, which means that all of Carriers 1-8 are available within DAU1 and DAU2 to transport to RRU1, RRU2, RRU3 and RRU4 depending on software settings within the networked DAU system comprised of DAU1 and DAU2. The software settings

within RRU1 are configured either manually or automatically such that Carriers 1-8 are present in the downlink output signal 109 at the antenna port of RRU1. The presence of all 8 carriers means that RRU1 is potentially able to access the full capacity of both base stations feeding DAU1 and DAU2. A possible application for RRU1 is in a wireless distribution system is e.g., a cafeteria in an enterprise building during the lunch hour where a large number of wireless subscribers are gathered. RRU2 is fed by a second optical port of RRU1 via bidirectional optical cable 114 to RRU2. Optical cable 114 performs the function of daisy chaining RRU2 with RRU1. The software settings within RRU2 are configured either manually or automatically such that Carriers 1, 3, 4 and 6 are present in downlink output signal 110 at the antenna port of RRU2. The capacity of RRU2 is set to a much lower value than RRU1 by virtue of its specific Digital Up Converter settings. The individual Remote Radio Units have integrated frequency selective DUCs and DDCs with gain control for each carrier. The DAUs can remotely turn on and off the individual carriers via the gain control parameters.

[0031] In a similar manner as described previously for RRU1, the software settings within RRU3 are configured either manually or automatically such that Carriers 2 and 6 are present in downlink output signal 111 at the antenna port of RRU3. Compared to the downlink signal 110 at the antenna port of RRU2, the capacity of RRU3 which is configured via the software settings of RRU3 is much less than the capacity of RRU2. RRU4 is fed by a second optical port of RRU3 via bidirectional optical cable 115 to RRU4. Optical cable 115 performs the function of daisy chaining RRU4 with RRU3. The software settings within RRU4 are configured either manually or automatically such that Carriers 1, 4, 5 and 8 are present in downlink output signal 112 at the antenna port of RRU4. The

capacity of RRU4 is set to a much lower value than RRU1. The relative capacity settings of RRU1, RRU2, RRU3 and RRU4 and can be adjusted dynamically as discussed in connection with Figure 7 to meet the capacity needs within the coverage zones determined by the physical positions of antennas connected to RRU1, RRU2, RRU3 and RRU4 respectively.

[0032] The present invention facilitates conversion and transport of several discrete relatively narrow RF bandwidths. This approach allows conversion of only those multiple specific relatively narrow bandwidths which carry useful or specific information. This approach also allows more efficient use of the available optical fiber transport bandwidth for neutral host applications, and allows transport of more individual operators' band segments over the optical fiber. As disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 and also referring to Figure 1 of the instant patent application, Digital Up Converters located within the RRU which are dynamically software-programmable as discussed hereinafter can be re-configured to transport from the DAU input to any specific RRU output any specific narrow frequency band or bands, RF carriers or RF channels which are available at the respective RF input port of either DAU. This capability is illustrated in Figure 1 where only specific frequency bands or RF carriers appear at the output of a given RRU.

[0033] A related capability of the present invention is that not only can the Digital Up Converters located within each RRU be configured to transport any specific narrow frequency band from the DAU input to any specific RRU output, but also the Digital Up Converters within each RRU can be configured to transport any specific time slot or time slots of each carrier from the DAU input to

any specific RRU output. The DAU detects which carriers and corresponding time slots are active. This information is relayed to the individual RRUs via the management control and monitoring protocol software discussed hereinafter. This information is then used, as appropriate, by the RRUs for turning off and on individual carriers and their corresponding time slots.

[0034] Referring to Figure 1 of the instant patent application, an alternative embodiment of the present invention may be described as follows. In a previous description of Figure 1, a previous embodiment involved having downlink signals from two separate base stations belonging to the same wireless operator enter DAU1 and DAU2 input ports respectively. In an alternative embodiment, a second composite downlink input signal from e.g., a second base station belonging to a different wireless operator enters DAU2 at the DAU2 RF input port. In this embodiment, signals belonging to both the first operator and the second operator are converted and transported to RRU1, RRU2, RRU3 and RRU4 respectively. This embodiment provides an example of a neutral host wireless system, where multiple wireless operators share a common infrastructure comprised of DAU1, DAU2, RRU1, RRU2, RRU3 and RRU4. All the previously mentioned features and advantages accrue to each of the two wireless operators.

[0035] As disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 and also referring to Figure 1 of the instant patent application, the Digital Up Converters present in the RRU can be programmed to process various signal formats and modulation types including FDMA, CDMA, TDMA, OFDMA and others. Also, the Digital Up Converters present in the respective RRUs can be programmed to operate with signals to be transmitted within various

frequency bands subject to the capabilities and limitations of the system architecture disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010. In one embodiment of the present invention where a wideband CDMA signal is present within e.g., the bandwidth corresponding to carrier 1 at the input port to DAU1, the transmitted signal at the antenna ports of RRU1, RRU2 and RRU4 will be a wideband CDMA signal which is virtually identical to the signal present within the bandwidth corresponding to carrier 1 at the input port to DAU1.

[0036] As disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a Distributed Antenna System," filed August 17, 2010 and also referring to Figure 1 of the instant patent application, it is understood that the Digital Up Converters present in the respective RRUs can be programmed to transmit any desired composite signal format to each of the respective RRU antenna ports. As an example, the Digital Up Converters present in RRU1 and RRU2 can be dynamically software-reconfigured as described previously so that the signal present at the antenna port of RRU1 would correspond to the spectral profile shown in Figure 1 as 110, and also that the signal present at the antenna port of RRU2 would correspond to the spectral profile shown in Figure 1 as 109. The application for such a dynamic re-arrangement of RRU capacity would be e.g., if a company meeting were suddenly convened in the area of the enterprise corresponding to the coverage area of RRU2. []

[0037] Another embodiment of the Distributed Antenna System in accordance with the present invention is shown in Figure 2. As disclosed in U.S. Provisional Application S.N. 61/374593, entitled "Neutral Host Architecture for a

Distributed Antenna System," filed August 17, 2010 and also as shown in Figure 2 the Flexible Simulcast System 200 can be used to explain the operation of Flexible Simulcast with regard to uplink signals. As discussed previously with regard to downlink signals and by referring to Figure 1, the uplink system shown in Figure 2 is mainly comprised of DAU1 indicated at 201, RRU1 indicated at 203, RRU2 indicated at 204, DAU2 indicated at 202, RRU3 indicated at 205, and RRU4 indicated at 206. In a manner similar to the downlink operation explained by referring to Figure 1, the operation of the uplink system shown in Figure 2 can be understood as follows.

[0038] The Digital Down Converters present in each of RRU1, RRU2, RRU3 and RRU4 are dynamically software-configured as described previously so that uplink signals of the appropriate desired signal format(s) present at the receive antenna ports of the respective RRU1, RRU2, RRU3 and RRU4 are selected based on the desired uplink band(s) to be processed and filtered, converted and transported to the appropriate uplink output port of either DAU1 or DAU2. The DAUs and RRUs frame the individual data packets corresponding to their respective radio signature using the Common Public Interface Standard (CPRI). Other Interface standards are applicable provided they uniquely identify data packets with respective RRUs. Header information is transmitted along with the data packet which indentifies the RRU and DAU that corresponds to the individual data packet.

[0039] In one example for the embodiment shown in Figure 2, RRU1 and RRU3 are configured to receive uplink signals within the Carrier 2 bandwidth, whereas RRU2 and RRU4 are both configured to reject uplink signals within the Carrier 2 bandwidth. When RRU3 receives a strong enough signal at its receive antenna port within the Carrier 2 bandwidth to be properly filtered and

processed, the Digital Down Converters within RRU3 facilitate processing and conversion. Similarly, when RRU1 receives a strong enough signal at its receive antenna port within the Carrier 2 bandwidth to be properly filtered and processed, the Digital Down Converters within RRU1 facilitate processing and conversion. The signals from RRU1 and RRU3 are combined based on the active signal combining algorithm, and are fed to the base station connected to the uplink output port of DAU1. The term simulcast is frequently used to describe the operation of RRU1 and RRU3 with regard to uplink and downlink signals within Carrier 2 bandwidth. The term Flexible Simulcast refers to the fact that the present invention supports dynamic and/or manual rearrangement of which specific RRU are involved in the signal combining process for each Carrier bandwidth.

[0040] Referring to Figure 2, the Digital Down Converters present in RRU1 are configured to receive and process signals within Carrier 1-8 bandwidths. The Digital Down Converters present in RRU2 are configured to receive and process signals within Carrier 1, 3, 4 and 6 bandwidths. The Digital Down Converters present in RRU3 are configured to receive and process signals within Carrier 2 and 6 bandwidths. The Digital Down Converters present in RRU4 are configured to receive and process signals within Carrier 1, 4, 5 and 8 bandwidths. The respective high-speed digital signals resulting from processing performed within each of the four RRU are routed to the two DAUs. As described previously, the uplink signals from the four RRUs are combined within the respective DAU corresponding to each base station.

[0041] An aspect of the present invention includes an integrated Pilot Beacon function within the each RRU. In an embodiment, each RRU comprises a unique software programmable Pilot Beacon as discussed hereinafter This approach is

intended for use in CDMA and/or WCDMA indoor DAS networks. A very similar approach can be effective for indoor location accuracy enhancement for other types of networks such as LTE and WiMAX. Because each RRU is already controlled and monitored via the DAUs which comprise the network, there is no need for costly deployment of additional dedicated wireless modems for remote monitoring and control of pilot beacons.

[0042] An RRU-integrated Pilot Beacon approach is employed for both CDMA and WCDMA networks. Each operational pilot beacon function within an RRU employs a unique PN code (in that area) which effectively divides the WCDMA or CDMA indoor network coverage area into multiple small "zones" (which each correspond to the coverage area of a low-power Pilot Beacon). Each Pilot Beacon's location, PN code and RF Power level are known by the network. Each Pilot Beacon is synchronized to the WCDMA or CDMA network, via its connection to the DAU.

[0043] Unlike the transmit signal from a base station which is "dynamic", the Pilot Beacon transmit signal will be effectively "static" and its downlink messages will not change over time based on network conditions.

[0044] For a WCDMA network, in Idle mode each mobile subscriber terminal is able to perform Pilot Signal measurements of downlink signals transmitted by base stations and Pilot Beacons. When the WCDMA mobile subscriber terminal transitions to Active mode, it reports to the serving cell all its Pilot Signal measurements for base stations and for Pilot Beacons. For CDMA networks, the operation is very similar. For some RRU deployed in an indoor network, the RRU can be provisioned as either a Pilot Beacon or to serve mobile subscribers in a particular operator bandwidth, but not both.

[0045] For a WCDMA network, existing inherent capabilities of the globally-standardized networks are employed. The WCDMA mobile subscriber terminal is able to measure the strongest CPICH RSCP (Pilot Signal Code Power) in either Idle mode or any of several active modes. Also, measurements of CPICH Ec/No by the mobile subscriber terminal in either Idle mode or any of several active modes are possible. As a result, the mobile subscriber terminal reports all available RSCP and Ec/No measurements via the serving base station (whether indoor or outdoor) to the network. Based on that information, the most likely mobile subscriber terminal location is calculated and/or determined. For CDMA networks, the operation is very similar to the process described herein.

[0046] A previously described embodiment of the present invention referring to Figure 1 involved having a wideband CDMA signal present within e.g., the bandwidth corresponding to carrier 1 at the input port to DAU1. In the previously described embodiment, the transmitted signal at the antenna ports of RRU1, RRU2 and RRU4 is a wideband CDMA signal which is virtually identical to the signal present within the bandwidth corresponding to carrier 1 at the input port to DAU1. An alternative embodiment of the present invention is one where a wideband CDMA signal is present within e.g., the bandwidth corresponding to carrier 1 at the input port to DAU1. However, in the alternative embodiment the transmitted signal at the antenna port of RRU1 differs slightly from the previous embodiment. In the alternative embodiment, a wideband CDMA signal is present within e.g., the bandwidth corresponding to carrier 1 at the input port to DAU1. The transmitted signal from RRU1 is a combination of the wideband CDMA signal which was present at the input port to DAU1, along with a specialized WCDMA pilot beacon signal. The WCDMA pilot beacon signal is intentionally set well below the level of the base station pilot signal.

[0047] A further alternative embodiment can be explained referring to Figure 1 which applies in the case where CDMA signals are generated by the base station connected to the input port of DAU1. In this further alternative embodiment of the present invention, the transmitted signal at the antenna port of RRU1 is a combination of the CDMA signal which was present at the input port to DAU1, along with a specialized CDMA pilot beacon signal. The CDMA pilot beacon signal is intentionally set well below the level of the base station pilot signal.

[0048] An embodiment of the present invention provides enhanced accuracy for determining location of indoor wireless subscribers. Figure 4 depicts a typical indoor system employing multiple Remote Radio Head Units (RRUs) and a central Digital Access Unit (DAU). Each Remote Radio Head provides a unique header information on data received by that Remote Radio Head. This header information in conjunction with the mobile user's radio signature are used to localize the user to a particular cell. The DAU signal processing can identify the individual carriers and their corresponding time slots. A header is included with each data packet that uniquely identifies the corresponding RRU. The DAU can detect the carrier frequency and the corresponding time slot associated with the individual RRUs. The DAU has a running data base that identifies each carrier frequency and time slot with a respective RRU. The carrier frequency and time slot is the radio signature that uniquely identifies the GSM user.

[0049] The DAU communicates with a Network Operation Center (NOC) via a Ethernet connection or an external modem, as depicted in Figure 5. Once a E911 call is initiated the Mobile Switching Center (MSC) in conjunction with the NOC can identify the corresponding BaseTransceiver Station (BTS) where the user has placed the call. The user can be localized within a BTS cell. The NOC

then makes a request to the individual DAUs to determine if the E911 radio signature is active in their indoor cell. The DAU checks its data base for the active carrier frequency and time slot. If that radio signature is active in the DAU, then that DAU will provide the NOC with the location information of the corresponding RRU.

[0050] A further embodiment of the present invention includes LTE to provide enhanced accuracy for determining the location of indoor wireless subscribers. GSM uses individual carriers and time slots to distinguish users whereas LTE uses multiple carriers and time slot information to distinguish users. The DAU can simultaneously detect multiple carriers and their corresponding time slots to uniquely identify the LTE user. The DAU has a running data base that identifies the carrier frequencies and time slot radio signature for the respective RRU. This information can be retrieved from the NOC once a request is made to the DAU.

[0051] Referring next to Figure 7, the DAU embedded software control module and RRU embedded software control module can be better understood in connection with the operation of key functions of the DAU and RRU. One such key function is determining and/or setting the appropriate amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular RRU or group of RRUs to meet desired capacity and throughput objectives. The DAU embedded software control module comprises a DAU Monitoring module that detects which carriers and corresponding time slots are active for each RRU. The DAU embedded software control module also comprises a DAU Management Control module which communicates with the RRU over a fiber optic link control channel via a control protocol with the RRU Management Control module. In turn, the RRU Management Control module sets the individual parameters of all the RRU Digital Up-Converters to enable or

disable specific radio resources from being transmitted by a particular RRU or group of RRUs, and also sets the individual parameters of all the RRU Digital Down-Converters to enable or disable specific uplink radio resources from being processed by a particular RRU or group of RRUs.

[0052] In an embodiment, an algorithm operating within the DAU Monitoring module, that detects which carriers and corresponding time slots for each carrier are active for each RRU, provides information to the DAU Management Control module to help identify when, e.g., a particular downlink carrier is loaded by a percentage greater than a predetermined threshold whose value is communicated to the DAU Management Control module by the DAU's Remote Monitoring and Control function. If that occurs, the DAU Management Control module adaptively modifies the system configuration to slowly begin to deploy additional radio resources (such as RF carriers, CDMA codes or TDMA time slots) for use by a particular RRU which need those radio resources within its coverage area. At the same time, in at least some embodiments the DAU Management Control module adaptively modifies the system configuration to slowly begin to remove certain radio resources (such as RF carriers, CDMA codes or TDMA time slots) for use by a particular RRU which no longer needs those radio resources within its coverage area. Another such key function of the DAU embedded software control module and RRU embedded software control module is determining and/or setting and/or analyzing the appropriate transmission parameters and monitoring parameters for the integrated Pilot Beacon function contained within each RRU. These Pilot Beacon transmission and monitoring parameters include Beacon Enable/Disable, Beacon Carrier Frequencies, Beacon Transmit Power, Beacon PN Code, Beacon Downlink BCH Message Content, Beacon Alarm, Beacon Delay Setting and Beacon Delay

Adjustment Resolution. The RRU Pilot Beacon Control module communicates with the pilot beacon generator function in the RRU to set and monitor the pilot beacon parameters as listed herein.

[0053] In summary, the Reconfigurable Distributed Antenna System of the present invention described herein efficiently conserves resources and reduces costs. The reconfigurable system is adaptive or manually field-programmable, since the algorithms can be adjusted like software in the digital processor at any time.

[0054] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

What is Claimed is:

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ABSTRACT

The present disclosure is a novel utility of a software defined radio (SDR) based Distributed Antenna System (DAS) that is field reconfigurable and support multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands and multi-channels. The present disclosure enables a high degree of flexibility to manage, control, enhance, facilitate the usage and performance of a distributed wireless network such as flexible simulcast, automatic traffic load-balancing, network and radio resource optimization, network calibration, autonomous/assisted commissioning, carrier pooling, automatic frequency selection, frequency carrier placement, traffic monitoring, traffic tagging, pilot beacon, etc. As a result, the SDR DAS can increase the efficiency and traffic capacity of the operators' wireless network.

APPENDIX I

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
BTS	Base Transceiver System or Base Station
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DAU	Digital Access Unit
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter

MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
PN	Pseudo-Noise
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRH	Remote Radio Head
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS

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SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit. Multi-mode radios capable of operating according to GSM, HSPA, LTE, and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multi-frequency bands within a single RRU to economize the cost of radio network deployment.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G. Wireless and mobile technology standards are

evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years. Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution, Figure 6. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept constitutes a fundamental part of a state-of-the-art base station architecture. However, RRUs to-date are power inefficient, costly and inflexible. Their poor DC to RF power conversion insures that they will have a large mechanical housing. The RRU demands from the service providers are also for greater flexibility in the RRU platform. As standards evolve, there is a need for a software upgradable RRU. Today RRUs lack the flexibility and performance that is required by service providers. The RRU performance limitations are driven in part by the poor power efficiency of the RF amplifiers. Thus there has been a need for an efficient, flexible RRU architecture that is field reconfigurable.

SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems in the prior art, and it is an object of the present invention to provide a high performance and cost effective method of multi-frequency bands RRU systems enabled by high linearity and high efficiency power amplifiers for wideband communication system applications. The present disclosure enables a RRU to be field reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels.

[002] To achieve the above objects, according to the present invention, the technique is generally based on the method of adaptive digital predistortion to linearize RF power amplifiers. Various embodiments of the invention are disclosed, including single band, dual band, and multi-band RRU's. Another embodiment is a multi-band multi-channel RRU. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[003] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations,

distributed antenna systems, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram showing the basic form of a Remote Radio head unit system.

[007] Figure 2 is a block diagram showing a multi-channel Remote Radio Head Unit according to one embodiment of the present invention.

[007] Figure 3 is a block diagram showing polynomial based predistortion in a Remote Radio head system of the present invention.

[008] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a remote radio head unit system of the present invention.

[009] Figure 5 illustrates an analog modulator compensation block.

[0010] Figure 6 depicts schematically a variety of potential installation schemes for an RRU-based system architecture.

[0011] Figure 7 depicts a three-sector arrangement of an RRU system architecture comprising optical links to a base station server.

[0012] Figure 8 shows in block diagram form various DSP-based functions including crest factor reduction and digital predistortion.

[0013] Figure **9** is a Digital Hybrid Module with either an RF input signal or a baseband modulated signal or an optical interface according to another embodiment of the present invention.

[0014] Figure **10** is a Dual Channel Remote Radio head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present invention.

[0015] Figure **11** is an alternative Dual Channel Remote Radio Head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present

[0016] Figure **12** is an 8 channel Dual Band Remote Radio Head block diagram showing a digital hybrid module with an optical interface, and further comprises a calibration algorithm for insuring that each power amplifier output is time-aligned, phase-aligned and amplitude-aligned with respect to each other.

GLOSSARY

Acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector

AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter

MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
SERDES	Serializer/Deserializer
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network.

DETAILED DESCRIPTION OF THE INVENTION

[001] The present invention is a novel RRU **s**ystem that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[002] Figure 1 is a high level block diagram showing the basic system architecture of what is sometimes referred to as a Remote Radio Head Unit, or RRU, which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention operates as a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a Remote Radio head Unit (RRU) hereinafter.

[003] Figure 2 illustrates in schematic block diagram form an embodiment of an eight channel (or n channel) RRU in which an input signal 200 is provided. Depending on the implementation, the input signal can take the form of an RF modulated signal, a baseband signal, or an optical signal. The input signal 200 is fed to a plurality of channels, where each channel includes a digital predistortion (DPD) controller, indicated at 201, 211 and 271, respectively. The DPD can be implemented in an FPGA in at least some embodiments. For each channel, the DPD outputs are fed to

associated PA's 202, 212 and 272, respectively, and the PA outputs 203, 213 and 273 are fed back to that channel's DPD's.

[004] Figure 3 illustrates a polynomial-based digital predistorter function in the RRU system of the present invention. The PD in the present invention generally utilizes an adaptive LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3, and in embodiments disclosed from Figures 9-12 discussed hereinafter, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the RRU system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistorter algorithm based on the error between the reference input signal and the amplified power output signal.

[005] Figure 4 shows in block diagram form additional details of an embodiment including a DPD in accordance with the present invention and is discussed in greater detail hereinafter. In general, the input 400 is provided to the DPD 401. The output of the DPD is fed to a DAC 402 and thence to the PA 403. A feedback signal from the output of the PA is received by ADC 406, and the digital form is supplied to alignment logic 405, after which the aligned signal is provided to DPD estimator logic 404, which also receives an

input from the output of the DPD 401. The output of the DPD estimator is then fed back to the DPD 401.

[006] Figure 5 illustrates an analog modulator compensation block. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11 , g12 , g21 , g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to an AQM's in-phase and quadrature ports, discussed hereinafter in connection with Figure 9.

[007] Figure 6 illustrates a plurality of possible implementations of an RRU-based system architecture, in with a base station server 600 is connected to, for example, a tower-mounted RRU 605, a rooftop-mounted RRU 610, and/or a wall-mounted RRU 615.

[008] Figure 7 illustrates an embodiment of a three-sector implementation of an RRU-based system architecture, in which a base station server 700 is optically linked to a plurality of RRU's 710 to provide adequate coverage for a site.

[009] Figure 8 illustrates in simplified form an embodiment of the DSP functionality of some implementations of the present invention. An input signal is fed to an interface 800, which can take several forms including OBSAI, CPRI or IR. The incoming signal is fed to a digital up-converter (DUC) 805 and then to CFR/DPD logic 810, such as an FPGA. The output of

the CFR/DPD logic 810 is then supplied to a DAC 815. The DAC provides an output signal to the analog RF portion 820 of the system, which in turn provides a feedback signal to a ADC 825, and back through the DSP block in the form of inputs to the CFR/DPD and a DDC 830. The DDC outputs a signal to the interface 800, which in turn can provide an output.

[0010] Figure 9 is a block diagram showing a more sophisticated embodiment of a RRU system, where like elements are indicated with like numerals. The embodiment of Figure 9 applies crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in US patent application SN 61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0011] Figure 9 is a block diagram showing a RRU system according to one embodiment of the present invention (the "FIG. 9. System"). RRU systems consist of three primary blocks: power amplifiers, baseband processing and an optical interface. The optical interface contains an optical to electrical interface for the transmit/receive mode. The optical interface 901,

shown in Figure 9, is coupled to a FPGA. The FPGA 902 performs the functions of SERDES/Framer/De-Framer/Control and Management. This FPGA 902 interfaces with another FPGA 903 that performs the following Digital Signal Processing tasks: Crest Factor Reduction/ Digital Upconversion/Digital Downconversion and Digital Predistortion. Another embodiment will be to integrate 902 with 903 in a single FPGA. The Serializer/De-serializer (SERDES) module converts the high speed serial bit stream from the optical to electrical receiver to a parallel bit stream. The De-Framer decodes the parallel bit stream and extracts the In-phase and Quadrature (I/Q) modulation and delivers this to the digital signal processing module 903. The Control and Management module extracts the control signals from the parallel bit stream and performs tasks based on the requested information. The received I/Q data from the optical interface is frequency translated to an Intermediate Frequency in the Digital Upconverter Module (DUC). This composite signal then undergoes Crest Factor Reduction (CFR) in order to reduce the peak to average power ratio. The resultant signal is then applied to a Digital Predistorter in order to compensate for the distortion in the Power Amplifier module 905. The RRU operates in a receive mode as well as a transmit mode. The RRU receives the signal from the output duplexer and passes this signal to the Rx path or paths, depending on the number of channels. The received signal is frequency translated to an Intermediate Frequency (IF) in the receiver (Rx1 and Rx2 in Figure 10). The IF signal is further downconverted using a Digital Downconverter (DDC) module and demodulated into the In-phase and quadrature components. The recovered I/Q signal is then sent to the Framer module/ SERDES and prepared for transmission over the optical interface.

[0012] The FIG. 9. System has a multi-mode of RF or multi-carrier digital signal or optical at the input, and an RF signal at the output 910. The multi-mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode") or optical input (the "Optical-in Mode"). The FIG. 9. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 915, a power amplifier module 960, a receiver 965 and a feedback path 925.

[0013] The FPGA-based Digital part comprises either one of two digital processors 902,903 (e.g. FPGA), digital-to-analog converters 935 (DACs), analog-to-digital converters 940 (ADCs), and a phase-locked loop (PLL) 945. Since the FIG. 9 System has a multi-input mode, the digital processor has three paths of signal processing. For the baseband signal input path, the digital processor has implemented a digital up-converter (DUC), CFR, and a PD. For the optical input path, SERDES, Framer/ Deframer, digital up-converter (DUC), CFR, and PD are implemented. For the RF input path, analog downconverter, DUC, CFR and PD are implemented.

[0014] The Baseband-in Mode of FIG. 9 contains the I-Q signals. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0015] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a wideband feedback which requires a very high speed ADC. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DACs . As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals 935, respectively. The gate bias voltage 950 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 935 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. The PLL 945 sweeps the local oscillation signal for the feedback part in order to translate the RF output signal to baseband, for processing in the Digital Module.

[0016] The power amplifier part comprises an AQM for real and complex signals (such as depicted in the embodiments shown in Figure 9) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental RRU system. One such Doherty power amplifier

technique is presented in commonly assigned U.S. Provisional Patent Application SN 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0017] The feedback portion comprises a directional coupler, a mixer, a low pass filter (LPF), gain amplifiers and, and a band pass filter (BPF),. Depending upon the embodiment, these analog components can be mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the LPF, the gain amplifier, and the BPF which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the DET 970 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, which shows a polynomial-based predistortion algorithm and from Figure 4, which shows the primary adaptive predistorter blocks which can be used in some embodiments of the invention.

[0018] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a

small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 907, hence maximizing the RRU system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC in the FPGA-based Digital portion and an extra UPC in the power amplifier part. The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0019] FIG. 9. is a block diagram showing a RRU system implemented with AQM according to another embodiment of the present invention (the "FIG. 9 System"). The digital processor of FIG. 9 System has implemented a CFR, a PD, and an analog quadrature modulator corrector (AQMC).

[0020] FIG. 9. is a block diagram showing a RRU system implemented with AQM and AQM-based Clipping Error Restoration Path according to another embodiment of th_e present invention (the "FIG. 9 System"). The Clipping Error Restoration Path in FIG. 9 System has two DACs in the FPGA-based Digital part and an AQM in lieu of the UPC in the power amplifier part.

[0021] Figure 10 is a block diagram showing a dual channel RRU implemented with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as $occu_{rs}$ in a $_T$ime

Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. An additional switch is used for calibrating the Digital Predistorter for each power amplifier. Another embodiment of the RRU is extending its applications to multi-frequency bands. In an embodiment, a multi-frequency band (ie. 2 or more bands) implementation comprises adding additional channelized power amplifiers in parallel. The output of the additional power amplifiers will be combined in an N by 1 duplexer and fed to a single antenna, although multiple antenna can also be utilized in some embodiments. Another embodiment of the multi-frequency band RRU combines two or more frequency bands in one or more of the power amplifiers.

Figure 11 is a block diagram showing another embodiment of the dual channel RRU. In this embodiment the Rx switch is placed on the third port of the circulator, thereby reducing the insertion loss between the PA output and the duplexer.

Figure 12 is a block diagram showing an embodiment of an 8 channel RRU. In this embodiment, the feedback path consists of a receiver chain plus a wideband capture chain. The receiver chain is required when the RRU is switched to a receive mode. The wideband capture chain is required for capturing the wideband distortion of the power amplifier. In addition a channel calibration algorithm is required in order to insure that each power amplifier output is time, phase and amplitude aligned to each other.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA).

Figure 1 shows the block diagram of linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The primary DPD blocks are shown in Figure 4.

Delay Estimation Algorithm:

The DPD estimator compares $\mathrm{x(n)}$ and its corresponding feedback signal $\mathrm{y(n-\Delta d)}$ to find the DPD coefficients, where $\mathrm{\Delta d}$ is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $\mathrm{x(n)}$, and feedback data, $\mathrm{y(n)}$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign(y(i+m+1) - y(i+m))$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $\mathrm{C(m)}$ is the feedback path delay..

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is

necessary. To simplify the design, only a half-sample delay is considered in this design. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel.

The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{jo,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{jhe}$$

Magnitude correction:

As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

The choice of N will depend on the accuracy desired.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^j$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = k_a k_b / k_a'$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & \overline{d(1)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_1^{1/2}} & 0 \\ \overline{q_1^*} & \overline{e_a^*(1)\gamma^{\frac{1}{2}}(1)} \\ \overline{h_1 \Phi_1^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(1)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{*}_{z}}[w_i - \bar{w}] = \bar{q}_1$$

In the iterative process, a block of data (in this design, there is 4096 data in one block) is stored in memory, and the algorithm uses all the data in memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data are processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficient as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

Channel Calibration Algorithm

The 8 channel RRU in Figure 12 has 16 distinct power amplifiers. Half the power amplifiers are designed for one band and the other for a second band . The bands are hereafter referred to as band A and band B, they occupy two distinct frequencies. The 8 channel RRU uses 8 antennas and both bands will coexist on each antenna. In order to maximize performance, each power amplifier's output signal needs to be time, phase and amplitude aligned with respect to each other. The antenna calibration algorithms consist of three distinct approaches: 1) A Pilot Tone is injected into each PA 2) a Reference Modulated signal is transmit through each PA 3) the Real Time I/Q data is used as the reference signal . The Pilot Tone approach requires the injection of a single carrier IF tone that will be tracked in either the feedback calibration path or the individual PA's receiver. Each transmitter

path for band A will be time, phase and amplitude aligned with respect to each other, similarly for band B. The Reference Modulated approach will utilize a stored complex modulated signal which will be transmitted through each of the band A PAs, similarly for the band B PAs. The transmitters will then be time, phase and amplitude aligned with respect to each other. Either the feedback calibration path or the individual receivers can be used for obtaining the PA output signals. The Real Time approach will operate on the real-time transmitted signals. This approach will utilize the DPD time alignment, phase and magnitude offset information to synchronize each PA output with respect to each other.

[0022] In summary, the RRU system of the present invention could enhance the performance for the efficiency and linearity more effectively since the RRU system is able to implement CFR, DPD and adaptation algorithm in one digital processor, which subsequently saves hardware resources and processing time. The high power efficiency of RF power amplifiers inside the RRU means that less thermal dissipation mechanism such as heat sink is needed; therefore, significantly reducing the size and volume of the mechanical housing. This smaller RRU can then enable service provider to deploy the RRU in areas where heavy or large RRU could not be deployed, such as pole tops, top of street lights, etc. due to lack of real estate, or weight limitation, wind factor, type of safety issues. The RRU system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime.

[0023] **M**oreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. The multi-frequency bands benefits mean that mobile operators can deploy fewer RRUs to cover more frequency bands for more mobile subscribers; hence significantly reducing CAPEX and OPEX. Other benefits of the RRU system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0024] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A remote radio head unit (RRU) system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier inside the RRU. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are monitored by a wideband feedback path and controlled by the adaptation algorithm in a digital module. Therefore, the present invention could compensate the nonlinearities as well as memory effects of the power amplifier systems and also improve performances, in terms of power added efficiency, adjacent channel leakage ratio and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

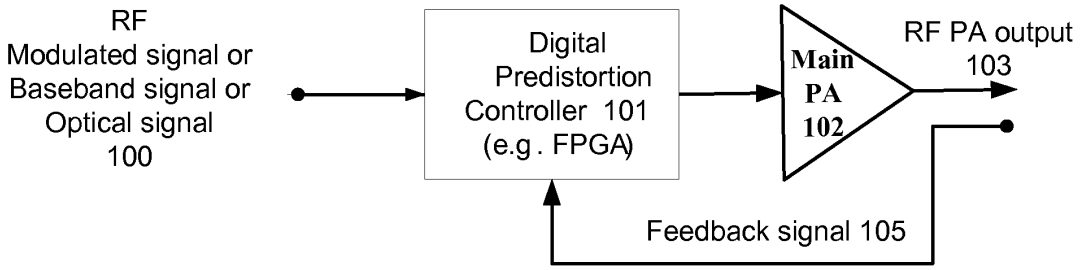
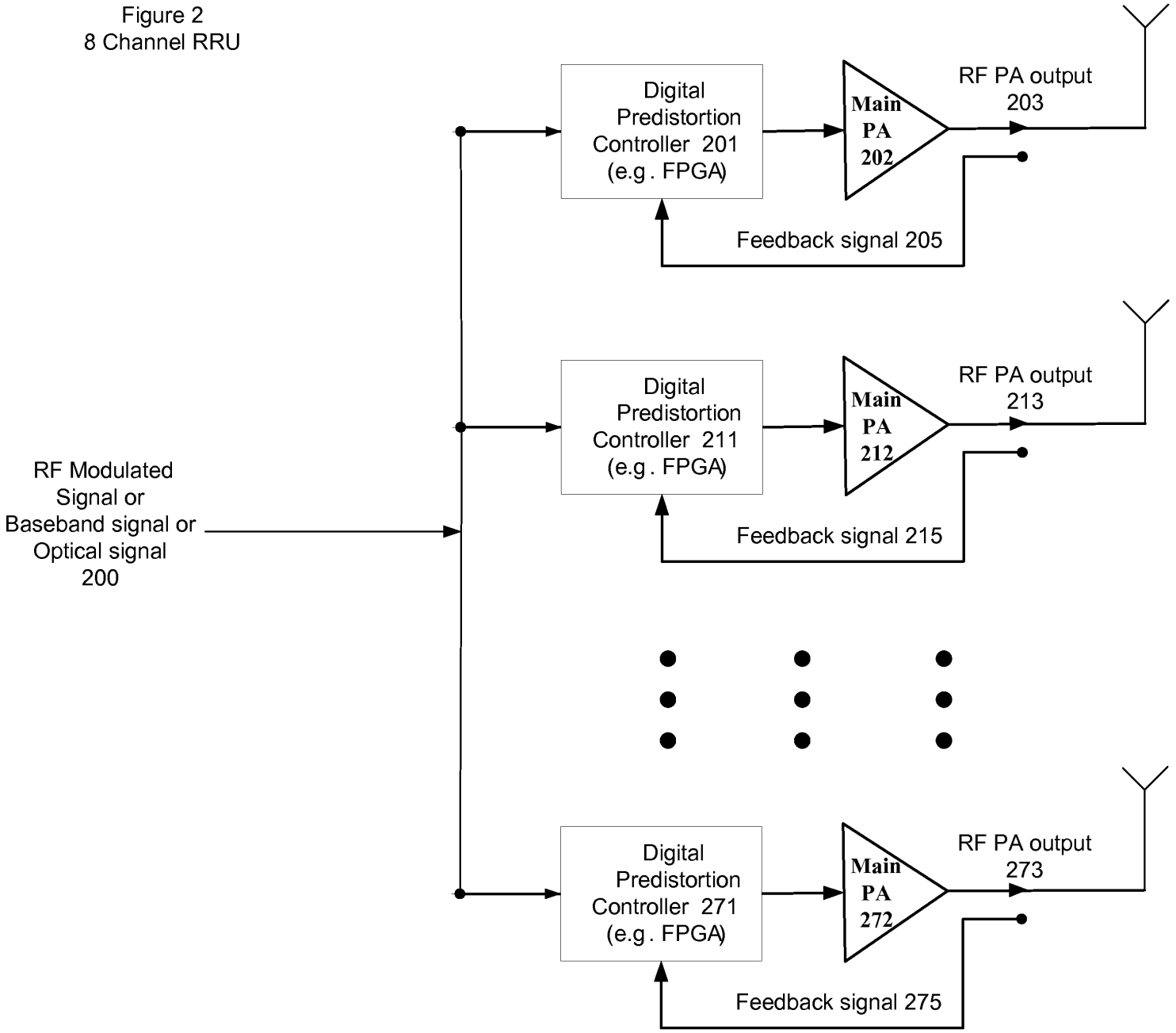


FIG. 1. Remote Radio Head Unit

Figure 2
8 Channel RRU



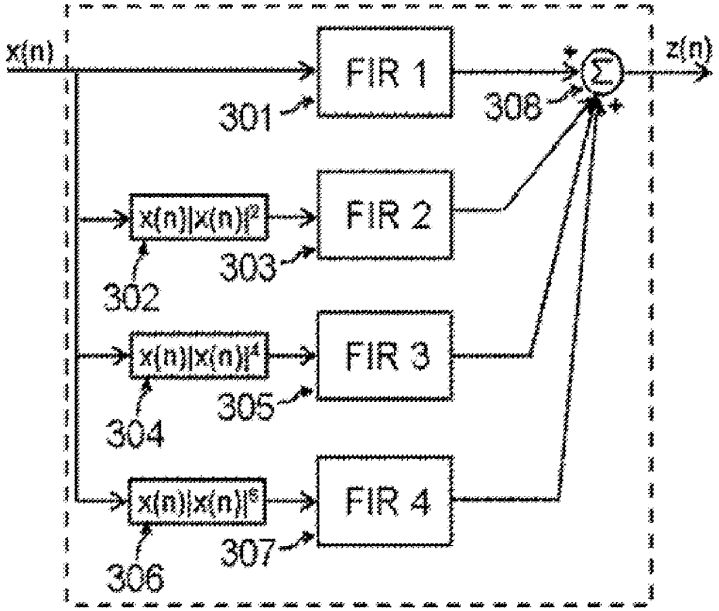


Figure 3. Polynomial based digital predistorter function

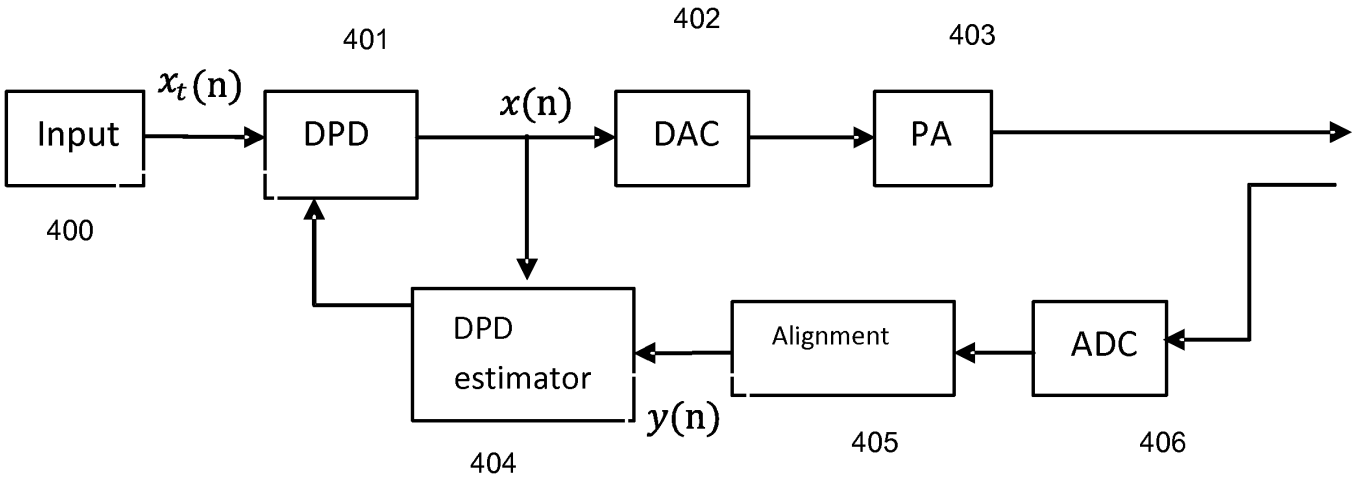


FIG. 4. Digital Predistortion Block Diagram

Figure 5 Analog Quadrature Modulator Compensation Block

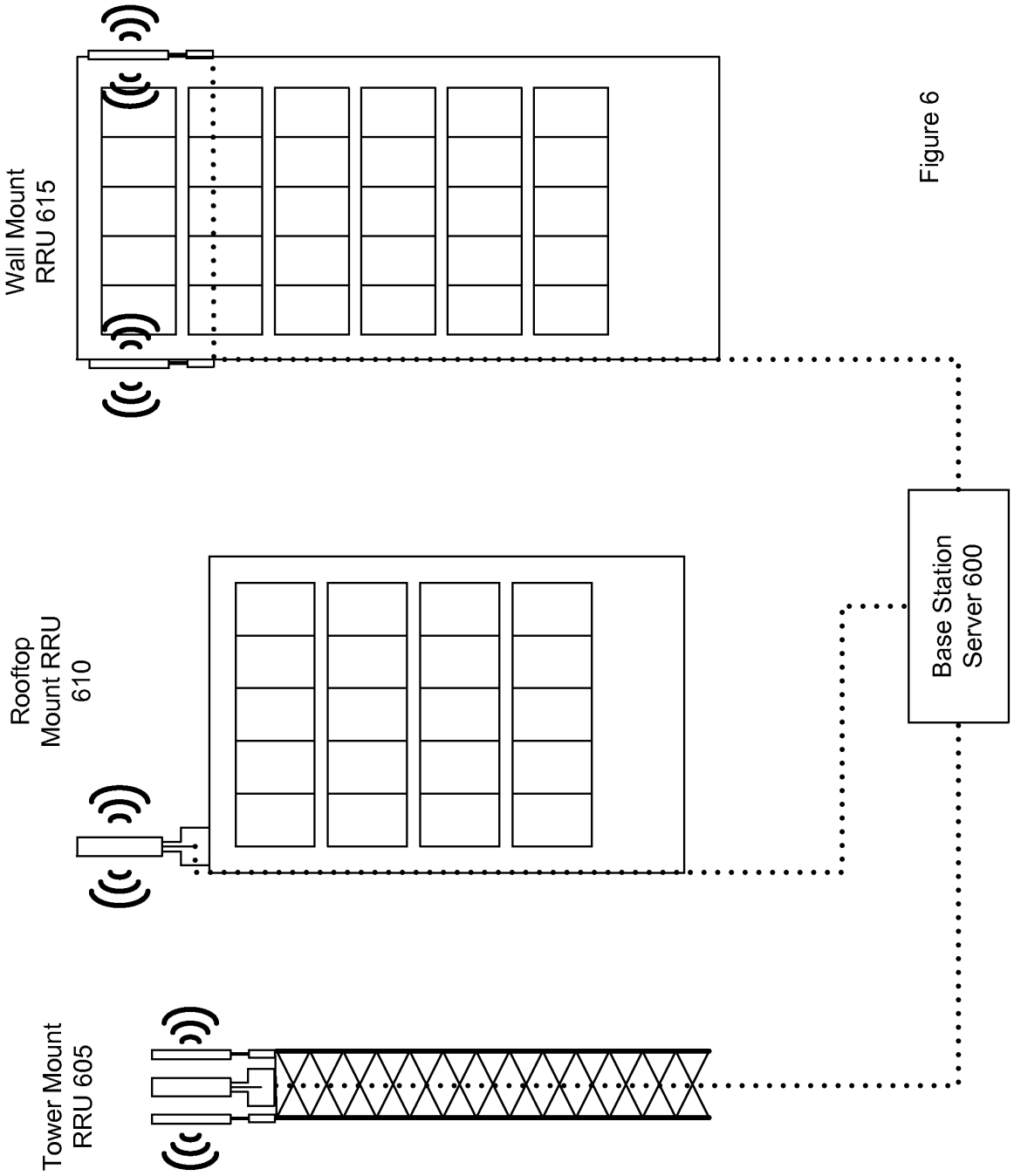

Wall Mount
RRU 615
Rooftop
Mount RRU
610
Tower Mount
RRU 605
Base Station
Server 600

Figure 6

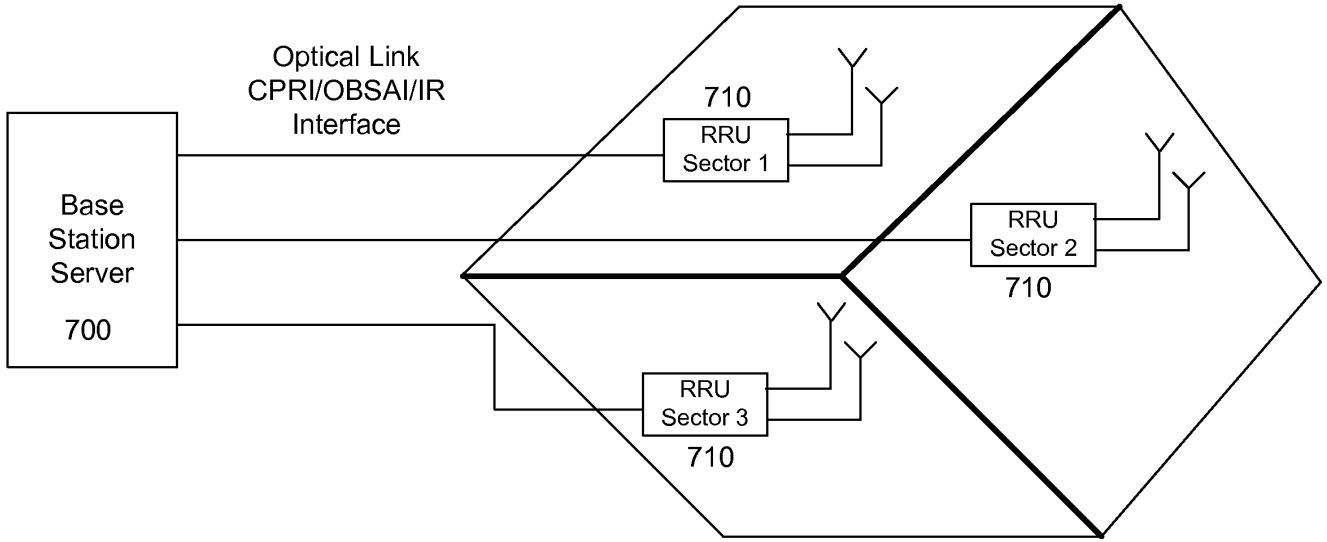

Optical Link
CPRI/OBSAI/IR
Interface
Base
Station
Server
700
710
RRU
Sector 1
RRU
Sector 2
710
RRU
Sector 3
710

Figure 7

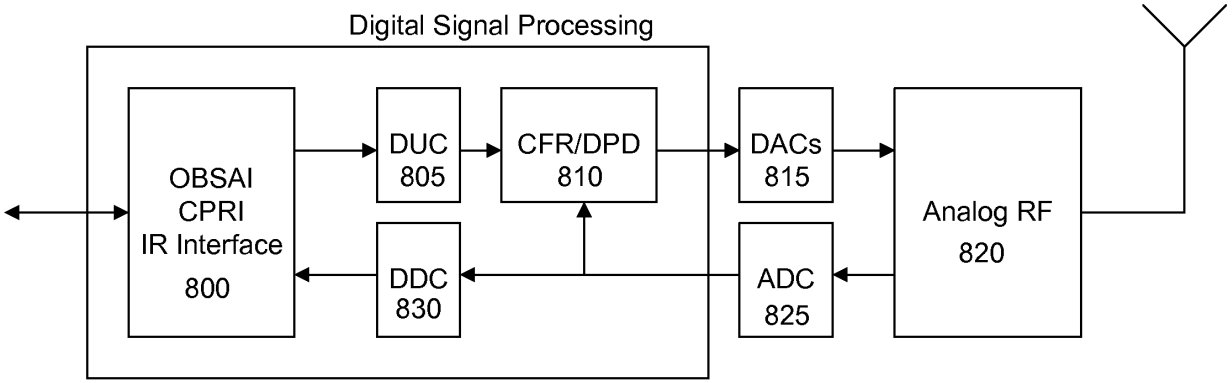

Digital Signal Processing
OBSAI
CPRI
IR Interface
800
DUC
805
CFR/DPD
810
DDC
830
DACs
815
ADC
825
Analog RF
820

Figure 8

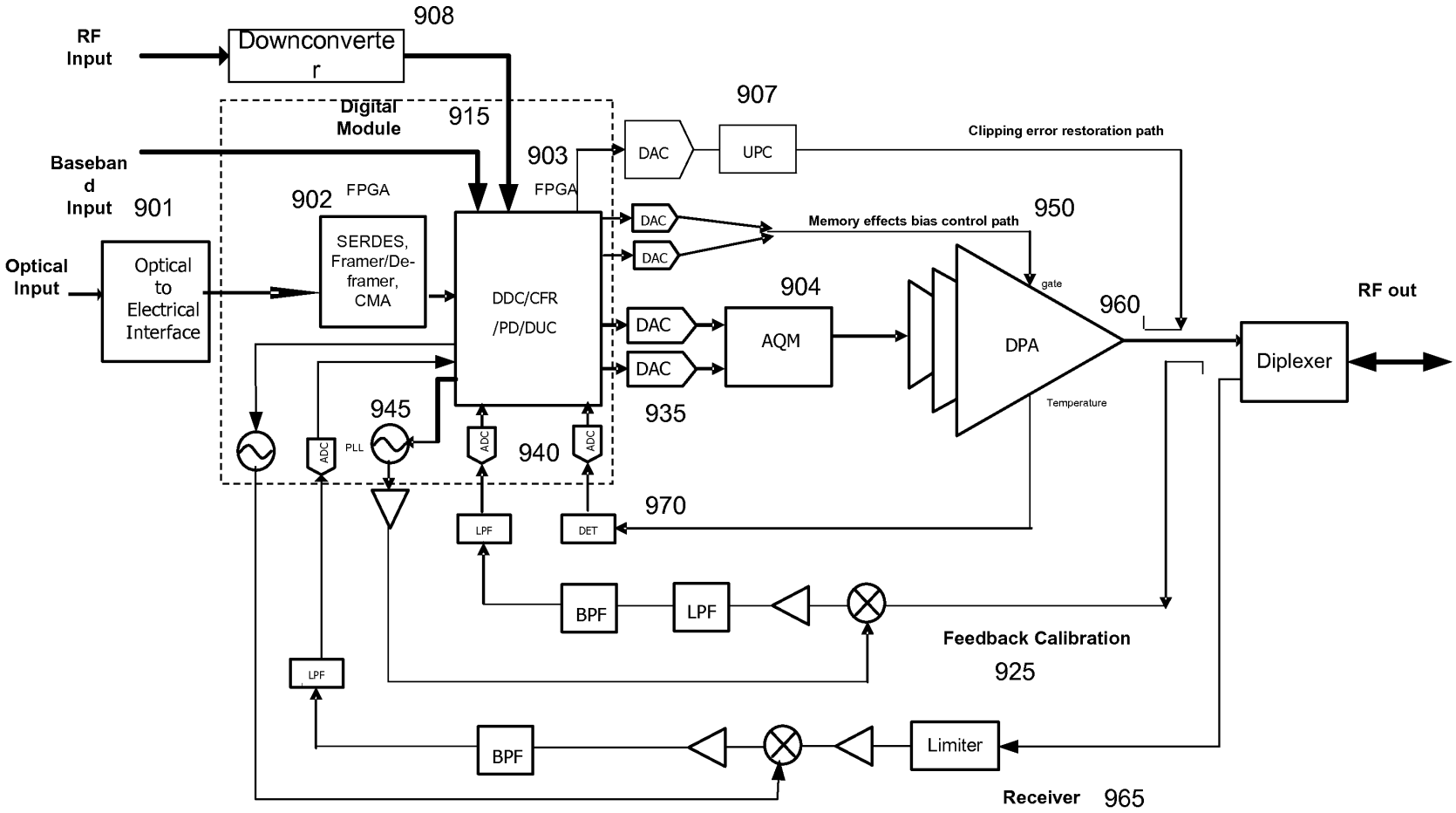


Figure 9 Digital Hybrid Module

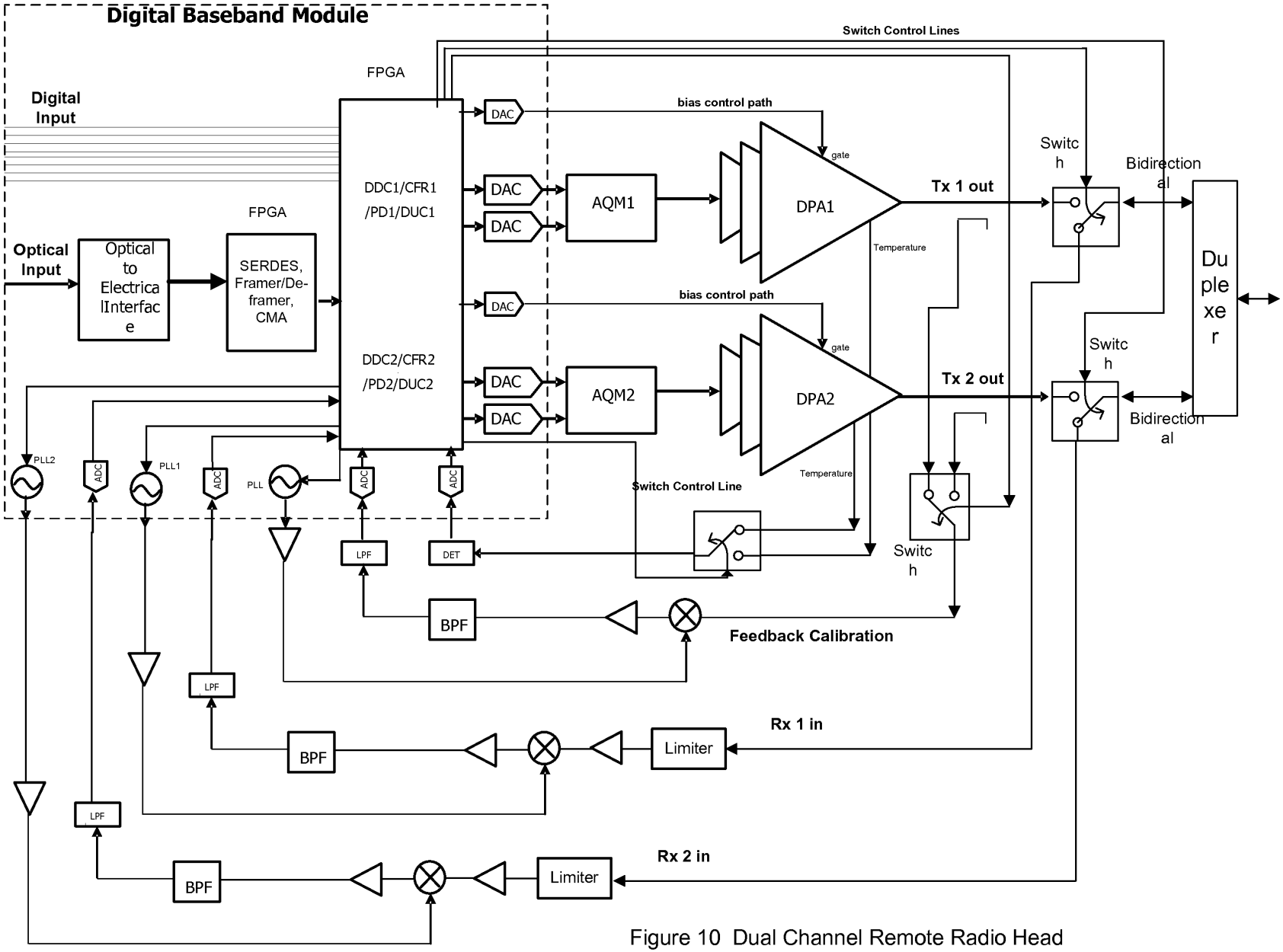


Figure 10 Dual Channel Remote Radio Head

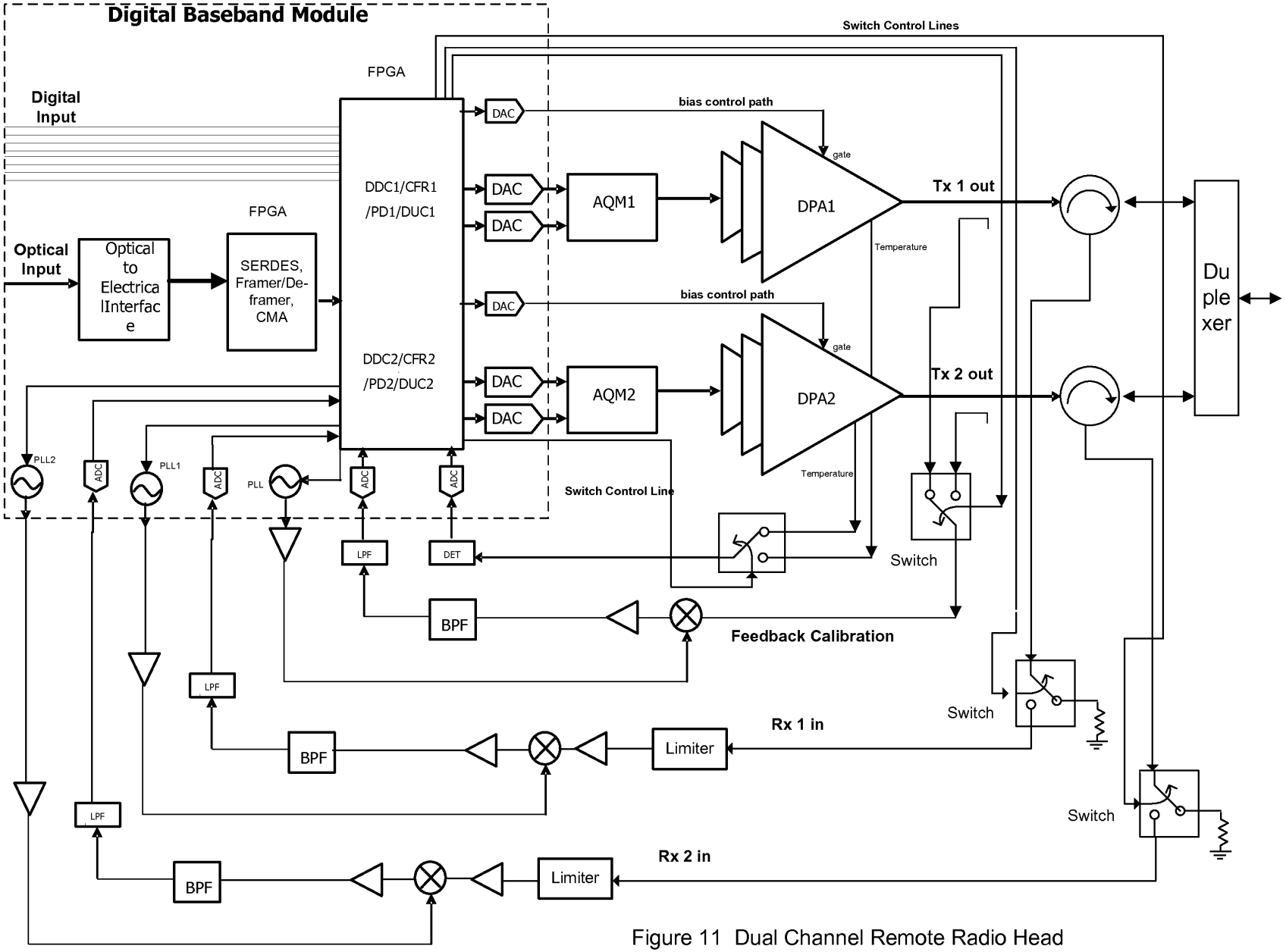
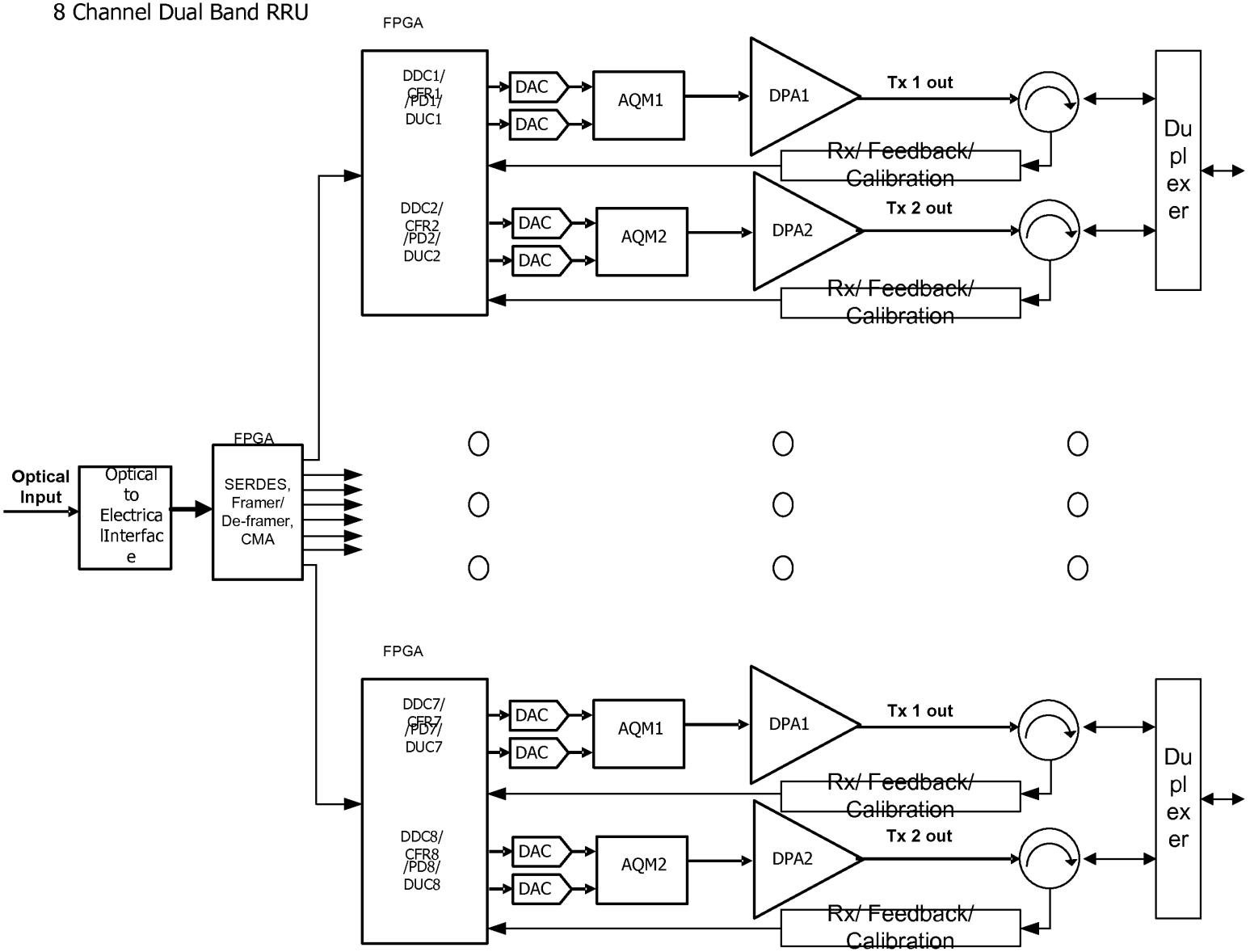


Figure 11 Dual Channel Remote Radio Head

Figure 12
8 Channel Dual Band RRU



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM

INVENTORS

Wan-Jong Kim, Citizen of Korea

Kyoung-Joon Cho, Citizen of Korea

Shawn Patrick Stapleton, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[002] A wideband mobile communication system using complex modulation techniques, such as wideband code division access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. Conventional digital predistortion (DPD) techniques have an operational bandwidth limitation.

[003] Conventional DSP-based DPD schemes utilize FPGAs, DSPs or microprocessors to compute, calculate and correct the PA's nonlinearities: they perform fast tracking and adjustments of signals in the PA system. However, conventional DSP-based DPD schemes are challenged by variations of the linearity performance of the power amplifier over wide bandwidths due to the environment changing such as temperature and the

asymmetric distortions of the output signal of the PA resulting from memory effects. Conventional DPD algorithms are based on a wideband feedback signal, they require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. Multi-frequency band, or simply multi-band, applications can have their operating frequencies spaced significantly apart. Conventional DPD architectures use an ADC sampling rate that is greater than twice the nonlinear distortion bandwidth of the input signal. This sampling rate is typically more than double a factor of five times the operating bandwidth of the complex modulated signal. The factor of five accounts for the spectral re-growth attributed to the nonlinear distortion created by the power amplifier. This restriction on sampling rate, limits the feasibility of the conventional predistortion architectures to single band applications. Higher sampling rate ADCs have lower resolution, consume more power and are more expensive.

SUMMARY OF THE INVENTION

[004] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers, and multi-channels.

[005] To achieve the above objects, according to the present invention, the technique is based on the method of adaptive digital predistortion to linearize a RF power amplifier. The present invention is based on using distinct signals from different frequencies (Multi-Band Signals). These Multi-Band Signals will experience distortion by the power amplifier and create nonlinear distortion centered on each carrier that is approximately five times their individual bandwidths. The feedback signal from the power amplifier's are down converted to an intermediate frequency (IF) that insures that the fundamental carrier bandwidths will not be aliased onto each other after sampling in the ADC. The present invention can accommodate aliasing of the nonlinear distortion of the individual carriers.

[006] Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction (CFR), DPD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator (AQM) compensation structure is also utilized to enhance performance.

[007] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called an adaptive DPD algorithm, which is implemented in the digital domain and taught in the applications incorporated herein by reference and attached as an Appendix.

Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless

devices, and other wireless communication systems such as microwave and satellite communications.

THE FIGURES

[008] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[009] Figure 1 is a block diagram showing the basic form of a digital predistortion power amplifier system.

[0010] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0011] Figure 3 is a block diagram showing polynomial based predistorter of the present invention.

[0012] Figure 4 is a block diagram of the digital predistortion Direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0013] Figure 5 is a block diagram of the digital predistortion In-direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0014] Figure 6 is a depiction of the frequency domain signals present in the aliased digital predistortion system.

[0015] Figure 7 is an embodiment of the Quadrature Modulator compensation block architecture.

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DPD	Digital Predistortion
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude

FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0016] The present invention is a novel multi-band predistortion system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers that operate simultaneously over multiple, distinct frequency bands.

[0017] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the DPD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system, as further discussed in the applications incorporated by reference. The present invention is a “black box”, plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101.

[0018] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD, Figure 2. The coefficients of the DPD are adapted by a synchronizing the wideband captured, aliased output Multi-BandSignal *ya[n]* from the feedback path (Sampled Feedback Aliased Signal) with the reference Multi-Band Signal *x[n]* (Input Signal). The DPD algorithm performs the synchronization and compensation. The synchronization aligns the reference signal with the aliased feedback signal in the alignment block. In one embodiment of the DPD algorithm, the reference signal and the aliased Sampled Feedback Aliased Signal *ya[n]* are used in the Direct Learning adaptive algorithm. In another embodiment of the DPD algorithm, the aliased predistorted signal *za[n]* (Predistorted Output Aliased Signal) and the Sampled Feedback Aliased Signal *ya[n]* are used in an Indirect Learning adaptive algorithm.

[0019] Some embodiments apply crest factor reduction (CFR) prior to the DPD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is typically used, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems,

incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0020] In all embodiments, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD. The coefficients of the DPD are adapted by synchronizing the wideband captured output signal from the feedback path with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal via a DAC. The DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals, respectively.

[0021] FIG 3. is a block diagram showing a predistortion (PD) part in the DPD system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the PD system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306.

The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows the block diagram of a digitally predistorted PA system. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4 and Figure 5. The coefficients are obtained using the QR RLS adaptive algorithm in the DPD estimator block.

Figure 4 shows one embodiment of the multi-band digital predistorter. The Direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the aliased sampled Multi-Band Signal *xa[n]* (Sampled Input Aliased Signal) as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

Figure 5 shows another embodiment of the multi-band digital predistorter. The in-direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the Predistorted Output Aliased

Signal *za[n]* as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

A depiction of the spectrum domain plots are shown in Figure 6. The reference Input Signal *x[n]* shows two distinct bands centered at frequencies F_a and F_b. The operating bandwidth of the individual carriers is small in comparison to the frequency spacing between the carriers. The nonlinearities in the power amplifier will cause spectral re-growth as shown in the analog feedback Multi-Band Signal *y(t)* (Analog Feedback Signal). The Analog Feedback Signal is down converted to an intermediate frequency Fi which is selected to be in the 1st Nyquist zone as shown in Figure 6. The choice of frequency Fi is dependent on the ADC sampling rate used, the operating bandwidth of the carriers and the frequency separation (F_a - F_b) between the carriers. The ADC sampling rate is typically the limiting factor in the choice of Fi. For a two carrier system F_a is positioned in the 1st Nyquist zone and F_b is positioned in the 2nd Nyquist zone in at least some embodiments. The choice of Fi limits how close Fa and Fb can be separated together.

Sampling on the Analog Feedback Signal *y(t)* generates images as shown in the spectrum for the Sampled Feedback Aliased Signal *ya[n]*. The nonlinear distortion from the individual carriers are allowed to alias onto each other as long as the aliased part of the signal does not adversely impact the original Multi-Band signal. A Direct Learning algorithm uses the difference between *xa[n]* and *ya[n]* to minimize the resultant error signal. The QR RLS algorithm uses this error to adapt the predistorter coefficients in the DPD estimator. The In-Direct learning algorithm first models the power amplifier using the Predistorted Output Aliased Signal *za[n]* and the Sampled Feedback Aliased

Signal *ya[n]*. The modelled power amplifier coefficients are then used to calculate the predistorter coefficients.

[0022] FIG. 7. is a block diagram showing the analog quadrature modulator compensation structure. The analog quadrature modulator will translate the baseband signal ouput from the DACs to an RF frequency. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12 , g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12 , g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

[0023] In summary, the multi-band wideband power amplifier predistortion system of the present invention can significantly reduce the feedback ADC sampling rate requirements. This will enable multi-band wideband applications and reduce the power consumption and cost. The system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime, as discussed in greater detail in the applications incorporated by reference and attached as an Appendix.

[0024] Moreover, the multi-band wideband DPD system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that

the DPD system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DPD system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0025] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A high performance and cost effective method of RF-digital hybrid mode power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications is disclosed. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels.

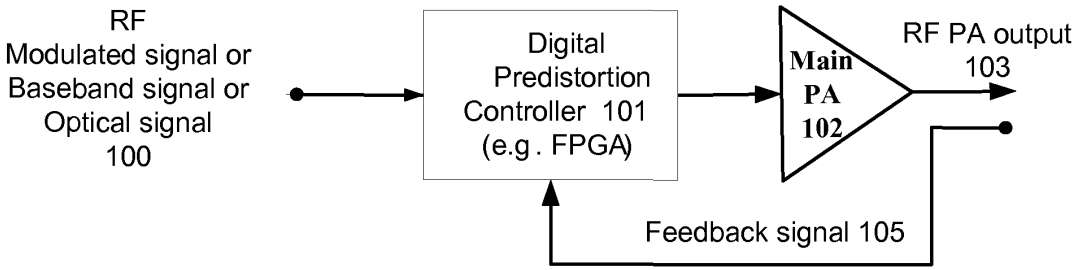

RF
Modulated signal or
Baseband signal or
Optical signal
100
Digital
Predistortion
Controller 101
(e.g. FPGA)
Main
PA
102
RF PA output
103
Feedback signal 105

Figure 1

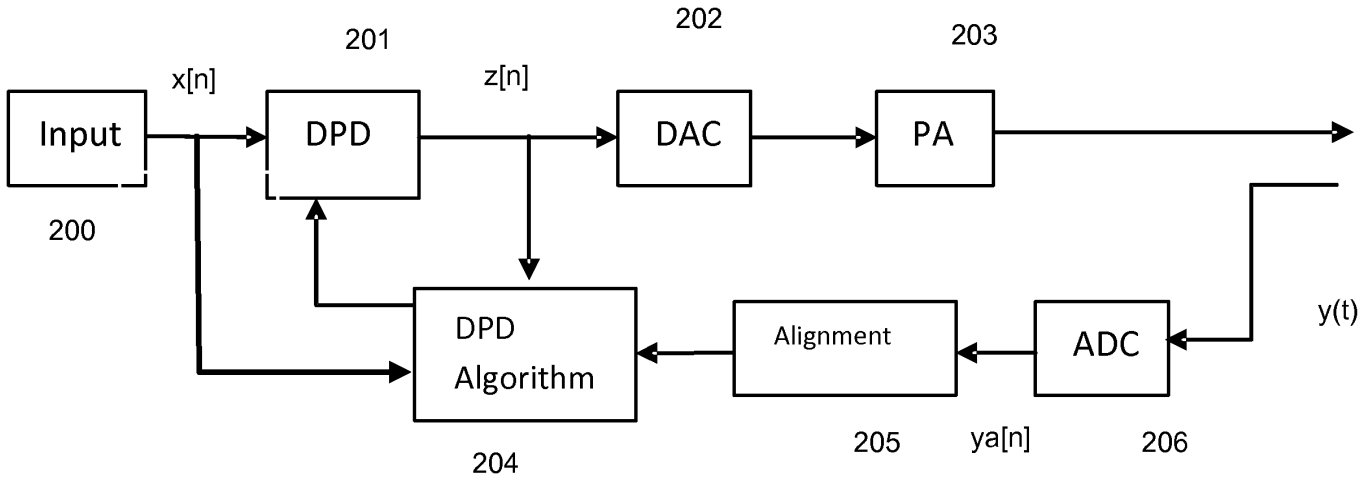


FIG. 2. Digital Predistortion Block Diagram

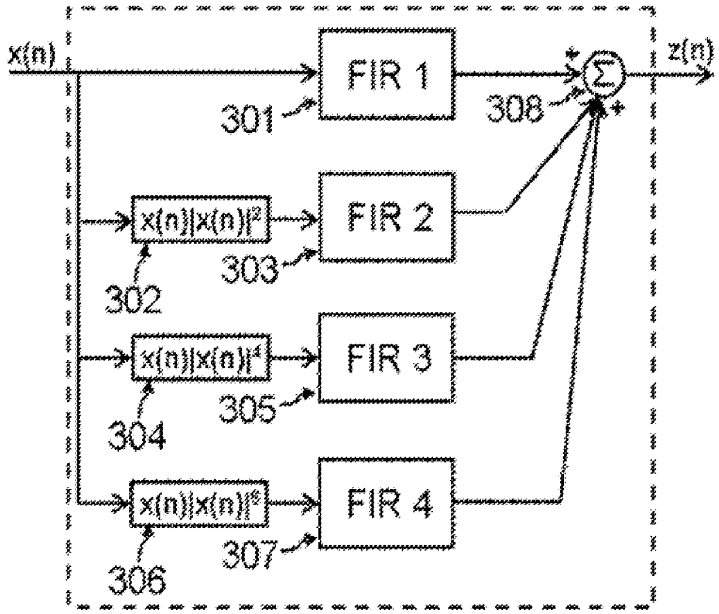


FIG. 3. Polynomial based Predistorter

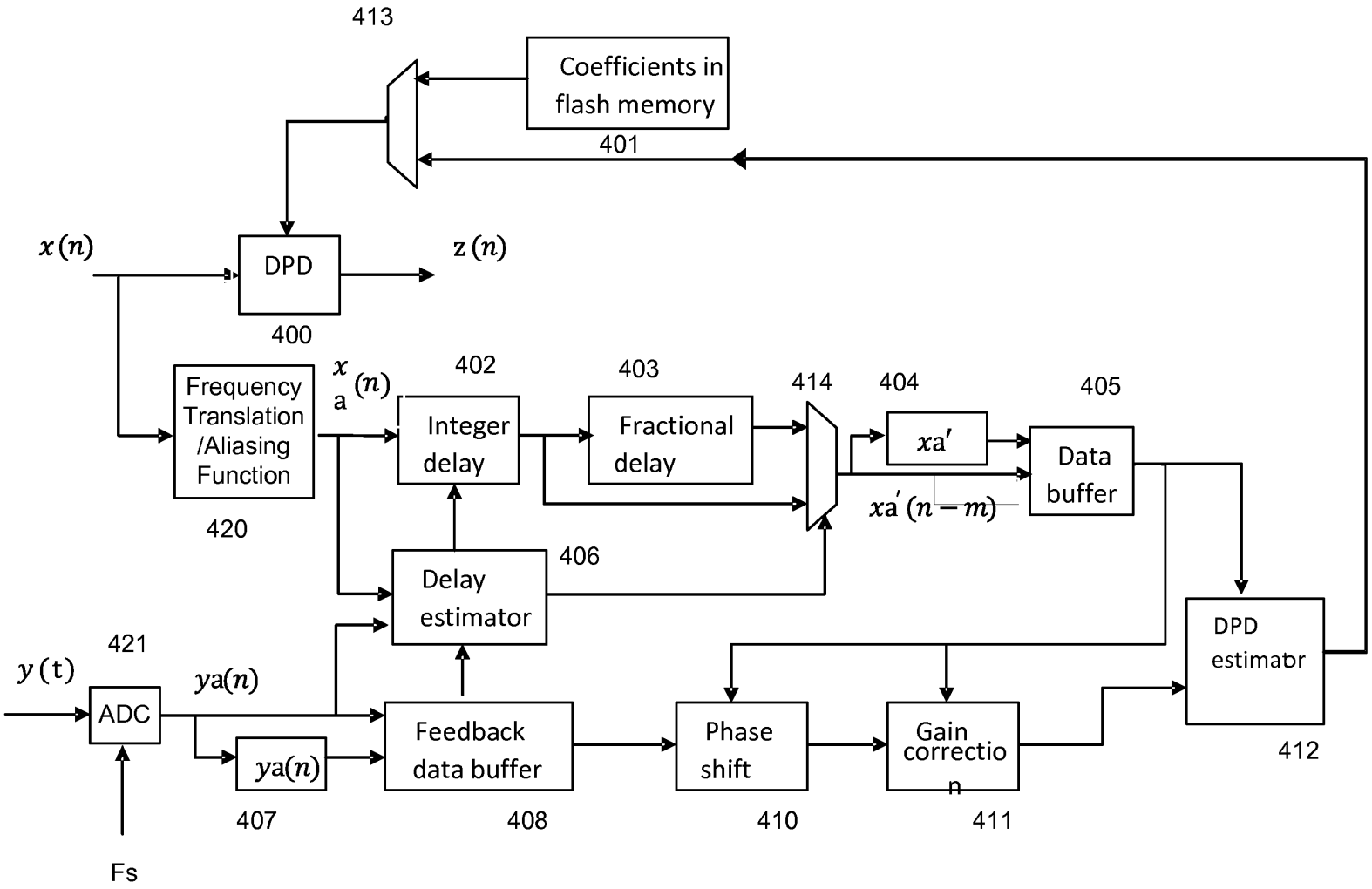


FIG. 4. Digital Predistortion Direct Learning Algorithm

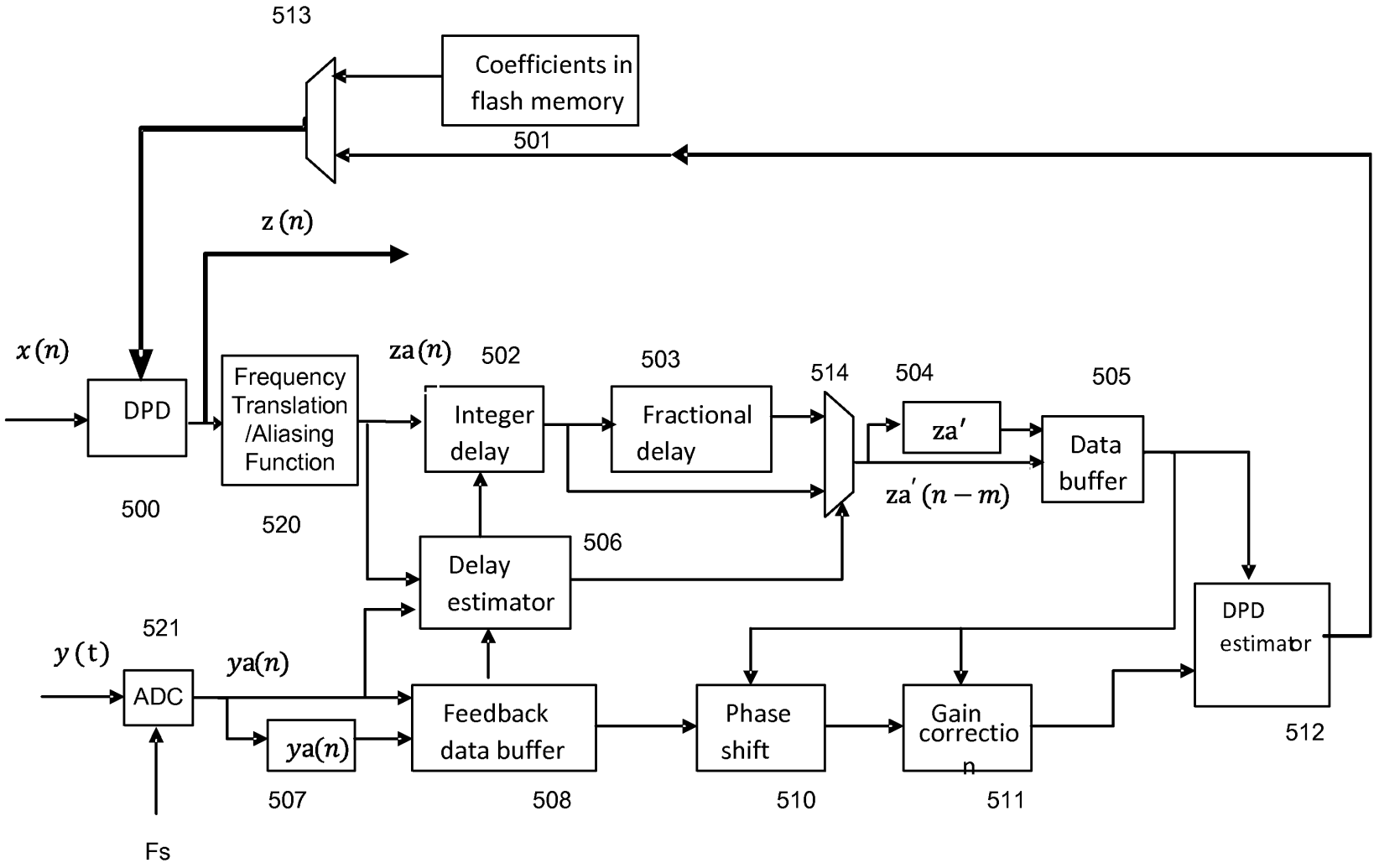


FIG. 5. Digital Predistortion Indirect Learning Algorithm

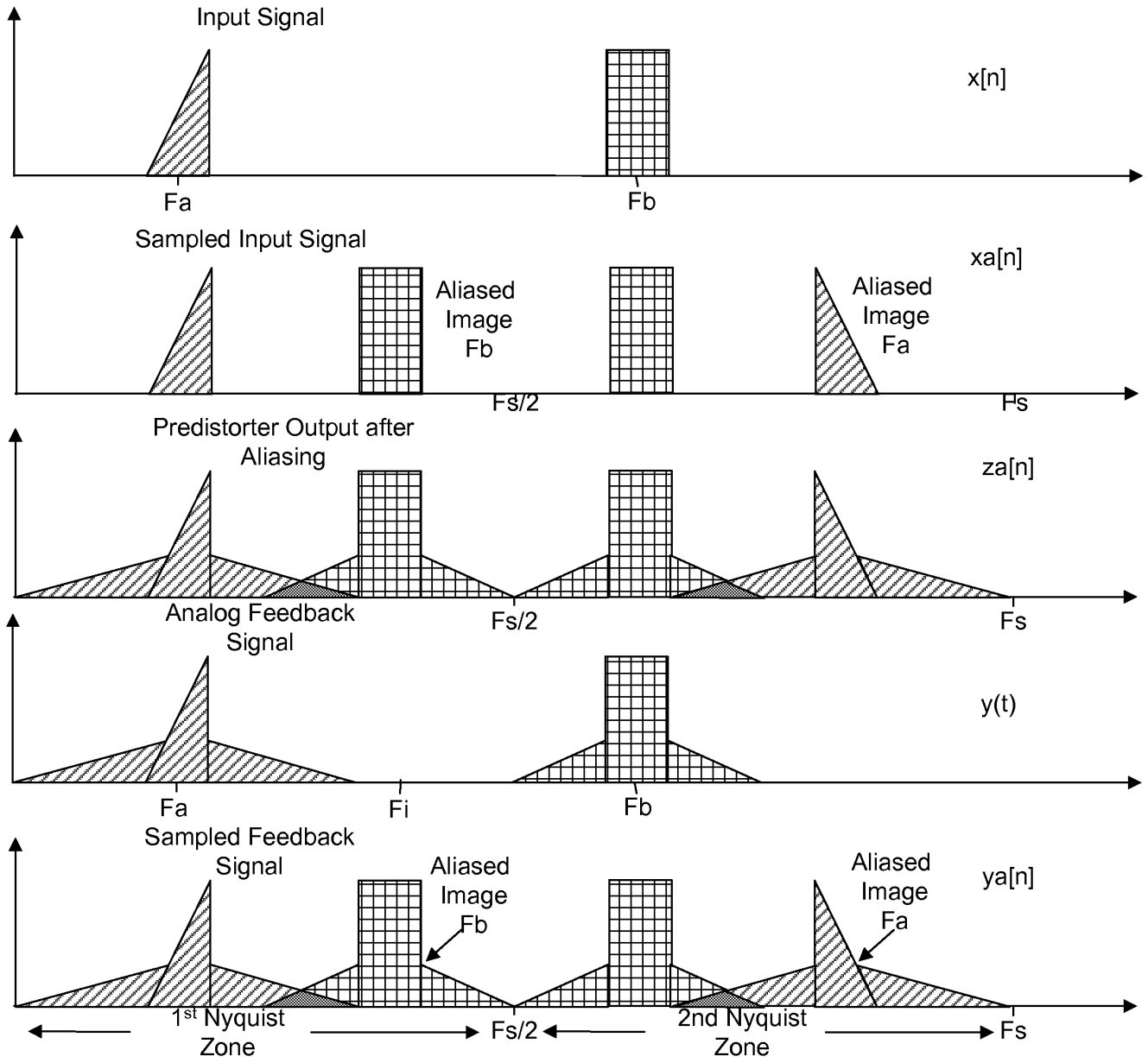

Input Signal
x[n]
Fa
Fb
Sampled Input Signal
xa[n]
Aliased
Image
Fb
Aliased
Image
Fa
Fs/2
Fs
Predistorter Output after
Aliasing
za[n]
Analog Feedback
Signal
Fs/2
Fs
y(t)
Fa
Fi
Fb
Sampled Feedback
Signal
Aliased
Image
Fb
Aliased
Image
Fa
ya[n]
1st Nyquist
Zone
Fs/2
2nd Nyquist
Zone
Fs

Figure 6

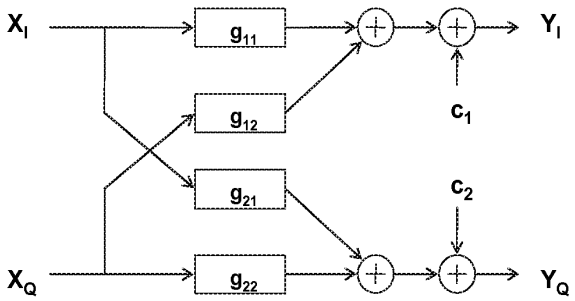


Figure 7: Analog Quadrature Modulator Compensation Block

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

REMOTE RADIO HEAD UNIT WITH WIDEBAND POWER AMPLIFIER AND METHOD

INVENTORS

Chengxun Wang, Citizen of People's Republic of China

Shawn Patrick Stapleton, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications, attached as Appendices:

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US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

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US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER

SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective solutions to expand network capacity and evolution towards 4G and beyond.

Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years.

Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept is a fundamental part of a state-of-the-art base station architecture. 2G/3G/4G base stations are typically connected to RRUs over optical fibers. Either CPRI, OBSAI or IR Interfaces may be used to carry data to the RRH to cover a three-sector cell. The RRU incorporates a large number of digital interfacing and processing functions. Traditionally, a multi-channel RRU means that multiple antennas are used, typically with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as occurs in a Time Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. To extent the prior art architecture to multiple bands (i.e., two or more bands) implementation would consist of adding additional channelized power

amplifiers in parallel. The output of the additional power amplifiers is typically combined in an N by 1 duplexer and fed to a single antenna.

While conventional RRU architecture offers some benefits, RRUs to date are power- inefficient, costly and inflexible. Further, their poor DC-to-RF power conversion insures that they will have a large mechanical housing. In addition, current RRU designs are inflexible. As standards evolve, there is a need for multi-band RRUs that can accommodate two or more operating channels using a single wideband power amplifier. This creates an isolation problem at the individual receivers because the wideband power amplifier is always turned on. Isolation between the wideband transmitter and receivers is a problem with any modulation standard (HSPA+, WiMAX, LTE, etc.) when multi-band RRUs are developed using a single power amplifier This is a common problem for all communication systems that utilize a wideband power amplifier in a multi-band scenario.

SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective technique for implementing RRU systems that service multi-frequency bands. Further, the present disclosure enables a RRU to be field-reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels. The present invention also serves multi-frequency bands within a single RRU to economize the cost of radio network deployment. In particular, the present invention resolves an isolation issue for a RRU with fewer power amplifiers than the number of operating frequency bands. Multi-

mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks.

[002] The present invention achieves the above objects using techniques generally based on methods and techniques for maximizing the isolation between the transmitted signal (Tx Signal) and the received signal (Rx Signal). The Tx Signal may comprise noise generated at the output of the power amplifier or it may comprise an unwanted transmitter band leaking into the receiver. With the use of the present invention, conventional RRU's can be extended to a multi-band and multi-channel configuration. Multi-band means that more than one frequency bands are used in the RRU and multi-channel means that more than one output antenna is used. Various embodiments of the invention are disclosed.

[003] An embodiment of the present invention utilizes duplexers, switches and circulators to maximize the isolation between the transmitter and receiver. Another embodiment of the present invention utilizes an Interference Cancellation System (ICS) together with duplexers, switches and circulators.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations, distributed antenna systems, access points, repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram of a TD-SCDMA dual-band single PA configuration in a remote radio head unit system in accordance with the present invention.

[007] Figure 2 is a block diagram of the TD-SCDMA dual-band single PA with a Interference Cancellation System (ICS) configuration in a remote radio head unit system in accordance with the present invention.

[008] Figure 3 is a FDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[009] Figure 4 is an Interference Cancellation System using Power Detection.

[0010] Figure 5 is a TDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[0011] Figure 6 is an Interference Cancellation System using Correlation.

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter

AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications

I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

The present invention is a novel RRU system that utilizes a wideband power amplifier. The present invention is a hybrid system of digital and

analog modules. The interplay of the digital and analog modules of the hybrid system eliminates interference between the wideband power amplifier output and the receiver's inputs.. The present invention, therefore, achieves higher Transmitter (Tx) to Receiver (Rx) isolation when using wideband power amplifiers with multiple frequency bands .

Referring first to Figure 1, an embodiment of some aspects of the invention is shown in block diagram form. Figure 1 depicts the analog section of a dual channel RRU. In this embodiment a single wideband power amplifier 404 is used. The two distinct frequency band signals are combined in a duplexer 403 and input to the wideband power amplifier 404. The output of the wideband power amplifier 404 is sent to a diplexer 405 in order to separate the two frequency band signals. This configuration enables the individual transmitter frequency bands to be independently turned-off. The Tx switches 405 and 407 are placed in the signal path after the diplexer 405. The signals are then passed through circulators 411 and 412 and a duplexer 413 in order to gain further isolation between the Tx signals and the Rx signals. The Rx switches 408 and 410 are placed on the third port of the circulator. Alternatively, two or more frequency bands can be combined in one power amplifier using the same architecture as in Figure 1.

Figure 2 illustrates a further alternative embodiment of the dual-band single wideband power amplifier RRU analog section. In the embodiment of Figure 2, an interference cancellation system (ICS) 520 is utilized to improve the isolation between the transmitter and receivers. The interference cancellation system generates a replicate of the unwanted feedback signal but in anti-phase so as to eliminate the interference. The interference

cancellation system comprises five primary blocks: Delay, variable attenuator, variable phase shifter, Down Converter (DNC) and DSP controller, alternative arrangements of which are shown in Figures 4 and 6, discussed hereinafter. The ICS receives incoming signals through links 506 and 507. The anti-phase output of the ICS is combined with the signals from switches Rx1 and Rx2, indicated at 510 and 511, respectively, by the use of adders 551 and 552, and the resulting signal provides the inputs to the LNA's 515 and 516. The ICS is an adaptive control system which continuously adjusts the variable attenuator as well as the variable phase shifter so as to maintain good interference cancellation. Alternatively, an embodiment of the ICS can comprise a fixed attenuator and phase shifter setting, eliminating the need for DSP control, although in at least some cases this results in inferior performance compared to the adaptive ICS system of Figure 2. The remaining elements of Figure 2 correspond to those shown in Figure 1, and are indicated by the same numerals except that the most significant digit has been changed from "4" to "5".

Figure 3 shows another embodiment of the analog section of a dual-band single wideband power amplifier RRU in Frequency Division Duplex (FDD) mode. This embodiment is modulation agnostic for FDD standard systems, and elements 601-604 operate analogously to elements 401-404 of Figure 1. The triplexer 608 separates the transmitter bands from the receiver bands. FDD systems use different transmit and receive frequencies for each channel. The function of the triplexer 608 is to pass the output of power amplifier 604 to the antenna while isolating the receivers from the transmitter output. The ICS 609 system is utilized for increasing the isolation between

the transmitter output and the receiver inputs as with Figure 2, and receives the output of PA 604 through link 605. The output of the ICS 609 is combined with the appropriate triplexer outputs through adders 610 and 611, and the links 605 feeding the LNA's 612 and 613.

Figure 4 is a depiction of one embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. Coupler 605 is used to sample the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 710. This separates the two frequencies into distinct sections. The delay block 701 time-aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 702 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 703 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 707 or Microprocessor is used to control the attenuator and phase shifter. A power detection based adaptive algorithm in the DSP continuously monitors the signal at the Down Converter (DNC) 708 output and minimizes the level of the interference based on the detected power level . The power level of the interference is measured at the receiver while that band is in the transmit mode of operation. The second band is similarly processed using elements 704, 705 and 706.

Figure 5 shows an embodiment of the analog section of a dual-band single wideband power amplifier RRU in Time Division Duplex (TDD) mode.

This embodiment is modulation agnostic for TDD standard systems. The output of wideband power amplifier 804 feeds a circulator 807. The circulator provides some isolation between the transmitted signals and the receiver inputs. A multi-band filter 820 is placed between the circulator and the output antenna in order to attenuate out-of-band emissions. The third port of the circulator 807 is delivered to a diplexer 808, which separates the two distinct operating bands. TDD mode requires the transmitter and receiver to operate using the same frequency band at distinct times. In order to provide isolation between the transmitter and receiver, switches 821, 822 are used. The switches can provide some isolation but additional isolation may be required depending on the system specifications. The ICS 809 can provide additional isolation between the transmitter output and the receiver inputs in the manner described above.

Figure 6 is a depiction of another embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 910. This separates the two frequencies into distinct sections. The delay block 901 time aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 902 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 903 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 907 or Microprocessor is used to control the attenuator and

phase shifter. A correlation-based adaptive algorithm in the DSP is used to minimize the level of interference. The DSP correlates the two signals by controlling the output of switch 911 and the output of switch 912 after the signals have been translated to baseband using the two Downconverters 920 and 909. The switches 911 and 912 alternate between the two channels. The objective of the algorithm is to minimize the correlation between the sampled power amplifier output and the interference at the receiver. The computed correlation coefficient is used as the error function in an adaptive algorithm such as a Least Mean Squared (LMS) algorithm.

[001] From the foregoing teachings, those skilled in the art will appreciate that the RRU system of the present invention enables the use of single wideband power amplifier for multi-band operation , which consequently saves hardware resources and reduces costs. The RRU system is also reconfigurable and field-programmable since the algorithms can be adjusted like software in the digital processor at anytime.

[002] Moreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-frequency bands and multi-channels.

[003] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such

substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A remote radio head unit (RRU) system for multiple operating frequency bands, multi-channels, driven by a single or more wide band power amplifiers. More specifically, the present invention enables multiple-bands RRU to use fewer power amplifers in order to reduce size and cost of the multi-band RRU. The present invention is based on the method of using duplexers and/or interference cancellation system technique to increase the isolation between the transmitter signal and receiver signal of the RRU.

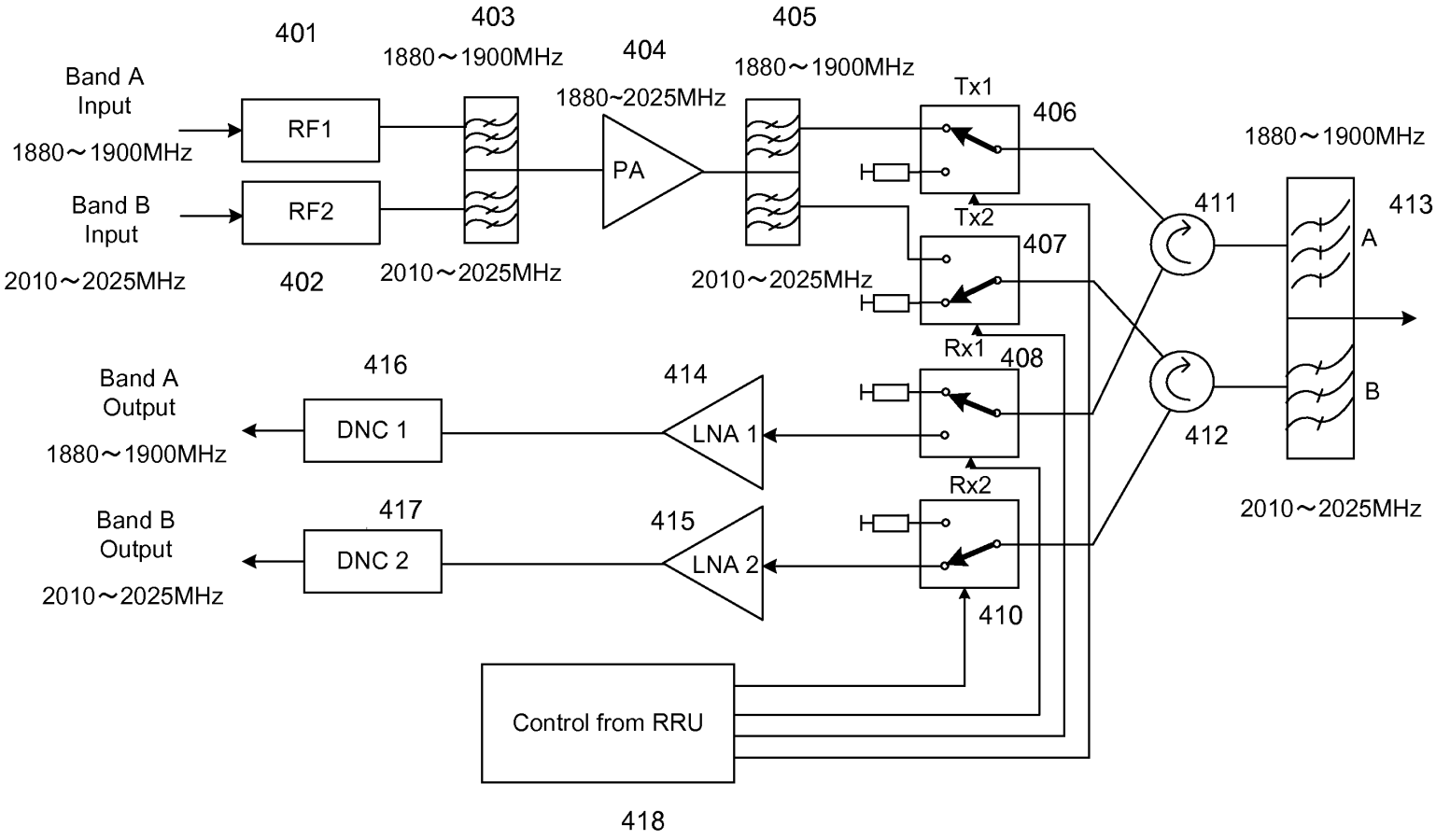


Figure 1: Dual Band TD-SCDMA RRU

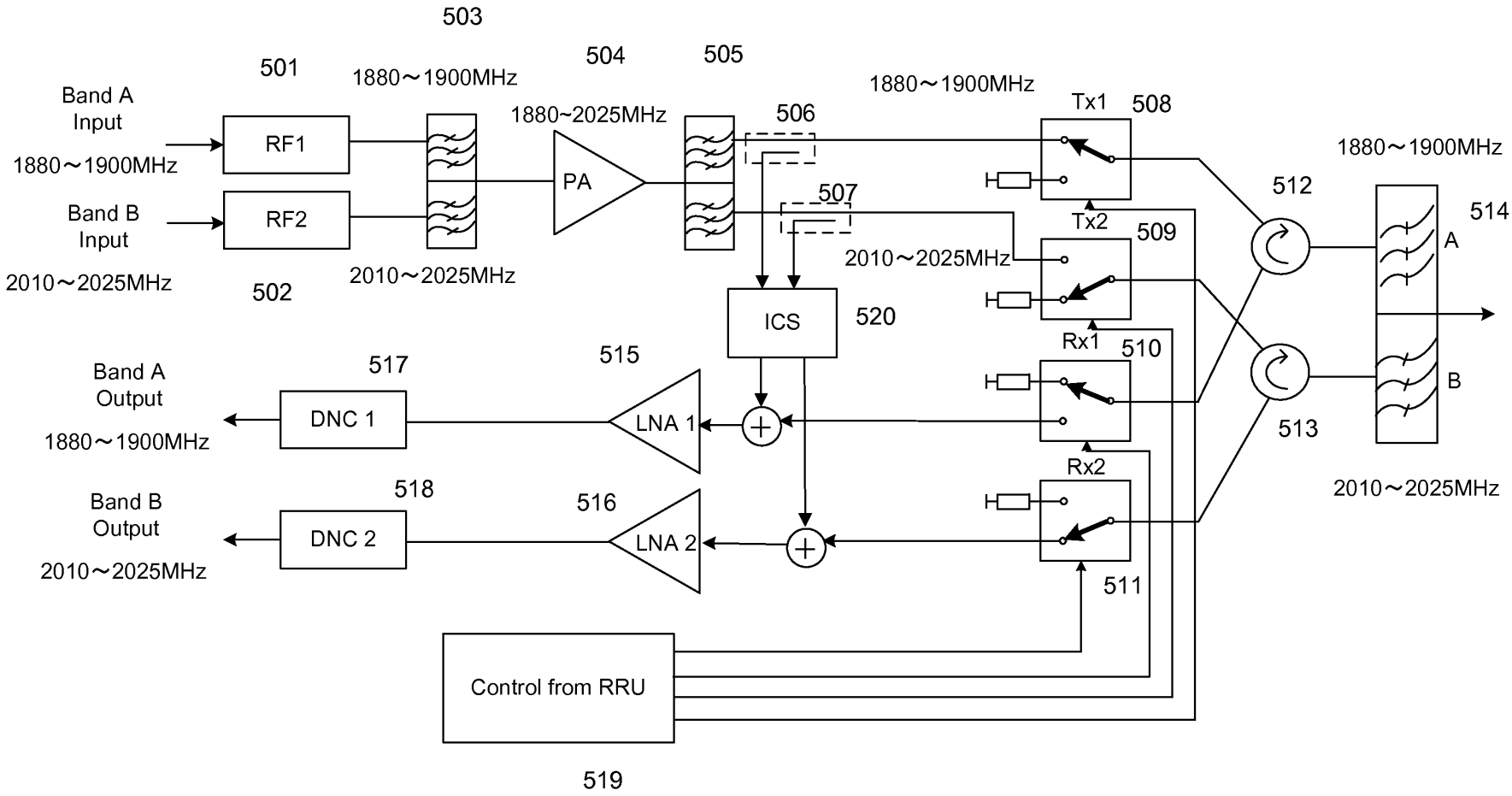


Figure 2: Dual Band TD-SCDMA RRU with Interference Cancellation System

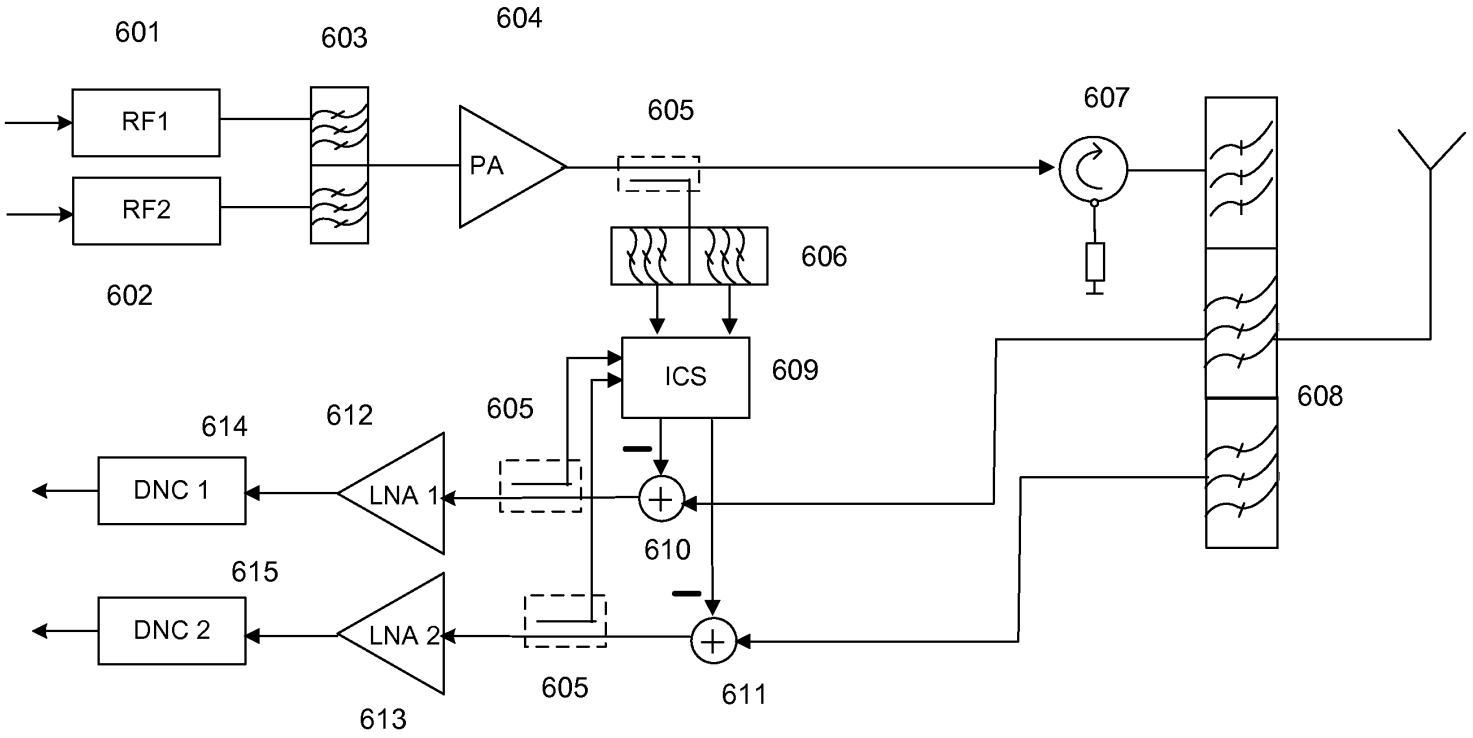


Figure 3: FDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

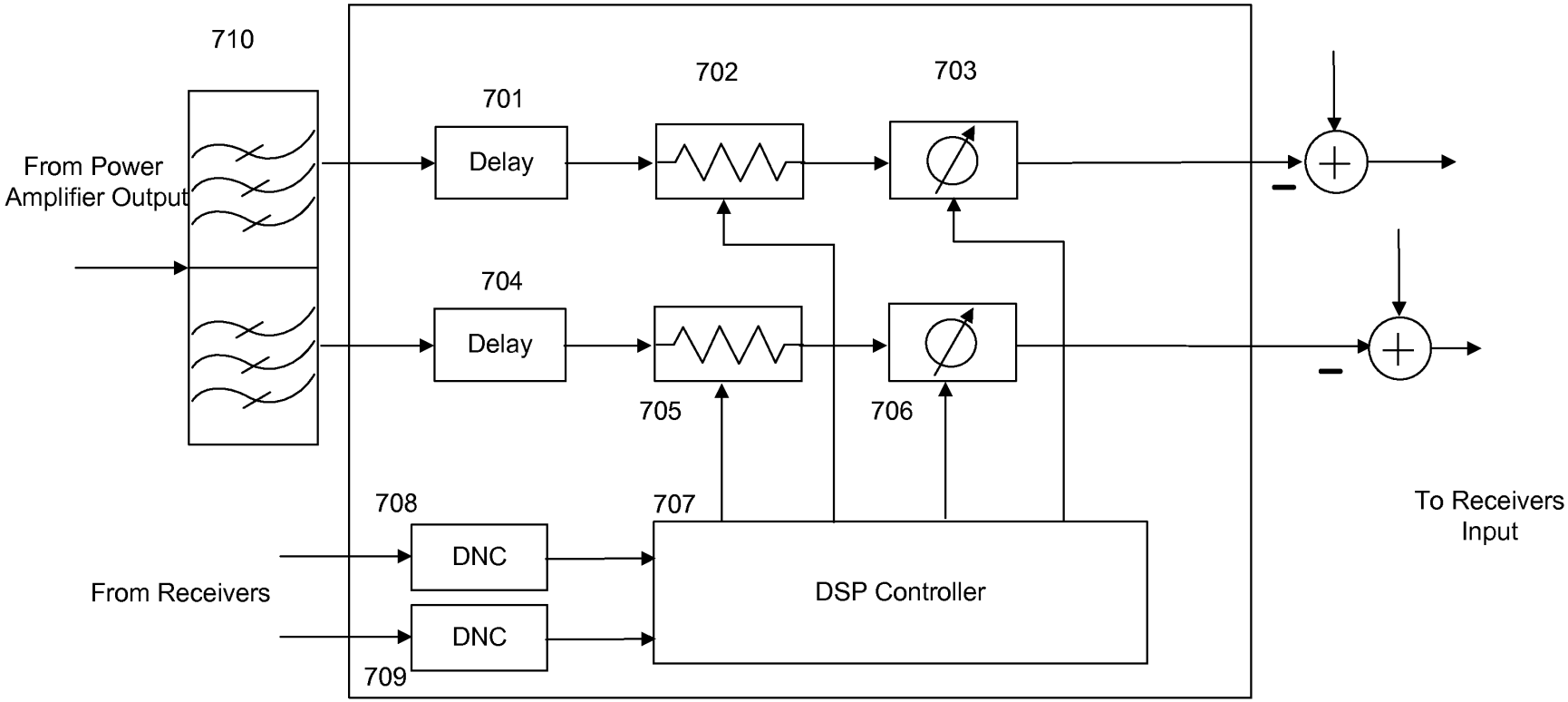


Figure 4: Dual-Band Interference Cancellation System using power detection

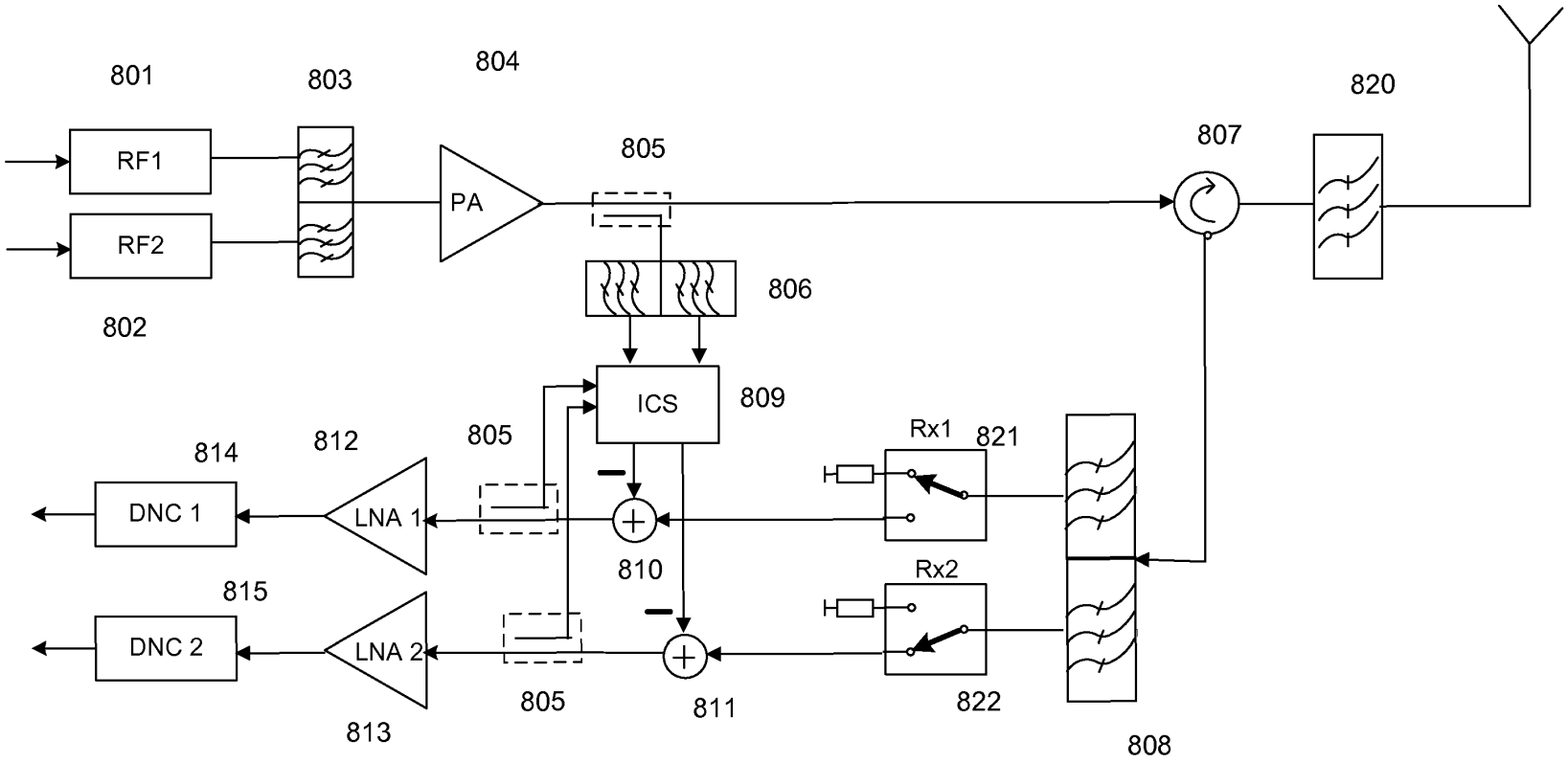


Figure 5: TDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

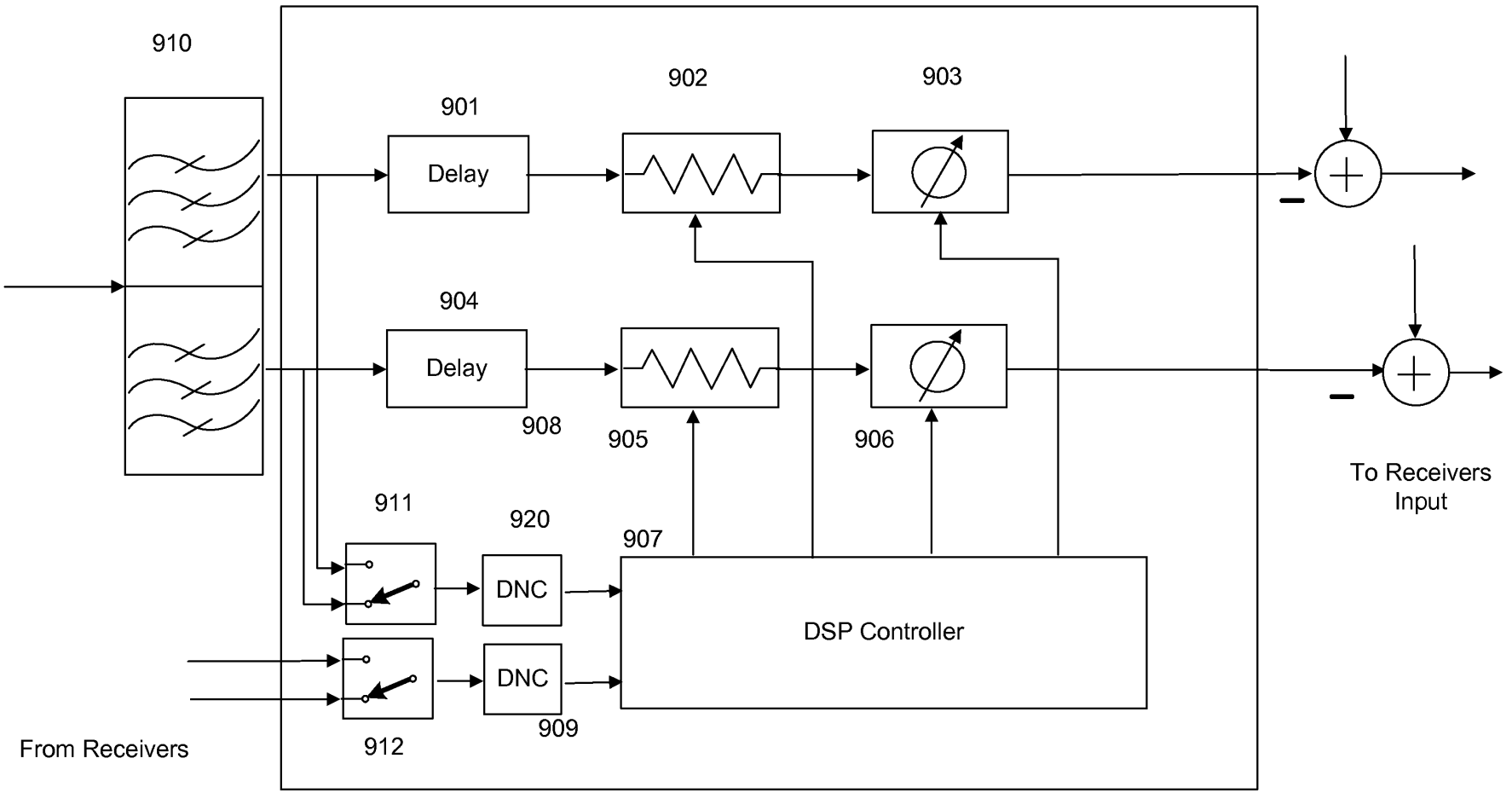


Figure 6: Dual-Band Interference Cancellation System using Correlation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD

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SPECIFICATION

RELATED APPLICATIONS

[001] This application claims the benefit of the following applications:

[002] US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

[003] US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

[004] US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

[005] US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

[006] US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

[007] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

[008] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

[0009] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

[0010] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

[0011] All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[0012] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[0013] A wideband mobile communication system using complex modulation techniques, such as wideband code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. The conventional feedforward linear power amplifier (FFLPA) has been widely utilized due to its excellent linearity performance in spite of poor power efficiency.

[0014] Conventional FFLPAs are mainly based on the principle of error subtraction and power-matching with dedicated hardware circuitries to realize non-linear corrections to PA. These approaches must use an auxiliary PA and complicated hardware circuitries to match exactly the transmitted power-balance, time-delay and errors generated by the main PA. After a perfect matching is obtained, the non-linear distortion errors from the main PA can then be canceled by those distortion errors from the auxiliary PA. Due to the complexities of the nonlinear predistortion circuits, which among other things involve many variables and parameters, FFLPAs require significant fine tuning and other calibration efforts. In addition, such traditional FFLPA schemes are also vulnerable to fluctuating environmental conditions, such as temperature and humidity changes, since perfect alignment of the main PA's signal and that of the auxiliary PA are vital. As a result, traditional predistortion schemes are costly to implement and are limited in their predistortion accuracy and stability in a commercial wireless system environment.

[0015] In order to overcome the FFLPA's poor efficiency, digital baseband predistortion (PD) has been demonstrated due to the recent advances in digital signal processing (DSP) technology. In addition, Doherty power amplifiers (DPA) have also been applied to these linearization systems to improve power efficiency. However, there is still a demand for higher performance of the power amplifier such as more linearity and better efficiency with less expensive architecture.

[0016] Conventional DSP-based PD schemes utilize digital microprocessors to compute, calculate and correct the PA's nonlinearities, typically by performing fast tracking and adjustments of signals in the PA system. However, conventional DSP-based PD schemes are challenged by

variations of the linearity performance of the amplifier due to changes in the environment such as temperature and the asymmetric distortions of the output signal of the PA resulting from memory effects. All of these variations and distortions have to be compensated for. Conventional PD algorithms are based on a wideband feedback signal, and require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. In addition, time-synchronizations are typically required to capture an error signal between a reference signal and a distorted signal. This time-matching process may result in small synchronization errors which can further affect conventional PD schemes' linearization performance. Amplitude and phase synchronization is also required in order to align the reference signal and the distorted signal.

[0017] Moreover, conventional PD schemes necessitate coded in-phase (I) and quadrature (Q) channel signals in the baseband as the required ideal or reference signals. As a result, conventional PD schemes are often standard or modulation specific and must be closely tailored to each baseband system. Therefore, in order to deploy conventional PD schemes into base-stations, the PD engines must be embedded into the baseband architecture of base-stations. This embedment is a practical implementation challenge since it is frequently inconvenient or impossible to modify the baseband architectures of existing base-stations or base-station designs. Once the PD scheme is set up for a specific base-station design, it is often not reconfigurable and hence not upgradeable to future changes in standards or modulations. Furthermore, since traditional PD approaches require baseband I-Q signal sources to operate, they are inapplicable to certain RF systems that

do not possess any baseband I-Q signal sources, such as repeater and indoor signal coverage sub-systems.

SUMMARY OF THE INVENTION

[0018] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for wideband communication system applications. The present disclosure provides a field-reconfigurable power amplifier system that supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. In multi-channel configurations of the present invention there can be more than one PA for multiple bands.

[0019] To achieve the above objects, the present invention is generally based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[0020] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[0021] Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

[0022] A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are sampled in a feedback path and controlled by the adaptation algorithm in a digital module. Therefore, in an embodiment, the present invention is capable of compensating for the nonlinearities as well as memory effects of power amplifier systems and also improves performance, in terms of power added efficiency, adjacent channel leakage ratio (ACLR) and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

THE FIGURES

[0023] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0024] Figure 1 is a block diagram showing the basic form of a digital hybrid mode power amplifier system.

[0025] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0026] Figure 3 is a block diagram showing polynomial-based predistortion in a digital hybrid mode power amplifier system of the present invention.

[0027] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a digital hybrid mode power amplifier system of the present invention.

[0028] Figure 5 is a delay estimation block diagram of the present invention.

[0029] Figure 6 is a block diagram of a fractional delay for the present invention.

[0030] Figure 7 is a block diagram showing a digital hybrid mode power amplifier system implemented with a down converter (DNC) and UPC-based clipping error restoration path according to another embodiment of the present invention..

[0031] Figure 8 is a block diagram showing a digital hybrid mode power amplifier system implemented with a DNC and an analog quadrature modulator (AQM) according to another embodiment of the present invention.

Figure 9 is a block diagram showing an embodiment of the analog quadrature modulator compensation structure.

GLOSSARY

The acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter

EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access

WLAN Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0032] The present invention is a novel RF-out PA system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[0033] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention is a “black box”, plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a digital hybrid mode power amplifier (DHMPA) system hereinafter.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows in block diagram form an embodiment of a linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3), and complies with the formula:

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4.

[0034] FIG 3. is a block diagram showing a predistortion (PD) part in the DHMPA system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 and in embodiments disclosed in FIG. 7 and FIG. 8, discussed below, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the DHMPA system in FIG. 3 has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

Delay Estimation Algorithm:

The DPD estimator compares $x(n)$ and its corresponding feedback signal $y(n-\Delta d)$ to find the DPD coefficients, where Δd is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $x(n)$, and feedback data, $y(n)$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign(y(i+m+1) - y(i+m))$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $C(m)$ is the feedback path delay. The delay estimation block is shown in Figure 5.

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is necessary. To simplify the design, only a half-sample delay is considered in this design, as shown in Figure 6. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel. The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{j\theta_o,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{j\theta_o}$$

Magnitude correction:

As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

In this design, N is chosen to be 4096. The choice of N will depend on the desired accuracy.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^{j}$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = k_a k_b / k_a'$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & \frac{}{d(i)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_i^{1/2}} & \frac{0}{} \\ \overline{q_i^*} & \overline{e_a^*(i)\gamma^{\frac{1}{2}}(i)} \\ \overline{h_i \Phi_i^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(i)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{\frac{*}{2}}}[w_i - \bar{w}] = \overline{q_i}$$

In the iterative process, a block of data (in this design, there are 4096 data in one block) is stored in memory, and the algorithm uses all the data in

memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data is processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficients as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

[0035] Figures 7 and 8 are block diagrams showing more sophisticated embodiments of DHMPA system, where like elements are indicated with like numerals and elements not numbered in Figure 8 have the same reference numerals as shown in Figure 7. The embodiments of Figures 7and 8 apply crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is

included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0036] Figure 7 is a block diagram showing a DHMPA system implemented with DQM in accordance with an embodiment of the present invention (the "FIG. 7. System"). The system shown in Figure 7 has a dual mode of RF-in 700 and/or multi-carrier digital signal 705 at the input, and an RF signal at the output 710. The dual mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode"). The FIG. 7. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 715, a power amplifier module 760 and a feedback path 725.

[0037] The FPGA-based Digital part comprises a digital processor 715 (e.g. FPGA), digital-to-analog converters 735 (DACs), analog-to-digital converters 740 (ADCs), and a phase-locked loop (PLL) 745. Since the FIG. 7 System has a dual input mode, the digital processor has two paths of signal processing. For the RF signal input path, the digital processor has implemented a digital quadrature demodulator (DQDM), a CFR, a PD, and a digital quadrature modulator (DQM). For the baseband digital input path, a digital up-converter (DUC), CFR, PD, and a DQM are implemented.

[0038] The RF-in Mode of the FIG. 7. System has implemented a down converter (DNC) 750 prior to the FPGA-based Digital part and an ADC 740 prior to the FPGA. An analog down converted signal is provided to the FPGA-based Digital module and converted to a digital signal by the ADC 740. The digitally converted signal is demodulated by the DQDM to generate both real and imaginary signals and then PAPR of the signal is reduced by CFR. The peak reduced signal is predistorted to linearize the amplifier and is

passed through a DQM to generate the real signal and then converted to an intermediate frequency (IF) analog signal by a DAC in the FPGA-based Digital part. However, it is not required in all embodiments to implement DQDM and DQM in the FPGA. If, as shown in Figures 7 and 8, a digital modulator will not be used, then two DAC's 801 behind the FPGA feeding AQM module 800 can be used to generate real and imaginary signals, respectively (the "AQM Implementation").

[0039] The Baseband-in Mode of FIG. 7. works slightly different from the RF-in Mode. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. From this point onwards, the Baseband-in Mode and RF-in Mode proceeds identically. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0040] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a synchronizing the wideband captured output signal from the feedback path 725 with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. . The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DAC 740 as shown. As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. Alternatively, if the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to

generate real and imaginary signals, respectively. The gate bias voltage 753 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 535 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. .

[0041] The power amplifier part comprises a UPC for a real signal (such as illustrated in the embodiment shown in Figures 7), or an AQM for real and complex signals (such as the embodiment of a DHMPA system depicted in Figure 8) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental DHMPA system. One such Doherty power amplifier technique is presented in commonly assigned U.S. Provisional Patent Application S.N. 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference, together with U.S. Patent Application S.N. 12/603,419, filed 10/21/2009, entitled N-Way Doherty Distributed Power Amplifier with Power Tracking. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0042] The feedback portion comprises a directional coupler, a mixer, a gain amplifier, a band pass filter (BPF), and a Digital to Analog Converter (DAC). Depending upon the embodiment, these analog components can be

mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the the gain amplifier, and the BPF (e.g., surface acoustic wave filter) which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the digital PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the detector 580 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, discussed above, which shows a polynomial-based predistortion algorithm and from Figure 4, also discussed above, which shows the block diagram of the digital predistorter synchronization algorithm which can be used in some embodiments of the invention.

[0043] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 790, hence maximizing the DHMPA system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC 735 in the FPGA-

based Digital portion and an extra UPC 720 in the power amplifier part (see FIG. 7. & 8.). The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0044] Referring again to Figure 7, the RF input signal is first down-converted to baseband digital signals, and then digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz). If the system of Figure 7 has a Baseband-in Mode, then the digital data streams from multi-channels are digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz) directly as they enter the digital processor. The CFR then reduces the PAPR. The peak-reduced signal is predistorted to linearize the DPA and is passing through two DACs for real and imaginary signals and finally through an AQM.

[0045] FIG. 9. is a block diagram showing an embodiment of the analog quadrature modulator compensation structure. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12, g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2. The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

[0046] The configuration of the power amplifier part and the feedback part of the system shown in FIG. 8 are the same as for the system shown in FIG. 7.

[0047] In FIG. 8 System, the DNC frequency translates the RF signal into a low IF signal. The IF signal is then presented to the ADC whereupon it is digitally down-converted to baseband followed by CFR and predistortion (PD). The output of the PD is a baseband signal which will then be digitally upconverted to an IF frequency and presented to the DAC. The output of the DAC is then further frequency translated to a RF frequency through the up-converter (UPC.) The configuration of the power amplifier part and the feedback part of FIG. 8 System are the same as for the FIG. 7 System.

[0048] In summary, the DHMPA system of the present invention enhances efficiency and linearity relative to the prior art since the DHMPA system is able to implement CFR, DPD and adaptation algorithms in one digital processor, which consequently saves hardware resources and processing time. The DHMPA system is also reconfigurable and field-programmable since the algorithms and power-efficiency-enhancing features can be adjusted like software in the digital processor at anytime.

[0049] Furthermore, since the DHMPA system accepts RF modulated signal as input, it is not necessary to use coded I and Q channel signals in the baseband. Therefore, the performance of wireless base-station systems can be enhanced simply by replacing the existing PA modules with the DHMPA. The result is that the present invention provides a “plug and play” PA system solution such that the structure of existing base-station systems does not

need to be modified or rebuilt for a new set of signal channels in order to benefit from high efficiency and high linearity PA system performance.

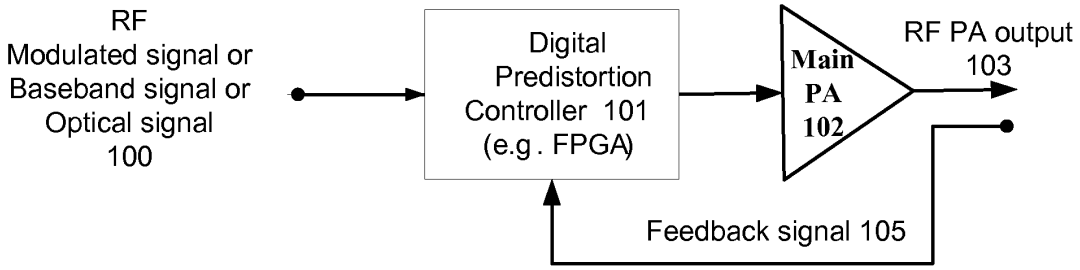
[0050] Moreover, the DHMPA system is agnostic to modulation schemes such as quadrature phase shift keying (QPSK), quadrature amplitude modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM), etc. in code division multiple access (CDMA), global system for wireless communications (GSM), WCDMA, CDMA2000, and wireless LAN systems. This means that the DHMPA system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DHMPA system of the present invention include correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0051] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

FIG. 1. Basic Digital Hybrid Mode Power Amplifier System



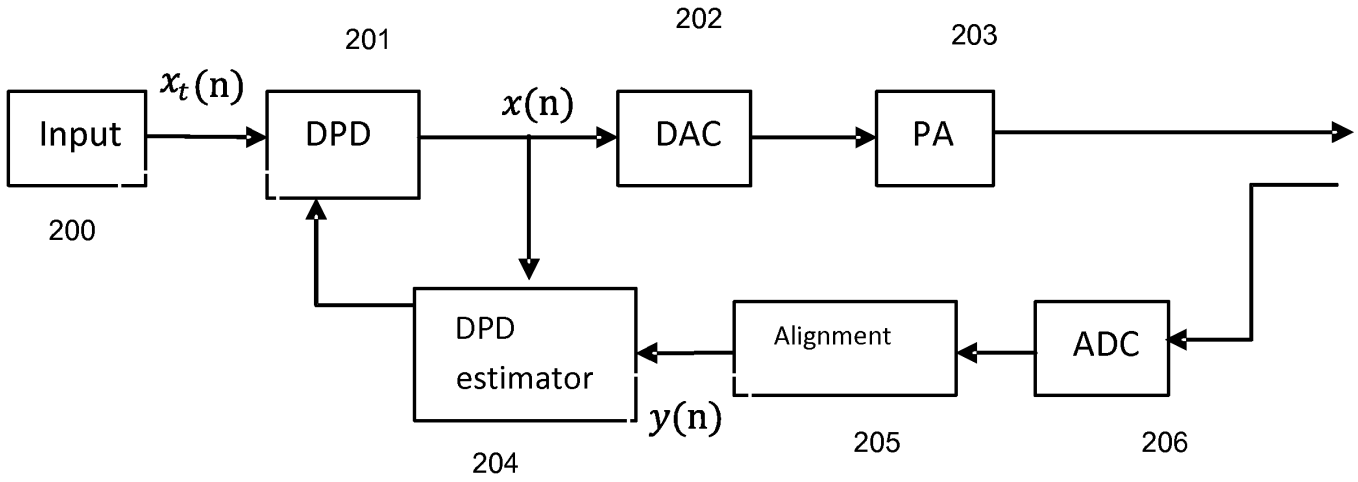


FIG. 2. Digital Predistortion Block Diagram

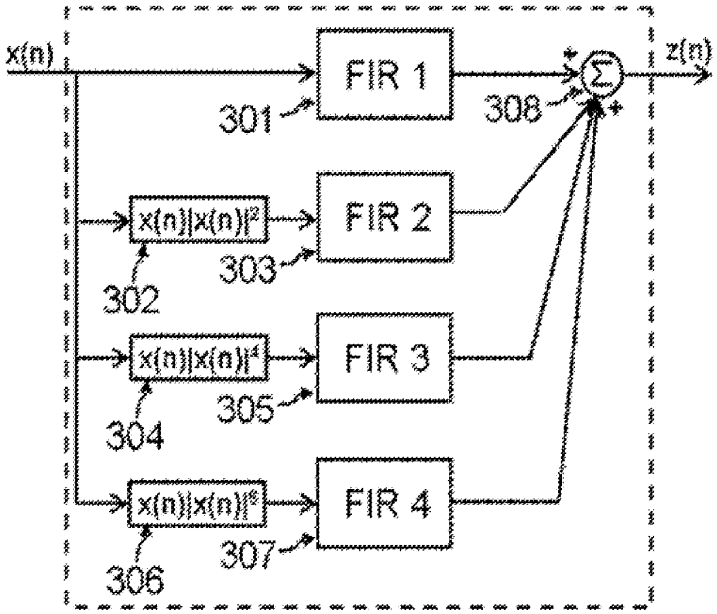


FIG. 3. Polynomial based PD in an embodiment of Digital Hybrid Mode Predistortion PA System

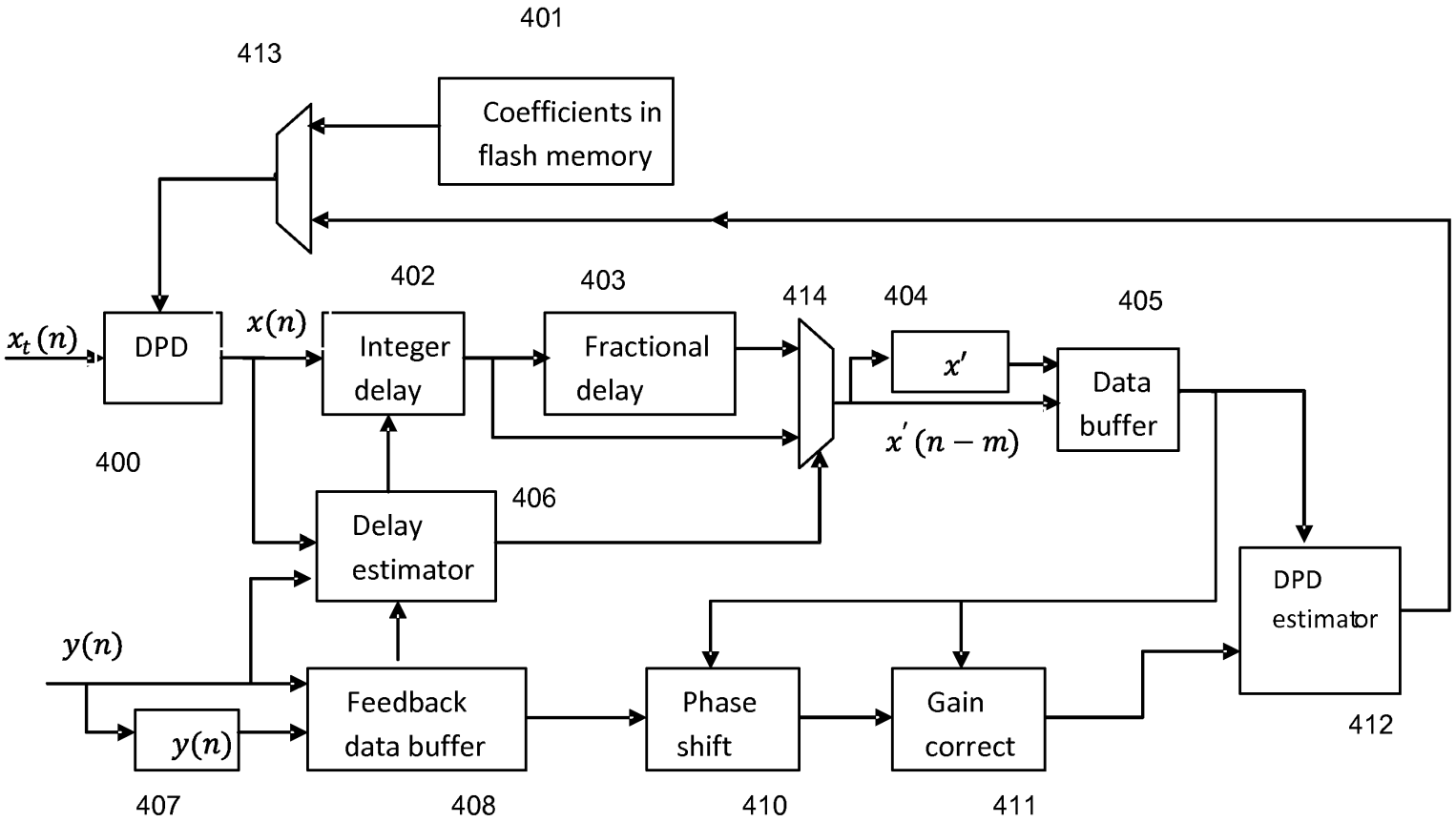


FIG. 4. Digital Predistortion Algorithm

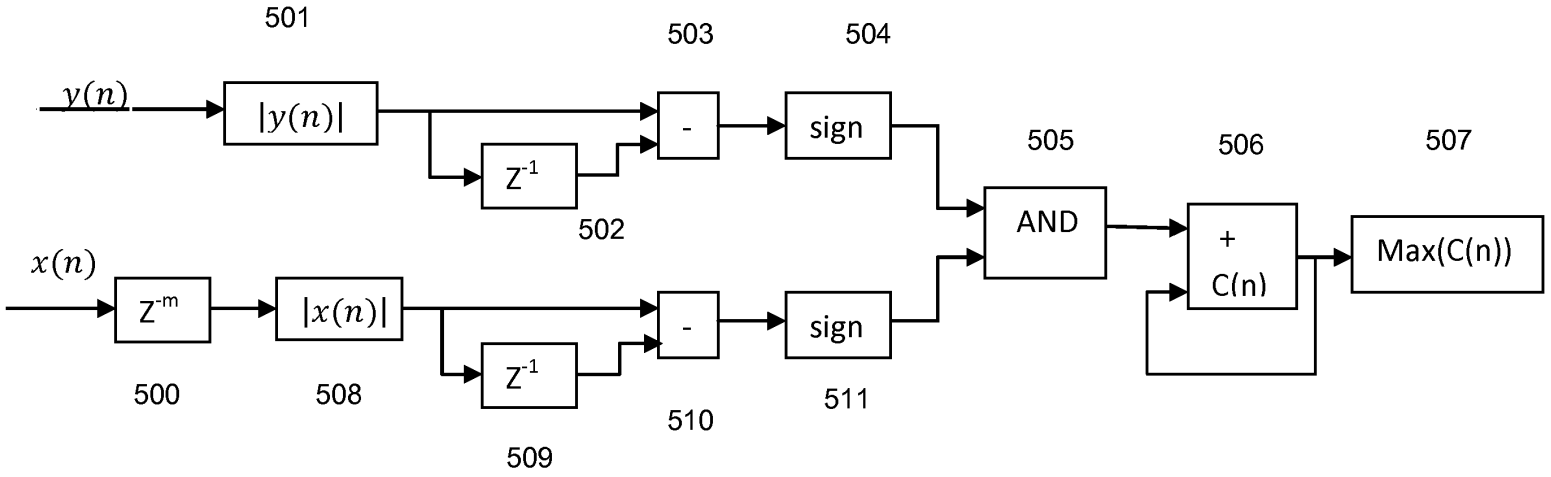


FIG. 5. Delay Estimation Block

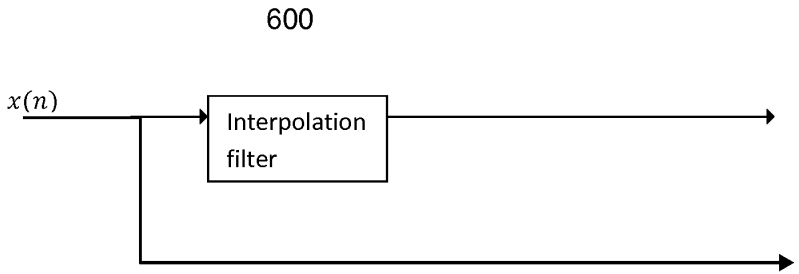


Figure 6 Fractional Delay Block

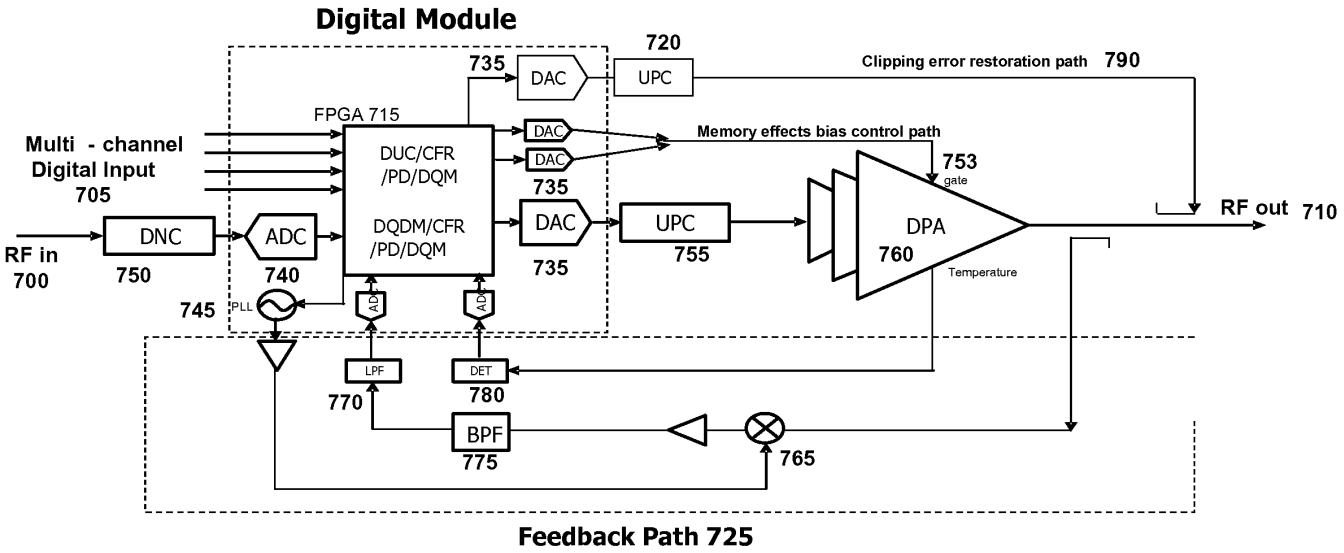


FIG. 7. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input

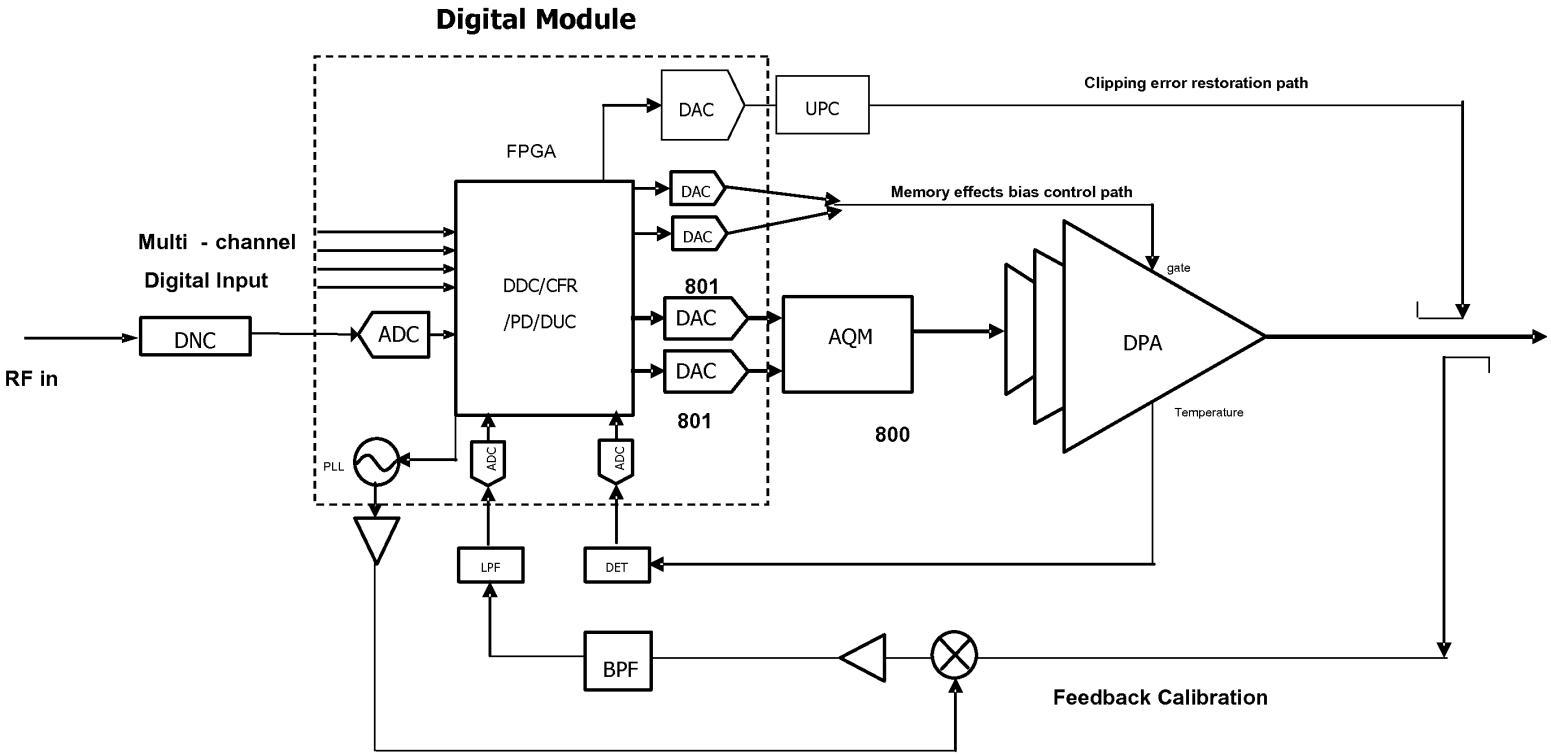


FIG. 8. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input, with Feedback Calibration

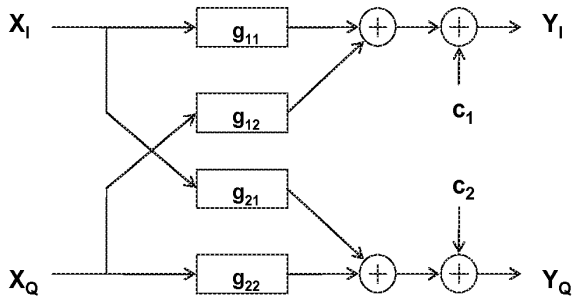


Figure 9 Analog Quadrature Modulator Compensation Block

DW-1022P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM

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SPECIFICATION

RELATED APPLICATIONS

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems employing Distributed Antenna Systems (DAS). More specifically, the present invention relates to a DAS which is part of a distributed wireless network

base station in which all radio-related functions that provide network coverage and/or capacity for a given area are contained in a small single unit that can be deployed in a location remote from the remaining distributed wireless network base station unit or units which are not performing radio-related functions. Multi-mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA, UMTS and WiMAX standards with advanced software configurability are features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multiple operators and multi-frequency bands per operator within a single DAS to reduce the costs associated with radio network equipment and radio network deployment.

BACKGROUND OF THE INVENTION

[002] Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users requires end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G and other advanced network capabilities. Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting these higher bandwidth requirements are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must deal with the limited availability of new spectrum,

leverage existing spectrum, and ensure operation of all desired wireless technology standards. The processes of scarce resource optimization while ensuring a future-proof implementation must both take place at the same time during the transition phase, which usually spans many years and thus can encompass numerous future developments. Distributed open base station architecture concepts have evolved in parallel with the evolution of the various technology standards to provide a flexible, lower-cost, and more scalable modular environment for managing the radio access evolution. Such advanced base station architectures can generally be appreciated from Figure 1 [PRIOR ART], which shows an architecture for a prior art Distributed Wireless Network Base Station. In Figure 1, 100 is a depiction of a Distributed Wireless Network Base Station. The Base Transceiver Station (BTS) or Digital Access Unit (DAU) 101 coordinates the communication between the Remote Radio Head Units 102, 103 and the Base Station Controller (BSC). The BTS communicates with multiple Remote Radio Heads via optical fiber. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI), and the IR Interface standards introduced publicly-defined interfaces separating the Base Transceiver Station (BTS) or Digital Access Unit and the remote radio head unit (RRU) parts of a base station by employing optical fiber transport.

[003] The RRU concept constitutes a fundamental part of an advanced state-of-the-art base station architecture. RRU-based system implementation is driven by the need to achieve consistent reductions in both Capital Expenses (CAPEX) and Operating Expenses (OPEX), and enable a more optimized, energy-efficient, and greener base deployment. An existing application employs an architecture where a 2G/3G/4G base station is connected to RRUs over

multiple optical fibers. Either CPRI, OBSAI or IR Interfaces may be used to carry RF data to the RRUs to cover a sectorized radio network coverage area corresponding to a radio cell site. A typical implementation for a three-sector cell employs three RRU's. The RRU incorporates a large number of digital interfacing and processing functions. However, commercially available RRU's are power inefficient, costly and inflexible. Their poor DC-to-RF power conversion insures that they will need to have a large mechanical housing to help dissipate the heat generated. The demands from wireless service providers for future RRU's also includes greater flexibility in the RRU platform, which is not presently available. As standards evolve, there will be a need for multi-band RRUs that can accommodate two or more operators using a single wideband power amplifier. Co-locating multiple operators in one DAS system would reduce the infrastructure costs and centralize the Remote Monitoring Function of multiple Operators on the Network. To accommodate multiple operators and multiple bands per operator would require a very high optical data rate to the RRUs which is not achievable with prior art designs.

SUMMARY OF THE INVENTION

[004] The present invention substantially overcomes the limitations of the prior art discussed above. Accordingly, it is an object of the present invention to provide a high performance, cost-effective DAS system, architecture and method for an RRU-based approach which enables each of multiple operators to use multi-frequency bands. The present disclosure enables a RRU to be field reconfigurable, as presented in US Patent application US 61/172,642 (DW-1016P), filed 4/24/2009, entitled Remotely Reconfigurable Power Amplifier

System and Method, US Patent application US 12/108,502 (DW-1011U), filed 4/23/2008, entitled Digital Hybrid Mode Power Amplifier System, US Patent application SN 61/288,838 (DW-1018P), filed 12/21/2009, entitled Multi-band Wideband Power Amplifier Digital Predistortion System, US Patent application SN 61/288,840 (DW-1019P), filed 12/21/2009, entitled Remote Radio Head Unit with Wideband Power Amplifier and Method, US Patent application SN 61/288,844 (DW-1020P), filed 12/21/2009, entitled Modulation Agnostic Digital Hybrid Mode Power Amplifier System, and US Patent application SN 61/288,847 (DW-1021P), filed 12/21/2009, entitled High Efficiency Remotely Reconfigurable Remote Radio Head Unit System and Method for Wireless Communications, all of which are incorporated herein by reference. In addition, the system and method of the present invention supports multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands, and multi-channels. To achieve the above objects, the present invention maximizes the data rate to the Remote Radio Head Unit in a cost effective architecture. Figures 2 and 3 depict a low power RRU and high power RRU. The RRUs depicted in Figures 2 and 3 can be extended to a multi-band and multi-channel configuration. Multi-band implies more than two frequency bands and multi-channel implies more than one output to an antenna system. Various embodiments of the invention are disclosed.

[005] An embodiment of the present invention utilizes a RRU Access Module. The objective of the access module is to de-multiplex and multiplex high speed data to achieve aggregate data rates sufficient for operation of a plurality of RRU Band Modules which are geographically distributed. An alternative embodiment of the present invention utilizes the physical separation of the RRU Band Modules from the RRU Access Module using an optical fiber cable,

Ethernet cables, RF cable and any other form of connection between the modules. In an alternative embodiment, a Remote Radio Unit comprised of one or more RRU Band Modules may be collocated with the antenna or antennas. In a further alternative embodiment, the RRU Access Module can also supply DC power on the interconnection cabling. In other aspects of the invention, control and measurement algorithms are implemented to permit improved network deployment, network management, and optimization.

[006] Applications of the present invention are suitable to be employed with all wireless base-stations, remote radio heads, distributed base stations, distributed antenna systems, access points, repeaters, distributed repeaters, optical repeaters, digital repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

[007] Appendix I is a glossary of terms used herein, including acronyms.

THE FIGURES

[008] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[009] Figure 1 [PRIOR ART] is a block diagram showing the basic structure of a prior art Distributed Wireless Base Station system.

[0010] Figure 2 is a block diagram showing a multi-channel High Power Remote Radio Head Unit according to one embodiment of the present invention.

[0011] Figure 3 is a block diagram multi-channel High Power Remote Radio Head Unit according to one embodiment of the present invention.

[0012] Figure 4 is a block diagram of a Remote Radio Head Unit high level system of the present invention.

[0013] Figure 5 is a block diagram of the Remote Radio Head Unit Access Module of the present invention.

[0014] Figure 6 is a Remote Radio Head Unit Band Module according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention is a novel Distributed Antenna System that utilizes a high speed Remote Radio Head Unit Access Module interconnected with Remote Radio Head Unit Band Module.

[0016] An embodiment of a Remote Radio Head Unit in accordance with the invention is shown in Figure 2. Fiber 1, indicated at 200A, is a high speed fiber cable that transports data between the BTS and the Remote Radio Head Unit. Fiber 2, indicated at 200B, is used to daisy chain other remote radio head units which are thereby interconnected to the BTS or DAU. The software-defined digital platform 216 performs baseband signal processing, typically in an FPGA or equivalent. Building block 203 is a Serializer/Deserializer. The deserializer portion extracts the serial input bit stream from the optical fiber 201 and converts it into a parallel bit stream. The serializer portion performs the inverse operation for sending data from the Remote Radio Head Unit to the BTS. In an embodiment, the two distinct bit streams communicate with the BTS using

different optical wavelengths over one fiber, although multiple fibers can be used in alternative arrangements. The deframer 204 deciphers the structure of the incoming bit stream and sends the deframed data to the Crest Factor Reduction Algorithm 209. The Crest Factor Reduction block 209 reduces the Peak-to-Average Ratio of the incoming signal so as to improve the Power amplifier DC-to-RF conversion efficiency. The waveform is then presented to the Digital Predistorter block 208. The digital predistorter compensates for the nonlinearities of the Power Amplifier 221 in an adaptive feedback loop. Digital Upconverter 210 filters and digitally translates the deframed signal to an IF frequency. The Framer 204 takes the data from the two digital downconverters 206, 207 and packs it into a Frame for transmission to the BTS over the optical fiber 201. Elements 211 and 212 are Analog to Digital converters that are used to translate the two analog receive signals into digital signals. The receiver comprises a diversity branch which contains a downconverter 217 and a Band Pass Filter 223. The main branch has a receiver path comprised of a duplexer 224 and a downconverter 218.

[0017] The power amplifier has an output coupler for extracting a replica of the output signal in the feedback path. The feedback signal is frequency-translated by downconverter 219 to either an IF frequency or baseband and presented to an Analog to Digital converter 213. This feedback signal is used in an adaptive loop for performing Digital Predistortion to compensate for any nonlinearities created by the power amplifier.

[0018] The Ethernet cable is used to locally communicate with the Remote Radio Head Unit. Switch 226 is used to allow easy access to either the FPGA or the CPU. DC power converters 228 and 229 are used to obtain the desired DC voltages for the Remote Radio Head Unit. Either an external voltage can be

connected directly into the RRU or the DC power may be supplied through the Ethernet cable.

[0019] Although the description of the instant embodiment is directed to an application where a second optical fiber connection provides a capability for daisy chaining to other Remote Radio Head Units, an alternative embodiment provides multiple optical fiber connections to support a modified "hybrid star" configuration for appropriate applications which dictate this particular optical transport network configuration.

[0020] Figure 3 depicts a remote radio head unit. In at least some designs, this architecture offers benefits when the RF output power is relatively low. In the embodiment shown in Figure 3, digital predistrortion and crest factor reduction are not employed as was the case in Figure 2. Even though this topology shows a non-diversity configuration, a diversity receive branch can be added along with an additional transmitter path for development of a Multiple Input Multiple Output (MIMO) Remote Radio Head Unit.

[0021] The Remote Radio Head Unit high level system is shown in Figure 4. It comprises a Remote Radio Head Unit Access Module 400 which communicates directly with the BTS or DAU. The function of the Remote Radio Head Unit Access Module 400 is to route the high speed data (at any desired speed, e.g., such as 10 Gbps as illustrated in Fig. 4) (the "Data Speed") to the multiple Remote Radio Head Unit Band Modules and allows for local communications with them via Ethernet. A backplane 401 is used to interconnect the Remote Radio Head Unit Access Module 400 with the various Remote Radio Head Unit Band Modules 402,403,404,405 at any speed lower than the Data Speed (e.g., less than or equal to 3Gbps as illustrated in Fig. 4). The output ports of the Remote Radio Head Unit Band Modules are combined

and sent to an antenna for transmission. An alternative embodiment is described as follows. Although the description of instant embodiment is directed to applications for up to four Remote Radio Head Unit Band Modules, an alternative embodiment involves feeding a much larger quantity of Remote Radio Head Unit Band Modules with signals of various bandwidths at various frequency bands covering multiple octaves of frequency range, to support a wide range of applications including location-based services, mobile internet, public safety communications, private enterprise telecommunications and broadband, and other wireless applications. The system can in theory support an infinite quantity of RRUs. Also, the Remote Radio Head Unit Band Modules may be set up remotely to have RF power values selected based on the specific desired applications as well as location-specific radio signal propagation factors. A further alternative embodiment leverages the flexibility of the architecture shown in Figure 4 to provide a capability known as Flexible Simulcast. With Flexible Simulcast, the amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular RRU or group of RRUs by each RRU Access Module can be set via software control to meet desired capacity and throughput objectives or wireless subscriber needs.

[0022] The detailed topology of the Remote Radio Head Unit Access Module is shown in Figure 5. It comprises a Small form Factor Pluggable optic transceiver (SFP) 500 which operates on two distinct wavelengths, one for communicating from the BTS to the Remote Radio Head Unit Access Module and the other for communicating in the opposite direction. The SFP contains a Laser Diode for converting the electronic signal to a digital optical signal and an Optical detector for converting the digital optical signal into an electronic signal.

A multiplexer/demultiplexer 501 converts the high speed data to multiple lower speed data paths for delivery to a FPGA 502. The multiplexer/demultiplexer 501 performs the opposite function when data is being sent back to the BTS or DAU. The framer/deframer 503 routes the data to the appropriate Remote Radio Head Unit Band Modules. An additional multiplexer/demultiplexer 506 allows for further expansion of lower speed Remote Radio Head Units. The number of Remote Radio Head units is only limited by the capability of the FPGA. Local communication with the Remote Radio Head Unit's Access Module's FPGA or the individual Remote Radio Head Unit Band Modules is via an Ethernet connection 508. Although the description of this embodiment is mainly directed to an application where a BTS and/or DAU (or multiple BTS and/or multiple DAU) feeds the Remote Radio Head Unit Access Module, an alternative embodiment is described as follows. The alternative embodiment is one where the digital optical signals fed to the Remote Radio Head Unit Access Module may be generated by an RF-to-Digital interface which receives RF signals by means of one or more antennas directed to one or more base stations located at some distance from the Remote Radio Head Unit Access Module. A further alternative embodiment is one where the signals fed to the Remote Radio Head Unit Access Module may be generated in a combination of ways; some may be generated by an RF-to-Digital interface and some may be generated by a BTS and/or DAU. Some neutral host applications gain an advantage with regard to cost-effectiveness from employing this further alternative embodiment. Although the optical signals fed to the Remote Radio Head Unit Access Module described in the preferred and alternative embodiments are digital; the optical signals are not limited to digital, and can be analog or a combination of analog and digital. A further alternative embodiment employs transport on one or multiple optical wavelengths fed to the Remote Radio Head Unit Access Module.

[0023] The Remote Radio Head Unit Band Module is shown in Figure 6. It comprises a Software Defined Digital (SDD) section 610 and an RF section 622. An alternative embodiment employs a Remote Antenna Unit comprising a broadband antenna with RRU Band Module Combiner and multiple plug-in module slots, into which multiple RRU Band Modules intended for operation in different frequency bands are inserted. To provide an overall compact unit with low visual impact, this embodiment employs RRU Band Modules which each have a physically small form factor. One example of a suitably small form factor for the RRU Band Module is the PCMCIA module format. A further alternative embodiment employs RRU Band Modules where each has an integral antenna, and the embodiment does not require a common antenna shared by multiple RRU Band Modules.

[0024] In summary, the Neutral Host Distributed Antenna System (NHDAS) of the present invention enables the use of remote radio heads for multi-operator multi-band configurations , which subsequently saves hardware resources and reduces costs. The NHDAS system is also reconfigurable and remotely field-programmable since the algorithms can be adjusted like software in the digital processor at any time.

[0025] Moreover, the NHDAS system is flexible with regard to being able to support various modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, LTE and wireless LAN systems. This means that the NHDAS system is capable of supporting multi-modulation schemes, multi-bands and multi-operators.

[0026] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

What is Claimed is:

5

ABSTRACT

A remote radio head unit (RRU) system for achieving high data rate communications in a Distributed Antenna System is disclosed. The Distributed Antenna System is configured as a Neutral Host enabling multiple operators to exist on one DAS system. The present disclosure enables a remote radio head unit to be field reconfigurable and support multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

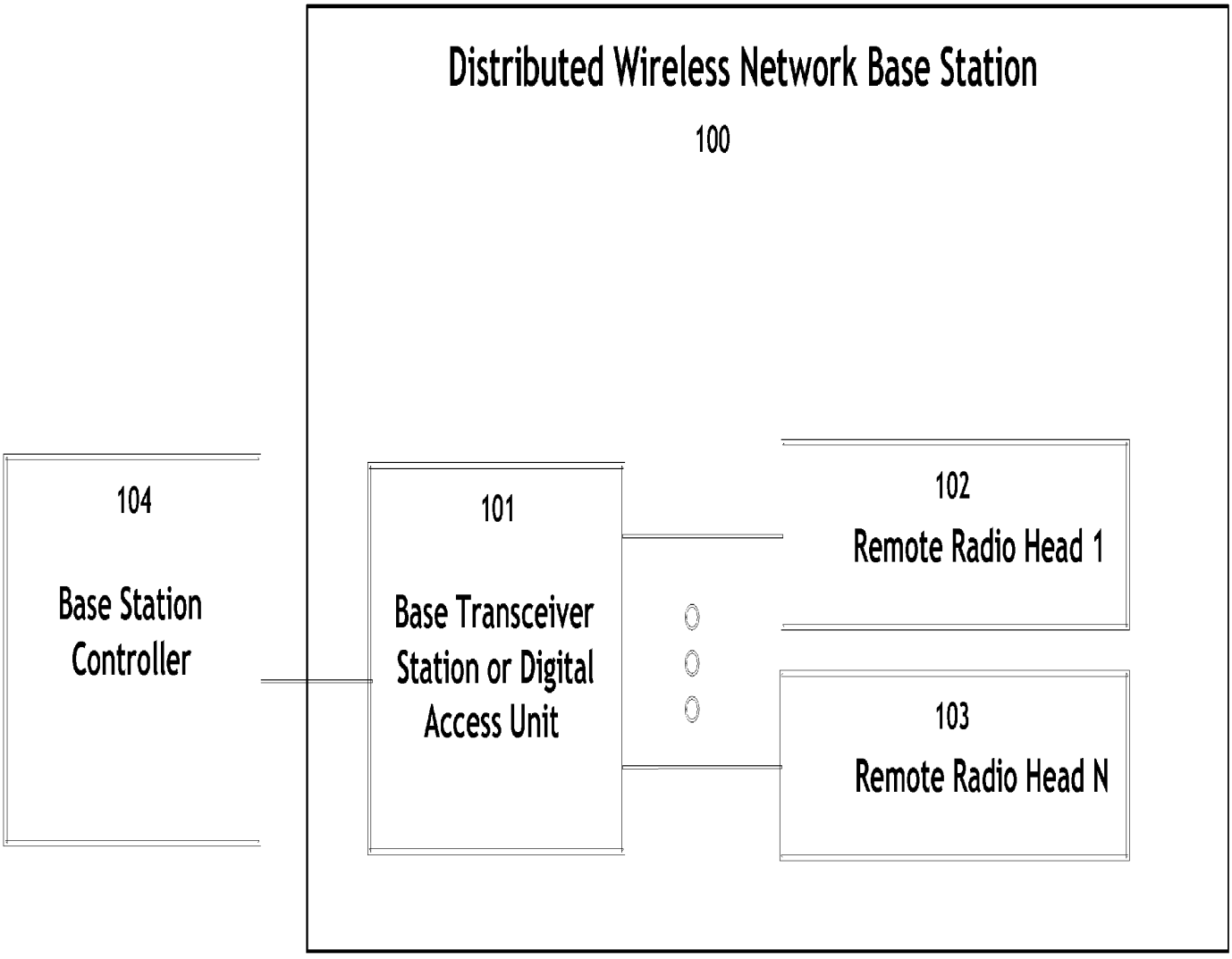
APPENDIX I

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing

PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRH	Remote Radio Head
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Figure 1: PRIOR ART



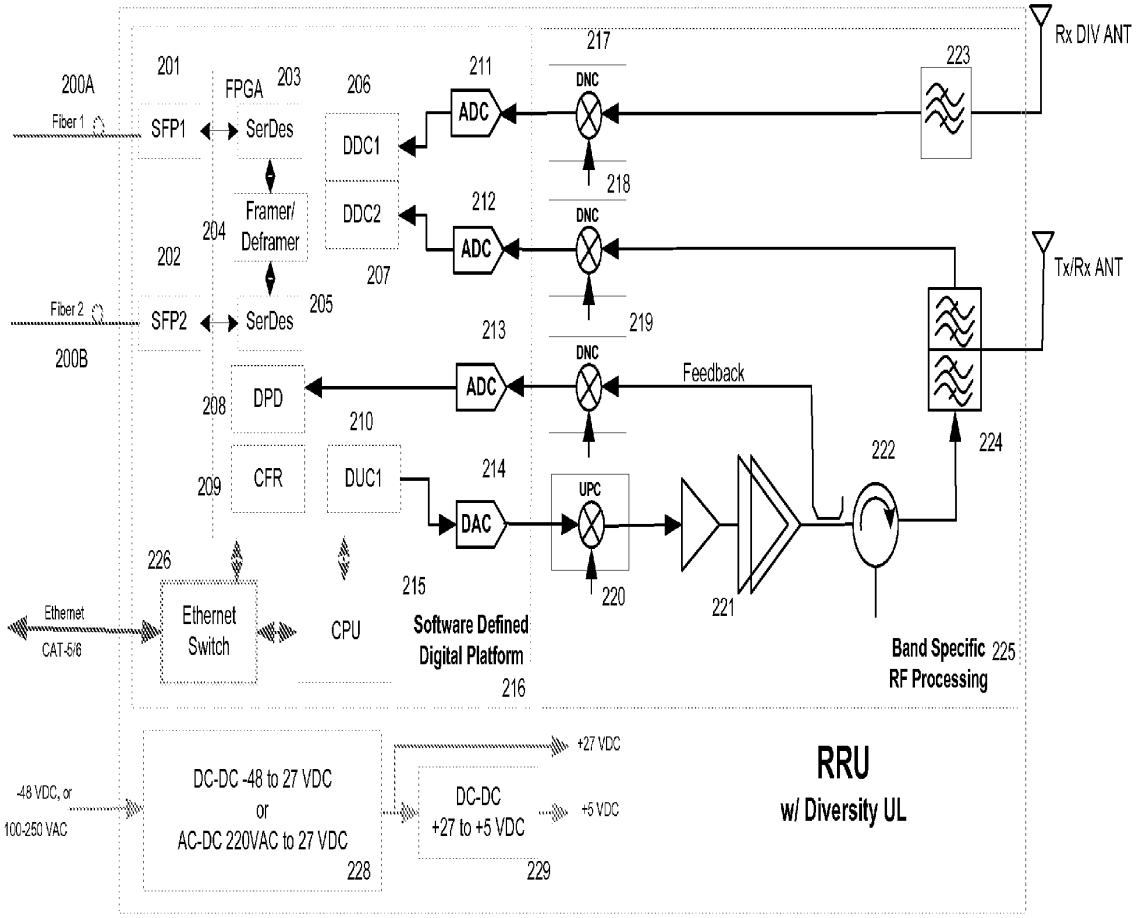


Figure 2. Remote Radio Head Unit

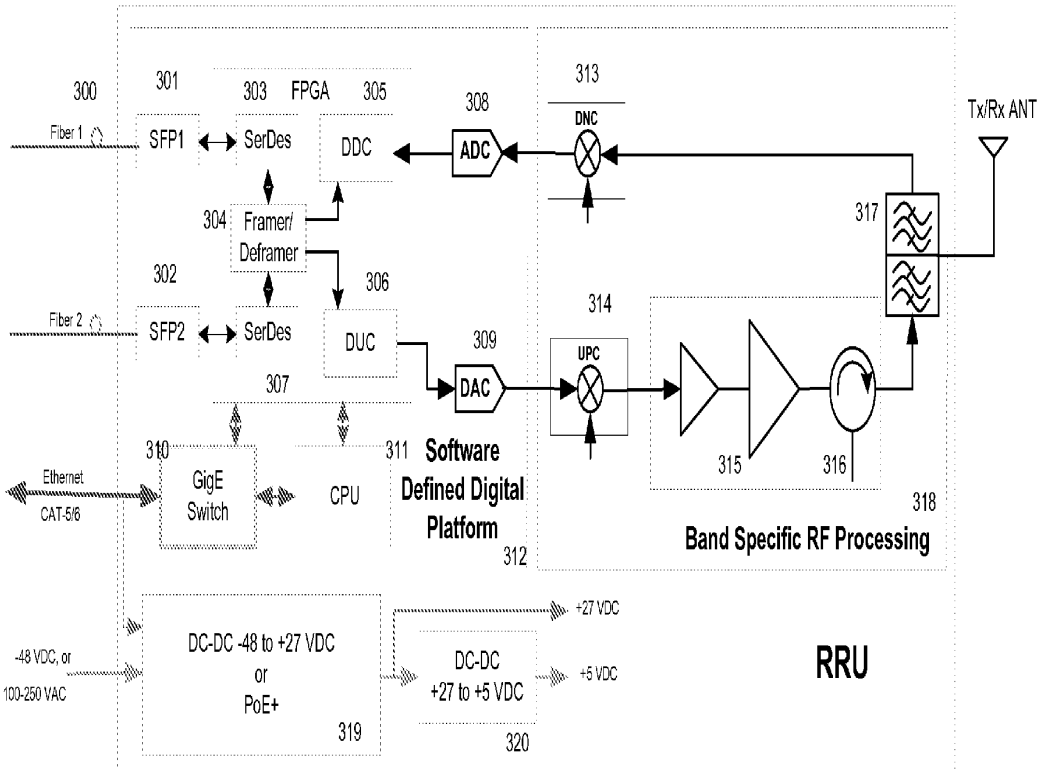


Figure 3. Remote Radio Head Unit

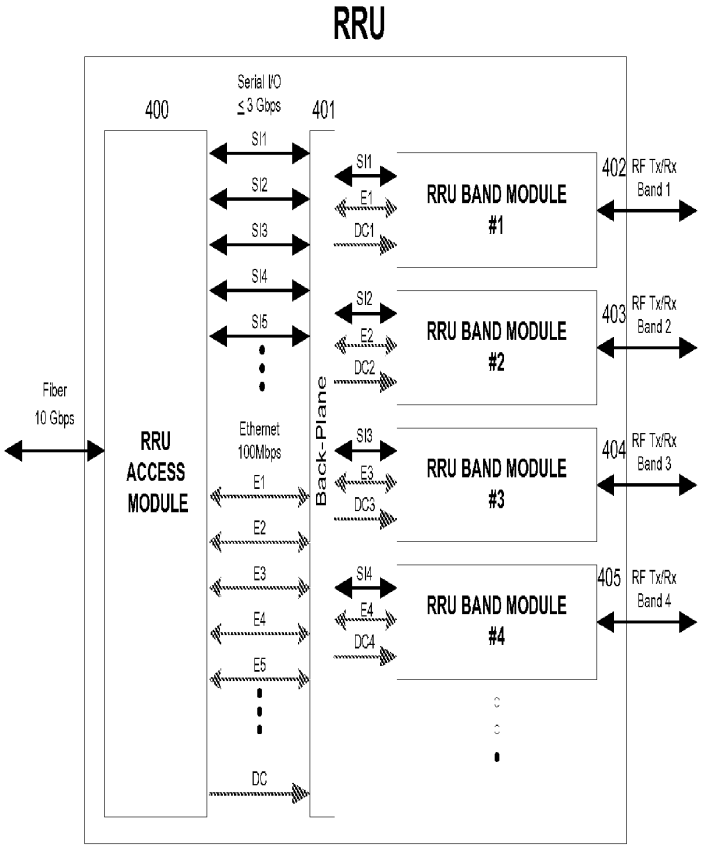


Figure 4. Remote Radio Head Unit High Level System

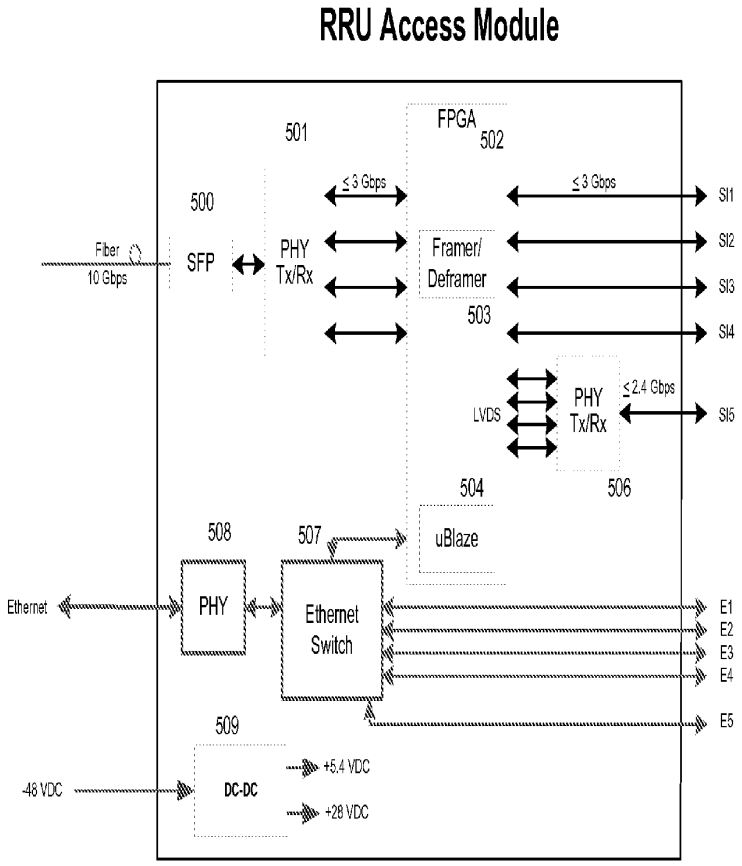


Figure 5. Remote Radio Head Unit Access Module

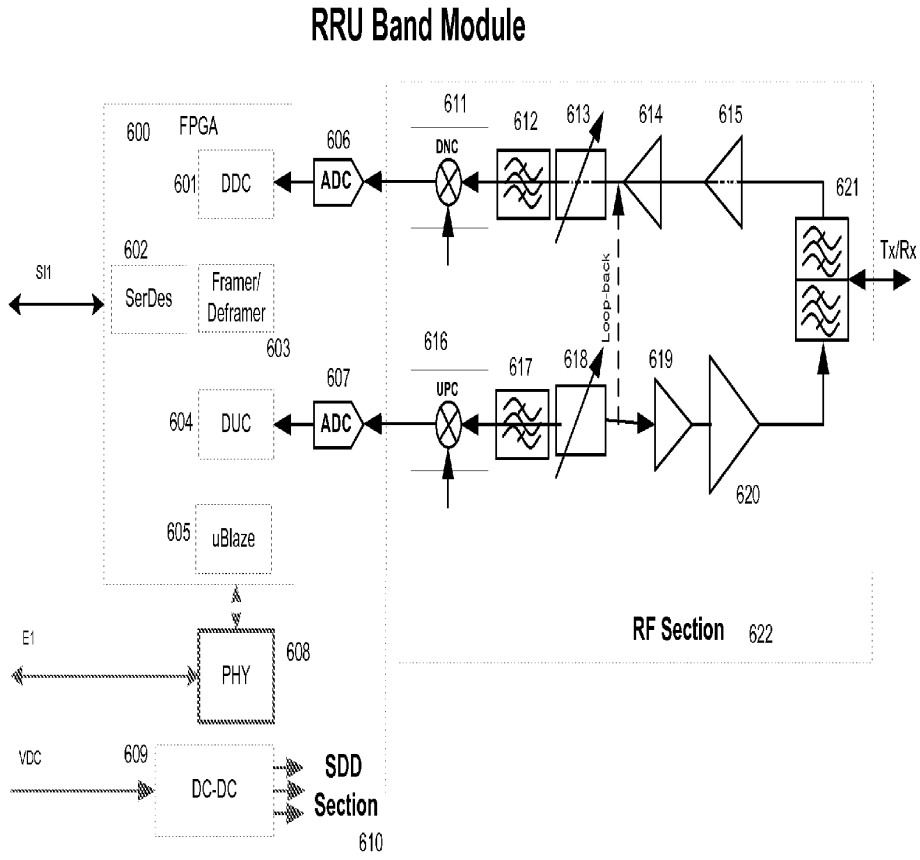


Figure 6. Remote Radio Head Unit Band Module

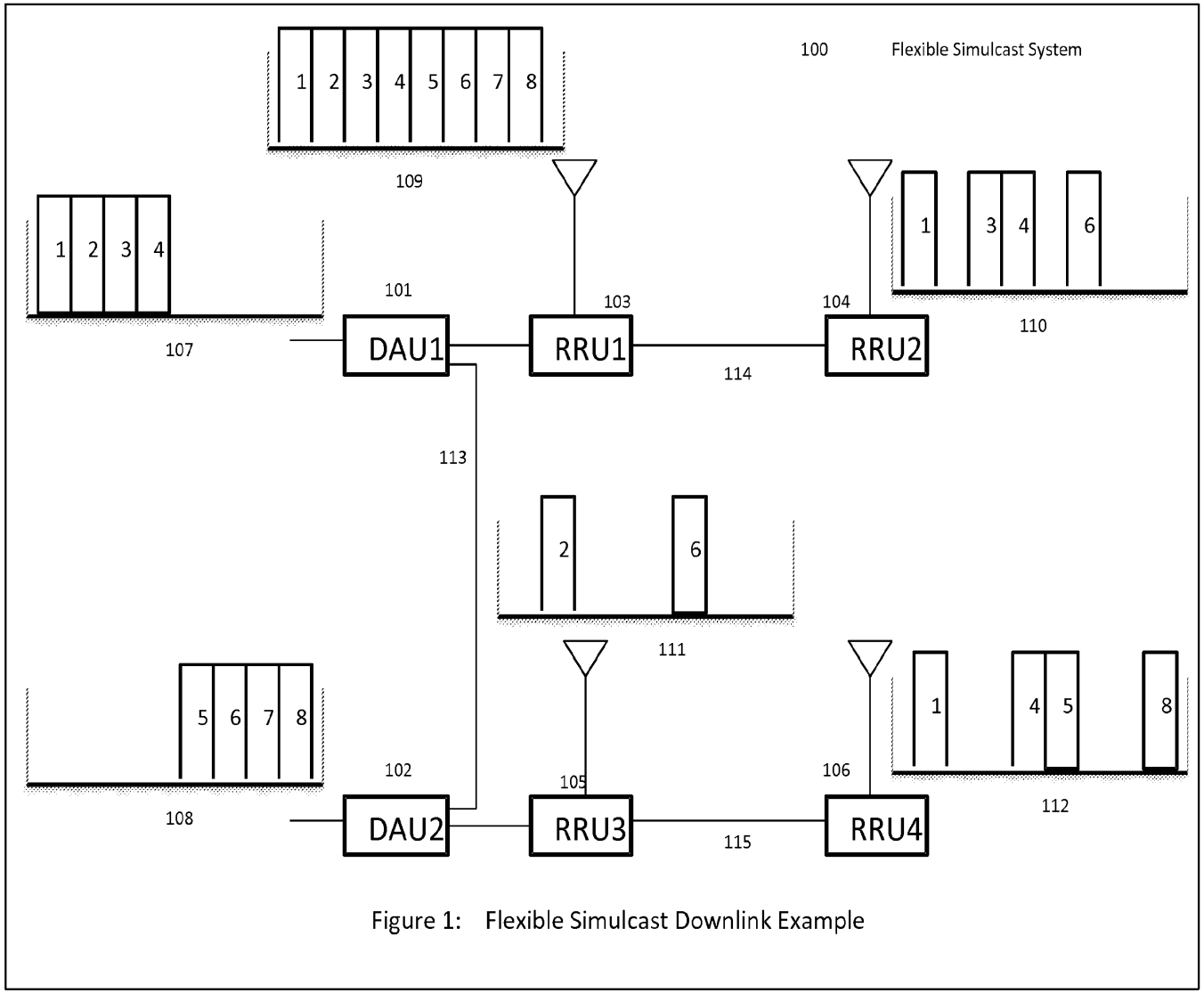


Figure 1: Flexible Simulcast Downlink Example

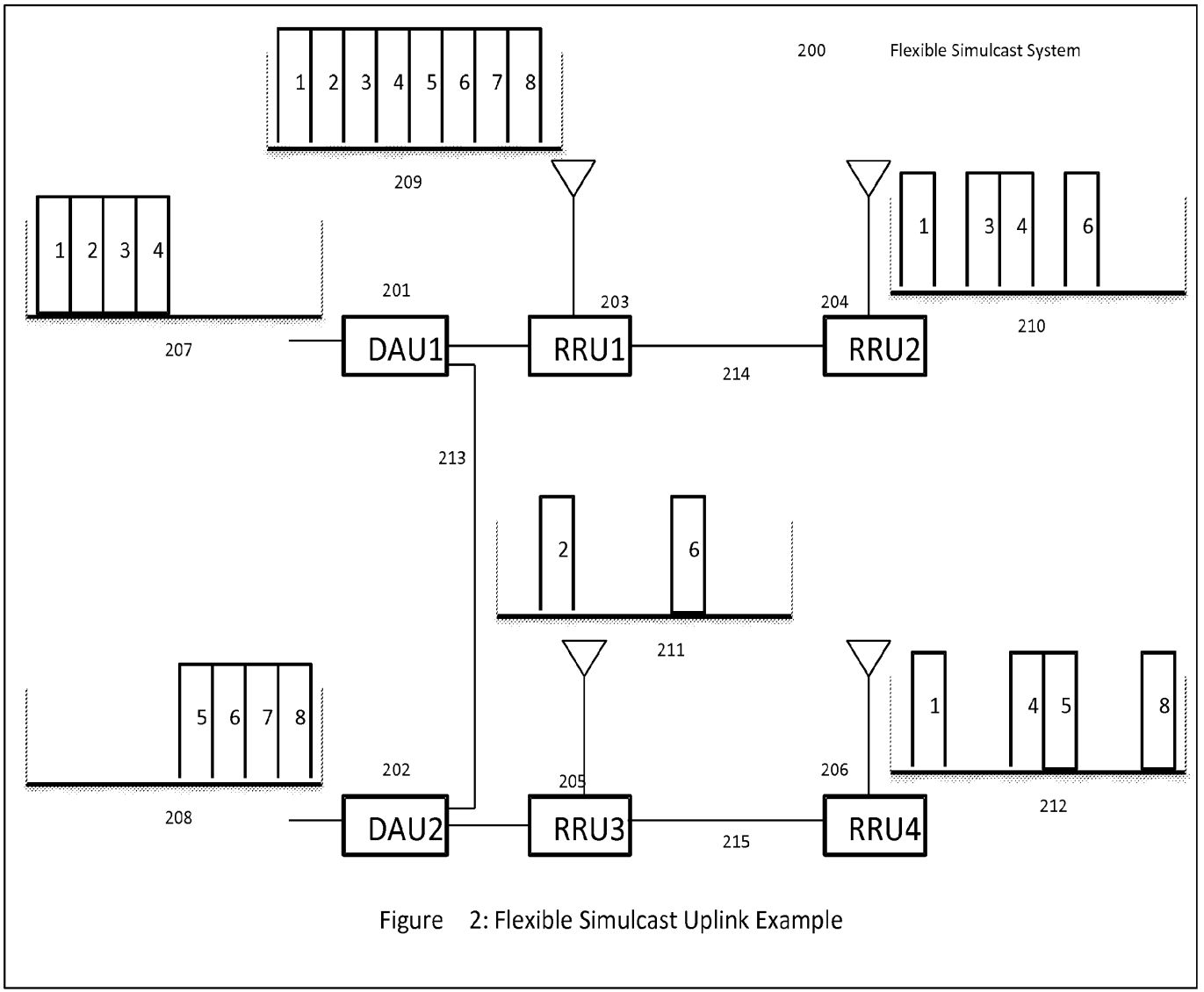


Figure 2: Flexible Simulcast Uplink Example

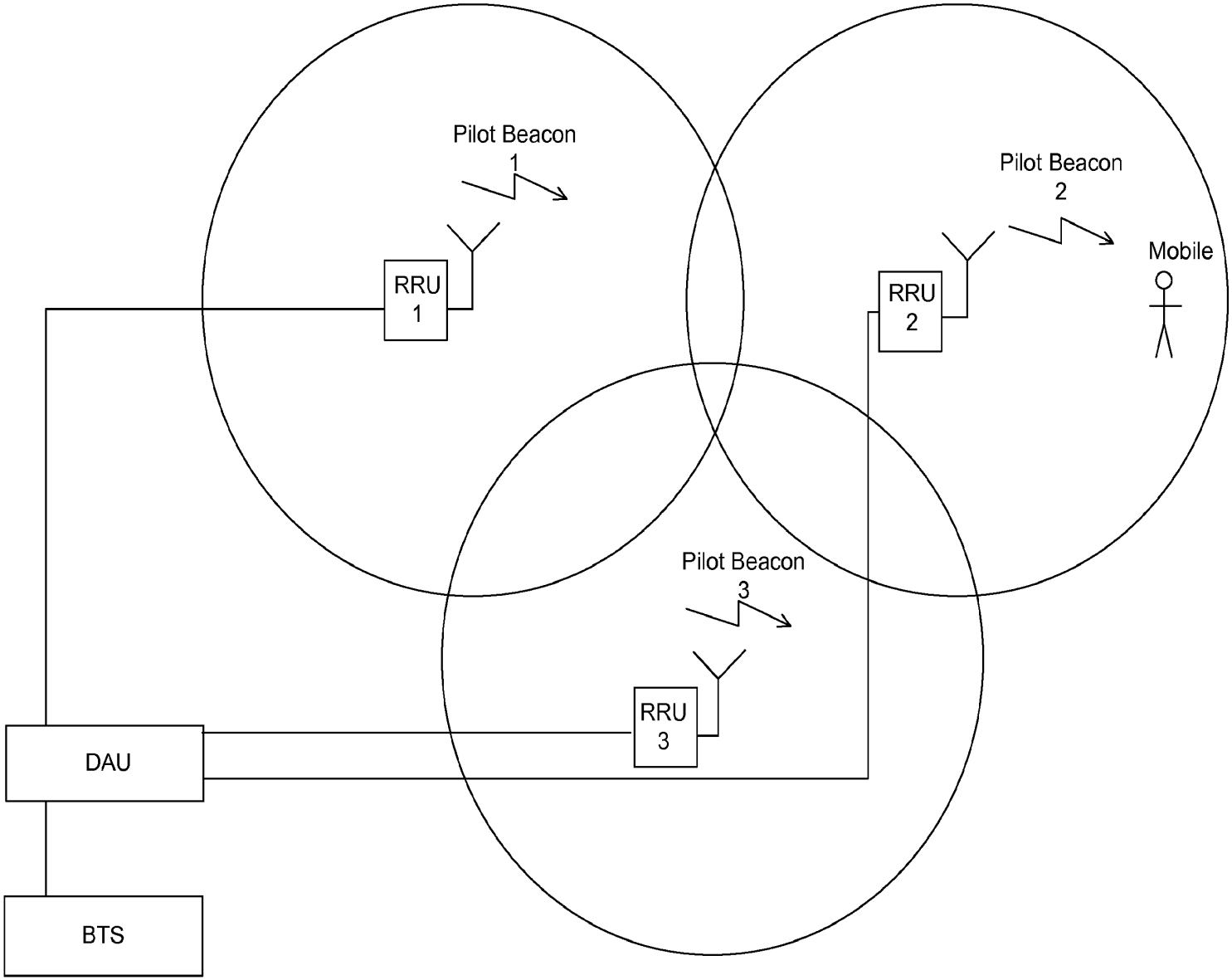


Figure 3 Pilot Beacon Indoor Localization System for CDMA and WCDMA

Figure 4 Indoor Localization System of GSM and LTE

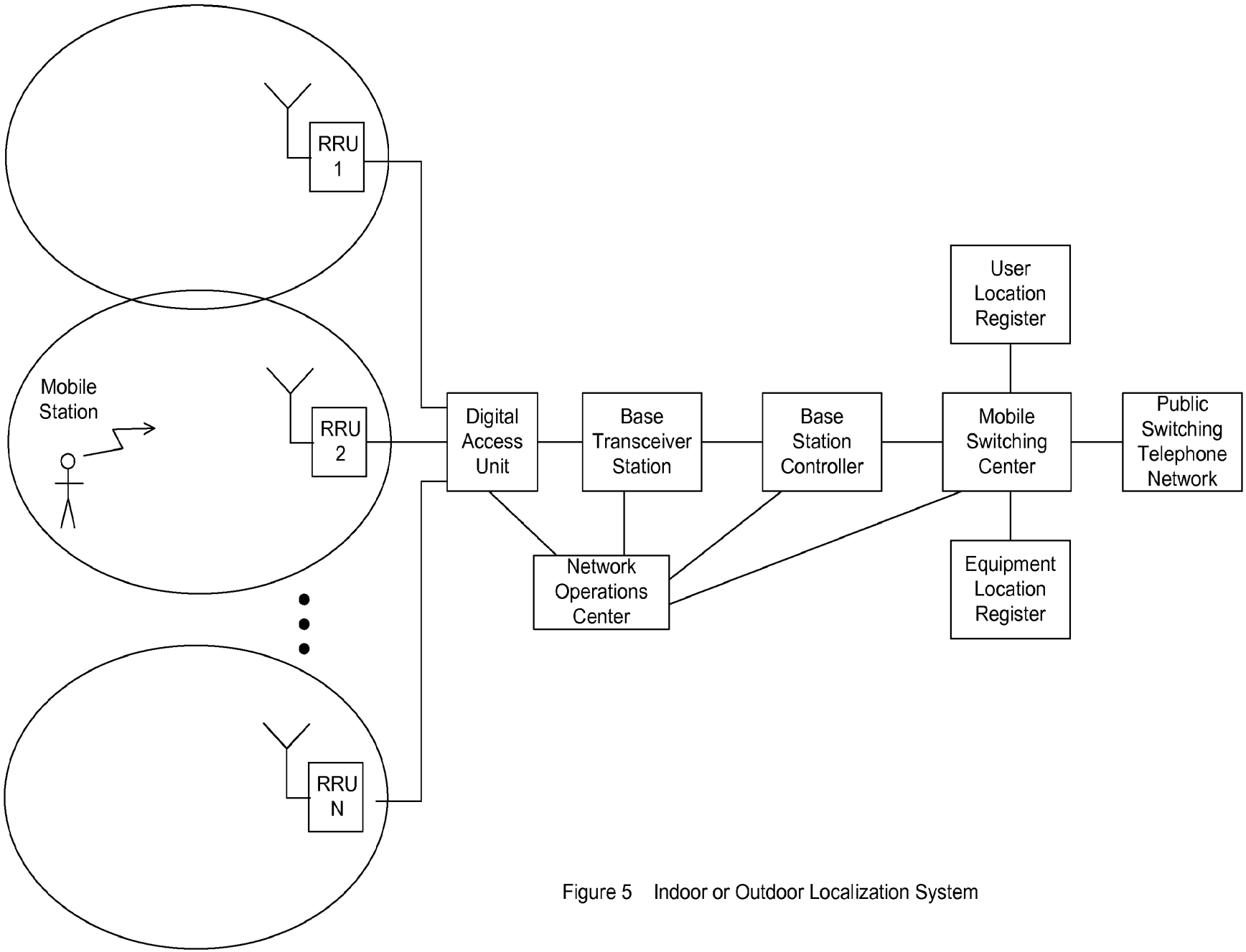


Figure 5 Indoor or Outdoor Localization System

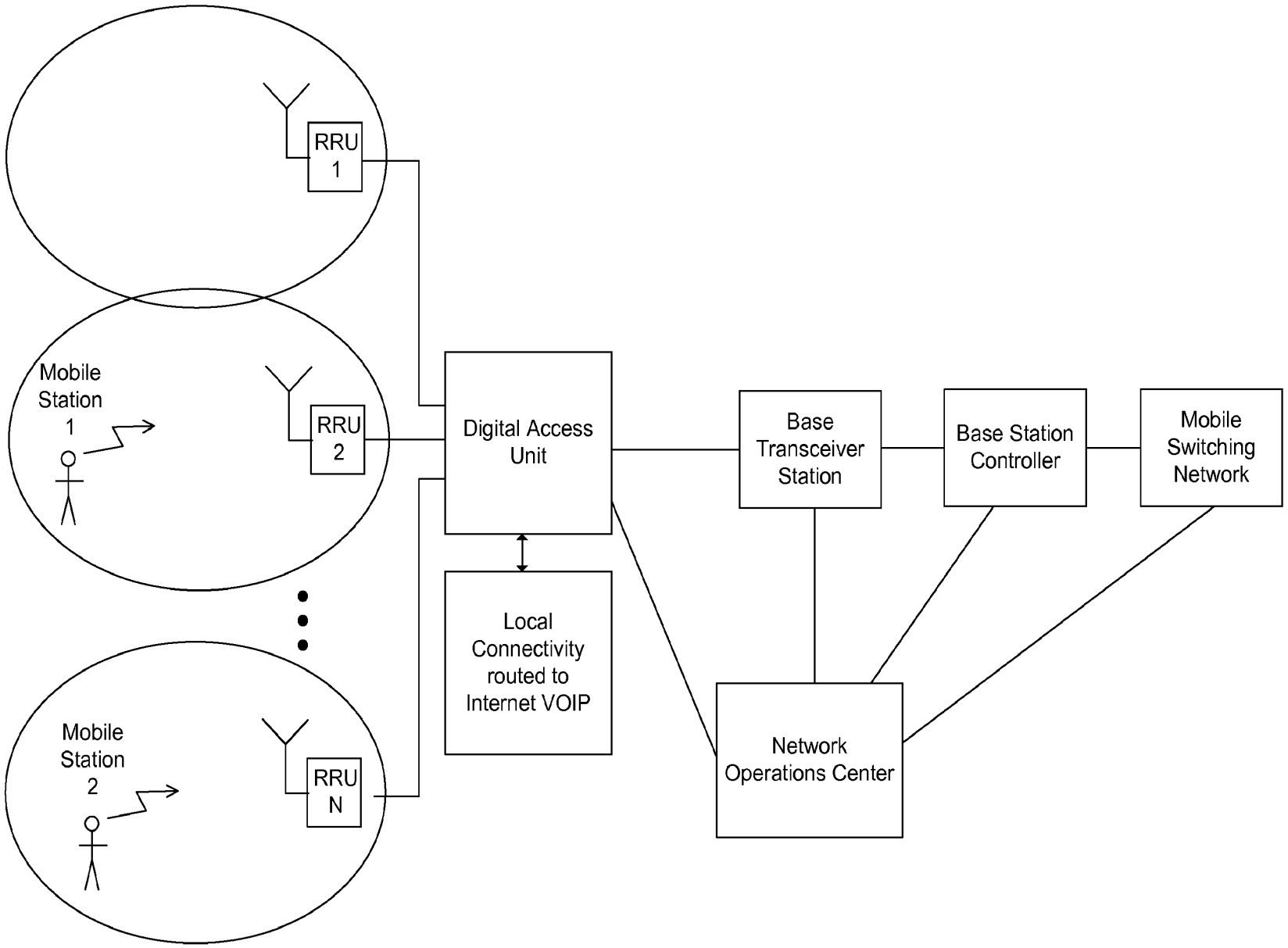


Figure 6 Local Connectivity

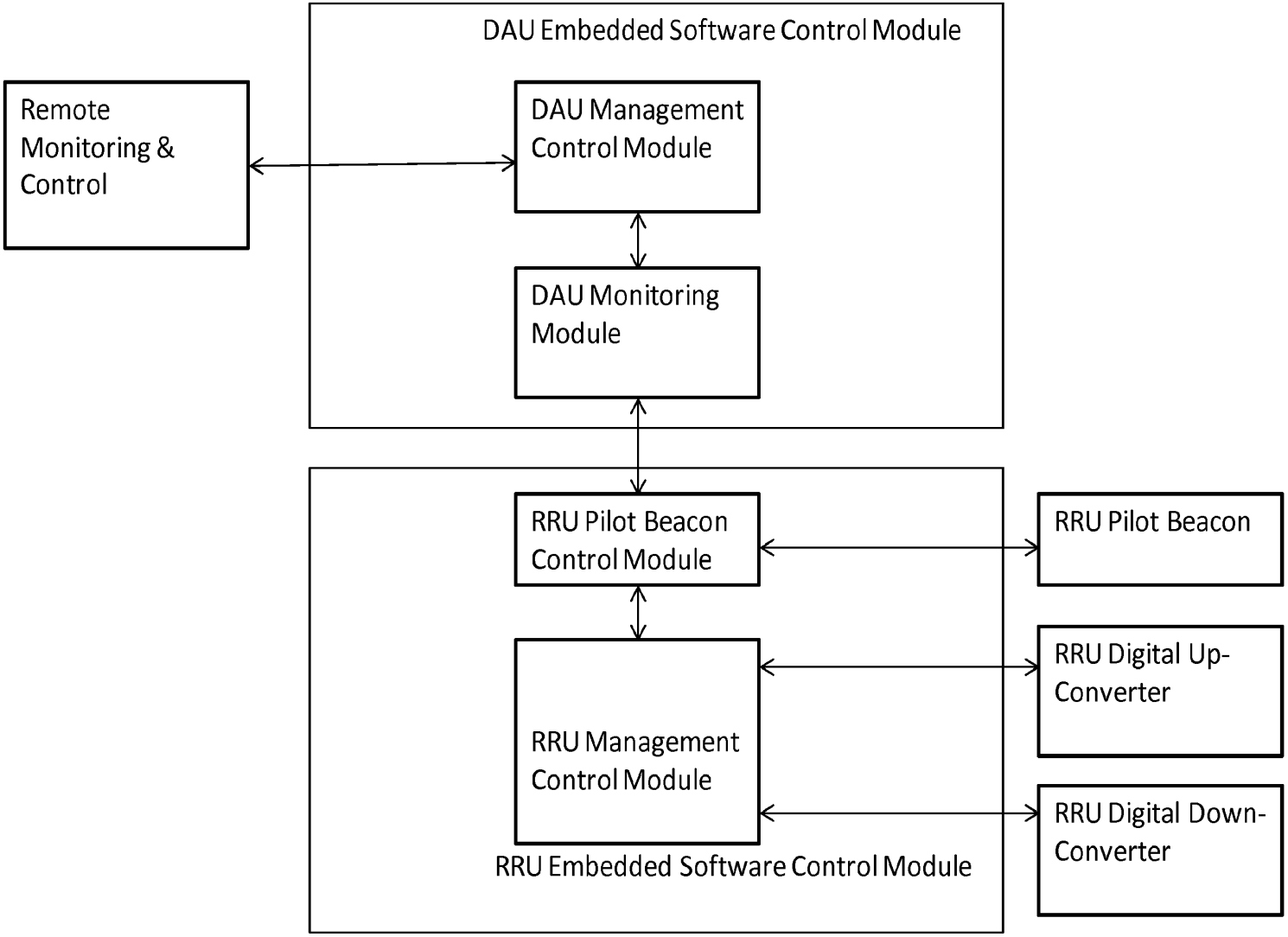


Figure 7: Embedded Software Control Modules

DW-1022P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

NEUTRAL HOST ARCHITECTURE FOR A DISTRIBUTED ANTENNA SYSTEM

INVENTORS

Paul Lemson, Citizen of the United States
Shawn Patrick Stapleton, Citizen of Canada
Sasa Trajkovic, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems employing Distributed Antenna Systems (DAS). More specifically, the present invention relates to a DAS which is part of a distributed wireless network

base station in which all radio-related functions that provide network coverage and/or capacity for a given area are contained in a small single unit that can be deployed in a location remote from the remaining distributed wireless network base station unit or units which are not performing radio-related functions. Multi-mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA, UMTS and WiMAX standards with advanced software configurability are features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multiple operators and multi-frequency bands per operator within a single DAS to reduce the costs associated with radio network equipment and radio network deployment.

BACKGROUND OF THE INVENTION

[002] Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users requires end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G and other advanced network capabilities. Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting these higher bandwidth requirements are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must deal with the limited availability of new spectrum,

leverage existing spectrum, and ensure operation of all desired wireless technology standards. The processes of scarce resource optimization while ensuring a future-proof implementation must both take place at the same time during the transition phase, which usually spans many years and thus can encompass numerous future developments. Distributed open base station architecture concepts have evolved in parallel with the evolution of the various technology standards to provide a flexible, lower-cost, and more scalable modular environment for managing the radio access evolution. Such advanced base station architectures can generally be appreciated from Figure 1 [PRIOR ART], which shows an architecture for a prior art Distributed Wireless Network Base Station. In Figure 1, 100 is a depiction of a Distributed Wireless Network Base Station. The Base Transceiver Station (BTS) or Digital Access Unit (DAU) 101 coordinates the communication between the Remote Radio Head Units 102, 103 and the Base Station Controller (BSC). The BTS communicates with multiple Remote Radio Heads via optical fiber. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI), and the IR Interface standards introduced publicly-defined interfaces separating the Base Transceiver Station (BTS) or Digital Access Unit and the remote radio head unit (RRU) parts of a base station by employing optical fiber transport.

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SUMMARY OF THE INVENTION

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System and Method, US Patent application US 12/108,502 (DW-1011U), filed 4/23/2008, entitled Digital Hybrid Mode Power Amplifier System, US Patent application SN 61/288,838 (DW-1018P), filed 12/21/2009, entitled Multi-band Wideband Power Amplifier Digital Predistortion System, US Patent application SN 61/288,840 (DW-1019P), filed 12/21/2009, entitled Remote Radio Head Unit with Wideband Power Amplifier and Method, US Patent application SN 61/288,844 (DW-1020P), filed 12/21/2009, entitled Modulation Agnostic Digital Hybrid Mode Power Amplifier System, and US Patent application SN 61/288,847 (DW-1021P), filed 12/21/2009, entitled High Efficiency Remotely Reconfigurable Remote Radio Head Unit System and Method for Wireless Communications, all of which are incorporated herein by reference. In addition, the system and method of the present invention supports multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands, and multi-channels. To achieve the above objects, the present invention maximizes the data rate to the Remote Radio Head Unit in a cost effective architecture. Figures 2 and 3 depict a low power RRU and high power RRU. The RRUs depicted in Figures 2 and 3 can be extended to a multi-band and multi-channel configuration. Multi-band implies more than two frequency bands and multi-channel implies more than one output to an antenna system. Various embodiments of the invention are disclosed.

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[0014] Figure 6 is a Remote Radio Head Unit Band Module according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention is a novel Distributed Antenna System that utilizes a high speed Remote Radio Head Unit Access Module interconnected with Remote Radio Head Unit Band Module.

[0016] An embodiment of a Remote Radio Head Unit in accordance with the invention is shown in Figure 2. Fiber 1, indicated at 200A, is a high speed fiber cable that transports data between the BTS and the Remote Radio Head Unit. Fiber 2, indicated at 200B, is used to daisy chain other remote radio head units which are thereby interconnected to the BTS or DAU. The software-defined digital platform 216 performs baseband signal processing, typically in an FPGA or equivalent. Building block 203 is a Serializer/Deserializer. The deserializer portion extracts the serial input bit stream from the optical fiber 201 and converts it into a parallel bit stream. The serializer portion performs the inverse operation for sending data from the Remote Radio Head Unit to the BTS. In an embodiment, the two distinct bit streams communicate with the BTS using

different optical wavelengths over one fiber, although multiple fibers can be used in alternative arrangements. The deframer 204 deciphers the structure of the incoming bit stream and sends the deframed data to the Crest Factor Reduction Algorithm 209. The Crest Factor Reduction block 209 reduces the Peak-to-Average Ratio of the incoming signal so as to improve the Power amplifier DC-to-RF conversion efficiency. The waveform is then presented to the Digital Predistorter block 208. The digital predistorter compensates for the nonlinearities of the Power Amplifier 221 in an adaptive feedback loop. Digital Upconverter 210 filters and digitally translates the deframed signal to an IF frequency. The Framer 204 takes the data from the two digital downconverters 206, 207 and packs it into a Frame for transmission to the BTS over the optical fiber 201. Elements 211 and 212 are Analog to Digital converters that are used to translate the two analog receive signals into digital signals. The receiver comprises a diversity branch which contains a downconverter 217 and a Band Pass Filter 223. The main branch has a receiver path comprised of a duplexer 224 and a downconverter 218.

[0017] The power amplifier has an output coupler for extracting a replica of the output signal in the feedback path. The feedback signal is frequency-translated by downconverter 219 to either an IF frequency or baseband and presented to an Analog to Digital converter 213. This feedback signal is used in an adaptive loop for performing Digital Predistortion to compensate for any nonlinearities created by the power amplifier.

[0018] The Ethernet cable is used to locally communicate with the Remote Radio Head Unit. Switch 226 is used to allow easy access to either the FPGA or the CPU. DC power converters 228 and 229 are used to obtain the desired DC voltages for the Remote Radio Head Unit. Either an external voltage can be

connected directly into the RRU or the DC power may be supplied through the Ethernet cable.

[0019] Although the description of the instant embodiment is directed to an application where a second optical fiber connection provides a capability for daisy chaining to other Remote Radio Head Units, an alternative embodiment provides multiple optical fiber connections to support a modified "hybrid star" configuration for appropriate applications which dictate this particular optical transport network configuration.

[0020] Figure 3 depicts a remote radio head unit. In at least some designs, this architecture offers benefits when the RF output power is relatively low. In the embodiment shown in Figure 3, digital predistrortion and crest factor reduction are not employed as was the case in Figure 2. Even though this topology shows a non-diversity configuration, a diversity receive branch can be added along with an additional transmitter path for development of a Multiple Input Multiple Output (MIMO) Remote Radio Head Unit.

[0021] The Remote Radio Head Unit high level system is shown in Figure 4. It comprises a Remote Radio Head Unit Access Module 400 which communicates directly with the BTS or DAU. The function of the Remote Radio Head Unit Access Module 400 is to route the high speed data (at any desired speed, e.g., such as 10 Gbps as illustrated in Fig. 4) (the "Data Speed") to the multiple Remote Radio Head Unit Band Modules and allows for local communications with them via Ethernet. A backplane 401 is used to interconnect the Remote Radio Head Unit Access Module 400 with the various Remote Radio Head Unit Band Modules 402,403,404,405 at any speed lower than the Data Speed (e.g., less than or equal to 3Gbps as illustrated in Fig. 4). The output ports of the Remote Radio Head Unit Band Modules are combined

and sent to an antenna for transmission. An alternative embodiment is described as follows. Although the description of instant embodiment is directed to applications for up to four Remote Radio Head Unit Band Modules, an alternative embodiment involves feeding a much larger quantity of Remote Radio Head Unit Band Modules with signals of various bandwidths at various frequency bands covering multiple octaves of frequency range, to support a wide range of applications including location-based services, mobile internet, public safety communications, private enterprise telecommunications and broadband, and other wireless applications. The system can in theory support an infinite quantity of RRUs. Also, the Remote Radio Head Unit Band Modules may be set up remotely to have RF power values selected based on the specific desired applications as well as location-specific radio signal propagation factors. A further alternative embodiment leverages the flexibility of the architecture shown in Figure 4 to provide a capability known as Flexible Simulcast. With Flexible Simulcast, the amount of radio resources (such as RF carriers, CDMA codes or TDMA time slots) assigned to a particular RRU or group of RRUs by each RRU Access Module can be set via software control to meet desired capacity and throughput objectives or wireless subscriber needs.

[0022] The detailed topology of the Remote Radio Head Unit Access Module is shown in Figure 5. It comprises a Small form Factor Pluggable optic transceiver (SFP) 500 which operates on two distinct wavelengths, one for communicating from the BTS to the Remote Radio Head Unit Access Module and the other for communicating in the opposite direction. The SFP contains a Laser Diode for converting the electronic signal to a digital optical signal and an Optical detector for converting the digital optical signal into an electronic signal.

A multiplexer/demultiplexer 501 converts the high speed data to multiple lower speed data paths for delivery to a FPGA 502. The multiplexer/demultiplexer 501 performs the opposite function when data is being sent back to the BTS or DAU. The framer/deframer 503 routes the data to the appropriate Remote Radio Head Unit Band Modules. An additional multiplexer/demultiplexer 506 allows for further expansion of lower speed Remote Radio Head Units. The number of Remote Radio Head units is only limited by the capability of the FPGA. Local communication with the Remote Radio Head Unit's Access Module's FPGA or the individual Remote Radio Head Unit Band Modules is via an Ethernet connection 508. Although the description of this embodiment is mainly directed to an application where a BTS and/or DAU (or multiple BTS and/or multiple DAU) feeds the Remote Radio Head Unit Access Module, an alternative embodiment is described as follows. The alternative embodiment is one where the digital optical signals fed to the Remote Radio Head Unit Access Module may be generated by an RF-to-Digital interface which receives RF signals by means of one or more antennas directed to one or more base stations located at some distance from the Remote Radio Head Unit Access Module. A further alternative embodiment is one where the signals fed to the Remote Radio Head Unit Access Module may be generated in a combination of ways; some may be generated by an RF-to-Digital interface and some may be generated by a BTS and/or DAU. Some neutral host applications gain an advantage with regard to cost-effectiveness from employing this further alternative embodiment. Although the optical signals fed to the Remote Radio Head Unit Access Module described in the preferred and alternative embodiments are digital; the optical signals are not limited to digital, and can be analog or a combination of analog and digital. A further alternative embodiment employs transport on one or multiple optical wavelengths fed to the Remote Radio Head Unit Access Module.

[0023] The Remote Radio Head Unit Band Module is shown in Figure 6. It comprises a Software Defined Digital (SDD) section 610 and an RF section 622. An alternative embodiment employs a Remote Antenna Unit comprising a broadband antenna with RRU Band Module Combiner and multiple plug-in module slots, into which multiple RRU Band Modules intended for operation in different frequency bands are inserted. To provide an overall compact unit with low visual impact, this embodiment employs RRU Band Modules which each have a physically small form factor. One example of a suitably small form factor for the RRU Band Module is the PCMCIA module format. A further alternative embodiment employs RRU Band Modules where each has an integral antenna, and the embodiment does not require a common antenna shared by multiple RRU Band Modules.

[0024] In summary, the Neutral Host Distributed Antenna System (NHDAS) of the present invention enables the use of remote radio heads for multi-operator multi-band configurations , which subsequently saves hardware resources and reduces costs. The NHDAS system is also reconfigurable and remotely field-programmable since the algorithms can be adjusted like software in the digital processor at any time.

[0025] Moreover, the NHDAS system is flexible with regard to being able to support various modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, LTE and wireless LAN systems. This means that the NHDAS system is capable of supporting multi-modulation schemes, multi-bands and multi-operators.

[0026] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

What is Claimed is:

5

ABSTRACT

A remote radio head unit (RRU) system for achieving high data rate communications in a Distributed Antenna System is disclosed. The Distributed Antenna System is configured as a Neutral Host enabling multiple operators to exist on one DAS system. The present disclosure enables a remote radio head unit to be field reconfigurable and support multi-modulation schemes (modulation-independent), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

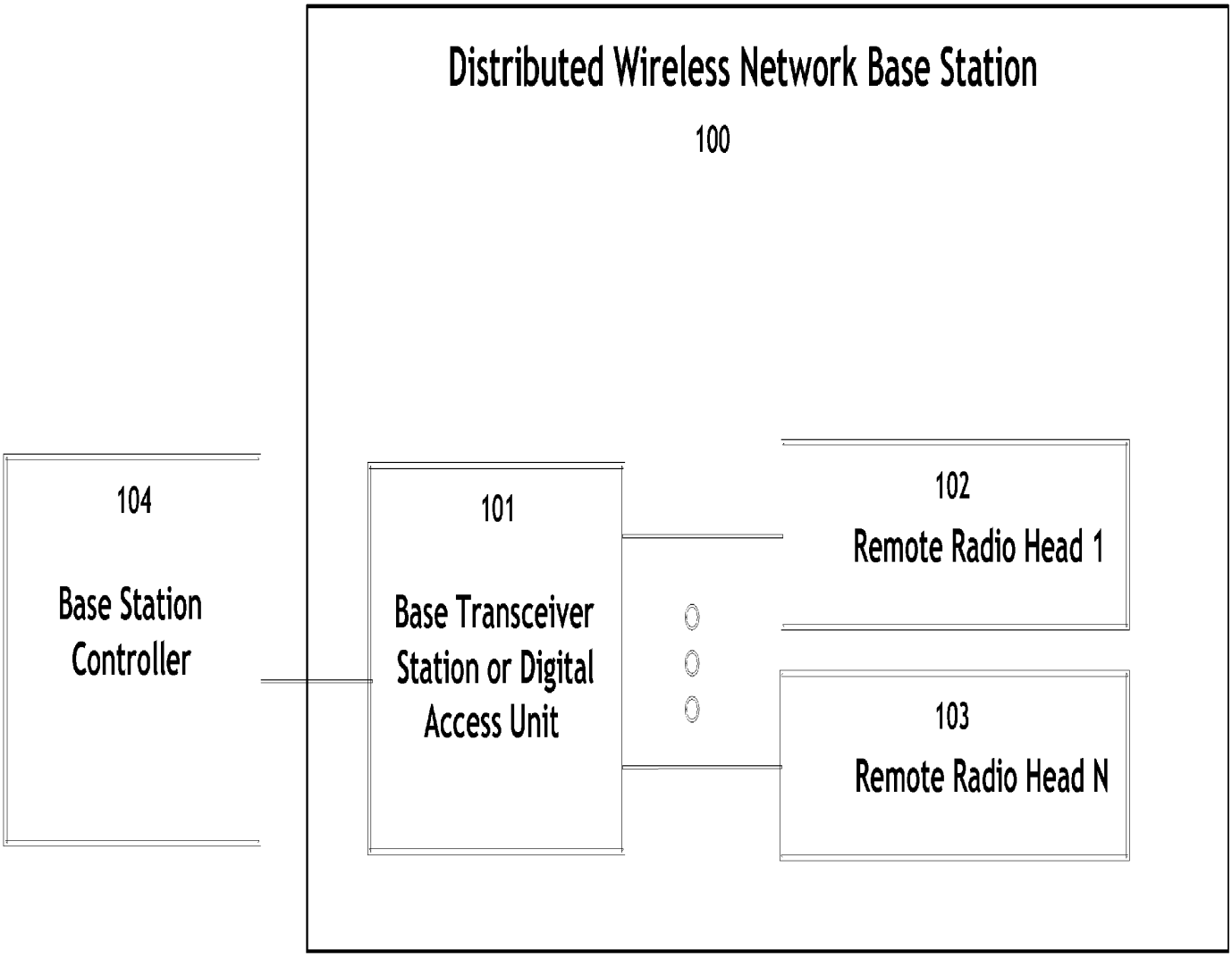
APPENDIX I

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing

PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRH	Remote Radio Head
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Figure 1: PRIOR ART



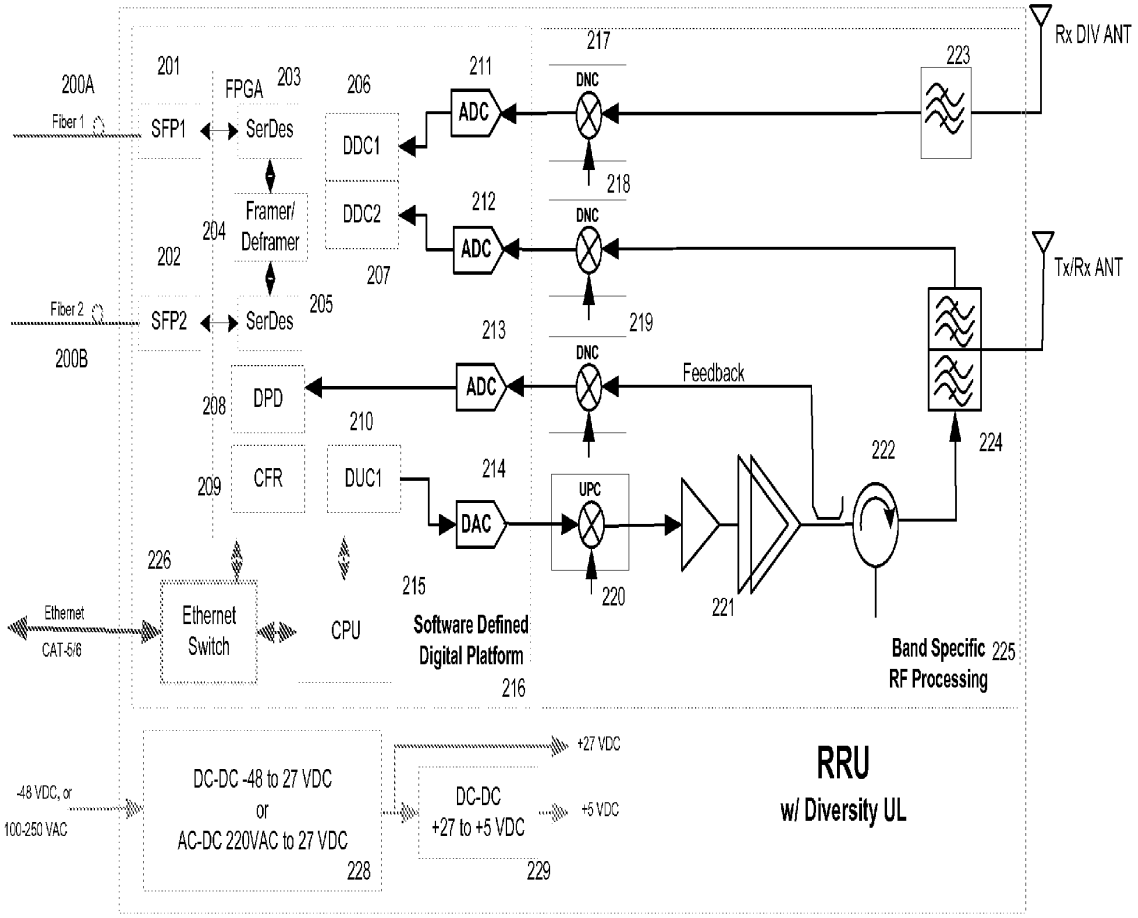


Figure 2. Remote Radio Head Unit

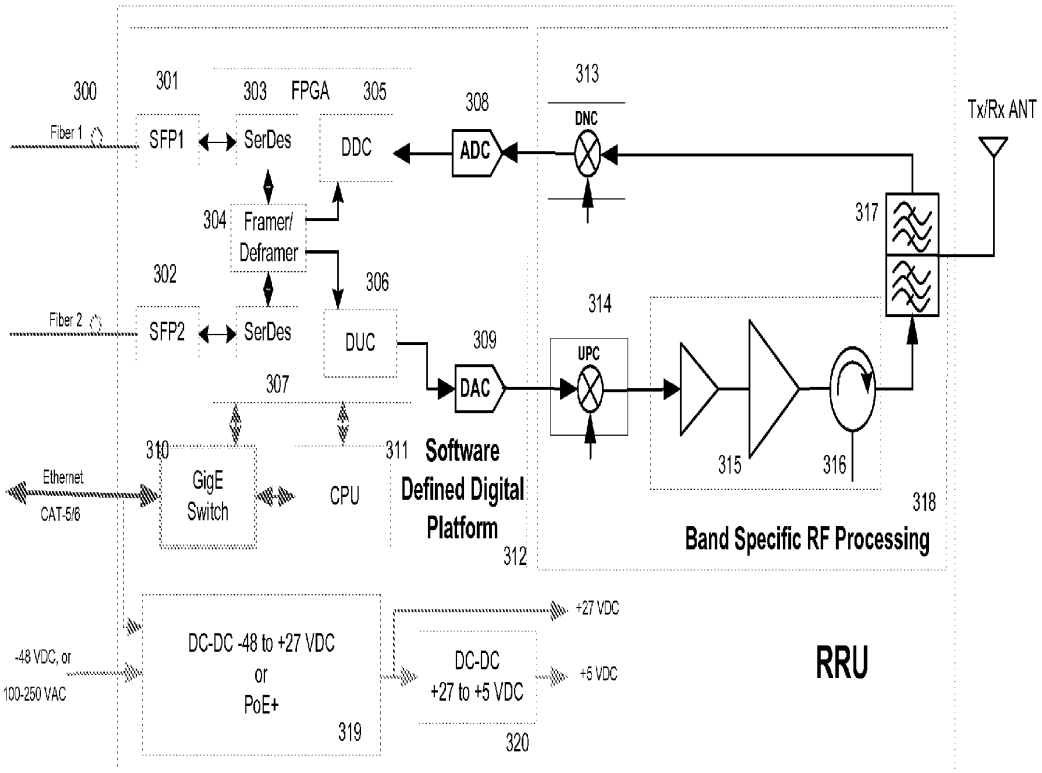


Figure 3. Remote Radio Head Unit

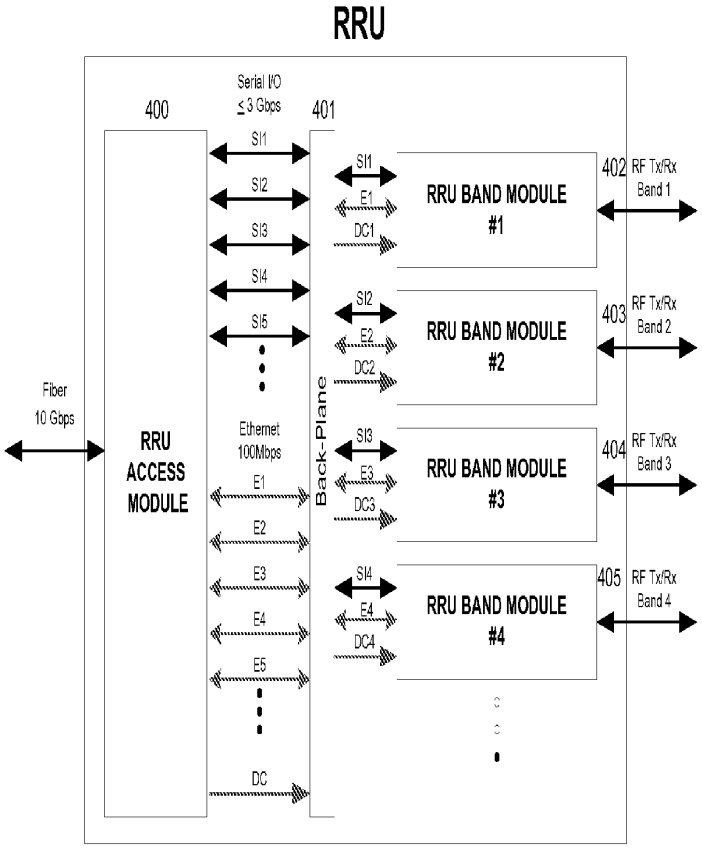


Figure 4. Remote Radio Head Unit High Level System

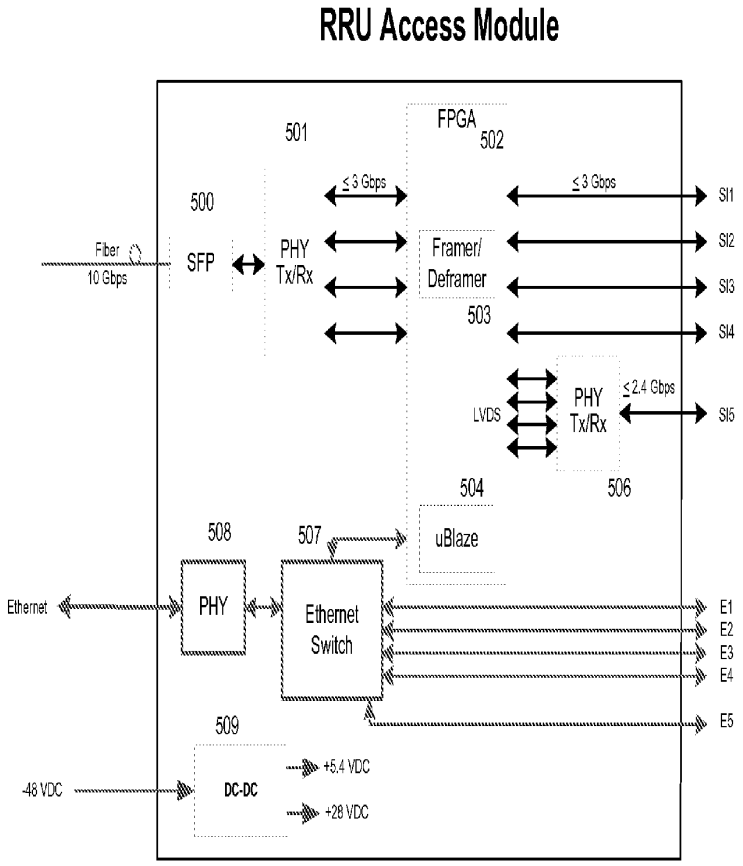


Figure 5. Remote Radio Head Unit Access Module

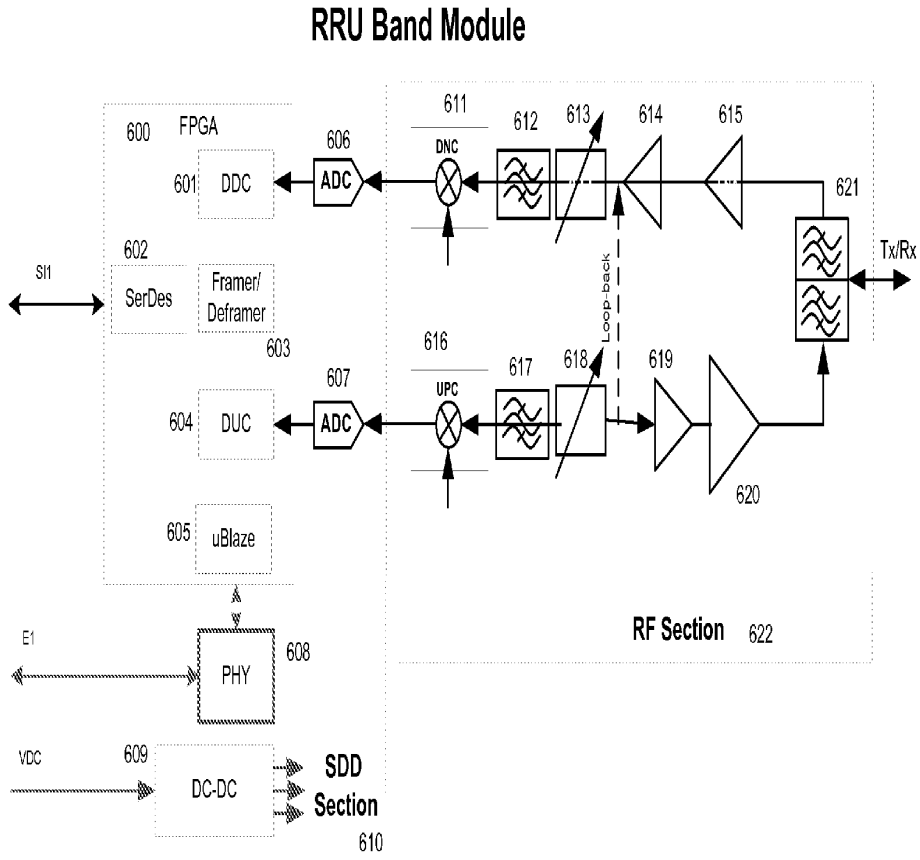


Figure 6. Remote Radio Head Unit Band Module

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS

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Ying Xiao, Citizen of China

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit. Multi-mode radios capable of operating according to GSM, HSPA, LTE, and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks. The present invention can also serve multi-frequency bands within a single RRU to economize the cost of radio network deployment.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G. Wireless and mobile technology standards are

evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years. Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution, Figure 6. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept constitutes a fundamental part of a state-of-the-art base station architecture. However, RRUs to-date are power inefficient, costly and inflexible. Their poor DC to RF power conversion insures that they will have a large mechanical housing. The RRU demands from the service providers are also for greater flexibility in the RRU platform. As standards evolve, there is a need for a software upgradable RRU. Today RRUs lack the flexibility and performance that is required by service providers. The RRU performance limitations are driven in part by the poor power efficiency of the RF amplifiers. Thus there has been a need for an efficient, flexible RRU architecture that is field reconfigurable.

SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems in the prior art, and it is an object of the present invention to provide a high performance and cost effective method of multi-frequency bands RRU systems enabled by high linearity and high efficiency power amplifiers for wideband communication system applications. The present disclosure enables a RRU to be field reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels.

[002] To achieve the above objects, according to the present invention, the technique is generally based on the method of adaptive digital predistortion to linearize RF power amplifiers. Various embodiments of the invention are disclosed, including single band, dual band, and multi-band RRU's. Another embodiment is a multi-band multi-channel RRU. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[003] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations,

distributed antenna systems, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications. The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram showing the basic form of a Remote Radio head unit system.

[007] Figure 2 is a block diagram showing a multi-channel Remote Radio Head Unit according to one embodiment of the present invention.

[007] Figure 3 is a block diagram showing polynomial based predistortion in a Remote Radio head system of the present invention.

[008] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a remote radio head unit system of the present invention.

[009] Figure 5 illustrates an analog modulator compensation block.

[0010] Figure 6 depicts schematically a variety of potential installation schemes for an RRU-based system architecture.

[0011] Figure 7 depicts a three-sector arrangement of an RRU system architecture comprising optical links to a base station server.

[0012] Figure 8 shows in block diagram form various DSP-based functions including crest factor reduction and digital predistortion.

[0013] Figure **9** is a Digital Hybrid Module with either an RF input signal or a baseband modulated signal or an optical interface according to another embodiment of the present invention.

[0014] Figure **10** is a Dual Channel Remote Radio head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present invention.

[0015] Figure **11** is an alternative Dual Channel Remote Radio Head block diagram showing a digital hybrid module with an optical interface according to another embodiment of the present

[0016] Figure **12** is an 8 channel Dual Band Remote Radio Head block diagram showing a digital hybrid module with an optical interface, and further comprises a calibration algorithm for insuring that each power amplifier output is time-aligned, phase-aligned and amplitude-aligned with respect to each other.

GLOSSARY

Acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector

AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter

MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
SERDES	Serializer/Deserializer
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network.

DETAILED DESCRIPTION OF THE INVENTION

[001] The present invention is a novel RRU **s**ystem that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[002] Figure 1 is a high level block diagram showing the basic system architecture of what is sometimes referred to as a Remote Radio Head Unit, or RRU, which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention operates as a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a Remote Radio head Unit (RRU) hereinafter.

[003] Figure 2 illustrates in schematic block diagram form an embodiment of an eight channel (or n channel) RRU in which an input signal 200 is provided. Depending on the implementation, the input signal can take the form of an RF modulated signal, a baseband signal, or an optical signal. The input signal 200 is fed to a plurality of channels, where each channel includes a digital predistortion (DPD) controller, indicated at 201, 211 and 271, respectively. The DPD can be implemented in an FPGA in at least some embodiments. For each channel, the DPD outputs are fed to

associated PA's 202, 212 and 272, respectively, and the PA outputs 203, 213 and 273 are fed back to that channel's DPD's.

[004] Figure 3 illustrates a polynomial-based digital predistorter function in the RRU system of the present invention. The PD in the present invention generally utilizes an adaptive LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3, and in embodiments disclosed from Figures 9-12 discussed hereinafter, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the RRU system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistorter algorithm based on the error between the reference input signal and the amplified power output signal.

[005] Figure 4 shows in block diagram form additional details of an embodiment including a DPD in accordance with the present invention and is discussed in greater detail hereinafter. In general, the input 400 is provided to the DPD 401. The output of the DPD is fed to a DAC 402 and thence to the PA 403. A feedback signal from the output of the PA is received by ADC 406, and the digital form is supplied to alignment logic 405, after which the aligned signal is provided to DPD estimator logic 404, which also receives an

input from the output of the DPD 401. The output of the DPD estimator is then fed back to the DPD 401.

[006] Figure 5 illustrates an analog modulator compensation block. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11 , g12 , g21 , g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to an AQM's in-phase and quadrature ports, discussed hereinafter in connection with Figure 9.

[007] Figure 6 illustrates a plurality of possible implementations of an RRU-based system architecture, in with a base station server 600 is connected to, for example, a tower-mounted RRU 605, a rooftop-mounted RRU 610, and/or a wall-mounted RRU 615.

[008] Figure 7 illustrates an embodiment of a three-sector implementation of an RRU-based system architecture, in which a base station server 700 is optically linked to a plurality of RRU's 710 to provide adequate coverage for a site.

[009] Figure 8 illustrates in simplified form an embodiment of the DSP functionality of some implementations of the present invention. An input signal is fed to an interface 800, which can take several forms including OBSAI, CPRI or IR. The incoming signal is fed to a digital up-converter (DUC) 805 and then to CFR/DPD logic 810, such as an FPGA. The output of

the CFR/DPD logic 810 is then supplied to a DAC 815. The DAC provides an output signal to the analog RF portion 820 of the system, which in turn provides a feedback signal to a ADC 825, and back through the DSP block in the form of inputs to the CFR/DPD and a DDC 830. The DDC outputs a signal to the interface 800, which in turn can provide an output.

[0010] Figure 9 is a block diagram showing a more sophisticated embodiment of a RRU system, where like elements are indicated with like numerals. The embodiment of Figure 9 applies crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in US patent application SN 61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0011] Figure 9 is a block diagram showing a RRU system according to one embodiment of the present invention (the "FIG. 9. System"). RRU systems consist of three primary blocks: power amplifiers, baseband processing and an optical interface. The optical interface contains an optical to electrical interface for the transmit/receive mode. The optical interface 901,

shown in Figure 9, is coupled to a FPGA. The FPGA 902 performs the functions of SERDES/Framer/De-Framer/Control and Management. This FPGA 902 interfaces with another FPGA 903 that performs the following Digital Signal Processing tasks: Crest Factor Reduction/ Digital Upconversion/Digital Downconversion and Digital Predistortion. Another embodiment will be to integrate 902 with 903 in a single FPGA. The Serializer/De-serializer (SERDES) module converts the high speed serial bit stream from the optical to electrical receiver to a parallel bit stream. The De-Framer decodes the parallel bit stream and extracts the In-phase and Quadrature (I/Q) modulation and delivers this to the digital signal processing module 903. The Control and Management module extracts the control signals from the parallel bit stream and performs tasks based on the requested information. The received I/Q data from the optical interface is frequency translated to an Intermediate Frequency in the Digital Upconverter Module (DUC). This composite signal then undergoes Crest Factor Reduction (CFR) in order to reduce the peak to average power ratio. The resultant signal is then applied to a Digital Predistorter in order to compensate for the distortion in the Power Amplifier module 905. The RRU operates in a receive mode as well as a transmit mode. The RRU receives the signal from the output duplexer and passes this signal to the Rx path or paths, depending on the number of channels. The received signal is frequency translated to an Intermediate Frequency (IF) in the receiver (Rx1 and Rx2 in Figure 10). The IF signal is further downconverted using a Digital Downconverter (DDC) module and demodulated into the In-phase and quadrature components. The recovered I/Q signal is then sent to the Framer module/ SERDES and prepared for transmission over the optical interface.

[0012] The FIG. 9. System has a multi-mode of RF or multi-carrier digital signal or optical at the input, and an RF signal at the output 910. The multi-mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode") or optical input (the "Optical-in Mode"). The FIG. 9. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 915, a power amplifier module 960, a receiver 965 and a feedback path 925.

[0013] The FPGA-based Digital part comprises either one of two digital processors 902,903 (e.g. FPGA), digital-to-analog converters 935 (DACs), analog-to-digital converters 940 (ADCs), and a phase-locked loop (PLL) 945. Since the FIG. 9 System has a multi-input mode, the digital processor has three paths of signal processing. For the baseband signal input path, the digital processor has implemented a digital up-converter (DUC), CFR, and a PD. For the optical input path, SERDES, Framer/ Deframer, digital up-converter (DUC), CFR, and PD are implemented. For the RF input path, analog downconverter, DUC, CFR and PD are implemented.

[0014] The Baseband-in Mode of FIG. 9 contains the I-Q signals. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0015] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a wideband feedback which requires a very high speed ADC. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DACs . As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals 935, respectively. The gate bias voltage 950 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 935 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. The PLL 945 sweeps the local oscillation signal for the feedback part in order to translate the RF output signal to baseband, for processing in the Digital Module.

[0016] The power amplifier part comprises an AQM for real and complex signals (such as depicted in the embodiments shown in Figure 9) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental RRU system. One such Doherty power amplifier

technique is presented in commonly assigned U.S. Provisional Patent Application SN 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0017] The feedback portion comprises a directional coupler, a mixer, a low pass filter (LPF), gain amplifiers and, and a band pass filter (BPF),. Depending upon the embodiment, these analog components can be mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the LPF, the gain amplifier, and the BPF which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the DET 970 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, which shows a polynomial-based predistortion algorithm and from Figure 4, which shows the primary adaptive predistorter blocks which can be used in some embodiments of the invention.

[0018] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a

small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 907, hence maximizing the RRU system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC in the FPGA-based Digital portion and an extra UPC in the power amplifier part. The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0019] FIG. 9. is a block diagram showing a RRU system implemented with AQM according to another embodiment of the present invention (the "FIG. 9 System"). The digital processor of FIG. 9 System has implemented a CFR, a PD, and an analog quadrature modulator corrector (AQMC).

[0020] FIG. 9. is a block diagram showing a RRU system implemented with AQM and AQM-based Clipping Error Restoration Path according to another embodiment of th_e present invention (the "FIG. 9 System"). The Clipping Error Restoration Path in FIG. 9 System has two DACs in the FPGA-based Digital part and an AQM in lieu of the UPC in the power amplifier part.

[0021] Figure 10 is a block diagram showing a dual channel RRU implemented with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as $occu_{rs}$ in a $_T$ime

Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. An additional switch is used for calibrating the Digital Predistorter for each power amplifier. Another embodiment of the RRU is extending its applications to multi-frequency bands. In an embodiment, a multi-frequency band (ie. 2 or more bands) implementation comprises adding additional channelized power amplifiers in parallel. The output of the additional power amplifiers will be combined in an N by 1 duplexer and fed to a single antenna, although multiple antenna can also be utilized in some embodiments. Another embodiment of the multi-frequency band RRU combines two or more frequency bands in one or more of the power amplifiers.

Figure 11 is a block diagram showing another embodiment of the dual channel RRU. In this embodiment the Rx switch is placed on the third port of the circulator, thereby reducing the insertion loss between the PA output and the duplexer.

Figure 12 is a block diagram showing an embodiment of an 8 channel RRU. In this embodiment, the feedback path consists of a receiver chain plus a wideband capture chain. The receiver chain is required when the RRU is switched to a receive mode. The wideband capture chain is required for capturing the wideband distortion of the power amplifier. In addition a channel calibration algorithm is required in order to insure that each power amplifier output is time, phase and amplitude aligned to each other.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA).

Figure 1 shows the block diagram of linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The primary DPD blocks are shown in Figure 4.

Delay Estimation Algorithm:

The DPD estimator compares $\mathrm{x(n)}$ and its corresponding feedback signal $\mathrm{y(n-\Delta d)}$ to find the DPD coefficients, where $\mathrm{\Delta d}$ is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $\mathrm{x(n)}$, and feedback data, $\mathrm{y(n)}$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign(y(i+m+1) - y(i+m))$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $\mathrm{C(m)}$ is the feedback path delay..

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is

necessary. To simplify the design, only a half-sample delay is considered in this design. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel.

The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{jo,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{jhe}$$

Magnitude correction:

As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

The choice of N will depend on the accuracy desired.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^j$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = k_a k_b / k_a'$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & \overline{d(1)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_1^{1/2}} & 0 \\ \overline{q_1^*} & \overline{e_a^*(1)\gamma^{\frac{1}{2}}(1)} \\ \overline{h_1 \Phi_1^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(1)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{*}_{z}}[w_i - \bar{w}] = \bar{q}_1$$

In the iterative process, a block of data (in this design, there is 4096 data in one block) is stored in memory, and the algorithm uses all the data in memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data are processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficient as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

Channel Calibration Algorithm

The 8 channel RRU in Figure 12 has 16 distinct power amplifiers. Half the power amplifiers are designed for one band and the other for a second band . The bands are hereafter referred to as band A and band B, they occupy two distinct frequencies. The 8 channel RRU uses 8 antennas and both bands will coexist on each antenna. In order to maximize performance, each power amplifier's output signal needs to be time, phase and amplitude aligned with respect to each other. The antenna calibration algorithms consist of three distinct approaches: 1) A Pilot Tone is injected into each PA 2) a Reference Modulated signal is transmit through each PA 3) the Real Time I/Q data is used as the reference signal . The Pilot Tone approach requires the injection of a single carrier IF tone that will be tracked in either the feedback calibration path or the individual PA's receiver. Each transmitter

path for band A will be time, phase and amplitude aligned with respect to each other, similarly for band B. The Reference Modulated approach will utilize a stored complex modulated signal which will be transmitted through each of the band A PAs, similarly for the band B PAs. The transmitters will then be time, phase and amplitude aligned with respect to each other. Either the feedback calibration path or the individual receivers can be used for obtaining the PA output signals. The Real Time approach will operate on the real-time transmitted signals. This approach will utilize the DPD time alignment, phase and magnitude offset information to synchronize each PA output with respect to each other.

[0022] In summary, the RRU system of the present invention could enhance the performance for the efficiency and linearity more effectively since the RRU system is able to implement CFR, DPD and adaptation algorithm in one digital processor, which subsequently saves hardware resources and processing time. The high power efficiency of RF power amplifiers inside the RRU means that less thermal dissipation mechanism such as heat sink is needed; therefore, significantly reducing the size and volume of the mechanical housing. This smaller RRU can then enable service provider to deploy the RRU in areas where heavy or large RRU could not be deployed, such as pole tops, top of street lights, etc. due to lack of real estate, or weight limitation, wind factor, type of safety issues. The RRU system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime.

[0023] **M**oreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. The multi-frequency bands benefits mean that mobile operators can deploy fewer RRUs to cover more frequency bands for more mobile subscribers; hence significantly reducing CAPEX and OPEX. Other benefits of the RRU system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0024] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A remote radio head unit (RRU) system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier inside the RRU. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are monitored by a wideband feedback path and controlled by the adaptation algorithm in a digital module. Therefore, the present invention could compensate the nonlinearities as well as memory effects of the power amplifier systems and also improve performances, in terms of power added efficiency, adjacent channel leakage ratio and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands and multi-channels. As a result, the remote radio head system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems.

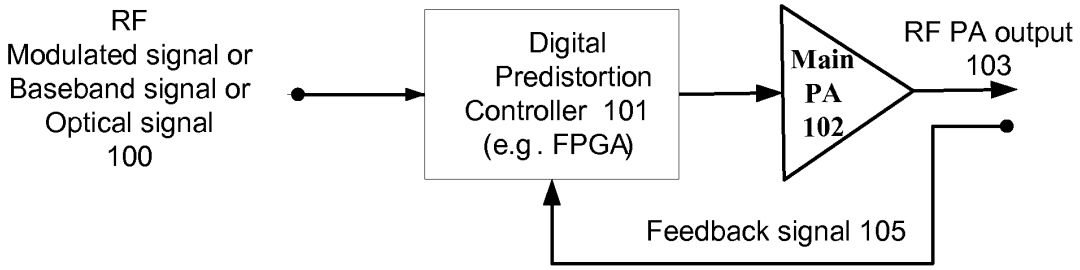
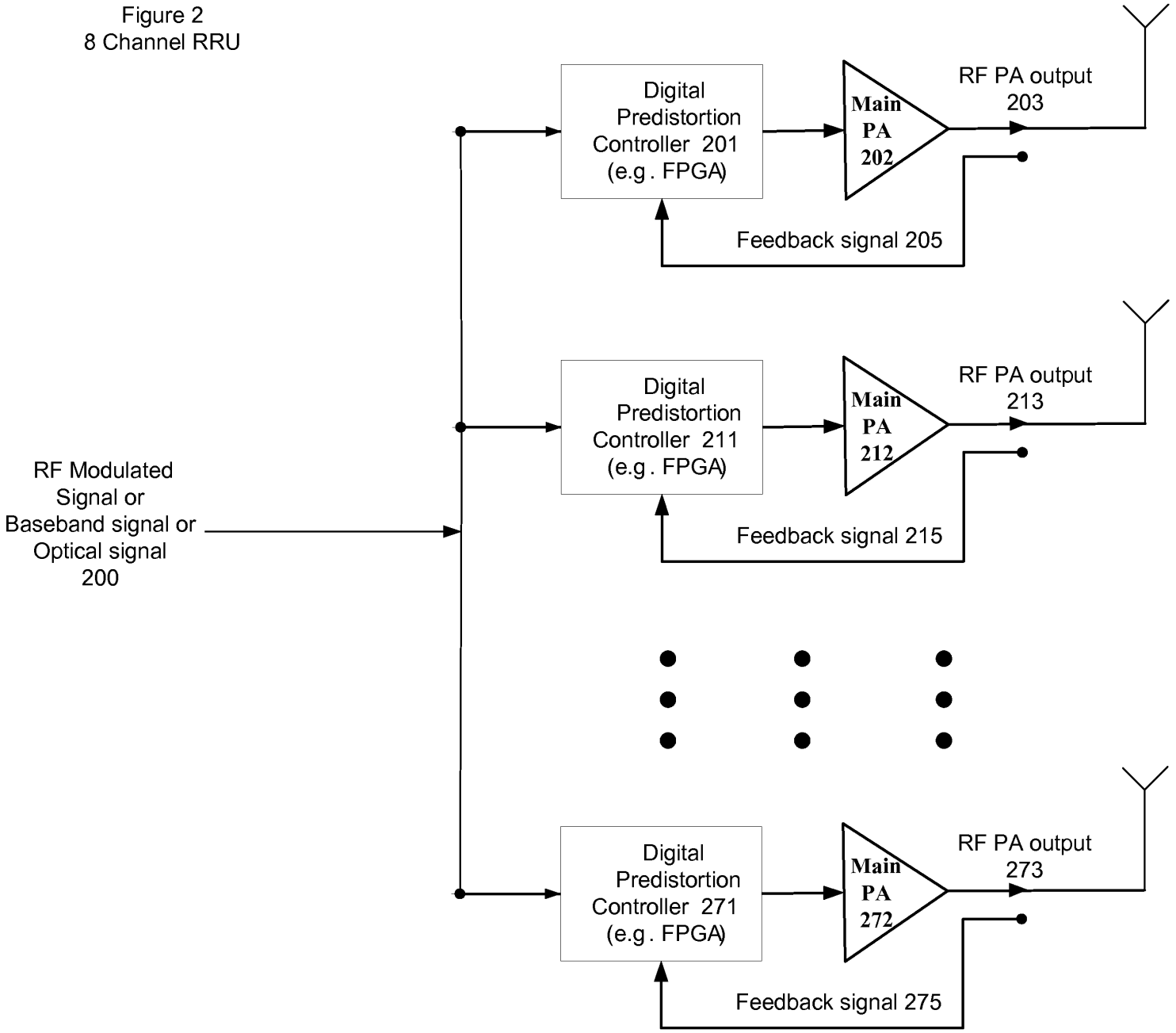


FIG. 1. Remote Radio Head Unit

Figure 2
8 Channel RRU



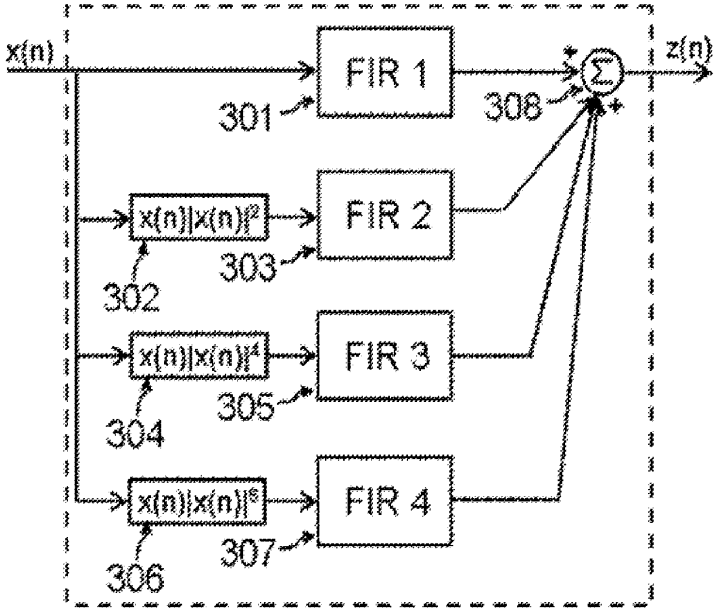


Figure 3. Polynomial based digital predistorter function

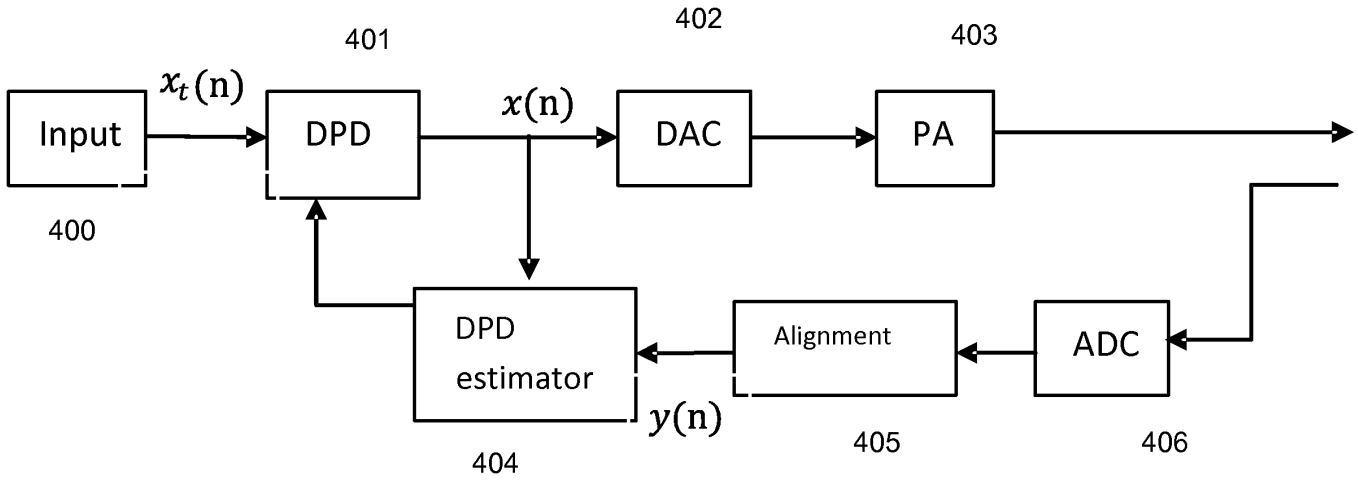


FIG. 4. Digital Predistortion Block Diagram

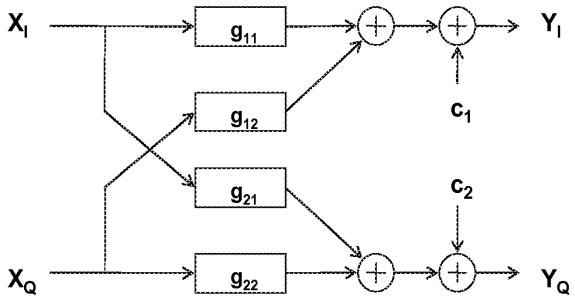


Figure 5 Analog Quadrature Modulator Compensation Block

Wall Mount
RRU 615
Rooftop
Mount RRU
610
Tower Mount
RRU 605
Base Station
Server 600

Figure 6

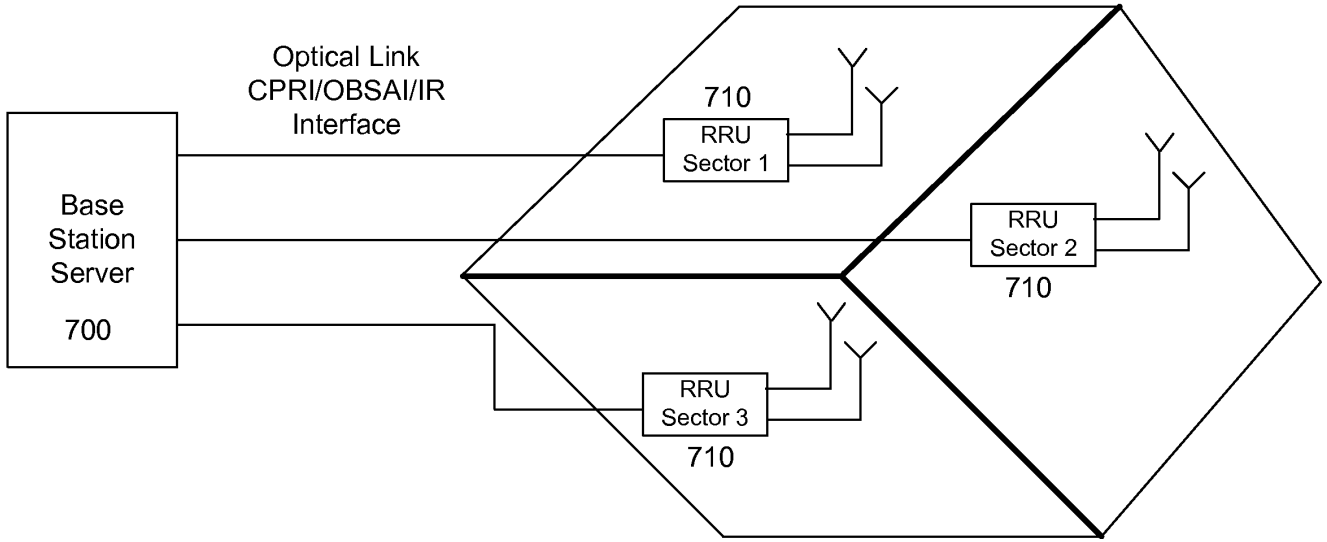

Optical Link
CPRI/OBSAI/IR
Interface
Base
Station
Server
700
710
RRU
Sector 1
RRU
Sector 2
710
RRU
Sector 3
710

Figure 7

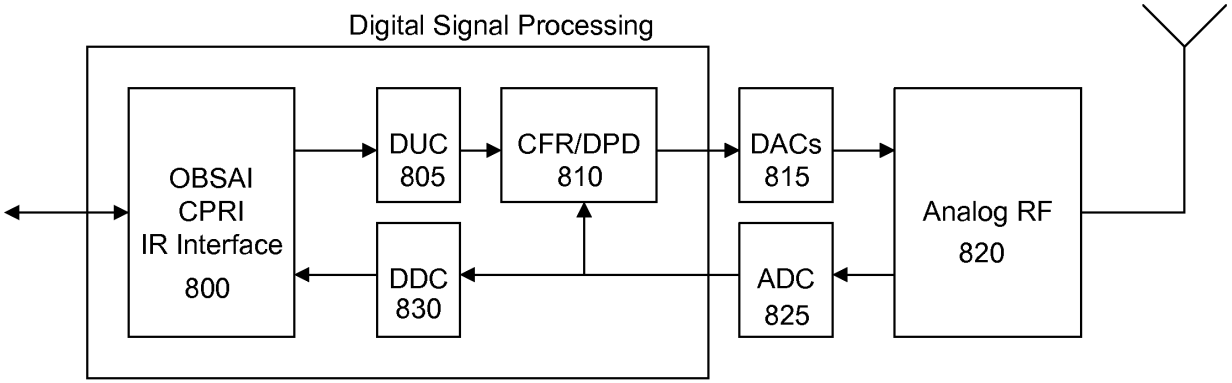

Digital Signal Processing
OBSAI
CPRI
IR Interface
800
DUC
805
CFR/DPD
810
DDC
830
DACs
815
ADC
825
Analog RF
820

Figure 8

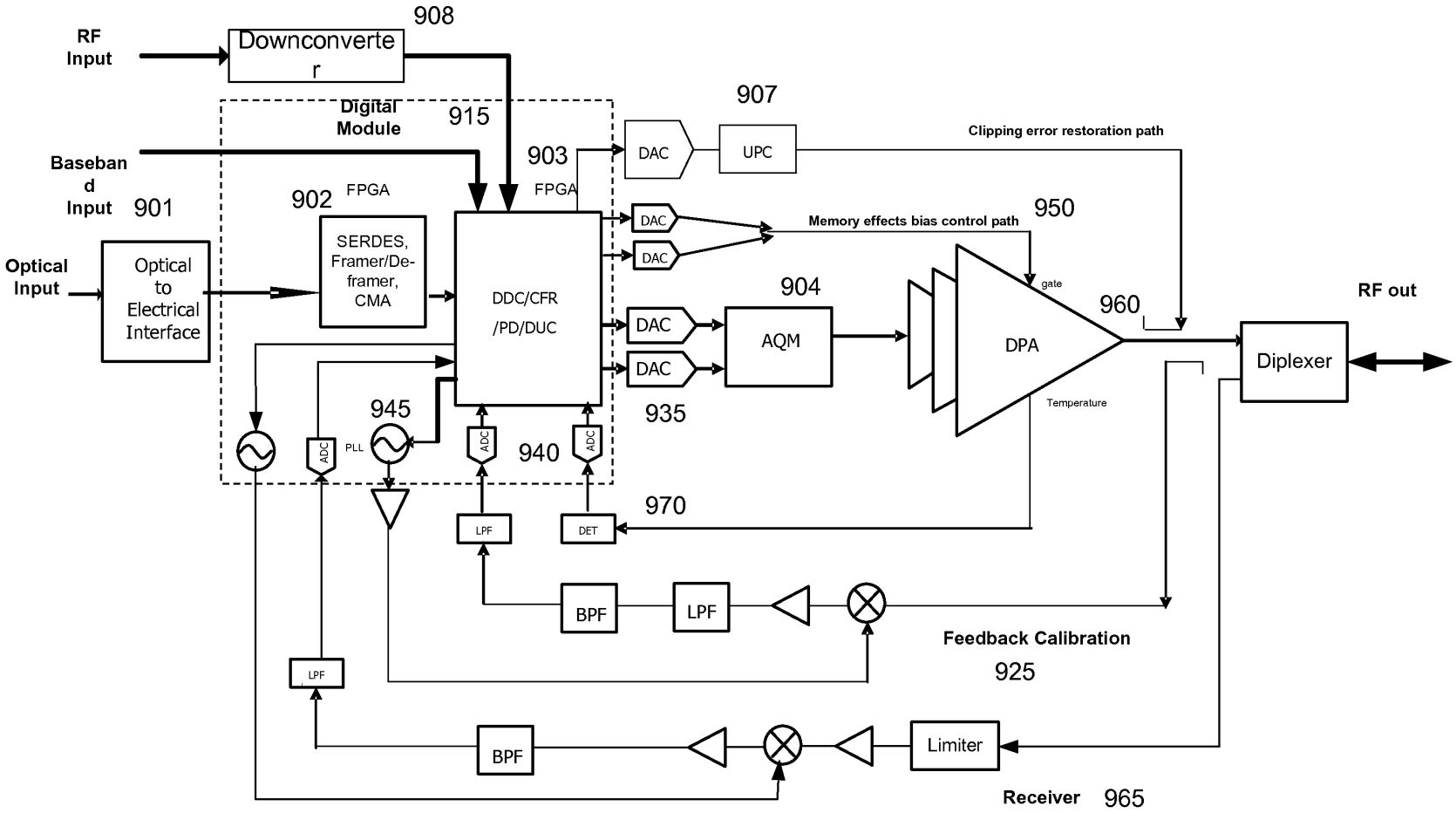


Figure 9 Digital Hybrid Module

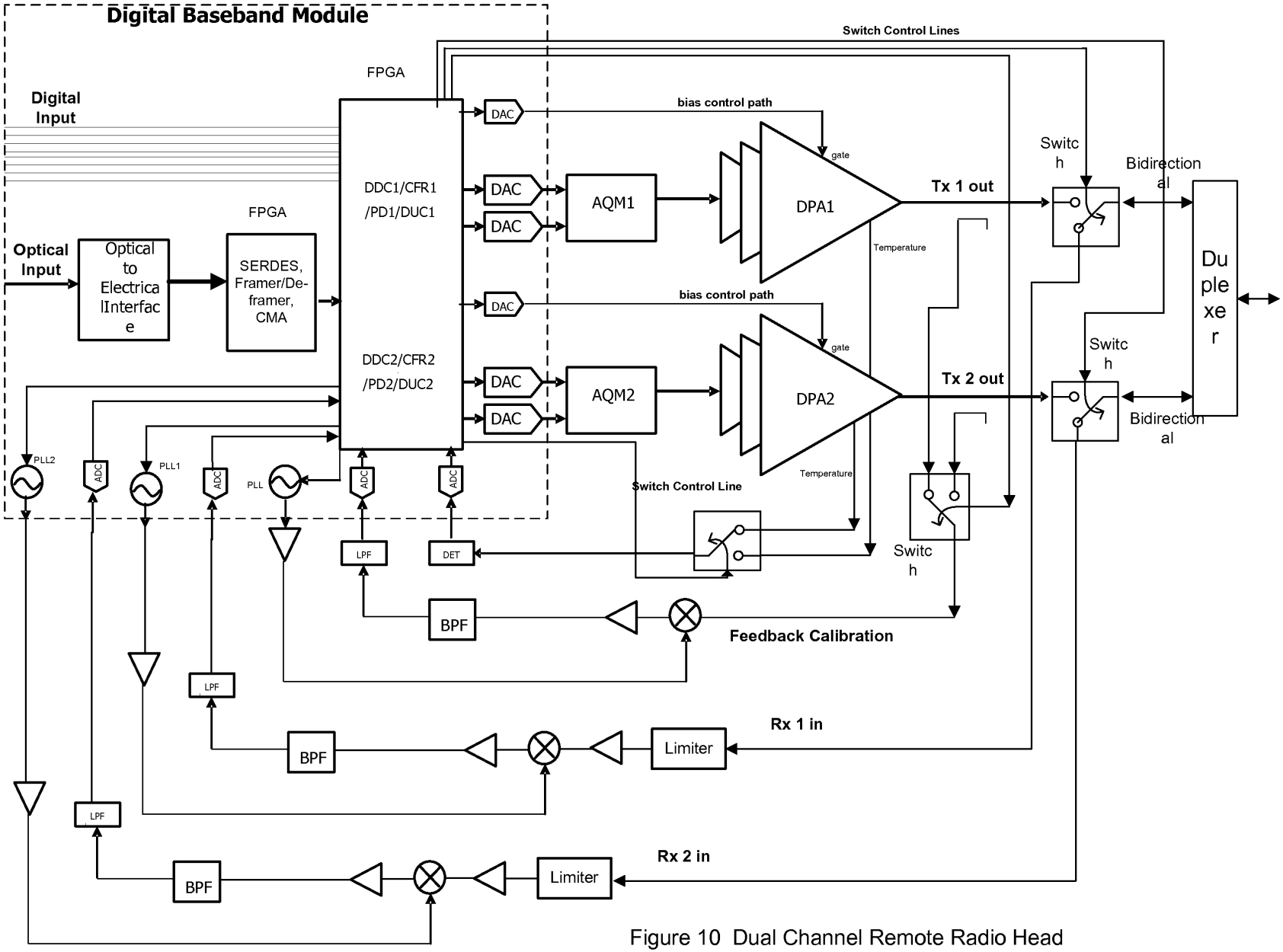


Figure 10 Dual Channel Remote Radio Head

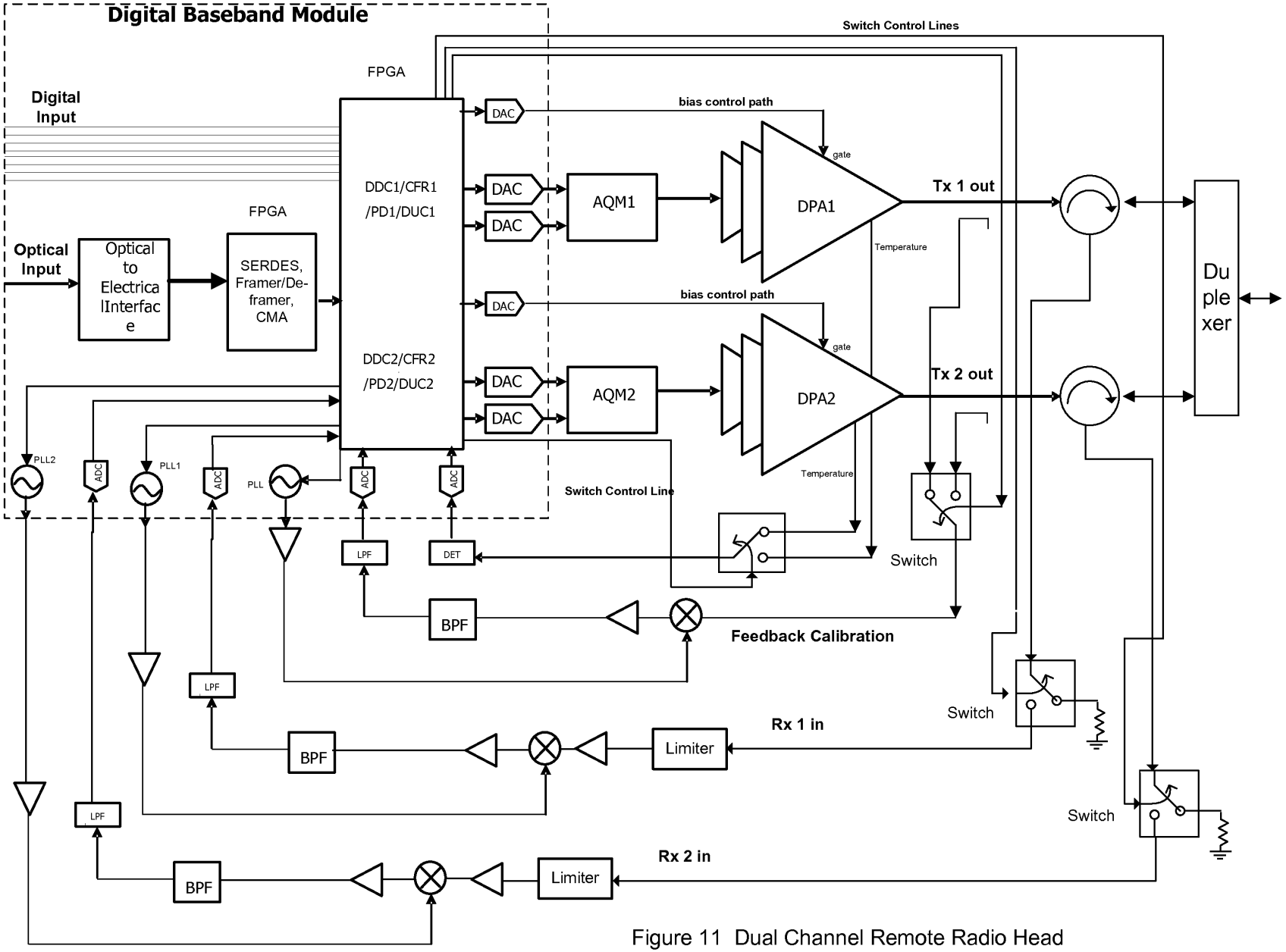
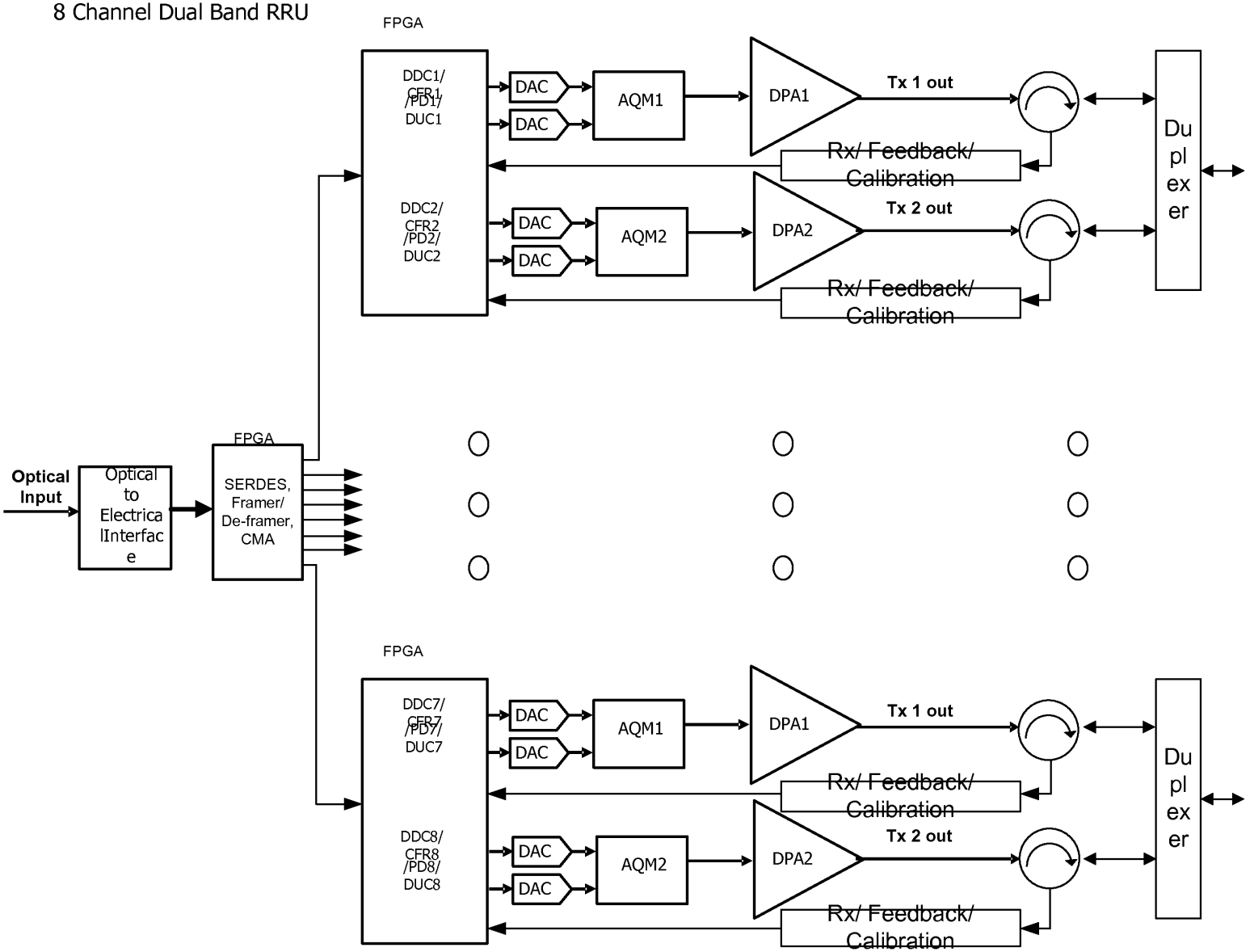


Figure 11 Dual Channel Remote Radio Head

Figure 12
8 Channel Dual Band RRU



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM

INVENTORS

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Kyoung-Joon Cho, Citizen of Korea

Shawn Patrick Stapleton, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[001] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[002] A wideband mobile communication system using complex modulation techniques, such as wideband code division access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. Conventional digital predistortion (DPD) techniques have an operational bandwidth limitation.

[003] Conventional DSP-based DPD schemes utilize FPGAs, DSPs or microprocessors to compute, calculate and correct the PA's nonlinearities: they perform fast tracking and adjustments of signals in the PA system. However, conventional DSP-based DPD schemes are challenged by variations of the linearity performance of the power amplifier over wide bandwidths due to the environment changing such as temperature and the

asymmetric distortions of the output signal of the PA resulting from memory effects. Conventional DPD algorithms are based on a wideband feedback signal, they require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. Multi-frequency band, or simply multi-band, applications can have their operating frequencies spaced significantly apart. Conventional DPD architectures use an ADC sampling rate that is greater than twice the nonlinear distortion bandwidth of the input signal. This sampling rate is typically more than double a factor of five times the operating bandwidth of the complex modulated signal. The factor of five accounts for the spectral re-growth attributed to the nonlinear distortion created by the power amplifier. This restriction on sampling rate, limits the feasibility of the conventional predistortion architectures to single band applications. Higher sampling rate ADCs have lower resolution, consume more power and are more expensive.

SUMMARY OF THE INVENTION

[004] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers, and multi-channels.

[005] To achieve the above objects, according to the present invention, the technique is based on the method of adaptive digital predistortion to linearize a RF power amplifier. The present invention is based on using distinct signals from different frequencies (Multi-Band Signals). These Multi-Band Signals will experience distortion by the power amplifier and create nonlinear distortion centered on each carrier that is approximately five times their individual bandwidths. The feedback signal from the power amplifier's are down converted to an intermediate frequency (IF) that insures that the fundamental carrier bandwidths will not be aliased onto each other after sampling in the ADC. The present invention can accommodate aliasing of the nonlinear distortion of the individual carriers.

[006] Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction (CFR), DPD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator (AQM) compensation structure is also utilized to enhance performance.

[007] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called an adaptive DPD algorithm, which is implemented in the digital domain and taught in the applications incorporated herein by reference and attached as an Appendix.

Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless

devices, and other wireless communication systems such as microwave and satellite communications.

THE FIGURES

[008] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[009] Figure 1 is a block diagram showing the basic form of a digital predistortion power amplifier system.

[0010] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0011] Figure 3 is a block diagram showing polynomial based predistorter of the present invention.

[0012] Figure 4 is a block diagram of the digital predistortion Direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0013] Figure 5 is a block diagram of the digital predistortion In-direct Learning algorithm applied for self-adaptation in a digital predistortion power amplifier system of the present invention.

[0014] Figure 6 is a depiction of the frequency domain signals present in the aliased digital predistortion system.

[0015] Figure 7 is an embodiment of the Quadrature Modulator compensation block architecture.

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DPD	Digital Predistortion
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude

FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0016] The present invention is a novel multi-band predistortion system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers that operate simultaneously over multiple, distinct frequency bands.

[0017] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the DPD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system, as further discussed in the applications incorporated by reference. The present invention is a “black box”, plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101.

[0018] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD, Figure 2. The coefficients of the DPD are adapted by a synchronizing the wideband captured, aliased output Multi-BandSignal *ya[n]* from the feedback path (Sampled Feedback Aliased Signal) with the reference Multi-Band Signal *x[n]* (Input Signal). The DPD algorithm performs the synchronization and compensation. The synchronization aligns the reference signal with the aliased feedback signal in the alignment block. In one embodiment of the DPD algorithm, the reference signal and the aliased Sampled Feedback Aliased Signal *ya[n]* are used in the Direct Learning adaptive algorithm. In another embodiment of the DPD algorithm, the aliased predistorted signal *za[n]* (Predistorted Output Aliased Signal) and the Sampled Feedback Aliased Signal *ya[n]* are used in an Indirect Learning adaptive algorithm.

[0019] Some embodiments apply crest factor reduction (CFR) prior to the DPD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is typically used, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems,

incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0020] In all embodiments, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the DPD. The coefficients of the DPD are adapted by synchronizing the wideband captured output signal from the feedback path with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal via a DAC. The DQM is not required to be implemented in the FPGA, or at all, in all embodiments. If the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals, respectively.

[0021] FIG 3. is a block diagram showing a predistortion (PD) part in the DPD system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the PD system in FIG. 3. has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306.

The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows the block diagram of a digitally predistorted PA system. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3) .

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4 and Figure 5. The coefficients are obtained using the QR RLS adaptive algorithm in the DPD estimator block.

Figure 4 shows one embodiment of the multi-band digital predistorter. The Direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the aliased sampled Multi-Band Signal *xa[n]* (Sampled Input Aliased Signal) as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

Figure 5 shows another embodiment of the multi-band digital predistorter. The in-direct Learning adaptive algorithm has two inputs into the DPD estimator. The DPD estimator uses the Predistorted Output Aliased

Signal *za[n]* as a reference and the Sampled Feedback Aliased Signal *ya[n]* as an input.

A depiction of the spectrum domain plots are shown in Figure 6. The reference Input Signal *x[n]* shows two distinct bands centered at frequencies F_a and F_b. The operating bandwidth of the individual carriers is small in comparison to the frequency spacing between the carriers. The nonlinearities in the power amplifier will cause spectral re-growth as shown in the analog feedback Multi-Band Signal *y(t)* (Analog Feedback Signal). The Analog Feedback Signal is down converted to an intermediate frequency Fi which is selected to be in the 1st Nyquist zone as shown in Figure 6. The choice of frequency Fi is dependent on the ADC sampling rate used, the operating bandwidth of the carriers and the frequency separation (F_a - F_b) between the carriers. The ADC sampling rate is typically the limiting factor in the choice of Fi. For a two carrier system F_a is positioned in the 1st Nyquist zone and F_b is positioned in the 2nd Nyquist zone in at least some embodiments. The choice of Fi limits how close Fa and Fb can be separated together.

Sampling on the Analog Feedback Signal *y(t)* generates images as shown in the spectrum for the Sampled Feedback Aliased Signal *ya[n]*. The nonlinear distortion from the individual carriers are allowed to alias onto each other as long as the aliased part of the signal does not adversely impact the original Multi-Band signal. A Direct Learning algorithm uses the difference between *xa[n]* and *ya[n]* to minimize the resultant error signal. The QR RLS algorithm uses this error to adapt the predistorter coefficients in the DPD estimator. The In-Direct learning algorithm first models the power amplifier using the Predistorted Output Aliased Signal *za[n]* and the Sampled Feedback Aliased

Signal *ya[n]*. The modelled power amplifier coefficients are then used to calculate the predistorter coefficients.

[0022] FIG. 7. is a block diagram showing the analog quadrature modulator compensation structure. The analog quadrature modulator will translate the baseband signal ouput from the DACs to an RF frequency. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12 , g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2 . The frequency dependence of the AQM will be compensated by the filters {g11, g12 , g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

[0023] In summary, the multi-band wideband power amplifier predistortion system of the present invention can significantly reduce the feedback ADC sampling rate requirements. This will enable multi-band wideband applications and reduce the power consumption and cost. The system is also reconfigurable and field-programmable since the algorithms and power efficiency enhancing features can be adjusted like software in the digital processor at anytime, as discussed in greater detail in the applications incorporated by reference and attached as an Appendix.

[0024] Moreover, the multi-band wideband DPD system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that

the DPD system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DPD system includes correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0025] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A high performance and cost effective method of RF-digital hybrid mode power amplifier systems with high linearity and high efficiency for multi-frequency band wideband communication system applications is disclosed. The present disclosure enables a power amplifier system to be field reconfigurable and support multiple operating frequency bands on the same PA system over a very wide bandwidth. In addition, the present invention supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels.

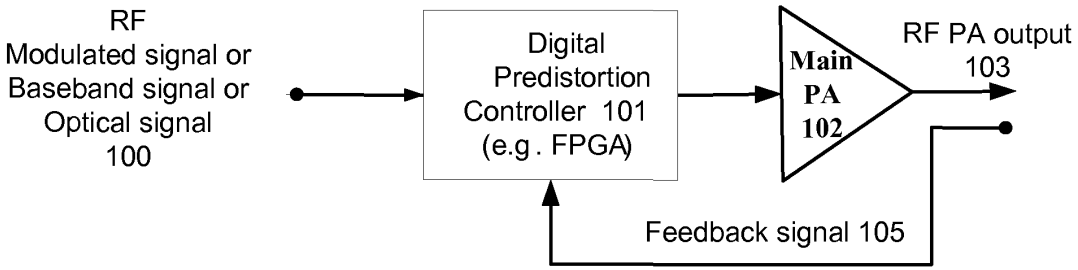

RF
Modulated signal or
Baseband signal or
Optical signal
100
Digital
Predistortion
Controller 101
(e.g. FPGA)
Main
PA
102
RF PA output
103
Feedback signal 105

Figure 1

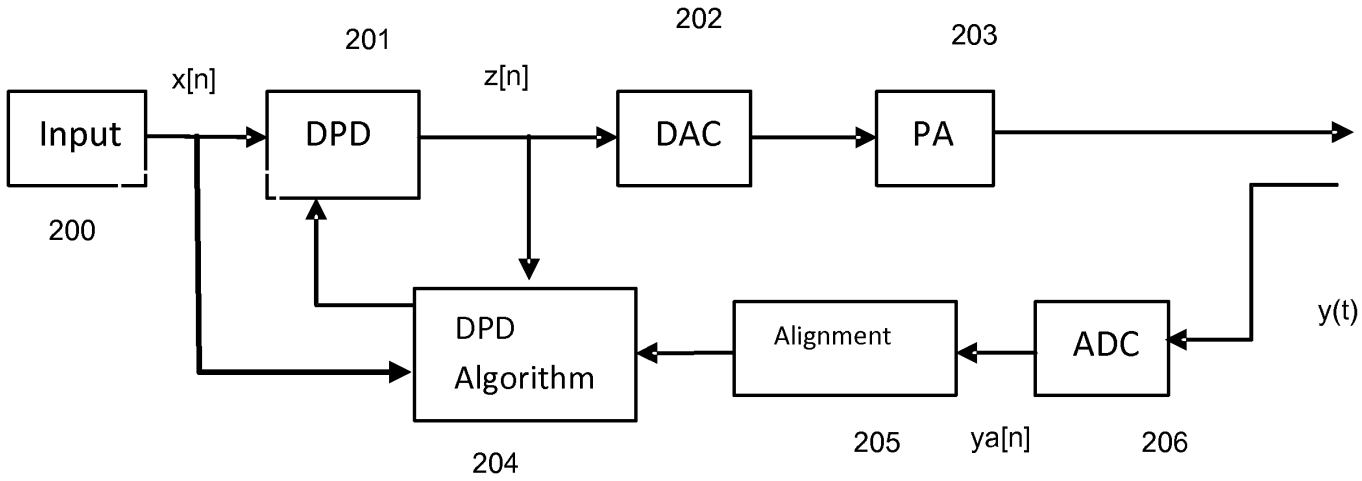


FIG. 2. Digital Predistortion Block Diagram

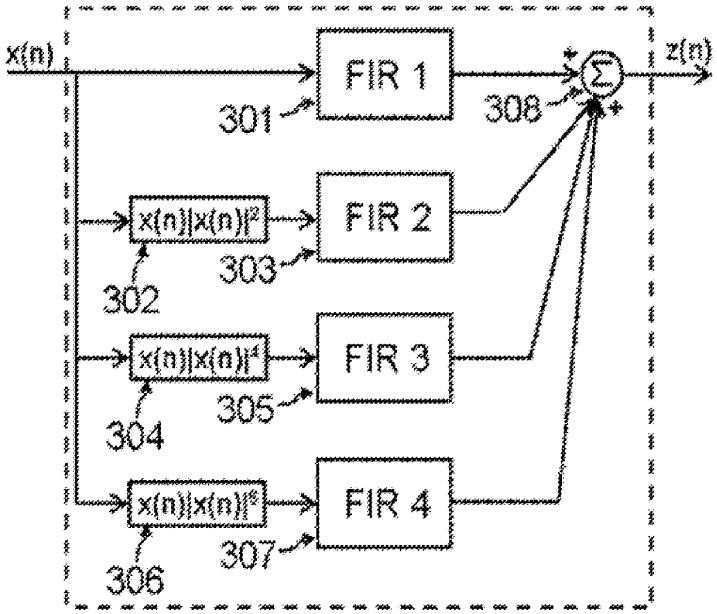


FIG. 3. Polynomial based Predistorter

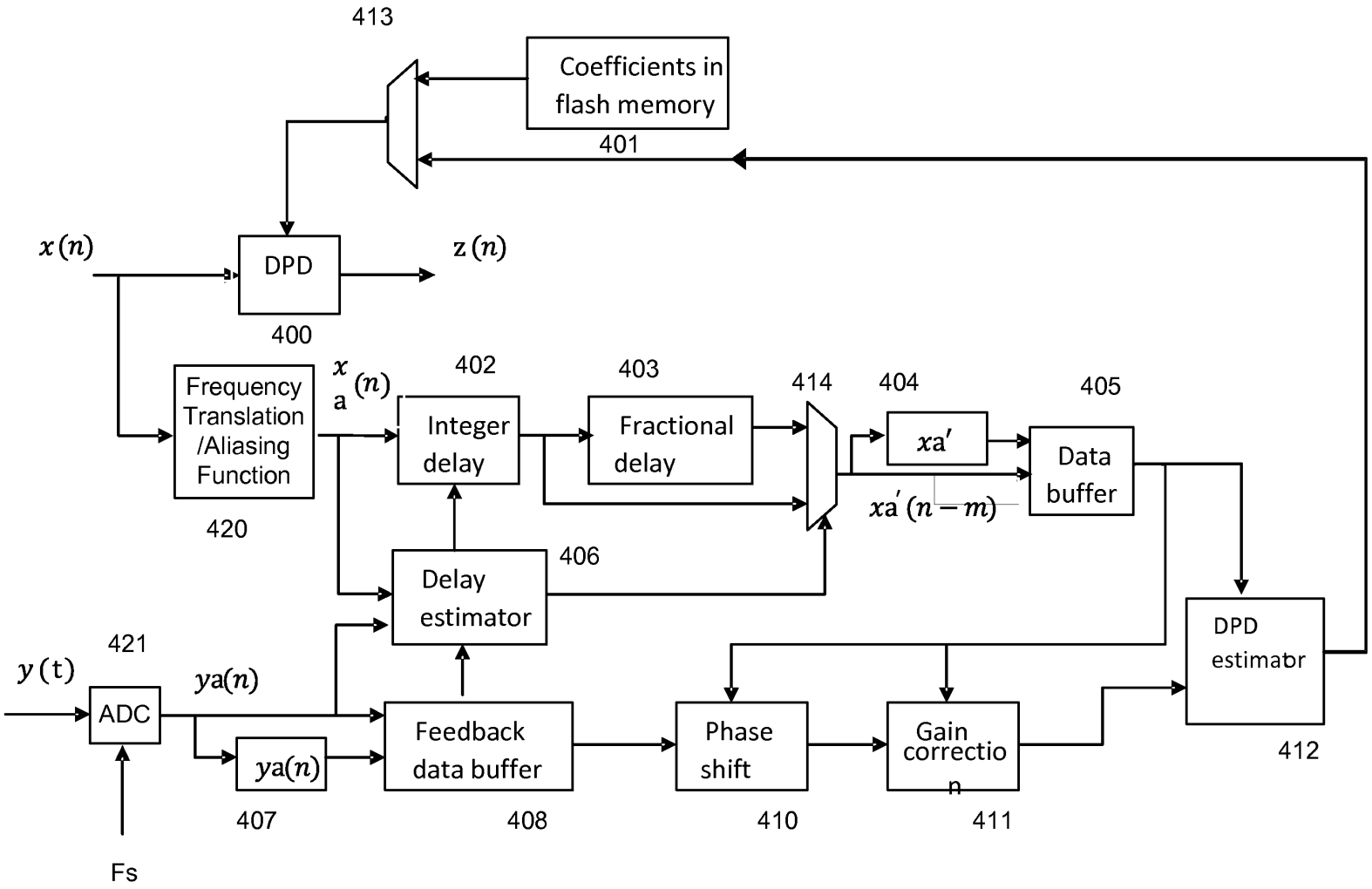


FIG. 4. Digital Predistortion Direct Learning Algorithm

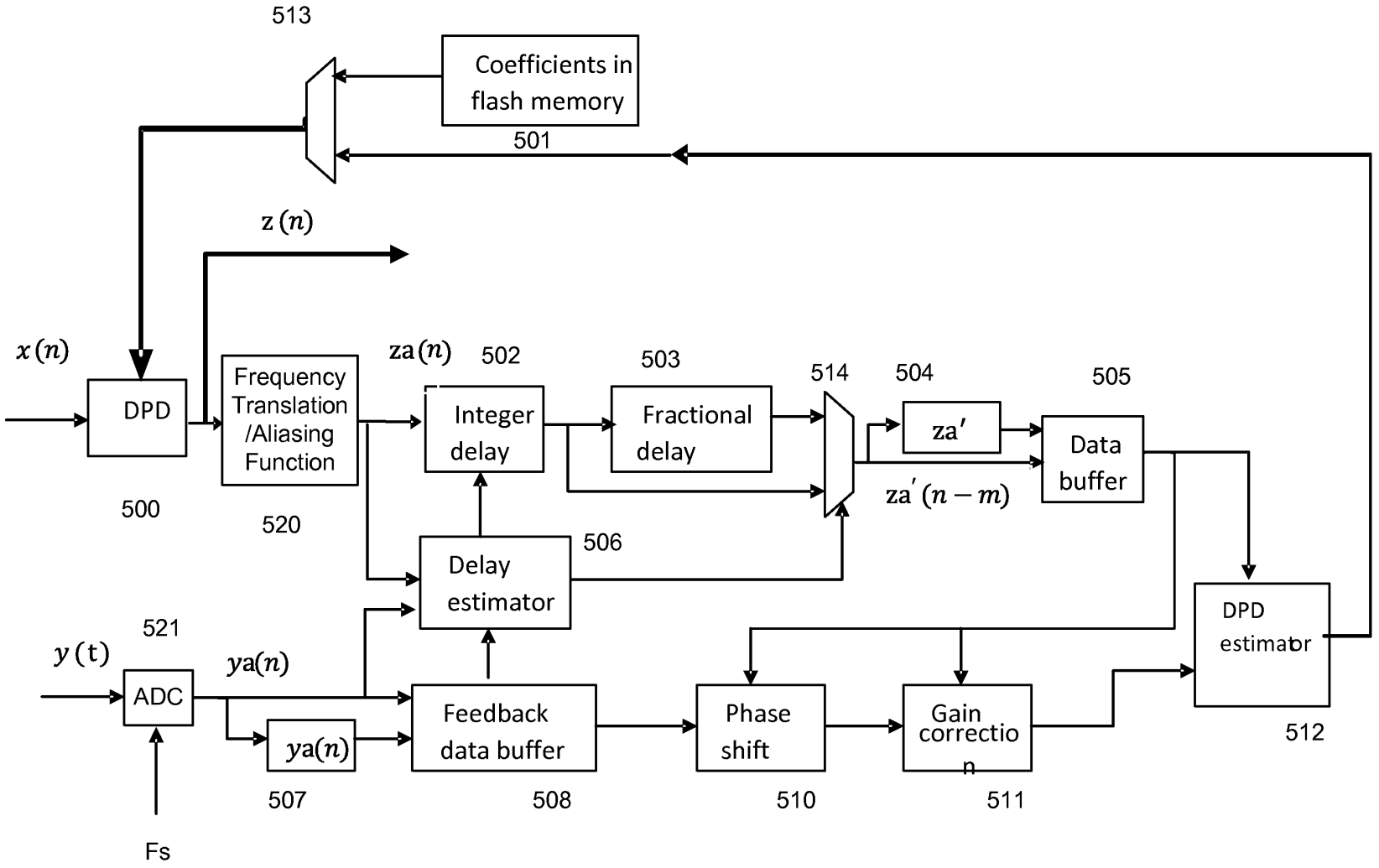


FIG. 5. Digital Predistortion Indirect Learning Algorithm

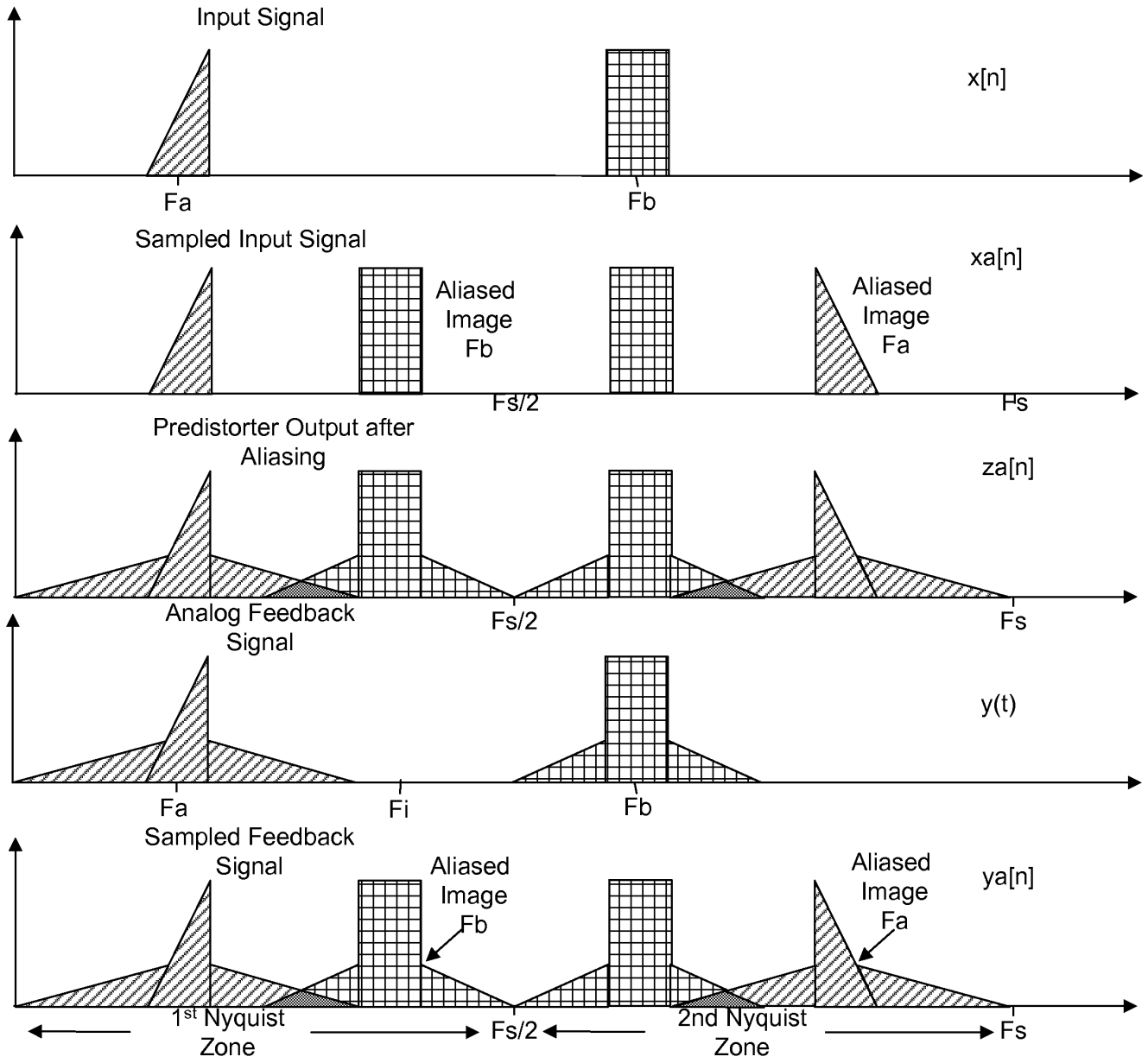

Input Signal
x[n]
Fa
Fb
Sampled Input Signal
xa[n]
Aliased
Image
Fb
Aliased
Image
Fa
Fs/2
Fs
Predistorter Output after
Aliasing
za[n]
Analog Feedback
Signal
Fs/2
Fs
y(t)
Fa
Fi
Fb
Sampled Feedback
Signal
Aliased
Image
Fb
Aliased
Image
Fa
ya[n]
1st Nyquist
Zone
Fs/2
2nd Nyquist
Zone
Fs

Figure 6

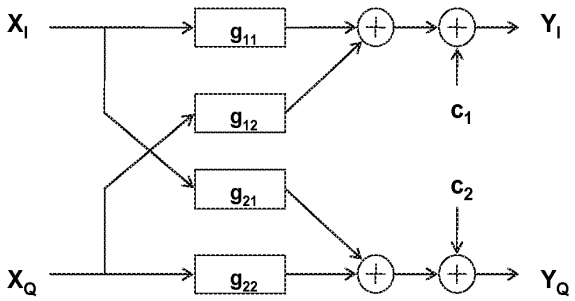


Figure 7: Analog Quadrature Modulator Compensation Block

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

REMOTE RADIO HEAD UNIT WITH WIDEBAND POWER AMPLIFIER AND METHOD

INVENTORS

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Shawn Patrick Stapleton, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

This application claims the benefit of the following applications, attached as Appendices:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

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US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER

SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

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All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present invention generally relates to wireless communication systems using power amplifiers and remote radio head units (RRU or RRH). More specifically, the present invention relates to RRU which are part of a distributed base station in which all radio-related functions are contained in a small single unit that can be deployed in a location remote from the main unit.

BACKGROUND OF THE INVENTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective solutions to expand network capacity and evolution towards 4G and beyond.

Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell throughput growth. The latest standards supporting this are HSPA+, WiMAX, TD-SCDMA and LTE. The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years.

Distributed open base station architecture concepts have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the Open Base Station Architecture Initiative (OBSAI), the Common Public Radio Interface (CPRI) , and the IR Interface standards introduced standardized interfaces separating the Base Station server and the remote radio head part of a base station by an optical fiber.

The RRU concept is a fundamental part of a state-of-the-art base station architecture. 2G/3G/4G base stations are typically connected to RRUs over optical fibers. Either CPRI, OBSAI or IR Interfaces may be used to carry data to the RRH to cover a three-sector cell. The RRU incorporates a large number of digital interfacing and processing functions. Traditionally, a multi-channel RRU means that multiple antennas are used, typically with two power amplifiers for two distinct bands. A duplexer is used to combine the two power amplifier outputs. Switches are used to isolate the transmit signals from the received signals as occurs in a Time Division Synchronous Code Division Multiple Access (TD-SCDMA) modulation. To extent the prior art architecture to multiple bands (i.e., two or more bands) implementation would consist of adding additional channelized power

amplifiers in parallel. The output of the additional power amplifiers is typically combined in an N by 1 duplexer and fed to a single antenna.

While conventional RRU architecture offers some benefits, RRUs to date are power- inefficient, costly and inflexible. Further, their poor DC-to-RF power conversion insures that they will have a large mechanical housing. In addition, current RRU designs are inflexible. As standards evolve, there is a need for multi-band RRUs that can accommodate two or more operating channels using a single wideband power amplifier. This creates an isolation problem at the individual receivers because the wideband power amplifier is always turned on. Isolation between the wideband transmitter and receivers is a problem with any modulation standard (HSPA+, WiMAX, LTE, etc.) when multi-band RRUs are developed using a single power amplifier This is a common problem for all communication systems that utilize a wideband power amplifier in a multi-band scenario.

SUMMARY OF THE INVENTION

[001] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective technique for implementing RRU systems that service multi-frequency bands. Further, the present disclosure enables a RRU to be field-reconfigurable, and supports multi-modulation schemes (modulation agnostic), multi-carriers, multi-frequency bands, and multi-channels. The present invention also serves multi-frequency bands within a single RRU to economize the cost of radio network deployment. In particular, the present invention resolves an isolation issue for a RRU with fewer power amplifiers than the number of operating frequency bands. Multi-

mode radios capable of operating according to GSM, HSPA, LTE, TD-SCDMA and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks.

[002] The present invention achieves the above objects using techniques generally based on methods and techniques for maximizing the isolation between the transmitted signal (Tx Signal) and the received signal (Rx Signal). The Tx Signal may comprise noise generated at the output of the power amplifier or it may comprise an unwanted transmitter band leaking into the receiver. With the use of the present invention, conventional RRU's can be extended to a multi-band and multi-channel configuration. Multi-band means that more than one frequency bands are used in the RRU and multi-channel means that more than one output antenna is used. Various embodiments of the invention are disclosed.

[003] An embodiment of the present invention utilizes duplexers, switches and circulators to maximize the isolation between the transmitter and receiver. Another embodiment of the present invention utilizes an Interference Cancellation System (ICS) together with duplexers, switches and circulators.

[004] Applications of the present invention are suitable for use with all wireless base-stations, remote radio heads, distributed base stations, distributed antenna systems, access points, repeaters, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

The present invention is also field upgradable through a link such as an Ethernet connection to a remote computing center.

THE FIGURES

[005] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[006] Figure 1 is a block diagram of a TD-SCDMA dual-band single PA configuration in a remote radio head unit system in accordance with the present invention.

[007] Figure 2 is a block diagram of the TD-SCDMA dual-band single PA with a Interference Cancellation System (ICS) configuration in a remote radio head unit system in accordance with the present invention.

[008] Figure 3 is a FDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[009] Figure 4 is an Interference Cancellation System using Power Detection.

[0010] Figure 5 is a TDD Modulation Agnostic Dual-Band Remote Radio Head with an Interference Cancellation System.

[0011] Figure 6 is an Interference Cancellation System using Correlation.

Glossary of Terms

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter

AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
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I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRU	Remote Radio Head Unit
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

The present invention is a novel RRU system that utilizes a wideband power amplifier. The present invention is a hybrid system of digital and

analog modules. The interplay of the digital and analog modules of the hybrid system eliminates interference between the wideband power amplifier output and the receiver's inputs.. The present invention, therefore, achieves higher Transmitter (Tx) to Receiver (Rx) isolation when using wideband power amplifiers with multiple frequency bands .

Referring first to Figure 1, an embodiment of some aspects of the invention is shown in block diagram form. Figure 1 depicts the analog section of a dual channel RRU. In this embodiment a single wideband power amplifier 404 is used. The two distinct frequency band signals are combined in a duplexer 403 and input to the wideband power amplifier 404. The output of the wideband power amplifier 404 is sent to a diplexer 405 in order to separate the two frequency band signals. This configuration enables the individual transmitter frequency bands to be independently turned-off. The Tx switches 405 and 407 are placed in the signal path after the diplexer 405. The signals are then passed through circulators 411 and 412 and a duplexer 413 in order to gain further isolation between the Tx signals and the Rx signals. The Rx switches 408 and 410 are placed on the third port of the circulator. Alternatively, two or more frequency bands can be combined in one power amplifier using the same architecture as in Figure 1.

Figure 2 illustrates a further alternative embodiment of the dual-band single wideband power amplifier RRU analog section. In the embodiment of Figure 2, an interference cancellation system (ICS) 520 is utilized to improve the isolation between the transmitter and receivers. The interference cancellation system generates a replicate of the unwanted feedback signal but in anti-phase so as to eliminate the interference. The interference

cancellation system comprises five primary blocks: Delay, variable attenuator, variable phase shifter, Down Converter (DNC) and DSP controller, alternative arrangements of which are shown in Figures 4 and 6, discussed hereinafter. The ICS receives incoming signals through links 506 and 507. The anti-phase output of the ICS is combined with the signals from switches Rx1 and Rx2, indicated at 510 and 511, respectively, by the use of adders 551 and 552, and the resulting signal provides the inputs to the LNA's 515 and 516. The ICS is an adaptive control system which continuously adjusts the variable attenuator as well as the variable phase shifter so as to maintain good interference cancellation. Alternatively, an embodiment of the ICS can comprise a fixed attenuator and phase shifter setting, eliminating the need for DSP control, although in at least some cases this results in inferior performance compared to the adaptive ICS system of Figure 2. The remaining elements of Figure 2 correspond to those shown in Figure 1, and are indicated by the same numerals except that the most significant digit has been changed from "4" to "5".

Figure 3 shows another embodiment of the analog section of a dual-band single wideband power amplifier RRU in Frequency Division Duplex (FDD) mode. This embodiment is modulation agnostic for FDD standard systems, and elements 601-604 operate analogously to elements 401-404 of Figure 1. The triplexer 608 separates the transmitter bands from the receiver bands. FDD systems use different transmit and receive frequencies for each channel. The function of the triplexer 608 is to pass the output of power amplifier 604 to the antenna while isolating the receivers from the transmitter output. The ICS 609 system is utilized for increasing the isolation between

the transmitter output and the receiver inputs as with Figure 2, and receives the output of PA 604 through link 605. The output of the ICS 609 is combined with the appropriate triplexer outputs through adders 610 and 611, and the links 605 feeding the LNA's 612 and 613.

Figure 4 is a depiction of one embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. Coupler 605 is used to sample the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 710. This separates the two frequencies into distinct sections. The delay block 701 time-aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 702 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 703 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 707 or Microprocessor is used to control the attenuator and phase shifter. A power detection based adaptive algorithm in the DSP continuously monitors the signal at the Down Converter (DNC) 708 output and minimizes the level of the interference based on the detected power level . The power level of the interference is measured at the receiver while that band is in the transmit mode of operation. The second band is similarly processed using elements 704, 705 and 706.

Figure 5 shows an embodiment of the analog section of a dual-band single wideband power amplifier RRU in Time Division Duplex (TDD) mode.

This embodiment is modulation agnostic for TDD standard systems. The output of wideband power amplifier 804 feeds a circulator 807. The circulator provides some isolation between the transmitted signals and the receiver inputs. A multi-band filter 820 is placed between the circulator and the output antenna in order to attenuate out-of-band emissions. The third port of the circulator 807 is delivered to a diplexer 808, which separates the two distinct operating bands. TDD mode requires the transmitter and receiver to operate using the same frequency band at distinct times. In order to provide isolation between the transmitter and receiver, switches 821, 822 are used. The switches can provide some isolation but additional isolation may be required depending on the system specifications. The ICS 809 can provide additional isolation between the transmitter output and the receiver inputs in the manner described above.

Figure 6 is a depiction of another embodiment of an Interference Cancellation System (ICS). The function of the ICS is to generate a replicate of the interfering signal and place it in anti-phase to the interference, thereby eliminating the interfering signal. The input to the ICS system is a sample of the power amplifier output. The power amplifier's output is sampled and sent to a diplexer 910. This separates the two frequencies into distinct sections. The delay block 901 time aligns the feedback interfering signal with the sampled power amplifier output. The variable attenuator 902 is adjusted to insure that the interfering signal and the sampled signal have equal magnitude. The variable phase shifter 903 is adjusted to insure that the interfering signal and the sampled signal are in anti-phase. A Digital Signal Processor (DSP) 907 or Microprocessor is used to control the attenuator and

phase shifter. A correlation-based adaptive algorithm in the DSP is used to minimize the level of interference. The DSP correlates the two signals by controlling the output of switch 911 and the output of switch 912 after the signals have been translated to baseband using the two Downconverters 920 and 909. The switches 911 and 912 alternate between the two channels. The objective of the algorithm is to minimize the correlation between the sampled power amplifier output and the interference at the receiver. The computed correlation coefficient is used as the error function in an adaptive algorithm such as a Least Mean Squared (LMS) algorithm.

[001] From the foregoing teachings, those skilled in the art will appreciate that the RRU system of the present invention enables the use of single wideband power amplifier for multi-band operation , which consequently saves hardware resources and reduces costs. The RRU system is also reconfigurable and field-programmable since the algorithms can be adjusted like software in the digital processor at anytime.

[002] Moreover, the RRU system is agnostic to modulation schemes such as QPSK, QAM, OFDM, etc. in CDMA, TD-SCDMA, GSM, WCDMA, CDMA2000, and wireless LAN systems. This means that the RRU system is capable of supporting multi-modulation schemes, multi-frequency bands and multi-channels.

[003] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such

substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A remote radio head unit (RRU) system for multiple operating frequency bands, multi-channels, driven by a single or more wide band power amplifiers. More specifically, the present invention enables multiple-bands RRU to use fewer power amplifers in order to reduce size and cost of the multi-band RRU. The present invention is based on the method of using duplexers and/or interference cancellation system technique to increase the isolation between the transmitter signal and receiver signal of the RRU.

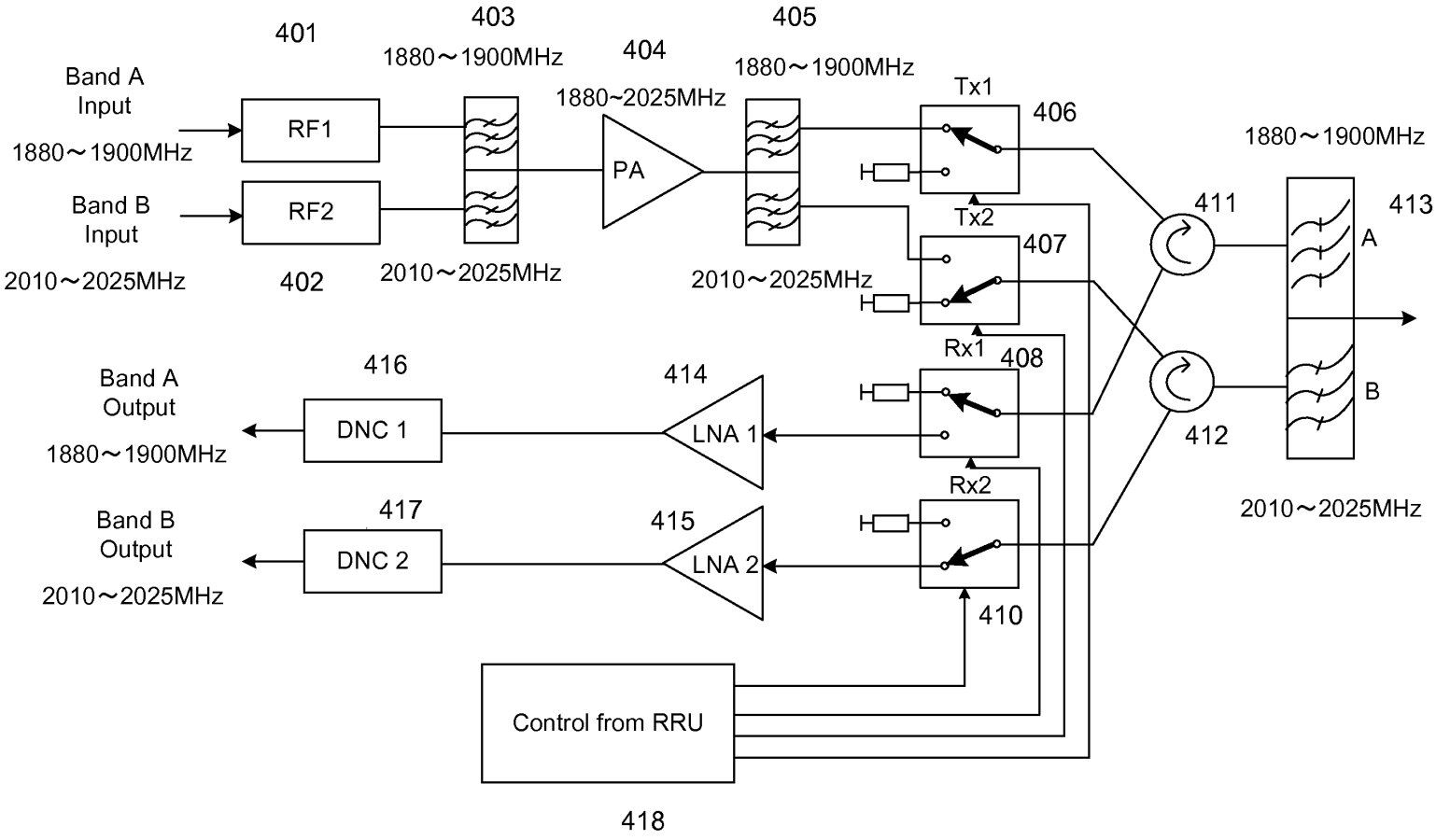


Figure 1: Dual Band TD-SCDMA RRU

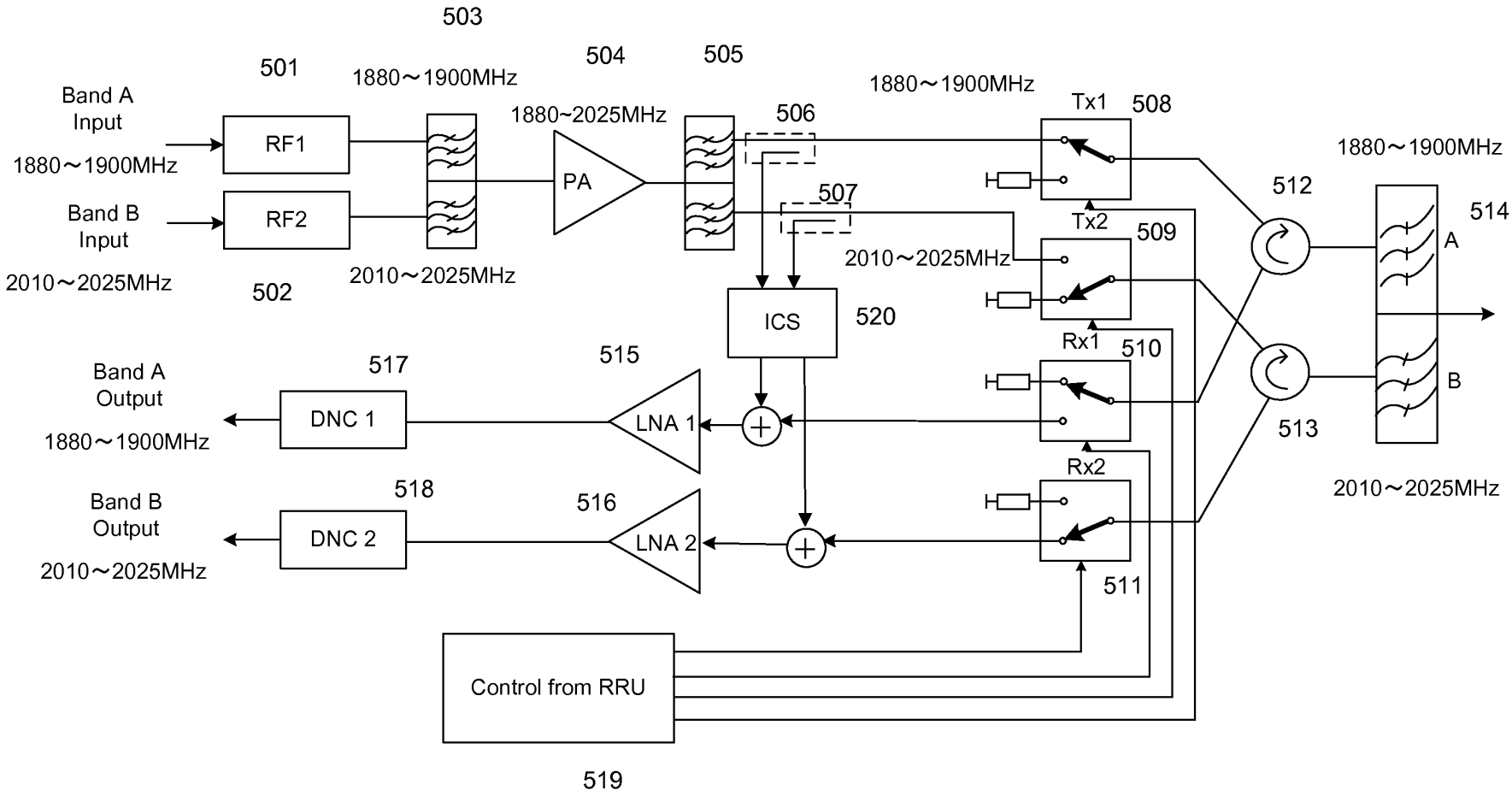


Figure 2: Dual Band TD-SCDMA RRU with Interference Cancellation System

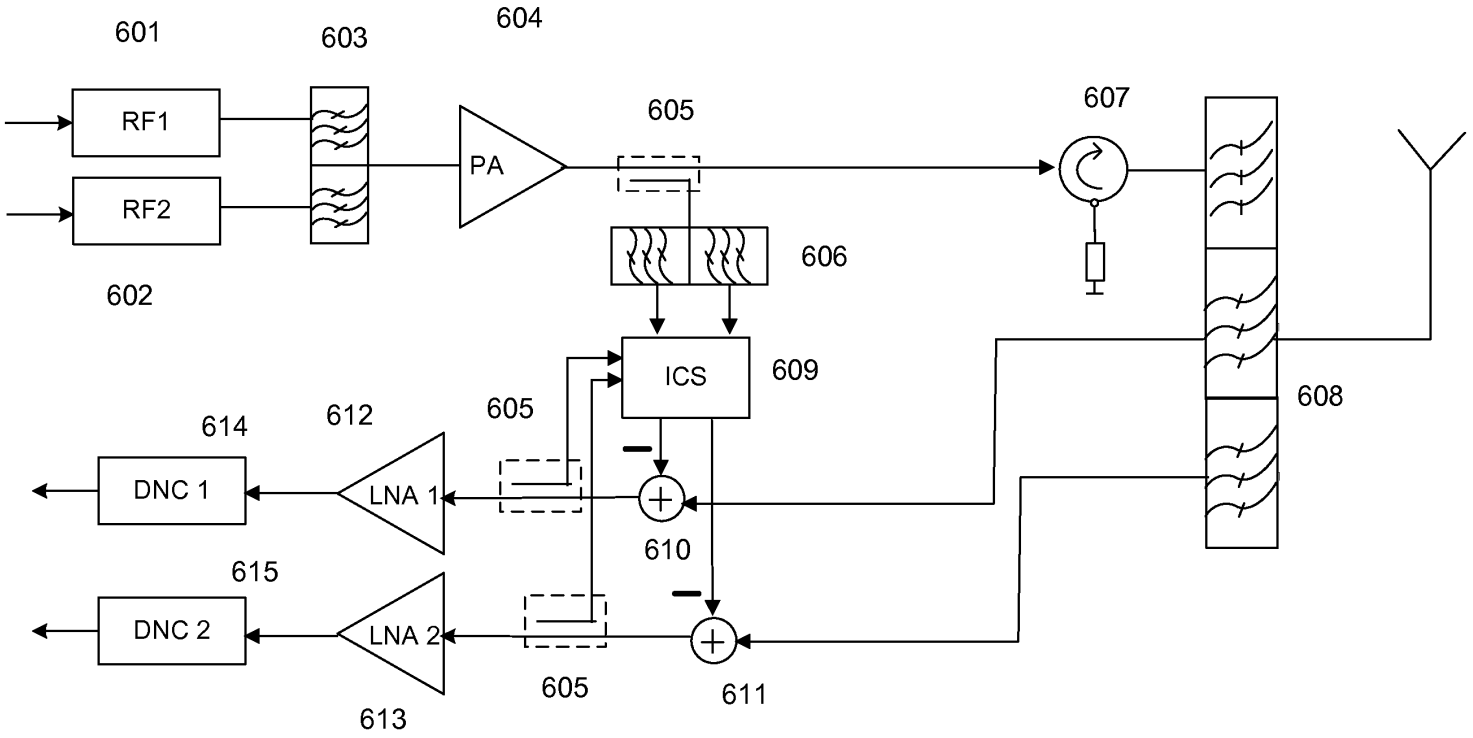


Figure 3: FDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

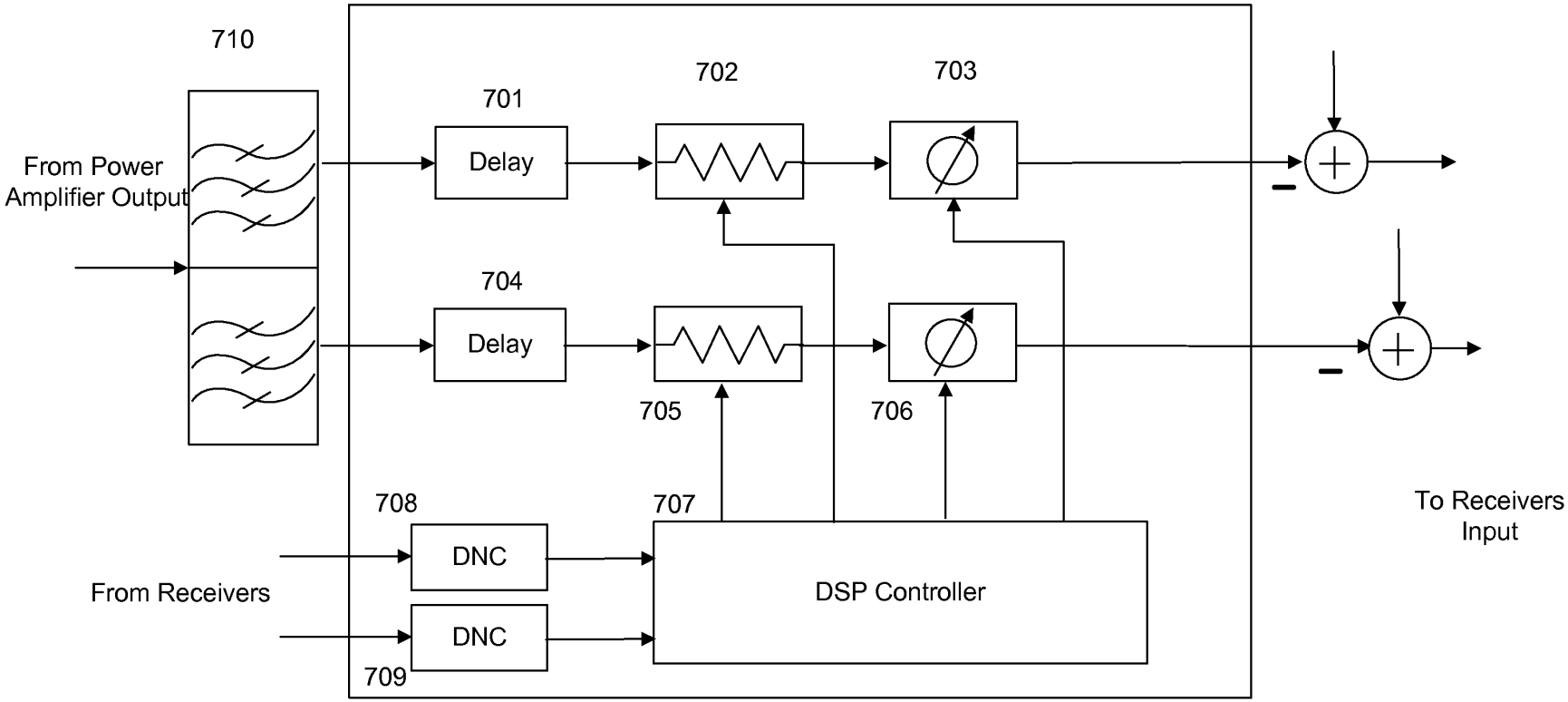


Figure 4: Dual-Band Interference Cancellation System using power detection

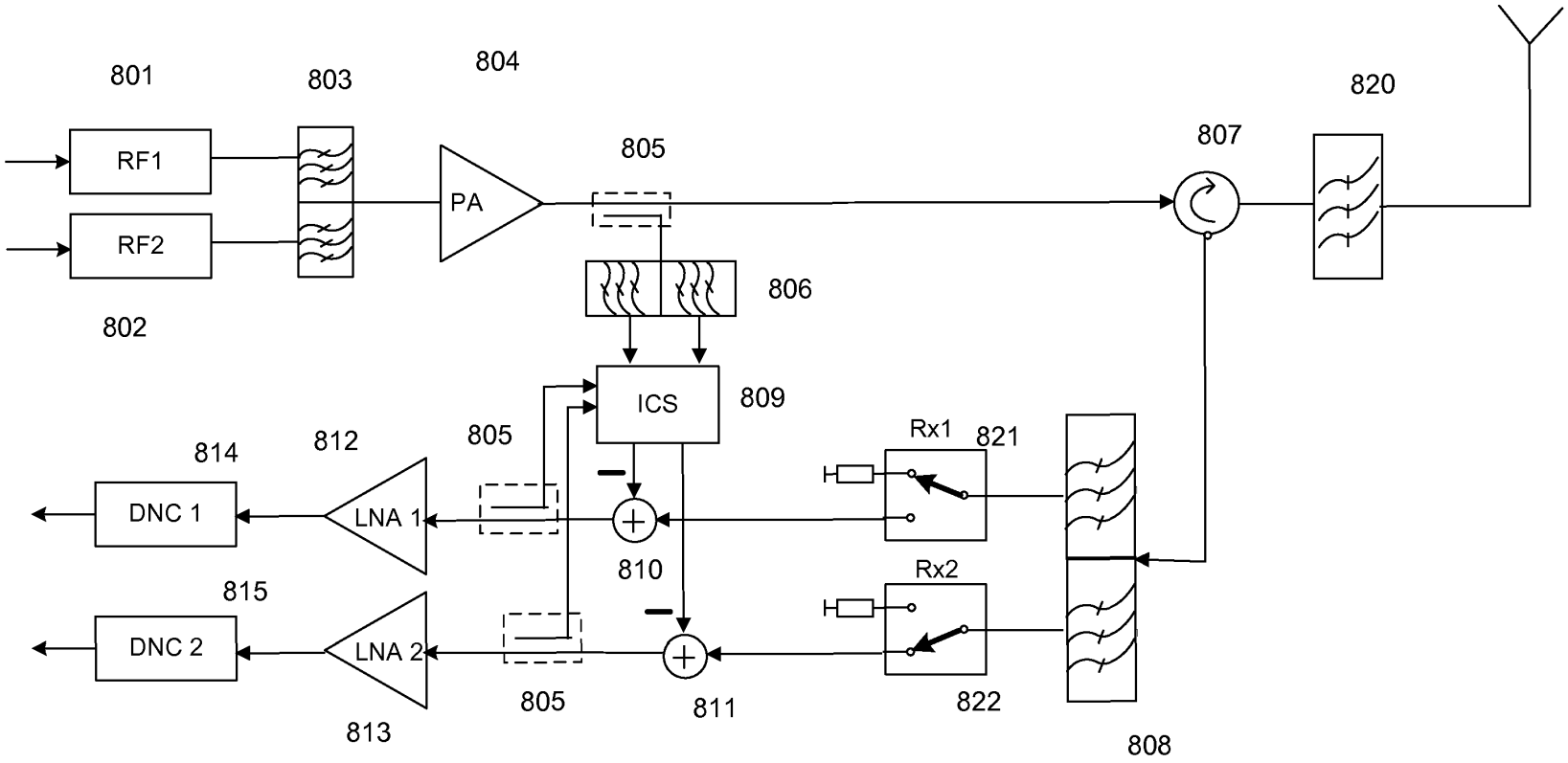


Figure 5: TDD Modulation Agnostic Dual Band RRU with Interference Cancellation System

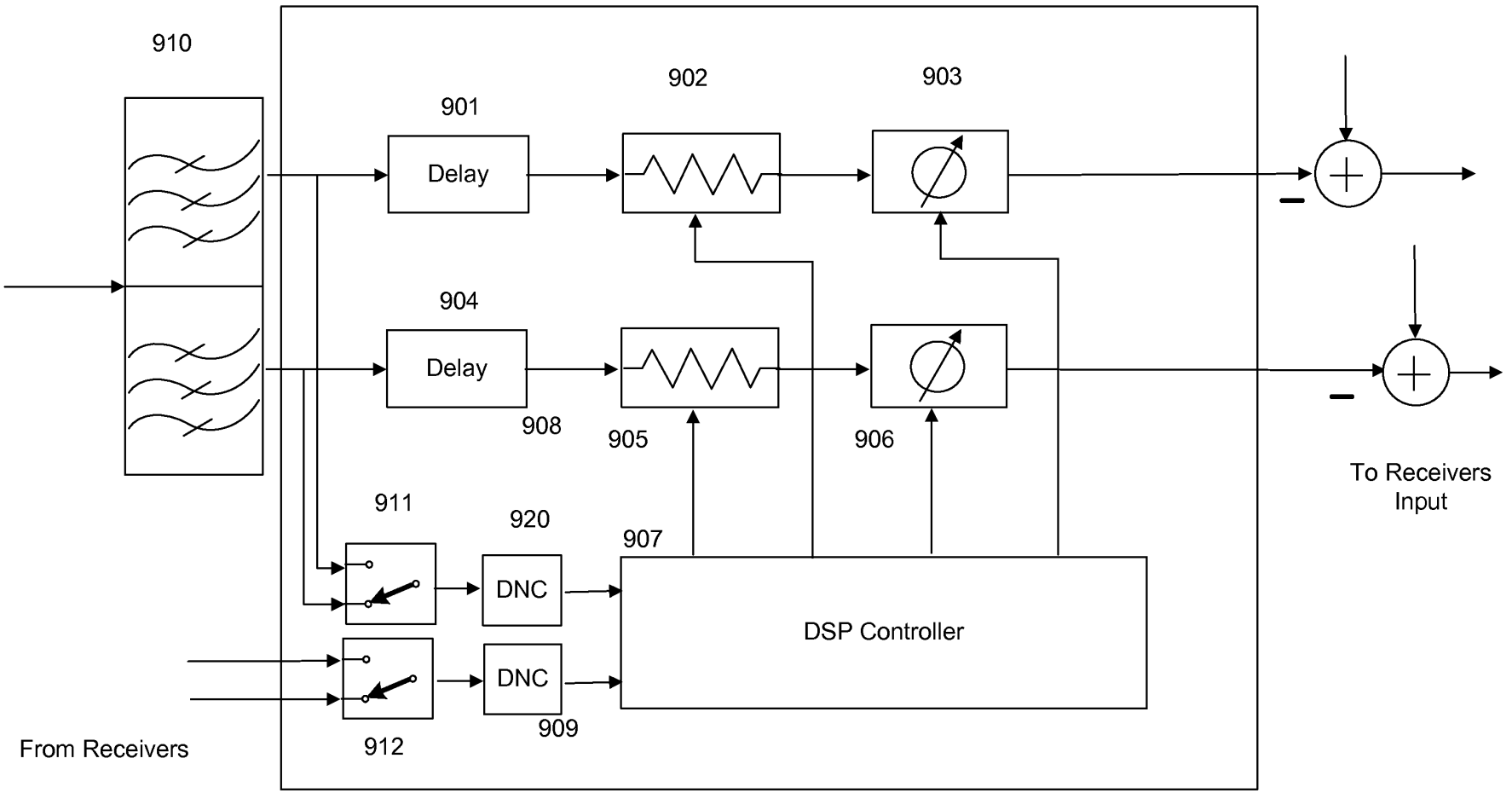


Figure 6: Dual-Band Interference Cancellation System using Correlation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

FOR

UNITED STATES PATENT

FOR

ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD

INVENTORS

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Ying Xiao, Citizen of Canada

SPECIFICATION

RELATED APPLICATIONS

[001] This application claims the benefit of the following applications:

[002] US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

[003] US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

[004] US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

[005] US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

[006] US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

[007] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1018, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

[008] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1019, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

[0009] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1020, entitled ADVANCED DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

[0010] US Patent Application S.N. _____, filed 12/21/2009, attorney's docket DW-1021, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

[0011] All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[0012] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[0013] A wideband mobile communication system using complex modulation techniques, such as wideband code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. The conventional feedforward linear power amplifier (FFLPA) has been widely utilized due to its excellent linearity performance in spite of poor power efficiency.

[0014] Conventional FFLPAs are mainly based on the principle of error subtraction and power-matching with dedicated hardware circuitries to realize non-linear corrections to PA. These approaches must use an auxiliary PA and complicated hardware circuitries to match exactly the transmitted power-balance, time-delay and errors generated by the main PA. After a perfect matching is obtained, the non-linear distortion errors from the main PA can then be canceled by those distortion errors from the auxiliary PA. Due to the complexities of the nonlinear predistortion circuits, which among other things involve many variables and parameters, FFLPAs require significant fine tuning and other calibration efforts. In addition, such traditional FFLPA schemes are also vulnerable to fluctuating environmental conditions, such as temperature and humidity changes, since perfect alignment of the main PA's signal and that of the auxiliary PA are vital. As a result, traditional predistortion schemes are costly to implement and are limited in their predistortion accuracy and stability in a commercial wireless system environment.

[0015] In order to overcome the FFLPA's poor efficiency, digital baseband predistortion (PD) has been demonstrated due to the recent advances in digital signal processing (DSP) technology. In addition, Doherty power amplifiers (DPA) have also been applied to these linearization systems to improve power efficiency. However, there is still a demand for higher performance of the power amplifier such as more linearity and better efficiency with less expensive architecture.

[0016] Conventional DSP-based PD schemes utilize digital microprocessors to compute, calculate and correct the PA's nonlinearities, typically by performing fast tracking and adjustments of signals in the PA system. However, conventional DSP-based PD schemes are challenged by

variations of the linearity performance of the amplifier due to changes in the environment such as temperature and the asymmetric distortions of the output signal of the PA resulting from memory effects. All of these variations and distortions have to be compensated for. Conventional PD algorithms are based on a wideband feedback signal, and require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. In addition, time-synchronizations are typically required to capture an error signal between a reference signal and a distorted signal. This time-matching process may result in small synchronization errors which can further affect conventional PD schemes' linearization performance. Amplitude and phase synchronization is also required in order to align the reference signal and the distorted signal.

[0017] Moreover, conventional PD schemes necessitate coded in-phase (I) and quadrature (Q) channel signals in the baseband as the required ideal or reference signals. As a result, conventional PD schemes are often standard or modulation specific and must be closely tailored to each baseband system. Therefore, in order to deploy conventional PD schemes into base-stations, the PD engines must be embedded into the baseband architecture of base-stations. This embedment is a practical implementation challenge since it is frequently inconvenient or impossible to modify the baseband architectures of existing base-stations or base-station designs. Once the PD scheme is set up for a specific base-station design, it is often not reconfigurable and hence not upgradeable to future changes in standards or modulations. Furthermore, since traditional PD approaches require baseband I-Q signal sources to operate, they are inapplicable to certain RF systems that

do not possess any baseband I-Q signal sources, such as repeater and indoor signal coverage sub-systems.

SUMMARY OF THE INVENTION

[0018] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for wideband communication system applications. The present disclosure provides a field-reconfigurable power amplifier system that supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. In multi-channel configurations of the present invention there can be more than one PA for multiple bands.

[0019] To achieve the above objects, the present invention is generally based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[0020] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[0021] Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

[0022] A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are sampled in a feedback path and controlled by the adaptation algorithm in a digital module. Therefore, in an embodiment, the present invention is capable of compensating for the nonlinearities as well as memory effects of power amplifier systems and also improves performance, in terms of power added efficiency, adjacent channel leakage ratio (ACLR) and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

THE FIGURES

[0023] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0024] Figure 1 is a block diagram showing the basic form of a digital hybrid mode power amplifier system.

[0025] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0026] Figure 3 is a block diagram showing polynomial-based predistortion in a digital hybrid mode power amplifier system of the present invention.

[0027] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a digital hybrid mode power amplifier system of the present invention.

[0028] Figure 5 is a delay estimation block diagram of the present invention.

[0029] Figure 6 is a block diagram of a fractional delay for the present invention.

[0030] Figure 7 is a block diagram showing a digital hybrid mode power amplifier system implemented with a down converter (DNC) and UPC-based clipping error restoration path according to another embodiment of the present invention..

[0031] Figure 8 is a block diagram showing a digital hybrid mode power amplifier system implemented with a DNC and an analog quadrature modulator (AQM) according to another embodiment of the present invention.

Figure 9 is a block diagram showing an embodiment of the analog quadrature modulator compensation structure.

GLOSSARY

The acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter

EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access

WLAN Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0032] The present invention is a novel RF-out PA system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[0033] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention is a “black box”, plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a digital hybrid mode power amplifier (DHMPA) system hereinafter.

Digital Predistorter Algorithm

Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows in block diagram form an embodiment of a linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3), and complies with the formula:

$$z(n) = \sum_{i=0}^{n-1} x_t(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_t(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients a_{ij}, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4.

[0034] FIG 3. is a block diagram showing a predistortion (PD) part in the DHMPA system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 and in embodiments disclosed in FIG. 7 and FIG. 8, discussed below, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the DHMPA system in FIG. 3 has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

Delay Estimation Algorithm:

The DPD estimator compares $x(n)$ and its corresponding feedback signal $y(n-\Delta d)$ to find the DPD coefficients, where Δd is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, $x(n)$, and feedback data, $y(n)$, is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign(y(i+m+1) - y(i+m))$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $C(m)$ is the feedback path delay. The delay estimation block is shown in Figure 5.

Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is necessary. To simplify the design, only a half-sample delay is considered in this design, as shown in Figure 6. Although smaller fractional delays can be utilized.

To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel. The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

In which c_i is the weight coefficient.

Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

Phase offset Estimation and Correction Algorithm:

Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

The transmission signal $x(n)$ and feedback signal $y(n)$ can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x - \theta_y)}$ can be calculated through

$$e^{j(\theta_x - \theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{j\theta o,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{j\theta o}$$

Magnitude correction:

As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

In this design, N is chosen to be 4096. The choice of N will depend on the desired accuracy.

QR_RLS Adaptive Algorithm:

The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F\big(x(n)\big) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^{j}$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\gamma^{\frac{1}{2}}(i) \\ h_i \Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = k_a k_b / k_a'$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2}q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_1^{1/2}} & 0 \\ \overline{q_1^*} & \overline{e_a^*(1)\gamma^{\frac{1}{2}}(1)} \\ \overline{h_1 \Phi_1^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(1)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{\frac{*}{2}}}[w_i - \bar{w}] = \overline{q_1}$$

In the iterative process, a block of data (in this design, there are 4096 data in one block) is stored in memory, and the algorithm uses all the data in

memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data is processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

To make sure the stable performance of DPD, a weighting factor f is used when updating the DPD coefficients as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

[0035] Figures 7 and 8 are block diagrams showing more sophisticated embodiments of DHMPA system, where like elements are indicated with like numerals and elements not numbered in Figure 8 have the same reference numerals as shown in Figure 7. The embodiments of Figures 7and 8 apply crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is

included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0036] Figure 7 is a block diagram showing a DHMPA system implemented with DQM in accordance with an embodiment of the present invention (the "FIG. 7. System"). The system shown in Figure 7 has a dual mode of RF-in 700 and/or multi-carrier digital signal 705 at the input, and an RF signal at the output 710. The dual mode of signal input allows maximum flexibility: RF-in (the "RF-in Mode") or baseband digital-in (the "Baseband-in Mode"). The FIG. 7. System comprises three key portions: a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 715, a power amplifier module 760 and a feedback path 725.

[0037] The FPGA-based Digital part comprises a digital processor 715 (e.g. FPGA), digital-to-analog converters 735 (DACs), analog-to-digital converters 740 (ADCs), and a phase-locked loop (PLL) 745. Since the FIG. 7 System has a dual input mode, the digital processor has two paths of signal processing. For the RF signal input path, the digital processor has implemented a digital quadrature demodulator (DQDM), a CFR, a PD, and a digital quadrature modulator (DQM). For the baseband digital input path, a digital up-converter (DUC), CFR, PD, and a DQM are implemented.

[0038] The RF-in Mode of the FIG. 7. System has implemented a down converter (DNC) 750 prior to the FPGA-based Digital part and an ADC 740 prior to the FPGA. An analog down converted signal is provided to the FPGA-based Digital module and converted to a digital signal by the ADC 740. The digitally converted signal is demodulated by the DQDM to generate both real and imaginary signals and then PAPR of the signal is reduced by CFR. The peak reduced signal is predistorted to linearize the amplifier and is

passed through a DQM to generate the real signal and then converted to an intermediate frequency (IF) analog signal by a DAC in the FPGA-based Digital part. However, it is not required in all embodiments to implement DQDM and DQM in the FPGA. If, as shown in Figures 7 and 8, a digital modulator will not be used, then two DAC's 801 behind the FPGA feeding AQM module 800 can be used to generate real and imaginary signals, respectively (the "AQM Implementation").

[0039] The Baseband-in Mode of FIG. 7. works slightly different from the RF-in Mode. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. From this point onwards, the Baseband-in Mode and RF-in Mode proceeds identically. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0040] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a synchronizing the wideband captured output signal from the feedback path 725 with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. . The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DAC 740 as shown. As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. Alternatively, if the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to

generate real and imaginary signals, respectively. The gate bias voltage 753 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 535 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. .

[0041] The power amplifier part comprises a UPC for a real signal (such as illustrated in the embodiment shown in Figures 7), or an AQM for real and complex signals (such as the embodiment of a DHMPA system depicted in Figure 8) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental DHMPA system. One such Doherty power amplifier technique is presented in commonly assigned U.S. Provisional Patent Application S.N. 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference, together with U.S. Patent Application S.N. 12/603,419, filed 10/21/2009, entitled N-Way Doherty Distributed Power Amplifier with Power Tracking. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0042] The feedback portion comprises a directional coupler, a mixer, a gain amplifier, a band pass filter (BPF), and a Digital to Analog Converter (DAC). Depending upon the embodiment, these analog components can be

mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the the gain amplifier, and the BPF (e.g., surface acoustic wave filter) which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the digital PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the detector 580 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, discussed above, which shows a polynomial-based predistortion algorithm and from Figure 4, also discussed above, which shows the block diagram of the digital predistorter synchronization algorithm which can be used in some embodiments of the invention.

[0043] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 790, hence maximizing the DHMPA system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC 735 in the FPGA-

based Digital portion and an extra UPC 720 in the power amplifier part (see FIG. 7. & 8.). The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier. Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0044] Referring again to Figure 7, the RF input signal is first down-converted to baseband digital signals, and then digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz). If the system of Figure 7 has a Baseband-in Mode, then the digital data streams from multi-channels are digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz) directly as they enter the digital processor. The CFR then reduces the PAPR. The peak-reduced signal is predistorted to linearize the DPA and is passing through two DACs for real and imaginary signals and finally through an AQM.

[0045] FIG. 9. is a block diagram showing an embodiment of the analog quadrature modulator compensation structure. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12, g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2. The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals Y_I and Y_Q will be presented to the AQM's in-phase and quadrature ports.

[0046] The configuration of the power amplifier part and the feedback part of the system shown in FIG. 8 are the same as for the system shown in FIG. 7.

[0047] In FIG. 8 System, the DNC frequency translates the RF signal into a low IF signal. The IF signal is then presented to the ADC whereupon it is digitally down-converted to baseband followed by CFR and predistortion (PD). The output of the PD is a baseband signal which will then be digitally upconverted to an IF frequency and presented to the DAC. The output of the DAC is then further frequency translated to a RF frequency through the up-converter (UPC.) The configuration of the power amplifier part and the feedback part of FIG. 8 System are the same as for the FIG. 7 System.

[0048] In summary, the DHMPA system of the present invention enhances efficiency and linearity relative to the prior art since the DHMPA system is able to implement CFR, DPD and adaptation algorithms in one digital processor, which consequently saves hardware resources and processing time. The DHMPA system is also reconfigurable and field-programmable since the algorithms and power-efficiency-enhancing features can be adjusted like software in the digital processor at anytime.

[0049] Furthermore, since the DHMPA system accepts RF modulated signal as input, it is not necessary to use coded I and Q channel signals in the baseband. Therefore, the performance of wireless base-station systems can be enhanced simply by replacing the existing PA modules with the DHMPA. The result is that the present invention provides a “plug and play” PA system solution such that the structure of existing base-station systems does not

need to be modified or rebuilt for a new set of signal channels in order to benefit from high efficiency and high linearity PA system performance.

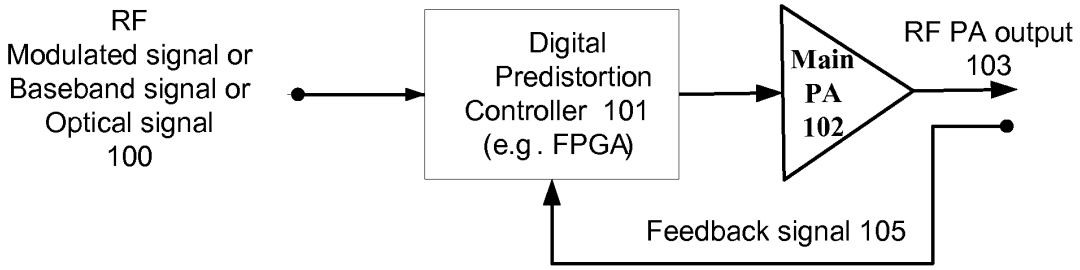
[0050] Moreover, the DHMPA system is agnostic to modulation schemes such as quadrature phase shift keying (QPSK), quadrature amplitude modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM), etc. in code division multiple access (CDMA), global system for wireless communications (GSM), WCDMA, CDMA2000, and wireless LAN systems. This means that the DHMPA system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DHMPA system of the present invention include correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0051] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

ABSTRACT

A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

FIG. 1. Basic Digital Hybrid Mode Power Amplifier System



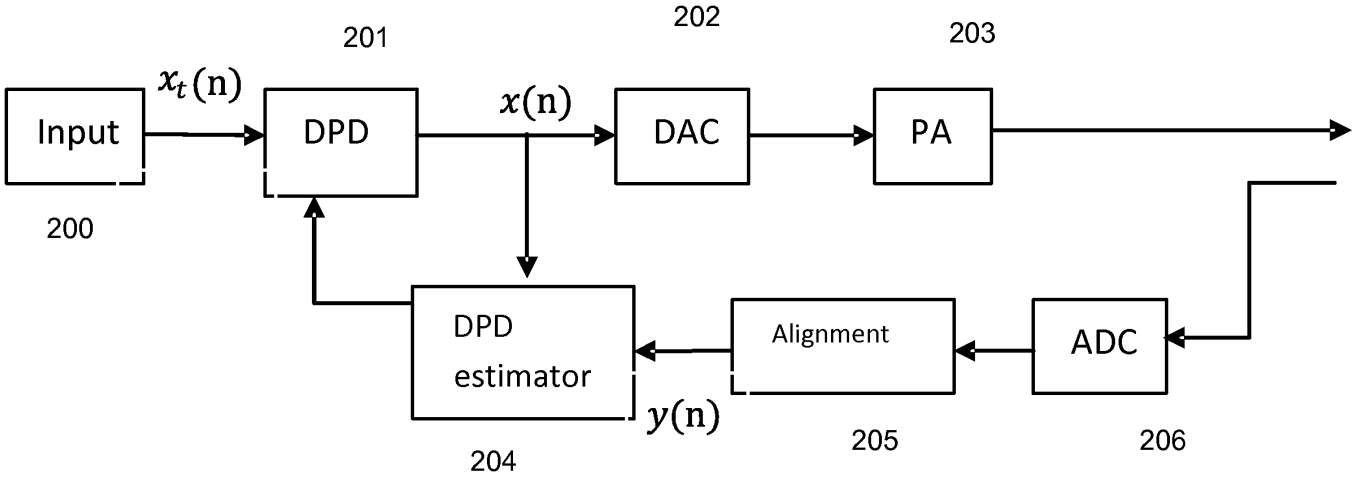


FIG. 2. Digital Predistortion Block Diagram

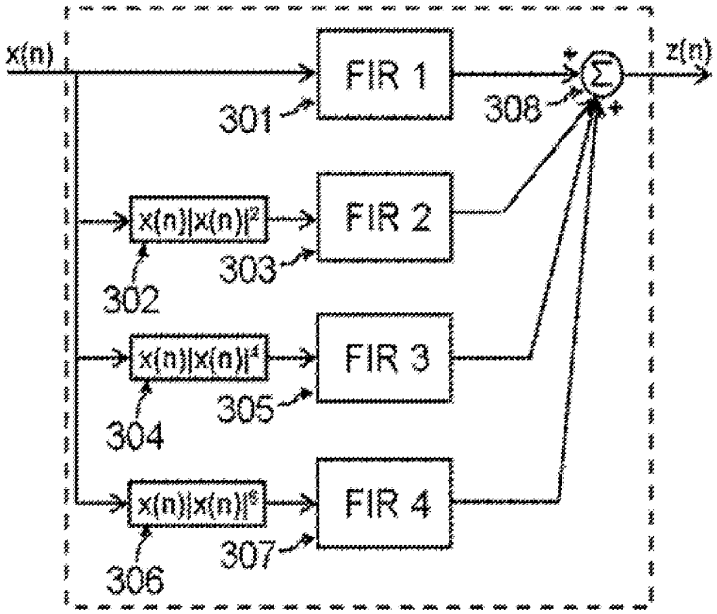


FIG. 3. Polynomial based PD in an embodiment of Digital Hybrid Mode Predistortion PA System

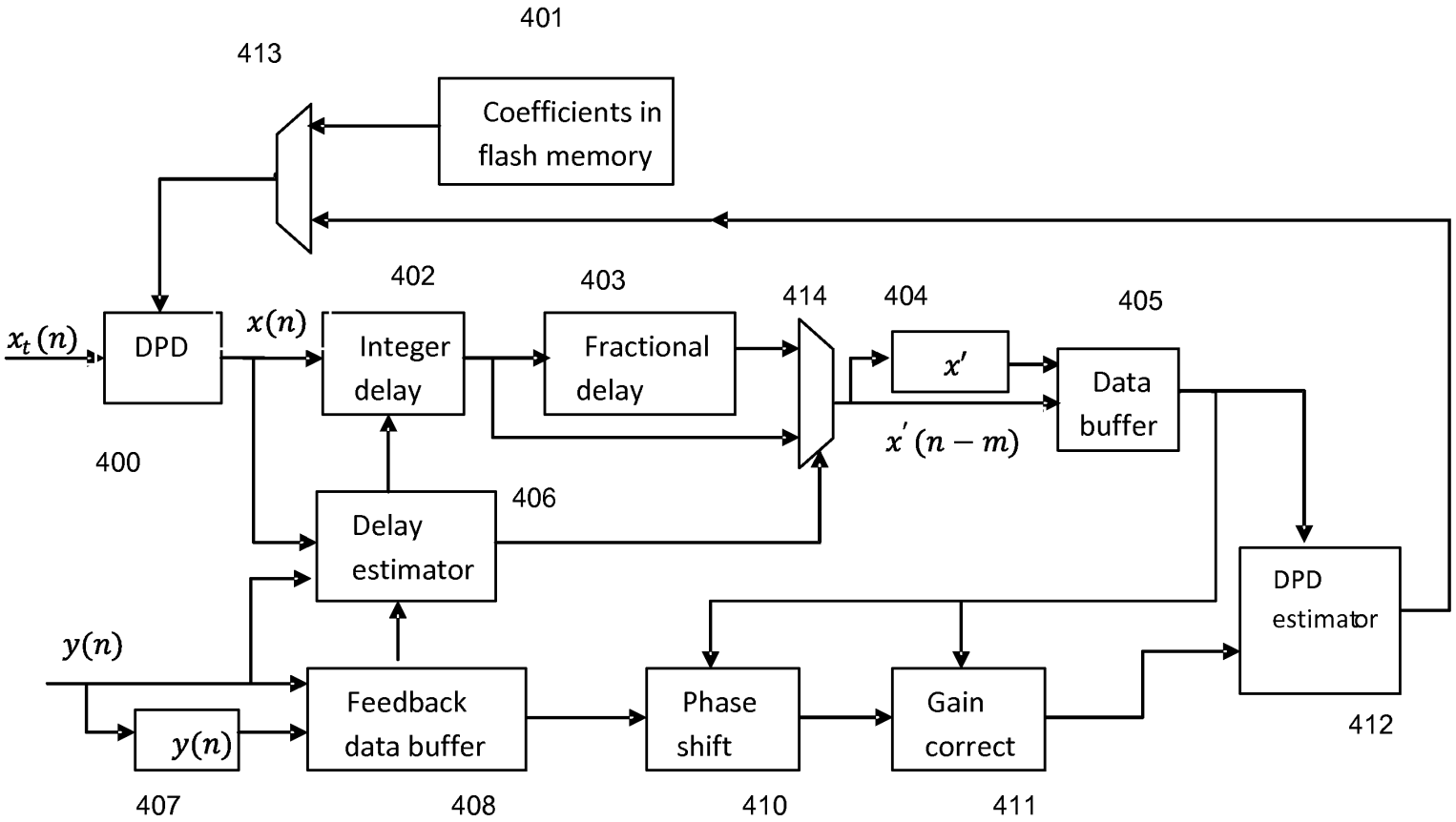


FIG. 4. Digital Predistortion Algorithm

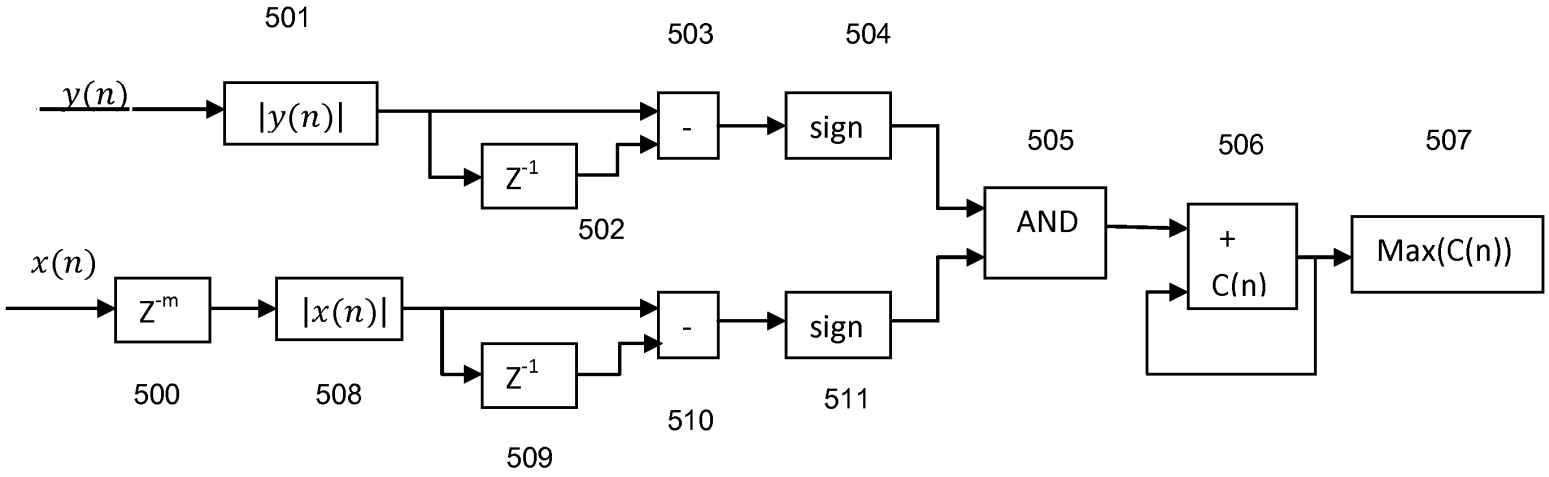


FIG. 5. Delay Estimation Block

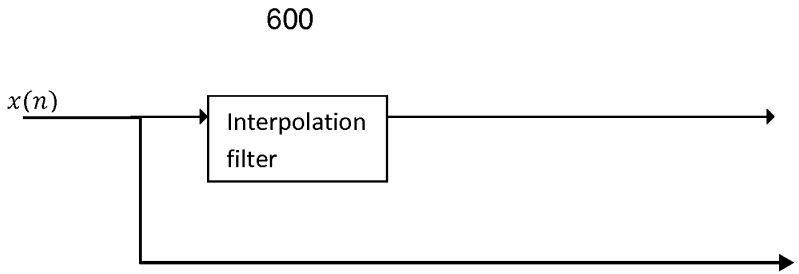


Figure 6 Fractional Delay Block

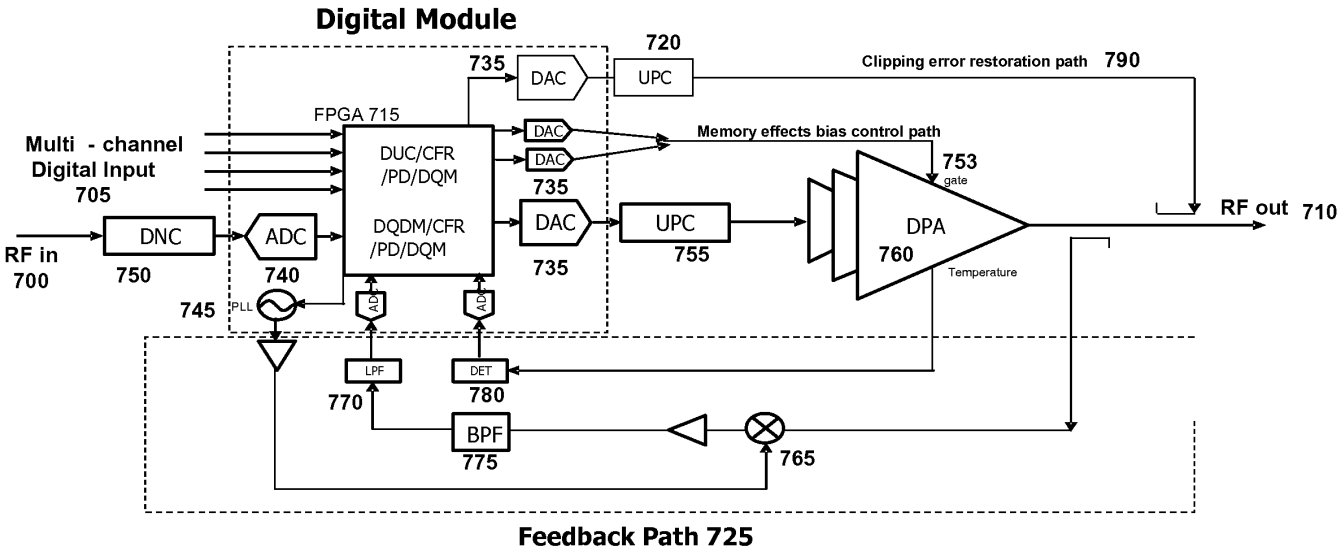


FIG. 7. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input

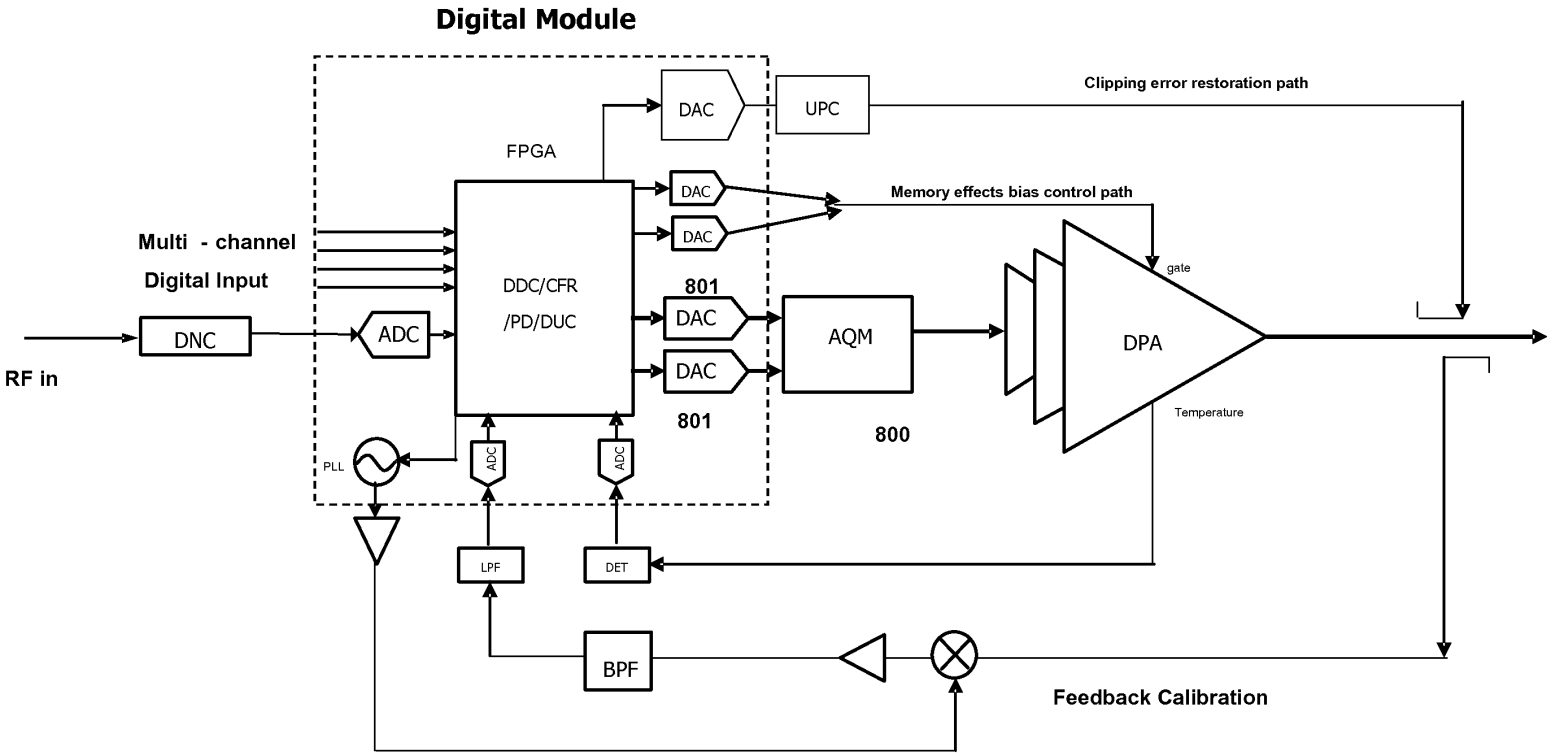


FIG. 8. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input, with Feedback Calibration

Figure 9 Analog Quadrature Modulator Compensation Block

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	Application Number	
Title of Invention	Daisy Chained Ring of Remote Units for A Distributed Antenna System	

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Title of the Invention	Daisy Chained Ring of Remote Units for A Distributed Antenna System		
Attorney Docket Number	DW-1024P	**Small Entity Status Claimed**	☒
Application Type	Provisional		
Subject Matter			
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

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	Application Number	
Title of Invention	Daisy Chained Ring of Remote Units for A Distributed Antenna System	

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Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

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Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
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City	George Town Grand Cayman	**State/Province**	
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Title of Invention	Daisy Chained Ring of Remote Units for A Distributed Antenna System	

Signature	/James E. Eakin/			Date (YYYY-MM-DD)	2011-02-04
First Name	James E.	Last Name	Eakin	Registration Number	27874

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Daisy Chained Ring of Remote Units for a Distributed Antenna System
First Named Inventor/Applicant Name:	Shawn Patrick Stapleton
Filer:	James E. Eakin
Attorney Docket Number:	DW-1024P

Filed as Small Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional Application filing fee	2005	1	110	110
Pages:				
Provis. Appl Size fee per 50 sheets >100	2085	4	135	540
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**650**

Electronic Acknowledgement Receipt	
EFS ID:	9384238
Application Number:	61439940
International Application Number:	
Confirmation Number:	5356
Title of Invention:	Daisy Chained Ring of Remote Units for a Distributed Antenna System
First Named Inventor/Applicant Name:	Shawn Patrick Stapleton
Customer Number:	54412
Filer:	James E. Eakin
Filer Authorized By:	
Attorney Docket Number:	DW-1024P
Receipt Date:	07-FEB-2011
Filing Date:	
Time Stamp:	03:53:46
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$650
RAM confirmation Number	7151
Deposit Account	503576
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	**Document Description**	**File Name**	**File Size(Bytes)/ Message Digest**	**Multi Part /.zip**	**Pages (if appl.)**
1	Specification	DW1024P_Ring_Network_of_Daisy_Chained_DAS_jee_final.pdf	189577 8f5a51b35dbce1b5da62200b363f35e626049391	no	31
Warnings:					
Information:					
2	Drawings-only black and white line drawings	1024P_Figures_1_8_final.pdf	217354 6cd0883a7099a523b6fd3fb1ad90e7b26811cf20	no	8
Warnings:					
Information:					
3	Appendix to the Specification	Appendix_A_USSN_61382836.pdf	4766729 b80338d22ed357a395b88d7b52d1bf32348390f3	no	176
Warnings:					
Information:					
4	Appendix to the Specification	Appendix_B_USSN_61374593.pdf	3809164 9be4b0e1194a78044ee8ba7667ee470f47d8a82b	no	141
Warnings:					
Information:					
5	Application Data Sheet	Application_Data_Sheet.pdf	1031529 52df16d16d57f5b9c18257085c315a5a80c3da65	no	5
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	31245 5ea700bf3ebfe0d93e3a5c7875102a856aee0a85	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	10045598		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/439,940	02/07/2011		650	DW-1024P		

CONFIRMATION NO. 5356

54412
Law Offices of James E. Eakin
P.O. Box 1250
Menlo Park, CA 94026

FILING RECEIPT

OC000000046262614

Date Mailed: 03/04/2011

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Shawn Patrick STAPLETON, Burnaby, CANADA;
Paul LEMSON, Woodinville, WA;
Bin LIN, Burnaby, CANADA;

Power of Attorney:
James Eakin--27874

If Required, Foreign Filing License Granted: 02/28/2011
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/439,940**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
** **SMALL ENTITY** **
Title

Daisy Chained Ring of Remote Units for A Distributed Antenna System

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing

of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of

State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PTO/AIA/80 (07-17)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 167137

OR

[ ] Practitioner(s) named below (If more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 167137

OR

[ ]

Firm or individual name		
Address		
City	State	Zip
Country		
Telephone	Email	

Assignee name and address: Dali Wireless, Inc.
535 Middlefield Road
Menlo Park, CA 94025

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature	Date December 13, 2019
Name Albert Lee, Ph.D.	Telephone
Title Founder, Chairman and Chief Executive Officer	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	38533335
Application Number:	61439940
International Application Number:	
Confirmation Number:	5356
Title of Invention:	Daisy Chained Ring of Remote Units for A Distributed Antenna System
First Named Inventor/Applicant Name:	Shawn Patrick STAPLETON
Customer Number:	54412
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	DW-1024P
Receipt Date:	09-FEB-2020
Filing Date:	07-FEB-2011
Time Stamp:	13:10:54
Application Type:	Provisional

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Statement_Under_373c_w_POA_10333-22-PROV.pdf	1630305 f8f12cf1c76e167684093a2d93a8f138d30d1dbd	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73	1	2
	Power of Attorney	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	1630305	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: DALI WIRELESS, INC.

Application No./Patent No.: 61/439,940 Filed/Issue Date: February 7, 2011

Titled: Daisy Chained Ring of Remote Units for A Distributed Antenna System

DALI WIRELESS, INC., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Shawn Patrick Stapleton, Paul Lemson, Bin Lin To: DALI SYSTEMS CO. LTD.

   The document was recorded in the United States Patent and Trademark Office at Reel 026177, Frame 0495, or for which a copy thereof is attached.

2. From: DALI SYSTEMS CO. LTD. To: DALI WIRELESS, INC.

   The document was recorded in the United States Patent and Trademark Office at Reel 045126, Frame 0677, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jason H. Vick/	February 9, 2020
Signature	Date
Jason H. Vick	45,285
Printed or Typed Name	Title or Registration Number

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
61/439,940	02/07/2011	Shawn Patrick STAPLETON	DW-1024P

CONFIRMATION NO. 5356

167137
SHERIDAN ROSS PC
1560 Broadway
Suite 1200
Denver, CO 80202

POA ACCEPTANCE LETTER

OC000000114641433

Date Mailed: 02/12/2020

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/09/2020.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cnguyen/