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Title: System & Method for Performing Broadband Transmission over an optical Network

☒ Specification, sheets: 10 ☒ Drawing(s), sheets: 7

☒ Check or Credit Card Payment (use PTO-2038) for \$ 80.00 for ☒ small entity
☐ large entity filing fee

☒ Return Receipt Postcard Addressed to Inventor # 1.

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Form 3-5: Provisional Patent Application

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

(\$)

Complete if Known

Application Number

Filing Date

First Named Inventor

Examiner Name

Art Unit

Attorney Docket No.

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number
Deposit Account Name

The Commissioner is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	80
SUBTOTAL (1)				(\$)	80.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent Claims	-20** =	X	
Multiple Dependent	-3** =	X	

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

(\$)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$)

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6/21/03

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SYSTEM AND METHOD FOR PERFORMING BROADBAND TRANSMISSION OVER AN OPTICAL NETWORK

FIELD OF THE INVENTION

- 5 [0001] The present invention relates to optical fiber communications generally, and more specifically to a system and method for performing broadband transmission rates over an optical network.

BACKGROUND OF THE INVENTION

- 10 [0002] In Datacom, Telecom and Storage Access Network (SAN) applications that operate at very high data rates of 10Gbps and higher have consistently attracted hundreds of millions of research and development investment dollars to improve the overall port density provided by system vendor solutions. These improvements in port density have primarily been obtained through power and thermal improvements of a
15 given physical layer implementation by eliminating MUX/DEMUX functions, reducing pin count and increasing the serial interface data rate of the optical module. Since Service Provider's business case demands that System Vendor's cost and performance efficiencies continue to exceed previous generation designs and implementation capabilities, System Vendors are forced to explore new methods for reducing power
20 while enabling higher levels of system-on-a-chip integration, versatility and reducing thermal characteristics. Other issues like Electro Magnetic Interference (EMI) that is generated by these new platforms are a constant ongoing challenge to system vendors and component suppliers.

- [0003] In an effort to standardize, harmonize and set aggressive cost, power, area
25 and performance goals the industry, System Vendors have sponsored and supported Multi-Source Agreements (MSA) between several component suppliers that define and specify all the physical and electrical requirements for optical transponders and transceivers. For example, over the past few years both the Datacom and Telecom industries have seen a race toward smaller and lower power optical 10Gbps platforms.
30 Component vendors started with an initial IEEE driven 300-pin specification that specified sixteen 622Mbps electrical interfaces. Component manufacturers continued the

race with two MSAs called X2 and XPAK both of which specified four 3.125Gbps channels on the electrical interface side (also known as media attachment layer). A competing Xenpak MSA that was physically smaller while maintaining the same pin count and four serial 3.125Gbps channel interface followed this. And now the latest and most advanced 10Gbps optical transceiver MSA based on a 10Gbps XFI serial interface called the XFP MSA and only consumes 30-pins. This rush of investment, development and improvement in the industry, during an industry wide market slowdown, is a large indicator of the importance System Vendors and Service Providers place on port density and the impact greater density has on business cases for Datacom, Telecom and SAN markets. Some estimates are that the industry will save close to a billion dollars of additional capital expenditures over the next 3 years due mainly to the per port power and area density improvements stemming from the XFP MSA for each Line card deployed.

[0004] There are practical system chip-to-chip interface design challenges at the PHY layer however with the XFP due to the 10Gbps serial interface data rate which cause component PHY manufactures to incur a greater amount of investment CMOS fab processes due to the 10GHz serial data rate circuit requirements. And since these new processes suffer from high leakage current and other production reliability issues, the proliferation of the XFP may stall and cause significant delay in the deployment of new high density 10Gbps line cards. In addition, direct modulation of 10Gbps data rates cause significant restrictions on the reach for a given implementation over all types of fiber. Addressing these practical constraints that plagues all high-speed PHY and PMD implementations while enabling more performance, functionality and data rate flexibility from a single optical transceiver and PHY subsystem is a tremendous value to Component Suppliers, System Vendors and Service Providers.

[0005] This invention solves these practical PHY & PMD constraints for 10Gbps and higher data rate applications and enables extremely high-density solutions equivalent to those found at 1Gbps and below. Remarkable improvements in system power consumption, thermal performance and reach along with system interface simplifications that address practical chip-to-chip interface designs and EMI issues are enabled via this invention. From a Service Provider, System Vendor or Component Supplier perspective, this invention will profoundly improve the overall financial and service offerings that

bound every business case in the Telecom, Datacom and SAN markets and has the potential of revolutionizing point-to-multipoint deployments.

SUMMARY OF THE INVENTION

5 [0006] A system and method for performing broadband transmission rates over an optical network using a plurality of fibers, m-ary modulation, channel equalization, coding, forward error correction and a plurality of bi-directional optical sub-assemblies within a single optical transceivers.

BRIEF DESCRIPTION OF THE DRAWINGS

10

[0007] FIG. 1 is a block diagram of a combined Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS) device according to an exemplary embodiment of the invention.

[0008] FIG. 2 is a block diagram of a Physical Medium Dependent (PMD) device
15 according to an exemplary embodiment of the invention.

[0009] FIG. 3 is a block diagram of a combined PMA/PCS and PMD device called a PHY according to an embodiment of the invention.

[0010] FIG. 4 is a block diagram of a Passive Optical Network (PON) utilizing the PHY according to an embodiment of the invention.

20 [0011] FIG. 5 is a block diagram of an example PMA/PCS device according to an exemplary embodiment of the invention.

[0012] FIG. 6 is a block diagram of an example PMD device according to an exemplary embodiment of the invention.

[0013] FIG. 7 is a block diagram of an example PHY device according to an
25 exemplary embodiment of the invention.

DETAILED DESCRIPTION

[0014] The invention involves a complex design of digital, analog and optical components in two primary parts. One part called a PMA/PCS and the other PMD in the
30 vernacular of I.E.E.E 802.3. The total of these two parts is called a PHY and is a significant portion of the Physical layer in an OSI 7 Layer reference model. The

PMA/PCS device would be a mixture of digital and analog that with current technology can be manufactured in the same process in CMOS. The PMD could be a mixture of analog in a SiGe process with optical components within an optical transceiver. An example of a preferred exemplary embodiment of the invention would have; transmission
5 rates from 155 Mbits/sec to 10 Gbits/sec; would employ an XGMII interface connecting to the PMA/PCS device but other interface protocols are possible; would also be employed in a Passive Optical Network (PON). The former example to be discussed in a concluding section with references to FIG 5, 6 and 7. Higher rates of transmission are envisioned possible with advancements in technologies. The following will discuss the
10 PMA/PCS device 100 followed by the PMD device 200. The preferred exemplary embodiment of the invention would have two transmit and receive paths from PMA/PCS to PMA/PCS device and will be discussed as such but a single or plurality of transmit and receive paths are possible.

[0015] FIG. 1 is a block diagram of a combined Physical Medium Attachment
15 (PMA) and Physical Coding Sublayer (PCS) device 100 according to an exemplary embodiment of the invention. The preferred exemplary embodiment would employ an asynchronous or synchronous interface that is represented by the TX Path 101 and RX Path 108 blocks. These blocks would manage the PMA/PCS interface that feed data into 101 and get data from 108 the TC-Layer block 106. The Transmission Convergence
20 Layer (TC-Layer) 106 block is crucial for a PON. The TC-layer is responsible to create the transport system that user traffic will exploit. The need for a TC-Layer arises in PONs because of its tree-based topology in a physical layer that must be hidden from higher layers where layer 2 bridging functions are performed. The TC-Layer could, for design performance of the embodiment, perform the additional functions of an Equalizer
25 state machine and an outer encoder and outer decoder. The TC-Layer 106 would send outgoing data to the Scrambler and Digital DEMUX block 102. The purpose of the scrambler 102 would be to randomize the data for possible improvement of the transmission. The purpose of the Digital DEMUX 102 would be to split into a plurality the transmitting data streams that would maintain the aggregated data rate equivalent to
30 the input to the Digital DEMUX 102. As mentioned previously the envisioned embodiment would have two transmit and receive paths. The advantage in splitting

transmit and receive paths is that the bit clock rates are reduced at the cost of an additional fibers. Reducing the bit clock on fiber has the effect of improving optical loss budget thereby increasing reach and/or number of clients in a point-to-multipoint PON network. Again embodiments of the invention need not split transmit and receive paths.

5 After digital DEMUX, the two transmit paths have analogous processing blocks. In order to improve the energy per bit required to deliver the transmitting data an encoding method is employed and is represented by blocks 103a & 103b. If the TC-Layer 106 employs an outer encoder/decoder then the encoding method of 103a & 103b would be an inner encoding method and the system would be enabling forward error correction
10 (FEC) recovery of bit errors. To improve communications performance by enabling the transmitted signals to better withstand the effects of various channel impairments and to increase the number of bits per symbol transmitted by the invention, the Modulation (MOD) 104a & 104b is performed. Following MOD the transmitting data would be converted to an analog signal by a Digital to Analog Converter (DAC) 105a and 105b
15 that would include ability to shape the signal for improved transmission performance. On the path of reception of data, the data would be received as an analog signal therefore an Analog to Digital Converter (ADC) 112a & 112b would be needed. To aid the ADC, a Clock Recovery (CR) 113 device is needed that is capable of recovering the clock of many data. A second CR is not needed because a Digital Delay Loop (DDL) 114 can be
20 used to aid the other ADC 112b. Note that a PON system is assumed to have a closed clock loop where the OLTs transmit clock is used to synchronize the entire PON system, which implies that PON client's recovered receive clock is used for the upstream transmit transmission. Following the ADCs 112a & 112b, the received data is processed through an Equalization method 111a & 111b to remove unwanted noise added by various
25 channel impairments. After equalization the received data would be sent into a De-Modulation/Decoder 110a & 110b block to demodulate and decode the received data. Next, the received data is descrambled and MUXed back together before being feed into the TC-Layer 106 by the De-Scrambler and Digital MUX 109 block.

[0016] FIG. 2 is a block diagram of a Physical Medium Dependent (PMD) device
30 according to an exemplary embodiment of the invention. The inputs and outputs of the PMD are analog signals. As discuss before, the preferred embodiment would have two

transmit and receive paths hence there would be two Laser Drivers 203a & 203b; two Bidirectional optical sub-assemblies often referred to as simply Bidi 202a & 202b; and two Linear Amplifiers 211a & 211b. The Bidis would employ at a minimum a Transimpedance Amplifier (TIA) 205a & 205b, a Laser Diode 206a & 206b and a Photo Diode 207a & 207b. The PMD 200 could employ a course equalization method 210a & 210b and a Receive Sensitivity Signal Interface (RSSI) that reports the measured received power. The preferred embodiment would have a serial interface (PMD intf.) 204 to enable control 209 of the course equalization 210a & 210b and the RSII1 212a and RSII2 212b.

10 [0017] FIG. 3 is a block diagram of a combined PMA/PCS and PMD device called a PHY according to an embodiment of the invention. FIG. 3 shows the two fibers 300a & 300b as envisioned in the preferred embodiment. The fibers would have particular wavelength for the transmit path and a particular wavelength for the receive path. The PMA/PCS and PMD devices are connected with analog signals capable of very high data rates; 301a & 301b; 303a and 303b. The serial interface is connected between them 302 and FIG. 3 shows the asynchronous or synchronous interface 304 and 305.

[0018] FIG. 4 is a block diagram of a Passive Optical Network (PON) utilizing the PHY according to an embodiment of the invention. The envisioned PON network with the OLT 400 and ONTs 401 are connected by the PHY through fibers and splitters.

[0019] FIG. 5 is a block diagram of an example PMA/PCS device according to an exemplary embodiment of the invention. In the example, a specific implementation of the embodiment of the invention is discussed. The example is designed to implement a 10Gbit/sec PON. For the asynchronous or synchronous interface the asynchronous XGMII interface 501 & 508 is chosen. GPON, a current PON standard from the I.T.U. used for 2.5Gbps and below data rates, is chosen for the TC-Layer implementation 506 with the addition of equalization training control and a reed-solomon encoder/decoder. GPON has it own defined Scrambler and De-scrambler method and would be implemented with the Digital MUX and DEMUX, blocks 502 & 509. For the encoding method, a 4/5 trellis method 503a & 503b is selected along with QAM-32 for the modulation 504a & 504b. With a 10Gbit/sec PON using QAM-32 modulation on dual

fibers leaves a 1.25G Symbol/sec as the symbol rate of the transmitted carrier. Therefore a 1.25GHz 5-bit DAC 505a & 505b with a corresponding 1.25G 6-bit ADC 512a & 512b are needed. The CR 513 and DDL 514 would be designed appropriately to handle the 1.25G Symbol/sec rates. Similarly if the 10G user data rate PON were to be enabled via
5 12.5G 8B/10B XAUI interface, a 12.5Gbit/sec implementation would translate into a 1.56G symbol/sec modulation rate. The equalization method selected is a Decision Feedback Equalization 511a & 511b or possibly a blind equalization method. De-modulation and Viterbi decoding 510a & 510b are selected to complement the example design decisions already made.

10 [0020] FIG. 6 is a block diagram of an example PMD device according to an exemplary embodiment of the invention. The example PMD device would comply with the Small Form-factor Pluggable (SFP) 600 specification. This specification has constraints on all physical aspects such as package size and pins. The SFP 600 would contain the necessary; LDs 603a & 603b; LAs 611a & 611b; TIAs 605a & 605b; RSSIs
15 612a & 612b; Course EQs 610a & 610b; and PDs 607a & 607b. The SFP 600 would use Distributed Feedback (DFB) edge emitter laser diodes 606a & 606b and a Monitor Photo Diode (MPD) 613a & 613b. The SFP would have an I²C bus interface 604 that would allow control by the PMA/PCS device of the Course EQs 610a & 610b, RSSIs 612a & 612b and MPD.

20 [0021] FIG. 7 is a block diagram of an example PHY device according to an exemplary embodiment of the invention. The PMA/PCS and PMD are connected through high-speed analog lines 701a 701b & 703a 703b, as well as the I²C bus 702. XGMII 704 & 705 connections for the PMA/PCS are shown as well.

25 [0022] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

30

What is claimed is:

1. A system and the method for performing broadband transmission over optical networks comprising of:
 - a. A system and method of a Physical Medium Attachment/Physical Coding Sublayer (PMA/PCS) device.
 - b. A system and method of a Physical Medium Dependent (PMD) device.
 - c. A system and method of a PHY device.
2. The method of claim 1, wherein step (a) contains an asynchronous or synchronous interface interfacing to a TC-Layer.
3. The method of claim 1, wherein step (a) contains a TC-Layer to provide management of user traffic.
4. The method of claim 3, wherein the TC-Layer controls a separate equalizer process method.
5. The method of claim 3, wherein the TC-Layer performs an outer encoding and decoding method on user traffic.
6. The method of claim 1, wherein step (a) contains a scrambling and descrambling of user traffic
7. The method of claim 1, wherein step (a) contains a MUX and DEMUX of user traffic.
8. The method of claim 1, wherein step (a) contains an encoding and decoding of user traffic or inner encoding and decoding of user traffic.
9. The method of claim 1, wherein step (a) contains a modulation and demodulation of user traffic.
10. The method of claim 1, wherein step (a) contains a digital to analog converter with the ability to pre-shape user traffic.

11. The method of claim 1, wherein step (a) contains an analog to digital converter.
12. The method of claim 1, wherein step (a) contains a clock recovery method for
5 received user traffic.
13. The method of claim 1, wherein step (a) contains a plurality digital delay loop to
be used with a clock recovery method.
14. The method of claim 1, wherein step (a) contains an equalizer for received user
10 traffic.
15. The method of claim 1, wherein step (a) contains a plurality of transmit and
receive process paths.
16. The method of claim 1, wherein step (b) contains a plurality of bidirectional
15 transceivers.
17. The method of claim 16, wherein the bidirectional optical sub-assemblies used
20 within the optical transceiver contains a Monitor Photo Diode.
18. The method of claim 16, wherein the bidirectional optical sub-assemblies used
within the optical transceiver contains a Photo Diode.
19. The method of claim 16, wherein the bidirectional optical sub-assemblies used
25 within the optical transceiver contains a Laser Diode.
20. The method of claim 16, wherein the bidirectional optical sub-assemblies used
within the optical transceiver contains a Transimpedance Amplifier.
21. The method of claim 1, wherein step (b) contains a plurality of laser drivers.
30
22. The method of claim 1, wherein step (b) contains a plurality of linear amplifiers.
23. The method of claim 1, wherein step (b) contains a plurality of course equalizers.
35

24. The method of claim 1, wherein step (b) contains a serial interface.

5 25. The method of claim 24, wherein the serial interface enables manipulation of
course equalizer and received signal swing interface (RSSI).

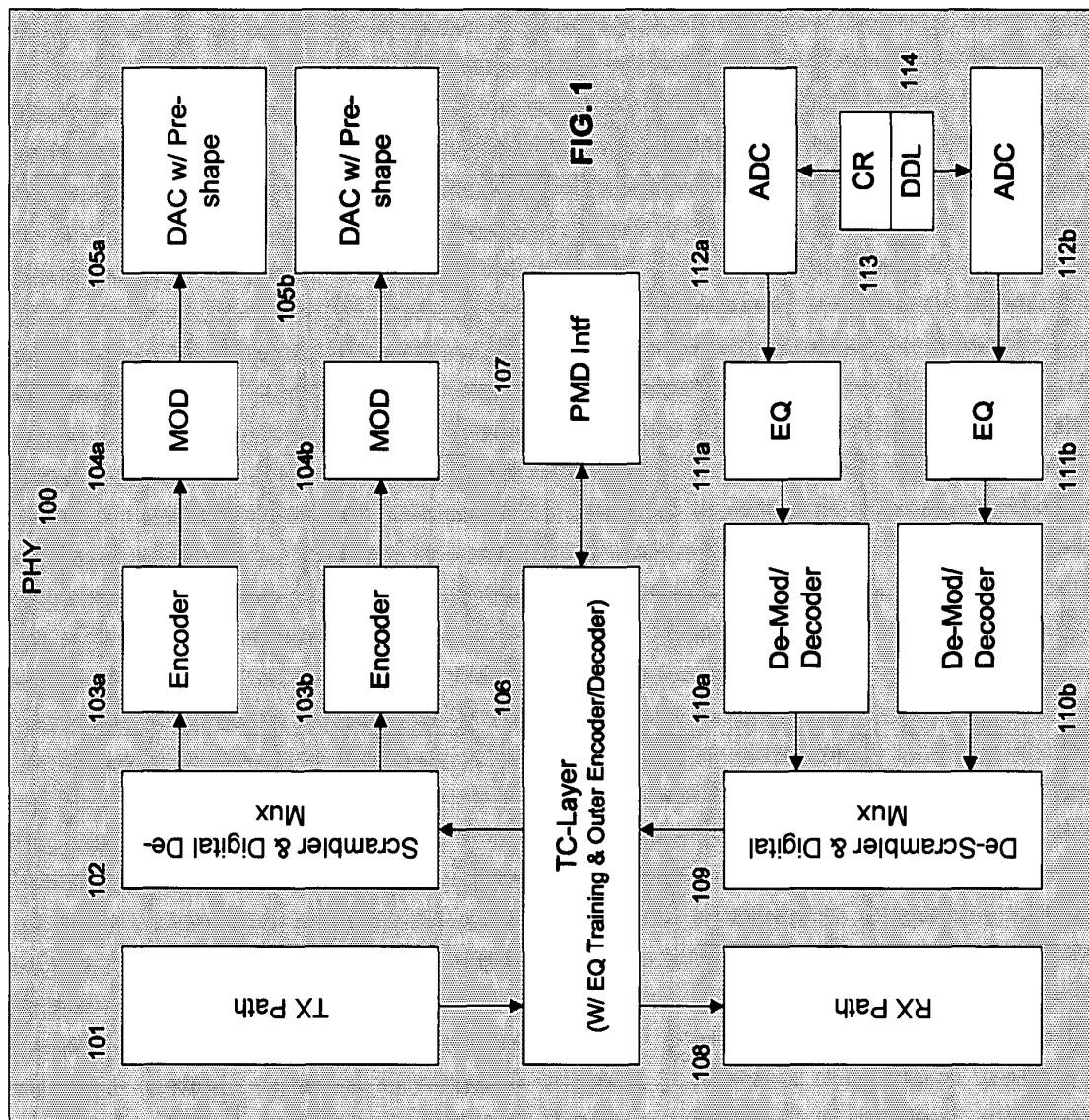
26. The method of claim 1, wherein step (b) contains a received signal serial interface
(RSSI).

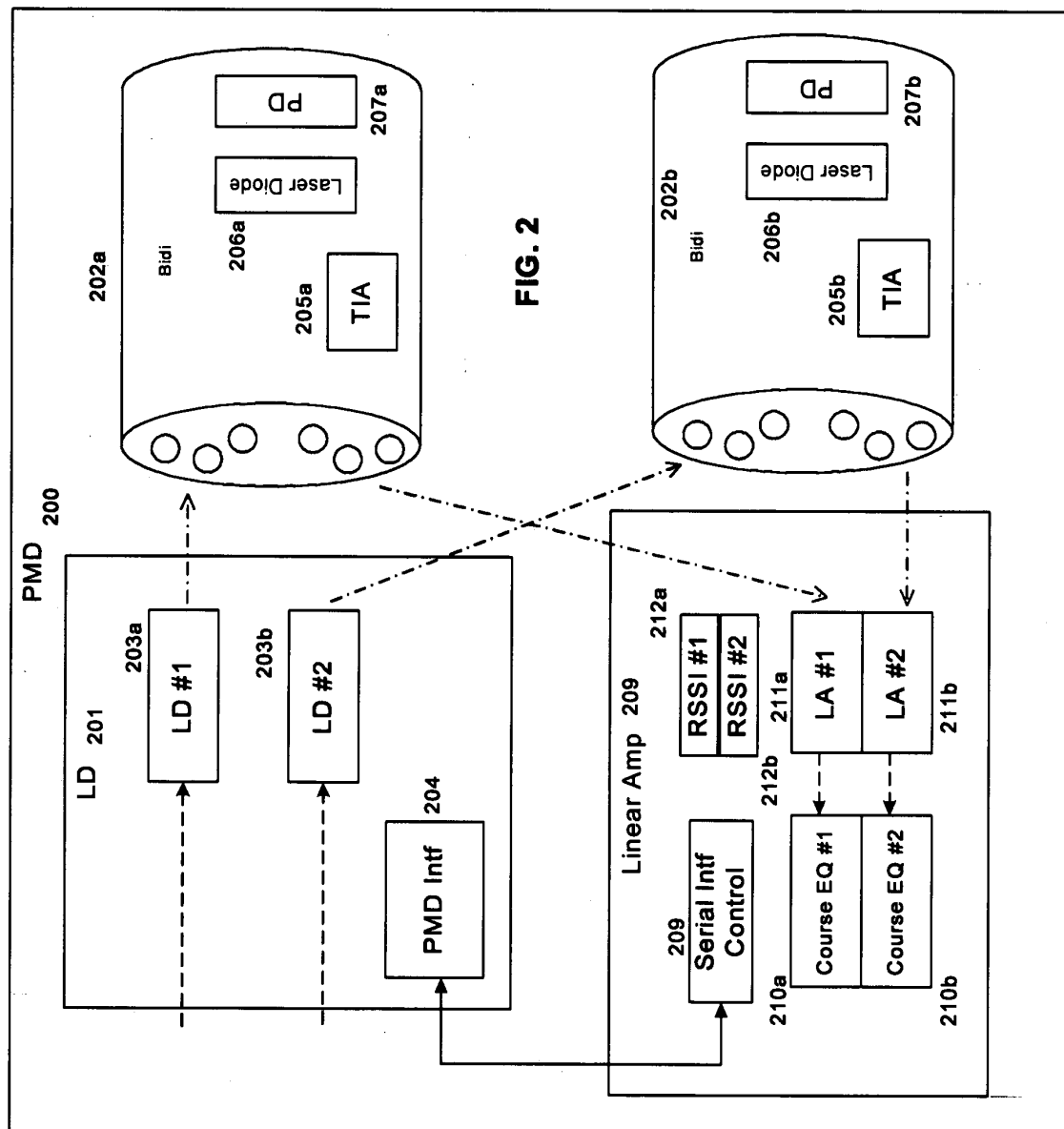
10 27. The method of claim 1, wherein step (c) contains high-speed analog connections
for the PMA/PCS and PMD devices.

28. The method of claim 1, wherein step (c) contains a plurality of fibers connecting
to the PMD device.

15 29. The method of claim 1, wherein step (c) contains an asynchronous or synchronous
interface to connect the PMA/PCS device to Layer 2 system.

20





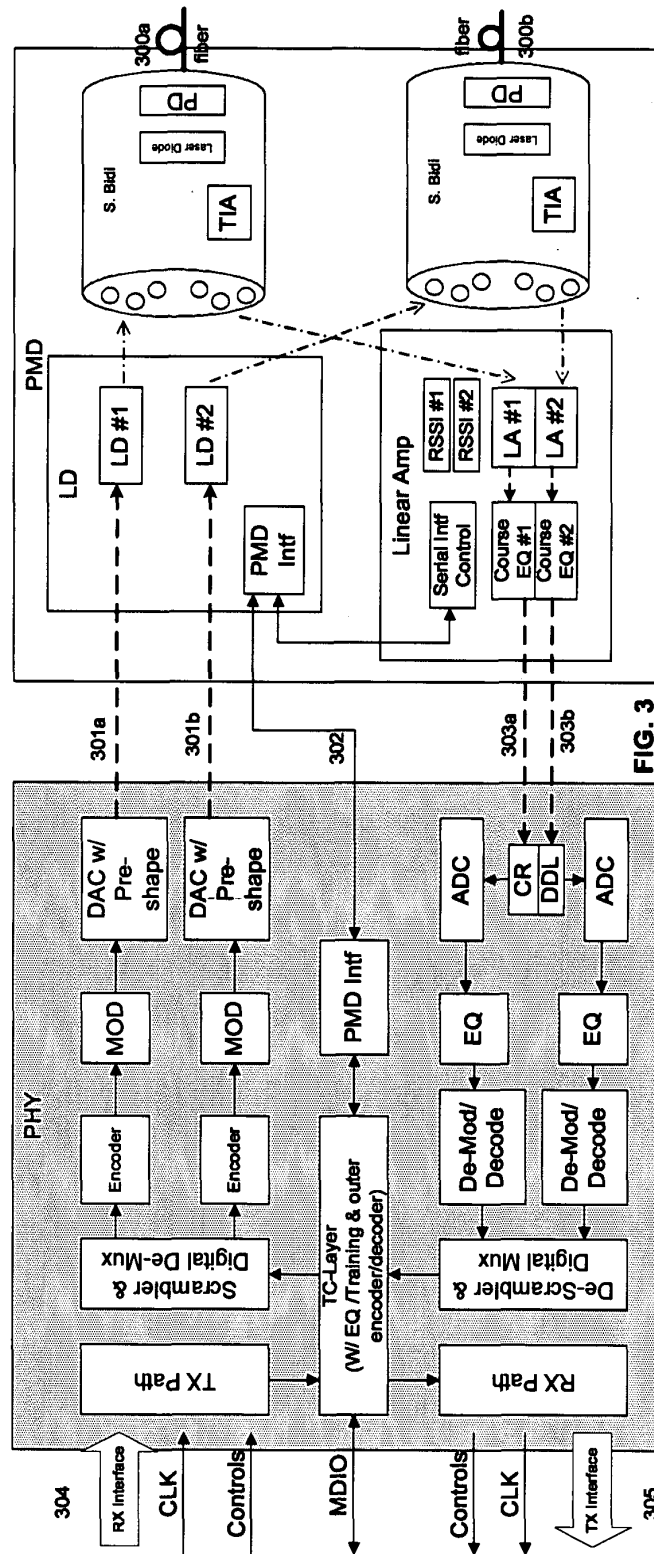


FIG. 3

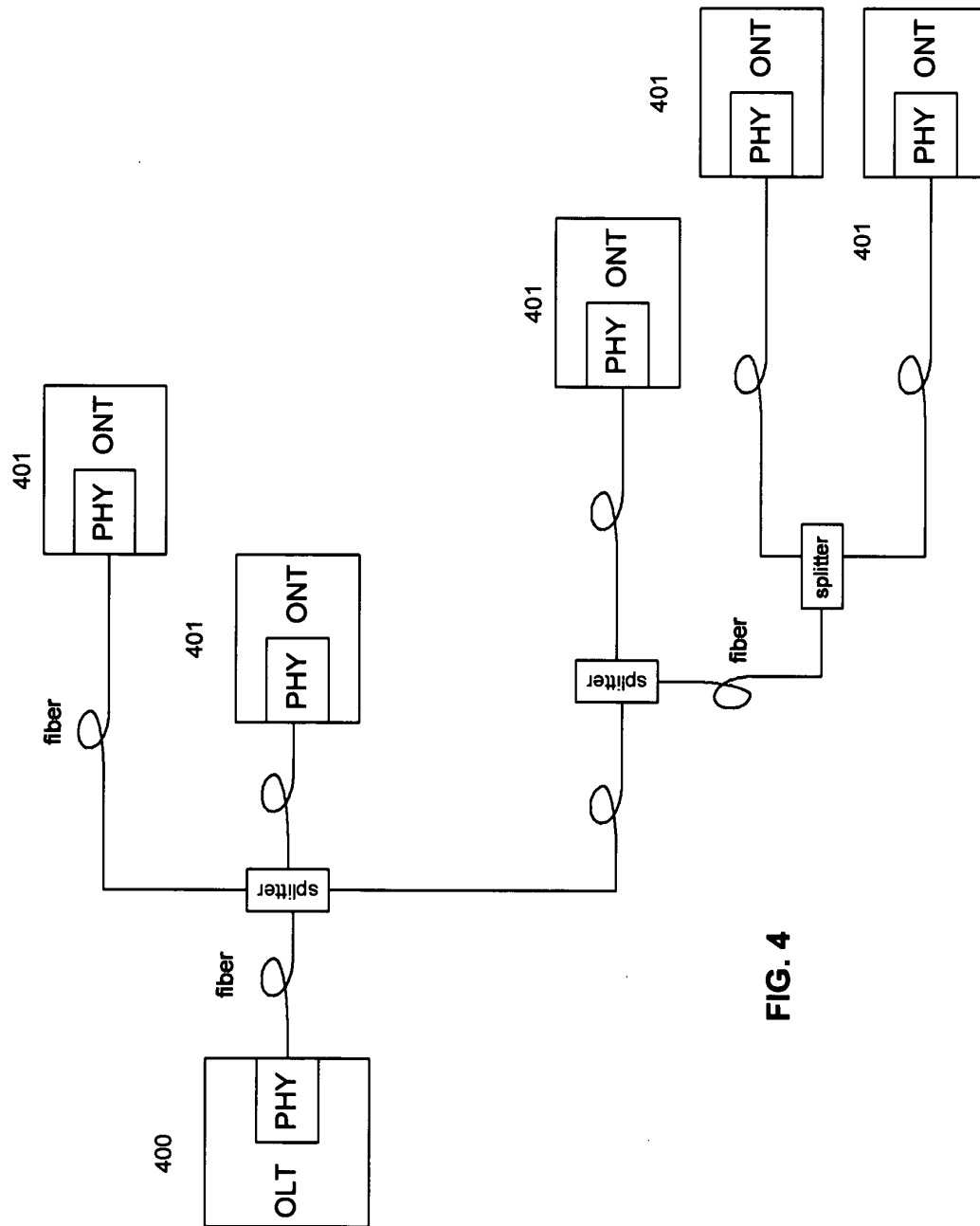
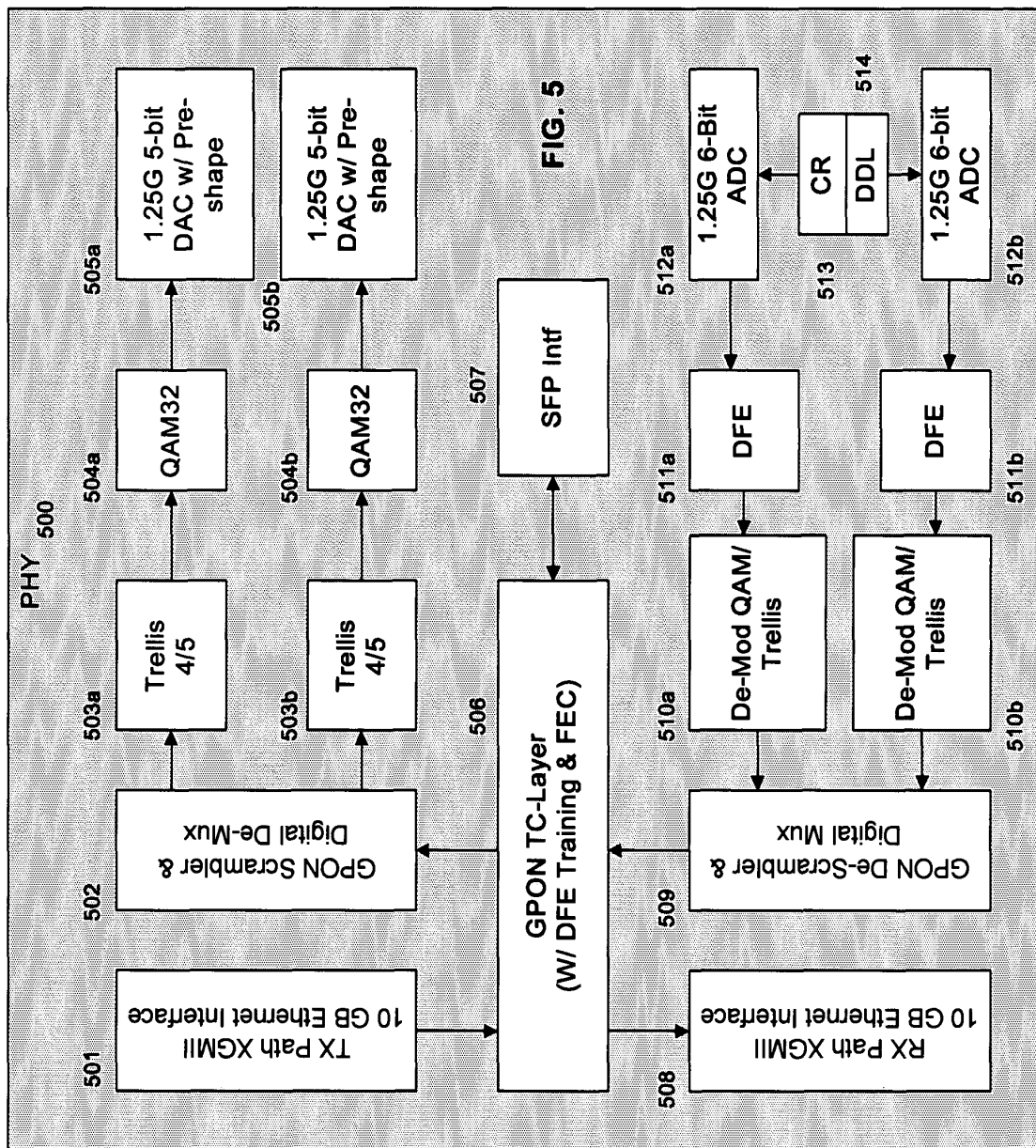
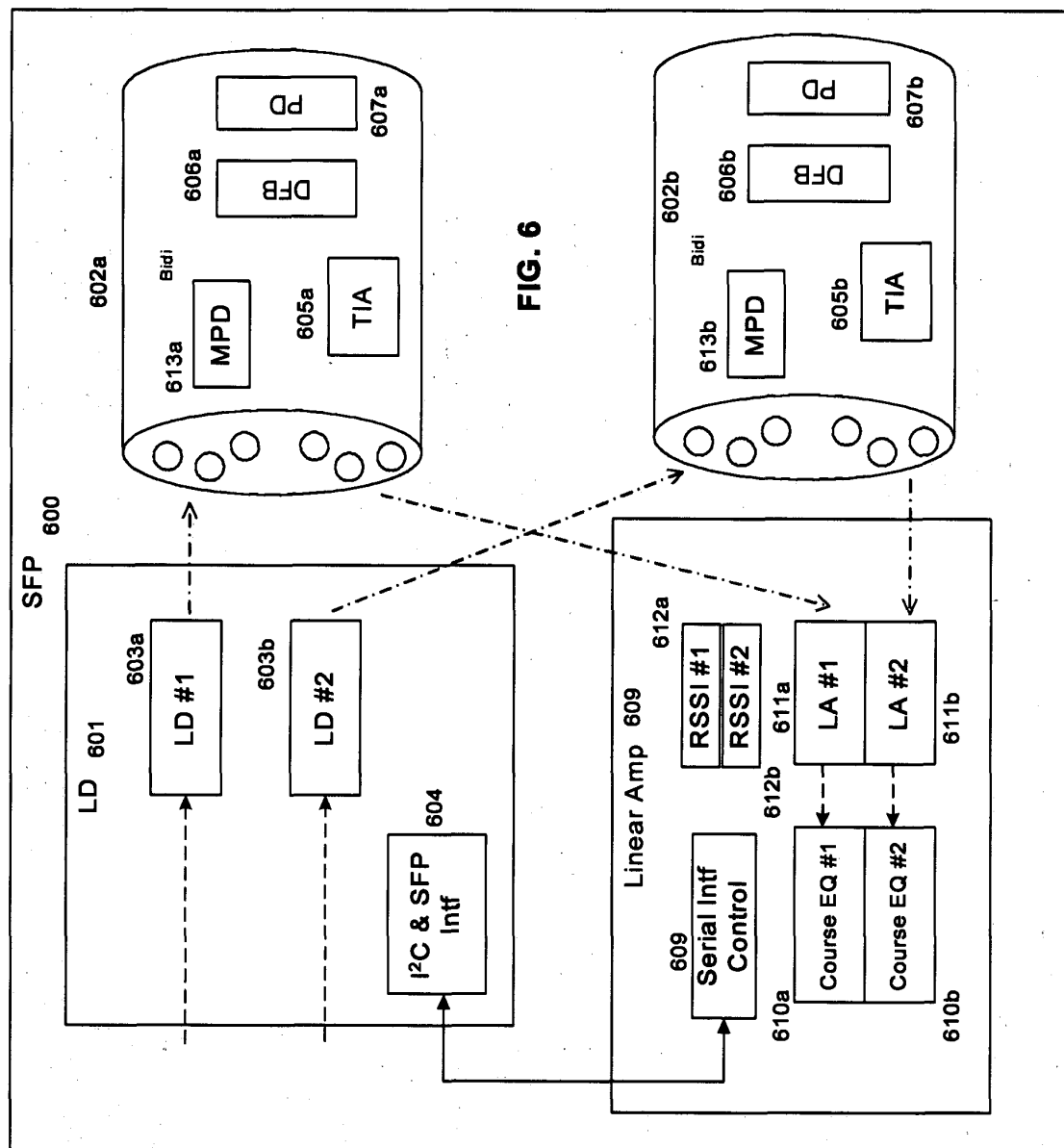


FIG. 4





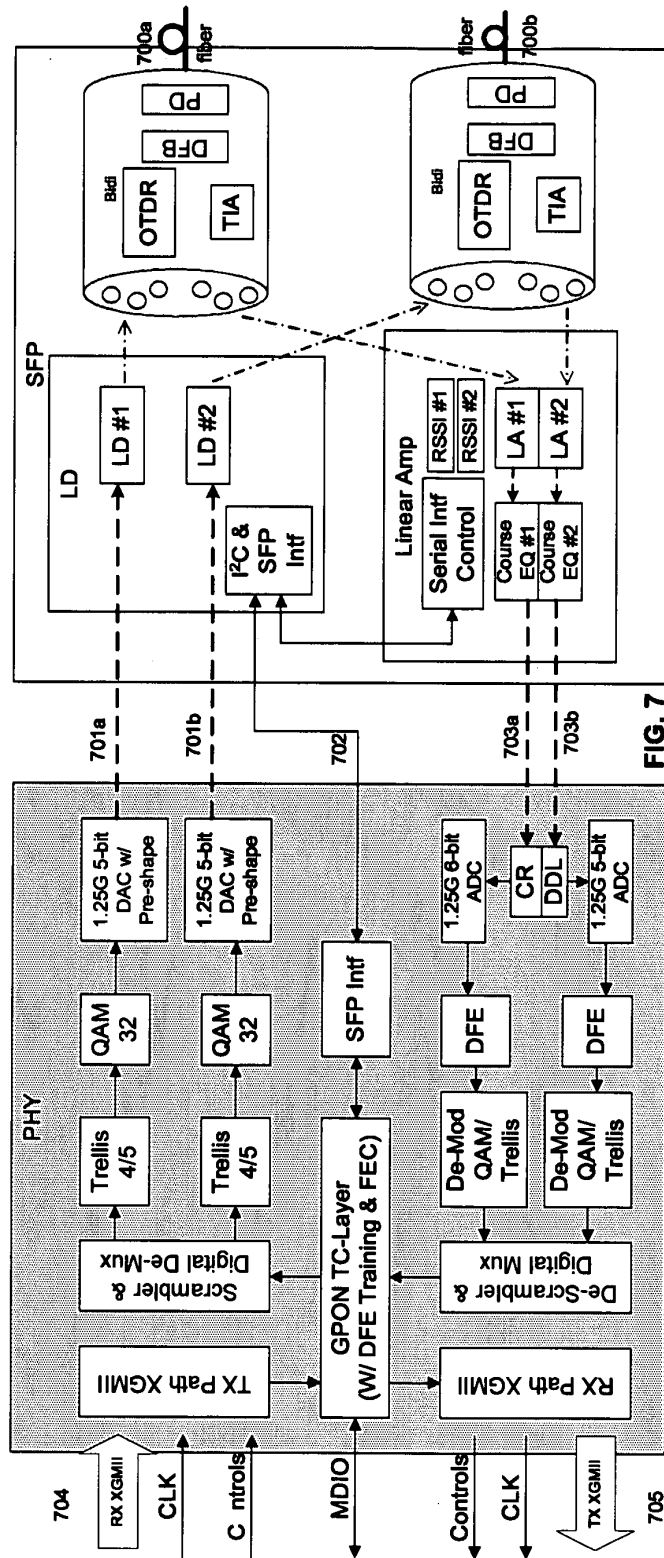


FIG. 7

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/25/2003 BABRAHA1 00000042 60480488

01 FC:2005

80.00 DP

PTO-1556
(5/87)