

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ARISTA NETWORKS, INC.,
Petitioner

v.

CORRIGENT CORPORATION,
Patent Owner.

Case No. IPR2023-00837

U.S. Patent No. 6,957,369

Petition for Inter Partes Review of U.S. Patent No. 6,957,369

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PETITIONER’S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 6,957,369 (“the ’369 patent”)
1002	Prosecution History of the ’369 patent
1003	Declaration of Dr. Paul Min
1004	Curriculum Vitae of Dr. Paul Min
1005	<i>Corrigent Corp. v. Dell Technologies et al.</i> , No. 1:22-cv-00496 (D. Del.) Docket
1006	<i>Corrigent Corp. v. Arista Networks, Inc.</i> , No. 1:22-cv-00497 (D. Del.) Docket
1007	<i>Corrigent Corp. v. Cisco Systems, Inc.</i> , No. 6:22-cv-00396 (W.D. Tex.) Docket
1008	U.S. Patent No. 5,841,788 to Ke (“Ke”)
1009	U.S. Patent No. 4,685,102 to Lewis et al. (“Lewis”)
1010	U.S. Patent No. 4,074,352 to Cook et al. (“Cook”)
1011	U.S. Patent Pub. No. 2003/0101426 to Sarkinen (“Sarkinen”)
1012	Braden, R., Ed., “Requirements for Internet Hosts – Communication Layers,” STD 3, RFC 1122, DOI 10.17487/RFC1122, October 1989, < https://www.rfc-editor.org/info/rfc1122 >.
1013	Excerpt of William Stallings, <i>Data & Computer Communications</i> 236 (6 th ed. 2000)
1014	Western District of Texas Statistics (Docket Navigator)
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1016	<i>Dell Technologies Inc. et. al v. Corrigent Corp.</i> , IPR2023-00464, Paper 1 (Jan. 19, 2023)
1017	<i>Corrigent Corp. v. Cisco Systems, Inc.</i> , No. 6:22-cv-00396 (W.D. Tex.) Dkt No. 69
1018	Declaration of Dr. Nader Mir

I. INTRODUCTION

Arista Networks, Inc. (“Arista”) hereby petitions for *inter partes* review of U.S. Patent No. 6,957,369 (the “ ’369 Patent”) and seeks cancellation of claims 1-26 (“the Challenged Claims”) because they are unpatentable under 35 U.S.C. §103.

The ’369 Patent is directed to the very simple idea of a loop back test. The patent also discusses the advantages of performing such tests on traces or lines that are known to be idle, or not currently in use, so that hidden failures can be detected. However, this invention is not novel. Both the problem and solution were disclosed in the prior art, as discussed herein. Consistent with the analysis that follows and is supported by Petitioner’s expert, Petitioner respectfully requests that the Board institute IPR proceedings and find the Challenged Claims unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest

The real party-in-interest is Arista Networks, Inc. (“Petitioner”). No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

B. Related Matters

The ’369 Patent is the subject of this IPR Petition, is also asserted in the following patent litigation suits brought by Patent Owner Corrigent Corporation, against parties, including against Petitioner, and is the subject of an existing IPR:

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- *Corrigent Corp. v. Dell Technologies et al.*, No. 1:22-cv-00496 (D. Del.)
(EX1005) (“*Dell* litigation”);
- *Corrigent Corp. v. Arista Networks, Inc.*, No. 1:22-cv-00497 (D. Del.)
(EX1006) (“*Arista* litigation” or “co-pending litigation”);
- *Corrigent Corp. v. Cisco Systems, Inc.*, No. 6:22-cv-00396 (W.D. Tex.)
(EX1007) (“*Cisco* litigation”); and
- *Dell Technologies Inc. et. al v. Corrigent Corp.*, IPR2023-00464, Jan. 19,
2023 (EX1016) (“*Dell* petition”).

C. Lead and Backup Counsel

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of counsel:

Lead Counsel	Back-up Counsel
Eliot D. Williams (Reg. No. 50,822) Baker Botts L.L.P. 700 K Street, N.W. Washington, D.C., 20001-5692 Tel: 202-639-1334 Eliot.Williams@BakerBotts.com	Kurt Pankratz (Reg. No. 46,977) Baker Botts L.L.P. 2001 Ross Avenue, Suite 900 Dallas, TX 75201-2980 Tel: 214-953-6500 Kurt.Pankratz@BakerBotts.com Jeremy J. Taylor (Reg. No. 73,912) Baker Botts L.L.P. 101 California Street, Suite 3200 San Francisco, CA 94111 Tel: 415-291-6200 Jeremy.Taylor@BakerBotts.com

Pursuant to 37 C.F.R. §42.10(b), a power of attorney accompanies this Petition.

D. Service Information

Service via hand delivery or postal mail may be made at the addresses of the lead and back-up counsel above. Petitioner hereby consents to electronic service, and service via electronic mail may be made at the email addresses provided above for the lead and back-up counsel.

III. PAYMENT OF FEES

Pursuant to 37 C.F.R. §§42.103 and 42.15(a), the required fee is being submitted herewith.

IV. REQUIREMENTS OF *INTER PARTES* REVIEW

A. Standing

Pursuant to 37 C.F.R. §42.104(a), Petitioner certifies that the '369 Patent is available for IPR, and that Petitioner is not barred from requesting an IPR on the grounds identified in this Petition.

B. Identification of Challenge and Relief Requested

Pursuant to 37 C.F.R. §42.104(b), Petitioner requests that the Board institute IPR of claims 1-26 of the '369 Patent (the "Challenged Claims") under 35 U.S.C. §103 on the prior art and grounds described below:

Ground	'369 Patent Claims	Basis for Rejection¹
1	1-26	Obvious over Ke and Lewis
2	3, 6, 8, 13, 14, 17, 21, 25, and 26	Obvious over Ke, Lewis, and Sarkinen
3	1-26	Obvious over Cook and Lewis
4	3, 6, 8, 13, 14, 17, 21, 25, and 26	Obvious over Cook, Lewis, and Sarkinen

U.S. Patent No. 5,841,788 (“**Ke**”, EX1008) qualifies as prior art under 35 U.S.C. § 102(a) (b) and (e). Ke was filed on October 18, 1996 and issued on November 24, 1998.

U.S. Patent No. 4,685,102 (“**Lewis**”, EX1009) qualifies as prior art under 35 U.S.C. § 102 (a) (b) and (e). Lewis was filed on May 11, 1984 and issued on August 4, 1987.

U.S. Patent No. 4,074,352 (“**Cook**”, EX1010) qualifies as prior art under 35 U.S.C. § 102 (a) (b) and (e). Cook was filed on September 30, 1976 and issued on February 14, 1978.

U.S. Patent Application Pub. No. 2003/0101426 (“**Sarkinen**”, EX1011) qualifies as prior art under 35 U.S.C. § 102(e). Sarkinen was filed on November 27, 2001 and published on May 29, 2003.

¹ All obviousness grounds include the knowledge of a POSITA.

C. How the Challenged Claims Are to Be Construed Under 37 C.F.R. §42.104(b)(3)

A claim subject to *inter partes* review “shall be construed using the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. §42.100(b) (Nov. 13, 2018); 83 Fed. Reg. 51358 (2018). Claim construction proceedings have been completed in the *Cisco* litigation. EX 1017. The plain and ordinary meaning was adopted for several terms that appear in the ’369 Patent. *Id.* Petitioner does not believe any express construction of the claim terms in the ’369 Patent is necessary for any of the grounds presented in this IPR. The claims are invalid under the constructions adopted by the district court in the *Cisco* litigation.

D. How the Challenged Claims Are Unpatentable Under 37 C.F.R. §42.104(b)(4)

The following sections explain how the Challenged Claims are unpatentable under the statutory grounds identified above, including where each element of the claim is found in the prior art patents or printed publications.

E. Supporting Evidence Under 37 C.F.R. §42.104(b)(5)

The exhibit numbers of the supporting evidence relied upon, and the relevance of the evidence to the Challenged Claims, including an identification of specific portions of the evidence that support the challenge, are provided below. The

technical information and grounds for unpatentability explained in the petition are further supported by the Declaration of Dr. Paul Min (EX1003). A List of Exhibits is included in this paper pursuant to 37 C.F.R. §42.63(e).

V. THRESHOLD REQUIREMENT FOR *INTER PARTES* REVIEW

Under 35 U.S.C. §314(a), institution of *inter partes* review requires “a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition.” This petition meets this threshold for each of the asserted grounds of unpatentability.

VI. PERSON OF ORDINARY SKILL IN THE ART

The alleged invention relates to testing lines or traces between modules optionally connected via a backplane. EX1001, Abstract. A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention (May 2002) would have had a degree in electrical engineering, computer engineering, or a similar discipline, with at least two years of relevant industry or research experience (or additional education). EX1003, ¶19. The relevant experience would include a working understanding of networks, switches and electronic devices including devices that possess a backplane. *Id.* More experience can substitute for less education and vice versa. *Id.*

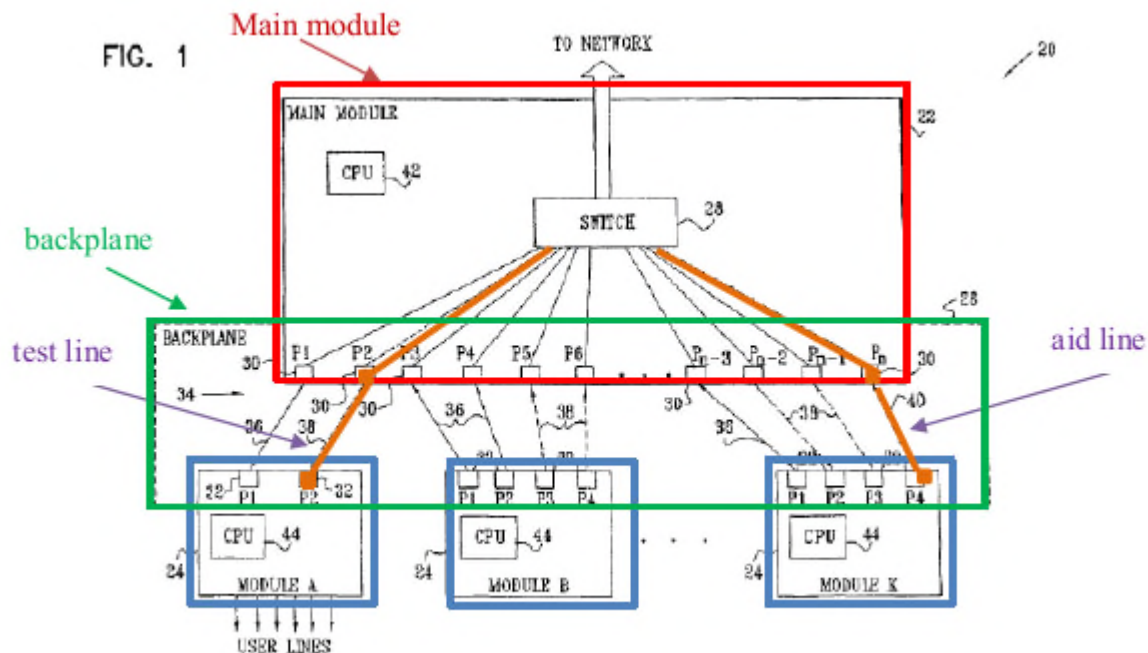
VII. OVERVIEW OF THE ’369 PATENT

The ’369 Patent is directed to a “loop back” test to determine whether lines or traces (especially those known to be idle or inactive) are functioning properly

“without intruding on normal traffic carried by the system’s active lines.” EX1001, 2:26-29. Without self-testing, the ’369 Patent states that failures in lines, especially idle lines, may go undetected. *Id.*, 1:11-15.

The ’369 Patent describes a principal embodiment comprising a backplane system in which a “main module” and two or more “subsidiary modules” are plugged into the backplane and communicate over traces on the printed circuit board of the backplane. *Id.*, 1:11-36; 1:61-2:4; 2:40-47; 3:12-20; 3:51-4:37; 6:54-67.

Figure 1 (annotated below) depicts this arrangement:



The patent explains that the disclosed backplane configuration was commonly known, stating the invention relies on “existing components in the system.” *Id.*, 1:25-26; 2:29-32. As shown above, the **main module 22** is connected to the network. *Id.*, 1:67-2:2; 5:13-14. It contains a system control processor 42 and a switch 28.

Id., 1:30-32; 5:1-31. The main module is then connected via the **backplane 28** to two or more “subsidiary modules” 24. *Id.*, 1:25-30. To test the system without interrupting service, the **idle lines 38** are tested instead of the active lines 36. *Id.*, 5:26-31.

The patent describes a six-step process to test an idle line for “hidden failures.” *Id.*, Fig. 2, 5:55-6:39.

1. The main module selects an idle line that connects a first subsidiary module to a port of the switch of the main module to serve as the “aid line” 40, an idle line in which traffic will be looped back through. *Id.*, 5:61-67.
2. The main module then instructs the first subsidiary module to loop back all traffic via the aid line. *Id.*, 5:63-6:9.
3. The main module selects another idle line connected to a second subsidiary module to be the test line 38. *Id.*, 6:10-13.
4. The main module then configures its switch to connect the aid line and the test line, creating a loop or a “virtual connection” (depicted as orange in the figure above). *Id.*, 6:14-17.
5. The main module then instructs the second subsidiary module to send test traffic over the configured loop-back. *Id.*, 6:18-22.

6. The main module determines a failure has occurred if the test traffic does not return properly. *Id.*, 6:23-39.

This process, with a few variations, is claimed in all independent claims. *Id.*, claims 1, 8, 15, 21. For example, certain claims do not require a backplane, and certain claims do not require the lines or traces to be idle when tested.

A. Summary of the Prosecution History of the '369 Patent

During prosecution, the examiner, *inter alia*, rejected original claims 1-4, 6-9 and 11-14 as anticipated by two prior art references. EX1002, 68. During an Examiner Interview, it was discussed that an amendment which included “wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module” would overcome the prior art challenge. EX1002, 85-95. Because the Examiner was not presented with any reference (such as is now presented with Lewis) that sets up a testing loop between a main module and a subsidiary module through a switch, the Examiner allowed the claims after the discussion wherein the clause was added, and the patent issued on October 18, 2005. EX1002, 111; EX1001, [45]. As discussed below, that sole ground of patentability is rebutted by the Lewis reference, when combined with a backplane testing system such as Ke or Cook.

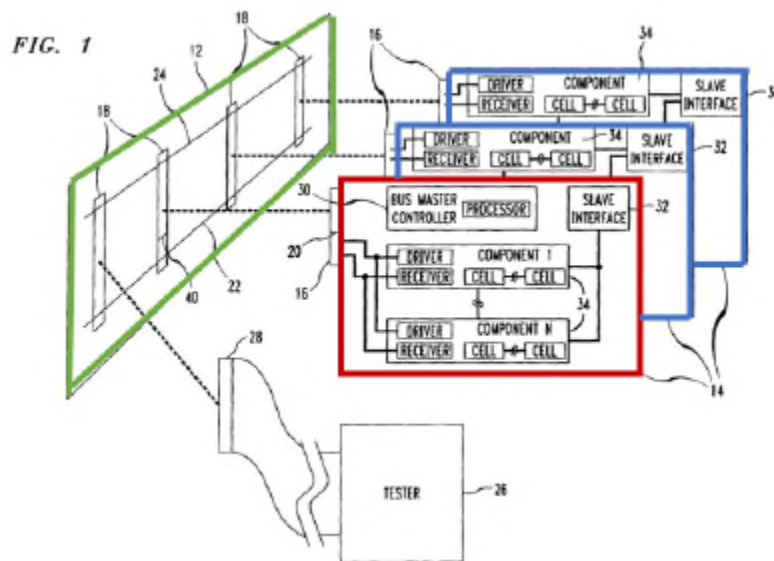
VIII. GROUNDS OF UNPATENTABILITY

A. Ground 1: Ke in View of Lewis Renders Obvious the Challenged Claims.

The combination of Ke and Lewis (“Ke-Lewis”) renders obvious claims 1-26 of the ’369 Patent.

1. Ke

Ke discloses a method for detecting errors in the traces associated with backplanes. According to Ke, “[b]ackplane testing involves testing the interconnects to ensure that the assembled backplane is functioning properly.” EX1008, 1:26-28. More specifically, Ke-Figure 1 depicts the structure for backplane testing. There is a board that has the “bus master controller” 30 that may perform the testing of the backplane by driving the other boards via a slave interface 32. *Id.*, 3:24-36. The master board and the other boards are all plugged into a backplane 12. *Id.*, 3:16-36.



EX1008, Fig. 1.²

Ke further explains that when the bus master drives the testing, messages may be “addressed” to each of the other boards using protocols communicated via the test bus 24 on the backplane 12. *Id.*, 3:28-35.

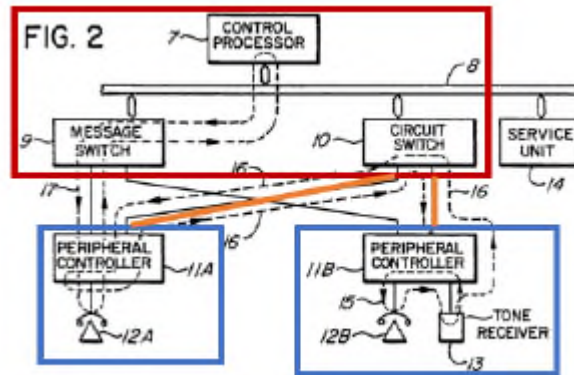
Ke acknowledges that there are different ways to test backplanes in the prior art and states that, because backplanes are highly configurable, it may be difficult to test certain configurations. *Id.*, 1:30-2:19. Ke discloses one such testing configuration for boundary testing where the backplane connections are tested one at a time by toggling the connections on and off to test one connection at a time. *Id.*, 3:61-4:40. When errors in the system are detected, they may be reported and classified to the system. *Id.*, 4:1-12.

2. Lewis

Lewis discloses a “loop back” system test circuit that can be used to test links between peripherals to detect failures in components. EX1009, Abstract, 1:25-38. In connection with Figure 2, Lewis explains that the **circuit switch 10—which communicates with a control processor 7 and message switch 9**—can set up a communication loop for testing the connection with **peripherals 12A and 13**.

² Annotations added on all figures unless otherwise noted.

EX1009, 3:47-60. In this example, the circuit switch sets up a loop 16 that connects peripheral 12A with peripheral 13 through the circuit switch 10.



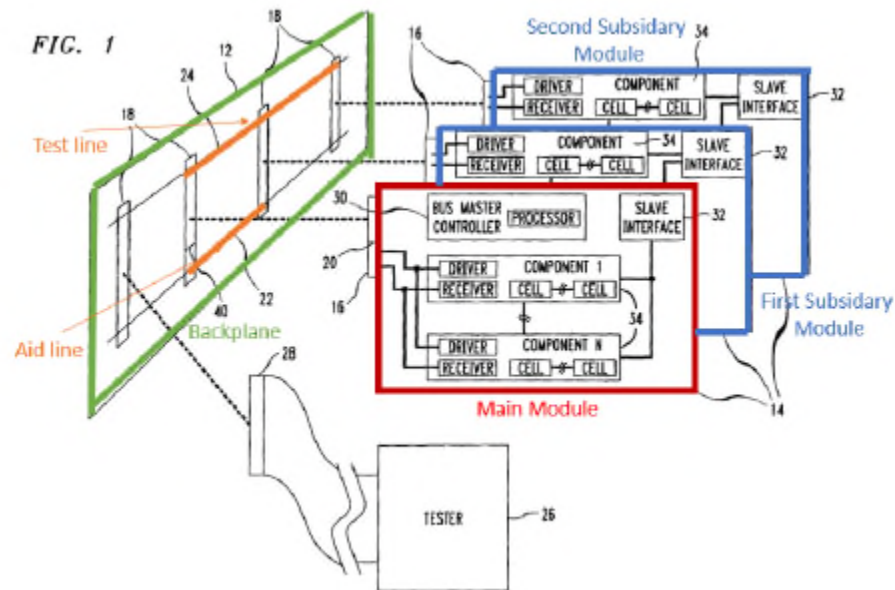
Id., Fig. 2.

According to Lewis, the control processor can send a message to peripheral 12A to trigger a loop back test. The loop back test would travel via loop 16 from 12A to circuit switch 10 to peripheral 13. Peripheral 13 would be configured to loop back the message to circuit switch 10 and then back to peripheral 12A. *Id.*, 4:42-54. Lewis further explains that testing should be performed during times when the links are idle. *Id.*, 2:19-20, 14:31-34. After the loop back test is performed, the result of the test is reported back to the message switch. *Id.*, 4:34-41, 4:49-52.

3. Motivations to Combine Ke and Lewis

A POSITA would have been motivated to combine the backplane testing described in Ke with the loop back testing described in Lewis as depicted below.

EX1003, ¶¶ 77-85.



EX1008, Fig. 1. (annotated)

The main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as disclosed in Lewis. The backplane modules in Ke would then perform the loop back test described in Lewis set forth above, where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines. EX1009, 4:42-54. This combination would have been obvious to a POSITA for multiple reasons.

First, both references are generally directed to testing connections within a system with multiple components. Ke recites a master controller that directs testing in other boards plugged into a backplane. EX1008, 3:24-37. Lewis recites a similar set up where the control processor/circuit switch direct the testing of peripheral controllers. EX1009, 3:47-60. A POSITA would have been motivated to combine the testing protocol in Lewis in the structure disclosed in Ke because a POSITA

would have understood the benefits of a loop back test in the context of a backplane with a master controller. EX1003, ¶¶78-79.

Second, Ke makes clear that its backplanes are highly configurable with many different board types, so the testing configurations should be adaptable and flexible. EX1008, 1:30-2:18. For example, Ke explains that there are many types of boards that may be plugged into a backplane, like memory and input/output devices. *Id.*, 1:65-67. A POSITA therefore would have been motivated to look at other testing configurations, like the one disclosed in Lewis for the creation of a loop back test. It would have been obvious to a POSITA that testing in a backplane could benefit from such a loop back test because there are many times when the different boards in a backplane need to communicate with each other. EX1003, ¶80. A POSITA would have recognized that there are times when data needs to be transferred to and from different boards on the backplane, e.g., from memory to an input-output device. *Id.* A POSITA therefore would have been motivated to apply the loop back testing between two peripherals in Lewis to the structure in Ke to test the connection between two boards in the backplane. *Id.*, ¶81.

Third, a POSITA would have been motivated to test the backplane lines while they were idle as disclosed in Lewis. EX1009, 2:19-20. As Ke explains, testing the backplane traces may require disabling certain parts to avoid damage to circuit components. EX1008, 2:29-35. A POSITA would understand that the best time to

disable those parts and perform the test is when the lines are otherwise idle because that would avoid disrupting traffic when the lines were in use. EX1003, ¶82.

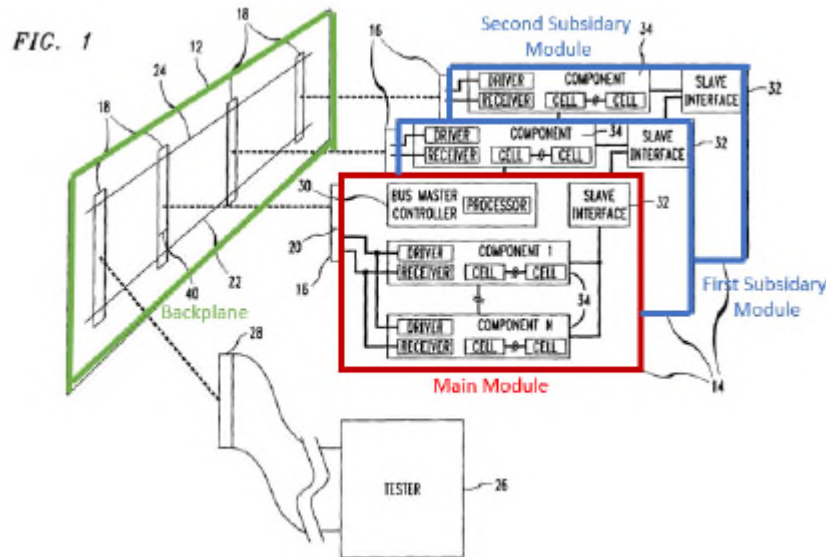
Reasonable expectation of success. A POSITA would have had a reasonable expectation of success to implement the testing in Lewis in the backplane structure from Ke because Ke acknowledged that there were multiple possible techniques for testing backplanes. EX1008, 1:30-2:18. A POSITA would therefore have a reasonable expectation of success to apply different testing techniques to the backplane structure in Ke, including the one from Lewis. EX1003, ¶83. Furthermore, Ke also explains that the bus master may control the test and send test data to different boards by addressing the data to those boards. EX1008, 3:28-35. A POSITA would have therefore understood that the loop back testing between specific peripherals in Lewis could be employed in Ke by using the master bus controller to control testing between specific boards. EX1003, ¶84.

4. Claim 1[pre]³:

To the extent the preamble is limiting, Ke-Lewis render obvious 1[pre]. Ke discloses an “**electronic system** having a backplane to be tested.” EX1008, 2:55-56 (emphasis added). That electronic system has **a card with the bus master controller 30 (main module)** and **at least two other cards (first and second subsidiary modules)**.

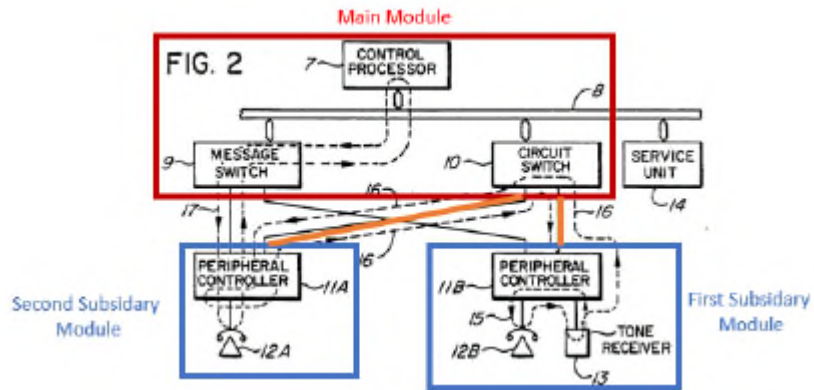
³The corresponding claim language is available in the APPENDIX: CHALLENGED CLAIM LISTING

The **main module** and **subsidiary modules** are connected by a **backplane 12** (one or more lines for carrying data). *Id.*, Fig. 1; EX1003, ¶186.



EX1008, Fig. 1.

This same basic structure from Ke is mirrored in Lewis, and it would have been obvious to combine Ke with Lewis as set forth above. EX1003, ¶187. Like Ke, Lewis describes a **circuit switch 10**—which communicates with a **control processor 7** and **message switch 9**—(**main module**) that can set up a communication loop for testing the connection with peripherals **12A** (**second subsidiary module**) and **13** (**first subsidiary module**). EX1009, 3:47-60.



Id., Fig. 2.

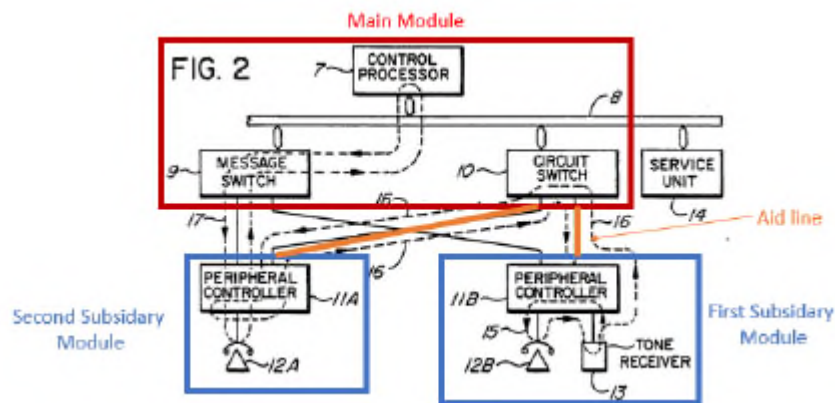
Ke further discloses that the lines may sometimes not be in use or disabled. EX1008, 3:61-67. Alternatively, it would have been obvious to a POSITA that the lines in the backplane would sometimes be idle or not in use. EX1003, ¶90. Lewis also makes clear that there are times when the lines or connections are idle and that testing should be done at the times when such lines are idle. EX1009, 2:19-20. It would have been obvious to a POSITA to combine Ke with Lewis for the reasons disclosed above. EX1003, ¶¶89-90.

Ke discloses that the main module acts as a switch by driving the testing and addressing data to be sent to different boards. EX1008, 3:61-67; EX1003, ¶90. Ke further explains that the main module is connected to the backplane by a number of pins on the edge connectors 16. EX1008, 3:16-23. A POSITA would have understood that these pins act as the interconnect or port between the board and the backplane, which connect it to other interconnects. EX1003, ¶¶90-91.

Ke further discloses that the main module performs testing on the interconnects in the backplane (self-testing). EX1008, Abstract, Title; EX1003, ¶¶92-93.

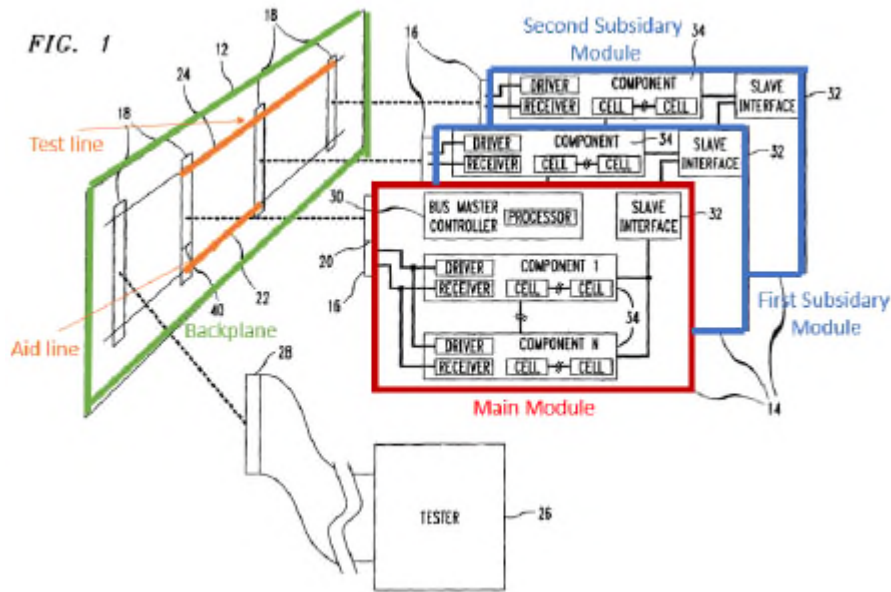
5. Claim 1[a]:

Ke-Lewis discloses 1[a]. Lewis discloses setting up a loop back test when the lines are idle. EX1009, 2:19-20. When the lines are idle, the system sets up a loop back circuit by choosing an aid line between the first subsidiary module and the circuit switch in the main module. *Id.*, 4:23-25; 4:42-54.



Id., Fig. 2.

This same set up is mirrored by the structure in Ke as depicted below.



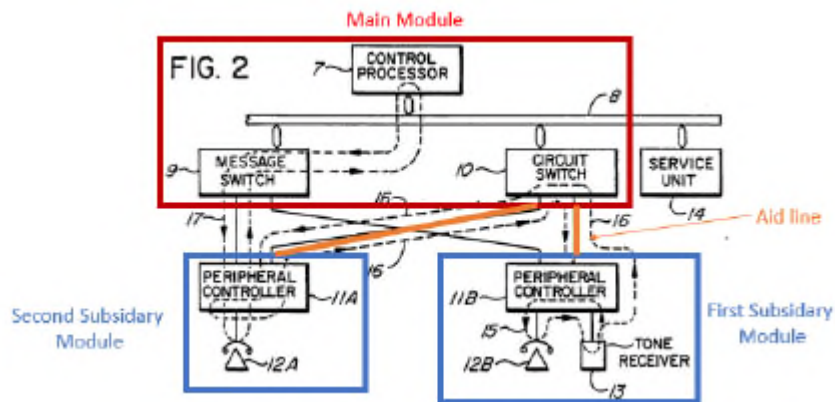
EX1008, Fig. 1.

As described in 1[pre], moreover, the modules in Ke are connected via a port, so a POSITA would have understood that the first subsidiary module is connected to a port in the main module; that is how connections between the modules are made in the backplane in Ke. EX1003, ¶¶94-96. Alternatively, it would have been obvious to a POSITA that the module could have been connected to the main module via a port. *Id.*¶95.

6. Claim 1[b]:

Ke-Lewis discloses 1[b]. Lewis discloses that the control processor of the main module sets up a communication loop between the first and second subsidiary modules. EX1009, 4:42-54. A POSITA would have understood that this requires instructing the first subsidiary module to loop back traffic it receives back to the circuit switch in the main module. EX1003, ¶97. Indeed, a POSITA would have

understood that the first subsidiary module must be instructed to loop back the traffic or else the traffic would not be returned as described in Lewis: “the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface.” EX1009, 4:42-49; EX1003, ¶97.



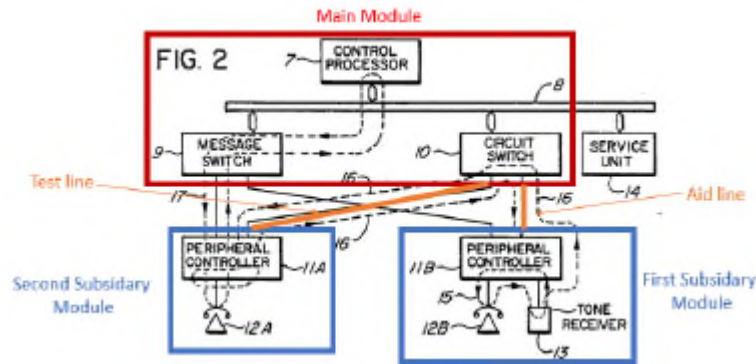
EX1009, Fig. 2.

Alternatively, it would have been obvious to a POSITA the main module would instruct the subsidiary module to loop back traffic so that traffic is, in fact, looped back. *Id.* ¶97.

7. Claim 1[c]:

Ke-Lewis discloses 1[c]. When the system sets up the loop back as described in 1[a], the system also selects a line between the second subsidiary module and the

circuit switch of the main module for testing (“test line”). EX1009, 4:42-54 (disclosing “[a] test tone signal is injected into the loop by service unit 14.”).



Id., Fig. 2.

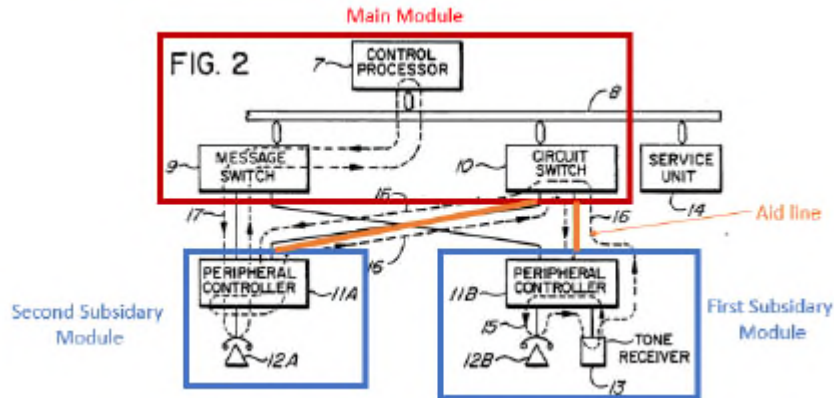
For the same reasons in 1[a], a POSITA would have understood or found it obvious that the second subsidiary module is connected via a port to the circuit switch. EX1003, ¶¶99-101.

8. Claim 1[d]:

Ke-Lewis discloses 1[d]. A POSITA would have understood that, when the loop back is set up as described in 1[a] to 1[c], the circuit switch is configured to link the first and second ports to form the loop back circuit. *Id.*, ¶103.

For example, a POSITA would have understood that the switch must be configured to link the ports that would set up the loop as described in Lewis: “the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16

from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface.” *Id.*, 4:42-49.



Id., Fig. 2.

Alternatively, it would have been obvious to a POSITA that the main module in Ke would link the first and second ports to close the loop between the subsidiary modules. EX1003, ¶¶102-103.

9. Claim 1[e]:

Ke-Lewis discloses 1[e]. Lewis discloses sending a test message over the test line from the second subsidiary module to the circuit switch and that the circuit switch then sends the test message to the first subsidiary module over the aid line. EX1009, 4:42-54. Ke similarly discloses sending test data to subsidiary modules. EX1008, 3:61-4:40. A POSITA therefore would have found it obvious that Ke-Lewis discloses this limitation. EX1003, ¶¶105-106.

10. Claim 1[f]:

Ke-Lewis discloses 1[f]. Lewis discloses that the main module acknowledges receiving the return signal if the test message returns successfully. EX1009, 14:3-11. A POSITA would have understood that, if the main module did not receive the test message from the second subsidiary module within a predetermined period of time, it would have reported the failure by logging the error or notifying the user. EX1003, ¶107. This is the normal way errors are handled when test packets are sent. For example, since the 1980s, every POSITA would be familiar with the ping command, which sends out a test packet and will wait to receive a response or time out if a response is not received. *Id.*, ¶¶107-108; EX1012, 52-58 (describing timeouts in ICMP); EX1013, 549.

At minimum, it would have been obvious to a POSITA for an error to be reported if a response to a test packet was not received for the same reasons. EX1003, ¶¶109-110.

11. Claim 2:

Ke-Lewis discloses claim 2 for the same reasons as claim 1[b]. Lewis discloses that the message just passes through the loop and back to the main module. EX1009, 4:49-54; *see also id.*, 4:35-41. A POSITA would have understood that this means it went through the first subsidiary module without substantial processing of the test traffic since it is simply “passed through the loop.” EX1003, ¶¶111-112.

12. Claim 3:

Ke-Lewis discloses claim 3. EX1003, ¶¶113-116; see Claim 2. Ke discloses that messages are sent via protocols communicated over the bus and that test vector data is specifically loaded into the message for test traffic transmitted to the subsidiary modules (second format). EX1008, 3:30-37. A POSITA would have understood that a different format of message (without the test vector data) would have been used for normal messages (first format). EX1003, ¶113. In sum, Ke explicitly discloses that the first and second subsidiary modules are configured to transmit and receive data in different formats, including a second format for test traffic. Alternatively, it would have been obvious to a POSITA that the subsidiary modules would need to send and receive data in multiple formats because different messages passed between the modules in Ke may require different information and would have been organized differently in a different format. *Id.*, ¶114.

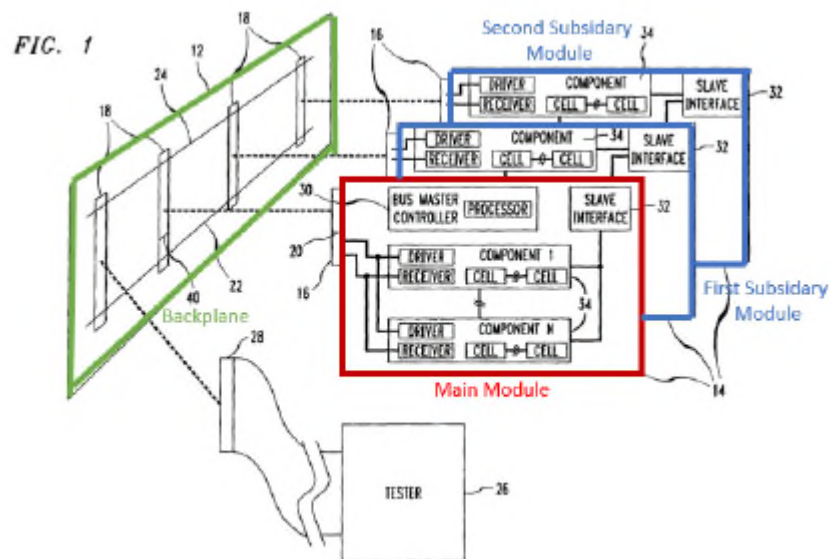
13. Claim 4:

Ke-Lewis discloses claim 4 for the same reasons as it discloses claims 1[a] and 1[c]. Lewis also discloses that “local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system.” EX1009, 4:23–25. Lewis also provides multiple exemplary loops created for testing. EX1009, 4:25-41, 4:43-54. Noting that “[i]n a similar manner other forms of loops can be set up and tested.” EX1009, 4:49-50. Lewis advises that “[t]esting is also preferred to be performed during times when the switches or links are idle.” EX1009, 2:19-20. It

would have been obvious to a POSITA that the same process for choosing idle lines could be repeated after the test is done and that the test should be repeated until all the idle lines have been tested. EX1003, ¶117. Indeed, a POSITA would have known how to create a loop in the testing logic to simply run the test multiple times until all idle lines are tested. *Id.* A POSITA would have been motivated to do so to make sure all idle lines are still working. *Id.*

14. Claim 5:

Ke-Lewis discloses claim 5. As detailed for 1[pre], Ke discloses a card with the bus master controller 30 (main module) and at least two other cards (first and second subsidiary modules). The main module and subsidiary modules are connected by a backplane 12 with traces thereon. EX1008, 3:16-23, 5:4-9.



EX1008, Fig. 1; EX1003, ¶119.

A POSITA would have understood that Ke discloses that the modules are plugged into the backplane because that is how cards are connected to a backplane. EX1003, ¶120. Furthermore, Ke states that the cards may be “misplugged” into the backplane, which implies they are plugged into the backplane. EX1008, 1:23-32; EX1003, ¶120.

15. Claim 6:

Ke-Lewis discloses claim 6. Although Ke does not explicitly discuss the types of electrical systems to which it may be associated, a POSITA would have understood that one such electrical system that commonly used backplanes would have been a network switch or other type of network device. EX1003, ¶¶122-123. A POSITA would have further understood one of the cards inserted into the backplane, like the main module, would have a connection to the broader internet, and other modules could connect to the internet through that network trunk. *Id.*, ¶¶124-127.

16. Claim 7:

Ke-Lewis discloses claim 7. Lewis discloses only sending the test messages after the link is determined to be idle. EX1009, 2:19-20, 14:30-34. A POSITA would have understood that the test is therefore conducted on idle lines while other lines that are not idle continued to be used for carrying normal data. EX1003, ¶¶128, 130.

Although Ke suggests temporarily disabling boards that are not currently being tested (EX1008, 3:61-67), the loop back test from Lewis would not have required disabling the other boards because the loop back would narrowly target certain cards. EX1003, ¶129.

**17. Claim 8

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[pre]
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Ke-Lewis discloses 8

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[pre]
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 for the same reasons as 1

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[pre]
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. *Id.*, ¶131.

18. Claim 8[a]:

Ke-Lewis discloses 8[a] for the same reasons as 1[a], 1[c], and claim 3. *Id.*, ¶132. Ke-Lewis further discloses that the first and second subsidiary modules are different types because Ke discloses that each of the cards connected could be different types (e.g., memory, input-output). EX1008, 1:65-67. Lewis likewise discloses different types of modules. EX1009, 4:23-54, Fig. 2. A POSITA therefore would have understood that the first and second modules could be different types of modules. EX1003, ¶133.

19. Claim 8[b]:

Ke-Lewis discloses 8[b] for the same reasons as 1[b]. *Id.*, ¶134.

20. Claim 8[c]:

Ke-Lewis discloses 8[c] for the same reasons as 1[c], 1[d], and 1[e]. *Id.*, ¶135.

21. Claim 8[d]:

Ke-Lewis discloses 8[d] for the same reasons as 1[e], 1[f] and claim 3. *Id.*, ¶136. Lewis discloses that the main module acknowledges receiving the return

signal if the test message returns successfully. EX1009, 14:3-25. A POSITA would understand that the main module would make sure that the test message returned intact before it acknowledged a receipt because the test would not be “successful[]” if the message did not return intact or did not return. EX1003, ¶¶136-137.

22. Claim 9:

Ke-Lewis discloses claim 9 for the same reasons as claim 2. *Id.*, ¶138.

23. Claim 10:

Ke-Lewis discloses claim 10 for the same reasons as claim 5. *Id.*, ¶139.

24. Claim 11:

Ke-Lewis discloses claim 11 for the same reasons as claim 6 and 1[d]. *Id.*, ¶140. A POSITA would understand that, by linking the first and second ports, the switch is connecting lines of the first and second subsidiary modules. *Id.* At minimum, it would have been obvious to a POSITA that the switch could connect the lines of the first and second subsidiary modules so they can send the test traffic to each other. *Id.*

25. Claim 12:

Ke-Lewis discloses claim 12 for the same reasons as claim 7. *Id.*, ¶142.

26. Claim 13:

Ke-Lewis discloses claim 13 for the same reasons as claim 3. *Id.*, ¶143. It would have been obvious to a POSITA that the test traffic in the second format could have used a different protocol than normal traffic, which would result in different

protocols because the test traffic is handled by the modules differently than normal traffic, and therefore a POSITA would have been motivated to use a different protocol so the module knows how to handle the test traffic. *Id.* ¶¶143-148.

27. Claim 14:

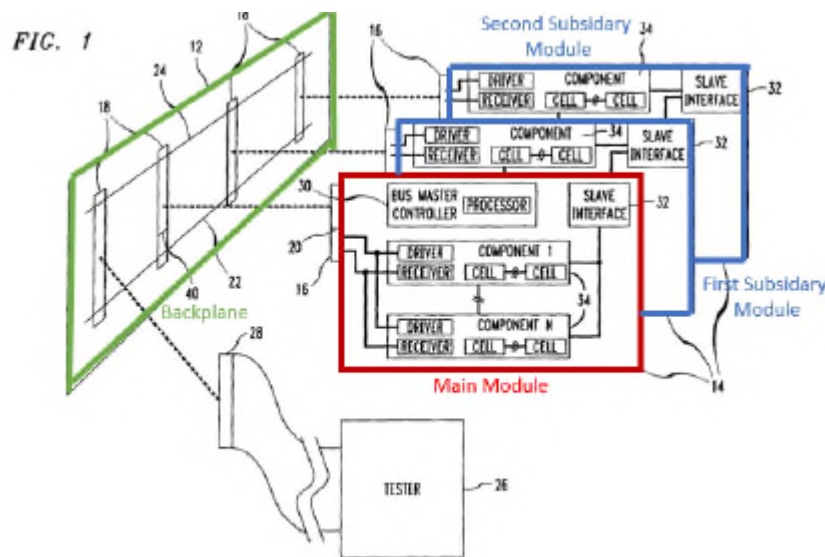
Ke-Lewis discloses claim 14. *Id.*, ¶¶149-154. Lewis discloses a time division switching network and the use of a TDM protocol. *Id.*, ¶¶150-151. It would have been obvious to a POSITA that multiple different protocols could be used by the first and second modules, including TDM protocols and packet data protocols. *Id.*, ¶152. For example, a POSITA would have recognized that a module could use a TDM protocol for communications with other modules and a packet data protocol to communicate with other devices over a network. EX1013, 236; EX1003, ¶152. A POSITA would have understood that a packet data protocol is used to communicate over an IP-based network. EX1003, ¶152.

Ke discloses a system that provides “communication pathways for data and control signals between boards 14.” EX1008, 3:22-23. Ke also discloses that “[v]arious data structures may be used to define the configuration of the system 10 prior to performing a walking enable test.” EX1008, 4:66-5:1. Ke also uses the term “network” to describe the system being tested. EX1008, 2:63-67. A POSITA would consider the term “network” to suggest a system that uses data packet for transmission. EX1003, ¶153. Data sent through networks are usually sent in packets

and as Ke notes various protocols can be used for enabling the testing functionality. EX1003, ¶153. A POSITA would thus consider a packet data protocol in the Ke-Lewis combination. EX1003, ¶153. Thus, it would be an obvious implementation choice for one protocol to be TDM and another to be a packet data protocol. *Id.*

28. Claim 15[pre]:

To the extent the preamble is limiting, Ke-Lewis render obvious 15[pre]. Ke discloses an electronic apparatus, comprising a backplane into which multiple cards may be plugged. EX1008, 2:55-56, Fig.1. A POSITA would have understood that the cards can be inserted and removed in a modular fashion, making the disclosure in Ke a modular electronic apparatus. EX1003, ¶¶155-156.



29. Claim 15[a]:

Ke-Lewis discloses 15[a] for the same reasons as claim 5. *Id.*, ¶157.

30. Claim 15[b]:

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of U.S. Patent No. 6,957,369*

¶158.

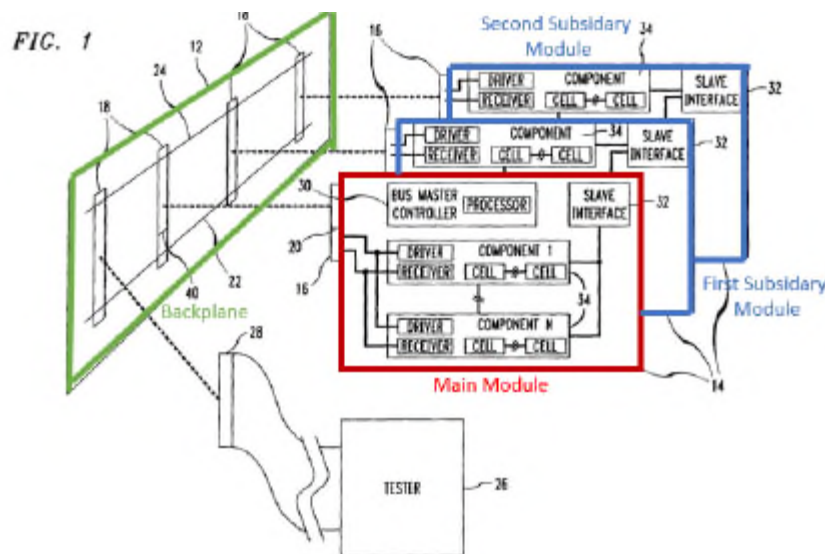
31. Claim 15[c]:

Ke-Lewis discloses 15[c] for the same reasons as 1[pre] and claim 5. *Id.*,

¶159.

32. Claim 15[d]:

Ke-Lewis discloses 15[d] for the same reasons as 1[a]. *Id.*, ¶¶160-161. Ke further discloses a processor as part of the master controller in the main module that controls the testing. EX1008, Fig.1; EX1003, ¶160.



33. Claim 15[e]:

Ke-Lewis discloses 15[e] for the same reasons as 1[b]. EX1003, ¶162.

34. Claim 15[f]:

Ke-Lewis discloses 15[f] for the same reasons as 1[c]. *Id.*, ¶163.

35. Claim 15[g]:

Ke-Lewis discloses 15[g] for the same reasons as 1[d]. *Id.*, ¶164.

36. Claim 15[h]:

Ke-Lewis discloses 15[h] for the same reasons as 1[e]. *Id.*, ¶165.

37. Claim 15[i]:

Ke-Lewis discloses 15[i] for the same reasons as 1[f]. *Id.*, ¶166.

38. Claim 16

See Claim 2; *see also* EX1003, ¶167.

39. Claim 17

See Claim 3; *see also* EX1003, ¶168.

40. Claim 18

See Claim 4; *see also* EX1003, ¶169.

41. Claim 19

See Claim 6; *see also* EX1003, ¶170.

42. Claim 20

See Claim 7; *see also* EX1003, ¶171.

43. Claim 21[pre]:

See Claim 15[pre]; *see also* EX1003, ¶172.

44. Claim 21[a]:

See Claim 15[a]; *see also* EX1003, ¶173.

45. Claim 21[b]:

See Claim 15[b]; *see also* EX1003, ¶174.

46. Claim 21[c]:

See Claim 15[c]; *see also* EX1003, ¶175.

47. Claim 21[d]:

See Claims 8[a] and 15[d]-15[i]; *see also* EX1003, ¶176.

48. Claim 22

See Claim 2; *see also* EX1003, ¶177.

49. Claim 23

See Claim 11; *see also* EX1003, ¶178.

50. Claim 24

See Claim 12; *see also* EX1003, ¶179.

51. Claim 25

See Claim 13; *see also* EX1003, ¶180.

52. Claim 26

See Claim 14; *see also* EX1003, ¶181.

**B. Ground 2: Ke in View of Lewis and Sarkinen Renders Obvious
Claims 3, 6, 8, 13, 14, 17, 21, 25, and 26**

To the extent the additional limitations of claims 3, 6, 8 13, 14, 17, 21, 25, and 26 are not rendered obvious by Ke-Lewis, it would have been obvious to combine Ke and Lewis with Sarkinen.

1. Sarkinen

Sarkinen discloses a system and method for isolating network switching/routing interface functions through the use of standards. Ex. 1011, ¶11; *see also* EX1033, ¶¶ 65-67. Embodiments of the inventions disclosed include a network switch or router that utilizes a backplane with multiple line and fabric cards

connected thereto. EX1011, ¶12; *see also Id.* ¶¶64-66. For example, Figure 3 depicts a fabric interface (316), multiple line cards (304, 306), and fabric cards (310, 312) all plugged into a midplane 314. EX1011, ¶55.

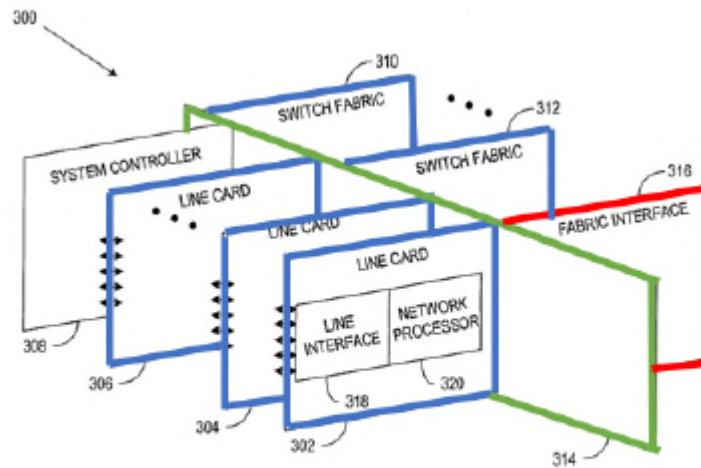


FIG. 3

EX1011, Fig. 3.

Sarkinen makes clear that the midplane can also be implemented as a backplane. *Id.*, ¶¶12, 54. Sarkinen discloses that the system may include a traffic manager to support multiple standards Ex. 1011, ¶15. The system also includes fabric processors that can convert data from one format to another to distribute the data over the fabric interface. Ex. 1011, ¶49.

2. Motivations to Combine Ke, Lewis and Sarkinen

It would have been obvious to a POSITA to combine Sarkinen with Ke in view of Lewis.⁴ A POSITA looking to expand on the formats available in the Ke-Lewis combination would have looked to Sarkinen because it shares a similar architecture as the Ke-Lewis combination and enables the use of different formats through the use of its fabric and traffic manager. EX1003, ¶183. Sarkinen discloses one type of network switch with backplane architecture, similar to that in the Ke-Lewis combination, to which the loop back testing system available in the Ke-Lewis combination could apply. EX1003, ¶183. Sarkinen also discloses that the invention enables “[u]sing [a line-to-switch] interface and isolating such an interface in accordance with the invention, routers and switches can provide multiple service classes, efficiently handle multicast traffic, and instantaneously direct the flow of traffic to other ports should there be a failure on a link.” EX1011, ¶58. The Ke-Lewis combined system would be a backplane system with subsidiary modules able to implement loop back testing to test specific links, traces or lines. A POSITA would have been motivated to apply the testing from Ke and Lewis (a backplane system implementing loop back testing to test specific links, traces or lines connecting subsidiary modules) to ensure that the line cards traces, or links of

⁴ This combination does not alter the combination discussed in Ground 1. Claims discussed under this combination continue to map to the Ground 1 claims of relevance for the reasons explained in those sections.

Sarkinen were functioning properly and to know the links available to which traffic could be instantaneously directed to in the event of a failure on a link. EX1003, ¶183. A POSITA would have understood that the fabric interface would act as a switch to help address traffic of different formats between the line cards and that the fabric interface would operate in between the line cards and could set up the paths between the line cards as shown in Figure 4.

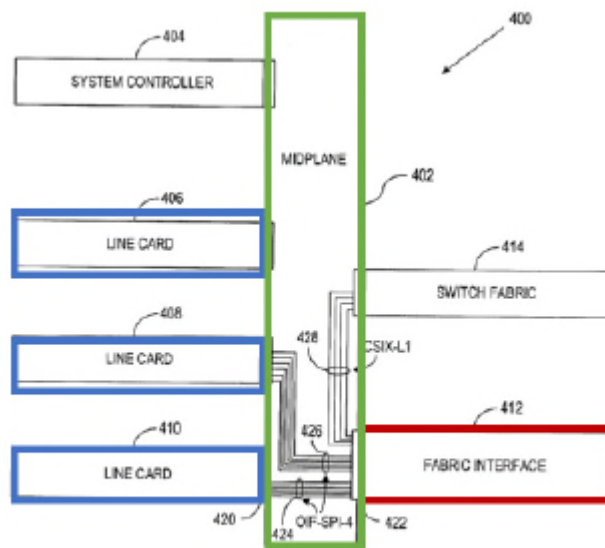


FIG. 4

3. Claim 6

The architecture of the Ke-Lewis system is similar to the architecture of the embodiments disclosed by Sarkinen. Sarkinen discloses a backplane device, such as a network switch or router, with **line cards and fabric cards (subsidiary modules)** controlled by a **fabric interface (main module)**, all of which are plugged into a **backplane or midplane 314**. Sarkinen further makes it clear that the line cards

include a network line interface, which plugs into a network link or trunk to a broader network. *Id.*, ¶13. Sarkinen also discloses that the invention relates generally to “communication networks.” *Id.*, ¶3. It also notes that one standard that can be utilized in implementing the invention is the “CSIX-L1 standard which defines an interface between a network processor (e.g., traffic manager, or any processor used for packetized information) and a switch fabric in data communications applications.” *Id.*, ¶¶ 66, 106. A POSITA looking to expand the formats supported by the Ke-Lewis combination, would have combined Ke-Lewis with Sarkinen. EX1003, ¶186. A POSITA would have understood that for the combined system traffic transmitted over the line cards and fabric cards is communication traffic for routing over the network to which the switch/router is connected. EX1003, ¶¶184-187.

4. Claims 3, 8, 13, 14, 17, 21, 25, and 26

Claims 3, 8, 13, 14, 17, 21, 25, and 26 further recite that the subsidiary modules transmit and receive data in at least two different formats. To the extent Ke-Lewis does not render obvious this limitation, it would have been obvious to combine Sarkinen with Ke-Lewis because Sarkinen is an example of a network switch with the backplane architecture disclosed in Ke as set forth above. EX1003, ¶189. Sarkinen makes clear that the switch may support multiple protocols and multiple data formats. EX1011, ¶¶49, 58, 66. A POSITA would have understood

that, for example, each line card may support a different protocol and that each protocol would have a different format associated with the protocol. EX1003, ¶189. Sarkinen discloses that protocols and formats are typically defined by a standard. EX1011, ¶¶ 47, 69; EX1003, ¶190. It would have been obvious to a POSITA that the different line cards that support different protocols may support data in different formats. EX1003, ¶191. Sarkinen also discloses the use of a traffic manager for different formats. EX1011, ¶68. Sarkinen also discloses the use of a fabric processor to manage traffic of different formats across line cards. *Id.*, ¶49. It also would have been obvious to a POSITA that the subsidiary modules would have had to have chosen a common data format to communicate a test message, and it would have been obvious to choose one of the data formats already in use by the line card. EX1003, ¶191.

5. Claims 13 and 25

Claims 13 and 25 further recite that the different formats are determined by different protocols. The combination of Ke-Lewis and Sarkinen would do this because Sarkinen's fabric processor 220 converts the data stream from one format to another, such as from POS frames to Common Switch Interface (CSIX) cells, and distributes the cells over the switch fabric, and would continue to perform this functionality when implementing the Ke-Lewis techniques. EX1011, ¶49. Sarkinen also discloses that "the CSIX-L1 specification defines an interface between a traffic

manager and a switch fabric for data communication applications, and specifies certain data formats.” *Id.*, ¶66. The combination thus discloses different formats determined by the different standards supported by the switches, or multiple line card system. EX1003, ¶¶188-191, 192.

6. Claims 14 and 26

Claims 14 and 26 recite that one protocol is a TDM protocol and the other is a packet data protocol. Sarkinen discloses the use of “Packet-Over-SONET/SDH (POS) frames” which is “known in the art, [as] a high-speed time division multiplexing (TDM) physical-layer transport technology.” EX1011, ¶47. Sarkinen also discloses that “[t]ypically, the data packet stream is converted to a particular format, such as converted to comply with the CSIX standard.” *Id.*, ¶69. A POSITA would have been familiar with both TDM protocols and packet data protocols and would have understood Sarkinen disclosed the use of a TDM and packet data protocol, and would continue to perform this functionality in the combination with Ke-Lewis. EX1003, ¶¶ 188-191, 193-194.

C. Ground 3: Cook in View of Lewis Renders Obvious the Challenged Claims

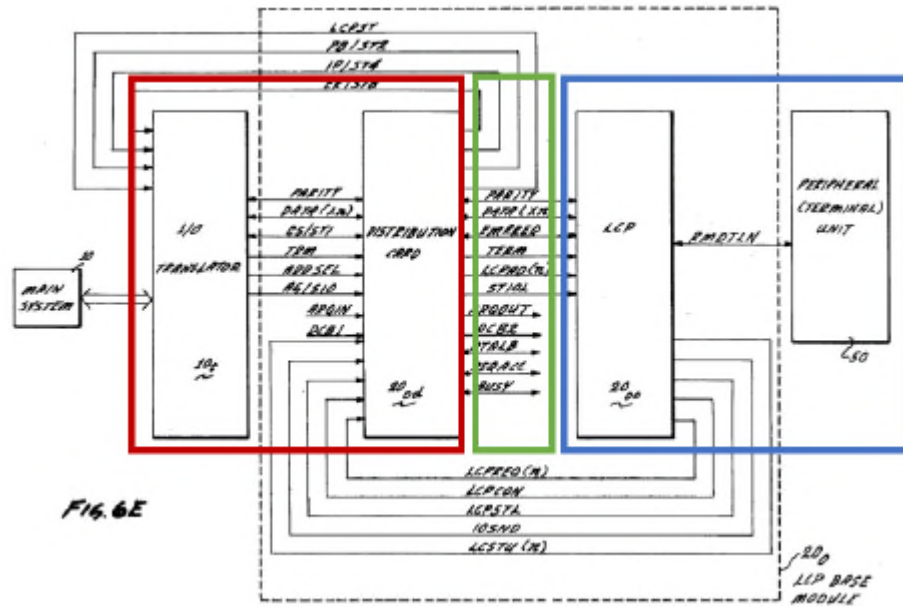
The combination of Cook and Lewis (“Cook-Lewis”) renders obvious claims 1-26 of the ’369 Patent.

1. Cook

Cook discloses a computer system with multiple “line control processors” (“LCPs”) that are connected to each other via a “backplane.” EX1010, 4:39-45, 28:62-29:7. According to Cook, the LCPs are organized into groups of eight to form an LCP Base Module (“LCPBM”). *Id.*, 4:39-5:10. Cook explains that each LCPBM also has a “distribution card unit” (“DCU”) that interfaces with the Input-Output Translator (“IOT”). *Id.* 5:5-10, 5:20-31. The DCU and IOT send to and receive data from the peripheral devices connected to the LCPs. *Id.* Figure 2 depicts this structure:



The LCPs, each of which has an associated peripheral device, are connected to each other and the distribution card unit via a backplane. *Id.*, 28:62-29:7. Figure 6E depicts this same structure in a slightly different way, showing that the backplane connects each LCP/peripheral with the DCU and IOT.

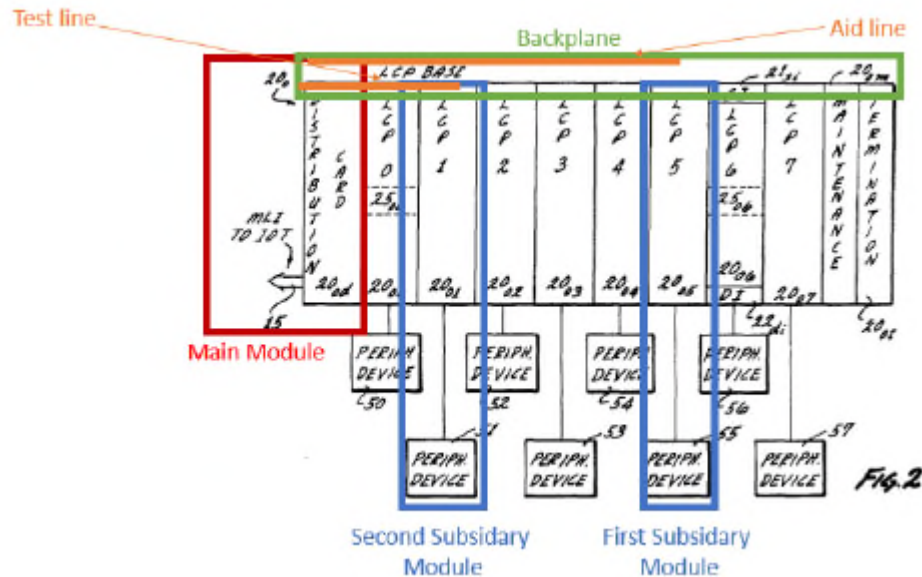


Id., Fig. 6E.

Cook further discloses that the DCU, in connection with the IOT, acts as a switch by sending and receiving messages with each of the LCPs using a specific address. *Id.*, 31:63-32:47; EX1003, ¶¶61-64. Cook also discloses using a “poll test” to establish a connection between the DCU on the LCPBM and the LCPs. The poll test identifies errors or indicates the port is busy. EX1010, 23:43-24:27.

2. Motivations to Combine Cook and Lewis

A POSITA would have been motivated to combine the backplane testing described in Cook with the loop back testing described in Lewis as depicted below.



EX1010, Fig. 2.

The main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as disclosed in Lewis. The backplane modules in Cook would then perform the loop back test described in Lewis set forth above, where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines. EX1009, 4:42-54. This combination would have been obvious to a POSITA for multiple reasons.

First, both references are generally directed to testing connections within a system with multiple components. Cook recites a DCU coupled to the IOT that directs traffic to the LCPs plugged into a backplane as the DCU. EX1010, 28:62-29:7. Lewis recites a similar set up where the control processor/circuit switch directs the testing of peripheral controllers. EX1009, 3:47-60. A POSITA would have been motivated to combine the testing protocol in Lewis with the structure disclosed in

Cook because a POSITA would have understood the benefits of a loop back test in the context of a backplane with a DCU. EX1003, ¶¶196-197.

Second, Cook makes clear that there are many different types of peripheral devices that can be added to the LCPs, including “card readers, magnetic tape units, card punches, printers, disk files, supervisory terminals, and so on”. EX1010, 1:47-49. A POSITA would have understood that the testing configurations must be adaptable and flexible. EX1003, ¶197. A POSITA therefore would have been motivated to look at other testing configurations, like the one disclosed in Lewis for the creation of a loop back test. EX1003, ¶197. It would have been obvious to a POSITA that testing in a backplane could benefit from such a loop back test because there are times when the different boards in a backplane need to communicate with each other. EX1003, ¶198. A POSITA would have recognized that there are times when data needs to be transferred to and from different boards on the backplane, e.g., from a storage unit to a printer. As Cook explained, moreover, it was desirable to take the load off of the processing unit and main memory, which is accomplished by the DCU and IOT handling messages between peripherals. EX1010, 1:22-31. A POSITA therefore would have been motivated to apply the loop back testing between two peripherals in Lewis to the peripherals in Cook to test the connection between two peripherals connected via the backplane in Cook. EX1003, ¶198.

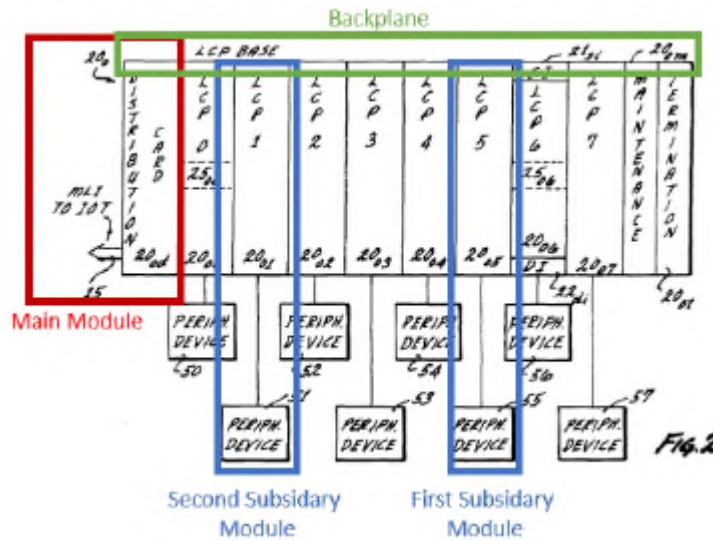
Third, a POSITA would have been motivated to test the backplane lines while they were idle as disclosed in Lewis. EX1009, 2:19-26, 4:23-25. As Cook explains, connections may not be made to LCPs when they are busy. EX1010, 23:61-24:27. A POSITA would understand that the best time to disable those parts and perform the test is when the lines are otherwise idle because that would avoid disrupting traffic when the lines were in use. EX1003, ¶200.

Reasonable expectation of success. A POSITA would have had a reasonable expectation of success to implement the testing in Lewis to the backplane structure from Cook. Cook happens to disclose a “poll test,” EX1010, 23:42-24:27, but, also discloses the use the process by which Test instructions can be received. EX1010, 52:15-30. This indicates that tests are interchangeable. A POSITA would therefore have a reasonable expectation of success to apply a different type of testing technique. EX1003, ¶201. Furthermore, Cook explains that the DCU and IOT control the communications and addressing to the individual LCPs. EX1010, 31:63-32:41. A POSITA would have therefore understood that the loop back testing between specific peripherals in Lewis could be employed in Cook by using the DCU to control testing between specific LCPs, including two LCPs within a single LCPBM in which case data need not even go to the IOT. EX1003, ¶¶201-203.

3. Claim 1[pre]:

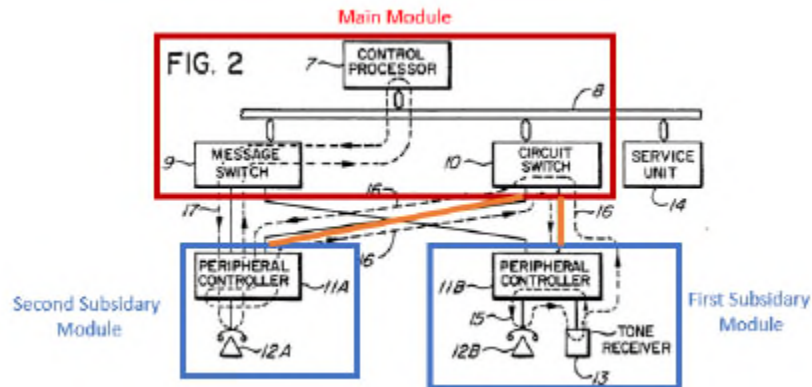
To the extent the preamble is limiting, Cook-Lewis render obvious 1[pre].

Cook discloses a digital computing system (*electronic system*) with a DCU (connected to an IOT) (main module) and up to eight LCPs (subsidiary modules) connected by lines in a backplane in the LCPBM. EX1010, Fig.2; EX1003, ¶205.



EX1010, Fig. 2.

This same basic structure from Cook is mirrored in Lewis, and it would have been obvious to combine Cook with Lewis as set forth above. EX1003, ¶¶205-206. Like Cook, Lewis describes a circuit switch 10—which communicates with a control processor 7 and message switch 9—(main module) that can set up a communication loop for testing the connection with peripherals 12A (second subsidiary module) and 13 (first subsidiary module). EX1009, 3:47-60.



EX1009, Fig. 2.

Cook recognizes that there are times when the backplane is “inactive” or idle and discloses that the inactivity may be detected by the system. EX1010, 52:48-61. Lewis makes clear that there are times when the lines or connections are idle, and that testing should be done when they are not in use. EX1009, 2:19-20. Alternatively, it would have been obvious to a POSITA that the lines in the backplane would sometimes be idle or not in use. EX1003, ¶207. It also would have been obvious to a POSITA to combine Cook with Lewis for the reasons disclosed above. *Id.*

Cook discloses that the main module (DCU and IOT) acts as the switch by driving the poll test and also addressing the data to the different LCPs. EX1010, 31:63-32:41; EX1003, ¶209. Cook discloses that the LCPs and DCU are connected to the backplane and further characterizes that connection as a “port.” EX1010, 28:62-29:7. A POSITA would have understood that the connections with the

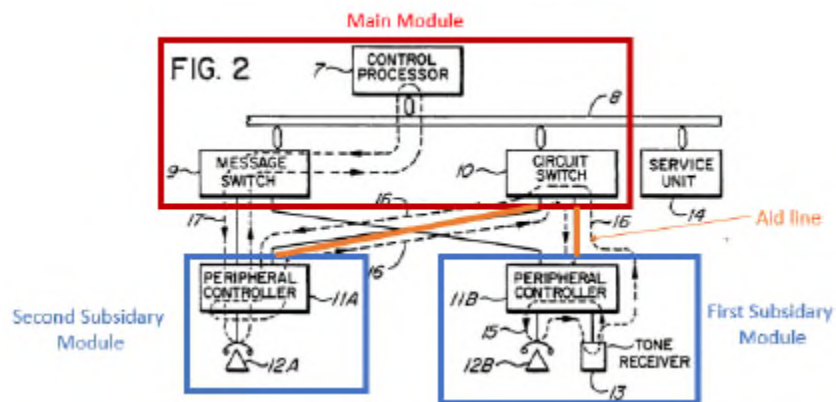
backplane act as the interconnect or port between the card and the backplane.

EX1003, ¶¶209-210.

Cook further discloses the DCU performing a “poll test” on the LCPs.
EX1010, 23:43-24:27.

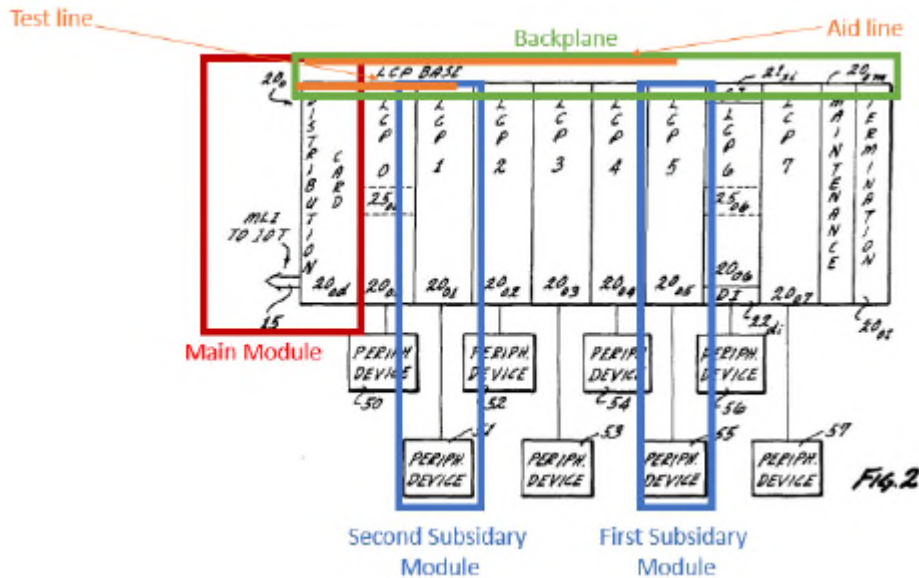
4. Claim 1[a]:

Cook-Lewis discloses 1[a]. Lewis discloses setting up a loop back test when the lines are idle. EX1009, 2:19-20. When the lines are idle, the system sets up a loop back circuit by choosing an aid line between the first subsidiary module and the circuit switch in the main module. *Id.*, 4:42-54.



EX1009, Fig. 2.

This same set up is mirrored by the structure in Cook as depicted below.



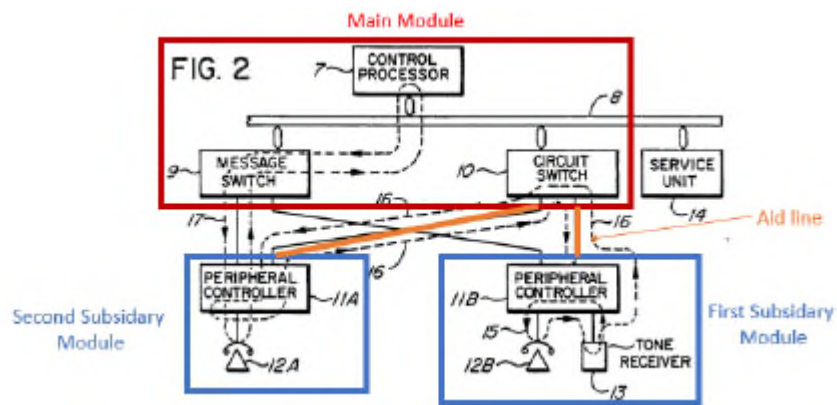
EX1010, Fig. 2; EX1003, ¶212.

A POSITA would have understood that the first subsidiary module is connected to the circuit switch via a port, which is how connections between the switch and the peripherals would have been made. EX1003, ¶¶212-213. Alternatively, it would have been obvious to a POSITA that the peripherals could have been connected to the switch via a port. *Id.*

5. Claim 1[b]:

Cook-Lewis discloses 1[b]. Lewis discloses that the control processor of the main module sets up a communication loop between the first and second subsidiary modules. EX1009, 4:42-54. A POSITA would have understood that this requires instructing the first subsidiary module to loop back traffic it receives back to the circuit switch in the main module. EX1003, ¶¶214-215. Indeed, a POSITA would have understood that the first subsidiary module must be instructed to loop back the

traffic or else the traffic would not be returned as described in Lewis: “the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface.” EX1009, 4:42-49.

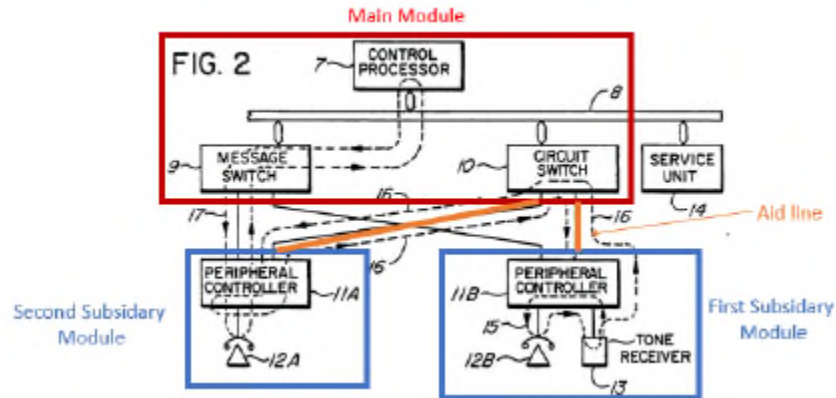


Id., Fig. 2.

Alternatively, it would have been obvious to a POSITA that the instruction to loop back must have occurred because Lewis discloses that traffic is looped back from the first subsidiary module to the main module. EX1003, ¶214.

6. Claim 1[c]:

Cook-Lewis discloses 1[c]. When the system sets up the loop back as described in 1[a], the system also selects a line between the second subsidiary module and the circuit switch of the main module for testing (“test line”). EX1009, 4:42-54.



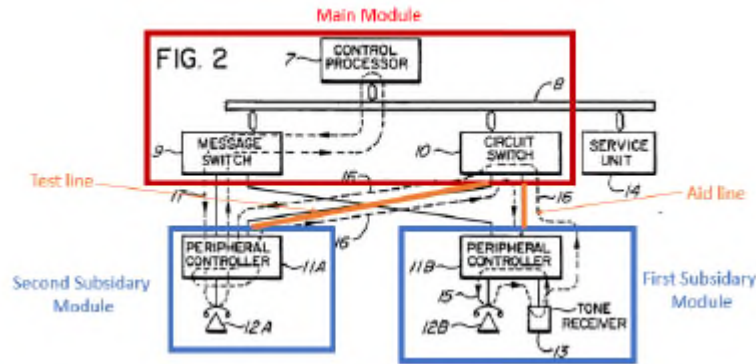
Id., Fig. 2.

For the same reasons in 1[a], a POSITA would have understood or found it obvious that the second subsidiary module is connected via a port to the circuit switch. EX1003, ¶¶216-219. Cook also discloses that “[t]he Distribution Card also works on conjunction with the IOT Connection Module 10tb to establish a data path to a specified LCP.” EX1010, 28:36-38; EX1003, ¶218

7. Claim 1[d]:

Cook-Lewis discloses 1[d]. A POSITA would have understood that, when the loop back is set up as described in 1[a] and 1[c], the circuit switch is configured to link the first and second ports to form the loop back circuit. *Id.*, ¶¶220-221. For example, a POSITA would have understood that the switch must be configured to link the ports that would set up the loop as described in Lewis: “the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a

peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface.” EX1009, 4:42-49.



Id., Fig. 2.

Alternatively, it would have been obvious to a POSITA that the circuit switch could link the first and second ports to form that circuit. EX1003, ¶¶220-221.

8. Claim 1[e]:

Cook-Lewis discloses 1[e]. Lewis discloses sending a test message over the test line from the second subsidiary module to the circuit switch and that the circuit switch then sends the test message to the first subsidiary module over the aid line. EX1009, 4:42-54; EX1003, ¶¶222-223.

9. Claim 1[f]:

Cook-Lewis discloses 1[f]. Lewis discloses that the main module acknowledges receiving the return signal if the test message returns successfully. EX1009, 14:3-11. A POSITA would have understood that, if the main module did not receive the test message from the second subsidiary module within a predetermined period of time, it would have reported the failure by logging the error

or notifying the user. EX1003, ¶224. This is the normal way errors are handled when test packets are sent. For example, since the 1980s, every POSITA would be familiar with the ping command, which sends out a test packet and will wait to receive a response or time out if a response is not received. *Id.*; EX1012, 52-58 (describing timeouts in ICMP).

At minimum, it would have been obvious to a POSITA for an error to be reported if a response to a test packet is not received within a set time period for the same reasons above. EX1003, ¶¶224-225.

10. Claim 2:

Cook-Lewis discloses claim 2 for the same reasons as 1[b]. Lewis discloses that the message just passes through the loop and back to the main module. EX1009, 4:34-41, 4:43-52. A POSITA would have understood that this means it went through the first subsidiary module without substantial processing of the test traffic since it is simply “passed through the loop.” *Id.*; EX1003, ¶¶226-227.

11. Claim 3:

Cook-Lewis discloses claim 3. EX1003, ¶228; *see* Claim 2. Lewis discloses that “the links are dedicated for each peripheral, the particular scan signal format and peripheral state message signal format can be set to suit the design.” EX1009, 12:18-20; EX1003, ¶228. Lewis further discloses a loop for testing. EX1009, 4:42-54. The loop utilizes a “test message” injecting the “test message into the loop of

lines to be tested. EX1009, 4:34-39, 4:49-54. A “signal” is returned through the loop. *Id.* Lewis distinguishes between a “test tone signal” being used as test traffic and a “test message.” *Id.* A POSITA would understand Lewis as disclosing two different formats for test traffic to be used in the loop for testing. EX1003, ¶229.

Alternatively, it would have been obvious to a POSITA that the subsidiary modules would need to send and receive data in multiple formats because different messages passed between the modules in Cook may require different information and would have been organized differently in a different format. *Id.*, ¶230.

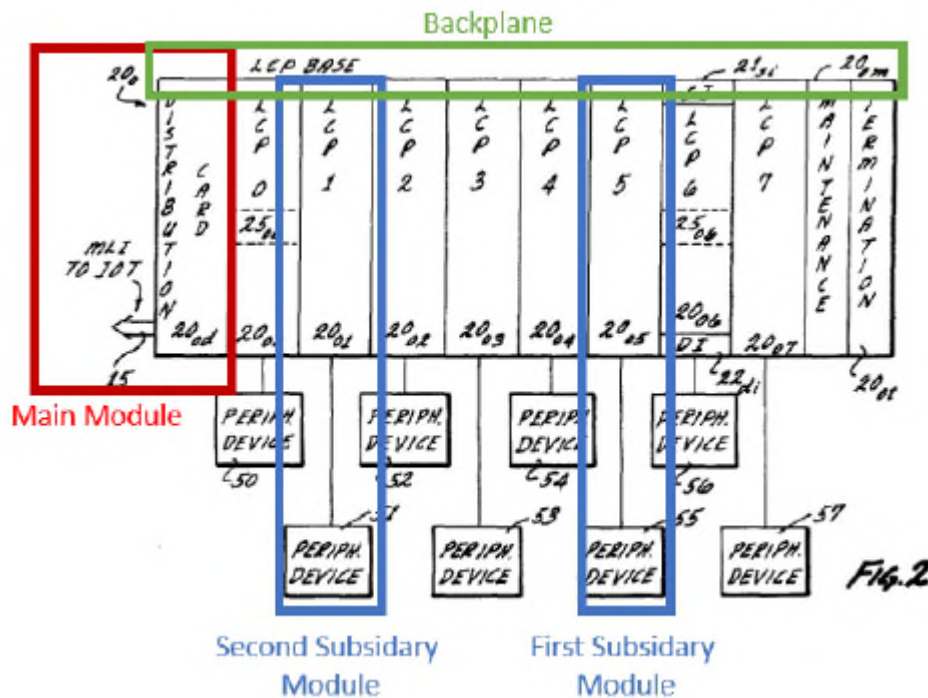
12. Claim 4:

Cook-Lewis discloses claim 4 for the same reasons as it discloses claims 1[a] and 1[c]. Lewis also discloses that “local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system.” EX1009, 4:23–25. Lewis also provides multiple exemplary loops created for testing. EX1009, 4:25-41, 4:43-54. Noting that “[i]n a similar manner other forms of loops can be set up and tested.” EX1009, 4:49-50. It advises that “[t]esting is also preferred to be performed during times when the switches or links are idle.” EX1009, 2:19-20. It would have been obvious to a POSITA that the same process for choosing idle lines could be repeated after the test is done and that the test should be repeated until all the idle lines have been tested. *Id.*, ¶¶ 232-233. Indeed, a POSITA would have known how to create a loop in the testing logic by simply running the test multiple times until all

idle lines are tested. A POSITA would have been motivated to do so to make sure all those lines are still working. *Id.*, ¶¶232-234.

13. Claim 5:

Cook-Lewis discloses claim 5. As detailed for 1[pre], Cook discloses a digital computing system (*electronic system*) with a DCU (connected to an IOT) and up to eight LCPs connected by a backplane in an LCPBM, with backplane lines (traces) thereon. EX1010, 28:62-29:7.



EX1010, Fig.2; EX1003, ¶235.

A POSITA would have understood that Cook discloses that the modules are plugged into the backplane because that is how cards (like the DCU and LCPs) are connected to a backplane. EX1003, ¶¶235-237.

14. Claim 6:

Cook-Lewis discloses claim 6. EX1003, ¶¶238-242. Cook in view of Lewis discloses a switch configured to connect lines to a network communication trunk. Cook discloses that “[t]he units known as Line Control Processors are the devices which establish a communication path from the System (Main Memory and Processor) to a specific peripheral device.” EX1010, 13:8-11; EX1003, ¶241. Lewis discloses that “[a] typical system is formed of a switching network which may have several stages, peripheral interface circuits such as line circuits, trunk circuits, etc. which are connected to the switching network, and a common control.” EX1009, 1:11-15; EX1003, ¶239. Lewis also discloses that “[t]runk circuits are connected in some cases as peripherals or in some cases via a further switching matrix . . .” EX1009, 3:4-6; EX1003, ¶239. The Cook-Lewis combination thus discloses the switching functionality connecting peripherals to a trunk circuit or system. EX1003, ¶242.

Lewis further discloses that the traffic in this system is communication traffic. EX1003, ¶242. It describes the system claimed by Lewis as a “communication circuit system.” EX1009, Abstract; EX1003, ¶240. Lewis discloses a system where “[a]ctual communication signals between peripherals pass through circuits set up via links connected from a peripheral, a peripheral controller, circuit switch 10, a peripheral controller to another peripheral.” EX1009, 4:1-4; EX1003, ¶240.

15. Claim 7:

Cook-Lewis discloses claim 7. Lewis discloses the need to identify the idle paths. EX1009, 14:30-34. Lewis also states that “[t]esting is preferred to be performed during times when the switches or links are idle.” EX1009, 2:19–20. 2:19-20. Cook claims as one of its features, a “means for providing on-line diagnostic signals to any selected line control processor and for simulating the peripheral unit corresponding to each line control processor.” EX1010, Claim 7(e2). Cook highlights the importance of testing while the system is actively in use or on-line. EX1003, ¶245. The teaching of Lewis highlight the need to identify only idle lines so those idle lines can be tested while the rest of the system is on-line. EX1003, ¶245. A POSITA would have understood that the test is therefore conducted on idle lines while other lines that are not idle continue to be used for carrying normal data. EX1003, ¶¶243-245.

**16. Claim 8

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[pre]
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Cook-Lewis discloses 8

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[pre]
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 for the same reasons as 1

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[pre]
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. *Id.*, ¶246.

17. Claim 8[a]:

Cook-Lewis discloses 8[a] for the same reasons as 1[a], 1[c], and claim 3. EX1003, ¶247. Cook-Lewis further discloses the first and second subsidiary modules are different types because Cook discloses that each of the peripherals attached to the LCPs could be different types. EX1010, 1:47-49. Lewis likewise discloses different types of peripherals. EX1009, 4:42-54, Fig. 2. A POSITA

therefore would have understood that the first and second modules could be different types. EX1003, ¶247.

18. Claim 8[b]:

Cook-Lewis discloses 8[b] for the same reasons as 1[b]. *Id.*, ¶248.

19. Claim 8[c]:

Cook-Lewis discloses 8[c] for the same reasons as 1[c], 1[d] and 1[e]. *Id.*, ¶249.

20. Claim 8[d]:

Cook-Lewis discloses 8[d] for the same reasons as 1[e], 1[f] and claim 3. *Id.*, ¶¶250-251. Lewis discloses that the main module acknowledges receiving the return signal if the test message returns successfully. EX1009, 14:3-25. A POSITA would understand that the main module would make sure that the test message returned intact before it acknowledged a receipt because the test would not be “successful[]” if the message did not return intact or did not return. EX1003, ¶¶250-251.

21. Claim 9:

Cook-Lewis discloses claim 9 for the same reasons as claim 2. *Id.*, ¶252.

22. Claim 10:

Cook-Lewis discloses claim 10 for the same reasons as claim 5. *Id.*, ¶253.

23. Claim 11:

Cook-Lewis discloses claim 11 for the same reasons as claim 6 and 1[d]. EX1003, ¶254. A POSITA would understand that, by linking the first and second

ports, the switch is connecting lines of the first and second subsidiary modules. *Id.*, ¶¶254-255. At minimum, it would have been obvious to a POSITA that the switch could connect lines of the first and second subsidiary modules so they can send the test traffic to each other. *Id.*

24. Claim 12:

Cook-Lewis discloses claim 12 for the same reasons as claim 7. *Id.*, ¶256.

25. Claim 13:

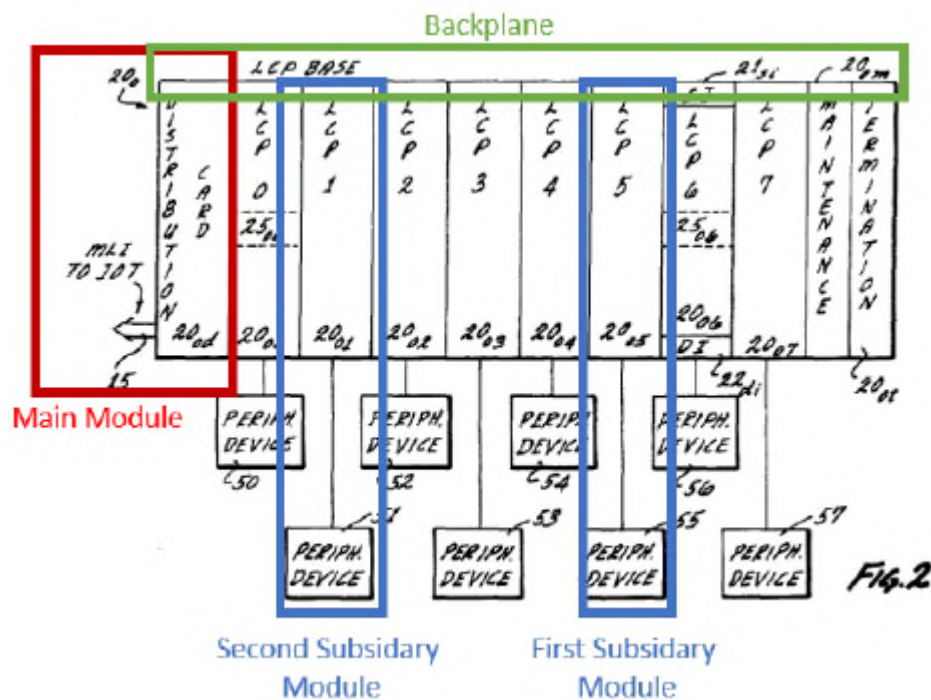
Cook-Lewis discloses claim 13 for the same reasons as claim 3. *Id.*, ¶257. It would have been obvious to a POSITA that the test traffic in the second format could have used a different protocol than normal traffic, which would result in different protocols because the test traffic is handled by the modules differently than normal traffic, and therefore a POSITA would have been motivated to use a different protocol so the module knows how to handle the test traffic. *Id.*, ¶¶257-258.

26. Claim 14:

Cook-Lewis discloses claim 14. EX1003, ¶¶259-263. Lewis discloses “input lines carrying time division multiplexed.” EX1009, 7:5-6; EX1003, ¶261. An embodiment of the system in Lewis to which the loopback testing is applied is “described with reference to a PCM time division multiplex switching network”. EX1009, 3:42-43; EX1003, ¶261. Lewis discloses that “general functions are provided whether the system operates as a space division switching network or as a time division switching network.” EX1009, 1:19-21; EX1003, ¶260.

27. Claim 15[pre]:

To the extent the preamble is limiting, Cook and Lewis render obvious 15[pre]. EX1003, ¶¶264-266. Cook discloses an electronic apparatus, comprising a backplane (LCP Base Module) into which multiple LCPs may be plugged. EX1010, 2:55-56, 5:5-19, 28:61-29:7, Fig. 1. A POSITA would have understood that the cards can be inserted and removed in a modular fashion, making the disclosure in Cook a modular electronic apparatus. EX1003, ¶¶264-265. Indeed, the title of Cook is “Modular block unit for input-output subsystem.” EX1010, ¶54.



EX1010, Fig. 2; EX1003, ¶264.

28. Claim 15[a]:

Cook-Lewis discloses 15[a] for the same reasons as claim 5. EX1003, ¶267.

29. Claim 15[b]:

Cook-Lewis discloses 15[b] for the same reasons as 1[pre] and claim 5. *Id.*, ¶268.

30. Claim 15[c]:

Cook-Lewis discloses 15[c] for the same reasons as 1[pre] and claim 5. *Id.*, ¶269.

31. Claim 15[d]:

Cook-Lewis discloses 15[d] for the same reasons as 1[a]. *Id.*, ¶¶270-271. A POSITA would have understood that the DCU has a processor so that it can process data sent to it and route the data to the correct LCP or to the IOT. *Id.* ¶270.

32. Claim 15[e]:

Cook-Lewis discloses 15[e] for the same reasons as 1[b]. *Id.*, ¶272.

33. Claim 15[f]:

Cook-Lewis discloses 15[f] for the same reasons as 1[c]. *Id.*, ¶273.

34. Claim 15[g]:

Cook-Lewis discloses 15[g] for the same reasons as 1[d]. *Id.*, ¶274.

35. Claim 15[h]:

Cook-Lewis discloses 15[h] for the same reasons as 1[e]. *Id.*, ¶275.

36. Claim 15[i]:

Cook-Lewis discloses 15[i] for the same reasons as 1[f]. *Id.*, ¶276.

37. Claim 16

See Claim 2; *see also* EX1003, ¶277.

38. Claim 17

See Claim 3; see also EX1003, ¶278.

39. Claim 18

See Claim 4; see also EX1003, ¶279.

40. Claim 19

See Claim 6; see also EX1003, ¶280.

41. Claim 20

See Claim 7; see also EX1003, ¶281.

42. Claim 21[pre]

See Claim 15[pre]; see also EX1003, ¶282.

43. Claim 21[a]

See Claim 15[a]; see also EX1003, ¶283.

44. Claim 21[b]

See Claim 15[b]; see also EX1003, ¶284.

45. Claim 21[c]

See Claim 15[c]; see also EX1003, ¶285.

46. Claim 21[d]

See Claims 8[a] and 15[d]-15[i]; see also EX1003, ¶286.

47. Claim 22

See Claim 2; see also EX1003, ¶287.

48. Claim 23

See Claim 11; see also EX1003, ¶288.

49. Claim 24

See Claim 12; *see also* EX1003, ¶289.

50. Claim 25

See Claim 13; *see also* EX1003, ¶290.

51. Claim 26

See Claim 14; *see also* EX1003, ¶291.

**D. Ground 4: Cook in View of Lewis and Sarkinen Renders Obvious
Claims 3, 6, 8, 13, 14, 17, 21, 25, and 26**

To the extent the additional limitations of claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 are not rendered obvious by Cook and Lewis, it would have been obvious to combine Cook and Lewis with Sarkinen. EX1003, ¶¶292-300.

1. Motivations to Combine Cook, Lewis and Sarkinen

It would have been obvious to a POSITA to combine Sarkinen with Cook and Lewis.⁵ It would have been obvious to a POSITA that Sarkinen discloses a backplane system similar to the backplane system disclosed in Cook. *Id.*, ¶293. A POSITA looking to expand the formats supported by Cook-Lewis combination would have reason to look to Sarkinen. *Id.*, ¶293. Sarkinen also discloses one type of backplane device to which the loopback testing system available in the Cook-Lewis combination could apply. *Id.*, ¶293. Sarkinen discloses that the invention enables “[u]sing [a line-to-switch] interface and isolating such an interface in accordance

⁵ This combination does not alter the combination discussed in Ground 2. Claims discussed under this combination continue to map to the Ground 2 claims of relevance for the reasons explained in those sections.

with the invention, routers and switches can provide multiple service classes, efficiently handle multicast traffic, and instantaneously direct the flow of traffic to other ports should there be a failure on a link.” EX1011, ¶58. A POSITA would have been motivated to apply the testing from Cook and Lewis to ensure that the line cards, traces, or links of Sarkinen were functioning properly so as to know the links available to which traffic could be instantaneously directed to in the event of a failure on a link. EX1003, ¶293. Indeed, a POSITA would have recognized that the path between two line cards would be a loop that would commonly be used and should be tested periodically when the trace is idle. *Id.* This would result in a combined backplane system with subsidiary modules able to implement loop back testing to test specific links, traces, or lines. A POSITA would have understood that the fabric interface would act as a switch to help address traffic of different formats between the line cards and that the fabric interface would operate in between the line cards and could set up the paths between the line cards as shown in Figure 4. *Id.*

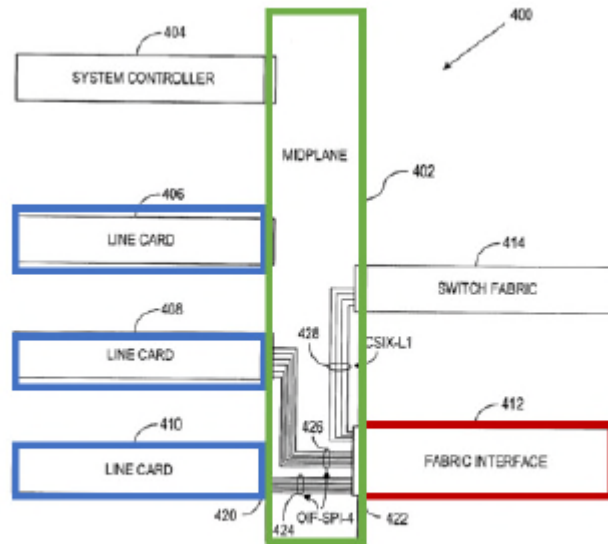


FIG. 4

2. Claim 6

The architecture of the Cook-Lewis system is similar to the architecture of the embodiments disclosed by Sarkinen. Sarkinen discloses a backplane device, such as a network switch or router, with **line cards and fabric cards (subsidiary modules)** controlled by a **fabric interface (main module)**, all of which are plugged into a **backplane or midplane 314**. EX1003, ¶294. Sarkinen further makes it clear that the line cards include a network line interface, which plugs into a network link or trunk to a broader network. EX1011, ¶13; EX1003, ¶296. Sarkinen also discloses that the invention relates generally to “communication networks.” EX1011 ¶3. It also notes that one standard that can be utilized in implementing the invention is the “CSIX-L1 standard which defines an interface between a network processor (e.g., traffic

manager, or any processor used for packetized information) and a switch fabric in data communications applications.” *Id.*, ¶¶ 66, 106; EX1003, ¶295. A POSITA would have understood that the traffic transmitted over the line cards and fabric cards is communication traffic for routing over the network to which the switch/router is connected. EX1003, ¶¶294-297.

3. Claims 3, 8, 13, 14, 17, 21, 25, and 26

Claims 3, 8, 13, 14, 17, 21, 25, and 26 further recite that the subsidiary modules transmit and receive data in at least two different formats. EX1003, ¶¶298-299. To the extent Cook-Lewis does not render obvious this limitation, it would have been obvious to combine Sarkinen with the Cook-Lewis system because Sarkinen is an example of a network switch with the backplane architecture disclosed in Cook, that supports multiple formats and would benefit from the Cook-Lewis testing techniques for the same reasons. EX1003, ¶299. Sarkinen explains that the switch may support multiple protocols. EX1011, ¶¶49, 58, 66; EX1003, ¶¶299. Sarkinen discloses the use of multiple formats for traffic in the network switch transported across the fabric. EX1011, ¶¶49, 58, 66. Sarkinen discloses that protocols and formats are typically defined by a standard. *Id.*, ¶¶47, 69. Sarkinen also discloses the use of a traffic manager for different formats. EX1011, ¶68. Sarkinen also discloses the use of a fabric processor to manage traffic of different formats across line cards. EX1011, ¶49. It would have been obvious to a POSITA

that each line card could support a different protocol with a different format and that traffic utilizing these different formats could be transmitted from one line card, or subsidiary module, to another. EX1003, ¶¶298-299.

4. Claims 13 and 25

Claims 13 and 25 further recite that the different formats are determined by different protocols. Sarkinen discloses that the fabric processor 220 converts the data stream from one format to another, such as from POS frames to Common Switch Interface (CSIX) cells, and distributes the cells over the switch fabric. EX1011, ¶49. Sarkinen also discloses that the CSIX-L1 specification defines an interface between a traffic manager and a switch fabric for data communication applications, and specifies certain data formats.” *Id.*, ¶66. Sarkinen thus discloses different formats determined by the different standards supported by the switches, or multiple line card system and this functionality would remain when combined with the Cook-Lewis techniques. EX1003, ¶¶298-299, 300.

5. Claims 14 and 26

Claims 14 and 26 recite that one protocol is a TDM protocol and the other is a packet data protocol. Sarkinen discloses the use of “Packet-Over-SONET/SDH (POS) frames” which is “known in the art, [as] a high-speed time division multiplexing (TDM) physical-layer transport technology.” EX1011, ¶47. Sarkinen also discloses that “[t]ypically, the data packet stream is converted to a particular

format, such as converted to comply with the CSIX standard.” EX1011, ¶69. A POSITA would have been familiar with both TDM protocols and packet data protocols and would have understood Sarkinen disclosed the use of a TDM and packet data protocol and this functionality would remain when combined with Cook-Lewis. EX1003, ¶¶298-299, 301-302.

IX. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. Discretionary denial under the *Fintiv* factors is not appropriate

1. Factor 1: Institution will increase the likelihood of stay

The Delaware District Court is likely to find a motion to stay prior to institution of an IPR premature but is very likely to stay a case post-institution of this IPR. Notwithstanding, the Board has repeatedly stated it will not speculate on how a district court will treat a motion to stay. *See, e.g., VMware Inc. v. Intellectual Ventures II LLC*, IPR2020-00859, Paper No. 13, at 12 (PTAB Nov. 5, 2020) (informative) (“We agree with Petitioner. In the absence of any evidence specific to this case, we decline to speculate about the presiding judge’s inclinations.”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) (“We decline to infer, based on actions taken in different cases with different facts, how the District Court would rule should a stay be requested by the parties in the parallel case here.”). As such, this factor at best favors institution and is at worst neutral.

2. Factor 2: District Court schedule

There is no scheduling order in the *Arista* litigation. The current average time to trial for the Delaware District Court, where the *Arista* and *Dell* litigations were filed, is over 3 years. EX1015 (median time to trial of 39 months). Claim construction in the *Cisco* litigation has been completed. EX1007. No date has been set for trial. The average time-to-trial for cases in the Western District of Texas where the *Cisco* litigation is pending is over 2 years. EX1014 (showing W.D. Texas median time to trial of 28.3 months); *In re Apple Inc.*, 979 F.3d 1332, 1350 (Fed. Cir. 2020). A Final Written Decision (“FWD”) would be expected in July 2024. However, Petitioner notes that “a court’s general ability to set a fast-paced schedule is not particularly relevant...where, like here, the forum itself has not historically resolved cases so quickly.” *Id.* at 1344.

Accordingly, this factor weighs against discretionary denial. *See Sand Revolution II, LLC v. Continental Intermodal Grp.*, IPR2019-01393, Paper 24 (PTAB June 16, 2020) (granting institution on rehearing based on finding that uncertainty over district court’s trial date weighed against discretionary denial).

3. Factor 3: Petitioner’s investment in IPR outweighs forced investment in litigation to date

The *Arista* litigation is in its early stages, and the investment has been minimal. There is no scheduling order entered in the case. As such this factor weighs against denial.

4. Factor 4: The Petition raises unique issues

Invalidity contentions have not been served in the *Arista* litigation. Invalidity contentions in the *Cisco* litigation were served on Patent Owner on September 28, 2022. Instituting this proceeding will allow the Board to address the asserted prior art, narrowing the issues in the co-pending litigations due to the estoppel provisions of 35 U.S.C. § 315(e)(2). This factor therefore weighs against denial.

5. Factor 5: Whether the Petitioner and Defendant in the parallel litigation are the same party

Petitioner is a defendant in a co-pending litigation. While the *Fintiv* case indicates that a difference between the district court defendant and the petitioner may weigh against discretionary denial, nothing in *Fintiv* suggests that having the same party between the proceedings weighs in favor of discretionary denial. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13, at 9 (PTAB Jan. 14, 2021) (having the “same parties as parallel proceeding” makes factor 5 “neutral”). Accordingly, this factor is neutral and should not be a basis for denying institution.

6. Factor 6: Other circumstances support institution

The prior art presented in this Petition renders the Challenged Claims unpatentable as obvious. The merits of Petitioner’s arguments are compelling because they lead to a strong conclusion that one or more claims are unpatentable by a preponderance of the evidence. This factor therefore weighs against discretionary denial. As such, the *Fintiv* factors are either neutral or weigh against

discretionary denial. Because this Petition was filed before the statutory bar date, institution should not be denied on discretionary factors.

B. PTAB should not exercise its discretion to deny institution under *Becton and Advanced Bionics*

Furthermore, institution should not be denied under the framework set forth in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to §III.C.5, first paragraph) and *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). Although Ke was before the Examiner during prosecution, the Examiner did not have the benefit of evaluating Ke in combination with Lewis as described herein. Furthermore, neither Cook nor Lewis (nor their combination) was before the Examiner during prosecution. Therefore, the arguments presented in this Petition are not the same as, or substantially similar to, arguments previously presented to the Office. Thus, the first prong of the *Advanced Bionics* framework is not met, and there is no need to reach the second prong to resolve against discretionary denial under Section 325(d). *Oticon Medical AB v. Cochlear Ltd.*, IPR2019-00975, Paper 15, at 20 (PTAB Oct. 16, 2019) (precedential).

C. Discretionary denial under *General Plastic* is not appropriate

None of the *General Plastic* discretionary institution factors favor denial. *See General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16 (Sept. 6, 2016) (Section II.B.4.i. precedential).

1. Factor 1

Factor 1 weighs against discretionary denial because Petitioner Arista has not previously filed a petition directed to any claims of the '369 Patent. Arista is not a defendant in the same litigation matter as Cisco or Dell. *Cf. Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11 at 9-10 (PTAB Apr. 2, 2019) (precedential) (finding a “significant relationship” between different petitioners when they were “co-defendants in the [same] District Court litigation” matter). Arista is also not in privity with Cisco or Dell. EX1016, at 2 (Dell and Cisco certified they were the only parties-in-interest to their Dell petition.) Thus, there is no “significant relationship” with either Cisco or Dell. *Valve* at 10. This weighs against discretionary denial.

2. Factors 2-5

Given the relatively short time between the filing of Dell’s petition and the present Petition, Factors 2 and 4 also weigh against discretionary denial. *See Mercedes-Benz USA, LLC v. Carucel Investments, L.P.*, IPR2019-01404, Paper at 13 (Jan. 22, 2020). This Petition is being filed less than four months after Dell’s Petition.

Importantly, Corrigent has not filed a Patent Owner Preliminary Response to IPR2023-00464, so Petitioner receives no potential benefit or tactical advantage. Factors 2-5 therefore weigh against discretionary denial.

3. Factors 6-7

There is substantial overlap between this petition and Dell's petition challenging the same claims and using overlapping prior art. Arista's petition includes the same grounds as Dell's petition. The similarities that exist between these petitions provide a strong basis for efficiency. The Arista and Dell petitions could be joined, due to the substantial overlap. Arista agrees to allow Dell's counsel to take the lead on overlapping issues.

Petitioner has a meaningful due process interest in being heard in this forum on the merits, because of its choice to raise the unpatentability grounds before the Board. This fact also favors not denying institution.

X. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable. Petitioner respectfully requests that the IPR of the '369 Patent be instituted.

DATED: April 18, 2023

Respectfully Submitted,

/s/

Eliot D. Williams (Reg. No. 50,822)
Baker Botts L.L.P.
700 K Street, N.W.
Washington, D.C., 20001-5692

*Petition for Inter Partes Review
of U.S. Patent No. 6,957,369*

Tel: 202-639-1334

Eliot.Williams@BakerBotts.com

Attorney for Petitioner Arista Networks, Inc.

CERTIFICATION UNDER 37 C.F.R. §42.24(d)

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 12,754 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman.

Date: April 18, 2023

Respectfully submitted,

/s/ Eliot D. Williams

Eliot D. Williams (Reg. No. 50,822)
700 K Street, N.W.
Washington, D.C., 20001-5692
Tel: 202-639-1334
Eliot.Williams@BakerBotts.com
Lead Attorney for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 17th day of April 2023, the foregoing was provided via Priority Mail Express or by means at least as fast and reliable as Priority Mail Express, postage prepaid, to the Patent Owner and its known representatives by serving the correspondence address of record for the U.S. Patent No. 6,957,369 owner and the patent owner's counsel:

Date of service April 18, 2023

Manner of service Federal Express for physical addresses; USPS for P.O. Box

Documents served Petition for Inter Partes Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 7,330,431; Petitioner's Exhibit List; Exhibits 1001 - 1018.

Counsel for Patent Owner May Patents Ltd. (attorney/agent of record)
c/o Dorit Shem-Tov
P.O. Box 7230
Ramat-Gan, -5217102
Israel

Corrigent Corporation (assignee of record)
126 Yigal Allon Street
Tel Aviv, Israel 67443

*Petition for Inter Partes Review
of U.S. Patent No. 6,957,369*

Corrigent Corporation (assignee of record)
291 Main St.
C/O New England Intellectual Property
West Newbury, Massachusetts 01985

Date: April 18, 2023

Respectfully submitted,

/s/ Eliot D. Williams

Eliot D. Williams (Reg. No. 50,822)
700 K Street, N.W.
Washington, D.C., 20001-5692
Tel: 202-639-1334
Eliot.Williams@BakerBotts.com
Lead Attorney for Petitioner

APPENDIX: CHALLENGED CLAIM LISTING

No.	Limitation
1[pre]	In an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:
1[a]	selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;
1[b]	instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line;
1[c]	selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;
1[d]	configuring the switch to link the first and second ports;
1[e]	transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and
1[f]	reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.
2	A method according to claim 1, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.
3	A method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.
4	A method according to claim 1, further comprising: selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and repeating the configuring the switch, transmitting the test traffic, and reporting that the failure has occurred

No.	Limitation
	with respect to the further idle lines until all the idle lines have been tested.
5	A method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.
6	A method according to claim 1, wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic.
7	A method according to claim 6, wherein transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk.
8[pre]	In an electronic system that includes a main module and multiple subsidiary modules, each of said multiple subsidiary modules being connected to the main module by one or more lines for carrying data, a method for self-testing the system, comprising:
8[a]	selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats;
8[b]	instructing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module;
8[c]	configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module; and
8[d]	testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.
9	A method according to claim 8, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.
10	A method according to claim 8, wherein the main module and subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

No.	Limitation
11	A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module.
12	A method according to claim 11, wherein testing the system comprises testing one or more of the lines of the second subsidiary module while continuing to use at least some of the lines that are not under test for carrying the data from the subsidiary modules to the network communication trunk.
13	A method according to claim 8, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.
14	A method according to claim 13, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.
15[pre]	Modular electronic apparatus, comprising:
15[a]	a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
15[b]	a main module, plugged into the backplane, the main module comprising a switch having ports for connection to the traces of the backplane;
15[c]	at least first and second subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces, at least some of which traces are sometimes idle;
15[d]	a system control processor, which is operative to select a first idle trace among idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace,
15[e]	to instruct the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid trace,
15[f]	to select for testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module,
15[g]	to configure the switch to link the first and second ports,

No.	Limitation
15[h]	the system control processor being further operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module, and
15[i]	to report that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.
16	Apparatus according to claim 15, wherein the first subsidiary module is configured, under control of the system control processor, to loop back the traffic on the aid trace to the main module substantially without processing data comprised in the test traffic.
17	Apparatus according to claim 16, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.
18	Apparatus according to claim 15, wherein the system control processor is operative to select one or more further idle traces for testing among the idle traces in the system, wherein the further idle traces connect to further ports of the switch on the main module, and to repeatedly configure the switch, cause the test traffic to be transmitted, and report the failure when it occurs with respect to the further idle traces until all the idle lines have been tested.
19	Apparatus according to claim 15, wherein the switch is configured to connect the traces to a network communication trunk, and wherein the traffic comprises communication traffic.
20	Apparatus according to claim 19, wherein the test traffic is transmitted over the second idle trace while continuing to use the trace that are not idle for carrying the data to the network communication trunk.
21[pre]	Modular electronic apparatus, comprising:
21[a]	a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
21[b]	a main module, plugged into the backplane;
21[c]	a plurality of subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces; and
21[d]	a system control processor, which is operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules

No.	Limitation
	being configured to transmit and receive the data in different, respective first and second formats, and which is further operative to test the modules by causing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module, by configuring the main module to connect the first and second subsidiary modules, so that a traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module, and by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.
22	Apparatus according to claim 21, wherein the first subsidiary module is configured to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.
23	Apparatus according to claim 21, wherein the main module comprises a switch, which is coupled to connect the traces to a network communication trunk, and wherein the system control processor is operative to configure switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module during the test.
24	Apparatus according to claim 23, wherein the system control processor is operative to test one or more of the traces connected to the second subsidiary module while at least some of the traces that are not under test continue to be used for carrying the data from the subsidiary modules to the network communication trunk.
25	Apparatus according to claim 21, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.
26	Apparatus according to claim 25, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.