

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELL TECHNOLOGIES INC., DELL INC., and
CISCO SYSTEMS, INC.,
v.
CORRIGENT CORPORATION,
Patent Owner.

IPR2023-00464
Patent 6,957,369 B2

Before KRISTEN L. DROESCH, NATHAN A. ENGELS, and
BRENT M. DOUGAL, *Administrative Patent Judges*.

ENGELS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Dell Technologies Inc., Dell Inc., and Cisco Systems, Inc. (collectively, “Petitioner”) filed a Petition (Paper 4, “Pet.”) requesting *inter partes* review of claims 1–26 of U.S. Patent No. 6,957,369 B2 (Ex. 1001, “the ’369 patent”). Patent Owner Corrigent Corporation filed a Preliminary Response. Paper 17 (“Prelim. Resp.”).

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition and any response thereto shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon consideration of the Petition and the evidence of record, we determine Petitioner has not demonstrated a reasonable likelihood of prevailing in establishing unpatentability of at least one claim of the ’369 patent. Accordingly, we do not institute *inter partes* review.

A. *Real Parties-in-Interest*

Petitioner identifies Dell Technologies Inc., Dell Inc., and Cisco Systems, Inc. as the real parties-in-interest. Pet. 2. Patent Owner identifies itself as the sole real party-in-interest. Paper 5, 2.

B. *Related Matters*

The parties state that the ’369 patent is involved in the following district court cases: *Corrigent Corp. v. Cisco Systems, Inc.*, No. 6:22-cv-396 (W.D. Tex.); *Corrigent Corp. v. Dell Technologies Inc.*, No. 1:22-cv-00496 (D. Del.); and *Corrigent Corp. v. Arista Networks, Inc.*, No. 1:22-cv-497 (D. Del.). Pet. 2; Paper 5, 2.

C. Illustrative Claim

Of the challenged claims, claims 1, 8, 15, and 21 are independent claims. Claim 1 is copied below.

1. In an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:

selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;

instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line;

selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;

configuring the switch to link the first and second ports;

transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and

reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

D. Alleged Grounds of Unpatentability

Petitioner asserts that claims 1–26 would have been unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–26	103(a) ¹	Ke, ² Lewis ³
3, 6, 8, 13, 14, 17, 21, 25, 26	103(a)	Ke, Lewis, Sarkinen ⁴
1–26	103(a)	Cook, ⁵ Lewis
3, 6, 8, 13, 14, 17, 21, 25, 26	103(a)	Cook, Lewis, Sarkinen

Pet. 5. Petitioner also supports its challenge with a Declaration of Samrat Bhattacharjee, Ph.D. Ex. 1004.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends a person of ordinary skill in the art at the time of the invention (“POSITA”) would have had “a degree in electrical

¹ The ’605 patent was filed before the Leahy-Smith America Invents Act (“AIA”) revisions to 35 U.S.C. § 103 became effective. Therefore, we apply the pre-AIA version of § 103; however, our analysis would be the same under the AIA version of the statute.

² US 5,841,788; issued Nov. 24, 1998. Ex. 1008.

³ US 4,685,102; issued Aug. 4, 1987. Ex. 1009.

⁴ US 2003/0101426 A1; published May 29, 2003. Ex. 1011.

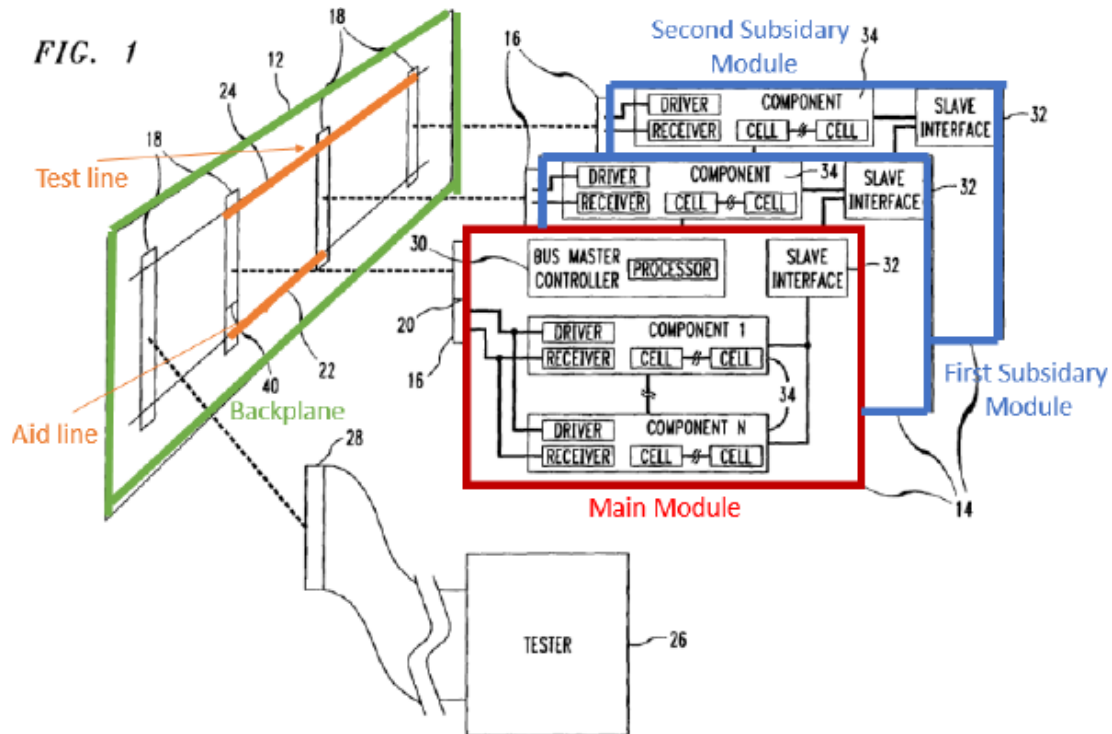
⁵ US 4,074,352; issued Feb. 14, 1978. Ex. 1010.

engineering, computer engineering or a similar discipline, with at least two years of relevant industry or research experience (or additional education)” and “a working understanding of backplanes and other printed circuit boards, including the connections thereto.” Pet. 8 (citing Ex. 1003 ¶ 17). Petitioner also states that more experience can substitute for less education and vice versa. Pet. 8.

Patent Owner does not address the level of ordinary skill in its Preliminary Response. For the purposes of this Decision, we apply Petitioner’s level of ordinary skill, which is consistent with the level reflected by the ’369 patent and the asserted prior art.

B. Petitioner Fails to Establish that a POSITA Would Have Combined Ke and Lewis

Petitioner challenges claims 1–26 as obvious based on the combined teachings of Ke and Lewis and claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 as obvious based on the combined teachings of Ke, Lewis, and Sarkinen. Pet. 14–42. Among other things, citing the annotated version of Ke’s Figure 1, copied below, Petitioner argues “[a] POSITA would have been motivated to combine the backplane testing described in Ke with the loopback testing described in Lewis.” Pet. 14.



Pet. 15. Petitioner’s annotated version of Ke’s Figure 1 depicts backplane 40 connected to tester 26 and three individual boards 14, the first board is labeled by Petitioner as the “Main Module” and two additional boards are labeled by Petitioner as the “First Subsidiary Module” and the “Second Subsidiary Module.” Pet. 15. Petitioner argues “[t]he main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as disclosed in Lewis.” Pet. 15 (Petitioner’s added text colors omitted). According to Petitioner, “[t]he backplane modules in Ke would then perform the loopback test described in Lewis . . . , where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines.” Pet. 15.

But Petitioner’s arguments are inconsistent with the teachings of Ke. Contrary to Petitioner’s arguments regarding “combin[ing] the backplane testing described in Ke with the loopback testing described in Lewis,” Ke

describes techniques for testing backplane interconnects in which “test vectors are applied to circuit boards individually, while the remaining boards in the system are disabled.” Ex. 1008, 2:24–26; *see* Ex. 1008, 3:61–67, 4:20–23, 5:35–39, 7:26–34, Figs. 11, 13. In particular, Ke describes two testing techniques, a “walking enable test” and an “intraboard counting technique,” both of which begin with a step of disabling all boards and then enabling only one individual board for testing. Ex. 1008, 5:35–39, 7:26–34, Figs. 11, 13.

In one instance, Petitioner acknowledges these teachings of Ke: “Ke discloses one such testing configuration for boundary testing where the backplane connections are tested one at a time by toggling the connections on and off to test one connection at a time.” Pet. 13. But Petitioner does not reconcile these teachings with its arguments. Petitioner instead argues “Ke acknowledges that there are different ways to test backplanes” (Pet. 13) and “Ke makes clear that its backplanes are highly configurable with many different board types, so the testing configurations should be adaptable and flexible” (Pet. 16). This mischaracterizes Ke.

Ke states that “other techniques for providing test vectors can be used, *provided that test vectors are applied to drivers on a single board at a time while the remaining boards in the system are disabled.*” Ex. 1008, 7:26–34 (emphasis added). Petitioner’s declarant Dr. Mir recognizes that warning: “Ke discusses testing the backplane traces by disabling certain parts of the system to avoid damage to circuit components.” Ex. 1003 ¶ 77 (citing Ex. 1008, 2:29–35); *see* Ex. 1008, 3:38–60 (stating that synchronization problems can occur with boundary scan backplane testing with multiple boards; “intermediate vectors between the current vector and the next vector

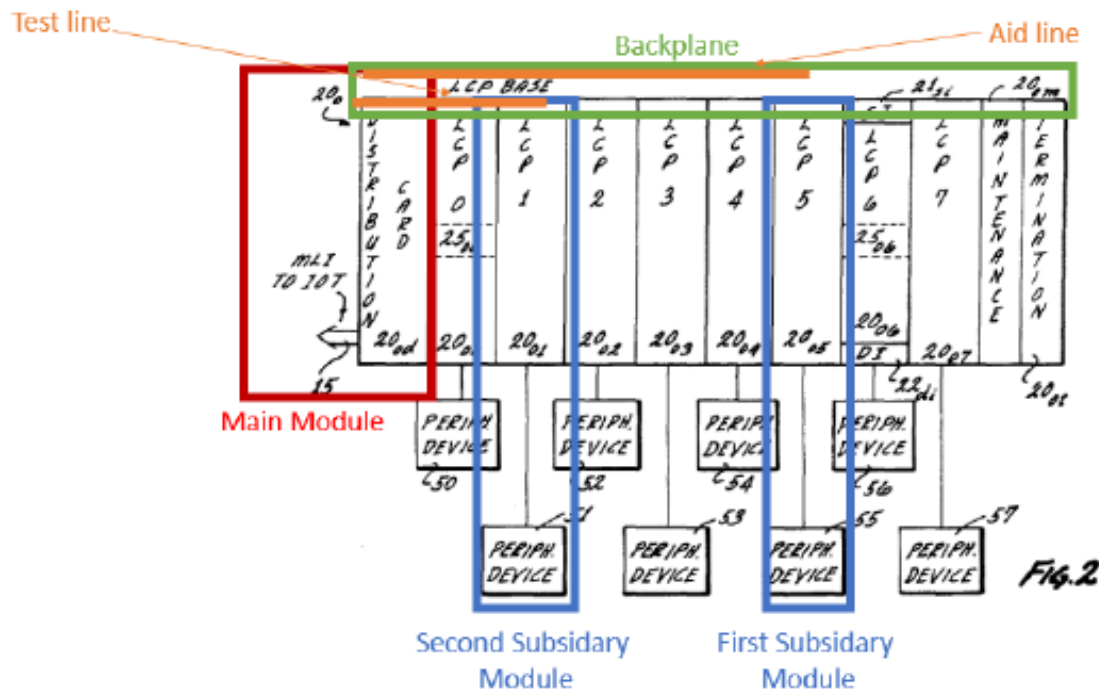
may create contentions, whereby components on different boards simultaneously attempt to drive the same interconnect on the backplane. It could therefore damage the system if the intermediate vectors shown in FIG. 2 were to be applied.”). Yet, neither Petitioner nor Dr. Mir adequately explains why or how a person of ordinary skill would have chosen Ke’s teachings for combining with Lewis’s teachings, when Ke directly warns against testing with more than one board enabled. *Cf.* Pet. 17 (arguing “because Ke acknowledged that there were multiple possible techniques for testing backplanes. A POSITA would therefore have a reasonable expectation of success to apply different testing techniques to the backplane structure in Ke, including the one from Lewis.” (citing Ex. 1008, 1:30–2:18; Ex. 1003 ¶ 78)).

Thus, we agree with Patent Owner that Petitioner has not shown adequate reasons for combining Ke and Lewis with a reasonable expectation of success. Further, particularly in light of the teachings of Ke, Petitioner employs improper hindsight in suggesting that a POSITA would have combined Ke and Lewis to arrive at the claimed invention. Accordingly, we determine Petitioner has not shown a reasonable likelihood of prevailing in its challenge to any of claims 1–26 as being unpatentable in view of Ke and Lewis and claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 as being unpatentable in view of Ke, Lewis, and Sarkinen.

C. Petitioner Fails to Establish that a POSITA Would Have Combined Cook and Lewis

Petitioner challenges claims 1–26 as obvious based on the combined teachings of Cook and Lewis and claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 as obvious based on the combined teachings of Cook, Lewis, and Sarkinen. Pet. 42–72. Citing the annotated version of Cook’s Figure 2, copied below,

Petitioner contends “[a] POSITA would have been motivated to combine the backplane testing described in Cook with the loopback testing described in Lewis.” Pet. 45.



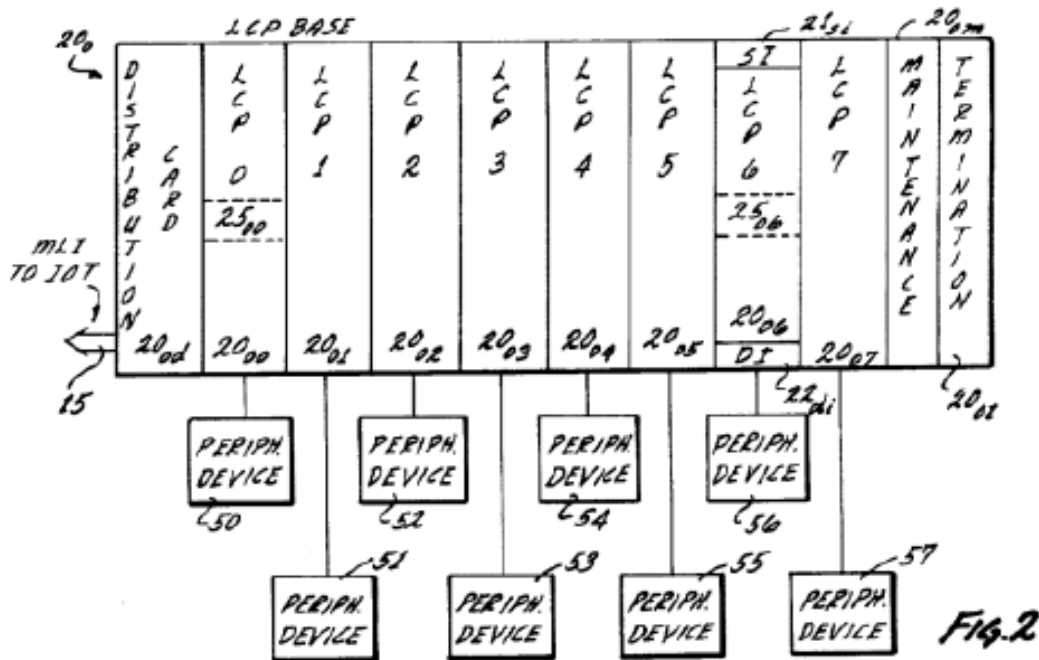
Pet. 45. Petitioner’s annotated version of Cook’s Figure 2 depicts line control processors (“LCP”) 0–7 connected to a distribution card unit (“DCU”), boxed in red and labeled “Main Module,” via a LCP base module, boxed in green and labeled “Backplane.” Each of LCP 0–7 is connected to one of peripheral devices 50–57, two of which are boxed in blue and labeled “First Subsidiary Module” and “Second Subsidiary Module.”

Petitioner argues “[t]he main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as described in Lewis. The backplane modules in Cook would then perform the loopback test described in Lewis set forth above, where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines.” Pet. 45 (citing Ex. 1009, 4:42–54).

But Petitioner’s proposed combination is inconsistent with the teachings of Cook. Cook teaches poll testing backplanes with gated lines dedicated for each LCP. Ex. 1010, 23:28–24:27. According to Cook, “[b]y providing a separate channel from the Main System to each peripheral, there is no need for data transfers (between a particular peripheral unit and the Main System) to have to wait for use of a shared communication channel, since each individual peripheral unit is provided with its own channel.” Ex. 1010, 5:34–40. Cook states that “[o]f the lines which go to the Distribution Card, and on to the IOT [I/O Translator], some, such as the data an [sic] the parity lines, *must be gated to individual LCPs*. This gating is enabled only when the LCP is in the ‘connected’ state; when the LCP disconnects, the gating is disabled.” Ex. 1010, 29:8–12 (emphasis added). “In addition to the gated lines, there are some lines which are dedicated to each individual LCP, for example, the line which goes from the Distribution card to only one LCP.” Ex. 1010, 29:18–21. And, “[d]uring the time an LCP is connected to the IOT, that LCP has the *exclusive access* to the Base Module Backplane [and] the IOT-LCP data transfer occurs.” Ex. 1010, 29:24–27 (emphasis added). “Upon cessation of the data transfers, the LCP disconnects from both the IOT and the Base Module Backplane, thus *freeing them for use by other LCP’s* in the system.” Ex. 1010, 29:28–31 (emphasis added).

These teachings are inconsistent with Petitioner’s annotated Figure 2 and proposed loopback testing, in which “the main module routes the test packets between the first and second subsidiary modules *over the test and aid lines*.” Pet. 45 (citing Ex. 1009, 4:42–54) (emphasis added). As

reflected in the *unannotated* version of Cook's Figure 2 below, Cook's teachings do not include "test and aid lines."



Ex. 1010, Fig. 2. With Cook teaching backplane poll tests using gated lines dedicated for each LCP, neither Petitioner nor Dr. Mir adequately explains why or how "a POSITA would have been motivated to combine the backplane testing described in Cook with the loopback testing described in Lewis" (Pet. 45). Cf. Pet. 46 ("It would have been obvious to a POSITA that testing in a backplane could benefit from such a loopback test because there are times when the different boards in a backplane need to communicate with each other." (citing Ex. 1003 ¶ 175)); Ex. 1003 ¶ 177 ("Cook explains that the DCU and IOT work together to control the communications and testing of individual LCPs, which would indicate to a POSITA that a test like that described in Lewis could be implemented" (citing Ex. 1010, 31:63–32:41)). Thus, Petitioner has not adequately explained reasons for combining Cook and Lewis, and we agree with Patent Owner (Prelim.

Resp. 23–25) that Petitioner’s proposal to combine Cook and Lewis employs improper hindsight.

Accordingly, we determine Petitioner has not demonstrated a reasonable likelihood of prevailing in its challenge of any of claims 1–26 as being unpatentable in view of Cook and Lewis as well as claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 in view of Cook, Lewis, and Sarkinen.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has not demonstrated a reasonable likelihood that it will prevail with respect to at least one of claims 1–26 of the ’369 patent. Accordingly, we do not institute an *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied and *inter partes* review of the ’369 patent is not instituted.

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