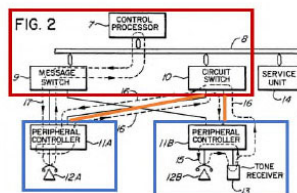


Comparison of “Motivation to Combine Ke and Lewis” Section Between Petition and Petition in Dell-Cisco IPR (EX1016)

Petition

*Petition for Inter Partes Review
of U.S. Patent No. 6,957,369*

EX1009, 3:47-60. In this example, the circuit switch sets up a **loop 16** that connects peripheral 12A with peripheral 13 through the **circuit switch 10**.



Id., Fig. 2.

According to Lewis, the control processor can send a message to peripheral 12A to trigger a **loop back** test. The **loop back** test would travel via loop 16 from 12A to circuit switch 10 to peripheral 13. Peripheral 13 would be configured to loop back the message to circuit switch 10 and then back to peripheral 12A. *Id.*, 4:42-54. Lewis further explains that testing should be performed during times when the links are idle. *Id.*, 2:19-20, 14:31-34. After the **loop back** test is performed, the result of the test is reported back to the message switch. *Id.*, 4:34-41, 4:49-52.

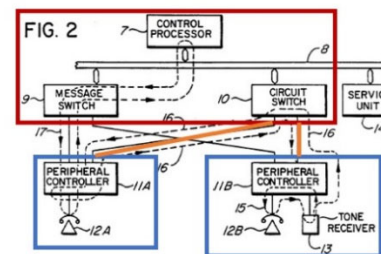
3. **Motivations** to Combine Ke and Lewis

A POSITA would have been motivated to combine the backplane testing described in Ke with the **loop back** testing described in Lewis as depicted below.

EX1003, ¶¶ 77-85.

Petition in Dell-Cisco IPR (EX1016)

*Petition for Inter Partes Review
of U.S. Patent No. 6,957,369*



Id., Fig. 2.

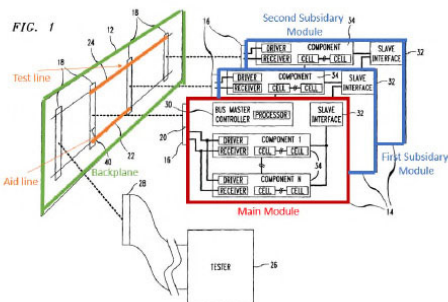
According to Lewis, the control processor can send a message to peripheral 12A to trigger a **loopback** test. The **loopback** test would travel via loop 16 from 12A to circuit switch 10 to peripheral 13. Peripheral 13 would be configured to loop back the message to circuit switch 10 and then back to peripheral 12A. *Id.*, 4:42-54. Lewis further explains that testing should be performed during times when the links are idle. *Id.*, 2:19-20, 14:31-34. After the **loopback** test is performed, the result of the test is reported back to the message switch. *Id.*, 4:34-41.

c) **Motivation** to Combine Ke and Lewis

A POSITA would have been motivated to combine the backplane testing described in Ke with the **loopback** testing described in Lewis as depicted below.

Petition

Petition for Inter Partes Review
of U.S. Patent No. 6,957,369



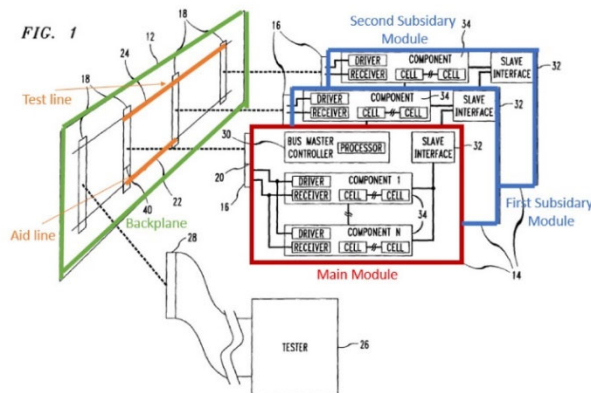
EX1008, Fig. 1. (annotated)

The main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as disclosed in Lewis. The backplane modules in Ke would then perform the loop back test described in Lewis set forth above, where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines. EX1009, 4:42-54. This combination would have been obvious to a POSITA for multiple reasons.

First, both references are generally directed to testing connections within a system with multiple components. Ke recites a master controller that directs testing in other boards plugged into a backplane. EX1008, 3:24-37. Lewis recites a similar set up where the control processor/circuit switch direct the testing of peripheral controllers. EX1009, 3:47-60. A POSITA would have been motivated to combine the testing protocol in Lewis in the structure disclosed in Ke because a POSITA

Petition in Dell-Cisco IPR (EX1016)

Petition for Inter Partes Review
of U.S. Patent No. 6,957,369



EX1008, Fig. 1.

The main module would set up an aid line with the first subsidiary module and a test line with the second subsidiary module, as disclosed in Lewis. The backplane modules in Ke would then perform the loopback test described in Lewis set forth above, where the main module routes the test packet between the first and second subsidiary modules over the test and aid lines. EX1009, 4:42-54. This combination would have been obvious to a POSITA for multiple reasons.

First, both references are generally directed to testing connections within a system with multiple components. Ke recites a master controller that directs testing in other boards plugged into a backplane. EX1008, 3:24-37. Lewis recites a similar

Petition	Petition in Dell-Cisco IPR (EX1016)
<i>Petition for Inter Partes Review of U.S. Patent No. 6,957,369</i> would have understood the benefits of a loop back test in the context of a backplane with a master controller. EX1003, ¶¶ 78-79. Second. Ke makes clear that its backplanes are highly configurable with many different board types, so the testing configurations should be adaptable and flexible. EX1008, 1:30-2:18. For example, Ke explains that there are many types of boards that may be plugged into a backplane, like memory and input/output devices. <i>Id.</i>, 1:65-67. A POSITA therefore would have been motivated to look at other testing configurations, like the one disclosed in Lewis for the creation of a loop back test. It would have been obvious to a POSITA that testing in a backplane could benefit from such a loop back test because there are many times when the different boards in a backplane need to communicate with each other. EX1003, ¶ 80. A POSITA would have recognized that there are times when data needs to be transferred to and from different boards on the backplane, e.g., from memory to an input-output device. <i>Id.</i> A POSITA therefore would have been motivated to apply the loop back testing between two peripherals in Lewis to the structure in Ke to test the connection between two boards in the backplane. <i>Id.</i>, ¶ 81. Third, a POSITA would have been motivated to test the backplane lines while they were idle as disclosed in Lewis. EX1009, 2:19-20. As Ke explains, testing the backplane traces may require disabling certain parts to avoid damage to circuit components. EX1008, 2:29-35. A POSITA would understand that the best time to 14	<i>Petition for Inter Partes Review of U.S. Patent No. 6,957,369</i> set up where the control processor/circuit switch direct the testing of peripheral controllers. EX1009, 3:47-60. A POSITA would have been motivated to combine the testing protocol in Lewis in the structure disclosed in Ke because a POSITA would have understood the benefits of a loopback test in the context of a backplane with a master controller. EX1003, ¶ 74. Second. Ke makes clear that its backplanes are highly configurable with many different board types, so the testing configurations should be adaptable and flexible. EX1008, 1:30-2:18. For example, Ke explains that there are many types of boards that may be plugged into a backplane, like memory and input/output devices. <i>Id.</i>, 1:65-67. A POSITA therefore would have been motivated to look at other testing configurations, like the one disclosed in Lewis for the creation of a loopback test. It would have been obvious to a POSITA that testing in a backplane could benefit from such a loopback test because there are many times when the different boards in a backplane need to communicate with each other. EX1003, ¶ 75. A POSITA would have recognized that there are times when data needs to be transferred to and from different boards on the backplane, e.g., from memory to an input-output device. A POSITA therefore would have been motivated to apply the loopback testing between two peripherals in Lewis to the structure in Ke to test the connection between two boards in the backplane. <i>Id.</i>, ¶ 76. 16 ARISTA NETWORKS, INC. EXHIBIT 1016 Arista Networks, Inc. v. Corrigent Corporation, IPR2023-00837, Page 31

Petition	Petition in Dell-Cisco IPR (EX1016)
<i>Petition for Inter Partes Review of U.S. Patent No. 6,957,369</i> disable those parts and perform the test is when the lines are otherwise idle because that would avoid disrupting traffic when the lines were in use. EX1003, ¶82 <u>Reasonable expectation of success.</u> A POSITA would have had a reasonable expectation of success to implement the testing in Lewis in the backplane structure from Ke because Ke acknowledged that there were multiple possible techniques for testing backplanes. EX1008, 1:30-2:18. A POSITA would therefore have a reasonable expectation of success to apply different testing techniques to the backplane structure in Ke, including the one from Lewis. EX1003, ¶83 Furthermore, Ke also explains that the bus master may control the test and send test data to different boards by addressing the data to those boards. EX1008, 3:28-35. A POSITA would have therefore understood that the <u>loop back</u> testing between specific peripherals in Lewis could be employed in Ke by using the master bus controller to control testing between specific boards. EX1003, ¶84	<i>Petition for Inter Partes Review of U.S. Patent No. 6,957,369</i> <u>Third,</u> a POSITA would have been motivated to test the backplane lines while they were idle as disclosed in Lewis. EX1009, 2:19-20. As Ke explains, testing the backplane traces may require disabling certain parts to avoid damage to circuit components. EX1008, 2:29-35. A POSITA would understand that the best time to disable those parts and perform the test is when the lines are otherwise idle because that would avoid disrupting traffic when the lines were in use. EX1003, ¶77 <u>Reasonable expectation of success.</u> A POSITA would have had a reasonable expectation of success to implement the testing in Lewis in the backplane structure from Ke because Ke acknowledged that there were multiple possible techniques for testing backplanes. EX1008, 1:30-2:18. A POSITA would therefore have a reasonable expectation of success to apply different testing techniques to the backplane structure in Ke, including the one from Lewis. EX1003, ¶78 Furthermore, Ke also explains that the bus master may control the test and send test data to different boards by addressing the data to those boards. EX1008, 3:28-35. A POSITA would have therefore understood that the <u>loopback</u> testing between specific peripherals in Lewis could be employed in Ke by using the master bus controller to control testing between specific boards. EX1003, ¶78