

Inverse Multiplexing for ATM. Operation, Applications and Performance Evaluation for the Cell Loss Ratio

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Abstract: The growing demand of bandwidth users made, indicates that access to ATM networks is an important issue. The Inverse Multiplexing for ATM (IMA) is a technology that combines multiple T1/E1 links to create a single logical data trunk which bandwidth is the aggregate of the T1/E1 ones, minus a small amount due to overhead. By using this technology, it is possible to have ATM connections with data rates between the T1/E1 (an economical but too slow option) and T3/E3 ones (with high bandwidth, but expensive). Also, it is interesting to have expressions easy to compute that approximate the main Quality of Service parameters of Inverse Multiplexers (IMUX) to help network planners in the dimensioning of these systems. In this paper, we study an estimate for the Cell Loss Ratio (CLR) measured in the IMUX devices.

Keywords: ATM, Performance Evaluation, Inverse Multiplexing, Modeling, Approximate Analysis.

1. Introduction

The growing demand of high-speed services is accelerating the B-ISDN (Broadband-Integrated Services Digital Network) deployment to offer and integrate data, voice and video applications in a single network. This network is based on the Asynchronous Transfer Mode (ATM) to handle any type of traffic efficiently. Users want to access the ATM network in a cost-effective manner. Simultaneously, network operators are providing this access using the existing network infrastructure.

At present, there are basically only two options available to provide access to the ATM services. One option employs T3/E3 links offering high bandwidth (44.736 Mbps/34.368 Mbps) but at high cost, usually not justified because they are under-utilized by prospective users. The other and more economical alternative, is by means of T1/E1 links (1.544 Mbps/2.048 Mbps), however they are too slow for some user needs. Typically the average cost of

a 25-kilometer T1/E1 circuit is \$850/\$2,900 per month respectively. In comparison, the average cost for the same distance T3/E3 link is \$7,500/\$29,000 per month [1]. Therefore, the T1/E1 tariffs offered by service providers and operators are substantially less expensive than T3/E3 ones. In the light of these facts, it is interesting for companies and customers requiring connection to broadband services, to lease several T1/E1 links instead of a T3/E3 link. Therefore, they are able to acquire a capacity according to the current user needs usually located between the T1/E1 and T3/E3 data rates. In addition, T3/E3 links are, in general, only available in big cities, consequently in some places it is not possible to obtain these services [1, 2].

To cover this gap of bandwidth, the ATM Forum published the IMA standard (Inverse Multiplexing for ATM Specification, version 1.0) in July, 1997 [3]. This specification explains how to accommodate a high-speed stream of ATM cells spreading them onto several T1/E1 lower-speed links, and how to recombine the partial streams into the original one at the receiving end. This is transparently made to the ATM layer, since the separated T1/E1 lines, form a single logical connection. Therefore, it is possible an intermediate capacity at some multiple of the T1/E1 rate, using readily-available services and simultaneously permitting a smooth migration to the future global ATM network because both technologies have the same nature: ATM cell transmission previous establishment of a logical link and fulfilling the Quality of Service (QoS) parameters required by each individual connection.

The IMUX (Inverse Multiplexer) is in charge of distributing ATM cells over various T1/E1 links, forming the so-called IMA group. It is done according to a round-robin algorithm. That is, the first cell is transmitted over the first link, the second cell over the second link, and so on. An equivalent de-multiplexing algorithm at the remote extreme reassembles all the cells into the original flow.

An IMUX accepts ATM cells as well as other type of traffics, i.e. LAN (Local Area Network) streams, that are adapted and converted into ATM cell format.

The IMUX introduces two types of OAM (Operation and Maintenance) cells: ICP (IMA Control Protocol) and Filler cells. They are appropriately inserted in the corresponding links and allow configuring and controlling the links belonging to the IMA group. Also they maintain the synchronism between the sending and receiving IMUX.

In this framework, we plan to obtain a methodology to help engineers and network planners to characterize and dimension an IMUX device. We are especially interested in expressions easy to compute that allow us to find the buffer size and the number of output links that guarantee the QoS parameters required by users. These parameters are basically the average cell delay, *CDV* (Cell Delay Variation) and *CLR* (Cell Loss Ratio). In this paper thus, the main network applications and the operation of the Inverse Multiplexing for ATM are explained in Sections 2 and 3. Then, a model for an IMUX device is developed through Sections 4, 5 and 6. Results for the *CLR* obtained by computer simulation and approximate analysis are presented and studied in Section 7. Finally, in Section 8 some concluding remarks and future work lines are addressed.

2. Origins and Applications

A conventional multiplexer combines various independent low-speed channels from different sources into one high-speed link for efficient transmission. However, the situation changes when applications and local traffic had just the opposite requirement: Users have high-speed LAN data, video-on-demand, multimedia applications, etc., to interconnect and inter-operate between remote ends. Instead of leasing a wide-bandwidth circuit, which capacity has to be full-used to justify its expensive cost, users can, as an alternative, use a cost-cutting scheme. The process in an Inverse Multiplexer is the reverse of multiplexing, because it involves breaking a wider signal into a number of smaller and independent low-cost channels for transmission [2].

The origin of the Inverse Multiplexing was based in leasing a number of small bandwidth synchronized digital telephone circuits (56/64 kbps) to obtain a higher-speed connection which capacity was approximately the addition of link capacities, minus a small amount of overhead [4]. In this way, it was possible to send a wide-bandwidth signal over the existing switched digital telephone network, available on a dial-up basis. In addition, customers use the minimum required bandwidth (with the granularity of one channel rate) and for the minimum time necessary, and they also have the flexibility to use as

much or as little bandwidth as required, paying only for the time the bandwidth is used. Inverse Multiplexing for ATM follows this scheme. But, in this case, it uses multiple T1/E1 links to constitute an IMA group of the necessary high-speed to transmit ATM services [3].

Network customers have other alternatives to employ multiple T1/E1 links for WAN (Wide Area Network) connections, i.e. Load Sharing. As it is shown in Figure 1, both strategies are similar in the sense they use various T1/E1 links. But while Inverse Multiplexing combines multiple T1/E1 into a single logical connection, the Load Sharing treats the T1/E1 as separate links. Load Sharing can be implemented according to two options: Route Caching and Frame-by-Frame. Route Caching directly assigns each individual connection to one T1/E1 link, therefore an application has its bandwidth limited to the data rate offered by that link. Moreover, with Route Caching the entire connection is lost if a physical failure occurs.

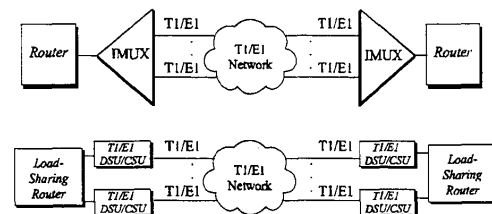


Figure 1. Inverse Multiplexing vs. Load Sharing.

With Frame-by-Frame, each packet is individually routed over one available T1/E1 line. Therefore, there is no bandwidth-per-application limitation, except for the total number of T1/E1 links leased. But in this case, the receiving router has to reorder packets which can be received out of order due to the different delays suffered among the links. This makes the hardware complexity of the receiver high. Furthermore, the processing time and therefore, the latency increase. On the other hand, Inverse Multiplexing has the additional advantage over Load Sharing to be able to recover from T1/E1 failures, because the connections are still preserved, although eventually reducing the total bandwidth. The failed T1/E1 links are automatically added back to the IMA group when they are restored. Consequently, it is possible to continue offering service to the applications, although reducing the QoS for the duration of the failure [3].

Besides that, Inverse Multiplexing could offer bandwidth on demand, adding T1/E1 links dynamically to a session already in progress if more bandwidth is requested. The circuit could be torn down when the bandwidth is no longer needed. Currently, this is one of the ATM Forum sub-working groups goals. There are some manufacturers (Nortel Magellan, Newbridge Networks, ADC Kentrox,

Ascend Communications Inc., ...) that incorporate a more efficient bandwidth management providing various levels of priorities in order to satisfy the QoS constraints of diverse applications and traffic classes [5].

The three typical network configurations where the IMUX technology applies are depicted in Figure 2.

- 1) Access connection to the ATM network.
- 2) Internal connection between ATM switches of the ATM network.
- 3) Dedicated bandwidth connection between two remote places.

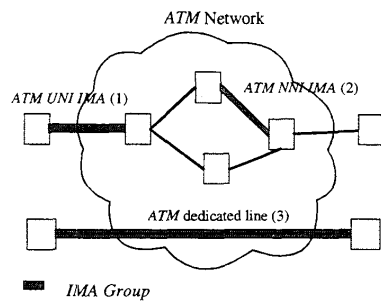


Figure 2. Usual network configurations with IMUX technology.

Using IMA, it is possible to get high-speed rates easily and, thus, it is feasible to provide broadband services immediately with the available infrastructure, before a global ATM network with very high-speed rates, 155/622 Mbps, be deployed. Moreover, using this technique it results more economical to extend ATM connectivity to remote places where it is really expensive to access it with high-speed links. IMA also provides MIB (Management Information Base) and hence, it is possible to configure and manage the IMUX devices as part of the overall network, from a remote location. MIB is based on SNMP (Simple network Management Protocol), an Internet standard network management framework [3].

3. IMUX: Operation of the Device

The IMUX device cyclically distributes a high-speed stream of ATM cells across the T1/E1 links on a per-cell basis, using a round-robin algorithm, as it can be seen in Figure 3. At the receiving end, a de-multiplexing algorithm reassembles again the cells. Special control cells are also introduced by the IMUX transmitter helping the receiver to reconstruct the original ATM cell stream.

IMA specification defines two OAM (Operations Administration and Maintenance) cells: The ICP (IMA Control Protocol) cells and the Filler cells, which are inserted into the data stream [3].

ICP cells carry information regarding the state of the link, the number of links being multiplexed, when a T1/E1 link from an IMA group should be added or removed, and differential delay values between links. To control IMA operation, an IMA frame is defined as M consecutive cells on each link, being one of these cells an ICP cell. The value of M is selected by the user and by default, the specification sets $M=128$ [3], thus an ICP cell is inserted every 127 ATM or Filler cells, resulting in an IMA frame of 128 cells. IMA frames are synchronized or aligned at the sending end. However, differential link delays can occur, although all the links in the IMA group run at the same speed. Therefore, some cells onto different links can arrive faster than others. Once the ICP cell position into the frame is known (this value is recognized as cell offset and it is included in the octet 9 of the ICP cell), the receiving device is able to align the frames and to maintain them synchronized before reassembling ATM cells without errors. An ICP cell includes information about the state of the link (active, with errors, etc.) and the remaining links in the IMA group. With this information, it is possible to remove a link from the group if it falls below an acceptable performance level. Then, the data rate is reduced to the equivalent one of the remaining active links, and once the link is recovered, it is automatically restored to the group, increasing the data rate to its original level.

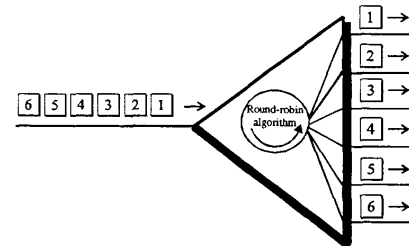


Figure 3. Round-robin algorithm for the distribution of ATM cells.

To compensate for timing differences among the T1/E1 links within the same IMA group, two consecutive ICP cells are inserted every 2,048 ATM, ICP or Filler cells. They are introduced in the TRL (Timing Reference Link), which is selected in the set up phase. These two cells together are called Stuff cells or SICP (Stuff ICP) cells, and they are also inserted in all output lines as required to avoid link de-synchronisms due to clock divergences [3, 6].

Finally, the sending device generates Filler cells when there are no information cells coming from the ATM layer. In this way, the links are kept saturated and the round-robin process at both ends is synchronized. That is, they perform a speed-matching or cell rate decoupling function. The logical link created by the IMA group has a rate known as IDCR (IMA Data Cell Rate); thus if cells

arrive at a rate faster than the IDCR one, they will be stored into a buffer, and if they arrive slower than IDCR, Filler cells will have to be necessarily inserted into the cell stream. The IDCR rate is defined, at both transmit and receive ends, according to the following equation [3, 6]:

$$IDCR = N_{on} * TRLCR * \left(\frac{M-1}{M} \right) * \left(\frac{2048}{2049} \right) \quad (1)$$

Being N_{on} the number of links which currently transmit cells in the IMA group; M is the IMA frame length; the $(M-1)/M$ factor accounts for an ICP cell every M cells; and the $2048/2049$ component relate to the insertion of one stuff event on the TRL (Timing Reference Link). Finally, $TRLCR$ is the TRL cell rate.

With all these control cells it is possible to achieve the IMA process, as it is illustrated in Figure 4.

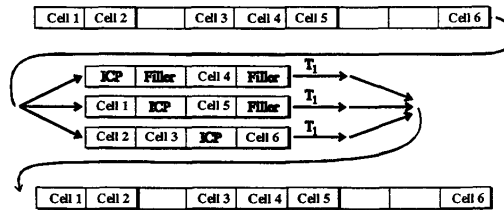


Figure 4. Inverse Multiplexing for ATM: ICP and Filler cell insertion. Cell distribution and reassembling according to a round-robin algorithm.

4. The IMUX Device Model

All these overhead cells have to be considered to dimension the IMUX resources. It means deciding which number of links are going to be in the IMA group and which be the number of buffers needed. For that purpose, some parameters have to be contemplated. The number of output links in the IMA group is chosen as a function of the bandwidth required. The buffer size has to be estimated according to the main QoS parameters agreed (basically the CLR and the CDV). Also, the buffer capacity depends on the traffic load applied to the device. The traffic load can be further divided into the actual ATM load the device has to process, and the overhead load due to the additional IMA control cells that has an impact on the performance offered by the IMUX as well.

To study the IMUX behavior under different traffic patterns, load conditions, number of output links and different buffer sizes, we have developed an IMUX simulator written in C++ [6]. It simulates independent IMUX devices as well as an end-to-end IMA group, implementing the receiver, too. We have also developed an analytical model to help in the IMUX dimensioning, obtaining mathematical expressions easy to compute that

approximate the CLR and the Mean Waiting Time for the ATM cells in the IMUX. The results obtained from computer simulation and the ones derived from the analysis are compared to appreciate the accuracy of our proposed approximations.

The IMUX is first modeled by an input queue of finite size B , and s identical output links, with a constant service time (ATM cells have constant length). Time is divided into slots of fixed duration (the cell transmission time), taken as the unity to simplify the analysis. As a first insight, we consider that cells arrive to the system according to a Poisson process. In this way, the IMUX device operation can be related to the discrete-time behavior of a $M/D/s/s+B$ queue system. However, the insertion of protocol cells (Filler, ICP and SICP cells) can be seen as an additional load, which (even though it is light) has to be characterized to get accurate results. Intuitively, it is easy to foresee that the CLR is going to be greater in the real IMUX (obtained by simulation) than the one achieved by solving the preliminary $M/D/s/s+B$ model. Three different approaches to find an equivalent analytical model for the CLR have been considered [6]:

- To increase the offered load ρ to the $M/D/s/s+B$ system with respect to the one offered to the IMUX, keeping constant the number of links s and the number of buffers B . Thus, the $M/D/s/s+B$ system receives more cells per unit of time with the same number of buffers, causing an increase in the CLR .
- To increase the number of links s in the $M/D/s/s+B$ model with respect to the ones in the IMUX, maintaining the number of buffers B , and the load per link ρ . Therefore, the input traffic $\rho \cdot s$ grows and the CLR also grows.
- To reduce the buffer size B in the $M/D/s/s+B$ queue regarding the one in the IMUX, keeping constant the number of links s and the offered load per link ρ . This directly causes an increase in the CLR .

These three options have been thought over. The c option has been developed in previous tasks [6, 7] and presents the advantage that reduces the system of $B+1$ equations with $B+1$ unknowns necessary to solve exactly the $M/D/s/s+B$ queue system [8]. The b option has been studied in [9]. A detailed explanation of both methods is out of the scope of this paper. Here, we present the first option, therefore we will know how much load the IMUX process: the load due to the cells coming from the ATM layer, as well as the fictitious overhead load in the IMUX due to the control protocol. We say fictitious since control cells are introduced during IMUX operation and they do not occupy memory. However, their insertion causes the storing and delay of ATM layer cells increasing the CLR . We try to capture this effect as an imaginary increasing in the applied load. Next Section describes how this

overhead load can be characterized.

5. The Overhead Load Added by Control Cells

We want to compute all the load processed by the IMUX, in order to find analytical models that characterize the *CLR* as a function of the buffer size, number of links and the load offered by ATM layer cells.

The IMUX device introduces ICP and SICP cells according to a fixed procedure as it was explained in Section 3: one of every 128 cells is an ICP cell and one of every 2048 is a SICP cell. The service times for ATM cells are deterministic and equal to one time slot unit. The total load applied to the system is $A = \lambda/\mu = \rho \cdot s$ Erlang, being λ the number of cells arriving to the system per unit of time, ρ the offered load per link, s the number of links, and $1/\mu \equiv 1$ the service rate. Then, the equivalent traffic load introduced by ICP and SICP cells is $A_{ICP} = (1/128) \cdot s$ and $A_{SICP} = (1/2048) \cdot s$ Erlang, respectively. In addition, there is the amount of load due to Filler cells, which we develop below. Finally, the total load processed by the IMUX can be seen as:

$$\rho_{total} = \rho + \frac{1}{128} + \frac{1}{2048} + \rho_{Filler} \quad (2)$$

In Equation (2), and for the rest of the paper, ρ denotes the load per output link coming from the ATM layer. At first glance, it is possible to think of that $\rho_{Filler} = 0$, since these cells are inserted in the ATM cell stream by the IMUX whenever they are needed, and thus, any buffer space is consumed [6]. However, the insertion of Filler cells can be also interpreted as an additional load. In fact, there are moments in which the IMUX has an available ATM layer cell ready to be transmitted, but the device has already decided to transmit a Filler cell instead. The IMA group constitutes a logical link which rate is equal to *IDCR*, see Equation (1). The IMUX checks for the introduction of an ATM cell at this rate, and if there is not any ATM cell when the check is done, the device inserts a Filler cell into the corresponding link instead. Nevertheless, in a $M/D/s/s+B$ system the number of cells to be transmitted is decided at the end of each time slot not at *IDCR* rate. This subtle difference is illustrated in Figure 5 [6].

We can see an example in Figure 6. If there is no ATM layer cell in the first decision instant, the IMUX introduces a Filler cell in the corresponding output link, although some ATM cells could arrive later during the same slot interval. Therefore, the *CLR* in the real IMUX is bigger than in the $M/D/s/s+B$ model, because it is possible that ATM layer cells must wait in the buffer of the IMUX while some Filler cells have occupied their possible places at the output links. So, it is as if there is an extra load due to the effect of the Filler cells. We refer to it as ρ_{Filler} .

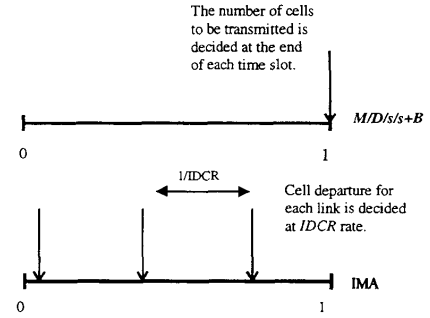


Figure 5. Cell departure moments for the $M/D/s/s+B$ and the IMA systems.

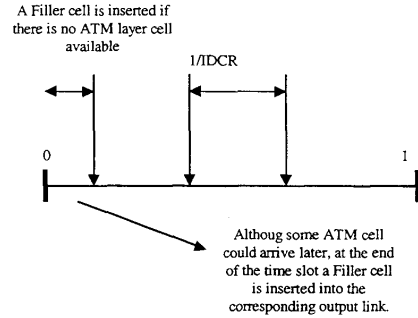


Figure 6. Filler cell insertion although some ATM cells could arrive during the time slot.

6. IMUX Dimensioning Issues and Approximation for the *CLR*

Whenever an IMUX designer needs to dimension the device resources, some parameters have to be considered. For instance, the number of output links in the IMA group for a required bandwidth, the number of buffers needed to guarantee the agreed values for the QoS parameters (Mean Waiting Time, *CDV* and *CLR*). Finally, the designer will have to decide the buffer threshold values for cell discarding if different levels of priority or different classes of service for the ATM traffic are supported [10, 11].

As it was explained in Section 4, a simulator which characterizes in detail the IMUX and the end-to-end IMA group behavior has been developed in [6]. We evaluate the *CLR* and Average Cell Delay as a function of the offered load, the buffer size and the number of lines that constitute the IMA group. In our simulations, we measure the performance of the device under medium and heavy load conditions, so the ATM applied load takes values between 50% and 90%. The number of links in the IMA group varies between 2 and 8, since this is the typical range used by the manufacturers because net managers

can not justify the cost of purchasing or leasing a greater number of T1/E1 lines in front of the T3/E3 link cost. The input buffer size is also a variable.

Simultaneously, we have developed an analytical model for the Mean Waiting Time and the *CLR* in the IMUX devices. The description used to obtain an estimate of the Mean Waiting Time, the complete methodology to dimension an IMUX device and the end-to-end study are out of the scope of this paper. Special attention is paid to the mathematical model that approximates the *CLR* in the IMUX.

The behavior of the IMA system is compared to the characteristics of the $M/D/s/s+B$ [11, 12] queue with an equivalent load per link equal to the total load processed by the IMUX, which is expressed in Equation (2). The extra load results of the insertion of Filler cells; ρ_{Filler} is empirically obtained, but provides an easy manner to compute the approximation for the *CLR* and, therefore, a simple way to dimension the system by means of solving a well known queue system.

Our proposed analytical model is based on a transform free approximation of the exact solution of the $M/D/s/s+B$ queue [8], avoiding solving the system of $B+1$ equations with $B+1$ unknowns resulting from the direct study of the state probabilities. This could be a tedious job specially if the buffer size, B , is big.

We use the approximation for the *CLR* in the continuous-time $M/D/s/s+B$ queue proposed by F. Barceló and M. Aguilar in [13]. We developed our approximation from [14] and from previous tasks of F. Barceló found in [10, 15]. If cells are assumed to arrive at the system according to a Poisson process, Poisson arrivals see time averages (PASTA property). It implies that the cell loss probability or *CLR* is the state probability of the congested system, P_{s+B} . For the continuous time $M/D/s/s+B$ queue [13, 14]:

$$CLR_{M/D/s/s+B}^{cont}(\rho, s, B) = P_{s+B}(M/D/s/s+B) \equiv \frac{PD}{1 - \rho \left(\rho_{eq} \right)^B PD} (1 - \rho) \left(\rho_{eq} \right)^B \quad (3)$$

Where PD is the delay probability in the continuous-time $M/M/s$ queue, given by the Erlang delay formula, $PD=C(s, \rho)$ and ρ_{eq} the equivalent load for the continuous $M/M/s$ queue that gives the same average queue length as in the $M/D/s$ queue. It has a simple expression as it can be seen in [13, 15].

To obtain the *CLR* in the discrete-time $M/D/s/s+B$ queue, it is suggested to add another amount that is known as CLR_{extra} [13]. In a discrete-time queue, time is slotted into intervals of fixed length (slots). This means that services

initiate at the beginning of each slot and cells leave the system at the end of the time slot. Cells also arrive to the system while services happen and they are gathered into the buffer, if there is any free position. On the other hand, in a continuous-time queue, cells are served (if there is any server free) as they arrive to the system. This accumulation of cells over each service interval cause an additional *CLR* amount with regard to the *CLR* in a continuous-time queue. The approximation proposed for the CLR_{extra} is extensively developed in [13] and its expression is given by Equation (4).

$$CLR_{M/D/s/s+B}^{extra}(\rho, s, B, \bar{Q}_D) \equiv 1 - e^{-\lambda \sum_{k=0}^{\lceil B - \bar{Q}_D + \lambda/2 - 1 \rceil} \frac{\lambda^k}{k!}} \equiv e^{-\lambda \lambda^L \left(\frac{L + \lambda + 1}{(L + 1)!} \right)} \quad (4)$$

Where $\bar{Q}_D(\rho, s)$ is the average queue length in the $M/D/s$ queue computed by approximation in [13, 15] from the average queue length in the $M/M/s$ one, and $L = \lceil B - \bar{Q}_D + \lambda/2 \rceil$, being $\lceil i \rceil$ the smallest integer greater than or equal to i .

Derivation of Equation (4) is completely detailed in [13], but at this point the main ideas for its understanding are outlined.

Since cells arrive according to a Poisson process, the probability of k cells arriving to the system during a service interval is:

$$\pi_k = \frac{\lambda^k e^{-\lambda}}{k!} \quad (5)$$

Being λ the offered load to the buffer or mean arrival rate. We assume that there are $\bar{Q}_D - \lambda/2$ cells into the buffer at the beginning of each time slot, where $\lambda/2$ is approximately the time average number of cell arrivals during the service interval [8]. Thus the number of free buffers for the incoming cells during the service interval is $B - (\bar{Q}_D - \lambda/2)$. Let $\bar{A}$ be the mean number of cells admitted in the buffer during one time slot, which can be understood as the mean admission rate in the buffer during a service time interval. Thus, we have:

$$\bar{A} = \sum_{k=1}^{\lceil B - \bar{Q}_D + \lambda/2 \rceil} k \pi_k \quad (6)$$

Then we formulate the next approximation for the extra *CLR*:

$$CLR^{extra}(\rho, s, B, \bar{Q}_D) \equiv \frac{\lambda - \bar{A}}{\lambda} = 1 - \frac{\bar{A}}{\lambda} \quad (7)$$

From Equations (6) and (7) and after elementary manipulations which are explained in [13], we arrive to the final expression in Equation (4).

Finally, we obtain the approximation for the CLR in a discrete-time $M/D/s/s+B$ proposed in [13], just adding Equations (3) and (4):

$$CLR_{M/D/s/s+B}^{discr}(\rho, s, B) \equiv CLR_{M/D/s/s+B}^{cont}(\rho, s, B) + CLR_{M/D/s/s+B}^{extra}(\rho, s, B) \quad (8)$$

Now, the total load ρ_{total} processed by an IMUX is going to be found in order to characterize the CLR in this device:

$$CLR_{IMUX}(\rho, s, B) \equiv CLR_{M/D/s/s+B}^{discr}(\rho_{total}, s, B) \quad (9)$$

The amount of additional load due to the Filler cells, ρ_{Filler} is obtained by using an experimental method. Its behavior has been observed in our IMUX simulator [6], as a function of the ATM load ρ , the buffer size B and the number of output links s . The values for ρ_{Filler} have been found from Equation (9), where $CLR_{IMUX}(\rho, s, B)$ are the CLR values for the IMUX obtained by simulation [6], and $CLR_{M/D/s/s+B}^{discr}(\rho, s, B)$ with $\rho = \rho_{total}$ are the values acquired by combining Equation (2) and (8). Finally, Equation (2) gives the values for $\rho_{Filler}(\rho, s, B)$. As a future objective, we will justify these values analytically. That is, with total independence from the simulations.

To get them easily, we have tabulated the results for $\rho_{Filler}(\rho, s, B)$, considering a wide range of values: $0.5 \leq \rho \leq 0.9$, $2 \leq s \leq 8$, $8 \leq B \leq 40$. As an example one can see in Table 1 and Table 2 the values for $\rho_{Filler}(s, B)$ for an ATM offered load per output link equal to 70% and 90%, respectively.

Figures 7 and 8 plot the distribution of $\rho_{Filler}(s, B)$ for an ATM applied load of 60% and 80% respectively. The dotted values are obtained by simulation and the continuous lines are also these values, but represented by an adequate decreasing exponential function for each case. It can be seen that both performances are very alike, and thus, these simple exponential functions can be used to express the $\rho_{Filler}(\rho, s, B)$ obtained from the simulator. It can be observed that this negative exponential behavior starts from a certain buffer amount, different for different values of ρ and s . There is no point in have this load characterized for lower values of B , because their corresponding CLR are too big (order of magnitude 10^2) comparing to the typical values of QoS required for ATM.

Thus, it has been obtained $a(s)$ and $b(s)$ for $\rho_{Filler}(s, B) = a(s) e^{-b(s)B}$ with $s=2, 4, 6$ and 8 as the number of output links, and then making a polynomial interpolation of the four values of $a(s)$ obtained in each case, to have a as a function of s . The same is done for $b(s)$, but in this case it is enough with a second degree polynomial. As an example, these expressions have been obtained for an IMUX 60% and 80% loaded:

$$\rho_{Filler}(\rho = 0.6, s, B) = (0.8538 - 0.2268s + 0.05744s^2 - 0.003735s^3) * e^{-(0.2017 - 0.03413s + 0.002082s^2)B} \quad (10)$$

$$\rho_{Filler}(\rho = 0.8, s, B) = (0.3078 - 0.05645s + 0.01461s^2 - 0.000879s^3) * e^{-(0.1506 - 0.02561s + 0.001616s^2)B} \quad (11)$$

As Figures 7 and 8 show the additional load due to Filler cells, ρ_{Filler} , decreases with the applied ATM load. This is because for heavy load there are more available ATM layer cells in the IMUX and therefore, it is not necessary to add so many Filler cells as under a light load condition.

Table 1. Additional load due to Filler cells, (ρ_{Filler}) for an IMUX with $\rho=0.7$.

$\rho=0.7$		$s=2$	$s=3$	$s=4$	$s=5$	$s=6$	$s=7$	$s=8$
B								
8		1.34E-01	1.48E-01	1.42E-01				
12		9.14E-02	1.43E-01	1.43E-01	1.66E-01	1.82E-01		
16		5.52E-02	9.34E-02	1.11E-01	1.49E-01	1.82E-01	1.84E-01	1.86E-01
20		3.49E-02	6.39E-02	7.69E-02	1.09E-01	1.43E-01	1.75E-01	1.85E-01
24		2.19E-02	4.50E-02	5.51E-02	8.09E-02	1.08E-01	1.35E-01	1.48E-01
28		1.28E-02	3.17E-02	3.99E-02	6.13E-02	8.36E-02	1.07E-01	1.17E-01
32		5.99E-03	2.19E-02	2.86E-02	4.68E-02	6.58E-02	8.56E-02	9.45E-02
36		7.85E-04	1.44E-02	1.98E-02	3.56E-02	5.21E-02	6.93E-02	7.70E-02
40					2.67E-02	4.12E-02	5.64E-02	6.31E-02

Table 2. Additional load due to Filler cells, (ρ_{Filler}) for an IMUX with $\rho=0.9$.

$\rho=0.9$		$s=2$	$s=3$	$s=4$	$s=5$	$s=6$	$s=7$	$s=8$
B								
12		2.19E-02	1.24E-02					
16		2.79E-02	3.53E-02	3.26E-02	2.56E-02	2.28E-02	1.74E-02	6.38E-03
20		1.74E-02	3.02E-02	3.52E-02	3.95E-02	4.01E-02	3.47E-02	2.79E-02
24		1.12E-02	2.10E-02	2.55E-02	3.61E-02	4.50E-02	4.54E-02	4.11E-02
28		7.14E-03	1.51E-02	1.87E-02	2.72E-02	3.61E-02	4.52E-02	4.73E-02
32		4.30E-03	1.11E-02	1.40E-02	2.11E-02	2.84E-02	3.60E-02	3.96E-02
36		2.20E-03	7.86E-03	1.05E-02	1.65E-02	2.28E-02	2.93E-02	3.23E-02
40		5.78E-04	5.60E-03	7.82E-03	1.31E-02	1.86E-02	2.42E-02	2.68E-02

Looking over each of these Figures, it can be seen that ρ_{Filler} grows if the number of output links s increases. When the number of channels increases, the $IDCR$ rate also grows, as it can be seen in Equation (1) where $N_{on}=s$. And therefore, the time between the insertion instants of Filler cells, that is $1/IDCR$, decreases. So, more often we have decision instants, and thus, the insertion of a Filler cell when there is no ATM layer cell, is more probable.

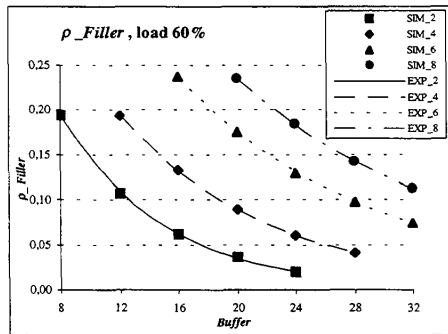


Figure 7. Exponential distribution of ρ_{Filler} for an IMUX 60% loaded.

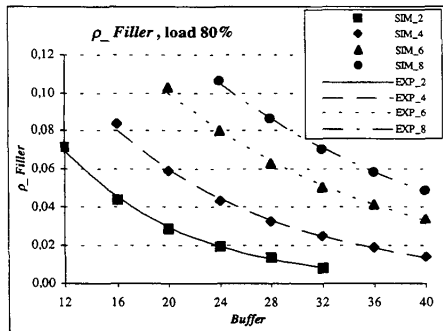


Figure 8. Exponential distribution of ρ_{Filler} for an IMUX 80% loaded.

Finally, it can be observed that ρ_{Filler} decreases as the buffer size increases. For a big number of buffers, less ATM layer cells are lost, and there are more available ATM cells in the buffer. Therefore, it is necessary to insert less Filler cells to maintain the output links busy. This effect is more pronounced for high loads, because the probability of ATM layer cell generation augments and there are more ATM layer cells in the buffer.

7. Numerical Results

In Figures 9 and 10, it can be observed the CLR as a function of the buffer size and the number of output links

in an IMUX device. The dotted values are obtained by simulation while the continuous lines are computed using our approximation inferred from Equations (2), (8), (10) and (11). Looking at these Figures, a good agreement between the proposed estimate and the simulation results can be noticed. It is also true for the remaining applied load values.

In Figure 9, we plot both, simulated and analytical results for the CLR in an IMUX where each link is 60% loaded and the buffer capacity takes values from 8 to 28 cells. In Figure 10, it can be seen the CLR for an IMUX with an ATM load equal to 80% and a buffer size ranging from 8 to 40 cells. In both cases, the IMA system has 2, 4, 6 and 8 output links.

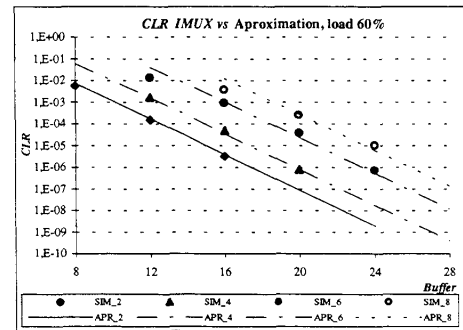


Figure 9. CLR for an IMUX 60% loaded.

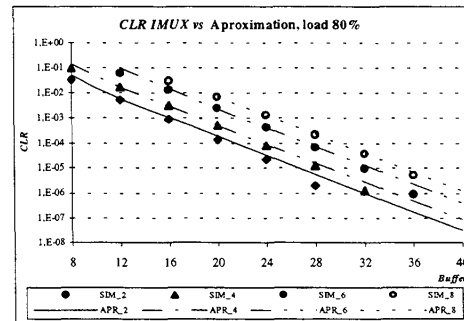


Figure 10. CLR for an IMUX 80% loaded.

The minimum CLR achieved in our simulations is in the order of magnitude of 10^{-6} because no more than ten million cells has been processed due to time computing limitations. From the study of all the results, it can be concluded that the cell loss probability or CLR depends on the applied load, number of output links and buffer size. The CLR decreases with the buffer size, but slower as the load grows, and therefore the slope is smoother. Note that for high loads, an increase in the number of output links

has less influence than for low loads.

An IMUX designer could use easily the proposed methodology for dimensioning these devices. As an example, let us consider an IMUX device which has to provide a bandwidth of 6 Mbps and a cell loss probability lesser or equal than 10^{-5} for an offered load per link of 80%. In this case, and assuming Poisson cell arrivals, it is enough to lease 4 individual T1/E1 lines and an IMUX buffer 28 cells deep, as it can be deduced from Figure 10. Note that once an equivalent analytical scheme is elaborated, it is not necessary to execute costly simulations.

8. Conclusions and Future Work

In this paper, the main features of an IMUX device are outlined, how it works, the main network configurations it has been thought for, and the problems it presents when an analytical model is developed to help in its dimensioning. The IMUX performance is evaluated under different load conditions, different number of output links and number of buffers. Finally, a simple methodology to dimension its main parameters (number of channels and buffer size) is proposed as a function of the required *CLR*.

The performance of the IMA system is studied aided by an IMUX simulator designed in [6]. It simulates IMA systems according to the ATM Forum IMA specification [3]. An analysis of the insertion of control cells (ICP, SICP and Filler cells) for representative values of the number of output lines is also conducted.

As a first insight, it is considered that cells arrive to the system according to a Poisson process. This is a reasonable hypothesis when the exact arrival process is unknown and it presents a small coefficient of variation (not too greater than the unity), as it happens when the process is not very bursty and there is a great level of mixture in the aggregated traffic at high levels of the network hierarchy [11, 16].

Currently, we are working towards the validity of our model under several types of traffic, such as bursty traffic, corporate and residential traffic models. Some of them presenting self-similar behavior and disperse distribution functions.

We are also studying the application of different mathematical models based on the exact and approximate resolution of the system of equations obtained from the Markov chain characterizing the IMUX operation. We have an special interest to derive expressions easy to compute for the *CLR* and the average cell delay as a function of buffer size, number of output links and offered load. On the other hand, we are also examining the impact of various levels of priority and buffer scheduling policies to support different ATM traffic classes.

The resulting analytical expressions will be compared and validated with the results obtained by computer simulation. The final goal is to develop a methodology to dimension IMUX resources under multiple conditions by using simple formulas and avoiding the need to carry on costly simulations. In addition, we are investigating how to iterate these formulas to help in the planning of a complete ATM network composed of IMA systems.

9. Acknowledgements

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