

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 10,541,334

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,541,334**

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LIST OF EXHIBITS

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Ex. 1004	File History of U.S. Patent No. 10,541,334
Ex. 1005	U.S. Patent Publication No. 2012/0153387 to Murthy et al. (“Murthy”)
Ex. 1006	U.S. Patent Publication No. 2015/0053928 to Ching et al. (“Ching”)
Ex. 1007	U.S. Patent Publication No. 2015/0035017 to Wann <i>et al.</i> (“Wann”)
Ex. 1008	U.S. Patent Publication No. 2014/0335674 to Liao <i>et al.</i> (“Liao”)
Ex. 1009	U.S. Patent Publication No. 2011/0147842 to Cappellani <i>et al.</i> (“Cappellani”)
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Ex. 1012	U.S. Patent Publication No. 2015/0137181 to Basker <i>et al.</i> (“Basker”)
Ex. 1013	U.S. Patent Publication No. 2016/0181366 to Oh <i>et al.</i> (“Oh”)
Ex. 1014	U.S. Patent No. 9,379,108 to Wann <i>et al.</i> (“Wann-108”)
Ex. 1015	Neaman, <u>Semiconductor Physics and Devices (Third Edition)</u> , 2003 (“Neaman”)
Ex. 1016	Hisamoto et al., <u>FinFET- A self-Aligned Double-Gate MOSFET Scalable to 20 nm</u> , IEEE Transactions on Electronic Devices, Vol. 47, No 12, December 2000 (“Hisamoto”)
Ex. 1017	Plummer <i>et al.</i> , <u>Silicon VLSI Technology, Fundamentals, Practice and Modeling</u> , 2000

Ex. 1018	Leobandung <i>et al.</i> , <u>Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Chanel Effects</u> , J. Vac. Sci. Technol. B 15(6), Nov/Dec 1997 (“Leobandung”)
Ex. 1019	Tang <i>et al.</i> , <u>FinFET – A Quasi-Planar Double-Gate MOSFET</u> , 2001 IEEE International Solid-State Circuits Conference, 2001 (“Tang”)
Ex. 1020	Thelander <i>et al.</i> , <u>Nanowire-Based One-Dimensional Electronics</u> , MaterialsToday Vol. 9, No. 10, October 2006 (“Thelander”)
Ex. 1021	Iwai, <u>Roadmap for 22nm and Beyond</u> , Microelectron. Eng. 2009 (Iwai)
Ex. 1022	Memorandum from Director Vidal (dated June 21, 2022)
Ex. 1023	Docket Control Order (dated Dec. 12, 2022)
Ex. 1024	RESERVED
Ex. 1025	Exhibit A of Daedalus’ Initial Infringement Contentions, <i>Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al</i> , Case No. 2:22-CV-353 (E.D. Tex. Sep. 12, 2022)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) requests *inter partes* review of claims 1, 2, 5-8, 10-14, 16-18, and 20 (“the challenged claims”) of U.S. Patent No. 10,541,334 (“the ’334 patent”) (Ex. 1001), which, according to PTO records, is assigned to Daedalus Prime LLC (“Patent Owner” or “PO”). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC.

Related Matters

The ’334 patent is at issue in *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al*, Case No. 2:22-CV-00353.

Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Howard Herr (*pro hac vice* to be filed). Service information is Paul Hastings LLP,

2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,
email: PH-Samsung-Daedalus-IPR@paulhastings.com. Petitioner consents to
electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge any fees due during this proceeding to
Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '334 patent is available for review and Petitioner
is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1, 2, 5-8, 10-14, 16-18, and 20 should be canceled as unpatentable
based on the following grounds:

Ground 1: Claims 1, 2, 5-8, 10, 12-14, and 16 are anticipated under 35 U.S.C.
§ 102 based on Murthy (Ex. 1005);

Ground 2: Claim 12 is obvious under 35 U.S.C. § 103 based on Murthy and
Kuhn (Ex. 1010);

Ground 3: Claims 11, 17, 18, and 20 are obvious under 35 U.S.C. § 103 based
on Murthy and Ching (Ex. 1006);

Ground 4: Claims 1, 2, 6-8, 10, and 12-14 are anticipated under 35 U.S.C. §

102 based on Wann (Ex. 1007);

Ground 5: Claim 12 is obvious under 35 U.S.C. § 103 based on Wann and Kuhn;

Ground 6: Claims 11, 17, and 18 are obvious under 35 U.S.C. § 103 based on Wann and Ching;

Ground 7: Claims 1, 2, 5-7, 10, and 12 are obvious under 35 U.S.C. § 103 based on Wann and Liao (Ex. 1008);

Ground 8: Claim 12 is obvious under 35 U.S.C. § 103 based on Wann, Liao, and Kuhn;

Ground 9: Claim 11 is obvious under 35 U.S.C. § 103 based on Wann, Liao, and Ching;

Ground 10: Claims 1, 2, 5-7, 10, and 12 are obvious under 35 U.S.C. § 103 based on Wann in view of Cappellani (Ex. 1009);

Ground 11: Claim 12 is obvious under 35 U.S.C. § 103 based on Wann, Cappellani, and Kuhn; and

Ground 12: Claim 11 is obvious under 35 U.S.C. § 103 based on Wann,

Cappellani, and Ching.¹

The '334 patent claims priority to an application filed March 21, 2014. (Ex. 1001, Cover.) Petitioner assumes for this proceeding only, without conceding, that the earliest effective filing date of the '334 patent is March 21, 2014.

Murthy published June 21, 2012, Cappellani published June 23, 2011, and Kuhn published June 7, 2012. Ching was filed August 20, 2013, Wann was filed July 31, 2013, and Liao was filed May 13, 2013. Therefore, Murthy, Cappellani, and Kuhn are prior art under 35 U.S.C. § 102(a)(1), while Ching, Wann, and Liao are prior art under 35 U.S.C. § 102(a)(2).

None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

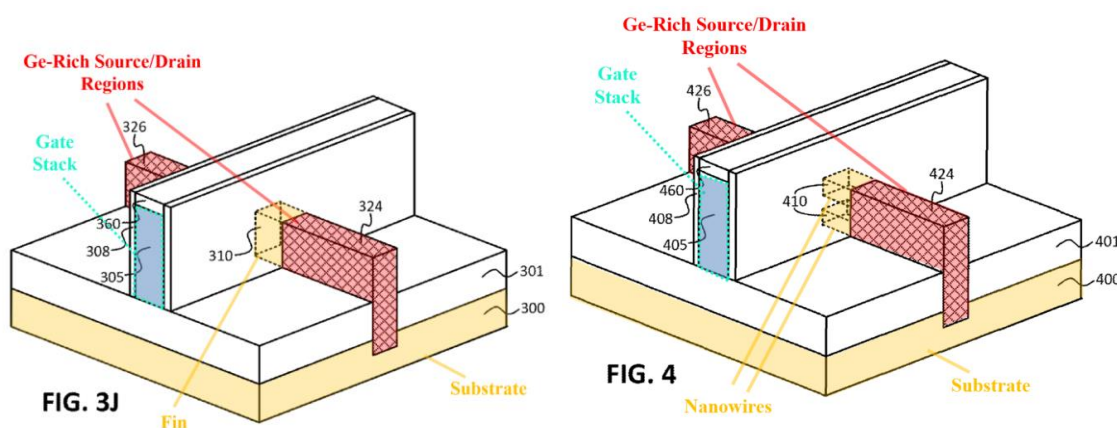
A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the '334 patent would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics,

¹ Other references discussed herein are provided to show the state of the art at the time of the alleged invention of the '334 patent.

electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. (Ex. 1002, ¶¶16-17.)² More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '334 PATENT

The '334 patent discloses the use of germanium-rich material in source/drain regions of transistors, including planar and non-planar transistors (e.g., FinFETs and nanowire transistors), in order to reduce contact resistance and improve performance. (Ex. 1001, 1:61-63, 2:21-26, 2:10-14; Ex. 1002, ¶¶29-33.) Annotated figures 3J and 4A below show such a FinFET and nanowire transistor, respectively.



(Ex. 1001, FIGs. 3J, 4 (annotated); Ex. 1002, ¶¶[0031], [0033].)

² Petitioner submits the declaration of Dr. Stanley Shanfield (Ex. 1002), an expert in the field of the '334 patent. (*Id.*, ¶¶5-12; Ex. 1003.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; see also *id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

IX. Detailed Explanation of Unpatentability

A. Ground 1 – Murthy Anticipates Claims 1, 2, 5-8, 10, 12-14, and 16

1. Claim 1

a) “An integrated circuit, comprising:”

To the extent the preamble is limiting, Murthy discloses the limitations therein. (Ex. 1002, ¶¶35-37, 51-52.) Murthy discloses transistors included on a semiconductor substrate with other devices, where the substrate including those devices is “an integrated circuit.” (Ex. 10015, ¶[0001]; see also *id.*, [0045]; Ex. 1002, ¶51.) Murthy further discloses a FinFET transistor included on the

semiconductor device (“integrated circuit”). (Ex. 1005, ¶[0009] (“FIG. 4 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.”), ¶¶[0013] [0050]-[0053], [0056], claims 1, 2; Ex. 1002, ¶52.)

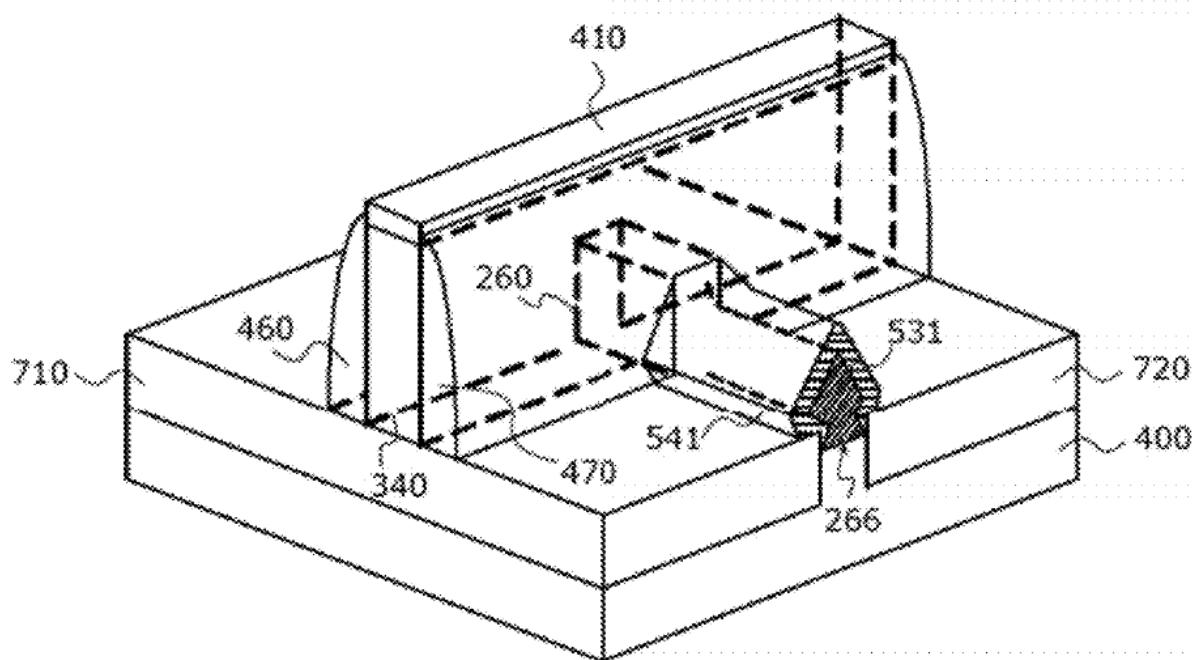


FIG. 4

(Ex. 1005, FIG. 4.)

b) “a non-planar body comprising semiconductor material, wherein the non-planar body has top and side surfaces;”

Murthy discloses this claim limitation. (Ex. 1002, ¶¶53-54.) As shown in annotated figure 4 below, Murthy’s FinFET includes a substrate 400, which is etched to form a fin 260 made of semiconductor material that constitutes a “non-planar body.” (Ex. 1005, ¶[0051] (“As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin).”), ¶¶[0052], [0056], claims 1, 2; Ex. 1002, ¶53.) The fin 260 being a “non-planar body” is consistent with claim 10 of the ’334 patent, which recites “the non-planar body is a fin.” (Ex. 1001, claim 10; section IX.A.7.)

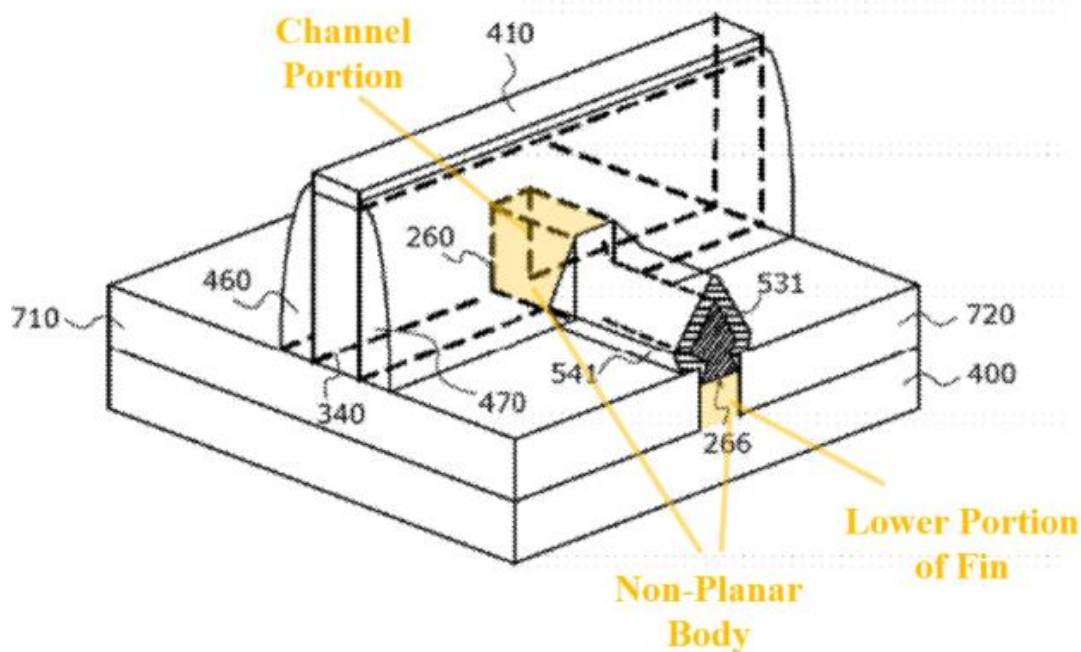


FIG. 4

(Ex. 1005, FIG 4 (annotated); Ex. 1002, ¶53.)

Murthy’s fin has top and side surfaces. (Ex. 1005, ¶[0051] (“current runs along both sidewalls of the fin...as well as along the top of the fin”), ¶[0052], [0056], FIG. 4; Ex. 1002, ¶54.)

c) “a gate structure on at least the top and side surfaces of the non-planar body;”

Murthy discloses this limitation. (Ex. 1002, ¶55.) For example, as shown in annotated figure 4 below, Murthy discloses a gate electrode 340 on the top and side surfaces of the channel portion of the fin (“non-planar body”), where the gate

electrode is separated from the fin by a gate dielectric. (Ex. 1005, ¶[0051], ¶[0052] (“A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates.”), ¶[0056], FIG. 4, claims 1, 2; Ex. 1002, ¶55.) The gate electrode 340 and gate dielectric constitute a “gate structure,” which is formed on the top and side surfaces of the fin. (Ex. 1002, ¶55.)

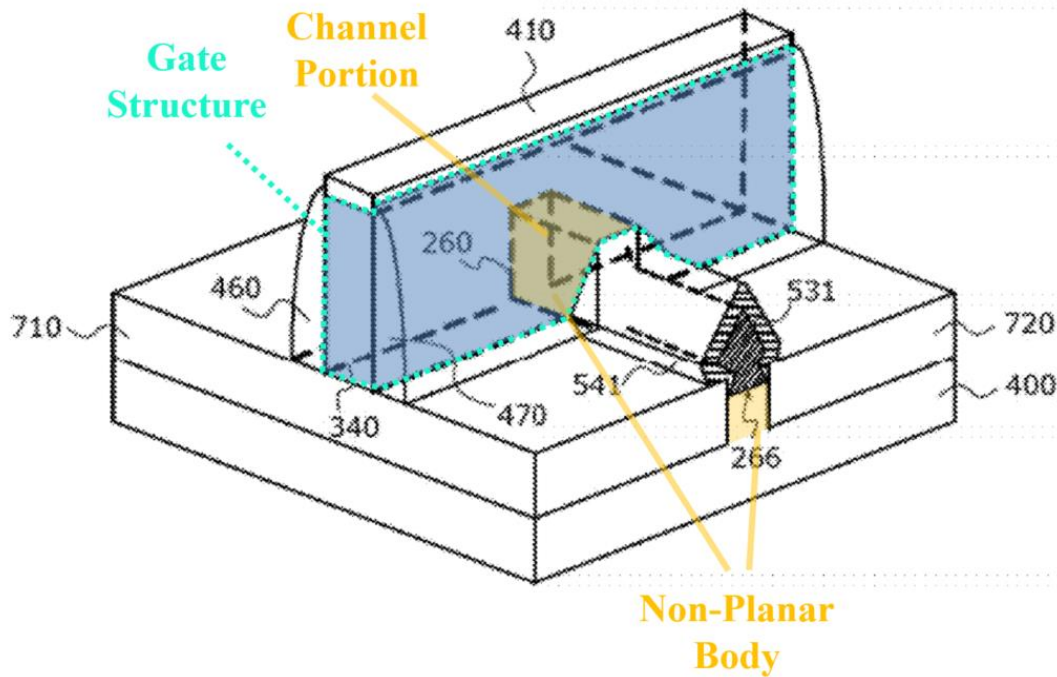


FIG. 4

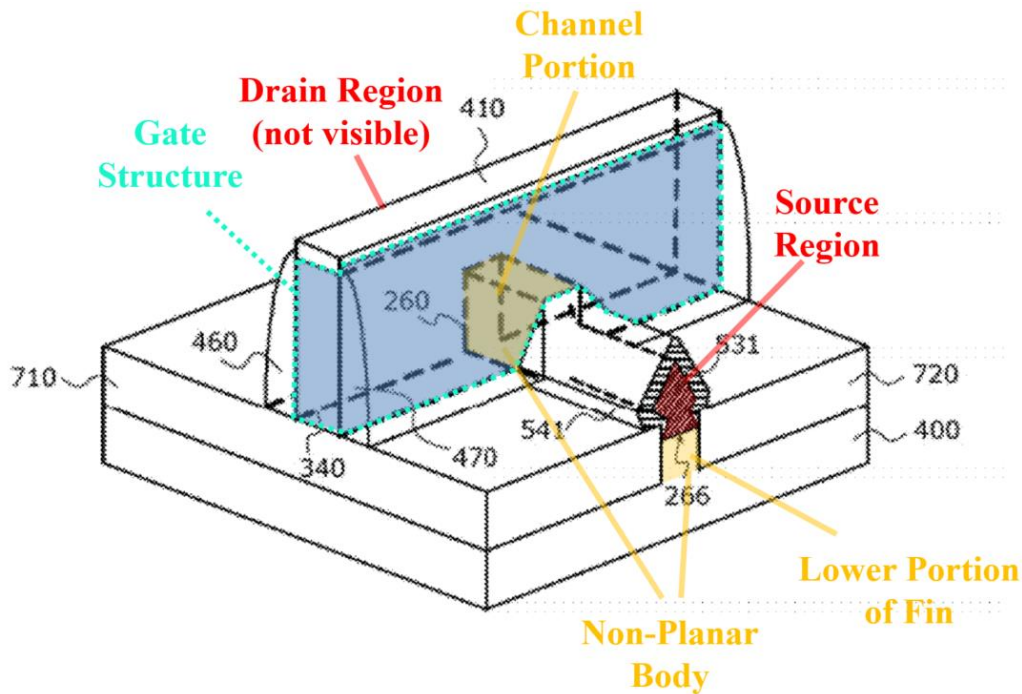
(Ex. 1005, FIG. 4 (annotated); Ex. 1002, ¶55.)

d) “a source region adjacent the non-planar body, the source region including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon; and”

e) “a drain region adjacent the non-planar body, the drain region including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with a surface that consists essentially of silicon.”

Murthy discloses these features to the extent they can be understood.³ (Ex. 1002, ¶¶56-58.) For example, Murthy discloses a source region on one fin sidewall and a drain region on the opposite fin sidewall, where the source/drain regions include epitaxial regions 531. (Ex. 1005, ¶[0051]-[0052], ¶[0056] (“The device further includes source and drain regions formed in the substrate and adjacent to the channel region.”), FIG. 4, claims 1, 2; Ex. 1002, ¶56.)

³ While it is unclear what “consists essentially of silicon” requires, the present Petition maps this claim feature to a portion of a silicon substrate, which discloses this claim feature under any reasonable interpretation.



(Ex. 1005, FIG. 4 (annotated); Ex. 1002, ¶56.)

The epitaxial regions (“first/second portions”) of the source/drain regions are “adjacent to the non-planar body” as they lie on top of the lower portion the fin and abut the channel portion of the fin. (Ex. 1005, ¶¶[0052], [0056]; Ex. 1002, ¶57.) Substrate 400, and hence the fin formed by etching the substrate, is silicon or silicon-on-insulator (SOI), so each of the epitaxial regions is in direct contact with a side surface of the channel portion and the top surface of the lower portion of the fin (“a surface that consists essentially of silicon”). (Ex. 1005, ¶[0019], ¶[0052]; Ex. 1002, ¶57.)

Murthy further discloses implementing the epitaxial regions 531 (“first/second portions”) with germanium or silicon germanium with nearly 100% germanium (e.g., 95% or more germanium) such that they include “germanium at a concentration of at least 50 atomic percent throughout the [first/second] portion.” (Ex. 1005, Abstract, (“**Germanium concentration can be**, for example, in excess of 50 atomic % and **up to 100 atomic %**”)⁴, ¶[0042] (“In some example embodiments, a **germanium concentration of 95 atomic % and up to pure germanium (100 atomic %)** can be used to achieve such benefits.”), ¶¶[0013], [0018], [0020], [0041], [0048], [0053], [0056], [0059], claims 1, 2; Ex. 1002, ¶58.)

2. Claim 2

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

Murthy discloses this limitation. (Ex. 1002, ¶59.) As discussed above for claim elements 1[d]-[e], the epitaxial regions (“first/second portions”) of the source/drain regions are in direct contact with the channel portion of the fin and the underlying lower portion of the fin, both of which are formed from the silicon or

⁴ Emphasis added unless otherwise noted.

silicon-on-insulator (SOI) substrate. (Ex. 1005, ¶¶[0019], [0028], [0052]; Ex. 1002, ¶59.) Therefore, the “surface,” which corresponds to either the channel portion side surface or the upper surface of the lower portion of the fin is a surface of “a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate” as claimed. (Ex. 1002, ¶59; *see also* Ex. 1001, 5:35-40; Ex. 1015, 103, 115; Ex. 1017, 93-97.)

3. Claim 5

“The integrated circuit of claim 1, wherein the first and second portions further include one or both of silicon and tin.”

Murthy discloses this limitation. (Ex. 1002, ¶¶60-61.) Murthy discloses that, for embodiments that do not use pure germanium for the epitaxial regions (“first and second portions”), the epitaxial regions can be silicon-germanium with nearly 100% (e.g., 95%+) germanium, where a small percentage of silicon is included in the silicon-germanium epitaxial regions. (Ex. 1005, Abstract (“boron doped germanium, or alternatively, **boron doped silicon germanium** ... are provided using selective epitaxial deposition in the source and drain regions ... **germanium concentration can be, for example,** in excess of 50 atomic % and **up to 100 atomic %**”), ¶[0042] (“In some example embodiments, a **germanium concentration of 95**

atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.”), ¶¶[0053], [0056], [0058]; Ex. 1002, ¶60.)

4. Claim 6

“The integrated circuit of claim 1, wherein the first and second portions include a p-type dopant.”

Murthy discloses this limitation. (Ex. 1002, ¶¶62-63.) Murthy discloses that the epitaxial portions (“first and second portions”) are doped with boron, which is a p-type dopant. (Ex. 1005, Abstract, ¶¶[0013], [0020], [0041]-[0042], [0048], [0053], [0059], [0056] (“the source and drain regions comprise a boron doped germanium layer”); Ex. 1001, 2:60-64; Ex. 1002, ¶¶62-63.)

5. Claim 7

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is undoped.”

Murthy discloses this limitation. (Ex. 1002, ¶64.) As discussed above for claim elements 1[d]-[e] and claim 2, the “surface that consists essentially of silicon” is part of the silicon substrate, which can be bulk silicon or a silicon on insulator substrate. (Sections IX.A.1(d)-(e), IX.A.2; Ex. 1005, ¶¶[0019], [0028], [0052]; Ex. 1002, ¶64.) A POSITA would have understood that, absent any indication that the substrate is doped, bulk silicon material is “undoped.” (Ex. 1005, ¶[0043]; Ex. 1002, ¶64; *see also* Ex. 1015, 103, 115; Ex. 1017, 93-97.) Such an understanding is

consistent with PO's infringement contentions. (Ex. 1025, 48 ("comprised of undoped silicon from bulk substrate.").)

6. Claim 8

"The integrated circuit of claim 1, further comprising an additional portion on the first and second portions, the additional portions including a metal and germanium."

Murthy discloses this limitation. (Ex. 1002, ¶¶65-67.) For example, consistent with the disclosure of the '334 patent (Ex. 1001, 10:34-61), Murthy discloses forming metal-germanide contacts ("additional portions including a metal and germanium") on the epitaxial regions ("first and second portions") of the source and drain regions. (Ex. 1005, ¶[0048], ¶[0056] ("In another such case, the device may include metal-germanide source and drain contacts."), claim 3; Ex. 1002, ¶¶65, 67.) Murthy further discloses how to form such metal-germanide contacts on the source/drain regions, where metal is deposited on the germanium or silicon-germanium with nearly 100% germanium (e.g., 95%+) epitaxial regions, and then annealing is performed to form a germanide. (Ex. 1005, ¶[0048]; Ex. 1002, ¶66.)

7. Claim 10

"The integrated circuit of claim 1, wherein the non-planar body is a fin, the fin between portions of the gate structure."

Murthy discloses this limitation. (Ex. 1002, ¶68.) As discussed with respect to claim 1, the fin that extends upward from the planar surface of the substrate

constitutes the claimed “non-planar body.” (Section IX.A.1(b).) Murthy discloses that the “gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates.” (Ex. 1005, ¶[0052]; section IX.A.1(c).) Therefore, the fin is “between portions of the gate structure.” (Ex. 1002, ¶68.)

8. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

Murthy discloses this limitation. (Ex. 1002, ¶¶69-70.) As discussed above for claim element 1[a], Murthy discloses transistors that are included on a semiconductor substrate with other devices, where the substrate that includes those devices is “an integrated circuit.” (Section IX.A.1(a); Ex. 1005, ¶[0001] (“circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate”).) A circuit device that includes that includes Murthy’s FinFET transistor is a “computing system” in a manner consistent with the ’334 patent, as such a circuit device is an electronic device that includes an interconnected set of components and “employs one or more transistor devices” that includes the features of claim 1. (Ex. 1001, 14:14-23 (“computing system 1000 ... the system 1000 may be **any other electronic device that processes data or employs one or more transistor devices as variously described herein**”); Ex. 1002, ¶70.)

9. Claim 13

a) “An integrated circuit, comprising:”

To the extent the preamble is limiting, Murthy discloses the limitations therein for the same reasons discussed above for claim element 1[a]. (Section IX.A.1(a); Ex. 1002, ¶71.)

b) “a fin structure comprising semiconductor material, wherein the fin structure has top and side surfaces;”

Murthy this claim limitation. (Ex. 1002, ¶72.) Murthy discloses a “fin structure” with top and side surfaces for the same reasons discussed above for the “non-planar body” recited in claim 1. (Section IX.A.1(b); Ex. 1002, ¶72.)

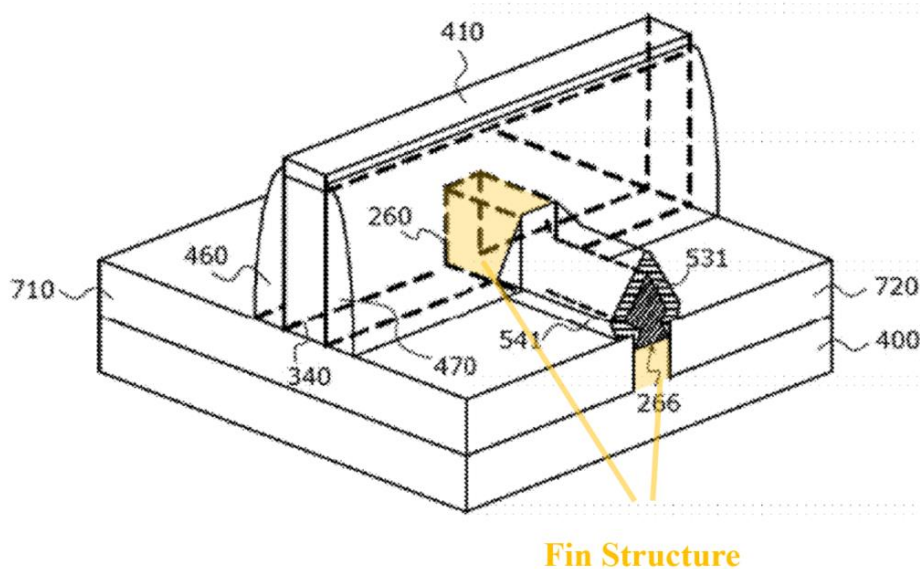


FIG. 4

(Ex. 1005, FIG. 5 (annotated); Ex. 1002, ¶72.)

c) “a gate structure on the top and side surfaces of the fin structure;”

Murthy discloses this limitation for the same reasons discussed above for claim element 1[c], where the gate structure covers the top and side surfaces of the channel portion of the “fin structure.” (Section IX.A.1(c); Ex. 1002, ¶73.)

d) “a source structure to one side of the gate structure and abutting the fin structure, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”

e) “a drain structure to an opposite side of the gate structure and abutting the fin structure, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon; ”

Murthy discloses these features to the extent they can be understood.⁵ (Ex. 1002, ¶74.) As discussed above for claim elements 1[d] and 1[e], Murthy discloses a source region (“source structure”) on one fin sidewall and a drain region (“drain structure”) on the opposite fin sidewall. (Sections IX.A.1(d)-(e).) Because the

⁵ See note 3 above.

source/drain regions are on sidewalls of the fin structure and the top of a lower portion 266 of the fin, the source and drain regions abut the “fin structure.” (Sections IX.A.1(d)-(e), IX.A.9(b); Ex. 1002, ¶74.) As also discussed above, Murthy discloses forming epitaxial regions (“first/second portion”) of the source/drain regions that include “at least 50 atomic percent” germanium throughout, where each of the epitaxial regions is in direct contact with the top surface of the underlying lower portion of the fin and the channel region, both of which “consist essentially of silicon.” (Sections IX.A.1(d)-(e), IX.A.9(b); Ex. 1002, ¶74.)

f) “a first contact structure on the first portion of the source structure and including a metal-germanide; and”

g) “a second contact structure on the second portion of the drain structure and including a metal-germanide. ”

Murthy discloses these features. (Ex. 1002, ¶75.) For example, as discussed above for claim 8, Murthy discloses forming metal-germanide source/drain contacts (“first/second contact structure”) on the epitaxial regions (“first/second portion of the source/drain structure”). (Section IX.A.6; Ex. 1002, ¶75.)

10. Claim 14

“The integrated circuit of claim 13, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

Murthy discloses this limitation for the same reasons discussed above for claim 2. (Ex. 1002, ¶76; section IX.A.2.)

11. Claim 16

“The integrated circuit of claim 13, wherein the first and second portions further include one or both of silicon and tin, and further include a p-type dopant.”

Murthy discloses these features for the same reasons discussed above for claims 5 and 6. (Sections IX.A.3-4; Ex. 1002, ¶77.)

B. Ground 2 – Murthy in View of Kuhn Renders Claim 12 Obvious

1. Claim 12⁶

Murthy in combination with Kuhn discloses or suggests this feature. (Ex. 1002, ¶¶78-81.) As discussed above in section IX.A.8, Murthy discloses a circuit device that includes Murthy’s non-planar transistor, which constitutes a “computing system” in a manner consistent with the ’334 patent. (Section IX.A.8.) To the extent PO argues that Murthy does not disclose a “computing system,” Kuhn discloses

⁶ The claim language is not repeated.

using non-planar transistors on integrated circuits in a computing system, and a POSITA would have found it obvious to use Murthy's transistor in a computing device as disclosed by Kuhn. (Ex. 1002, ¶78.)

Kuhn is in a similar field as Murthy as it discloses non-planar transistors that include silicon-germanium source/drain regions, and therefore a POSITA implementing a transistor like that disclosed by Murthy would have reason to look to Kuhn. (Ex. 1010, ¶¶[0011]-[0015]; Ex. 1002, ¶79.) Kuhn discloses that the non-planar transistors can be used in integrated circuits included in computing systems. (Ex. 1015, ¶[0038] (“FIG. 6 shows a computer system according to an embodiment.”), ¶[0039] (“One or more of the components shown in system 600 may include one or more nanowire devices of the various embodiments included herein.”), ¶¶[0040]-[0041], FIG. 6; Ex. 1002, ¶80.)

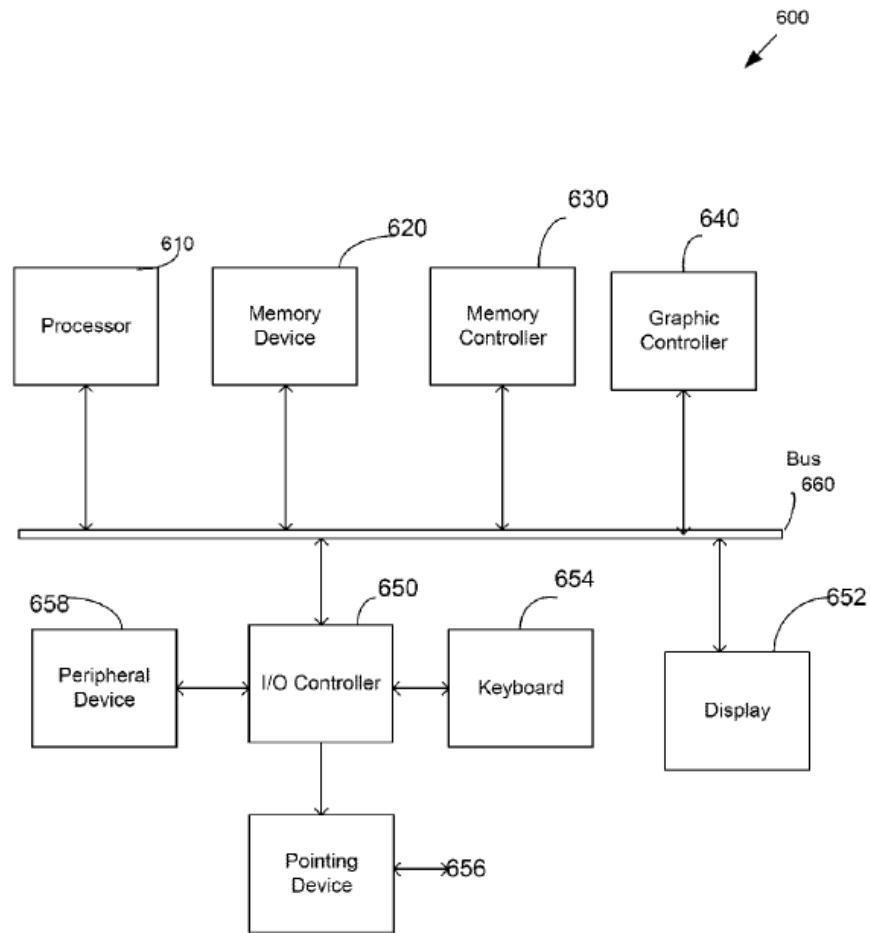


FIG. 6

(Ex. 1010, FIG. 6.)

In view of Kuhn and a POSITA's knowledge, a POSITA would have found it obvious to implement a non-planar transistor like that disclosed by Murthy in a computing device. (Ex. 1002, ¶81.) A POSITA would have known that transistors are used in integrated circuit devices that are included in computing devices. (*Id.*)

Such a skilled person would have been motivated to include Murthy's transistor in a computing system in order to provide utility to the transistor, and, based on Kuhn's disclosure and their knowledge, would have had a reasonable expectation of success. (*Id.*)

C. Ground 3 – Murthy in View of Ching Renders Claims 11, 17, 18, and 20 Obvious

1. Claim 11

“The integrated circuit of claim 1, wherein the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons.”

Murthy in combination with Ching discloses or suggests these features. As discussed above in section IX.A.1, Murthy discloses a FinFET that includes a “non-planar body” in the form of a fin. (Ex. 1002, ¶¶82-92; Section IX.A.1(b).) Murthy does not explicitly disclose nanowires or nanoribbons, but Ching discloses a fin-based non-planar structure similar to that of Murthy that uses nanowires, and, in view of Ching and their knowledge, a POSITA would have found it obvious to implement a non-planar transistor like Murthy's using nanowires. (Ex. 1002, ¶82.)

Ching, like Murthy, discloses a fin-based transistor where a channel region separates source and drain regions that include epitaxially-formed material. (Ex. 1006, ¶¶[0001], [0019], [0021]; Ex. 1002, ¶¶41-43, 83.) Rather than a fin-shaped

channel with a gate structure on the top and sides, Ching's nanowire transistor includes multiple nanowires within the channel, where the gate completely surrounds each nanowire in a "gate-all-around structure." (Ex. 1006, ¶¶[0024], [0025], Ex. 1002, ¶84; *see also* Ex. 1011, ¶[0044].) Ching's device 500 with epitaxially-grown material in the source/drain regions on either side of a nanowire channel is shown below. (Ex. 1006, ¶¶[0021]-[0023], [0030]-[0032]; Ex. 1002, ¶84.)

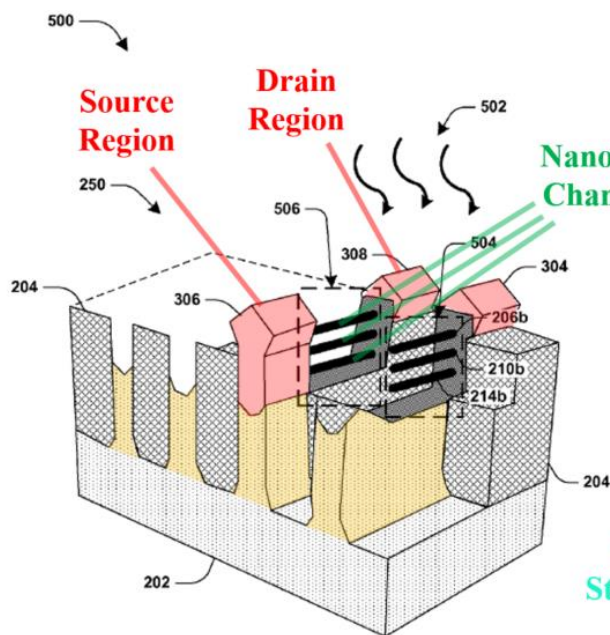


FIG. 5

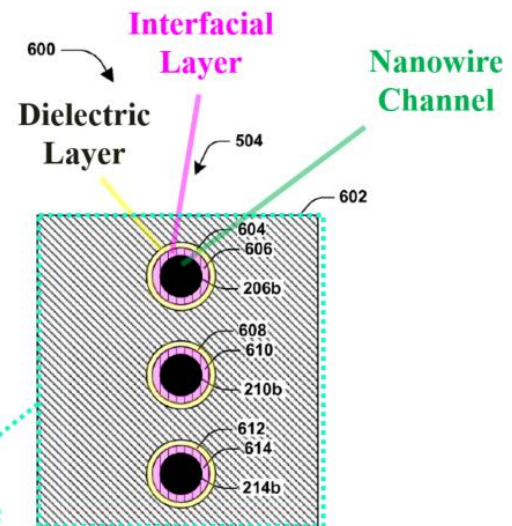


FIG. 6

(Ex. 1006, FIGs. 5, 6 (annotated); Ex. 1002, ¶84.)

Ching discloses that the gate-all-around structure increases gate control for the transistors. (Ex. 1006, ¶¶[0001], [0025]; Ex. 1002, ¶85; *see also* Ex. 1011, ¶[0044].)

A POSITA implementing a FinFET device like that disclosed by Murthy would have looked to Ching, particularly because Murthy and Ching are references in the same field and disclose fin-based devices with epitaxially grown source/drain regions on either side of a channel. (Ex. 1002, ¶86.) Having looked to Ching, a POSITA would have found it obvious to implement the channel of a fin-based device like that of Murthy such that it includes one or more nanowires like those disclosed by Ching. (*Id.*) As disclosed by Ching and known in the art, including nanowires in the channel region provides added gate control, where the gate-all-around aspect of nanowires provides even more control than the three-sided gate structure for FinFETs like those disclosed by Murthy. (Ex. 1006, ¶¶[0001], [0025]; Ex. 1010, ¶¶[0001], [0024]; Ex. 1002, ¶87.) Moreover, nanowire-based transistors also allow for reduced chip size by stacking the transistor channels vertically. (Ex. 1010, ¶[0010], FIG. 1i; Ex. 1002, ¶87.) Accordingly, a POSITA would have been motivated to implement a nanowire-based channel region when fabricating FinFET devices like those disclosed by Murthy. (Ex. 1002, ¶87.)

Moreover, non-planar nanowire devices were well-known in the art, and a POSITA would have understood that structures and teachings related to fin-based non-planar devices like those disclosed by Murthy are compatible with, and applicable to, nanowire non-planar devices like those disclosed by Ching. (Ex. 1011, ¶[0044]; Ex. 1012, ¶¶[0024], [0033], [0068]; Ex. 1013 ¶[0042]; Ex. 1010, ¶¶[0013], [0024]; Ex. 1002, ¶88.) Indeed, Murthy states that the disclosed “techniques can be embodied, for instance, in planar or non-planar transistor devices” and does not limit the non-planar devices to FinFETS using a fin that is a thin strip of semiconductor material. (Ex. 1005, Abstract, ¶[0013]; Ex. 1002, ¶89.)

As a POSITA would have appreciated, using nanowires for the channel region as disclosed by Ching as opposed to a fin would have been the simple substitution of one type of transistor channel (Ching’s nanowires) for another (Murthy’s fin) in a similar device in a predictable manner to produce the expected result of a functional non-planar transistor. (Ex. 1002, ¶90.) Put another way, Ching’s nanowires would have been a “suitable option” in place of Murthy’s fin. *Intel Corp. v. PACT XPP Schweiz AG*, No. 2022-1037, 2023 WL 2469631, at *5 (Fed. Cir. Mar. 13, 2023) (holding that Petitioner need not show that the proposed substitution was necessarily an improvement but rather would have been a suitable option) (citing *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797 (Fed. Cir. 2021)). Indeed, “when a

patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.” *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Based on their knowledge of such well-known nanowire transistors and Ching’s detailed disclosure of nanowire formation in a similar device, a POSITA would have had a reasonable likelihood of success. (Ex. 1002, ¶¶91, 24-28; Ex. 1016, 1; Ex. 1018, 1; Ex. 1019, 1; Ex. 1020, 1; Ex. 1021, Abstract, 9, FIG. 19.) Therefore, the Murthy-Ching combination discloses or suggests using nanowires with gate-all-around channel regions (“the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons”) in a non-planar device like that discussed above in section IX.A.1.

To the extent PO argues that Ching teaches using germanium nanowires for PMOS devices such that the nanowires do not present “a surface that consists essentially of silicon” with which the first and second portions are “in direct contact,” the first and second portions of the Murthy-Ching combination are in direct contact with the underlying lower portion of the fin, which is silicon. (Sections IX.A.1(d)-(e); Ex. 1002, ¶92.)

2. Claim 17

a) “An integrated circuit, comprising:”

To the extent the preamble is limiting, Murthy discloses the limitations therein for the same reasons discussed above in section IX.A.1(a). (Section IX.A.1(a); Ex. 1002, ¶93.)

b) “a nanowire or nanoribbon comprising semiconductor material;”

As discussed above for claim 11, the Murthy-Ching combination discloses or suggests a non-planar transistor that includes a nanowire. (Section IX.C.1; Ex. 1002, ¶94.) Ching further discloses that the nanowires are made of silicon or germanium (“semiconductor material”). (Ex. 1006, Title, Abstract, ¶¶[0014]-[0015], [0018], [0022]-[0025]; *see also* Ex. 1011, ¶[0044]; Ex. 1002, ¶94.)

c) “a gate structure wrapped around the nanowire or nanoribbon;”

The Murthy-Ching combination discloses or suggests this limitation. (Ex. 1002, ¶95.) As discussed above for claim 11, the Murthy-Ching combination discloses or suggests a “gate-all-around” structure where the gate is wrapped around the nanowire. (Section IX.C.1; Ex. 1002, ¶95.)

d) “a source structure to one side of the gate structure and abutting the nanowire or nanoribbon, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”

e) “a drain structure to an opposite side of the gate structure and abutting the nanowire or nanoribbon, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;”

The Murthy-Ching combination discloses or suggests these limitations to the extent they can be understood.⁷ (Ex. 1002, ¶96.) As discussed above for claim 11, the Murthy-Ching combination includes a nanowire channel instead of a fin. (Sections IX.C.1, IX.A.1(b); Ex. 1002, ¶96.) Therefore, for the same reasons discussed above for the “source structure” and “drain structure” in the context Murthy and claim 13, the Murthy-Ching combination discloses or suggests a “source structure” on one side of the gate structure surrounding the channel region that includes the nanowire and a “drain structure” on the opposite side of the gate structure, where the source and drain structures abut the nanowire in order to form a

⁷ See note 3 above.

transistor device, where the source/drain structures include first/second portions having germanium at a concentration of at least 50 atomic percent throughout as recited in claim 17. (Sections IX.C.1, IX.A.9(d)-(e); Ex. 1002, ¶96.) Moreover, as also discussed above for claim 11 and claim elements 13[d]-[e], the source/drain structures are in direct contact with the lower portion of the silicon fin underlying the source/drain structures. (Sections IX.C.1, IX.A.9(d)-(e); Ex. 1002, ¶96.)

f) “a first contact structure on the first portion of the source structure and including a metal-germanide; and”

g) “a second contact structure on the second portion of the drain structure and including a metal-germanide. ”

The Murthy-Ching combination discloses or suggests these limitations for the same reasons presented above for claim elements 13[f]-[g] in section IX.A.9. (Sections IX.A.9(f)-(g); Ex. 1002, ¶97.)

3. Claim 18

“The integrated circuit of claim 17, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

Murthy in combination with Ching discloses or suggests these features. As discussed above for claim elements 17[d]-[e] and 13[d]-[e], the “first/second portions” of the source/drain structures are in direct contact with the upper surface of the underlying lower portion of the fin, which is part of the bulk silicon or silicon-

on-insulator substrate. (Sections IX.C.2(d)-(e), IX.A.9(d)-(e), IX.A.2; Ex. 1002, ¶198.)

4. Claim 20

“The integrated circuit of claim 17, wherein the first and second portions further include one or both of silicon and tin, and further include a p-type dopant.”

The Murthy-Ching combination discloses or suggests the first/second portions include silicon and a p-type dopant for the same reasons discussed above for claim 16 in section IX.A.11. (Section IX.A.11; Ex. 1002, ¶199.)

D. Ground 4 – Wann Anticipates Claims 1, 2, 6-8, 10, and 12-14

1. Claim 1

a) Element 1[a]

To the extent the preamble is limiting, Wann discloses the limitations therein. (Ex. 1002, ¶¶39-40, 100-102.) Wann discloses an integrated circuit that includes a fin field effect transistor, FinFET 200, shown in figures 9A and 9B below. (Ex. 1007, ¶[0009] (“The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).); *see also id.*, [0001]-[0002]; Ex. 1002, ¶¶101-102.)

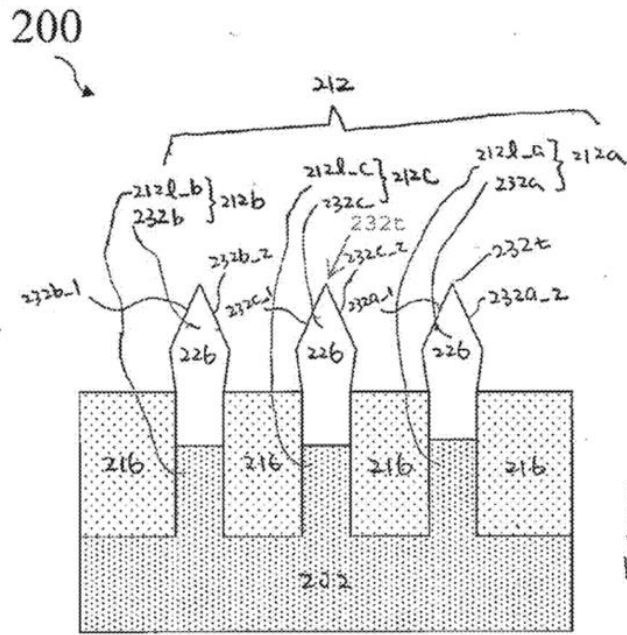


FIG. 9B

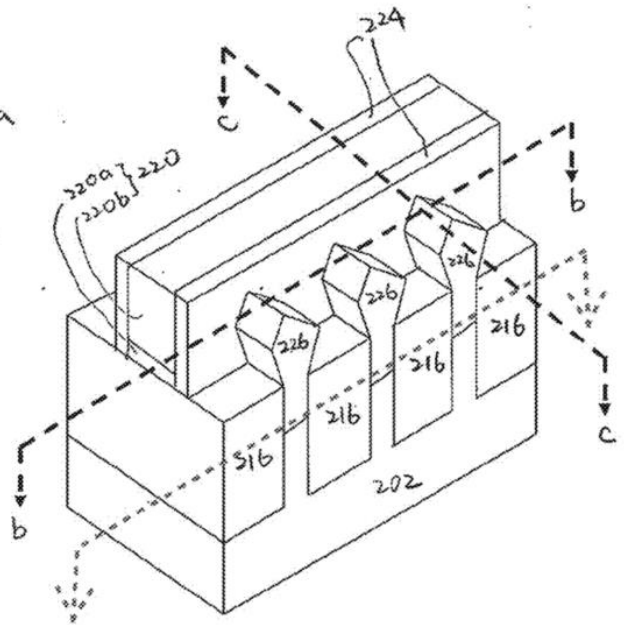


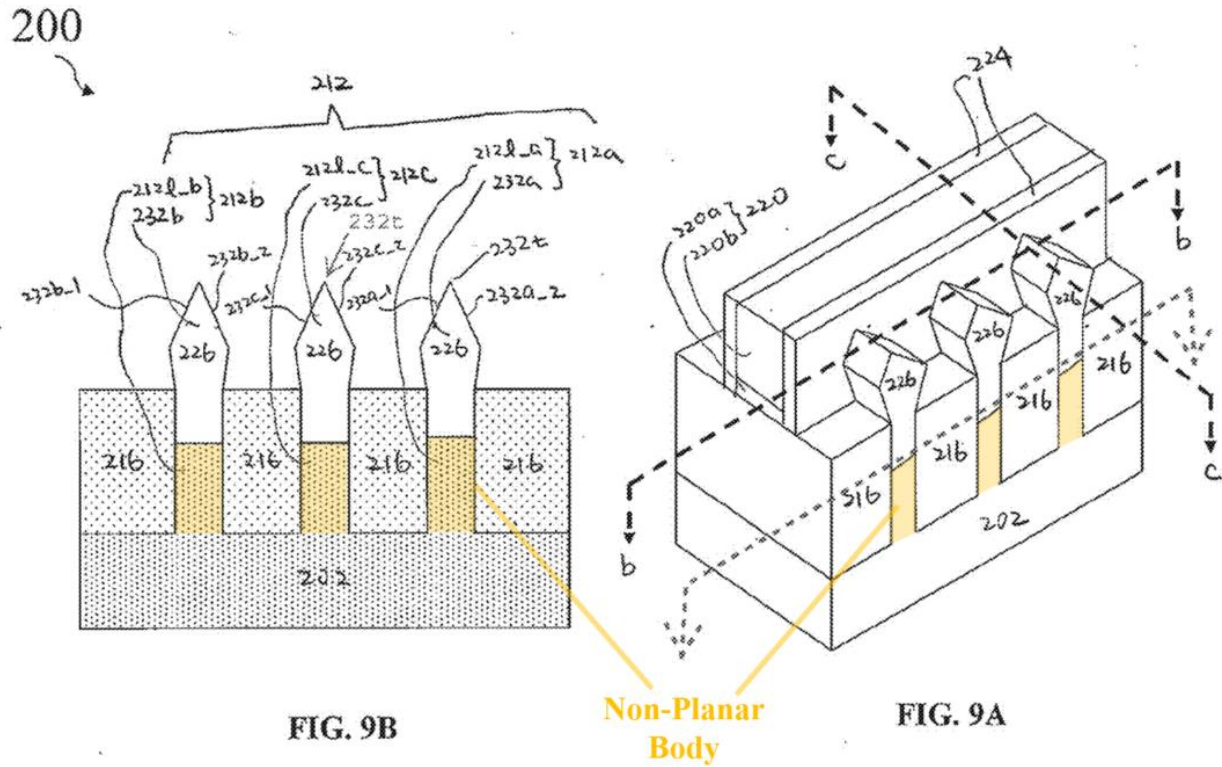
FIG. 9A

(Ex. 1007, FIGs 9B, 9A.)

b) Element 1[b]

Wann discloses this claim feature. (Ex. 1002, ¶¶103-105.) As shown in annotated figures 9B and 9A below, Wann’s FinFET 200 includes a substrate 202, which is etched to form fins 212, each of which constitutes a “non-planar body.” (Ex. 1007, Abstract (“a fin structure extending upward from the substrate major surface, wherein the fin structure comprises a first fin, a second fin, and a third fin between the first fin and the second fin;”), ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”) ¶[0015]; Ex.

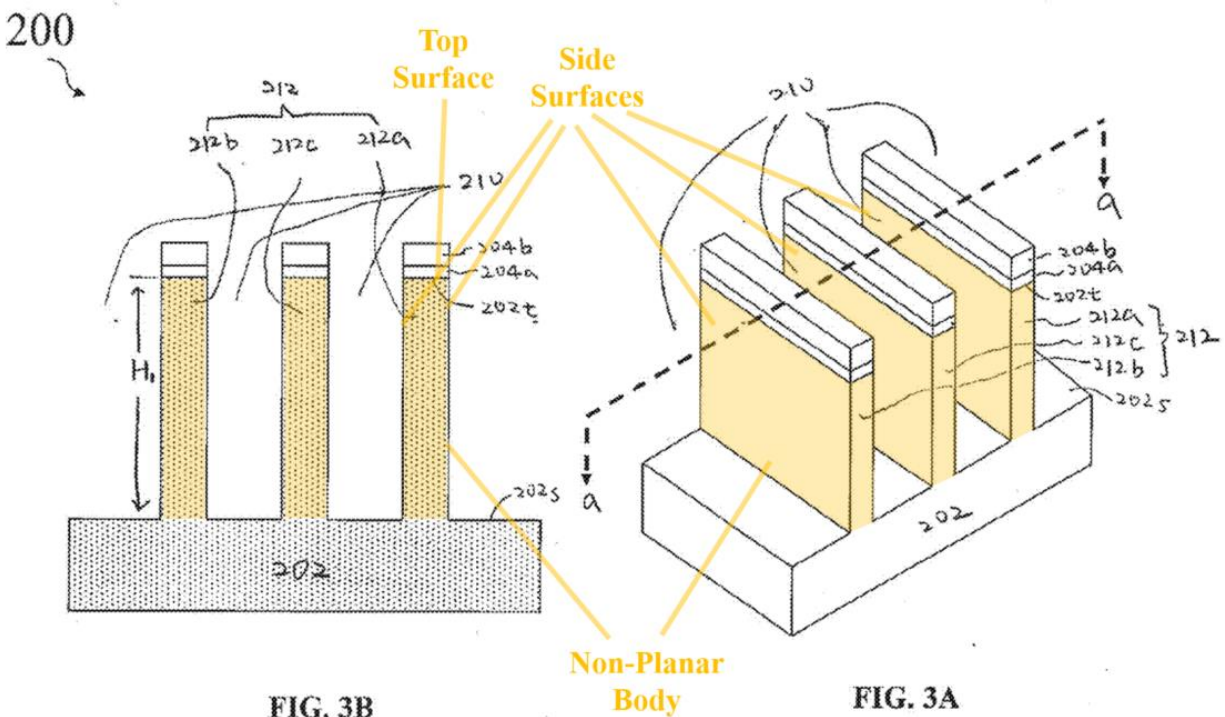
1002, ¶103.) Each fin corresponding to a non-planar body is consistent with claim 10 of the '334 patent, which recites “the non-planar body is a fin.” (Ex. 1001, claim 10; section IX.D.6.)



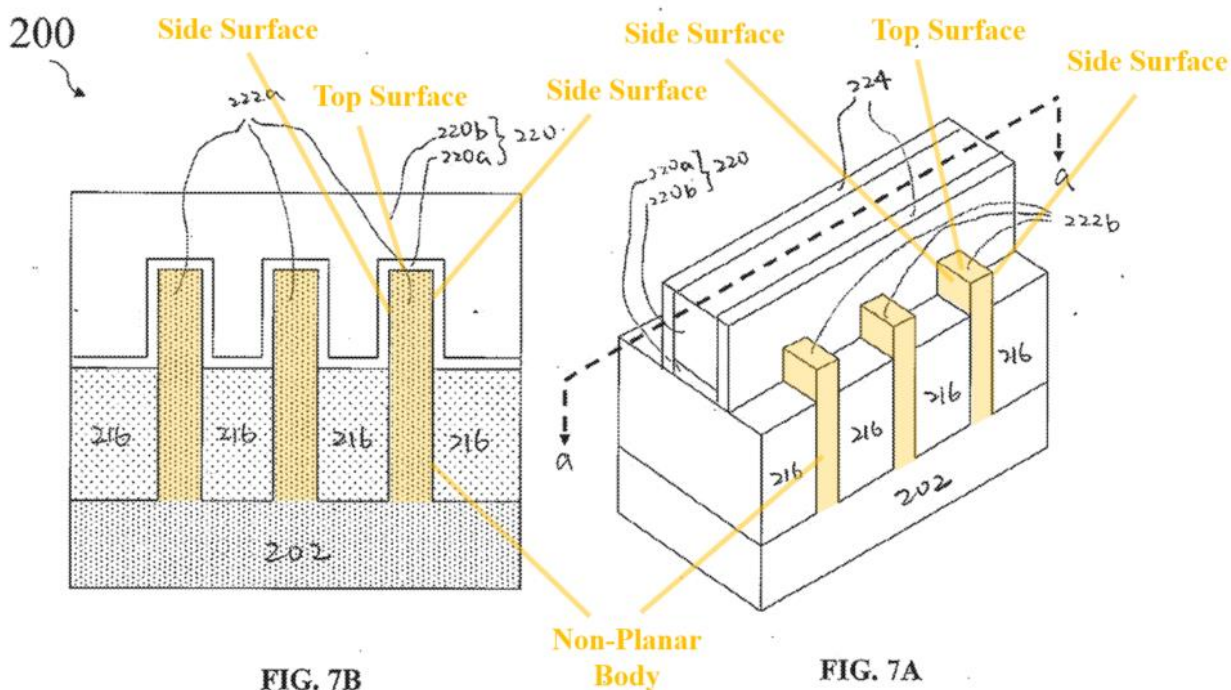
(Ex. 1007, FIGs 9B, 9A (annotated); Ex. 1002, ¶103.)

As shown in annotated figures 3B, 3A, 7B, and 7A below, which correspond to the structure shown above in figures 9B and 9A earlier stages in the fabrication process, each of the fins (“non-planar body”) includes a top surface and side surfaces. (Ex. 1007, ¶[0015] (“FIG. 3A is a perspective view of the semiconductor device 200 at one of the various stages of fabrication according to an embodiment,

and FIG. 3B is a cross-sectional view of semiconductor device 200 taken along the line a-a of FIG. 3A. ... The exposed semiconductor substrate 202 is then etched to form trenches 210 lower than the top surface 202t of the semiconductor substrate 202. Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins (i.e., the fin structure 212).”); Ex. 1002, ¶104.)



(Ex. 1007, FIGs 3B, 3A (annotated); Ex. 1002, ¶104.)



(Ex. 1007, FIGs 7B, 7A (annotated); Ex. 1002, ¶105.)

c) Element 1[c]

Wann discloses this limitation. (Ex. 1002, ¶¶106-107.) For example, as shown in annotated figure 9A below, Wann discloses a gate stack 220 (“gate structure”) that includes gate dielectric layer 220a (green) and gate electrode layer 220b (blue), on the top and side surfaces of the fin (“non-planar body”). (Ex. 1007, ¶[0020]; Ex. 1002, ¶106.)

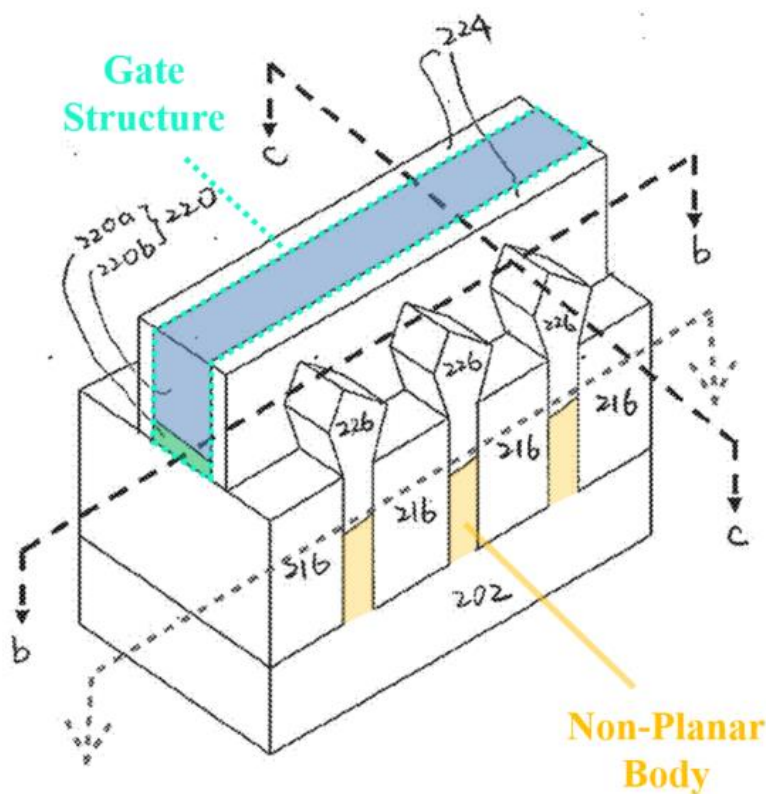
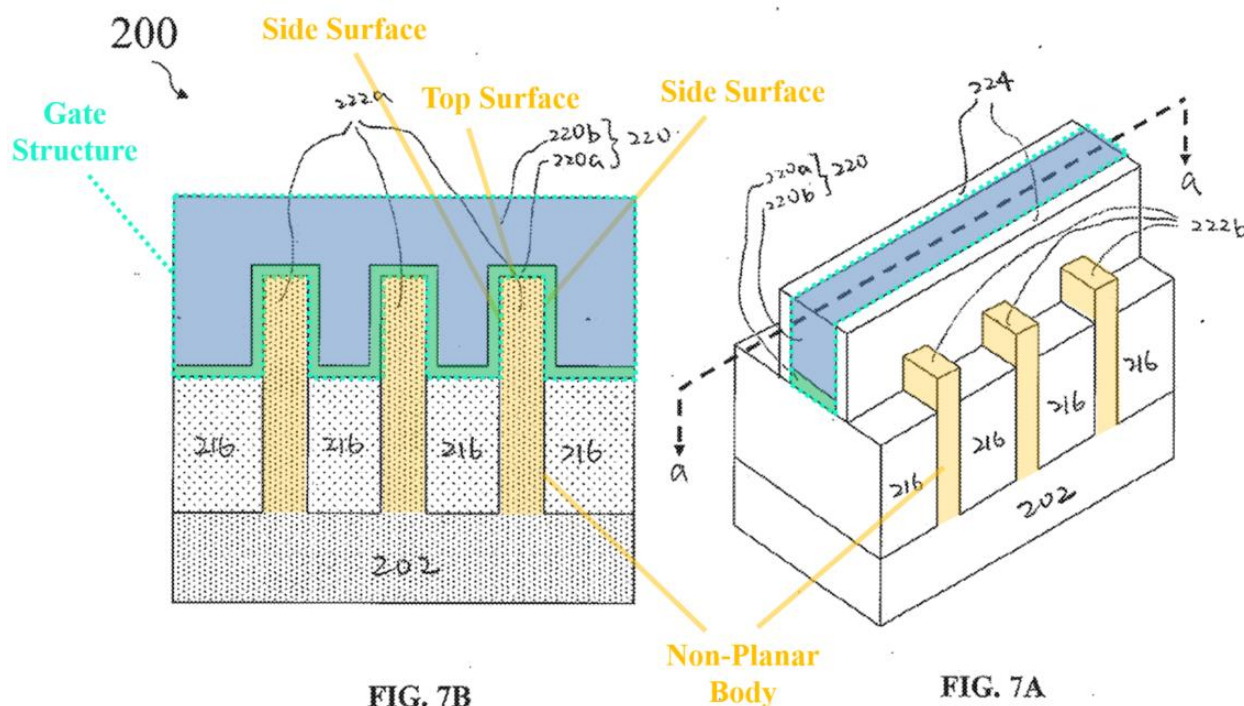


FIG. 9A

(Ex. 1007, FIG. 9A (annotated); Ex. 1002, ¶106.)

As shown in annotated figures 7B and 7A below, Wann discloses that the gate stack 220 is formed covering the top and side surfaces of channel portions 222a, which corresponds to a portion of each of the fins (“non-planar body”). (Ex. 1007, ¶[0020] (“A gate stack 220 is formed over the channel portions 222a of the upper portion 222 of the fins 212 and extending to the top surface 216t of the STI region 216. In some embodiments, the gate stack 220 comprises a gate dielectric layer 220a and a gate electrode layer 220b over the gate dielectric layer.”), ¶[0021] (“In FIGS.

7A and 7B, the gate dielectric 220a is formed to cover the channel portions 222a of the upper portions 222 of the fins 212.”), ¶[0002], FIGS. 7A, 7B; Ex. 1002, ¶107.)



(Ex. 1007, FIGs. 7A, 7B (annotated); Ex. 1002, ¶107.)

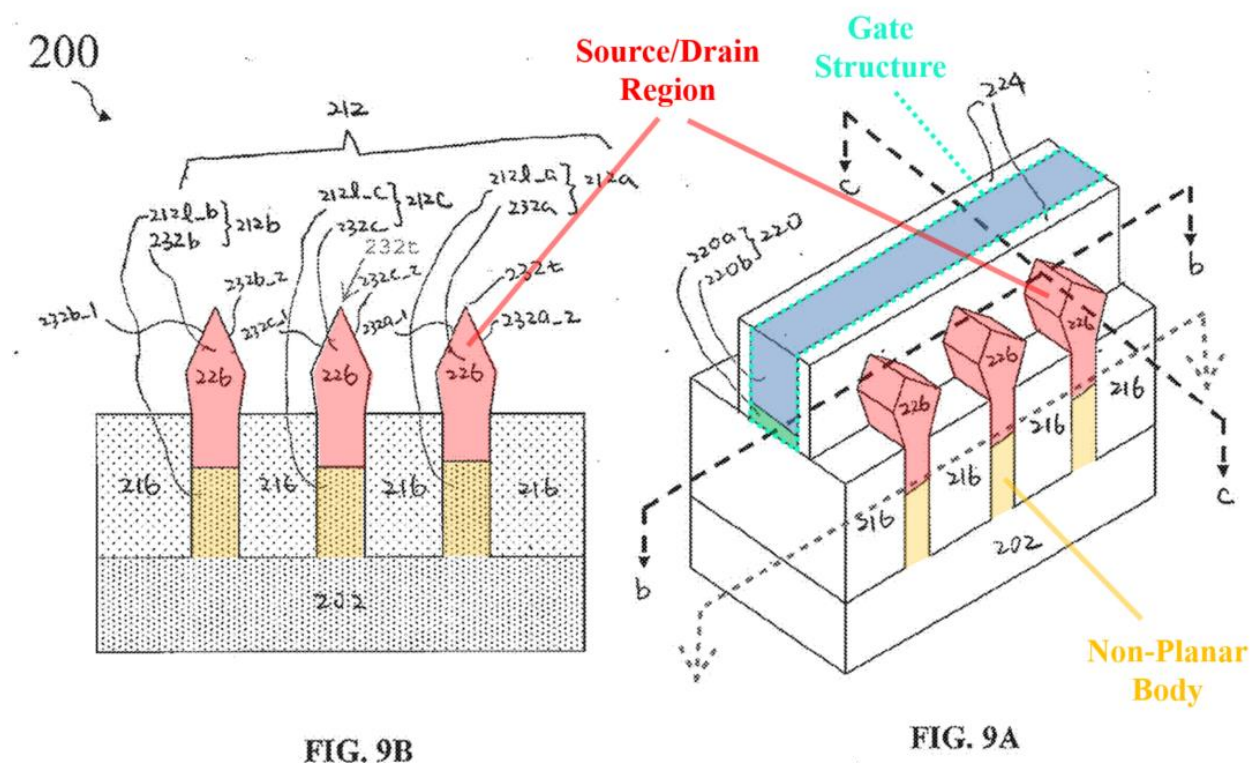
d) Element 1[d]

e) Element 1[e]

Wann discloses these features to the extent they can be understood.⁸ (Ex. 1002, ¶¶108-117.) As shown in annotated figure 9B and 9A below, Wann discloses strained material 226 (“first/second portions”) included in the source/drain regions

⁸ See note 3 above.

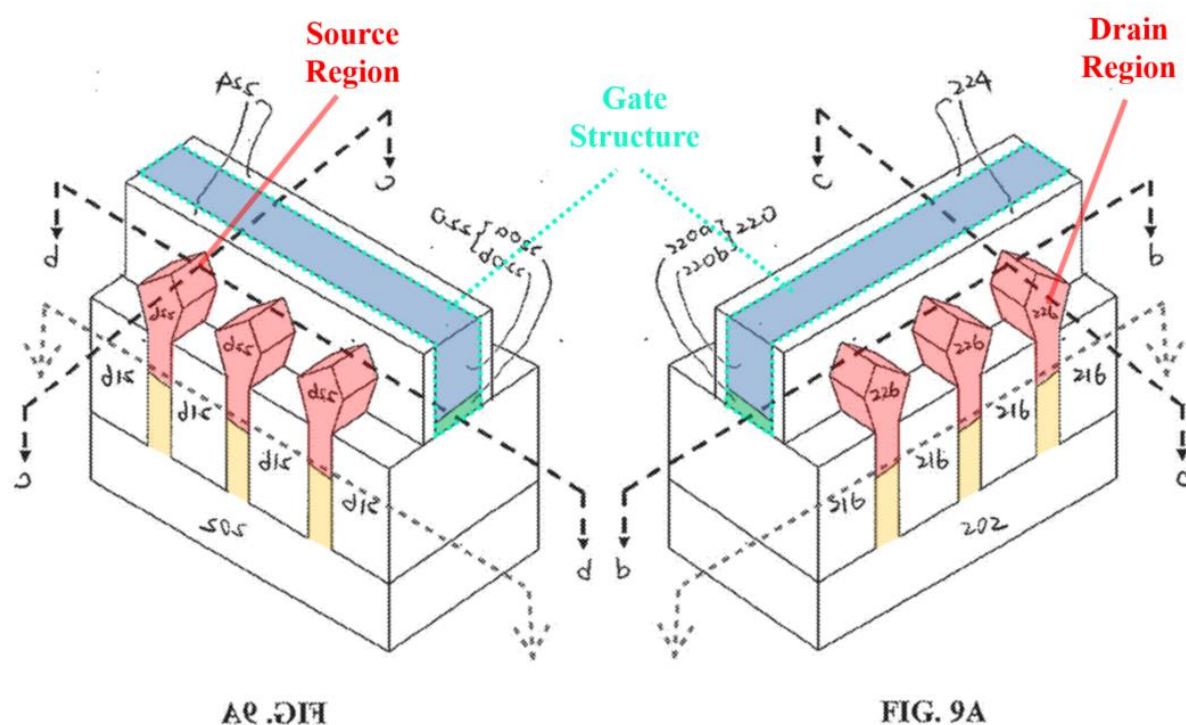
223 of the FinFET. (Ex. 1007, ¶[0025] (“Referring to FIGS. 9A and 9B, after the formation of the S/D cavities 228 in the S/D portions 222b, the structure in FIGS. 9A and 9B is produced by epi-growing a strained material 226 in the S/D cavities 228 ...”), ¶[0026] (“In some embodiments, the strained material 226 is hereinafter referred to as S/D regions 232 (comprising 232a, 232b, and 232c).”))



(Ex. 1007, FIG. 9A (annotated); Ex. 1002, ¶108.)

While not visible in figure 9A, there is an additional source/drain (S/D) region on the opposite side of the gate structure corresponding to each of the visible S/D regions 226. (Ex. 1002, ¶109; *see also* Ex. 1005, ¶[0052] (“A source region

comprises the epitaxial regions 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown).”).) This is shown in the horizontally-flipped version of figure 9A below.



(Ex. 1007, FIG. 9A (rotated, annotated); Ex. 1002, ¶109.)

Depending on how the FinFET is coupled to surrounding circuitry, the S/D region on a first side of the gate structure functions as the “source region,” whereas the corresponding S/D region on the other side functions as the “drain region.” (Ex. 1002, ¶110.) For example, as shown in annotated figure 9A above, if the S/D region

on the back side of the FinFET (only visible in the horizontally flipped figure 9A) is designated as the source region, then the S/D region on the front side of the FinFET is the drain region. (*Id.*) A POSITA would have appreciated that, from the perspective of the FinFET device itself, the source and drain regions are interchangeable. (*Id.*)

Wann’s disclosure of corresponding S/D regions lying on opposite sides of the gate structure is confirmed by Wann’s description of the formation of the S/D regions with respect to figures 6A-8B.⁹ For example, Wann discloses that in annotated figure 6A below, “the upper portions 222 of the fins 212 may comprise channel portions 222a and source/drain (S/D) portions 222b,” where “[t]he channel portions 222a are used to form channel regions of the semiconductor device 200.” (Ex. 1007, ¶[0019]; Ex. 1002, ¶111.) The “channel region” of the FinFET is the portion that lies between the source and drain regions. (Ex. 1002, ¶111.)

⁹ The disclosure is also supported by U.S. Patent 9,379,108 (Ex. 1014) (“Wann-108”), which is a patent derived from a continuation application claiming priority to Wann and shows source/drain regions on both side of the gate structure in figures 7A and 9A. (Ex. 1014, FIGs. 7A, 9A; Ex. 1002, ¶111, n. 5.)

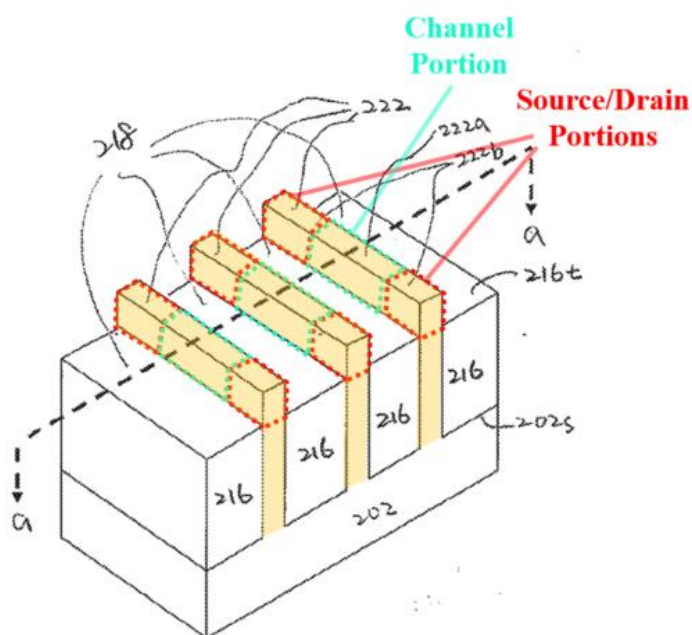


FIG. 6A

(Ex. 1007, FIG. 6A; Ex. 1002, ¶111.)

As shown in annotated figure 7A below, the gate stack 220 is formed covering the top and side surfaces of channel portions 222a, leaving source/drain portions 222b exposed on both sides of the gate stack 220. (Ex. 1007, ¶¶[0020], [0021], FIGS. 7A, 7B; Ex. 1002, ¶112.)

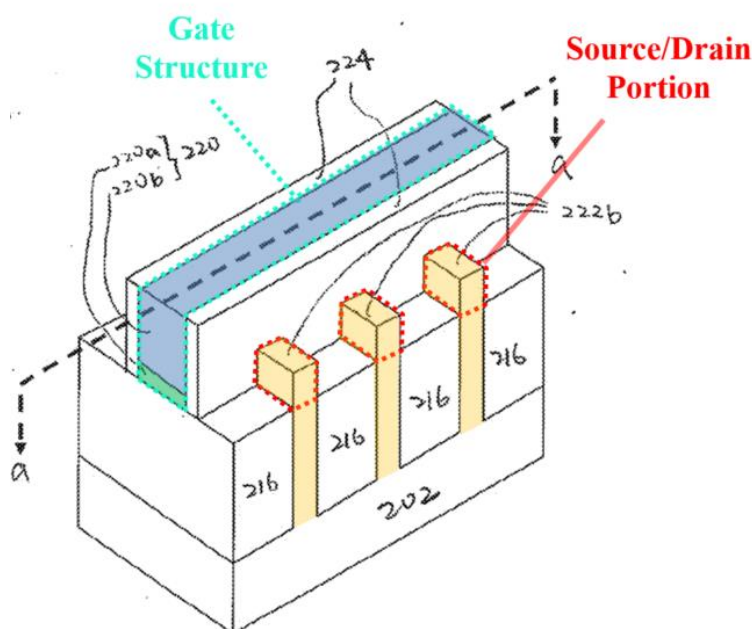
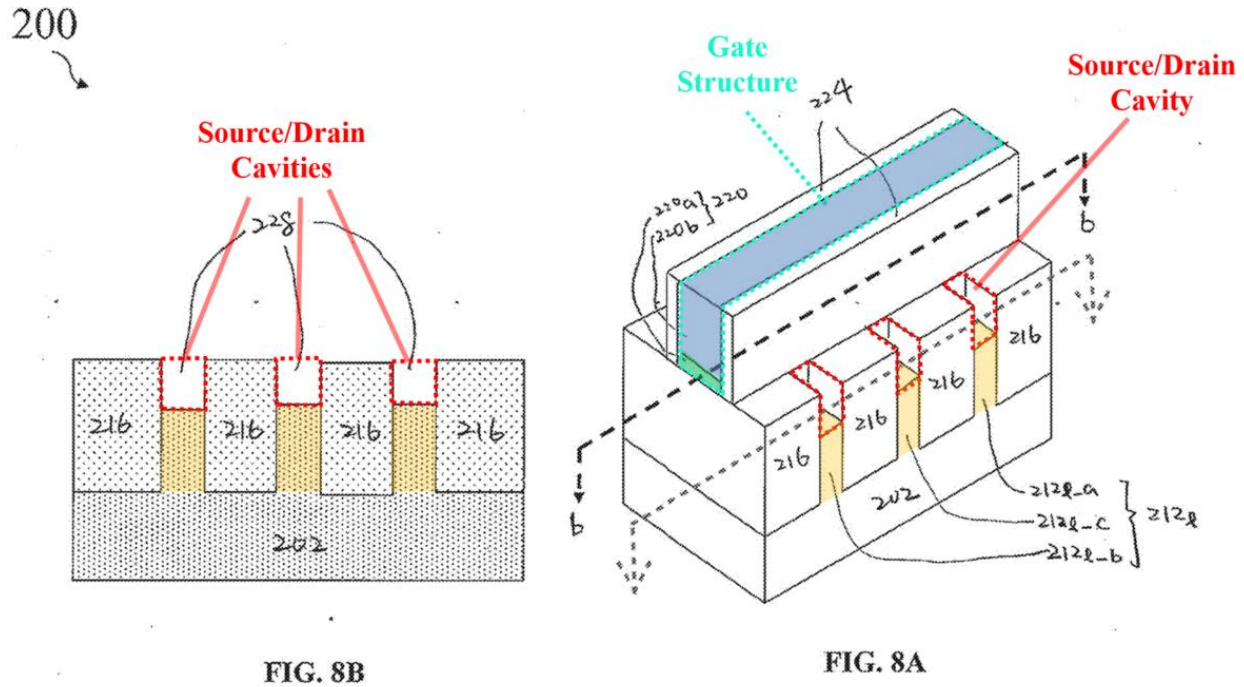


FIG. 7A

(Ex. 1007, FIG. 7A (annotated); Ex. 1002, ¶112.)

As shown in annotated figures 8B and 8A below, selective etching is used to recess the source/drain portions 222b of the upper portion 222 of the fins to form source/drain cavities 228. (Ex. 1007, ¶[0024] (“Using the gate stack 220, dielectric layer 224, and STI region 216 as hard masks, a biased etching process is performed to recess the S/D portions 222b (shown in FIGS. 6A and 7A) of the upper portions 222 of the fins 212 that are unprotected or exposed to form the S/D cavities 228 below the top surface 202t, thereby leaving lower portions 212l (comprising 212l_a, 212l_b, and 212l_c) of the fin structure 212”).) Because, as shown in figure 6A

above, source drain portions 222b are on both sides of the gate stack 220, the cavities for the source/drain regions are formed on both sides of the gate stack. (Ex. 1002, ¶113.)



(Ex. 1007, FIGs. 8B, 8A (annotated); Ex. 1002, ¶113.)

Following formation of the source/drain cavities, “the structure in FIGS. 9A and 9B is produced by epi-growing a strained material 226 in the S/D cavities 228,” where the strained material corresponds to the claimed “first/second portions” of the “source/drain regions” for the FinFET. (Ex. 1007, ¶¶[0025]-[0026]; Ex. 1002, ¶114.)

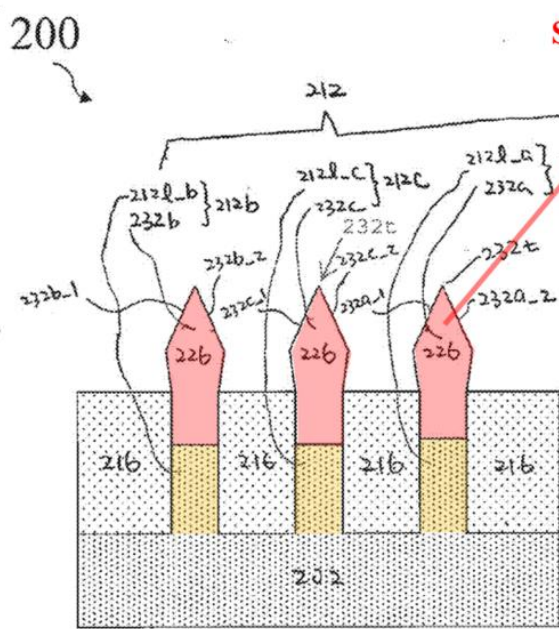


FIG. 9B

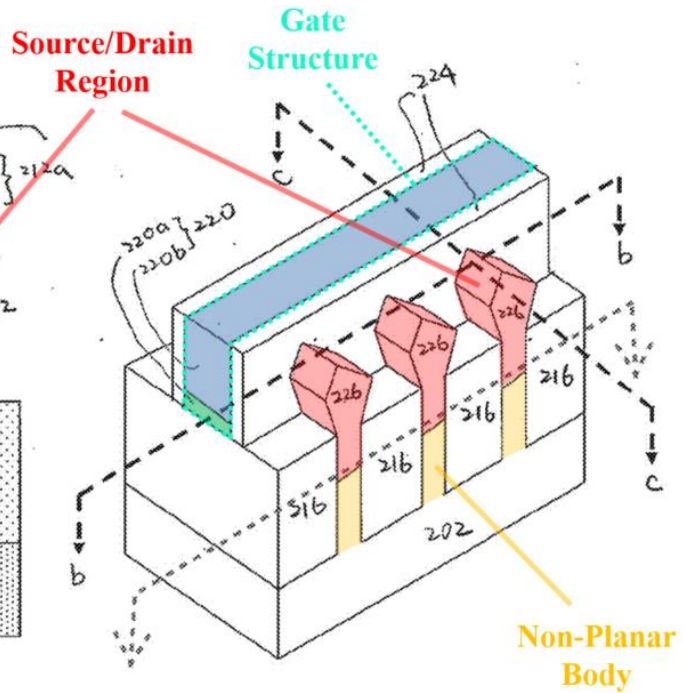


FIG. 9A

(Ex. 1007, FIG. 9A (annotated); Ex. 1002, ¶114.)

The source/drain regions that include the strained regions 226 grown in the source/drain cavities for each of the fins of the FinFET 200 are “adjacent to the non-planar body” as they lie on top of a portion the fin (“non-planar body”) and also have the channel portion 222a of the upper portion 222 of the fin between them. In other words, the source and drain regions are “adjacent” to the non-planar body, which is a fin of the silicon substrate 202, because they are separated by the channel portion of the fin and also because they lie on top of the lower portion the fin. (Ex. 1007, FIGs. 9A, 9B; Ex. 1002, ¶115.) Indeed, a POSITA would have understood that S/D

regions 232 are in direct contact with channel portion 222a of the fin in order to form a functioning transistor. (Ex. 1002, ¶115.)

Wann discloses an embodiment in which the strained material 226 (“first/second portions”) is germanium (Ge). (Ex. 1007, ¶[0025] (“In some embodiments, the **strained material 226 comprises Ge** or SiGe for a p-type FinFET.”); Ex. 1002, ¶116.) Therefore, Wann discloses “first/second portions” made of germanium (“including germanium at a concentration of at least 50 atomic percent throughout the [first/second] portion”) as recited in claim 1. (Ex. 1002, ¶116.) Such an understanding is confirmed by Wann’s differentiation between using straight germanium (Ge) for the strained material in one embodiment as opposed to silicon-germanium (SiGe) for the strained material in another embodiment. (Ex. 1007, ¶[0025], ¶[0028] (“In the Ge-growing embodiment...”), ¶[0029] (“In the SiGe-growing embodiment...”); Ex. 1002, ¶116.)

As discussed above, the strained material (“first/second portions of the source/drain regions”) is in direct contact with the channel portion 222a of the upper portion 222 of the fin, which is between the source/drain regions, as well as in direct contact with the underlying lower portion of the fin. The fin is part of the silicon substrate, and therefore first and second portions of the germanium source/drain regions are “in direct contact with a surface that consists essentially of silicon.” (Ex.

1007, ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”), ¶[0011] (“In at least one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer).”), ¶[0015], FIGs. 3A, 3B; Ex. 1002, ¶117.)

2. Claim 2

Wann discloses this limitation. (Ex. 1002, ¶118.) As discussed above for claim elements 1[d]-[e], the strained material (“first/second portion”) of the source/drain regions are in direct contact with the channel portion 222a of the upper portion 222 of the fin and the underlying lower portion of the fin which is part of the silicon substrate 202, which is “crystalline silicon substrate (e.g., wafer).” (Sections IX.D.1(d)-(e); Ex. 1007, ¶[0002], ¶[0011] (“In at least one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer).”), ¶[0015], FIGs. 3A, 3B; Ex. 1002, ¶118.) Therefore, the “surface,” which corresponds to either the side surface of the channel portion 222a or the upper surface lower portion of the fin is a surface of “a bulk silicon substrate” as claimed. (Ex. 1002, ¶118; *see also* Ex. 1001, 5:35-40.)

3. Claim 6

Wann discloses this limitation. (Ex. 1002, ¶119.) For example, Wann discloses that strained material 226 (“first and second portions”) “comprises Ge or SiGe for a **p-type FinFET**.” (Ex. 1007, ¶[0025].) A POSITA would have understood that for a p-type FinFET the S/D regions 232, including the strained material, are doped to include p-type dopants. (*Id.*, ¶[0011] (“doped regions may be doped with p-type dopants, such as boron or BF₂”); Ex. 1002, ¶119; *see also* Ex. 1017, 15-17; Ex. 1015, 115-117.) Such an understanding is consistent with the disclosure of the ’334 patent. (Ex. 1001, 2:60-64 (“Note that the Ge-rich layer as variously described herein is to be used for p-MOS source/drain contacts and is therefore a p-type layer, meaning it has p-type doping (e.g., using boron (B), gallium (Ga), and/or any other suitable dopant).”); Ex. 1002, ¶119.)

4. Claim 7

Wann discloses this limitation. (Ex. 1002, ¶120.) As discussed above for claim elements 1[d]-[e] and claim 2, the “surface that consists essentially of silicon” is part of the silicon substrate 202, which is a “crystalline silicon substrate (e.g., wafer).” (Sections IX.D.1(d)-(e), IX.D.2; Ex. 1007, ¶[0002], ¶[0011] (“substrate 202 comprises a **crystalline silicon substrate (e.g., wafer)**.”), ¶[0015], FIGs. 3A, 3B; Ex. 1002, ¶120.) A POSITA would have understood that, absent any indication

that the substrate is subsequently doped, crystalline silicon material is “undoped.” (Ex. 1002, ¶120; Ex. 1015, 103, 115; Ex. 1017, 93-97.) Wann does not disclose doping the channel portion 222a of the upper portion 222 of the fin or the lower portion of the fin underlying the source/drain regions. (Section IX.D.2; Ex. 1007, ¶¶[0002], [0011], [0015]; Ex. 1002, ¶120.)

5. Claim 8

Wann discloses this limitation. (Ex. 1002, ¶¶121-123.) For example, consistent with the disclosure of the '334 patent (Ex. 1001, 10:34-61), Wann discloses forming metal germanide (“additional portions including a metal and germanium) over the germanide strained material 226 (“first and second portions”):

The processing steps up to this point have provided the substrate 202 having the strained material 226 over each lower portion 212l. Conventionally, metal germanide over the strained material 226 may be formed by blanket depositing a thin layer of metal material, such as Ni, Pt, Ti, Co, Pd, and combinations thereof. The substrate 202 is then heated, which causes Ge to react with the metal where contacted. After the reaction, a layer of metal germanide is formed between the Ge-containing material and the metal.

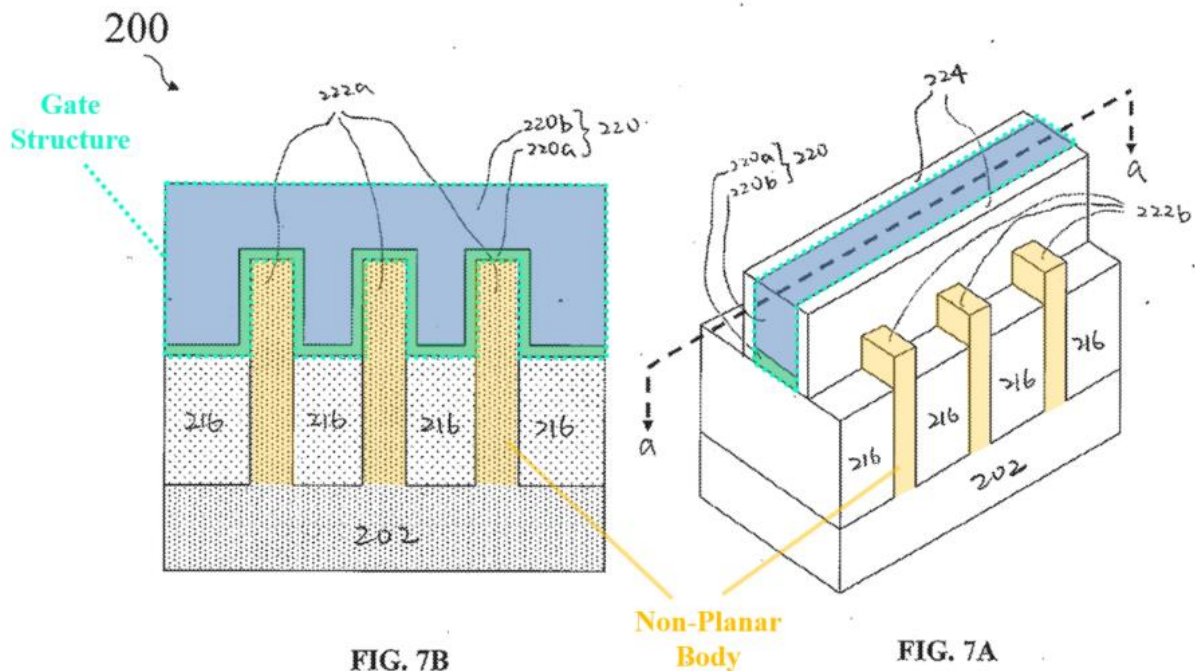
(Ex. 1007, ¶[0030]; Ex. 1002, ¶¶121, 123.)

Wann further discloses that, for the particular geometry for the facets of the strained material shown in the embodiment of figure 9, the conventional process can result in “triangular germanide” with “small-volume germanide on the strained material 226 [that] causes high contact resistance of S/D regions of the FinFET and thus degrades the device performance.” (Ex. 1007, ¶[0030].) Therefore, Wann discloses another technique for forming a “rectangular germanide to replace the triangular germanide.” (*Id.*, ¶[0031]; *see also id.*, ¶¶[0032]-[0042], FIGs. 10-13; Ex. 1002, ¶122.) Like the conventional germanide formation, Wann’s “rectangular germanide” technique deposits metal on the strained material 226 (Ex. 1007, ¶[0037]), and then the substrate is heated to form germanide (*id.*, ¶[0038].) (Ex. 1002, ¶122.) “In other words, the first metal layer 242 in contact with the strained material 226 is then transformed into a germanide by a thermal process,” where “the germanide 246 comprises NiGe, PtGe, TiGe₂, CoGe₂, or PdGe.” (Ex. 1007, ¶[0038].)

Therefore, Wann discloses “additional portions” of germanide “on the first and second portions,” where the additional portions include a metal and germanium as recited in claim 8. (Ex. 1002, ¶123.)

6. Claim 10

Wann discloses this limitation. (Ex. 1002, ¶124.) As discussed with respect to claim 1, each of Wann’s fins that extend upward from the planar surface of the substrate constitutes the claimed “non-planar body.” (Section IX.D.1) As shown in figures 7A and 7B below, each fin includes a channel portion 222a that is covered on the top and sides by the gate structure (“the fin between portions of the gate structure”).



(Ex. 1007, FIGs. 7B, 7A (annotated); Ex. 1002, ¶124.)

7. Claim 12

Wann discloses this limitation. (Ex. 1002, ¶125.) Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (Ex. 1007, ¶[0009]; Ex. 1002, ¶125.) A microprocessor that includes that includes Wann’s FinFET transistor is a “computing system,” as it is an electronic device that includes an interconnected set of components that processes data. (Ex. 1002, ¶125.) Such an understanding is consistent with the disclosure of the ’334 patent. (Ex. 1001, 14:14-23 (“... computing system 1000 ... **the system 1000 may be any other electronic device that processes data or employs one or more transistor devices as variously described herein.**”); Ex. 1002, ¶125.)

8. Claim 13

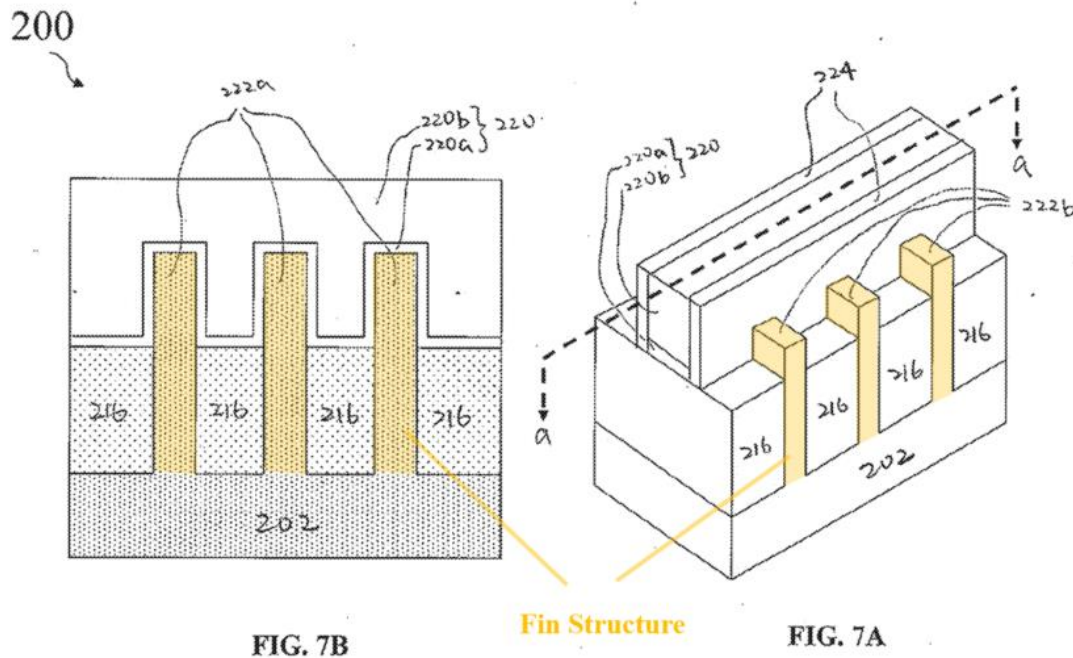
a) Element 13[a]

To the extent the preamble is limiting, Wann discloses the limitations therein for the same reasons discussed above for claim element 1[a]. (Section IX.C.1(a).) Ex. 1002, ¶126.)

b) Element 13[b]

Wann this claim feature. (Ex. 1002, ¶127.) As discussed above for claim element 1[b] and shown in annotated figures 9A and 9B below, Wann’s FinFET 200 includes a substrate 202 that is etched to form fins 212, where each fin constitutes a

“fin structure” as recited in claim element 13[b]. (Section IX.C.1(b); Ex. 1007, Abstract (“a fin structure extending upward from the substrate major surface, wherein the fin structure comprises a first fin, a second fin, and a third fin between the first fin and the second fin;”), ¶¶[0002], [0015]; Ex. 1002, ¶127.) For the same reasons discussed above for the “non-planar body” recited in claim 1, Wann discloses a “fin structure” with top and side surfaces as recited in claim 13, where the “fin structure” includes one of the fins extending from the underlying substrate. (Section IX.C.1(b); Ex. 1002, ¶127.)



(Ex. 1007, FIGs 7B, 7A (annotated); Ex. 1002, ¶127.)

c) Element 13[c]

Wann discloses this limitation for the same reasons discussed above for claim element 1[c]. (Section IX.D.1(c); Ex. 1002, ¶128.) Gate stack 220 is formed covering the top and side surfaces of channel portion 222a included in the “fin structure.” (Section IX.D.1(c); Ex. 1002, ¶128.)

d) Element 13[d]

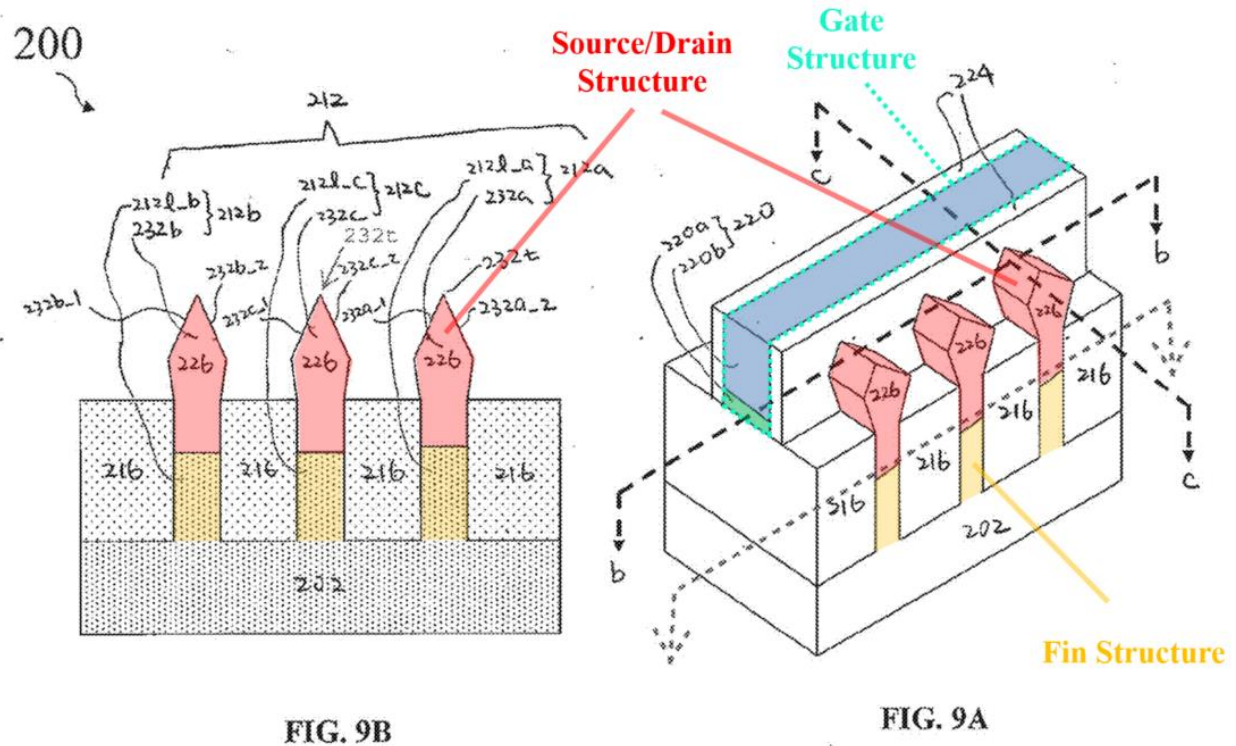
e) Element 13[e]

Wann discloses these features to the extent they can be understood.¹⁰ (Ex. 1002, ¶129.) As discussed above for claim elements 1[d] and 1[e] and shown in figures 9A and 9B below, Wann discloses strained material 226 (“first/second portions”) included in the source/drain regions 223 (“source structure” and “drain structure”) that are on opposite sides of the gate structure and abut the channel region 222a, which is part of the “fin structure.” (Sections IX.D.1(d)-(e), IX.D.8(b); Ex. 1002, ¶129.) As also discussed above for claim elements 1[d]-[e], Wann discloses forming the strained material 226 (“first/second portions”) of germanium such that the first/second portions include “at least 50 atomic percent” germanium throughout, where the first/second portions are in direct contact with the underlying lower

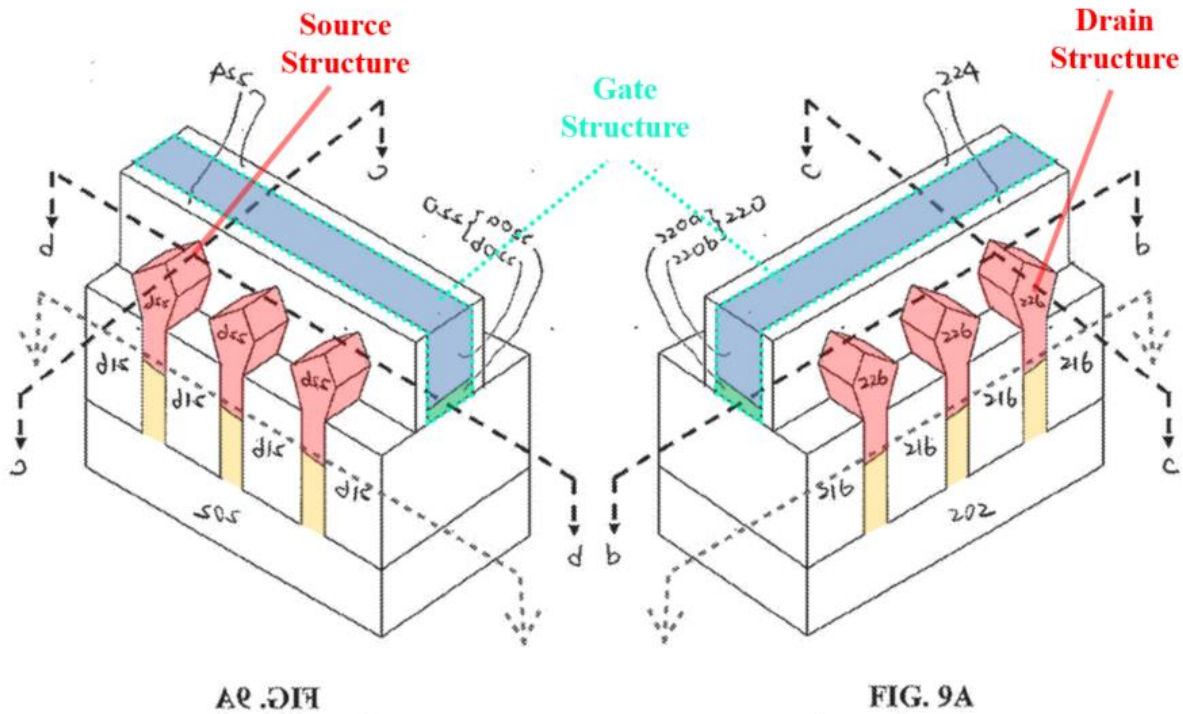
¹⁰ See note 3 above.

portion of the fin and the channel region, which “consist essentially of silicon.”

(Sections IX.D.1(d)-(e), IX.D.8(b); Ex. 1002, ¶129.)



(Ex. 1007, FIGs. 9B, 9A (annotated); Ex. 1002, ¶129.)



(Ex. 1007, FIG. 9A (rotated, annotated); Ex. 1002, ¶129.)

f) Element 13[f]

g) Element 13[g]

Wann discloses these features. (Ex. 1002, ¶¶130-132.) For example, as discussed above for claim 8 (section IX.C.5), Wann discloses forming metal germanide (“first/second contact structure”) on the strained material 226 (“first/second portion of the source/drain structure”). (Section IX.C.5; Ex. 1007, ¶¶[0030]-[0042].)

9. Claim 14

Wann discloses this limitation for the same reasons discussed above for claim 2. (Section IX.C.2; Ex. 1002, ¶133.)

E. Ground 5 – Wann in View of Kuhn Renders Claim 12 Obvious

1. Claim 12

Wann in combination with Kuhn discloses or suggests these features. (Ex. 1002, ¶¶134-136.) As discussed above in section IX.D.7, Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (Section IX.D.7; Ex. 1007, ¶[0009].) To the extent PO argues that Wann does not disclose a “computing system,” including Wann’s microprocessor in a computing system would have been obvious. (Ex. 1002, ¶134.) Moreover, Kuhn discloses using non-planar transistors on integrated circuits in a computing system, and a POSITA would have found it obvious to use Murthy’s transistor in a computing device as disclosed by Kuhn. (Ex. 1002, ¶134.)

Both Kuhn and Wann disclose using non-planar transistors in microprocessors. (Ex. 1010, ¶[0039]; Ex. 1007, ¶[0009]; Ex. 1002, ¶135.) Kuhn further discloses that such microprocessors can be included in a computing system. (Ex. 1010, ¶¶[0038]-[0041], FIG. 6; Ex. 1002, ¶135.) For reasons similar to those presented above for the Murthy-Kuhn combination, a POSITA would have found it

obvious to implement a non-planar transistor like that disclosed by Wann in a computing device. (Section IX.B.1; Ex. 1002, ¶136.)

F. Ground 6 – Wann in View of Ching Renders Claims 11, 17, and 18 Obvious

1. Claim 11

Wann in combination with Ching discloses or suggests these features. (Ex. 1002, ¶¶137-148.) As discussed above in section IX.D.1, Wann discloses a FinFET that includes a “non-planar body” in the form of a fin. (Section IX.D.1(b).) Wann does not explicitly disclose nanowires or nanoribbons, but Ching discloses a fin-based non-planar structure similar to that of Wann that uses nanowires, and, in view of Ching and their knowledge, a POSITA would have found it obvious to implement a non-planar transistor as disclosed by Wann using nanowires. (Ex. 1002, ¶137.)

As discussed above in section IX.C with respect to the Murthy-Ching combination, Ching, like Wann, discloses a fin-based transistor where a channel region separates epitaxially-formed source drain regions. (Ex. 1006, ¶¶[0001], [0019], [0021]; section IX.C.1; Ex. 1002, ¶¶138-141.) As such, a POSITA implementing a transistor as disclosed by Wann would have had reason to look to Ching. (Ex. 1002, ¶142.) Having looked to Ching, such a POSITA would have found it obvious to implement a transistor as disclosed by Wann using nanowires as disclosed by Ching for the same reasons presented above for the Murthy-Ching

combination. (Section IX.C.1; Ex. 1002, ¶¶142-144, 146-148.) Indeed, Wann states that “FinFET 200 refers to any fin-based, multi-gate transistor” and that “[o]ther transistor structures and analogous structures are within the contemplated scope of the disclosure,” thereby supporting the understanding the Wann’s teachings are compatible with nanowire architectures. (Ex. 1007, ¶[0009]; Ex. 1002, ¶145.)

2. Claim 17

a) Element 17[a]

To the extent the preamble is limiting, Wann discloses the limitations therein for the same reasons discussed above in section IX.D.1(a). (Section IX.D.1(a); Ex. 1002, ¶149.)

b) Element 17[b]

As discussed above for claim 11, the Wann-Ching combination discloses or suggests a non-planar transistor that includes a nanowire. (Section IX.F.1; Ex. 1002, ¶150.) Ching further discloses that the nanowires can be made of silicon and germanium, both of which constitute “semiconductor material.” (Ex. 1006, Title, Abstract, ¶¶[0014]-[0015], [0018], [0022]-[0025]; *see also* Ex. 1011, ¶[0044]; Ex. 1002, ¶150.)

c) Element 17[c]

The Wann-Ching combination discloses or suggests this limitation. (Ex. 1002, ¶151.) The Wann-Ching combination includes a nanowire with a gate structure that is a “gate-all-around” structure that is wrapped around the nanowire. (Section IX.F.1; Ex. 1002, ¶151.)

d) Element 17[d]

e) Element 17[e]

The Wann-Ching combination discloses or suggests these limitations to the extent they can be understood.¹¹ (Ex. 1002, ¶152.) The Wann-Ching combination includes a nanowire channel and discloses or suggests a “source structure” on one side of the gate structure surrounding the channel that includes the nanoribbon and a “drain structure” on the opposite side, where the source/drain structures abut the nanoribbon in order to form a transistor. (Sections IX.D.8(d)-(e), IX.F.1; Ex. 1002, ¶152.) For the same reasons discussed above for Wann disclosing a “source structure” and “drain structure” in claim 13, the Wann-Ching combination discloses or suggests that the source/drain structures include first/second portions having germanium at a concentration of at least 50 atomic percent throughout as recited in

¹¹ See note 3 above.

claim 17. (Sections IX.F.1, IX.D.8(d)-(e); Ex. 1002, ¶152.) Moreover, as also discussed above for claim 11 and claim elements 13[d]-[e], the first/second portions of the source/drain structures are in direct contact with the lower portion of the silicon fin. (Sections IX.F.1, IX.D.8(d)-(e); Ex. 1002, ¶152.)

f) Element 17[f]

g) Element 17[g]

The Wann-Ching combination discloses or suggests these limitations for the same reasons presented above for claim elements 13[f]-[g]. (Sections IX.D.8(f)-(g); Ex. 1002, ¶153.)

3. Claim 18

Wann in combination with Ching discloses or suggests these features. (Ex. 1002, ¶154.) As discussed above for claim elements 17[d]-[e] and 13[d]-[e], the “first portion” and “second portion” of the source/drain structures are in direct contact with the underlying lower portion of the fin, which is part of the “crystalline silicon substrate (e.g., wafer).” (Sections IX.F.2(d)-(e), IX.D.8(d)-(e), IX.D.2; Ex. 1007, ¶¶[0002], [0011], [0015], FIGs. 3A, 3B; Ex. 1002, ¶154.) Therefore, the “surface,” which corresponds to the upper surface lower portion of the fin is a surface of “a bulk silicon substrate” as claimed. (Ex. 1002, ¶154; *see also* Ex. 1001, 5:35-40; Ex. 1015, 103, 115; Ex. 1017, 93-97.)

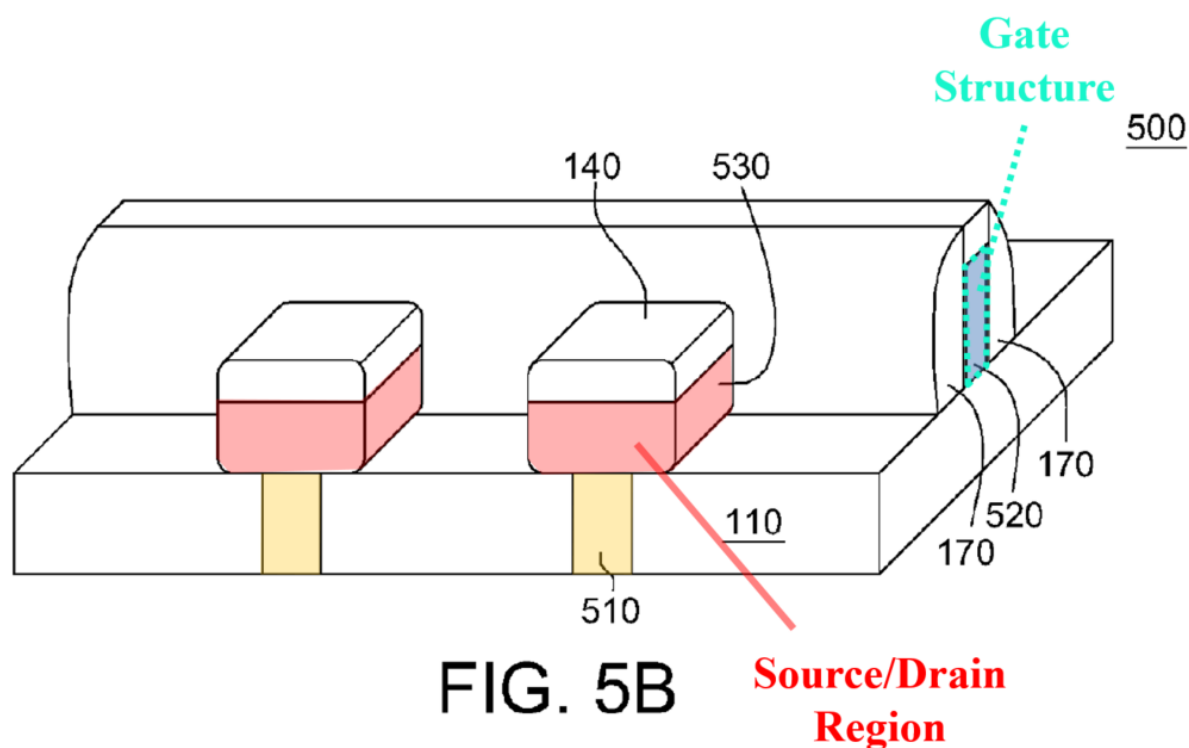
G. Ground 7 – Wann in View of Liao Renders Claims 1, 2, 5-7, 10, and 12 Obvious

1. Claims 1, 2, 10, and 12

Wann in view of Liao discloses or suggests the features of claims 1, 2, 10, and 12. (Ex. 1002, ¶¶155-168.) Wann discloses one embodiment in which the strained material of the source/drain regions of the FinFET is germanium (Ge), and therefore the source/drain regions that include portions that have at least 50 percent germanium. (Sections IX.D.1(d)-(e).) Wann discloses another embodiment where the strained material is silicon-germanium (SiGe), but does not explicitly disclose that the SiGe includes at least 50 percent germanium. (Ex. 1007, ¶[0025], (“In some embodiments, the strained material 226 comprises Ge or SiGe for a p-type FinFET.”); Ex. 1002, ¶155.) Liao, however, discloses forming epitaxial portions of source/drain regions in a similar FinFET device using SiGe where the germanium concentration is ≥ 50 percent, and, in view of Liao, a POSITA would have found it obvious to form the strained material of the source/drain regions in the device like that disclosed by Wann using $\geq 50\%$ germanium SiGe. (Ex. 1002, ¶155.)

Liao is in the same or similar field as Wann as, like Wann, Liao discloses forming a FinFET with source/drain regions 530 on either side of a gate structure 520. (Ex. 1008, ¶[0046], ¶[0050] (“semiconductor device 500 is such as a fin field-effect transistor (FINFET)”), FIG. 5B; Ex. 1002, ¶156.) Thus, a POSITA would

have had reason to consider the teachings of Liao when implementing Wann's device. (Ex. 1002, ¶157.)



(*Id.*, FIG. 5B; Ex. 1002, ¶157.)

Liao discloses that epitaxial structure 530 corresponding to the source/drain regions comprises SiGe, where “the Ge concentration in the epitaxial structure 530 is equal to or higher than 45%, preferably up to 55-60%.” (Ex. 1008, ¶[0047]; *see also id.*, [0017]; Ex. 1002, ¶158.) Liao also discloses another embodiment where the epitaxial structure includes two layers, a first layer that includes “about 55%”

germanium concentration and the second layer that includes “about 60%” germanium. (*Id.*, ¶[0042]; Ex. 1002, ¶158.)

Liao further discloses that “the higher the Ge concentration in the epitaxial structure is, the higher the driving current of the device will be, and thus the power is higher, such that the overall performance of the device is improved.” (Ex. 1008, ¶¶[0018]-[0019], [0022]; *see also id.*, ¶¶[0004], [0006]; Ex. 1009, ¶[0042]-[0043]; Ex. 1005, ¶[0044]; Ex. 1002, ¶159.)

A POSITA implementing a FinFET device like that disclosed by Wann would have looked to Liao, particularly because Wann and Liao are in the same field and disclose FinFET devices with silicon-germanium epitaxial material in source/drain regions. (Ex. 1002, ¶160.) Having looked to Liao, such a POSITA would have found it obvious to implement the SiGe strained material in a device like that disclosed by Wann such that it includes at least 50% germanium as recited by claim 1. (*Id.*)

Wann does not disclose specific details regarding the percentage of germanium included in the SiGe material of the source/drain regions. (Ex. 1007, ¶[0025]; Ex. 1002, ¶161.) Liao, however, discloses that using SiGe with a germanium percentage of at least 45%, and more preferably of about 55-60%, results

in higher speed operation for the FinFET device. (Ex. 1008, ¶¶[0004]-[0005], [0047]; Ex. 1002, ¶162.)

A POSITA would have appreciated that using 55-60% germanium SiGe in a FinFET like that disclosed by Wann would have been nothing more than the simple substitution of one known element (Liao's 55-60% germanium SiGe source/drain regions) for another (Wann's unknown germanium content SiGe source/drain regions) to obtain the predictable result of a functional FinFET device with high-Ge percentage SiGe portions of source/drain regions. (Ex. 1002, ¶163.) *KSR* at 417. Put another way, Liao's 55-60% germanium SiGe source/drain regions would have been a "suitable option" in place of Wann's unknown germanium content SiGe source/drain regions. *Intel Corp.*, No. 2022-1037, 2023 WL 2469631, at *5 (citing *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797 (Fed. Cir. 2021)). Moreover, a POSITA would also have appreciated that using 55-60% germanium SiGe material would simply have been the use of a known technique (55-60% germanium as disclosed by Liao) in a similar device (Wann's FinFET) to realize the advantage of better performance. (Ex. 1002, ¶163.) *KSR* at 417.

Using a germanium concentration of at least 50% in a SiGe source/drain region would have been a matter of routine optimization of a result-effective variable (the percentage of germanium), well within a POSITA's grasp and technical ability.

(Ex. 1002, ¶164.) See *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1010 (Fed. Cir. 2018) (“[D]iscovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art.”) (quoting *In re Boesch*, 617 F.2d 272, 276 (CCPA 1980)).

Liao discloses SiGe source/drain regions that include germanium concentrations of “equal to or higher than 45%, preferably up to 55-60%.” (Ex. 1008, ¶[0047].) Thus, Liao’s disclosed range of 45% or greater overlaps the claimed range of 50% or greater. (Ex. 1002, ¶164.) See *E.I. DuPont de Nemours & Co.*, 904 F.3d at 1006-11 (concluding that a *prima facie* case of obviousness exists when the prior art range overlaps a claimed range); *In re Aller*, 220 F.2d 454, 456 (CCPA 1955) (“[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”).

The percentage of germanium in the SiGe source/drain regions is a result-effective variable because the germanium percentage was known to effect the strain stress generated in the channel region and improve the performance of the device. (Ex. 1008, ¶[0004]-[0005]; Ex. 1005, ¶¶[0013], [0023], [0044]; Ex. 1001, 3:31-33, 7:46-49; Ex. 1002, ¶165.) See *In re Applied Materials, Inc.*, 692 F.3d 1289, 1297 (Fed. Cir. 2012) (“A recognition in the prior art that a property is affected by the

variable is sufficient to find the variable result-effective.”). This known relationship, coupled with Liao’s disclosure of a range (greater than 45%) overlapping the claimed range, as well as disclosing specific examples (55-60%) within the claimed range, is sufficient to render this claim obvious.

This is especially true given that the ’334 patent provides no evidence that the claimed range has any criticality or produces a new or unexpected result. Indeed, the ’334 patent simply states that “the Ge-rich layer material may be SiGe, having Ge in the range of 50-99%” (Ex. 1001, 49-51) without any explanation as to why the 50% bottom end of the range is specified. (Ex. 1002, ¶165.)

Liao’s disclosure of embodiments having 55%-60% germanium SiGe also confirms that a POSITA could have readily derived the claimed feature via routine optimization. (Ex. 1002, ¶165.) Thus, the claimed percentage of germanium cannot form the basis of patentability, given it is a result-effective variable that a POSITA would have found obvious to optimize.

Based on their knowledge and Liao’s disclosure, a POSITA would have had a reasonable likelihood of success. (Ex. 1002, ¶166.) Indeed, Liao discloses how to form such SiGe portions of source/drain regions in a similar device structure to that of Wann, and a POSITA would have been able to implement the strained material using at least 50% germanium SiGe as claimed. (*Id.*) Indeed, a POSITA would have

understood that Wann using germanium alone for the strained material demonstrates that high-percentage germanium SiGe is compatible with Wann's device, and there is nothing difficult about controlling the germanium percentage in SiGe. (*Id.*, ¶167.)

Therefore, the Wann-Liao combination discloses or suggests claim features 1[d]-[e] for the reasons discussed for the germanium strained material presented in sections IX.D.1(d)-(e) above, where, instead of the germanium, at least 50% germanium silicon-germanium (SiGe) is used. (*Id.*, ¶168.) The remaining features of claims 1, 2, 10, and 12 are disclosed or suggested by the Wann-Liao combination for the same reasons presented in sections IX.D.1-2 and IX.D.6-7 above. (*Id.*)

2. Claim 5

Wann in view of Liao discloses or suggests this limitation. (Ex. 1002, ¶169.) The Wann-Liao combination discloses or suggests at least 50% germanium SiGe strained material ("first/second portions"), which includes silicon. (Section IX.G.1; Ex. 1002, ¶169.)

3. Claim 6

Wann in view of Liao discloses or suggests this limitation. (Ex. 1002, ¶¶170-171.) As discussed above in section IX.D.3, a POSITA would have understood that the strained material would include p-type dopants for a p-type FinFET. (Section IX.D.3; Ex. 1007, ¶[0025]; Ex. 1002, ¶170.) To the extent PO argues that Wann

does not explicitly disclose that the “first and second portions” “include a p-type dopant,” it would have been obvious to include a p-type dopant for Wann’s p-type transistor. (Ex. 1002, ¶170.) Moreover, Liao discloses doping the epitaxial portions of source/drain regions with boron, which is a p-type dopant, and a POSITA would have found it obvious to dope the strained material of the Wann-Liao combination with boron in view the disclosure of Wann, Liao, and their knowledge of p-type devices and dopants. (Ex. 1008, ¶[0048], ¶[0050]; Ex. 1002, ¶171.)

4. Claim 7

As discussed above in section IX.D.4, Wann discloses that the “surface that consists essentially of silicon” is part of a “crystalline silicon substrate (e.g., wafer)” and therefore is undoped. (Section IX.D.4; Ex. 1002, ¶172.) To the extent PO argues that Wann does not explicitly disclose that the crystalline silicon substrate is undoped, using an undoped silicon substrate would have been obvious. (Ex. 1002, ¶173.) For example, because Wann does not indicate that the silicon wafer is doped, a POSITA would have found it obvious to leave the silicon wafer undoped as it would have eliminated the doping operation and simplified processing. (*Id.*) Moreover, leaving the silicon surface undoped would have been obvious for a POSITA to choose (i.e., obvious to try) as it is one of a finite number of predictable options (doped or undoped). (*Id.*)

H. Ground 8 – Wann in View of Liao and Kuhn Renders Claim 12 Obvious

1. Claim 12

For reasons similar to those presented above for the Murthy-Kuhn combination, a POSITA would have found it obvious to implement a non-planar transistor like that disclosed or suggested by the Wann-Liao combination in a computing system. (Sections IX.B.1, IX.G.1; Ex. 1002, ¶174.)

I. Ground 9 – Wann in View of Liao and Ching Renders Claim 11 Obvious

1. Claim 11

Wann in view of Liao and Ching discloses or suggests the features of claim 11. (Ex. 1002, ¶¶175-177.) As discussed above in section IX.G.1, a POSITA would have found it obvious to use SiGe with a germanium concentration of at least 50% in non-planar devices as disclosed or suggested by the Wann-Liao combination. As discussed above in section IX.F.1, a POSITA would have found it obvious, in view of Ching, to include nanowires in the non-planar devices of Wann such that the Wann-Ching combination discloses or suggests the features of claim 11. For the same reasons discussed above in section IX.F.1, a POSITA would have found it obvious to use nanowires, as disclosed by Ching, in the non-planar device of the Wann-Liao combination. (Ex. 1002, ¶¶176-177.) The use of $\geq 50\%$ germanium

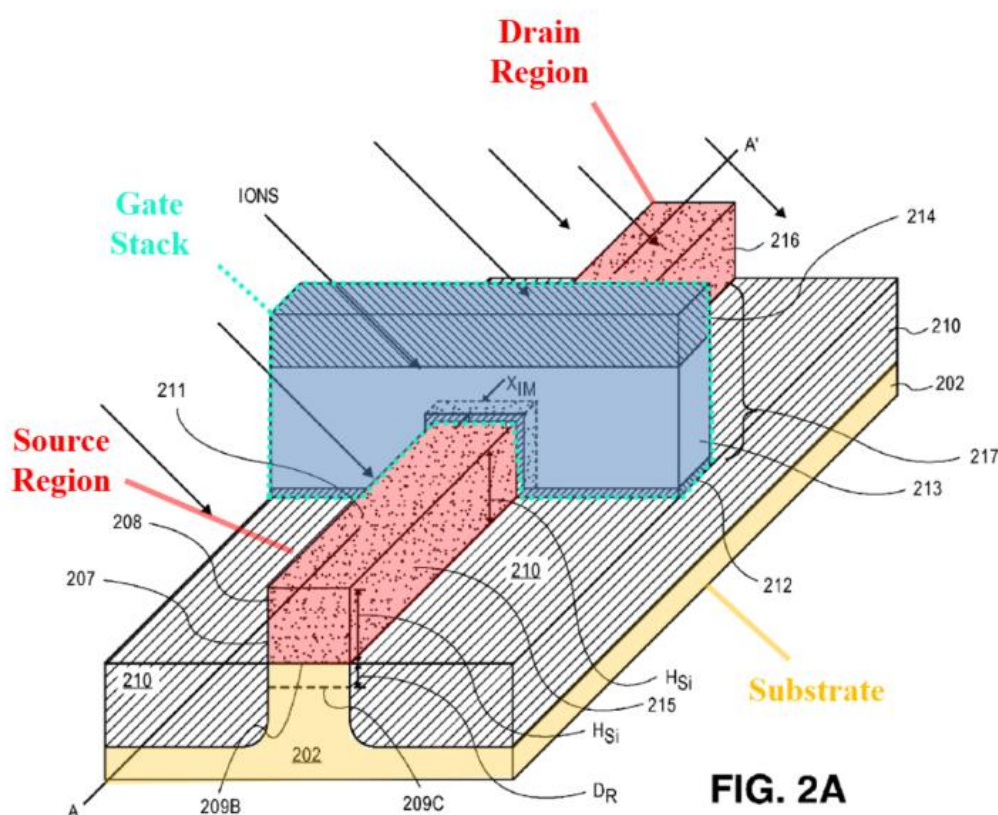
SiGe for the strained material does not impact the use of nanowires in the channel. (Ex. 1002, ¶177.) Therefore, the Wann-Liao-Ching combination discloses or suggests the features of claim 11 for the same reasons discussed above in section IX.F, where, instead of germanium strained material as discussed in section IX.D, the non-planar devices have SiGe strained material as discussed in section IX.G.1. (*Id.*)

J. Ground 10 – Wann in View of Cappellani Renders Claims 1-2, 5-7, 10, and 12 Obvious

1. Claims 1-2, 10, and 12

Wann in view of Cappellani discloses or suggests the features of claims 1-2, 10, and 12. (Ex. 1002, ¶¶178-190.) Wann discloses an embodiment where the strained material (“first/second portions”) of the source/drain regions is silicon-germanium (SiGe), but does not explicitly disclose that the strained material has at least 50 percent germanium as recited in claim 1. (Ex. 1007, ¶[0025]; Ex. 1002, ¶179.) Cappellani, however, discloses forming epitaxial regions for the source/drain regions in a similar FinFET device using $\geq 50\%$ germanium SiGe, and, in view of Cappellani, a POSITA would have found it obvious to form the epitaxial regions (i.e., strained material) in the device like that disclosed by Wann using $\geq 50\%$ germanium SiGe. (Ex. 1002, ¶179.)

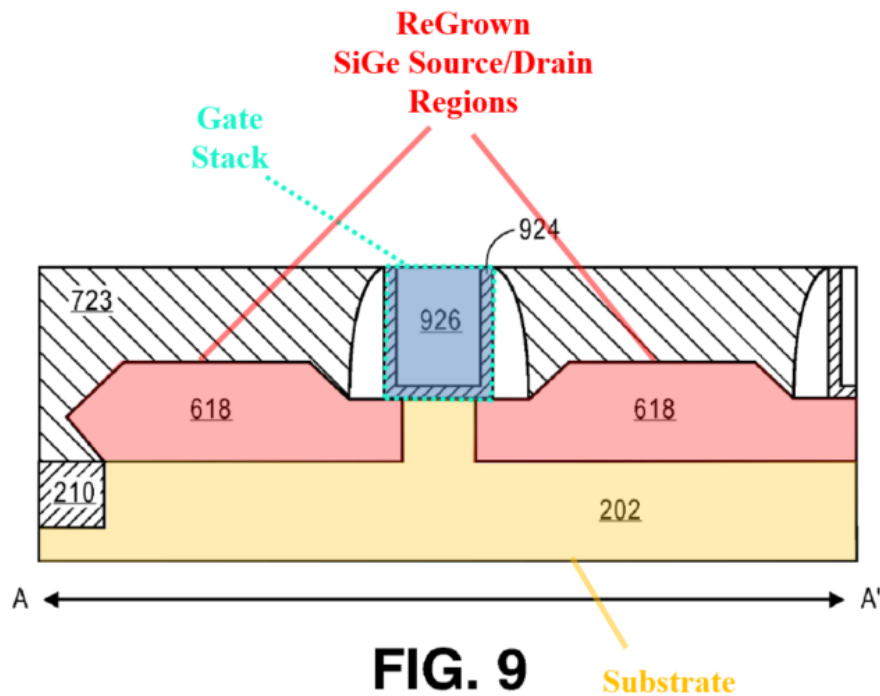
Like Wann, Cappellani discloses forming a FinFET device that includes source/drain regions. (Ex. 1009, ¶[0022] (“Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’).”); Ex. 1002, ¶180.) Annotated figure 2A of Cappellani below shows the FinFET at an early stage of fabrication. (Ex. 1009, ¶¶[0007], [0026].)



(Ex. 1009, FIG. 2A (annotated); Ex. 1002, ¶180.)

Cappellani discloses doping the source/drain regions of the fin portion to allow for very accurate etching to form cavities for regrown source/drain regions. (Ex. 1009, ¶¶[0027], [0030]-[0031], [0033]-[0035], FIGs. 2A-B, 4A-C; Ex. 1002,

¶181.) Cappellani further discloses that after selectively etching to form the source/drain cavities, epitaxial deposition is used to form the source/drain regions. (Ex. 1009, ¶[0041]; Ex. 1002, ¶182.) Cappellani discloses the stress on the channel region in the resulting FinFET “increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current,” where stress can be imparted by using a silicon-germanium alloy with 10-80% germanium in the source/drain regions (Ex. 1009, ¶¶[0042]-[0043], [0045] [0050]; Ex. 1002, ¶182.)



(Ex. 1009, FIG. 9 (annotated); Ex. 1002, ¶183.)

A POSITA implementing a FinFET device like that disclosed by Wann would have looked to Cappellani for guidance, particularly because Wann and Cappellani are references in the same field and disclose FinFET devices with epitaxially deposited silicon-germanium in the source/drain regions. (Ex. 1002, ¶184.) Having looked to Cappellani, such a POSITA would have found it obvious to implement the SiGe strained material in the source/drain regions in a device like that disclosed by Wann such that it includes at least 50% germanium as recited in claim 1 and as disclosed by Cappellani for the same reasons discussed above for the Wann-Liao combination in section IX.G. (*Id.*, ¶¶184-185.)

Using $\geq 50\%$ germanium SiGe material as disclosed by Cappellani would have simply been the use of known material in a similar device to obtain a predictable result. (*Id.*, ¶186.) Moreover, using a germanium concentration of at least 50% would have been a matter of routine optimization of a result-effective variable (the percentage of germanium), well within a POSITA's grasp and technical ability. (Section IX.G.1) Like Liao's range, Cappellani's disclosed range of 10-80% overlaps the claimed range of 50% or greater and confirms that a POSITA could have readily derived the claimed feature via routine optimization. Thus, the claimed percentage of germanium cannot form the basis of patentability, given it is a result-

effective variable that a POSITA would have found obvious to optimize. (Ex. 1002, ¶¶186-187.)

Based on their knowledge and Cappellani's disclosure of using 10-80% germanium SiGe in a FinFET device similar to that of Wann, a POSITA would have had a reasonable likelihood of success. (Ex. 1002, ¶¶188-189.)

Therefore, the Wann-Cappellani combination discloses or suggests claim elements 1[d]-[e] for the reasons discussed for the germanium strained material presented in section IX.D.1(d)-(e) above, where, instead of the germanium strained material, $\geq 50\%$ silicon-germanium (SiGe) strained material ("first/second portions") is included. The remaining features of claims 1, 2, 10, and 12 are disclosed or suggested by the Wann-Cappellani combination for the same reasons presented in sections IX.D.1-2 and IX.D.6-7 above. (Ex. 1002, ¶¶190.)

2. Claim 5

The Wann-Cappellani combination discloses or suggests this limitation. (Ex. 1002, ¶191.) As discussed above for claim elements 1[d]-[e], the Wann-Cappellani combination discloses or suggests $\geq 50\%$ germanium SiGe strained material ("first/second portions"), which includes silicon. (Section IX.J.1; Ex. 1002, ¶191.)

3. Claim 6

The Wann-Cappellani combination discloses or suggests this limitation. (Ex. 1002, ¶¶192-194.) As discussed above in section IX.D.3, a POSITA would have understood that the strained material includes p-type dopants for a p-type FinFET. (Ex. 1007, ¶[0025]; Ex. 1002, ¶192.) To the extent PO argues that Wann does not explicitly disclose this claim feature, it would have been obvious for Wann’s p-type FinFET. (Ex. 1002, ¶192.) Moreover, Cappellani discloses doping the epitaxial portions of source/drain regions for a PMOS (p-type) FinFET with boron, which is a p-type dopant. (Ex. 1009, ¶¶[0043], [0045], [0050]; Ex. 1002, ¶193.)

In view of their own knowledge and Cappellani’s disclosure, a POSITA would have found it obvious to use boron (“a p-type dopant”) to dope the strained material. (Ex. 1002, ¶¶193-194.) Cappellani describes details as to the appropriate dopant to use for a p-type transistor that are not explicitly disclosed by Wann, thereby motivating a POSITA to look to, and implement, Cappellani’s teachings.

4. Claim 7

As discussed above in section IX.D.4, Wann discloses that the “surface that consists essentially of silicon” is part of the silicon substrate 202, which can be a “crystalline silicon substrate (e.g., wafer)” and therefore is undoped. (Section IX.D.4; Ex. 1002, ¶195.) To the extent PO argues that Wann does not explicitly

disclose claim 7, the Wann-Cappellani combination discloses or suggests this feature for the same reasons presented in section IX.G.4. (Ex. 1002, ¶¶195-196.)

Moreover, Cappellani discloses doping the source/drain regions of the fin portion of the silicon substrate in order to allow for very accurate etching of the doped regions to form cavities for subsequent formation of regrown source/drain regions. (Ex. 1009, ¶¶[0027], [0030]-[0031], [0033]-[0035], FIGs. 2A-B, 4A-C; Ex. 1002, ¶197.) Therefore, like Wann, Cappellani discloses removing/etching fin regions 208 and then regrowing a different material, e.g., SiGe of high Ge content, to serve as source/drain regions for a FinFET device. (Ex. 1009, ¶¶[0022], [0025]). A POSITA would have recognized that Cappellani's method of providing accurate etching would have been provided the same benefits to the FinFET device of the Wann-Cappellani combination, including better control of the etch profile and improved electrical performance for the FinFET. (Ex. 1002, ¶198; Ex. 1009, ¶¶[0025], [0033], [0050] (disclosing that the regrown source/drain regions form an "abrupt boundary" between the source/drain regions with another region); Ex. 1002, ¶198.)

Therefore, a POSITA would have found it obvious to leave the portions of the fins that are not etched away (e.g. channel region and lower portion of the fin under the source/drain regions) in the Wann-Cappellani combination undoped in order to

allow for more accurate etching as disclosed by Cappellani. (Ex. 1002, ¶199.)

Therefore the Wann-Cappellani combination discloses or suggests claim 7.

**K. Ground 11 – Wann in View of Cappellani and Kuhn Renders
Claim 12 Obvious**

1. Claim 12

For reasons similar to those presented above for the Murthy-Kuhn combination, a POSITA would have found it obvious to implement a non-planar transistor like that disclosed or suggested by the Wann-Cappellani combination in a computing system. (Sections IX.B.1, IX.J.1; Ex. 1002, ¶200.)

**L. Ground 12 – Wann in View of Cappellani and Ching Renders
Claim 11 Obvious**

1. Claim 11

Wann in view of Cappellani and Ching discloses or suggests the features of claim 11 for the same reasons discussed above for the Wann-Liao-Ching combination discussed in section IX.H above, where the inclusion of $\geq 50\%$ germanium SiGe strained material is disclosed or suggested by the Wann-Cappellani combination discussed above in section IX.J.1 instead of by the Wann-Liao combination discussed above in section IX.G.1. (Ex. 1002, ¶¶201-203.)

X. Discretionary Denial is not Appropriate

A. The Board Should Not Deny Institution Under *Fintiv*

The six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because Samsung has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** is neutral. Jury selection is scheduled for May 20, 2024. (Ex. 1023, 1.) Even if trial proceeds as scheduled, the timing does not tip in favor of denying institution in this case as a FWD would be expected around October 2024. *See also, e.g., Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13 (PTAB June 3, 2021).

The **third factor** weighs against denial. The district court case is in its infancy, and the parties have made little investment to date. PO filed its complaint on September 12, 2022, served its initial infringement contentions on November 17, 2022, and filed an amended complaint on January 24, 2023. Petitioner's diligence in pursuing this petition less than seven months after PO's Complaint and not long after receiving the infringement contentions weighs in favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions). Indeed, Petitioner already filed two IPR petitions against another patent asserted in the district court litigation, IPR2023-00562 and -00562.

The **fourth factor** weighs against denial because this Petition challenges claims 8, 16-18, and 20 which are not asserted against Petitioner in district court. This IPR petition is thus the only venue in which certain invalidity challenges will be adjudicated, which promotes system efficiency. *See Fintiv*, Paper 11 at 4. Accordingly, this factor weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial given the undeniable similarity between the prior art references presented herein and the '334 patent. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021); *see also* Section IX. Indeed, as shown above, both Murthy and Wann independently anticipate many of the challenged claims. Thus, this is a highly meritorious Petition which “strengthen[s] the patent system by allowing the review of patents challenged with a sufficiently strong initial merits showing of unpatentability.” *CommScope Tech. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 43 23 at 4 (Feb. 27, 2023) (precedential). There is also a significant public interest against “leaving bad patents enforceable,” and institution

will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020)

XI. Conclusion

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1, 2, 5-8, 10-14, 16-18, and 20 of the '334 patent.

Respectfully submitted,

Dated: April 12, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,541,334 contains, as measured by the word processing system used to prepare this paper, 12,960 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: April 12, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on April 12, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,541,334 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record:

Finch & Maloney PLLC
50 Commercial Street
Gateway One, Suite 300
Manchester, NH 03101

Respectfully submitted,

Dated: April 12, 2023

By: /Naveen Modi/
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