

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 10,541,334

**DECLARATION OF DR. STANLEY SHANFIELD IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,541,334**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND AND QUALIFICATIONS	1
III.	MATERIALS REVIEWED.....	5
IV.	LEVEL OF ORDINARY SKILL IN THE ART	7
V.	TECHNICAL BACKGROUND	8
A.	Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs).....	8
B.	Fin Field Effect Transistors (FinFETs)	13
C.	Nanowire FET	15
VI.	OVERVIEW OF THE '334 PATENT.....	20
VII.	CLAIM CONSTRUCTION.....	23
VIII.	OVERVIEW OF THE PRIOR ART	24
A.	Murthy.....	24
B.	Wann	26
C.	Ching.....	29
D.	Liao	31
E.	Cappellani.....	33
IX.	THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS	35
A.	Murthy Discloses the Features of Claims 1, 2, 5-8, 10, 12-14, and 16.....	35
1.	Claim 1.....	36
2.	Claim 2.....	47
3.	Claim 5.....	48
4.	Claim 6.....	49
5.	Claim 7.....	52

6.	Claim 8.....	53
7.	Claim 10.....	54
8.	Claim 12.....	55
9.	Claim 13.....	56
10.	Claim 14.....	59
11.	Claim 16.....	60
B.	Murthy in Combination with Kuhn Discloses or Suggests the Features of Claim 12	60
1.	Claim 12.....	60
C.	Murthy in Combination with Ching Discloses or Suggests the Features of Claims 11, 17, 18, and 20	63
1.	Claim 11.....	63
2.	Claim 17.....	71
3.	Claim 18.....	74
4.	Claim 20.....	75
D.	Wann Discloses All of the Features of Claim 1, 2, 6-8, 10, and 12-14	75
1.	Claim 1.....	75
2.	Claim 2.....	91
3.	Claim 6.....	92
4.	Claim 7.....	92
5.	Claim 8.....	93
6.	Claim 10.....	95
7.	Claim 12.....	96
8.	Claim 13.....	97
9.	Claim 14.....	103
E.	Wann in Combination with Kuhn Discloses or Suggests the Features of Claim 12	103
1.	Claim 12.....	103
F.	Wann in Combination with Ching Discloses or Suggests the Features of Claims 11, 17, and 18	106
1.	Claim 11.....	106
2.	Claim 17.....	114
3.	Claim 18.....	117
G.	Wann in Combination with Liao Discloses or Suggests the Features of Claims 1, 2, 5-7, 10, and 12	118
1.	Claims 1, 2, 10, and 12.....	118

2.	Claim 5.....	126
3.	Claim 6.....	127
4.	Claim 7.....	128
H.	Wann in Combination with Liao and Kuhn Discloses or Suggests the Features of Claim 12	129
1.	Claim 12.....	129
I.	Wann in Combination with Liao and Ching Discloses or Suggests the Features of Claim 11	130
1.	Claim 11.....	130
J.	Wann in Combination with Cappellani Discloses or Suggests the Features of Claims 1, 2, 5-7, 10, and 12	131
1.	Claims 1, 2, 10, and 12.....	131
2.	Claim 5.....	139
3.	Claim 6.....	140
4.	Claim 7.....	142
K.	Wann in Combination with Cappellani and Kuhn Discloses or Suggests the Features of Claim 12	145
1.	Claim 12.....	145
L.	Wann in Combination with Cappellani and Ching Discloses or Suggests the Features of Claim 11	146
1.	Claim 11.....	146
X.	CONCLUSION	147

I, Stanley Shanfield, declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 10,541,334 (“the ’334 patent”) (Ex. 1001). I have been asked to consider whether certain references disclose or suggest the features recited in claims 1, 2, 5-8, 10-14, 16-18, and 20 of the ’334 patent. My opinions are set forth below.

2. I am being compensated at a rate of \$385/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and fabricating integrated circuits, including interconnect structures used in such integrated circuits.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current

curriculum vitae, which details my education and professional and academic experience, is attached as an addendum with this declaration. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I received a B.S. in Physics from the University of California, Irvine in 1977. I received the University of California Regents Award for Outstanding Research Project for my experimental and theoretical work on rotating relativistic electron beams. Under full ERDA (DOE) scholarship, I received a Ph.D. in Physics from the Massachusetts Institute of Technology in 1981.

6. After receiving my doctorate degree, I worked at Spire Corporation in Bedford, Massachusetts from 1981-1984, where I served as a Staff Scientist, and later, a Senior Staff Scientist. At Spire, I developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. In addition, I built, operated, and characterized an ion-assisted deposition system for making coating for semiconductor and machine tool industries.

7. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers (photoresist, polyimide, etc.). For example, I developed a low

damage, high selectivity process as part of the FET gate formation step. I was responsible for purchasing equipment and developing processes for several plasma systems typical of those used in the semiconductor industry, including load-locked RIE, microwave ECR RIE, barrel etchers, single-wafer elevated temperature RIE systems, etc.

8. In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300 employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

9. From 1999-2001, I worked at AXSUN Technologies as part of the founding team, first as the Director of Manufacturing & Wafer Fab Technology, and later, as the Vice President of Operations. As Director of Manufacturing & Wafer Fab Technology, I led device and module manufacturing, creating a wafer fab and circuit board assembly infrastructure; my responsibilities included hiring over 70 individuals and leading production design efforts. In my role as Vice President of

Operations, I designed, fabricated, and productized AXSUN's microelectromechanical (MEM) Fabry-Perot optical filter, and I managed a new generation of electronics module design. In addition, I established a process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator devices. As a result of my work at AXSUN, I was awarded patents on semiconductor processing and control electronics.

10. I have served since 2003 at the Charles Stark Draper Laboratory ("Draper Laboratory") in Cambridge, Massachusetts, ultimately becoming a Distinguished Member of Technical Staff and Technical Director in Advanced Hardware Development. I led the Advanced Hardware Development Division (approximately 80 staff) in their work on the laboratory's multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization operations in MEMS devices, and I have been involved in their operation and optimization.

11. I have authored more than 25 journal and conference papers. My publications include numerous papers on topics relating to semiconductor processing, advanced semiconductor devices, electronic circuit design and packaging. I have been invited to give professional talks at various conferences. I am also a co-inventor of several U.S. Patents.

12. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

13. The opinions in this Declaration are based on the documents I reviewed, my knowledge and experience, and professional judgment. In forming my opinions expressed in this Declaration, I have reviewed the following materials: U.S. Patent No. 10,541,334 (Ex. 1001); the prosecution history of U.S. Patent No. 10,541,334 (Ex. 1004); U.S. Patent Publication No. 2012/0153387 to Murthy et al. (“Murthy”) (Ex. 1005); U.S. Patent Publication No. 2015/0053928 to Ching et al. (“Ching”) (Ex. 1006); U.S. Patent Publication No. 2015/0035017 to Wann *et al.* (“Wann”) (Ex. 1007); U.S. Patent Publication No. 2014/0335674 to Liao *et al.* (“Liao”) (Ex. 1008); U.S. Patent Publication No. 2011/0147842 to Cappellani *et al.* (“Cappellani”) (Ex. 1009); U.S. Patent Publication No. 2012/0138886 to Kuhn *et al.* (“Kuhn”) (Ex. 1010); U.S. Patent Publication No. 2013/0277752 to Glass *et al.* (“Glass”) (Ex. 1011); U.S. Patent Publication No. 2015/0137181 to Basker *et al.* (“Basker”) (Ex. 1012); U.S. Patent Publication No. 2016/0181366 to Oh *et al.* (“Oh”) (Ex. 1013); U.S. Patent No. U.S. Patent 9,379,108 to Wann *et al.* (“Wann-108”) (Ex. 1014); Neaman, Semiconductor Physics and Devices (Third Edition), 2003 (“Neaman”) (Ex. 1015); Hisamoto et al., FinFET- A self-Aligned Double-Gate MOSFET

Scalable to 20 nm, IEEE Transactions on Electronic Devices, Vol. 47, No 12, December 2000 (“Hisamoto”) (Ex. 1016); Plummer *et al.*, Silicon VLSI Technology, Fundamentals, Practice and Modeling, 2000 (“Plummer”) (Ex. 1017); Leobandung *et al.*, Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Channel Effects, J. Vac. Sci. Technol. B 15(6), Nov/Dec 1997 (“Leobandung”) (Ex. 1018); Tang *et al.*, FinFET – A Quasi-Planar Double-Gate MOSFET, 2001 IEEE International Solid-State Circuits Conference, 2001 (“Tang”) (Ex. 1019); Thelander *et al.*, Nanowire-Based One-Dimensional Electronics, MaterialsToday Vol. 9, No. 10, October 2006 (“Thelander”) (Ex. 1020); Iwai, Roadmap for 22nm and Beyond, Microelectron. Eng. 2009 (Iwai) (Ex. 1021); and any other materials I refer to in this declaration in support of my opinions.

14. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the ’334 patent at the time of the alleged invention, which I have been asked to initially consider as the mid 2010s (including March 21, 2014, the filing date of International Application PCT/US2014/031486 (“the ’486 PCT application”) to which the ’334 patent claims priority, which I understand is the earliest possible priority date for the ’334 patent).

My opinions reflect how one of ordinary skill in the art would have understood the '334 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

15. Based on my experience and expertise, it is my opinion that certain prior art references disclose or suggest all the features recited in claims 1, 2, 5-8, 10-14, 16-18, and 20 of the '334 patent, as I discuss in detail below.

IV. LEVEL OF ORDINARY SKILL IN THE ART

16. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '334 patent as of what I understand is the earliest possible priority date of March 21, 2014, which is the filing date of the '486 PCT application to which the '334 patent claims priority. Specifically, based on my review of the '334 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had a bachelor's degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person,

it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

17. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe (mid 2010s timeframe).

V. TECHNICAL BACKGROUND

18. In this section, I present a brief overview of certain aspects of transistors used in integrated circuits and the manufacture of such transistors at the time of the alleged invention that will assist in better understanding the '334 patent and the prior art that I discuss in this declaration.

A. Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

19. Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have long been used as building blocks for integrated circuits (ICs).

The MOSFET, in conjunction with other circuit elements, is capable of voltage gain and signal-power gain. The MOSFET is also used extensively in digital circuit applications where, because of its relatively small size, thousands of devices can be fabricated in a single integrated circuit. The MOSFET is, without doubt, the core of integrated circuit design at the present time.

(Ex. 1015, 449.)

20. A typical MOSFET includes four terminals, i.e., the gate terminal (G), the source terminal (S), the drain terminal (D), and the body terminal (B), as shown in the figure and corresponding symbol below. (*Id.*, 484.)

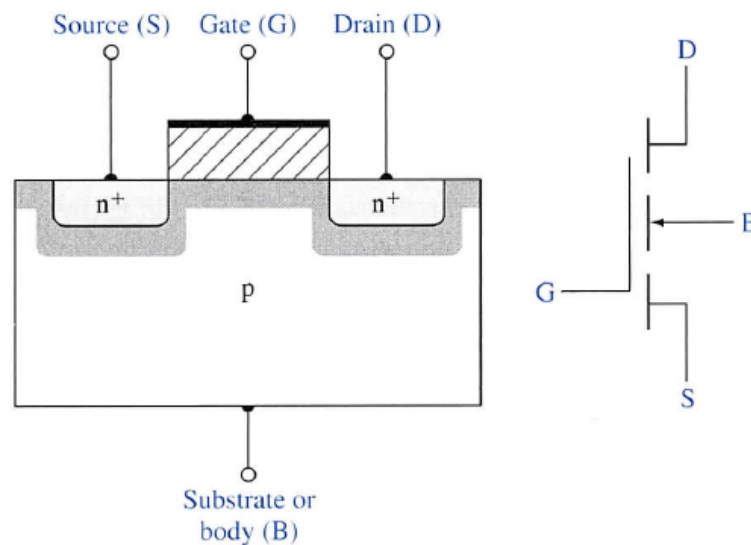
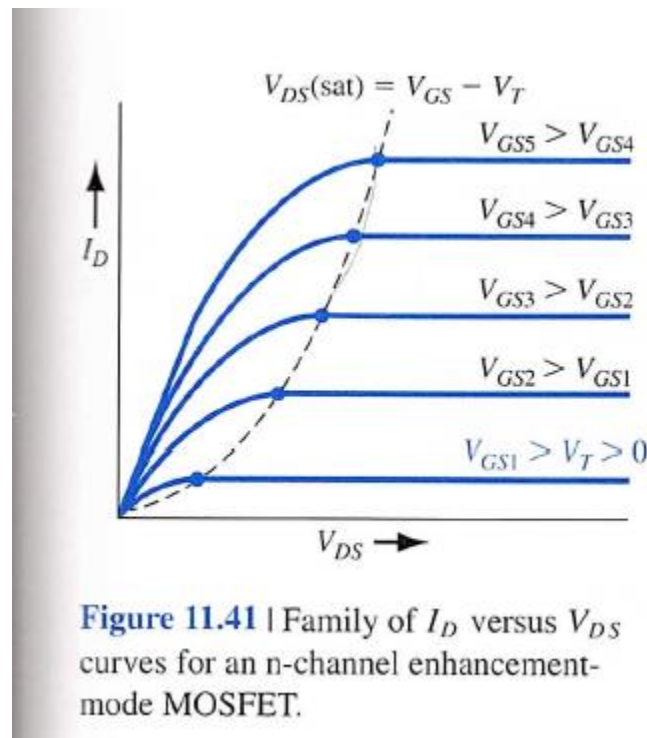


Figure 11.35 | Cross section and circuit symbol for an n-channel enhancement-mode MOSFET.

(*Id.*, FIG. 11.35.)

21. In many cases, a MOSFET functions like a switch. Using an n-channel MOSFET as an example, when a sufficiently large positive gate voltage is applied, an electron inversion layer is formed, which establishes a channel that connects the source and drain terminals, allowing the charge carriers to flow from the source terminal through the channel to the drain terminal. (*Id.*, 484; *see also id.*, 484-485 (disclosing that, in addition to n-channel MOSFETs, other known MOSFET types

are p-channel MOSFETs.) In particular, by applying a certain drain bias (V_{DS}) and a gate bias (V_{GS}) that is sufficiently large, i.e., larger than the threshold voltage (V_T) of the MOSFET, a current may flow through the MOSFET (i.e., from the source terminal, through the channel, and then to the drain terminal). (*Id.*, 484-490.) Under this scenario, the MOSFET is turned “on.”



(*Id.*, FIG. 11.41.) When the gate bias is less than the threshold voltage, no current (other than some leakage current) flows between the source and drain terminals. (*Id.*, 487 (“When $V_{GS} < V_T$, the drain current is zero.”).) Under this scenario, the MOSFET is turned “off.” In other words, a MOSFET may be turned on or off based on the voltage applied to the gate terminal.

22. In MOSFETs, the conductivity of semiconductor material may be modified by adding impurity atoms, which are known as dopant atoms or simply as dopants. (*Id.*, 103.) Depending on the type of dopants added, the dominant electrical charge carriers may either be electrons (negative charge carriers) or holes (positive charge carriers). (*Id.*; *see also id.*, 115 (“the real power of semiconductors is realized by adding small, controlled amounts of specific dopant, or impurity, atoms.... [Such] doping process can greatly alter the electrical characteristics of the semiconductor.”).) An n-type semiconductor refers to a semiconductor material that has electrons as the majority carrier, and a p-type semiconductor refers to a semiconductor material that has holes as the majority carrier. (*Id.*, 116-119 (discussion regarding typical dopants used for silicon, which is a semiconductor material, to form either an n-type or p-type semiconductor material).)

23. As the size of MOSFETs is downscaled in order to fit more transistors in a single device, the feature size (i.e., the physical dimensions of the device), including the channel length, is reduced. The reduction in feature size is reflected in Figure 1-2 of Plummer below.

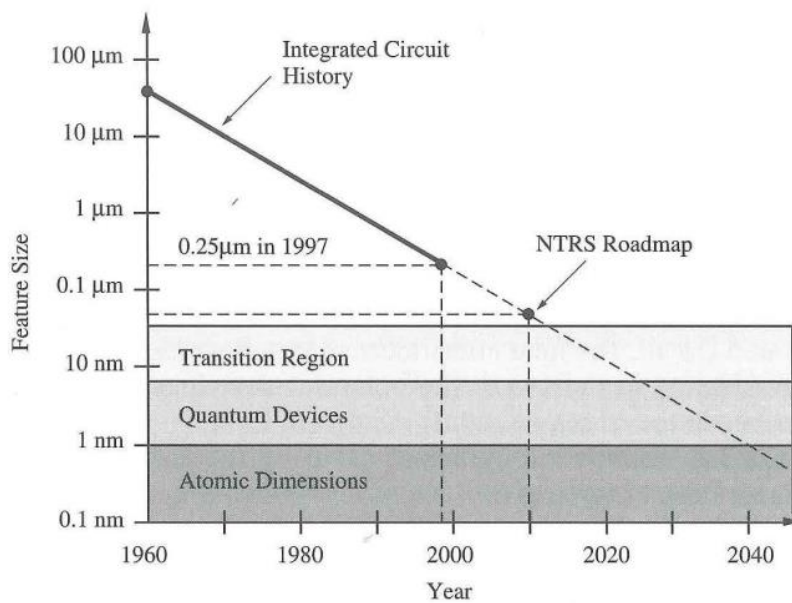


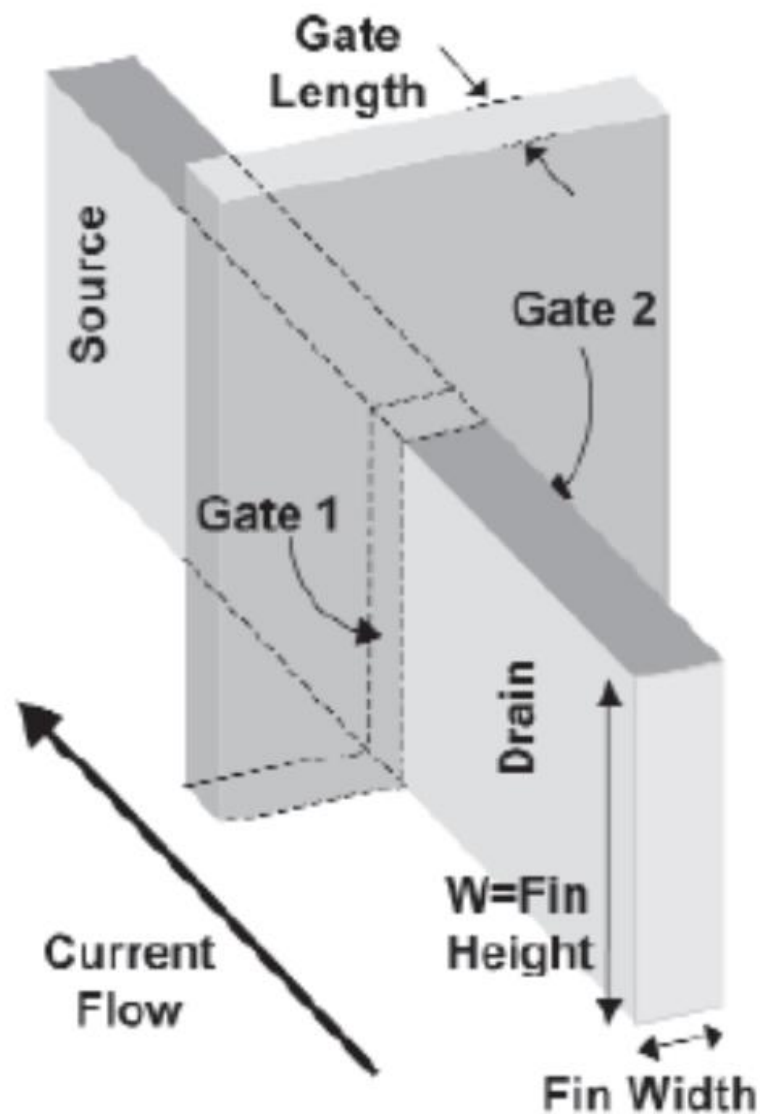
Figure 1-2 Historical trends and future projections for the minimum feature size used in integrated circuits in manufacturing.

(Ex. 1017, 3 (FIG. 1-2).) The reduced channel length leads to several non-ideal effects, including “short-channel effects” that negatively impact the performance of MOSFETs. For example, short-channel effects can lead to an increased leakage current, making it difficult to turn the transistor completely off. In other words, the gate terminal loses control of the channel’s conductivity as the channel remains conductive (i.e., conducting increased leakage current) even when the applied gate voltage should have the channel in the non-conductive (“off”) state. (Ex. 1018, 1 (“When the size of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) is reduced to the deep submicron regime, the transistors usually suffer severe short channel effects (SCEs). One of the effects is a large subthreshold slope, which leads to a large leakage current.”).) Increased leakage current can result

inefficient transistor operation and excess power consumption, thereby making it difficult to achieve low power operations as desired for many portable devices.

B. Fin Field Effect Transistors (FinFETs)

24. FinFETs are a non-planar form of MOSFET that provides better control of channel's conductivity by effectively having multiple gates, which can help combat short-channel effects. A FinFET has a slab of semiconductor material that is vertically oriented like a “fin” that extends from the surface of the substrate, where the gate generally wraps around the top and sides of the fin. The schematic below shows features of such a fin field-effect transistor (FinFET).



(Ex. 1019, 2 (FIG. 7.4.1).)

25. Such a FinFET is similar to the MOSFETs that I discuss above in Section V.A, as both include source/drain regions, a channel region, and a gate electrode. In a FinFET, however, the channel, source, and drain are located in the “fin” and a FinFET has multiple gates, e.g., on the vertical sidewalls of the fin for two-gate FinFETs, where three-gate FinFETs also have a gate on the top side of the

fin. A FinFET transistor is desirable because it can provide greater gate-to-channel overlap without significantly increasing the lateral dimensions of the transistor. The greater gate-to-channel overlap results in improved gate control, which can reduce short channel effects and unwanted leakage current. (Ex. 1019, 1 (“Scaling conventional CMOS transistors much below 50nm is difficult. Control of leakage currents requires gate dielectrics so thin and bodies doped so heavily that a process window sufficiently large for manufacturing might not be found. Double-gate MOSFET [e.g., FinFET] structures can overcome these and other limitations to transistor scaling. By placing a second gate on the opposite side of the device, the gate capacitance to the channel is doubled and the channel potential is better controlled by the gate electrode, thus limiting the leakage current.”).)

26. FinFETs may be fabricated using conventional MOSFET process technologies. (Ex. 1016, 1 (“The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.”), 5 (“In spite of its double-gate structure, FinFET is close to its root, the conventional MOSFET in terms of layout and fabrication. The result is a quasiplanar device.”).)

C. Nanowire FET

27. As discussed above, short channel effects in MOSFETs may be reduced by increasing the number of gates, such as by forming gate material over the top side

and the two vertical sidewalls of the fin of a FinFET in order to gain a better gate control. Nanowire FETs take this one step further and have the gate completely surround the channel. Like conventional MOSFETs and FinFETs, nanowire FETs include source/drain regions, a channel region, and a gate electrode. Nanowire FETs, however, include one or more wire-shaped channels, where the gate electrode completely surrounds the wire-shaped channel in a gate-all-around (GAA) structure. Such a nanowire FET is shown in Figure 1 of Leobandung below.

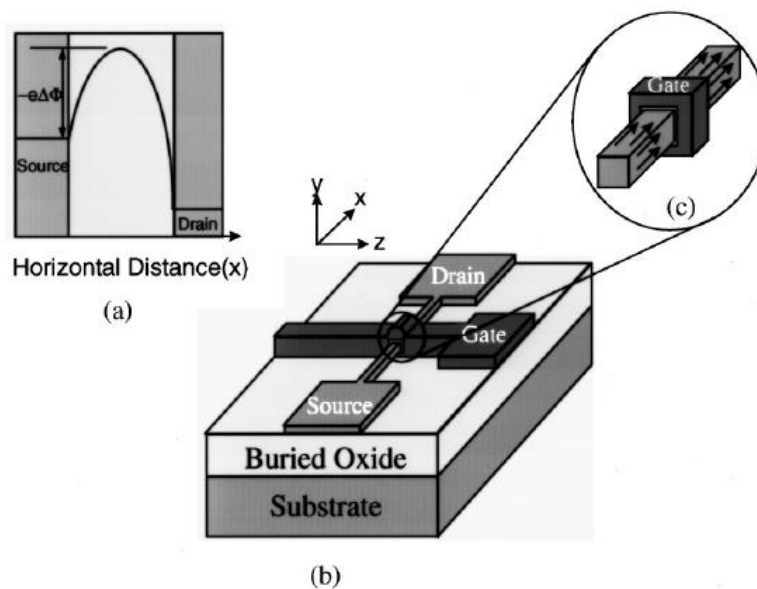


FIG. 1. WW MOSFET. (a) Electron potential profile between source and drain; (b) schematic of WW MOSFET; (c) in the WW structure, current flows along four surfaces of the channel.

(Ex. 1018, 1.) The gate-all-around nanowire structure provides even greater gate control and is beneficial as the semiconductor industry continues to downscale FETs to increase transistor performance and device functionality. The industry has been

aware of the gate-all-around concept for nanowire-like transistors, which helps suppress short channel effects and provide a better gate control, since the late 1990s.

When the size of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) is reduced to the deep submicron regime, the transistors usually suffer severe short channel effects (SCEs). ... Double-gate and silicon on insulator (SOI) DELTA MOSFETs have previously been proposed to suppress the SCEs. In the double-gate structure, a top gate and a bottom gate sandwich a thin silicon layer, giving better gate control over the channel potential than a conventional MOSFET. The SOI DELTA structure is essentially a vertical version of the double-gate structure, where the silicon channel has a narrow wall shape with two gates at both sides of the wall. Using these structures, near long channel behavior has been achieved in a transistor of 0.15 μm channel length.

However, to further reduce the SCEs, both the channel width and the channel thickness need to be reduced. **This will allow the gate to wrap around the channel and control the channel potential from all four surfaces, which leads to an optimum structure of reducing SCEs**—a wire-channel wrap-around-gate (WW) structure, shown in Fig. 1.

(*Id.*, (emphasis added).)

28. As the industry continued to downscale transistors sizes, universities and the semiconductor industry recognized that FinFETs and nanowire FETs were promising device structures. This is reflected in the semiconductor development roadmaps in figure 4 of Thelander and figure 19 of Iwai below. (Ex. 1020, 1 (“The roadmap for downscaling and introducing new technologies in the semiconductor industry is well laid out for the next ten years. In a special section on Emerging Research Devices in the International Technology Roadmap for Semiconductors, one-dimensional structures, such as carbon nanotubes and semiconductor nanowires, are explicitly mentioned as realistic additions.”), FIG. 4; Ex. 1021, Abstract (“In order to suppress the off-leakage current, double gate (DG) or fin-FET type MOSFETs are the most promising. Then, it is a natural extension for DG FETs to evolve to Si-nanowire MOSFETs as the ultimate structure of transistors for CMOS circuit applications. Si-nanowire FETs are more attractive than the conventional DG FETs because of higher on-current conduction due to their quantum nature and also because of their adoptability for high-density integration including that of 3D.”), 9 (“In the long term, Si-nanowire FETs are the most promising candidate because of process compatibility with the current planar CMOS LSIs, and also because of its small off-leakage current and high on-current.”), FIG. 19.)

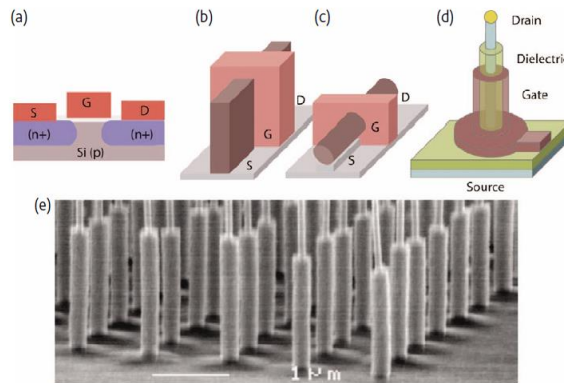


Fig. 4 Possible evolution of the field-effect transistor. (a) Metal-oxide-semiconductor FET (MOSFET): the planar gate affects the conducting channel from one direction. (b) FINFET: the gate surrounds the channel from all but one side. (c) Nanowire FINFET: complete, but nonuniform wrap-around gate. (d) Vertical nanowire FET: the gate has a complete, uniform wrap-around gate. (e) Vertical array of nanowires after wrap-gate formation. (Reprinted with permission from¹⁹. © 2006 Institute of Physics Publishing.)

(Ex. 1020, FIG. 4.)

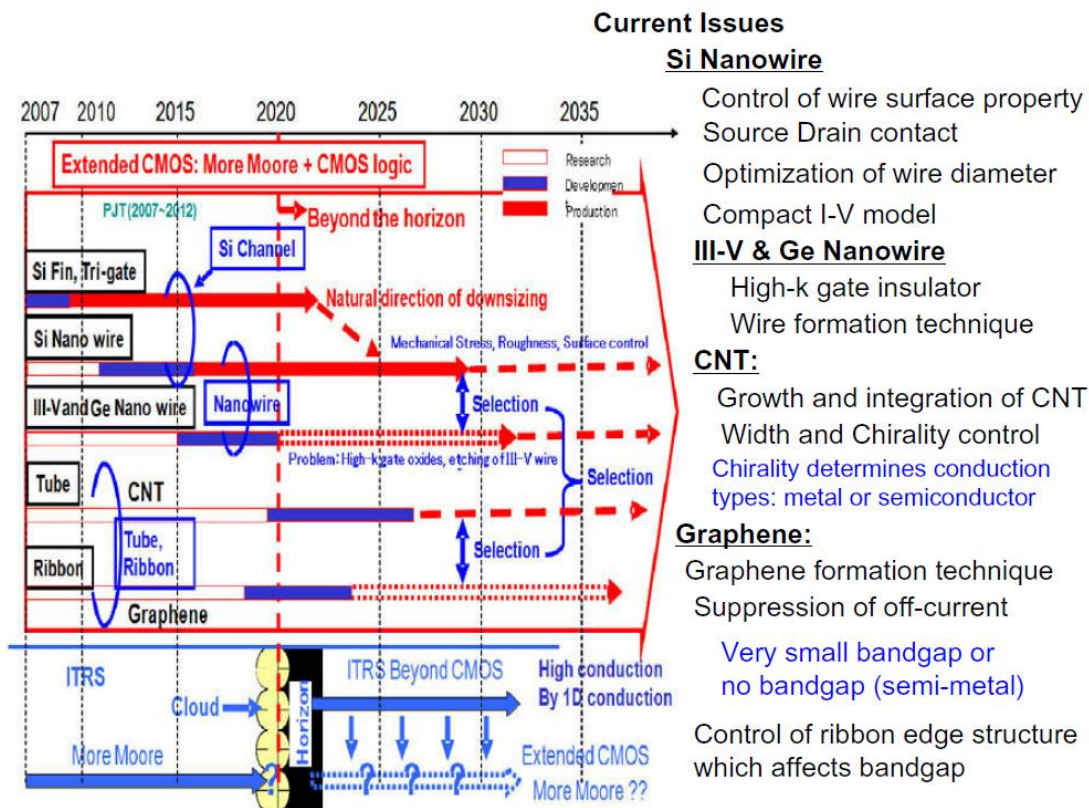


Fig. 19. Long range roadmap for logic CMOS transistors for next 30 years.

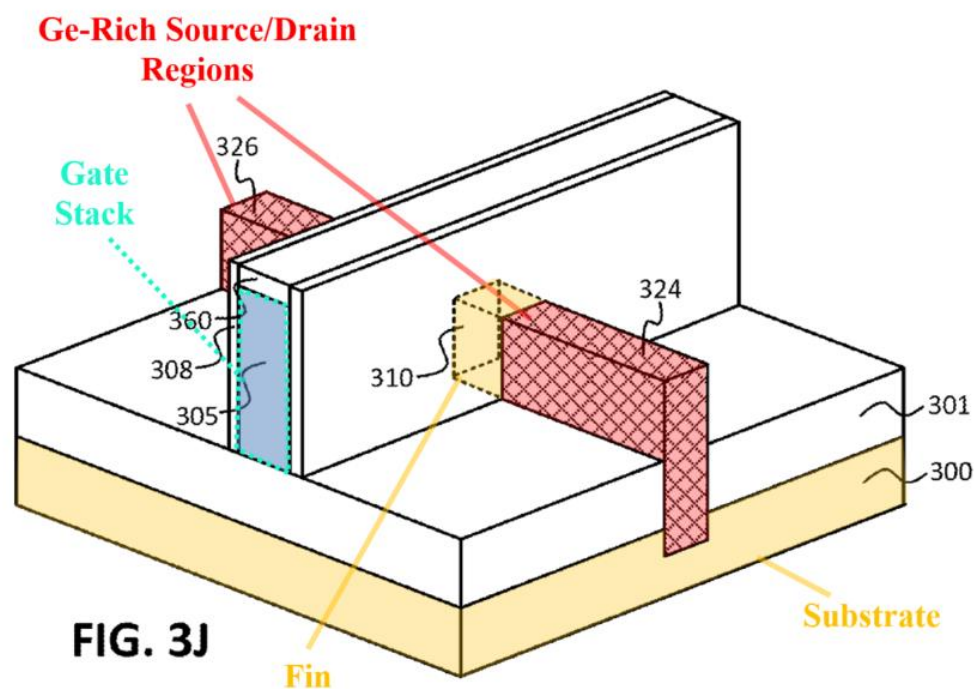
(Ex. 1021, FIG. 19.)

VI. OVERVIEW OF THE '334 PATENT

29. The '334 patent is entitled “Techniques for Integration of Ge-Rich P-MOS Source/Drain.” (Ex. 1001, Title.) The '334 patent discloses that “during design and manufacture or forming of metal-oxide-semiconductor (MOS) transistor devices, such as those used in complementary metal-oxide-semiconductor (CMOS) devices, it is often desired to minimize resistance associated with source/drain regions and contacts, otherwise known as components of external resistance.” (*Id.*, 1:21-26.) “Decreasing external resistance enables improved transistor current for a given source to drain.” (*Id.*, 1:26-28.)

30. According to the '334 patent, the inclusion of Ge-rich source/drain contacts reduces contact resistance, thereby promoting improved transistor performance. (*Id.*, 1:61-63, 2:21-26 (“As previously explained, increased drive current in transistors can generally be achieved by reducing external resistance, such as contact resistance. In some cases, contact resistance can be reduced for p-type MOS (p-MOS) transistors by using a germanium (Ge)-rich material as an effective ohmic contact material.”) The '334 patent further discloses that “[n]umerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., finned and nanowire/nanoribbon configurations).” (*Id.*, 2:10-14.)

31. Annotated figure 3J below shows a non-planar (e.g. finned) transistor architecture according to an embodiment disclosed by the '334 patent, where some of the details disclosed by the '334 patent with respect to different aspects of earlier-described planar transistor devices are also applicable to the non-planar transistor shown in figure 3J. (*Id.*, 1:45-48, 11:15-27.)



(*Id.*, FIG. 3J (annotated).)

32. As shown above, the FinFET transistor includes a gate stack that includes gate electrode 305 on three sides of the fin 310, where Ge-rich source/drain regions 324 and 326 lie on either side of the fin. (*Id.*, 11:32-34, 11:54-55, 12:6-7 (“FIG. 3J shows the structure of FIG. 3J after depositing 118 p-type Ge-rich layer 324/326.”).) The '334 patent further discloses that the “Ge-rich layer material may

be comprised of at least 50% Ge,” “in the range of 50-100%” Ge, or, in the case where the material includes silicon “may be comprised of Ge in the range of 50-99%.” (*Id.*, 10:12-16.) Additionally, the ’334 patent discloses that in the p-type (PMOS) transistor disclosed, “the Ge-rich layer is a p-type layer and therefore is p-type doped (e.g., B doped).” (*Id.*, 10:20-21; *see also id.*, 2:23-26, 2:60-64.)

33. In addition to the non-planar FinFET transistor shown in figure 3J above, the ’334 patent also discloses the non-planar nanowire transistor shown in annotated figure 4 below, where, instead of a fin-shaped channel, the transistor includes nanowires where the gate material surrounds the channel region on all sides. (*Id.*, 12:36-42.) The nanowire transistor includes nanowires 410 that can be silicon, germanium, or silicon-germanium. (*Id.*, 12:47-52.) As with the FinFET transistor, the nanowire transistor includes “Ge-rich layers” 424/426 deposited in the source drain regions. (*Id.*, 12:52-55.)

VIII. OVERVIEW OF THE PRIOR ART

A. Murthy

35. Murthy is entitled “Transistors with High Concentration of Boron Doped Germanium.” (Ex. 1005, Title) As shown in annotated figure 4 below, Murthy’s discloses a FinFET is formed using a substrate 400, which is etched to form a fin 260 that is made of semiconductor material. (*Id.*, ¶[0051] (“As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin).”), ¶[0052] (“FIG. 4 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 400 having a semiconductor body or fin 260 (represented by the dashed lines) extending from the substrate 400 through the isolation regions 710, 720.”) As shown in figure 4 below, a gate electrode 340 is on the top and side surfaces of the fin between source and drain regions, where the gate electrode is separated from the fin by a gate dielectric. (*Id.*, ¶[0051] (“The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel resides on the outer sides of the fin beneath the gate dielectric. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric.”).)

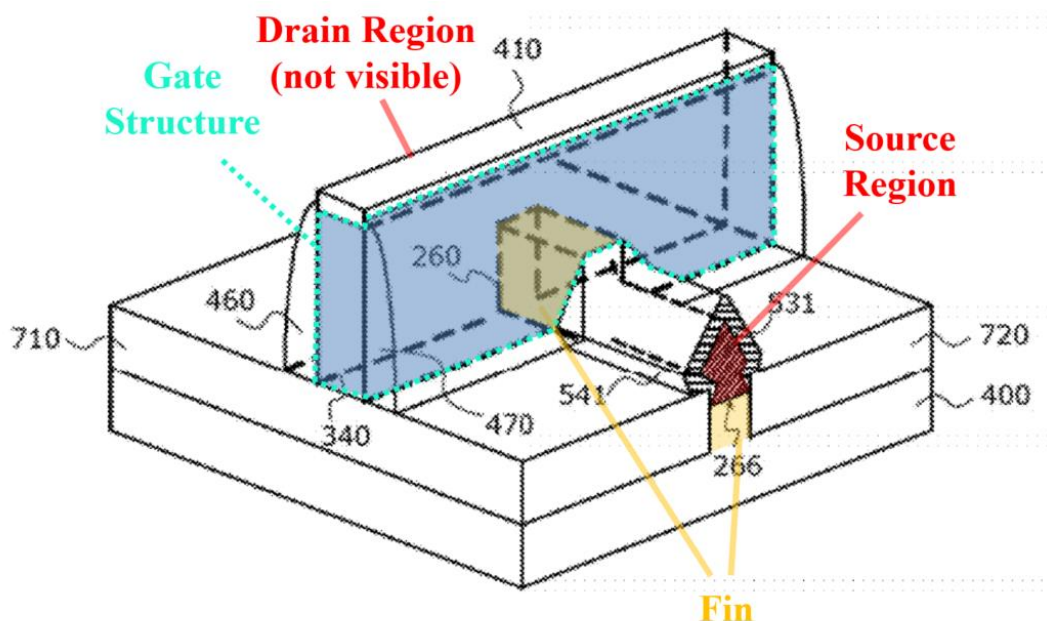


FIG. 4

(*Id.*, FIG. 4 (annotated).)

36. Murthy discloses that the epitaxial regions 531 corresponding to the source/drain regions are on opposite fin sidewalls, where both the source and drain regions are formed on a recessed lower portion of the fin (e.g. recessed source interface 266 shown above). (Ex. 1005, ¶[0051], ¶[0052] (“A source region comprises the epitaxial region 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown).”) Murthy further discloses that the epitaxial regions 531 corresponding to the source/drain regions “can be implemented using an in situ boron doped silicon

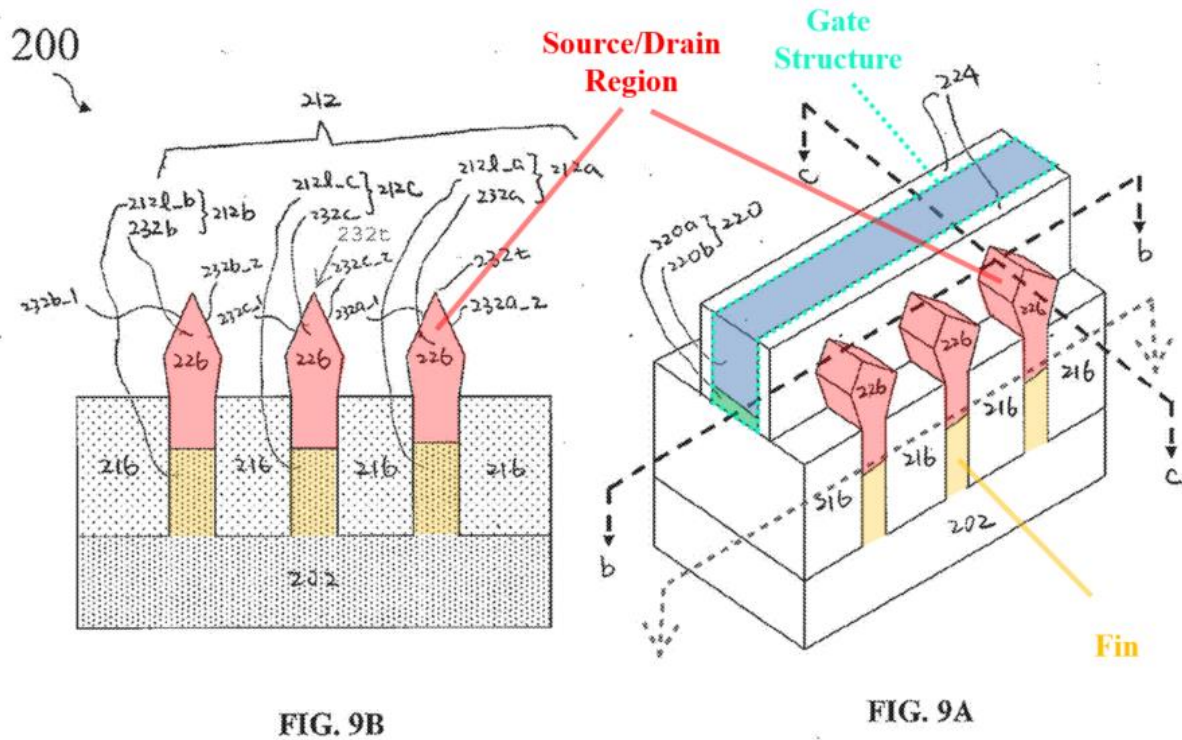
germanium.” (Ex. 1005, ¶[0053].) Murthy further discloses that the source/drain regions are rich in germanium, where the germanium concentration can be at least 50% and up to 100%. (Ex. 1005, Abstract (“Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. In some embodiments, an in situ boron doped germanium, or alternatively, boron doped silicon germanium capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions. In some such cases, germanium concentration can be, for example, in excess of 50 atomic % and up to 100 atomic %.”), ¶[0056] (“the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic %”).)

37. Murthy further discloses forming metal-germanide contacts over the germanium-rich source and drain regions. (Ex. 1005, ¶[0056] (“In another such case, the device may include metal-germanide source and drain contacts.”), ¶[0048] (“Metalization of the source and drain contacts can be carried out using a silicidation process (generally deposition of contact metal and subsequent annealing).”)

B. Wann

38. As shown in annotated figures 9A and 9B below, Wann discloses a FinFET 200 that includes a substrate 202, which is etched to form fins 212. (Ex. 1007, Abstract (“a fin structure extending upward from the substrate major surface,

wherein the fin structure comprises a first fin, a second fin, and a third fin between the first fin and the second fin;”), ¶[0002], ¶[0015] (“Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins (i.e., the fin structure 212).”) As shown in figures 9A and 9B, a gate stack 220 that includes gate dielectric layer 220a (green) and gate electrode layer 220b (blue), is on the top and side surfaces of the fin. (*Id.*, ¶[0020].) Wann discloses strained material 226 that corresponds to the source/drain regions 223 of the FinFET. (*Id.*, ¶[0025] (“Referring to FIGS. 9A and 9B, after the formation of the S/D cavities 228 in the S/D portions 222b, the structure in FIGS. 9A and 9B is produced by epi-growing a strained material 226 in the S/D cavities 228”), ¶[0026] (“In some embodiments, the strained material 226 is hereinafter referred to as S/D regions 232 (comprising 232a, 232b, and 232c).”).)



(*Id.*, FIGs. 9B, 9A (annotated).)

39. While not visible in figure 9A above, each of the source/drain regions 226 has a corresponding source/drain region on the opposite side of the gate structure. (*Id.*, ¶¶[0019]-[0021], FIGs. 6A, 7A; Ex. 1014, FIGs. 7A, 9A.) As shown in figures 9A and 9B above, the strained material of the source/drain regions 226 grown for each of the fins of the FinFET 200 lies on top of a portion the fin and has the channel portion 222a of the upper portion 222 of the fin between them. Wann discloses one embodiment in which the strained material 226 of the source/drain regions is germanium (Ge) and another embodiment where the strained material is

silicon-germanium (SiGe). (*Id.*, ¶[0025] (“In some embodiments, the strained material 226 comprises Ge or SiGe for a p-type FinFET.”).)

40. Wann further discloses forming metal germanide over the strained material 226 corresponding to the source drain regions:

The processing steps up to this point have provided the substrate 202 having the strained material 226 over each lower portion 212l. Conventionally, metal germanide over the strained material 226 may be formed by blanket depositing a thin layer of metal material, such as Ni, Pt, Ti, Co, Pd, and combinations thereof. The substrate 202 is then heated, which causes Ge to react with the metal where contacted. After the reaction, a layer of metal germanide is formed between the Ge-containing material and the metal. The unreacted metal is selectively removed through the use of an etchant that attacks the metal material but does not attack germanide.

(*Id.*, ¶[0030].)

C. Ching

41. Ching, like Murthy and Wann, discloses a fin-based transistor where a channel region separates epitaxially-formed source drain regions:

A transistor, such as a FinFET transistor, comprises a source region, a drain region, and a channel region between the source region and the drain region. The transistor comprises a gate region that controls the channel

region to operate the transistor. The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.

(Ex. 1006, ¶[0001].)

42. Ching further discloses a “nanowire transistor,” where, instead of a fin-shaped channel region, Ching’s nanowire transistor includes multiple wires within the channel region, where gate dielectric and the gate electrode completely surround each nanowire in a “gate-all-around structure.” (Ex. 1006, ¶¶[0024], [0025].)

Ching’s nanowire transistor is shown in annotated figures 5 and 6 below.

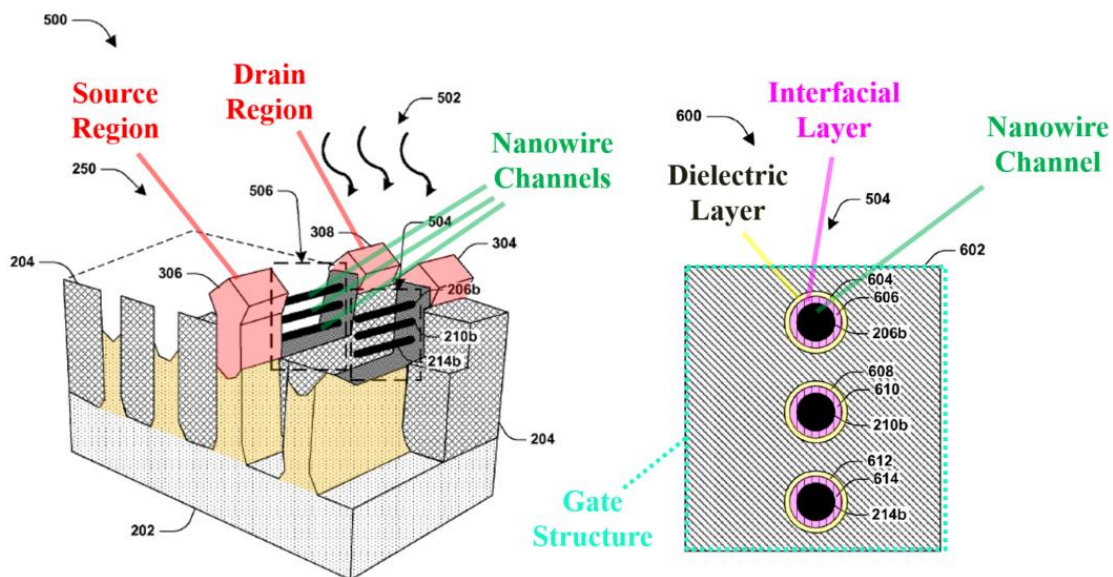


FIG. 5

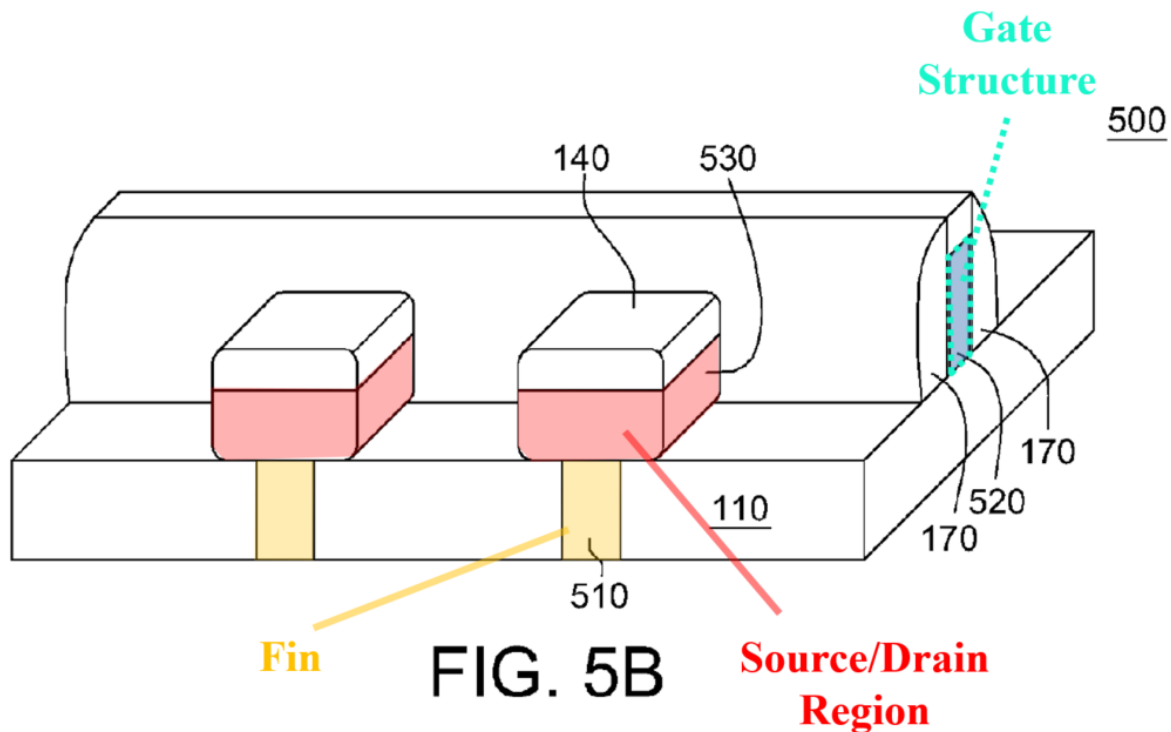
FIG. 6

(*Id.*, FIGs. 5, 6 (annotated).)

43. Ching discloses that having a gate-all-around structure like that shown for the nanowire transistors above increases gate control for the transistors. (*Id.*, ¶[0025] (“In an example, the first gate structure 602 is formed as a gate-all-around structure surrounding the germanium nanowire channels to increase gate control, as illustrated in embodiment 600 of FIG. 6.”); ¶[0001] (“The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.”).)

D. Liao

44. As shown in annotated figure 5B below, Liao discloses a FinFET device 500 with source/drain regions 530 on either side of a gate structure 520. (Ex. 1008, ¶[0050] (“In an embodiment, the semiconductor device 500 is such as a fin field-effect transistor (FINFET). After an ion implantation is performed to the epitaxial structure 530, the regions with the p-type or n-type dopants of the epitaxial structure 530 located on two sides of the gate structure 520 may serve as source/drain regions.”).)



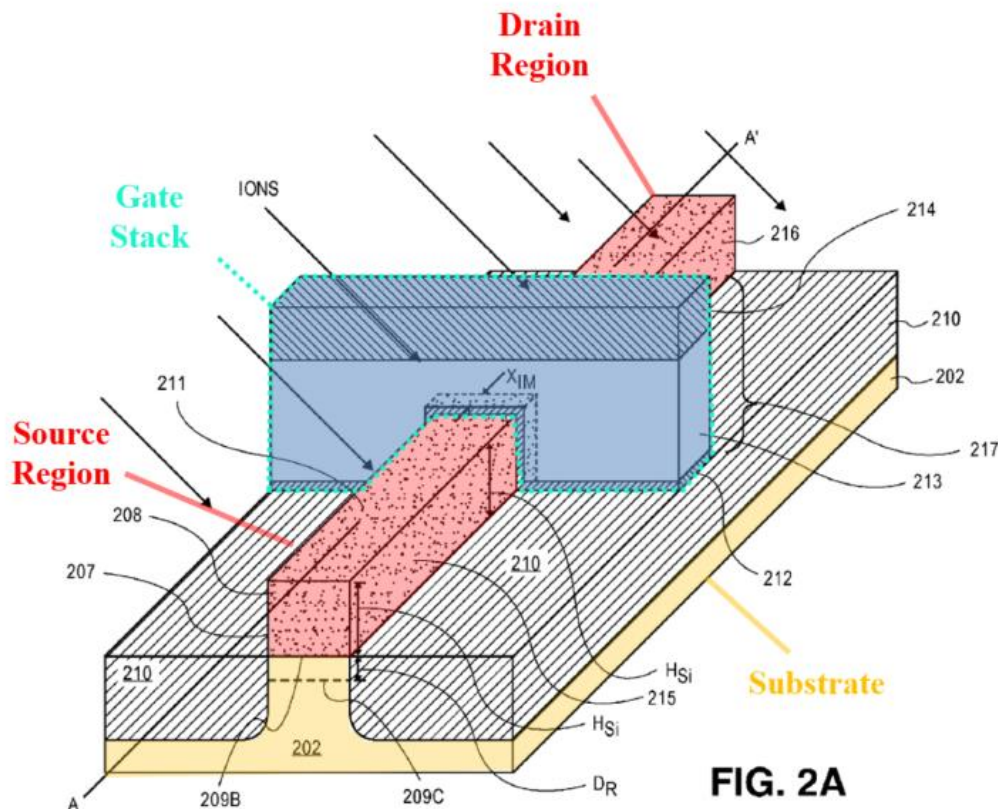
(*Id.*, FIG. 5B (annotated).)

45. Liao discloses that epitaxial structure 530 corresponding to the source/drain regions comprises SiGe, where “the Ge concentration in the epitaxial structure 530 is equal to or higher than 45%, preferably up to 55-60%.” (Ex. 1008, ¶[0047].) Liao also discloses another embodiment where the epitaxial structure is SiGe with a germanium content of at least 45%, where, in the example for that embodiment, the epitaxial structure includes two layers, a first layer that includes “about 55%” germanium concentration and the second layer that includes “about 60%” germanium. (*Id.*, ¶[0042].) According to Liao, “the higher the Ge concentration in the epitaxial structure is, the higher the driving current of the device

will be, and thus the power is higher, such that the overall performance of the device is improved.” (*Id.*, ¶[0018].)

E. Cappellani

46. As shown in annotated figure 2A below, which corresponds to an early stage of fabrication, Cappellani discloses a FinFET device that includes source/drain regions. (Ex. 1009, ¶[0022] (“Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’).”), ¶[0026].)



(*Id.*, FIG. 2A (annotated).)

47. Cappellani discloses doping the source/drain regions of the fin portion of the silicon substrate in order to allow for very accurate etching of the doped regions to form cavities for subsequent formation of regrown source/drain regions. (*Id.*, ¶¶[0027], [0030]-[0031], [0033]-[0035], FIGs. 2A-B, 4A-C.) Cappellani further discloses that after selectively etching to form the cavities for the source/drain regions, epitaxial deposition is used to form the source/drain regions. (*Id.*, ¶[0041].)

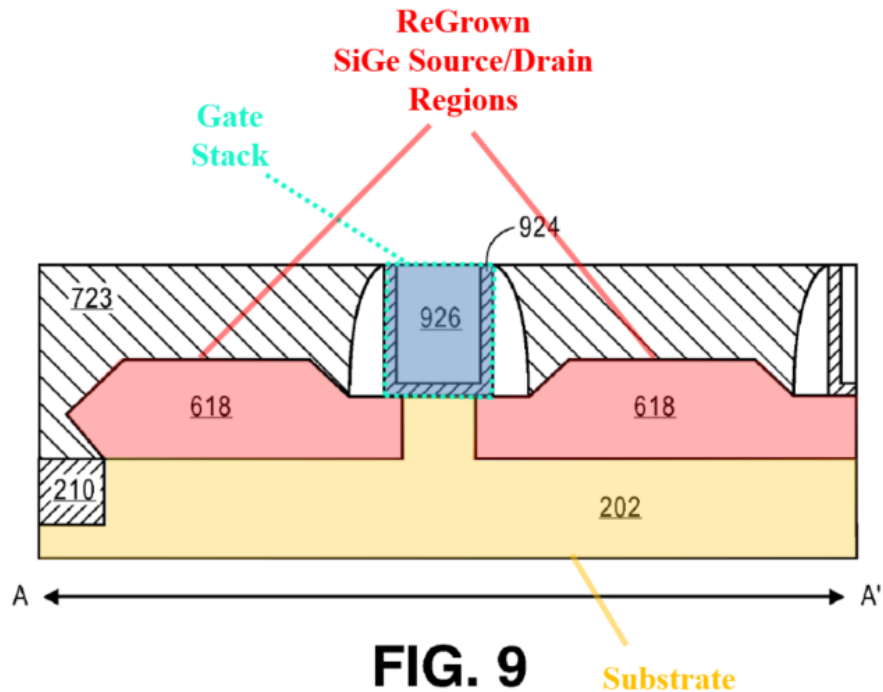
48. Cappellani discloses that stress on the channel region in FinFET “increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current” (*id.*, ¶[0042]), where the strain can be imparted on the channel by using a silicon germanium alloy as the material for the regrown source/drain regions:

In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel)

(*Id.*, ¶[0043].)

49. Cappellani further discloses that the germanium concentration in the silicon germanium alloy used for the source/drain regions can “range from 10 atomic

% to 80 atomic %.” (*Id.*, ¶[0045].) Annotated figure 9 below shows the regrown SiGe source/drain regions in Cappellani’s FinFET. (*Id.*, ¶[0048].)



(*Id.*, FIG. 9 (annotated).)

IX. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS

A. Murthy Discloses the Features of Claims 1, 2, 5-8, 10, 12-14, and 16

50. In my opinion, Murthy discloses all of the features of claims 1, 2, 5-8, 10, 12-14, and 16 of the '334 patent.

1. Claim 1

a) “An integrated circuit, comprising:”

51. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 1 of the ’334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Murthy discloses the limitations therein. For example, Murthy is entitled “Transistors with High Concentration of Boron Doped Germanium” (Ex. 1005, Title) and discloses transistors that are included on a semiconductor substrate with other devices, where the semiconductor substrate that includes those devices is “an integrated circuit”:

Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) channel regions and to increase movement of positive charged holes in P-type MOS device (PMOS) channel regions.

(*Id.*, ¶[0001]; *see also id.*, [0045] (“The ILD layer may be formed using materials known for the applicability in dielectric layers for **integrated circuit structures.**”)) (emphasis added).)

52. Murthy further discloses a FinFET transistor that can be included on the semiconductor device (“integrated circuit”). (Ex. 1005, ¶[0009] (“FIG. 4 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.”), ¶[0013] (“The techniques can be embodied, for instance, in planar or non-planar FinFET transistor devices.”), ¶¶[0050]-[0053], ¶[0056] (“One example embodiment of the present invention provides a transistor device”) (“In one such case, the device is one of a planar or FinFET PMOS transistor.”), claim 1 (“A transistor device, comprising:”), claim 2 (“The device of claim 1, wherein the device is one of a planar or FinFET PMOS transistor”).)

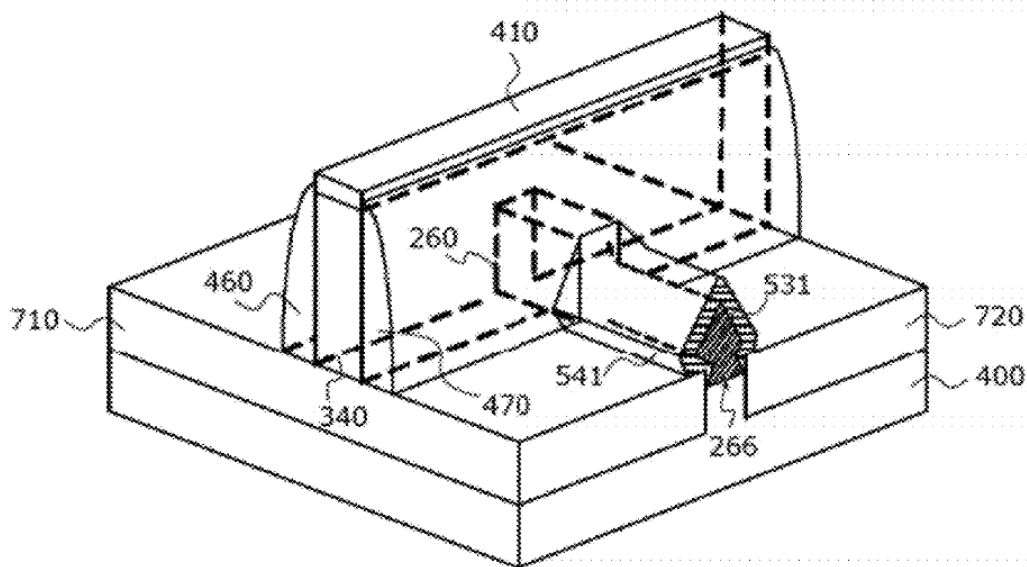


FIG. 4

(*Id.*, FIG. 4.)

- b) “a non-planar body comprising semiconductor material, wherein the non-planar body has top and side surfaces;”**

53. In my opinion, Murthy discloses this claim feature. As shown in annotated figure 4 below, Murthy’s FinFET includes a substrate 400, which is etched to form a fin 260 that is made of semiconductor material and constitutes a “non-planar body.” (Ex. 1005, ¶[0051] (“As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin).”), ¶[0052] (“FIG. 4 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-

gate device includes a substrate 400 having a semiconductor body or fin 260 (represented by the dashed lines) extending from the substrate 400 through the isolation regions 710, 720.”), (“In one embodiment, the isolation regions 710, 720 are shallow trench isolation (STI) regions formed by common techniques, such as etching the substrate 200 to form trenches, and then depositing oxide material onto the trenches to form the STI regions.”), ¶[0056] (“One example embodiment of the present invention provides a transistor device”) (“In one such case, the device is one of a planar or FinFET PMOS transistor.”), claim 1 (“a substrate having a channel region”), claim 2 (“The device of claim 1, wherein the device is one of a planar or FinFET PMOS transistor”).) As shown, the fin includes a channel portion corresponding to the channel of the transistor and a lower portion that lies under the source/drain regions. Moreover, the fin 260 corresponding to a “non-planar body” is consistent with claim 10 of the ’334 patent, which recites “the non-planar body is a fin.” (Ex. 1001, claim 10; see my discussion below in section IX.A.7.)

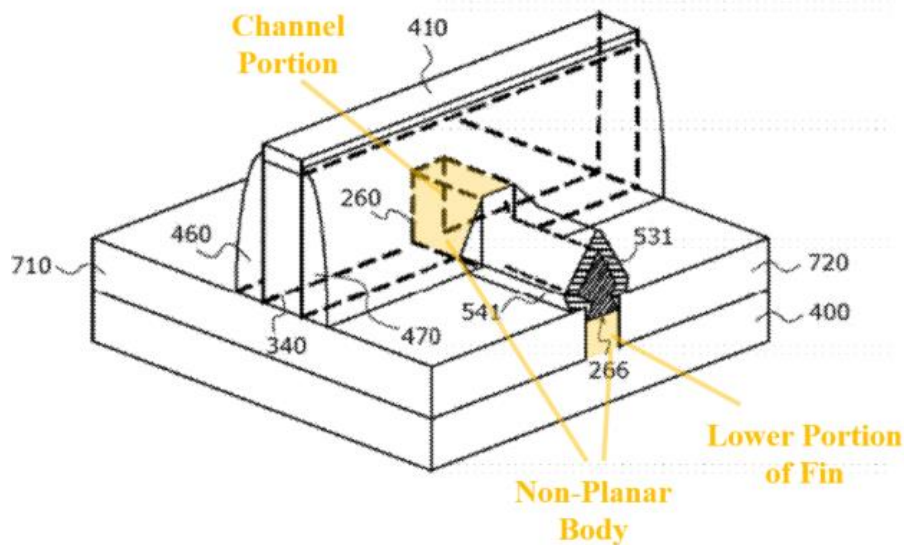


FIG. 4

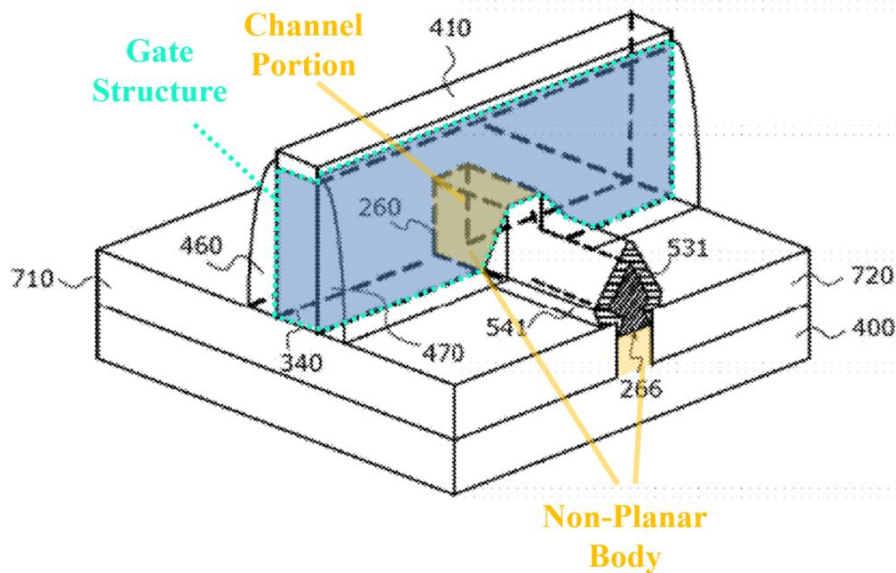
(Ex. 1005, FIG. 4 (annotated).)

54. Murthy discloses that the fin includes a top surface and side surfaces. (*Id.*, ¶[0051] (“The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET.”), ¶[0052] (“A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates.”), ¶[0056] (“The device includes a substrate having a channel region.”) (“In one such case, the device is one of a planar or FinFET PMOS transistor.”), FIG. 4.)

c) “a gate structure on at least the top and side surfaces of the non-planar body;”

55. In my opinion, Murthy discloses this limitation. For example, as shown in annotated figure 4 below, Murthy discloses a gate electrode 340 on the top and side surfaces of the channel portion of the fin (“non-planar body”), where the gate electrode is separated from the fin by a gate dielectric. (Ex. 1005, ¶[0051] (“The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel resides on the outer sides of the fin beneath the gate dielectric. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET.”), ¶[0052] (“A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates.”), ¶[0056] (“The device further includes a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region”), FIG. 4, claim 1 (“a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region”), claim 2 (“The device of claim

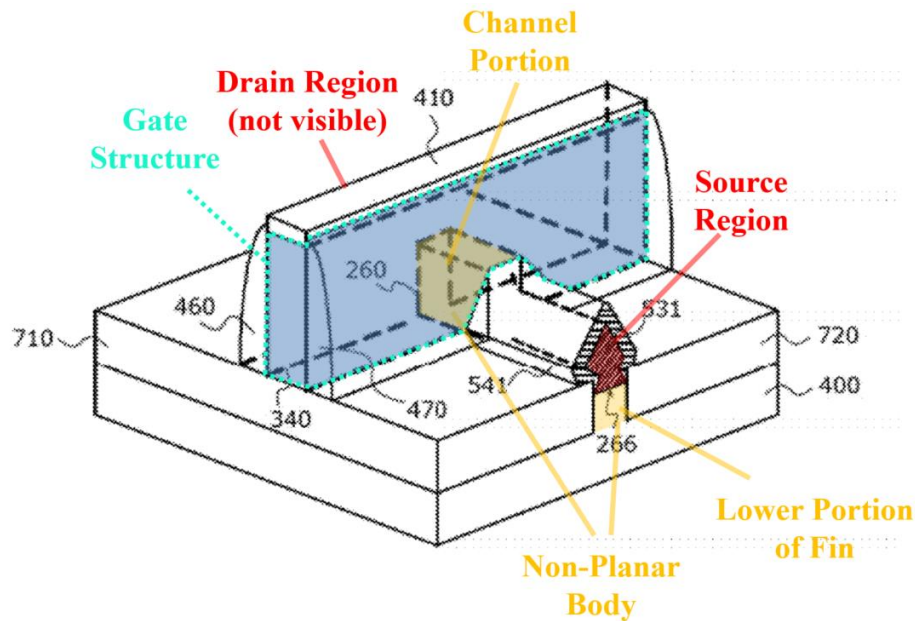
1, wherein the device is one of a planar or FinFET PMOS transistor”).) The gate electrode 340 and underlying gate dielectric together constitute a “gate structure.”



(*Id.*, FIG. 4 (annotated).)

- d) “a source region adjacent the non-planar body, the source region including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon; and”
- e) “a drain region adjacent the non-planar body, the drain region including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with a surface that consists essentially of silicon.”

56. In my opinion, Murthy discloses these features. For example, Murthy discloses a source region on one fin sidewall and a drain region on the opposite fin sidewall, where the source/drain regions include epitaxial regions 531 (“first/second portions”). (Ex. 1005, ¶[0051] (“The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, **a source region, and a drain region.**”), ¶[0052] (“A source region comprises the epitaxial regions 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown).”), ¶[0056] (“The device further includes source and drain regions formed in the substrate and adjacent to the channel region.”) (“In one such case, the device is one of a planar or FinFET PMOS transistor.”), FIG. 4, claim 1 (“source and drain regions formed in the substrate and adjacent to the channel region”), claim 2 (“The device of claim 1, wherein the device is one of a planar or FinFET PMOS transistor”).)



(*Id.*, FIG. 4 (annotated).)

57. The epitaxial regions 531 (“first/second portions”) of the source/drain regions are “adjacent to the non-planar body” as they lie on top of the lower portion of the fin (“non-planar body”) and also have the channel portion of the fin between them. (*Id.*, ¶[0052] (“A source region comprises the epitaxial regions 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown).”), ¶[0056], claim 1 (“source and drain regions formed in the substrate and adjacent to the channel region”).) Murthy discloses that that substrate 400, and hence the fin formed by etching the substrate, can be silicon or silicon-on-insulator (SOI), so each of the epitaxial regions (“first/second portions”) is in direct contact with the side surface of the channel

portion and the top surface of the lower portion of the fin (“a surface that consists essentially of silicon”), as recited in claim 1. (*Id.*, ¶[0019] (“For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate...”), ¶[0052] (“The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).”).)

58. Murthy further discloses that the epitaxial regions 531 (“first/second portions”) corresponding to the source/drain regions “can be implemented using an in situ boron doped silicon germanium.” (*Id.*, ¶[0053]; *see also id.*, ¶[0056].) Murthy further discloses that the germanium concentration in the epitaxial portions can be implemented with germanium or silicon germanium with nearly 100% germanium such that those portions include at least 50% germanium as recited in claim 1. (*Id.*, Abstract (“Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. In some embodiments, an **in situ boron doped germanium**, or alternatively, boron doped silicon germanium capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions. In some such cases, **germanium concentration can be**, for example, in excess of 50 atomic % and **up to 100 atomic %** The techniques can be embodied, for instance, in planar or non-planar

transistor devices.”), claim 1 (“wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic %”), claim 2 (“the device is one of a planar or FinFET PMOS transistor”), ¶[0013] (“In some embodiments, this is accomplished by use of an in situ **boron doped germanium provided by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions**. In other embodiments, selective epitaxial deposition is used to form a bilayer construction of boron doped silicon germanium capped with a heavily boron doped germanium layer in the source/drain and respective tip regions. In such cases, the germanium concentration can be, for example, in the range of 20 atomic % to 100 atomic %, and the boron concentration can be, for instance, in the range of $1 \text{ E}20 \text{ cm}^{-3}$ to $2\text{E}21 \text{ cm}^{-3}$ (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of $2\text{E}20 \text{ cm}^{-3}$).”), ¶[0018], ¶[0020] (“the boron doped germanium layer can be configured with **a germanium concentration graded** from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to **70 atomic %) up to 100 atomic %**.”), ¶[0042] (“As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g. in excess of 50 atomic % and up to pure germanium) In some example embodiments, a **germanium concentration of 95 atomic % and up to pure germanium (100 atomic %)** can be used to achieve such benefits.”), ¶[0056] (“the

source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic %”), ¶[0059] (“Moreover, some embodiments may include source and drain regions fabricated as described herein (e.g. having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{cm}^{-3}$), but still use conventional processing (e.g., implantation and annealing) to form the tips of the source and drain regions.”); see also *id.*, ¶¶[0041], [0048].) Therefore, Murthy discloses that the source region includes a “first portion” and the drain region includes a “second portion” that includes “germanium at a concentration of at least 50 atomic percent throughout the [first/second] portion” as recited in claim 1.

2. Claim 2

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

59. In my opinion, Murthy discloses this limitation. As I discuss above for claim elements 1[d]-[e], the epitaxial regions (“first/second portions”) of the source/drain regions are in direct contact with the channel portion of the fin and the underlying lower portion of the fin, both of which are formed from the substrate 400. (See my discussion above in sections IX.A.1(d)-(e).) Murthy discloses that the substrate can be a silicon or silicon-on-insulator (SOI) substrate. (Ex. 1005, ¶[0019] (“For instance, the substrate 102 can be a silicon substrate, or a silicon film of a

silicon on insulator (SOI) substrate, or a multi-layered substrate....”), ¶[0052] (“The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).”), ¶[0028] (“The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration.”).) Therefore, the “surface,” which corresponds to either the side surface of the channel portion of the fin or the upper surface of the lower portion of the fin is a surface of “a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate” as claimed. Such an understanding is consistent with the disclosure of the ’334 patent. (Ex. 1001, 5:35-40 (“As can be seen in FIGS. 1 and 1’, the example methods include performing 102 shallow trench isolation (STI) on a semiconductor substrate. The substrate may be formed using a silicon base or substrate, such as silicon single crystal wafer. Substrate may be implemented, for example, with a bulk silicon, a silicon-on-insulator configuration (SOI)”); *see also* Ex. 1015, 103, 115; Ex. 1017, 93-97.)

3. Claim 5

“The integrated circuit of claim 1, wherein the first and second portions further include one or both of silicon and tin.”

60. In my opinion, Murthy discloses this limitation. Murthy discloses that, for embodiments that do not use pure germanium for the epitaxial regions (“first and

second portions”), the epitaxial regions also include silicon. For example, Murthy discloses that the epitaxial regions can be silicon-germanium with nearly 100% germanium, where a small percentage of silicon would be included in the silicon-germanium epitaxial regions. (Ex. 1005, Abstract (“In some embodiments, an in situ boron doped germanium, or alternatively, **boron doped silicon germanium** capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions. In some such cases, **germanium concentration can be**, for example, in excess of 50 atomic % and **up to 100 atomic %** The techniques can be embodied, for instance, in planar or non-planar transistor devices.”), ¶[0056] (“the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$.”), ¶[0053] (“boron doped SiGe deposited for epitaxial region 531”), ¶[0058].)

61. Therefore, the high-germanium content silicon-germanium epitaxial portions (“first and second portions”) of the source/drain regions include silicon (“one or both of silicon and tin”) as recited in claim 5.

4. Claim 6

“The integrated circuit of claim 1, wherein the first and second portions include a p-type dopant.”

62. In my opinion, Murthy discloses this limitation. Murthy discloses that that the epitaxial portions (“first and second portions”) of the source/drain regions

are doped with boron. (Ex. 1005, ¶[0056] (“the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{cm}^{-3}$.”) For example, Murthy discloses that the source/drain regions that include epitaxial region 531 “can be implemented using an in situ **boron doped** silicon germanium ... germanium and/or boron concentration grading can be implemented directly in the epitaxial region.” (*Id.*, ¶[0053] (emphasis added); *see also id.*, Abstract (“Techniques are disclosed for forming transistor devices having source and drain regions with **high concentrations of boron doped germanium**. In some embodiments, an **in situ boron doped germanium**, or alternatively, **boron doped silicon germanium** capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions.”) (emphasis added), claim 1 (“wherein the **source and drain regions comprise a boron doped germanium layer** having a germanium concentration in excess of 50 atomic %”) (emphasis added), claim 2 (“the device is one of a planar or FinFET PMOS transistor”), ¶[0013] (“In some embodiments, this is accomplished by use of an in situ **boron doped germanium provided by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions**. In other embodiments, selective epitaxial deposition is used to form a **bilayer construction of boron doped silicon germanium capped with a heavily**

boron doped germanium layer in the source/drain and respective tip regions.

In such cases, the germanium concentration can be, for example, in the range of 20 atomic % to 100 atomic %, **and the boron concentration can be, for instance, in the range of $1 \times 10^{20} \text{ cm}^{-3}$ to $2 \times 10^{21} \text{ cm}^{-3}$ (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of $2 \times 10^{20} \text{ cm}^{-3}$).**) (emphasis added), ¶[0020] (“the **boron doped germanium layer** can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %.”) (emphasis added), ¶[0042] (“As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g. in excess of 50 atomic % and up to pure germanium) and high boron concentration...”), ¶[0059] (“Moreover, some embodiments may include source and drain regions fabricated as described herein (e.g. having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of $1 \times 10^{20} \text{ cm}^{-3}$), but still use conventional processing (e.g., implantation and annealing) to form the tips of the source and drain regions.”); *see also id.*, ¶¶[0041], [0048].)

63. Boron is a well-known and often-used p-type dopant. (Ex. 1007, ¶[0011]; Ex. 1011, ¶[0014]; Ex. 1001, 2:60-64 (“Note that the Ge-rich layer as variously described herein is to be used for p-MOS source/drain contacts and is

therefore a p-type layer, meaning it has p-type doping (e.g., using boron (B), gallium (Ga), and/or any other suitable dopant).”).)

5. Claim 7

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is undoped.”

64. In my opinion, Murthy discloses this limitation. As I discuss above for claim elements 1[d]-[e] and claim 2, the “surface that consists essentially of silicon” is part of the silicon substrate, which can be bulk silicon or a silicon on insulator substrate. (See my discussion above in sections IX.A.1(d)-(e), IX.A.2; Ex. 1005, ¶[0019] (“For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate...”), ¶[0052] (“The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).”), ¶[0028] (“The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration.”).) A person of ordinary skill in the art would have understood that, absent any indication that the substrate is doped, bulk silicon material is “undoped.” (*Id.*, ¶[0043] (“On one side of the interface is the heavily boron doped germanium layer (layer 318/320 of FIG 3F or cap 317/319 of FIG. 3G) and on the other side of the interface is the substrate 300 material that makes up the channel region.”); *see also* Ex. 1015, 103, 115; Ex. 1017, 93-97.)

6. Claim 8

“The integrated circuit of claim 1, further comprising an additional portion on the first and second portions, the additional portions including a metal and germanium.”

65. In my opinion, Murthy discloses this limitation. For example, Murthy discloses forming metal-germanide contacts (“additional portions including a metal and germanium”) on the epitaxial regions (“first and second portions”) of the source and drain regions. (Ex. 1005, ¶[0048], ¶[0056] (“In another such case, the device may include metal-germanide source and drain contacts.”), claim 3 (“metal-germanide source and drain contacts”).)

66. Murthy further discloses how to form such metal-germanide contacts on the source/drain regions, where metal is deposited on the germanium or silicon-germanium with nearly 100% germanium (e.g., 95%+) epitaxial regions epitaxial regions, and then annealing is performed to form a germanide:

Metalization of the source and drain contacts can be carried out using a silicidation process (generally deposition of contact metal and subsequent annealing). For instance silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The boron doped germanium epi layer allows for metal-germanide formation (e.g., nickel-

germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including Rext) over that in conventional metal-silicide systems.

(Ex. 1005, ¶[0048].)

67. Murthy's formation of metal-germanide contacts is consistent with the disclosure of the '334 patent. (Ex. 1001, 10:34-61.) Therefore, Murthy discloses source/drain contacts of metal-germanide that are on the source/drain regions ("additional portions on the first and second portions"). The source/drain contacts ("additional portions") include a metal and germanium as recited in claim 8.

7. Claim 10

"The integrated circuit of claim 1, wherein the non-planar body is a fin, the fin between portions of the gate structure."

68. In my opinion, Murthy discloses this limitation. As I discuss above with respect to claim 1, the fin 260 that extends upward from the planar surface of the substrate 400 constitutes the claimed "non-planar body." (See my discussion above in section IX.A.1(b).) Murthy discloses that the "gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates." (Ex. 1005, ¶[0052].) Therefore, the gate structure, which includes the gate electrode and the gate dielectric, has portions on three sides of the fin such that the fin is "between portions of the gate structure." (See my discussion above in section IX.A.1(c).)

8. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

69. In my opinion, Murthy discloses this limitation. As discussed above for claim element 1[a], Murthy discloses transistors that are included on a semiconductor substrate with other devices, where the semiconductor substrate that includes those devices is “an integrated circuit”:

Increased performance of **circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate** is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) channel regions and to increase movement of positive charged holes in P-type MOS device (PMOS) channel regions.

(Ex. 1005, ¶[0001] (emphasis added).)

70. A circuit device that includes that includes Murthy’s FinFET transistor is a “computing system” in a manner consistent with the ’334 patent, as such a circuit

device is an electronic device that includes an interconnected set of components and “employs one or more transistor devices” that includes the features of claim 1:

In various implementations, the **computing system 1000** may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, **the system 1000 may be any other electronic device that processes data or employs one or more transistor devices as variously described herein.**

(Ex. 1001, 14:14-23 (emphasis added).)

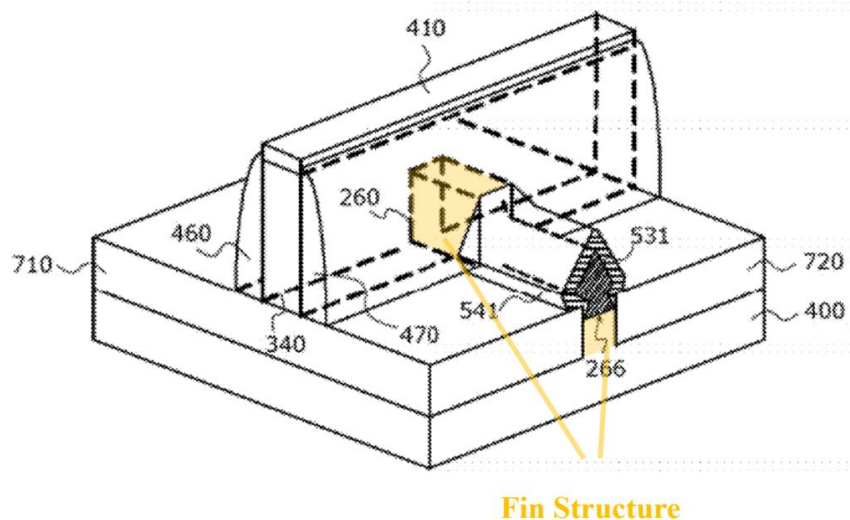
9. Claim 13

a) “An integrated circuit, comprising:”

71. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 13 of the ’334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Murthy discloses “an integrated circuit” for the same reasons I discuss above for claim element 1[a]. (See my discussion above in section IX.A.1(a).)

b) “a fin structure comprising semiconductor material, wherein the fin structure has top and side surfaces;”

72. In my opinion, Murthy this claim limitation. As I discuss above for claim element 1[b] and as is shown in annotated figure 4 below, Murthy's FinFET includes a substrate 400 that is etched to form a non-planar body that includes a fin 260 ("fin structure"). (See my discussion above in section IX.A.1(b).) For the same reasons I discuss above for the "non-planar body" recited in claim 1, Murthy's fin 260 discloses a "fin structure" as recited in claim 13, where the "fin structure" has top and side surfaces. (See my discussion above in section IX.A.1(b).)



(Ex. 1005, FIG. 4 (annotated).)

c) **"a gate structure on the top and side surfaces of the fin structure;"**

73. In my opinion, Murthy discloses this limitation for the same reasons I discuss above for claim element 1[c]. (See my discussion above in section

IX.A.1(c).) The gate structure, which includes the gate electrode 340 and gate dielectric between the gate electrode and the fin, covers the top and side surfaces of the channel portion of the “fin structure.” (*Id.*)

- d) **“a source structure to one side of the gate structure and abutting the fin structure, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”**
- e) **a drain structure to an opposite side of the gate structure and abutting the fin structure, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;”**

74. In my opinion, Murthy discloses these features. As I discuss above for claim elements 1[d] and 1[e], Murthy discloses a source region (“source structure”) on one fin sidewall (“to one side of the gate structure”) and a drain region (“drain structure”) on the opposite fin sidewall (“to an opposite side of the gate structure”). (See my discussion above in sections IX.A.1(d)-(e).) Because the source and drain regions are on the sidewalls of the fin structure and also on top of a lower portion 266 of the fin, the source and drain regions (“source structure” and “drain structure”) abut the “fin structure.” (See my discussion above in sections IX.A.1(d)-(e), IX.A.9(b).) As I also discuss above for claim elements 1[d] and 1[e], Murthy

discloses forming epitaxial regions (“first/second portions”) of the source/drain regions (“source/drain structures”) that include “at least 50 atomic percent” germanium throughout, where the epitaxial regions (“first/second portions”) are in direct contact with the underlying lower portion of the fin and the channel region, both of which “consist essentially of silicon.” (See my discussion above in sections IX.A.1(d)-(e), IX.A.9(b).)

- f) **“a first contact structure on the first portion of the source structure and including a metal-germanide; and;”**
- g) **“a second contact structure on the second portion of the drain structure and including a metal-germanide.”**

75. In my opinion, Murthy discloses these features. For example, as I discuss above for claim 8, Murthy discloses forming metal germanide source/drain contacts (“first contact structure” and “second contact structure”) on the epitaxial regions (“first portion of the source structure” and “second portion of the drain structure”). (See my discussion above in section IX.A.6.)

10. Claim 14

“The integrated circuit of claim 13, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

76. In my opinion, Murthy discloses this limitation for the same reasons I discuss above for claim 2. (See my discussion above in section IX.A.2.)

11. Claim 16

“The integrated circuit of claim 13, wherein the first and second portions further include one or both of silicon and tin, and further include a p-type dopant.”

77. In my opinion, Murthy discloses these features for the same reasons I discuss above for claims 5 and 6. (See my discussion above in sections IX.A.3-4.)

B. Murthy in Combination with Kuhn Discloses or Suggests the Features of Claim 12

1. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

78. As I discuss above in section IX.A.8, Murthy discloses a circuit device that includes that includes Murthy’s non-planar transistor, which constitutes a “computing system” in a manner consistent with the ’334 patent. (See my discussion above in section IX.A.8.) I have been asked to assume a scenario in which Murthy does not disclose a “computing system” as recited in claim 12. Under such an assumption, Kuhn discloses using non-planar transistors on integrated circuits in a computing system, and, in my opinion, a person of ordinary skill in the art would have had good reason to use Murthy’s transistor in a computing device as disclosed by Kuhn.

79. Kuhn is in the same field as Murthy. For example, like Murthy, Kuhn discloses non-planar transistors that include silicon-germanium source/drain

regions. (Ex. 1010, ¶¶[0011]-[0015].) Thus, a person of ordinary skill in the art implementing a transistor like that disclosed by Murthy would have reason to look to Kuhn. For example, Kuhn discloses “[i]n an embodiment, the fin structures 107 may comprise a dual channel portion of a gate all around (GAA) nanowire device.” (*Id.*, ¶[0013].) Like Murthy, Kuhn discloses “silicon germanium source drain structures 110 may be grown utilizing epitaxial growth techniques in the source/drain regions 109.” (*Id.*, ¶[0015].)

80. Kuhn discloses that the non-planar transistors can be used in integrated circuits included in computing systems. (Ex. 1010, ¶[0038] (“FIG. 6 shows a computer system according to an embodiment.”), ¶[0039] (“One or more of the components shown in system 600 may include one or more nanowire devices of the various embodiments included herein.”), ¶¶[0040]-[0041], FIG. 6.)

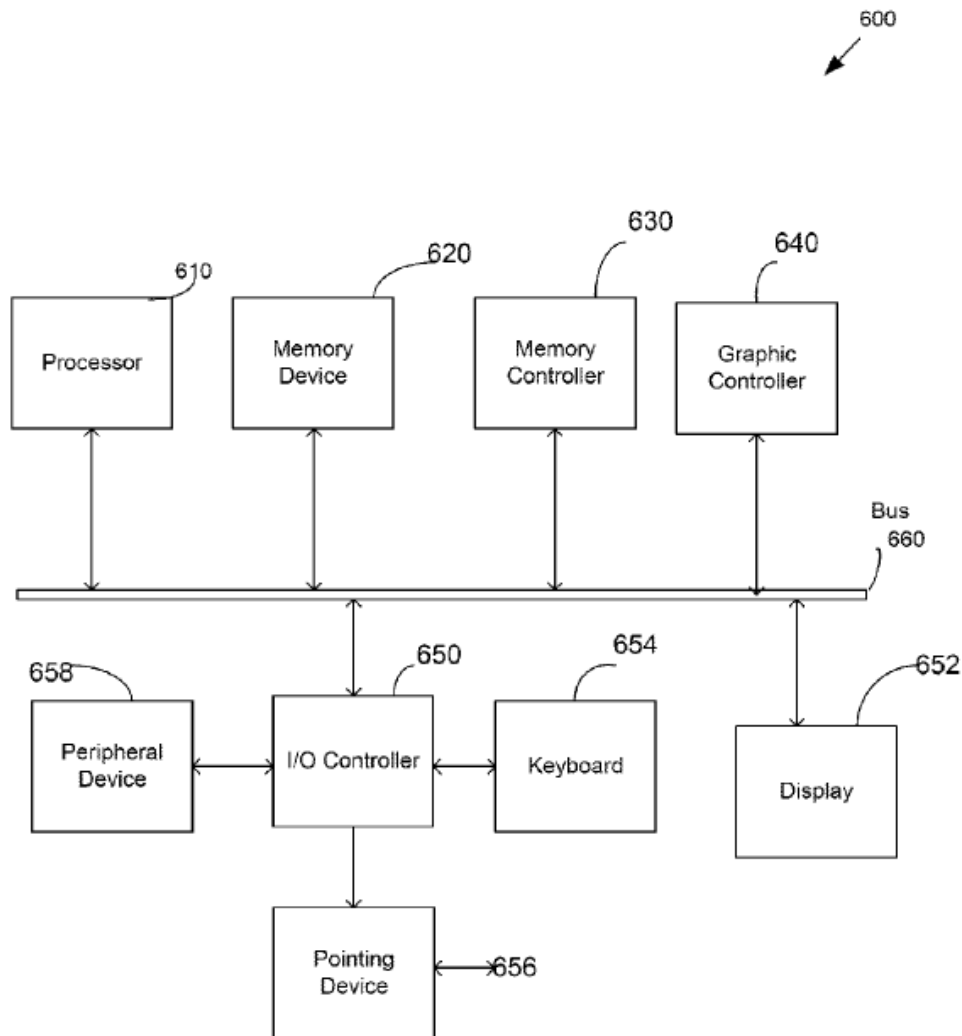


FIG. 6

(*Id.*, FIG. 6.)

81. In view of Kuhn and their knowledge of the state of the art, a person of ordinary skill in the art would have found it good reason to implement a non-planar transistor like that disclosed by Murthy in a computing device. Indeed, a person of

ordinary skill in the art would have known that transistors are often used in integrated circuit devices that are included in computing devices. Such a skilled person would have been motivated to include Murthy's transistor in a computing system in order to provide utility to the transistor, and, based on Kuhn's disclosure and their knowledge, would have had a reasonable expectation of success.

C. Murthy in Combination with Ching Discloses or Suggests the Features of Claims 11, 17, 18, and 20

1. Claim 11

“The integrated circuit of claim 1, wherein the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons.”

82. In my opinion, Murthy in combination with Ching discloses or suggests these features. As I discuss above in section IX.A.1, Murthy discloses a FinFET that includes a “non-planar body” in the form of a fin extending from the substrate surface. (See my discussion above in section IX.A.1(b).) Murthy does not explicitly disclose nanowires or nanoribbons, but Ching discloses a fin-based non-planar structure similar to that of Murthy that uses nanowires, and, in view of Ching and their knowledge of the state of the art, a person of ordinary skill in the art would have good reason to implement a non-planar transistor like that disclosed by Murthy using nanowires.

83. Ching, like Murthy, discloses a fin-based transistor where a channel region separates source and drain regions that include epitaxially-formed material:

A transistor, such as a FinFET transistor, comprises a source region, a drain region, and a channel region between the source region and the drain region. The transistor comprises a gate region that controls the channel region to operate the transistor. The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.

(Ex. 1006, ¶[0001].)

Source and drain material is formed within the first source region 302 and the first drain region 304, such as through an epitaxial growth technique, to create a first source and a first drain for a first nanowire transistor. Other source regions, such as a second source region 306, and drain regions, such as a second drain region 308, are formed for other nanowire transistors that are to be formed for the semiconductor arrangement 250.

(*Id.*, ¶[0021]; *see also id.*, ¶[0019] (“In an example, the substrate 202 comprises silicon, and the substrate 202 is formed according to a FinFET arrangement

comprising one or more silicon fins separated by isolation structures 204, such as shallow trench isolation (STI).”)

84. Instead of a fin-shaped channel region that has a gate structure on the top and sides of the channel, Ching’s nanowire transistor includes multiple wires within the channel region, where gate dielectric and the gate electrode completely surround each nanowire in a “gate-all-around structure.” (*Id.*, ¶¶[0024], [0025]; see also Ex. 1011,¹ ¶[0044] (“A non-planar architecture can be implemented, for instance, using FinFETs or nanowire configurations. A FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). ... Other types of FinFET configurations are also available ... A nanowire transistor (sometimes referred to as gate-all-around FET) is configured very similarly, but instead of a fin, a nanowire (e.g., silicon or SiGe or Ge nanowire) is used and the gate material generally surrounds the channel region on all sides.”); section V.C above.) Ching’s device 500 with epitaxially-grown material in a source region and a drain region on either side of a channel region that includes nanowire channels 206, 210, and 214 for a nanowire transistor is shown in annotated figures 5 and 6 below. (Ex. 1006, ¶¶[0021]-[0023], [0030]-[0032].)

¹ I cite to Glass (Ex. 1011) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

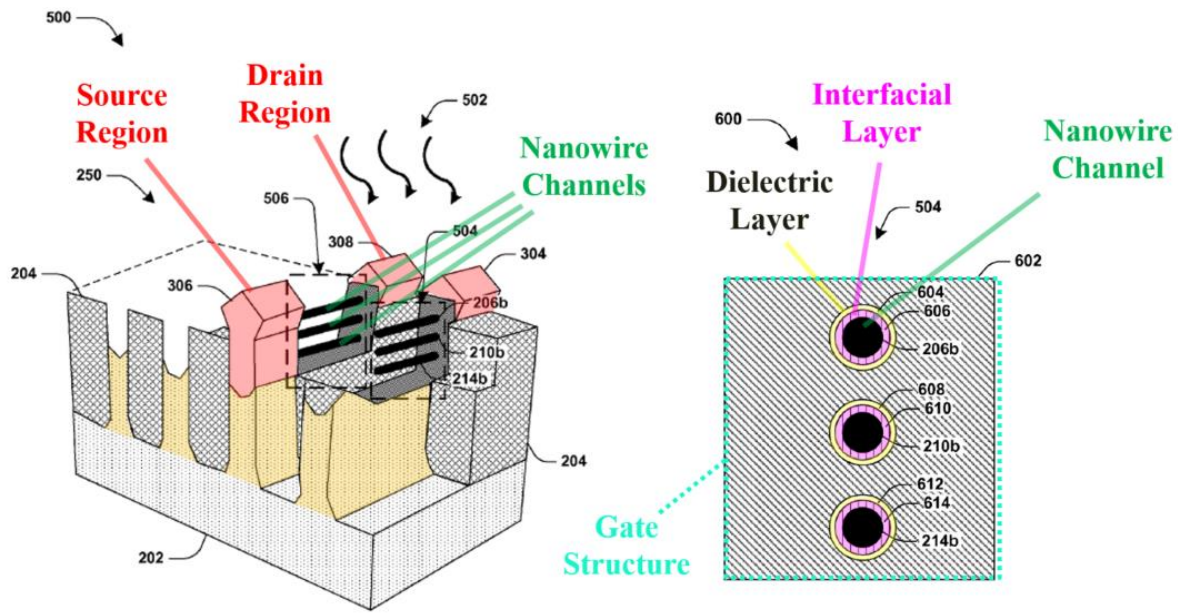


FIG. 5

FIG. 6

(*Id.*, FIGs. 5, 6 (annotated).)

85. Ching discloses that having a gate-all-around structure like that shown for the nanowire transistors above increases gate control for the transistors. (*Id.*, ¶[0025] (“In an example, the first gate structure 602 is formed as a gate-all-around structure surrounding the germanium nanowire channels to increase gate control, as illustrated in embodiment 600 of FIG. 6.”), ¶[0001] (“The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.”); *see also* Ex. 1011, ¶[0044]

(“Depending on the particular design, nanowire transistors have, for instance, four effective gates.”).)

86. In my opinion, a person of ordinary skill in the art implementing a FinFET device like that disclosed by Murthy would have looked to Ching, particularly because Murthy and Ching are references in the same field and disclose fin-based devices with epitaxially grown source/drain regions on either side of a channel region. Having looked to Ching, such a skilled person would have had good reason to implement the channel region of a fin-based device like that of Murthy such that it includes one or more nanowires like those disclosed by Ching.

87. As disclosed by Ching and known in the art, including nanowires in the channel region provides added gate control, where the gate-all-around aspect of nanowires provides even more control than the three-sided gate structure for FinFETs like those disclosed by Murthy. (Ex. 1006, ¶¶[0001], [0025]; Ex. 1010,² ¶[0001] (“Nanowires used to fabricate devices provide improved short channel control.”), ¶[0024] (“Nanowire channel devices exhibit lower sub-threshold leakage due to short channel effect (SCE) reduction.”), (“Implementation of [gate-all-around] GAA SiGe high mobility channel device...suppress[es] SCE effects” and

² I cite to Kuhn (Ex. 1010) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

“maximize[s] the electrostatic gate control to the channel”).) Moreover, nanowire-based transistors would also have allowed for reduced semiconductor chip size by stacking the transistor channels vertically. (Ex. 1010, ¶[0010] (“enable[ing] enhanced isolation of channels from the substrate, mitigation of the capacitance associated with spacer-gap separation, and vertical architecture scaling with nanowires”), FIG. 1i.) Accordingly, in my opinion, a person of ordinary skill in the art would have been motivated to implement a nanowire-based channel region in place of a fin-shaped channel region when fabricating devices like those disclosed by Murthy.

88. Indeed, non-planar nanowire devices were well-known in the art, and a person of ordinary skill in the art would have understood that structures and teachings related to fin-based non-planar devices like those disclosed by Murthy are compatible with, and applicable to, nanowire non-planar devices like those disclosed by Ching. (Ex. 1011, ¶[0044] (“A non-planar architecture can be implemented, for instance, using FinFETs or nanowire configurations.”); Ex. 1012, ¶[0024] (“the semiconductor structure 300 may include a first plurality of fins 102 ... formed from a semiconductor substrate”), ¶[0033] (describing a fin based device with high germanium concentration source/drain regions), ¶[0068] (“In another embodiment of the present invention, the method described above may be applicable to other semiconductor structures, such as nanowire FET devices. In this case, the gate

structure 14 may enfold a nanowire channel located between a source-drain region.”); Ex. 1013,³ ¶[0042] (“Although the portions of the structures described herein take the form of a fin, it will be understood that the different doping levels provided to threshold voltage control regions and carrier regions can be applied to other geometries such as a ‘gate-all-around’ structure (such as a nanowire structure).”); Ex. 1010, ¶[0013] (“In an embodiment, the fin structures 107 may comprise a dual channel portion of a gate all around (GAA) nanowire device,” where “[t]he number of channels in the device will depend on the numbers of layers in the fin structures 107.”), ¶[0024] (“Embodiments herein enable the fabrication of self-aligned gate-all-around (GAA) silicon and silicon germanium channel transistor structures and devices.”).)

89. Indeed, Murthy states that the disclosed “techniques can be embodied, for instance, in planar or non-planar transistor devices” and does not limit the non-planar devices to FinFETS using a fin that is a thin strip of semiconductor material. (Ex. 1005, Abstract, ¶[0013].)

90. As a person of ordinary skill in the art would have appreciated, using nanowires for the channel region as disclosed by Ching as opposed to a single thin

³ I cite to Basker (Ex. 1012) and Oh (Ex. 1013) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

strip of semiconductor material as disclosed by Murthy would have been the simple substitution of one type of transistor channel (Ching's nanowires) for another (Murthy's fin portion) in a similar device in a predictable manner to produce the expected result of a functional non-planar transistor.

91. Based on their knowledge of such well-known nanowire transistors and Ching's detailed disclosure of formation of nanowires in a device similar to that disclosed by Murthy, a person of ordinary skill in the art would have had a reasonable likelihood of success in implementing a nanowire-channel transistor based on the teachings of Murthy and Ching. Therefore, in my opinion, the Murthy-Ching combination discloses or suggests using nanowires with gate-all-around channel regions ("the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons") in a non-planar device like that I discuss above in section IX.A.1. In other words, other than having a different channel region (i.e., nanowires instead of a fin-shaped channel), the transistor has the same structure discussed above for claim 1 in section IX.A.1.

92. I have been asked to assume a scenario in which the Murthy-Ching combination is limited to a PMOS device that uses germanium nanowires such that the nanowires do not present "a surface that consists essentially of silicon" with which the first and second portions of the source/drain regions are "in direct

contact.” Under such an assumption, the first and second portions of the source/drain regions of the Murthy-Ching combination are in direct contact with the underlying lower portion of the fin that, as I discuss above in sections IX.A.1(d)-(e) “consists essentially of silicon.” (See my discussion above in sections IX.A.1(d)-(e).) As I noted above, in the Murthy-Ching combination, the channel portion of the fin as disclosed by Murthy is replaced with nanowires, while the fin structure upon which the source/drain regions are formed remains the same as in a non-nanowire FinFET like that disclosed by Murthy.

2. Claim 17

a) “An integrated circuit, comprising:”

93. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 17 of the ’334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Murthy discloses “an integrated circuit” for the same reasons I discuss above for claim element 1[a]. (See my discussion above in section IX.A.1(a).)

b) “a nanowire or nanoribbon comprising semiconductor material;”

94. In my opinion, the Murthy-Ching combination discloses or suggests this claim limitation. As I discuss above for claim 11, the Murthy-Ching combination discloses or suggests a non-planar transistor that includes a nanowire. (See my discussion above in section IX.C.1.) Ching further discloses that the

nanowires can be made of silicon and germanium, both of which constitute “semiconductor material.” (Ex. 1006, Title (“Silicon and Germanium Nanowire Formation”), Abstract (“germanium nanowire channels”) (“silicon nanowire channels”), ¶¶[0014]-[0015], [0018], [0022]-[0025]; *see also* Ex. 1011, ¶[0044] (“A nanowire transistor (sometimes referred to as gate-all-around FET) is configured very similarly, but instead of a fin, a nanowire (e.g., silicon or SiGe or Ge nanowire) is used and the gate material generally surrounds the channel region on all sides.”).)

c) “a gate structure wrapped around the nanowire or nanoribbon;”

95. In my opinion, the Murthy-Ching combination discloses or suggests this claim limitation. For example, as I discuss above for claim 11, the Murthy-Ching combination discloses or suggests a non-planar transistor that includes a nanowire with a gate structure that is a “gate-all-around” structure that is wrapped around the nanowire. (See my discussion above in section IX.C.1)

d) “a source structure to one side of the gate structure and abutting the nanowire or nanoribbon, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”

e) a drain structure to an opposite side of the gate structure and abutting the nanowire or nanoribbon, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout

the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;”

96. In my opinion, the Murthy-Ching combination discloses or suggests these features. As I discuss above for claim 11, the Murthy-Ching combination includes a nanowire channel region as opposed to a fin channel region (as disclosed by Murthy and discussed above in section IX.A.1). (See my discussion above in sections IX.C.1, IX.A.1.) Therefore, for the same reasons I discuss above for the “source structure” and “drain structure” in the context Murthy and claim 13, the Murthy-Ching combination discloses or suggests a “source structure” on one side of the gate structure surrounding the channel region that includes the nanowire and a “drain structure” on the opposite side of the gate structure, where the source and drain structures abut the nanowire in order to form a transistor device, where the source/drain structures include first/second portions having germanium at a concentration of at least 50 atomic percent throughout as recited in claim 17. (See my discussion above in sections IX.C.1, IX.A.9(d)-(e). As I discuss above for claim 11 and claim elements 13[d] and 13[e] with respect to the recited “source structure” and “drain structure,” the first/second portions of the source/drain structures are in direct contact with the lower portion of the fin underlying the source/drain structures, where the fin is made of silicon. (See my discussion above in sections IX.C.1, IX.A.9(d)-(e).)

- f) **“a first contact structure on the first portion of the source structure and including a metal-germanide; and;”**
- g) **“a second contact structure on the second portion of the drain structure and including a metal-germanide.”**

97. In my opinion, the Murthy-Ching combination discloses or suggests these limitations for the same reasons I discuss above that show Murthy discloses the features included in claim elements 13[f] and 13[g]. (See my discussion above in sections IX.A.9(f)-(g).)

3. Claim 18

“The integrated circuit of claim 17, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

98. In my opinion, the Murthy-Ching combination discloses or suggests these features. As I discuss above for claim elements 17[d]-[e] and 13[d]-[e], the “first portion” and “second portion” of the source/drain structures are in direct contact with the underlying lower portion of the fin which is part of the substrate, which can be a “bulk silicon,” or silicon on insulator substrate. (See my discussion above in sections IX.C.2(d)-(e), IX.A.9(d)-(e), IX.A.2; Ex. 1005, ¶[0019] (“For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate....”), ¶[0052] (“The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate

400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).”), ¶[0028] (“The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration.”).) Therefore, the “surface,” which corresponds to the upper surface of the lower portion of the fin is a surface of “a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator” as claimed. (Ex. 1001, 5:35-40; *see also* Ex. 1015, 103, 115; Ex. 1017, 93-97.)

4. Claim 20

“The integrated circuit of claim 17, wherein the first and second portions further include one or both of silicon and tin, and further include a p-type dopant.”

99. In my opinion, the Murthy-Ching combination discloses or suggests these features for the same reasons I discuss above for claim 16 in section IX.A.11. (See my discussion above in sections IX.A.11.)

D. Wann Discloses All of the Features of Claim 1, 2, 6-8, 10, and 12-14

100. In my opinion, Wann discloses all of the features of claims 1, 2, 6-8, 10, and 12-14 of the '334 patent.

1. Claim 1

a) “An integrated circuit, comprising:”

101. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 1 of the '334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Wann discloses the

limitations therein. For example, Wann discloses an integrated circuit that includes a fin field effect transistor, FinFET 200:

FIGS. 2A-15 are perspective and cross-sectional views of a semiconductor device 200 comprising a contact structure 230 at various stages of fabrication according to various embodiments of the present disclosure. As employed in the present disclosure, the term semiconductor device 200 refers to a fin field effect transistor (FinFET) and is hereinafter referred to as a FinFET 200. The FinFET 200 refers to any fin-based, multi-gate transistor. Other transistor structures are within the contemplated scope of the disclosure. **The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).**

(Ex. 1007, ¶[0009] (emphasis added); *see also id.*, [0001]-[0002])

102. Wann's FinFET 200 is shown in figures 9B and 9A below.

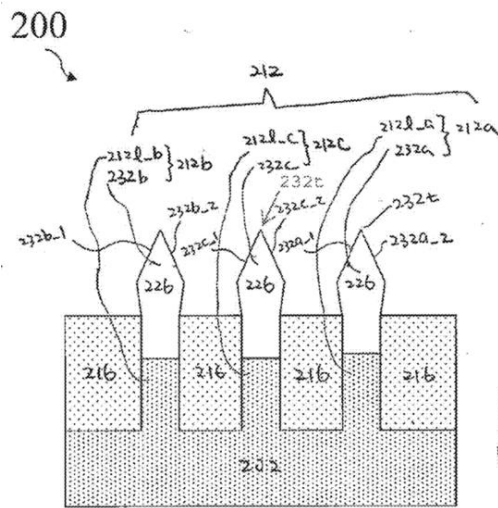


FIG. 9B

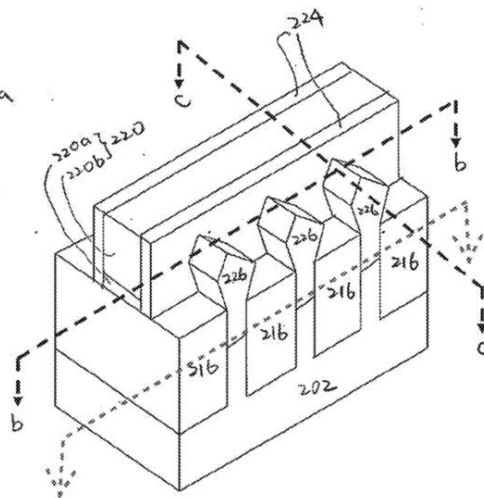


FIG. 9A

(Id., FIGs. 9B, 9A.)

b) **“a non-planar body comprising semiconductor material, wherein the non-planar body has top and side surfaces;”**

103. In my opinion, Wann discloses this claim feature. As shown in annotated figures 9A and 9B below, Wann’s FinFET 200 includes a substrate 202, which is etched to form fins 212, each of which constitutes a “non-planar body.” (Ex. 1007, Abstract (“a fin structure extending upward from the substrate major surface, wherein the fin structure comprises a first fin, a second fin, and a third fin between the first fin and the second fin;”), ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”), ¶[0015].) Each fin corresponding to a non-planar body is consistent with claim 10 of the ’334 patent,

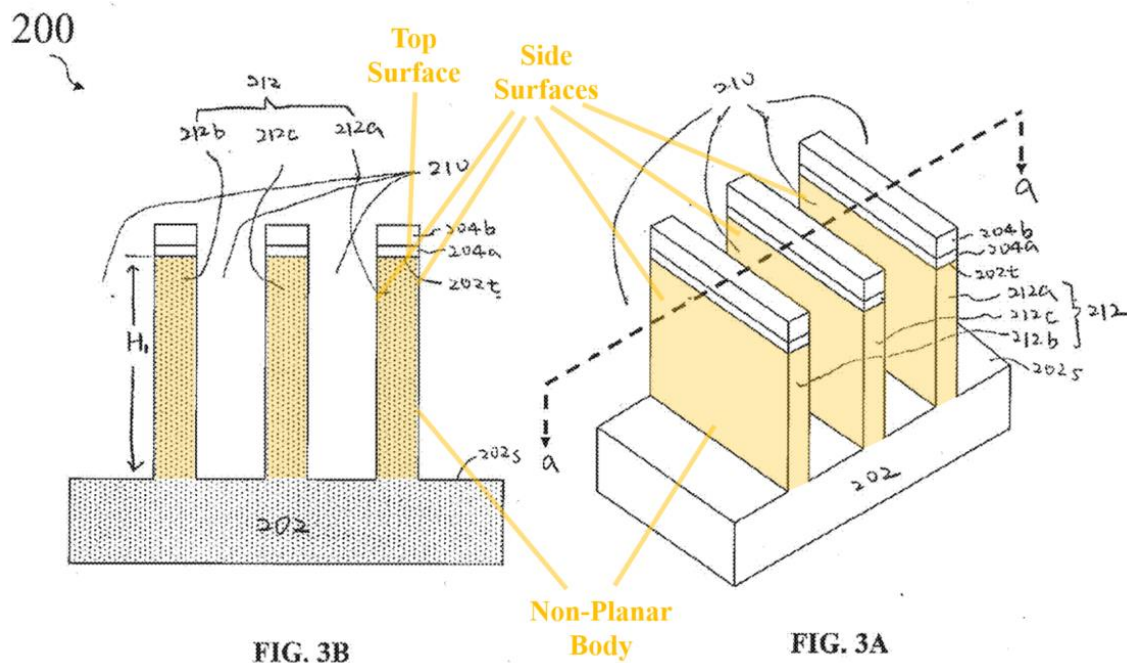
below in section IX.D.6.)



(Ex. 1007, FIGs. 9B, 9A (annotated).)

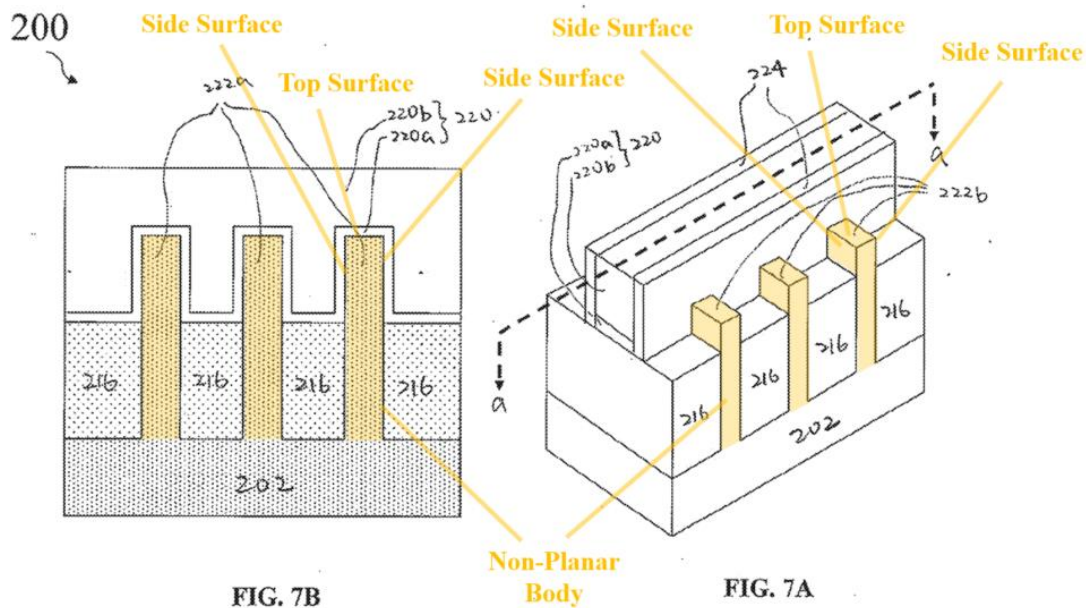
104. As shown in annotated figures 3B and 3A below, which correspond to the structure shown above in figures 9B and 9A at an earlier stage in the fabrication process, each of the fins (“non-planar body”) that extends upward from substrate 202, includes a top surface and side surfaces. (*Id.*, ¶[0015] (“FIG. 3A is a perspective view of the semiconductor device 200 at one of the various stages of fabrication according to an embodiment, and FIG. 3B is a cross-sectional view of semiconductor device 200 taken along the line a-a of FIG. 3A. The mask layer 204b and pad layer 204a are etched through openings 208 to expose underlying semiconductor substrate

202. The exposed semiconductor substrate 202 is then etched to form trenches 210 lower than the top surface 202t of the semiconductor substrate 202. Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins (i.e., the fin structure 212). In the depicted embodiment, the semiconductor fins 212 extend downward from the substrate top surface 202t to the major surface 202s to a first height H_1 , thereby extending upward from the major surface 202s of the substrate 202.”.)



(*Id.*, FIGs. 3B, 3A (annotated).)

105. As shown in annotated figures 7B and 7A below, which correspond to the structure shown above in figures 9B and 9A at an earlier stage in the fabrication process, the fins of the substrate 202 include a top surface and side surfaces.



(*Id.*, FIGs. 7B, 7A (annotated).)

c) “a gate structure on at least the top and side surfaces of the non-planar body;”

106. In my opinion, Wann discloses this limitation. For example, as shown in annotated figure 9A below, Wann discloses a gate stack 220 (“gate structure”) that includes gate dielectric layer 220a (green) and gate electrode layer 220b (blue), on the top and side surfaces of the fin (“non-planar body”). (Ex. 1007, ¶[0020].)

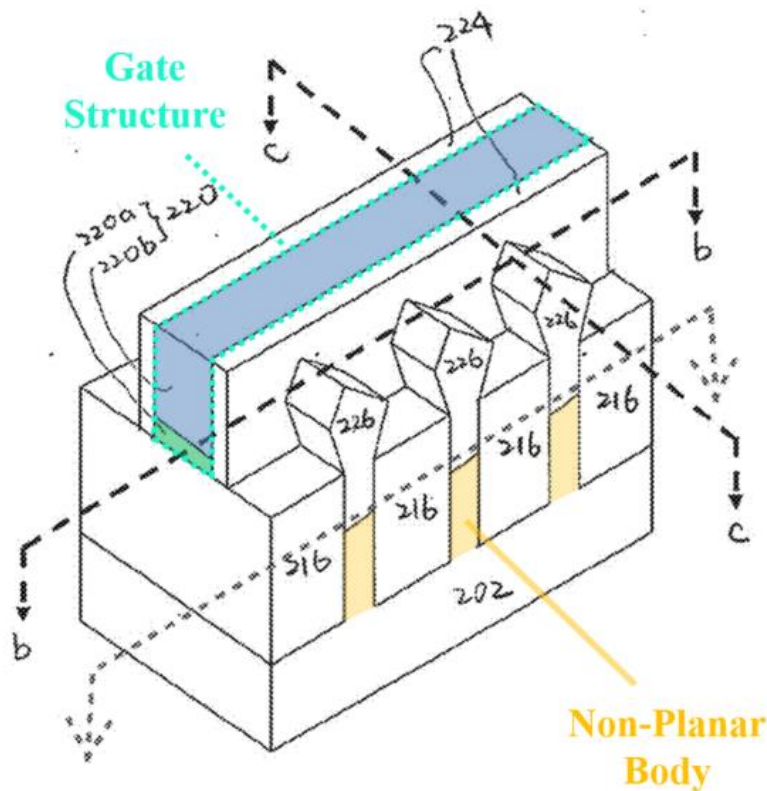
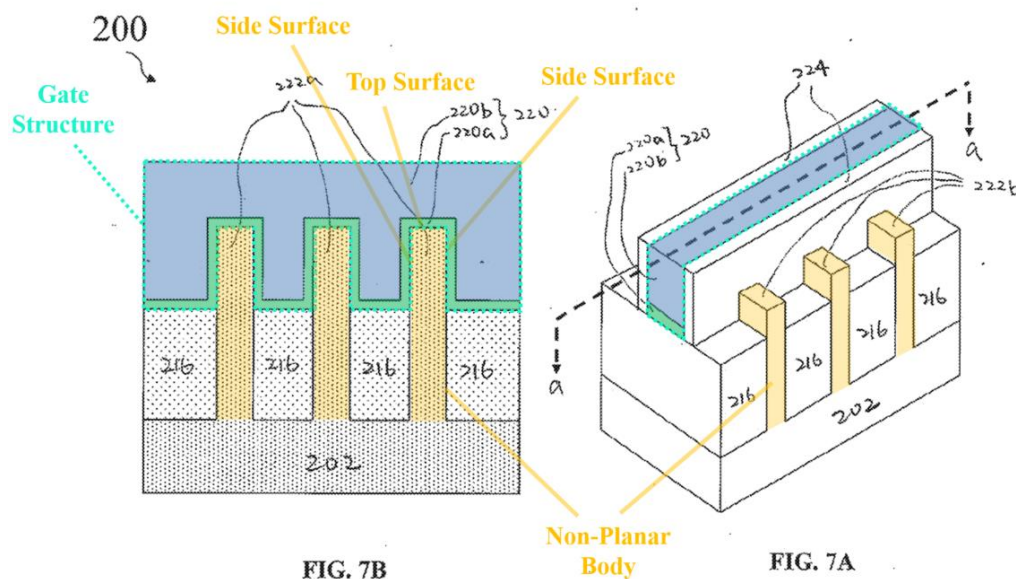


FIG. 9A

(*Id.*, FIG. 9A (annotated).)

107. As shown in annotated figures 7B and 7A below, which correspond to the structure shown above in figures 9B and 9A at an earlier stage in the fabrication process, Wann discloses that the gate stack 220 is formed covering the top and side surfaces of channel portions 222a, which corresponds to a portion of each of the fins (“non-planar body”). (*Id.*, ¶[0020] (“FIG. 7A is a perspective view of the semiconductor device 200 at one of the various stages of fabrication according to an embodiment, and FIG. 7B is a cross-sectional view of semiconductor device 200 taken along the line a-a of FIG. 7A. A gate stack 220 is formed over the channel

portions 222a of the upper portion 222 of the fins 212 and extending to the top surface 216t of the STI region 216. In some embodiments, the gate stack 220 comprises a gate dielectric layer 220a and a gate electrode layer 220b over the gate dielectric layer.”), ¶[0021] (“In FIGS. 7A and 7B, the gate dielectric 220a is formed to cover the channel portions 222a of the upper portions 222 of the fins 212.”), ¶[0002] (“A gate is provided over (e.g., wrapping) the fin.”), FIGS. 7A, 7B.)

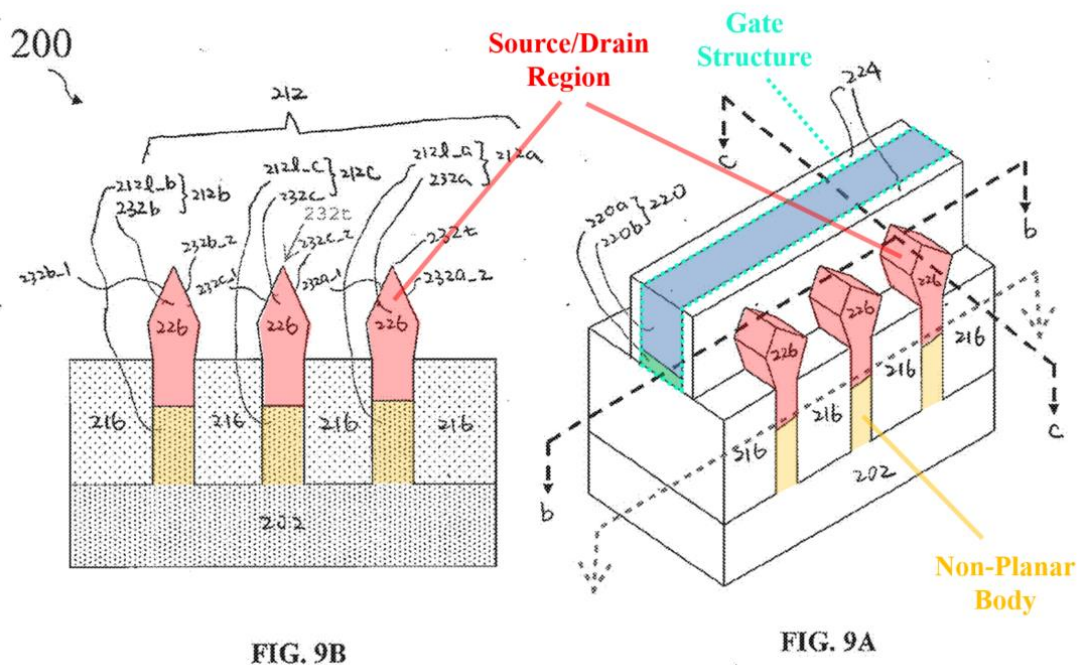


(*Id.*, FIGs. 7B, 7A (annotated).)

- d) “a source region adjacent the non-planar body, the source region including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon; and”
- e) “a drain region adjacent the non-planar body, the drain region including a second portion, the second portion including germanium at a concentration of at

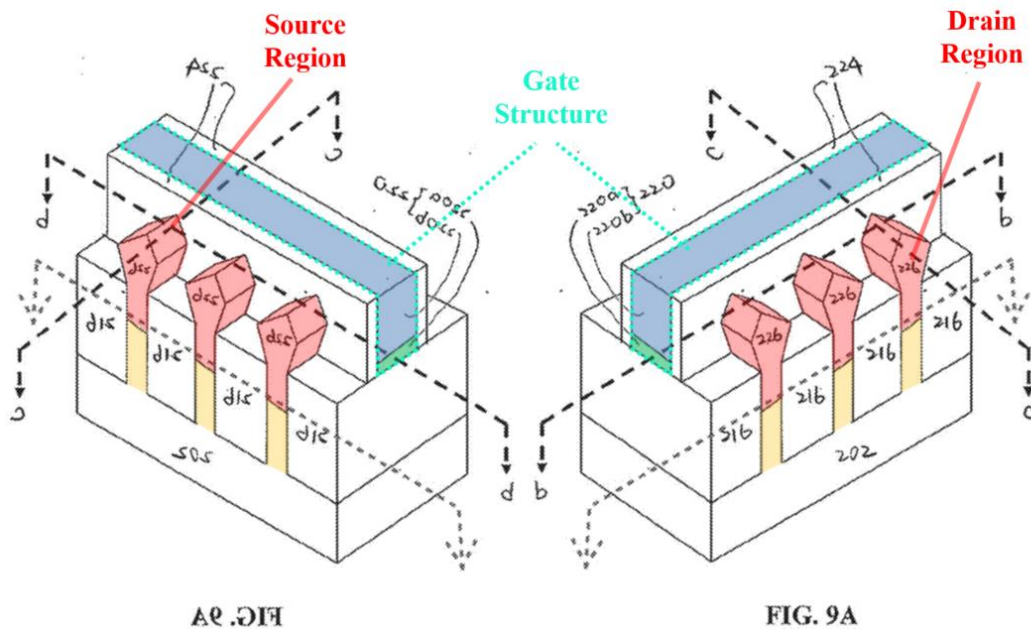
least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with a surface that consists essentially of silicon.”

108. In my opinion, Wann discloses these features. For example, as shown in annotated figures 9B and 9A below, Wann discloses strained material 226 (“first/second portions”) included in the source/drain regions 223 (“source region” and “drain region”) of the FinFET. (Ex. 1007, ¶[0025] (“Referring to FIGS. 9A and 9B, after the formation of the S/D cavities 228 in the S/D portions 222b, the structure in FIGS. 9A and 9B is produced by epi-growing a strained material 226 in the S/D cavities 228”), ¶[0026] (“In some embodiments, the strained material 226 is hereinafter referred to as S/D regions 232 (comprising 232a, 232b, and 232c).”).)



(Id., FIG. 9B, 9A (annotated).)

109. While not visible in figure 9A, a person of ordinary skill in the art would have understood that there are additional source/drain (S/D) regions on the opposite side of the gate structure corresponding to each of the visible S/D regions 226. (See Ex. 1005⁴, ¶[0052] (“A source region comprises the epitaxial regions 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown).”).) Figure 9A has been horizontally flipped below in order to help illustrate this understanding.



(Ex. 1007, FIG. 9A (rotated, annotated).)

⁴ I cite to Murthy to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

110. Depending on how the FinFET is coupled to surrounding circuitry, the S/D region on a first side of the gate structure functions as the “source region,” whereas the corresponding S/D region on the other side functions as the “drain region.” For example, as shown in annotated figure 9A above, if the S/D region on the back side of the FinFET (only visible in the horizontally flipped figure 9A) is designated as the source region, then the S/D region on the front side of the FinFET is the drain region. A person of ordinary skill in the art would have appreciated that, from the perspective of the FinFET device itself, the source and drain regions are interchangeable.

111. Wann’s disclosure of corresponding S/D regions lying on opposite sides of the gate structure is confirmed by Wann’s description of the formation of the S/D regions with respect to figures 6A-8B.⁵ For example, Wann discloses that in annotated figure 6A below, “the upper portions 222 of the fins 212 may comprise

⁵ The understanding that a corresponding source/drain region is on the opposite side of the channel region from the source/drain region visible in figure 9A of Wann is also supported by Wann-108 (Ex. 1014), which is a patent derived from a continuation application claiming priority to Wann and shows source/drain regions on both side of the gate structure in, for example, figures 7A and 9A. (Ex. 1014, FIGs. 7A, 9A.)

channel portions 222a and source/drain (S/D) portions 222b,” where “[t]he channel portions 222a are used to form channel regions of the semiconductor device 200.” (Ex. 1007, ¶[0019].) The “channel region” of the FinFET is the portion that lies between the source and drain regions.

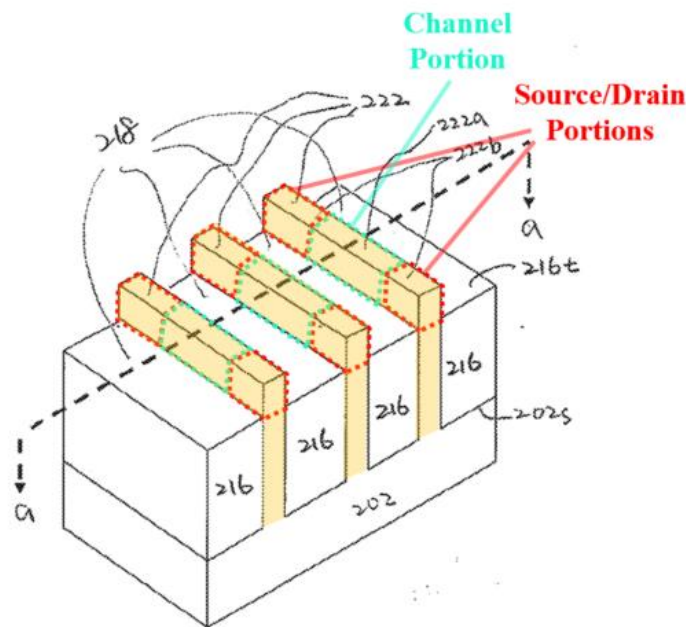


FIG. 6A

(*Id.*, FIG. 6A (annotated).)

112. As shown in annotated figure 7A below, the gate stack 220 is formed covering the top and side surfaces of channel portions 222a, leaving source/drain portions 222b exposed on both sides of the gate stack 220. (*Id.*, ¶[0020] (“FIG. 7A is a perspective view of the semiconductor device 200 at one of the various stages of fabrication according to an embodiment, and FIG. 7B is a cross-sectional view of

semiconductor device 200 taken along the line a-a of FIG. 7A. A gate stack 220 is formed over the channel portions 222a of the upper portion 222 of the fins 212 and extending to the top surface 216t of the STI region 216.”), ¶[0021] (“In FIGS. 7A and 7B, the gate dielectric 220a is formed to cover the channel portions 222a of the upper portions 222 of the fins 212.”), FIGS. 7A, 7B.)

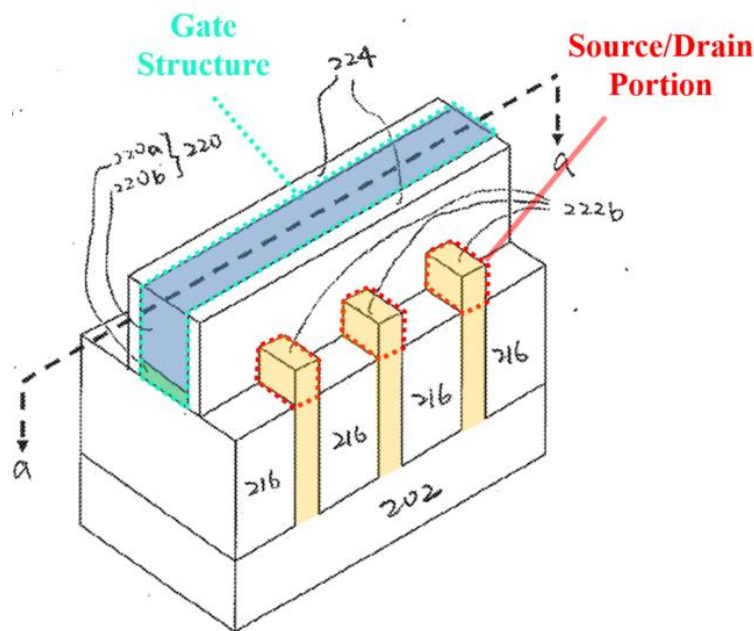


FIG. 7A

(*Id.*, FIG. 7A (annotated).)

113. As shown in annotated figures 8B and 8A below, selective etching is used to recess the source/drain portions 222b of the upper portion 222 of the fins to form source/drain cavities 228. (Ex. 1007, ¶[0024] (“Using the gate stack 220, dielectric layer 224, and STI region 216 as hard masks, a biased etching process is

performed to recess the S/D portions 222b (shown in FIGS. 6A and 7A) of the upper portions 222 of the fins 212 that are unprotected or exposed to form the S/D cavities 228 below the top surface 202t, thereby leaving lower portions 212l (comprising 212l_a, 212l_b, and 212l_c) of the fin structure 212”).) Because, as shown in figure 6A above, source drain portions 222b are on both sides of the gate stack 220, the cavities for the source/drain regions are formed on both sides of the gate stack.

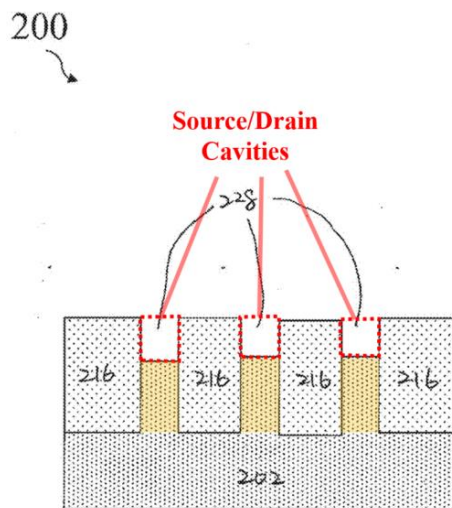


FIG. 8B

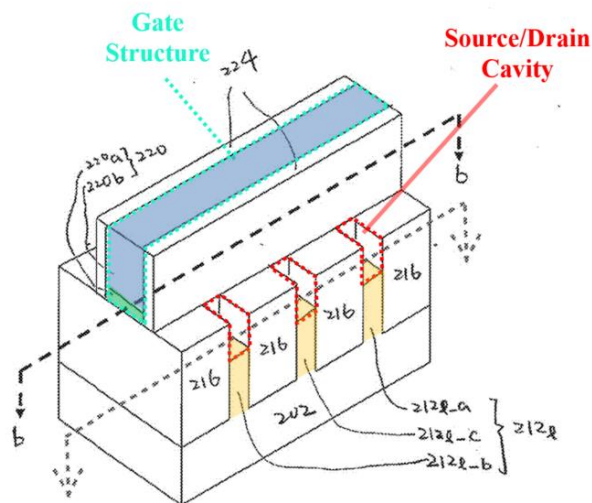


FIG. 8A

(*Id.*, FIGs. 8B, 8A (annotated).)

114. Following formation of the source/drain cavities shown in figures 8A and 8B above, “the structure in FIGS. 9A and 9B is produced by epi-growing a strained material 226 in the S/D cavities 228,” where the strained material corresponds to the claimed “first/second portions” of the “source/drain regions” for the FinFET. (*Id.*, ¶¶[0025]-[0026].)

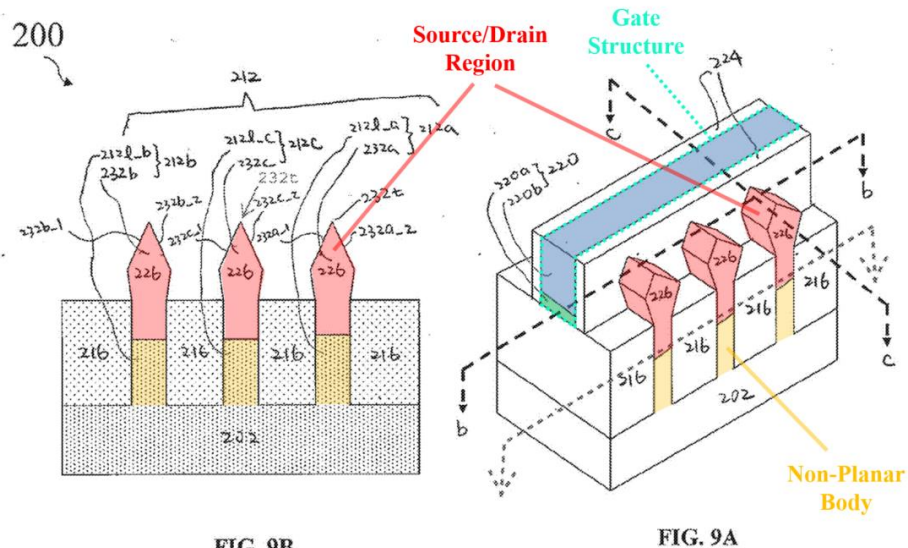


FIG. 9B

FIG. 9A

(*Id.*, FIGs. 9B, 9A (annotated).)

115. The source/drain regions that include the strained regions 226 grown in the source/drain cavities for each of the fins of the FinFET 200 are “adjacent to the non-planar body” as they lie on top of a portion the fin (“non-planar body”) and also have the channel portion 222a of the upper portion 222 of the fin between them. In other words, the source and drain regions are “adjacent” to the non-planar body, which is a fin of the silicon substrate 202, because they are separated by the channel portion of the fin and also because they lie on top of the lower portion the fin. (*Id.*, FIGs. 9A, 9B.) Indeed, a person of ordinary skill in the art would have understood that S/D regions 232 are in direct contact with channel portion 222a of the fin in order to form a functioning transistor.

116. Wann discloses an embodiment in which the strained material 226 (“first/second portions”) is germanium (Ge). (Ex. 1007, ¶[0025] (“In some

embodiments, the **strained material 226 comprises Ge** or SiGe for a p-type FinFET.”).) Therefore, Wann discloses “first/second portions” made of germanium (“including germanium at a concentration of at least 50 atomic percent throughout the [first/second] portion”) as recited in claim 1. Such an understanding is confirmed by Wann’s differentiation between using straight germanium (Ge) for the strained material in one embodiment as opposed to silicon-germanium (SiGe) for the strained material in another embodiment. (*Id.*, ¶[0025], ¶[0028] (“In the Ge-growing embodiment...”), ¶[0029] (“In the SiGe-growing embodiment...”).)

117. As I discuss above, the strained material (“first/second portions of the source/drain regions”) is in direct contact with the channel portion 222a of the upper portion 222 of the fin, which is between them, as well as in direct contact with the underlying lower portion of the fin. The fin is part of the silicon substrate, and therefore first and second portions of the germanium source/drain regions are “in direct contact with a surface that consists essentially of silicon.” (*Id.*, ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”), ¶[0011] (“In at least one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer).”), ¶[0015] (“The exposed semiconductor substrate 202 is then etched to form trenches 210 lower than the top surface 202t of the semiconductor substrate 202. Portions of the semiconductor substrate 202

between trenches 210 form semiconductor fins (i.e., the fin structure 212).”), FIGs. 3A, 3B.)

2. Claim 2

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

118. In my opinion, Wann discloses this limitation. As I discuss above for claim elements 1[d]-[e], the strained material (“first/second portion”) of the source/drain regions is in direct contact with the channel portion 222a of the upper portion 222 of the fin and the underlying lower portion of the fin which is part of the silicon substrate 202, which can be a “crystalline silicon substrate (e.g., wafer).” (See my discussion above in sections IX.D.1(d)-(e); Ex. 1007, ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”), ¶[0011] (“In at least one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer).”), ¶[0015] (“The exposed semiconductor substrate 202 is then etched to form trenches 210 lower than the top surface 202t of the semiconductor substrate 202. Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins (i.e., the fin structure 212).”), FIGs. 3A, 3B.) Therefore, the “surface,” which corresponds to either the side surface of

the channel portion 222a or the upper surface lower portion of the fin is a surface of “a bulk silicon substrate” as claimed. (See Ex. 1001, 5:35-40.)

3. Claim 6

“The integrated circuit of claim 1, wherein the first and second portions include a p-type dopant.”

119. In my opinion, Wann discloses this limitation. For example, Wann discloses that strained material 226 (“first and second portions”) “comprises Ge or SiGe for a **p-type FinFET**.” (Ex. 1007, ¶[0025] (emphasis added).) A person of ordinary skill in the art would have understood that for a p-type FinFET the S/D regions 232, including the strained material, are doped to include p-type dopants. (*Id.*, ¶[0011] (“doped regions may be doped with p-type dopants, such as boron or BF₂”); see also Ex. 1017, 15-17; Ex. 1015, 115-117.) Such an understanding is consistent with the disclosure of the ’334 patent. (Ex. 1001, 2:60-64 (“Note that the Ge-rich layer as variously described herein is to be used for p-MOS source/drain contacts and is therefore a p-type layer, meaning it has p-type doping (e.g., using boron (B), gallium (Ga), and/or any other suitable dopant).”).)

4. Claim 7

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is undoped.”

120. In my opinion, Wann discloses this limitation. As I discuss above for claim elements 1[d]-[e] and claim 2, the “surface that consists essentially of silicon”

is part of the silicon substrate 202, which can be a “crystalline silicon substrate (e.g., wafer).” (See my discussion above in sections IX.D.1(d)-(e), IX.D.2; Ex. 1007, ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”), ¶[0011] (“In at least one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer).”), ¶[0015] (“The exposed semiconductor substrate 202 is then etched to form trenches 210 lower than the top surface 202t of the semiconductor substrate 202. Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins (i.e., the fin structure 212).”), FIGs. 3A, 3B.) A person of ordinary skill in the art would have understood that, absent any indication that the substrate is doped, crystalline silicon material is “undoped.” (Ex. 1015, 103, 115; Ex. 1017, 93-97.) Wann does not disclose doping the channel portion 222a of the upper portion 222 of the fin or the lower portion of the fin underlying the source/drain regions. (See my discussion above in section IX.D.2; Ex. 1007, ¶¶[0002], [0011], [0015].)

5. Claim 8

“The integrated circuit of claim 1, further comprising an additional portion on the first and second portions, the additional portions including a metal and germanium.”

121. In my opinion, Wann discloses this limitation. For example, Wann discloses forming metal germanide (“additional portions including a metal and germanium) over the germanide strained material 226 (“first and second portions”):

The processing steps up to this point have provided the substrate 202 having the strained material 226 over each lower portion 212l. Conventionally, **metal germanide over the strained material 226 may be formed** by blanket depositing a thin layer of metal material, such as Ni, Pt, Ti, Co, Pd, and combinations thereof. The substrate 202 is then heated, which causes Ge to react with the metal where contacted. After the reaction, **a layer of metal germanide is formed** between the Ge-containing material and the metal. The unreacted metal is selectively removed through the use of an etchant that attacks the metal material but does not attack germanide.

(Ex. 1007, ¶[0030] (emphasis added).)

122. Wann further discloses that, for the particular geometry for the facets of the strained material shown in the embodiment of figure 9, the conventional process can result in “triangular germanide” with “small-volume germanide on the strained material 226 [that] causes high contact resistance of S/D regions of the FinFET and thus degrades the device performance.” (*Id.*, ¶[0030].) Therefore, Wann discloses another technique for forming a “rectangular germanide to replace the triangular germanide.” (*Id.*, ¶[0031]; *see also id.*, ¶¶[0032]-[0042], FIGs. 10-

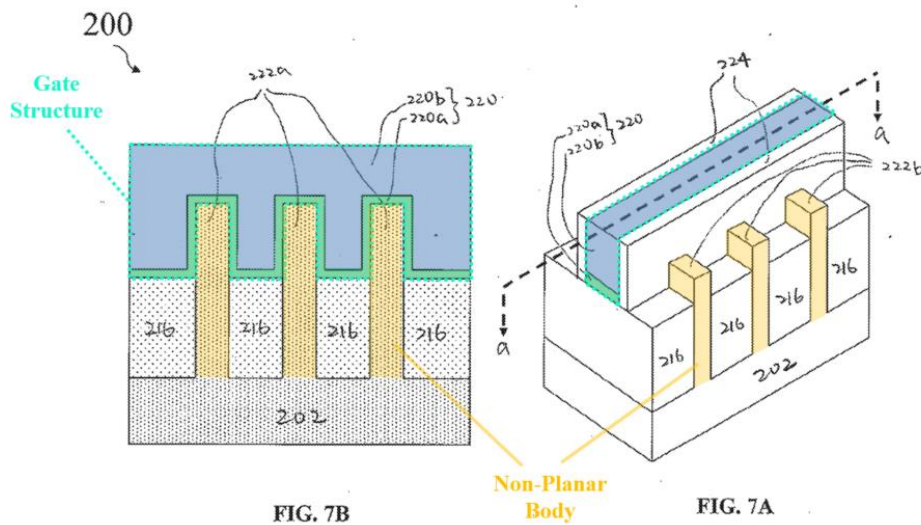
13.) Like the conventional germanide formation, Wann's "rectangular germanide" technique deposits metal on the strained material 226 (*id.*, ¶[0037]), and then the substrate is heated to form germanide (*id.*, ¶[0038].) "In other words, the first metal layer 242 in contact with the strained material 226 is then transformed into a germanide by a thermal process," where "the germanide 246 comprises NiGe, PtGe, TiGe₂, CoGe₂, or PdGe." (*Id.*, ¶[0038].)

123. Wann's disclosure of formation of the germanide is consistent with the disclosure of the '334 patent. (Ex. 1001, 10:34-61.) Therefore, Wann discloses "additional portions" of germanide "on the first and second portions," where the additional portions include a metal and germanium as recited in claim 8.

6. Claim 10

"The integrated circuit of claim 1, wherein the non-planar body is a fin, the fin between portions of the gate structure."

124. In my opinion, Wann discloses this limitation. As I discuss above with respect to claim 1, each of Wann's fins that extend upward from the planar surface of the substrate constitutes the claimed "non-planar body." (See my discussion above in section IX.D.1(b)) As shown in figures 7A and 7B below, each fin includes a channel portion 222a that is covered on the top and sides by the gate structure ("the fin between portions of the gate structure").



(*Id.*, FIGs. 7B, 7A (annotated).)

7. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

125. In my opinion, Wann discloses this limitation. Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (Ex. 1007, ¶[0009] (“The FinFET 200 refers to any fin-based, multi-gate transistor. ... **The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).**”) (emphasis added).) A microprocessor that includes that includes Wann’s FinFET transistor is a “computing system,” as it is an electronic device that includes an interconnected set of components that processes data. Such an understanding is consistent with the disclosure of the ’334 patent:

In various implementations, the **computing system 1000** may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, **the system 1000 may be any other electronic device that processes data or employs one or more transistor devices as variously described herein.**

(Ex. 1001, 14:14-23 (emphasis added).)

8. Claim 13

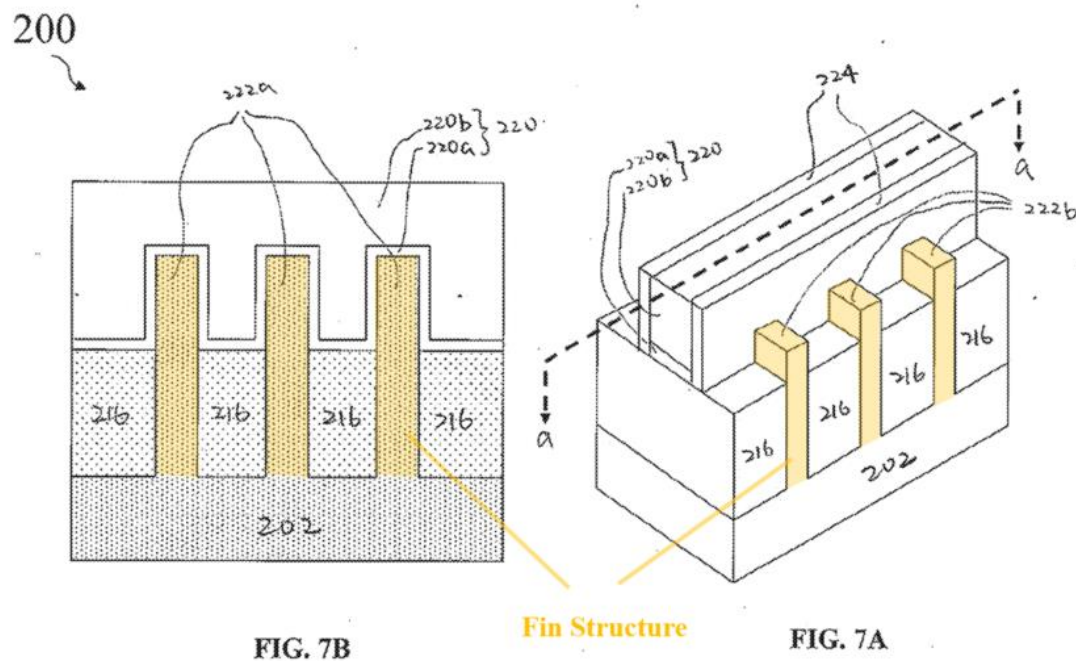
a) “An integrated circuit, comprising:”

126. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 13 of the ’334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Wann discloses “an integrated circuit” for the same reasons I discuss above for claim element 1[a]. (See my discussion above in section IX.D.1(a).)

b) “a fin structure comprising semiconductor material, wherein the fin structure has top and side surfaces;”

127. In my opinion, Wann this claim limitation. As I discuss above for claim element 1[b] and shown in annotated figures 9A and 9B below, Wann’s FinFET 200 includes a substrate 202 that is etched to form fins 212, where each fin constitutes a

“fin structure” as recited in claim element 13[b]. (See my discussion above in section IX.D.1(b); Ex. 1007, Abstract (“a fin structure extending upward from the substrate major surface, wherein the fin structure comprises a first fin, a second fin, and a third fin between the first fin and the second fin;”), ¶[0002] (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate.”) ¶[0015].) For the same reasons I discuss above for the “non-planar body” recited in claim 1, Wann discloses a “fin structure” with top and side surfaces as recited in claim 13, where the “fin structure” includes one of the fins extending from the underlying substrate. (See my discussion above in section IX.D.1(b).)



(Ex. 1007, FIGs. 7B, 7A (annotated).)

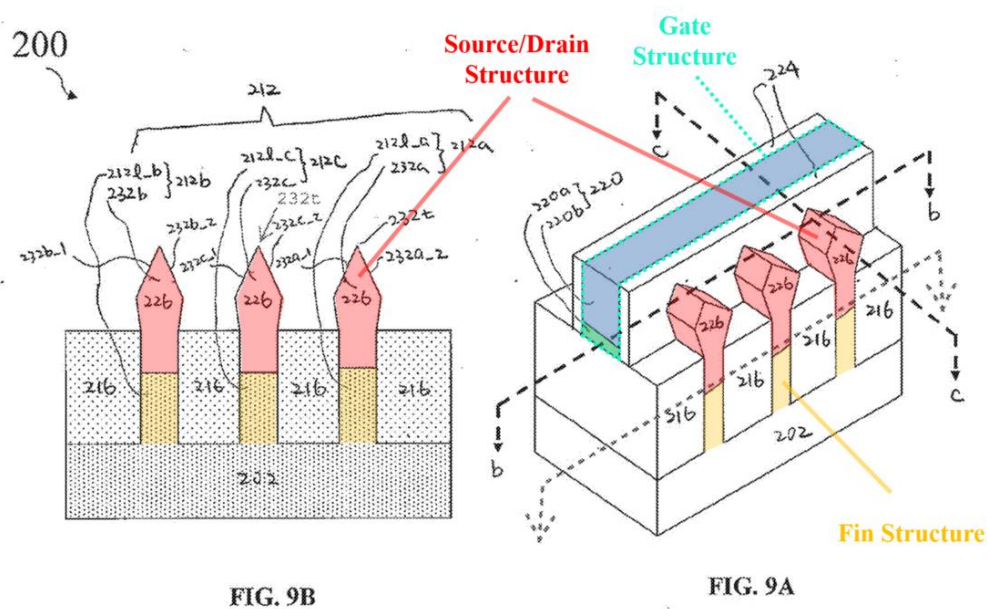
- c) **“a gate structure on the top and side surfaces of the fin structure;”**

128. In my opinion, Wann discloses this limitation for the same reasons I discuss above for claim element 1[c]. (See my discussion above in section IX.D.1(c).) Gate stack 220 is formed covering the top and side surfaces of the channel portion 222a included in the “fin structure.” (*Id.*)

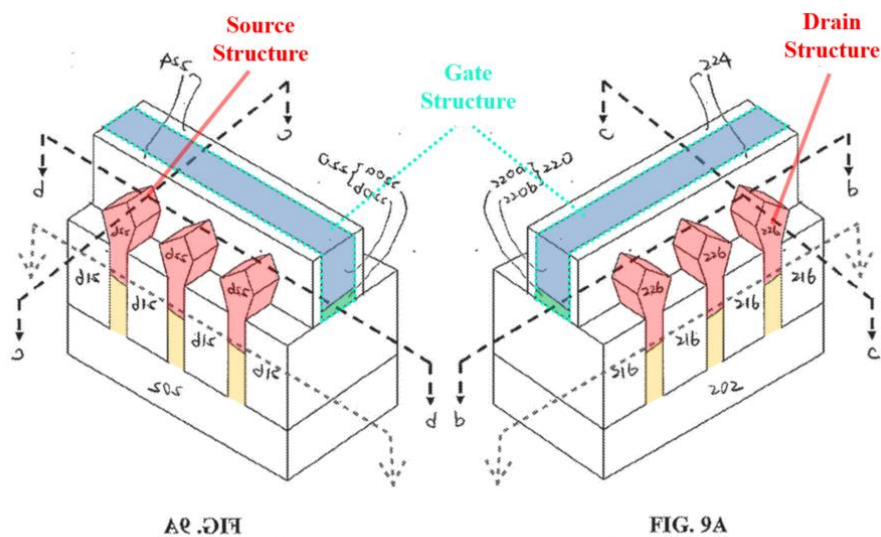
- d) **“a source structure to one side of the gate structure and abutting the fin structure, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”**
- e) **a drain structure to an opposite side of the gate structure and abutting the fin structure, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;”**

129. In my opinion, Wann discloses these features. As I discuss above for claim elements 1[d] and 1[e] and shown in figures 9A and 9B below, Wann discloses strained material 226 (“first/second portions”) included in the source/drain regions 223 (“source structure” and “drain structure”) that are on opposite sides of the gate structure, and abut the channel region 222a, which is part of the “fin structure.” (See my discussion above in sections IX.D.1(d)-(e), IX.D.8(b).) As also discussed above for claim elements 1[d] and 1[e], Wann discloses forming the strained material 226

(“first/second portions”) of germanium such that the first/second portions include “at least 50 atomic percent” germanium throughout, where the first/second portions are in direct contact with the underlying lower portion of the fin and the channel region, which “consist essentially of silicon.” (See my discussion above in sections IX.D.1(d)-(e), IX.D.8(b).)



(Ex. 1007, FIGs. 9B, 9A (annotated).)



(*Id.*, FIG. 9A (rotated, annotated).)

- f) **“a first contact structure on the first portion of the source structure and including a metal-germanide; and;”**
- g) **“a second contact structure on the second portion of the drain structure and including a metal-germanide.”**

130. In my opinion, Wann discloses these features. For example, as I discuss above for claim 8, Wann discloses forming metal germanide (“first contact structure” and “second contact structure”) on the strained material 226 (“first portion of the source structure” and “second portion of the drain structure”):

The processing steps up to this point have provided the substrate 202 having the strained material 226 over each lower portion 212l. Conventionally, metal germanide over the strained material 226 may be formed by blanket depositing a thin layer of metal material, such as Ni, Pt, Ti, Co, Pd, and combinations thereof. The substrate 202 is

then heated, which causes Ge to react with the metal where contacted. After the reaction, a layer of metal germanide is formed between the Ge-containing material and the metal. The unreacted metal is selectively removed through the use of an etchant that attacks the metal material but does not attack germanide.

(Ex. 1007, ¶[0030].)

131. Wann further discloses that, for the particular geometry for the facets of the strained material shown in the embodiment of figure 9, the conventional process can result in “triangular germanide” with “small-volume germanide on the strained material 226 [that] causes high contact resistance of S/D regions of the FinFET and thus degrades the device performance.” (*Id.*) Therefore, Wann discloses another technique for forming a “rectangular germanide to replace the triangular germanide.” (*Id.*, ¶[0031]; *see also id.*, ¶¶[0032]-[0042], FIGs. 10-13.) Like the conventional germanide formation, Wann’s “rectangular germanide” technique deposits metal on the strained material 226 (*Id.*, ¶[0037]), and then the substrate is heated to form germanide (*id.*, ¶[0038]). “In other words, the first metal layer 242 in contact with the strained material 226 is then transformed into a germanide by a thermal process,” where “the germanide 246 comprises NiGe, PtGe, TiGe₂, CoGe₂, or PdGe.” (*Id.*, ¶[0038].)

132. Therefore, Wann discloses the features recited in claim elements 13[f] and 13[g].

9. Claim 14

“The integrated circuit of claim 13, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

133. In my opinion, Wann discloses this limitation for the same reasons I discuss above for claim 2. (See my discussion above in section IX.D.2.)

E. Wann in Combination with Kuhn Discloses or Suggests the Features of Claim 12

1. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

134. As I discuss above in section IX.D.7, Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (See my discussion above in section IX.D.7; Ex. 1007, ¶[0009] (“The FinFET 200 refers to any fin-based, multi-gate transistor. ... **The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).**”) (emphasis added).) I have been asked to assume a scenario in which Wann does not disclose a “computing system” as recited in claim 12. Under such an assumption, a person of ordinary skill in the art would have been motivated to include Wann’s microprocessor in a computing system in order to give

it utility. Moreover, Kuhn discloses using non-planar transistors on integrated circuits in a computing system, and, in my opinion, a person of ordinary skill in the art would have had good reason to use Wann's transistor in a computing device as disclosed by Kuhn.

135. Like Wann, Kuhn discloses using non-planar transistors in microprocessors. (Ex. 1010, ¶[0039] (“One or more of the components shown in the system 600 may include one or more nanowire devices of the various embodiments included herein. For example, processor 610, or memory device 620, or at least a portion of I/O controller 650, or a combination of these components may include [] an integrated circuit package that includes at least one embodiment of the structures herein.”); Ex. 1007, ¶[0009]).) Kuhn discloses that the non-planar transistors can be used in integrated circuits included in computing systems. (Ex. 1010, ¶[0038] (“FIG. 6 shows a computer system according to an embodiment.”), ¶[0039] (“One or more of the components shown in system 600 may include one or more nanowire devices of the various embodiments included herein.”), ¶[0040]-[0041], FIG. 6.)

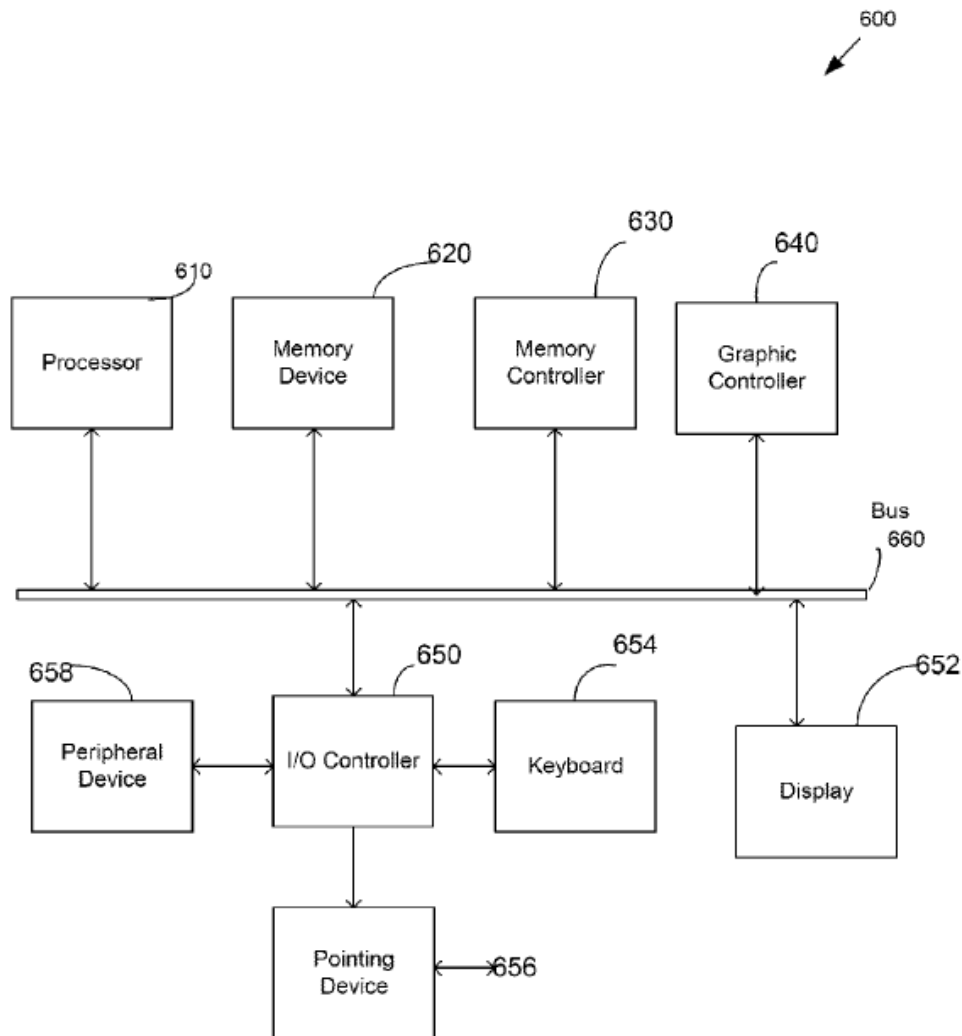


FIG. 6

(*Id.*, FIG. 6.)

136. In view of Kuhn and their knowledge of the state of the art, a person of ordinary skill in the art would have had good reason to implement a non-planar transistor like that disclosed by Wann in a computing device. Indeed, a person of

ordinary skill in the art would have known that transistors are often used in integrated circuit devices that are included in computing devices. Such a skilled person would have been motivated to include Wann’s transistor in a computing system in order to provide utility to the transistor, and, based on Kuhn’s disclosure and their knowledge, would have had a reasonable expectation of success.

F. Wann in Combination with Ching Discloses or Suggests the Features of Claims 11, 17, and 18

1. Claim 11

“The integrated circuit of claim 1, wherein the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons.”

137. In my opinion, Wann in combination with Ching discloses or suggests these features. As I discuss above in section IX.D.1, Wann discloses a FinFET that includes a “non-planar body” in the form of a fin extending from the substrate surface. (See my discussion above in section IX.D.1(b).) Wann does not explicitly disclose nanowires or nanoribbons, but Ching discloses a fin-based non-planar structure similar to that of Wann that uses nanowires, and, in view of Ching and their knowledge of the state of the art, a person of ordinary skill in the art would have good reason to implement a non-planar transistor like that disclosed by Wann using nanowires.

138. Ching, like Wann, discloses a fin-based transistor where a channel region separates epitaxially-formed source drain regions:

A transistor, such as a FinFET transistor, comprises a source region, a drain region, and a channel region between the source region and the drain region. The transistor comprises a gate region that controls the channel region to operate the transistor. The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.

(Ex. 1006, ¶[0001].)

Source and drain material is formed within the first source region 302 and the first drain region 304, such as through an epitaxial growth technique, to create a first source and a first drain for a first nanowire transistor. Other source regions, such as a second source region 306, and drain regions, such as a second drain region 308, are formed for other nanowire transistors that are to be formed for the semiconductor arrangement 250.

(*Id.*, ¶[0021]; *see also id.*, ¶[0019] (“In an example, the substrate 202 comprises silicon, and the substrate 202 is formed according to a FinFET arrangement

comprising one or more silicon fins separated by isolation structures 204, such as shallow trench isolation (STI).”)

139. Instead of a fin-shaped channel region that has a gate structure on the top and sides of the channel, Ching’s nanowire transistor includes multiple wires within the channel region, where gate dielectric and the gate electrode completely surround each nanowire in a “gate-all-around structure.” (*Id.*, ¶¶[0024], [0025]; *see also* Ex. 1011, ¶[0044] (“A non-planar architecture can be implemented, for instance, using FinFETs or nanowire configurations. A FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). ... Other types of FinFET configurations are also available ... A nanowire transistor (sometimes referred to as gate-all-around FET) is configured very similarly, but instead of a fin, a nanowire (e.g., silicon or SiGe or Ge nanowire) is used and the gate material generally surrounds the channel region on all sides.”).)

140. Ching’s device 500 with an epitaxially-grown source region and a drain region on either side of a channel region that includes nanowire channels 206, 210, and 214 for a nanowire transistor is shown in annotated figures 5 and 6 below. (Ex. 1006, ¶¶[0021]-[0023], [0030]-[0032].)

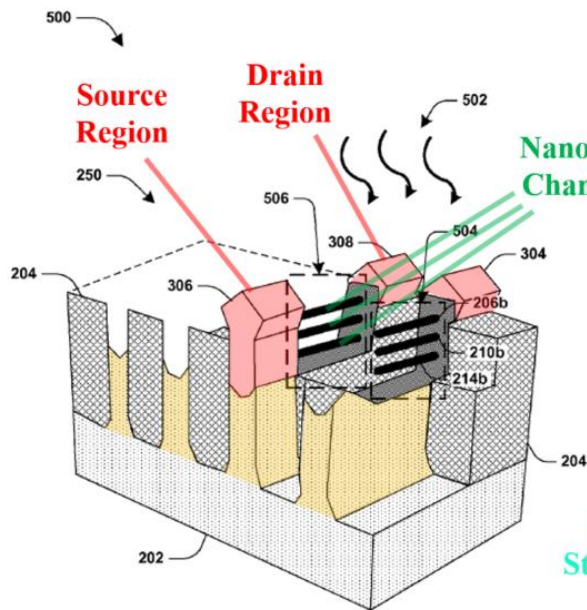


FIG. 5

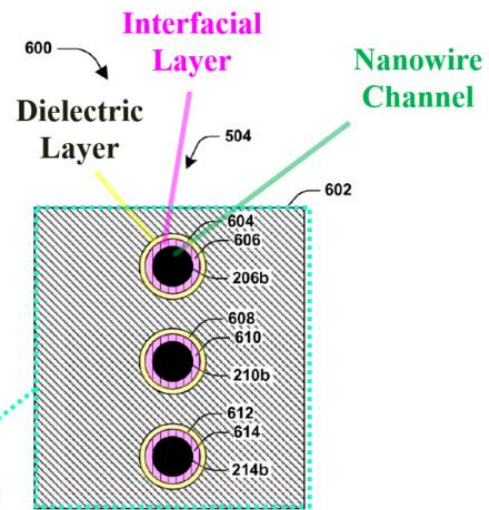


FIG. 6

(*Id.*, FIGs. 5, 6 (annotated).)

141. Ching discloses that having a gate-all-around structure like that shown for the nanowire transistors above increases gate control for the transistors. (*Id.*, ¶[0025] (“In an example, the first gate structure 602 is formed as a gate-all-around structure surrounding the germanium nanowire channels to increase gate control, as illustrated in embodiment 600 of FIG. 6.”); ¶[0001] (“The gate region can be formed around one or more surfaces of the channel region, which provides the gate region with increased control over the channel region because the transistor can be controlled by a 3D gate area, as opposed to being controlled merely by a 2D gate area associated with a 2D planar transistor.”); *see also* Ex. 1011, ¶[0044]

(“Depending on the particular design, nanowire transistors have, for instance, four effective gates.”).)

142. In my opinion, a person of ordinary skill in the art implementing a FinFET device like that disclosed by Wann would have looked to Ching, particularly because Wann and Ching are references in the same field and disclose fin-based devices with epitaxially grown source/drain regions on either side of a gate region. Having looked to Ching, such a skilled person would have had good reason to implement the channel region of a fin-based device like that of Wann such that it includes one or more nanowires like those disclosed by Ching.

143. As disclosed by Ching and known in the art, including nanowires in the channel region provides added gate control, where the gate-all-around aspect of nanowires provides even more control than the three-side gate structure for FinFETs like those disclosed by Wann. (Ex. 1006, ¶¶[0001], [0025]; Ex. 1010, ¶[0001] (“Nanowires used to fabricate devices provide improved short channel control.”), ¶[0024] (“Nanowire channel devices exhibit lower sub-threshold leakage due to short channel effect (SCE) reduction”; “[i]mplementation of [gate-all-around] GAA SiGe high mobility channel device...suppress[es] SCE effects” and “maximize[s] the electrostatic gate control to the channel”).) Moreover, nanowire-based transistors would have also allowed for reduced semiconductor chip size by stacking the transistor channels vertically. (Ex. 1010, ¶[0010] (“enable[ing] enhanced

isolation of channels from the substrate, mitigation of the capacitance associated with spacer-gap separation, and vertical architecture scaling with nanowires”), FIG. 1i.) Accordingly, in my opinion, a person of ordinary skill in the art would have been motivated to implement a nanowire-based channel region in place of a fin-shaped channel region when fabricating devices like those disclosed by Wann.

144. Indeed, non-planar nanowire devices were well-known in the art, and a person of ordinary skill in the art would have understood that structures and teachings related to fin-based non-planar devices like those disclosed by Wann are compatible with nanowire non-planar devices like those disclosed by Ching. (Ex. 1011, ¶[0044] (“A non-planar architecture can be implemented, for instance, using FinFETs or nanowire configurations.”); Ex. 1012, ¶[0024] (“the semiconductor structure 300 may include a first plurality of fins 102 ... formed from a semiconductor substrate”), ¶[0033] (describing a fin based device with high germanium concentration source/drain regions), ¶[0068] (“In another embodiment of the present invention, the method described above may be applicable to other semiconductor structures, such as nanowire FET devices. In this case, the gate structure 14 may enfold a nanowire channel located between a source-drain region.”); Ex. 1013, ¶[0042] (“Although the portions of the structures described herein take the form of a fin, it will be understood that the different doping levels provided to threshold voltage control regions and carrier regions can be applied to

other geometries such as a ‘gate-all-around’ structure (such as a nanowire structure).”); Ex. 1010, ¶[0013] (“In an embodiment, the fin structures 107 may comprise a dual channel portion of a gate all around (GAA) nanowire device,” where “[t]he number of channels in the device will depend on the numbers of layers in the fin structures 107.”), ¶[0024] (“Embodiments herein enable the fabrication of self-aligned gate-all-around (GAA) silicon and silicon germanium channel transistor structures and devices.”).)

145. Indeed, Wann states that “FinFET 200 refers to any fin-based, multi-gate transistor” and that “[o]ther transistor structures and analogous structures are within the contemplated scope of the disclosure,” thereby supporting the understanding the Wann’s teachings are compatible with nanowire architectures. (Ex. 1007, ¶[0009]; section VI.C.)

146. As a person of ordinary skill in the art would have appreciated, using nanowires for the channel region as disclosed by Ching as opposed to a three-sided single portion of fin material as disclosed by Wann would have been the simple substitution of one type of transistor channel (Ching’s nanowires) for another (Wann’s fin portion) in a similar device in a predictable manner to produce the expected result of a functional non-planar transistor with added gate control.

147. Based on their knowledge of such well-known nanowires and Ching’s detailed disclosure of formation of nanowires in a device similar to that disclosed by

Wann, a person of ordinary skill in the art would have had a reasonable likelihood of success in implementing a nanowire channel transistor based on the teachings of Wann and Ching. Therefore, in my opinion, the Wann-Ching combination discloses or suggests using nanowires with gate-all-around channel regions (“the non-planar body includes one or more nanowires and/or nanoribbons, and the gate structure wraps around the one or more nanowires and/or nanoribbons”) in a non-planar device like that I discuss above in section IX.D.1. In other words, other than having a different channel region (i.e., nanowires instead of a fin), the transistor has a structure like that discussed above for claim 1 in section IX.D.1.

148. I have been asked to assume a scenario in which the Wann-Ching combination is limited to a PMOS device that uses germanium nanowires such that the nanowires do not present “a surface that consists essentially of silicon” with which the first and second portions of the source/drain regions are “in direct contact.” Under such an assumption the first and second portions of the source/drain regions of the Wann-Ching combination are in direct contact with the underlying lower portion of the fin that, as I discuss above in sections IX.D.1(d)-(e) “consists essentially of silicon.” (See my discussion above in sections IX.D.1(d)-(e).) As I noted above, in the Wann-Ching combination, the channel portion of the fin as disclosed by Wann is replaced with nanowires, while the fin structure upon which

the source/drain regions are formed remains the same as in a non-nanowire FinFET as disclosed by Wann.

2. Claim 17

a) “An integrated circuit, comprising:”

149. I understand that “[a]n integrated circuit, comprising” is the preamble to claim 17 of the ’334 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Wann discloses “an integrated circuit” for the same reasons I discuss above for claim element 1[a]. (See my discussion above in section IX.D.1(a).)

b) “a nanowire or nanoribbon comprising semiconductor material;”

150. In my opinion, the Wann-Ching combination discloses or suggests this claim limitation. As I discuss above for claim 11, the Wann-Ching combination discloses or suggests a non-planar transistor that includes a nanowire. (See my discussion above in section IX.F.1.) Ching further discloses that the nanowires can be made of silicon and germanium, both of which constitute “semiconductor material.” (Ex. 1006, Title (“Silicon and Germanium Nanowire Formation”), Abstract (“germanium nanowire channels”) (“silicon nanowire channels”), ¶¶[0014]-[0015], [0018], [0022]-[0025]; see also Ex. 1011, ¶[0044] (“A nanowire transistor (sometimes referred to as gate-all-around FET) is configured very

similarly, but instead of a fin, a nanowire (e.g., silicon or SiGe or Ge nanowire) is used and the gate material generally surrounds the channel region on all sides.”.)

c) “a gate structure wrapped around the nanowire or nanoribbon;”

151. In my opinion, the Wann-Ching combination discloses or suggests this claim limitation. For example, as I discuss above for claim 11, the Wann-Ching combination discloses or suggests a non-planar transistor that includes a nanowire with a gate structure that is a “gate-all-around” structure that is wrapped around the nanowire. (See my discussion above in section IX.F.1)

d) “a source structure to one side of the gate structure and abutting the nanowire or nanoribbon, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon;”

e) a drain structure to an opposite side of the gate structure and abutting the nanowire or nanoribbon, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;”

152. In my opinion, the Wann-Ching combination discloses or suggests these features. As I discuss above for claim 11, the Wann-Ching combination includes a nanowire channel region as opposed to a fin channel region. (See my

discussion above in sections IX.F.1.) Therefore, for the same reasons I discuss above for claim elements 13[d]-[e], the Wann-Ching combination discloses or suggests a “source structure” on one side of the gate structure surrounding the channel region that includes the nanoribbon and a “drain structure” on the opposite side of the gate structure, where the source and drain structures abut the nanoribbon in order to form a transistor device. (See my discussion above in sections IX.F.1, IX.D.8(d)-(e).) Moreover, for the same reasons discussed above for the “source structure” and “drain structure” in the context Wann and claim 13, the Wann-Ching combination discloses or suggests that the source and drain structures include a first portion and a second portion having germanium at a concentration of at least 50 atomic percent throughout as recited in claim 17. (See my discussion above in sections IX.F.1, IX.D.8(d)-(e).) As I discuss above for claim 11 and claim elements 13[d] and 13[e], the first/second portions of the source/drain structures are in direct contact with the lower portion of the fin underlying the source/drain structures, where the fin is made of silicon. (See my discussion above in sections IX.F.1, IX.D.8(d)-(e).)

- f) **“a first contact structure on the first portion of the source structure and including a metal-germanide; and;”**
- g) **“a second contact structure on the second portion of the drain structure and including a metal-germanide.”**

153. In my opinion, the Wann-Ching combination discloses or suggests these limitations for the same reasons I discuss above that show Wann discloses the features included in claim elements 13[f] and 13[g]. (See my discussion above in sections IX.D.8(f)-(g).)

3. Claim 18

“The integrated circuit of claim 17, wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.”

154. In my opinion, the Wann-Ching combination discloses or suggests these features. As I discuss above for claim elements 17[d]-[e] and 13[d]-[e], the “first portion” and “second portion” of the source/drain structures are in direct contact with the underlying lower portion of the fin which is part of the substrate, which can be a “bulk silicon,” or silicon on insulator substrate. (See my discussion above in sections IX.F.2(d)-(e), IX.D.8(d)-(e), IX.D.2; Ex. 1007, ¶¶[0002], [0011], [0015], FIGs. 3A, 3B.) Therefore, the “surface,” which corresponds to the upper surface of the lower portion of the fin is a surface of “a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator” as claimed. (Ex. 1001, 5:35-40; *see also* Ex. 1015, 103, 115; Ex. 1017, 93-97.)

G. Wann in Combination with Liao Discloses or Suggests the Features of Claims 1, 2, 5-7, 10, and 12

1. Claims 1, 2, 10, and 12

155. In my opinion, Wann in view of Liao discloses or suggests the features of claims 1, 2, 10, and 12. As I discuss above for claim elements 1[d] and 1[e], Wann discloses one embodiment in which the strained material of the source/drain regions of the FinFET is germanium (Ge), and therefore Wann discloses the source and drain regions that include portions that have at least 50 percent germanium as recited in claim 1. (See my discussion above in sections IX.D.1(d)-(e).) Wann discloses another embodiment where the strained material is silicon-germanium (SiGe), but does not explicitly disclose that the SiGe includes at least 50 percent germanium. (Ex. 1007, ¶[0025], (“In some embodiments, the strained material 226 comprises Ge or SiGe for a p-type FinFET.”).) Liao, however, discloses forming epitaxial portions of source/drain regions in a similar FinFET device using SiGe where the germanium concentration is greater than 50 percent, and, in view of Liao, a person of ordinary skill in the art would have had good reason to form the strained material of the source/drain regions in the device like that disclosed by Wann using SiGe where the germanium concentration is greater than 50 percent.

156. Liao is in the same or similar field as Wann. For example, like Wann, Liao discloses forming a FinFET device, where the FinFET device corresponds to Liao’s fifth embodiment:

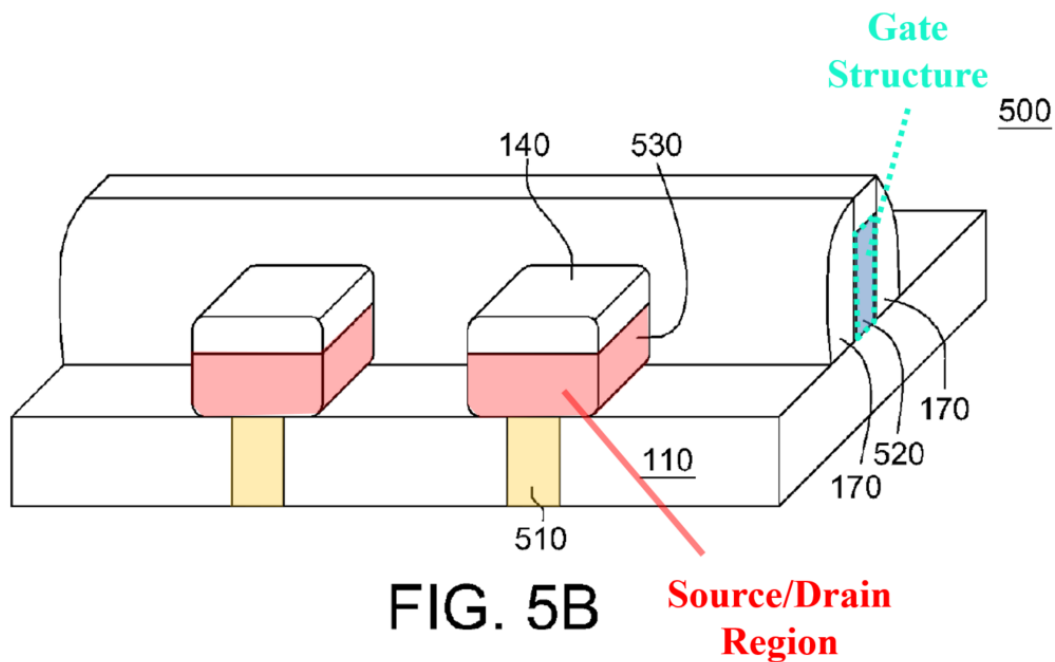
Referring to FIGS. 5A-5B, FIGS 5A-5B illustrate a manufacturing method of a semiconductor device 500 according to a fifth embodiment of the disclosure. The elements in the first to fifth embodiments sharing the same labeling are the same elements, and the description of which are as aforementioned.

(Ex. 1008, ¶[0046].)

In an embodiment, the semiconductor device 500 is such as a fin field-effect transistor (FinFET). After an ion implantation is performed to the epitaxial structure 530, the regions with the p-type or n-type dopants of the epitaxial structure 530 located on two sides of the gate structure 520 may serve as source/drain regions.

(*Id.*, ¶[0050].)

157. Thus, a person of ordinary skill in the art would have had reason to consider the teachings of Liao when implementing Wann's device. Liao's FinFET device 500 with source/drain regions 530 on either side of a gate structure 520 is shown in annotated figure 5B below.



(*Id.*, FIG. 5B (annotated).)

158. Liao discloses that epitaxial structure 530 corresponding to the source/drain regions comprises SiGe, where “the Ge concentration in the epitaxial structure 530 is equal to or higher than 45%, preferably up to 55-60%.” (Ex. 1008, ¶[0047]; *see also id.*, [0017] (disclosing the same for a SiGe epitaxial structure 130 discussed with reference to Figure 1B). Liao also discloses another embodiment where the epitaxial structure is SiGe with a germanium content of at least 45%, where, in the example for that embodiment, the epitaxial structure includes two layers, a first layer that includes “about 55%” germanium concentration and the second layer that includes “about 60%” germanium. (*Id.*, ¶[0042].)

159. Liao further discloses that “the higher the Ge concentration in the epitaxial structure is, the higher the driving current of the device will be, and thus the power is higher, such that the overall performance of the device is improved.” (*Id.*, ¶¶[0018]-[0019], [0022]; *see also id.*, ¶¶[0004], [0006] (“superior device performance”); Ex. 1009, ¶[0042] (“As previously described, this stress increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current.”), ¶[0043] (“In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel) ...”); Ex. 1005, ¶[0044] (“Forming the source and drain epi-tips in relatively close proximity to the channel region also imparts a larger hydrostatic stress on the channel. This stress increases the strain within the channel, thereby increasing mobility in the channel and increasing drive current. This stress can be further amplified by increasing the germanium concentration of the source and drain epi-tips.”).)

160. A person of ordinary skill in the art implementing a FinFET device like that disclosed by Wann would have looked to Liao for guidance, particularly because Wann and Liao are references in the same field and both disclose FinFET devices with source/drain regions that include epitaxial regions of silicon-germanium

(SiGe). Having looked to Liao, such a skilled person would have had good reason to implement the strained material in a device like that disclosed by Wann such that it includes at least 50% germanium.

161. Wann discloses using SiGe strained material in the source/drain regions, but Wann does not disclose specific details regarding the percentage of germanium included in the SiGe material used. (Ex. 1007, ¶[0025].) Liao, on the other hand, discloses using silicon-germanium as the epitaxial portions (e.g. strained material) of the source/drain regions, where Liao gives specific examples of how much germanium should be included in the silicon-germanium on a percentage basis. For example, Liao discloses using silicon-germanium with a germanium percentage of at least 45%, and more preferably of about 55-60%. (Ex. 1008, ¶¶[0004]-[0005], [0047].) Therefore, a person of ordinary skill in the art would have had good reason to look to Liao and would have had good reason, in view of Liao and the knowledge of a person of ordinary skill in the art, to implement the SiGe strained material in the source/drain regions as disclosed by Wann using at least 50% germanium as recited in claim 1. Wann does not provide any example germanium-content percentages for the SiGe material, but Liao provides such examples, thereby informing a person of ordinary skill in the art as to specific percentages of germanium that are appropriate for strained material used in the source/drain formation in a transistor like that disclosed by each of Wann and Liao.

162. Moreover, Liao further discloses that having a germanium percentage of at least 45% and more preferably, about 55-60%, results in higher speed operation for the FinFET device. (*Id.*, ¶¶[0018]-[0019], [0022]; *see also id.*, ¶¶[0004], [0006].) Therefore, a person of ordinary skill in the art would have been motivated to include 55-60% germanium (“the first/second portion including germanium at a concentration of at least 50 atomic percent throughout the first/second portion”) in order to achieve a FinFET with higher speed operation in comparison to a FinFET with a lower percentage of germanium in the source/drain regions.

163. A person of ordinary skill in the art would have appreciated that using 55-60% germanium SiGe in a FinFET like that disclosed by Wann would have been nothing more than the simple substitution of one known element (Liao’s germanium content of 55-60% in SiGe portions of the source/drain regions) for another (Wann’s unknown germanium content in SiGe portions of source/drain regions) to obtain the predictable result of a functional FinFET device with high-Ge percentage SiGe portions of source/drain regions. Moreover, such a skilled person would also have appreciated that using 55-60% germanium SiGe material as explicitly disclosed by Liao in the SiGe portions of source/drain regions of a FinFET as disclosed by Wann would simply have been the use of a known technique (55-60% germanium as disclosed by Liao) in a similar device (Wann’s FinFET) to realize the advantage of better performance.

164. Moreover, using a germanium concentration of at least 50% in the strained material of the SiGe source/drain region would have been a matter of routine optimization of a result-effective variable (the percentage of germanium), well within the understanding and technical ability of a person of ordinary skill in the art. As I discuss above, Liao discloses SiGe source/drain regions that include germanium concentrations of “equal to or higher than 45%, preferably up to 55-60%.” (Ex. 1008, ¶[0047].) Therefore, Liao’s disclosed range of 45% or greater overlaps range of 50% or greater recited in claim 1.

165. The percentage of germanium in the SiGe portions of the source/drain regions is a result-effective variable because the percentage of germanium was known to effect the strain stress generated in the channel region of the semiconductor device, which in turn can improve the performance of the device. (Ex. 1008, ¶[0004] (“Since the lattice constant of the epitaxial SiGe layer is larger than that of a silicon substrate, a strain stress generated to the channel region of the semiconductor device, such as a metal-oxide semiconductor (MOS) transistor device, may efficiently improve the device performance.”), ¶[0005] (“It is well-known that the strain stress is increased as the Ge concentration in the epitaxial SiGe layer is increased.”); Ex. 1005, ¶¶[0013], [0023], [0044]; Ex. 1001, 3:31-33 (“In embodiments, where the SiGe layer is functional, the SiGe layer may comprise 30-70% Ge, in some cases (e.g., to maximize strain for performance reasons).”), 7:46-49.) The ’334 patent does

not provide any indication as to why the lower end of the range (50%) is specified and does not provide describe the claimed range as being critical or producing an unexpected result. A person of ordinary skill in the art would have recognized that the specified range, which includes a germanium concentration of greater than 50%, could be readily derived through routine optimization.

166. Based on their knowledge and Liao's disclosure of using at least 45% and, more preferably, 55-60% germanium SiGe in a FinFET device similar to that of Wann, a person of ordinary skill in the art would have had a reasonable likelihood of success. Indeed, Liao discloses how to form such SiGe portion of source/drain regions in a similar device structure to that of Wann, and a person of ordinary skill in the art would have known how to, and been able to implement, any modifications to the teachings of Wann in order to implement the SiGe portions of the source/drain regions using at least 50% germanium SiGe as claimed.

167. Indeed, a person of ordinary skill in the art would have understood that Wann's disclosure of using germanium alone for the strained material of the source/drain regions demonstrates that source/drain regions made of SiGe with a high percentage of germanium are compatible with Wann's device structure. Such a skilled person would also have recognized that there is nothing particularly difficult about changing the percentage of germanium in the SiGe portions of the source/drain regions of Wann.

168. Therefore, the Wann-Liao combination discloses or suggests claim features 1[d] and 1[e] for the reasons I discuss above for the germanium strained material in the source/drain regions presented in sections IX.D.1(d)-(e), where, instead of the germanium strained material, silicon-germanium (SiGe) strained material in the source/drain regions with a germanium content of at least 50% as disclosed or suggested by the Wann-Liao combination is included. The remaining features of claims 1, 2, 10, and 12 are disclosed or suggested by the Wann-Liao combination for the same reasons I discuss above in sections IX.D.1-2 and IX.D.6-7.

2. Claim 5

“The integrated circuit of claim 1, wherein the first and second portions further include one or both of silicon and tin.”

169. In my opinion, the Wann-Liao combination I discuss immediately above in section IX.G.1 discloses or suggests this limitation. For example, as I discuss above for claim elements 1[d] and 1[e], the Wann-Liao combination discloses or suggests SiGe strained material (“first/second portions”) in the source/drain regions with at least 50% germanium. (See my discussion above in section IX.G.1.) Therefore, the strained material (“first/second portions”) include silicon (“one or both of silicon and tin”) and germanium as recited in claim 5.

3. Claim 6

“The integrated circuit of claim 1, wherein the first and second portions include a p-type dopant.”

170. As I discuss above in section IX.D.3, Wann discloses that the strained material (“first/second portions”) “comprises Ge or SiGe for a p-type FinFET,” and a person of ordinary skill in the art would have understood that the strained material of S/D regions 232 include p-type dopants for a p-type FinFET. (See my discussion above in section IX.D.3; Ex. 1007, ¶[0025].) I have been asked to assume a scenario in which Wann does not explicitly disclose that the “first and second portions” of the S/D regions 232 “include a p-type dopant.” Under such an assumption, it is my opinion that the Wann-Liao combination discloses or suggests this limitation.

171. For example, Liao discloses doping the epitaxial portions of source/drain regions with boron, which is a p-type dopant, and a person of ordinary skill in the art would have had good reason to use boron to dope the strained material in the source/drain regions of Wann using boron in view the disclosure of Wann, Liao, and such a skilled person’s knowledge of p-type devices and dopants. (Ex. 1008, ¶[0048] (“the epitaxial structure 530 may further be doped with boron.”), ¶[0050] (“the regions with the p-type or n-type dopants of the epitaxial structure 530 located on two sides of the gate structure 520 may serve as source/drain regions.”).) As a person of ordinary skill in the art would have understood, p-type MOS transistors include dopants in the source/drain regions to facilitate the functioning of

the transistor. (Ex. 1017, 15-17; Ex. 1015, 115-117.) Therefore, such a skilled person, who also would have been aware of commonly-used p-type dopants such as boron, would have had good reason to include such a p-type dopant in the strained material (“first/second portions”) of the source/drain regions.

4. Claim 7

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is undoped.”

172. As I discuss above in section IX.D.4, Wann discloses that the “surface that consists essentially of silicon” is part of the silicon substrate 202, which can be a “crystalline silicon substrate (e.g., wafer)” and therefore is undoped. (See my discussion above in section IX.D.4.). I have been asked to assume a scenario in which Wann does not explicitly disclose that the crystalline silicon substrate is undoped. Under such an assumption, it is my opinion that the Wann-Liao combination discloses or suggests this limitation.

173. Wann does not explicitly indicate that the silicon wafer is doped, and therefore, to the extent the wafer being undoped is not explicitly disclosed, a person of ordinary skill in the art would have had good reason to leave the silicon wafer undoped. Wann’s disclosure does not indicate the surface of the silicon wafer is doped, and leaving it undoped would have eliminated the need for a doping step. Therefore, a person of ordinary skill in the art would have been motivated to leave the silicon wafer undoped in order to reduce the number of process steps required.

Moreover, leaving the silicon surface undoped would have been one of two choices for a person of ordinary skill in the art, and therefore such a skilled person would have been motivated to choose an undoped wafer as it is one of a finite number of predictable options (doped or undoped).

H. Wann in Combination with Liao and Kuhn Discloses or Suggests the Features of Claim 12

1. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

174. As I discuss above in section IX.D.7, Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (See my discussion above in section IX.D.7; Ex. 1007, ¶[0009] (“The FinFET 200 refers to any fin-based, multi-gate transistor. ... **The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).**”) (emphasis added).) I have been asked to assume a scenario in which the Wann-Liao combination discussed in section IX.G does not disclose or suggest a “computing system” as recited in claim 12. Under such an assumption, Kuhn discloses using non-planar transistors on integrated circuits in a computing system, and, in my opinion, a person of ordinary skill in the art would have had good reason to use the transistor of the Wann-Liao combination in a

computing device as disclosed by Kuhn for the same reasons I discuss above in section IX.E.

I. Wann in Combination with Liao and Ching Discloses or Suggests the Features of Claim 11

175. In my opinion, Wann in combination with Liao and Ching discloses or suggests all of the features of claim 11 of the '334 patent.

1. Claim 11

176. Wann in view of Liao and Ching discloses or suggests the features of claim 11. As I discuss above in section IX.G.1, it is my opinion that a person of ordinary skill in the art would have had good reason to use SiGe with a germanium concentration of at least 50% in non-planar devices as disclosed or suggested by the Wann-Liao combination. (See my discussion above in section IX.G.1.) As I discuss above in section IX.F.1, a person of ordinary skill in the art would have had good reason, in view of Ching, to include nanowires in the non-planar devices of Wann such that the Wann-Ching combination discloses or suggests the features of claims 11. (See my discussion above in section IX.F.1.)

177. For the same reasons I discuss above in section IX.F.1, a person of ordinary skill in the art would have had good reason to use nanowires, as disclosed by Ching, in the non-planar device of the Wann-Liao combination. (See my discussion above in section IX.F.1.) The use of SiGe with a germanium concentration of more than 50% for the strained material in the source/drain regions

of the non-planar transistor does not impact the use of nanowires in the channel region. Therefore, the Wann-Liao-Ching combination discloses or suggests the features of claim 11 for the same reasons I discuss above in section IX.F, where, instead of germanium strained material as discussed in section IX.D, the non-planar devices have SiGe strained material as discussed in section IX.G.1. (See my discussion above in sections IX.F, IX.G.1)

J. Wann in Combination with Cappellani Discloses or Suggests the Features of Claims 1, 2, 5-7, 10, and 12

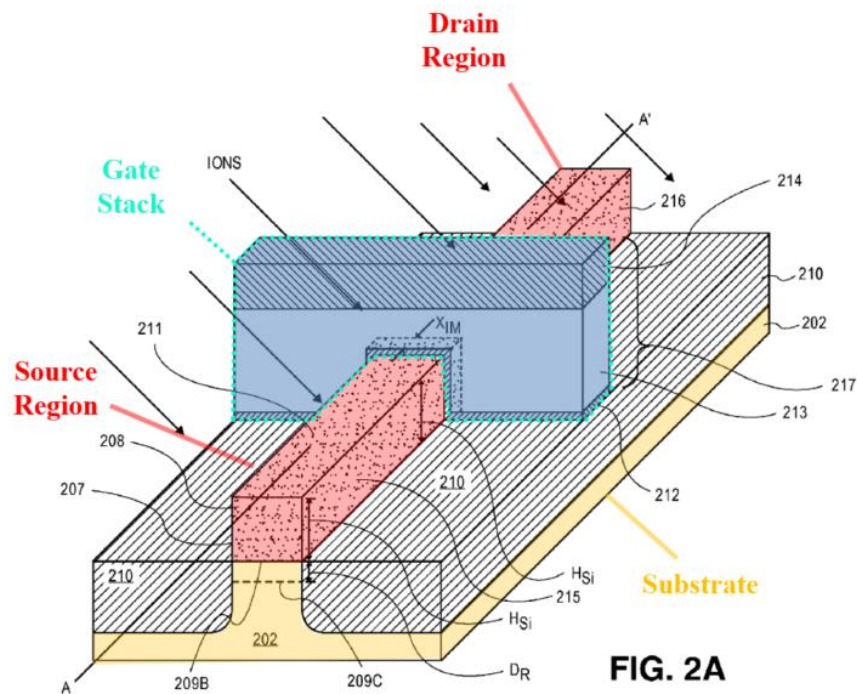
178. In my opinion, Wann in combination with Cappellani discloses or suggests all of the features of claims 1, 2, 5-7, 10, and 12 of the '334 patent.

1. Claims 1, 2, 10, and 12

179. In my opinion, Wann in view of Cappellani discloses or suggests the features of claims 1, 2, 10, and 12. As I discuss above in section IX.G.1, Wann discloses an embodiment where the strained material (“first/second portions”) of the source/drain regions is silicon-germanium (SiGe), but does not explicitly disclose that the strained material has at least 50 percent germanium as recited in claim 1. (Ex. 1007, ¶[0025], (“In some embodiments, the strained material 226 comprises Ge or SiGe for a p-type FinFET.”); see my discussion above in sections IX.D.1(d)-(e), IX.G.1.) Cappellani, however, discloses forming epitaxial regions in source/drain regions in a similar FinFET device using SiGe where the germanium concentration is greater than 50 percent, and, in view of Cappellani, a person of ordinary skill in

the art would have had good reason to form the epitaxial regions (i.e., strained material) in the device like that disclosed by Wann using SiGe where the germanium concentration is greater than or equal to 50 percent.

180. Like Wann, Cappellani discloses forming a FinFET device that includes source/drain regions. (Ex. 1009, ¶[0022] (“Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’).”).) Annotated figure 2A of Cappellani below shows the FinFET at an early stage of fabrication. (*Id.*, ¶¶[0007], [0026].)



(*Id.*, FIG. 2A (annotated).)

181. Cappellani discloses doping the source/drain regions of the fin portion of the silicon substrate in order to allow for very accurate etching of the doped

regions to form cavities for subsequent formation of regrown source/drain regions. (Ex. 1009, ¶¶[0027], [0030]-[0031], [0033]-[0035], FIGs. 2A-B, 4A-C.) Cappellani discloses that “[t]he dopant used in the ion implantation operation 106 is chosen based on its ability to increase the etch rate of the semiconductor fin material in which it is implanted.” (*Id.*, ¶[0030].) After doping, “an etch process is performed at operation 110 to etch the doped fin region.” (*Id.*, ¶[0033].) Cappellani discloses that by using a selective etch, the desired structure for the source/drain regions of the FinFET can be achieved:

The etch operation 110 uses etchants that complements the dopant used in the ion implantation process to increase the etch rate of the doped regions. This enables the etching process to remove the doped fin region at a faster rate than the remainder of the undoped (or more lightly doped) substrate. As such, with an appropriate increase in etch rate, the etching process can selectively remove substantially the entire semiconductor fin (i.e., entire height H_{si} over the entire channel width W_{si} , as shown in FIG. 3A) and retain only the channel region with good profile and depth control. This includes portions of the doped regions that undercut the gate stack space and the gate dielectric, thereby defining a self-aligned source/drain fin extensions of the multi-gate transistor.

(*Id.*, ¶[0033].)

182. Cappellani further discloses that after selectively etching to form the cavities for the source/drain regions, epitaxial deposition is used to form the source/drain regions. (Ex. 1009, ¶[0041] (“The epitaxial deposition operation 114 therefore regrows source/drain regions and source/drain extensions in one process.”).) Cappellani discloses the stress on the channel region in the resulting FinFET “increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current.” (*Id.*, ¶[0042]-[0043].) Such strain can be imparted on the channel by using a silicon germanium alloy as the material for the regrown source/drain regions:

In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel)

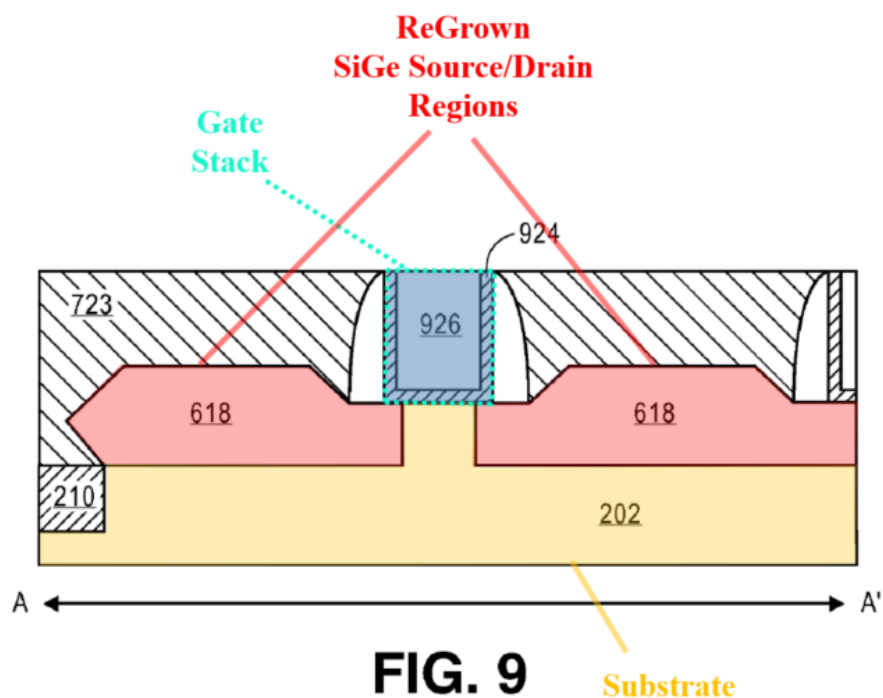
(*Id.*, ¶[0043].)

For one PMOS transistor embodiment, the regrown source/drain fin 618 may be filled with silicon germanium. The silicon germanium may be epitaxially deposited. The germanium concentration may range from 10 atomic % to 80 atomic %.

(*Id.*, ¶[0045]; *see also id.*, ¶[0050] (“Accordingly, a multi-gate transistor with self-aligned epitaxially regrown source/drain regions has been disclosed that reduce the

overall resistance of the multi-gate transistor and increase channel strain due to increased doped silicon volume (e.g., boron doped silicon germanium volume) combined with reduced channel silicon volume.”.)

183. Annotated figure 9 below shows the regrown SiGe source/drain regions in Cappellani’s FinFET. (Ex. 1009, ¶[0048], FIG. 9.)



(*Id.*, FIG. 9 (annotated).)

184. A person of ordinary skill in the art implementing a FinFET device like that disclosed by Wann would have looked to Cappellani for guidance, particularly because Wann and Cappellani are references in the same field and disclose FinFET devices with epitaxially deposited silicon-germanium in the source/drain regions. Having looked to Cappellani, such a person of ordinary skill in the art would have

had good reason to implement the strained material in the SiGe source/drain regions in a device like that disclosed by Wann such that it includes at least 50% germanium as recited in claim 1, and as disclosed by Cappellani, for the same reasons I discuss above for the Wann-Liao combination. (See my discussion above in section IX.G.1.)

185. While Wann discloses using SiGe strained material, Wann does not disclose specific details regarding the percentage of germanium included in the SiGe material. (Ex. 1007, ¶[0025].) Cappellani, however, discloses using SiGe with a germanium percentage 10-80%. (Ex. 1009, ¶¶[0042]-[0043], [0045].) Therefore, a person of ordinary skill in the art would have had good reason to look to Cappellani and would have had good reason, in view of Cappellani and the knowledge of a person of ordinary skill in the art, to implement the strained material (“first/second portions”) as disclosed by Wann using at least 50% germanium as recited in claim 1.

186. As a person of ordinary skill in the art would have appreciated, using SiGe material having a germanium concentration of greater than 50% for the strained material as disclosed by Cappellani would have simply been the use of known material in a similar device to obtain a predictable result. Moreover, as I discuss above in section IX.G.1, using a germanium concentration of at least 50% in SiGe strained material portions of the source/drain region would have been a matter of routine optimization of a result-effective variable. (See my discussion above in

section IX.G.1.) Cappellani discloses SiGe epitaxial portions of source/drain regions that include germanium concentrations 10-80%. (Ex. 1009, ¶[0047].) Thus, Cappellani's disclosed range of 10-80% overlaps the claimed range of 50% or greater.

187. As I also discuss above in section IX.G.1, the percentage of germanium in the SiGe strained material is a result-effective variable because the percentage of germanium was known to effect the strain stress generated in the channel region of the semiconductor device, which in turn can improve the performance of the device. (See my discussion above in section IX.G.1; Ex. 1008, ¶[0004] ("Since the lattice constant of the epitaxial SiGe layer is larger than that of a silicon substrate, a strain stress generated to the channel region of the semiconductor device, such as a metal-oxide semiconductor (MOS) transistor device, may efficiently improve the device performance."), ¶[0005] ("It is well-known that the strain stress is increased as the Ge concentration in the epitaxial SiGe layer is increased."); Ex. 1009, ¶[0043] ("In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel)"); Ex. 1005, ¶[0044] ("Forming the source and drain epi-tips in relatively close proximity to the channel region also imparts a larger hydrostatic stress on the channel. This stress

increases the strain within the channel, thereby increasing mobility in the channel and increasing drive current. This stress can be further amplified by increasing the germanium concentration of the source and drain epi-tips.”); Ex. 1001, 3:31-33 (“In embodiments, where the SiGe layer is functional, the SiGe layer may comprise 30-70% Ge, in some cases (e.g., to maximize strain for performance reasons).”), 7:46-49.) The ’334 patent does not provide any indication as to why the lower end of the range (50%) is specified and does not provide describe the claimed range as being critical or producing an unexpected result. A person of ordinary skill in the art would have recognized that the specified range, which includes a germanium concentration of greater than 50%, could be readily derived through routine optimization.

188. Based on their knowledge and Cappellani’s disclosure of using 10-80% germanium SiGe in a FinFET device similar to that of Wann, a person of ordinary skill in the art would have had a reasonable likelihood of success. Cappellani discloses how to form such SiGe strained material (“first/second portions”) in a similar device structure to that of Wann, and a person of ordinary skill in the art would have known how to, and been able to implement, any modifications to the teachings of Wann in order to implement the strained material portions using at least 50% germanium SiGe as claimed.

189. Indeed, a person of ordinary skill in the art would have understood that Wann’s disclosure of using germanium alone for the strained material portions of

the source/drain regions demonstrates that strained material portions made of SiGe with a high percentage of germanium is compatible with Wann's device structure. Such a skilled person would also have recognized that there is nothing particularly difficult about changing the percentage of germanium in the SiGe strained material portions of the source/drain regions of Wann.

190. Therefore, the Wann-Cappellani combination discloses or suggests claim features 1[d] and 1[e] for the reasons I discuss above for the germanium strained material portions presented in sections IX.D.1(d)-(e), where, instead of the germanium strained material portions, silicon-germanium (SiGe) strained material portions of the source/drain regions having a germanium content of at least 50% as disclosed or suggested by the Wann-Cappellani combination are included. The remaining features of claims 1, 2, 10, and 12 are disclosed or suggested by the Wann-Cappellani combination for the same reasons I discuss above in sections IX.D.1-2 and IX.D.6-7.

2. Claim 5

“The integrated circuit of claim 1, wherein the first and second portions further include one or both of silicon and tin.”

191. In my opinion, the Wann-Cappellani combination I discuss immediately above discloses or suggests this limitation. For example, as I discuss above for claim elements 1[d] and 1[e], the Wann-Cappellani combination discloses

or suggests SiGe strained material (“first/second portions”) in the source/drain regions with at least 50% germanium. (See my discussion above in section IX.J.1.) Therefore, the silicon-germanium portions include silicon (“one or both of silicon and tin”) and germanium as recited in claim 5.

3. Claim 6

“The integrated circuit of claim 1, wherein the first and second portions include a p-type dopant.”

192. As I discuss above in section IX.D.3, Wann discloses that the strained material (“first/second portions”) “comprises Ge or SiGe for a p-type FinFET,” and a person of ordinary skill in the art would have understood that the “first and second portions” of S/D regions 232 include p-type dopants for a p-type FinFET. (See my discussion above in section IX.D.3; Ex. 1007, ¶[0025].) I have been asked to assume a scenario in which Wann does not explicitly disclose that the strained material portions of the S/D regions 232 “include a p-type dopant.” Under such an assumption, it is my opinion that the Wann-Cappellani combination discloses or suggests this limitation.

193. For example, Cappellani discloses doping the epitaxial portions of source/drain regions for a PMOS (p-type) FinFET with boron, which is a p-type dopant:

In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may

impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel)

(Ex. 1009, ¶[0043].)

For one PMOS transistor embodiment, the regrown source/drain fin 618 may be filled with silicon germanium. The silicon germanium may be epitaxially deposited. The germanium concentration may range from 10 atomic % to 80 atomic %. In further implementations, the silicon germanium may be further doped in situ with boron. The boron concentration may range from $2 \times 10^{19}/\text{cm}^3$ to $2 \times 10^{21}/\text{cm}^3$.

(Ex. 1009, ¶[0045]; *see also id.*, ¶[0050] (“Accordingly, a multi-gate transistor with self-aligned epitaxially regrown source/drain regions has been disclosed that reduce the overall resistance of the multi-gate transistor and increase channel strain due to increased doped silicon volume (e.g., boron doped silicon germanium volume) combined with reduced channel silicon volume.”).)

194. In view of Cappellani’s disclosure of doping the epitaxial portions of source/drain regions with boron for a PMOS device, a person of ordinary skill in the art would have had good reason to use boron (“a p-type dopant”) to dope the strained material in the source/drain regions of the p-type FinFET according to the Wann-Cappellani combination. As a person of ordinary skill in the art would have

understood, p-type MOS transistors include dopants in the source/drain regions to facilitate the functioning of the transistor. (Ex. 1017, 15-17; Ex. 1015, 115-117.) Therefore, such a skilled person, who also would have been aware of commonly-used p-type dopants such as boron, would have had good reason to include such a p-type dopant in the strained material 226 (“first/second portions”) included in the source/drain regions 223.

4. Claim 7

“The integrated circuit of claim 1, wherein the surface that consists essentially of silicon is undoped.”

195. As I discuss above in section IX.D.4, Wann discloses that the “surface that consists essentially of silicon” is part of the silicon substrate 202, which can be a “crystalline silicon substrate (e.g., wafer)” and therefore is undoped. (See my discussion above in section IX.D.4.). I have been asked to assume a scenario in which Wann does not explicitly disclose that the crystalline silicon substrate is undoped. Under such an assumption, it is my opinion that the Wann-Cappellani combination discloses or suggests this limitation.

196. Wann does not explicitly indicate that the silicon wafer is doped, and therefore, to the extent the wafer being undoped is not explicitly disclosed, a person of ordinary skill in the art would have had good reason to leave the silicon wafer undoped. Wann’s disclosure does not indicate the surface of the silicon wafer is doped, and leaving it undoped would have eliminated the need for a doping step.

Therefore, a person of ordinary skill in the art would have been motivated to leave it undoped in order to reduce the number of process steps required.

197. Moreover, as I discuss above in section IX.G.1, Cappellani discloses doping the source/drain regions of the fin portion of the silicon substrate in order to allow for very accurate etching of the doped regions to form cavities for subsequent formation of regrown source/drain regions. (Ex. 1009, ¶¶[0027], [0030]-[0031], [0033]-[0035], FIGs. 2A-B, 4A-C.) Cappellani discloses that by using a selective etch, doped areas are etched at a faster rate than the undoped substrate:

The etch operation 110 uses etchants that complements the dopant used in the ion implantation process to increase the etch rate of the doped regions. This enables the etching process to remove the doped fin region at a faster rate than the remainder of the **undoped** (or more lightly doped) **substrate**. As such, with an appropriate increase in etch rate, the etching process can selectively remove substantially the entire semiconductor fin (i.e., entire height H_{si} over the entire channel width W_{si} , as shown in FIG. 3A) and retain only the channel region with good profile and depth control. This includes portions of the doped regions that undercut the gate stack space and the gate dielectric, thereby defining a self-aligned source/drain fin extensions of the multi-gate transistor.

(*Id.*, ¶[0033].)

198. Therefore, like Wann, Cappellani discloses removing/etching fin regions 208 and then regrowing a different material, e.g., SiGe of high Ge content, to serve as source/drain regions for a FinFET device. (*Id.*, ¶¶[0022], [0025]). A person of ordinary skill in the art would have recognized that Cappellani’s method of providing accurate etching would have been applicable to the FinFET device of the Wann-Cappellani combination. Such a person of ordinary skill in the art would have recognized that the same benefits provided by such accurate etching, as disclosed by Cappellani, would similarly benefit the Wann-Cappellani FinFET. For example, the dopant-aided etching process not only “enables excellent control of the etch profile allowing shaping of the regrown source and drain regions” but also improves electrical performance of the FinFET devices by providing “optimal sub-fin leakage characteristics and channel strain.” (*Id.*, ¶[0025]; *see also id.*, ¶[0033] (“with an appropriate increase in etch rate, the etching process can selectively remove substantially the entire semiconductor fin...and retain only the channel region with good profile and depth control.”), ¶[0050] (disclosing that the regrown source/drain regions form an “abrupt boundary” between the source/drain regions with another region).)

199. Therefore, in view of Cappellani’s disclosure of performing more accurate etching using selective etching to remove doped source/drain regions at a faster rate than undoped silicon substrate, a person of ordinary skill in the art would

have had good reason to leave the portions of the fins that are not etched away in the Wann-Cappellani combination undoped. Such remaining portions include the channel portion 222a of the upper portion 222 of the fin, which is between the source and drain regions, and the lower portion of the fin underlying the source/drain regions. (See my discussion above in section IX.D.1(d)-(e).) Therefore, in my opinion, the Wann-Cappellani combination discloses or suggests that “the surface that consists essentially of silicon is undoped” as recited in claim 7.

K. Wann in Combination with Cappellani and Kuhn Discloses or Suggests the Features of Claim 12

1. Claim 12

“A computing system comprising the integrated circuit of claim 1.”

200. As I discuss above in section IX.D.7, Wann discloses that “[t]he FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).” (See my discussion above in section IX.D.7; Ex. 1007, ¶[0009] (“The FinFET 200 refers to any fin-based, multi-gate transistor. ... **The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC).**”) (emphasis added).) I have been asked to assume a scenario in which the Wann-Cappellani combination discussed in section IX.J does not disclose or suggest a “computing system” as recited in claim 12. Under such an assumption, Kuhn discloses using non-planar transistors on integrated circuits in a

computing system, and, in my opinion, a person of ordinary skill in the art would have had good reason to use the transistor of the Wann-Liao combination in a computing device as disclosed by Kuhn for the same reasons I discuss above in section IX.E.

L. Wann in Combination with Cappellani and Ching Discloses or Suggests the Features of Claim 11

201. In my opinion, Wann in combination with Cappellani and Ching discloses or suggests all of the features of claim 11 of the '334 patent.

1. Claim 11

202. Wann in view of Cappellani and Ching discloses or suggests the features of claims 11. As I discuss above in section IX.J.1, it is my opinion that a person of ordinary skill in the art would have had good reason to use SiGe with a germanium concentration of at least 50% in non-planar devices as disclosed or suggested by the Wann-Cappellani combination. (See my discussion above in section IX.J.1.) As I discuss above in section IX.F.1, a person of ordinary skill in the art would have had good reason, in view of Ching, to include nanowires in the non-planar devices of Wann such that the Wann-Ching combination discloses or suggests the features of claim 11. (See my discussion above in section IX.F.1.)

203. For the same reasons I discuss above in section IX.F.1, a person of ordinary skill in the art would have had good reason to use nanowires, as disclosed by Ching, in the non-planar device of the Wann-Cappellani combination. (See my

discussion above in section IX.F.1.) The use of SiGe with a germanium concentration of more than 50% for the strained material in the source/drain regions of the non-planar transistor does not impact the use of nanowires in the channel region. Therefore, the Wann-Cappellani-Ching combination discloses or suggests the features of claim 11 for the same reasons I discuss above in section IX.F, where, instead of germanium strained material in the source/drain regions as discussed in section IX.D, the non-planar devices have SiGe strained material in the source/drain regions as discussed in section IX.J.1. (See my discussion above in sections IX.F, IX.J.1)

X. CONCLUSION

204. In summary, it is my opinion that all of the features recited in claims 1, 2, 5-8, 10-14, 16-18, and 20 of the '334 patent are disclosed or suggested by the prior art.

205. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: April 10, 2023

A handwritten signature in cursive script, reading "Stanley Shanfield". The signature is written in dark ink and is positioned above a horizontal line.

Stanley Shanfield