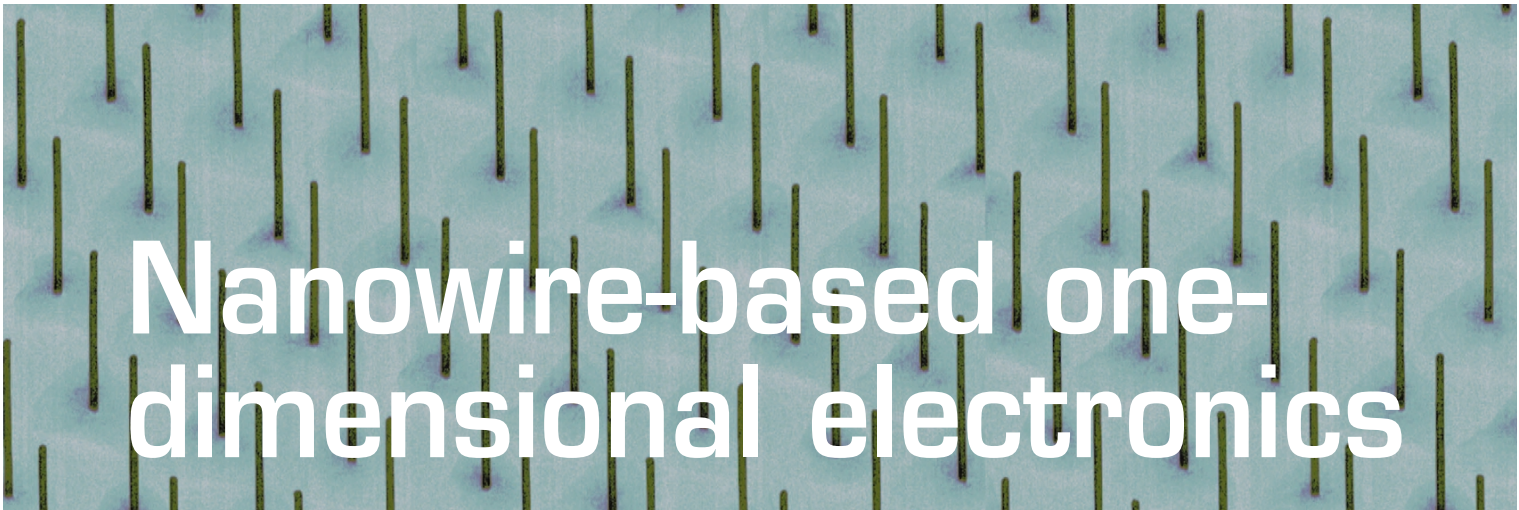


A scanning electron micrograph (SEM) showing a dense array of vertical, cylindrical nanowires. The nanowires are light blue or grey, standing out against a darker, textured background. They are arranged in a somewhat regular grid pattern, though with some variations in spacing and height.

Nanowire-based one-dimensional electronics

During the last half century, a dramatic downscaling of electronics has taken place, a miniaturization that the industry expects to continue for at least a decade. We present efforts to use the self-assembly of one-dimensional semiconductor nanowires¹ in order to bring new, high-performance nanowire devices as an add-on to mainstream Si technology. The nanowire approach offers a coaxial gate-dielectric-channel geometry that is ideal for further downscaling and electrostatic control, as well as heterostructure-based devices on Si wafers.

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Title image shows nanowires grown in arrays, courtesy of Linus Fröberg, Lund University, Sweden.

The roadmap for downscaling and introducing new technologies in the semiconductor industry is well laid out for the next ten years². In a special section on Emerging Research Devices in the *International Technology Roadmap for Semiconductors*, one-dimensional structures, such as carbon nanotubes and semiconductor nanowires, are explicitly mentioned as realistic

additions. Devices based on such materials are, however, still in an embryonic stage from an industrial point of view. Whether they will really have an impact on future post-complementary metal-oxide-semiconductor (CMOS) technology depends on more factors than just superior single-device performance. From the history of the semiconductor industry, we have learned that only those

technologies that can be integrated and scaled up for large hierarchical systems will survive and have impact.

A project was initiated in September 2005 within the European Union to address these open questions³. The aim of the project is to consolidate and transfer semiconductor nanowire technology from a research level to an industrial development environment. The partners in the project will assess the compatibility of nanowire growth with conventional semiconductor processing, and evaluate the potential performance of key device concepts based on nanowires. The main issues that the project deals with are discussed here.

This review is divided into five sections, each addressing important steps toward the implementation of semiconductor nanowires. The first section describes tasks related to understanding, and ultimately controlling, various aspects of nanowire growth. This is followed by a section discussing the development and optimization of new, nanowire-specific processing techniques. After that, we briefly cover the importance of characterizing, modeling, and extracting important physical properties in order to evaluate and optimize nanowire growth and processing. Potential devices that can benefit from being built around nanowires then need to be identified, modeled, and characterized, which is briefly described in the next section. The last section deals with integration and up-scaling issues, such as compatibility with CMOS and reproducibility of the processes.

Nanowire growth

A semiconductor nanowire is a solid rod with a diameter less than 100–200 nm composed of one or several semiconductor materials. A lower limit is hard to define – wires of 5 nm in diameter are realistic options for this technology. Nanowires can be synthesized using many techniques, and a comprehensive review on this subject is given by Xia *et al.*⁴. The particular type of nanowire we focus on here is typically grown from a metal particle, the size of which determines the diameter of the wire. The growth is in general described by the vapor-liquid-solid (VLS) growth mechanism^{5,6}, although in some systems evidence for a vapor-solid-solid (VSS) mechanism has been observed^{7,8}. In both of these cases, the crystal growth rate in one dimension at a given temperature is greatly enhanced with respect to the typical two-dimensional growth rate, resulting in structures with a large aspect ratio. Nanowires can also be grown without a metal seed, for example in the presence of an oxide⁹ or by masking a substrate¹⁰.

Many techniques for epitaxial crystal growth are currently used to produce nanowires, such as molecular/chemical beam epitaxy, vapor phase epitaxy/chemical vapor deposition, and laser ablation. The particular method used influences the potential material compositions, doping (intentional and unintentional), crystal quality (microstructure and chemical purity), and growth rate. It is therefore important to establish the relative merits of the various growth techniques.

Nanowires are of interest to both the scientific and technical communities because of the possibilities for greatly reduced device

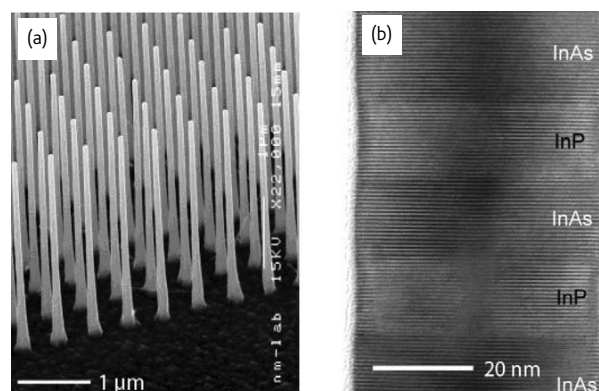


Fig. 1 (a) Position-controlled InP nanowires grown on an InP substrate¹¹. (b) High-resolution transmission electron microscopy image of a low bandgap InAs nanowire (dark) with two InP tunnel-barrier segments (bright). (Part (a) reprinted with permission from¹². © 2004 American Chemical Society.)

dimensions, radial epitaxial capping, and axial growth of lattice mismatched structures. To be of real interest to industry, however, it is necessary to solve not only generic issues related to epitaxy (crystal quality, doping, and reproducibility), but also obtain control of those properties unique to nanowires, such as wire position, direction, and shape. The main challenges for nanowire growth can be divided into four areas: control of growth, heterostructures, doping, and integration with Si.

General growth control

An understanding of the fundamentals of nanowire growth is of great importance to optimize nanowire positioning (Fig. 1a), growth direction, morphology, and crystal structure (hexagonal/cubic). This will require further knowledge of the conditions under which one-dimensional crystals preferentially form, and how the various growth mechanisms differ from each other. In particular, the role of the commonly used metal collector particle must be better understood. The development of models for particle-free nanowire growth is also critical. Detailed investigation of the physical and chemical processes involved (adsorption, diffusion, interactions) is key to this understanding.

Heterostructures

Nanowire heterostructures are mainly divided into two categories, axial and radial. Axial heterostructures, where the wire material is varied in the growth direction, are produced using normal nanowire growth techniques, including the common particle-assisted growth mechanism. Efficient strain relaxation in thin nanowires allows the combination of non-lattice-matched materials¹³ (Fig. 1b). The bandgap can thus be tuned locally along the length of a nanowire, giving access to completely new alternatives for device optimization, e.g. allowing formation of tunnel-barrier and quantum-confined structures. Radial

heterostructures are formed under bulk-like conditions around an existing nanowire. These can, for example, be used to cap the nanowire with a higher bandgap material, either for passivation or modulation doping. Furthermore, strain from a lattice mismatch between the core and the shell may be used as an additional means of altering the energy structure within the nanowire.

Doping

One of the main reasons for the usefulness of semiconductors in electronics is the possibility of controlling the conductivity and carrier type by adding impurities. In this way, a semiconductor can be 'doped' to conduct with negative electrons (*n*-type) or positive holes (*p*-type), enabling *p-n* junctions and transistors to be formed. This is also a key advantage of semiconductor nanowires over carbon nanotubes – the major competitor in the field of one-dimensional electronics – for which the bandgap and doping are hard to control. However, it is not yet fully understood how dopants are incorporated in particle-assisted growth of nanowires, and how the presence of dopants affects wire growth. Many growth techniques use carbon-containing precursor materials, which may under some conditions introduce unintentional carbon impurities into the nanowire. It is therefore necessary to understand how, and under which conditions, impurities incorporate into nanowires. Another intriguing problem associated with the doping of nanometer-scale structures relates to statistics: a doping level of 10^{18} cm^{-3} in a 5 nm thick Si wire correlates to only one dopant every 50 nm of wire. Hence, a short gate-length transistor of, say, 30 nm gate length will either be empty of dopants or have one dopant atom in the active transistor region. For this reason, it seems clear that one may choose to design a technology to operate without impurity dopants in the active device volume.

Si integration

Integration on Si is essential for nanowires to be of interest for large-scale electronic applications. Further details of this will be discussed in a later section; however, it does present a few specific challenges for nanowire growth. The most significant is probably the elimination of Au from the process. Since Au has to be avoided in CMOS, compatible catalysts or catalyst-free growth techniques must be developed. The difficulty here is that, while many other metals have been studied for use as collector particles and a few have indicated promise¹⁴, the crystal quality, reproducibility, and direction control achievable using Au have not been demonstrated with any other metal. It may turn out that particle-free techniques provide the best solution to this problem. For this to be the case, better length and diameter control must be developed.

It is also necessary to find processing conditions that either favor or force growth of nanowires in certain crystal directions, preferably the [001] direction. Such 'forced' growth of InP nanowires in the [001] direction on InP substrates has been demonstrated¹⁵; it will be of

interest to develop similar results on Si substrates. Growth temperatures will also be restricted, depending on whether growth occurs at the front-end-of-line (FEOL) or back-end-of-line (BEOL) of CMOS.

Nanowire processing

Once nanowires have been grown they must be connected to the outside world to eventually become part of an electronic circuit. However, the high aspect ratio of these objects requires the development of new, nanowire-specific processing techniques. We will describe here a simplified case of sample processing where the growth substrate acts as bottom contact to the nanowires. This section is divided into three parts describing important steps in the formation of source, drain, and gate contacts to the nanowires.

Seed patterning for nanowire growth

In one sense, contact formation starts when the nanowire seeds are defined on the semiconductor surface. To grow semiconductor nanowires at defined locations, the seeds have to be positioned. The most common process for the definition of seeds is electron-beam lithography exposure of a resist layer, metal evaporation, and a lift-off step. Figs. 2a–2c show the cross section of a sample during the seed fabrication process. While the size, periodicity, and thickness of the nanowires do not impose strong demands on the fabrication process, proper surface preparation before seed deposition is crucial for well-controlled nanowire growth. If contamination or an oxide layer is present between the seed and the semiconductor surface, the seed may still initiate growth but crystallographic alignment with the substrate may be lost. Development of a standardized process for pregrowth wafer treatment will be an important milestone for reproducible nanowire growth.

Nanowire contacts

The most widely used method to define contacts to nanowires is to remove the nanowires from the growth substrate and deposit them on a second substrate. Usually the wires are suspended in a liquid that is then applied to the substrate¹⁶, but 'dry' transfer methods also work. Inspection under an electron microscope then reveals promising candidates for electrical characterization. Contacts are made to individual wires using electron beam lithography, metallization, and lift-off.

However, for up-scaling, an approach that does not rely on a random process step is required. If nanowires are grown epitaxially on the substrate from defined seed locations, the wires can be left in place and contacts can be post-processed to the top of the wires. This requires a planarization step, which can be achieved, for example, by spinning a polymer onto the nanowire sample. Fig. 3 shows (a) as-grown and (b) planarized nanowires. Contacts to the top of the wires can then be formed by metal evaporation.

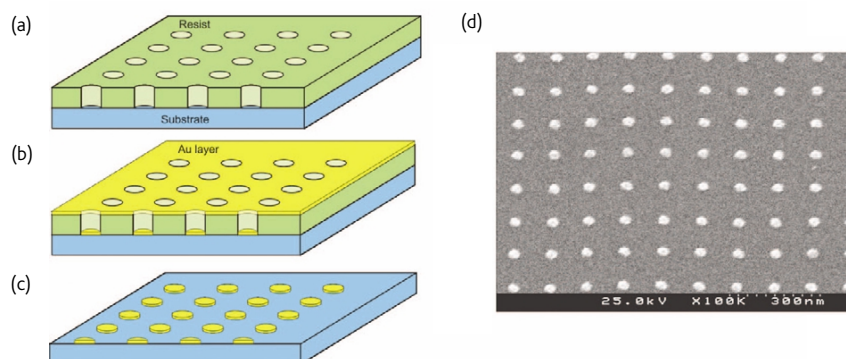


Fig. 2 Seed fabrication process: (a) resist exposure and development; (b) evaporation of Au layer; and (c) lift-off. (d) Scanning electron micrograph of Au seeds on a GaP substrate. The dots have diameters of 30 nm and a height of 15 nm.

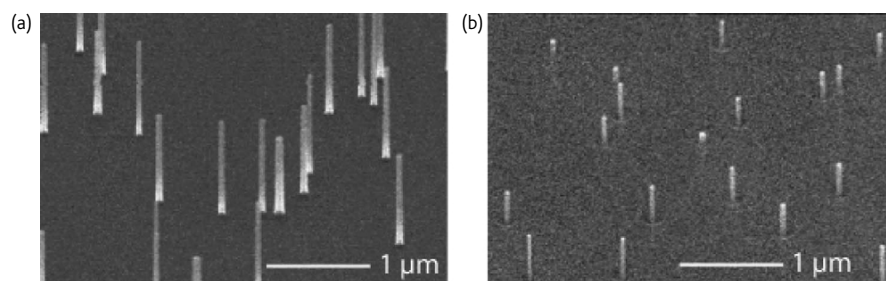


Fig. 3 Scanning electron micrographs of GaP nanowires (a) before planarization and (b) after planarization.

Wrap gates

A field-effect transistor (FET) also requires a gate besides the source and drain contacts. It is predicted that the vertical geometry of nanowires, which makes it possible for a gate to surround the nanowire, will lead to superior electrostatic control of the conductivity in the FET channel. However, wrap-gate formation in the lateral

geometry is also possible, as recently demonstrated by Samsung¹⁷. The important steps in forming a vertical wrap gate are deposition of a dielectric layer followed by gate metal deposition and an etch-back process¹⁸. Fig. 4 shows a vertical array of nanowires fully covered in a Si_3N_4 dielectric, where the thick base of the nanowires indicates the length of the metal wrap gate.

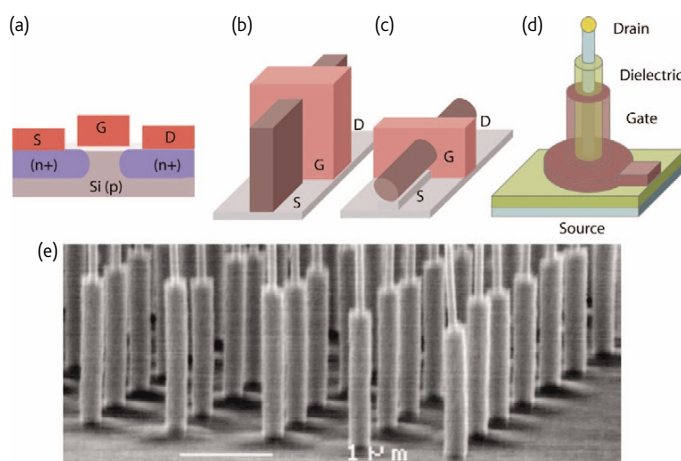


Fig. 4 Possible evolution of the field-effect transistor. (a) Metal-oxide-semiconductor FET (MOSFET): the planar gate affects the conducting channel from one direction. (b) FinFET: the gate surrounds the channel from all but one side. (c) Nanowire FinFET: complete, but nonuniform wrap-around gate. (d) Vertical nanowire FET: the gate has a complete, uniform wrap-around gate. (e) Vertical array of nanowires after wrap-gate formation. (Reprinted with permission from¹⁹. © 2006 Institute of Physics Publishing.)

Nanowire physics and characterization

To integrate nanowires into electronic components reliably, a thorough understanding of their relevant physical properties is required. The well-established physics of three-dimensional, two-dimensional, and more recently zero-dimensional semiconductor materials must be revised for the specific one-dimensional nanowire properties, such as surface and interface relaxation, carrier confinement (electrons and holes), and the strong dielectric index change at the nanowire-environment interface. These new theories must be compared with experiments on actual nanowire structures, such as the verification of electronic structure calculations for nanowire heterostructures by photoluminescence measurements.

Electronic properties

Crucial parameters for the electrical performance of nanowire devices are the carrier concentration (defined by the doping level), carrier mobility, and bandgap. Since these parameters can strongly depend on details of the nanowire growth, direct feedback between electrical characterization and growth optimization is necessary. Although future devices are envisioned with direct electrical contacts to the wires on a suitably structured growth substrate, nanowire characterization is usually performed horizontally (Fig. 5) as described in the previous section on nanowire contacts. The mobility can then be estimated based on how the nanowire conductance changes with the back-gate voltage. In parallel, optical techniques with micrometer-range spatial resolution (μ -photoluminescence) can also address individual wires and, in particular, reveal the bandgap.

Structural properties

The intrinsic band structure and density of states of nanowires depend directly on the structural design and quality, in particular on the occurrence of growth-related defects (dislocations, stacking faults, etc.). Consequently, these have to be investigated and understood before the electronic properties can be optimized. The crystalline nanowire

structure may be quite different from that of bulk materials or other semiconductor heterostructures (superlattices, quantum dots) because of surface relaxation effects or kinetic limitations. For example, longitudinal or axial InAs/InP nanowire heterostructures grown on InAs(111)B have a hexagonal lattice (Fig. 1b), while both of these materials are cubic in the bulk. In small-diameter nanowire heterostructures, interface strain can be more easily accommodated. This inhibits the formation of misfit dislocations of mismatched materials and allows extended bandgap engineering. Additionally, the use of core-shell structures can strongly impact the electrical and optical properties²⁰. Understanding the strain in nanowires is thus a demanding problem for device optimization. Here, electron microscopy is a very efficient tool to obtain quantitative information about crystal structure and strain, as well as to identify growth-related defects like surface faceting, twins, and stacking faults. X-ray diffraction techniques also help to gain statistical information about shapes, misorientations, elastic and intermixing strain relaxations, and structural defects of epitaxial samples (Fig. 6). The results can then be compared with atomistic electronic and transport simulations to quantify the impact of important growth defects.

Nanowire devices

Electronic devices form the basic constituents of modern integrated circuits. They come in many varieties and are used to amplify and rectify electronic signals, perform logic operations, or store charge in digital memories. Next to these purely electronic functions, other devices interact with light, heat flow, or even biological fluids. The small size and unprecedented capability of combining semiconductors with widely differing lattice parameters^{12,21} offer exciting new possibilities for devices. Nanowire device researchers face the exciting challenge of deciding which devices, and thus which future applications, are particularly promising for this new class of material.

Field-effect transistors

Among the many possibilities, the FET stands out as being the modern workhorse of the semiconductor industry. Therefore, it is not surprising that most efforts on nanowire devices have focused on making nanowire FETs. Researchers have typically either studied individual nanowires²² randomly placed on a substrate (that frequently also functions as the gate electrode), or have tried to fabricate transistors from arrays of vertical nanowires. Although the latter approach is much more complex in terms of device fabrication, it has the advantage of studying a large number of wires and hence taking full account of the expected statistical device fluctuations from the start. European research groups have made significant contributions in this area including wrap-gated Si²³ and InAs nanowires²⁴, even incorporating first attempts at bandgap engineering into the channel of the device. This work, together with similar research from the US²⁵, has shown that Si nanowires can deliver drive currents comparable to standard Si

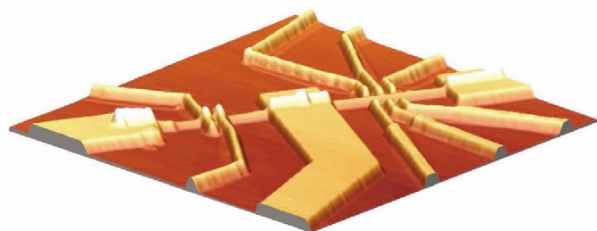


Fig. 5 Three-dimensional representation of an atomic force microscope image ($7\ \mu\text{m} \times 7\ \mu\text{m}$) of a nanowire test device. The InP nanowire (diameter 70 nm) spans the image from left to right. Three wide metallic contacts are used as ohmic current leads for two test structures on the same nanowire: the left part shows two additional electrodes (voltage probes for four-point measurements), whereas the right part features several side-gates for local gating.

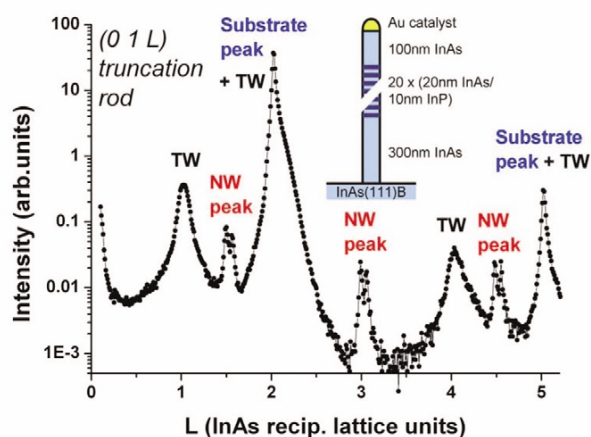


Fig. 6 Grazing incidence X-ray diffraction of epitaxial InAs/InP heterostructure nanowires. The reciprocal units are indexed with the hexagonal surface lattice of the face-centered cubic InAs substrate. The experiment is performed with a grazing incidence of 0.1° and 10 keV photon energy. Note the scattering contributions of the hexagonal close-packed nanowires (NW) as well as twins (TW) in the cubic phase that come from a small substrate overgrowth in-between the NWs. The peak doubling of the NW peaks comes from multiple scattering effects.

devices, and that bandgap engineering of the nanowire channel adds a completely new degree of freedom in tuning the device performance of the FET. These are important milestones in nanowire device research. Especially in devices with a controlled number of wires per electrode, the characterization of nanowire devices can be taken to a level more comparable to the industry standard.

Besides FETs, there are other natural device candidates for nanowires. One example is a high-performance radio-frequency transistor, illustrated in Fig. 7. Such a device could be used in future mobile phones or other communication devices. Initial modeling of a nanowire device indicates a particularly promising combination of high speed and high breakdown voltages. Experimental work to confirm these predictions is on-going.

Device characterization and optimization

One handicap that nanowire device researchers face is the absence of easy capacitance-based characterization tools. This is primarily because of the small amount of charge involved in nanowire device

operation, which is well below today's standard measurement techniques.

Throughout the history of semiconductor devices, capacitance-voltage measurements on large-area structures have been essential for determining the quality of contacts, heterojunctions, dopant incorporation, and metal-oxide-semiconductor sandwiches. For nanowire devices, a large and controlled number of devices must typically be connected in parallel, and 'parasitic' capacitances arising from the environment must be carefully minimized to be smaller than those of the active devices. In practice, this amounts to solving the nanowire integration and up-scaling problem first – a huge challenge in itself, as will be discussed in the next section. Instead, nanowire device characterization typically relies only on current-voltage measurements on a small number of devices. An innovation in this area, such as a special device geometry or measurement technique, could significantly accelerate the development of new devices

While research at the individual device level is beginning to produce interesting experimental results, an important aspect is awareness of

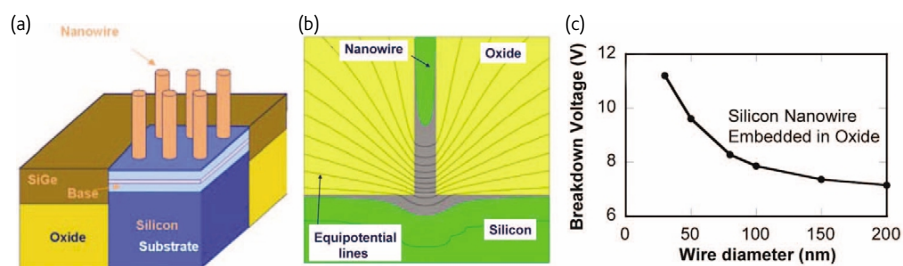


Fig. 7 A possible nanowire junction transistor. (a) Sketch of the device geometry. (b) Potential distribution in a Si nanowire junction. The depletion zone is indicated in gray. (c) Simulated breakdown voltage of a nanowire-substrate junction in Si.

the intimate link between device performance and the way the devices are assembled or integrated to make any functional unit in future circuits. While it was possible to separate the devices from their environment in the past, this is no longer true in modern integrated circuits, which are increasingly dominated by the capacitances and resistances of the connecting elements rather than the devices themselves. The need for minimizing these parasitic elements will be touched upon in the next section concerning nanowire device integration.

Nanowire integration and up-scaling

Nanowires allow researchers to carry out beautiful physics experiments²⁶ and may also have great potential for both future device applications and novel device architectures²⁷. From an implementation point of view, however, it would be naive to assume that nanowires will suddenly replace CMOS technology. Instead, we can expect that nanowire technology will gradually find its place by adding functionality, offering process advantages, and delivering superior performance in selected areas. This will be driven by advantages such as the potential for wrap gates, three-dimensional integration, and the ability to grow heterostructures of materials with a large lattice mismatch. It is of vital importance to carefully investigate this potential.

Moreover, in comparison to other 'nanotechnology' device options, semiconductor nanowires may have the potential to be implemented on an existing semiconductor infrastructure and can thus benefit from continuous improvements in CMOS technology. This scenario, however, needs on-going innovations and breakthroughs, and there is no doubt that there are further challenges to overcome before nanowires are implemented in a high-end product. A few of the main challenges are now briefly discussed.

Compatibility with manufacturing

Contamination issues are a major source of concern when considering implementation of new processes in an actual production line. However, many new materials have been introduced in recent years in light of physical limitations faced by the more traditional materials used in the microelectronics industry for decades (Si, SiO₂, polycrystalline Si). For instance in FEOL, HfO₂ and other 'nonstandard' high dielectric constant (*k*) materials are used as replacements for SiO₂ as the gate dielectric. At the contact level, Ti, Ni, and Ni/Pt self-aligned silicides have gradually replaced Co as the material of choice. Also, in BEOL, the transition from Al and SiO₂ to Cu and so-called low-*k* dielectrics has helped to pave the road for the acceptance of many more exotic materials.

It is critical for this last implementation that a diffusion barrier material can be reliably placed between the interconnect metal and Si, because some metals (such as Cu and Au) create deep trap levels in the Si bandgap and thus cause undesirable changes to the electrical properties of Si.

Also, as contamination resulting from process errors is unavoidable, cleaning solutions need to be available for encapsulation and effective removal of any material used in production. This last requirement is the main differentiator between the now widely accepted use of Cu as the interconnect metal of choice and the continuing strong resistance against the use of Au. Today, Au is the most common material used for particle-assisted nanowire growth, as discussed in the first section. However, Au has the disadvantage of being difficult to remove/clean and therefore other, CMOS-compatible catalysts are being considered.

Wire growth and thermal budget

The thermal budget available for nanowire growth limits the materials that can be used. Clearly, this boundary condition and the contamination issues mentioned above depend on where in the process implementation is to be considered.

In FEOL, high temperatures are used for dopant activation (flash anneal to 1100°C), while the replacement of Co by nickel silicide limits subsequent process temperatures to below 450°C for stability reasons. Low-*k* materials used in BEOL typically become unstable between 400°C and 450°C.

This clearly limits the maximum temperature for growth of nanowires intended to bring additional functionality to existing CMOS. However, nanowire growth has been reported at consistently lower temperatures, which indicates that implementation may be possible within the thermal constraints of the process.

Device fabrication and variability

Once good control over wire growth has been achieved, further processing is required to integrate nanowires into a functional device. However, to make a nanowire transistor with stable and reproducible electrical characteristics, several critical issues need to be addressed, as shown in Fig. 8.

Firstly, the length and diameter of the wire need to be controlled within tight limits. After growth, the wire surface needs to be properly passivated by thermal oxidation or conformal atomic layer deposition of a high-*k* material serving as gate dielectric.

Next, the formation of a gate with an accurately controlled length needs to be accomplished. As impurity doping is no longer effective in ultrathin body devices, the threshold voltage of the transistor needs to be set by the gate material with an appropriate work function. This issue is, however, not specific to nanowire technology and breakthroughs in scaled CMOS will help.

Source and drain regions are created by conventional impurity doping or, alternatively, by metallization to form so-called Schottky barrier transistors. In general, the overlap region of gate to source and drain must be optimized for high performance and an unwanted voltage drop has to be reduced to a minimum, i.e. the source and the drain region have to have ohmic contacts to the metal wiring (this has in fact recently been achieved with silicide contacts²⁸).

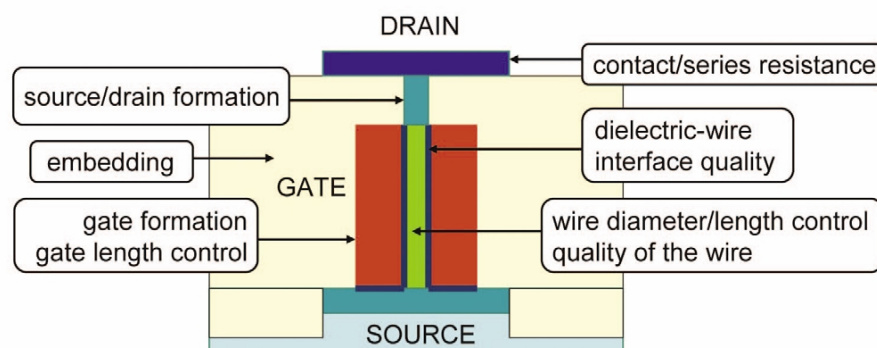


Fig. 8 Schematic cross section of a vertical nanowire transistor; critical areas are indicated.

As a result of the extremely small contact and current-carrying area, parasitic series resistance is believed to be critical in a nanowire transistor, again very similar to scaled CMOS. The mechanical properties of nanowires also need to be investigated in order to determine how well they withstand such process steps as spin-on of dielectric materials and mechanical polishing. However, the first realizations of vertical nanowire FETs look very encouraging^{18,23,25}.

Summary

This review has identified and discussed important technological questions that need to be addressed when evaluating the device-integration potential of semiconducting nanowires. The main issues related to growth of nanowires are control over nanowire nucleation on Si substrates, and that a replacement for Au as the seed material appears necessary. When selecting a device to implement with nanowire technology, it is important to make use of the unique advantages of nanowires: the ability to grow heterostructures and

achieve vertical alignment of high-quality crystals. Specifically, FETs are identified as promising candidates, although a lot of work is still required on the formation of a wrap gate, such as wire-passivation, dielectric and gate-metal deposition. While new material combinations can enable better transistors and the small size of nanowires can lead to high density for devices, the holy grail still remains, i.e. to find, understand, and use quantum-mechanical effects that are useful and impossible to obtain in standard Si technology. With the basic building blocks now becoming available, this is perhaps one of the most exciting and challenging areas of device research today. 

Acknowledgments

The authors would like to thank T. Bryllert, K. Dick, L. Kouwenhoven, G. Van den Bosch, P. Vereecken, F. Jacopi, G. Groeseneken, R. Vijayaraghavan, H. Riel, M. Björk, H. Schmid, O. Hayden, L. Fröberg, M. Kamp, V. Schmidt, P. Werner, H. Riechert, A. Tredicucci, and T. Mårtensson for valuable input and comments to this article. This work was supported by the EU program NODE 015783.

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