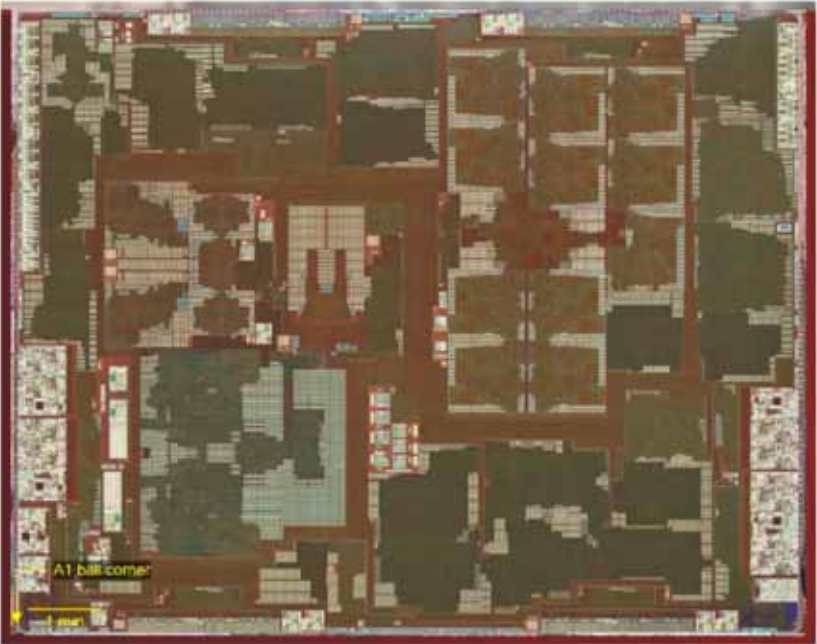
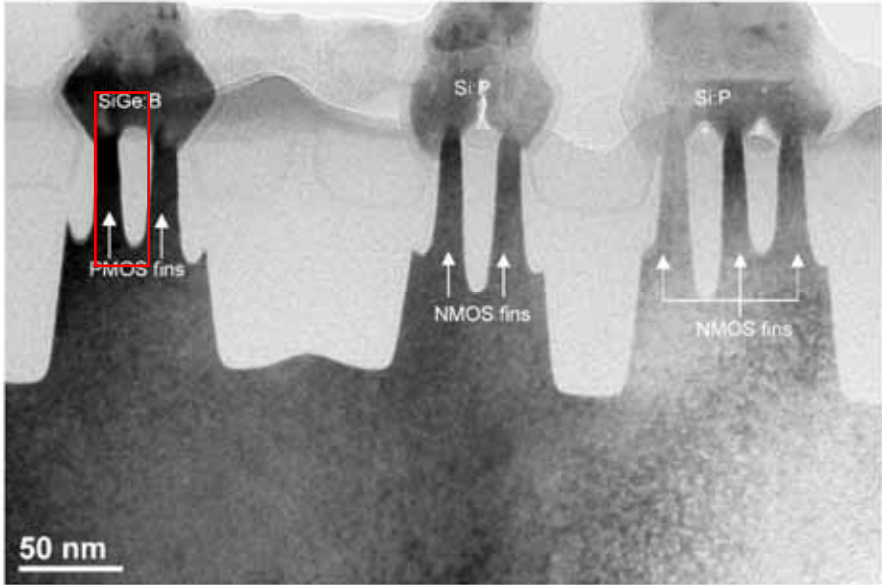


EXHIBIT A
(INFRINGEMENT OF U.S PATENT NO. 10,541,334)

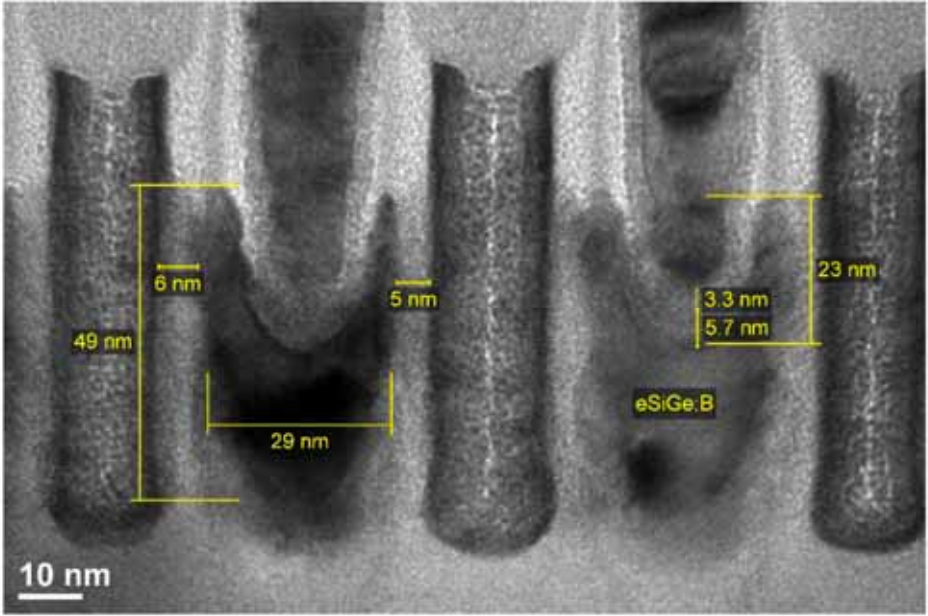
#	Claim Language	Accused Instrumentalities
1.1	1. An integrated circuit, comprising:	To the extent the preamble of Claim 1 is limiting, each of the '334 Patent Accused Products, including for example the, Samsung Exynos 990 – 7 nm processor, comprises an integrated circuit.¹³³ 
1.2	a non-planar body comprising semiconductor material, wherein the non-planar	Each of the '334 Patent Accused Products comprises a non-planar body comprising semiconductor material, wherein the non-planar body has top and side surfaces.

¹³³ TechInsights Report ACE-2003801, pg. 11.

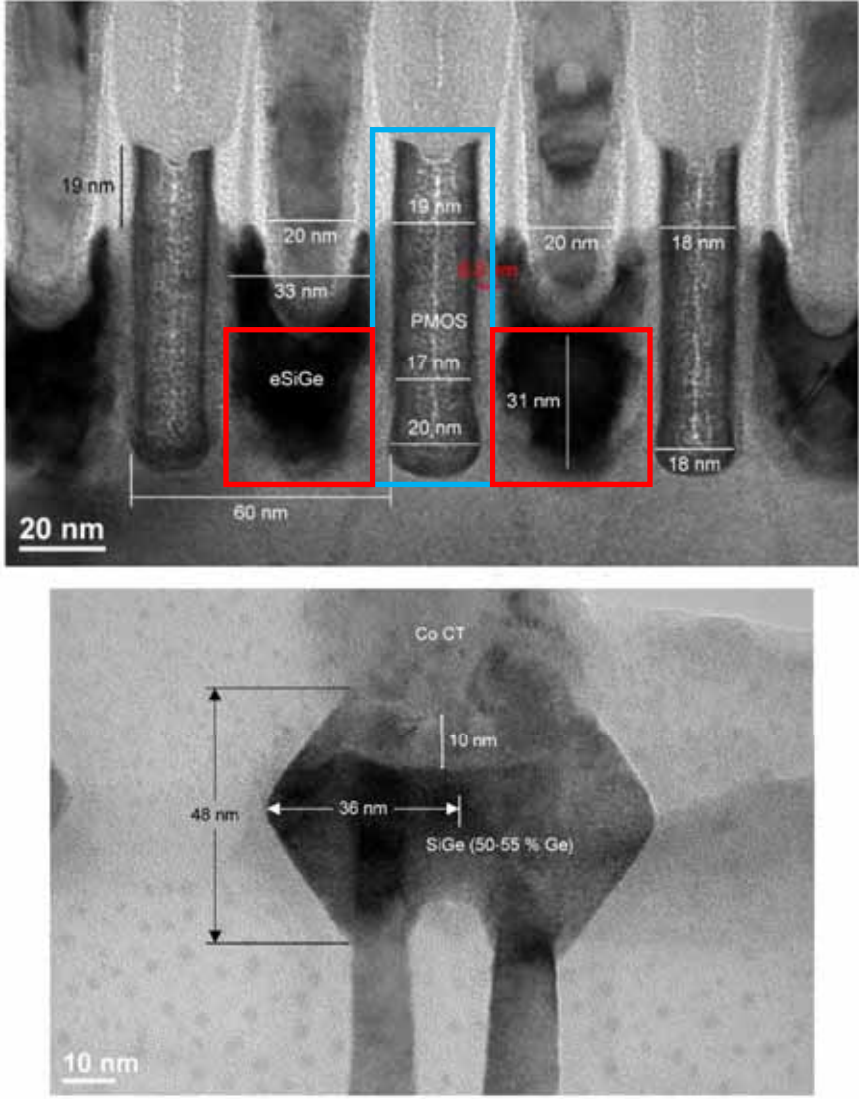
#	Claim Language	Accused Instrumentalities
	body has top and side surfaces;	For example, the fins contained in the Samsung Exynos 990 – 7 nm microprocessors are formed from the silicon substrate and have a non-planar body comprising semiconductor material, wherein the non-planar body has top and side surfaces.¹³⁴ 
1.3	a gate structure on at least the top and side surfaces of the non-planar body;	Each of the '334 Patent Accused Products comprises a gate structure on at least the top and side surfaces of the non-planar body. For example, the Samsung Exynos 990 – 7nm microprocessor comprises a gate structure on at least the top and side surfaces of the non-planar body.¹³⁵

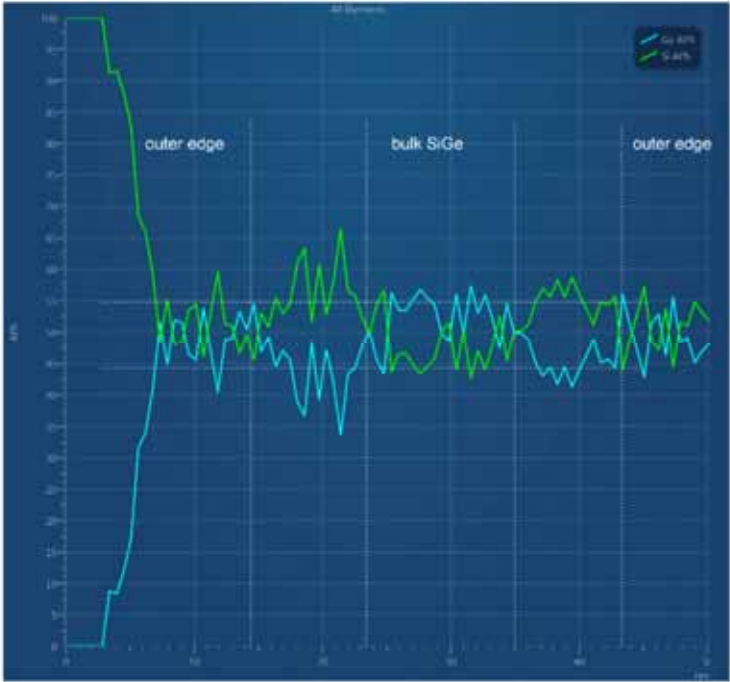
¹³⁴ TechInsights Report ACE-2003-801, pg. 27.

¹³⁵ TechInsights Report ACE-2003-801, pg. 29.

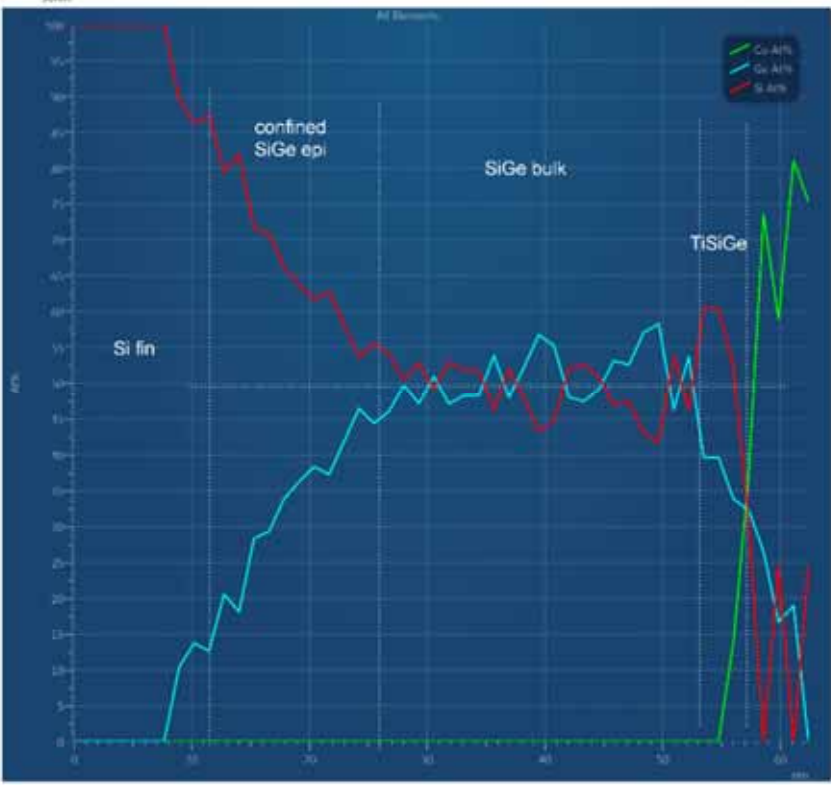
#	Claim Language	Accused Instrumentalities
		 A cross-sectional transmission electron micrograph (TEM) of a semiconductor device. The image shows a series of vertical structures. Dimensions are indicated with yellow lines and text: a total height of 49 nm on the left, a top width of 6 nm, a central width of 29 nm, a small gap of 5 nm, a bottom width of 3.3 nm, a bottom layer of 5.7 nm, and a total height of 23 nm on the right. A label 'eSiGe:B' is located near the bottom right. A scale bar at the bottom left indicates 10 nm.
1.4	a source region adjacent the non-planar body, the source region including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface	Each of the '334 Patent Accused Products further comprises a source region adjacent the non-planar body, the source region including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is direct contact with a surface that consists essentially of silicon. For example, in the Samsung Exynos 990 – 7 nm microprocessor, the source and drain pairs (shown in red) are formed on either side of the non-planar body and on either side of the gate structure (shown in blue).¹³⁶

¹³⁶ TechInsights Report ACE-2003-801, pg. 19.

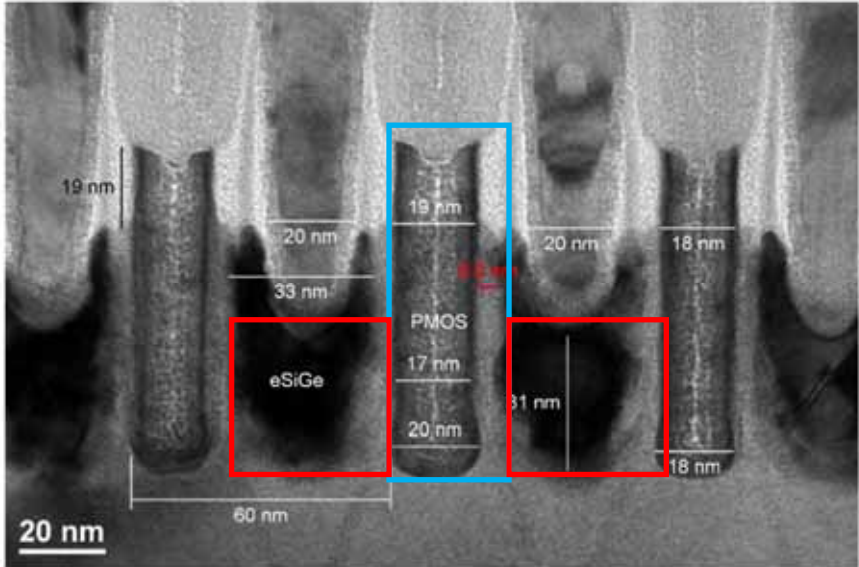
#	Claim Language	Accused Instrumentalities
	that consists essentially of silicon; and	 The top image is a cross-sectional SEM micrograph of a semiconductor device. It shows a series of vertical structures. Dimensions are labeled: 19 nm, 20 nm, 33 nm, 19 nm, 20 nm, 18 nm, 17 nm, 20 nm, 31 nm, 18 nm. A blue box highlights a central structure, and two red boxes highlight structures on either side. Labels include 'eSiGe', 'PMOS', and '20 nm' scale bar. The bottom image is a cross-sectional SEM micrograph of a single structure. Dimensions are labeled: 48 nm, 36 nm, 10 nm. Labels include 'Co CT', 'SiGe (50-55 % Ge)', and '10 nm' scale bar.

#	Claim Language	Accused Instrumentalities
		Additionally, on information and belief, the source is comprised of an embedded SiGe material, which further comprises a portion that has a Germanium concentration of at least 50% that is in direct contact with a silicon surface.¹³⁷ 

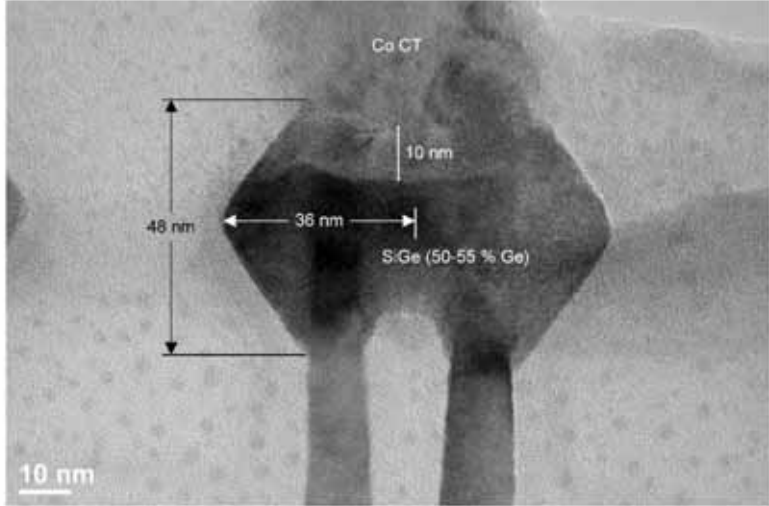
¹³⁷ TechInsights Report ACE-2003-801, pg. 6, 19, 27-29.

#	Claim Language	Accused Instrumentalities
		
1.5	a drain region adjacent the non-planar body, the drain region including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent	Each of the '334 Patent Accused Products comprises a drain region adjacent the non-planar body, the drain region including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon. For example, in the Samsung Exynos 990 – 7 nm microprocessor, the source and drain pairs (shown in red) are formed on either side of the non-planar body and on either side of the gate structure (shown in blue).¹³⁸ Additionally, on information and belief, the drain is comprised

¹³⁸ TechInsights Report ACE-2003-801, p. 19.

#	Claim Language	Accused Instrumentalities
	throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon.	of an embedded SiGe material, which further comprises a portion that has a Germanium concentration of at least 50% that is in direct contact with a silicon surface.¹³⁹  The image is a cross-sectional scanning electron micrograph (SEM) of a semiconductor device. It shows several vertical layers and features. Key labels and dimensions include: 19 nm: Dimension for the top layer on the left and right. 20 nm: Dimension for the layer below the top layer in the center and right. 33 nm: Dimension for a layer in the center. PMOS: Label for a transistor gate structure in the center. 17 nm: Dimension for a layer below the PMOS gate. 20 nm: Dimension for a layer below the 17 nm layer in the center. 31 nm: Dimension for a layer on the right. 18 nm: Dimension for the bottom layer on the right. eSiGe: Label for a layer in the center, highlighted with a red box. 60 nm: Dimension for the width of the central structure. 20 nm: Scale bar at the bottom left.

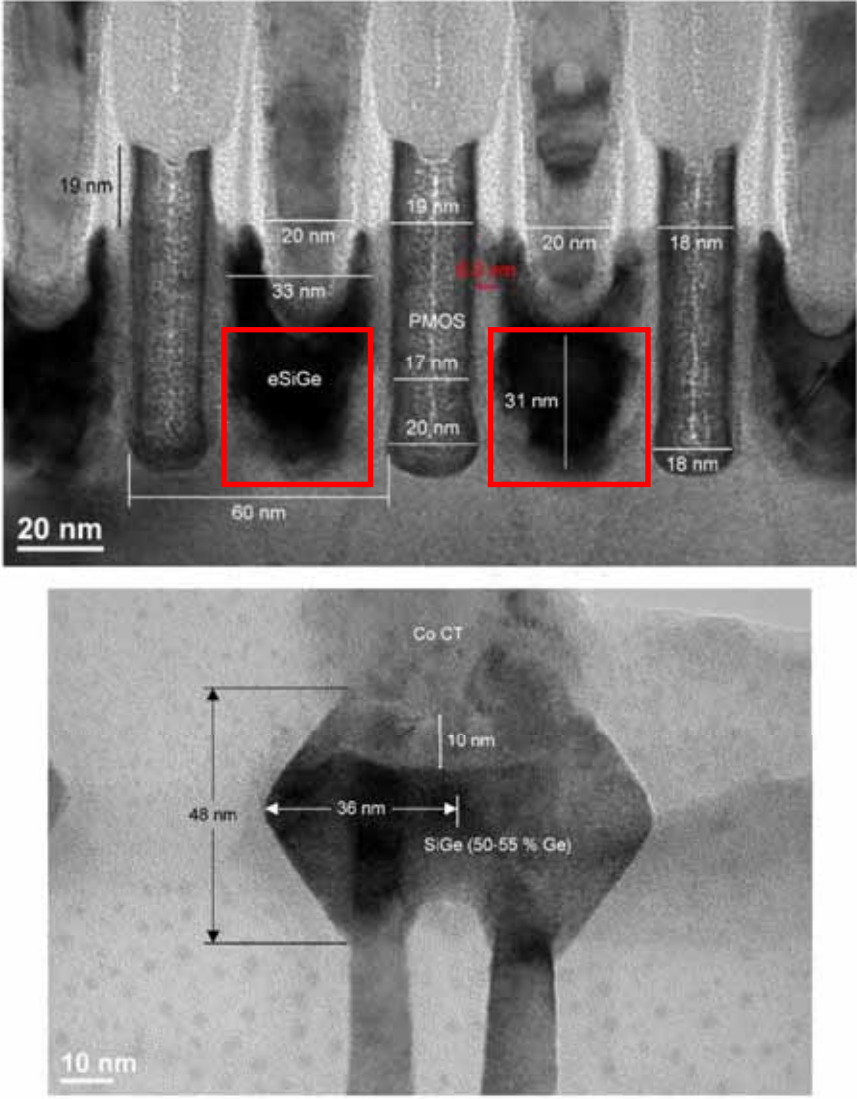
¹³⁹ TechInsights Report ACE-2003-801, pp. 6, 19, 27-29.

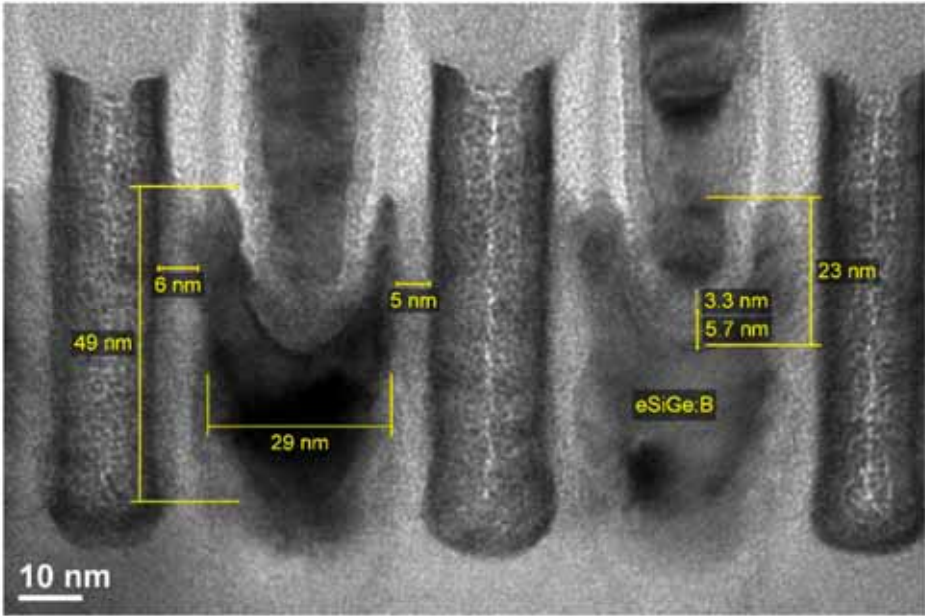
#	Claim Language	Accused Instrumentalities
		
2.1	2. The integrated circuit of claim 1,	See Claim 1, above.
2.2	wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.	On information and belief, each of the '334 Patent Accused Products comprises a surface that consists essentially of silicon and is one of a surface of bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate. For example, on information and belief, the fin is comprised of bulk silicon substrate.¹⁴⁰

¹⁴⁰ TechInsights Report ACE-2003-801, pp. 18, 27, 28.

#	Claim Language	Accused Instrumentalities
5.1	5. The integrated circuit of claim 1,	See Claim 1, above.
5.2	wherein the first and second portions further include one or both of silicon and tin.	In each of the '334 Patent Accused Products, the first and second portions further include one or both of silicon and tin. For example, in the Samsung Exynos 990 – 7 nm microprocessor, the source and drain pairs (shown in red) are comprised of an embedded SiGe material containing Silicon.¹⁴¹

¹⁴¹ TechInsights Report ACE-2003-801, pg. 19.

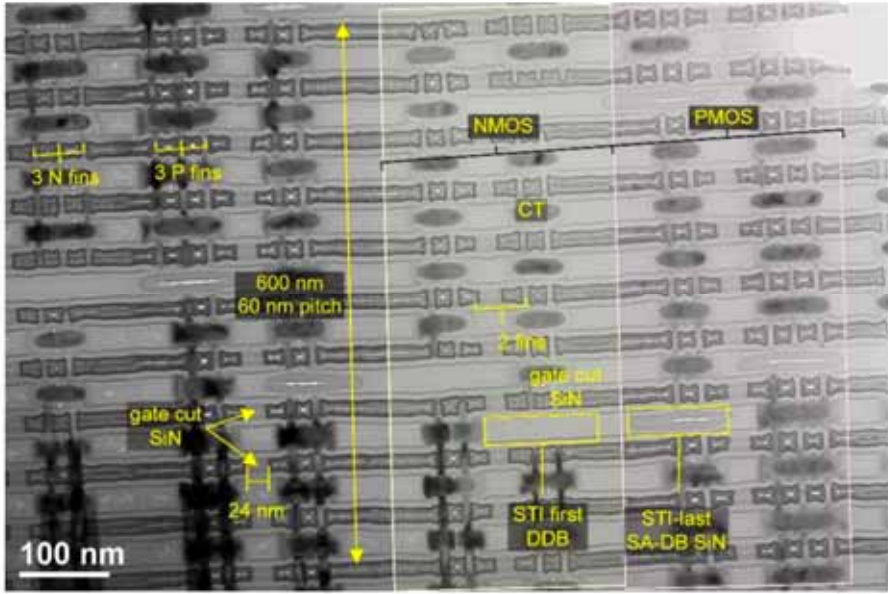
#	Claim Language	Accused Instrumentalities
		 The top image is a cross-sectional SEM micrograph of a semiconductor device. It shows a series of vertical structures. Various layer thicknesses are labeled: 19 nm, 20 nm, 33 nm, 17 nm, 20 nm, 18 nm, and 31 nm. Two regions are highlighted with red boxes and labeled 'eSiGe'. A scale bar of 20 nm is present. The bottom image is a cross-sectional SEM micrograph of a single structure. It shows a central region labeled 'SiGe (50-55 % Ge)' with a thickness of 36 nm. Above it is a layer labeled 'Co CT' with a thickness of 10 nm. The total height of the structure is labeled as 48 nm. A scale bar of 10 nm is present.

#	Claim Language	Accused Instrumentalities
6.1	6. The integrated circuit of claim 1,	See Claim 1, above.
6.2	wherein the first and second portions include a p-type dopant.	Each of the '334 Patent Accused Products comprises an integrated circuit according to Claim 1, wherein the first and second portions include a p-type dopant. For example, the Samsung Exynos 990 – 7 nm microprocessor includes source and drain structures that are doped with Boron, and thus comprise a p-type doped PMOS.¹⁴²  The image is a cross-sectional scanning electron micrograph (SEM) of a transistor structure. It shows several vertical pillars (source and drain regions) and a central gate structure. Yellow dimension lines indicate various measurements: a pillar width of 6 nm, a gate width of 5 nm, a pillar height of 49 nm, a gate height of 29 nm, a pillar width of 23 nm, and a gate width of 3.3 nm. A label 'eSiGe:B' is present near the base of the pillars. A scale bar at the bottom left indicates 10 nm.

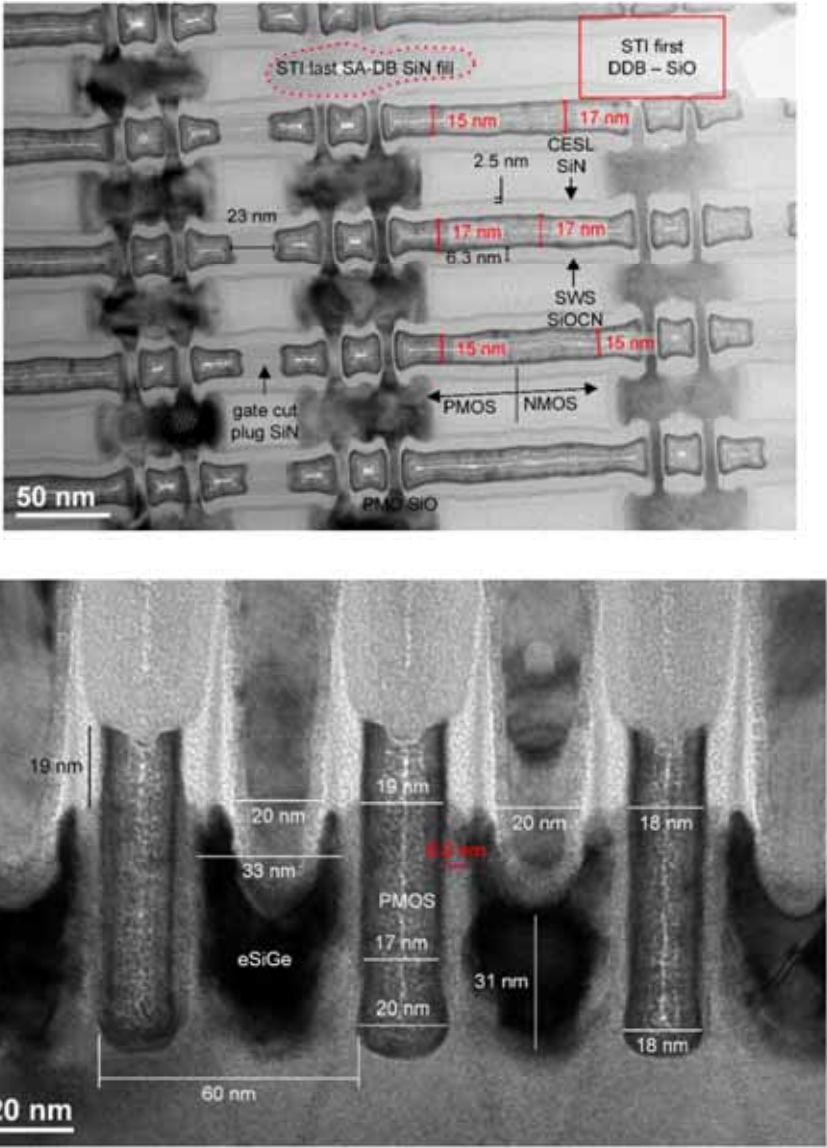
¹⁴² TechInsights Report ACE-2003-801, pp. 46-47.

#	Claim Language	Accused Instrumentalities
7.1	7. The integrated circuit of claim 1,	See Claim 1, above.
7.2	wherein the surface that consists essentially of silicon is undoped.	Each of the '334 Patent Accused Products a surface that consists essentially of silicon that is undoped. For example, the Samsung Exynos 990 – 7 nm microprocessor is comprised of undoped silicon from bulk substrate.¹⁴³

¹⁴³ TechInsights Report ACE-2003-801, p. 5, 46, 47, 49, 54, 55.

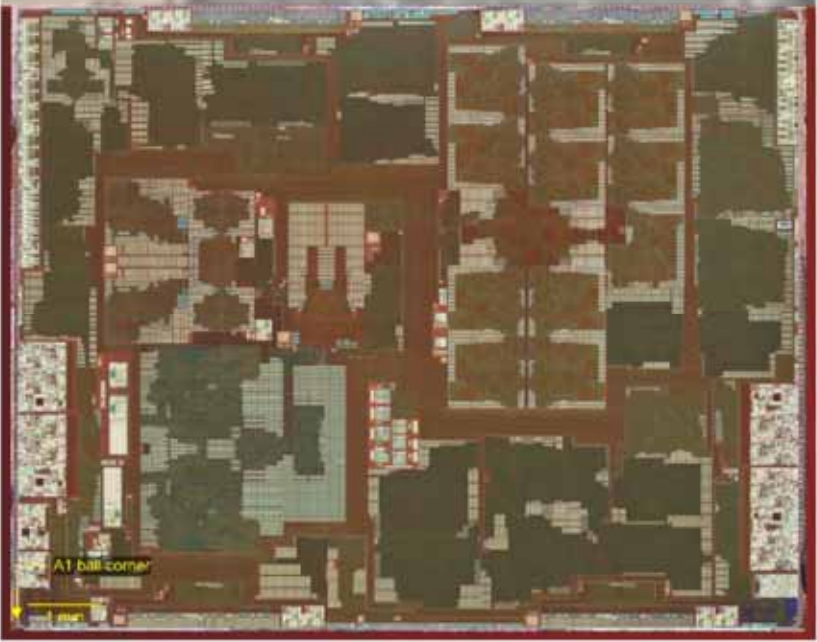
#	Claim Language	Accused Instrumentalities
10.1	10. The integrated circuit of claim 1,	See Claim 1, above.
10.2	wherein the non-planar body is a fin, the fin between portions of the gate structure.	Each of the '334 Patent Accused Products comprises an integrated circuit, wherein the non-planar body is a fin, the fin between portions of the gate structure. For example, the Samsung Exynos 990 – 7 nm microprocessor is comprised of a nonplanar fin structure between portions of the gate structure.¹⁴⁴ 

¹⁴⁴ TechInsights Report ACE-2003-801, p. 17, 19.

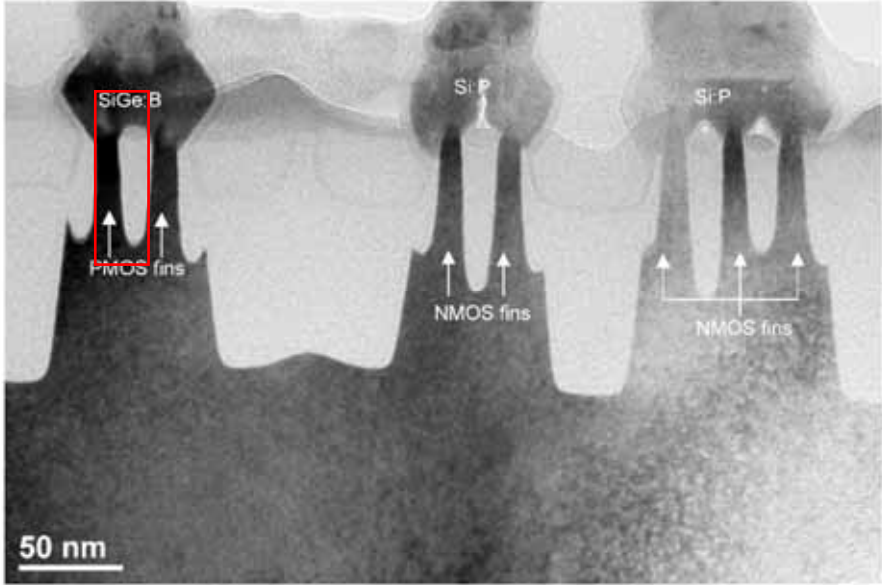
#	Claim Language	Accused Instrumentalities
		 The top image is a cross-sectional SEM micrograph of a semiconductor device. It shows a gate stack with various layers and dimensions. Labels include: 'STI last SA-DB SiN fill' (dashed red circle), 'STI first DDB - SiO' (red box), '15 nm', '17 nm', '2.5 nm', 'CESL SiN', '17 nm', '17 nm', '6.3 nm', 'SWS SiOCN', '15 nm', '15 nm', 'PMOS', 'NMOS', 'gate cut plug SiN', 'PMO SiO', and a '50 nm' scale bar. The bottom image is a cross-sectional SEM micrograph of the same device, showing a different cross-section. Labels include: '19 nm', '20 nm', '33 nm', 'eSiGe', 'PMOS', '17 nm', '20 nm', '31 nm', '18 nm', '18 nm', and a '20 nm' scale bar.

#	Claim Language	Accused Instrumentalities
12.1	A computing system comprising the integrated circuit of claim 1.	See Claim 1, above. Each of the '334 Patent Accused Products comprises an integrated circuit in a computing system. For example, the Exynos 990 – 7 nm microprocessor is employed in Samsung mobile devices as part of a computing system.
13.1	13. An integrated circuit, comprising:	To the extent the preamble of Claim 13 is limiting, each of the '334 Patent Accused Products, including for example the, Samsung Exynos 990 – 7 nm processor, comprises an integrated circuit. ¹⁴⁵

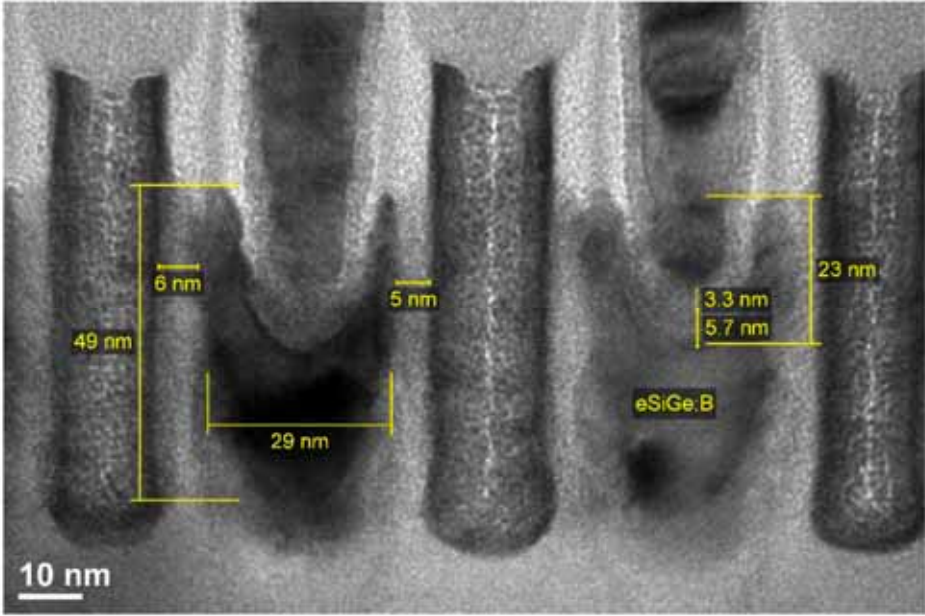
¹⁴⁵ TechInsights Report ACE-2003801, pg. 11.

#	Claim Language	Accused Instrumentalities
		
13.2	a fin structure comprising semiconductor material, wherein the fin structure has top and side surfaces;	Each of the '334 Patent Accused Products comprises a fin structure comprising semiconductor material, wherein the fin structure has top and side surfaces. For example, the fins contained in the Samsung Exynos 990 – 7 nm microprocessors are formed from the silicon substrate and have top and side surfaces that are non-planar.¹⁴⁶

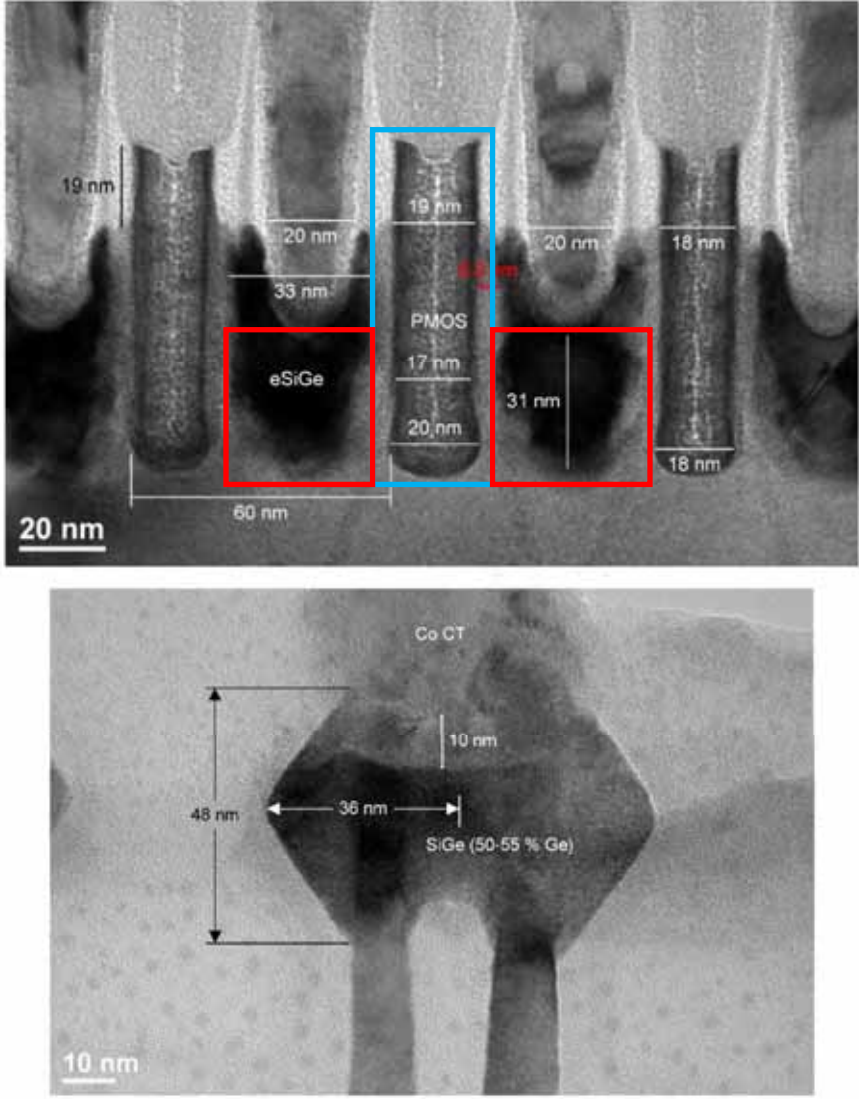
¹⁴⁶ TechInsights Report ACE-2003-801, pg. 27.

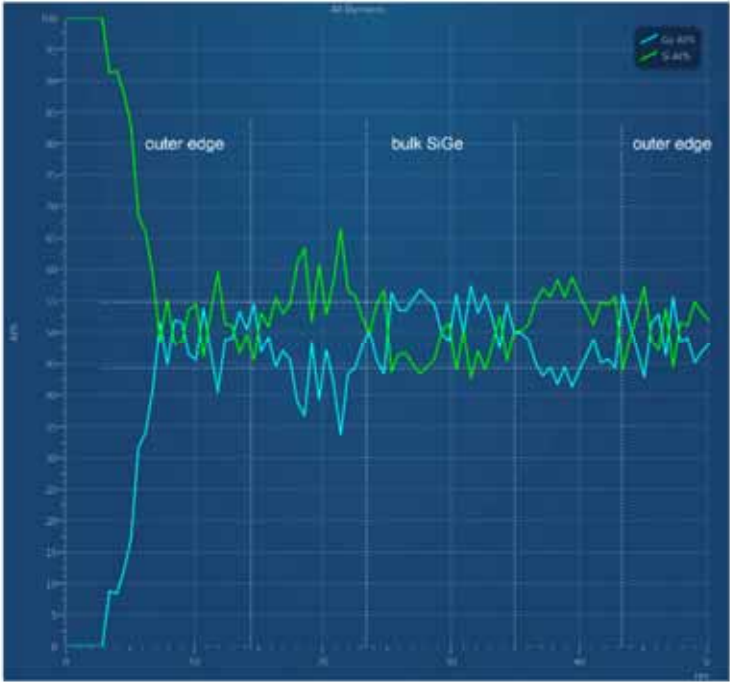
#	Claim Language	Accused Instrumentalities
		
13.3	a gate structure on the top and side surfaces of the fin structure;	Each of the '334 Patent Accused Products comprises a gate structure on the top and side surfaces of the fin structure. For example, the Samsung Exynos 990 – 7nm microprocessor comprises a gate structure on the top and side surfaces of the fin structure.¹⁴⁷

¹⁴⁷ TechInsights Report ACE-2003-801, pg. 29.

#	Claim Language	Accused Instrumentalities
		 A cross-sectional scanning electron micrograph (SEM) of a semiconductor device. The image shows a series of vertical structures (fins) separated by gaps. Yellow dimension lines indicate various measurements: a fin height of 49 nm, a fin width of 6 nm, a gap width of 29 nm, a fin width of 5 nm, a fin height of 3.3 nm, a fin width of 5.7 nm, and a gap width of 23 nm. A scale bar at the bottom left indicates 10 nm. A label 'eSiGe:B' is visible on one of the fins.
13.4	a source structure to one side of the gate structure and abutting the fin structure, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon	Each of the '334 Patent Accused Products further comprises a source structure to one side of the gate structure and abutting the fin structure, the source structure including a first portion, the first portion including germanium at a concentration of at least 50 atomic percent throughout the first portion, wherein the first portion is in direct contact with a surface that consists essentially of silicon. For example, in the Samsung Exynos 990 – 7 nm microprocessor, the source and drain pairs (shown in red) are formed to one side of the gate structure (shown in blue) and abutting the fin structure.¹⁴⁸

¹⁴⁸ TechInsights Report ACE-2003-801, pg. 19.

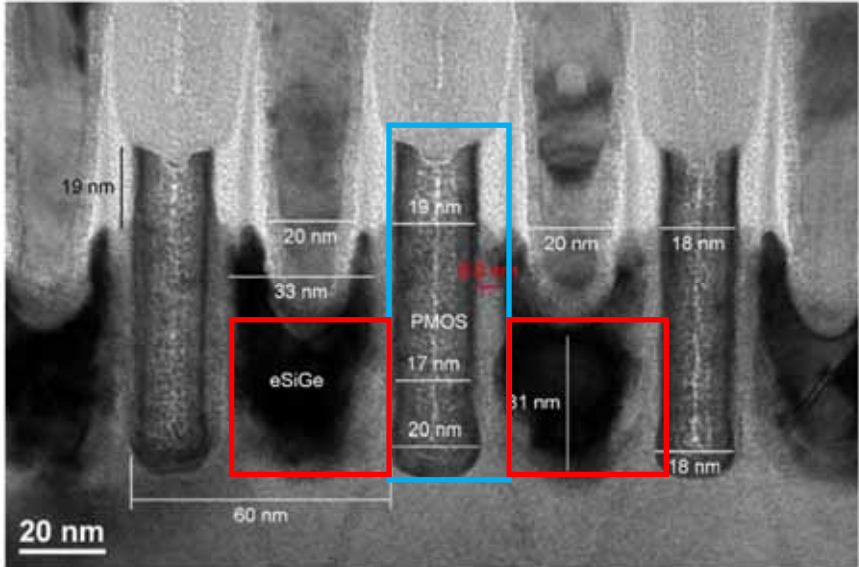
#	Claim Language	Accused Instrumentalities
	portion is in direct contact with a surface that consists essentially of silicon;	 The top image is a cross-sectional SEM micrograph showing a series of vertical structures. The structures are labeled with dimensions: 19 nm, 20 nm, 33 nm, 17 nm, 20 nm, 31 nm, and 18 nm. A 20 nm scale bar is at the bottom left. The bottom image is a higher magnification view of a single structure, showing a Co CT layer (10 nm thick) on top of a SiGe (50-55 % Ge) layer. Dimensions of 48 nm and 36 nm are indicated. A 10 nm scale bar is at the bottom left.

#	Claim Language	Accused Instrumentalities
		Additionally, on information and belief, the source is comprised of an embedded SiGe material, which further comprises a portion that has a Germanium concentration of at least 50% that is in direct contact with a silicon surface.¹⁴⁹ 

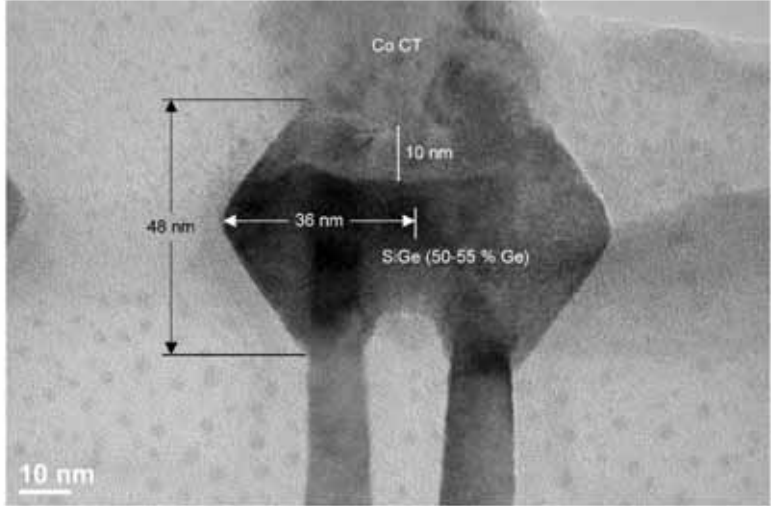
¹⁴⁹ TechInsights Report ACE-2003-801, pg. 6, 19, 27-29.

#	Claim Language	Accused Instrumentalities
13.5	a drain structure to an opposite side of the gate structure and abutting the fin structure, the drain structure including a second portion, the second portion including germanium at a concentration of at least	Each of the '334 Patent Accused Products comprises a drain structure to an opposite side of the gate structure and abutting the fin structure, the drain structure including a second portion, the second portion including germanium at a concentration of at least 50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon. For example, in the Samsung Exynos 990 – 7 nm microprocessor, the drain structure is formed opposite to the gate structure (shown in blue) and abutting the fin structure.¹⁵⁰ Additionally, on information and belief, the drain is comprised of an embedded SiGe

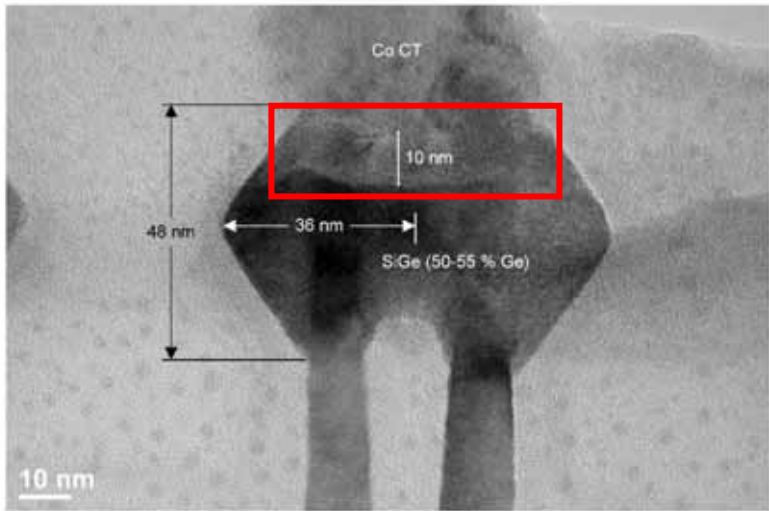
¹⁵⁰ TechInsights Report ACE-2003-801, p. 19.

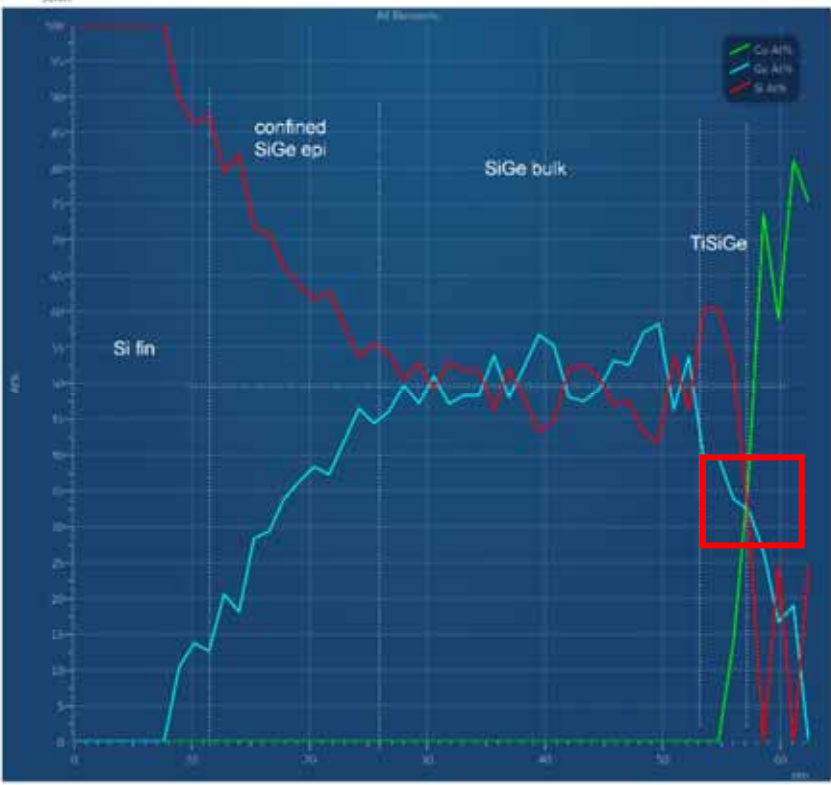
#	Claim Language	Accused Instrumentalities
	50 atomic percent throughout the second portion, wherein the second portion is in direct contact with the surface that consists essentially of silicon;	material, which further comprises a portion that has a Germanium concentration of at least 50% that is in direct contact with a silicon surface of the fin structure.¹⁵¹  The image is a cross-sectional scanning electron micrograph (SEM) of a semiconductor device. It shows a series of vertical fin structures on a substrate. Key features and dimensions labeled include: Dimensions: 19 nm, 20 nm, 33 nm, 17 nm, 20 nm, 31 nm, 18 nm, 60 nm, and a 20 nm scale bar. Layers: A central layer is labeled "PMOS". Below it, a layer is labeled "eSiGe". Annotations: A blue box highlights a specific fin structure. Two red boxes highlight regions of the device, one labeled "eSiGe" and another labeled "31 nm".

¹⁵¹ TechInsights Report ACE-2003-801, pp. 6, 19, 27-29.

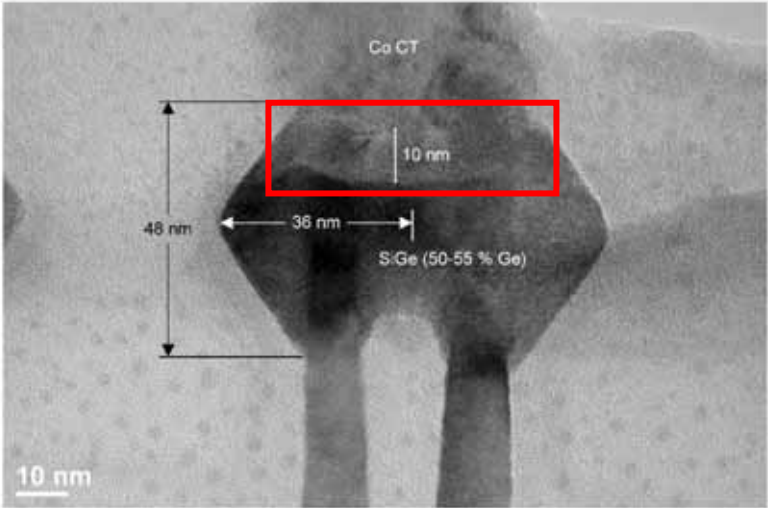
#	Claim Language	Accused Instrumentalities
		
13.6	a first contact structure on the first portion of the source structure and including a metal-germanide; and	Each of the '334 Patent Accused Products comprises a first contact structure on the first portion of the source structure and including a metal-germanide. For example, in the Samsung Exynos 990 – 7 nm microprocessor, a trinitride barrier comes into contact with a first contact structure on the embedded SiGe material of the source structure.¹⁵² When heated during the manufacture of the '334 Patent Accused Products, this creates a metal germanide on the first portion of the source structure.

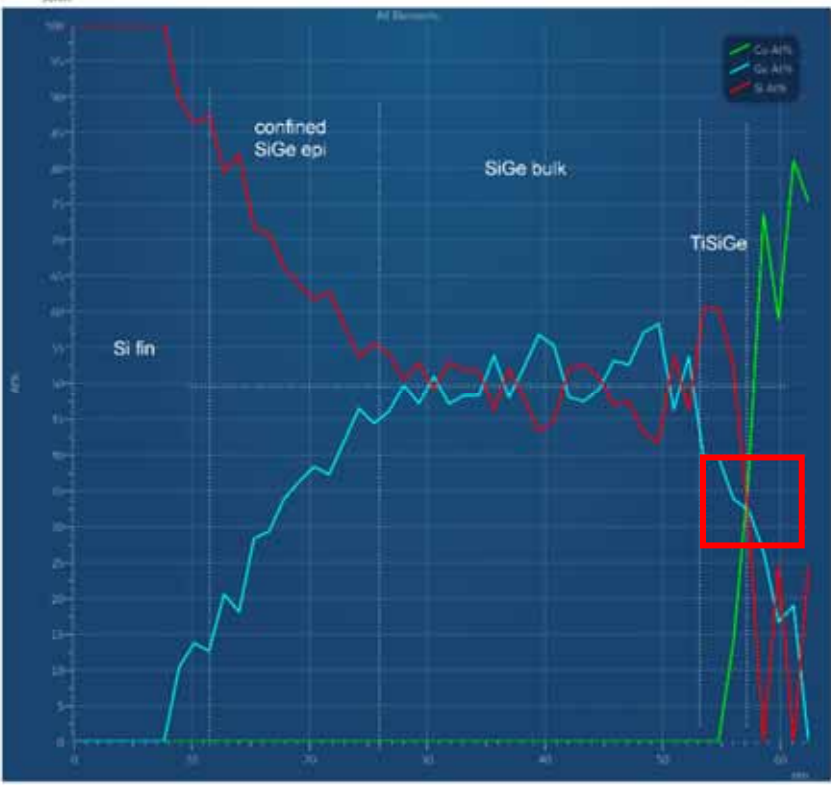
¹⁵² TechInsights Report ACE-2003-801, pp. 27, 28.

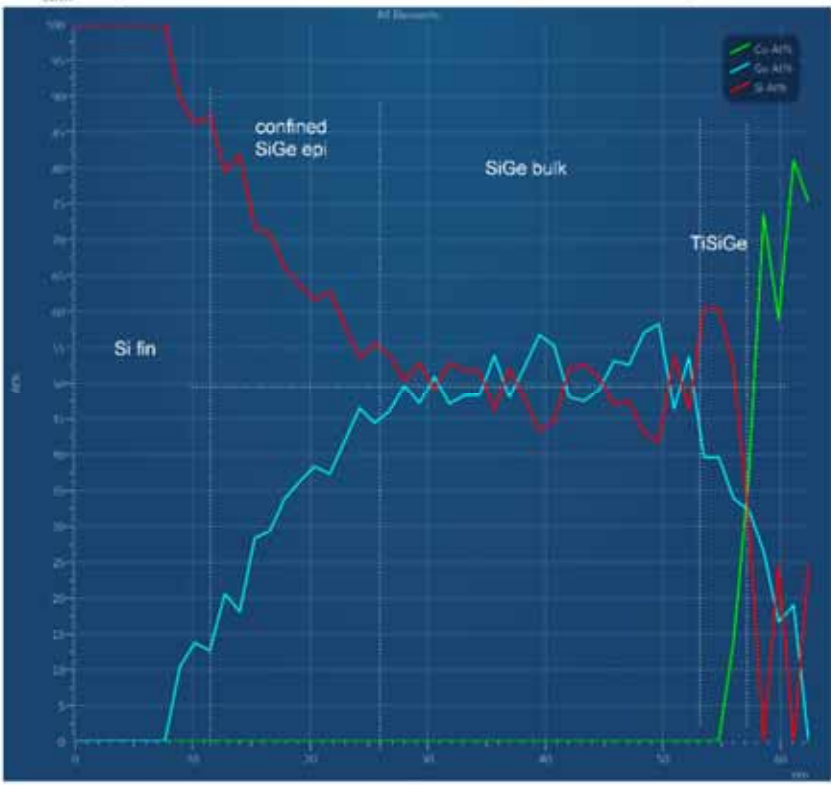
#	Claim Language	Accused Instrumentalities
		 A cross-sectional transmission electron micrograph (TEM) of a device. The image shows a central dark region labeled 'S:Ge (50-55 % Ge)' with a width of 36 nm. Above this region is a layer labeled 'Co CT' with a thickness of 10 nm, which is highlighted by a red rectangular box. The total height of the central structure is 48 nm. A scale bar in the bottom left corner indicates 10 nm.

#	Claim Language	Accused Instrumentalities
		
13.7	a second contact structure on the second portion of the drain structure and including a metal-germanide.	Each of the '334 Patent Accused Products comprises a second contact structure on the second portion of the drain structure and including a metal-germanide. For example, in the Samsung Exynos 990 – 7 nm microprocessor, a trinitride barrier comes into contact with a second contact structure on the embedded SiGe material of the drain structure.¹⁵³ When heated during the manufacture of the '334 Patent Accused Products, this creates a metal germanide on the second portion of the drain structure.

¹⁵³ TechInsights Report ACE-2003-801, pp. 27, 28.

#	Claim Language	Accused Instrumentalities
		 A cross-sectional transmission electron micrograph (TEM) of a device structure. The image shows a central dark region labeled 'S:Ge (50-55 % Ge)' at the bottom, which is wider at the base and tapers upwards. Above this is a lighter, textured region labeled 'Co CT'. Dimensions are indicated with arrows: a vertical arrow on the left indicates a height of 48 nm for the central dark region, and a horizontal arrow indicates a width of 36 nm at its base. A red rectangular box highlights a portion of the 'Co CT' layer, with a vertical dimension line indicating a height of 10 nm. A scale bar in the bottom left corner represents 10 nm.

#	Claim Language	Accused Instrumentalities
		
14.1	The integrated circuit of claim 13,	See Claim 13, above.
14.2	wherein the surface that consists essentially of silicon is one of a surface of a bulk silicon substrate or a surface of the silicon	On information and belief, each of the '334 Patent Accused Products comprises a surface that consists essentially of silicon and is one of a surface of bulk silicon substrate or a surface of the silicon layer of a silicon-on-insulator substrate.

#	Claim Language	Accused Instrumentalities
	layer of a silicon-on-insulator substrate.	For example, on information and belief, the fin is comprised of bulk silicon substrate.¹⁵⁴ 

¹⁵⁴ TechInsights Report ACE-2003-801, pp. 18, 27, 28.

