

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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WESTERN DIGITAL TECHNOLOGIES, INC.  
Petitioner

v.

SHAMROCK INNOVATIONS, LLC  
Patent Owner

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Case No. IPR2023-00842  
Patent No. 9,535,454

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**PETITION FOR *INTER PARTES* REVIEW**

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**EXHIBITS**

- 1001 U.S. Patent No. 9,535,454 to Ahern et al. (“’454 patent”)
- 1002 Prosecution History of the ’454 patent (“’454 Prosecution History”)
- 1003 Declaration of Michael Caloyannides, Ph.D.
- 1004 Curriculum Vitae of Michael Caloyannides, Ph.D.
- 1005 U.S. Patent No. 6,289,386 to Vangemert (“Vangemert”)
- 1006 U.S. Patent No. 5,179,661 to Copeland, III et al. (“Copeland”)
- 1007 U.S. Patent No. 5,717,870 to Dobson (“Dobson”)
- 1008 U.S. Patent No. 6,005,414 to Reay (“Reay”)
- 1009 U.S. Patent No. 6,088,752 (“’752 patent”)
- 1010 U.S. Patent No. 6,070,214 (“’214 patent”)
- 1011 U.S. Patent No. 8,060,675 (“’675 patent”)
- 1012 Excerpt from Prosecution History of the ’675 patent

## **I. INTRODUCTION**

Western Digital Technologies, Inc. (“Petitioner” or “WD”) seeks *inter partes* review (“IPR”) under 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 to invalidate claims 1, 2, 3, 4, 6, 7, 15, 16, and 17 (“challenged claims”) of U.S. Patent No. 9,535,454 (“’454 patent”; EX. 1001), titled “COMPUTING MODULE WITH SERIAL DATA CONNECTIVITY” owned by Shamrock Innovations, LLC (“Shamrock” or “Patent Owner”).

As explained below, the prior art presented renders the challenged claims unpatentable, and Petitioner is reasonably likely to prevail on at least one asserted ground. Petitioner respectfully requests the Board institute an IPR and cancel the challenged claims.

## **II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104**

### **A. Grounds for Standing Under 37 C.F.R. § 42.104(a)**

Petitioner certifies the ’454 patent is available for IPR. Petitioner is not barred or estopped from requesting this review.

### **B. Challenge/Relief Requested Under 37 C.F.R. § 42.22(a)(1) and 42.104(b)(1)-(2)**

This Petition is based on the below-summarized grounds. All references to 35 U.S.C. §§ 102-103 are pre-AIA.

| <b>Ground</b> | <b>Claims</b>                | <b>Basis for Unpatentability</b>                                                                       |
|---------------|------------------------------|--------------------------------------------------------------------------------------------------------|
| 1             | 1, 2, 3, 4, 7, 15,<br>16, 17 | Obvious under 35 U.S.C. § 103 over U.S. Patent Nos. 6,289,386 (“Vangemert”) and 5,179,661 (“Copeland”) |
| 2             | 4                            | Obvious under 35 U.S.C. § 103 over Vangemert, Copeland, and U.S. Patent No. 5,717,870 (“Dobson”)       |
| 3             | 6                            | Obvious under 35 U.S.C. § 103 over Vangemert, Copeland, and U.S. Patent No. 6,005,414 (“Reay”)         |
| 4             | 1, 2, 3, 4, 7, 16            | Obvious under 35 U.S.C. § 103 over Dobson and Copeland                                                 |
| 5             | 6                            | Obvious under 35 U.S.C. § 103 over Dobson, Copeland, and Reay                                          |
| 6             | 15, 17                       | Obvious under 35 U.S.C. § 103 over Dobson, Copeland, and Vangemert                                     |

### III. OVERVIEW OF THE ART AND THE '454 PATENT

#### A. Background

The following background is based on the Declaration of Michael Caloyannides, Ph.D. (EX 1003) and is supported by various prior art references (see EX. 1005, EX. 1006, EX. 1007, and EX. 1008).

Serial communication has been known as far back as the invention of Morse code, which transmitted data one bit at a time, in the form of a dot or dash. EX. 1003, ¶ 19. As digital devices became more prolific and operational speeds increased, devices were designed with parallel data busses to increase device bandwidth. *Id.* For devices separated by some distance, however, the use of serial data communication advantageously reduced cost, weight, interference, and electrical loading issues associated with parallel data communications. *Id.*, ¶ 20.

Sending data between parallel devices using serial communications requires converting parallel data to serial data, and vice versa. *Id.*, ¶ 22. Such conversion has been commonplace for decades. *Id.* Received parallel data can be stored in a receive buffer until it can be read out of the buffer. *Id.*, ¶ 24. To prevent buffer overflow, flow control functions may be used to stop data flow between devices until the buffer capacity is sufficient to continue without overflowing the buffer. *Id.*

**B. The '454 Patent**

The '454 patent issued on January 3, 2017, from U.S. Patent Application No. 13/652,823, filed October 16, 2012. EX 1001, 1. The '454 patent purports to claim priority to Application No. 13/240,773, filed on September 22, 2011, now U.S. Patent No. 8,291,140, which is a continuation of Application No. 12/644,511, filed December 22, 2009, now U.S. Patent No. 8,060,675 ("'675 patent"), which is a continuation of Application No. 11/300,131, filed December 13, 2005, now U.S. Patent No. 7,657,678, which is a continuation of Application No. 09/559,678, filed April 27, 2000, now U.S. Patent No. 7,734,852, which is a continuation-in-part of Application No. 09/130,057, filed August 6, 1998, now U.S. Patent No. 6,088,752 ("'752 patent"), and a continuation-in-part of Application No. 09/130,058, filed August 6, 1998, now U.S. Patent No. 6,070,214 ("'214 patent"). *Id.* The '454 patent also claims priority to provisional Application No. 60/198,317, filed April 19, 2000. *Id.* The earliest date to which the '454 patent can claim priority is August 6, 1998. *Id.* Petitioner does not concede the '454 patent's priority claims are supported.

The '454 patent generally discloses facilitating communication between two parallel busses across a serial link such that the serial link is "transparent" to software on the communicating devices. EX. 1001, col. 3:59-67. Transparency is purportedly accomplished using the "Split-Bridge™" technology disclosed in at

least the '454 patent's parent Application Nos. 09/130,057 (now the '752 patent) (EX. 1009) and 09/130,058 (now the '214 patent) (EX. 1010).

The '214 patent explains the "Split-Bridge™" technology includes two separate interface devices operable to "(a) send bus-related information serially through the link in a format different from that of the first bus and the second bus, (b) approve an initial exchange between the first bus and the second bus in response to a pending transaction having a characteristic signifying a destination across the bridge, and (c) allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus compatible devices on the second bus. . . ." EX. 1010, col. 3:45-54. Thus, the Split-Bridge™ technology required specific steps to provide the desired "transparency" between devices. The '214 patent describes this process in detail. *See, e.g., id.*, cols. 12:29 – 18:63. The '752 patent discloses similar subject matter.

Disregarding the Split-Bridge™-specific protocols and implementations of the '454 patent and parent '214 and '752 patents, claim 1 of the '454 patent covers a general serial interface with flow control. Claim 1 is summarized as follows: (a) converting received serial data into deserialized data followed by decoding; (b) storing decoded data in a first buffer; (c) converting parallel data to serial data for storage in a second buffer and transmission over a serial link; and (d) generating and transmitting a flow control signal when the first buffer reaches a fill amount.

These general concepts were well known in the art at the time of the claimed invention. EX. 1003, ¶¶ 18-24.

The '454 patent issued after a brief prosecution. The Examiner rejected claim 1 (original claim 107) as obvious over U.S. Patent Nos. 5,613,141 and 6,192,422. EX. 1002 at 180 – 193. Following the Applicant's amendment of claim 1, the Examiner allowed the claims. *Id.* at 205-251, 266-270.

#### **IV. THE PRIOR ART**

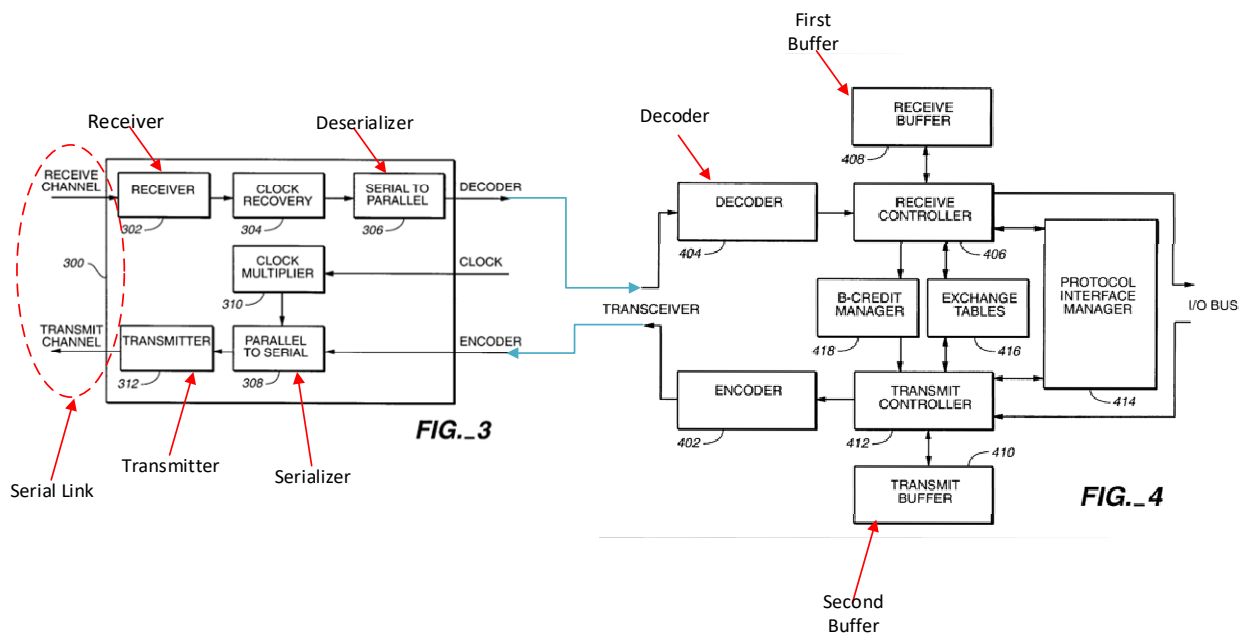
The earliest possible priority date of the '454 patent is August 6, 1998. As shown below, the applied references are prior art to the '454 patent under § 102(a), (b), and/or (e).

##### **A. Vangemert (EX 1005)**

Vangemert is prior art to the '454 patent under § 102(e) because it issued from a patent application filed on May 11, 1998, before the '454 patent's purported priority date. The examiner did not consider Vangemert. EX. 1001, 1-2.

Vangemert describes a network interface, coupled to one or more devices via a serial communication link, that implements a low latency algorithm for determining buffer credit (i.e., flow control). EX. 1003, ¶ 27. Vangemert has a serial transceiver module that couples a node device to a serial communication link. *Id.* Vangemert's transceiver includes a receiver, a transmitter, and a deserializer (serial to parallel converter 306). *Id.* The transceiver is coupled to a

node device's input-output ("I/O") bus via a network interface unit, which includes a decoder 404 for decoding deserialized data from the transceiver 300, a receive buffer 408, and a transmit buffer 410. *Id.* A modified combination of FIGs. 3 and 4 shows several key features related to the '454 patent claims.

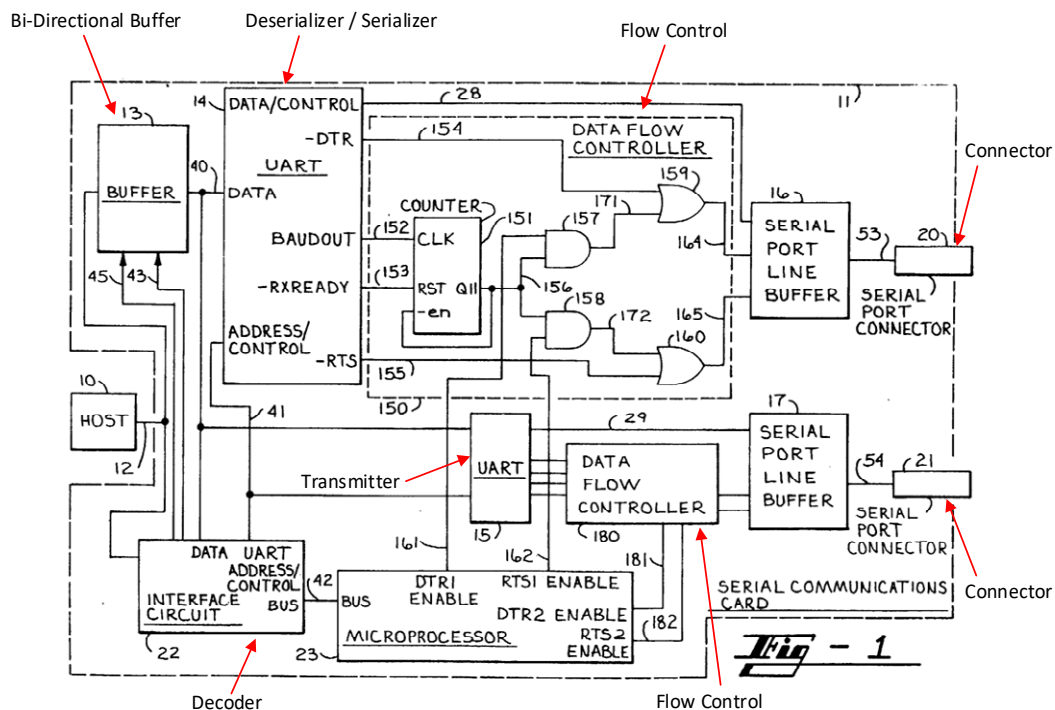


***Vangemert Modified Combined FIGs. 3 and 4 (Annotated)***

**B. Copeland (EX 1006)**

Copeland is prior art under § 102(b) because it issued on January 12, 1993, more than one year before the '454 patent's purported priority date. EX. 1006, 1. The examiner did not consider Copeland. EX. 1001, 1-2.

Copeland is directed to a data flow controller for monitoring and controlling serial communication between a remote transmitter and a host device. EX. 1003, ¶ 29. Copeland discloses a serial communications card 11, which includes a “host data buffer 13, two parallel-serial converters such as universal asynchronous receiver-transmitters (UARTs) 14 and 15 . . . two data flow controllers 150 and 180, two serial port line buffers 16 and 17, [and] two serial port connectors 20 and 21.” *Id.* Annotated Figure 1 illustrates the general architecture of Copeland’s serial communications card.



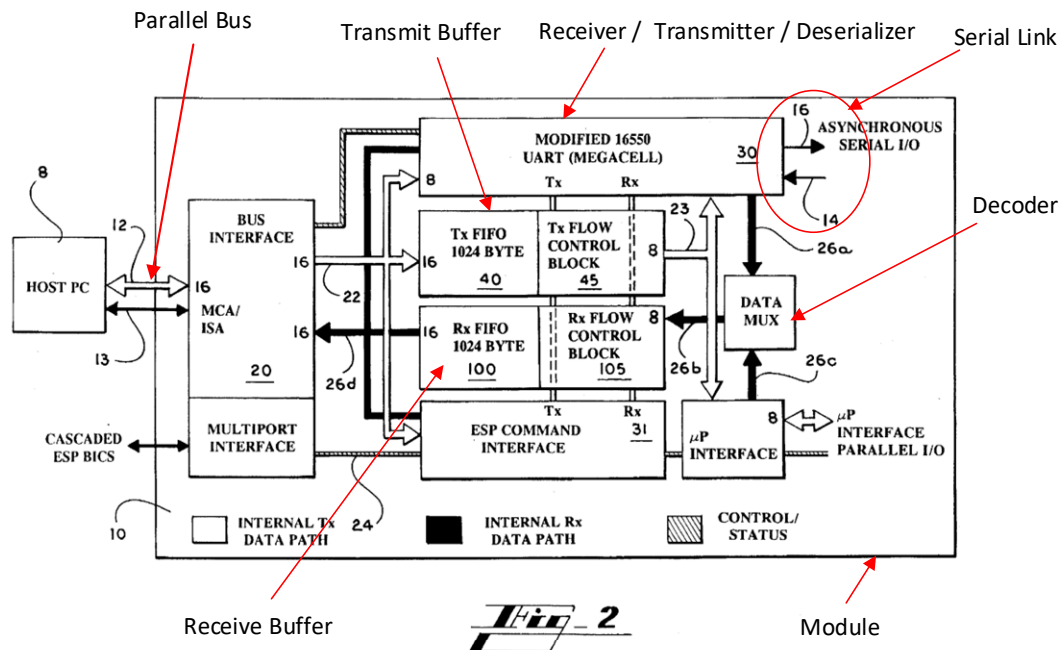
**Copeland FIG. 1 (Annotated)**

**C. Dobson (EX 1007)**

Dobson is prior art to the '454 patent under § 102(a) because it was patented on February 10, 1998, before the invention of the '454 patent. EX. 1007, 1.

Dobson is also prior art under § 102(e) because it issued from a patent application filed on October 26, 1994, before the '454 patent's purported priority date. *Id.* The examiner did not consider Dobson. EX. 1001, 1-2.

Dobson is directed to an improved input/output FIFO buffering device for use with a universal asynchronous receiver/transmitter ("UART"). EX. 1003, ¶ 31. This allows for communication application programs to support high speed transfer rates while being backwards compatible with software written for conventional serial port devices. *Id.* FIFO buffers provide buffering for serial to parallel and parallel to serial converters. *Id.* The serial interface device 10 also outputs a flow control signal when the receive buffer's fill level reaches a predetermined threshold. *Id.* Annotated Dobson Figure 1 (below) highlights relevant features.



**Dobson FIG. 2 (Annotated)**

**D. Reay (EX 1008)**

Reay is prior art under § 102(e) because it issued from a patent application filed on June 3, 1997, before the '454 patent's purported priority date. EX. 1008, 1. The examiner did not consider Reay. EX 1001, 1-2.

Reay discloses a “mixed-mode multi-protocol serial interface driver for conforming output signals to one of a plurality of selectable electrical interface standards.” EX. 1003, ¶ 34. The output terminals 106 and 108 provide inverted and non-inverted output signals, to create a differential output. *Id.*

## **V. LEVEL OF ORDINARY SKILL IN THE ART**

A PHOSITA at the time of the alleged invention of the '454 patent would have had at least a bachelor's degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communication within or between computing devices or systems. EX. 1003, ¶ 37. More education can supplement practical experience and vice versa. *Id.*

## **VI. CLAIM CONSTRUCTION UNDER 37 C.F.R. §§ 42.104(B)(3)**

Claim terms should be construed according to the *Phillips* standard and given their ordinary and customary meaning as understood by a PHOSITA at the time of the invention, in light of the claim language, the specification, and the prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc); 37 C.F.R. § 42.100.<sup>1</sup>

### **A. “Decoder”**

Claim 1 recites “a decoder configured to decode the deserialized data.” The terms “decoder” and “decode” are not in the '454 patent specification. The term

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<sup>1</sup> Petitioner reserves its rights to raise claim construction and other arguments in district court as relevant to those proceedings. For example, a comparison of claims to an accused product may raise claim construction controversies not present here. Also, challenges under 35 U.S.C. § 112 are not applicable here.

“decoder” is included in the ’214 patent, which the ’454 patent incorporates by reference. The ’214 patent states “[u]pon receipt, decoder 32 restores the frames into the original 38-bit format and loads the last two described cycles onto the stack of register 24.” EX. 1010, col. 10:50-54. Based on the ’214 patent’s disclosure, the decoder is understood to restore received data into its desired format. EX 1003, ¶ 40.

**B. “Generate a Clock Signal . . .”**

Dependent claim 17 recites “the module is further configured to ***generate a clock signal*** for use by the module, using the first serial data.” EX 1001, col. 11:42-43. This term does not appear anywhere in the specifications of the ’454 patent, its parent applications, or incorporated applications. *See id.*; EX 1009; EX. 1010. During prosecution of the related ’675 patent (EX. 1011), the applicant added a similar limitation by amendment and cited portions of the related ’214 patent in support. EX. 1012, 4, 12 (citing U.S. Application No. 09/130,058 (now the ’214 patent (EX 1010)), cols. 6:33-46, 8:38-53)). The cited portions of the ’214 patent, however, do not include “generate a clock signal . . .” and do not inform its intended meaning. *See* EX 1010, cols. 6:33-46, 8:38-53; EX 1003, ¶¶ 41-42.

Without any other helpful intrinsic evidence, a PHOSITA is left to derive meaning from the language and context of the claim. In particular, claim 17 recites “generate a clock signal,” not out of thin air or in the absence of additional

information, but rather, “*using the first serial data.*” EX 1003, ¶ 42. Thus, in the context of claim 17, a PHOSITA would have understood that “generat[ing] a clock signal . . . using first serial data” would include ways of producing a clock signal by *using* the first serial data, such as by extracting or recovering a clock signal *from* (i.e., using) the first serial data. *Id.*

## **VII. AT LEAST ONE CHALLENGED CLAIM IS UNPATENTABLE**

The below prior art combinations teach each limitation of the challenged claims, rendering them obvious.

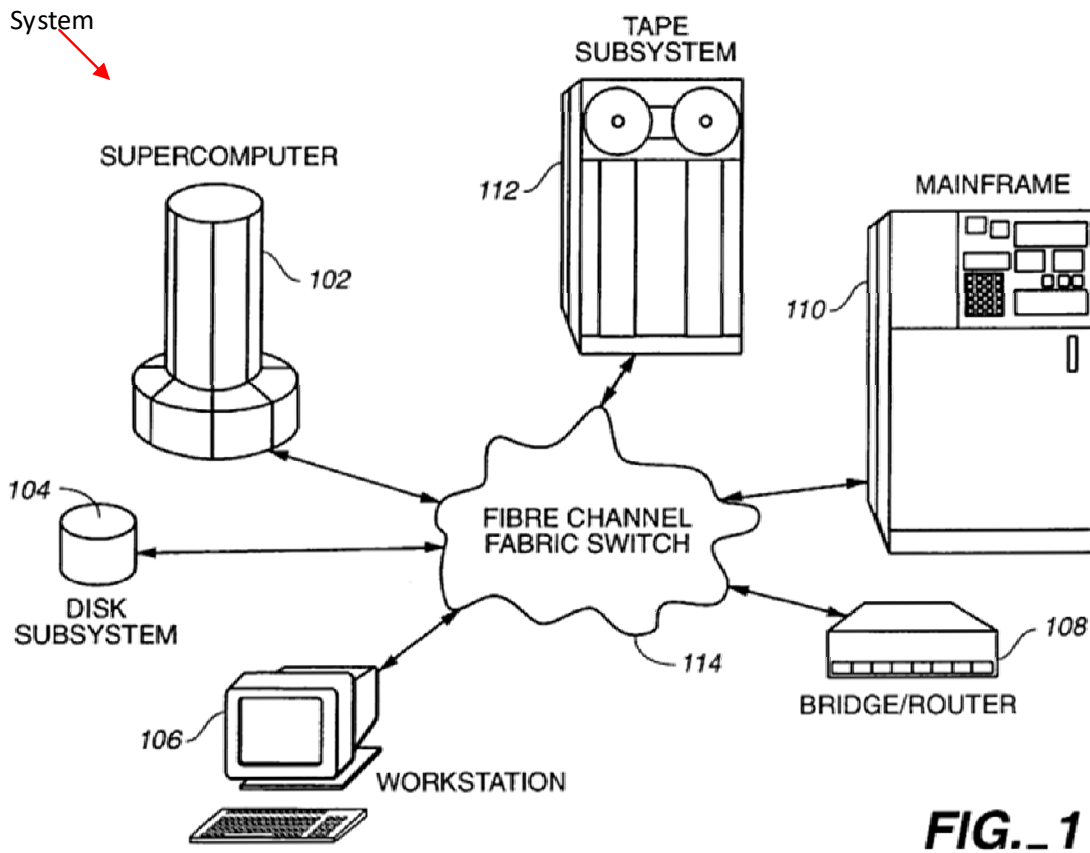
### **A. Ground 1: Claims 1, 2, 3, 4, 7, 15, 16, and 17 are Obvious Over Vangemert and Copeland**

#### **1. Claim 1**

Claim 1 is obvious over Vangemert (EX. 1005) and Copeland (EX. 1006).

##### **a. A system, comprising:**

Vangemert teaches a system in the form of the system network shown in FIG. 1. EX. 1003, ¶ 45; EX. 1005, col. 2:58-61, FIG. 1.



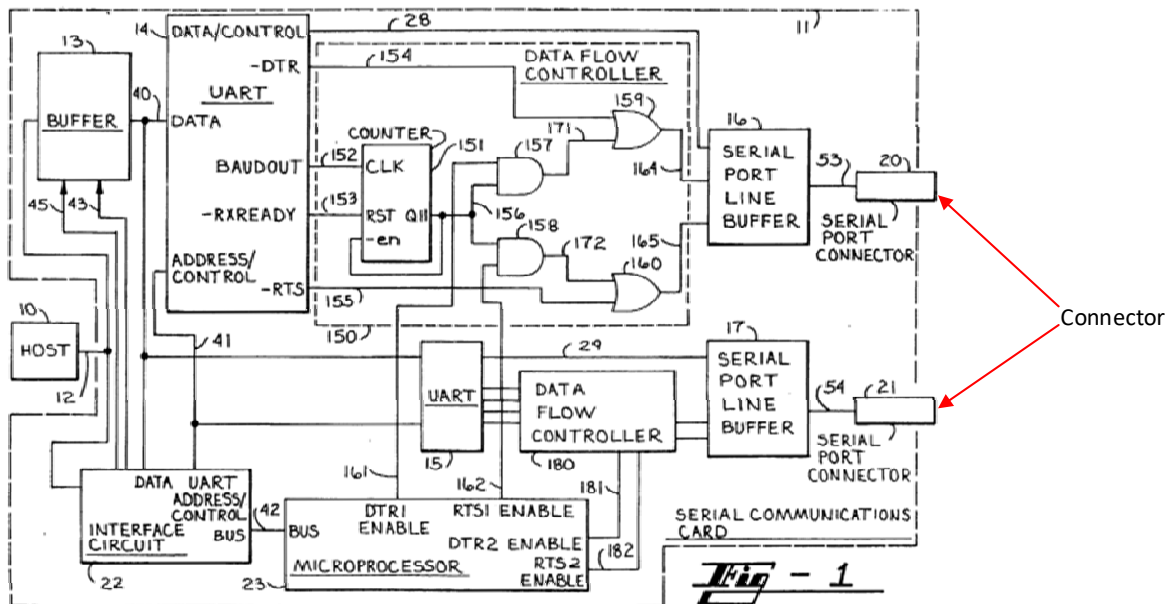
*Vangemert FIG. 1 (Annotated)*

- b. *a connector configured to be connectable to a serial link; and*

Vangemert discloses a “serial link,” explaining that nodes 102, 104, 106, 108, 110, 112 of FIG. 1 are “coupled to a central ‘fabric switch’ 114 by a serial link having a receive channel and a transmit channel.” EX. 1005, col. 2:61-63. In another example, “the nodes are coupled in an ‘arbitrated loop’ topology, in which the transmit channel from one node is directly connected to the receive channel of

the next node.” *Id.*, col. 3:5-7. A PHOSITA would have understood the FIG. 1 and FIG. 2 systems to require a connector to interconnect devices via the serial link, as described. EX. 1003, ¶ 46.

Copeland also teaches a connector connectable to a serial link. EX. 1003, ¶ 47. Copeland is directed to a dual channel asynchronous serial communications card 11 that includes “two serial port connectors 20 and 21.” EX. 1006, col. 3:49-60. Serial port connectors 20 and 21 are “connected to a communication device (not shown) such as a modem” and “preferably define an EIA RS-232-D serial interface.” EX. 1006, col. 4:31-34. RS 232-D connectors were well known in the art as common connectors for interconnecting serial devices. EX. 1003, ¶ 47. Copeland FIG. 1 shows connector 20 configured to connect the UART 14 with an external device via line 28. EX. *Id.* ¶ 48.



***Copeland FIG. 1 (Annotated)***

While Copeland teaches two serial port connectors 20 and 21, each is used for a single channel of the dual channel asynchronous serial communication card 11. *Id.* Copeland therefore discloses a “connector configured to be coupled to a serial link.”

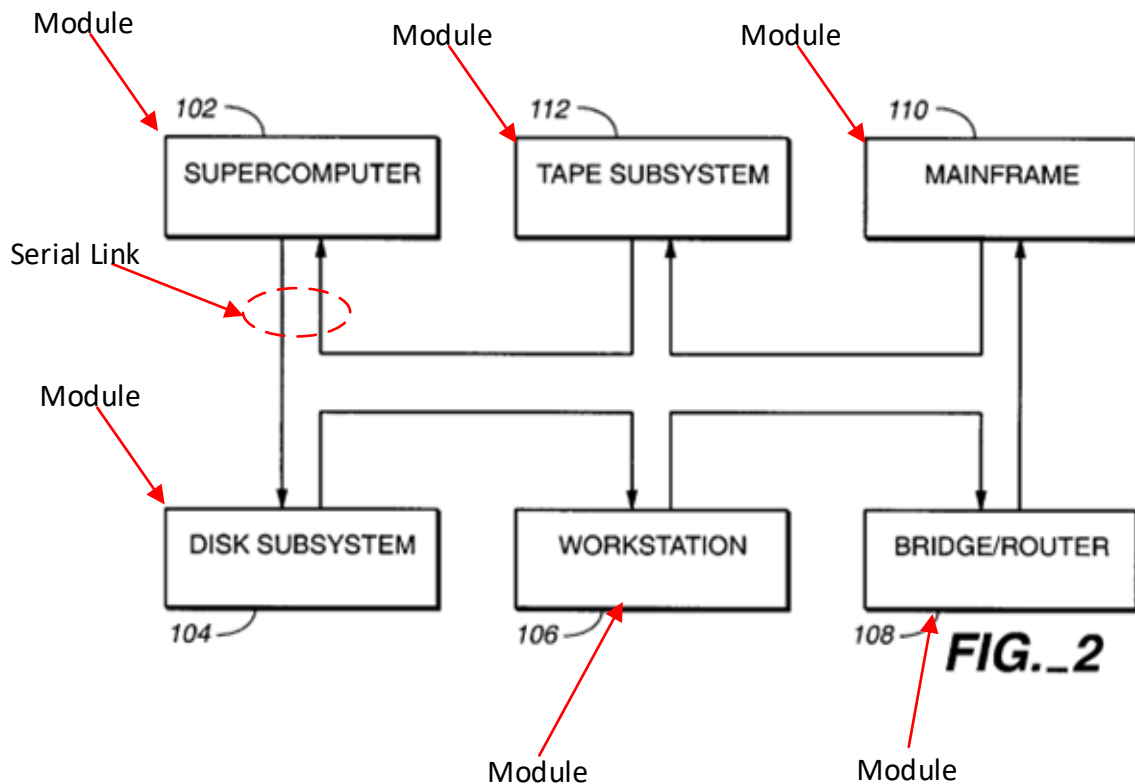
A PHOSITA would have found it obvious to combine Copeland's connector 20 with Vangemert's serial link to facilitate connections between the serial link of the individual nodes 102 – 112 with one or more external devices, such as other of the nodes 102 – 112, because both Vangemert and Copeland are directed to serial interface devices for providing serial communication between devices,

Vangemert's systems would have required such a connector, and connectors, including Copeland's connectors, were well-known. EX. 1003, ¶¶ 49-50. For at least these reasons, a PHOSITA would have been motivated to combine Copeland's well-known connector with Vangemert's serial link and would have had a reasonable expectation of success in doing so. *Id.*

- c. ***a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, and wherein the module includes:***

Vangemert's FIG. 1 shows a "fabric switch 114" configured to "transport data frames and control words from the transmit channel of a source node to the receive channel of a destination node." EX. 1005, cols. 2:65–3:1, FIG. 1.

Vangemert's FIG. 2 embodiment shows nodes "coupled in an 'arbitrated loop' topology, in which the transmit channel from one node is directly connected to the receive channel of the next node." *Id.*, col. 3:5-7, FIG. 2.

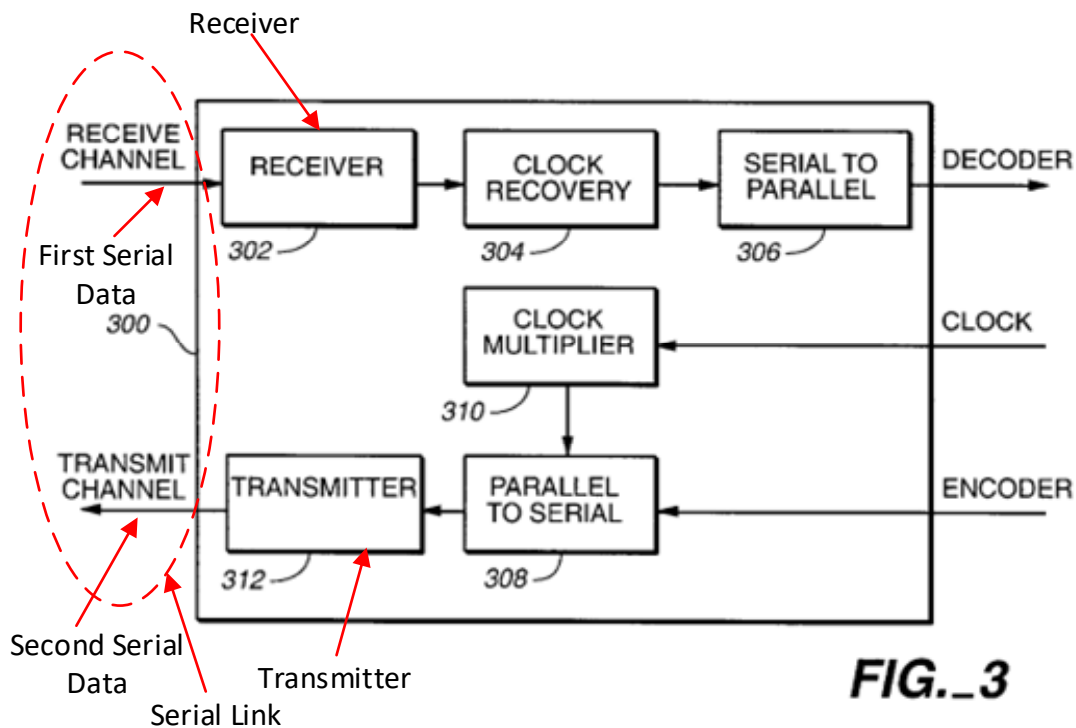


***Vangemert FIG. 2 (Annotated)***

While the embodiments of FIGS. 1 and 2 vary in connection topology, with FIG. 1's nodes in a typical star topology and FIG. 2's nodes in a daisy chain topology (arbitrated loop), both examples disclose the nodes in serial communication with each other. *Id.* ¶¶ 51-52. Thus, each node (module) receives and transmits data over the serial link. *Id.* ¶ 51. A PHOSITA would have understood that each node 102-112 includes a serial communication transceiver 300 and a network interface unit as described in Vangemert. *Id.*, ¶¶ 53-54, FIG. 4.

Vangemert's FIG. 3 "illustrates a serial communication transceiver 300 which may be used by the nodes to couple to the serial communications link.

Transceiver 300 includes a receiver 302 coupled to the receive channel to sense incoming levels.” EX. 1005, col. 3:19-23.



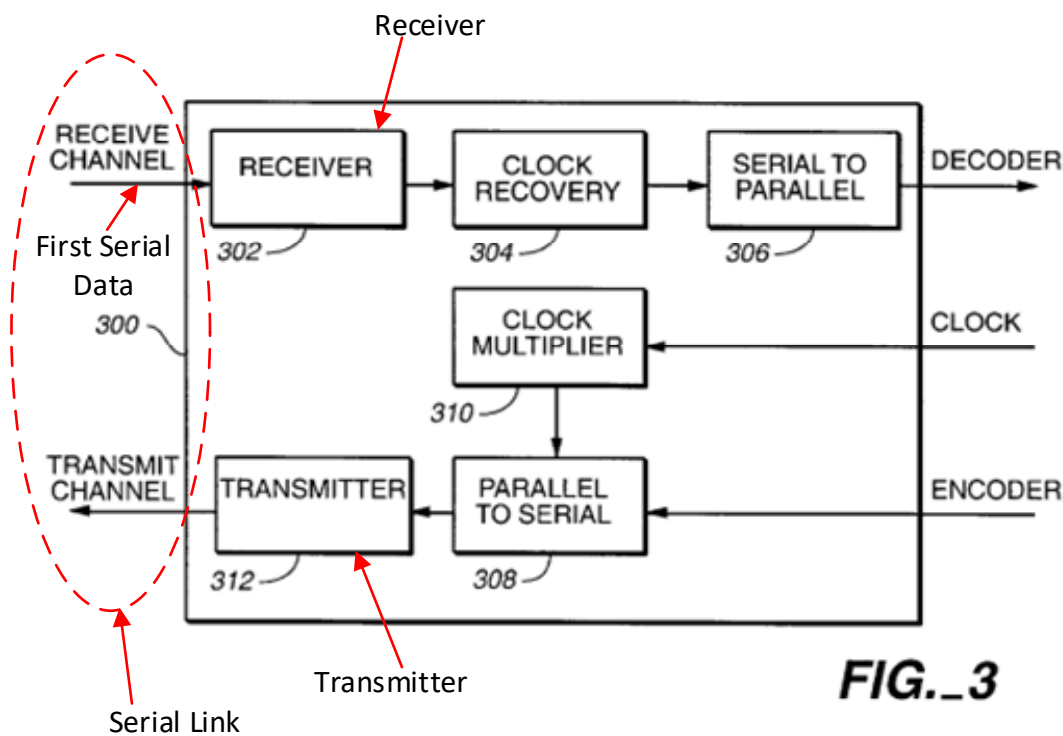
***Vangemert FIG. 3 (Annotated)***

The transceiver 300 also includes a transmitter 312 which “converts the serial bitstream into signals suitable for transport by the transmit channel.” EX. 1005, col. 3:35-36. The transceiver 300 therefore teaches that the node (module) is configured to receive first serial data (via receiver 302) and transmit second serial data (via transmitter 312) over a serial link (the receive channel and the transmit channel, respectively). EX. 1003, ¶ 54. Furthermore, a PHOSITA would have understood that interconnecting Vangemert’s nodes would have required connectors, as described above, thereby motivating the PHOSITA to combine

Copeland's known connector with Vangemert's nodes to connect the nodes to the serial link. *Id.*, ¶ 55.

**d. a receiver operable to receive the first serial data from the serial link through the connector;**

Vangemert's transceiver 300 includes a "receiver 302 coupled to the [serial link's] receive channel to sense incoming signal levels." EX. 1005, col. 3:21-23, FIG. 3. A PHOSITA would have understood that the nodes, and their associated receivers, would be connected to the serial link through a connector, such as Copeland's connector 20, described above. EX. 1003, ¶ 57. Accordingly, Vangemert combined with Copeland teaches "a receiver operable to receive the first serial data from the serial link through the connector."



**Vangemert FIG. 3 (Annotated)**

- e. *a first circuit configured to deserialize the first serial data to generate deserialized data;*

Vangemert's transceiver 300 includes a serial-to-parallel circuit 306 that receives data from the receiver via a clock recovery unit and "uses the clock signal to convert the incoming signal from serial form to parallel form." EX. 1005, col. 3:26-28, FIG. 3. Vangemert's serial-to-parallel circuit discloses the claimed "first circuit configured to deserialize the first serial data to generate deserialized data." EX 1003, ¶ 58.

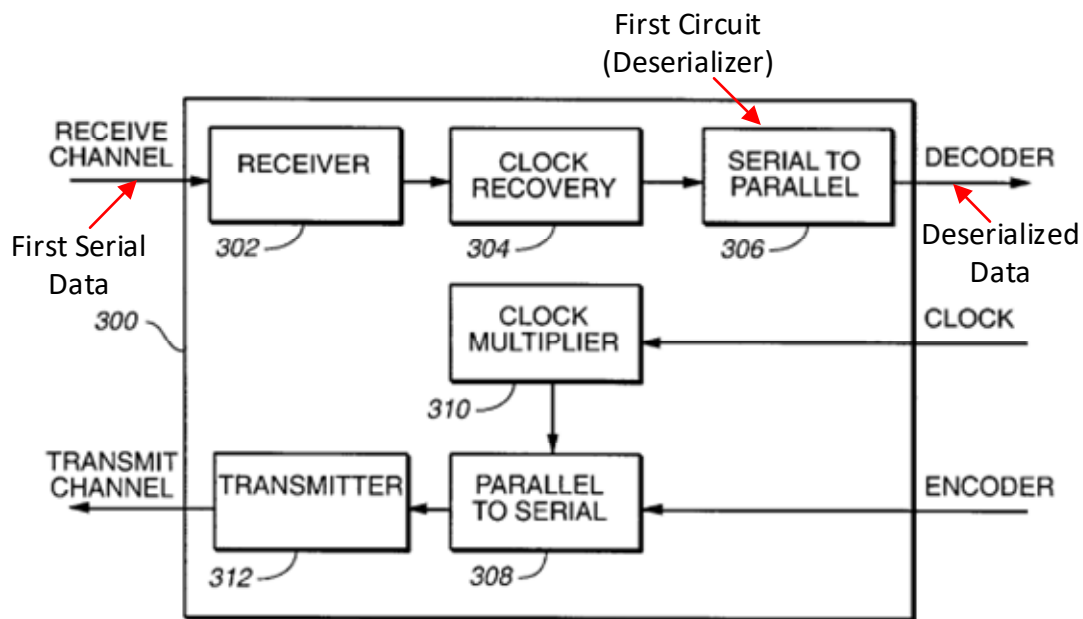
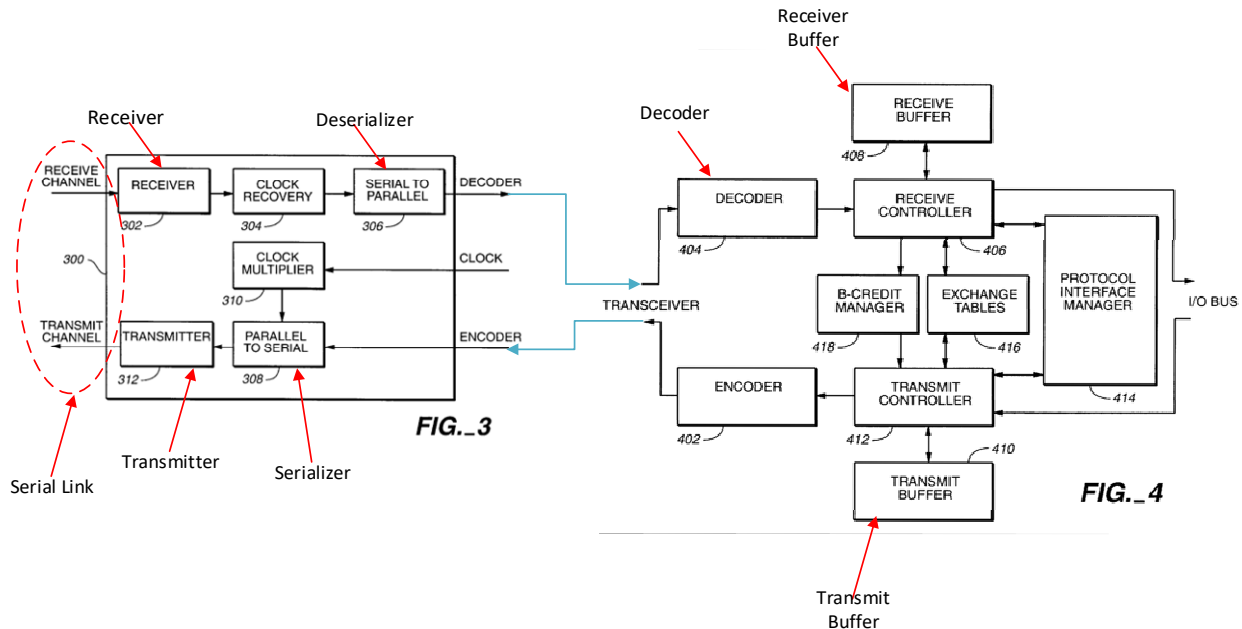


**FIG.\_3**

***Vangemert FIG. 3 (Annotated)***

- f. *a decoder configured to decode the deserialized data;*

Vangemert illustrates the serial to parallel converter 306 (deserializer) outputting data to a decoder (404), as shown in combined FIGs. 3 and 4 below.

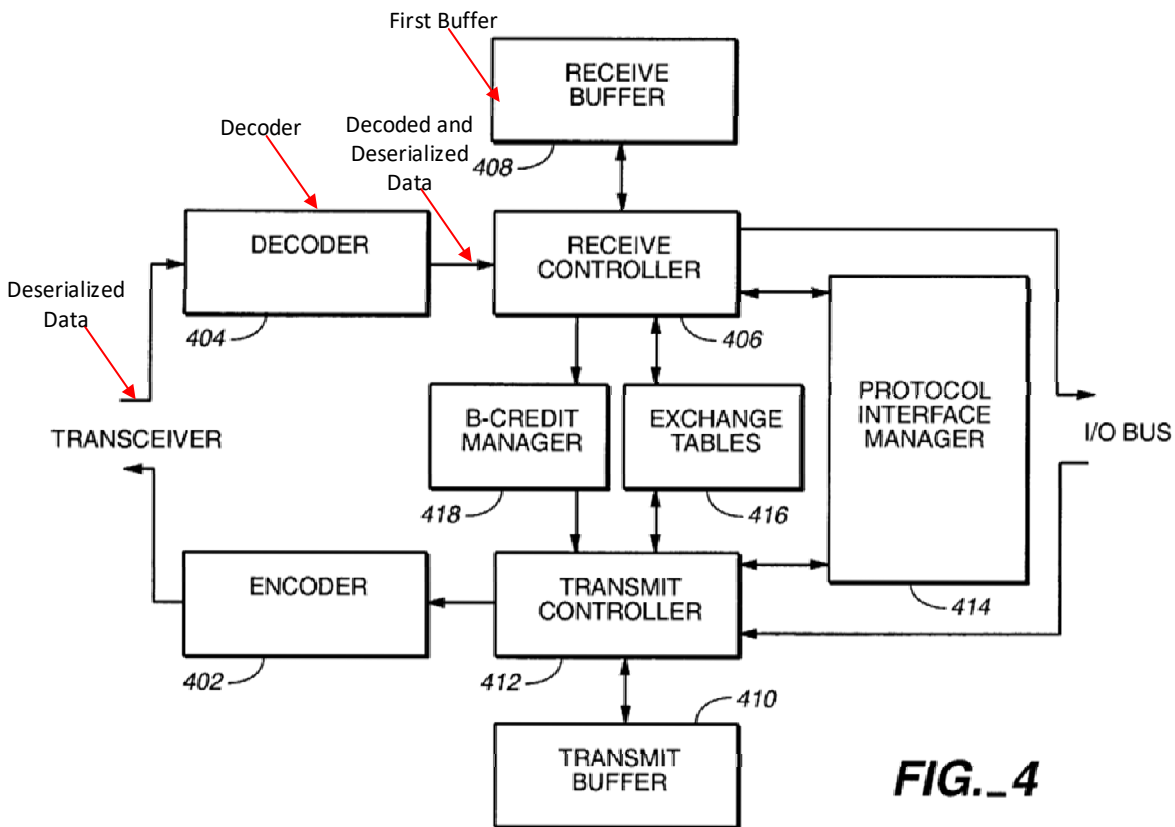


### ***Vangemert Combined FIGs. 3 and 4 (Annotated)***

Vangemert’s serial to parallel “converter 306 outputs one 10-bit channel codeword at a time. The output from the converter 306 is sent to a decoder.” EX. 1005, col. 3:28-30. “Encoder 402 and decoder 404 provide error correction coding and decoding for information transmitted across the serial link.” *Id.*, col. 3:43-45. Thus, decoder 404 is configured to decode the deserialized data output from the serial to parallel converter 306. EX. 1003, ¶¶ 59-60.

- g. ***a first buffer operable to store data that has been deserialized and decoded by the first circuit and the decoder, respectively;***

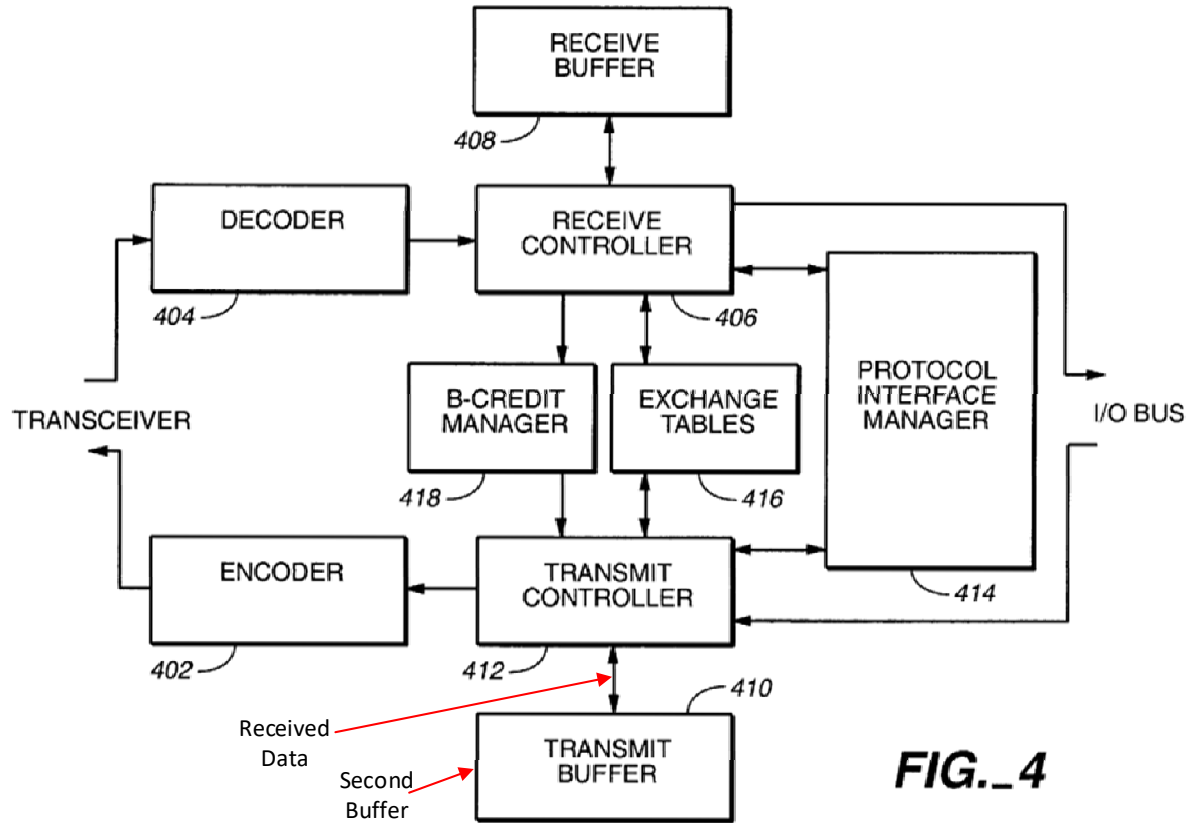
Vangemert's decoder 404 provides decoded data to receive controller 406, which "stores [the] received control words and data frames in receive buffer 408." EX 1005, col. 3:45-48. Thus, Vangemert's receive buffer 408 teaches the claimed first buffer that stores the decoded (and already deserialized) data. *Id.*, FIG. 4; EX. 1003, ¶ 62.



***Vangemert FIG. 4 (Annotated)***

- h. a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and**

Vangemert FIG. 4 illustrates the claimed “second buffer” as transmit buffer 410 that receives data from, and transmits data to, the transmit controller 412. EX. 1003, ¶ 63; EX 1005, col. 3:49-52, FIG. 4.

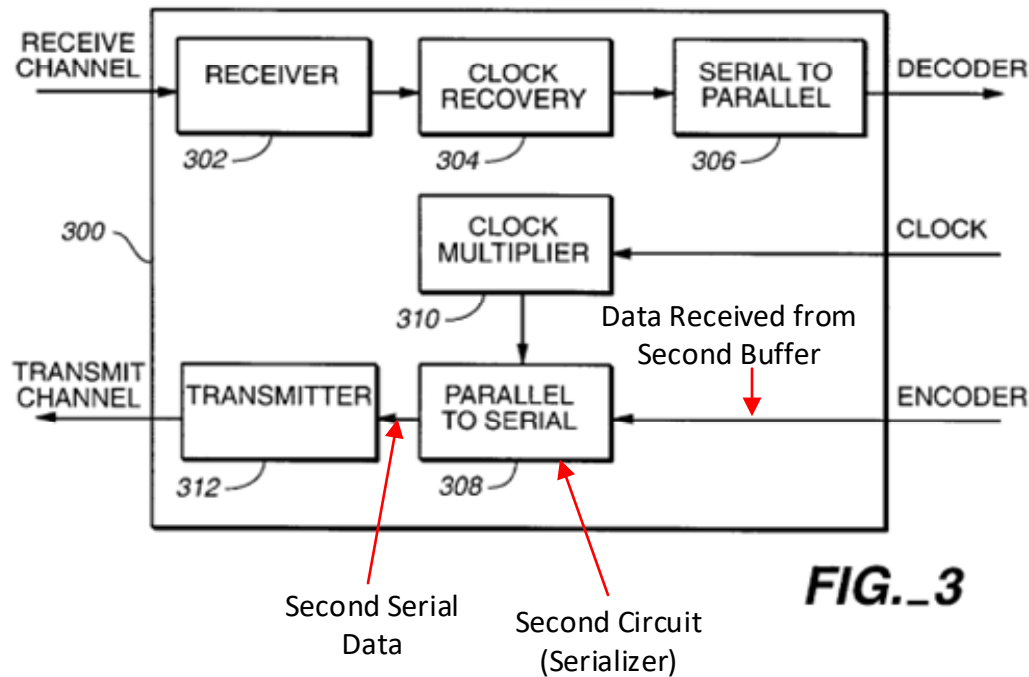


**Vangemert FIG. 4 (Annotated)**

Vangemert further teaches the claimed “second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data.” EX. 1003, ¶ 64.

Vangemert explains the transmit controller 412 (shown above in FIG. 4) retrieves data from the transmit buffer (second buffer) and provides the retrieved data to the encoder 402 (shown in FIGS. 3, 4). EX. 1003, ¶ 64; EX 1005, col. 4:49-52.

Vangemert FIG. 3 (annotated below) shows the encoder 402 then encodes the data and provides it to a parallel-to-serial converter 308 to serialize the data (converting parallel data to serial data), thereby generating the second serial data. EX. 1003, ¶¶ 64-65; EX 1005, col. 3:31-34.



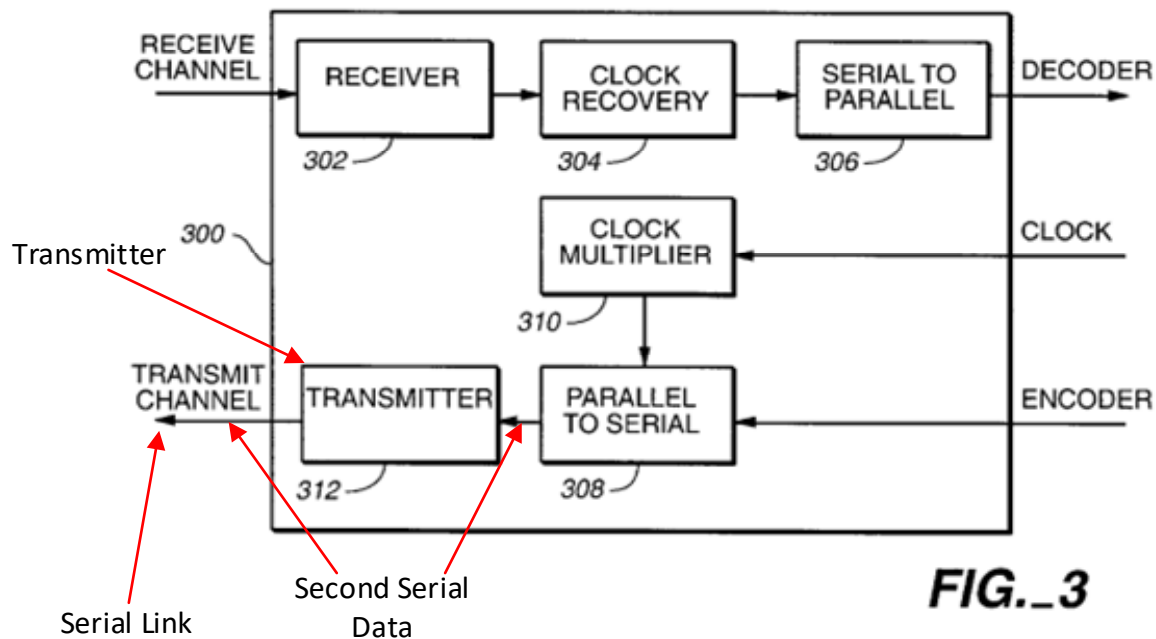
***Vangemert FIG. 3 (Annotated)***

Thus, Vangemert's transmit buffer (second buffer) is in data communication with an encoder 402 and a parallel-to-serial converter 308 (second circuit) configured to serialize data received via the transmit buffer (second buffer) to generate the second serial data. EX. 1003, ¶ 65.

- i. ***a transmitter operable to transmit the second serial data to the serial link through the connector;***

Vangemert teaches a transmitter 312 that “converts the serial bitstream [second serial data] into signals suitable for transport by the [serial link's] transmit channel.” EX. 1005, col. 3:35-36, FIG. 3. A PHOSITA would have understood that

the nodes and associated transmitters would be connected to the serial link through a connector, such as Copeland's connector 20, described above. EX. 1003, ¶ 66.



*Vangemert FIG. 3 (Annotated)*

- j. *wherein the module is configured to determine whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer; and*

Vangemert explains that “[r]eceive controller 406 includes a counter or register which tracks the amount of available buffer space [of] the receive buffer 408.” EX. 1005, col. 4:32-34. A comparator 502 within a buffer credit manager determines whether buffer space committed but not yet occupied is less than a buffer capacity by a predetermined amount. EX. 1003, ¶ 67; EX. 1005, col. 4:32-

34. The comparator 502 evaluates the available buffer capacity (based on the amount of data stored in the first buffer) against the fill amount (available buffer capacity less committed buffer space). EX. 1003, ¶ 67. Vangemert therefore teaches determining “whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer,” as claimed. *Id.*

**k. *wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,***

Vangemert teaches generating a flow control signal in the form of a buffer credit signal when the buffer has sufficient space for a new data frame. EX. 1003, ¶ 68. Because the buffer credit must be provided to an initiating node before that node can transmit data, the buffer credit signal is a flow control signal that controls data flow from the initiating device to the receive device. *Id.* ¶ 69; EX. 1005, col. 4:9-11. Thus, the bit credit signal is generated when the available buffer space is sufficient (***equal to the fill amount***) to accept the data word to be transmitted. EX 1003, ¶ 69 (emphasis added).

To the extent Vangemert is deficient, Copeland teaches overflow control by activating a signal upon the buffer capacity reaching a predetermined threshold. *Id.* ¶ 70. In Copeland, “data flow control is activated when the FIFO buffer is forty percent full.” EX. 1006, col. 5:38-40. The data flow control is executed by sending

a low Request to Send (“RTS”) signal over the connector 20 to instruct a remote device to stop sending data upon the FIFO buffer reaching the fill amount. EX. 1003, ¶ 71. The RTS signal is a flow control signal because it is generated to instruct a remote device to stop sending data. *Id.* ¶¶ 71-72.

If Vangemert is deficient, a PHOSITA would have found it obvious to either (i) combine Copeland’s flow control signal generation with Vangemert’s bit credit manager 418, as a redundancy to prevent receive buffer overflow or (ii) substitute Copeland’s flow control signal for Vangemert’s bit credit signal to safeguard the receive buffer from data overflow. EX. 1003, ¶¶ 73-74. A PHOSITA would have understood that both flow control methods may be used together or interchangeably. *Id.* ¶¶ 73-75.

For example, while Vangemert prevents overflow by preventing data transmission until sufficient buffer space exists, Copeland provides a backstop for Vangemert’s system because if, for some reason, the data stored in the buffer reaches or exceeds a predetermined fill threshold, a flow control signal could be sent to the sending device to prevent buffer overflow by instructing the sending device to stop transmitting data, as described above. EX. 1003, ¶ 73. Such a redundant system would minimize the risk of data loss due to the receive buffer overflowing. *Id.* Moreover, a PHOSITA could have easily incorporated Copeland’s signal into Vangemert’s system with a reasonable expectation of success. *Id.* ¶ 75.

Alternatively, a PHOSITA would have understood Copeland's flow control signal as simply another way to avoid buffer overflow. EX. 1003, ¶ 74. If data is retrieved from the receive buffer at or above the rate data is stored in the buffer, Copeland's methodology would advantageously eliminate the need to authorize the sending of each new data frame, which would reduce signal traffic and buffer credit computational delay. *Id.* A PHOSITA would recognize the advantages of adopting Copeland's interrupt signal into Vangemert's system that retrieves data from the receive buffer at, or above, the rate the data is deposited in the buffer and would be motivated to do so. *Id.* ¶¶ 74-75. A PHOSITA could have easily made such modifications. *Id.* ¶ 76.

Again, as both Vangemert and Copeland describe serial interfaces for providing serial communication between devices, a PHOSITA would have been motivated to combine their teachings to avoid buffer overflow and would have had a reasonable expectation of success in doing so. EX. 1003, ¶¶ 75-76.

- 1. and wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.***

Vangemert teaches that the transmit controller 412 transmits buffer credit control words received directly from the buffer credit manager 418 and passes them directly to the encoder 402, which sends them to the transmitter 312. EX.

1003, ¶ 77. The transmitter 312 then outputs the buffer credit signal (i.e., flow control signal) to other devices via the serial link. *Id.* Vangemert does not disclose or suggest that the buffer credit signal or associated buffer credit control words are ever stored in or passed through the transmit buffer 410 (second buffer). *Id.* Rather, Vangemert teaches that when the buffer credit manager is enabled in response to a request to transmit data from a remote device, “the transmit controller 412 begins transmitting buffer credit control words in response to a credit signal from buffer credit manager.” EX. 1005, col. 4:11-16. This teaches that the transmit controller 412 outputs data directly upon receiving it from the bit credit manager 418. EX. 1003, ¶¶ 77-78. This efficient transfer of the bit credit signal from the bit credit manager 418 through the transmit controller 412 aids in maintaining the minimum latencies Vangemert desires. EX. 1003, ¶ 79. If Copeland’s teachings were used to improve Vangemert, a PHOSITA would similarly strive to minimize latencies by routing the interrupt signal directly to the transmitting device, as disclosed by Copeland. *Id.* ¶ 81. As both Vangemert and Copeland teach directly transmitting flow control signals, avoiding their respective transmit buffers, a PHOSITA would have had a reasonable expectation of success in combining them. *Id.* ¶ 82.

Accordingly, Vangemert and Copeland render claim 1 obvious.

## **2. Claim 2**

Claim 2 is obvious over Vangemert and Copeland.

***The system of claim 1, wherein: the system is configured to transmit the first serial data and the second serial data asynchronously over the serial link.***

Vangemert discloses the claimed asynchronous transmission of first and second serial data over the serial link because transceiver 300 relies on reconstructing a clock signal embedded within the received data to process the received data, rather than relying on a common dedicated synchronizing clock signal that would be indicative of a synchronous system. EX. 1003, ¶ 83. Specifically, “[t]ransceiver 300 includes a receiver 302 coupled to the [serial link’s] receive channel to sense incoming signal levels, clean them up as much as possible, and provide them to a clock recover module 304. Clock recovery module 304 uses the incoming signal [first serial data] to reconstruct a clock signal synchronized to the incoming data [first serial data], and a serial-to-parallel converter 306 uses the clock signal to convert the incoming signal [first serial data] from serial form to parallel form.” EX. 1005, col. 3:21-28.

Transceiver 300 also transmits second serial data asynchronously over the serial link because the clock signal, in combination with the clock multiplier 310, is only used to convert “the stream of codewords into a serial bitstream.” *Id.*, col. 3:31-34; EX 1003, ¶ 84. Neither the clock signal, nor the clock multiplier generates a common clock signal separately transmitted to other devices in the system. EX. 1003, ¶ 84. Again, neither the transmitter 312, nor any other part of the transceiver

300, outputs a synchronizing clock signal, as would occur in a synchronous system. *Id.* Vangemert also does not require the transceiver 300's clock signal to be synchronized to any other device within the system, as would also be required in a synchronous system. *Id.* ¶¶ 83-84.

Thus, a PHOSITA would understand Vangemert teaches asynchronous transmission of first and second serial data over the serial link. *Id.* ¶¶ 83-85.

Additionally, Copeland discloses a “dual channel **asynchronous** serial communications card 11” and “two parallel-serial converters such as universal **asynchronous** receiver transmitters (UARTs)” coupled to the serial port connectors 20 and 21. EX. 1006, col. 3:49-60 (emphasis added). A PHOSITA would have understood that a UART would, by definition, asynchronously **transmit and receive** data, such as via Copeland's connector 20 which couples to Vangemert's serial link. EX. 1003, ¶ 87. (emphasis added). Furthermore, like Vangemert, Copeland discloses no separate, common synchronizing clock signal provided to, or used by, the serial communications card 11. *Id.* ¶¶ 87-88.

If Vangemert were somehow deemed deficient in disclosing asynchronous communication, a PHOSITA would have found it obvious and been motivated to incorporate Copeland's expressly asynchronous communication into Vangemert's serial communication disclosure because: (i) Vangemert and Copeland are both directed to serial communication devices not synchronized to a common,

separately provided clock signal; (ii) asynchronous communication is less complex and more cost effective than synchronous communication; and (iii) Vangemert's configuration (extracting a clock signal from received data) would have readily accommodated Copeland's asynchronous communication. EX. 1003, ¶¶ 88-90. By contrast, incorporating a synchronous communication scheme into Vangemert's system would add both cost and complexity, as it would require adding a separate clock line and common clock signal and further components and modifications to process the common clock signal. *Id.* ¶ 90. Thus, for at least these reasons, a PHOSITA would have been motivated to combine Vangemert and Copeland to allow Vangemert to take advantage of Copeland's simpler and more cost-effective asynchronous communication system and would have had a reasonable expectation of success in doing so. *Id.*

Accordingly, Vangemert and Copeland render claim 2 obvious.

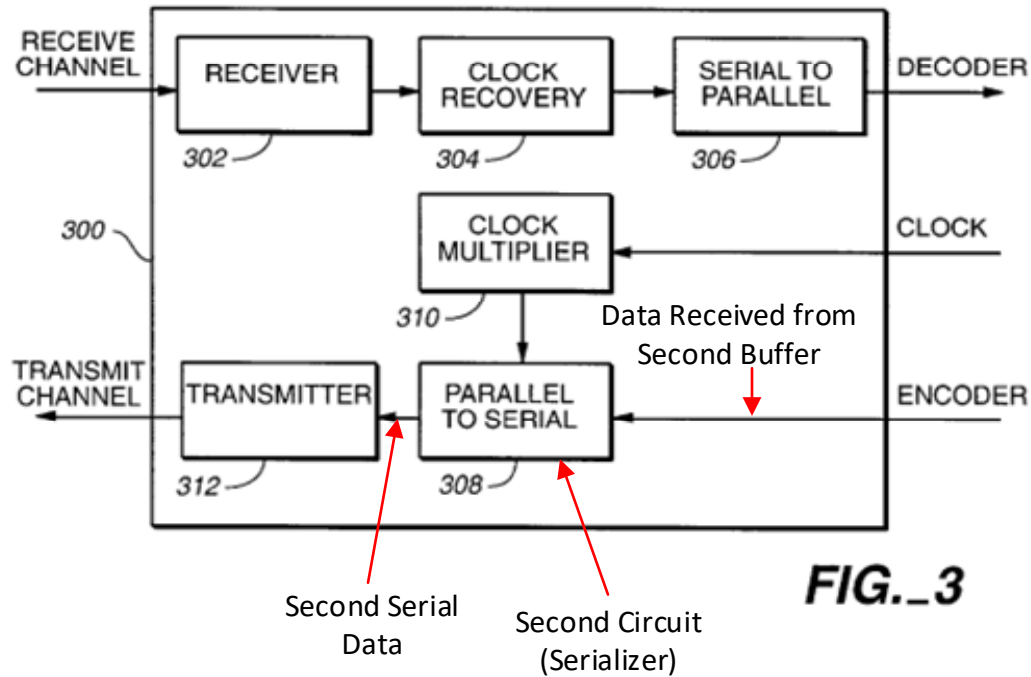
### **3. Claim 3**

Claim 3 is obvious over Vangemert and Copeland.

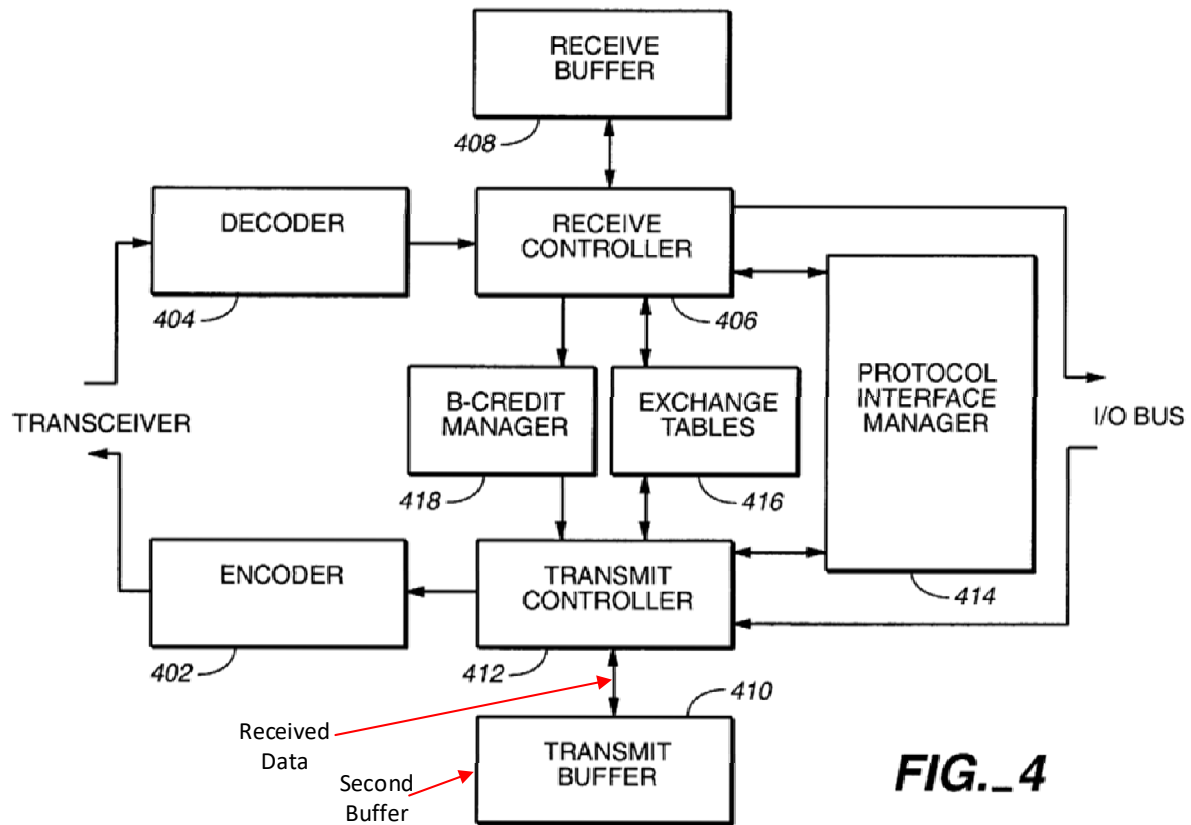
***The system of claim 1, wherein: the data received by the second buffer comprises parallel data.***

As discussed above regarding claim 1, Vangemert teaches that the transmit controller 412 retrieves data frames from the transmit buffer (second buffer) and provides them to the encoder 402, which provides encoded data to the parallel-to-

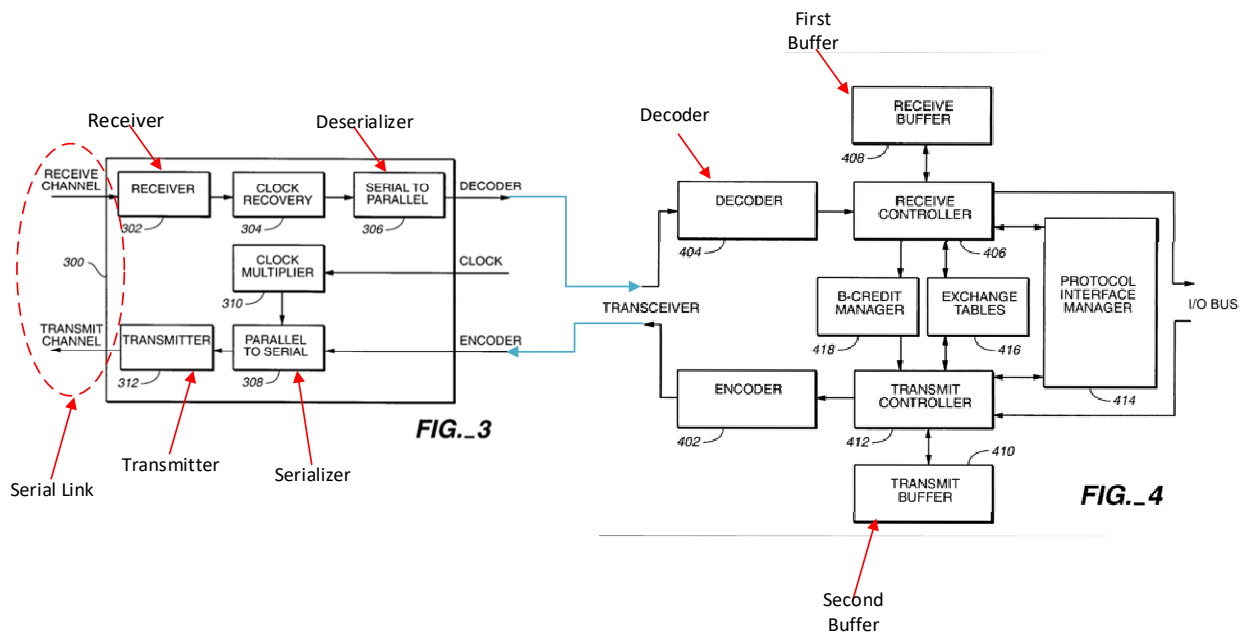
serial converter 308 for converting *parallel data* into serial data. EX. 1003, ¶ 93;  
EX. 1005, FIGS. 3, 4. Thus, the data received by Vangemert's second buffer is  
parallel data. EX 1003, ¶ 93.



**Vangemert FIG. 3 (Annotated)**



*Vangemert FIG. 4 (Annotated)*



***Vangemert Modified Combined FIGs. 3 and 4 (Annotated)***

Accordingly, Vangemert and Copeland render claim 3 obvious.

**4. Claim 4**

Claim 4 is obvious over Vangemert and Copeland.

***The system of claim 1, wherein: the module is further operable to repeatedly transmit the second serial data through the serial link and the connector without receiving acknowledgement during transmission.***

Vangemert teaches that, upon receiving a bit credit signal from a target device, a data frame is transmitted. EX. 1005, col. 2:3-6. “Transmit controller 416 creates or updates exchange information in exchange tables 416 in response to commands and data from the node’s i/o bus, generates control words and data frames in transmit buffer 410, and forwards them to encoder.” EX 1005, col. 3:57-

61. Vangemert does not teach or suggest that an acknowledgment signal is required to continue the transmission.

Vangemert's teaching is commensurate with this limitation's support in the '454 and '214 patent specifications. Like Vangemert, the specifications require no acknowledgment to start or maintain transmission. This disclosure resembles Vangemert's data transmission with no stated requirement for an acknowledgment during transmission of a specific data packet. EX. 1003, ¶ 89; see EX 1010, col. 10:18-25.

Furthermore, a PHOSITA would have understood that communication of an entire data packet without requiring intervening acknowledgements is fundamental to serial communication via Fiber Channel, as described in Vangemert, which transmits all data in a data frame once the bit credit is issued. *Id.* ¶ 90.

Thus, Vangemert and Copeland render claim 4 obvious.

## **5. Claim 7**

Claim 7 is obvious over Vangemert and Copeland.

***The system of claim 1, wherein: the flow control signal is configured to be used to control transmission of the first serial data over the serial link to prevent overflow of the first buffer.***

Vangemert teaches using buffer-credits to control data flow by permitting an initiating device's serial data transmission only upon receipt of a buffer credit signal from the receiving node. EX. 1003, ¶ 96. This buffer credit signal is only

sent to the initiating node when the receiving node is determined to have space available to receive the data. *Id.* This ensures the receive buffer (first buffer) does not receive data unless it has sufficient space, thereby preventing buffer overflow. *Id.* Thus, the buffer-credit signal is a flow control signal preventing overflow of the first buffer.

If Vangemert is deficient, Copeland teaches a flow control signal configured to instruct a transmitting device to stop transmitting when the buffer fill level reaches a predetermined value, thereby controlling transmission of the first serial data over the serial link to prevent overflow of a first buffer. EX. 1003, ¶ 98. As noted above, it would have been obvious to combine Copeland's teachings with Vangemert. *Id.*

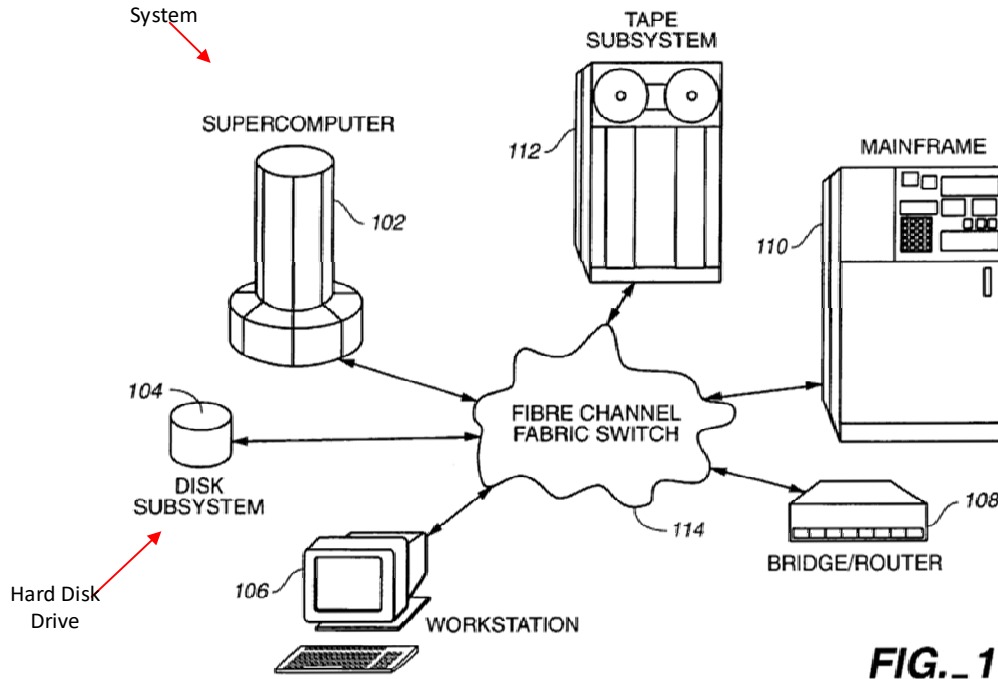
Thus, claim 7 is obvious over Vangemert and Copeland.

## **6. Claim 15**

Claim 15 is obvious over Vangemert and Copeland.

***The system of claim 1, wherein the system comprises a hard disk drive.***

Vangemert's FIG. 1 system includes a "disk subsystem 104." EX. 1003, ¶ 100.



**Vangemert FIG. 1 (Annotated)**

A PHOSITA would have understood this disk subsystem to include one or more hard disk drives. *Id.* Thus, claim 15 is obvious over Vangemert and Copeland.

## **7. Claim 16**

Claim 16 is obvious over Vangemert and Copeland.

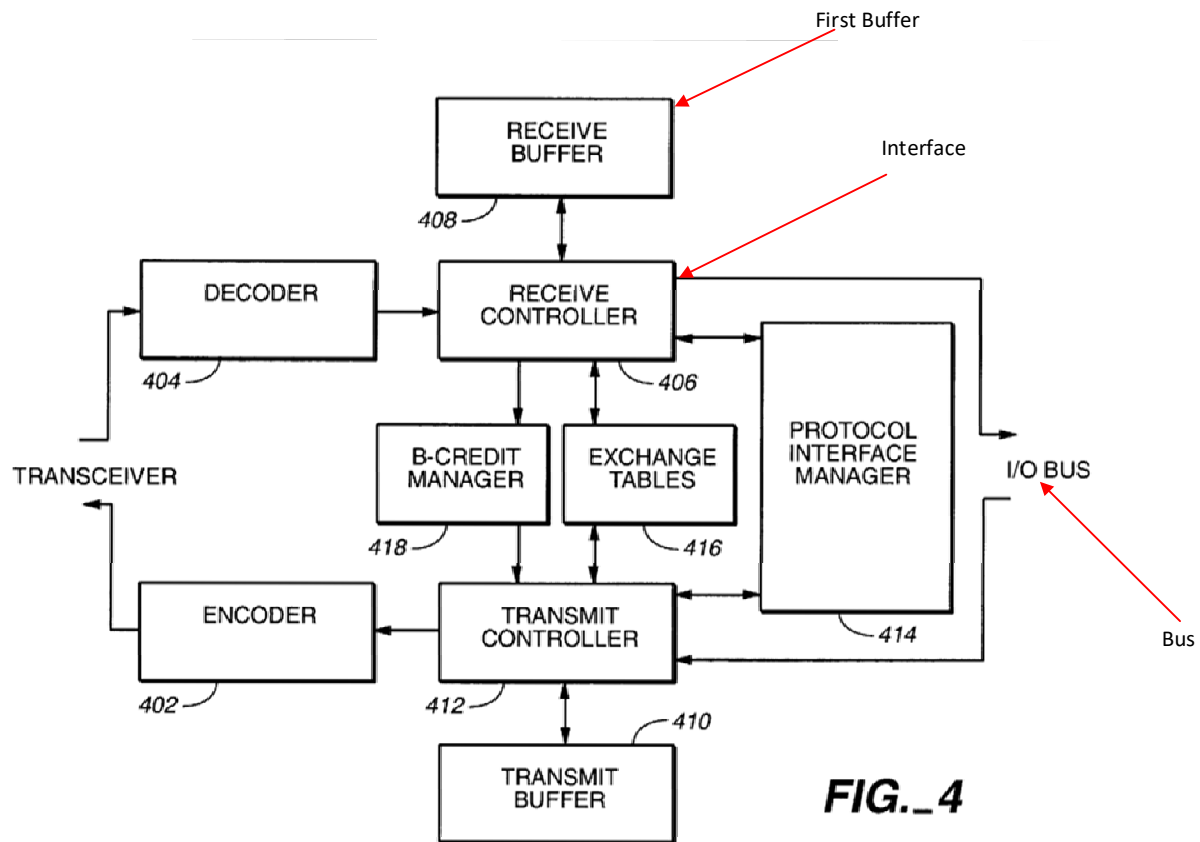
***The system of claim 1, further comprising:***

***an interface included in the module coupled to the first buffer and operable to receive the data stored in the first buffer;***

***a bus coupled to the module and configured to receive the data from the interface; and***

***a processor coupled to the bus.***

Vangemert's FIG. 4 illustrates the interface, first buffer, and bus of claim 16.



**Vangemert FIG. 4 (Annotated)**

First, Vangemert discloses a receive controller 406 [interface] positioned between the receive buffer [first buffer] and the I/O Bus. The receive controller 406 stores received control words and data frames in receive buffer 408. EX. 1003, ¶ 101; EX. 1005, col. 3:46-48. The receive controller 406 also creates or updates “exchange information in exchange tables 416 in response to received control words or data frames,” which as noted above are stored in the receive buffer. EX. 1005, col. 3:52-57. The receive controller also receives data from the receive

buffer (first buffer), and therefore teaches the “interface included in the module coupled to the first buffer and operable to receive the data stored in the first buffer.” EX. 1003, ¶ 101.

Second, the receive controller 406 forwards “data from the received data frames to the node’s i/o bus.” EX. 1005, col. 5:56-57. The node’s i/o bus (*see* FIG. 4, above) teaches the claimed “bus coupled to the module and configured to receive the data from the interface.” EX. 1003, ¶ 101.

Third, Vangemert discloses a “processor coupled to the bus.” EX. 1003, ¶ 102. Again, the receive controller 406 “forwards data from received data frames to the node’s i/o bus.” EX. 1005, col. 3:56-57. The referenced node includes the exemplary nodes shown in Vangemert’s FIG. 1, such as “supercomputer 102.” A PHOSITA would have understood the “supercomputer” includes a processor and the supercomputer node would communicate with other nodes through its i/o bus and associated network interface, as depicted in FIGs. 3 and 4. Therefore, Vangemert teaches a processor coupled to the bus. EX. 1003, ¶ 102.

Thus, claim 16 is obvious over Vangemert and Copeland.

## **8. Claim 17**

Claim 17 is obvious over Vangemert and Copeland.

***The system of claim 1, wherein: the module is further configured to generate a clock signal, for use by the module, using the first serial data.***

Vangemert recites that “[t]ransceiver 300 includes a receiver 302 coupled to the receive channel to sense incoming signal levels [first serial data], clean them up as much as possible, and provide them to a clock recovery module 304. Clock recovery module 304 **uses** the incoming signal [**first serial data**] to **reconstruct a clock signal** synchronized to the incoming data, and a serial-to-parallel converter 306 **uses the clock signal** to convert the incoming signal from serial form to parallel form.” EX. 1005, col. 3:21-28 (emphasis added). Thus, the clock signal is “generated” (reconstructed) for use by the module, specifically, the serial-to-parallel converter 306 within the module, using the first serial data. EX. 1003, ¶ 103.

Accordingly, claim 17 is obvious over Vangemert and Copeland.

**B. Ground 2: Claim 4 is obvious over Vangemert, Copeland, and Dobson**

Claim 4 is obvious over Vangemert (EX 1005), Copeland (EX 1006), and Dobson (EX 1007).

***The system of claim 1, wherein: the module is further operable to repeatedly transmit the second serial data through the serial link and the connector without receiving acknowledgement during transmission.***

To the extent Vangemert does not expressly state that no acknowledgement is required, Dobson teaches transmitting data by inputting parallel data into the UART 30, which is then converted to serial and output from the UART 30 on line

16 (serial link). EX 1003, ¶ 105; EX 1007, col. 1:36-47. This transmission requires no acknowledgement or other signal from the receiving device. EX. 1003, ¶ 106. Rather, data is simply serialized and transmitted over the line 16. *Id.* In fact, none of Dobson's data transmission functions require receiving an acknowledgement (or other) signal to allow data to be continually and repeatedly transmitted. *Id.*

If Vangemert's disclosure is deemed deficient, a PHOSITA would have found it obvious and would have been motivated to combine Dobson's transmission protocol with Vangemert and Copeland. *Id.* ¶ 108. This would ensure all data frames within a message of Vangemert would be transmitted in a specific data exchange without having to wait for an acknowledgement or other response after each portion of the data is transmitted. *Id.* Such would maintain Vangemert's stated goal of minimizing latency rates. *Id.* As Vangemert, Copeland, and Dobson are all directed to serial port controllers with flow control functionality, a PHOSITA would have had a reasonable expectation of success in combining them. *Id.*

Thus, claim 4 is obvious over Vangemert, Copeland, and Dobson.

**C. Ground 3: Claim 6 is obvious over Vangemert, Copeland, and Reay**

Claim 6 is obvious over Vangemert (EX 1005), Copeland (EX 1006), and Reay (EX 1008).

***The system of claim 1, wherein: the module is further operable to transmit the first serial data over the serial link and to transfer the second serial data over the serial link using differential signals.***

First, claim 6 appears to contain a typographical error because it recites the module is operable to “transmit” the first serial data over the serial link. Claim 1, however, recites the module is operable to “**receive** first serial data transmitted over the serial link.” While the actual intent is unclear, for this analysis, this portion of claim 6 is interpreted as the module is operable to “receive” first serial data over the serial link using differential signals. EX. 1003, ¶ 111.

As discussed, Vangemert teaches that the modules (various nodes, via a fabric switch) receive first serial data and transmit second serial data. EX. 1003, ¶ 112. Furthermore, the nodes (nodes 102-114) are coupled to a “serial link having a receive channel and a transmit channel.” EX. 1005, cols. 2:65 – 3:1. Therefore, Vangemert teaches that serial data (e.g., data over the serial link) is transmitted and received at each module.

Additionally, the transceiver 300 includes a transmitter 312 and a receiver 302 configured to, respectively, transmit data over the transmit channel and receive data over the receive channel. The transmit channel and the receive channel form a serial link for communicating between nodes. EX. 1003, ¶ 113. Thus, Vangemert

teaches that the module is “operable to [receive] the first serial data over the serial link and to transfer the second serial data over the serial link.” *Id.*

Reay teaches transmitting and receiving data using differential signals. Specifically, Reay states that “[o]utput terminals 106 and 108 provide inverted and non-inverted output signals, respectively, of the input signal received at terminal 102. Thus, **a differential**, or balanced-line, output can be provided for those interface standards that require such output.” EX. 1008, col. 4:15-20.

Reay further explains that the advantage of using differential outputs is “noise immunity: any noise that appears on one of the two output lines is likely to appear on the other as well and is thus cancelled as the difference between the two output signal voltages is taken.” *Id.*, col. 4:32-35. A PHOSITA would therefore have found it obvious and been motivated to combine Reay’s noise cancelling/reducing differential signal output with Vangemert’s serial link to reduce errors or data corruption caused by noise on either the receive or transmit channels. EX. 1003, ¶ 114. A PHOSITA would have had a reasonable expectation of success in modifying Vangemert’s serial link with Reay’s differential signals, as the use of differential signals for serial transmission was well known in the art before the time of the claimed invention. *Id.* Thus, claim 6 is obvious over Vangemert, Copeland, and Reay.

**D. Ground 4: Claims 1, 2, 3, 4, 7, and 16 are obvious over Dobson and Copeland.**

Claims 1-4, 7, and 16 are obvious over Dobson (EX 1007) and Copeland (EX 1006).

**1. Claim 1**

Claim 1 is obvious over Dobson and Copeland.

**a. A system, comprising:**

Dobson teaches a system having an enhanced serial port controller 10 that facilitates communication with various devices, such as host computer 8, as shown below in annotated FIG. 2. EX. 1003, ¶ 117.

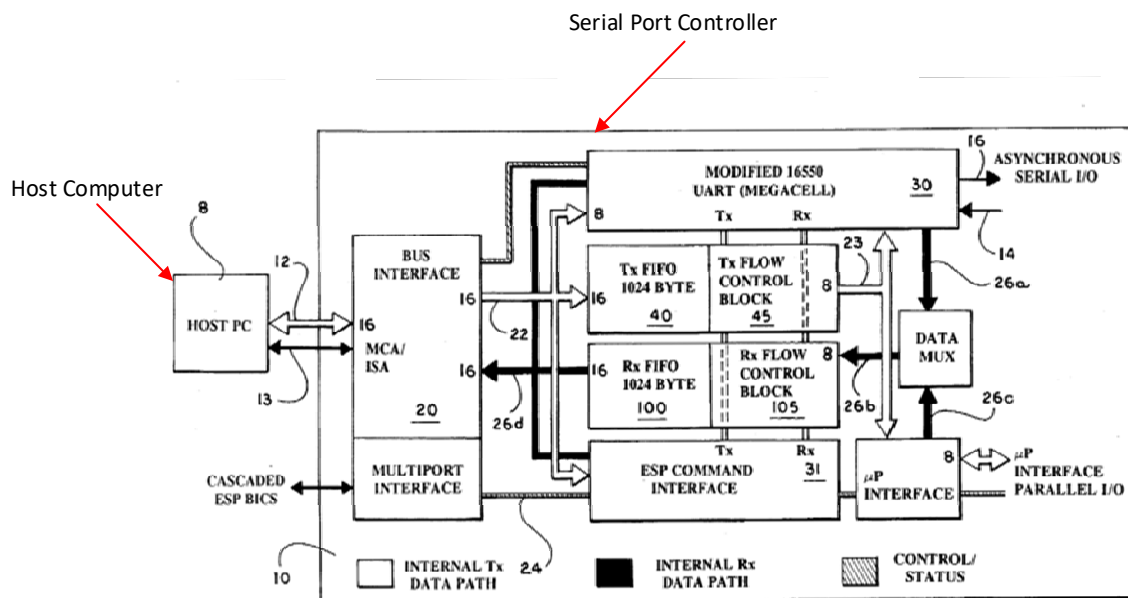
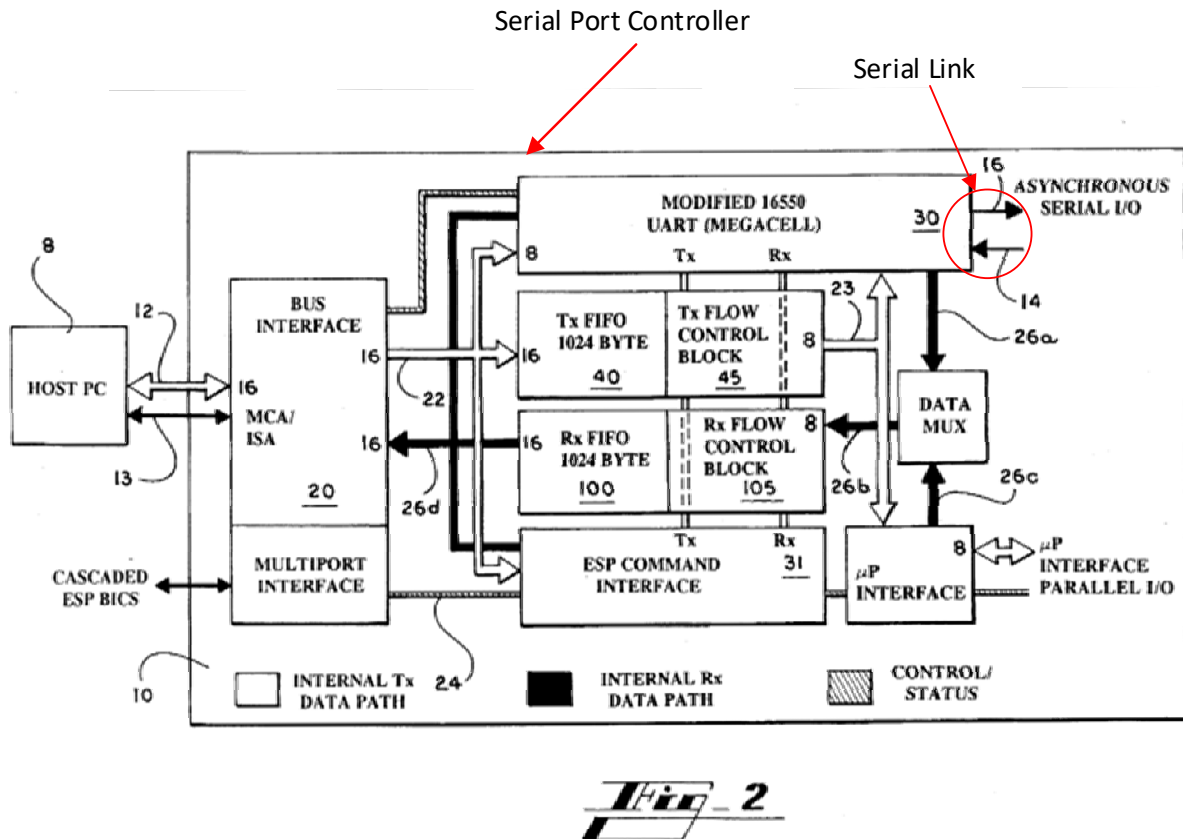


**Fig. 2**

**Dobson FIG. 2 (Annotated)**

**b. a connector configured to be connectable to a serial link; and**

Dobson teaches a serial link. As shown in annotated Dobson FIG. 2, a serial link is formed by receive line 14 and transmit line 16. EX. 1007, FIG 2.

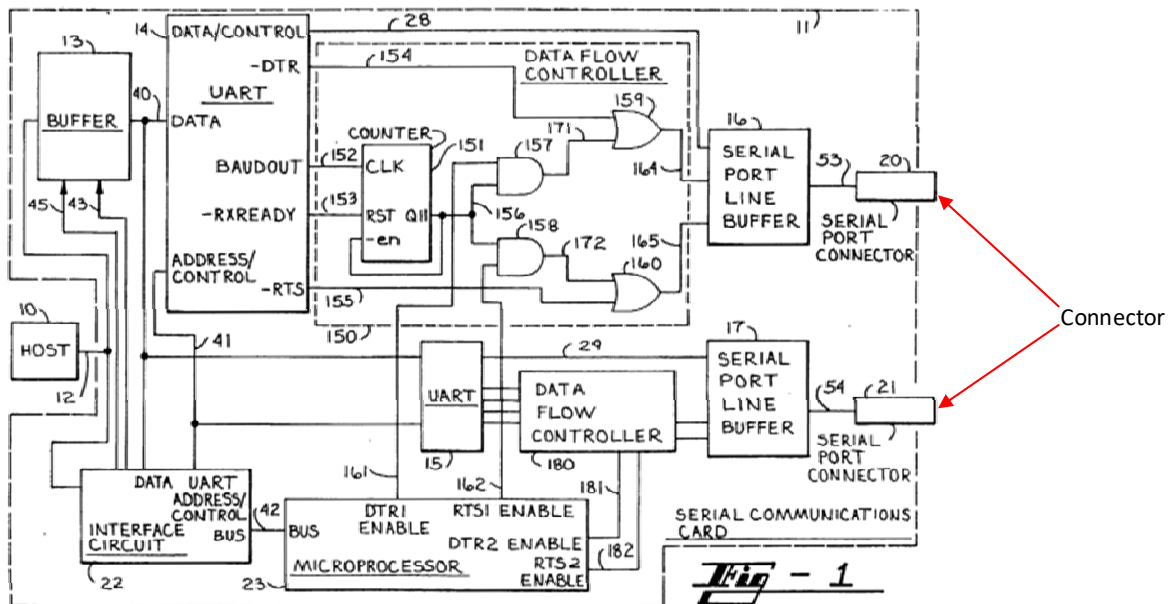


***Dobson FIG. 2 (Annotated)***

Dobson explains that the UART 30 converts parallel data to serial data, which is output on line 16. *Id.*, col. 6:10-12. Dobson further explains that the enhanced serial port controller 10 is configured to receive asynchronous, serial data on line 14. *Id.*, col. 7:54-56. Accordingly, the combination of the transmit line

16 and the receive line 14 is a serial link. EX 1003, ¶ 118. A PHOSITA would have understood that a connector would have been required to connect to Dobson's enhanced serial port controller 10 to external devices via the serial link, such as a modem or other communication device. *Id.*; see EX 1007, col. 1:23-26.

Copeland also teaches a connector configured to be connectable to a serial link. Specifically, Copeland is directed to a dual channel asynchronous serial communications card 11 that includes "two serial port connectors 20 and 21." EX. 1006, col. 3:49-60. Serial port connectors 20 and 21 are "connected to a communication device (not shown) such as a modem" and "preferably define an EIA RS-232-D serial interface." EX. 1006, col. 4:31-34. RS-232-D connectors are well known as common connectors for interconnecting serial devices. EX. 1003, ¶ 119. Copeland FIG. 1 shows serial port connector 20 configured to connect the UART 14 with an external device via line 28. EX. 1003, ¶ 120.



**Copeland FIG. 1 (Annotated)**

While Copeland teaches two serial port connectors 20 and 21, each one is used for a single channel of the dual channel asynchronous serial communication card 11. *Id.* Copeland, therefore, discloses a “connector configured to be coupled to a serial link.”

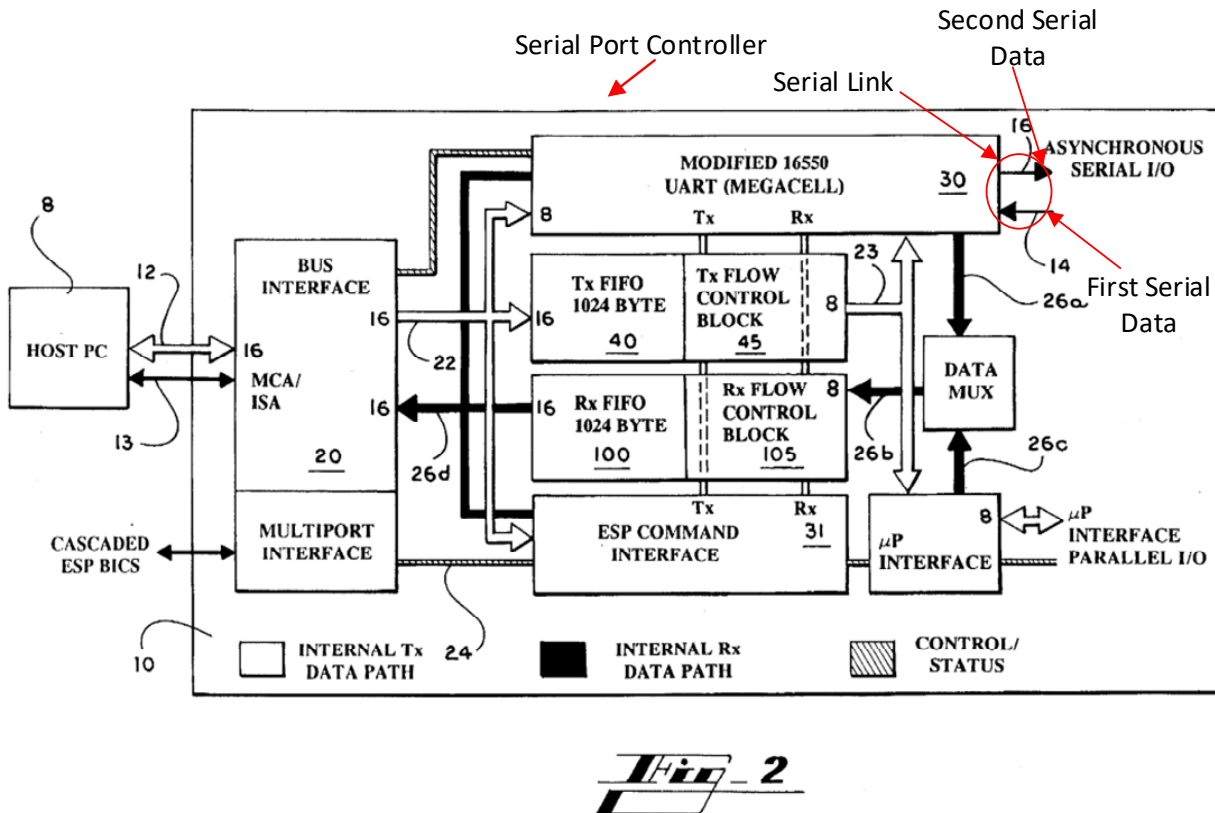
A PHOSITA would have found it obvious and been motivated to combine Copeland’s connector 20 with Dobson’s serial link (receive line 14 and transmit line 16) to provide a mechanism for connecting Dobson’s serial link with one or more external devices. EX. 1003, ¶ 121. Dobson and Copeland are directed to the **same art**—serial port controllers configured to control a serial interface of host devices—in the **same class/subclass** (395/250). *Id.* Copeland was cited in Dobson.

EX. 1007, 1. Dobson and Copeland describe the **same technology** (serial port controllers) developed by the **same applicant** (Hayes Microcomputer Products, Inc.) utilizing the **same main component** (a 16550 UART). *Id.* Dobson states that its invention embodies “a part of an improved serial port circuit that includes the basics of a type 16550 UART, and multiple enhancements to same” and expressly contemplates combination with art such as the earlier-filed Copeland, stating that it “is specifically designed to be backwardly compatible with machines and applications designed for use with 16550 type UARTs.” EX. 1007, col. 3:20-29. Further, the Dobson system would have required a connector mechanism, such as Copeland’s. EX. 1003, ¶ 121. Accordingly, a PHOSITA would have been motivated to combine Copeland’s well-known connector with Dobson’s the serial link and would have had a reasonable expectation of success in doing so. *Id.*, ¶ 122.

- c. ***a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, and wherein the module includes:***

Dobson teaches a module “operable to receive first serial data transmitted over the serial link” and “transmit second serial data to the serial link.” As shown below in annotated Dobson FIG. 2, the serial port controller 10 (module) receives

and transmits serial communications on the receive line 14 and transmission line 16, respectively (serial link). EX. 1003, ¶ 123.



**Dobson FIG. 2 (Annotated)**

As explained above, the serial line 14 acts as a serial receive line and is coupled to a receive side of the serial port controller 10. EX. 1003, ¶ 124. The serial port controller 10 is configured to accept asynchronous, serial data, via serial line 14. *Id.* The asynchronous serial data received via line 14 would have been understood by a PHOSITA to be the claimed “first serial data received over the serial link.” *Id.*

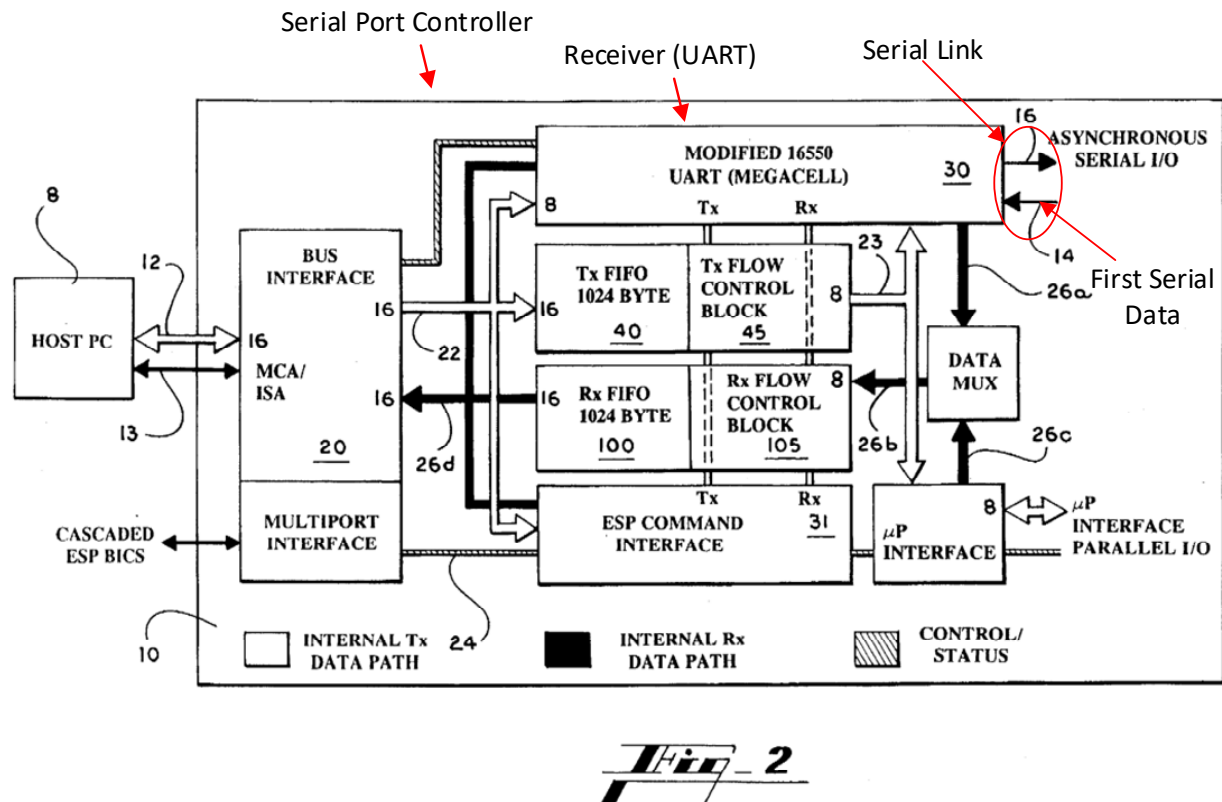
Dobson further teaches that parallel data is provided to the UART 30, converted to serial data, and then transmitted out on line 16 (serial link). *Id.*, ¶ 125; EX 1007, col. 6:10-12. A PHOSITA would have understood that the serial data output from the UART 30 on line 16 teaches that the module is operable to “transmit second serial data to the serial link.” EX. 1003, ¶ 125. The received first serial data and the transmitted second serial data are shown in Dobson FIG. 2, annotated above.

Copeland teaches, as noted above, the connector in the form of serial port connector 20. The serial port connector 20 is coupled to the serial communication card 11, similar to Dobson’s serial port controller 10. EX. 1003, ¶ 126; EX 1006, col. 3:46-63. As noted above, a PHOSITA would have understood that Dobson’s serial link would have been connected to external devices, such as a modem, through a connector, such as Copeland’s connector 20. A PHOSITA would have found it obvious and been motivated to combine Copeland’s connector 20 with Dobson’s serial port controller 10 and would have had a reasonable expectation of success in doing so. EX. 1003, ¶ 126.

**d.     *a receiver operable to receive the first serial data from the serial link through the connector;***

As shown in annotated FIG. 2, below, Dobson teaches that the serial port controller 10 includes a UART (“universal asynchronous **receiver**-transmitter”) 30,

which by definition includes a receiver. EX. 1003, ¶ 127; EX. 1007, col. 1:36-38 (emphasis added). As further shown below, the UART 30 receives data (first serial data) via link 14 (serial link). *Id.*



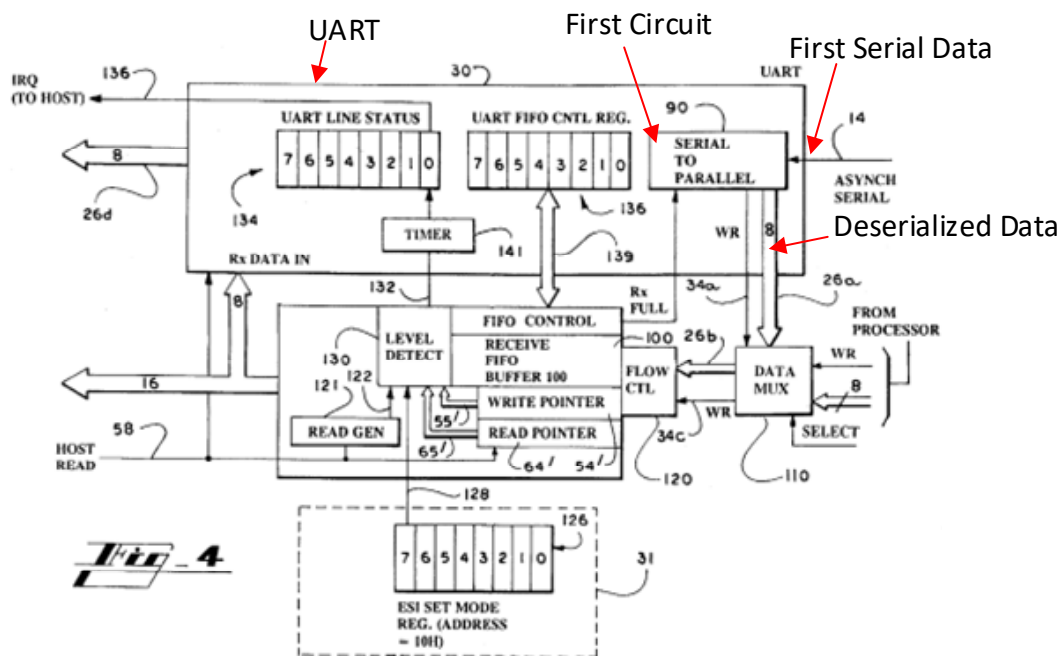
***Dobson FIG. 2 (Annotated)***

Thus, Dobson's UART 30 discloses the claimed "receiver operable to receive the first serial data from the serial link." Furthermore, a PHOSITA would have understood that the enhanced serial controller 10, and therefore the associated receiver (UART 30), would have been connected to the serial link, including the receive line 14, through a connector, such as Copeland's connector 20, described

above. EX. 1003, ¶ 127. As noted above, a PHOSITA would have understood that Dobson's serial link would have been connected to external devices, such as a modem, through a connector, such as Copeland's connector 20. A PHOSITA would have found it obvious and been motivated to combine Copeland's connector 20 with Dobson's serial port controller 10 to provide data to the receiver. *Id.*

**e. a first circuit configured to deserialize the first serial data to generate deserialized data;**

Dobson describes and illustrates in annotated FIG. 4 below the UART 30 as having a serial to parallel circuit 90 for converting received serial data into parallel data, thereby deserializing the received first serial data. EX. 1003, ¶ 129; EX. 1007, cols. 7:67 – 8:6.



**Dobson FIG. 4 (Annotated)**

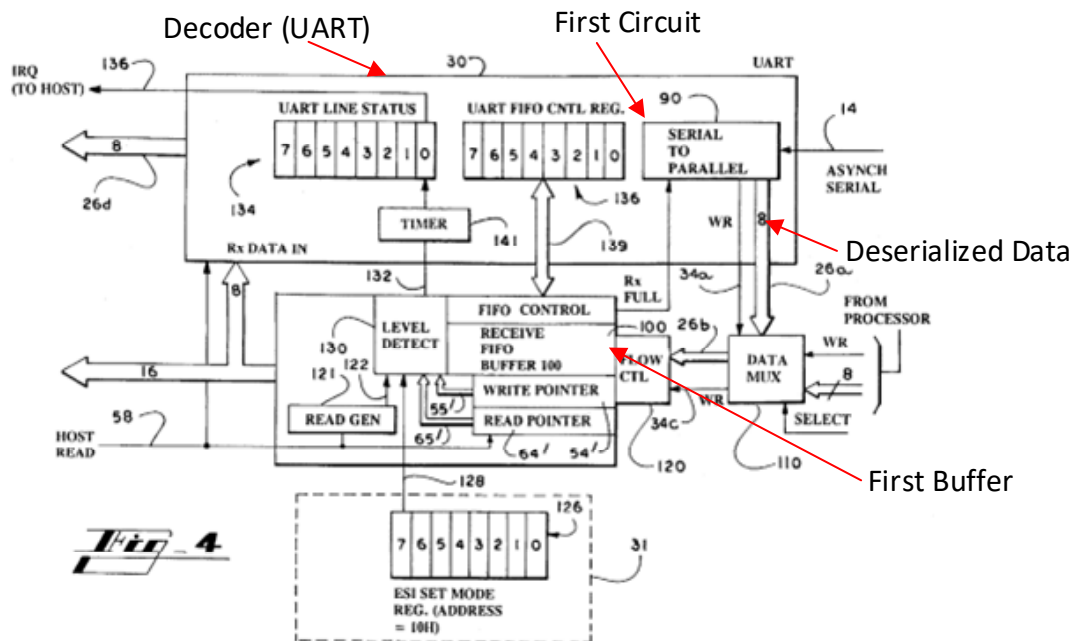
Dobson teaches that the data output of the UART 30's serial to parallel circuit 90 (deserialized data) is provided to the data multiplexor 110 over data bus 26a. EX. 1003, ¶ 129. Thus, Dobson teaches the claimed "first circuit configured to deserialize the first serial data to generate deserialized data." *Id.*

**f. a decoder configured to decode the deserialized data;**

Dobson teaches the claimed decoder. As discussed above, serial data is received at the UART 30 and deserialized by a serial to parallel circuit 90. EX. 1003, ¶ 130. Dobson teaches that a UART, upon deserializing the serial data "responds to and strips start and stop bits and can give an indication of when a parity error is detected." EX. 1007, col. 1:47-49. This stripping of bits and error detection teaches a decoder configured to decode the deserialized data as it separates the data package from the associated control bits and extracts other information (e.g., parity errors) from the received data. EX. 1003, ¶ 130. Thus, the UART 30 teaches the claimed decoder configured to decode the deserialized data by restoring the received frames into their desired form by separating the data package from the associated control bit (i.e., start and stop bits). *Id.* Dobson's disclosure of decoding is commensurate with the purported support for this claim limitation.

- g. *a first buffer operable to store data that has been deserialized and decoded by the first circuit and the decoder, respectively;*

As shown below in annotated Dobson FIG. 4, the serial port controller 10 includes a receive FIFO buffer 100. EX. 1003, ¶ 132; EX 1007, FIG. 4.



***Dobson FIG. 4 (Annotated)***

Dobson teaches that after deserializing and decoding the data, as described above, the data is output over the bus 26a to the multiplexor 110 and then “clocked into the receive FIFO buffer 100 using the write signal on line 34a.” EX. 1007, col. 8:24-25. The receive FIFO buffer 100 therefore teaches the claimed “first buffer,” as it is configured to store the deserialized and decoded data output by the UART 30. EX. 1003, ¶ 132.

- h. a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and**

Dobson teaches the claimed second buffer. As shown below in annotated FIG. 2, a transmit FIFO buffer 40 is configured to receive data from the host device 8 via the bus interface 20 and over the transmit data bus 22. EX. 1003, ¶ 133. Thus, the transmit FIFO buffer 40 teaches the claimed “second buffer operable to receive data.”

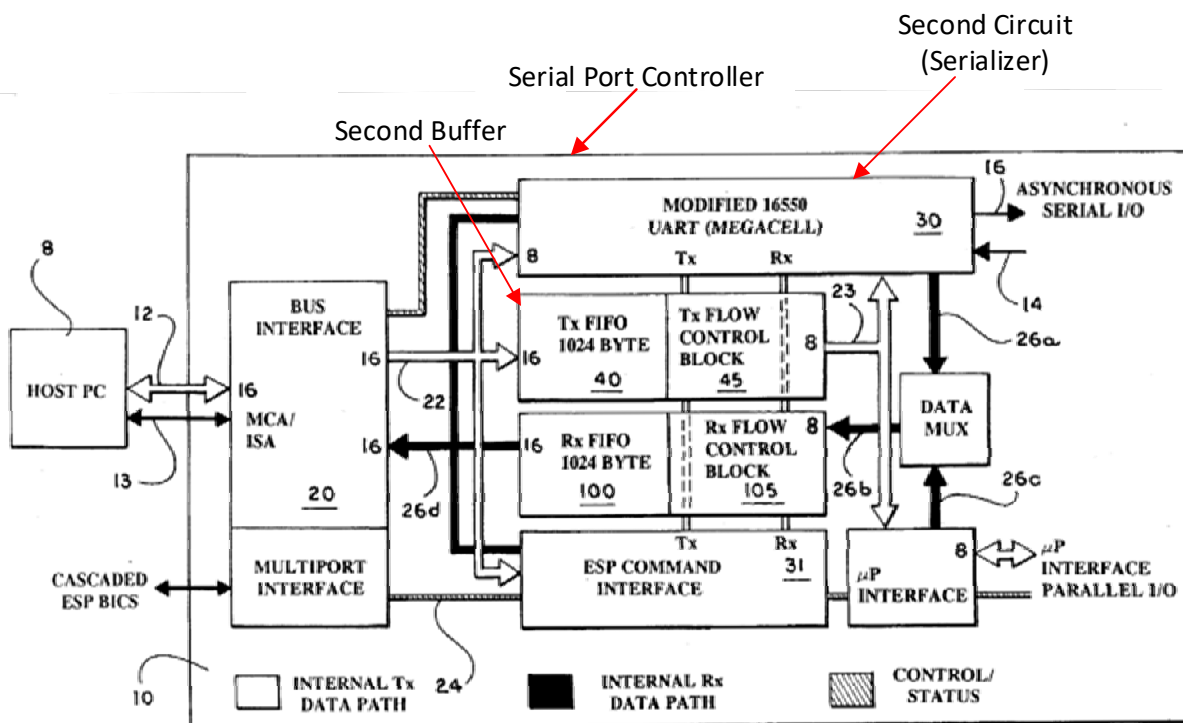


**FIG. 2**

**Dobson FIG. 2 (Annotated)**

Dobson further teaches that the transmit buffer 40 (second buffer) is “in communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data,” as recited in claim 1. *Id.* ¶ 134. The transmit buffer 40 outputs data to the UART 30 via the data bus 23, the UART 30 converts the data from parallel to serial, and the data is output on transmit line 16 (serial link). *Id.* While the figures do not illustrate a parallel to serial converter, Dobson states “[a]s will be familiar to those skilled in the art, the data is converted from parallel to serial in the UART 30 and output on line 16.” EX. 1007, col. 7:1-4. Accordingly, Dobson teaches the second buffer in data communication with a “second circuit that is configured to serialize data received via the second buffer to generate the second serial data.” EX. 1003, ¶ 134.

**i. *a transmitter operable to transmit the second serial data to the serial link through the connector;***

Dobson teaches the claimed transmitter. As described above, the serial port controller 10 includes a “UART 30,” which is a “universal asynchronous receiver-***transmitter***.” EX. 1003, ¶ 135; EX. 1007, col. 1:36-38 (emphasis added). Dobson further discloses serial data transmission, stating “data is input to the UART 30 in parallel, is converted by the UART 30 to serial and is output [transmitted] from the UART 30 on line 16.” EX. 1007, col. 6:10-12. As previously discussed, line 16 is the transmit portion of the serial link. A PHOSITA would have understood that the

data output by the UART 30 on line 16 would have been connected to an external device over the serial link through a connector, such as Copeland's connector 20, as described above. EX. 1003, ¶ 135.

Accordingly, Dobson and Copeland teach a transmitter “operable to transmit the second serial data to the serial link through the connector,” as claimed.

- j. ***wherein the module is configured to determine whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer; and***

Dobson teaches that the serial port controller includes circuitry for detecting a data level in the receive FIFO buffer 100 (first buffer). EX. 1003, ¶ 137; EX 1007, col. 8:53-57. Dobson states the “value on bus 147 is compared with the number of data bytes written into the receive FIFO buffer 100” and “[w]hen the number of bytes written into the receive FIFO buffer 100 [first buffer] equals the selected scalable trigger level on bus 147, the comparator 138 outputs the trigger level reached signal on line 132.” *Id.*, col. 9:32-39. This comparison of the number of bytes stored in the FIFO buffer 100 (amount of data stored in the first buffer) against a predetermined trigger level (fill amount) teaches “determin[ing] whether an amount of data stored in the first buffer equals or exceeds a fill amount,” as claimed. EX. 1003, ¶¶ 137-138.

Copeland also teaches detecting a data level in the receive FIFO buffer 100 (first buffer). EX. 1003, ¶ 139. Copeland's flow control operation for the FIFO buffer of UART is activated when the FIFO buffer reaches a threshold fill value (equals or exceeds a fill amount). *Id.* The amount of data in the FIFO buffer is determined by counting a number of cycles output by UART 14 before the FIFO buffer is emptied. *Id.*, ¶ 140.

**k. *wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,***

Dobson teaches that when a comparator 138 determines that the number of bytes written into the receive FIFO buffer 100 (first buffer) equals a trigger level, the comparator 138 outputs a trigger level reached signal on line 132. EX. 1003, ¶ 141; EX. 1007, col. 9:32-42. The trigger level reached signal is used to service the buffer, which may include emptying the buffer to prevent overflow or overwriting data within the FIFO buffer 100. EX. 1003, ¶ 141. Further, the trigger level reached signal is generated when the amount of data written into the receive buffer (first buffer) equals or exceeds the predetermined selected scalable trigger level (fill amount). *Id.*

Copeland teaches "the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount," as claimed. *Id.*, ¶ 142. Copeland's flow control is "activated when

the FIFO buffer [of UART 14] is forty percent full.” EX. 1006, col. 5:38-40. The receive FIFO buffer of UART 14 corresponds to the claimed “first buffer” because the UART’s FIFO buffer receives data transmitted from serial data port 20 from a remote transmitter and the flow control signal is generated based on a fill level of the UART’s FIFO buffer. EX. 1003, ¶ 142; EX. 1006, col. 3:9-12, 5:52-55.

Once Copeland’s flow control is activated, the data flow controller 150 outputs a low value on a Request to Send (“RTS”) line, which is output to the serial port connector 20 as a flow control signal (a logic low RTS signal). EX. 1003, ¶¶ 143-145. Copeland further explains the flow control signal (RTS low) prevents overflow of the UART 14’s FIFO buffer whenever host 10 is unable to keep up with the data transfer rate by stopping the transmitting device from transmitting data to the receiving device. *Id.*



***Dobson FIG. 4 (Annotated)***

A PHOSITA would have found it obvious and been motivated to combine Copeland's data flow controller with Dobson's interrupt driven serial port controller 10. *Id.* ¶ 146. As discussed, Dobson and Copeland relate to the ***same art*** in the ***same class/subclass*** and describe use with the ***same technology*** developed by the ***same applicant***, utilizing the ***same main component*** (a 16550 UART). *Id.*

As both Dobson and Copeland are directed to serial interfaces utilizing 16550 UARTs to provide a serial interface for a host device, a PHOSITA would have been motivated to combine Copeland's receive flow control functionality with Dobson's flow control functionality to prevent the remote transmitting device

from sending data until the host PC could read the data from the receive FIFO buffer, thereby preventing overflow of the receive FIFO buffer. *Id.*

Dobson and Copeland also state similar, and complementary, objectives. Dobson teaches providing additional buffering to reduce the number of interrupts provided to the host device instructing it to clear the buffer. *Id.* ¶ 147. Dobson explains that reducing interrupts and demands on the host device reduces instances of overwhelming the host's processor and risks of overwriting received data. EX. 1007, col. 4:27-43. Likewise, Copeland seeks to relieve "the host of the duty of managing flow control" by timely signaling a remote device to stop transmitting a data signal. EX. 1006, col. 3:3-8. Copeland's flow control operation further prevents or reduces data loss risks due to buffer overflow. *Id.*, col. 2:26-29.

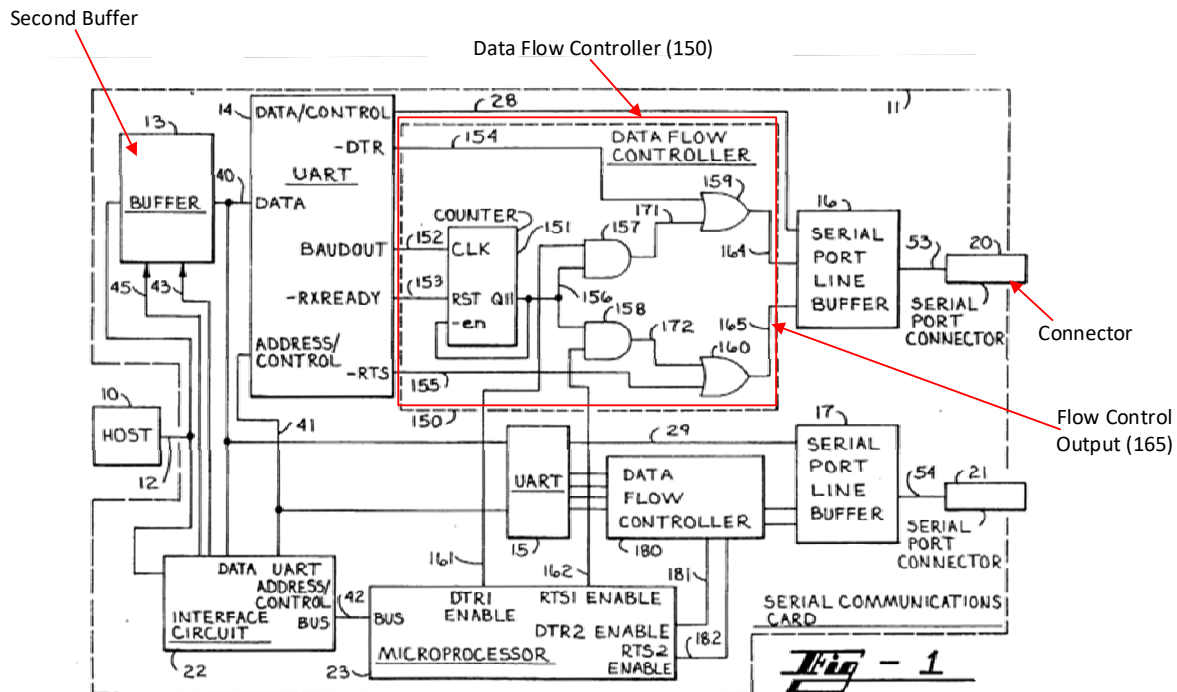
Given the complementary nature of the Dobson and Copeland systems, a PHOSITA would have been motivated to combine them to form a bulwark against data loss due to buffer overflow by both (i) increasing buffer size to reduce the amount of interrupt flow control signals provided to the host, thereby reducing the load on the host; and (ii) providing an expedient flow control system to further reduce the load on the host by performing external flow control (direct communication to transmitting device). EX. 1003, ¶ 149. For example, a PHOSITA would have been motivated to prevent Dobson's receive FIFO 100 from overflowing by providing a flow control signal to an external transmitting device

in the event the host 8 is unable to clear the buffer quickly enough to prevent an overflow after receiving Dobson's interrupt signal. *Id.*, ¶ 150. This combination furthers Dobson's and Copeland's common objective of preventing overwriting of received data without placing an undue burden on the respective host device. *Id.*, ¶ 151. Dobson would incorporate Copeland's circuitry to provide the "stop sending" signal to create the advantage articulated above. *Id.*, ¶ 150.

Dobson's and Copeland's common use of 16550 UARTs and Dobson's stated intent to be backwards compatible with devices using UARTs would provide a PHOSITA with a reasonable expectation of success in combining the references' teachings. EX. 1007, col. 4:21-25; EX. 1003, ¶ 152.

- l. and wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.***

Copeland teaches that a flow control signal is transmitted through the serial link and the connector without passing through the second buffer. EX. 1003, ¶ 153.



***Copeland FIG. 1 (Annotated)***

The data flow controller 150 is a separate circuit from the UART 14 and is configured to perform automatic flow control outside the host 10's control. EX. 1006, cols. 2:30-32, 5:65-6:11, EX. 1003, ¶ 154. The data flow controller 150 includes a counter 151 that counts a number of cycles output from the BAUDOT port of the UART 14, indicating that UART 14's internal buffer (first buffer) has at least one byte of received data stored and has not been emptied. EX. 1006, col. 5:24-38. Upon the counter reaching a value, such as 1024 (i.e., number of cycles indicating the FIFO buffer is 40% full), the counter generates a signal to drive the

outputs of the RTS and DTR signals low on the serial port connector 20 to instruct the remote device to stop transmitting. *Id.*, col. 5:38-55.

The data flow controller 150 outputs all signals (e.g., RTS and/or DTR) directly to the serial port connector 20 via the serial port line buffer. EX. 1003, ¶ 155. While the data flow controller 150's output signals pass through the serial port line buffer 16, the serial port line buffer 16 is not the claimed "second buffer." Copeland explains the serial port line buffer merely "performs standard line buffering and signal inverting functions," and FIG. 1 illustrates it is not "in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data," as required of claim 1's second buffer. *Id.* Rather, Copeland's buffer 13 equates to the claimed "second buffer" because buffer 13 controls data flow to and from the host, including to UART 14, for converting parallel data to serial data on line 40. *Id.* Copeland's flow control signal output from data flow controller 150 does not pass through the UART 14 or the buffer 13 and, therefore, does not pass through the claimed "second buffer." Accordingly, Copeland teaches the module "is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer," as claimed.

A PHOSITA would have found it obvious and been motivated to combine Copeland's data flow controller with Dobson's serial port controller 10. *Id.* ¶ 157.

As discussed, Dobson and Copeland relate to the **same art** in the **same class/subclass** and describe use with the **same technology** developed by the **same applicant**, utilizing the **same main component** (a 16550 UART). *Id.* In addition, as discussed in section VIII.D.1.k, a PHOSITA would have been motivated to combine Copeland's data flow controller with Dobson's serial port controller 10, and would have had a reasonable expectation of success in doing so. *See* EX. 1003, ¶¶ 158-165.

Accordingly, Dobson and Copeland render claim 1 obvious.

## 2. Claim 2

Claim 2 is obvious over Dobson and Copeland.

***The system of claim 1, wherein: the system is configured to transmit the first serial data and the second serial data asynchronously over the serial link.***

As noted above, Dobson's serial port controller utilizes a UART for asynchronous serial communication. EX. 1003, ¶ 166. Dobson's "enhanced serial port controller 10 provides **asynchronous**, serial digital data on line 16." EX. 1007, col. 6:12-13 (emphasis added). Line 16 is the transmit portion of the serial link, and therefore, the second serial data is transmitted "asynchronously" by the serial port controller 10. EX. 1003, ¶ 166.

Dobson further teaches that the first data is received asynchronously. EX. 1003, ¶ 167. Dobson's "enhanced serial port controller 10 also accepts

asynchronous, serial data on line 14. Asynchronous data received on line 14 is passed to the UART.” EX. 1007, col. 7:53-57. As line 14 is the serial link’s receive line, Dobson teaches that the first serial data is communicated asynchronously over the serial link. EX. 1003, ¶ 167.

Accordingly, Dobson and Copeland render claim 2 obvious.

### **3. Claim 3**

Claim 3 is obvious over Dobson and Copeland.

***The system of claim 1, wherein: the data received by the second buffer comprises parallel data.***

Dobson explains the “data stored in the transmit FIFO buffer 40 is output on data bus 23 to the UART 30. As will be familiar to those skilled in the art, the data is converted from **parallel** to serial in the UART 30 and output on line 16.” EX. 1007, col. 7:1-4 (emphasis added). As explained above, the transmit FIFO buffer 40 discloses the second buffer. Given the data stored in the transmit FIFO buffer 40 (second buffer) is later converted from parallel data to serial data, the data provided to the transmit FIFO buffer 40 must be parallel data. EX. 1003, ¶ 169. Accordingly, Dobson and Copeland render claim 3 obvious.

### **4. Claim 4**

Claim 4 is obvious over Dobson and Copeland.

***The system of claim 1, wherein: the module is further operable to repeatedly transmit the second serial data through the serial link and the connector without receiving acknowledgement during transmission.***

Dobson describes the data transmission process, which ultimately ends with the data “input to the UART 30 in parallel, [] converted by the UART 30 to serial, and [] output from the UART 30 on line 16 [serial link].” EX. 1007, col. 6:10-12. No acknowledgement or other feedback signal is required to be received before the serial port controller 10 transmits the data; data is simply serialized and transmitted. EX. 1003, ¶ 173.

Dobson’s disclosure is commensurate with the support provided for this limitation in the ’454 and ’214 patent specifications. Like Dobson, the specifications require no acknowledgment to start or maintain transmission. *Id.* ¶ 174; *see also* EX 1010, col. 10:18-25. This disclosure mirrors Dobson’s above-described data transmission in that no acknowledgment is required to start or maintain transmission. EX. 1003, ¶ 174.

Thus, Dobson and Copeland teach the claimed module “operable to repeatedly transmit the second serial data through the serial link and the connector without receiving acknowledgement during transmission.” As noted above, a PHOSITA would have understood that Dobson’s serial link would have been connected to external devices, such as a modem, through a connector, such as

Copeland's connector 20. A PHOSITA would have found it obvious and been motivated to combine Copeland's connector 20 with Dobson's serial port controller 10 and could have done so with a reasonable expectation of success. EX. 1003, ¶ 175.

Accordingly, Dobson and Copeland render claim 4 obvious.

## 5. Claim 7

Claim 7 is obvious over Dobson and Copeland.

***The system of claim 1, wherein: the flow control signal is configured to be used to control transmission of the first serial data over the serial link to prevent overflow of the first buffer.***

As noted above, Copeland teaches activating a flow control based on the receive buffer reaching a threshold fill level. EX. 1003, ¶ 177. Copeland states that “[i]t will therefore be appreciated that whenever host 10 is unable to keep up with the data transfer rate, the Q11 output of counter 151 will go high, thereby causing the DTR and/or RTS output [flow control signal] on serial port connector 20 to go low and ***signal the remote transmitter to stop sending.***” EX. 1006, cols. 5:65 – 6:2 (emphasis added). This instruction to the remote transmitter to stop sending data in response to the host processor being unable to process data in the receive FIFO quickly enough teaches a flow control signal “configured to be used to control transmission of the first serial data over the serial link to prevent overflow of the first buffer,” as recited in claim 7. EX. 1003, ¶ 178.

A PHOSITA would have found it obvious and been motivated to combine Copeland's data flow controller with Dobson's serial port controller 10 to provide a failsafe in preventing buffer overflow and would have had a reasonable expectation of success in doing so, as discussed in sections VII.D.1.k-l. *Id.* ¶¶ 179-180.

Accordingly, Dobson and Copeland render claim 7 obvious.

**6. Claim 16**

Claim 16 is obvious over Dobson and Copeland.

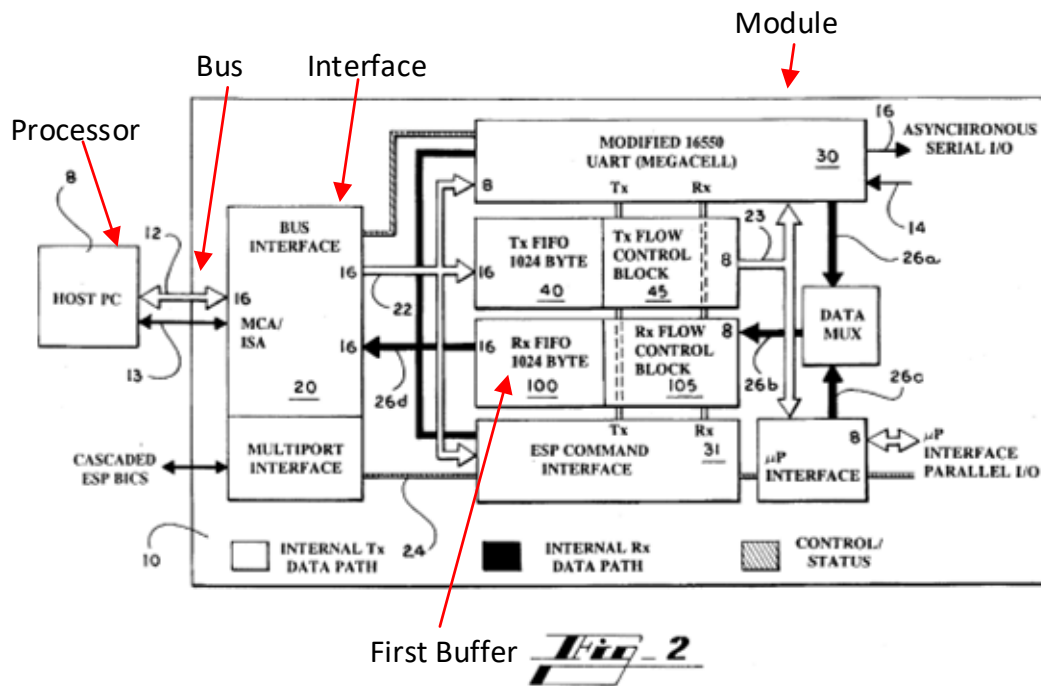
***The system of claim 1, further comprising:***

***an interface included in the module coupled to the first buffer and operable to receive the data stored in the first buffer;***

***a bus coupled to the module and configured to receive the data from the interface; and***

***a processor coupled to the bus.***

Dobson FIG. 2 (annotated below) illustrates that the enhanced processing device includes the claimed interface, bus coupled to the module, and processor coupled to the bus.



**Dobson FIG. 2 (Annotated)**

First, Dobson FIG. 2 shows that the enhanced serial port controller 10 includes a bus interface 20. EX. 1003, ¶ 182; EX 1007, FIG. 2. Dobson states that “[r]eceived data is passed from the receive FIFO buffer 100 to the host personal computer 8 via the receive data bus 26d, [and] bus interface circuit 20.” EX. 1007, col. 7:60-64. Accordingly, the bus interface 20 is “operable to receive data stored in the” FIFO 100 (first buffer of claim 1), as the data stored in the receive FIFO 100 (first buffer) must be received by the bus interface before being provided to the host PC 8. EX. 1003, ¶ 182.

Second, the interface 20 is coupled to the host PC 8 via data bus 12, which teaches the claimed “bus,” as it is coupled to the module (i.e., enhanced serial bus

controller 10) and is configured to receive data from the interface. EX. 1003, ¶ 183. Dobson states that the interface 20 is coupled to the host PC 8 via “the host personal computer data bus 12 and control bus 13, both of which are familiar to those skilled in the art.” EX. 1007, col. 5:52-58.

Finally, the bus is coupled to a host PC 8, as shown in FIG. 2, and described above. EX. 1003, ¶ 183. A PHOSITA would have understood that a PC (personal computer) would include a processor. *Id.* As the host PC is coupled to the bus 12, Dobson therefore teaches the claimed “processor coupled to the bus.”

Accordingly, Dobson and Copeland render claim 16 obvious. *Id.*

**E. Ground 5: Claim 6 is obvious over Dobson, Copeland, and Reay.**

***The system of claim 1, wherein: the module is further operable to transmit the first serial data over the serial link and to transfer the second serial data over the serial link using differential signals.***

As an initial matter, claim 6 appears to contain a typographical error in that it states that the module is operable to “transmit” the first serial data over the serial link. However, claim 1 specifically recites that the module is operable to “**receive** first serial data transmitted over the serial link.” While it is unclear what is actually intended, for this analysis, this portion of claim 6 is interpreted such that the module is operable to “receive” first serial data over the serial link using differential signals. EX. 1003, ¶ 185.

As discussed related to claim 1, Dobson teaches receiving “first serial data transmitted over the serial link through the connector and transmit the second serial data to the serial link.” *Id.* ¶ 186.

Reay teaches transmitting and receiving data using differential signals. Specifically, Reay states that “[o]utput terminals 106 and 108 provide inverted and non-inverted output signals, respectively, of the input signal received at terminal 102. Thus, **a differential**, or balanced-line, output can be provided for those interface standards that require such output.” EX. 1008, col. 4:15-20 (emphasis added). Accordingly, Reay teaches transmitting and receiving data using differential signals, as claimed.

Reay further explains the advantage of using differential outputs as “noise immunity: any noise that appears on one of the two output lines is likely to appear on the other as well and is thus cancelled as the difference between the two output signal voltages is taken.” *Id.*, col. 4:32-35. A PHOSITA would therefore have found it obvious and been motivated to combine Reay’s noise cancelling/reducing differential signal output with Dobson’s serial link to reduce errors or data corruption caused by noise on either the receive or transmit channels. EX. 1003, ¶ 187. The combination of Dobson, Copeland, and Reay, therefore, renders obvious claim 6. A PHOSITA would have had a reasonable expectation of success in modifying Dobson’s serial link with Reay’s differential signals, as the use of

differential signals for serial transmission was well known in the art at the time.

*Id.*, ¶ 188.

Accordingly, Dobson, Copeland, and Reay render claim 6 obvious.

**F. Ground 6: Claims 15 and 17 are obvious over Dobson, Copeland, and Vangemert.**

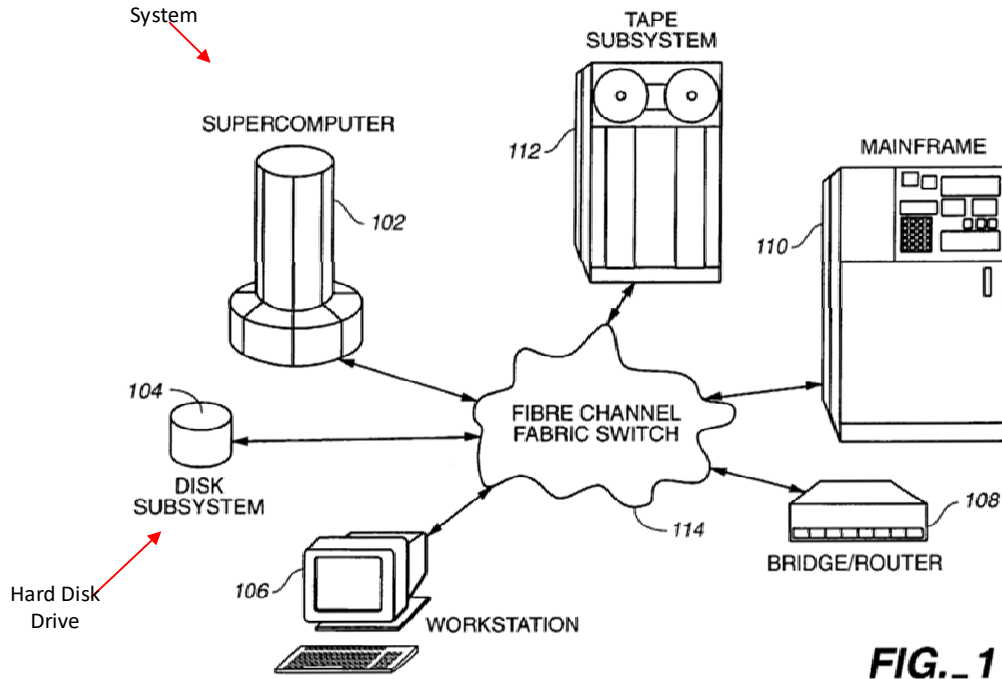
**1. Claim 15**

Claim 15 is obvious over Dobson, Copeland, and Vangemert.

***The system of claim 1, wherein the system comprises a hard disk drive.***

Dobson discloses a host PC 8, which a PHOSITA would be understood to include at least one hard disk drive. EX. 1003, ¶ 191.

If Dobson is deficient, Vangemert's FIG. 1 system includes a "disk subsystem 104." EX. 1005, FIG. 1. A PHOSITA would have understood this disk subsystem to include one or more hard disk drives. EX 1003, ¶ 191.



**Vangemert FIG. 1 (Annotated)**

A PHOSITA would have found it obvious and been motivated to combine Vangemert's disk subsystem with Dobson (and Copeland) because, for example, a high-speed serial port allows a host to communicate with peripheral devices, and a PHOSITA would understand the high-speed serial port device of the Dobson (and Copeland) system could be advantageously used to communicate with peripheral devices, like Vangemert's data storage devices. *Id.* ¶ 192. As Dobson is configured to couple to at least one external device as described above, a PHOSITA would have had a reasonable expectation of success in combining Dobson's teachings with Vangemert. *Id.*

Accordingly, Dobson, Copeland, and Vangemert render claim 15 obvious.

## 2. Claim 17

Claim 17 is obvious over Dobson, Copeland, and Vangemert.

***The system of claim 1, wherein: the module is further configured to generate a clock signal, for use by the module, using the first serial data.***

Dobson and Copeland both disclose asynchronous communication systems and, therefore, a PHOSITA would have understood them to generate clock signals using incoming data. EX. 1003, ¶ 194. While Dobson and Copeland do not discuss the details of clock signal generation, this concept must have been generally known by a PHOSITA given the lack of its disclosure in the '454 patent. *Id.* Vangemert, however, explains that “[t]ransceiver 300 includes a receiver 302 coupled to the receive channel to sense incoming signal levels [first serial data], clean them up as much as possible, and provide them to a clock recovery module 304. Clock recovery module 304 **uses** the incoming signal [**first serial data**] to **reconstruct a clock signal** synchronized to the incoming data, and a serial-to-parallel converter 306 **uses the clock signal** to convert the incoming signal from serial form to parallel form.” EX. 1005, col. 3:19-28 (emphasis added). Thus, the module “generates” (reconstructs) the clock signal for use by the module, specifically the serial-to-parallel converter 306, by using the first serial data (incoming signal/data). EX. 1003, ¶ 154.

A PHOSITA would have found it obvious and been motivated to combine Vangemert's clock recovery with Dobson's asynchronous, high-speed serial port to facilitate data synchronization as Dobson's received "data is clocked into the receive FIFO buffer 100 [first buffer] using the write signal on line 34a." EX. 1003, ¶ 155; EX. 1007, col. 8:24-25. Extracting the clock signal from the incoming serial data is an efficient and cost-effective method of creating the clock signal used in Dobson. EX. 1003, ¶ 195. Given the asynchronous communication described in Dobson and Copeland, a PHOSITA would have had a reasonable expectation of success in combining them with Vangemert's clock reconstruction.

Accordingly, Dobson, Copeland, and Vangemert render claim 17 obvious.

**G. Secondary Considerations of Nonobviousness**

Petitioner is unaware of secondary considerations indicating nonobviousness and reserves the right to respond to any such assertions by the Patent Owner. Rather, Petitioner understands that that neither Shamrock nor its predecessors ever successfully commercialized a product embodying any challenged claim.

**VIII. TRIAL SHOULD BE INSTITUTED**

The related litigation, *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.) ("Litigation"), does not warrant discretionary denial of institution under § 314(a). *See Apple Inc. v. Fintiv, Inc.*,

IPR2020-00019, Paper 11 at 5-6 (Pat. Tr. & App. Bd. Mar. 20, 2020)

(precedential).

**A. Factor 1: Either Party May Request a Stay**

Factor 1 weighs against discretionary denial of institution. Petitioner will request a stay contemporaneous with this Petition's filing.

**B. Factor 2: Proximity of Trial Date**

Factor 2 also weighs against discretionary denial. The current median time from filing to trial (civil only) in the U.S. District Court for the Eastern District of North Carolina is 36.5 months. See U.S. District Courts – Federal Court Management Statistics, December 31, 2022, [https://www.uscourts.gov/sites/default/files/data\\_tables/fcms\\_na\\_distprofile1231.2022.pdf](https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile1231.2022.pdf), p. 21. A final written decision would be issued before an estimated district court trial date in April 2025. Thus, the Board is the most efficient venue to determine the validity of the challenged claims.

**C. Factor 3: Petitioner's Diligence and Investment in IPR Outweigh the Parties' Minimal Investment in Litigation**

Factor 3 weighs against discretionary denial. The parties have not yet invested considerable resources in the Litigation, as claim construction briefs have not been filed, only one inventor has been deposed, minimal fact discovery has occurred, expert discovery has not started, and the court has not yet considered infringement or invalidity.

**D. Factor 4: There Will Be No Overlap of Issues**

Factor 4 also weighs against discretionary denial. If an IPR is instituted, Petitioner will not pursue in the Litigation the grounds raised, or that reasonably could have been raised, in the Petition, thus avoiding overlap.

**E. Factor 5: Institution Would Promote Judicial Efficiency**

All parties to the IPR are parties in the Litigation. This fact favors institution because the Board's FWD would cancel the asserted claims or bind Petitioner with estoppel if Petitioner's challenge is unsuccessful. As such "this factor does not weigh against exercising [the Board's] discretion to deny." *Cast Lighting, LLC v. Wangs Alliance Corp.*, PGR2021-00012, Paper 12 at 36 (Pat. Tr. & App. Bd. June 7, 2021).

**F. Factor 6: The Merits Strongly Favor Institution**

Factor 6 weighs against discretionary denial, as the merits are strong enough to outweigh inefficiencies from parallel litigation, and institution would promote the AIA's objectives of providing an efficient alternative to litigation.

Overall, the *Fintiv* factors weigh against discretionary denial or are neutral. Petitioner respectfully requests the Board institute this IPR.

**IX. NON-INSTITUTION UNDER § 325(D) WOULD BE IMPROPER**

The Board should institute this IPR under *Advanced Bionics* because the evidence presented was neither before the USPTO nor fully considered during

prosecution. *See Advanced Bionics, LLC v. MEDEL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6, at 6–11 (Pat. Tr. & App. Bd. Feb. 13, 2020) (precedential).

None of the relied-upon prior art references, or substantially the same references, were before the USPTO during examination. *See* EX1001, 1-2 (art of record). Accordingly, each ground alone is sufficient to find the first prong of the *Advanced Bionics* test not satisfied. *See Thorne Research, Inc. v. Tr. of Dartmouth Coll.*, IPR2021-00491, Paper 18, at 8–9 (Pat. Tr. & App. Bd. Aug. 12, 2021) (using a reference disclosing new or additional subject matter may prevent the Board from finding the art to be substantially the same).

Moreover, the references presented are not cumulative over the art cited during prosecution. The Examiner also did not have the benefit of expert testimony, like the declaration of Petitioner’s expert (EX 1003), which explains the prior art teachings, what a PHOSITA would have understood from them, and how a PHOSITA would readily combine those teachings as of the purported priority date.

The Board should reject any argument for non-institution under § 325(d).

**X. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)**

**A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)**

Petitioner Western Digital Technologies, Inc., and Western Digital Corporation, both Delaware corporations, are real parties-in-interest. Lenovo (United States), Inc., a Delaware corporation, is also a real party-in-interest.

**B. Related Matters Under 37 C.F.R. § 42.8(b)(2)**

Petitioner is not aware of any disclaimer or reexamination certificates for the '454 patent. The '454 patent is the currently subject of the following pending lawsuit: *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.), ("Litigation"). Shamrock filed the original complaint alleging infringement of the '454 patent and related '675 patent by Lenovo (United States), Inc. on March 21, 2022 and effectuated service on Lenovo on April 13, 2022. The Court recently granted WD's motion to intervene as a defendant in the Litigation. A decision on this Petition may impact the Litigation.

Additional lawsuits involving the '454 patent and related '675 patent and different defendants include: *Shamrock Innovations, LLC v. HP Inc.*, Case No. 1:21-cv-00222 (W.D. Tex.), dismissed; and *Shamrock Innovations, LLC v. Acer America Corporation et al.*, Case No. 6:20-cv-00696 (W.D. Tex.), dismissed.

Petitioner also recently filed IPR2023-00754 regarding the related '675 patent, which was given a provisional filing date of March 22, 2023.

**C. Lead and Back-Up Counsel and Service Information Under 37  
C.F.R. § 42.8(b)(3)-(4)**

Petitioner designates the following counsel.

| <b>Lead Counsel</b>                                                                                                                                                                                                                                | <b>Backup Counsel</b>                                                                                                                                                                                                                                                           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Jon R. Trembath, Reg. # 38,344<br>Michael Best & Friedrich LLP<br>675 15th Street<br>Suite 2000<br>Denver, CO 80202<br>Tel: 720.240.9515<br>Fax: 877.398.5240<br>Email: <a href="mailto:jrtrembath@michaelbest.com">jrtrembath@michaelbest.com</a> | Melanie J. Reichenberger, Reg. # 76,144<br>Michael Best & Friedrich LLP<br>790 North Water Street<br>Suite 2500<br>Milwaukee, WI 53202<br>Tel: 414.271.6560<br>Fax: 414.277.0656<br>Email: <a href="mailto:mjreichenberger@michaelbest.com">mjreichenberger@michaelbest.com</a> |
|                                                                                                                                                                                                                                                    | K. Sam Brooks, Reg. # 73,613<br>Michael Best & Friedrich LLP<br>790 North Water Street<br>Suite 2500<br>Milwaukee, WI 53202<br>Tel: 414.271.6560<br>Fax: 414.277.0656<br>Email: <a href="mailto:ksbrooks@michaelbest.com">ksbrooks@michaelbest.com</a>                          |

Please address correspondence/service to lead and backup counsel at the above addresses. Petitioner consents to email service to [mkeipdocket@michaelbest.com](mailto:mkeipdocket@michaelbest.com) (referencing 212420-0009) and copying [jrtrembath@michaelbest.com](mailto:jrtrembath@michaelbest.com), [mjreichenberger@michaelbest.com](mailto:mjreichenberger@michaelbest.com), and [ksbrooks@michaelbest.com](mailto:ksbrooks@michaelbest.com).

**XI. PAYMENT OF FEES – 37 C.F.R. § 42.103**

Petitioner authorizes charges to Deposit Account No. 133080 for the fee specified in 37 C.F.R. § 42.15 and any additional fees.

**XII. CONCLUSION**

The challenged claims are unpatentable over the art presented. Had the USPTO considered this art, it would not have allowed the challenged claims. Given the above art and argument, the Board is reasonably likely to find at least one challenged claim invalid. Petitioner respectfully requests the Board institute IPR and cancel the challenged claims.

Respectfully submitted,

Dated: April 12, 2023

s/ Jon R. Trembath  
Jon R. Trembath, Reg. No. 38,344  
Michael Best & Friedrich LLP  
675 15th Street, Suite 2000  
Denver, CO 80202  
Tel: 720.240.9515  
Fax: 877.398.5240  
[jrtrembath@michaelbest.com](mailto:jrtrembath@michaelbest.com)

Melanie J. Reichenberger, Reg. No. 76,144  
K. Sam Brooks , Reg. No. 73,613  
Michael Best & Friedrich LLP  
790 North Water Street, Suite 2500  
Milwaukee, WI 53202  
Tel: 414.271.6560  
Fax: 414.277.0656  
[mjreichenberger@michaelbest.com](mailto:mjreichenberger@michaelbest.com)  
[ksbrooks@michaelbest.com](mailto:ksbrooks@michaelbest.com)

*Attorneys for Petitioner*

**CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,880 words, according to the word-processing system used to prepare this Petition, excluding the words in the Table of Contents, Table of Authorities, Mandatory Notices, Certification Under 42.24(d), Certificate of Service, appendix of exhibits or claim listing, as set forth in 37 CFR § 42.24(a)(1).

Dated: April 12, 2023

s/ Jon R. Trembath  
Jon R. Trembath, Reg. No. 38,344  
Michael Best & Friedrich LLP  
675 15th Street, Suite 2000  
Denver, CO 80202  
Tel: 720.240.9515  
Fax: 877.398.5240

*Attorneys for Petitioner*

**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §§ 42.6(e)(4)(i) et seq. and 42.105(a), the undersigned certifies that on April 13, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

Meagan Leslie  
C. Graham Gerst  
GLOBAL IP LAW GROUP, LLC  
55 W. Monroe Street, Suite 3400  
Chicago, IL 60603  
mleslie@giplg.com  
ggerst@giplg.com

Dated: April 12, 2023

s/ Jon R. Trembath  
Jon R. Trembath, Reg. No. 38,344  
Michael Best & Friedrich LLP  
675 15th Street, Suite 2000  
Denver, CO 80202  
Tel: 720.240.9515  
Fax: 877.398.5240

*Attorneys for Petitioner*