

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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WESTERN DIGITAL TECHNOLOGIES, INC.,  
Petitioner,

v.

SHAMROCK INNOVATIONS, INC.,  
Patent Owner.

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IPR2023-00842  
Patent 9,535,454 B2

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Before SHEILA F. McSHANE, GARTH D. BAER, and  
IFTIKHAR AHMED, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”), requesting an *inter partes* review of claims 1, 2, 3, 4, 6, 7, 15, 16, and 17 of U.S. Patent No. 9,535,454 B2 (Ex. 1001, “the ’454 patent”). Shamrock Innovations, Inc. (“Patent Owner”) filed a Waiver of Preliminary Response under 37 C.F.R. § 42.107. Paper 8. We have authority under 35 U.S.C. § 314 to determine whether to institute *inter partes* review. For the reasons discussed below, we institute *inter partes* review of the challenged claims.

## II. BACKGROUND

### A. RELATED MATTERS

The ’454 patent is at issue in *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.). Pet. 83, Paper 5, 1.

### B. THE ’454 PATENT

The ’454 patent is titled “Computing Module with Serial Data Connectivity.” Ex. 1001, code (54). The patent is directed to “a modular computer system having a universal connectivity station adapted to connect and route data via serial data links to a plurality of devices.” *Id.* at 4:49–52. Patent Owner states that the ’454 patent expired on March 5, 2021. Paper 8, 1; *see also* Ex. 1001, code (63).

### C. THE CHALLENGED CLAIMS

Of the challenged claims, claim 1 is independent. Claim 1 is representative and reproduced below:

1. A system, comprising:  
a connector configured to be connectable to a serial link; and

a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, and wherein the module includes:

a receiver operable to receive the first serial data from the serial link through the connector;

a first circuit configured to deserialize the first serial data to generate deserialized data;

a decoder configured to decode the deserialized data;

a first buffer operable to store data that has been deserialized and decoded by the first circuit and the decoder, respectively;

a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and

a transmitter operable to transmit the second serial data to the serial link through the connector;

Ex. 1001, 9:55–10:21.

#### D. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner asserts the following grounds of unpatentability. Pet. 1.

| Reference(s)/Basis                             | 35 U.S.C § | Challenged Claim(s)       |
|------------------------------------------------|------------|---------------------------|
| Vangemert <sup>1</sup> , Copeland <sup>2</sup> | § 103      | 1, 2, 3, 4, 7, 15, 16, 17 |
| Vangemert, Copeland, Dobson <sup>3</sup>       | § 103      | 4                         |
| Vangemert, Copeland, Reay <sup>4</sup>         | § 103      | 6                         |

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<sup>1</sup> US Pat. No. 6,289,386 B1, Sep. 11, 2001 (Ex. 1005).

<sup>2</sup> US Pat. No. 5,179,661, Jan. 12, 1993 (Ex. 1006).

<sup>3</sup> US Pat. No. 5,717,870, Feb. 10, 1998 (Ex. 1007).

<sup>4</sup> US Pat. No. 6,005,414, Dec. 21, 1999 (Ex. 1008).

|                                |       |                   |
|--------------------------------|-------|-------------------|
| Dobson, Copeland               | § 103 | 1, 2, 3, 4, 7, 16 |
| Dobson, Copeland, Reay         | § 103 | 6                 |
| Dobson, Copeland,<br>Vangemert | § 103 | 15, 17            |

Petitioner also relies on a declaration from Dr. Michael Caloyannides (Ex. 1003).

### III. ANALYSIS

#### A. LEVEL OF SKILL IN THE ART

Petitioner contends a person of ordinary skill in the art “would have had at least a bachelor’s degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communication within or between computing devices or systems.” Pet. 11 (citing Ex. 1003 ¶ 37). Petitioner also explains that “[m]ore education can supplement practical experience and vice versa.” *Id.* At this stage, Patent Owner does not provide a description of the level of ordinary skill.

Petitioner’s description is supported by credible expert testimony. For the purpose of our decision, we adopt Petitioner’s description.

#### B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2021).

Dependent claim 17 recites “the module is further configured to generate a clock signal for use by the module, using the first serial data.” Ex. 1001, 11:42–43. Citing the claim’s plain language as well as support

from its expert, Petitioner asserts “‘generat[ing] a clock signal . . . using first serial data’ would include ways of producing a clock signal by *using* the first serial data, such as by extracting or recovering a clock signal *from* (i.e., using) the first serial data.” Pet. 13 (citing Ex. 1003 ¶ 42). For purposes of this decision, we agree with and adopt Petitioner’s construction. Although Petitioner proposes a construction for “decoder,” *see id.* at 11–12, we determine that we need not construe that term or any additional limitations to determine whether to institute *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

### C. DESCRIPTION OF PRIOR ART REFERENCES

#### 1. Vangemert (Ex. 1005)

Vangemert teaches “[a] network interface unit which implements a low latency algorithm for buffer credit calculation.” Ex. 1005, code (57). Vangemert’s Figure 3 is reproduced below.

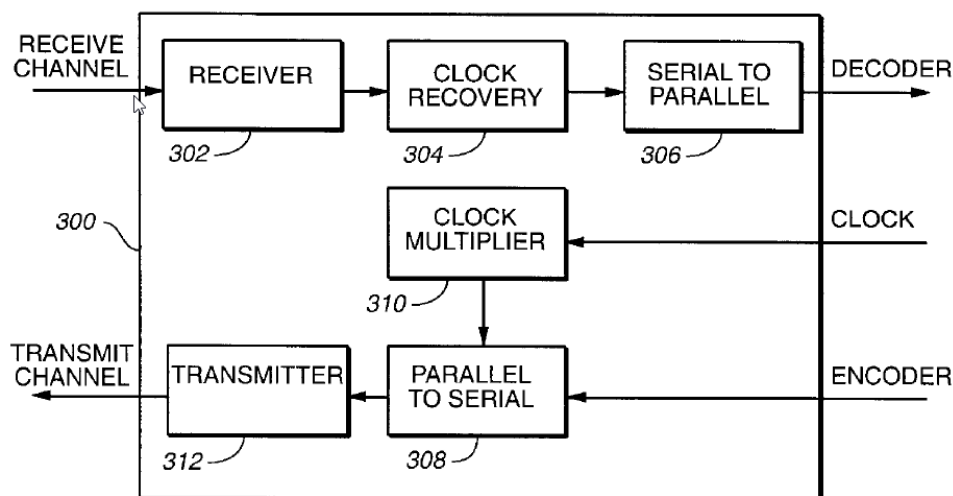


**FIG.\_3**

Figure 3 “shows a serial communication transceiver.” *Id.* at 2:41.

Figure 4 is reproduced below.

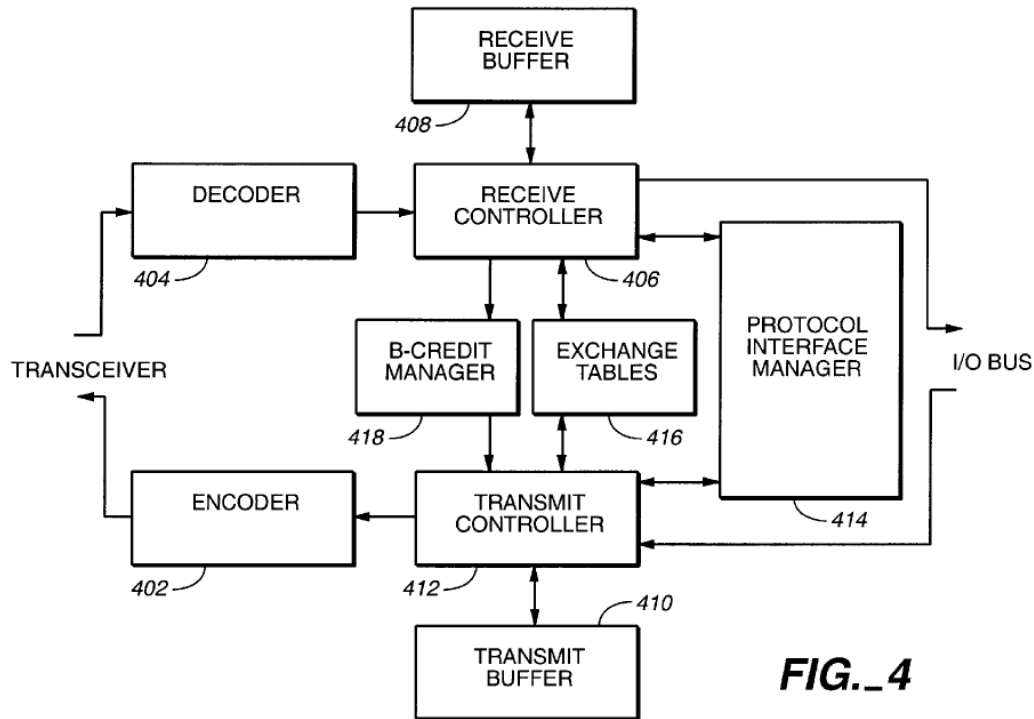


Figure 4 “shows a network interface unit.” *Id.* at 2:41.

2. Copeland (Ex. 1006)

Copeland teaches “[a] data flow controller . . . for monitoring and automatically controlling the flow of serial data from a remote transmitter to a host device.” Ex. 1006, code (57). Copeland’s Figure 1 is reproduced below.



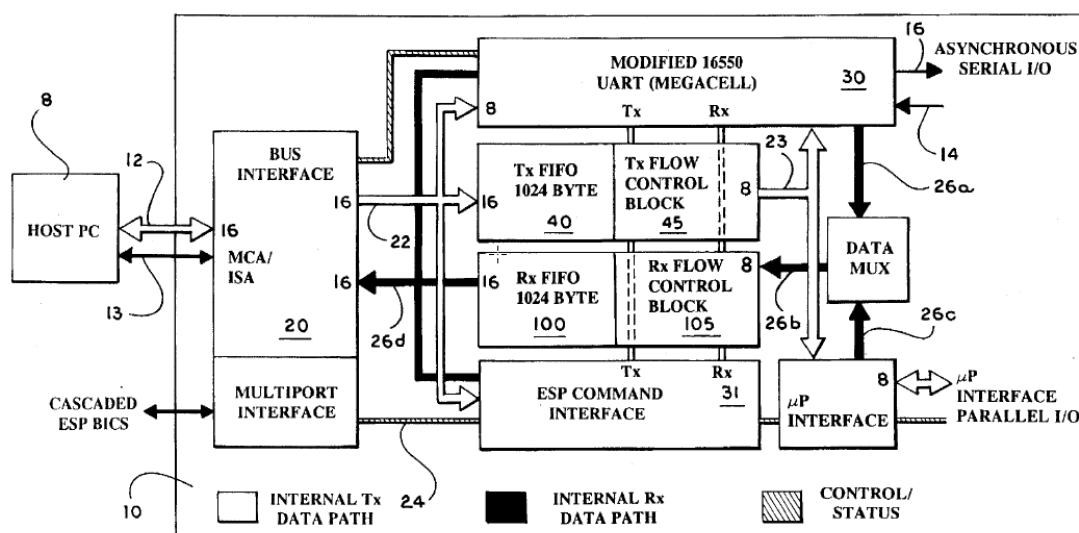


**Fig. 2**

Figure 2 is an “enhanced serial port controller.” *Id.* at 4:66–67.

#### 4. Reay (Ex. 1008)

Reay teaches “[a] mixed-mode multi-protocol serial interface driver.” Ex. 1008, code (57). Reay discloses that, as to output signals, “a differential, or balanced line, output can be provided for those interface standards that require . . . outputs.” *Id.* at 4:16–32.

### D. UNPATENTABILITY ANALYSIS

#### 1. Obviousness of Claim 1 based on Vangemert and Copeland

Petitioner contends independent claim 1 would have been obvious over Vangemert and Copeland. Pet. 13–31. Specifically, Petitioner asserts that together, Vangemert and Copeland teach claim 1’s “connector . . . connectable to a serial link” because Vangemert teaches a “serial link” while Copeland teaches “two serial port connectors 20 and 21.” *Id.* at 14–15 (quoting Ex. 1005, 2:61–63; Ex. 1006, 3:49–60). Further, Petitioner explains that a skilled artisan would have combined Copeland’s connector with Vangemert’s system “to facilitate connections between the serial link of

[Vangemert's] individual nodes 102 – 112 with one or more external devices, such as other of the nodes 102 – 112.” *Id.* at 16–17 (citing Ex. 1003 ¶¶ 49–50).

Petitioner corresponds Vangemert's “serial communication transceiver 300” to claim 1's “module,” which receives and transmits serial data. *Id.* at 18–19 (quoting Ex. 1005, 3:19–23, Fig. 3). According to Petitioner, Vangemert teaches the claimed “receiver,” “deserialize[r],” “decoder,” and “first buffer” because Vangemert's transceiver 300 includes a “receiver 302,” a “serial-to-parallel circuit 306,” a “decoder (404),” and a “buffer 408.” *Id.* at 20–23 (citing Ex. 1005, 3:21–23, 3:26–30, 3:45–48, Figs. 3, 4). Petitioner presents evidence that Vangemert teaches the claimed “second buffer” and “second circuit that is configured to serialize data” because Vangemert's transceiver includes a “transmit buffer 410” as well as a “parallel-to-serial converter 308 to serialize the data.” *Id.* at 24–25 (citing Ex. 1005, 3:31–34, 3:49–52, Figs. 3, 4). Petitioner also explains that Vangemert teaches claim 1's “transmitter” because Vangemert's transceiver includes a “transmitter 312.” *Id.* at 26 (citing Ex. 1005, 3:35–36, Fig. 3).

For claim 1's first wherein clause—“wherein the module is configured to determine whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer”—Petitioner explains that Vangemert discloses that its “[r]eceive controller 406 includes a counter or register which tracks the amount of available buffer space [of] the receive buffer 408,” and “[a] comparator 502 within a buffer credit manager determines whether buffer space committed but not yet occupied is less than a buffer capacity by a predetermined amount.” *Id.* at 27 (citing Ex. 1005, 4:32–34, Ex. 1003 ¶ 67).

For claim 1’s second wherein clause—“wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,” Petitioner relies on Copeland. *Id.* at 28–30. Specifically, according to Petitioner, while Vangemert’s control signal is sent when its buffer has sufficient space, Copeland teaches “data flow control is activated when the FIFO buffer is forty percent full . . . by sending a low Request to Send (‘RTS’) signal over the connector 20 to instruct a remote device to stop sending data.” *Id.* at 28–29 (citing Ex. 1005, 5:38–40, Ex. 1003 ¶¶ 71–72). Petitioner explains, with relevant support from its expert, that a skilled artisan “would have found it obvious to either (i) combine Copeland’s flow control signal generation with Vangemert’s [control] manager 418, as a redundancy to prevent receive buffer overflow or (ii) substitute Copeland’s flow control signal for Vangemert’s [control] signal to safeguard the receive buffer from data overflow.” *Id.* at 29 (citing Ex. 1003 ¶¶ 73–74).

For claim 1’s terminal wherein clause—“wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer”—Petitioner explains that “both Vangemert and Copeland teach directly transmitting flow control signals, avoiding their respective transmit buffers,” and that one skilled in the art would know to do so “to minimize latencies.” *Id.* at 30–31 (citing Ex. 1005, col. 4:11–16, Ex. 1003 ¶¶ 77–82); Ex. 1003 ¶¶ 81–82 (citing Ex. 1006, 2:30–32, 3:46–4:21, 4:37–38, 5:24–52, 5:65–6:11, Fig. 1).

We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently

demonstrates a reasonable likelihood of succeeding in its obviousness challenge to claim 1 based on Vangemert and Copeland.

2. Obviousness of Claims 2, 3, 4, 7, 15, 16, and 17 Based on Vangemert and Copeland

According to Petitioner, Vangemert teaches the additional features recited in the challenged dependent claims, including asynchronous transmission (claim 2), receiving parallel data (claim 3), transmission without acknowledgement (claim 4), overflow prevention (claim 7), a hard disc drive (claim 15), a bus and processor (claim 16), and clock signal (claim 17). *Id.* at 31–43. As noted above, Patent Owner does not challenge Petitioner’s analysis at this stage. We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenges to claims 2, 3, 4, 7, 15, 16, and 17 based on Vangemert and Copeland.

3. Additional Grounds with Vangemert as Primary Reference

Petitioner additionally asserts claim 4 would have been obvious over Vangemert, Copeland, and Dobson (*id.* at 43–44) and claim 6 would have been obvious over Vangemert, Copeland, and Reay (*id.* at 44–46). For these two grounds, Petitioner adds Dobson to address claim 4’s transmission without acknowledgement (*id.* at 44) and adds Reay to address claim 6’s differential signals (*id.* at 46). As noted above, Patent Owner does not challenge Petitioner’s analysis at this stage. We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenge to claim 4 based on Vangemert,

Copeland, and Dobson, and to claim 6 based on Vangemert, Copeland, and Reay.

4. *Additional Grounds with Dobson as Primary Reference*

Petitioner asserts three alternative grounds with Dobson as its primary reference. *Id.* at 47–79. Here, Petitioner relies on Dobson for teaching the claimed module, receiver, deserializer, decoder, first buffer, second buffer, and transmitter (*id.* at 51–60) and, once again, on Copeland for teaching the claimed connector and flow control signal that does not pass through the second buffer (*id.* at 53, 61–68). Petitioner adds Reay to address claim 6’s differential signals (*id.* at 75), and adds Vangemert for teaching claim 15’s hard disc drive, and claim 17’s clock signal (*id.* at 76–79). As noted above, Patent Owner does not challenge Petitioner’s analysis at this stage. We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its additional challenges to claims 1, 2, 3, 4, 6, 7, 15, 16, and 17 based on Dobson, Copeland, and Reay/Vangemert.

#### IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. ORDER

Accordingly, it is:

ORDERED that *inter partes* review of claims 1, 2, 3, 4, 6, 7, 15, 16, and 17 of the '454 patent is instituted on all grounds in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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