

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner,

v.

SHAMROCK INNOVATIONS, INC.,

Patent Owner.

Case No. IPR2023-00842

U.S. Patent No. 9,535,454

PATENT OWNER'S RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Ex. 2001	CV of Terry R. Lee
Ex. 2002	Declaration of Terry R. Lee
Ex. 2003	File History of U.S. Patent Appl. 09/130,058, filed August 6, 1998
Ex. 2004	'454 Patent Family Tree
Ex. 2005	U.S. Patent 5,613,141 (Szatkowski)
Ex. 2006	U.S. Patent 6,192,422 (Daines)
Ex. 2007	C. J. Georgiou and C. . -S. Li, "Scalable protocol engine for high-bandwidth communications," Proceedings of ICC'97 - International Conference on Communications, Montreal, QC, Canada, 1997, pp. 1121-1126 vol.2, doi: 10.1109/ICC.1997.610064.
Ex. 2008	Network World - July 31, 1995 - Page 64
Ex. 2009	The RS232 STANDARD. A Tutorial with Signal Names and Definitions. (renamed the "EIA232 Standard" in the early 1990's) Copyright © 1993-1997 by CAMI Research
Ex. 2010	Phil Storrs PC Hardware book The SCSI Interface (Small Computer Systems Interface) Copyright © Phil. Storr, last updated December 4 1998
Ex. 2011	Phil Storrs PC Hardware book The PC and Interrupts Copyright © Phil. Storr, last updated December 26 1998
Ex. 2012	An Introduction to Fibre Channel by M Primmer · October 1996 Hewlett-Packard Journal 1.
Ex. 2013	AMENDED COMPLAINT for Patent Infringement against Lenovo (United States), Inc., filed by Shamrock Innovations, LLC. 5:22cv102, Shamrock Innovations, Llc V. Lenovo (United States), Inc.
Ex. 2014	Joint Claim Construction Statement by Shamrock Innovations, LLC 5:22cv102, Shamrock Innovations, Llc V. Lenovo (United States), Inc.

Ex. 2015	Joint Claim Construction Statement Exhibit A by Shamrock Innovations, LLC 5:22cv102, Shamrock Innovations, Llc V. Lenovo (United States), Inc.
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I. INTRODUCTION

The Petition challenges claims 1, 2, 3, 4, 6, 7, 15, 16, and 17 (“Challenged Claims”) of U.S. Patent No. 9,535,454 (“‘454 Patent,” Ex. 1001) under six grounds of unpatentability. The Board should find that Petitioner has failed to demonstrate the unpatentability of the Challenged Claims. The cited references lack at least one limitation of each of the Challenged Claims, and would not have been combined for the reasons alleged in the Petition by a person of ordinary skill in the art. Patent Owner’s explanations herein are supported by the Declaration of Terry E. Lee, an expert in the field. Ex. 2002.

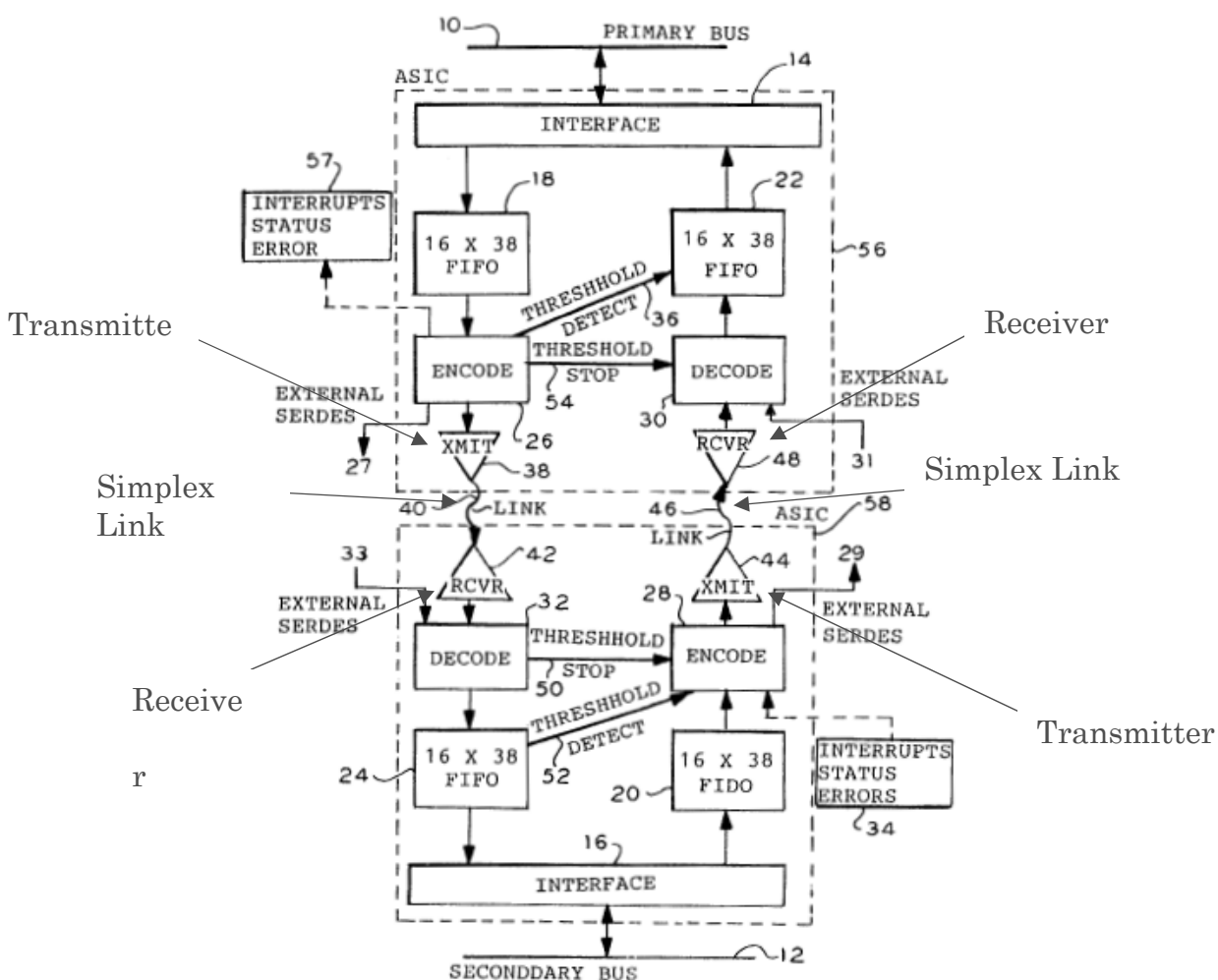
II. THE ‘454 PATENT SPECIFICATION

The Specification of the ‘454 Patent discloses a duplex serial connection formed with a pair of simplex links that pass data, referred to collectively as a serial data link. For example, the Specification¹ provides:

¹ The Specification of the ‘454 Patent claims priority based on a chain of earlier continuation and continuation-in part-applications, "all of which are incorporated by reference in their entireties." Ex. 1001, 1:7-20. One of the applications incorporated by reference is U.S. Patent Appl. 09/130,058, filed August 6, 1998 (the “’058 Application”)(*id.*, 1:19), a copy of which is attached as Ex. 2003. The ‘058 Application matured into U.S. Patent 6,070,214 (the “’214 Patent”) (Ex. 1010). For simplicity, the citations evidencing support in the ‘058 Application set forth herein correspond to the column and line numbers in the ‘214 Patent.

By employing apparatus and methods of the foregoing type, an improved system is achieved for transferring information between buses. In one preferred embodiment, two buses communicate over a duplex link formed with a pair of simplex links, each employing twisted pair or twin axial lines (depending on the desired speed and the anticipated transmission distance). Information from the buses are first loaded onto FIFO (first-in first-out) registers before being serialized into frames for transmission over the link. Received frames are deserialized and loaded into FIFO registers before being placed onto the destination bus. Ex. 1010, 4:16-28 (emphasis added).

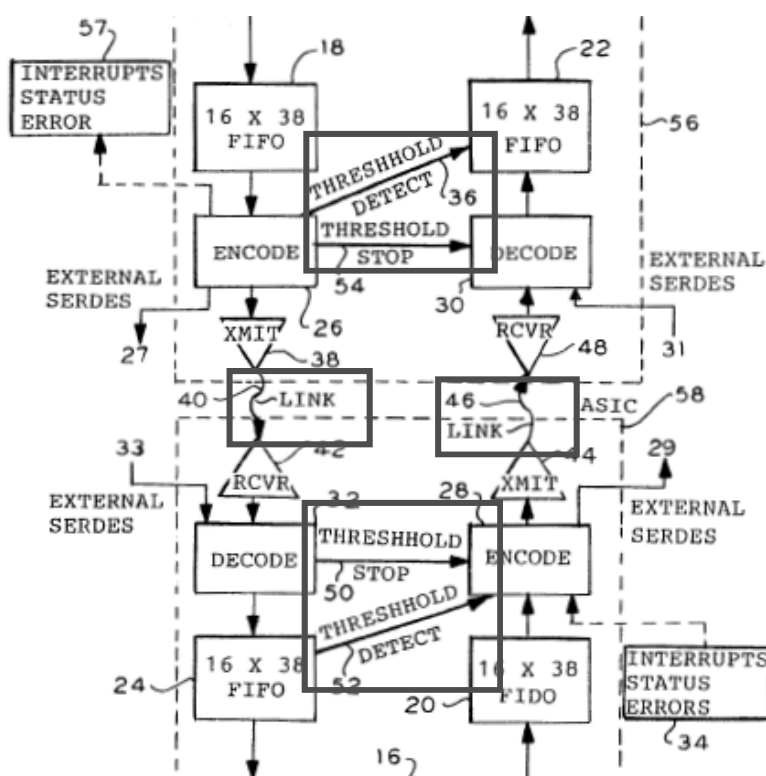
The Specification discloses an exemplary implementation of a serial data link in which frames produced by a first encoder are forwarded through a first transmitter via a first simplex link to a first receiver, which supplies the serial information to a first decoder. Likewise, a second encoder forwards serial information through a second transmitter along a second simplex link to a second receiver, which supplies the serial information to a second decoder. Ex. 1010, 6:39-46; Ex. 2002, 47. The Specification depicts this exemplary implementation as follows (red annotations by Patent Owner):



Ex. 1010, Figure 1. In connection with the above diagram, the Specification explains that “[f]rames produced by encoder 28 are forwarded through transmitter 44 along simplex link 46 to receiver 48, which supplies the serial information to decoder 30. Likewise, encoder 26 forwards serial information through transmitter 38 along simplex link 40 to receiver 42, which supplies the serial information to decoder 32.”

Ex. 1010, 6:39-46.

In connection with this implementation, the Specification identifies an overflow danger relating to registers (or buffers) 22 and 24, and discloses a flow control technique for addressing that danger. *Id.*, 6:47-48; Ex. 2002, 49. According to the disclosed example, each register generates a “threshold detect” signal when it is “almost full.” *Id.*, 6:49-50. The “threshold detect” signal is then forwarded via a simplex link to the decoder on the side of the link. That decoder then issues a “threshold stop” signal to an encoder, which then stops forwarding information to the register that originally generated the “threshold detect” signal. *Id.*, 6:49-58; Ex. 2002, 49. The Specification depicts the signal flow of the “threshold detect” and “threshold stop” signals as shown below (Patent Owner annotations in red). The diagram contains an obvious error, in that the arrow for signal 36 should point in the opposite direction (Ex. 2002, 49):



In connection with the above diagram, the Specification explains that “if FIFO register 22 is almost full, it supplies a threshold detect signal 36 to encoder 26, which forwards this information through link 40 to decoder 32. In response, decoder 32 issues a threshold stop signal 50 to encoder 28, which then stops forwarding serial information, thereby preventing an overflow in FIFO register 22. In a similar fashion, a potential 55 overflow in FIFO register 24 causes a threshold detect signal 52 to flow through encoder 28 and link 46 to cause decoder 30 to issue a threshold stop signal 54, to stop encoder 26 from sending more frames of information.” *Id.*, 6:48-58; Ex. 2002, 50.

Two aspects of the disclosed flow control example are worth emphasizing. First, each register (or buffer) 22 or 24 generates a flow control signal (referred to as a “threshold detect” signal) by comparing its fill amount to a threshold corresponding to being “almost full.” Ex. 2002, 49. Second, as shown in the diagram, the flow control signal generated by one register is transmitted in a manner that does not traverse the other register.

III. THE CHALLENGED CLAIMS OF THE '454 PATENT

Independent Claim 1 is representative of the Challenged Claims, and recites:

1. A system, comprising:

a connector configured to be connectable to a serial link; and

a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, and wherein the module includes:

a receiver operable to receive the first serial data from the serial link through the connector;

a first circuit configured to deserialize the first serial data to generate deserialized data;

a decoder configured to decode the deserialized data;

a first buffer operable to store data that has been deserialized and decoded by the first circuit and the decoder, respectively;

a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and

a transmitter operable to transmit the second serial data to the serial link through the connector;

wherein the module is configured to determine whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer; and
wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount, and wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.

Claim 1 captures the aspects of the disclosed flow control example emphasized above. Specifically, in response to the fill amount of a first buffer (e.g., register 22) being at or above a threshold, the module that includes the first buffer generates a flow control signal (e.g., the “threshold detect” signal), which is forwarded through the serial link (e.g., the simplex link) without passing through the second buffer (e.g., register 24). Ex. 2002, 42.

IV. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner has proposed that a POSITA for the ‘454 Patent “would have had at least a bachelor’s degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communication within or between computing devices or systems.” (Pet., 11) Petitioner further alleged that “More education can supplement practical experience and vice versa.” Patent Owner does not dispute the minimum qualifications for a POSITA proposed in the Petition. Ex. 2002, 35-36.

V. CLAIM CONSTRUCTION

The Federal Circuit explains that “[t]he terms used in the claims bear a presumption that they mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art.” *Honeywell Int’l, Inc. v. ITC*, 341 F.3d 1332, 1338 (Fed. Cir. 2003). Accordingly, “[p]roperly viewed, the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1358 (Fed. Cir. 2017). Further, “[t]he written description and other parts of the specification, for example, may shed contextual light on the plain and ordinary meaning.” *Aventis Pharm., Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013). As a result, although the “plain and ordinary meaning” is not based on any specialized definition, the meaning of the terms is established based on how a person of ordinary skill at the time (POSITA) would have understood the terms in the claim in the context of the entire patent, including the specification and the drawings.

In the present case, none of the terms in the Challenged Claims require a meaning other than the plain and ordinary meaning that a POSITA would apply after having read the patent in its entirety.²

VI. SUMMARY OF CITED REFERENCES

A. Vangemert

U.S. Patent 6,289,386, issued on September 11, 2001 (“Vangemert”), details an approach to buffer credit calculation in high-speed serial communication networks, particularly for systems using the Fibre Channel protocol. Vangemert introduces a network interface unit equipped with a low latency algorithm to manage buffer credits more efficiently. This unit comprises a receive buffer, a receive controller, a transmit controller, and a buffer credit manager. The buffer credit manager is responsible for calculating committed buffer space based on data stored in the receive buffer and signals from both the receive and transmit controllers. It uses a comparator to assess whether the available buffer space exceeds the committed, unoccupied space plus the maximum frame size, ensuring efficient and timely flow control in the network. (Ex. 2002, 55).

² In the parallel district court litigation, in which Petitioner is an intervenor, the defendant Lenovo proffered additional claim construction (see Ex. 2015). The Patent Owner maintains that no additional claim construction is required and all claims terms should have their plain and ordinary meaning.

Specifically, Vangemert describes that “[t]he buffer credit manager iteratively determines the additional committed buffer space (i.e., the space committed but not yet occupied by receive data) by counting the number of receive and transmit flags, and generates the credit signal using a comparator which compares the sum of additional committed buffer space and the maximum frame size to the available receive buffer storage capacity and asserts the credit signal if the available buffer space is greater than or equal to the sum of the maximum frame size and the additional committed buffer space.” (Ex. 1005, 2:19-29; Ex. 2002, 56) Vangemert’s buffer credit manager is graphically depicted in Figure 5 (reproduced below).

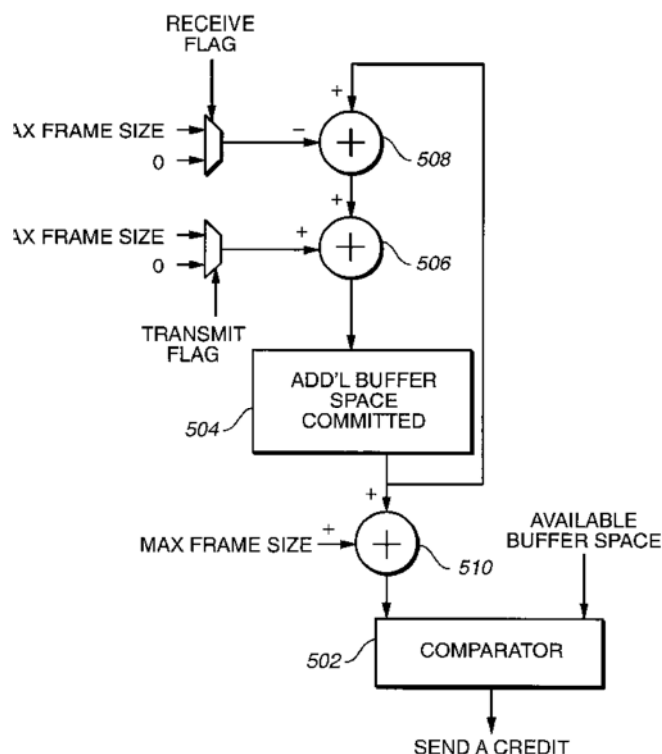


FIG. 5

With regard to Figure 5, Vangemert states:

Since the data storage required for completely received frames is accounted for in the available buffer space, the buffer credit manager doesn't need to continue reserving space for it. Since the actual amount of stored data is being used in this iterative buffer-credit management strategy, more efficient use of the buffer space is possible. When the size of the received data frames is less than the maximum frame size, the extra space can add up to allow additional buffer credits to be sent. Using this strategy, the number of credits made available by the buffer credit manager is at least equal to the maximum buffer capacity divided by the frame size, but it may be greater when received data frames are smaller than the maximum frame size. Importantly, the credits are generated quickly since only additions, subtractions, and comparisons are used. This incremental "one-more-credit?" evaluation is well

suited to the serial communication channel since only one credit can be sent at a time anyway. The hardware implementation of this buffer credit manager is advantageously fast, simple and inexpensive. (Ex. 1005, 4:52-5:4)

Accordingly, Vangemert describes a system where the buffer credit manager issues credits in proportion to the available space in the receiver's buffer. If there is no space in the buffer of the receiver, the transmitter cannot transmit. As a result, the buffer credit manager makes buffer overflows *impossible*. (Ex. 2002, 58).

B. Copeland

U.S. Patent 5,179,661, issued on January 12, 1993 ("Copeland"), describes a method and apparatus for automatically controlling the flow of serial data from a remote transmitter to a host device. The system includes a serial communications card with a UART (Universal Asynchronous Receiver/Transmitter) that has a buffer. A counter tracks the number of bytes received by the UART since the host last read all data in the buffer. If this count exceeds a predefined portion of the buffer capacity, it triggers a control signal to the remote transmitter to stop sending data, thus controlling data flow without the host's intervention. (Ex. 2002, 59).

Copeland outlines a mechanism within an asynchronous serial communications adapter card for host computers. It features a 16550A UART and a microprocessor, which can enable or disable the automatic flow control feature. The system includes circuitry to perform this automatic flow control, along with

gates allowing the microprocessor to manage the flow control circuitry. (Ex. 2002, 60).

The UART uses a BAUDOUT signal, a clock at 16 times the baud rate, and an inverted -RXREADY signal, which activates when there is at least one byte of serial data in the UART's 16-byte FIFO buffer. The flow control is executed through these signals and a counter. When the -RXREADY signal goes low, indicating the FIFO buffer isn't empty, the counter is enabled and starts counting the BAUDOUT cycles. Once a predetermined number of cycles is counted, it signals the remote transmitter to halt data transmission. (Ex. 2002, 61) In this regard, Copeland describes that:

After a predetermined number of BAUDOUT cycles are counted without the FIFO buffer being empty an output of the counter is enabled which disables the counter. This output deasserts the DTR and/or RTS signals to the remote transmitter. This signals the remote transmitter to stop sending. The enabling of the counter output thus results in the remote transmitter halting its transmission of data. (Ex. 1006, 2:56-63).

Copeland's process that automatically manages data flow, preventing overflow and data loss, is graphically depicted in Figure 3 (reproduced below).

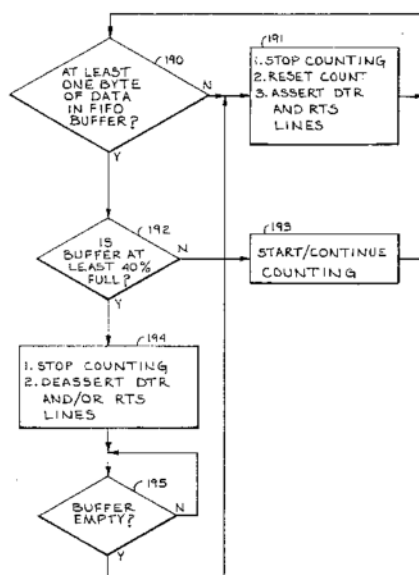


Fig. 3

Specifically, Copeland teaches a system where “data flow control is activated when the FIFO buffer is forty percent full.” (Ex. 1006, 5:39-40) Copeland further explains that the “data flow control drives either the DTR (Data Terminal Ready) or the RTS (Request To Send) line of the serial card to a “not ready” status to halt the flow of serial data from the remote transmitter.” (Ex. 1006, 2:12-16) By way of example, Copeland explains that “[t]he count of 1024 BAUDOUT cycles represents 64 bit times or, at 10 bits per character, 6.4 character times” (Ex. 1006, 5:33-35) and “[t]his leaves at least 9.6 character times remaining for the remote transmitter connected to serial data port 20 to respond before the FIFO buffer overflow.” (Ex. 1006, 5:35-38) Accordingly, Copeland teaches a system where transmission of data is halted when the receiver’s buffer reaches a

limit so that the amount of inflight data does not cause a buffer overflow. (Ex. 2002, 64).

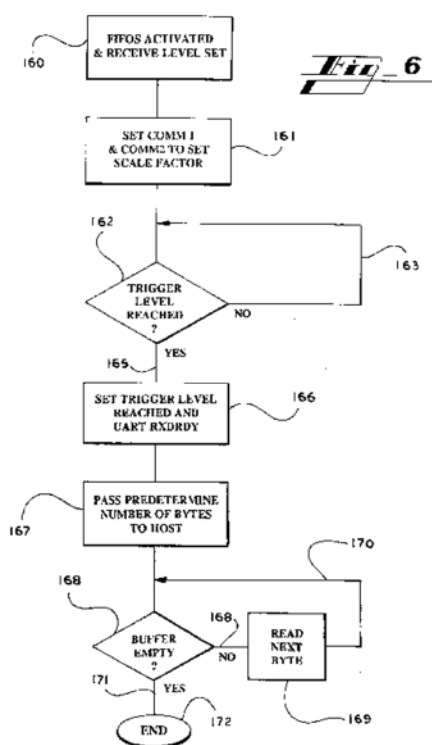
C. Dobson

U.S. Patent 5,717,870, issued on February 10, 1998 (“Dobson”), presents an advanced controller for serial ports in computers, particularly enhancing functionality with universal asynchronous receiver/transmitters (UARTs). The disclosure includes an expanded buffer, which connects to either the transmitter or receiver buffer of the UART. This setup significantly increases the data storage capacity for transmitted or received data through the serial port. (Ex. 2002, 65).

Dobson describes a scalable trigger circuit associated with the expanded buffer. This circuit detects when the data in the expanded buffer reaches a predetermined level and produces a service request signal. Furthermore, Dobson introduces a timer that responds to the service request signal to provide an interrupt signal to the computer. After an interrupt is serviced, the timer resets the interrupt signal and starts a predefined timeout period. During this period, the system is non-responsive to subsequent service requests, preventing repetitive interrupts. This mechanism reduces the load on the computer’s processing resources by managing the interrupt signals more effectively. (Ex. 2002, 66) In this regard, Dobson provides:

Basically stated, the present invention, which is embodied as a part of this device, is a set of expanded of transmit and receive FIFOs, together with scalable trigger level circuits to control the generation of service requests for data in the buffers. In particular, the present invention provides expanded buffers with scalable trigger levels for generation of service requests that are likewise expanded to approximately mimic the conventional selectable trigger levels of the type 16550 UART. This allows the present invention to be used with applications and devices that select one of the conventional trigger levels (i.e., 1, 4, 8, or 14 bytes in a 16 byte buffer) to physically select a larger number of bytes as the trigger level, in a way that will be essentially transparent to the application running on the computer. Therefore, the present invention can be used with much higher data rate modems in concurrent processing environments with respect to a conventional type 16550 UART, yet reliably handle high speed incoming and outbound data and servicing interrupts generated by the received data buffer without the loss of data. (Ex. 1007, 3:33-52)

Dobson's system of managing interrupt signals more efficiently is graphically depicted in Figure 6 (reproduced below).



Accordingly, Dobson teaches a system where interrupt signals are calculated and transmitted to a computer. (Ex. 2002, 69).

D. Reay

U.S. Patent No. 6,005,414, titled “Mixed-mode multi-protocol serial interface driver,” describes a driver that operates in both current-mode and voltage-mode. It is designed to conform output signals to various electrical interface standards, such as CCITT/EIA standards V.35, V.11/RS-422, V.28/RS-232, and V.10/RS-423. Reay features a mode-select input signal that enables the selection of a particular standard, activating the appropriate circuitry for that standard. When

certain parts of the circuitry are not in use, they are placed in a high impedance state to prevent interference with the active sections. (Ex. 2002, 70).

VII. THE PETITION FAILS TO DEMONSTRATE THE UNPATENTABILITY OF THE CHALLENGED CLAIMS

A. The Proposed Combination of Vangemert and Copeland Fails To Render The Challenged Claim Obvious Under 35 USC §103

1. Vangemert and Copeland Would Have Led A Person Of Ordinary Skill Away From The Combination Proposed In The Petition

“[A] showing that a prior art reference teaches away from a given combination is evidence that one of skill in the art would not have been motivated to make that combination to arrive at the claimed invention.” *Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, 853 F.3d 1370, 1379-80 (Fed. Cir. 2017). The Federal Circuit explains that “[a] reference teaches away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken in the claim.” *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017)(internal citation and markings omitted). In the present case, a POSITA, upon reading Vangemert or Copeland, would be led in a direction that diverges from the proposed combination. (Ex. 2002, 72-73).

Specifically, a POSITA would understand that “Vangemert teaches a flow control scheme based on buffer credits, which makes overflow impossible” and “Copeland teaches using a flow control signal to stop transmission to avoid a possible overflow, (i.e., in a system where overflow is possible). (Ex. 2002, 72). Accordingly, there would be no purpose in using a flow control signal to stop potential overflow when overflow is not possible, and therefore, the teachings of Vangemert and Copeland are divergent, and there is no motivation to combine Vangemert’s and Copeland’s flow control solutions.” (Ex. 2002, 72).

a. Vangemert Teaches A System That Uses Buffer Credits, Thereby Making Overflow Impossible

As explained by Terry Lee:

Buffer credits are a vital flow control mechanism in high-speed networks like Fibre Channel, designed to manage data transfer efficiently and prevent loss. Each device in the network has limited buffer space for incoming data, and buffer credits track this space’s availability. This tracking is crucial for maintaining an orderly data transfer process and ensuring that the receiver’s buffer isn’t overrun by incoming data. (Ex. 2002, 78)

A POSITA would understand that buffer credits serve as a communication mechanism between a sender and a receiver in data transmission. The receiver allocates a certain number of buffer credits to the sender, corresponding to the amount of data it can process simultaneously. Each credit usually represents a data unit, like a frame. As the receiver processes data and frees up space, it sends

additional credits to the sender. This ongoing exchange allows the sender to adjust its data transmission rate based on the receiver's processing capacity, ensuring a smooth and efficient flow of data. (Ex. 2002, 79-80).

Accordingly, a POSITA would understand that “[i]n a credit-controlled system, the receiver communicates this information by sending back a certain number of buffer credits to the sender. As a result, when the sender receives buffer credits, it knows how many units of data it can send without overwhelming the receiver's buffer.” (Ex. 2002, 83)

Vangemert implements a credit-controlled system from the Fibre Channel protocol. Specifically, Vangemert explains that “Under this methodology, before a first network node (initiating node) can transmit a data frame to a second network node (responding node), the initiating node must first receive a buffer credit from the responding node, indicating that the responding node has available space in its receive buffer for a data frame.” (Ex. 1005, 1:49-54; Ex. 2002, 84). Since the initiating node is required to receive the buffer credit in advance of sending the data, the possibility of buffer overflow is eliminated in such a credit-controlled system. (Ex. 2002, 84). Vangemert focuses on enhancing the buffer credit-based system to optimize the utilization of the receive buffer. This approach addresses the challenge of predetermining the number of buffer credits, which is complicated due to the

variability in the maximum frame size. Relying on a worst-case scenario for buffer credit allocation, as currently required, leads to inefficient usage of the receive buffer. To address this issue, Vangemert proposes the need for a low-latency method in the determination of buffer credits, aiming to improve the system's efficiency. (Ex. 1005, 1:58-63; Ex. 2002, 85).

Vangemert's method to prevent receiver buffer overflow in a buffer credit-based system involves ensuring that a transmitter only sends data frames when the receiver has confirmed sufficient buffer space. This process requires the receiving node to grant advance permission, indicated through buffer credits before the transmitter can proceed. Ex. 1005, 2:3-6; Ex. 2002, 86. The buffer credit manager plays a crucial role in this system. It continually assesses the additional buffer space that is committed but not yet occupied by calculating the number of received and transmitted flags. It then generates a credit signal by comparing the total of this additional committed buffer space and the maximum frame size against the receiver's available buffer storage capacity. The credit signal is asserted only if the available buffer space can accommodate the sum of the maximum frame size and additional committed buffer space. (Ex. 1005, 2:19-29; Ex. 2002, 86).

In addition, Vangemert explains how control signals and control words are integral to this flow control system. The buffer credit manager, upon being enabled,

instructs the transmit controller to begin sending buffer credit control words based on the credit signal it generates. Ex. 1005, 4:13-16; Ex. 2002, 86. This system ensures that data frames and control words are efficiently transported from a source node's transmit channel to a destination node's receive channel through a fabric switch. (Ex. 1005, 2:66-3:1, 4:13-16; Ex. 2002, 86). The underlying principle of this method is that a transmitter is only activated to transmit data frames when there is adequate space in the receiver's buffer, thus effectively preventing buffer overflow. (Ex. 2002, 86).

As a result, as explained by Terry Lee, "a POSITA would also understand that the buffer credit manager calculates available space, sends a buffer credit signal if sufficient space is available, and buffer control words are then sent to the transmit node via buffer control words, and that these buffer control words or "credits" enable the transmitter to send data frames." Without buffer credits, the transmitter is not allowed to send data frames and overflow the receiving buffer." (Ex. 2002, 87).

b. Copeland Teaches Using Out-of-Band Flow Control Signals To Stop Buffer Overflow

On the other hand, a POSITA would understand that in Copeland's system, overflow is indeed possible because the transmitter is not required to obtain advance permission from the receiver prior to transmitting data. Instead, "Copeland teaches using a flow control signal to stop transmission to avoid a possible overflow." (Ex.

2002, 88). Specifically, Copeland's system is designed to prevent data overflow in a receive buffer by signaling the transmitter to stop sending data when the receive buffer is getting full. In the preferred embodiment, the buffer stops at forty percent capacity. (Ex. 1006, 5:28-40; Ex. 2002, 88).

Copeland's mechanism involves a UART (Universal Asynchronous Receiver-Transmitter) with a BAUDOUT signal, a clock at 16 times the baud rate. A counter tracks BAUDOUT cycles, and when 1024 cycles pass without the FIFO (First In, First Out) buffer emptying, an output signal is triggered. This count of 1024 BAUDOUT cycles equals 64 bit times or 6.4 character times. This leaves about 9.6 character times for the remote transmitter to stop before the FIFO buffer overflows. Ex. 1006, 5:28-40. The system taught in Copeland also includes sending a low signal for the RTS (Ready To Send) and DTR (Data Terminal Ready) signals on the serial port, instructing the remote transmitter to stop sending data and thereby preventing data overflow in the UART's FIFO buffer. (Ex. 1006, 5:51-55; Ex. 2002, 88)

As a result, "a POSITA would understand that as the buffer becomes relatively full, a signal is sent to the transmitter to stop transmitting data frames so receive buffer overflow could be avoided, and that a certain amount of latency, 9.6 character times in the preferred embodiment, is provided for the transmitter to respond to avoid the receive buffer overflow." (Ex. 2002, 88)

Simply put, no purpose would be served by supplementing Vangemert's system where an overflow is impossible, with Copeland's flow control techniques designed to minimize overflow risk in systems where overflow is possible. Therefore, there would be no motivation to combine Vangemert's and Copeland's flow control solutions. (Ex. 2002, 89).

2. The Rational Proffered In The Petition For Combining Vangemert and Copeland Is Erroneous

Petitioner erroneously alleges that "If Copeland's teachings were used to improve Vangemert, a PHOSITA would similarly strive to minimize latencies by routing the interrupt signal directly to the transmitting device, as disclosed by Copeland." (Petition, 31).

The Petitioner's proffered motivation to combine "is incorrect because Copeland's teachings do not minimize latencies over Vangemert; rather, Copeland's teachings increase latencies." (Ex 2002, 110). Specifically, in the system taught by Copeland, "data flow control is activated when the FIFO buffer is forty percent full Ex. (1006, 5:39-40)," and "if the buffer is not emptied then, after a predetermined count, the DTR and/or RTS lines are de-asserted, thereby stopping the flow of data from the remote transmitter until the buffer has been emptied." (Ex. 1006, 7:23-26). As explained by Terry Lee, stopping the flow of data (as described in Copeland) "has a negative effect on serial link latency and performance." (Ex. 2002, 119)

In addition, Copeland states that “The present invention therefore automatically signals the remote transmitter to stop sending when the FIFO buffer fills to a certain point and to resume sending once the FIFO buffer has been completely emptied” (Ex. 1006, 3:3-6). Accordingly, a POSITA would understand that “once a buffer reaches its certain fill point, the data transmission must be suspended until the buffer is completely emptied” and therefore “[t]he transmission latency is dominated by the buffer empty time.” (Ex. 2002, 120).

A POSITA would understand that “Large fill points will result in longer latencies, and small fill points will result in inefficient use of the buffer and higher costs.” (Ex. 2002, 120).

Accordingly, combining Vangemert and Copeland would be contradictory and counterproductive. Vangemert’s solution already addresses and eliminates the issue of receiver buffer overflow in data communication. Therefore, adding Copeland’s flow control signal, which is designed to prevent such overflow, would be redundant. Moreover, even if these two methods were combined, incorporating Copeland’s flow control would lead to increased latencies in data transmission, contradicting the efficiency sought in the Petitioner’s proposal. Consequently, the combination of these two approaches does not align logically or functionally. (Ex. 2002, 120).

3. The Same Rational Preferred In The Petition For Combining Vangemert and Copeland Was Rejected Based On Cumulative References During Prosecution

Vangemert and Copeland are cumulative of the prior art applied by the Office during the prosecution of the '454 Patent. In the second office action, the Examiner cited U.S. Patent 5,613,141, "Szatkowski" (Ex. 2005) in view of U.S. Patent 6,192,422, "Daines" (Ex. 2006). (Ex. 1002, 182-186) Like the references relied on in this IPR, the Examiner asserted that it would have been obvious to combine Szatkowski (which disclosed a "flow control" mechanism that essentially prevented buffer overflow) with Daines (which disclosed a control mechanism responsive to the amount of data in the buffer crossing a threshold). (Ex. 2002, 90). In this regard, the Office Action stated:

Szathkowski discloses all the limitations as the above but does not explicitly disclose wherein the ASIC is configured to determine whether an amount of data stored in the first FIFO register equals or exceeds a fill amount associated with a storage capacity of the first FIFO register. However, Daines discloses this. (col.4, lines 4-17, i.e., a flow control mechanism comprising level indicators for the input buffers for indicating the amount of data stored in a buffer and a flow control device for monitoring the level indicators to determine if the amount of data in an input buffer crosses a first threshold).

It would have been obvious to an ordinary person skilled in the art at the time of the invention was made to incorporate the teachings of Daines with the teaching of Szathkowski to have control mechanism to determine the level indicators for the buffers for indicating the amount of data stored for comparison the threshold not to exceed would have been obvious because it would enhance the

system of Szatkowski to increase more functionality to prevent overloaded data in system. (Ex. 1002, at 185-186). (emphasis added).

In response, the Applicant explained that it would not have been obvious to combine the references because, *inter alia*, because the modification would have decreased (rather than increased) the ability of Szatkowski to prevent overflow:

... The rejection proposes modification in view of Daines “to have the control mechanism ... to increase more functionality to prevent overloaded data in system” (pages 5-6). Applicants traverse.

Szatkowski teaches a “flow control” mechanism, which prevents buffer overflow. For example:

The link has a simple protocol. Each node may transmit a packet on its outbound link subject to pacing responses and acknowledgements received from the remote node on its inbound link. (column 4, line 14 et seq.)

Thus, Szatkowski teaches a “flow control” mechanism that prevents buffer overflow. Szatkowski’s use of an acknowledgement-based protocol may eliminate most or all occurrences of buffer overflow, or “near” overflow. For example, Szatkowski teaches waiting on an acknowledgement from a receiver that the receiver has processed a message and is ready to receive another message before sending a subsequent message. Such a protocol may eliminate most or all occurrences of buffer overflow, or “near” overflow at the receiver. ...

... the acknowledgement-based protocol of Szatkowski may eliminate most or all occurrences of buffer overflow, or “near” overflow, rendering unmodified Szatkowski superior to Daines in terms of flow control. Thus, the proposed modification in view of Daines may actually be detrimental to Szatkowski, e.g., by eliminating the advantageous acknowledgement-based protocol of unmodified Szatkowski. (Ex. 1002, at 225-227)(emphasis added).

After the Applicant submitted its response to the second office action, the Applicant was allowed in the next office action. (Ex. 1002, at 266-270). The Petition fails to demonstrate how the Examiner erred in evaluating the combination of Szatkowski and Daines (which is cumulative of the references relied on in these proceedings), or present additional evidence that warrants reconsideration of the evaluation made during prosecution. *Cf., Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469 (PTAB Feb. 13, 2020) (Paper 6) (precedential).

4. The Combination of Vangemert and Copeland Would Have Been Illogical To A POSITA

The Federal Circuit observes that “[t]he degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference’s disclosure is unlikely to be productive of the result sought by the applicant.” *Arctic Cat Inc. v. Bombardier Rec. Prods.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017). As Terry Lee explains, “[i]t is illogical, if not nonsensical, to combine Vangemert with Copeland because Vangemert doesn’t allow buffer overflow to occur, so adding the flow control mechanism of Copeland to respond to pending overflow would have no purpose. “ (Ex 2002, 89).

Terry Lee further explains that “[e]ven if a POSITA were motivated to make the illogical combination of Vangemert and Copeland, the out of band RS-232 signals taught in Copeland are fundamentally incompatible with the addressable data frames taught in Vangemert.” (Ex. 2002, 91). For example, Copeland describes the use of the DTR (Data Terminal Ready) or the RTS (Request To Send) signals to signal the transmitter. A POSITA would understand that The DTR signal, sent from the data terminal equipment (DTE) to the data communication equipment (DCE), indicates the operational readiness of the DTE (like a computer or modem) for communication. When the DTE is ready, it sets the DTR to a high voltage, and a low voltage signifies it’s not ready or off, facilitating the handshaking process with the Data Set Ready (DSR) signal. Similarly, the RTS signal, used by the DTE to manage data flow, is activated when it has data to send, prompting the DCE to prepare to receive data. This is acknowledged by the DCE’s Clear To Send (CTS) signal, ensuring synchronized data transmission and preventing data loss. (Ex 2002, 91-92). Accordingly, a POSITA would understand that “DTE, DCE, CTS, and RTS are asynchronous level sensitive signals which indicate the status of the equipment based on the voltage level. Level sensitive signals differ from a serial bitstream where the symbol on the line can change sequentially with each symbol time.” (Ex 2002, 96).

In contrast, Vangemert describes a low latency algorithm for buffer credit calculation for an I/O bus that incorporates a higher-level protocol, SCSI (Small Computer System Interface), transmitted using the Fibre Channel protocol. Developed in the early 1980s, SCSI is a set of standards for connecting and transferring data between computers and peripheral devices like hard drives, printers, and scanners. Its flexibility and high performance have made it a popular choice. Unlike simpler protocols such as RS-232, SCSI supports multiple devices in a daisy-chain or bus configuration, allowing the connection of several devices to a single SCSI port. (Ex 2002, 97).

As explained by Terry Lee, a POSITA would have appreciated that it would not have been possible to transmit the signaling (e.g., +3 to +15 volts) taught with regard to Copeland's CTS and DTR signal over the higher level I/O bus, such as Fibre Channel protocol or SCSI, that transmits addressable data frames as taught in Vangemert (Ex 2002, 101).

Therefore, a POSITA would not have been motivated to combine Vangemert and Copeland because the references each respectively teach paths that diverge away from the proposed combination, and even if the proposed combination were attempted, the proposed combination would not achieve Vangemert's intended

purpose of providing a low “a low latency algorithm for buffer credit calculation” for use with the Fibre Channel protocol. (Ex. 1005, 1:65-2:1)

B. The Petition Fails To Demonstrate That Vangemert and Copeland Teach Transmitting The Flow Control Signal Through The Serial Link And Connector Without Passing The Flow Control Signal Through The Second Buffer

The last element of claim 1 recites in part:

...wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.

Thus, the recited “flow control signal” must both (i) pass through the serial link, and (ii) not pass through the second buffer. In attempting to map Vangemert to the claimed “flow control signal,” the Petition appears to rely on two different signals from Vangemert – i.e., a buffer credit signal and buffer control words. As described below, neither of these signals from Vangemert meets both of the requirements of the “flow control signal” recited in the claim language. Specifically, Vangemert’s buffer credit signal fails to meet the requirement of the “flow control signal” being transmitted “through the serial link.” In addition, Vangemert’s buffer control words fail to meet the requirement that the “flow control signal” not pass through the second buffer. Simply put, since the relied on reference fails to disclose a “flow control signal” that both (i) passes through the serial link, and (ii) does not

pass through the second buffer, the Petition has failed to show that all of the claim elements are met.

1. Vangemert's Buffer Credit Signal And Buffer Credit Control Words Are Different Signals

Vangemert makes a clear distinction between the buffer credit signal and buffer credit control words. Ex. 2002, 106. Vangemert explains (and shows in Figure 5) that the buffer credit signal is generated by comparator 502 in the buffer credit manager. Ex. 2002, 102. For example, Vangemert explains that “[t]he buffer credit manager iteratively determines the additional committed buffer space (i.e., the space committed but not yet occupied by receive data) by counting the number of receive and transmit flags, and generates the credit signal using a comparator which compares the sum of additional committed buffer space and the maximum frame size to the available receive buffer storage capacity and asserts the credit signal if the available buffer space is greater than or equal to the sum of the maximum frame size and the additional committed buffer space.” (Ex. 1005, 2:19-29)

By contrast, Vangemert explains that the buffer credit control words are generated by transmit controller 416 in transmit buffer 410 (which the Petition maps to the “second buffer.”) For example, Vangemert explains that “[u]sing control words, an initiating node first arbitrates to get control of the loop, then notifies a responding node of its desire to transmit data frames.” (Ex. 1005, 3:10-13)

Vangemert further explains that the “Transmit controller 416 creates or updates exchange information in exchange tables 416 in response to commands and data from the node’s i/o bus, generates control words and data frames in transmit buffer 410, and forwards them to encoder 402.” (Ex. 1005, 3:57-61, Ex. 2002, 102) Simply put, the fact that the buffer credit signal and buffer credit control words are generated by different components in Vangemert indicates that the signals are different.

Vangemert includes further disclosures confirming that the buffer credit signal and buffer credit control words are different signals. For example, Vangemert states that “when receive controller 406 receives a control word³ indicating that a remote node wishes to transmit data, the buffer credit manager 418 is enabled, and the transmit controller 412 begins transmitting buffer credit control words in response to a credit signal from buffer credit manager 418.” (Ex. 1005, 4:11-16, Ex. 2002, 102). The fact that the buffer credit control words are transmitted in response to a credit signal further underscores that the credit words and credit signals are different.

³ As explained by Terry Lee, “A POSITA would understand that the “credit control word” is a specific type of the control words described in Vangemert and transmitted by the Transmit controller 416 via the transmit buffer 410.” (Ex. 1005, 4:11-16, Ex. 2002, 102).

2. Vangemert's Buffer Credit Control Words Are Stored In And Pass Through The Second Buffer

The Petitioner erroneously alleges that “Vangemert does not disclose or suggest that the ... buffer credit control words are ever stored in or passed through the transmit buffer 410 (second buffer).” (Petition, 31). Vangemert says the opposite: “A transmit controller 412 retrieves control words and data frames from transmit buffer 410 and forwards them to encoder 402.” (Ex. 1005, 3:49-52) Vangemert similarly states: “Transmit controller 416 creates or updates exchange information in exchange tables 416 in response to commands and data from the node's i/o bus, generates control words and data frames in transmit buffer 410, and forwards them to encoder 402”. (Ex. 1005, 3:57-61). Furthermore, “Vangemert clearly explains that the transmit controller transmits credit control words to devices connected to the I/O bus via the transmit buffer (410) in response to the internal credit control signal generated by the comparator (502).” (Ex. 1005, 4:11-16, Ex. 2002, 103). Accordingly, Vangemert teaches that the control words pass through the transmit buffer 410.⁴

⁴ A POSITA would understand that Vangemert's transmit buffer 410 is simply a memory which could not on its own originate control words. In interpreting Vangemert's disclosure that transmit controller 416 generates control words "in transmit buffer 410," a POSITA would therefore understand that transmit controller 416 is generating control words that are input to transmit buffer 410 before being forwarded to encoder 402. (Ex. 2002, 105) Nonetheless, to the extent that the Board

3. There Is No Evidence That Vangemert's Buffer Credit Control Signal Is Transmitted Through The Serial Link

Vangemert does not disclose the internal credit control signal being transmitted over the I/O bus (mapped to the serial link). Ex. 2002, 107. In fact, sending such a control signal over the I/O bus, as taught in Vangemert, is not feasible because Vangemert's I/O bus uses a higher-level protocol like SCSI, which does not support this kind of signal transmission. This implies a fundamental limitation in the way the I/O bus in Vangemert's teaching can handle certain types of control signals. (Ex. 2002, 102).

For example, Vangemert's approach to managing credit control words in a transmit buffer is illustrated in Figures 3 and 4 of Vangemert's work. Specifically, the figures show the distinction Vangemert makes between internal buffer credit signals and buffer credit control words. Specifically, when the buffer credit manager

interprets the disclosure in Vengemert as teaching that the control words somehow originate from buffer 410, such an interpretation would still fail to meet the claim language prohibiting the control words (flow control signal) from passing through transmit buffer 410 (mapped to the second buffer). Even if the control words somehow originated within transmit buffer 410, the control words would still need to pass through at least some part of transmit buffer 410 in order for transmit buffer 410 to be able to output the control words to the encoder 402. By passing through at least some internal portion of transmit buffer 410, the control words pass through the second buffer. Nothing in the specification or prosecution history indicates that the flow control signal would need to traverse the entirety of the second buffer (from input to output) in order to meet the claim language.

is enabled, the transmit controller starts transmitting buffer credit control words in response to a credit signal from the buffer credit manager. Furthermore, Vangemert states that both data frames and control words are transported on the transmit channel, moving from the source (transmitter) to the destination (receiver). The fabric switch is responsible for transporting these data frames and control words, and the receive controller stores them in the receive buffer. As a result, “Vangemert discusses no other payloads on the transmit channel besides data frames and control words.” (Ex. 2002, 106).

Accordingly, a POSITA would understand that in Vangemert’s system, the buffer credit control words (and not credit control signal) serve as the flow control signals for transport on the serial link. It is explicitly stated that the transmit controller generates control words in the transmit buffer. Additionally, it is reiterated that the transmit controller retrieves these control words from the buffer and forwards them to the encoder for transmission on the transmit channel. From this, a POSITA would clearly comprehend that Vangemert’s credit control signal is not transmitted over the I/O bus (serial link). (Ex. 2002, 107).

4. Copeland Does Not Cure The Deficiencies In Vangemert With Respect To The Flow Control Signal

The suggested addition of Copeland does not cure the shortcomings of Vangemert. The Petition alleges that “In Copeland, “data flow control is activated

when the FIFO buffer is forty percent full.” The data flow control is executed by sending a low Request to Send (“RTS”) signal over the connector 20 to instruct a remote device to stop sending data upon the FIFO buffer reaching the fill amount” and “the RTS signal is a flow control signal because it is generated to instruct a remote device to stop sending data.” (Petition, 28-29). However, “the Petition seems to confuse the serial link with the connector 20.” (Ex. 2002, 117).

Copeland describes that “Serial port connectors 20 and 21 preferably define an EIA RS-232-D serial interface. UARTs 14 and 15 convert data between a serial data format on connectors 20 and 21 and a parallel data format on bus 40.” (Ex. 1006, 4:33-37, Ex. 2002, 115). A POSITA would recognize that RS-232 is a common specification for serial interfaces and that the 16550A UART is commonly used for serialization and deserialization in RS-232 applications. This information highlights the technical specifications and common practices in serial communication as described by Copeland. (Ex. 2002, 115).

As explained by Terry Lee, a “ POSITA would also know that RTS is a parallel out-of-band handshake signal used in RS-232,” which is transmitted “on a separate out-of-band connector pin from the serial data signals, RXD or TXD.” (Ex. 2002, 155). Accordingly, a POSITA would appreciate that the control signal for Copeland

is not transmitted through the serial link as required by the Challenged claims. (Ex. 2002, 116).

Therefore, neither Copeland nor Vangemert teaches a module is “configured to transmit the flow control signal through the serial link and connector without passing the flow control signal through the second buffer,” as recited in the challenged claims.

C. The Proposed Combination of Dobson and Copeland Fails To Teach All Of The Limitations Of The Challenged Claims

1. Dobson Fails To Disclose A Flow Control Signal Transmitted Through The Serial Link

The Petition attempts to map Dobson’s IRQ signal to the flow control signal recited in the claims. As explained below, that mapping fails because there is no evidence that Dobson’s IRQ signal is transmitted through the serial link.⁵

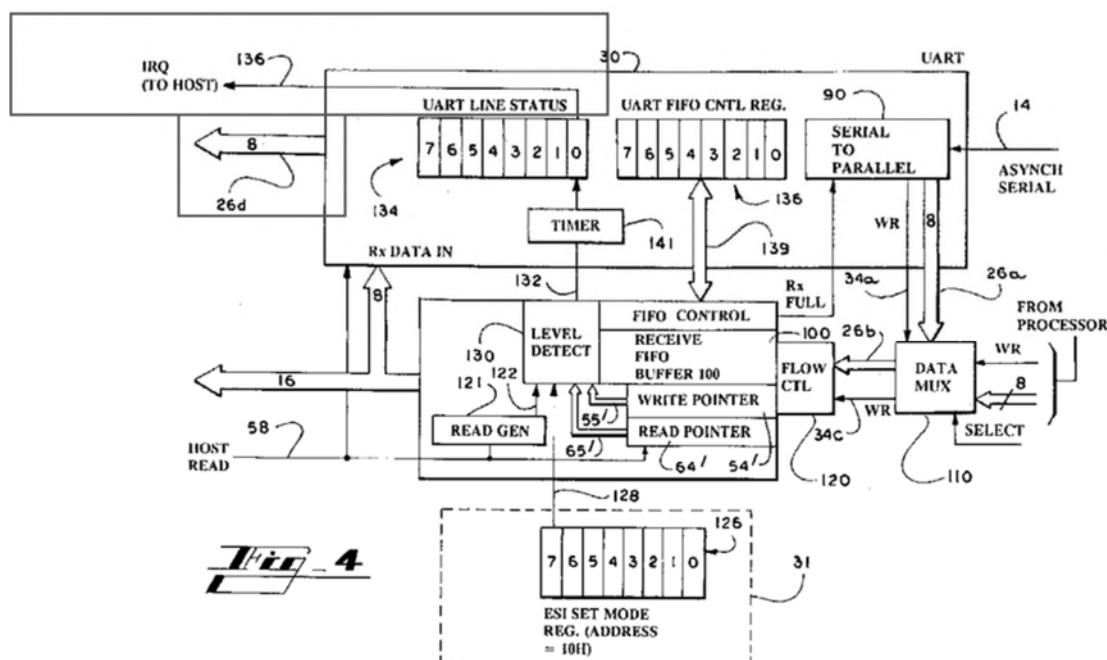
Dobson describes a system where a “level detect circuit 130 is provided with the write address bus 55’ and read address bus 65’.” (Ex. 1007, 8:32-33. Ex. 2002, 126). In addition, Dobson explains that the interrupt request (IRQ) generated in accordance with level detect circuit 130 is transmitted over line 136:

The level detect circuit 130 outputs receive data ready signal on line 132 to bit 0 in the UART line status register 134. Bit 0 in the UART line status register 134 is passed to the host computer 8 on line 136 as an interrupt request. The host computer 8 responds to the interrupt request on line 136 by

⁵ The Petition maps the claimed serial link to transmit line 16 in Dobson. Pet., at 59.

reading data from the receive HFO buffer 100, as set forth below. (Ex. 1007, 8:30-39 (emphasis added), Ex. 2002, 126)

In contrast to the IRQ signal sent over line 136, Dobson explains that data from the FIFO buffer is transmitted to the host personal computer 8 via receive databus 26d. For example, Dobson explains that “[r]eceived data is passed from the receive FIFO buffer 100 to the host personal computer 8 via the receive data bus 26d, bus interface circuit 20, and data bus 12.” (Ex. 1007, 7:61-64) Dobson’s system, where the Interrupt (labeled as IRQ) is transmitted to the computer over line 136 (red) and data is received over a different 8-bit wide parallel data bus 26d (blue), is graphically depicted in Figure 4 (annotated below).



Accordingly, a POSITA would appreciate that “Dobson teaches using a different line that is not part of the serial link to send an IRQ to the host computer.” (Ex 2002, 129). Therefore, Dobson does not teach “a module configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer,” as recited in the Challenged Claims.

In addition, a POSITA would appreciate that it is logical to send an IRQ using an out of band communication channel because “an IRQ (Interrupt Request) is a hardware signal sent to the processor that temporarily stops a running program and allows a special program, an interrupt handler or interrupt service routine, to run instead.” (Ex, 2002, 130). In some examples, the interrupt handler or service routine is run in response to events from hardware devices like keyboards and disk drives. When a device requires CPU attention, it issues an IRQ signal, causing the CPU to suspend its current tasks, save its state, and execute the specific interrupt handler. This immediate response is essential for handling time-sensitive tasks. Once the handler completes, the CPU resumes its previous activities. In the 1990s, managing IRQ lines was challenging due to the limited number of IRQ lines, often leading to conflicts when multiple devices attempted to use the same line.” (Ex, 2002, 131-132). Given the purpose of the IRQ, it makes perfect sense in the context of the state of the art in 1998 that Dobson teaches to use a separate line (136) that is discrete

from the serial bus (14) or the parallel received data bus (26d) to alert the computer. (Ex, 2002, 133).

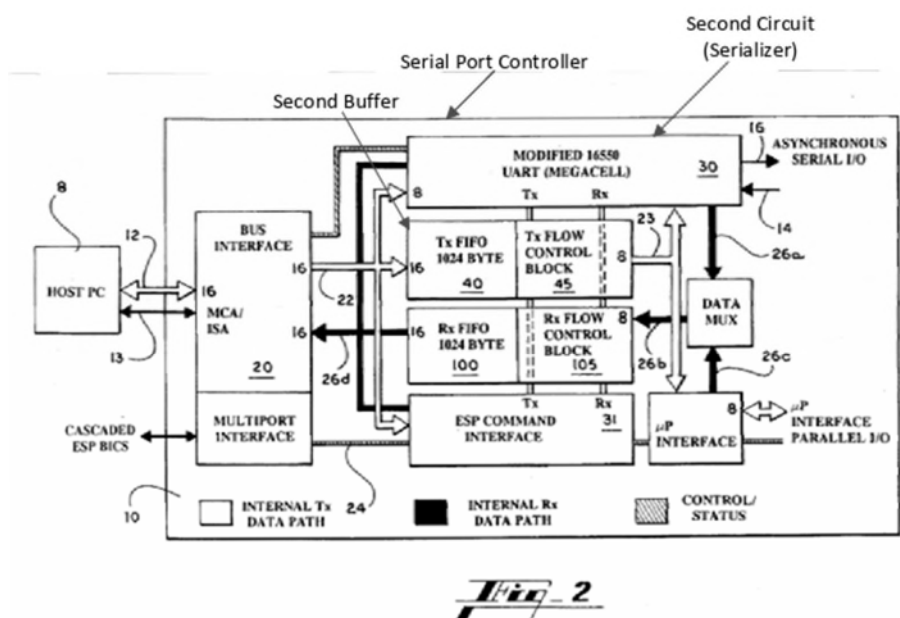
Therefore, Dobson does not expressly or inherently teach a module configured to transmit the IRQ (mapped to the claimed flow control signal) through the serial link (mapped to line 16 in Dobson), as recited in the Challenged Claims.

The additional teachings of Copeland do not cure the shortcomings of Dobson. Instead, as discussed above in Section VII(A)(1)(b), Copeland's flow control signal is an out-of-band parallel signal transmitted through a separate signal line and not through the serial link and the connector. As a result, Copeland, alone or in combination with Dobson, fails to teach or suggest "a module configured to transmit the flow control signal through the serial link and the connector," as recited in the Challenged Claims.

In addition, if Dobson were to be combined with Copeland as proposed by the Petitioner, the out of band signaling taught in Copeland (e.g., CTS and DTR signal) would be sent over the separate IRQ line and not through the serial link. Alternatively, if Copeland were combined with Dobson, the interrupt taught in Dobson would be transmitted over the CTS and/or DTR lines taught in Copeland and not through the serial link as recited in the Challenged Claims. (Ex. 2002, 135).

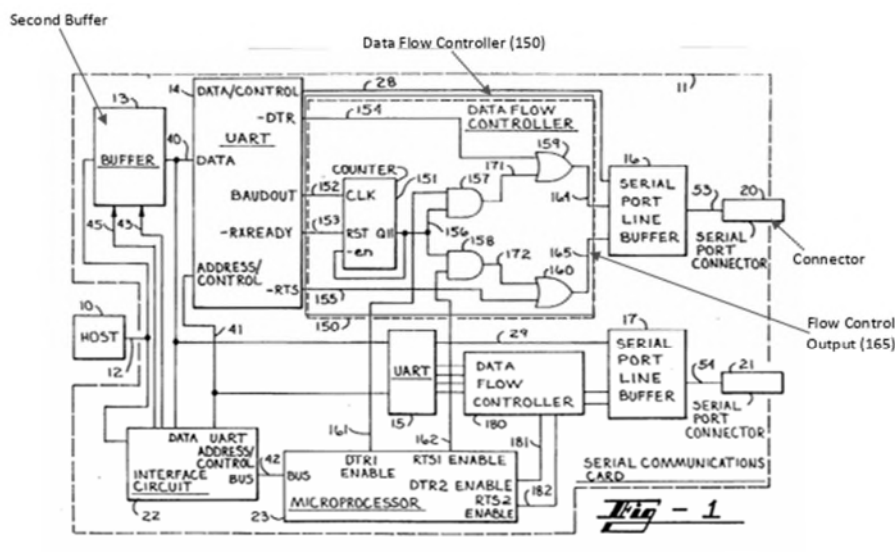
2. Petitioner's Mapping Of The "Second Buffer" Is Inconsistent And, Therefore, Does Not Show How The Proposed Combination Of Dobson And Copeland Teaches Every Element Of The Challenged Claims

The Petitioner maps the "second buffer" to TX FiFO Buffer (40) of Dobson, as shown in the annotation of Dobson's Figure 2 (reproduced below). (Petition, 58)



Dobson FIG. 2 (Annotated)

However, later in the Petition, the Petitioner changes the proposed mapping of the "second buffer" to Copeland's Buffer 13, as illustrated in Petitioner's annotated version of Copeland's Figure 1 (reproduced below).



Copeland FIG. 1 (Annotated)

The Petition states that “Copeland’s buffer 13 equates to the claimed “second buffer” because buffer 13 controls data flow to and from the host, including to UART 14, for converting parallel data to serial data on line 40.” (Petition, 67). However, the Petitioner and the Petitioner’s expert are completely silent as to how Copeland’s buffer 13 is the equivalent of Dobson’s TX FiFO Buffer (40).

In fact, Copeland expressly teaches that “Host data buffer 13 is a bidirectional buffer which controls the flow of data to and from host 10.” (Ex. 1006, 4:7-9) By contrast, Dobson’s buffer 40 is a transmit (TX) buffer and, therefore, unidirectional. Petitioner has offered no explanation for why a POSITA would equate Dobson’s unidirectional buffer (40) with Copeland’s bidirectional buffer. As a result, “the

only reason for a POSITA to equate the two buffers would be to use the ‘454 Patent as a blueprint.” (Ex. 2002, 140).

Therefore, the Petitioner has failed to meet their burden of showing how the proposed combination of Copeland and Dobson teaches “a module that “is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer,” as recited in the Challenged Claims.

VIII. CONCLUSION

The Board should find that the Petition has failed to demonstrate the unpatentability of any of the Challenged Claims.

Respectfully submitted,

Dated: January 10, 2024

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Patent Owner Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 8427 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Response.

Respectfully submitted,

Dated: January 10, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing **PATENT OWNER'S RESPONSE** was served via email (as consented to by counsel) on January 10, 2024 to lead and backup counsel of record for Petitioners as follows:

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