Terry R. Lee

Education :

2004 **MBA, University of Washington, Seattle, Executive MBA**
Honors Graduate, First in Class

1985 **MSEE, University of Southern California**
Emphasis: Computer Hardware and Integrated Circuits

1983 **BSEE, University of Missouri - Columbia**
Cum Laude

Work Experience:

2016 - present **IdaTech Consulting, LLC Boise, ID**

President and Subject Matter Expert

Subject Matter Expert in the areas of memory, semiconductors, and small electronic systems. Provide expertise in support of multiple intellectual property clients. Activities include research, reverse engineering, patent assessment, claim charting, expert witness, and litigation support.

1989 – 2015 **Micron Technology, Inc. Boise, ID**

Senior Director, Managed NAND Development

Led development team for eMMC and UFS Managed NAND products for Wireless and Automotive applications. Developed and released products that supported a 3x increase in Managed NAND revenue in one year. Released the company's first Managed NAND products based on internally developed firmware. Responsibilities included system architecture, firmware development, product validation, system validation and product engineering. Team size varied from 130 - 200 team members in the U.S., China, Italy, and Singapore spanning multiple company reorganizations. Led an overhaul of the product validation strategy to improve product quality and volume.

Engineering Director, Engineering Services

Directed large engineering teams that supported memory module and SSD PCB design, signal integrity for all products, competitor analysis, custom engineering tester development, NAND and DRAM component characterization, and Managed NAND characterization. I directed approximately 180 team members in U.S. and Italy. Supported a two-fold increase in products and product volume without significantly increasing team size.

Director, Memory Systems and Packaging

Managed 120 people in two geographic locations responsible for memory module product development, mixed signal ASIC and system development, and signal integrity for all NAND and DRAM products. Responsible for packaging technology and strategy and for the packaging roadmap for all memory products. Redesigned business processes across the company for:

- Module development and new product introduction
- Packaging technology development
- New product introduction for multi-chip package (MCP) products

Served the industry as an IEEE International Solid State Circuits Conference Memory Subcommittee Member in 2005 and 2006.

Executive Director, Advanced Technology and Strategic Marketing
Responsible for Strategic Marketing and Advanced Technology Development for memory products for a $3B business. Strategic Marketing functions include Segment Marketing, Product Definition, Outbound Marketing, and Applications Engineering. Technology development functions include ASIC and FPGA development, analog/mixed signal I.C. design, system design, PCB design, and research and development in signal integrity. Manager of approximately 130 employees in two geographic locations. Responsibilities also included consulting on technical and business issues for the legal department, and involvement in strategic business relationships and acquisitions, and establishing competitive strategies for the company. Presented technical presentations and keynote addresses at a variety of industry conferences.

Technical Director, Advanced Systems Research Lab
Led a team of 6 engineers and technicians involved in systems research and development for establishing electrical signaling schemes for future memory products and subsystems. I also cross-trained a group of RF engineers to solve new signal integrity problems to be encountered in future systems.

Re-engineered the following processes:

- Co-developed a frequency domain approach to circuit simulation that improved accuracy while reducing the CPU utilization by a factor of 10.
- Developed an automation technique for converting rapidly converting raw simulation results into useful quantitative data and graphs. This process converted a one-week task to less than one minute.

Strategic Product Development Engineer
Responsible for product definition and standardization of future DRAM products. This effort involved system design, applications engineering, circuit simulation, and representing the company in industry standardization committees.

Led the following industry activities:

- SLDRAM Consortium – Technical Director
- Joint Electronic Device Engineering Council (JEDEC) Task Group Leader
- Advanced DRAM Technology Consortium – Technical Director

I played a key role in the standardization of DDR and DDR2 memory technologies.

Senior Design Engineer
Responsible for CMOS integrated circuit design for memory products including 1Mb Video RAM and 4Mb DRAM.

1983 – 1989 **Hughes Aircraft Company, Radar Systems Group, El Segundo, CA**
Technical Head
Technical Supervisor
Member of Technical Staff

Led a group of 20 engineers and technicians responsible for system design and integrated circuit design for radar systems and electronic countermeasures. Project Manager and System Lead for state-of-the-art Digital RF Memory (DRFM) subsystem for the Air Force.

Led a group of 6 engineers involved in RF bipolar integrated circuit design for radar systems.

Designed multiple RF digital integrated circuits used in data acquisition systems.

1980 – 1983 **Texas Instruments, Inc., Consumer Products Group, Lubbock, TX**
Engineering Co-op Student
Custom CMOS integrated circuit design. Performed SPICE simulations, layout, and test of digital integrated circuits used in professional calculators.

Other Skills and Achievements:

- Inventor of over 130 U.S. patents