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☐ a) The term of this patent, subsequent to _____ (date) has been disclaimed.	Sumati Lefkowitz 2/15/00 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 2-25-00	
☒ b) The term of this patent shall not extend beyond the expiration date of U.S. Patent No. <u>pending</u>	AYAZ R. SHEIKH SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2700 (Primary Examiner) 4/21/00 (Date)			ISSUE FEE Amount Due \$ 605.00 Date Paid 4-7-00	
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(Rev. 10/97)Formal Drawings (shd) set

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ADDRESS	THOMAS L ADAMS
	10 PARK PLACE
	MORRISTOWN NJ 07960

TITLE	~~Serially Linked~~ Bus Bridge for Expanding Access over a First Bus
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In re Application of: Frank Ahern

THE COMMISSIONER OF PATENTS AND TRADEMARKS
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Sir:

Transmitted herewith for filing is the application of

Inventor: Frank Ahern

For: LINKED BRIDGE

Enclosed are:

Assignment, specification, and 4 sheets of drawings.

A verified statement to establish small entity status under 37 CFR 1.9 and 37
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THOMAS L. ADAMS
Reg No. 27,300

LINKED BRIDGEBACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to data processing systems, and more particularly, to bridge systems including mechanisms for transferring information between buses.

10 2. Description of Related Art

Computers can use buses to transfer data between a host processor and various devices, such as memory devices and input/output devices. As used herein an "input/output" device is a device that either generates an input or receives an output (or does both). Thus "input/output" is used in the disjunctive. These buses may be arranged in a hierarchy with the host processor connected to a high level bus reserved for exchanging the data most urgently needed by the processor. Lower level buses may connect to devices having a lower priority.

Other reasons exist for providing separate buses. Placing an excessive number of devices on one bus produces high loading. Such loading makes a bus difficult to drive because of the power needed and the delays caused by signaling so many devices. Also, some devices on a bus may periodically act as a master and request control over a bus in order to communicate with a slave device. By segregating some devices on a separate bus, master devices can communicate with other devices on the lower level bus without tying up the bus used by the host processor or other masters.

The PCI bus standard is specified by the PCI Special Interest Group of Hillsboro, Oregon. The PCI bus features a 32-bit wide, multiplexed address-data (AD) bus portion, and can be expanded to a 64-bit wide AD bus portion.

Maintaining a high data throughput rate (e.g., a 33 MHZ clock rate) on the PCI bus leads to a fixed limitation on the number of electrical AC and DC loads on the bus. Speed considerations also limit the physical length of the bus and the capacitance that can be placed on the bus by the loads, while future PCI bus rates (e.g., 66 MHZ) will exacerbate the electrical load and capacitance concerns. Failure to observe these load restrictions can cause propagation delays and unsynchronized operation between bus devices.

To circumvent these loading restrictions, the PCI bus standard specifies a bridge to allow a primary PCI bus to communicate with a secondary PCI bus through such a bridge. Additional loads may be placed on the secondary bus without increasing the loading on the primary bus. For bridges of various types see U.S. Patents 5,548,730 and 5,694,556.

The PCI bridge observes a hierarchy that allows an initiator or bus master on either bus to complete a transaction with a target on the other bus. As used herein, hierarchy refers to a system for which the concept of a higher or lower level has meaning. For example, a PCI bus system is hierarchical on several scores. An ordering of levels is observed in that a high level host processor normally communicates from a higher level bus through a bridge to a lower level bus. An ordering of levels is also observed in that buses at equal levels do not communicate directly but through bridges interconnected by a higher level bus. Also, an ordering of levels is observed in that data is filtered by their addresses before being allowed to pass through a bridge, based on the levels involved. Other hierarchical systems exist that may observe an ordering of levels by using one or more of the foregoing concepts, or by using different concepts.

Some personal computers have slots for add-on cards, which allow the card to connect to a peripheral bus in the computer. Because a user often needs additional slots, expansion cards have been designed that will connect between the peripheral bus and an external unit that offers additional slots for

SL add-on cards. For systems for expanding a bus, see U.S. Patents 5,006,981; 5,191,657; and 5,335,329. See also U.S. Patent 5,524,252.

For portable computers, special considerations arise when the user wishes to connect additional peripheral devices. Often a user will bring a portable computer to a desktop and connect through a docking station or port replicator to a keyboard, monitor, printer or the like. A user may also wish to connect to a network through a network interface card in the docking station. At times, a user may need additional devices such as hard drives or CD-ROM drives. While technically possible to a limited extent, extending a bus from a portable computer through a cable is difficult because of the large number of wires needed and because of latencies caused by a cable of any significant length.

SL In U.S. Patent 5,696,949 a host chassis has a PCI to PCI bridge that connects through a cabled bus to another PCI to PCI bridge in an expansion chassis. This system is relatively complicated since two independent bridges communicate over a cabled bus. This cabled bus includes essentially all of the lines normally found in a PCI bus. This approach employs a delay technique to deal with clock latencies associated with the cabled bus. A clock signal generated on the expansion side of the cabled bus: (a) is sent across the cabled bus, but experiences a delay commensurate with the cable length; and (b) is delayed an equivalent amount on the expansion side of the cabled bus by a delay line there, before being used on the expansion side. Such a design complicates the system and limits it to a tuned cable of a pre-designed length, making it difficult to accommodate work spaces with various physical layouts.

SL U.S. Patent 5,590,377 shows a primary PCI bus in a portable computer being connected to a PCI to PCI bridge in a docking station. When docked, the primary and secondary buses are physically very close. A cable is not used to allow separation between the docking station and the portable computer. With

this arrangement, there is no interface circuitry between the primary PCI bus
SL and the docking station. See also U.S. Patent 5,724,529.

SL U.S. Patent 5,540,597 suggests avoiding additional PCMCIA connectors
5 when connecting a peripheral device to a PC card slot in a portable computer,
but does not otherwise disclose any relevant bridging techniques.

SL U.S. Patents 4,882,702 and show a programmable controller for
controlling industrial machines and processes. The system exchanges data
10 serially with a variety of input/output modules. One of these modules may be
replaced with an expansion module that can serially communicate with several
groups of additional input/output modules. This system is not bridge-like in that
the manner of communicating with the expansion module is different than the
manner of communicating with the input/output modules. For the expansion
15 module the system changes to a block transfer mode where a group of status
bytes are transferred for all the expansion devices. This system is also limited
to input/output transactions and does not support a variety of addressable
SL memory transactions. See also U.S. Patent 4,413,319; and 4,504,927.

20 SL In U.S. Patent 5,572,525 another bus designed for instrumentation (IEEE
488 General Purpose Instrumentation Bus) connects to an extender that breaks
the bus information into packets that are sent serially through a transmission
cable to another extender. This other extender reconstructs the serial packets
into parallel data that is applied to a second instrumentation bus. This extender
25 is an intelligent system operating through a message interpretation layer and
several other layers before reaching the parallel to serial conversion layer. Thus
this system is unlike a bridge. This system is also limited in the type of
SL transactions that it can perform. See also U.S. Patent 4,959,833.

30 SL U.S. Patent 5,325,491 shows a system for interfacing a local bus to a
cable with a large number of wires for interfacing with remote peripherals. See

SL also U.S. Patents 3,800,097; 4,787,029; 4,961,140; and 5,430,847.

The Small Computer System Interface (SCSI) defines bus standards for a variety of peripheral devices. This SCSI bus is part of an intelligent system that responds to high-level commands. Consequently, SCSI systems require software drivers to enable hardware to communicate to the SCSI bus. This fairly complicated system is quite different from bridges such as bridges as specified under the PCI standard. A variety of other complex techniques and protocols exist for transferring data, including Ethernet, Token Ring, TCP/IP, ISDN, FDDI, HIPPI, ATM, Fibre Channel, etc., but these bear little relation to bridge technology.

SL See also U.S. Patents 4,954,949; 5,038,320; 5,111,423; 5,446,869; 5,495,569; 5,497,498; 5,507,002; 5,517,623; 5,530,895; 5,542,055; 5,555,510; 5,572,688; and 5,611,053.

Accordingly, there is a need for an improved system for transferring information between buses.

SUMMARY OF THE INVENTION

In accordance with the illustrative embodiments demonstrating features and advantages of the present invention, there is provided a bridge accessible by a host processor for expanding access over a first bus to a second bus. The first bus and the second bus are each adapted to separately connect to respective ones of a plurality of bus-compatible devices. Allowable ones of the devices include memory devices and input/output devices. The bridge has a link, together with a first and a second interface means. The first interface means is coupled between the first bus and the link. The second interface means is coupled between the second bus and the link. The first interface means and the second interface means are operable to (a) send bus-related information serially

through the link in a format different from that of the first bus and the second bus, (b) approve an initial exchange between the first bus and the second bus in response to a pending transaction having a characteristic signifying a destination across the bridge, and (c) allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus-compatible devices on the second bus, including memory devices and input/output devices that may be present: (i) using on the first bus substantially the same type of addressing as is used to access devices the first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on the second bus.

In accordance with another aspect of the invention a bridge accessible by a host processor can expand access over a first bus to a second bus. The first bus and the second bus each are adapted to separately connect to respective ones of a plurality of bus-compatible devices. Allowable ones of the devices include memory devices and input/output devices. The bridge has a link, together with a first and a second interface means. The first interface means is coupled between the first bus and the link. The second interface means is coupled between the second bus and the link. The first interface means and the second interface means are operable to (a) send bus-related information serially through the link in a format different from that of the first bus and the second bus, (b) exchange bus-related information between the first bus and the second bus according to a predetermined hierarchy giving the first bus a higher level than the second bus, and (c) allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus-compatible devices on the second bus, including memory devices and input/output devices that may be present: (i) using on the first bus substantially the same type of addressing as is used to access devices the first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on the second bus.

By employing apparatus and methods of the foregoing type, an improved system is achieved for transferring information between buses. In one preferred embodiment, two buses communicate over a duplex link formed with a pair of simplex links, each employing twisted pair or twin axial lines (depending on the desired speed and the anticipated transmission distance). Information from the buses are first loaded onto FIFO (first-in first-out) registers before being serialized into frames for transmission over the link. Received frames are deserialized and loaded into FIFO registers before being placed onto the destination bus. Preferably, interrupts, error signals, and status signals are sent along the link.

In this preferred embodiment, address and data are taken from a bus one transaction at a time, together with four bits that act either as control or byte enable signals. Two or more additional bits may be added to tag each transaction as either: an addressing cycle; acknowledgment of a non-posted write; data burst; end of data burst (or single cycle). If these transactions are posted writes they can be rapidly stored in a FIFO register before being encoded into a number of frames that are sent serially over a link. When pre-fetched reads are allowed, the FIFO register can store pre-fetched data in case the initiator requests it. For single cycle writes or other transactions that must await a response, the bridge can immediately signal the initiator to wait, even before the request is passed to the target.

In a preferred embodiment, one or more of the buses follows the PCI or PCMCIA bus standard (although other bus standards can be used instead). The preferred apparatus then operates as a bridge with a configuration register that is loaded with information specified under the PCI standard. The apparatus can transfer information between buses depending upon whether the pending addresses fall within a range embraced by the configuration registers. This scheme works with devices on the other side of the bridge, which can be given unique base addresses to avoid addressing conflicts.

In one highly preferred embodiment, the apparatus may be formed as two separate application-specific integrated circuits (ASIC) joined by a cable. Preferably, these two integrated circuits have the same structure, but can act in two different modes in response to a control signal applied to one of its pins. Working with hierarchical buses (primary and secondary buses) these integrated circuits will be placed in a mode appropriate for its associated bus. The ASIC associated with the secondary bus preferably has an arbiter that can grant masters control of the secondary bus. This preferred ASIC can also supply a number of ports to support a mouse and keyboard, as well as parallel and serial ports.

When used with a portable computer, one of the ASIC's can be assembled with a connector in a package designed to fit into a PC card slot following the PCMCIA standard. This ASIC can connect through a cable to the other ASIC, which can be located in a docking station. Accordingly, the apparatus can act as a bridge between a CardBus and a PCI bus located in a docking station. Since the preferred ASIC can also provide a port for a mouse and keyboard, this design is especially useful for a docking station. Also, the secondary PCI bus implemented by the ASIC can connect to a video card or to a video processing circuit on the main dock circuit board in order to drive a monitor.

In some embodiments, one ASIC will be mounted in the portable computer by the original equipment manufacturer (OEM). This portable computer will have a special connector dedicated to the cable that connects to the docking station with the mating ASIC. For such embodiments, the existence within the preferred ASIC of ports for various devices can be highly advantageous. An OEM can use this already existing feature of the ASIC and thereby eliminate circuitry that would otherwise have been needed to implement such ports.

BRIEF DESCRIPTION OF THE DRAWINGS

The above brief description as well as other objects, features and advantages of the present invention will be more fully appreciated by reference to the following detailed description of presently preferred but nonetheless illustrative embodiments in accordance with the present invention when taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic block diagram showing a bridge split by a link within the bridge, in accordance with principles of the present invention;

Figure 2 is a schematic block diagram showing a bridge in accordance with principles of the present invention using the link of Figure 1;

Figure 3 is a schematic block diagram showing the bridge of Figure 2 used in a docking system in accordance with principles of the present invention;

Figure 4 is a cross-sectional view of the cable of Figure 3;

Figure 5 is a schematic illustration of the bridge of Figure 3 shown connected to a portable computer and a variety of peripheral devices; and

Figure 6 shows a docking station similar to that of Figure 5 but with the portable computer modified to contain an application-specific integrated circuit designed to support a link to the docking station.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a bridge is shown connecting between a first bus 10 and a second bus 12 (also referred to as primary bus 10 and secondary bus 12). These buses may be PCI or PCMCIA 32-bit buses, although other types of buses are contemplated and the present disclosure is not restricted to any specific type of bus. Buses of this type will normally have address and data lines. In some cases, such as with the PCI bus, address and data are multiplexed onto the same lines. In addition, these buses will have signaling lines for allowing devices on the bus to negotiate transactions. For the PCI standard, these signaling lines will include four lines that are used either for control or byte enabling (C/BE[3:0]). Others signaling lines under the PCI standard exist for gaining control over the bus, for handshaking, and the like (e.g., FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, etc.)

Buses 10 and 12 are shown connecting to a first interface means 14 and second interface means 16, respectively (also referred to as interfaces 14 and 16). Bus information selected for transmission by interfaces 14 and 16 are loaded into registers 18 and 20, respectively. Incoming bus information that interfaces 14 and 16 select for submission to the buses are taken from registers 22 and 24, respectively. In one embodiment, registers 18-24 are each 16 X 38 FIFO registers, although different types of registers having different dimensions may be used in alternate embodiments.

In this embodiment, registers 18-24 are at least 38 bits wide. Thirty six of those bits are reserved for the 4 control bits (C/BE#[3:0]) and the 32 address/data bits (AD[31:0]) used under the PCI bus standard. The remaining two bits can be used to send additional tags for identifying the nature of the transaction associated therewith. Other bits may be needed to fully characterize every contemplated transaction. Transactions can be tagged as: addressing cycle; acknowledgment of a non-posted write; data burst; end of data burst for

single cycle). Thus outgoing write transactions can be tagged as a single cycle transaction or as part of a burst. Outgoing read requests can also be tagged as part of a burst with a sequence of byte enable codes (C/BE) for each successive read cycle of the burst. It will be appreciated that other coding schemes using a different number of bits can be used in other embodiments.

The balance of the structure illustrated in Figure 1 is a link designed to establish duplex communications between interfaces 14 and 16 through registers 18-24. For example, encoder 28 can accept the oldest 38 bits from register 20 and parse it into five bytes (40 bits). The extra two bits of the last byte are encoded to signify the interrupts, status signals and error signals that may be supplied from block 34.

Each of these five bytes is converted into a 10 bit frame that can carry the information of each byte, as well as information useful for regulating the link. For example, these frames can carry comma markers, idle markers, or flow control signals, in a well-known fashion. A transceiver system working with bytes that were encoded into such 10 bit frames is sold commercially by Hewlett Packard as model number HDMP-1636 or -1646. Frames produced by encoder 28 are forwarded through transmitter 44 along simplex link 46 to receiver 48, which supplies the serial information to decoder 30. Likewise, encoder 26 forwards serial information through transmitter 38 along simplex link 40 to receiver 42, which supplies the serial information to decoder 32.

Flow control may be necessary should FIFO registers 22 or 24 be in danger of overflowing. For example, if FIFO register 22 is almost full, it supplies a threshold detect signal 36 to encoder 26, which forwards this information through link 40 to decoder 32. In response, decoder 32 issues a threshold stop signal 50 to encoder 28, which then stops forwarding serial information, thereby preventing an overflow in FIFO register 22. In a similar fashion, a potential overflow in FIFO register 24 causes a threshold detect signal 52 to

flow through encoder 28 and link 46 to cause decoder 30 to issue a threshold stop signal 54, to stop encoder 26 from sending more frames of information. In some embodiments, the system will examine the received information to determine if it contains transmission errors or has been corrupted in some fashion. In such event the system can request a retransmission of the corrupted information and thereby ensure a highly reliable link.

In this embodiment, elements 14, 18, 22, 26, 30, 38 and 48 are part of a single, application specific integrated circuit (ASIC) 56. Elements 16, 20, 24, 28, 32, 42 and 44 are also part of an ASIC 58. As described further hereinafter, first ASIC 56 and second ASIC 58 have an identical structure but can be operated in different modes. It will be appreciated that other embodiments may not use ASIC's but may use instead alternate circuitry, such as a programmable logic device, or the like. As shown herein, ASIC 56 is operating in a mode designed to service primary bus 10, and (for reasons to be described presently) will be sending outputs to block 57. In contrast block 34 of ASIC 58 will receive inputs from block 34.

Encoders 26 and 28 have optional parallel outputs 27 and 29, respectively, for applications requiring such information. Also for such applications, decoders 30 and 32 have parallel inputs 31 and 33, respectively. These optional inputs and outputs may be connected to an external transceiver chip, such as the previously mentioned device offered by Hewlett Packard as model number HDMP-1636 or -1646. These devices will still allow the system to transmit serial information, but by means of an external transceiver chip. This allows the user of the ASIC's 56 and 58 more control over the methods of transmission over the link.

Referring to Figure 2, previously mentioned ASIC's 56 and 58 are shown in further detail. The previously mentioned encoders, decoders, transmitters, receivers, and FIFO registers are combined into blocks 60 and 62, which are

interconnected by a duplex cable formed of previously mentioned simplex links 40 and 46. Previously mentioned interface 14 is shown connected to primary bus 10, which is also connected to a number of bus-compatible devices 64. Similarly, previously mentioned interface 16 is shown connected to secondary bus 12, which is also connected to a number of bus-compatible devices 66. Devices 64 and 66 may be PCI-compliant devices and may operate as memory devices or input/output devices.

Interface 14 is shown connected to a first register means 68, which acts as a configuration register in compliance with the PCI standard. Since this system will act as a bridge, configuration registers 68 will have the information normally associated with a bridge. Also, configuration registers 68 will contain a base register and limit register to indicate a range or predetermined schedule of addresses for devices that can be found on the secondary bus 12. Under the PCI standard, devices on a PCI bus will themselves each have a base register, which allows mapping of the memory space and/or I/O space. Consequently, the base and limit registers in configuration registers 68 can accommodate the mapping that is being performed by individual PCI devices. The information on configuration registers 68 are mirrored on second configuration register 67 (also referred to as a second configuration means). This makes the configuration information readily available to the interfaces on both sides of the link.

In this embodiment, ASIC 58 has an arbiter 70. Arbiters are known devices that accept requests from masters on secondary bus 12 for control of the bus. The arbiter has a fair algorithm that grants the request of one of the contending masters by issuing it a grant signal. In this hierarchical scheme, secondary bus 12 requires bus arbitration, but primary bus 10 will provide its own arbitration. Accordingly, ASIC 56 is placed in a mode where arbiter 72 is disabled. The modes of ASIC's 56 and 58 are set by control signals applied to control pins 74 and 76, respectively. Because of this mode selection, the signal directions associated with blocks 57 and 34 will be reversed.

In this embodiment, ASIC 58 is in a mode that implements a third bus 78. Bus 78 may follow the PCI standard, but is more conveniently implemented in a different standard. Bus 78 connects to a number of devices that act as a port means. For example, devices 80 and 82 can implement PS/2 ports that can connect to either a mouse or a keyboard. Device 84 implements an ECP/EPP parallel port for driving a printer or other device. Device 86 implements a conventional serial port. Devices 80, 82, 84 and 86 are shown with input/output lines 81, 83, 85 and 87, respectively. Devices 80-86 may be addressed on bus 10 as if they were PCI devices on bus 12. Also in this embodiment, a bus 88 is shown in ASIC 56, with the same devices as shown on bus 78 to enable an OEM to implement these ports without the need for separate input/output circuits.

Referring to Figure 3, previously mentioned ASIC 58 is shown in a docking station 130 connected to an oscillator 91 for establishing a remote and internal clock. ASIC 58 has its lines 81 and 83 connected through a connection assembly 90 for connection to a keyboard and mouse, respectively. Serial lines 85 and parallel lines 87 are shown connected to transceivers 92 and 94, respectively, which then also connect to connection assembly 90 for connection to various parallel and serial peripherals, such as printers and modems.

ASIC 58 is also shown connected to previously mentioned secondary bus 12. Bus 12 is shown connected to an adapter card 96 to allow the PCI bus 12 to communicate with an IDE device such as a hard drive, backup tape drive, CD-ROM drive, etc. Another adapter card 98 is shown for allowing communications from bus 12 to a universal serial port (USB). A network interface card 100 will allow communications through bus 12 to various networks operating under the Ethernet standard, Token Ring standard, etc. Video adapter card 102 (also referred to as a video means) allows the user to operate another monitor. Add-on card 104 may be one of a variety of cards selected by the user to perform a useful function. While this embodiment

shows various functions being implemented by add-on cards, other embodiments may implement one or more of these function on a common circuit board in the dock (e.g., all functions excluding perhaps the IDE adapter card).

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ASIC 58 communicates through receiver/transmitter 106, which provides a physical interface through a terminal connector 108 to cable 40, 46. Connector 108 may be a 20 pin connector capable of carrying high speed signals with EMI shielding (for example a low force helix connector of the type offered by Molex Incorporated), although other connector types may used instead. The opposite end of cable 40, 46 connects through a gigabit, terminal connector 110 to physical interface 112, which acts as a receiver/transmitter. Interface 112 is shown connected to previously mentioned first ASIC 56, which is also shown connected to an oscillator 114 to establish a local clock signal. This specific design contemplates using an external transmitter/receiver (external SERDES of lines 27, 29, 31, and 33 of Figure 1), although other embodiments can eliminate these external devices in favor of the internal devices in ASIC's 56 and 58.

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This embodiment is adapted to cooperate with a portable computer having a PCMCIA 32-bit bus 10, although other types of computers can be serviced. Accordingly, ASIC 56 is shown in a package 116 having an outline complying with the PCMCIA standard and allowing package 116 to fit into a slot in a portable computer. Therefore, ASIC 56 has a connector 118 for connection to bus 10. Cable 40, 46 will typically be permanently connected to package 116, but a detachable connector may be used in other embodiments, where a user wishes to leave package 116 inside the portable computer.

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Power supply 120 is shown producing a variety of supply voltages used to power various components. In some embodiments, one of these supply lines can be connected directly to the portable computer to charge its battery.

Referring to Figure 4, the previously mentioned simplex links 40 and 46 are shown as twin axial lines 40A and 46A, wrapped with individual shields 40B and 46B. A single shield 122 encircles the lines 40 and 46. Four parallel wires 124 are shown (although a greater number may be used in other embodiments) mounted around the periphery of shields 122 for various purposes. These wires 124 may carry power management signals, dock control signals or other signals that may be useful in an interface between a docking station and a portable computer. While twin axial lines offer high performance, twisted pairs or other transmission media may be used in other embodiments where the transmission distance is not as great and where the bit transfer speed need not be as high. While a hard wire connection is illustrated, in other embodiments a wireless or other type of connection can be employed instead.

Referring to Figure 5, previously mentioned package 116 is shown in position to be connected to a PCMCIA slot in portable computer 126. Computer 126 is shown having primary bus 10 and a host processor 128. Package 116 is shown connected through cable 40, 46 to previously mentioned connector 108 on docking station 130. Previously mentioned docking station 130 is shown connecting through PS/2 ports to keyboard 132 and mouse 134. A printer 136 is shown connected to a parallel port in docking station 130. Previously mentioned video means 102 is shown connected to a monitor 138. Docking station 130 is also shown with an internal hard drive 140 connecting to the adapter card previously mentioned. A CD-ROM drive 142 is also shown mounted in docking station 130 and connects to the secondary bus through an appropriate adapter card (not shown). Previously mentioned add-on card 104 is shown with its own cable 144.

Referring to Figure 6, a modified portable computer 126' is again shown with a host processor 128 and primary bus 10. In this embodiment however, portable computer 126' contains previously mentioned ASIC 56. Thus there is no circuitry required (other than perhaps drivers) between ASIC 56 and cable

40,46. In this case, the laptop end of cable 40, 46 has a connector 142 similar to the one on the opposite end of the cable (connector 108 of Figure 5). Connector 143 is designed to mate with connector 141 and support the high-speed link. As before, connectors 141 and 143 can also carry various power management signals, and other signals associated with a docking system.

An important advantage of this arrangement is the fact that ASIC 56 contains circuitry for providing ports, such as a serial port, a parallel port, PS/2 ports for a mouse and keyboard, and the like. Since portable computer 126' would ordinarily provide such ports, ASIC 56 simplifies the design of the portable computer. This advantage is in addition to the advantage of having a single ASIC design (that is, ASIC's 56 and 58 are structured identically), which single design is capable of operating at either the portable computer or the docking station, thereby simplifying the ASIC design and reducing stocking requirements, etc.

To facilitate an understanding of the principles associated with the foregoing apparatus, its operation will be briefly described. This operation will be described in connection with the docking system of Figures 3 and 5 (which generally relates to Figure 2), although operation would be similar for other types of arrangements. For the docking system, a connection is established by plugging package 116 (Figure 5) into portable computer 126. This establishes a link between the primary bus 10 and ASIC 56 (Figure 3).

At this time an initiator (the host processor or a master) having access to primary bus 10 may assert control of the bus. An initiator will normally send a request signal to an internal arbiter (not shown) that will eventually grant control to this initiator. In any event, the initiator asserting control over primary bus 10 will exchange the appropriate handshaking signals and drive an address onto the bus 10. Control signals simultaneously applied to the signaling lines of bus 10 will indicate whether the transaction is a read, write, or other type of

transaction.

Interface 14 (Figure 2) will examine the pending address and determine whether it represents a transaction with devices on the other side of the bridge (that is, secondary bus 12) or with the bridge itself. Configuration register 68 has already been loaded in the usual manner with information that indicates a range of addresses defining the jurisdiction of the interface 14.

Assuming a write transaction is pending on bus 10, interface 14 will transfer 32 address bits together with four control bits (PCI standard) to FIFO register 18 (Figure 1). Encoder 26 will add at least two additional bits tagging this information as an addressing cycle. The information is then broken into frames that can carry flow control and other signals before being transmitted serially over link 40.

Without waiting, interface 14 will proceed to a data cycle and accept up to 32 bits of data from bus 10 together with four byte enable bits. As before, this information will be tagged, supplemented with additional information and broken into frames for serial transmission over link 40. This transmitted information will be tagged to indicate whether it is part of a burst or a single cycle.

Upon receipt, decoder 32 restores the frames into the original 38 bit format and loads the last two described cycles onto the stack of register 24. Interface 16 eventually notices the first cycle as an addressing cycle in a write request. Interface 16 then negotiates control over bus 12 in the usual fashion and applies the address to bus 12. A device on bus 12 will respond to the write request by performing the usual handshaking.

Next, interface 16 will drive the write data stacked on register 24 into bus 12. If this transaction is a burst, interface 16 will continue to drive data

onto bus 12 by fetching it from register 24. If however this transaction is a single cycle write, interface 16 will close the transaction on bus 12 and load an acknowledgment into register 20. Since this acknowledgment need not carry data or address information, a unique code may be placed into register 20, so that encoder 28 can appropriately tag this line before parsing it into frames for transmission over link 46. Upon receipt, decoder 30 will produce a unique code that is loaded into register 22 and eventually forwarded to interface 14, which sends an acknowledgment to the device on bus 10 that the write has succeeded.

If the initiator instead sets its control bits during the address cycle to indicate a read request, interface 14 would also accept this cycle, if it has jurisdiction. Interface 14 will also signal the initiator on bus 10 that it is not ready to return data (e.g., a retry signal, which may be the stop signal as defined under the PCI standard). The initiator can still start (but not finish) a data cycle by driving its signaling lines on bus 10 with byte enable information. Using the same technique, the address information, followed by the byte enable information, will be accepted by interface 14 and loaded with tags into register 18. These two lines of information will be then encoded and transmitted serially over link 40. Upon receipt, this information will be loaded into the stack of register 24. Eventually, interface 16 will notice the first item as a read request and drive this address information onto secondary bus 12. A device on bus 12 will respond and perform the appropriate handshaking. Interface 16 will then forward the next item of information from register 24 containing the byte enables, onto bus 12 so the target device can respond with the requested data. This responsive data is loaded by interface 16 into register 20. If pre-fetching is indicated, interface 16 will initiate a number of successive read cycles to accumulate data in register 20 from sequential addresses that may or may not be requested by the initiator.

link 46 to be decoded and loaded into register 22. The transmitted data can include pre-fetched data that will be accumulated in register 22. Interface 14 transfers the first item of returning data onto primary bus 10, and allows the initiator to proceed to another read cycle if desired. If another read cycle is conducted as part of a burst transaction, the requested data will already be present in register 22 for immediate delivery by interface 14 to bus 10. If these pre-fetched data are not requested for the next cycle, then they are discarded.

Eventually the initiator will relinquish control of bus 10. Next, an initiator on bus 12 may send a request for control of bus 12 to arbiter 70 (Figure 2). If arbiter 70 grants control, the initiator may make a read or write request by driving an address onto bus 12. Interface 16 will respond if this address does not fall within the jurisdictional range of addresses specified in configuration register 67 (indicating the higher level bus 10 may have jurisdiction). In the same manner as before, but with a reversed flow over links 40, 46, interface 16 may accept address and data cycles and communicate them across link 40, 46. Before being granted bus 10, interface 14 will send a request to an arbiter (not shown) associated with bus 10.

In some instances, an initiator on primary bus 10 will wish to read from, or write to, port means 80, 82, 84, or 86. These four items are arranged to act as devices under the PCI standard. Interface 16 will therefore act as before, except that information will be routed not through bus 12, but through bus 78.

Other types of transactions may be performed, including reads and writes to the configuration registers 67 and 68 (Figure 2). Other types of transactions, as defined under the PCI standard (or other bus standards) may be performed as well.

Interrupt signals may be generated by the ports or other devices in ASIC 58. Also external interrupts may be received as indicated by block 34. IPR2023-00842
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noted before, interrupt signals may be embedded in the code sent over link 46. Upon receipt, system 60 decodes the interrupts and forwards them on to block 57, which may be simply one or more pins from ASIC 56 (implementing, for example, INTA of the PCI standard). This interrupt signal can either be sent over the bus 10 or to an interrupt controller that forwards interrupts to the host processor. System errors may be forwarded in a similar fashion to produce an output on a pin of ASIC 56 that can be routed directly to bus 10 or processed using dedicated hardware. The designer may wish to send individual status signals, which can be handled in a similar fashion along link 40, 46.

It is appreciated that various modifications may be implemented with respect to the above described, preferred embodiment. In other embodiments the illustrated ASIC's may be divided into several discrete packages using in some cases commercially available integrated circuits. Also, the media for the link may be wire, fiber-optics, infrared light, radio frequency signals, or other media. In addition, the primary and secondary buses may each have one or more devices, and these devices may be in one or more categories, including memory devices and input/output devices. Moreover, the devices may operate at a variety of clock speeds, bandwidths and data rates. Furthermore, transactions passing through the bridge may be accumulated as posted writes or as pre-fetched data, although some embodiments will not use such techniques. Also, the bridge described herein can be part of a hierarchy using a plurality of such bridges having their primary side connected to the same bus or to buses of an equivalent or different level. Additionally, the illustrated ports can be of a different number or type, or can be eliminated in some embodiments. Also, the illustrated arbiter can be eliminated for secondary buses that are not design to be occupied by a master. While a sequence of steps is described above, in other embodiments these steps may be increased or reduced in number, or performed in a different order, without departing from the scope of the present invention.

Obviously, many modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

CLAIMS:

1. A bridge accessible by a host processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, allowable ones of said devices including memory devices and input/output devices, said bridge comprising:

a link;

a first interface means coupled between said first bus and said link; and

a second interface means coupled between said second bus and said link,

said first interface means and said second interface means being operable to (a) send bus-related information serially through said link in a format different from that of said first bus and said second bus, (b) approve an initial exchange between said first bus and said second bus in response to pending bus transactions having a characteristic signifying a destination across said bridge, and (c) allow said host processor, communicating through said first bus, to individually address different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices said first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus.

2. A bridge according to claim 1 wherein said first interface means and said second interface means are operable to exchange bus-related information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus.

3. A bridge according to claim 1 wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface means being operable in response to a pending transaction on said first bus to begin processing said

5 pending transaction and to apply a retry signal to at least one of said signaling lines
 6 of said first bus before the pending transaction on said first bus has been
 7 transmitted to and acknowledged by said second bus.

8 4. A bridge according to claim 3 wherein less than all of the information on
 9 the signaling lines of said first bus is transmitted by said first interface ~~means~~ over
 10 said link.

1 5. A bridge according to claim 3 wherein said first interface ~~means~~
 2 comprises:

3 a first pair of first in first out registers for stacking information for successive
 4 groups of ~~bus-related~~ information gathered from and destined for said first bus.

1 6. A bridge according to claim 5 wherein said second interface ~~means~~
 2 comprises:

3 a second pair of first in first out registers for stacking information for
 4 successive groups of ~~bus-related~~ information gathered from and destined for said
 5 second bus.

1 7. A bridge according to claim 1 wherein said first interface ~~means~~ is
 2 selectively responsive to those addresses appearing on said first bus that are on
 3 a predetermined schedule of addresses corresponding to the bus-compatible
 4 devices accessible through said second bus, in order to avoid responding to
 5 addresses corresponding to other ones of the bus-compatible devices on said
 6 first bus.

1 8. A bridge according to claim 7 comprising:
 2 a register ~~means~~ for storing said predetermined schedule.

1 9. A bridge according to claim 7 wherein said first interface ~~means~~
 2 comprises:

3 a first register ~~means~~ for storing said predetermined schedule, said
 4 second interface ~~means~~ comprising:
 5 a second register ~~means~~ for storing said predetermined schedule.

1 10. A bridge according to claim 8 wherein said register ~~means~~ is
 2 operable to establish with respect to said first bus a base address for one or
 3 more of the bus-compatible devices on said second bus.

1 11. A bridge according to claim 1 comprising:
 2 a register ~~means~~ for establishing with respect to said first bus a base
 3 address for one or more of the bus-compatible devices on said second bus.

1 12. A bridge according to claim 1 wherein said first interface ~~means~~ and
 2 said ^{second} ~~secondary~~ interface ~~means~~ are operable to permit communication between
 3 bus-compatible devices on said second bus without routing through said first
 4 bus.

1 13. A bridge according to claim 12 comprising:
 2 an arbiter with authority to grant the second bus and without authority
 3 to grant the first bus to either said second interface ~~means~~ or one of the bus-
 4 compatible devices on said second bus.

1 14. A bridge according to claim 1 wherein said first interface ~~means~~ and
 2 said second interface ~~means~~ comprise:
 3 a first and a second programmable logic device connected between said link
 4 and said first bus and said second bus, respectively.

1 15. A bridge according to claim 1 wherein said first interface ~~means~~ and
 2 said second interface ~~means~~ comprise:
 3 a first and a second application-specific integrated circuit connected
 4 between said link and said first bus and said second bus, respectively.

1 17. A bridge according to claim 16 wherein said first and said second
2 application-specific integrated circuit each comprise:

1 18. A bridge according to claim 15 wherein said first and said second
2 application-specific integrated circuit each comprise:

1 19. A bridge according to claim 1 wherein said host processor is
2 interrupt-driven, said second interface ~~means~~ being operable to transmit through
3 said link to said first interface ~~means~~ interrupt signals destined to interrupt the
4 host processor.

1 20. A bridge according to claim 19 wherein said host processor is
2 responsive to error signals, said second interface ~~means~~ being operable to
3 transmit through said link to said first interface ~~means~~ error signals destined to
4 affect the host processor.

21. A bridge according to claim 1 wherein said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface means and said second interface means at a bit transfer rate greater than said predetermined clock speed.

1 22. A bridge according to claim 21 wherein said link comprises:
2 a pair of simplex links for sending information in opposite directions..

1 23. A bridge according to claim 22 wherein said simplex links are driven
2 for differential signal transfers.

1 24. A bridge according to claim 22 wherein each of said simplex links
2 comprises a cable with twin axial lines.

1 25. A bridge according to claim 22 wherein each of said simplex links
2 comprises a twisted pair.

1 26. A bridge according to claim 24 comprising:
2 a single shield around both of said simplex links; and
3 a separate pair of individual shields around each of said simplex links.

1 27. A bridge according to claim 1 wherein said second bus comprises
2 a PCI bus.

* 1 28. A bridge according to claim 6 wherein said second interface ~~means~~
2 is operable in response to a transaction from said link signifying an initial read
3 request, to fetch and pre-fetch data from a competent one of the bus-
4 compatible devices on said second bus for transmission back over said link in
5 order to satisfy pending and anticipated transactions.

* 1 29. A bridge according to claim 28 wherein said first interface ~~means~~
2 is operable in response to a transaction from said link signifying an initial read
3 request, to fetch and pre-fetch data from a competent one of the bus-
4 compatible devices on said first bus for transmission back over said link in order
5 to satisfy pending and anticipated transactions.

30. Abridge according to claim 1 wherein said first interface ~~means~~ and said second interface ~~means~~ are operable to permit at least one of the bus-compatible devices on said second bus to address one or more of the bus-compatible devices on said first bus using on said second bus substantially the same type of addressing as is used to access devices on said second bus.

31. A bridge accessible by a host processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, allowable ones of said devices including memory devices and input/output devices, said bridge comprising:

a link;

a first interface means coupled between said first bus and said link; and

a second interface means coupled between said second bus and said link,

said first interface means and said second interface means being operable to (a) send bus-related information serially through said link in a format different from that of said first bus and said second bus, (b) exchange bus-related information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus, and (c) allow said host processor, communicating through said first bus, to individually address different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices said first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus.

32. A bridge according to claim 31 wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface ~~means~~ being operable in response to a pending transaction on said first bus to begin processing said

5 pending transaction and to apply a retry signal to at least one of said signaling lines
 6 of said first bus before the pending transaction on said first bus has been
 7 transmitted to and acknowledged by said second bus.

1 33. A bridge according to claim 32 wherein less than all of the information
 2 on the signaling lines of said first bus is transmitted by said first interface ~~means~~
 3 over said link.

1 34. A bridge according to claim 32 wherein said first interface ~~means~~
 2 comprises:
 3 a first pair of first in first out registers for stacking information for successive
 4 groups of ~~bus-related~~ information gathered from and destined for said first bus.

1 35. A bridge according to claim 34 wherein said second interface ~~means~~
 2 comprises:
 3 a second pair of first in first out registers for stacking information for
 4 successive groups of ~~bus-related~~ information gathered from and destined for said
 5 second bus.

1 36. A bridge according to claim 31 wherein said first interface ~~means~~
 2 is selectively responsive to those addresses appearing on said first bus that are
 3 on a predetermined schedule of addresses corresponding to the bus-compatible
 4 devices accessible through said second bus, in order to avoid responding to
 5 addresses corresponding to other ones of the bus-compatible devices on said
 6 first bus.

1 37. A bridge according to claim 36 comprising:
 2 a register ~~means~~ for storing said predetermined schedule.

1 38. A bridge according to claim 36 wherein said first interface ~~means~~
 2 comprises:

a first register ~~means~~ for storing said predetermined schedule, said
 second interface ~~means~~ comprising:
 a second register ~~means~~ for storing said predetermined schedule.

39. A bridge according to claim 37 wherein said register ~~means~~ is
 operable to establish with respect to said first bus a base address for one or
 more of the bus-compatible devices on said second bus.

40. A bridge according to claim 31 comprising:
 a register ~~means~~ for establishing with respect to said first bus a base
 address for one or more of the bus-compatible devices on said second bus.

41. A bridge according to claim 31 wherein said first interface ~~means~~
 and said ^{second} ~~secondary~~ interface ~~means~~ are operable to permit communication
 between bus-compatible devices on said second bus without routing through
 said first bus.

42. A bridge according to claim 41 comprising:
 an arbiter with authority to grant the second bus and without authority
 to grant the first bus to either said second interface ~~means~~ or one of the bus-
 compatible devices on said second bus.

43. A bridge according to claim 31 wherein said first interface ~~means~~ and
 said second interface ~~means~~ comprise:
 a first and a second programmable logic device connected between said link
 and said first bus and said second bus, respectively.

44. A bridge according to claim 31 wherein said first interface ~~means~~ and
 said second interface ~~means~~ comprise:
 a first and a second application-specific integrated circuit connected between
 said link and said first bus and said second bus, respectively.

1 45. A bridge according to claim 43 wherein said first and said second
2 application-specific integrated circuit are identically structured and each have a
3 control pin for receiving a control signal to establish operation in one of two modes.

1 46. A bridge according to claim 45 wherein said first and said second
2 application-specific integrated circuit each comprise:
3 an arbiter, enabled only in said second application-specific integrated circuit,
4 with authority to grant the second bus and without authority to grant the first bus to
5 either said second interface ~~means~~ or one of the bus-compatible devices on said
6 second bus.

1 47. A bridge according to claim 43 wherein said first and said second
2 application-specific integrated circuit each comprise:
3 a plurality of port means coupled to said second interface ~~means~~ for
4 providing a plurality of ports for input/output.

1 48. A bridge according to claim 31 wherein said host processor is
2 interrupt-driven, said second interface ~~means~~ being operable to transmit through
3 said link to said first interface ~~means~~ interrupt signals destined to interrupt the
4 host processor.

1 49. A bridge according to claim 48 wherein said host processor is
2 responsive to error signals, said second interface ~~means~~ being operable to
3 transmit through said link to said first interface ~~means~~ error signals destined to
4 affect the host processor.

1 50. A bridge according to claim 31 wherein said first bus operates at a
2 predetermined clock speed, said link being operable to propagate data between
3 said first interface ~~means~~ and said second interface ~~means~~ at a bit transfer rate
4 greater than said predetermined clock speed.

1 51. A bridge according to claim 50 wherein said link comprises:
2 a pair of simplex links for sending information in opposite directions.

1 52. A bridge according to claim 51 wherein said simplex links are driven
2 for differential signal transfers.

1 53. A bridge according to claim 51 wherein each of said simplex links
2 comprises a twisted pair.

1 54. A bridge according to claim 51 wherein each of said simplex links
2 comprises a cable with twin axial lines.

1 55. A bridge according to claim 54 comprising:
2 a single shield around both of said simplex links; and
3 a separate pair of individual shields around each of said simplex links.

1 56. A bridge according to claim 31 wherein said second bus comprises
2 a PCI bus.

1 57. A bridge according to claim 35 wherein said second interface ~~means~~
2 is operable in response to a transaction from said link signifying an initial read
3 request, to fetch and pre-fetch data from a competent one of the bus-
4 compatible devices on said second bus for transmission back over said link in
5 order to satisfy pending and anticipated transactions.

1 58. A bridge according to claim 57 wherein said first interface ~~means~~
2 is operable in response to a transaction from said link signifying an initial read
3 request, to fetch and pre-fetch data from a competent one of the bus-
4 compatible devices on said first bus for transmission back over said link in order
5 to satisfy pending and anticipated transactions.

~~add~~

00130050-000693

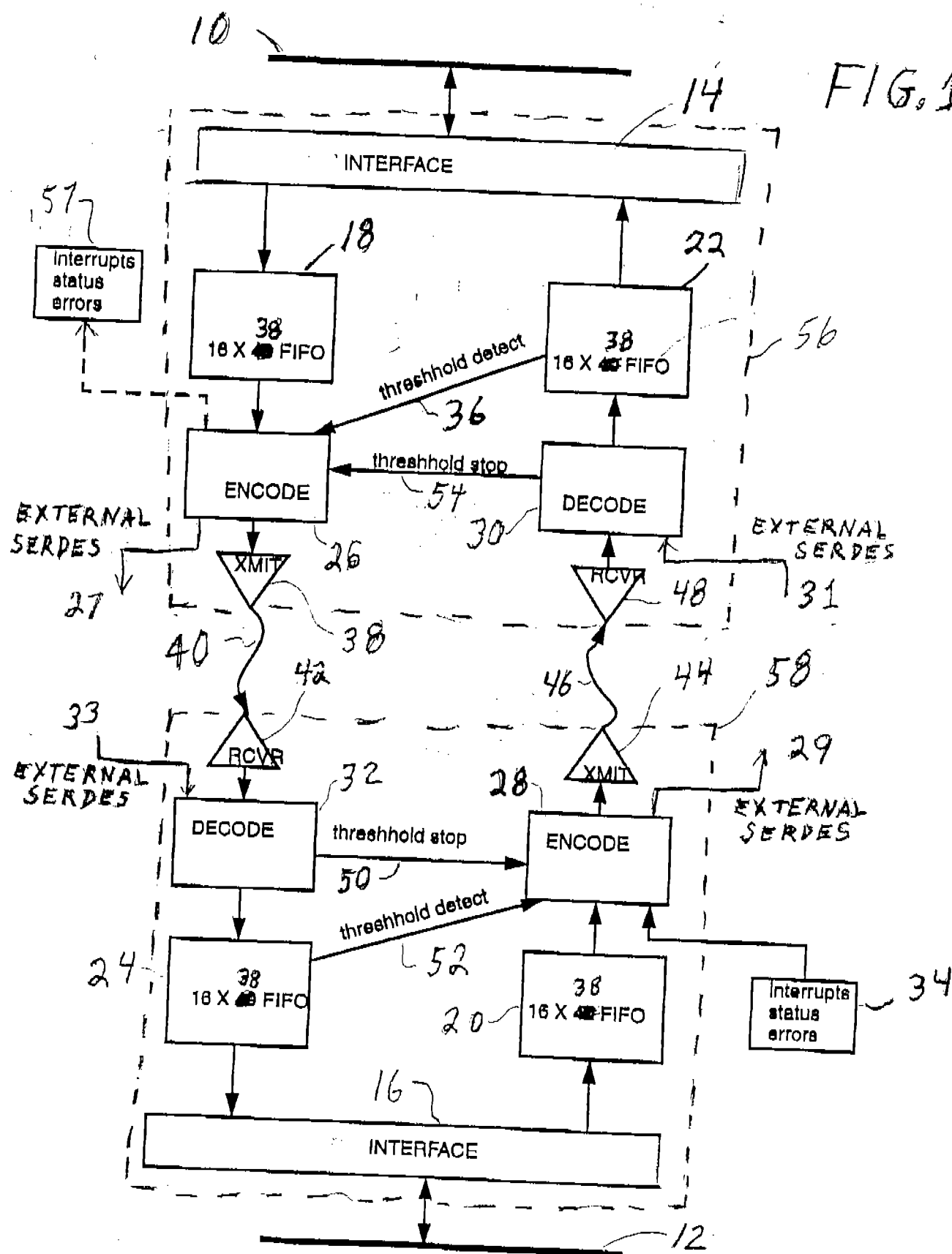


FIG. 3

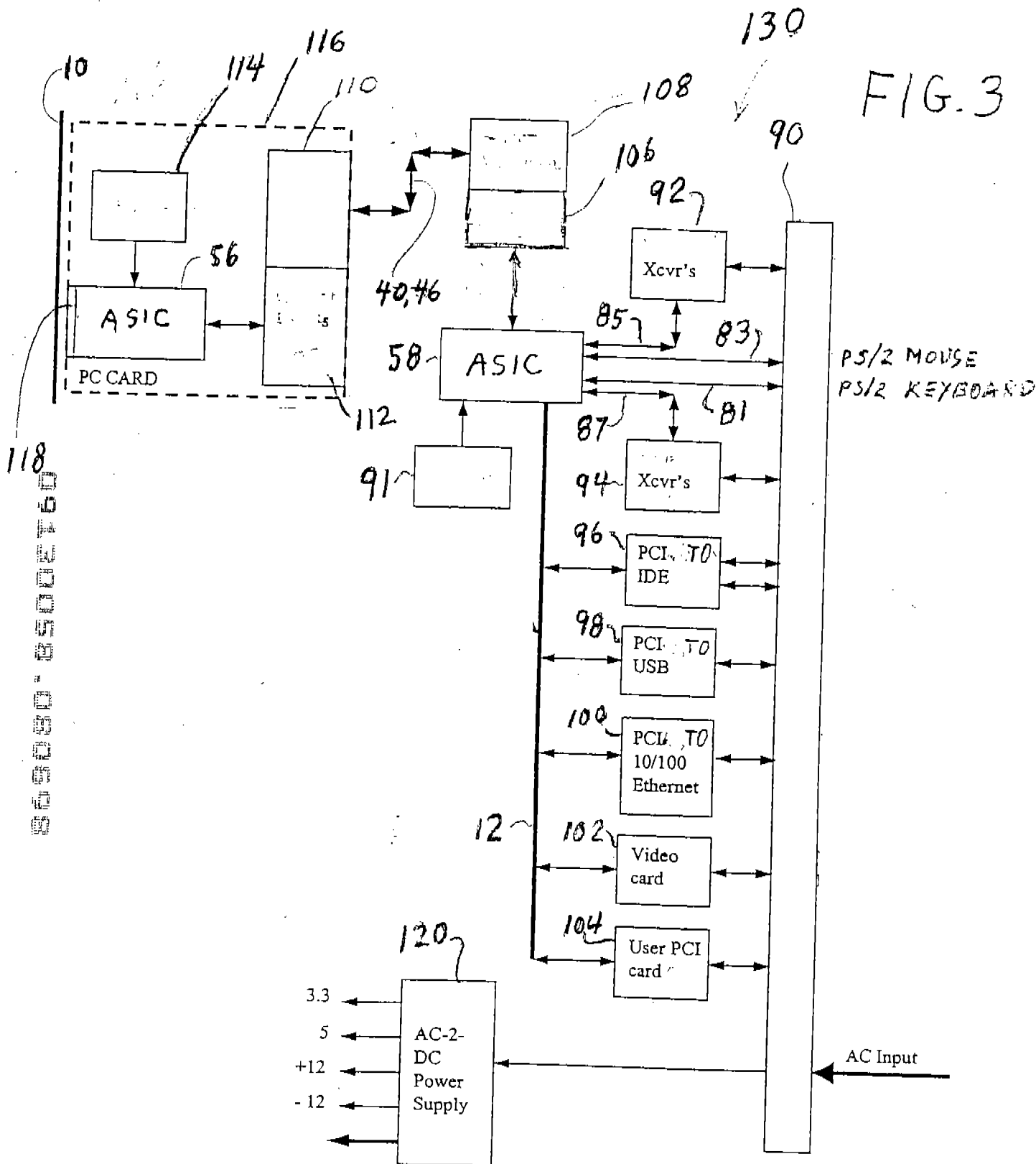
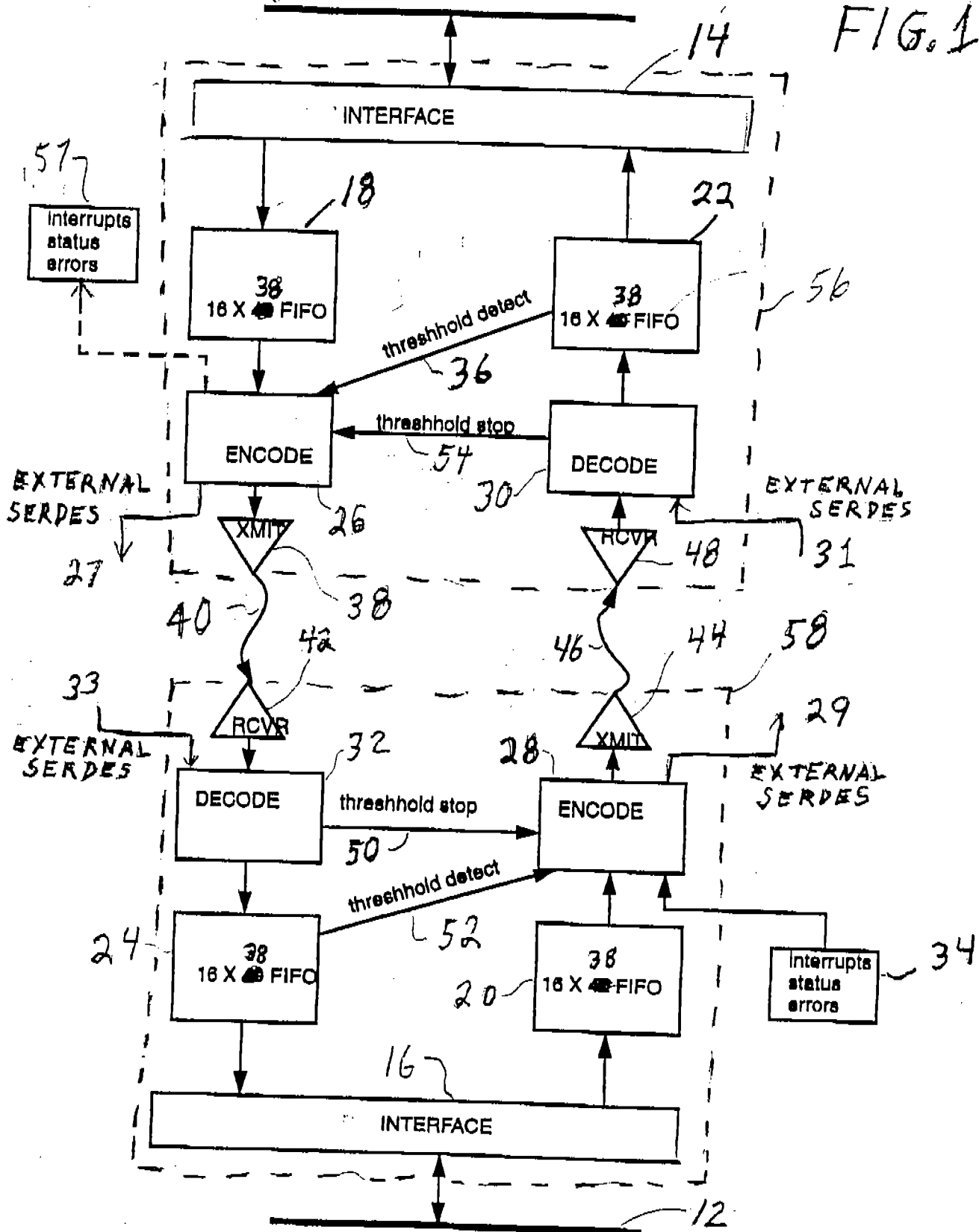


FIG. 5

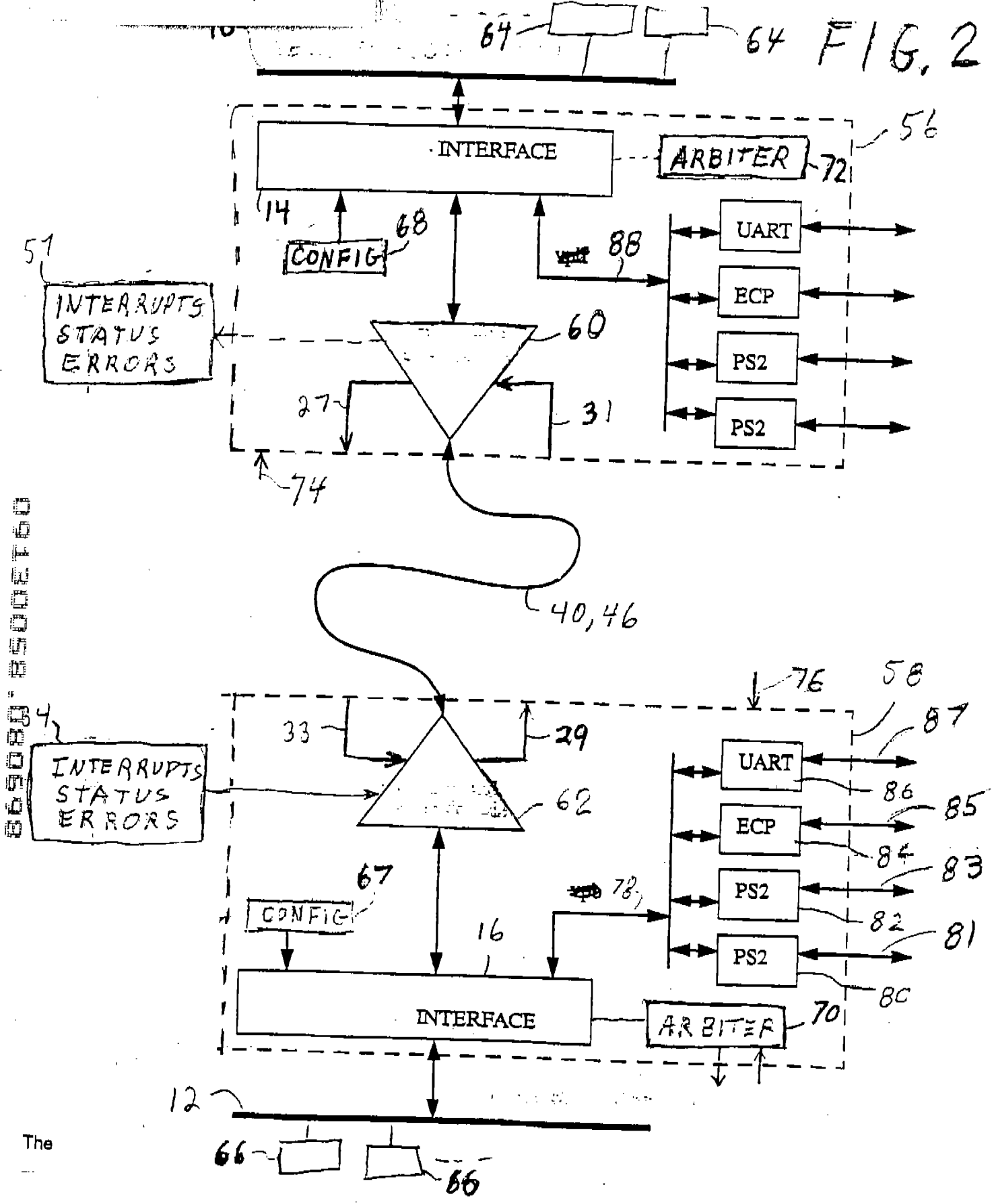
FIG. 6

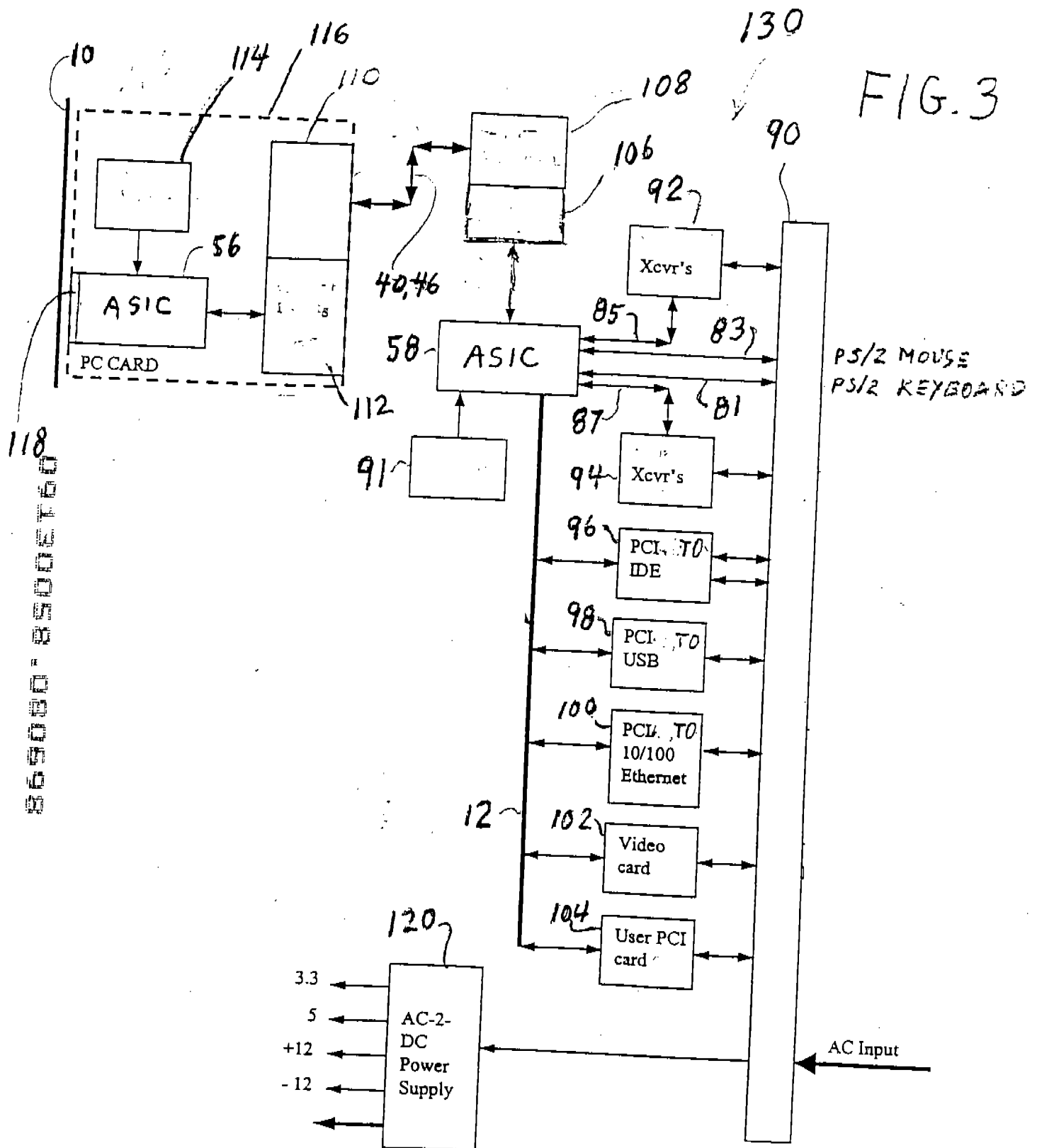
FIG. 4

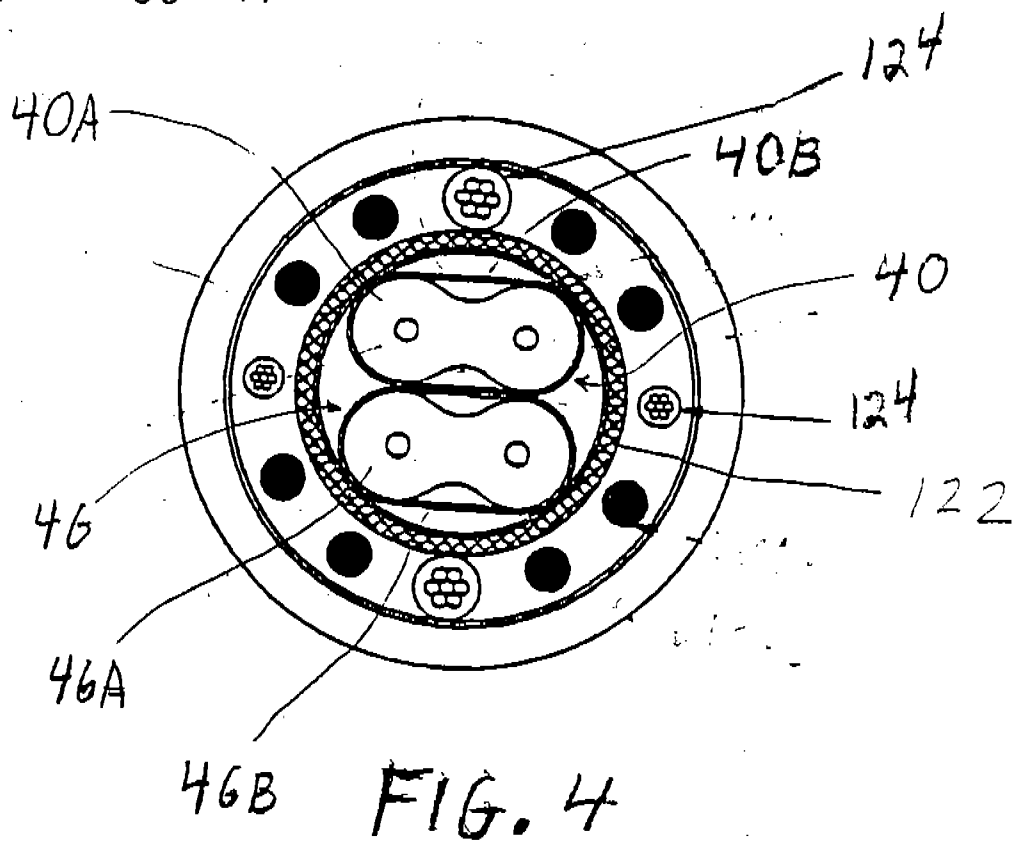
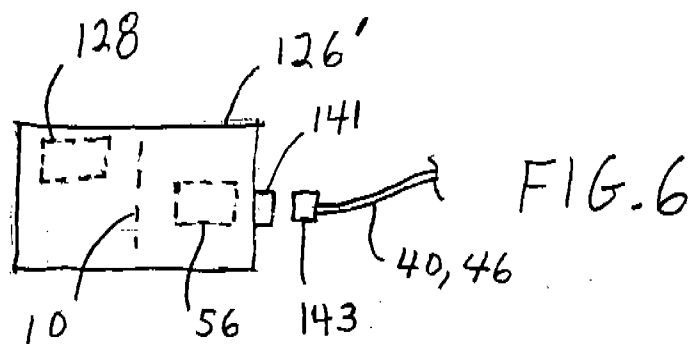
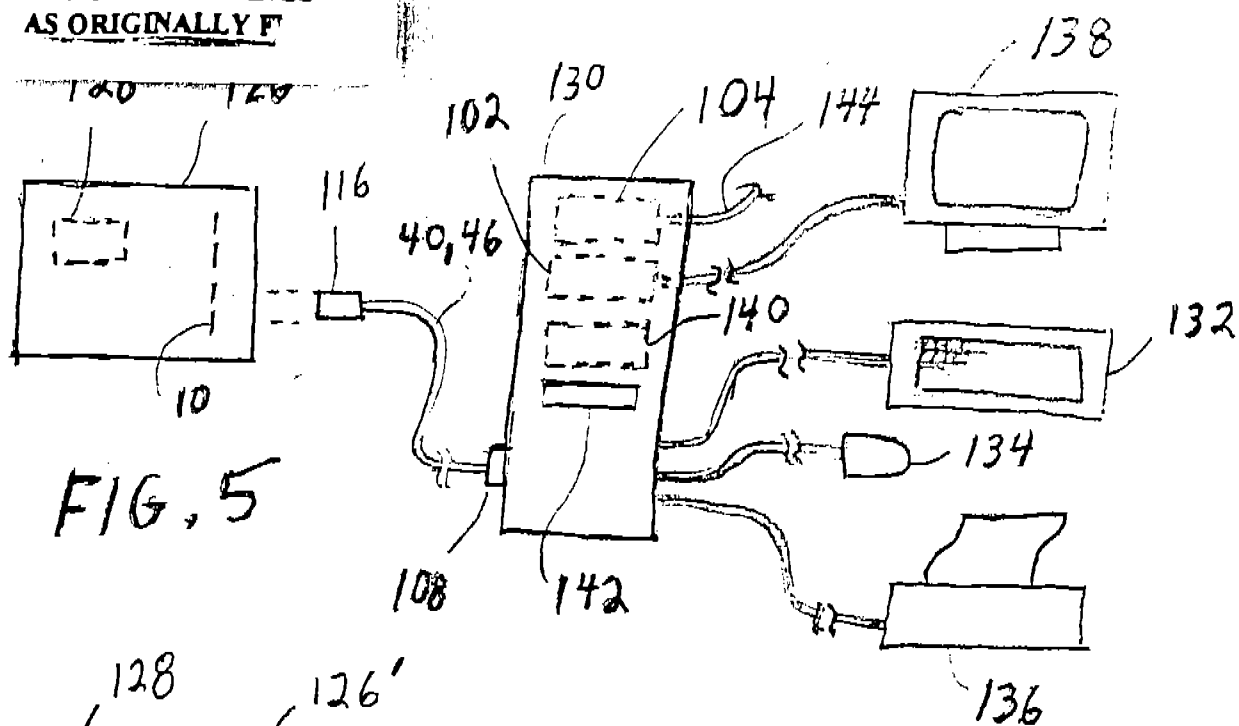
FIG. 1



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09130050-000500

Atty File: DOS14

COMBINED DECLARATION, PRIORITY CLAIM AND
POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LINKED BRIDGE

the specification of which is attached hereto; I hereby state that I have reviewed and understand the contents of the above identified specification including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56[a].

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

no prior foreign applications.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below:

no provisional applications.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT

(2)

international filing date of this application:

no United States or PCT International Applications claimed.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connect therewith: Thomas L. Adams, Esq., Reg. #27,300. Address all telephone calls to: Thomas L. Adams, Esq. at telephone no.: (973) 538-4112. Address all correspondence to: Thomas L. Adams, 10 Park Place, Morristown, New Jersey 07960.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor:

Frank Ahern

Residence:

6233 E. Janice Way, Scottsdale, AZ 85254

Citizenship: U.S.

Post Office Address: same

Dated:

8/3/98


Frank Ahern

Inventor: Frank Ahern
For: LINKED BRIDGE
Attorney's Docket No.: DOS14

**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) AND 1.27(c)) - SMALL BUSINESS CONCERN**

I hereby declare that I am an official of the small business concern and empowered to act on behalf of the concern identified below:

**MOBILITY ELECTRONICS, INC.
7955 East Redfield Road
Scottsdale, Arizona 85260**

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled LINKED BRIDGE by inventor Frank Ahern described in the specification filed herewith.

No rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and

9/130,058

Gr 2781 #

#2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

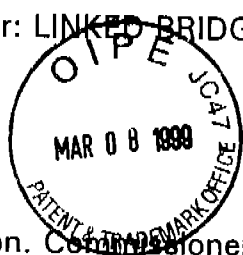
Attorney Docket: DOS14

Serial No.: 09/130,058

Group Art Unit: 2781

Filed: 8/6/98

For: LINKED BRIDGE



10 Park Place
Morristown, N.J.
March, 1999

RECEIVED

MAR 15 1999

Group 2700

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

SIR or MADAM:

PETITION TO MAKE APPLICATION SPECIAL
UNDER 37 CFR 1.102 and M.P.E.P. 708.02 (I)

Received

MAR 26 1999

Director's Office
Group 2700

The applicant respectfully petitions the Commissioner to treat the above application special under the manufacturing provision of MPEP §708.02(I). Enclosed herein is a check in the amount of \$130.00 as a petition fee (37 C.F.R. §1.17(ii)).

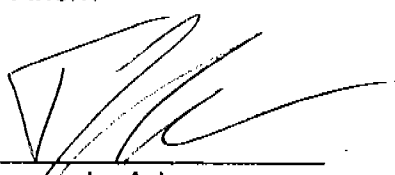
The present application has not been examined.

Prior to filing the above application, a preexamination search was made by the undersigned using various approaches, including a variety of word searches, using a commercially available, patent database offered by Corporate Intelligence of Browns Point, WA. The patents uncovered by these searches are listed in the accompanying List of Art, with copies enclosed.

Fee enclosed Declaration of the Chief Executive Officer of Mobility Electronics, Inc. demonstrates that (a) obtaining sufficient financing is dependent upon obtaining patent protection; (b) unless this patent-dependent financing is obtained, Mobility

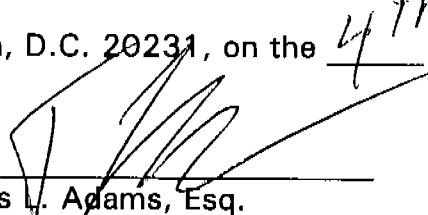
Electronics, Inc. "will be unable to fully develop this technology, manufacture related docking stations, and develop the market using the new technology disclosed in the above application;" (c) Mobility Electronics, Inc. has already made significant investments towards commercializing the technology in the above application and is committed to commercializing this technology if adequate financing can be obtained; and (d) a careful of thorough search of the prior art was made. The statements satisfy the requirements under MPEP 708.02(I).

Respectfully submitted,
Frank Ahern

By 
Thomas L. Adams
Reg. No. 27,300
(973) 538-4112

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the 4th day of March, 1999.


Thomas L. Adams, Esq.
Registration No. 27,300



INFORMATION CITED BY APPLICANT(S) THAT MAY BE MATERIAL
TO THE PROSECUTION OF THE SUBJECT APPLICATION

Applicant: Frank Ahern

Attorney Docket No.: DOS14

Serial No: 09/130,058

Group Art Unit: 2781

Filed: 08/06/98

Examiner: Unassigned

Title: LINKED BRIDGE

U.S. PATENT DOCUMENTS

Exmr Initial	ID	Document Number	Date	Name	Class	Sub Class	Filing Date
SL	A	3,800,097	03/26/74	Maruscak et al.	179	98	09/15/72
SL	B	4,413,319	11/01/83	Schultz et al.	364	200	03/09/81
SL	C	4,504,927	03/12/85	Callan	364	900	09/08/82
SL	D	4,787,029	11/22/88	Khan	364	200	09/29/86
SL	E	4,882,702	11/21/89	Struger et al.	364	900	05/16/88
SL	F	4,954,949	09/04/90	Rubin	364	200	10/02/89
SL	G	4,959,833	09/25/90	Mercola et al.	371	32	03/08/89
SL	H	4,961,140	10/02/90	Pechanek et al.	364	200	06/29/88
SL	I	5,006,981	04/09/91	Beltz et al.	364	200	11/08/88
SL	J	5,038,320	08/06/91	Heath et al.	364	900	01/06/89
SL	K	5,111,423	05/05/92	Kopec, Jr. et al.	395	500	07/21/88
SL	L	5,191,657	03/02/93	Ludwig et al.	395	325	11/09/89
SL	M	5,237,690	08/17/93	Bealkowski et al.	395	700	07/06/90
SL	N	5,274,711	11/28/93	Rutledge et al.	381	47	11/14/89
SL	O	5,325,491	06/28/94	Fasig	395	325	04/13/93
SL	P	5,335,329	08/02/94	Cox et al.	395	325	07/18/91
SL	Q	5,430,847	07/04/95	Bradley et al.	395	325	10/22/92

SL	R	5,446,869	08/29/95	Padgett et al.	395	500	12/30/93
SL	S	5,495,569	02/27/96	Kotzur	395	181	12/30/94
SL	T	5,497,498	03/05/96	Taylor	395	800	09/28/93
SL	U	5,507,002	04/09/96	Heil	395	828	12/24/92
SL	V	5,517,623	05/14/96	Farrell et al.	395	281	12/13/90
SL	W	5,524,252	06/04/96	Desai et al.	395	800	04/19/91
SL	X	5,530,895	06/25/96	Enstrom	395	829	02/25/93
SL	Y	5,540,597	07/30/96	Budman et al.	439	77	12/15/93
SL	Z	5,542,055	07/30/96	Amini et al.	395	281	05/28/93
SL	AA	5,548,730	08/20/96	Young et al.	395	280	09/20/94
SL	BB	5,555,510	09/10/96	Verseput et al.	364	514R	08/02/94
SL	CC	5,572,525	11/05/96	Shen et al.	370	85.1	05/31/95
SL	DD	5,572,688	11/05/96	Sytwu	395	309	09/30/94
SL	EE	5,590,377	12/31/96	Smith	395	842	06/07/95
SL	FF	5,611,053	03/11/97	Wu et al.	395	280	01/21/94
SL	GG	5,655,142	08/05/97	Gephardt et al.	395/800.32		08/28/96
SL	HH	5,694,556	12/02/97	Neal et al.	395	308	06/07/95
SL	II	5,696,949	12/09/97	Young	395	551	06/15/95
SL	JJ	5,701,483	12/23/97	Pun	395	681	01/24/97
SL	KK	5,724,529	03/03/98	Smith et al.	395	309	11/22/95

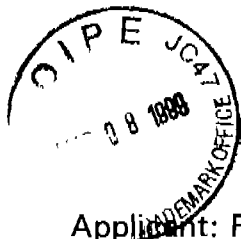
FOREIGN PATENT DOCUMENTS

Examiner Initial	ID	Document Number	Date	Name	Class	Sub Class	Trans
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OTHER INFORMATION

Sumati Lefkowitz 7/7/99
Examiner Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. §609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

Serial No.: 09/130,058

Filed: 8/6/98

For: LINKED BRIDGE

Attorney Docket: DOS14

Group Art Unit: 2781

RECEIVED

MAR 15 1999

Group 2700

DECLARATION OF CHIEF EXECUTIVE OFFICER OF MOBILITY ELECTRONICS INC.

1. I, Charles Mollo, am the Chief Executive Officer of Mobility Electronics Inc. (Mobility), the assignee of the above patent application.

2. Mobility is a three-year old company that specializes in making docking stations and related connectivity devices for portable and handheld computers.

3. In 1996 Mobility personnel conceived a new approach to docking that forms the basis of a new universal docking technology and approach that may dramatically impact the way portable computers are utilized. This new approach is disclosed in the above patent application.

4. Before filing this patent application, it is my understanding that a careful and thorough search of the prior art was conducted by our patent attorney. See the accompanying List of Art.

5. Using the technology in the above patent application, Mobility is in the process of developing and designing docking stations that (1) can be remotely located from a host computer, (2) will be compatible with almost any PCI computing device, regardless of brand or model, (3) require no special software, (4) are fully expandable,

and (4) have no performance degradation. Thus, the user can choose a docking station independent of the user's computer, and can configure the docking station in any manner the user desires (that is, by adding additional drive bays or PCI expansion cards).

6. To implement this new approach, Mobility is developing an application specific integrated circuit (ASIC), using the services of VLSI Technology, Inc. of San Jose, California. This ASIC is in the final design phase. Designing and troubleshooting this ASIC and all other aspects of the technology requires a fairly large capital investment.

7. To proceed this far, Mobility found it necessary to raise money from its founding shareholders and from select outside investors. However, to truly develop this technology and market requires a much more significant investment -- potentially in the range of the \$30-50 Million.

8. Mobility is currently in the process of raising the necessary funds through both private and potentially public sources. We envision that multiple financings will be required, most likely including one or two smaller private rounds in the near-term followed by a larger initial public offering later in 1999 or early in the year 2000.

9. Because the heart of Mobility's business proposition is the newly discovered universal docking technology, a central issue is Mobility's ability to secure patent protection on this new approach. This determination will have a dramatic impact on the company's ability to raise capital -- especially in the public market -- and the company's ability to truly commercialize this revolutionary approach to docking.

10. Mobility is committed to commercializing the technology in the above patent application, if it can obtain adequate financing.

11. Assuming Mobility is able to show investors that this new technology is proprietary and that the U.S. Patent Office has found claims of the above patent application allowable, Mobility will be able to obtain adequate financing.

12. Conversely, the opportunity to obtain financing will be impaired if Mobility is unable to demonstrate that this technology is patentable. Without adequate financing, Mobility will be unable to fully develop this technology, manufacture related docking stations, and develop the market using the new technology disclosed in the above application.

13. For this reason, an accelerated patent determination is critical to Mobility's success, and perhaps even its survival.

14. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



CHARLES MOLLO, CEO
MOBILITY ELECTRONICS, INC.

Dated: January 27, 1999



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

Paper No. 3

Thomas L. Adams
10 Park Place
Morristown, New Jersey 07960

Mailed

APR 15 1999

In re Application of
Frank Ahern
Application No.: 09/130,058
Filed: August 6, 1998
For: LINKED BRIDGE

Director's Office
Group 2700

DECISION ON PETITION TO
MAKE SPECIAL

This is a decision on the petition under 37 C.F.R. § 1.102(d) AND M.P.E.P. § 708.02(I), filed March 8, 1999, to make the above-identified application special.

The petition requests that the above-identified application be made special under the accelerated examination procedure set forth in M.P.E.P. § 708.02, Section I: Manufacture.

A grantable petition under 37 C.F.R. § 1.102(d), M.P.E.P. § 708.02, Section I, must be accompanied by the required fee and a statement by the applicant, assignee or attorney/agent registered to practice before the PTO alleging that:

1. the possession by the prospective manufacturer of sufficient presently available capital (stating approximately the amount) and facilities (stating briefly the nature thereof) to manufacture the invention in quantity or that sufficient capital and facilities will be made available if a patent is granted. If the prospective manufacturer is an individual, there must be a corroborating statement from some responsible party, as for example, an officer of a bank, showing that said individual has the required available capital to manufacture;
2. the prospective manufacturer will not manufacture, or will not increase present manufacture, unless certain that the patent will be granted;
3. the prospective manufacturer obligates himself, herself or itself, to manufacture the invention, in the United States or its possessions, in quantity immediately upon the allowance of the claims or issuance of a patent which will protect the investment of capital and facilities; and
4. the applicant has made or caused to be made a careful and thorough search of the prior art, or has a good knowledge of the pertinent prior art.

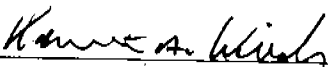
Applicant must provide one copy of each of the references deemed most closely related to the subject matter encompassed by the claims if the references are not already of record.

The petition does not include item 3 above.

The petition is **DENIED**.

Should applicant desire reconsideration, he or she should supplement this petition by providing the information for item 3 as outlined above. No further petition fee is required.

Any request for reconsideration must be filed within **TWO MONTHS** from the date of this decision.



Kenneth A. Wieder
Special Program Examiner
Technology Center 2700
Communications and Information Processing

OMRI M. BEHR
THOMAS L. ADAMS

GERALD J. WEISER*
PETER J. GAYLOR*
GABRIEL LOPEZ
OF COUNSEL

*PA BAR ONLY
*D.C. BAR ONLY



LAW OFFICES
BEHR & ADAMS
10 PARK PLACE
MORRISTOWN, NEW JERSEY 07960
FACSIMILE: (973) 538-7724
TELEPHONE: (973) 538-4112
<http://www.newidea.com>
E-mail: adams@newidea.com

June 2, 1999

Mr. Kenneth A. Weider
Special Program Examiner
Technology Center 2700
Communications and Information Processing
U. S. Patent and Trademark Office
Washington, D. C. 20231

Re: Linked Bridge (DOS14)
USSN: 09/130,058 Filed: 8/6/98

Dear Mr. Weider:

Our previously submitted Petition to Make Special was rejected by your decision mailed April 15, 1999.

Apparently, you found our previous submission adequate except for the requirement of alleging that "the prospective manufacturer obligates himself, herself or itself, to manufacture the invention, in the United States or its possessions, in quantity immediately upon the allowance of the claims or issuance of a patent which will protect the investment of capital and facilities."

It is believed the enclosed declaration by Mr. Winterich provides a basis for granting the petition.

Very truly yours,
BEHR & ADAMS

Thomas L. Adams

TLA/kc
encl.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on this 2nd day of June, 1999.

Thomas L. Adams
Registration No. 27,300

Received

JUN 17 1999

Director's Office
Group 2700

GROUP 2700

EDISON OFFICE
325 PIERSON AVENUE
EDISON, N.J. 08837
(732) 484-5240
CABLE: BEPAT EDISON, N.J.

ASSOCIATE OFFICE
WEISER & STAPLER
233 S. 18TH STREET
PHILADELPHIA, PA 19102
(215) 875-0383
PLEASE REPLY TO MORRISTOWN
JUN 15 AM 9:41
RECEIVED

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern
Serial No.: 09/130,058
Filed: 8/6/98
For: LINKED BRIDGE



Attorney Docket: 20514
Group Art Unit: 2781

99 JUN 11 AM 9:41
RECEIVED
2700

DECLARATION OF CHIEF FINANCIAL OFFICER OF MOBILITY ELECTRONICS INC.

1. I, Richard Winterich, am the Chief Financial Officer of Mobility Electronics Inc. (Mobility), the assignee of the above patent application.
2. To implement the technology of the above patent application, Mobility has developed an application specific integrated circuit (ASIC), using the services of VLSI Technology, Inc. of San Jose, California.
3. Mobility has issued purchase orders to VLSI to purchase the above ASICs.
4. Mobility has entered into a production agreement with Selectron, which will manufacture laptop computer docking stations incorporating the above noted ASIC.
5. Mobility will be attempting to license the technology of the above patent application to other original equipment manufacturers for applications outside the field of docking stations, but will be unable to perform licensing without patent approval.
6. Thus, Mobility has obligated itself to manufacture equipment incorporating the invention of the above application, in the United States or its possessions, in quantity immediately upon the allowance of the claims or issuance of a patent which will protect the investment of capital and facilities. In fact, Mobility will attempt such

manufacturing even before allowance of the claims or issuance of a patent, but its ability to continue doing so will be restricted or may fall without patent protection.

7. Specifically, Mobility wishes to show investors that this new technology is proprietary and that the U.S. Patent Office has found claims of the above patent application allowable, in order to obtain adequate financing to implement and expand manufacturing.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



RICHARD WINTERICH, CFO
MOBILITY ELECTRONICS, INC.

Dated: June 1, 1999



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

Paper No. **5**

Thomas L. Adams
10 Park Place
Morristown, New Jersey 07960

Revised

JUN 29 1999

*Director's Office
Group 2700*

In re Application of
Frank Ahern
Application No.: 09/130,058
Filed: August 6, 1998
For: LINKED BRIDGE

DECISION ON PETITION TO
MAKE SPECIAL

This is a decision on the request for reconsideration, filed June 4, 1999, of a previously filed petition under 37 C.F.R. § 1.102(d) and M.P.E.P. § 708.02(I), to make the above-identified application special.

In support of the request for reconsideration, petitioner submits a declaration from Richard Winterich, Chief Financial Officer of Mobility Electronic, Inc., in which he states that Mobility has obligated itself to manufacture equipment incorporating the invention of the subject application in the U.S., in a quantity which will protect the investment of capital and facilities.

The petition now meets all requirements as set forth in paper no. 3 .

The petition is **GRANTED**.

The application file will be forwarded to the examiner for expedited prosecution.

If the examiner can make this application special without prejudice to any possible interfering applications, and he or she should make a rigid search for such, he or she is authorized to do so for the next action. Should the application be rejected, the application will not be considered special for the subsequent action unless the applicant promptly makes a bona fide effort to place the application in condition for allowance, even if it is necessary to have an interview with the examiner to accomplish this purpose.

If the examiner finds any interfering application for the same subject matter, he or she should consider such application simultaneously with this application and should state in the official letter of such application that he or she is taking it out of its turn because of possible interference.

Should an appeal be taken in this application or should this application becomes involved in an interference, consideration of the appeal and the interference will be expedited by all Patent and

Application No. 09/130,058
On Petition

2

Trademark Office officials concerned, contingent likewise upon diligent prosecution by the applicant.

After allowance, this application will be given priority for printing. See M.P.E.P. § 1309.



Kenneth A. Wieder
Special Program Examiner
Technology Center 2700
Communications and Information Processing
(703) 305-4710



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/130,058 08/06/98 AHERN

F DOS14

THOMAS L ADAMS
10 PARK PLACE
MORRISTOWN NJ 07960

LM02/0721

EXAMINER

LEFKOWITZ, S

ART UNIT	PAPER NUMBER
----------	--------------

2781

DATE MAILED:

07/21/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
--------------------	-------------	-----------------------	---------------------

09/130,058 08/06/98 AHERN

F 00514

EXAMINER

LM02/0721

THOMAS L ADAMS
10 PARK PLACE
MORRISTOWN NJ 07960

ART UNIT 1 LIFE SCIENCES

DATE MAILED: 2781

07/21/99

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

- ☒ Responsive to communication(s) filed on 6/29/99
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

- ☒ Claim(s) 1-59 is/are pending in the application.
- Of the above, claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1-59 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claims _____ are subject to restriction or election requirement.

Application Papers

- ☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☒ The drawing(s) filed on 8/6/98 is/are objected to by the Examiner.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Series Code/Serial Number) _____
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

- ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- ☒ Notice of Reference Cited, PTO-892
- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) _____
- ☐ Interview Summary, PTO-413
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

Serial Number: 09/130,058

Page 2

Art Unit: 2781

DETAILED ACTION

1. Claims 1-59 are presented for examination.

Drawings

2. The drawings are objected to because:
 - in Figures 1 and 2, elements 10, 12, 56, 58, 88, 78, 40, and 46 are not labeled with textual information
 - in Figure 3, elements 10, 12, 40, 46, 116 and 130 are not labeled with textual information
 - in Figure 5, elements 120, 126, 10, 116, 102, 130, 104, 140, and 142 are not labeled with textual information
 - in Figure 6, elements 128, 10, 56, 40, 46, 126', 141, and 143 are not labeled with textual information

Correction is required.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A suggested title is "Serially Linked Bus Bridge For Expanding Access Over a First Bus to a Second Bus".

Claim Objections

4. Claims 12 and 41 are objected to because of the following informalities:

a. As to claims 12 and 41,

- on line 2, "secondary" should read --second--

Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-59 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8, 16-19, 16-46, and 53-63 of copending Application No. 09/130,057 in view of Hong, 5,764,924 and Goodrum et al., 5,819,053. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application is obvious in view of the copending application. The copending application discloses the same limitations as the present application with the exception

of having memory and input/output devices on the second bus and accessing the devices on the second bus without employing a second, intervening one of the devices on the second bus.

Although Hong fails to expressly teach having memory and input/output devices on the second bus, Hong does, however, disclose that the second bus (note Figure 3B, element 118) is coupled to a plurality of PCI add-in cards (note Figure 2, element 124 and column 3, lines 13-15) and further discloses that the PCI bus accommodates high performance peripherals such as motion, video, SCSI, and hard disk drives (note column 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to couple memory and input/output devices to the second bus so as to allow for the use of additional memory and input/output devices in the system without overloading the first bus.

Goodrum discloses accessing the devices (note Figure 1, elements 36) on the second bus (note Figure 1, element 32) without employing a second, intervening one of the devices on the second bus (note column 5, lines 53-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to access the devices on the second bus without employing a second, intervening one of the devices on the second bus so as to increase the speed and reduce the latency with which data transfer is performed.

7. Claims 5, 6, 34, and 35 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 47 and 48 of copending

Application No. 09/130,057 in view of Amini et al., 5,522,050 (hereinafter Amini). Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application is obvious in view of the copending application. The copending application discloses the same limitations as the present application with the exception of the stacking being performed by FIFOs.

Amini discloses that stacking in a bridge is performed by FIFOs (note Figure 4, element 102).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FIFO registers, as Amini teaches, so as to insure that the order of the data is preserved.

The mapping of the rejected claims in the present application to the copending application is as follows:

<u>Present Application</u>	<u>Copending Application</u>
<u>09/130,058</u>	<u>09/130,057</u>
1	1+3, 42+44
2	2, 43
3	4, 45
4	5, 46
5	6, 47
6	7, 48
7	23, 53
8	24
9	25
10	26, 54

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12	28, 55
13	29
14	16
15	17
16	18
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18	8
19	30, 56
20	31, 57
21	32, 58
22	33, 59
23	34
24	36
25	35
26	37
27	38, 60
28	39, 61
29	40, 62
30	41, 63
31	1+2, 42+43
32	4, 45
33	5, 46
34	6, 47
35	7, 48
36	23, 53
37	24
38	25
39	26, 54
40	27, 54
41	28, 55
42	29
43	16
44	17
45	18
46	19
47	8
48	30, 56
49	31, 57

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50	32, 58
51	33, 59
52	34
53	35
54	36
55	37
56	38, 60
57	39, 61
58	40, 62
59	41, 63

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52, and 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Goodrum et al., 5,819,053 (hereinafter Goodrum).

a. As to claim 1, Hong discloses a bridge (note Figure 2, elements 104, 114) accessible by a host processor (note Figure 3A, elements 220) for expanding access over a first bus (note Figure 2, element 106) to a second bus (note Figure 2, element 160, wherein the fact that 160 is a PCI interface implies that it is interfaced to a PCI bus), the first bus and the second

bus each being adapted to separately connect to respective ones of a plurality of bus compatible devices (note Figure 3A, elements 240 and column 4, lines 10-11 and Figure 3B, elements 124 and column 4, lines 16-17), allowable ones of the devices including memory devices and input/output devices (note column 1, lines 20-25), the bridge comprising a link (note Figure 2, element 140), a first interface means (note Figure 2, elements 106,107,158 and column 3, lines 34-37) coupled between the first bus and the link, and a second interface means (note Figure 2, elements 160,138 and column 3, lines 41-50) coupled between the second bus and the link, the first interface means and the second interface means being operable to (a) send bus related information serially through the link in a format (i.e., serial) different from that of the first bus and the second bus (i.e., parallel), (b) approve an initial exchange between the first bus and the second bus in response to pending bus transactions having a characteristic signifying a destination across the bridge (note column 5, lines 19-38, wherein the PCI configuration register, as detailed in the PCI specification, performs this function, and column 8, lines 51-54), and © allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus compatible devices on the second bus (note column 5, lines 19-36), using on the first bus substantially the same type of addressing as is used to access devices on the first bus (note column 1, line 64 - column 2, line 15 and column 8, lines 50-55).

Although Hong fails to expressly teach having memory and input/output devices on the second bus, Hong does, however, disclose that the second bus (note Figure 3B, element 118) is coupled to a plurality of PCI add-in cards (note Figure 2, element 124 and column 3, lines 13-15)

and further discloses that the PCI bus accommodates high performance peripherals such as motion, video, SCSI, and hard disk drives (note column 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to couple memory and input/output devices to the second bus so as to allow for the use of additional memory and input/output devices in the system without overloading the first bus.

Hong also fails to disclose that devices on the second bus are addressed without first employing a second, intervening one of the bus compatible devices on the second bus.

Goodrum discloses accessing the devices (note Figure 1, elements 36) on the second bus (note Figure 1, element 32) without employing a second, intervening one of the devices on the second bus (note column 5, lines 53-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to access the devices on the second bus without employing a second, intervening one of the devices on the second bus, as Goodrum teaches, in the system of Hong so as to increase the speed and reduce the latency with which data transfer is performed.

b. As to claim 2, Hong discloses that the first interface means and the second interface means are operable to exchange bus related information between the first bus and the second bus according to a predetermined hierarchy giving the first bus a higher level than the second bus (note column 3, lines 2-15, wherein the fact that the local and remote buses are both PCI buses implies that there is a predetermined hierarchy such that the first bus has a higher level than the second)

c. As to claim 3, Hong discloses that the first bus and the second bus each have a plurality of signaling lines (implicit in the fact that the first and second buses are PCI buses) for enabling bus compatible devices to negotiate bus communications, the first interface means being operable in response to a pending transaction on the first bus to begin processing the pending transaction and to apply a retry signal to at least one of the signaling lines of the first bus before the pending transaction on the first bus has been transmitted to and acknowledged by the second bus (note column 7, lines 14-26 and column 8, lines 55-59).

d. As to claim 4, Hong discloses that less than all of the information on the signaling lines of the first bus is transmitted by the first interface means over the link (note column 8, lines 4-14).

e. As to claim 7, Hong discloses that the first interface means is selectively responsive to those addresses appearing on the first bus that are on a predetermined schedule of addresses corresponding to the bus compatible devices accessible through the second bus, in order to avoid responding to addresses corresponding to other ones of the bus compatible devices on the first bus (note column 5, lines 19-34, wherein the PCI configuration register implicitly performs this function, as detailed in the PCI specification).

f. As to claim 8, Hong discloses a register means (i.e., configuration register) for storing the predetermined schedule (note column 5, lines 19-34).

g. As to claim 9, Hong discloses that the first interface means comprises a first register means (note Figure 4B, elements 319,331) for storing the predetermined schedule, the

second interface means comprising a second register means (note Figure 4B, elements 319,331) for storing the predetermined schedule (note column 4, lines 55-56 and column 5, lines 19-34).

h. As to claim 10, Hong discloses that the register means is operable to establish with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (note column 5, lines 19-34 and TABLES 1 and 2, wherein the PCI configuration register implicitly performs this function, as detailed in the PCI specification).

I. As to claim 11, Hong discloses a register means for establishing with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (note column 5, lines 19-34 and TABLES 1 and 2, wherein the PCI configuration register implicitly performs this function, as detailed in the PCI specification).

j. As to claim 12, Hong discloses that the first interface means and the second interface means are operable to permit communication between bus compatible devices on the second bus without routing through the first bus (note column 8, lines 46-47 and lines 59-63).

k. As to claim 13, Hong discloses an arbiter with authority to grant the second bus and without authority to grant the first bus to either the second interface means or one of the bus compatible devices on the second bus (note column 5, lines 39-45).

l. As to claim 14, Hong fails to disclose that the first interface means and the second interface means comprise a first and a second programmable logic device connected between the link and the first bus and the second bus, respectively.

Examiner takes Official Notice that programmable logic devices are commonly used in the art of bus systems.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of programmable logic devices in the system of Hong so as to allow the first and second interface means to be conveniently modified at the time of implementation, as needed.

m. As to claim 15, Hong discloses that the first interface means and the second interface means comprise a first and a second application specific integrated circuit connected between the link and the first bus and the second bus, respectively (note column 3, lines 8-13).

n. As to claim 16, Hong discloses the first and second application specific integrated circuits are identically structured (note column 3, lines 11-13 and column 4, lines 55-56).

Hong fails to disclose that each of the ASICs has a control pin for receiving a control signal to establish operation in one of two modes.

Goodrum discloses that each of the ASICs has a control pin for receiving a control signal to establish operation in one of two modes (note Figure 3 and column 6, lines 6-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a control pin to establish operation in one of two modes, as Goodrum teaches, in the system of Hong so as to allow for mass production, and therefore reduced cost of manufacturing, of the identical bridge chips while specifying the mode of operation through the use of a pin.

o. As to claim 17, Hong discloses that the first and second application specific integrated circuits each comprise an arbiter, enabled only in the second ASIC, with authority to grant the second bus and without authority to grant the first bus to either the second interface means or one of the bus compatible devices on the second bus (note column 3, lines 8-13 and column 5, lines 39-45).

p. As to claim 19, Hong discloses that the host processor is interrupt driven, the second interface means being operable to transmit through the link to the first interface means interrupt signals destined to interrupt the host processor (note column 5, lines 39-47 and column 6, lines 22-26).

q. As to claim 20, Hong discloses that the host processor is responsive to error signals, the second interface means being operable to transmit through the link to the first interface means error signals destined to affect the host processor (note column 9, lines 30-31, lines 46-60, column 10, lines 12-16, lines 43-47, column 11, lines 8-12).

r. As to claim 21, Hong discloses that the first bus operates at a predetermined clock speed, the link being operable to propagate data between the first interface means and the second interface means at a bit transfer rate greater than the predetermined clock speed (note column 5, lines 3-6).

s. As to claim 22, Hong discloses that the link comprises a pair of simplex links for sending information in opposite directions (note column 3, lines 28-32).

t. As to claim 23, Hong discloses that the simplex links are driven for differential signal transfers (note column 3, lines 28-32).

u. As to claim 27, Hong discloses that the second bus comprises a PCI bus (note Figure 3B, element 118).

v. As to claim 28, Hong discloses that the second interface means is operable in response to a transaction from the link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus compatible devices on the second bus for transmission back over the link in order to satisfy pending and anticipated transactions (note column 8, lines 46-47, column 9, lines 4-14 and column 9, line 63 - column 10, line 3).

w. As to claim 29, Hong discloses that the first interface means is operable in response to a transaction from the link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus compatible devices on the first bus for transmission back over the link in order to satisfy pending and anticipated transactions (note column 8, lines 46-47, column 9, lines 4-14 and column 9, line 63 - column 10, line 3).

x. As to claim 30, Hong discloses that the first interface means and the second interface means are operable to permit at least one of the bus compatible devices on the second bus to address one or more of the bus compatible devices on the first bus using on the second bus substantially the same type of addressing as is used to access devices on the second bus (note column 1, line 64 - column 2, line 15 and column 3, lines 33-50).

y. As to claim 31, Hong discloses a bridge (note Figure 2, elements 104, 114) accessible by a host processor (note Figure 3A, elements 220) for expanding access over a first bus (note Figure 2, element 106) to a second bus (note Figure 2, element 160, wherein the fact that 160 is a PCI interface implies that it is interfaced to a PCI bus), the first bus and the second bus each being adapted to separately connect to respective ones of a plurality of bus compatible devices (note Figure 3A, elements 240 and column 4, lines 10-11 and Figure 3B, elements 124 and column 4, lines 16-17), allowable ones of the devices including memory devices and input/output devices (note column 1, lines 20-25), the bridge comprising a link (note Figure 2, element 140), a first interface means (note Figure 2, elements 106,107,158 and column 3, lines 34-37) coupled between the first bus and the link, and a second interface means (note Figure 2, elements 160,138 and column 3, lines 41-50) coupled between the second bus and the link, the first interface means and the second interface means being operable to (a) send bus related information serially through the link in a format (i.e., serial) different from that of the first bus and the second bus (i.e., parallel), (b) exchange bus related information between the first bus and the second bus according to a predetermined hierarchy giving the first bus a higher level than the second bus (note column 3, lines 2-15, wherein the fact that the local and remote buses are both PCI buses implies that there is a predetermined hierarchy such that the first bus has a higher level than the second), and © allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus compatible devices on the second bus (note column 5, lines 19-36), using on the first bus substantially the same type of addressing as is

used to access devices on the first bus (note column 1, line 64 - column 2, line 15 and column 8, lines 50-55).

Although Hong fails to expressly teach having memory and input/output devices on the second bus, Hong does, however, disclose that the second bus (note Figure 3B, element 118) is coupled to a plurality of PCI add-in cards (note Figure 2, element 124 and column 3, lines 13-15) and further discloses that the PCI bus accommodates high performance peripherals such as motion, video, SCSI, and hard disk drives (note column 1, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to couple memory and input/output devices to the second bus so as to allow for the use of additional memory and input/output devices in the system without overloading the first bus.

Hong also fails to disclose that devices on the second bus are addressed without first employing a second, intervening one of the bus compatible devices on the second bus.

Goodrum discloses accessing the devices (note Figure 1, elements 36) on the second bus (note Figure 1, element 32) without employing a second, intervening one of the devices on the second bus (note column 5, lines 53-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to access the devices on the second bus without employing a second, intervening one of the devices on the second bus, as Goodrum teaches, in the system of Hong so as to increase the speed and reduce the latency with which data transfer is performed.

z. As to claim 32, Hong discloses that the first bus and the second bus each have a plurality of signaling lines (implicit in the fact that the first and second buses are PCI buses) for enabling bus compatible devices to negotiate bus communications, the first interface means being operable in response to a pending transaction on the first bus to begin processing the pending transaction and to apply a retry signal to at least one of the signaling lines of the first bus before the pending transaction on the first bus has been transmitted to and acknowledged by the second bus (note column 7, lines 14-26 and column 8, lines 55-59).

aa. As to claim 33, Hong discloses that less than all of the information on the signaling lines of the first bus is transmitted by the first interface means over the link (note column 8, lines 4-14).

bb. As to claim 36, Hong discloses that the first interface means is selectively responsive to those addresses appearing on the first bus that are on a predetermined schedule of addresses corresponding to the bus compatible devices accessible through the second bus, in order to avoid responding to addresses corresponding to other ones of the bus compatible devices on the first bus (note column 5, lines 19-34, wherein the PCI configuration register implicitly performs this function, as outlined in the PCI specification).

cc. As to claim 37, Hong discloses a register means (i.e., configuration register) for storing the predetermined schedule (note column 5, lines 19-34).

dd. As to claim 38, Hong discloses that the first interface means comprises a first register means (note Figure 4B, elements 319,331) for storing the predetermined schedule, the

second interface means comprising a second register means (note Figure 4B, elements 319,331) for storing the predetermined schedule (note column 4, lines 55-56 and column 5, lines 19-34).

ee. As to claim 39, Hong discloses that the register means is operable to establish with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (note column 5, lines 19-34 and TABLES 1 and 2, wherein the PCI configuration register implicitly performs this function, as detailed in the PCI specification).

ff. As to claim 40, Hong discloses a register means for establishing with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (note column 5, lines 19-34 and TABLES 1 and 2, wherein the PCI configuration register implicitly performs this function, as detailed in the PCI specification).

gg. As to claim 41, Hong discloses that the first interface means and the second interface means are operable to permit communication between bus compatible devices on the second bus without routing through the first bus (note column 8, lines 46-47 and lines 59-63).

hh. As to claim 42, Hong discloses an arbiter with authority to grant the second bus and without authority to grant the first bus to either the second interface means or one of the bus compatible devices on the second bus (note column 5, lines 39-45).

ii. As to claim 43, Hong fails to disclose that the first interface means and the second interface means comprise a first and a second programmable logic device connected between the link and the first bus and the second bus, respectively.

Examiner takes Official Notice that programmable logic devices are commonly used in the art of bus systems.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of programmable logic devices in the system of Hong so as to allow the first and second interface means to be conveniently modified at the time of implementation, as needed.

jj. As to claim 44, Hong discloses that the first interface means and the second interface means comprise a first and a second application specific integrated circuit connected between the link and the first bus and the second bus, respectively (note column 3, lines 8-13).

kk. As to claim 45, Hong discloses the first and second application specific integrated circuits are identically structured (note column 3, lines 11-13 and column 4, lines 55-56).

Hong fails to disclose that each of the ASICs has a control pin for receiving a control signal to establish operation in one of two modes.

Goodrum discloses that each of the ASICs has a control pin for receiving a control signal to establish operation in one of two modes (note Figure 3 and column 6, lines 6-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a control pin to establish operation in one of two modes, as Goodrum teaches, in the system of Hong so as to allow for mass production, and therefore reduced cost of manufacturing, of the identical bridge chips while specifying the mode of operation through the use of a pin.

ll. As to claim 46, Hong discloses that the first and second application specific integrated circuits each comprise an arbiter, enabled only in the second ASIC, with authority to grant the second bus and without authority to grant the first bus to either the second interface means or one of the bus compatible devices on the second bus (note column 3, lines 8-13 and column 5, lines 39-45).

mm. As to claim 48, Hong discloses that the host processor is interrupt driven, the second interface means being operable to transmit through the link to the first interface means interrupt signals destined to interrupt the host processor (note column 5, lines 39-47 and column 6, lines 22-26).

nn. As to claim 49, Hong discloses that the host processor is responsive to error signals, the second interface means being operable to transmit through the link to the first interface means error signals destined to affect the host processor (note column 9, lines 30-31, lines 46-60, column 10, lines 12-16, lines 43-47, column 11, lines 8-12).

oo. As to claim 50, Hong discloses that the first bus operates at a predetermined clock speed, the link being operable to propagate data between the first interface means and the second interface means at a bit transfer rate greater than the predetermined clock speed (note column 5, lines 3-6).

pp. As to claim 51, Hong discloses that the link comprises a pair of simplex links for sending information in opposite directions (note column 3, lines 28-32).

qq. As to claim 52, Hong discloses that the simplex links are driven for differential signal transfers (note column 3, lines 28-32).

rr. As to claim 56, Hong discloses that the second bus comprises a PCI bus (note Figure 3B, element 118).

ss. As to claim 57, Hong discloses that the second interface means is operable in response to a transaction from the link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus compatible devices on the second bus for transmission back over the link in order to satisfy pending and anticipated transactions (note column 8, lines 46-47, column 9, lines 4-14 and column 9, line 63 - column 10, line 3).

tt. As to claim 58, Hong discloses that the first interface means is operable in response to a transaction from the link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus compatible devices on the first bus for transmission back over the link in order to satisfy pending and anticipated transactions (note column 8, lines 46-47, column 9, lines 4-14 and column 9, line 63 - column 10, line 3).

uu. As to claim 59, Hong discloses that the first interface means and the second interface means are operable to permit at least one of the bus compatible devices on the second bus to address one or more of the bus compatible devices on the first bus using on the second bus substantially the same type of addressing as is used to access devices on the second bus (note column 1, line 64 - column 2, line 15 and column 3, lines 33-50).

10. Claims 5, 6, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Goodrum et al., 5,819,053 (hereinafter Goodrum), as applied to claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52, and 56-59 above, and further in view of Amini et al., 5,522,050 (hereinafter Amini).

a. As to claim 5, Hong discloses that the first interface means comprises a first pair of registers for stacking information for successive groups of bus related information gathered from and destined for the first bus (note column 5, lines 7-19, column 7, lines 2-13).

Hong fails to disclose that the registers are FIFO registers.

Amini discloses that registers used in a bridge are FIFO registers (note Figure 4, element 102).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FIFO registers, as Amini teaches, in the system of Hong so as to insure that the order of the data is preserved.

b. As to claim 6, Hong discloses that the second interface means comprises a second pair of registers for stacking information for successive groups of bus related information gathered from and destined for the second bus (note column 5, lines 7-19, column 7, lines 2-13).

Hong fails to disclose that the registers are FIFO registers.

Amini discloses that registers used in a bridge are FIFO registers (note Figure 4, element 102).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FIFO registers, as Amini teaches, in the system of Hong so as to insure that the order of the data is preserved.

c. As to claim 34, Hong discloses that the first interface means comprises a first pair of registers for stacking information for successive groups of bus related information gathered from and destined for the first bus (note column 5, lines 7-19, column 7, lines 2-13).

Hong fails to disclose that the registers are FIFO registers.

Amini discloses that registers used in a bridge are FIFO registers (note Figure 4, element 102).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FIFO registers, as Amini teaches, in the system of Hong so as to insure that the order of the data is preserved.

d. As to claim 35, Hong discloses that the second interface means comprises a second pair of registers for stacking information for successive groups of bus related information gathered from and destined for the second bus (note column 5, lines 7-19, column 7, lines 2-13).

Hong fails to disclose that the registers are FIFO registers.

Amini discloses that registers used in a bridge are FIFO registers (note Figure 4, element 102).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FIFO registers, as Amini teaches, in the system of Hong so as to insure that the order of the data is preserved.

11. Claims 18 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Goodrum et al., 5,819,053 (hereinafter Goodrum), as applied to claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52, and 56-59 above, and further in view of Wang et al., 5,799,207 (hereinafter Wang).

a. As to claim 18, Hong fails to disclose that the first and second application specific integrated circuits each comprise a plurality of port means coupled to the second interface means for providing a plurality of ports for input/output.

Wang discloses bridge circuitry that comprises a plurality of port means (note Figure 14, S-PORT and M-PORT) for providing a plurality of ports for input/output.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the first and second ASICs of Hong comprise a plurality of port means coupled to the second interface means for providing a plurality of ports for input/output, as Wang teaches, so as to reduce the likelihood of delays for transfers between the processor and I/O devices, thereby reducing the likelihood of total process execution blocking of the processor, as Wang teaches in column 16, lines 30-40.

b. As to claim 47, Hong fails to disclose that the first and second application specific integrated circuits each comprise a plurality of port means coupled to the second interface means for providing a plurality of ports for input/output.

Wang discloses bridge circuitry that comprises a plurality of port means (note Figure 14, S-PORT and M-PORT) for providing a plurality of ports for input/output.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the first and second ASICs of Hong comprise a plurality of port means coupled to the second interface means for providing a plurality of ports for input/output, as Wang teaches, so as to reduce the likelihood of delays for transfers between the processor and I/O devices, thereby reducing the likelihood of total process execution blocking of the processor, as Wang teaches in column 16, lines 30-40.

12. Claims 24, 26, 54, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Goodrum et al., 5,819,053 (hereinafter Goodrum), as applied to claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52, and 56-59 above, and further in view of Hardie et al., 5,483,020 (hereinafter Hardie).

a. As to claim 24, Hong fails to disclose that each of the simplex links comprises a cable with twin axial lines.

Hardie discloses a cable with twin axial lines (note abstract and column 1, lines 41-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the twin axial lines of Hardie into the system of Hong for the purpose of enabling high speed, high fidelity data transmission at a low cost, as Hardie teaches in column 1, lines 38-49.

b. As to claim 26, Hong fails to disclose a single shield around both of the simplex links and a separate pair of individual shields around each of the simplex links.

Hardie discloses a single shield around both of the simplex links and a separate pair of individual shields around each of the simplex links (note column 1, lines 41-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the shield configuration of Hardie into the system of Hong for the purpose of enabling high speed, high fidelity data transmission at a low cost, as Hardie teaches in column 1, lines 38-49.

c. As to claim 54, Hong fails to disclose that each of the simplex links comprises a cable with twin axial lines.

Hardie discloses a cable with twin axial lines (note abstract and column 1, lines 41-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the twin axial lines of Hardie into the system of Hong for the purpose of enabling high speed, high fidelity data transmission at a low cost, as Hardie teaches in column 1, lines 38-49.

d. As to claim 55, Hong fails to disclose a single shield around both of the simplex links and a separate pair of individual shields around each of the simplex links.

Hardie discloses a single shield around both of the simplex links and a separate pair of individual shields around each of the simplex links (note column 1, lines 41-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the shield configuration of Hardie into the system of Hong for the purpose of enabling high speed, high fidelity data transmission at a low cost, as Hardie teaches in column 1, lines 38-49.

13. Claims 25 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Goodrum et al., 5,819,053 (hereinafter Goodrum), as applied to claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52, and 56-59 above, and further in view of Potter, 5,809,262.

a. As to claim 25, Hong fails to disclose that each of the simplex links comprises a twisted pair.

Potter discloses links that comprise a twisted pair (note column 3, lines 63-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of links comprising a twisted pair, as Potter teaches, in the system of Hong, since twisted pairs have reduced susceptibility to noise coupling and allow for greater transmission lengths.

b. As to claim 53, Hong fails to disclose that each of the simplex links comprises a twisted pair.

Potter discloses links that comprise a twisted pair (note column 3, lines 63-64).

Serial Number: 09/130,058

Page 28

Art Unit: 2781

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of links comprising a twisted pair, as Potter teaches, in the system of Hong, since twisted pairs have reduced susceptibility to noise coupling and allow for greater transmission lengths.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses transferring data between parallel buses in a serial manner.

US Patents:	5,748,921	Lambrecht et al.	5,586,265	Beukema
	5,579,489	Dornier et al.	5,561,806	Fitchett et al.
	5,475,818	Molyneaux et al.	5,457,785	Kikinis et al.
	5,335,326	Nguyen et al.		

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is (703) 308-7790. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh, can be reached at (703) 305-9648. The FAX phone number for this Group is (703) 305-3718.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [sumati.lefkowitz@uspto.gov] or [ayza.sheikh@uspto.gov].

Serial Number: 09/130,058

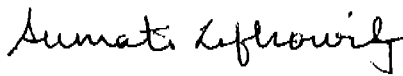
Page 29

Art Unit: 2781

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, whose telephone number is (703) 305-9600.

Sumati Lefkowitz
July 19, 1999


SUMATI LEFKOWITZ
PATENT EXAMINER

FORM PTO-892		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 09/130,058	GROUP ART UNIT 2781	ATTACHMENT TO PAPER NO.	6
NOTICE OF REFERENCES CITED				APPLICANT(S) Ahern			
U.S. PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	A	5,819,053	10/1998	Goodrum et al	710	126	
	B	5,809,262	9/1998	Potter	710	129	
	C	5,799,207	8/1998	Wang et al	710	38	
	D	5,793,995	8/1998	Riley et al	710	128	
	E	5,774,681	6/1998	Kunishige	710	128	
	F	5,764,924	6/1998	Hong	710	101	
	G	5,748,921	5/1998	Lambrecht et al	710	128	
	H	5,586,265	12/1996	Beukema	709	217	
	I	5,579,489	11/1996	Dornier et al.	710	101	
	J	5,561,806	10/1996	Fitchett et al.	709	250	
	K	5,483,020	1/1996	Hardie et al.	174	36	
FOREIGN PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB- CLASS
	L						
	M						
	N						
	O						
	P						
	Q						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
	R						
	S						
	T						
	U						
EXAMINER Sumati Lefkowitz			DATE July 15, 1999		Form892ccs2106b		
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)					IPR2023-00842 EX. 2003 Page 97 of 145		

FORM PTO-892		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 09/130,058	GROUP ART UNIT 2781	ATTACHMENT TO PAPER NO.	6
NOTICE OF REFERENCES CITED				APPLICANT(S) Ahern			
U.S. PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	A	5,475,818	12/1995	Molyneaux et al.	709	208	
	B	5,457,785	10/1995	Kikinis et al.	710	128	
	C	5,335,326	8/1994	Nguyen et al.		1	
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						
FOREIGN PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB- CLASS
	L						
	M						
	N						
	O						
	P						
	Q						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
	R						
	S						
	T						
	U						
EXAMINER Sumati Lefkowitz			DATE July 15, 1999				
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)					Form892ccs2106b IPR2023-00842 EX. 2003 Page 98 of 145		

130058

NOTICE OF DRAFTPERSON'S
PATENT DRAWING REVIEWThe drawing filed (insert date) 8/6/98 are:A. ☐ not objected to by the Draftperson under 37 CFR 1.84 or 1.152.B. ☒ objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings where necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.☐ Color drawing are not acceptable until petition is granted.

Fig(s) _____

☐ Pencil and non black ink is not permitted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84(b)

☐ Photographs are not acceptable until petition is granted.☐ 3 full-tone sets are required. Fig(s) _____☐ Photographs not properly mounted (must bryistol board or photographic double-weight paper). Fig(s) _____☐ Poor quality (half-tone). Fig(s) _____

3. TYPE OF PAPER. 37 CFR 1.84(e)

☐ Paper not flexible, strong, white and durable.

Fig(s) _____

☐ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not acceptable. (too thin)☐ Mylar, vellum paper is not acceptable (too thin).

Fig(s) _____

4. SIZE OF PAPER. 37 CFR 1.84(F): Acceptable sizes:

☐ 21.0 cm by 29.7 cm (DIN size A4)☐ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)☐ All drawings sheets not the same size.

Sheet(s) _____

5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: A4 SizeTop 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: 8 1/2 x 11Margins not acceptable. Fig(s) 1-3, 5☒ Top (T) ☒ Left (L)☐ Right (R) ☐ Bottom (B)

6. VIEWS. CFR 1.84(h)

REMINDER: Specification may require revision to correspond to drawing changes.

☐ Views connected by projection lines or lead lines.

Fig(s) _____

Partial views. 37 CFR 1.84(h)(2)

☐ Brackets needed to show figure as one entity.

Fig(s) _____

☐ Views not labeled separately or properly.

Fig(s) _____

☐ Enlarged view not labeled separately or properly.

Fig(s) _____

7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)

☐ Hatching not indicated for sectional portions of an object.

Fig(s) _____

☐ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig(s) _____☐ Views not on the same plane on drawing sheet. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.

Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)

☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable and black (poor line quality).Fig(s) 1-6

11. SHADING. 37 CFR 1.84(m)

☐ Solid black areas pale. Fig(s) _____☐ Solid black shading not permitted. Fig(s) _____☐ Shade lines, pale, rough and blurred. Fig(s) _____12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.
37 CFR 1.48(p)☐ Numbers and reference characters not plain and legible.

Fig(s) _____

☐ Figure legends are poor. Fig(s) _____☐ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig(s) _____☐ English alphabet not used. 37 CFR 1.84(p)(3) Fig(s) _____☐ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.48(t)

☐ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Fig(s) _____

15. NUMBERING OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from PTO-948 dated _____

17. DESIGN DRAWINGS. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____☐ Solid black shading not used for color contrast.

Fig(s) _____

COMMENTS



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#7
LIT
12-6-00

Applicant: Frank Ahern

Atty. Docket: DOS14

Serial No.: 09/130,058

Filed: 08/06/98

Group Art Unit: 2781

For: LINKED BRIDGE

10 Park Place
Morristown, N.J.
December, 1999

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Commissioner:

Kindly review the enclosed drawings for completeness and accuracy.

If satisfactory, kindly forward them with the enclosed letter to the Official Draftsman.

Respectfully submitted,
Frank Ahern



THOMAS L. ADAMS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the 20th day of December, 1999.



Thomas L. Adams, Esq.
Registration No. 27,300



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

Atty. Docket: DOS14

Serial No.: 09/130,058

Filed: 08/06/98

Group Art Unit: 2781

For: LINKED BRIDGE

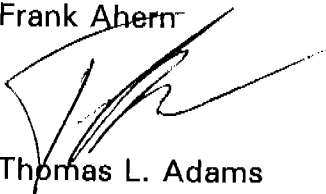
10 Park Place
Morristown, N.J.
December, 1999

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231
Attn: Official Draftsperson

Dear Commissioner:

Please review and file the enclosed drawings in place of those originally filed.

Respectfully submitted,
Frank Ahern

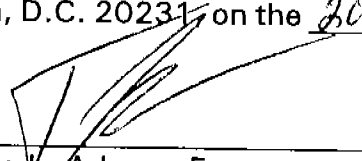
A handwritten signature in black ink, appearing to be "T. Adams".

Thomas L. Adams

TLA/kc
Enclosure

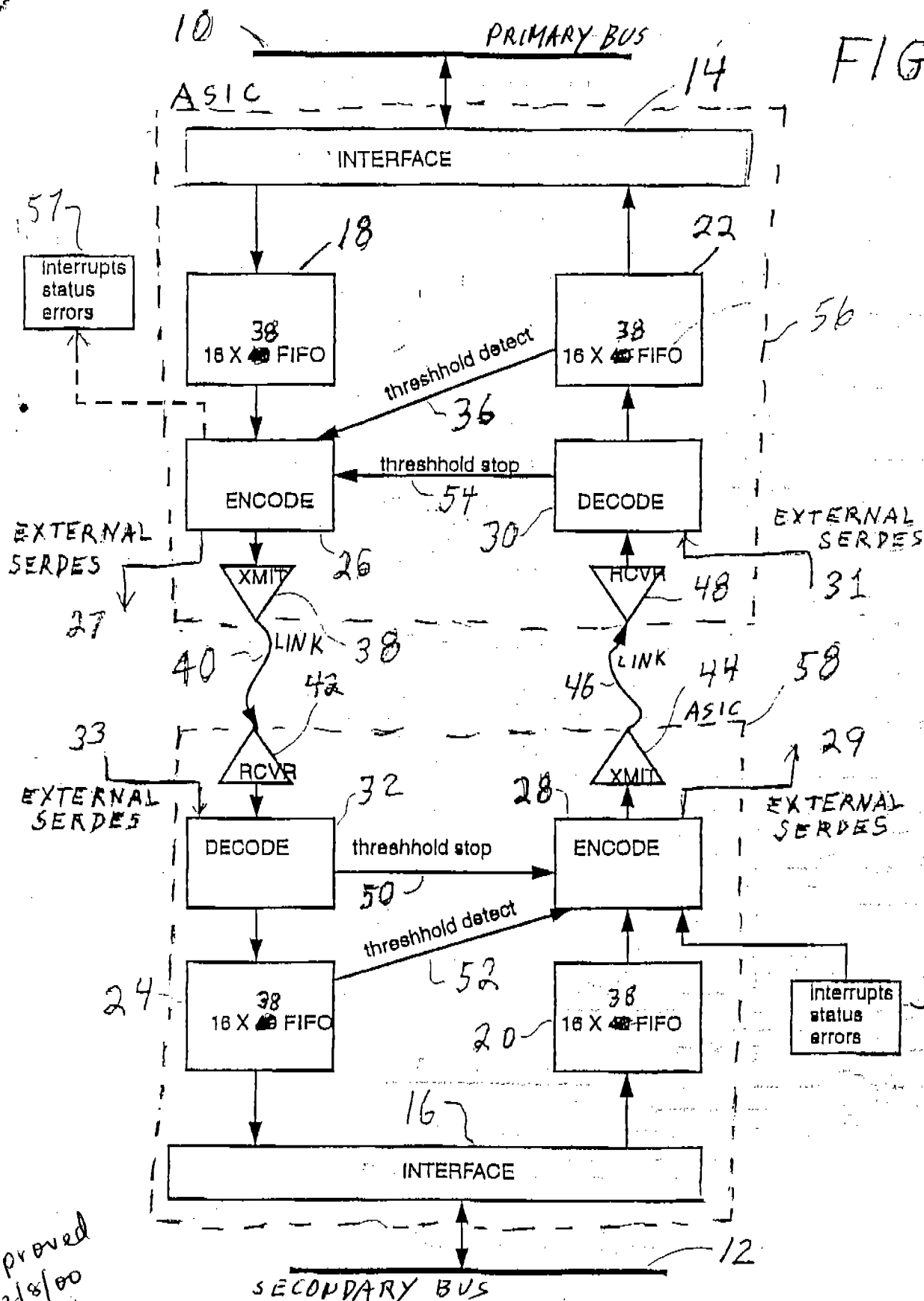
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on the 20th day of December, 1999.



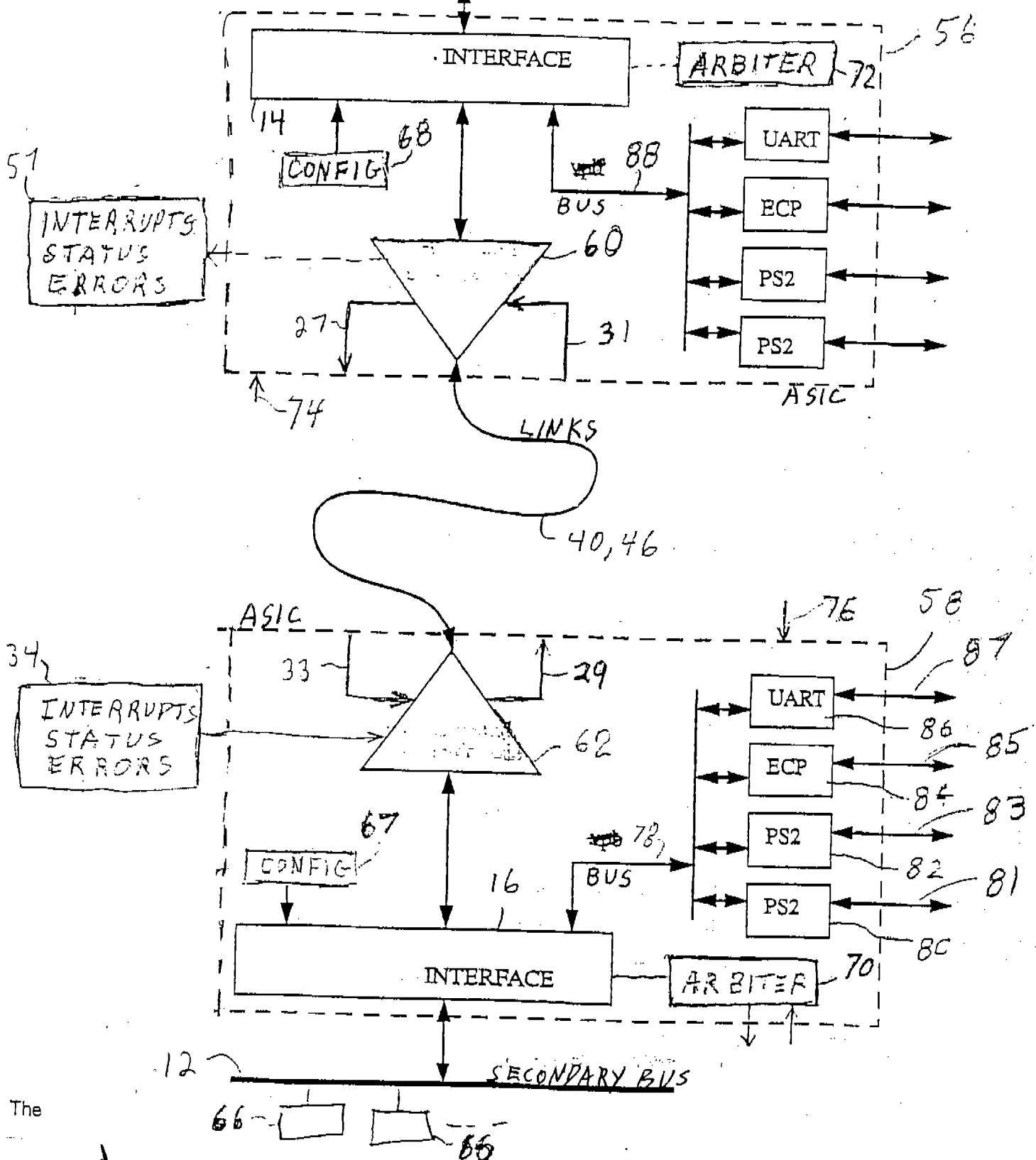
Thomas L. Adams, Esq.
Registration No. 27,300

FIG. 1



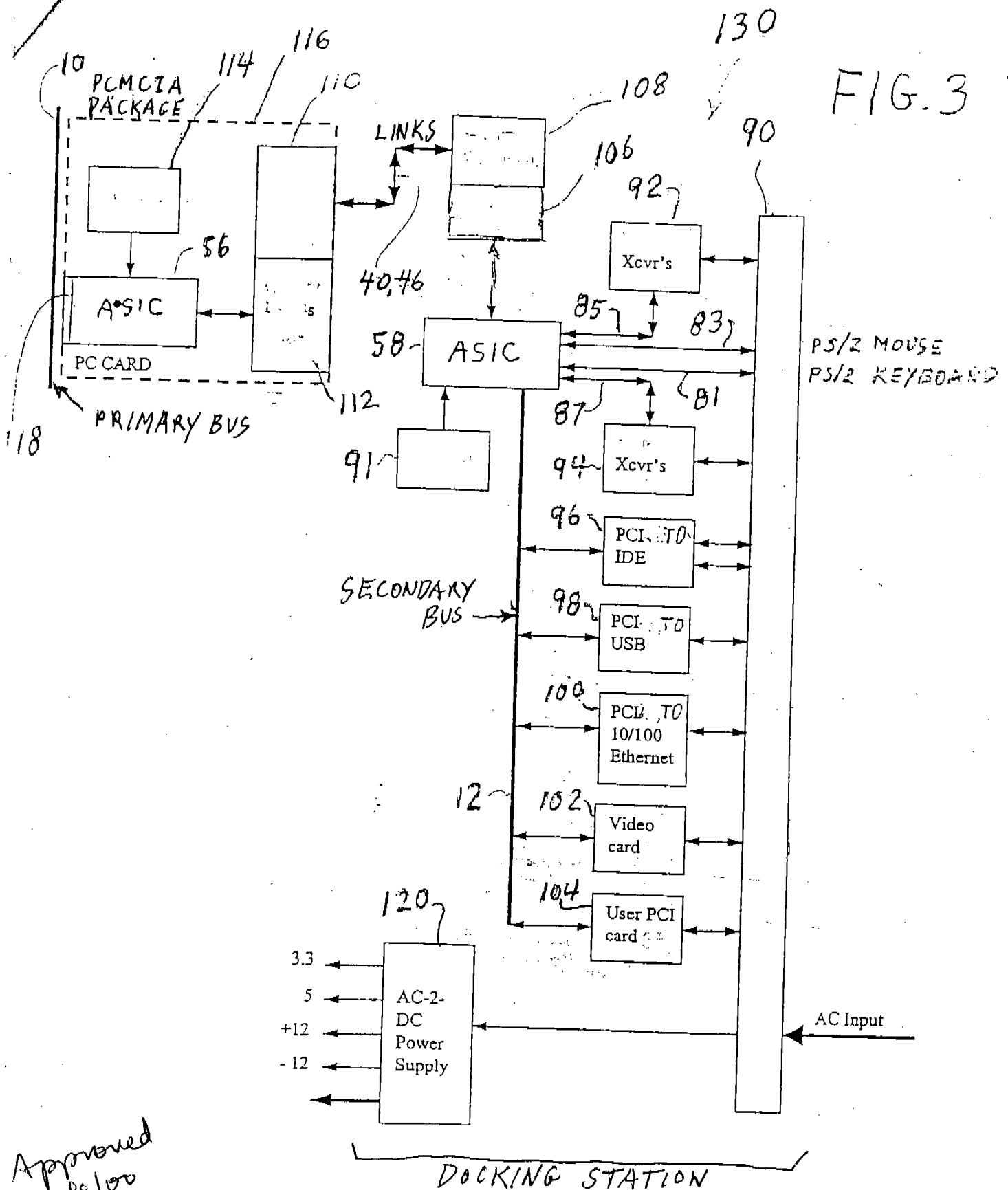
Approved
2/8/00
SL

FIG. 2

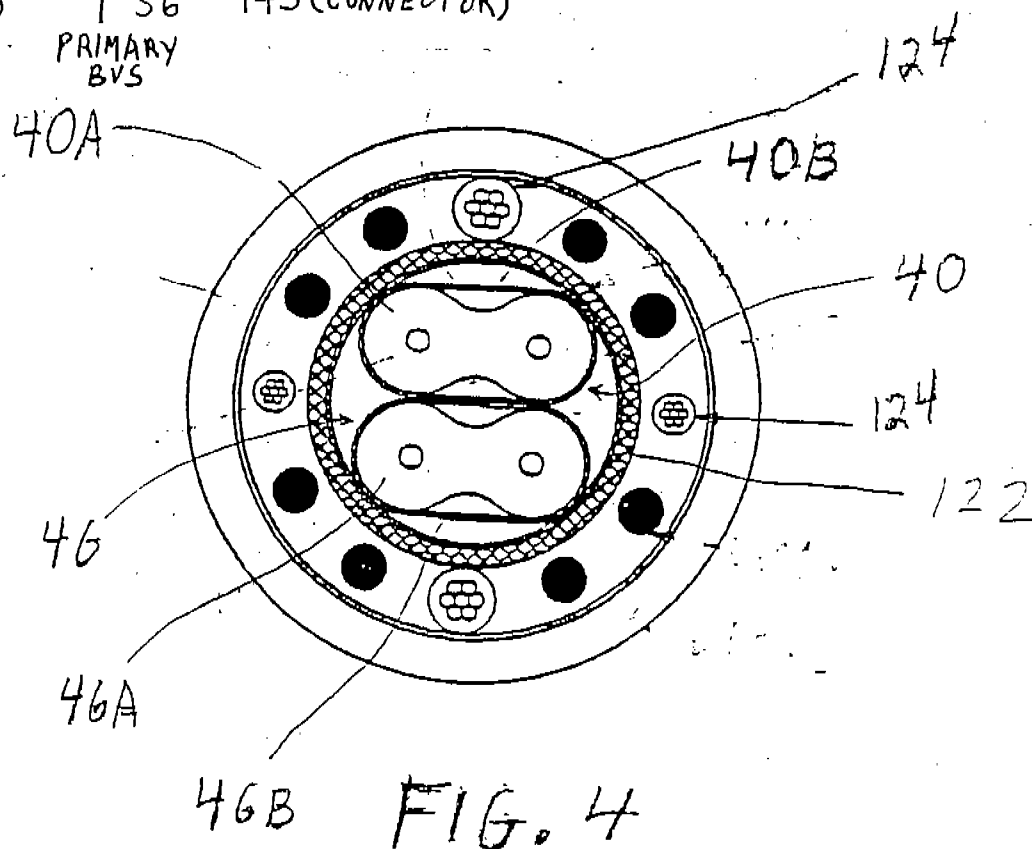
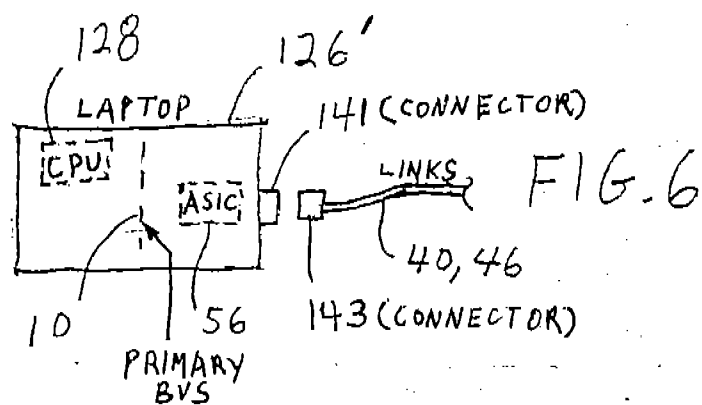
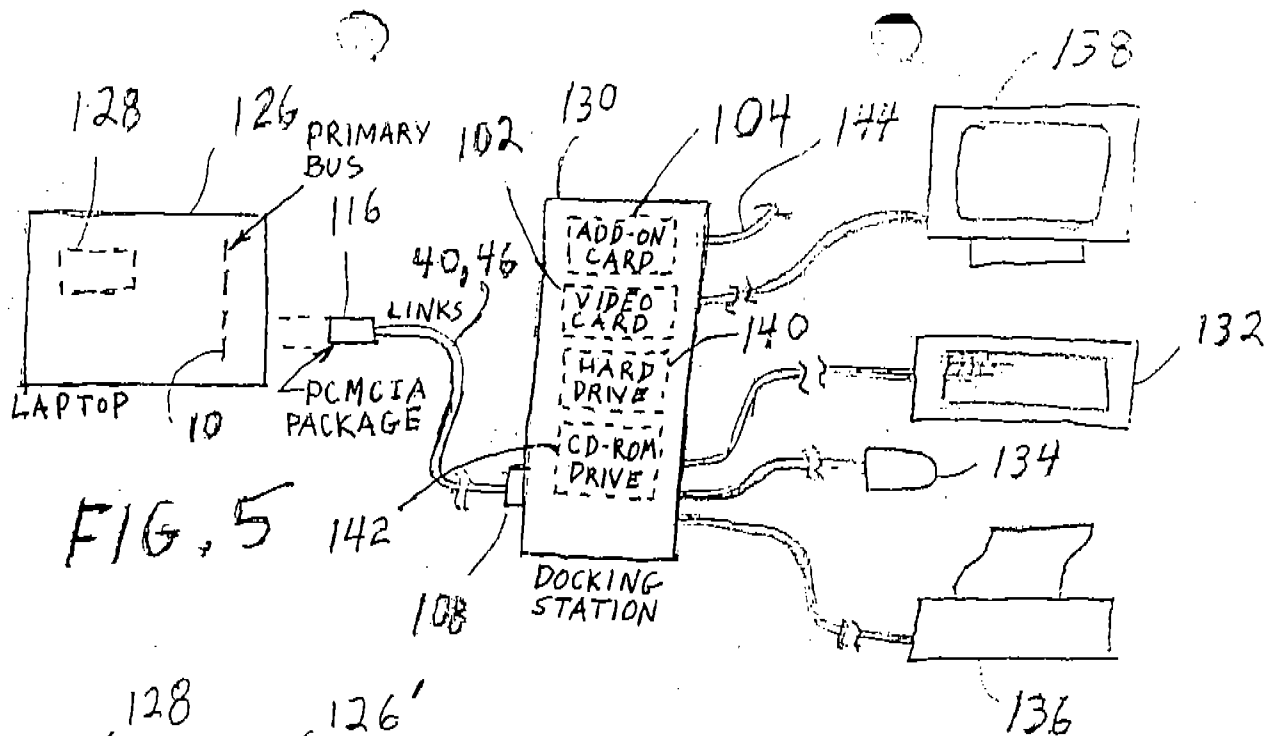


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FIG. 3



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SL

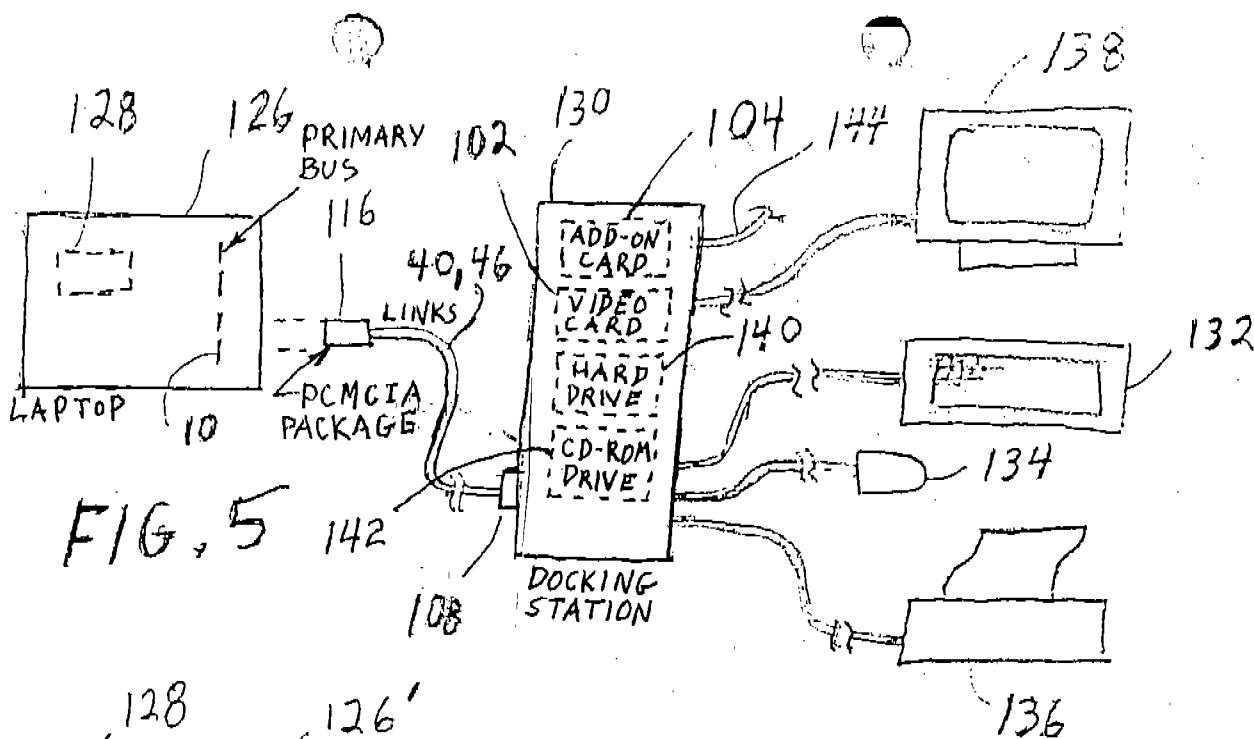


FIG. 5

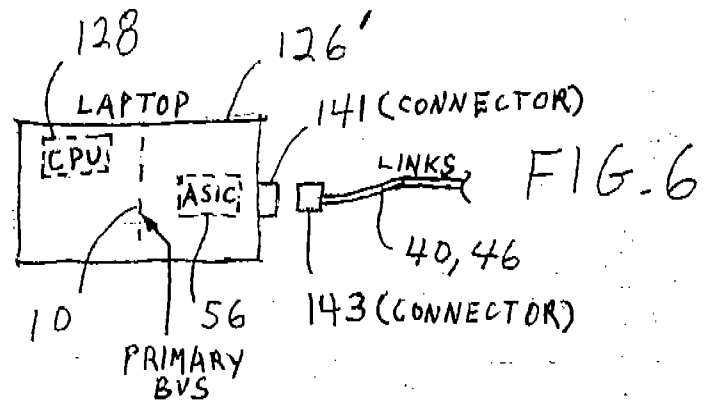


FIG. 6

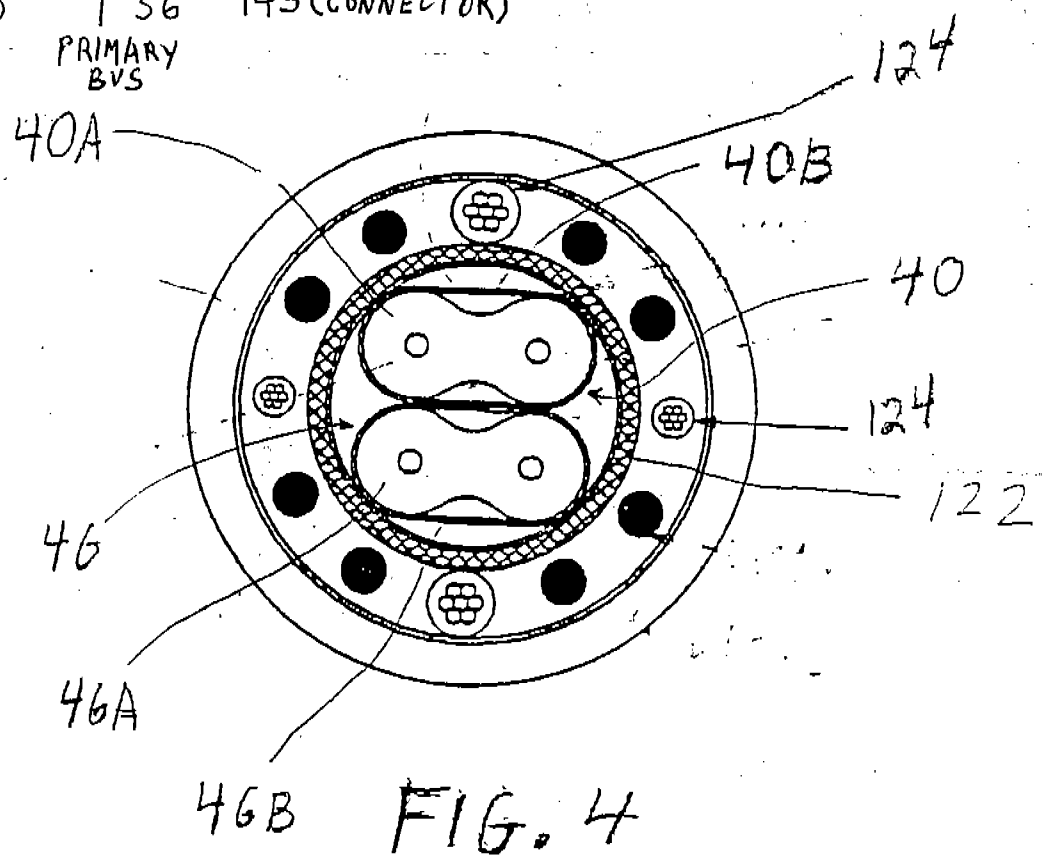


FIG. 4

Approved
2/8/00
SL



781 *[Signature]*

Atty File: DOS14

In re Application of: Frank Ahern

Serial No.09/130,058
Filed: 08/06/98
For: LINKED BRIDGE

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

RECEIVED
JAN - 3 2000
TECH CENTER 2700

Transmitted herewith is an amendment in the above identified application.
Small entity status of this Application under 37 CFR 1.9 and 1.27 has been
established by a Verified Statement previously submitted.

The fee is calculated as follows:

	Total	Independent
No. of Claims Paid for:	59	2
No. of Claims After Amendment:	81	3
No. of Extra Claims	22	1
Additional Fee:	198	39
Terminal Disclaimer		55
Late Fee:		190
TOTAL ADDITIONAL FEE:		482

My check in the amount of \$482.00 is enclosed.

[Signature]
THOMAS L. ADAMS
Reg No. 27,300

Dated: 12/20/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

Serial No: 09/130,058

Filed: 08/06/98

Title: LINKED BRIDGE



Atty. Docket: DOS14

Group Art Unit: 2781

Examiner: Sumati Lefkowitz

10 Park Place
Morristown, NJ
December, 1999

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

SIR:

FIRST AMENDMENT TO APPLICATION

Responsive to the Office Action mailed July 21, 1999, to which a response is due October 21, 1999 (extension fee of \$190.00 enclosed), please amend the above identified application as follows:

IN THE DRAWINGS:

Please replace the originally filed drawings with the enclosed four sheets of informal drawings.

TERMINAL DISCLAIMER:

Please file the enclosed Terminal Disclaimer for which a filing fee of \$55.00 is enclosed.

TITLE:

Please amend the title to "Serially Linked Bus Bridge for Expanding Access over a First Bus to a Second Bus."

#8/A

LOT

1-6-00

entered

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JAN - 3 2000

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12/29/1999 00000068 09130058

07 12/29/99
23 11/29/99

IN THE CLAIMS:

In claim 2, delete "means" from lines 1 and 2, and delete "bus-related" from line 2.

In the third lines of claims 3, 13, 32 and 42, delete "means".

In the second lines of claims 4, 8, 11, 33, 37 and 40, delete "means".

Delete "means" in the first lines and delete "bus-related" in the fourth lines of claims 5, 6, 34 and 35.

In the first lines of claims 7, 10, 28, 29, 36, 39, 57 and 58, delete "means".

In lines 1, 3, 4 and 5 of claim 9, delete "means".

In claim 12 delete "means" from lines 1 and 2, and in line 2 change "secondary" to -- second --.

In the first lines and the second lines of claims 14, 15, 30, 43, 44 and 59, delete "means".

In the fifth lines of claims 17 and 46, and delete "means".

In the third lines of claims 18 and 47, delete "means" (second occurrence).

In the second lines and third lines of claims 19, 20, 48 and 49, delete "means".

In the third lines of claims 21 and 50 delete "means" (both occurrences).

In lines 1, 3, 4 and 5 of claim 38, delete "means".

In claim 41 delete "means" from lines 1 and 2, and in line 2 change "secondary" to -- second --.

Please amend claims 1 and 31, as follows:

1. (amended once) A bridge accessible by a host processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, allowable ones of said devices including memory devices and input/output devices, said bridge comprising:

a link;

a first interface [means] adapted to couple[d] between said first bus and said link; and

A1 a second interface [means] adapted to couple[d] between said second bus and said link, said first interface [means] and said second interface [means] operating as a single bridge and being operable to (a) send outgoing, [bus-related] information serially through said link in a format different from that of said first bus and said second bus without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said information over said link, (b) approve an initial exchange between said first bus and said second bus in response to pending bus transactions having a characteristic signifying a destination across said bridge, and (c) allow said host processor, communicating through said first bus, to individually address different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices on said first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus.

31. (amended once) A bridge accessible by a host processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, allowable ones of said devices including memory devices and input/output devices, said bridge comprising:

a link;

a first interface [means] adapted to couple[d] between said first bus and said link; and

12 a second interface [means] adapted to couple[d] between said second bus and said link, said first interface [means] and said second interface [means] operating as a single bridge and being operable to (a) send outgoing, [bus-related] information serially through said link in a format different from that of said first bus and said second bus, (b) exchange [bus-related] information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus, and (c) allow said host processor, communicating through said first bus, to individually address different selectable ones of the bus-compatible devices on said second bus, including memory devices and input/output devices that may be present: (i) using on said first bus substantially the same type of addressing as is used to access devices on said first bus, [and] (ii) without first employing a second, intervening one of the bus-compatible devices on said second bus, and (iii) without passing the information through an intervening hierarchical level.

Please add new claims 60-81, as follows:

60. (new) A bridge accessible by a processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, said bridge comprising:

a link;

a first interface coupled between said first bus and said link; and

a second interface adapted to couple between said second bus and said link, said first interface and said second interface operating as a single bridge and being operable to transfer information serially through said link in a format different from that of said first bus and said second bus without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said information over said link.

61. (new) A bridge according to claim 60 wherein said first interface and said second interface are operable to exchange information between said first bus and said second bus according to a predetermined hierarchy giving said first bus a higher level than said second bus.

62. (new) A bridge according to claim 60 wherein said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a

pending transaction on said first bus to begin processing said pending transaction and to apply a retry signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus.

63. (new) A bridge according to claim 62 wherein less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link.

64. (new) A bridge according to claim 60 wherein said first interface is selectively responsive to those addresses appearing on said first bus that are on a predetermined schedule of addresses corresponding to the bus-compatible devices accessible through said second bus, in order to avoid responding to addresses corresponding to other ones of the bus-compatible devices on said first bus.

65. (new) A bridge according to claim 64 comprising:
a register for storing said predetermined schedule.

66. (new) A bridge according to claim 64 wherein said first interface comprises:

a first register for storing said predetermined schedule, said second interface comprising:

a second register for storing said predetermined schedule.

67. (new) A bridge according to claim 65 wherein said register is operable to establish with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

68. (new) A bridge according to claim 60 comprising:

a register for establishing with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus.

69. (new) A bridge according to claim 60 wherein said first interface and said secondary interface are operable to permit communication between bus-compatible devices on said second bus without routing through said first bus.

70. A bridge according to claim 60 wherein said first interface and said second interface comprise:

a first and a second programmable logic device connected between said link and said first bus and said second bus, respectively.

71. (new) A bridge according to claim 60 wherein said first interface and said second interface comprise:

a first and a second application-specific integrated circuit connected between

said link and said first bus and said second bus, respectively.

72. (new) A bridge according to claim 71 wherein said first and said second application-specific integrated circuit are identically structured and each have a control pin for receiving a control signal to establish operation in one of two modes.

73. (new) A bridge according to claim 71 wherein said first and said second application-specific integrated circuit each comprise:

a plurality of ports coupled to said second interface for providing input/output.

74. (new) A bridge according to claim 60 wherein said processor is interrupt-driven, said second interface being operable to transmit through said link to said first interface interrupt signals destined to interrupt the processor.

75. (new) A bridge according to claim 74 wherein said processor is responsive to error signals, said second interface being operable to transmit through said link to said first interface error signals destined to affect the processor.

76. (new) A bridge according to claim 60 wherein said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface and said second interface at a bit transfer rate greater than said predetermined clock speed.

77. (new) A bridge according to claim 76 wherein said link comprises:
a pair of simplex links for sending information in opposite directions..

78. (new) A bridge according to claim 77 wherein said simplex links are driven
for differential signal transfers.

79. (new) A bridge according to claim 60 wherein said second bus comprises
a PCI bus.

80. (new) A bridge according to claim 60 wherein said second interface is
operable in response to a transaction from said link signifying an initial read request,
to fetch and pre-fetch data from a competent one of the bus-compatible devices on
said second bus for transmission back over said link in order to satisfy pending and
anticipated transactions.

81. (new) A bridge according to claim 60 wherein said first interface and said
second interface are operable to permit at least one of the bus-compatible devices on
said second bus to address one or more of the bus-compatible devices on said first bus
using on said second bus substantially the same type of addressing as is used to
access devices on said second bus.

REMARKS

The enclosed marked copies of Figures 1, 2, 3, 5 and 6 were labeled with textual information as requested.

The title suggested by the Examiner was adopted.

Claims 12 and 41 were amended as suggested by the Examiner. Applicant sincerely appreciates the effort taken by the Examiner to find these informalities.

The Examiner provisionally rejected all claims under the judicially created doctrine of obviousness-type double patenting, citing certain claims of Applicant's co-pending application No. 09/130,057, in view of U.S. Patent 5,764,924 (Hong), and U.S. Patent 5,819,053 (Goodrum). The Examiner also provisionally rejected claims 5, 6, 34, and 35 under the same doctrine, citing a different group of claims from the same co-pending application, in view of U.S. Patent 5,522,050 (Amini). As suggested, Applicant encloses a terminal disclaimer under 37 CFR 1.321(c) in order to avoid the double patenting rejection.

The Examiner rejects claims 1-4, 7-17, 19-23, 27-33, 36-46, 48-52 and 56-59 under 35 U.S.C. 103(a), citing Hong in view of Goodrum. The Examiner also rejects claims 5, 6, 34, and 35 under 35 U.S.C. 103(a) citing Hong in view of Goodrum, and further in view of Amini. Claims 18 and 47 were rejected under 35 U.S.C. 103(a) as unpatentable over Hong, in view of Goodrum, and further in view of U.S. Patent 5,799,207 (Wang). Claims 24, 26, 54, and 55 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, in view of Goodrum, and further in view of U.S. Patent 5,483,020 (Hardie). Finally, claims 25 and 53 were rejected under 35 U.S.C.

103(a) as being unpatentable over Hong, in view of Goodrum, and further in view of U.S. Patent 5,809,262 (Potter). None of the other references were applied against any claims.

PRESENT DISCLOSURE

The present system facilitates the exchange of information between buses that may be separated by a moderate distance. For situations where buses are very close, some known systems make the connection with a single bridge or no bridge. See the present specification at page 3, line 28 through page 4, line 2. This approach will work if the bus is not too long and it has very light loading. Synchronization problems will arise, however, with even a moderate separation. If any cable that is not exceedingly short constitutes a bus with devices at either end, the loading of just a few devices combined with the transmission line effects will prevent the devices from responding to each other promptly enough to satisfy industry-wide specifications on such bus transactions.

One work-around approach taken by the prior art is to reduce the loading on the cable to two loads: two bridges at either end of a parallel interface. See page 3, lines 15-26 of the present specification. These parallel systems still have synchronization problems arising from the propagation delay along the parallel interface. The prior art has tried to deal with this problem (see the present specification at page 3, lines 15-26) by using a local clock only after it has been delayed by an amount equivalent to the expected delay along the parallel interface.

In any event, all of these approaches suffer from the disadvantage of using a

parallel interface requiring a large number of lines including additional lines for one or more clock signals.

The present invention avoids these difficulties by using a single bridge that can send information through a link in a serial fashion. A conventional way to establish a serial connection with decent bandwidth is a protocol-heavy, network connection under a standard like the Ethernet standard (although many other standards exist). While these protocol-heavy connections can solve the synchronization problems arising with conventional parallel interfaces, these solutions create different problems. These protocols introduce substantial delays by employing handshaking techniques for opening a communications channel and for avoiding collisions. Protocol-heavy networks also strive to maintain a high degree of adaptability, but at the cost of employing frames with complicated headers for specifying the length of the frame, etc.

The present serial system takes a more hardware-oriented approach, and overcomes the problems with protocol-heavy network solutions and with double bridges that employ a parallel interface. The presently disclosed system can examine incoming information on bus 10 before accepting it (Figures 1 and 2). However once the information is accepted, it is immediately serialized and sent across link 40, 46. See for example, page 18, lines 9-21. Assuming the interface 16 is not occupied with a previously received transaction, an attempt is made without delay to drive this newly arrived information onto bus 12. Page 18, lines 23-28. The same can be said for a reverse flow of information from bus 12 to bus 10. This is an entirely different approach than a networking solution involving complicated acknowledgement frames.

Also, the present system recognizes that the use of double bridges can itself cause special problems. For this reason, interfaces 14 and 16 (Figure 1), and the link between them, act as a single bridge. Thus, the apparatus on opposite sides of cables 40 and 46 may each be considered a half bridge.

Important and practical problems are avoided by employing a single bridge. For example, before a processor in a personal computer uses any of its resources, it will typically perform an enumeration process to identify the hardware available at various levels in a hierarchy. Some conventional enumeration processes will not cross the extra bridge to find certain hardware, such as VGA adapters.

Typically during enumeration, software will determine the existence of each bridge and its place in the hierarchy by examining its configuration register. As an example, this function of a configuration register is specified in the PCI bus standard referenced in the present specification on page 1, lines 29-30.

The present system makes certain that it appears as a single bridge, not double bridges on different hierarchical levels. For this purpose, the present system has only one unique configuration register, and therefore configuration software will "see" only one bridge at a single hierarchical level. Specifically, the disclosed bridge has matching configuration registers 67 and 68. Register 67 is simply a mirror of information on register 68 and is provided to meet critical timing of local transactions. See page 13, lines 18-21. With only one unique configuration register, this system will appear as a single bridge.

HONG

This reference uses a protocol-heavy serial connection between two distinct bridges: local serial bridge 104 and remote serial bridge 114 (Figure 9). This protocol uses complicated data packetizing techniques to manage information transfer. Thus this reference manages to take the worst of both worlds by taking the disadvantages of a protocol-heavy communications solution, as well as the disadvantages of a double bridge solution.

Time-consuming handshaking takes place between these two bridges. Figure 5 shows that after a requesting bridge sends a request frame, the responding bridge sends a separate acknowledgment frame, before sending its response frame. The requester then actually acknowledges the response. See column 7, lines 38-39 and lines 45-48.

The specific procedure followed in Hong when a bridge first receives such a request over the serial link is described in the flow chart of Figure 7A. First, the bridge detects a flag and decodes the subsequent header to determine the packet type in steps 500 and 502, before sending an acknowledgement in step 526. Accordingly, the link can be "busy" with traffic caused by the return of such acknowledgements. Consequently, critical information (for example, the return of responsive data) may be delayed by the regular transmission of acknowledgements. See also column 9, lines 26-30. Moreover, Hong employs a fixed delay that is invoked before sending an acknowledgement (column 9, lines 23-24), thereby exacerbating the bottleneck.

Tables 3 and 4 show the frame format for information sent over Hong's serial

link. The first 16-bits are dedicated to providing a flag for the beginning of the frame. The next 16 bits are dedicated to a header that indicates: (1) the packet type (request, response, or acknowledgement), (2) one of many possible operational codes, (3) PCI address length (or designator for flush command), (4) PCI data length (or APIC commands), (5) a transaction identification number, and (6) parity bits. The subsequent data payload can be either 48, 96, or 384 bits long, as specified in the header. In cases where the bridges are sending a long burst of data, the above frame will be unable to contain the entire burst. Therefore, acknowledgements will be sent repeatedly during the course of a single burst, thereby causing further traffic congestion.

Hong also suffers from disadvantages inherent with double bridges. Figure 9C of this patent shows two separate bridges: local serial bridge 104 and remote serial bridge 114. Hong's specification describes bridges 104 and 114 being handled as separate bridges, and describes how each separately and independently follows the PCI specification. For example at startup, different bus numbers are assigned to the buses served by these bridges, including the bus between the two bridges. See column 13, line 22, through column 14, line 49. Specifically, the secondary bus of local serial bridge 104 is identified as bus 1, while the secondary bus of remote serial bridge 114 is identified as bus 2. As a result, this additional logical bus, required by the extra bridge can cause a conventional enumeration process to fail to find important hardware downstream of the second bridge.

GOODRUM

This reference employs two separate bridges and a parallel interface. See column 6, lines 8-11; column 57, lines 57-60; and column 58, lines 43-49. Thus, Goodrum is another example of the prior art described on page 3, lines 15-26 in the introduction of the present specification. Thus, this reference has the problems of double bridges, as well as having a cable with many lines, including extra lines to deal with the synchronization problem.

Goodrum's cable 28 (Figure 3) has 50 pairs of shielded cables for providing parallel data transmission. See column 57, lines 57-60; and column 58, lines 43-49. (Expanding on the multiplexing used in the PCI standard, Goodrum multiplexes 60-bit message frame into three 20-bit frames, transmitting each twenty-bit frame as a parallel transaction.)

To deal with the synchronization problem, Goodrum sends two clock signals in opposite directions through the link between the bridges. See column 6, lines 23-37; and column 52, lines 1-8. Basically, the upstream clock is sent by the upstream bridge through line CABLE_CLK1 (Figure 5) and then through buffers 179 and 181 to synchronize phase locked loop 180 in the downstream bridge. This phase locked signal is then sent along line CABLE_CLK2 back to the upstream bridge.

Again, running with two separate bridges creates typical problems. Goodrum assigns a separate bus number to the logical bus between the two bridges. See column 98, lines 49-59. Following the PCI standard, Goodrum runs a type 0 configuration transaction on bus 24 to access the configuration space in configuration

register 105. A type 1 transaction is run on bus 24 to access configuration register 125 in the second bridge. See column 98, lines 23-59.

Goodrum goes so far as to describe the difficulties one would experience attempting to treat these two separate bridges as if they were one. See column 98, lines 8-22. According to Goodrum, the BIOS configuration routine would need to be modified so that the double bridges could be treated differently at different times. That modified BIOS configuration routine could produce unexpected results and is an approach that ought to be avoided. A larger problem with this "dual personality" approach is that the modified BIOS of the host computer must give up its compatibility with other systems in order to gain compatibility with Goodrum's system.

Overall, Goodrum is a completely different system, which lacks a serial link, and which employs two bridges instead of one. Goodrum has problems typical for double bridge systems. Of course, Goodrum has the disadvantage of requiring multiple parallel lines, including extra clock lines.

AMINI

The Examiner cites Amini simply to show a system allegedly having FIFO registers in a bridge. Amini is otherwise Irrelevant. For example it lacks a bridge having a serial link for communicating between two buses.

WANG

The Examiner cites Wang simply to show a system allegedly having "a plurality of port means ... for providing a plurality of ports for input/output." Wang is otherwise irrelevant. For example it lacks a bridge having a serial link for communicating

between two buses.

HARDIE

The Examiner cites Hardie simply to show "a cable with twin axial lines." Hardie is otherwise irrelevant. It is unconcerned with bridges.

POTTER

The Examiner cites Potter simply to show a system allegedly having "a twisted pair." Potter is otherwise irrelevant. For example it lacks a bridge having a serial link for communicating between two buses.

CLAIM ANALYSIS

None of the cited prior art show a single bridge containing a serial link for communicating between two buses. To emphasize this distinction, independent claims 1 and 31, were amended to recite: "said first interface and said second interface operating as a single bridge and being operable to ... send outgoing, bus-related information serially through said link." New claim 60 has the same recitation. None of the cited art show this feature.

Both Hong and Goodrum show communications through a pair of bridges. Thus, both have problems typical for double bridge systems. For example, an operating system or BIOS will see both bridges and in many cases will not cross the extra bridge when enumerating hardware.

The four other cited references are irrelevant to the independent claims. They are unconcerned with a bridge having a serial link for communicating between two buses.

CLAIM 1

In addition, amended claim 1 identifies features that avoid problems typically arising with conventional network connections. Specifically, claim 1 was amended to recite that the first and second interface will "send outgoing, information serially through said link ... without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said information over said link." See for example page 18, lines 23-28 of the present specification.

As noted above, Hong has separate bridges that require the receipt of an acknowledgement frame before data is sent. In the case of a long burst of data, Hong will periodically interrupt that data flow in order to send an acknowledgement frame. These delays are a consequence of Hong's protocol-heavy approach (complicated frames with flags and headers) and the failure to recognize the possibility of employing a single bridge.

Goodrum is a parallel interface and therefore is not in the same category. Regardless, Goodrum fails to "send outgoing, bus-related information serially through said link ... without waiting for an incoming acknowledgment over said link before inaugurating a transfer over said link," as recited in amended claim 1. Goodrum does not send any serial information at all.

The four other cited references are unconcerned with serial transfers of this type and are therefore irrelevant.

CLAIM 31

In addition, independent claim 31 was amended to recite features that avoid problems typical with double bridge arrangements. Specifically, amended claim 31 recites that the first and second interface "allow said host processor ... to individually address different selectable ones of the bus-compatible devices on said second bus ... without passing the bus-related information through an intervening hierarchical level." As noted before, the present system of Figure 1 operates as a single bridge. Configuration registers 67 and 68 mirror each other, so that a processor will see a single bridge across a single hierarchical level. See the present specification at page 13, lines 18-21.

In contrast, Goodrum has a parallel interface connecting between two separate bridges. See column 6, lines 8-11 of Goodrum. In a typical fashion, Goodrum assigns a separate bus number to the logical bus between the two bridges. See column 98, lines 49-59; and column 98, lines 23-59.

Likewise, Hong shows in Figure 9C different bus numbers assigned to the buses served by the two bridges, including the bus between the two bridges. See column 13, line 22, through column 14, line 49. Specifically, the secondary bus of local serial bridge 104 is identified as bus 1, while the secondary bus of remote serial bridge 114 is identified as bus 2.

Thus, both Hong and Goodrum will have problems typical for double bridge systems. For example, an operating system or BIOS will see both bridges and in many cases will not cross the extra bridge when enumerating hardware.

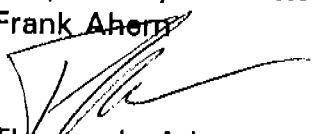
The four other cited references are unconcerned with serial transfers of the type defined in amended claim 31. Therefore, whether these other references show one or two bridges, they are irrelevant.

CONCLUSION

All other claims depend from independent claims 1, 31 and 60 and therefore distinguish over the cited art for at least the reasons given in connection with those claims.

It is believed that the foregoing fully responds to the objections and rejections entered by the Examiner and places this application in condition for allowance, which action is respectfully requested.

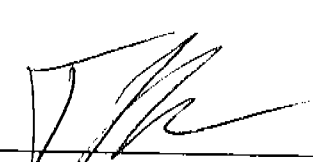
Respectfully submitted,
Frank Ahern



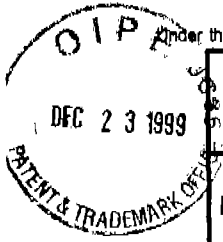
Thomas L. Adams
Registration No. 27,300

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on this 20th day of December, 1999.



Thomas L. Adams
Registration No. 27,300



#9
JCM
1-8-00

TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING SECOND APPLICATION		Docket Number (Optional) DOS14
In re Application of: Frank Ahern Application No. 09/130,058 Filed: 08/06/98 For: LINKED BRIDGE Mobility The owner*, <u>Electronics, Inc.</u> of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 to 156 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent granted on pending second Application Number <u>09/130,057</u> , filed on <u>08/06/98</u> . The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the second application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of any patent granted on the second application, as shortened by any terminal disclaimer filed prior to the patent grant, in the event that any such granted patent: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims cancelled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant. Check either box 1 or 2 below, if appropriate. 1. ☐ For submissions on behalf of an organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the organization. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. 2. ☒ The undersigned is an attorney of record.  Signature 12/20/99 Date Thomas L. Adams, Reg. No. 27,300 Typed or printed name ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included. *Certification under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.		

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**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231 *RW*

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/130,058	08/06/98	AHERN	F DOS14

THOMAS L ADAMS
10 PARK PLACE
MORRISTOWN NJ 07960

LM02/0225

EXAMINER

LEEQUITTZ
ART UNIT PAPER NUMBER

2781

10

DATE MAILED:

02/25/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to telephone conversation of 2/15/00

☒ The allowed claim(s) is/are 1-81

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. 6

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☒ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

Ayaz R. Sheikh
AYAZ R. SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2700

IPR2023-00842

EX. 2003

Page 130 of 145



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

NW

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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09/130,058 08/06/98 AMERN

F DOS14

EXAMINER

LM02/0225

THOMAS L. ADAMS
10 PARK PLACE
MORRISTOWN NJ 07960

ART UNIT	PAPER NUMBER
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2781

DATE MAILED:

02/25/00

INTERVIEW SUMMARY

All participants (applicant, applicant's representative, PTO personnel):

- (1) Thomas L. Adams (#27,300) (3) _____
(2) Sumati Lefkowitz (4) _____

Date of Interview: 2/15/00

Type: ☒ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No If yes, brief description: _____

Agreement ☒ was reached. ☐ was not reached.

Claim(s) discussed: 1, 3, 60

Identification of prior art discussed: 6,003,125 - Vicard et al., 5,696,911 - Frederiksson,
5,671,421 - Kardash et al.

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Applicant's representative was asked to review the above
cited references to confirm that the claims distinguish
over the references. It was agreed, after careful review
of the references, that the claims ~~do~~ do distinguish over
the references.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

1. ☒ It is not necessary for applicant to provide a separate record of the substance of the interview.

Unless the paragraph above has been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a response to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW.

2. ☒ Since the Examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action. Applicant is not relieved from providing a separate record of the interview unless box 1 above is also checked.

Examiner Note: You must sign this form unless it is an attachment to another form.

FORM PTO-892	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. 09/130,058	GROUP ART UNIT 2781	ATTACHMENT TO PAPER NO. 10
NOTICE OF REFERENCES CITED		APPLICANT(S) Ahern		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
*	A	6,003,105	12/1999	Vicard et al.	710	129	
*	B	5,671,421	9/1997	Kardach et al.	710	260	
*	C	5,696,911	12/1997	Fredriksson	710	106	
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER Sumati Lefkowitz	DATE February 16, 2000	Form 892ccs2106b IPR2023-00842
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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

THOMAS L. WATKINS
FOOTBALL PLAYERS
REGISTERED TRADEMARK

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/01,000	05/06/88	101	LEBRONITE, S.	05/25/90
First Named Applicant	THOMAS L. WATKINS, JR. OF ONE INVENTOR FORM ONLY			

TITLE OF INVENTION: FOOTBALL PLAYERS REGISTERED TRADEMARK

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
00014	21-132,000	000	UTILITY	YES	\$400.00	05/25/90

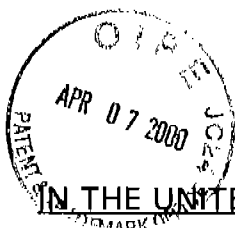
THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT.
PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS
APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
 - If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
 - If the status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:
 - Pay FEE DUE shown above, or
 - File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.
- Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

Atty. Docket: DOS14

Serial No.: 09/130,058

Filed: 08/06/98

For: LINKED BRIDGE

10 Park Place
Morristown, N.J.
April, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231
Attn: Official Draftsperson

Dear Commissioner:

Please review and file the enclosed drawings in place of those originally filed.

Respectfully submitted,
Frank Ahern

Thomas L. Adams

TLA/kc
Enclosure

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the 4th day of April, 2000.

Thomas L. Adams, Esq.
Registration No. 27,300

6070214

FIG. 1

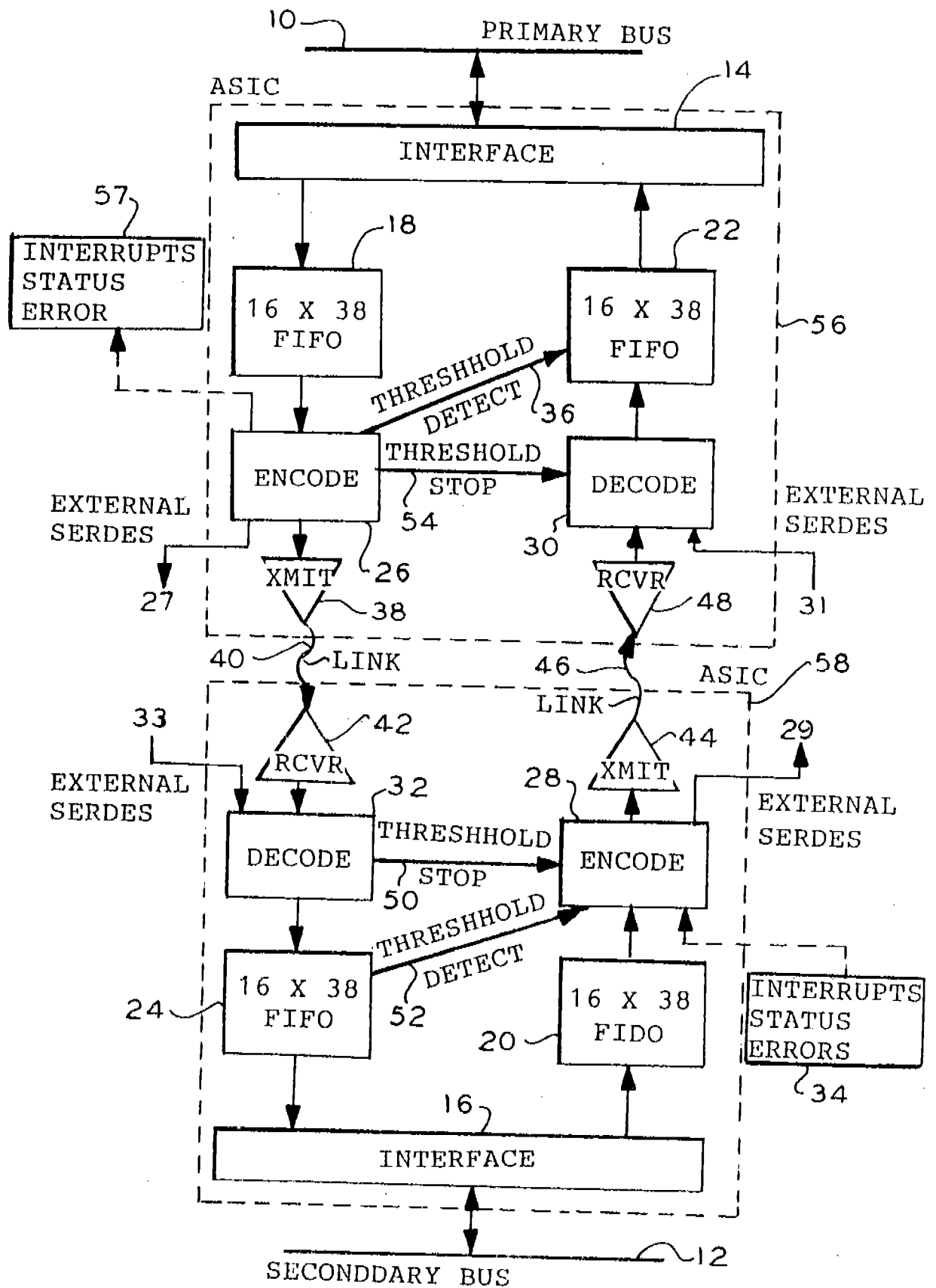
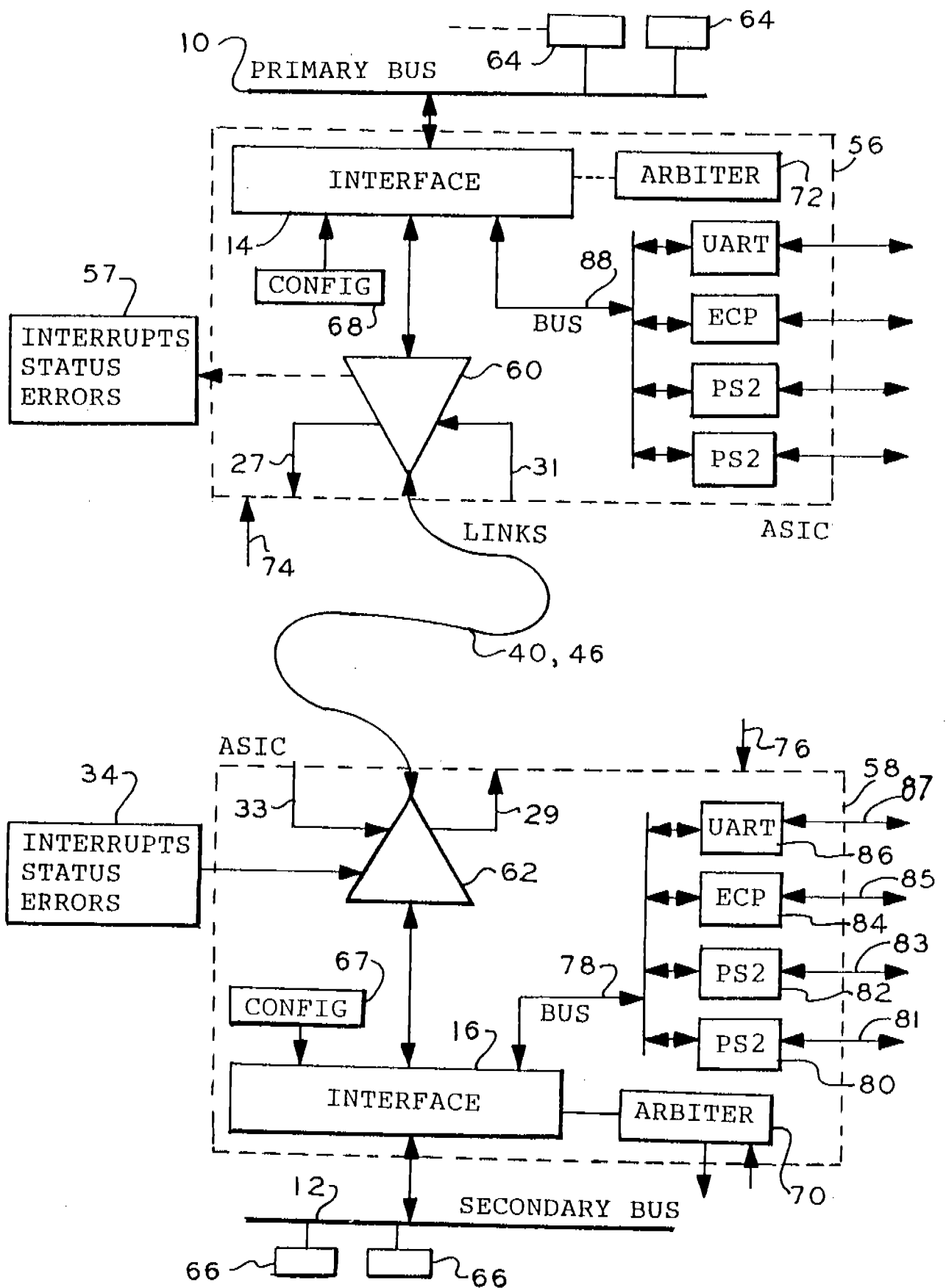


FIG. 2



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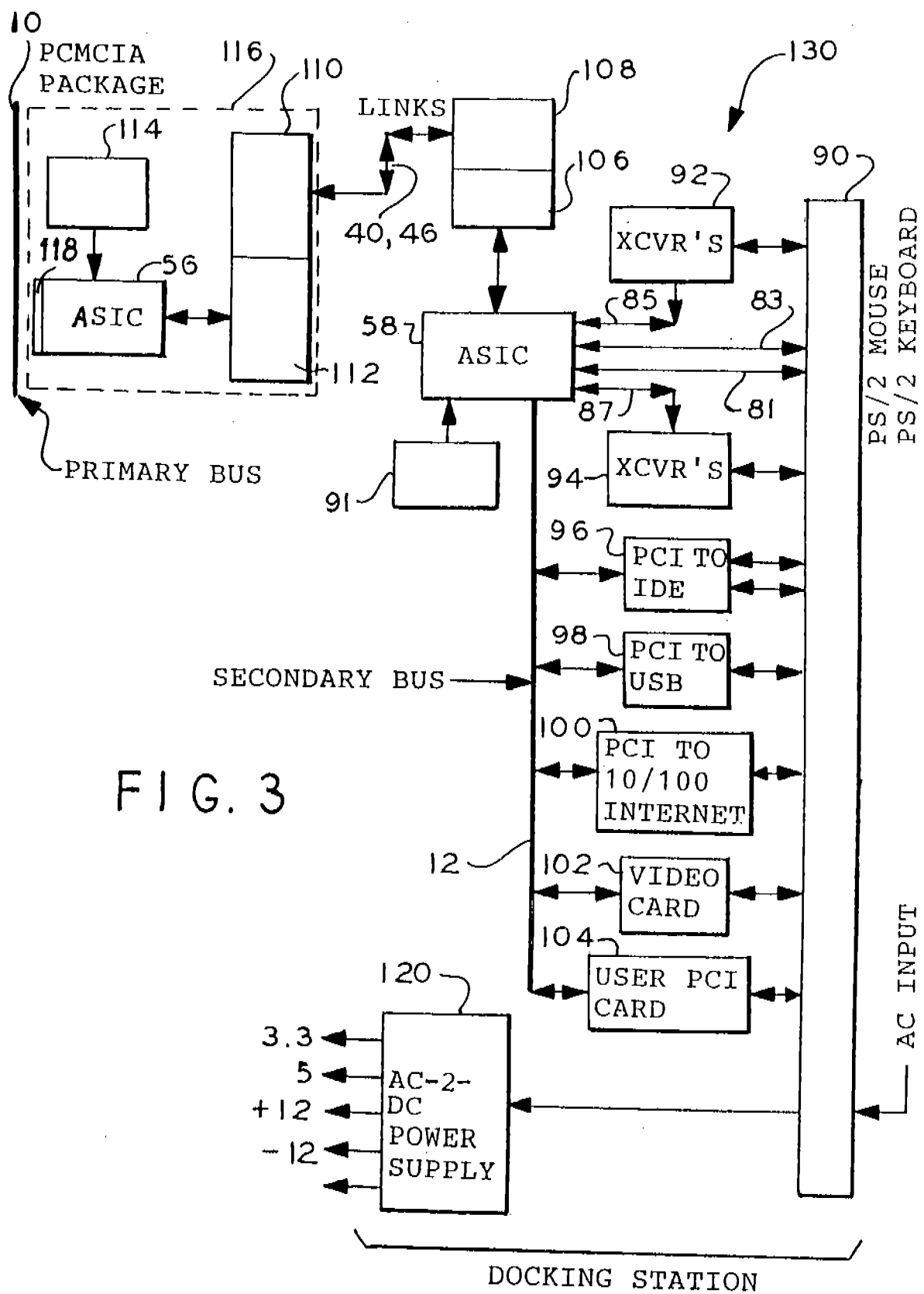


FIG. 3

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FIG. 5

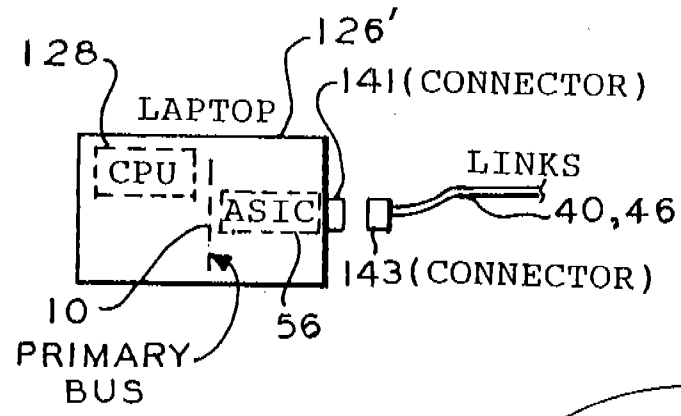
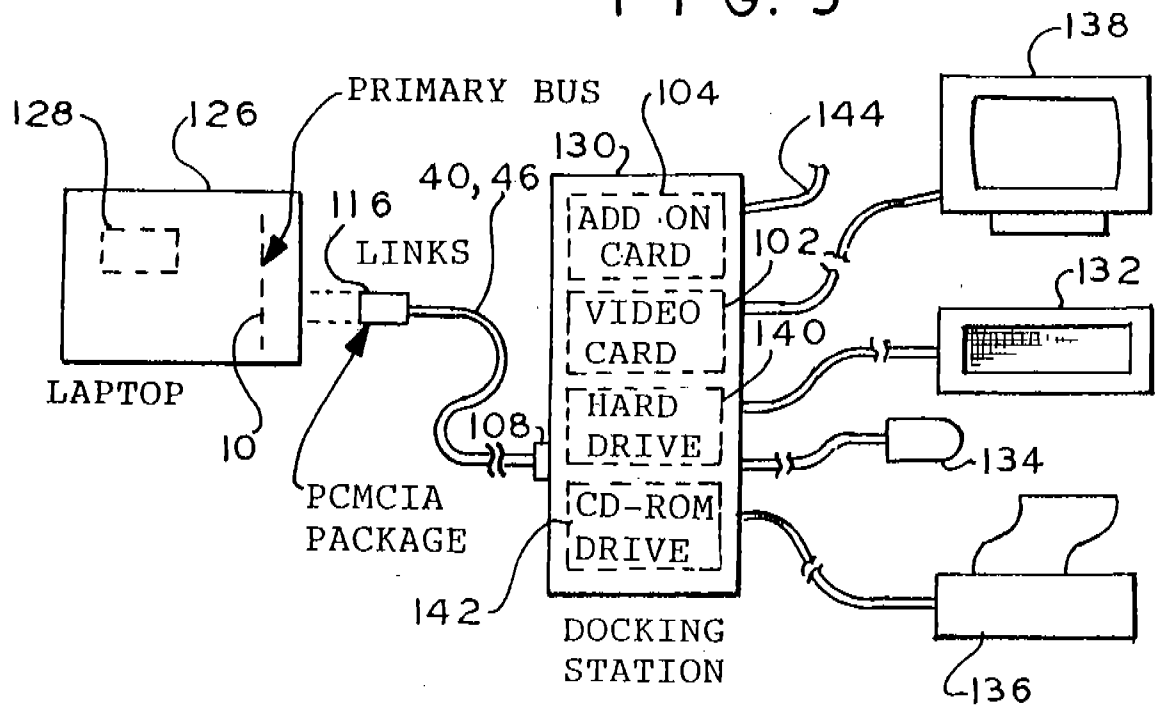
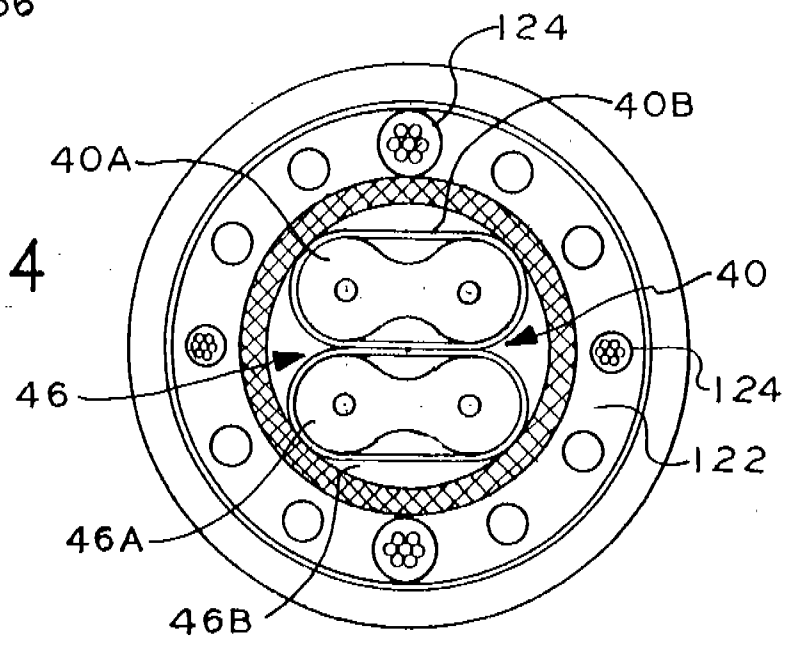


FIG. 6

FIG. 4



+

OMRI M. BEHR
THOMAS L. ADAMS

GERALD J. WEISER
PETER J. GAYLOR
GABRIEL LOPEZ
OF COUNSEL

*PA BAR ONLY
*D.C. BAR ONLY



LAW OFFICES
BEHR & ADAMS
10 PARK PLACE
MORRISTOWN, NEW JERSEY 07960
FACSIMILE: (973) 538-7724
TELEPHONE: (973) 538-4112
<http://www.newidea.com>
E-mail: adams@newidea.com

April 5, 2000

EDISON OFFICE
—
325 PIERSON AVENUE
EDISON, N.J. 08837
(732) 464-5240
CABLE: BEPAT EDISON, N.J.
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ASSOCIATE OFFICE
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PHILADELPHIA, PA 19102
(215) 875-9383

PLEASE REPLY TO MORRISTOWN

BOX ISSUE FEE

Assistant Commissioner for Patents
Washington, D.C. 20231

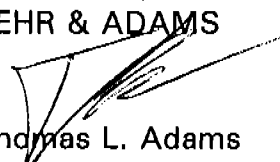
Re: Serial No. 09/130,058
Filed: 08/06/98
Class: 710-128.000
Inventor: Frank Ahern
Our File: DOS14
Examiner: S. Lefkowitz
For: Linked Bridge

Dear Sir:

Enclosed are completed form PTOL-85b, together with my business check in the amount of \$614.00 to cover the issue fee and three advance copies of the patent.

The drawings will be sent under separate cover to the Official Draftsman.

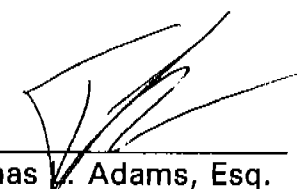
Respectfully submitted,
BEHR & ADAMS


Thomas L. Adams

TLA/kc

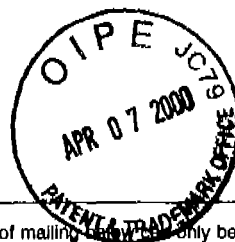
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to : Box Issue Fee, Assistant Commissioner for Patents, Washington, D.C. 20231, on the 5th day of April, 2000.


Thomas L. Adams, Esq.
Registration No. 27,300

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231



MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

THOMAS L. ADAMS
10 PARK PLACE
MORRISTOWN NJ 07960

LM02/0225

Note: The certificate of mailing may only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Thomas L. Adams, Esq. (Depositor's name)
[Signature] (Signature)
4/5/00 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/130,058	08/06/98	081	LEFKOWITZ, S	2781 02/25/00
First Named Applicant	AHERN, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION: **SERIALLY LINKED BUS BRIDGE FOR EXPANDING ACCESS OVER A FIRST BUS TO A SECOND BUS**

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 POS14	710-128.000	299	UTILITY	YES	\$605.00	05/25/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.303). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Thomas L. Adams, Esq.
Reg. No. 27,300

2. _____

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Mobility Electronics, Inc.

(B) RESIDENCE: (CITY & STATE OR COUNTRY)

7955 E. Redfield Road, Scottsdale, AZ 85260

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ Corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee

☒ Advance Order - # of Copies 3

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER _____
(ENCLOSE AN EXTRA COPY OF THIS FORM)

☐ Issue Fee

☐ Advance Order - # of Copies _____

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature)

(Date)

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IPR2023-00842

EX. 2003

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TRANSMIT THIS FORM WITH FEE



MELLON MAR 25 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Ahern

Patent No.: 6,070,214

Serial No.: 09/130,058

Examiner: Ayaz R. Sheikh

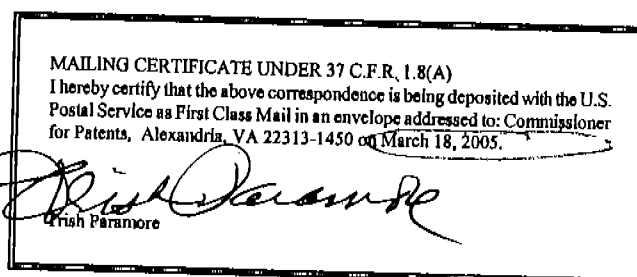
Filed: August 6, 1998

Docket: 101950.00054

For: Serially Linked bus Bridge for Expanding Access over a First Bus to a Second Bus
Notification of Loss of Small Entity Status Under 37 CFR 1.27 (g)(2)

March 18, 2005

Commissioner For Patents
Alexandria, VA 22313-1450



03/31/2005 DALLEN 00000032 6070214

01 FC:2551 Sir: 455.00 OP
02 FC:2554 65.00 OP

Notice is hereby provided that small entity status is no longer appropriate for this issued patent.

GOVERNMENT FEES	DATE PAID	AMOUNT PAID	AMOUNT DUE PAID HEREWITH
Maintenance Fee	May 27, 2004	\$445.00	\$ 445.00

A check for \$445.00 is enclosed. The Assistant Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1752.

Adjustment dates 03/31/2005 DALLEN
06/02/2004 RANDBTMF 00000937 6070214
01 FC:2551 -455.00 OP
02 FC:2554 -65.00 OP

Respectfully Submitted,

Robert C. Klinger
Reg. No. 34,365
Attorney for Applicant

Jackson Walker L.L.P.
2435 North Central Expressway, Suite 600
Richardson, Texas 75080
(972) 744-2902
(972) 238-3302 - Fax

03/31/2005 DALLEN 00000033 6070214

01 FC:1559 445.00 OP





UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Paper No. 13

JACKSON WALKER
2435 NORTH CENTRAL EXPRESSWAY
SUITE 600
RICHARDSON, TX 75080

COPY MAILED

JUN 15 2005

OFFICE OF PETITIONS

In re Patent No. 6,070,214 :
Issue Date: May 30, 2000 :
Application No. 09/130,058 : NOTICE
Filed: August 6, 1998 :
Attorney Docket No. 101950.00054 :

This is a notice regarding your request for acceptance of a fee deficiency submission under 37 CFR 1.28. On September 1, 1998, the Court of Appeals for the Federal Circuit held that 37 CFR 1.28(c) is the sole provision governing the time for correction of the erroneous payment of the issue fee as a small entity. See DH Technology v. Synergystex International, Inc. 154 F.3d 1333, 47 USPQ2d 1865 (Fed. Cir. Sept. 1, 1998).

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. 1098 Off. Gaz. Pat. Office 502 (January 3, 1989). Therefore, nothing in this Notice is intended to imply that an investigation was done.

Your fee deficiency submission under 37 CFR 1.28 is hereby **ACCEPTED**.

Inquiries related to this communication should be directed to Wan Laymon at (571) 272-3220.

This file is being forwarded to Files Repository.

Wan Laymon
Wan Laymon
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Pocket Number

09130058

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY
TYPE ☒

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	59 minus 20 =	* 39
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

RATE	FEE
	395.00
x\$11=	429.00
x41=	
+135=	
TOTAL	824.00

RATE	FEE
	790.00
x\$22=	
x82=	
+270=	
TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 81	Minus	** 59	= 22
	Independent	* 2	Minus	*** 3	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE
x\$11=	198
x41=	
+135=	
TOTAL ADDIT. FEE	237

RATE	ADDI- TIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE
x\$11=	
x41=	
+135=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE
x\$11=	
x41=	
+135=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
x\$22=	
x82=	
+270=	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" in this space is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" in this space is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 2.

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EX02003

Page 143 of 145

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	<i>JP</i>		8/11/98
O.I.P.E. CLASSIFIER		15	8/12/98
FORMALITY REVIEW	<i>134</i>	71473	8-19-98

INDEX OF CLAIMS

✓ Rejected
 = ... Allowed
 - (Through numeral) Canceled
 ÷ Restricted
 N Non-elected
 I Interference
 A Appeal
 O Objected

Claim	Final	Original	Date
1	1	7/15/98	
2	2	11/2/98	
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Claim	Final	Original	Date
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Claim	Final	Original	Date
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148	148		
149	149		
150	150		

If more than 150 claims or 10 actions
staple additional sheet here

IPR2023-00842

EX. 2003

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(LEFT INSIDE)

SEARCHED			
Class	Sub.	Date	Exmr.
710	126-130	7/7/99	SL
710	100-102	-7/9/99	
	105-106		
	1,2		
updated search 2/9/00 SL			

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
APS	7/7-7/9/99	SL
Paul Myers, 2781	7/8/99	SL
STN	2/9/00	SL

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
710	129	2/15/00	SL
	128		
	106		