

Exhibit A – Joint Claim Construction Statement

No.	Claim Term	Plaintiff’s Proposed Construction and Evidence	Defendant’s Proposed Construction and Evidence
1	“asynchronously, serially transferring first serial data” ’675 patent claim 7	Not indefinite. No construction necessary, plain and ordinary meaning. If construed, “asynchronously” means “independently of a synchronized timing” If construed, “serially transferring” means “transferring in series” <u>Intrinsic Evidence</u> At least ’675 Pat., Cls. 1, 7, 8, 15, 17; Abstract; Figs. 3, 4; 2:22-5, 3:7-10, 3:15-9, 3:34-7, 3:65-4:4, 4:37-9, 4:49-57, 4:58-5:15, 5:40-4, 5:49-8, 6:26-9, 6:49-57, 7:10-12, 7:39-43, 8:9-16, 9:3-7. ’675 File History (SH00002729 - SH00003087), including at least: 04/19/2011 Applicant Amendment and Remarks (SH00002880-SH00002881); 03/21/2011 Applicant Amendment and Remarks (SH00002907-2911); 11/19/2010 Final Rejection (SH00002930- SH00002939); 10/21/2010 Applicant Amendment and Remarks (SH00002969- SH00002975); 06/21/2010 Non-Final Rejection (SH00002987- SH00002995); Claims (SH00003071- SH00003074).	Indefinite Under 35 U.S.C. 112, first and second paragraph (35 U.S.C. 112(a), (b) – post AIA) The term “asynchronously, serially transferring first serial data,” is indefinite under at least 35 U.S.C. § 112, second paragraph as the term is vague and indefinite. Furthermore, the specification fails to provide sufficient written description of the above noted term. To the extent that the term “asynchronously, serially transferring first serial data” can be interpreted based on the lack of support and clarity within the specification, the following construction is the only possible interpretation based on the limited intrinsic evidence in combination with available extrinsic evidence that could satisfy the requirements of 35 U.S.C. § 112. Proposed Construction Unsolicited transmission of serialized data that relies on a start bit and a stop bit for each data packet with no timing coordination between the communicating devices

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
		<u>Extrinsic Evidence</u> <i>Webster's Ninth New Collegiate Dictionary</i> (1991) p. 111. Asynchronous: "not synchronous" Serially: "of or pertaining to a series" <i>Comprehensive Dictionary of Electrical Engineering</i> (1999) p. 37-38, 573 Asynchronous: "not synchronous"	<u>Primary intrinsic references</u> Specification ('675 Patent) – 2:62 – 3:7, 4:5-24, 4: 37-45, 4: 49-57, 5: 62-67, 6: 49-57, 7: 10-19, 8: 9-16, 8: 34-60, 9: 3-30. Specification ('214 Patent – incorporated by reference) 10:18 – 11:17, 8: 48-50; 11: 24-48; 12: 7-8; claim 1. <u>Primary Extrinsic References</u> "Serial Communication Protocols," Circuit Digest, Published April 29, 2019, available at www.circuitdigest.com "In asynchronous Serial Interface the absence of external Clock Source makes it rely on several parameters such as Data Flow Control, Error Control, Baud Rate Control, Transmission Control and Reception Control. On the transmitter side, there is a shifting of parallel data onto the serial line using its own clock." <i>The Art of Electronics</i>, Paul Horowitz, Section 10.17, p. 707. "The data IN/OUT protocol we described earlier constitutes a <i>synchronous</i> exchange of

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			data; data are asserted onto or retrieved from the bus synchronously with strobing signals generated in the CPU (or DMA controller). . . . The alternative is an <i>asynchronous</i> bus, in which a data IN transfer, for examples, goes something like this: The CPU asserts the port ADDRESS and a <i>level</i> (not a pulse) on a strobing line (call it IOR' as before) that signifies data IN from the addressed device.” (Italics in original) (Emphasis in bold added). <i>Microsoft Press Computer Dictionary</i>, 2d ed., (1994) p. 355 “Serial communications can be synchronous (controlled by some time standard such as a clock) or asynchronous (managed by the exchange of control signals that govern the flow of information). <i>Computer Desktop Encyclopedia</i>, 9th ed. (2001)p. 46. “[A]synchronous transmission [-] [t]he transmission of data in which each character is a self-contained unit with its own start and stop bits.” <i>Webster's New World Dictionary of Computer Terms</i>, 8th ed., (2000) p. 42.

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			“A method of data communication [asynchronous communication] in which the transmission of bits of data isn't synchronized by a clock signal but is accomplished by sending the bits one after another, with a start bit and a stop bit to mark the beginning and end, respectively, of each data unit.”
2	“first serial data, corresponding to first parallel bus data” '675 patent claim 7	No construction necessary, plain and ordinary meaning. <u>Intrinsic Evidence</u> At least '675 Pat., Cls. 1, 7, 15, 17; Figs., 3, Abstract; 1:44-8, 2:22-5, 3:7-10, 3:65-4:4, 4:16-8, 4:37-45, 4:49-5:15, 6:1-6. At least 6,070,214 Pat., Figs. 3, 4; Abstract; 3:34-59, 4:16-27. '675 File History (SH00002729 - SH00003087), including at least: 04/19/2011 Applicant Amendment and Remarks (SH00002880-SH00002881); 03/21/2011 Applicant Amendment and Remarks (SH00002907-2911); 11/19/2010 Final Rejection (SH00002930- SH00002939); 10/21/2010 Applicant Amendment and Remarks (SH00002969- SH00002975); 06/21/2010 Non-Final Rejection (SH00002987- SH00002995);	Serialized data generated from parallel data from a parallel bus of the first module. <u>Primary Intrinsic References</u> Specification 8:4-26, 8:40-53 ('675 Patent). Specification 10:1 – 11:12 ('214 Patent)

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
		Claims (SH00003071- SH00003074).	
3	“asynchronously, serially receiving second serial data” '675 patent claim 7	Not indefinite. No construction necessary, plain and ordinary meaning. If construed, “asynchronously” means “independently of a synchronized timing” If construed, “serially transferring” means “transferring in series” <u>Intrinsic Evidence</u> At least '675 Pat., Cls. 1, 7, 8, 15, 17; Abstract; Figs. 3, 4; 2:22-5, 3:7-10, 3:15-9, 3:34-7, 3:65-4:4, 4:37-9, 4:49-57, 4:58-5:15, 5:40-4, 5:49-8, 6:26-9, 6:49-57, 7:10-12, 7:39-43, 8:9-16, 9:3-7. '675 File History (SH00002729 - SH00003087), including at least: 04/19/2011 Applicant Amendment and Remarks (SH00002880- SH00002881); 03/21/2011 Applicant Amendment and Remarks (SH00002907-2911); 11/19/2010 Final Rejection (SH00002930- SH00002939); 10/21/2010 Applicant Amendment and Remarks (SH00002969- SH00002975); 06/21/2010 Non-Final Rejection (SH00002987- SH00002995); Claims (SH00003071- SH00003074).	Indefinite Under 35 U.S.C. 112, first and second paragraph (35 U.S.C. 112(a), (b) – post AIA) The term “asynchronously, serially receiving second serial data,” is indefinite under at least 35 U.S.C. § 112, second paragraph as the term is vague and indefinite. Furthermore, the specification fails to provide sufficient written description of the above noted term. To the extent that the term “asynchronously, serially receiving second serial data” can be interpreted based on the lack of support and clarity within the specification, the following construction is the only possible interpretation based on the limited intrinsic evidence in combination with available extrinsic evidence that could satisfy the requirements of 35 U.S.C. § 112. Proposed Construction Unsolicited reception of serialized data that relies on a start bit and a stop bit for each data packet with no timing coordination between the communicating devices <u>Primary intrinsic references</u>

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
		<u>Extrinsic Evidence</u> <i>Webster's Ninth New Collegiate Dictionary</i> (1991) p. 111. Asynchronous: "not synchronous" Serially: "of or pertaining to a series" <i>Comprehensive Dictionary of Electrical Engineering</i> (1999) p. 37-38, 573 Asynchronous: "not synchronous"	Specification ('675 Patent) – 2:62 – 3:7, 4:5-24, 4: 37-45, 4: 49-57, 5: 62-67, 6: 49-57, 7: 10-19, 8: 9-16, 8: 34-60, 9: 3-30. Specification ('214 Patent – incorporated by reference) 10:18 – 11:17, 8: 48-50 ; 11: 24-48; 12: 7-8; claim 1. <u>Primary Extrinsic References</u> "Serial Communication Protocols," Circuit Digest, Published April 29, 2019, available at www.circuitdigest.com "In asynchronous Serial Interface the absence of external Clock Source makes it rely on several parameters such as Data Flow Control, Error Control, Baud Rate Control, Transmission Control and Reception Control. On the transmitter side, there is a shifting of parallel data onto the serial line using its own clock." The Art of Electronics, Paul Horowitz, Section 10.17, p. 707. "The data IN/OUT protocol we described earlier constitutes a synchronous exchange of data; data are asserted onto or retrieved from the bus synchronously with strobing signals generated in the CPU (or DMA controller). . . . The alternative is an asynchronous bus, in

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			which a data IN transfer, for examples, goes something like this: The CPU asserts the port ADDRESS and a level (not a pulse) on a strobing line (call it IOR' as before) that signifies data IN from the addressed device.” (Italics in original) (Emphasis in bold added). Microsoft Press Computer Dictionary, 2d ed., (1994) p. 355 “Serial communications can be synchronous (controlled by some time standard such as a clock) or asynchronous (managed by the exchange of control signals that govern the flow of information). Computer Desktop Encyclopedia, 9th ed. (2001),. p. 46. (2001) “[A]synchronous transmission [-] [t]he transmission of data in which each character is a self-contained unit with its own start and stop bits.” Webster's New World Dictionary of Computer Terms, 8th ed., (2000) p. 42. (2000) “A method of data communication [asynchronous communication] in which the transmission of bits of data isn't synchronized by a clock signal but is accomplished by

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			sending the bits one after another, with a start bit and a stop bit to mark the beginning and end, respectively, of each data unit.”
4	“second serial data, corresponding to second parallel bus data;” ’675 patent claim 7	No construction necessary, plain and ordinary meaning. <u>Intrinsic Evidence</u> At least ’675 Pat., Cls. 1, 7, 15, 17; Figs., 3, Abstract; 1:44-8, 2:22-5, 3:7-10, 3:65-4:4, 4:16-8, 4:37-45, 4:49-5:15, 6:1-6. At least 6,070,214 Pat., Figs. 3, 4; Abstract; 3:34-59, 4:16-27. ’675 File History (SH00002729 - SH00003087), including at least: 04/19/2011 Applicant Amendment and Remarks (SH00002880-SH00002881); 03/21/2011 Applicant Amendment and Remarks (SH00002907-2911); 11/19/2010 Final Rejection (SH00002930- SH00002939); 10/21/2010 Applicant Amendment and Remarks (SH00002969- SH00002975); 06/21/2010 Non-Final Rejection (SH00002987- SH00002995); Claims (SH00003071- SH00003074).	Serialized data generated from parallel data from a parallel bus of the first module. <u>Primary Intrinsic References</u> Specification 8: 40-53 (’675 Patent). Specification 10:1 – 11: 12 (’214 Patent)
5	“generating a first clock signal, for use by the first module, using the second	Not indefinite. No construction necessary, plain and ordinary	Indefinite Under 35 U.S.C. 112, first and second paragraph (35 U.S.C. 112(a), (b) – post AIA)

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
	serial data” ’675 patent claim 7	meaning. <u>Intrinsic Evidence</u> At least ’675 Pat., Abstract; Cls. 7, 18, 21, 22; Figs. 1, 4; 1:30-6, 1:40-3, 2:22-5, 2:57-3:15, 3:49-53, 3:61-5, 3:65-4:4, 4:49-57, 4:58-5:36, 5:40-4, 5:49-8, 6:6-17, 6:30-48, 6:57-7:9, 7:29-8:3, 8:27-31, 8:60-9:16. At least 6,070,214 Pat., Fig. 3; 8:12-21, 8:38-53, 12:3-8. ’675 File History (SH00002729 - SH00003087), including at least: 04/19/2011 Applicant Amendment and Remarks (SH00002880- SH00002881); 03/21/2011 Applicant Amendment and Remarks (SH00002907-2911); 11/19/2010 Final Rejection (SH00002930- SH00002939); 10/21/2010 Applicant Amendment and Remarks (SH00002969- SH00002975); 06/21/2010 Non-Final Rejection (SH00002987- SH00002995); Claims (SH00003071- SH00003074).	The term “generating a first clock signal, for use by the first module, using the second serial data,” is indefinite under at least 35 U.S.C. § 112, second paragraph as the terms are vague and indefinite. Furthermore, the specification fails to provide sufficient written description related to the above noted term. To the extent that the term “generating a first clock signal, for use by the first module, using the second serial data” can be interpreted based on the lack of support and clarity within the specification, the following construction is the only possible interpretation based on the limited intrinsic evidence in combination with available extrinsic evidence that could satisfy the requirements of 35 U.S.C. § 112. Proposed Construction Recovering a clock signal using information contained within the received asynchronous data and the recovered clock signal is used by the first module. <u>Primary Intrinsic References</u> Specification 6:33-46, 8:38-53, and FIG. 3 (’214 Patent) <i>See also</i>, RESPONSE TO OFFICE ACTION DATED JUNE 21, 2010, p.

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			12 (citing to '214 Patent at 6:33-46 and 8:38-53) <u>Primary Extrinsic References</u> Webster's New World Dictionary of Computer Terms, 8th ed., (2000) p. 107. (2000) “clock An electronic circuit that generates evenly spaced pulses at speeds of millions of hertz (Hz). The pulses are used to synchronize the flow of information through the computer's internal communication channels. Most computers also contain a separate circuit that tracks the time of day, but this has nothing to do with the system clock's function.”
6	“a first buffer” '454 patent claim 1	No construction necessary, plain and ordinary meaning. <u>Intrinsic Evidence</u> At least '454 Pat., Cls. 1, 3, 7, 8, 10, 11, 12, 13, 14, 16, 18, 20, 23, 31, 32, 34, 35, 38, 41, 43, 45; 8:12-35. '454 File History (SH00003211 - SH00003553), including at least: 06/23/2016 Applicant Amendment and Remarks (SH00003315-	A receive FIFO buffer that is monitored for overflow of data received from a remote communication device. <u>Primary Intrinsic References</u> Specification 8:17-20 ('454 Patent referring to U.S. Ser. Nos. 09/130,057 and 09/130,058 by reference.) FIFO buffer 22, 24 of U.S. Ser. Nos. 09/130,057 and 09/130,058

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
		SH00003343); 02/23/2013 Non-Final Rejection (SH00003351- SH00003363); 11/16/2015 Applicant Amendment and Remarks (SH00003393- SH00003394); 08/19/2015 Non-Final Rejection (SH00003406- SH00003410); Claims (SH00003527- SH00003530).	Specification: 6:3-10, 6:47-58, 6:64 – 7:2, 10:41-44, 10:50-54, 10:67 – 11:7, and 11:13-23 (U.S. Ser. No. 09/130,058).
7	“a fill amount associated with a storage capacity of the first buffer” '454 patent claim 1	No construction necessary, plain and ordinary meaning. If construed, “fill amount” means “fill level” <u>Intrinsic Evidence</u> At least '454 Pat., Cls. 1, 3, 7, 8, 10, 11, 12, 13, 14, 16, 18, 20, 23, 31, 32, 34, 35, 38, 41, 43, 45; 8:12-35. '454 File History (SH00003211 - SH00003553), including at least: 06/23/2016 Applicant Amendment and Remarks (SH00003315- SH00003343); 02/23/2013 Non-Final Rejection (SH00003351- SH00003363); 11/16/2015 Applicant Amendment and Remarks (SH00003393- SH00003394); 08/19/2015 Non-Final Rejection (SH00003406- SH00003410); Claims (SH00003527- SH00003530).	Any predetermined level of data in a buffer below 100% of buffer capacity. <u>Primary Intrinsic References</u> Specification: 8:20-21 ('454 Patent referring to U.S. Ser. Nos. 09/130,057 and 09/130,058 by reference.) Specification 6: 31-43 (U.S. Ser. No. 09/130,057), and 6: 47-58 (U.S. Ser. No. 09/130,058)
8	“a flow control signal”	No construction necessary, plain and ordinary meaning.	A signal that controls the flow of data from a data device to ensure the data device does not

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
	'454 patent claim 1	If construed, “flow control signal” means “signal that’s used to control the flow of data” <u>Intrinsic Evidence</u> At least '454 Pat., Cls. 1, 7, 31, 34, 38, 43; 8:12-35. At least 6,070,214 Pat., Fig. 3, 6:33-63; 10:18-25. '454 File History (SH00003211 - SH00003553), including at least: 06/23/2016 Applicant Amendment and Remarks (SH00003315- SH00003343); 02/23/2013 Non-Final Rejection (SH00003351- SH00003363); 11/16/2015 Applicant Amendment and Remarks (SH00003393- SH00003394); 08/19/2015 Non-Final Rejection (SH00003406- SH00003410); Claims (SH00003527- SH00003530).	overwhelm a receiving device. <u>Primary Intrinsic References</u> Specification 8:20-21 ('454 Patent referring to U.S. Ser. Nos. 09/130,057 and 09/130,058 by reference.) Threshold detect signal 52 of U.S. Ser. Nos. 09/130,057 and 09/130,058 Specification: 6:47-58, FIG. 1 (U.S. Ser. No. 09/130,058). <u>Primary Extrinsic Reference</u> Webster's New World Dictionary of Computer Terms, 8th ed., (2000) p. 107. (2000) “A method of ensuring that the data device, such as a modem or a computer system, does not overwhelm the receiving device, such as a modem. Software handshaking (also called XON/XOFF handshaking) regulates communications between two modems. Hardware handshaking (CTS/RTS) regulates data flow between the computer and the modem.”
9	“generate a clock signal, for use by the module,	Not indefinite.	Indefinite Under 35 U.S.C. 112, first and second paragraph (35 U.S.C. 112(a), (b) –

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
	using the first serial data” ’454 patent claim 17	No construction necessary, plain and ordinary meaning. <u>Intrinsic Evidence</u> At least ’454 Pat., Cls. 17, 28, 32, 44; 2:15-9, 2:63-3:8, 3:63-4:2, 4:36-9, 4:49-57. At least 6,070,214 Pat., Fig. 3; 8:12-21, 8:38-53, 12:3-8. ’454 File History (SH00003211 - SH00003553), including at least: 06/23/2016 Applicant Amendment and Remarks (SH00003315-SH00003343); 02/23/2013 Non-Final Rejection (SH00003351- SH00003363); 11/16/2015 Applicant Amendment and Remarks (SH00003393- SH00003394); 08/19/2015 Non-Final Rejection (SH00003406- SH00003410); Claims (SH00003527- SH00003530).	post AIA) The term “generating a first clock signal, for use by the first module, using the second serial data,” is indefinite under at least 35 U.S.C. § 112, second paragraph as the terms are vague and indefinite. Furthermore, the specification fails to provide sufficient written description related to the above noted term.” To the extent that the term “generating a first clock signal, for use by the first module, using the second serial data” can be interpreted based on the lack of support and clarity within the specification, the following construction is the only possible interpretation based on the limited intrinsic evidence in combination with available extrinsic evidence that could satisfy the requirements of 35 U.S.C. § 112. Proposed Construction Recovering a clock signal using information contained within the received data and the recovered clock signal is used by the module. <u>Primary Intrinsic References</u> Specification 6:33-46, 8:38-53, and FIG. 3 (’214 Patent) <i>See also</i>, RESPONSE TO OFFICE ACTION DATED JUNE 21, 2010, p.

No.	Claim Term	Plaintiff's Proposed Construction and Evidence	Defendant's Proposed Construction and Evidence
			12 (citing to '214 Patent at 6:33-46 and 8:38-53)