

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner

v.

SHAMROCK INNOVATIONS, LLC,
Patent Owner

Case IPR2023-00842
Patent No. 9,535,454

DECLARATION OF KNUT GRIMSRUD, PH.D.

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I, Dr. Knut Grimsrud, declare as follows:

I. INTRODUCTION

1. I have been retained by Western Digital Technologies, Inc., (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office regarding U.S. Patent No. 9,535,454 (“the ’454 patent”), which I understand is labeled as Ex. 1001. I have been asked to analyze and respond to certain opinions of Patent Owner’s expert, Mr. Terry R. Lee. My opinions and the bases of my opinions are set forth below.

2. I am being compensated at my normal consulting rate for the time I spend on this matter. No part of my compensation is dependent on the outcome of this proceeding. I have no other interest in this proceeding.

II. QUALIFICATIONS

3. I am an expert in the fields of storage interfaces and solid-state storage technologies. I am an inventor or co-inventor on over 75 issued patents primarily in these fields. I am the primary author of “Serial ATA Storage Architecture and Applications: Designing High-Performance, Cost- Effective I/O Solutions" (ref ISBN-13: 978-0971786189).

4. I received a Bachelor of Science Degree in Electrical & Computer Engineering from Brigham Young University in 1988, a Master of Science Degree in Electrical & Computer Engineering from Brigham Young University a couple

years later, and a Ph.D. in Electrical & Computer Engineering from Brigham Young University in 1993.

5. In 1999, I was part of the Intel team that initiated the Serial ATA initiative based on industry (and Intel) need and enlisted the founding group of promoter companies to pursue definition and development of the technology.

6. In 2001, I was Intel's primary technical contributor in developing and delivering the original Serial ATA 1.0 specification, which later published in January 2003 as the Serial ATA 1.0a specification, and a member of the core promoter group forming the Serial ATA initiative (ref https://www.seagate.com/support/disc/manuals/sata/sata_im.pdf).

7. In 2004, I was the primary Intel technical contributor in delivering second-generation SATA 2.0 definition. I also drove the formation of a formal industry association (SATA-IO) to sustain and further advance the Serial ATA core technology (see www.sata-io.org) and served as the chairman of the board of directors for the SATA-IO organization from 2004-2016.

8. In 2008, I led the SATA-IO organization through development of the SATA 2.6 and 3.0 generations published in 2007 and 2008 respectively.

9. In 2008, I led the R&D team that developed and delivered Intel's first SATA solid-state drive (SSD) launched as the X25-M and X18-M and later that

year the enterprise-class X25-E. Subsequent iteration (dubbed G2) released the following year.

10. In 2012, I led the architecture team that delivered Intel's first SATA 3.0 enterprise-class (6gbps) SSD program DC-S3700.

11. I led the SATA-IO board of directors through the development of the SATA 3.1 (2011), 3.2 (2013) and 3.3 (2016) generations. At that point I stepped down from the SATA-IO board and from the initiative to pass the baton to the next generation of Intel representatives and devote more time to leading Intel's solid-state storage (SSD) architecture team.

12. I'm currently retired aside from IP consulting.

13. In light of all of the foregoing, I believe that I am well qualified to assess and opine authoritatively on the subject matter of the '454 patent.

14. A true and correct copy of my curriculum vitae is provided, and I understand that it will be labeled as Exhibit 1015.

III. SUMMARY OF OPINIONS

15. The opinions in this Declaration are based on the documents I have reviewed and my knowledge and professional judgment. In forming my opinions, I reviewed each of the publications that I discuss.

16. My opinions are based upon how a person having ordinary skill in the art ("PHOSITA") would have understood the '454 patent, the prior art, and the

state of the art at the time of the alleged invention, which I understand is assumed to be on or around August 6, 1998, for purposes of this analysis.

17. I have been informed that in determining whether a patent claim is invalid as being obvious, there are four considerations: (1) the level of ordinary skill in the art; (2) the scope and content of the prior art; and (3) any differences between the prior art and the claimed invention; and (4) any additional considerations that would suggest the claimed invention was obvious or nonobvious.

18. In my opinion, and as explained in detail below, Exhibit 2012 and the Tachyon Article (Exhibit 1014) plainly rebut Mr. Lee's assertion that one of skill would understand the Vangemert buffer credit control words ("BCCW") are transmitted "via the [Vangemert] transmit buffer" (the claimed "second buffer") (see Ex. 2002 ¶¶ 102-107), as doing so would increase latency and contradict sound engineering practice. This is further supported in Exhibit 2007, submitted by Patent Owner and Mr. Lee, which further rebuts Mr. Lee's assertion that the BCCWs of Vangemert are transmitted "via the transmit buffer" (the claimed "second buffer").

IV. LEVEL OF ORDINARY SKILL IN THE ART

19. I have been asked to assume that the time of the alleged invention described in the '454 patent is on or around August 6, 1998. I have applied that

timeframe and understanding to my analysis and opinions in this declaration. At the time of the alleged invention described in the '454 patent, I was a storage technologist at Intel working on finalizing a DMA protocol for parallel ATA which was incorporated into the ATA/ATAPI-4 industry standard.

20. It is my understanding that a person of ordinary skill in the art at the time of the alleged invention of the '454 patent would have had at least a bachelor's degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communications within a computing device or system and between different computing devices, systems, or subsystems. I further understand that more education can supplement practical experience and vice versa.

21. In view of my education and substantial experience in serial communication, I believe I am qualified to opine from the perspective of a person having ordinary skill in the art ("PHOSITA") at the time of the claimed invention.

V. A PHOSITA WOULD UNDERSTAND THE BCCW ARE NOT TRANSMITTED "VIA THE TRANSMIT BUFFER"

A. Vangemert Teaches That the Flow Control Signal Bypasses the Transmit Buffer

22. A fair reading of Vangemert is that the *transmit controller is configured* to create and transmit the BCCW without unnecessary delay.

Vangemert stressed the importance of a fast, low latency system such as Fibre

Channel, and configuring the transmit controller to simply and quickly achieve that end is what is disclosed. *See* Ex. 1005 at Abstract; 1:8-10; 1:54-55; 1:62-63; 1:66-2:1; 4:16-23; 5:2-4. The simplest and quickest way to send the BCCW to the transmitter 312 is to configure the transmit controller 412 to send it directly to the encoder 402 without adding the step of passing it through the transmit buffer 410.

23. Vangemert suggests control words may be used to arbitrate control of a loop and to convey the desire to transmit data frames. Ex. 1005 at 3:9-13. These arbitration control words may include various handshaking or protocol interlocks that are processed similarly to the BCCWs above and would not be stored in a transmit buffer with user data. However, Vangemert does describe some “control words” that are generally used in association with data frames in Vangemert. *See* Ex. 1005 at 3:41-60. It makes sense that some control words directly associated with individual user data frames (e.g., frame delineators, start/stop bits, etc.) would be stored in the transmit buffer with data frames because these control words would need to be attached to the data frames to facilitate the transmission of these specific user data frames from one node to the other. Such, however, does not support the logical leap that the BCCW must pass through the transmit buffer.

24. Storing the BCCW in the transmit buffer would be illogical and is not supported by the plain language of Vangemert. Vangemert taught a system to reduce latency. Ex. 1005 at 1:66-2:29. Creating the BCCW in the transmit

controller and subsequently passing the BCCW through the transmit buffer would add unnecessary steps and increase latency over a system in which “the transmit controller 412 *begins* transmitting buffer credit control words in response to a credit signal from the credit manager 418.” Ex. 1005 at 4:14-16. Immediately transmitting the BCCW upon receipt of a credit signal is faster than taking the additional step of passing the BCCW through the transmit buffer before transmitting the BCCW. Contrary to the teachings of Vangemert, Mr. Lee’s hypothesis would increase latency by introducing unnecessary steps and creating an unbounded transmission protocol by deferring transmission of flow control signals until an arbitrary amount of data in the transmit buffer is first sent. This not only increases latency but is adverse to sound engineering practices.

25. A PHOSITA would have understood that the Vangemert transmit buffer was a FIFO buffer. Because most communication protocols do not limit the size of transfer buffers, the time required for a flow control signal to pass through the buffer is unknown—e.g., it would take longer for a flow control signal to pass through a large buffer than it would take to get through a small buffer. Having unbounded times for control signals to get delivered is not sound engineering practice, makes the protocol exceedingly challenging to validate, and delays the delivery of flow control signals. This would also have led a PHOSITA to have

thought it illogical to interpret Vangemert to require the BCCW to pass through the transmit buffer.

26. Finally, a PHOSITA would have understood that the Vangemert BCCW had to bypass the transmit buffer to avoid the occurrence of a deadlock condition, which is explained in more detail below. Vangemert discloses a module that both receives and sends data. Ex. 1005 at 2:58-3:3. In other words, a node is sometimes a transmitter and sometimes a receiver. Thus, one of skill would not have interpreted Vangemert to teach passing the BCCW through the transmit buffer because Mr. Lee's conjecture would lead to an undesirable deadlock condition.

B. It Was and Is Common Practice for Flow Control Signals to Bypass the Transmit Buffer

27. It was common practice in the art as of the priority date for a flow control signal to bypass the transfer buffer. Two simple rationales for why this are provided below, which apply directly to Fibre Channel communication protocols and would therefore apply to the Fibre Channel system of Vangemert.

1. Time Bounding

28. In most communication protocols there is no inherent limitation placed on the size of the transfer buffer, and designers typically make tradeoffs between cost and performance in dimensioning the transfer buffer. If the protocol does not bound the transfer buffer size and the flow control signal is placed into the

transfer buffer transmit FIFO, then the time it takes for the flow control signal to subsequently be transmitted over a link becomes unbounded. Having unbounded times for control signals to be sent and received between device is not a sound protocol design and makes the protocol exceedingly challenging to validate.

2. Deadlock

29. The Fibre Channel protocol (and others such as Serial ATA) may experience a condition known as deadlock if the flow control signal is added to the tail of the transmit FIFO in the transfer buffer. The following scenario is a simple case that highlights this deadlock behavior if the flow control signal does not bypass the transmit buffer:

1. Side A is out of transfer credits (BCCWs) from Side B but has a frame of data already queued up in the transfer buffer (which you would expect if it has been waiting to get a flow control credit).
2. Side B is completing a transfer to Side A that exhausts Side B's transfer credits (BCCWs). Side B also has a subsequent pending frame to transmit in its transfer buffer after the current one finishes (which is expected since efficient implementations will strive to have the next frame ready to go as soon as previous one is done).
3. If Side A inserts its flow control signal granting Side B a credit into the transfer buffer (which has a frame of data already pending), then that signal will not be transmitted because it is stuck behind the data frame which cannot be transmitted due to lack of transfer credits on Side B, preventing further transmission by Side A.
4. Similarly, Side B cannot send Side A a credit to allow it to empty the data frame that is stuck ahead of the flow control credit because

it is also unable to transmit the data frame that is ahead of its flow control signal.

30. The system is then deadlocked, resulting in communication between Side A and Side B to stop. A PHOSITA at the time of the alleged invention of the '454 Patent would have understood the possibility of a deadlock condition occurring and would have accordingly designed a protocol where the flow control signal does not pass through the data buffers (e.g., the claimed "second" buffer).

C. Hewlett Packard ("HP") Publications Show Fibre Channel Flow Control Bypassing Transfer Buffer

1. Overview of Exhibit 2012 and the Tachyon Article (Exhibit 1014)

31. Hewlett-Packard was one of the early pioneers and leaders for Fibre Channel implementations. Their chip named "Tachyon" was one of the most common and popular implementations of Fibre Channel in the late 90's.

32. Hewlett-Packard used to publish a journal called "Hewlett-Packard Journal" and the archives for these journals can still be found in the HP archives at: http://hparchive.com/hp_journals. Two articles in their October 1996 issue are relevant, and I will discuss them in some details below: "An Introduction to Fibre Channel" (Ex. 1014 at pages 94 – 98) and "Tachyon: A Gigabit Fibre Channel Protocol Chip" (Ex. 1014 at pages 99 – 112).

33. I understand that Patent Owner and Mr. Lee relied on a 1996 article entitled "An Introduction to Fibre Channel" as Exhibit 2012 in the Patent Owner

Response. Exhibit 2012 references “Article 12” on page 5. I understand Article 12 was not provided by Patent Owner or Mr. Lee. Exhibit 2012 was published in the October 1996 Hewlett-Packard Journal and where Exhibit 2012 references “Article 12,” the Journal points to the Tachyon Article. I understand that Patent Owner and Mr. Lee relied on the Tachyon Article and that the Tachyon Article is referenced in Exhibit 2012 (and in fact is the immediately following article in the Journal having a common author, Meryem Primmer) and provides proper context for Exhibit 2012. Furthermore, Vangemert teaches a Fibre Channel system and therefore a PHOSITA would have been informed as to the operation of the Fibre Channel system of Vangemert by the Tachyon Article.

2. Summary of the Tachyon Article (Ex. 1014)

34. The Tachyon Article is clear and relevant on its face. Figures 4, 5, and 6 give a quick overview of the Fibre Channel system described. All three figures clearly show a separate “ACK” FIFO near the lower right corner of the diagrams. This is where the ACK receive flow control signals are sent. The Tachyon Article teaches that an ACK signal increments an end-to-end count, which “determines the number of frames that Tachyon can send to the remote designation without receiving an ACK.” *See* Ex. 1014 at p. 102. A transmitter starts with the number of flow control credits initially set, and with each transmission it decrements (decreases by one) the credits it has to transmit further. When it reaches zero

credits it may no longer transmit. For each ACK the transmitter receives back from the receiver, it increments (increases by one) the transmit credits it has available. Analogously, Vangemert teaches a similar credit based flow control system, requiring buffer credits to be obtained from a receiving device prior to transmitting data, and updating said credits as data is transmitted and received. EX. 1005 at 4:8–5:4. Thus, the ACK signal provides flow control by managing the number of credits the transmitter has available for sending further data and is analogous to the Vangemert BCCW.

35. Next to the ACK FIFO in all three figures (FIGS 4, 5, and 6) is the “Outbound FIFO,” which is shown clearly as a separate data path. The outbound FIFO is associated with the user data and is plainly separate from the corresponding ACK FIFO described above

36. Figure 6 from Ex. 1014 is reproduced below. As shown in the annotated version of Figure 6 (below), outbound data enters the logic block to be stored in Outbound Frame FIFO, which would correspond to the claimed second buffer and the Vangemert Transmit Buffer. This data path is illustrated in yellow. To the left of the Outbound Frame FIFO is the ACK FIFO. The ACK signal corresponding to Vangemert’s BCCW passes through a buffer different from the outbound data frame buffer (the claimed second buffer or Vangemert transmit buffer). Avoiding the data transmit buffer “[a]llows time-critical messages [such as

the BCCW] to bypass the normal traffic waiting for various resources via a low-latency, high-priority outbound path.” Ex. 1014 at 102.

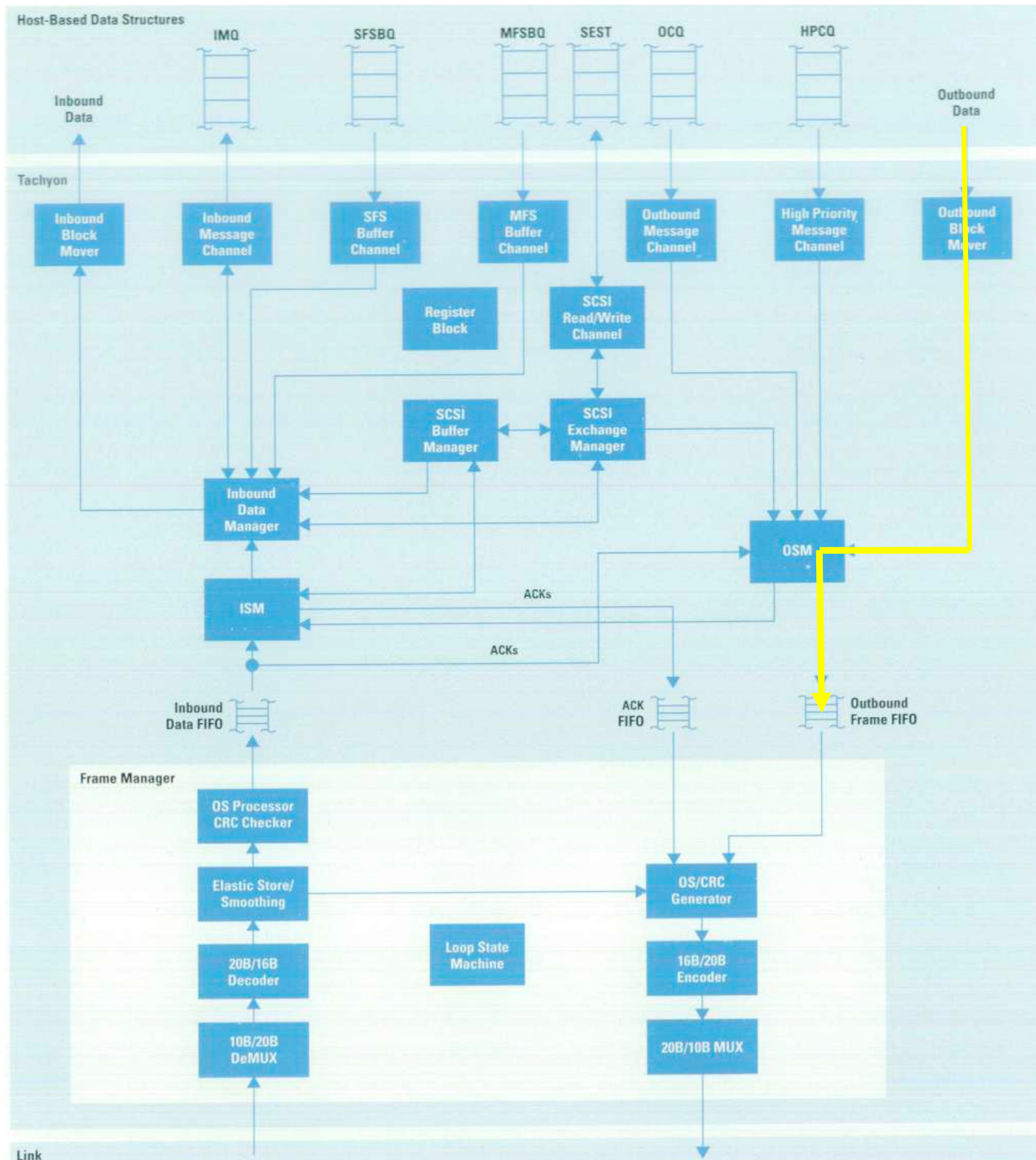


Exhibit 1014 Figure 6 (Annotated)

37. The Tachyon Article refutes Mr. Lee's argument hypothesizing the Vangemert BCCW had to pass through the transmit buffer. The plain language of Vangemert describing the transmit controller as being configured to begin transmitting the BCCW on receipt of a buffer credit signal would have been understood by a PHOSITA to teach that the BCCW does not pass through the transmit buffer of Vangemert. The Tachyon Article confirms that understanding. As noted above, issues relating to latency, system integrity and system failure would have led one of skill to understand Vangemert's low-latency improvement to the Fibre Channel protocol would not pass the BCCW through the transmit buffer. Mr. Lee's position that Vangemert requires the BCCW to pass through the transmit buffer is simply not reconcilable with the Tachyon Article's overview of how those of skill understood the Fibre Channel protocol was to be implemented.

38. The Tachyon product clearly implemented flow control within a Fibre Channel protocol that bypassed the transfer buffer.

D. The Tachyon Article Teaches Automated Flow Control With Transmit Buffer Bypass

39. The HP Journal article of October 1996 implements automated flow control that bypasses the transfer buffer. The details below describe the specifics of how this article teaches this implementation and approach.

40. There are a number of details disclosed in the article that all consistently define a behavior and implementation of automated flow control with

buffer bypass in a Fibre Channel system. Thus, while the Tachyon Article is not a one-to-one equivalent to the Fibre Channel system of Vangemert, it is illustrative of how a PHOSITA at the time would have developed a Fibre Channel system having buffer bypass of flow control signals. It is logical that Vangemert would have similarly been developed to bypass data buffers in the transmission of BCCWs to facilitate the desired minimization of latency within a Fibre Channel protocol. EX. 1005 at 1:47-63. Specific sections of the Tachyon Article will be highlighted to construct this clear picture.

1. Automated Flow Control

41. The top paragraph in the right column of page 101 of the Tachyon Article (copied below with added emphasis) clearly discloses that the Tachyon chip implement automated flow control in hardware. This paragraph is part of the section highlighting the basic attributes and capabilities of the chip.

Tachyon achieves high performance and efficiency because **many of its lower-level functions are implemented in hardware**, eliminating the need for a separate microprocessor chip. Functions such as disassembly of outbound user data from sequences into frames, reassembly of inbound data, **flow control**, data encoding and decoding, and simple low-level error detection at the transmission character level are **all built into hardware**. One set of hardware supports all upper-level protocols. Errors and exceptions are offloaded to host-based upper-level software to manage.

2. Flow Control Mechanism

42. The flow control mechanism is outlined in the tutorial in the article describing how transmission works along with the associated figures referenced as

part of this transmission/reception tutorial. The mechanism and associated Tachyon operation is spelled out in the second to bottom paragraph of the right column on page 102 (copied here with added emphasis).

Tachyon keeps track of the frame count for the sequence. The Fibre Channel header for each frame contains an incremental count of the number of frames transmitted for the sequence along with the relative position of that frame within the sequence. As Tachyon sends the frames for the sequence, it also tracks flow control for the sequence using a Fibre Channel flow control method called end-to-end credit (EE_Credit). EE_Credit determines the number of frames that Tachyon can send to the remote destination without receiving an ACK. **Each time Tachyon sends a frame, EE_Credit decrements. Each time Tachyon receives an ACK from the destination, EE_Credit increments. If EE_Credit goes to zero, Tachyon stops transmitting frames** and starts a watchdog timer called the ED_TOV timer (error detect timeout value). The ED_TOV timer counts down until ACKs arrive. If ACKs arrive, Tachyon resumes transmission. If the ED-TOV timer expires, Tachyon sends a completion message to the host indicating that the sequence has timed out.

43. As is known and understood as part of the Fibre Channel protocol, flow control is managed via a credit system. The receiving device signals to the transmitting device that it may transmit more data by transmitting an “ACK” signal which increments the buffer credits within the transmitting device and thereby allows the transmitting device to transmit additional data. Thus, the receiving device uses the ACK transmission as it’s mechanism for flow control by granting the transmitting device additional buffer credit to transmit more data.

3. ACK Buffer Bypass

44. It is important that the ACK flow control signal bypasses data buffers since the ACK signal is striving to control the flow of data between a transmitting device and a receiving device, and therefore can't be held up by the very data it is striving to control. The figures associated with the transmission process (Figure 4 on page 103, Figure 5 on page 104, and Figure 6 on page 105) all consistently and clearly show that the ACK flow control signal bypasses the data buffers. Some data buffers are in a completely different layer of the protocol (upper right corner in the figures). The ACK flow control signal bypasses these data buffers. The Outbound Frame FIFO is adjacent the ACK FIFO but the ACK signal is loaded into an ACK FIFO, thereby bypassing the Outbound Frame FIFO, as shown in the above noted Figures. The Tachyon Article consistently shows the ACK flow control signal, which as noted above is analogous to the Vangemert BCCW, bypassing any buffer that could correspond to the Vangemert transmit buffer (the claimed "second" buffer). Even where the ACK signal is loaded into an ACK buffer as discussed above, the ACK buffer is not equivalent to the claimed "second buffer." Such confirms a PHOSITA familiar with the Fibre Channel protocol would not read Vangemert to suggest its BCCW would pass through its transmit buffer.

45. Referring to Figure 5 (Figure 4 or Figure 6 could be substituted) reproduced below for convenience, inbound data from the link is processed by the ISM block (inbound sequence manager) which is shown to be in direct communication with an ACK FIFO that is separate and distinct from the Outbound Frame FIFO. Hence, the associated ACK signal bypasses the Outbound Frame FIFO entirely on its way to transmission over the link via the Frame Manager. The ISM block performs the automation for this flow control signal, as shown in the annotated version of FIG. 5, below.

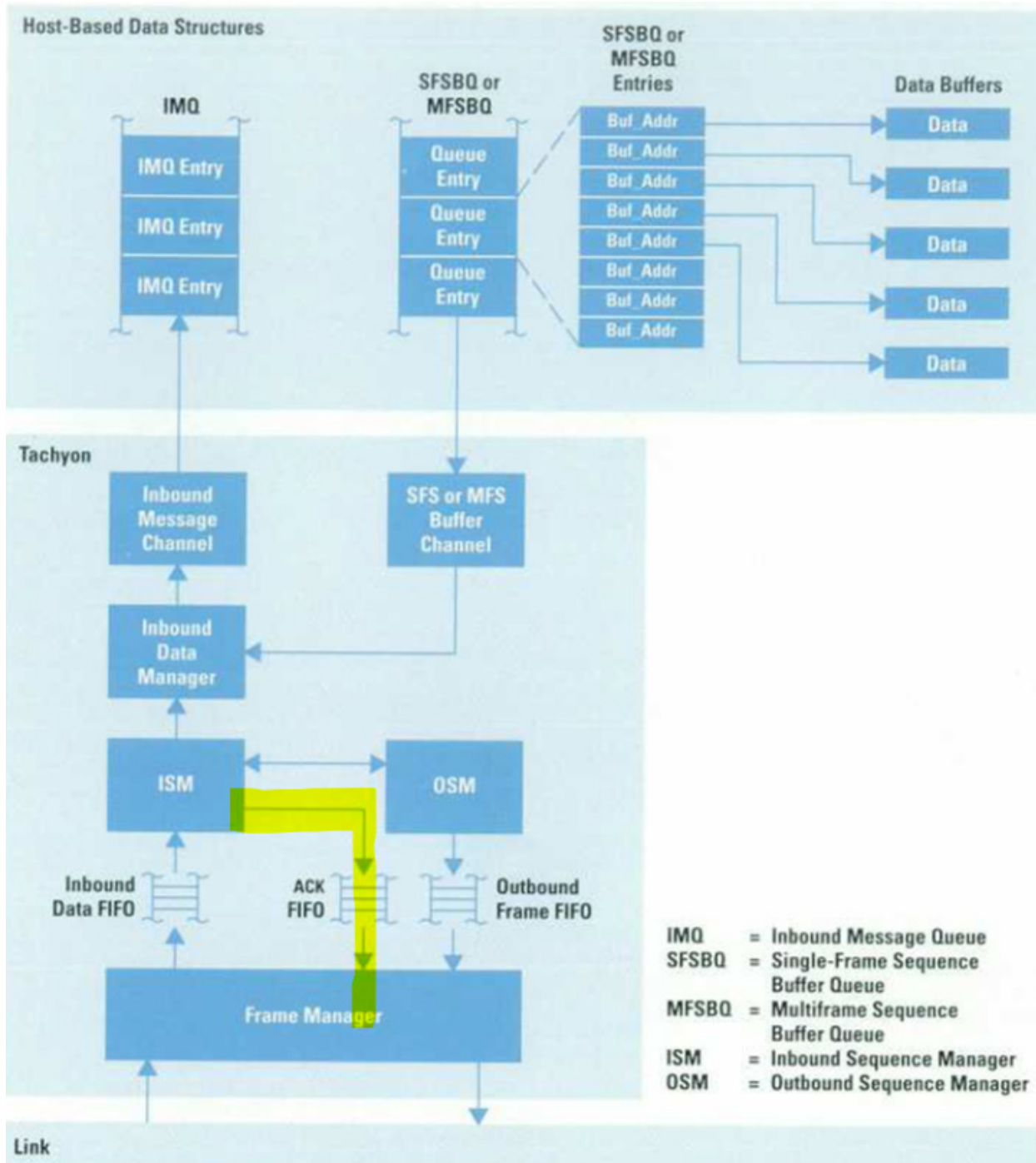


Exhibit 1014 Figure 5 (Annotated)

46. In the “Introduction” article, it’s helpful to note in the section “A Layered Approach” that the Tachyon chip implements Fibre Channel and as shown

in Figure 7 and the surrounding text the Fibre Channel specification is built in a layered approach with flow control handled in the FC-2 layer. The description of the FC-2 layer in that section specifically says “[i]ncluded in this layer is the framing protocol used to break sequences into individual frames for transmission and flow control...” The subsequent Tachyon Article is much more detailed but is consistent with and builds on this.

47. The importance of the flow control being in the FC-2 layer is that this layer is not where the user data buffers are. Generally, the user data buffers are in the FC-4 layer. It is known that within layered protocols, such as Fibre Channel, data flows downward through the layers and does not “loop” back up to the higher layers. For example, flow control signals generated in the FC-2 layer (as noted above) do not flow back to the higher FC-4 layer associated with the user data buffers. This again is highlighted in the Tachyon Article.

48. Thus, the ACK flow control signal of the Tachyon Article corresponding to Vangemert’s BCCW does not pass through any data buffer and illustrates that a PHOSITA would not have understood to teach otherwise.

4. Figure 6 ACK Clarification

49. Figure 6 on page 105 can create some confusion since there are two different paths indicated for ACK signals in the figure. This is due to the figure

representing the entire architecture block diagram that includes both the transmit and the receive details.

50. Figure 6 is copied below and annotated for convenience. When transmitting via the Outbound Frame FIFO, ACK signals are RECEIVED from the target receiving device via the link, and these ACK signals are used by the OSM to limit the data that gets transmitted by responding to the ACKs received from the target receiving device. This is highlighted by the ACK path highlighted in green. In essence, the green path represents buffer credits sent from the target receiving device that enable the node depicted to transmit outbound data. When RECEIVING data via the Inbound Data FIFO, the ISM determines whether there is buffer space in the depicted node to continue receiving data and signals this by transmitting ACK signals to the receiving device via the link. This is highlighted by the ACK path highlighted in yellow. There is no inconsistency in this symmetric arrangement for transmit vs receive handling of the flow control (ACK) signals.

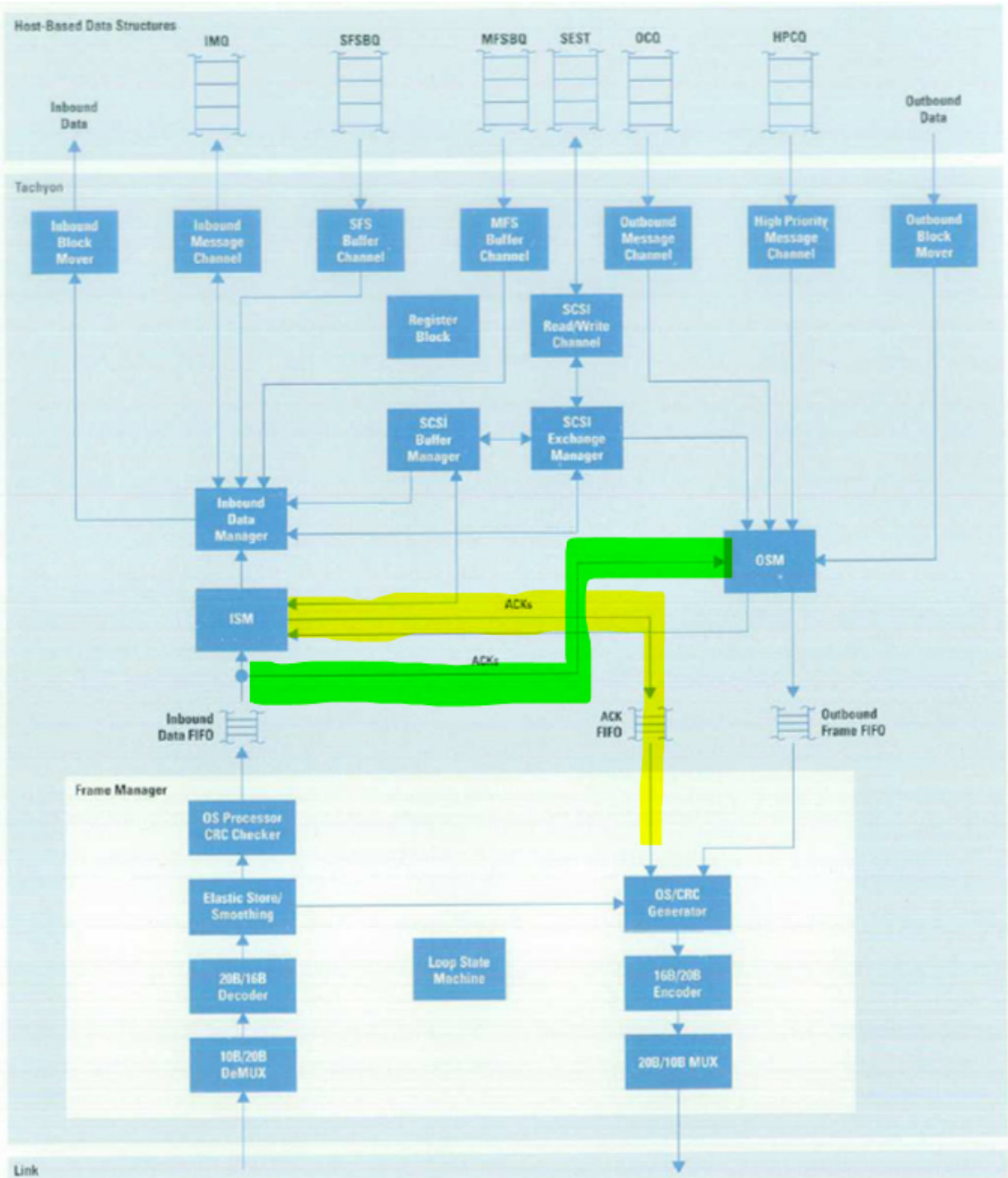


Exhibit 1014 Figure 6 (Annotated)

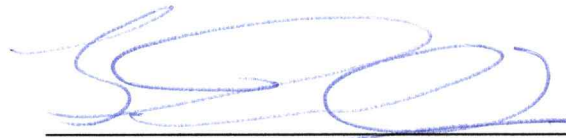
51. Thus, the Tachyon Article plainly illustrates that Fibre Channel implemented flow control that bypassed the data buffers (e.g., claimed “second” buffer”).

VI. CONCLUSION

52. As explained above, it is my conclusion that Exhibit 2012 and the Tachyon Article plainly rebut Mr. Lee’s assertion that one of skill would understand the BCCW are transmitted directly “via the transmit buffer” (*see* Ex. 2002 ¶¶ 102-107) and not via the claimed second buffer. Passing the BCCW through the Vangemert transmit buffer would increase latency, go against sound engineering practice and would be contrary to how a PHOSITA would have understood a Fibre Channel implementing system, such as that described in Vangemert, would have been designed. I believe Mr. Lee’s position is not objectively supportable.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge.

Executed on: April 3, 2024



Knut Grimsrud, Ph.D.