

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner,

v.

SHAMROCK INNOVATIONS, INC.,

Patent Owner.

Case No. IPR2023-00842

U.S. Patent No. 9,535,454

Patent Owner Demonstratives

Petitioner Never Mapped The Actual Claim Language In the Petition

Petitioner's Characterization of Vangemert	Claim Language
the bit credit signal is generated <u>when the available buffer space is sufficient</u> (equal to the fill amount) to accept the data word to be transmitted (emphasis added).	the module is operable to generate a flow control signal <u>in response to the amount of data stored</u> in the first buffer <u>equaling or exceeding</u> the fill amount (emphasis added).

- k. *wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,*

Sur-Reply, 9

Vangemert teaches generating a flow control signal in the form of a buffer credit signal when the buffer has sufficient space for a new data frame. EX. 1003, ¶ 68. Because the buffer credit must be provided to an initiating node before that node can transmit data, the buffer credit signal is a flow control signal that controls data flow from the initiating device to the receive device. *Id.* ¶ 69; EX. 1005, col. 4:9-11. Thus, the bit credit signal is generated when the available buffer space is sufficient (*equal to the fill amount*) to accept the data word to be transmitted. EX 1003, ¶ 69 (emphasis added).

Petition, 28

The First Time Petitioner Addressed “In Response To” Was In The Reply Brief

PO attempts to justify its new argument by alleging the Petition gave no notice that Vangemert alone teaches this limitation. But as identified in Section II above, the entire first paragraph of *the section devoted to this limitation* in the Petition addresses how Vangemert alone teaches this limitation while citing to Dr. Caloyannides’s Declaration similarly explaining how Vangemert alone teaches this limitation. See Paper 2 at 28; EX 1003, ¶¶ 68-69 (“Accordingly, Vangemert discloses generating ‘a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,’ as claimed.”). Even the introduction of the Petition’s alternative argument relying on Copeland, Paper 2 at 28 (“To the extent Vangemert is deficient, . . .”), demonstrates that the Petition’s initial argument for this limitation relies on Vangemert alone. PO’s attempted justification is thus refuted by the plain language of the Petition and the cited expert declaration; the assertion that PO lacked notice of this argument is not credible.

Motion to Strike, 3-4

Petitioner consistently explained Vangemert alone taught the above element of Claim 1. Pet. at 28 (“Vangemert teaches generating a flow control signal in the form of a buffer credit signal when the buffer has sufficient space for a new data frame.”); see also Ex. 1003, ¶ 69 (“Vangemert discloses generating ‘a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount,’ as claimed.”). In an abundance of caution, Petitioner explained, “[t]o the extent Vangemert is deficient, Copeland teaches overflow control by activating a signal upon the buffer capacity reaching a predetermined

Reply, 4

The Patent Owner Was Not Required To Respond To Arguments That Did Not Appear In The Petition

Unable to point to an allegation from the Petition that Vangemert met the actual claim language, the MTS cites a statement from the expert declaration filed with the Petition. See MTS, at 1-2. However, as explained in the Sur-Reply, PO is not obligated to respond to arguments not made in the Petition but are referenced only through citation to expert reports (see Sur-Reply, Footnote 7). Like the Petitioner in this case, the Petitioner in *3M Company v. Evergreen Adhesives, Inc.*, 860 Fed. Appx. 724 (Fed. Cir. 2021), sought to make an argument that “was not advanced in the briefing and [was] referenced only through citation to expert reports.” *Id.*, at 725. The Federal Circuit found that the Board properly rejected Petitioner’s strategy “as an attempt to introduce argument by citation to its expert declaration in violation of 37 C.F.R. §42.6(a)(3), the Board’s rule against incorporation by reference.” *Id.* As the Court explained:

The Reply quotes a statement from its expert to the effect that Vangemert discloses the “in response” to limitation. Reply, 4, citing Ex. 1003, ¶169. However, the Petition itself did not recite the same statement. Patent Owner was not required to respond to a position espoused by Petitioner’s expert that was not in the Petition itself.

Sur-Reply, 9

The Board’s rules concerning trial practice are set forth in 37 C.F.R. Chapter 1, Subchapter A, Part 42 (Trial Practice Before the Patent Trial and Appeal Board). Section 42.6 of the rules concerning Filing of Documents, regarding incorporation by reference, provides that “[a]rguments must not be incorporated by reference from one document into another document.” 37 C.F.R. § 42.6(a)(3). When promulgating § 42.6(a)(3), the Patent and Trademark Office explained that the rule “minimizes the chance that an argument would be overlooked and eliminates abuses that arise from incorporation and combination,” ..., and noted that without the rule, the Board would be forced to “play archeologist with the record” for arguments that might have been made outside the parties’ briefing. *Id.*, at 725-726 (emphasis added)(citations omitted).

3M Company v. Evergreen Adhesives, Inc., 860 Fed. Appx. 724 (Fed. Cir. 2021)

Petitioner's Characterization Of Vangemert Shows That It Doesn't Meet The Claim Element

Petitioner's Characterization of Vangemert	Claim Language
the bit credit signal is generated <u>when the available buffer space is sufficient</u> (equal to the fill amount) to accept the data word to be transmitted (emphasis added).	the module is operable to generate a flow control signal <u>in response to the amount of data stored</u> in the first buffer <u>equaling or exceeding</u> the fill amount (emphasis added).

Significantly, the Petition lacked any allegation that Vangemert met the actual claim language, which requires that a flow control signal be generated “in response to the amount of data stored in the first buffer equaling or exceeding the fill amount.” Instead, the Petition alleged that “the bit credit signal [in Vangemert] is generated when the available buffer space is sufficient. ...” In this context, there is a critical difference between generating a flow control signal “in response to” the action of stored data “equaling or exceeding the fill amount” and generating a flow control signal “when the available buffer space is sufficient” While Vangemert continually assesses the unoccupied buffer space and may generate advanced

permission signals “when” (at a time that) the unoccupied space equals a certain amount, in Vangemert, the generation of such signals is not triggered by the action of stored data in the buffer reaching or crossing a threshold, as claimed. This point was borne out in the prosecution history, where the Examiner found that claims patentable over, *inter alia*, Szatkowski which, for purposes of the claim limitation in question, is no different from Vangemert. POR,26-28. Since the Petition failed to allege that Vangemert mapped to the actual claim language, Petitioner's waiver argument is without merit.⁷

Sur-Reply, 9-10

Tachyon Is Not Included In Any Of The Asserted Grounds

Reference(s)/Basis	35 U.S.C §	Challenged Claim(s)
Vangemert ¹ , Copeland ²	§ 103	1, 2, 3, 4, 7, 15, 16, 17
Vangemert, Copeland, Dobson ³	§ 103	4
Vangemert, Copeland, Reay ⁴	§ 103	6

Dobson, Copeland	§ 103	1, 2, 3, 4, 7, 16
Dobson, Copeland, Reay	§ 103	6
Dobson, Copeland, Vangemert	§ 103	15, 17

¹ US Pat. No. 6,289,386 B1, Sep. 11, 2001 (Ex. 1005).

² US Pat. No. 5,179,661, Jan. 12, 1993 (Ex. 1006).

³ US Pat. No. 5,717,870, Feb. 10, 1998 (Ex. 1007).

⁴ US Pat. No. 6,005,414, Dec. 21, 1999 (Ex. 1008).

Petitioner Is Not Using The Tachyon Article To “Interpret” Vangemert

The Tachyon article teaches that an ACK signal increments an end-to-end count, which “determines the number of frames that Tachyon can send to the remote designation without receiving an ACK.” Ex. 1014 at 102. Thus, the ACK signal corresponds to the Vangemert BCCW. Ex. 1013, ¶ 36.

Reply, 13

An “ACK signal” is an acknowledgement that is sent after a previous transmission was received that confirms receipt³ -- which is indisputably different from Vangemert’s “buffer credit control word,” which a node must receive before it can transmit. The Reply attempts to analogize these different signals from Tachyon and Vangemert, referring to them as “corresponding.” Reply, 13 (“the ACK signal corresponding to Vangemert’s BCCW.”) In doing so, the Reply crosses the line from using Tachyon to “interpret” what Vangemert meant, to using Tachyon to fill a hole in Vangemert. In this respect, the Reply reads like a classic obviousness rejection seeking to combine references with different architectures based on various motivations or suggestions:

Sur-Reply, 5

Unlike in Cisco Sys., Inc. v. Crossroads Sys. Tachyon was not included in the Petition

PO introduced a 1996 article entitled “An Introduction to Fibre Channel” as Exhibit 2012. Page 5 of Exhibit 2012 references “Article 12” of the Hewlett-Packard Journal, which was published in the same October 1996 HP Journal, but was not cited by PO. “Article 12” in the Journal is entitled “Tachyon: A Gigabit Fibre Channel Protocol Chip” (the “Tachyon article”), and the two articles share a common author in addition to being published concurrently.² Compare Ex. 2012 at 5 with Ex. 1014 at 96.

Reply, 12

² The Board has even considered Exhibit 2012 and the Tachyon article as a single reference in a past IPR because they were published at the same time in the same journal and share a common author, with the Tachyon article providing a continuation of Exhibit 2012. *See Cisco Sys., Inc. v. Crossroads Sys., Inc.*, IPR2014-01463, Paper No. 49 at 2 n.3 (P.T.A.B. Mar. 16, 2016).

While the Reply states that “issues relating to latency, system integrity and system failure dictate a design bypassing data buffers,” the Reply does not state that it is inherent in Vangemert that Tachyon’s ACK functionality must necessarily be used to implement Vangemert’s buffer credit control word transmissions. Nor could Petitioner take such a position. Tachyon represents but one implementation of the Fibre Channel protocol, and the record is devoid of evidence that Tachyon’s specific buffer architecture is necessarily required by that protocol. The lack of an inherency argument underscores that Petitioner is not “interpreting” Vangemert -- rather, Petitioner is arguing that the specific implementation of the Fibre Channel protocol in Tachyon together with Vangemert renders the limitation at issue obvious.

Sur-Reply, 6

Vangemert's Buffer Credit Signal And Buffer Credit Control Words Are Different Signals

2

credit calculation. In one embodiment, a system network is provided with a remote node coupled to a local node by a serial communications link. The remote node is configured to transmit a data frame to the local node only if the remote node receives a buffer credit which indicates that the local node has available receive buffer space for a data frame. The local node includes a network interface unit for coupling to the serial communications link, and the network interface unit includes a receive buffer, a receive controller, a transmit controller, and a buffer credit manager. The receive controller stores incoming data frames in the receive buffer until they can be forwarded to the i/o bus of the local node. The transmit controller is configured to send buffer credits to the remote node in response to a credit signal from the buffer credit manager. The buffer credit manager is coupled to the receive controller to receive a receive flag for each data frame which is completely received by the receive buffer, and is also coupled to the transmit controller to receive a transmit flag for each buffer credit sent. The buffer credit manager iteratively determines the additional committed buffer space (i.e. the space committed but not yet occupied by receive data) by counting the number of receive and transmit flags, and generates the credit signal using a comparator which compares the sum of additional committed buffer space and the maximum frame size to the available receive buffer storage capacity and asserts the credit signal if the available buffer space is greater than or equal to the sum of the maximum frame size and the additional committed buffer space.

1005, Col. 2

One embodiment of a network interface unit is provided in FIG. 4. It includes an encoder 402 and a decoder 404 coupled to the transceiver 300. Encoder 402 and decoder 404 provide error correction coding and decoding for information transmitted across the serial link. Decoded data from decoder 404 is provided to receive controller 406. Receive controller stores received control words and data frames in receive buffer 408. If the node is in a "pass along" mode, the receive buffer 408 is also used as a transmit buffer 410. A transmit controller 412 retrieves control words and data frames from transmit buffer 410 and forwards them to encoder 402. If the node is transmitting or receiving data (i.e. participating in an exchange of data), receive controller 406 creates or updates exchange information in exchange tables 416 in response to received control words or data frames, and forwards data from received data frames to the node's i/o bus. Transmit controller 416 creates or updates exchange information in exchange tables 416 in response to commands and data from the node's i/o bus, generates control words and data frames in transmit buffer 410, and forwards them to encoder 402. The exchange tables 416 are used to track non-concurrent sequences of data frames that are related to a specific exchange. A protocol interface manager 414 is provided to manage exchanges in a way suitable to provide operations specified in a higher level protocol used by the i/o bus. One such protocol, SCSI, includes such operations as FORMAT UNIT, INQUIRY,

1005, Col. 3

Also shown in FIG. 4 is a buffer-credit manager 418. As described previously, before an initiating node can transmit a data frame to a responding node, it must first secure a buffer credit from that node. Consequently, when receive controller 406 receives a control word indicating that a remote node wishes to transmit data, the buffer credit manager 418 is enabled, and the transmit controller 412 begins transmitting buffer credit control words in response to a credit signal from buffer credit manager 418. At the beginning of an exchange, the receive buffer 408 is empty of data frames, and the buffer credit manager 418 is provided with the negotiated frame size and the receive buffer capacity, and it is expected to generate and manage a number of buffer credits at least equal to the maximum receive buffer capacity divided by the frame size, with as little delay as possible.

1005, Col. 4

Accordingly, a POSITA would understand that in Vangemert's system, the buffer credit control words (and not credit control signal) serve as the flow control signals for transport on the serial link. It is explicitly stated that the transmit controller generates control words in the transmit buffer. Additionally, it is reiterated that the transmit controller retrieves these control words from the buffer and forwards them to the encoder for transmission on the transmit channel. From this, a POSITA would clearly comprehend that Vangemert's credit control signal is not transmitted over the I/O bus (serial link). (Ex. 2002, 107).

"DEMONSTRATIVE EXHIBIT - NOT EVIDENCE"

Reply, 36

The Petition Failed To Show That Vangemert's Flow Control Signal Does Not Pass Through The Second Buffer

Vangemert teaches that the transmit controller 412 transmits buffer credit control words received directly from the buffer credit manager 418 and passes them directly to the encoder 402, which sends them to the transmitter 312. EX. 1003, ¶ 77. The transmitter 312 then outputs the buffer credit signal (i.e., flow control signal) to other devices via the serial link. *Id.* Vangemert does not disclose or suggest that the buffer credit signal or associated buffer credit control words are ever stored in or passed through the transmit buffer 410 (second buffer). *Id.* Rather, Vangemert teaches that when the buffer credit manager is enabled in response to a request to transmit data from a remote device, “the transmit controller 412 begins transmitting buffer credit control words in response to a credit signal from buffer credit manager.” EX. 1005, col. 4:11-16. This teaches that the transmit controller 412 outputs data directly upon receiving it from the bit credit manager 418. EX. 1003, ¶¶ 77-78. This efficient transfer of the bit credit signal from the bit credit manager 418 through the transmit controller 412 aids in maintaining the minimum latencies Vangemert desires. EX. 1003, ¶ 79. Pet.,30-31 (emphasis added).

Sur-Reply, 1-2

not stored in or passed through the transmit buffer 410 (second buffer). To the extent

Vangemert is silent or ambiguous as to whether or not the flow control signal passes

through the second buffer, Vangemert does not meet the claim limitation. *Dynamic*

Drinkware, L.L.C. v. Nat’l Graphics, Inc., 800 F.3d 1375, 1378-79 (Fed. Cir. 2015)

(“If the fact trier of the issue is left uncertain, the party with the burden loses”).²

The Petitioner erroneously alleges that “Vangemert does not disclose or suggest that the ... buffer credit control words are ever stored in or passed through the *transmit buffer 410* (second buffer).” (Petition, 31). Vangemert says the opposite: “A transmit controller 412 retrieves control words and data frames from transmit buffer 410 and forwards them to encoder 402.” (Ex. 1005, 3:49-52) Vangemert similarly states: “Transmit controller 416 creates or updates exchange information in exchange tables 416 in response to commands and data from the node’s i/o bus, generates control words and data frames in transmit buffer 410, and forwards them to encoder 402”. (Ex. 1005, 3:57-61). Furthermore, “Vangemert clearly explains that the transmit controller transmits credit control words to devices connected to the I/O bus via the transmit buffer (410) in response to the internal credit control signal generated by the comparator (502).” (Ex. 1005, 4:11-16, Ex. 2002, 103). Accordingly, Vangemert teaches that the control words pass through the transmit buffer 410. POR, 34 (emphasis added).

Sur-Reply, 3

Sur-Reply, 3

Petitioner Has Failed To Show That Vangemert's BCCW Are Treated Differently Than Other "Control Words"

Petitioner alleged that "[n]othing in Vangemert suggests the BCCW is treated the same as other, more general "control words" associated with data frames." Reply, 9. However, Petitioner adduced no evidence that they are necessarily treated differently. Vangemert never creates a distinction between the transmission of control words in general and buffer credit control words. For example, Vangemert states that it "is sufficient to stipulate that the fabric switch 114 transports data frames and control words from the transmit channel of a source node to the receive channel of a destination node." (Ex. 1005 2:65-3:1). There is no evidence in Vangemert of how the buffer credit control words get transmitted on the serial link (transmit and receive channel) unless they are included in the "control words" described in Vangemert.

Sur-Reply, 11

Petitioner's Expert Attempts To Fill Gaps In Vangemert By Making Conclusory Assumptions About The Operation Of Vangemert That Are Not Grounded In The Reference Or Record

One of skill would have understood the Vangemert transmit buffer is a FIFO buffer. Ex. 1013, ¶ 25. Because most communication protocols do not limit the size of transfer buffers, the time required for a flow control signal to pass through the buffer is unknown—e.g., it would take longer for a flow control signal to pass through a large buffer than it would take to get through a small buffer. *Id.* Having unbounded times for control signals to get delivered is not a sound protocol design and makes the protocol exceedingly challenging to validate. *Id.* This would also have led one of skill to have thought it illogical to interpret Vangemert to require the BCCW to pass through the transmit buffer. *Id.*

Reply, 11

Petitioner recognized that Vangemert does not teach the missing element of how BCCW is transmitted. In the Reply, Petitioner's expert attempts to fill this gap by making conclusory assumptions about the operation of Vangemert that are not grounded in the reference or any other exhibit. The first conclusory assumption is that "[a] POSITA would have understood that the Vangemert transmit buffer was a FIFO buffer. Ex. 1013, ¶25. That assertion lacks any citation or supporting reasoning and is, therefore, by definition, conclusory. Among other alternatives, Petitioner's expert does not address why Vangemert's transmit buffer could not have been implemented using, for example, a *priority queue* where control signals like buffer credit control words are given a higher priority, causing them to be inserted into the buffer queue ahead of other data.⁸ Such an approach would have solved the problems identified by Petitioner's expert (e.g., "unbounded times for control signals to be delivered" (see, Ex. 1013, ¶25)) without use of a FIFO buffer. An "expert's "conclusory statements and unspecific expert testimony d[o] not qualify as substantial evidence that could support the Board's conclusions regarding obviousness." *TQ Delta, L.L.C. v. Cisco Sys.*, 942 F.3d 1352, 1360-61 (Fed. Cir. 2019).

Facts are similar to Precedential Decision of Xerox Corp. v. Bytemark, Inc

In lieu of substantial evidence, Petitioner offers conclusory statements of its expert, which copies, word-for-word, Petitioner's conclusory assertions about Vangemert's buffer. *Compare*, Reply, 10 with Ex 1013, ¶25. In *Xerox Corp. v. Bytemark, Inc*, IPR2022-00624, Paper 9 (August 24, 2022) and Paper 12 (February 10, 2023) (designated Precedential) the PTAB rejected similar conclusory expert gap filing. There, like in the present case, Petitioner offered a declaration that "copies, word-for-word, Petitioner's conclusory assertions" and "sets forth Petitioner's conclusory assertions as though they are facts, rather than setting forth facts and evidence in support of Petitioner's assertions." Therefore, the PTAB held, and Director Vidal affirmed, that "the cited declaration testimony is conclusory and unsupported ...and is entitled to little weight."

Sur-Reply, 14

Here, Petitioner's leaps (e.g., Vangemert's transmit buffer is FIFO, and the BCCW bypasses the FIFO Buffer) to span the gap of the missing elements in Vangemert are unsupported by Vangemert or anything other than Ex 1013. Therefore, Petitioner has only offered conclusory statements and no substantial evidence that could support a finding of obviousness.

"DEMONSTRATIVE EXHIBIT - NOT EVIDENCE"

Vangemert 's Transmit Buffer Is Not Inherently FIFO

With respect to whether Vangemert's transmit buffer 410 is inherently FIFO, Petitioner hasn't even offered a conclusory statement that that is the case. "[T]he use of inherency ... must be carefully circumscribed in the context of obviousness" and "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency." *Par Pharm., Inc. v. TWi Pharms., Inc.*, 773 F.3d 1186, 1194-95 (Fed. Cir. 2014) (internal markings and citations omitted); *see also Southwire Co. v. Cerro Wire L.L.C.*, 870 F.3d 1306, 1310-11 (Fed. Cir. 2017). Inherency cannot be established by the fact that something may happen. Instead, the alleged feature must necessarily be present in the reference.

Here, Petitioner has offered no evidence or argument for why Vangemert's transmit buffer is not, e.g., **an addressable buffer** would allow different classes of service levels as supported by Fibre Channel (*see*, Ex. 2012, 6), **a random access memory**¹⁰ that is used to provide a shared buffer of control words, including BCCW and data frames, or **a priority queue** (*see*, Section IV(B)). Since Petitioner has failed to explain why a POSITA would not understand these as other possible implementations of Vangemert's transmit buffer, Petitioner has failed to show that Vangemert's transmit buffer is inherently a FIFO buffer.

Sur-Reply, 15

Copeland Is Relied Upon For The Same Flow Control Mechanism As Daines

In sum, Vangemert-Copeland provides “a more complete combination of the claimed elements than any other reference before the examiner” such that the combination cannot be considered cumulative. MPEP § 609.04(a).

MPEP 609.04(A)
CONTENT REQUIREMENTS FOR AN INFORMATION DISCLOSURE
STATEMENT

Reply, 22

Szathkowski discloses all the limitations as the above but does not explicitly disclose wherein the ASIC is configured to determine whether an amount of data stored in the first FIFO register equals or exceeds a fill amount associated with a storage capacity of the first FIFO register. However, Daines discloses this. (col.4, lines 4-17, i.e., a flow control mechanism comprising level indicators for the input buffers for indicating the amount of data stored in a buffer and a flow control device for monitoring the level indicators to determine if the amount of data in an input buffer crosses a first threshold).

It would have been obvious to an ordinary person skilled in the art at the time of the invention was made to incorporate the teachings of Daines with the teaching of Szathkowski to have control mechanism to determine the level indicators for the buffers for indicating the amount of data stored for comparison the threshold not to exceed would have been obvious because it would enhance the system of Szathkowski to increase more functionality to prevent overloaded data in system. (Ex. 1002, at 185-186). (emphasis added).

POR, 26-27

The Patent Was Not Allowed Because Of A Connector

A connector is not inherently a part of a serial link. For example, Szatkowski adapter 10 and controller 20 may be mounted to the same printed wiring board, e.g., without a connector. In addition, it is well known for wires to be directly soldered to a printed wiring board, e.g., without a connector. Accordingly, a connector is not inherently a part of a serial link.

1002, 231

Had the Examiner not been convinced of the flaws in combining Szatkowski-Daine, all the Examiner would have had to do was locate a reference, such as the R232 standard, that taught that serial ports have serial connectors. Clearly, the Examiner allowed the case because the Examiner was convinced that the rationale for combining the references was flawed.

Sur-Reply, 18

There is No Motivation To Combine Vangemert and Copeland

Specifically, a POSITA would understand that “Vangemert teaches a flow control scheme based on buffer credits, which makes overflow impossible” and “Copeland teaches using a flow control signal to stop transmission to avoid a possible overflow, (i.e., in a system where overflow is possible). (Ex. 2002, 72). Accordingly, there would be no purpose in using a flow control signal to stop potential overflow when overflow is not possible, and therefore, the teachings of Vangemert and Copeland are divergent, and there is no motivation to combine Vangemert’s and Copeland’s flow control solutions.” (Ex. 2002, 72).

Reply, 19

Accordingly, combining Vangemert and Copeland would be contradictory and counterproductive. Vangemert’s solution already addresses and eliminates the issue of receiver buffer overflow in data communication. Therefore, adding Copeland’s flow control signal, which is designed to prevent such overflow, would be redundant. Moreover, even if these two methods were combined, incorporating Copeland’s flow control would lead to increased latencies in data transmission, contradicting the efficiency sought in the Petitioner’s proposal. Consequently, the combination of these two approaches does not align logically or functionally. (Ex. 2002, 120).

Reply, 25

Petitioner Has Failed To Address Why A POSITA Would Implement Two Possibly Contradictory Control Systems

All Petitioner offers is the conclusory speculation from its expert that “the predetermined flow control threshold of Copeland may be set such that if there is miscalculation, or some sort of timing issue with the bit credit system of Vangemert such that the buffer begins to reach its maximum capacity, the flow control system of Copeland may instruct the transmitting device to stop transmitting to prevent a potential loss of data due to buffer overflow.” Ex 1003, [0073]. However, since Vangemert requires that a buffer credit be received in advance by the sending node *before* transmission, it is simply impossible for there to be a buffer overflow. See Ex. 1005, 1:49-54 and Ex. 2002, ¶84. **Petitioner’s expert provides no explanation how “miscalculations” or “timing issues” in Vangemert could lead to an overflow scenario, or how a POSITA would have recognized such a problem based on the disclosure in Vangemert.** Nor does Petitioner’s expert provide any citations to authorities that identify even the possibility of “miscalculations” or “timing issues” in Vangemert leading to an overflow scenario. Instead, all that is offered is unsupported speculation.

Further, Petitioner’s expert does not address the reasons why a POSITA would not implement two potentially contradictory flow control systems. For example, if buffer credits are available, then transmission could occur in one system, but the buffer capacity level flow control signal could terminate transmission, which would reduce the effective transmission bandwidth of a buffer credit system alone. See, Ex. 2002, ¶¶58, 59 and 120. **This would be like having a traffic light simultaneously showing both a green and red light.** A POSITA would not be motivated to utilize Vangemert’s credit control system with Copeland’s overflow control because they could send contradictory signals to the network.

Sur-Reply, 18-19

Dobson's internal signal on line 132 cannot be "the flow control signal" because it is not transmitted "through the serial link and the connector."

Claim 1 specifies the requirements of "the serial link" as follows:

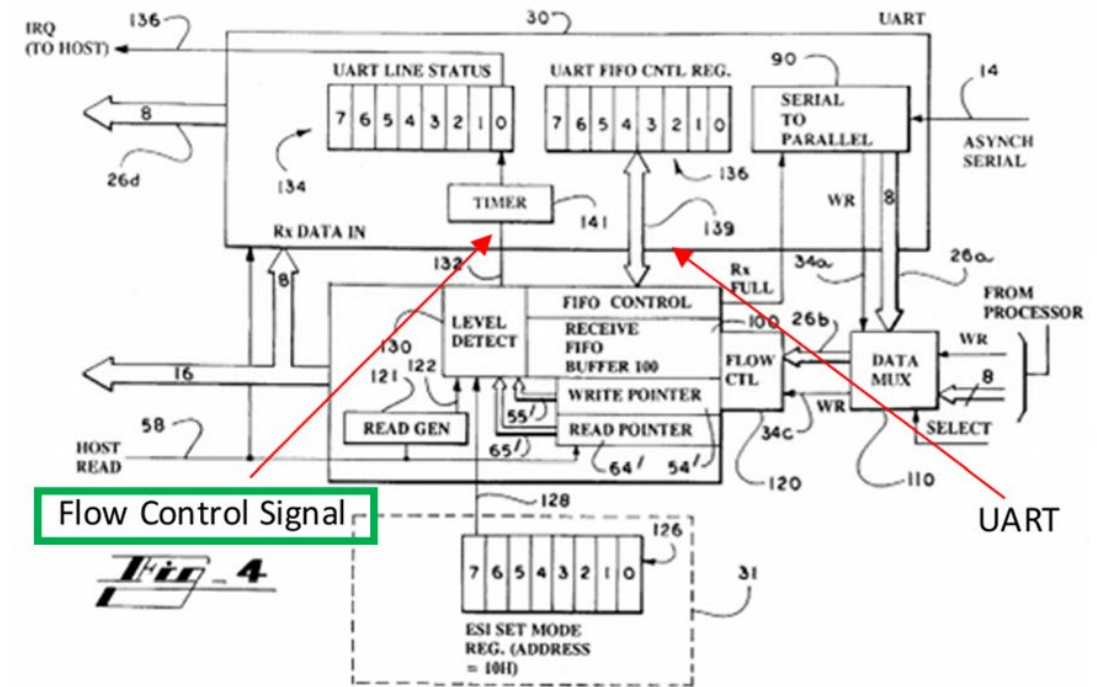
... a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, ...

a receiver operable to receive the first serial data from the serial link ...

a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and

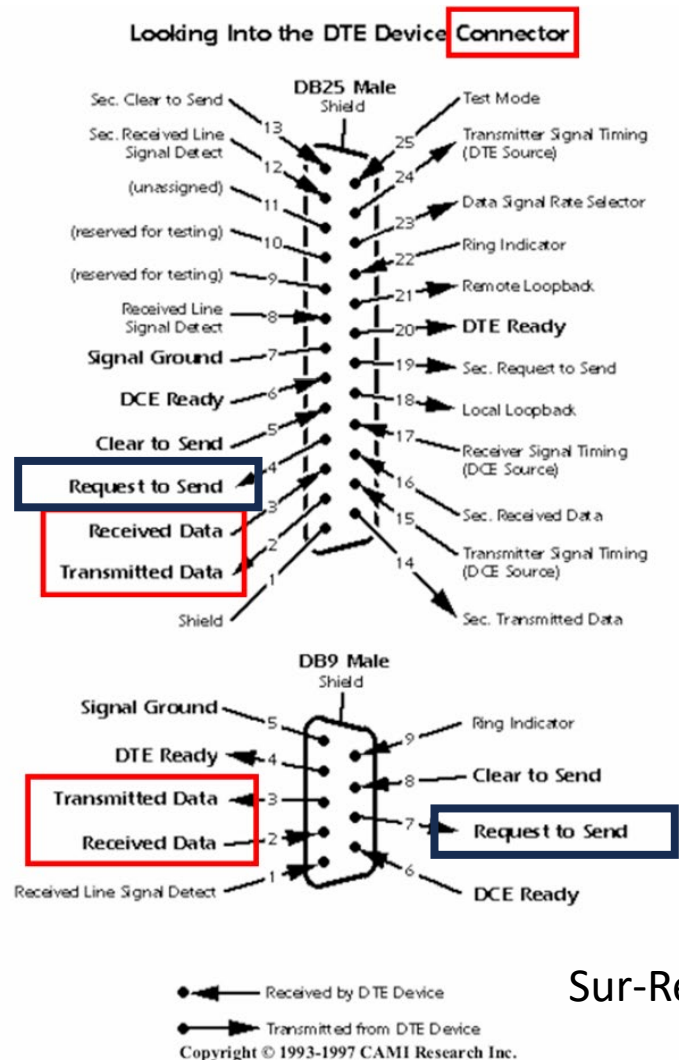
a transmitter operable to transmit the second serial data to the serial link through the connector; ...

wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.



Sur-Reply, 20-21

Copeland Does Not Teach Transmitting “The Flow Control Signal Through The Serial Link”



Sur-Reply, 22

In connection with Copeland, Petitioner has failed to show that the serial link (i.e., the data connection) carrying the serialized data also carries the flow control signal, as claimed. While the claim distinguishes between the “serial link” and the “connector,” Petitioner conflates them. Ex. 2002, ¶117. **While the RTS flow control signal is transmitted through the serial port connector -- it is not carried on the wires that form the “serial link” carrying the serialized data.** As explained by Terry Lee, a POSITA would know that RTS is a parallel out-of-band handshake signal used in RS-232, which is transmitted on a separate out-of-band connector pin from the serial data signals, RXD or TXD. *Id.* “DTE, DCE, CTS, and RTS are asynchronous level sensitive signals which indicate the status of the equipment based on the voltage level. Level sensitive signals differ from a serial bitstream where the symbol on the line can change sequentially with each symbol time.” Ex 2002, ¶96; POR, 29.

Sur-Reply, 24

As explained by Terry Lee, a **“ POSITA would also know that RTS is a parallel out-of-band handshake signal used in RS-232,” which is transmitted “on a separate out-of-band connector pin from the serial data signals, RXD or TXD.”** (Ex. 2002, 155). Accordingly, a POSITA would appreciate that the control signal for Copeland is not transmitted through the serial link as required by the Challenged claims. (Ex. 2002, 116).

Reply, 37-38

Vangemert Overview

Specifically, Vangemert describes that “[t]he buffer credit manager iteratively determines the additional committed buffer space (i.e., the space committed but not yet occupied by receive data) by counting the number of receive and transmit flags, and generates the credit signal using a comparator which compares the sum of additional committed buffer space and the maximum frame size to the available receive buffer storage capacity and asserts the credit signal if the available buffer space is greater than or equal to the sum of the maximum frame size and the additional committed buffer space.” (Ex. 1005, 2:19-29; Ex. 2002, 56) Vangemert’s buffer credit manager is graphically depicted in Figure 5

Accordingly, Vangemert describes a system where the buffer credit manager issues credits in proportion to the available space in the receiver’s buffer. If there is no space in the buffer of the receiver, the transmitter cannot transmit. As a result, the buffer credit manager makes buffer overflows impossible. (Ex. 2002, 58).

Since the data storage required for completely received frames is accounted for in the available buffer space, the buffer credit manager doesn’t need to continue reserving space for it. **Since the actual amount of stored data is being used in this iterative buffer-credit management strategy, more efficient use of the buffer space is possible.** When the size of the received data frames is less than the maximum frame size, the extra space can add up to allow additional buffer credits to be sent. Using this strategy, the number of credits made available by the buffer credit manager is at least equal to the maximum buffer capacity divided by the frame size, but it may be greater when received data frames are smaller than the maximum frame size. Importantly, the credits are generated quickly since only additions, subtractions, and comparisons are used. This incremental “one-more-credit?” evaluation is well suited to the serial communication channel since only one credit can be sent at a time anyway. The hardware implementation of this buffer credit manager is advantageously fast, simple and inexpensive. (Ex. 1005, 4:52-5:4)

POR, 9-12

Copeland Overview

Copeland's mechanism involves a UART (Universal Asynchronous Receiver-Transmitter) with a BAUDOUT signal, a clock at 16 times the baud rate. A counter tracks BAUDOUT cycles, and when 1024 cycles pass without the FIFO (First In, First Out) buffer emptying, an output signal is triggered. This count of 1024 BAUDOUT cycles equals 64 bit times or 6.4 character times. This leaves about 9.6 character times for the remote transmitter to stop before the FIFO buffer overflows. Ex. 1006, 5:28-40. The system taught in Copeland also includes sending a low signal for the RTS (Ready To Send) and DTR (Data Terminal Ready) signals on the serial port, instructing the remote transmitter to stop sending data and thereby preventing data overflow in the UART's FIFO buffer. (Ex. 1006, 5:51-55; Ex. 2002, 88)

POR, 23

As a result, "a POSITA would understand that as the buffer becomes relatively full, a signal is sent to the transmitter to stop transmitting data frames so receive buffer overflow could be avoided, and that a certain amount of latency, 9.6 character times in the preferred embodiment, is provided for the transmitter to respond to avoid the receive buffer overflow." (Ex. 2002, 88)

After a predetermined number of BAUDOUT cycles are counted without the FIFO buffer being empty an output of the counter is enabled which disables the counter. This output deasserts the DTR and/or RTS signals to the remote transmitter. This signals the remote transmitter to stop sending. The enabling of the counter output thus results in the remote transmitter halting its transmission of data. (Ex. 1006, 2:56-63).

POR, 13

POR, 23

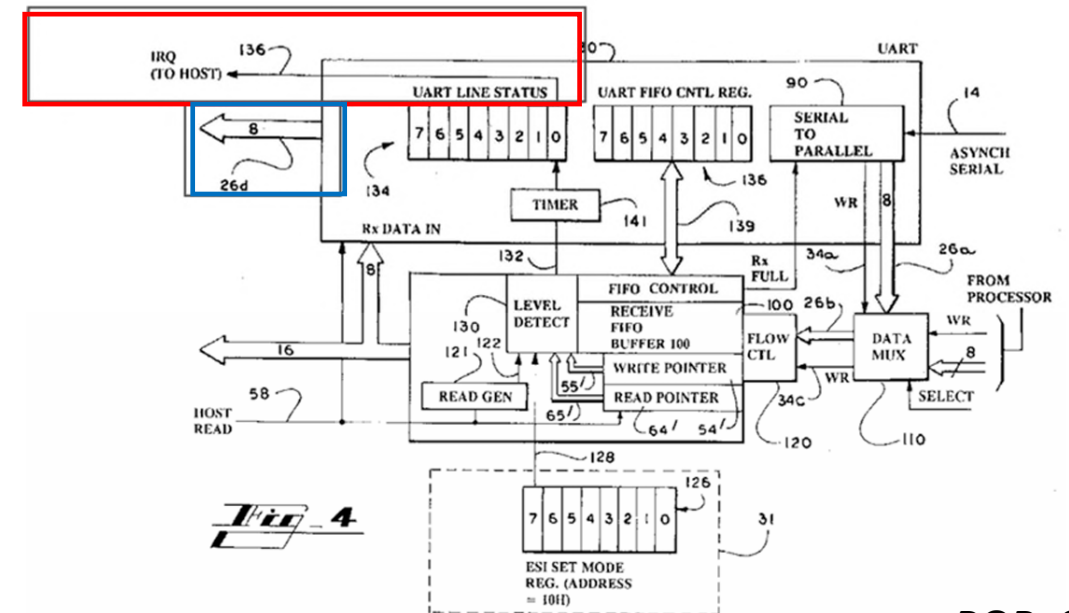
Dobson Overview

In contrast to the IRQ signal sent over line 136, Dobson explains that data from the FIFO buffer is transmitted to the host personal computer 8 via receive data bus 26d. For example, Dobson explains that “[r]eceived data is passed from the receive FIFO buffer 100 to the host personal computer 8 via the receive data bus 26d, bus interface circuit 20, and data bus 12.” (Ex. 1007, 7:61-64) Dobson’s system, where the Interrupt (labeled as IRQ) is transmitted to the computer over line 136 (red) and data is received over a different 8-bit wide parallel data bus 26d (blue), is graphically depicted in Figure 4 (annotated below).

POR, 39

The level detect circuit 130 outputs receive data ready signal on line 132 to bit 0 in the UART line status register 134. Bit 0 in the UART line status register 134 is passed to the host computer 8 on line 136 as an interrupt request. The host computer 8 responds to the interrupt request on line 136 by reading data from the receive HFO buffer 100, as set forth below. (Ex. 1007, 8:30-39 (emphasis added), Ex. 2002, 126)

POR, 38-39



POR, 39

Representative Claim

- 1. A system, comprising:
- a connector configured to be connectable to a serial link; and
- a module coupled to the connector, wherein the module is operable to receive first serial data transmitted over the serial link through the connector and transmit second serial data to the serial link through the connector, and wherein the module includes:
- a receiver operable to receive the first serial data from the serial link through the connector;
- a first circuit configured to deserialize the first serial data to generate deserialized data;
- a decoder configured to decode the deserialized data;
- a first buffer operable to store data that has been deserialized and decoded by the first circuit and the decoder, respectively;
- a second buffer operable to receive data, wherein the second buffer is in data communication with a second circuit that is configured to serialize data received via the second buffer to generate the second serial data; and
- a transmitter operable to transmit the second serial data to the serial link through the connector;
- wherein the module is configured to determine whether an amount of data stored in the first buffer equals or exceeds a fill amount associated with a storage capacity of the first buffer; and
- wherein the module is operable to generate a flow control signal in response to the amount of data stored in the first buffer equaling or exceeding the fill amount, and wherein the module is further configured to transmit the flow control signal through the serial link and the connector without passing the flow control signal through the second buffer.