TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number			
Filing Date	November 21, 2017		
First Named Inventor	Hyun Lee		
Title	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS		
Art Unit			
Examiner Name			
Attorney Docket Number	N3044.10009US05		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/JAMIE J. ZHENG/	**Date**	November 21, 2017
Name	Jamie Zheng	**Telephone**	(435) 252-1360
Registration Number	51167		

MASCHOFF BRENNAN, PLLC
1389 Center Drive, SUITE 300
PARK CITY, UTAH 84098, USA

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number.**

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

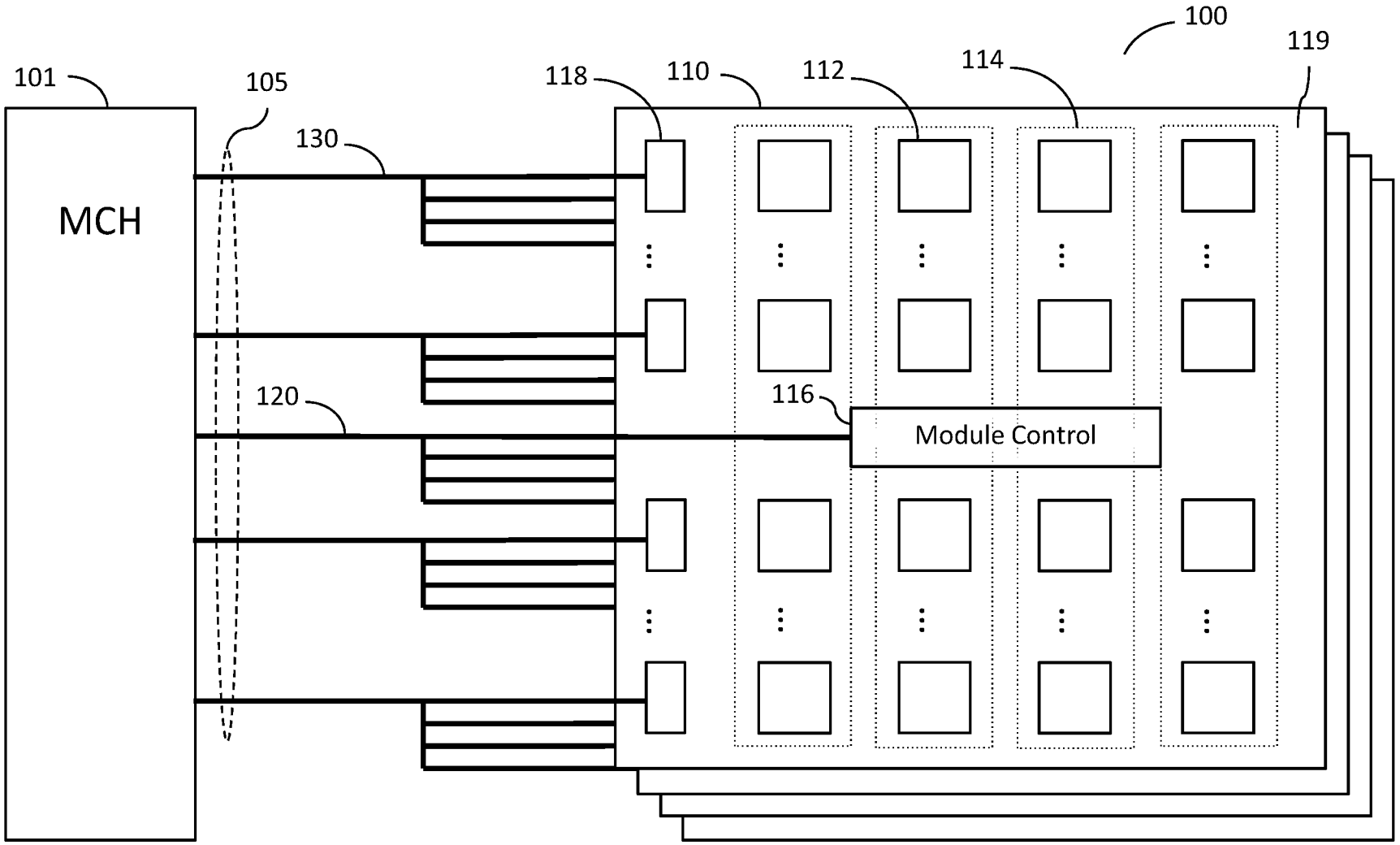

FIG. 1

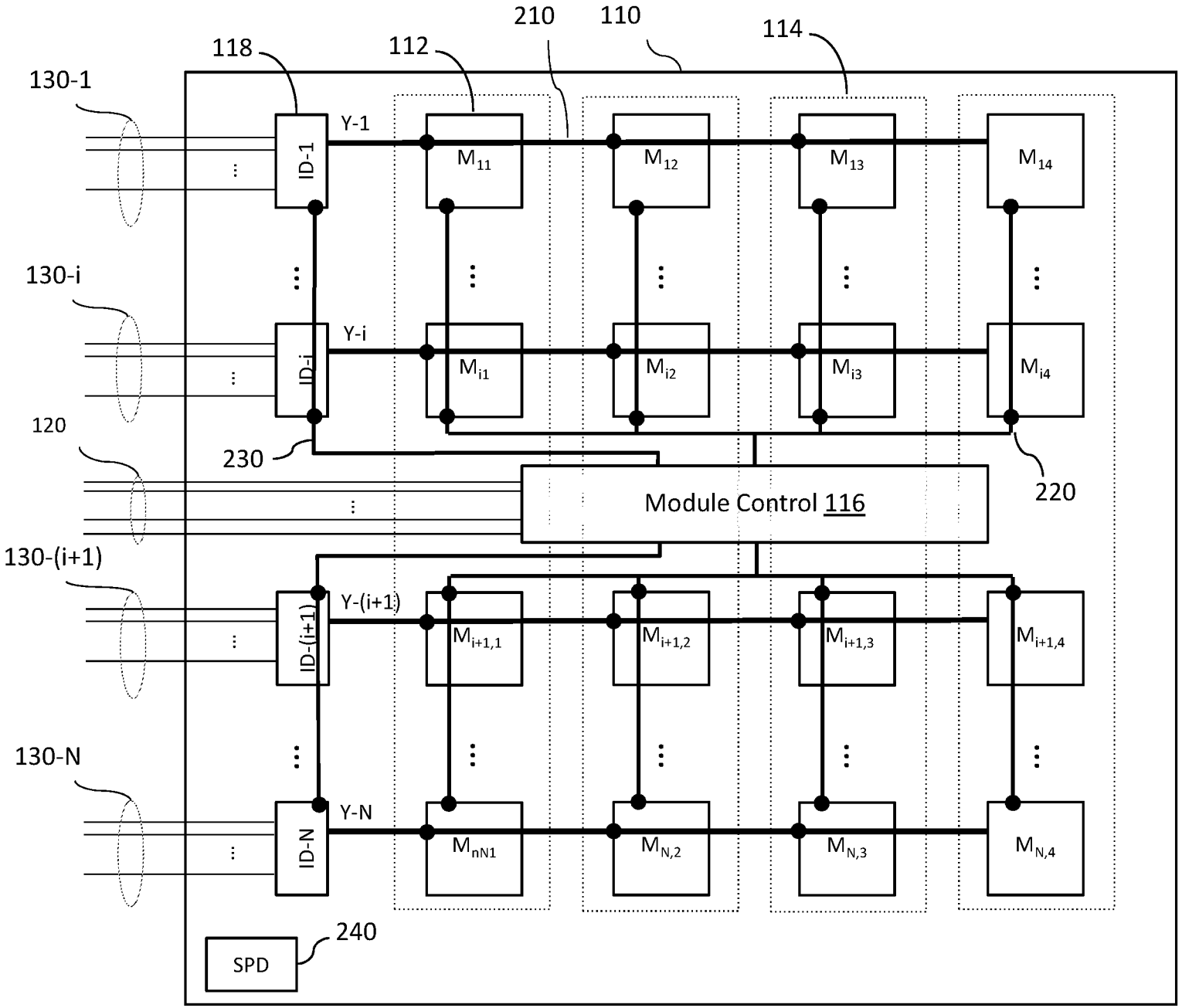
210
110
114
118
112
130-1
Y-1
ID-1
M11
M12
M13
M14
130-i
Y-i
ID-i
Mi1
Mi2
Mi3
Mi4
120
230
220
Module Control 116
130-(i+1)
Y-(i+1)
ID-(i+1)
Mi+1,1
Mi+1,2
Mi+1,3
Mi+1,4
130-N
Y-N
ID-N
MnN1
MN,2
MN,3
MN,4
240
SPD

FIG. 2A

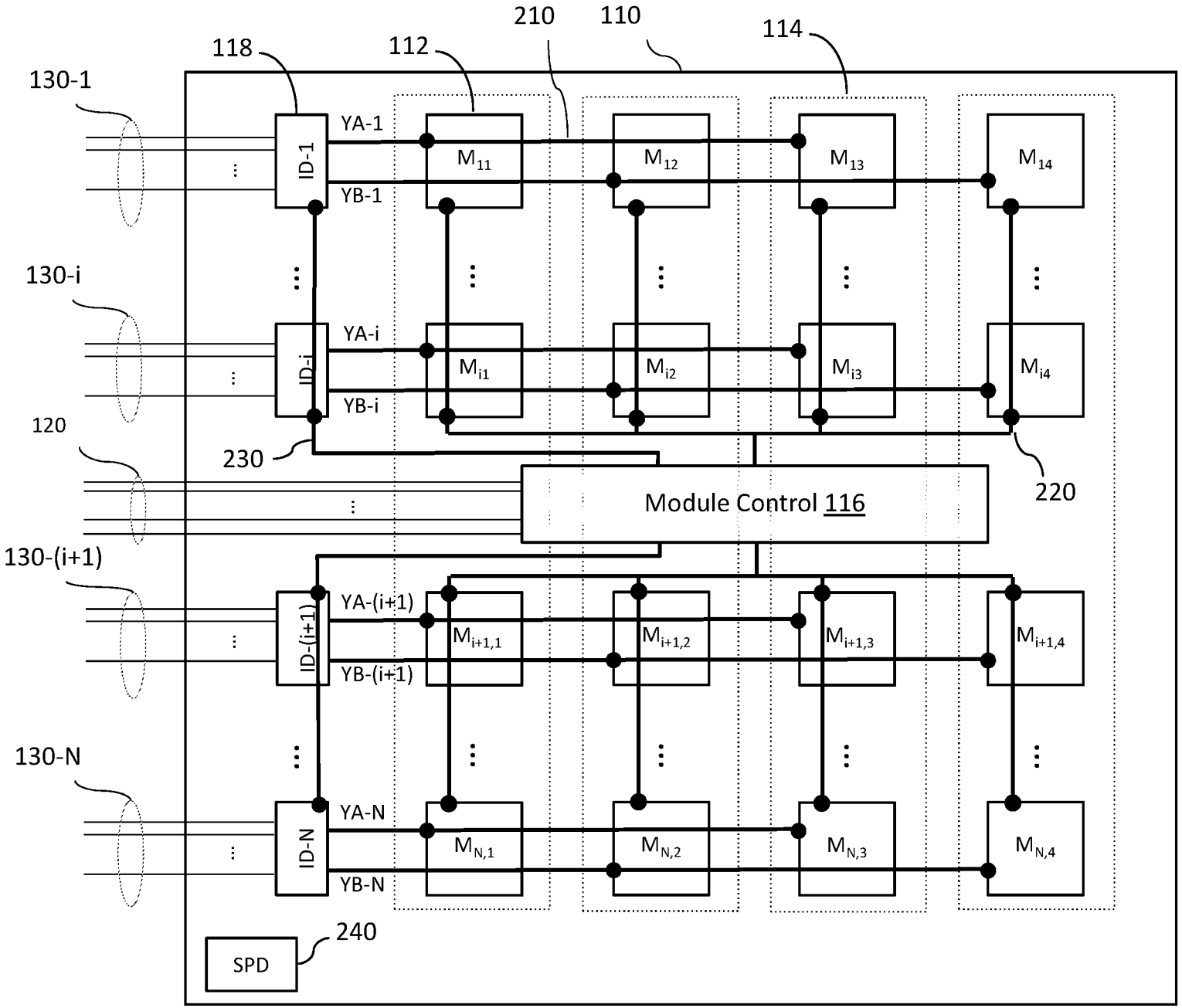
210
110
114
118
112
130-1
YA-1
ID-1
YB-1
M11
M12
M13
M14
130-i
YA-i
ID-i
YB-i
Mi1
Mi2
Mi3
Mi4
120
230
220
Module Control 116
130-(i+1)
YA-(i+1)
ID-(i+1)
YB-(i+1)
Mi+1,1
Mi+1,2
Mi+1,3
Mi+1,4
130-N
YA-N
ID-N
YB-N
MN,1
MN,2
MN,3
MN,4
240
SPD

FIG. 2B

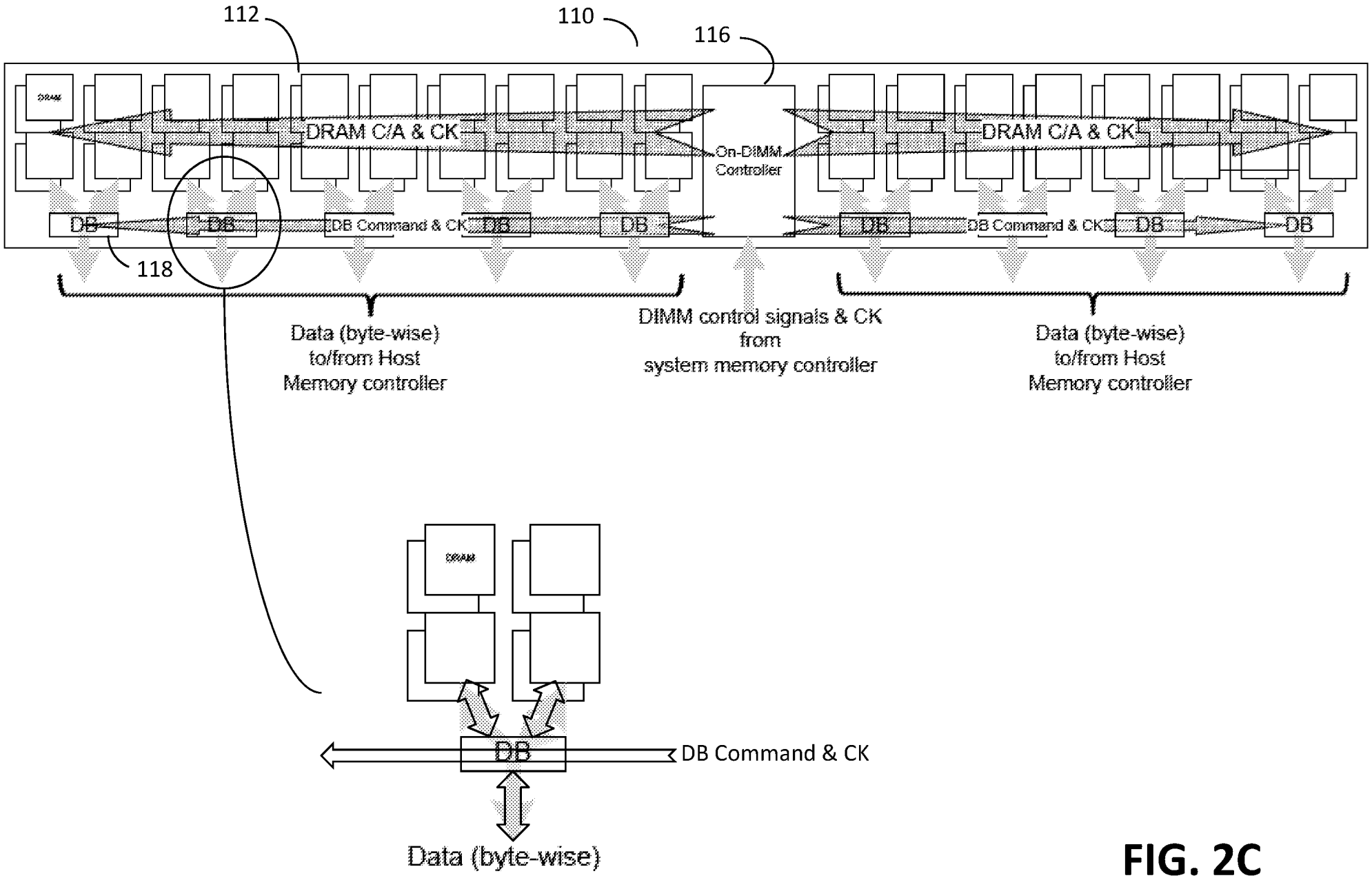
112
110
116
DRAM C/A & CK
On-DIMM Controller
DRAM C/A & CK
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
DB
DB Command & CK
Data (byte-wise)

FIG. 2C

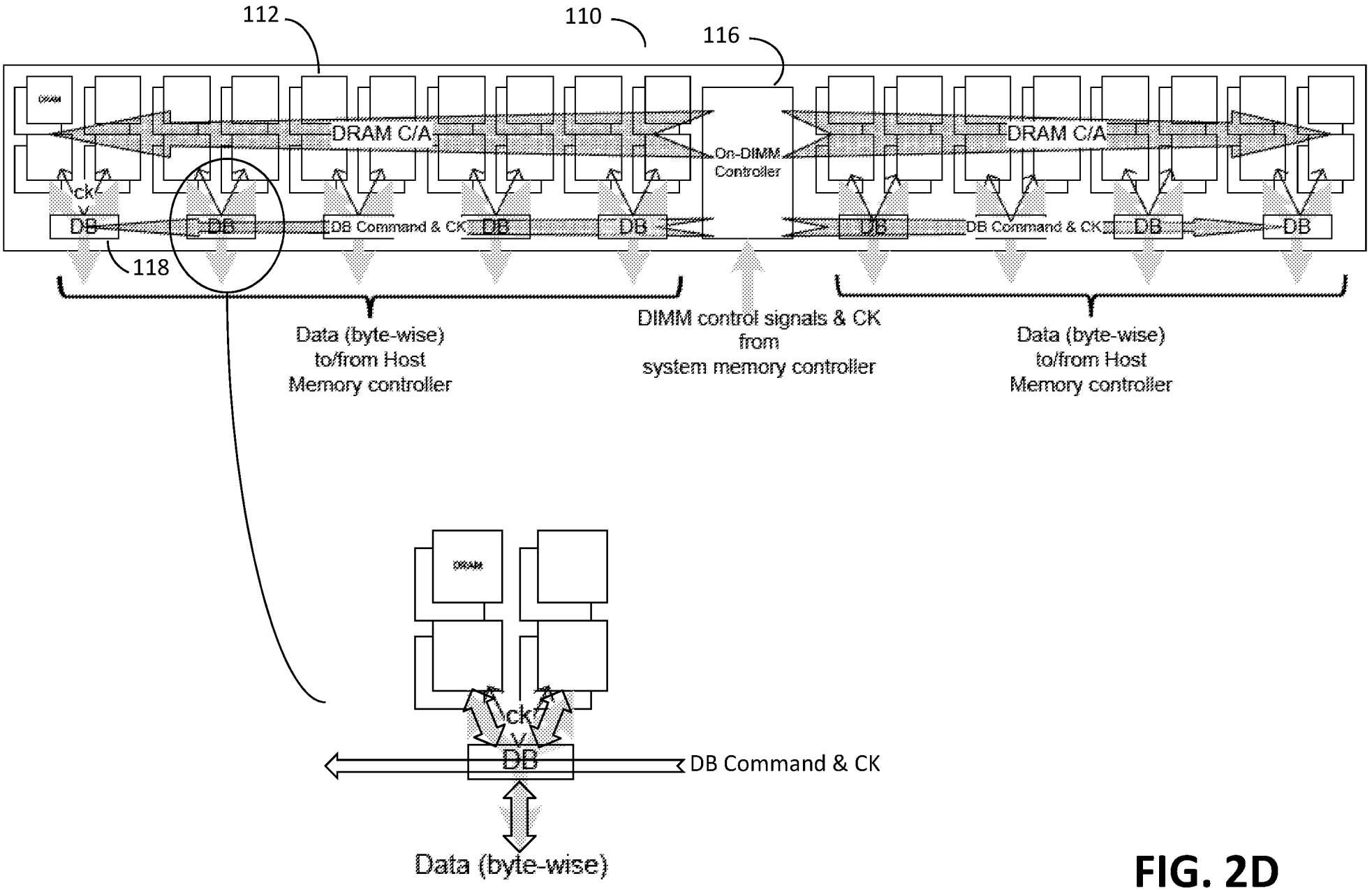

FIG. 2D

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Ex. 1002, p. 7

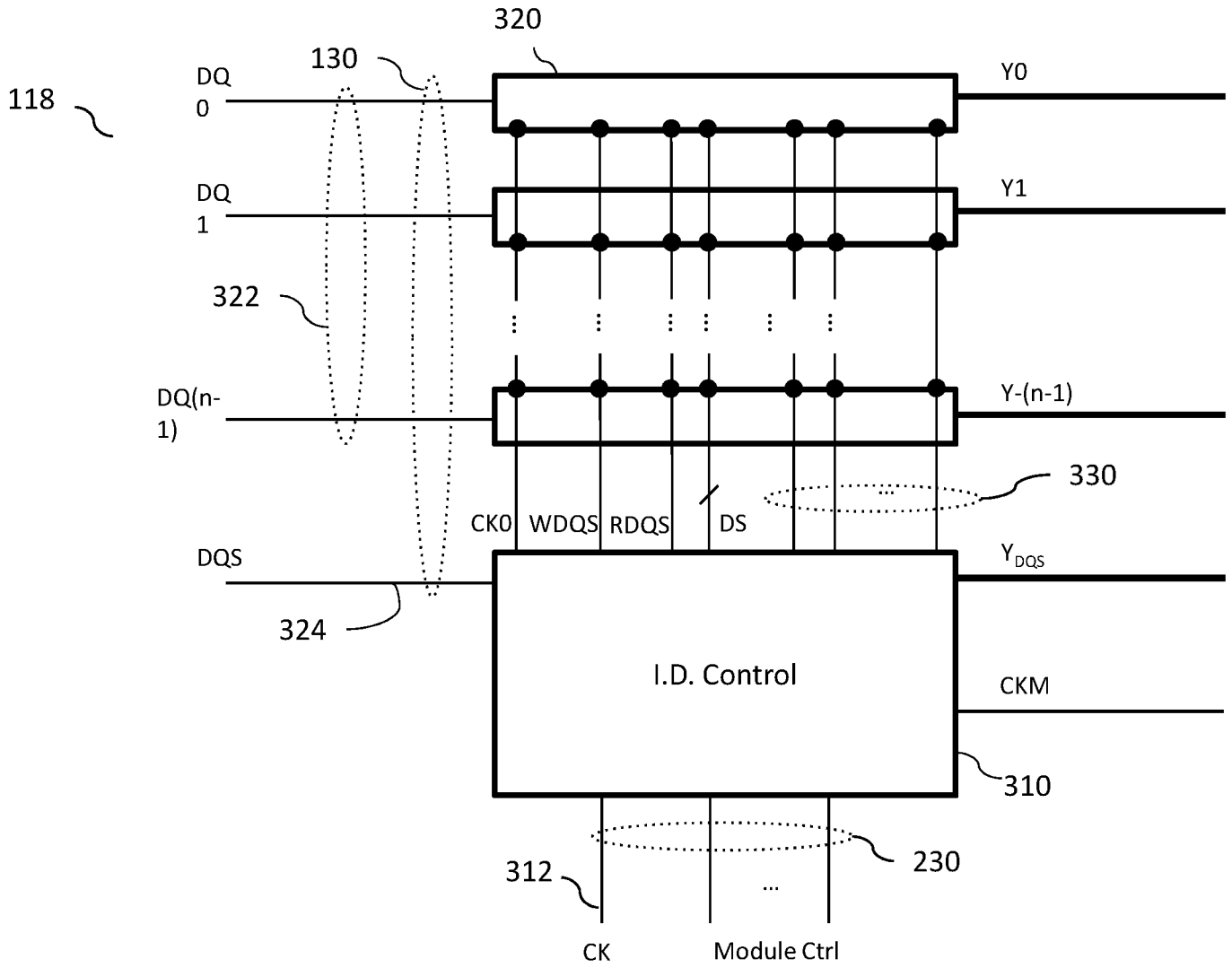
320
130
118
DQ 0
DQ 1
DQ(n-1)
322
DQS
324
Y0
Y1
Y-(n-1)
330
CK0
WDQS
RDQS
DS
Y_{DQS}
I.D. Control
CKM
310
312
230
CK
Module Ctrl

FIG. 3

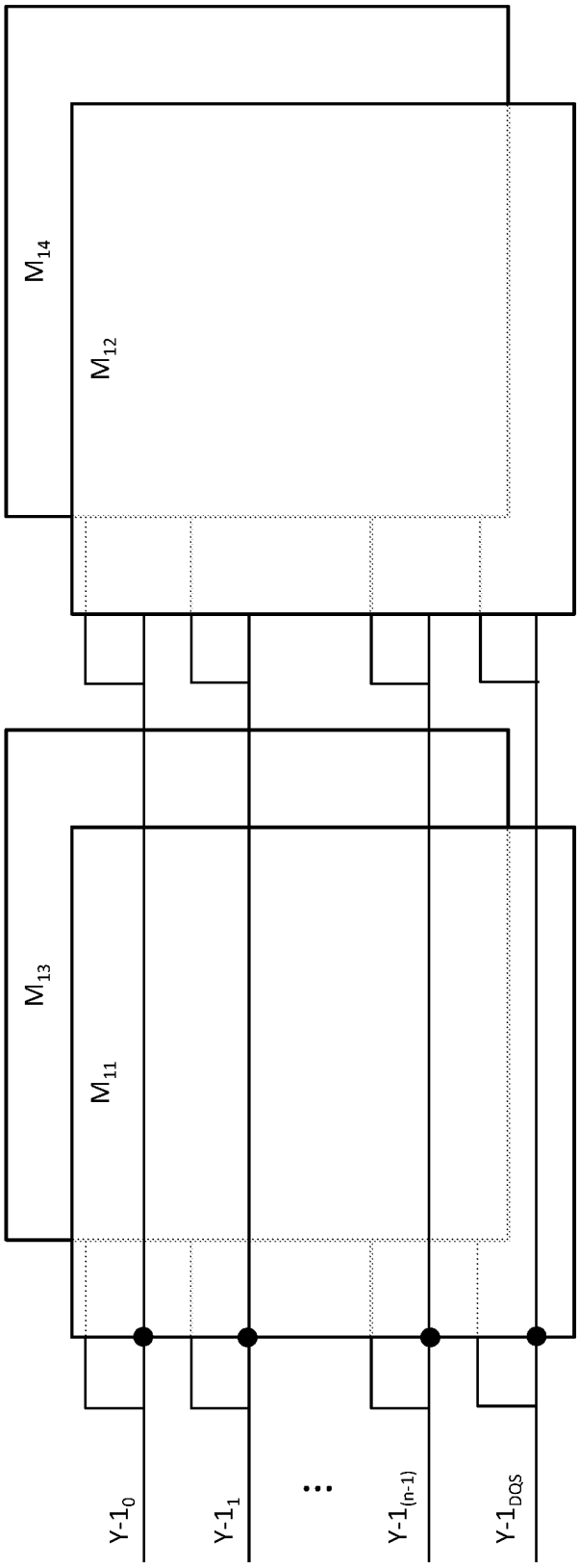

FIG. 4A

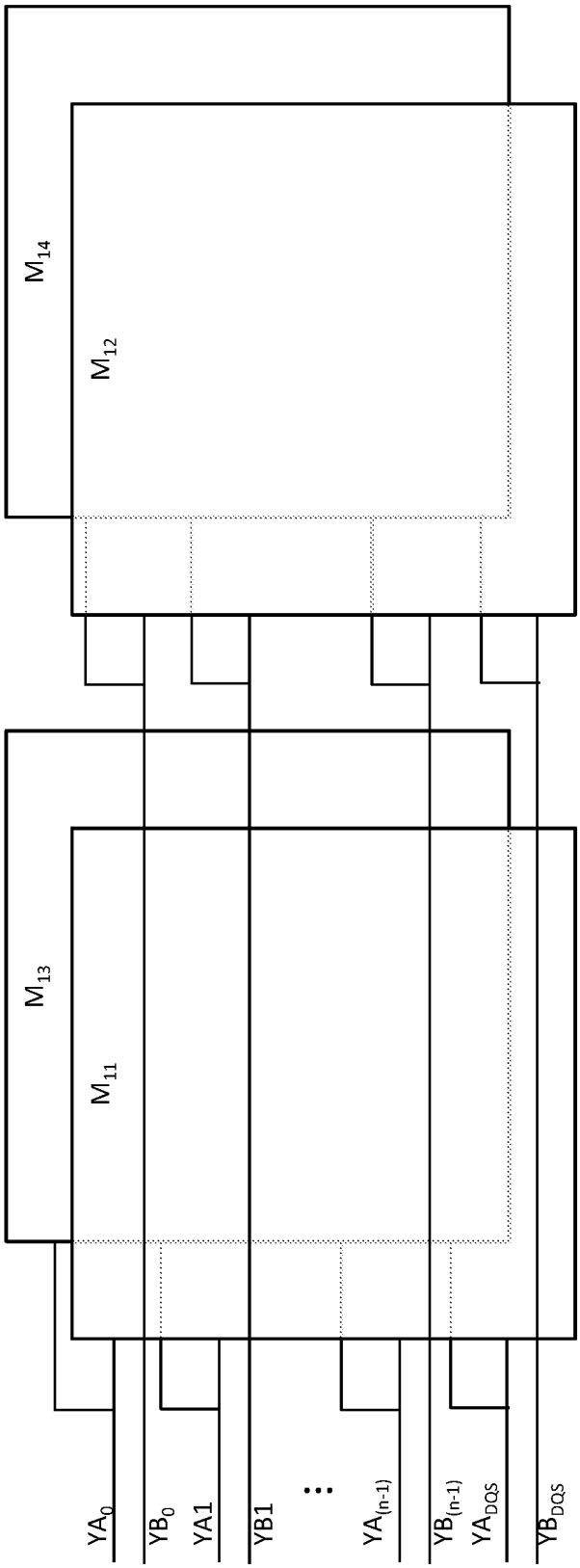

FIG. 4B

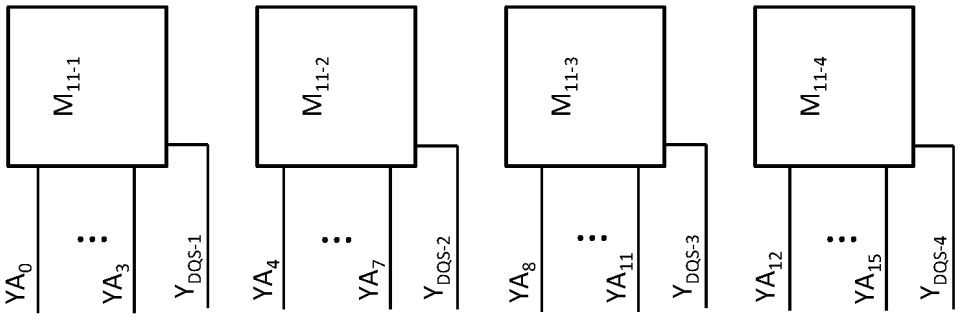
M11-1
M11-2
M11-3
M11-4
YA0
YA3
YA4
YA7
YA8
YA11
YA12
YA15
YDQS-1
YDQS-2
YDQS-3
YDQS-4

FIG. 5B

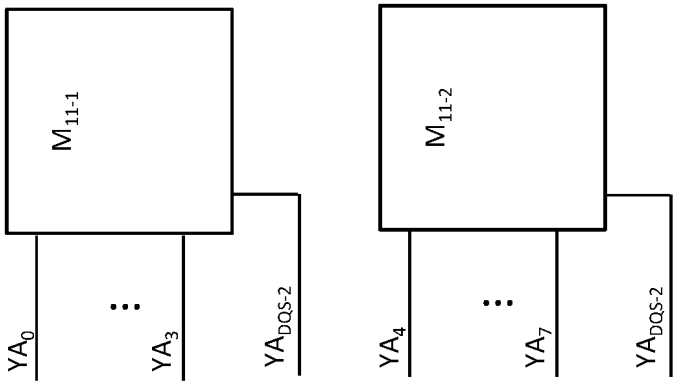
M11-1
M11-2
YA0
YA3
YA4
YA7
YADQS-2
YADQS-2

FIG. 5A

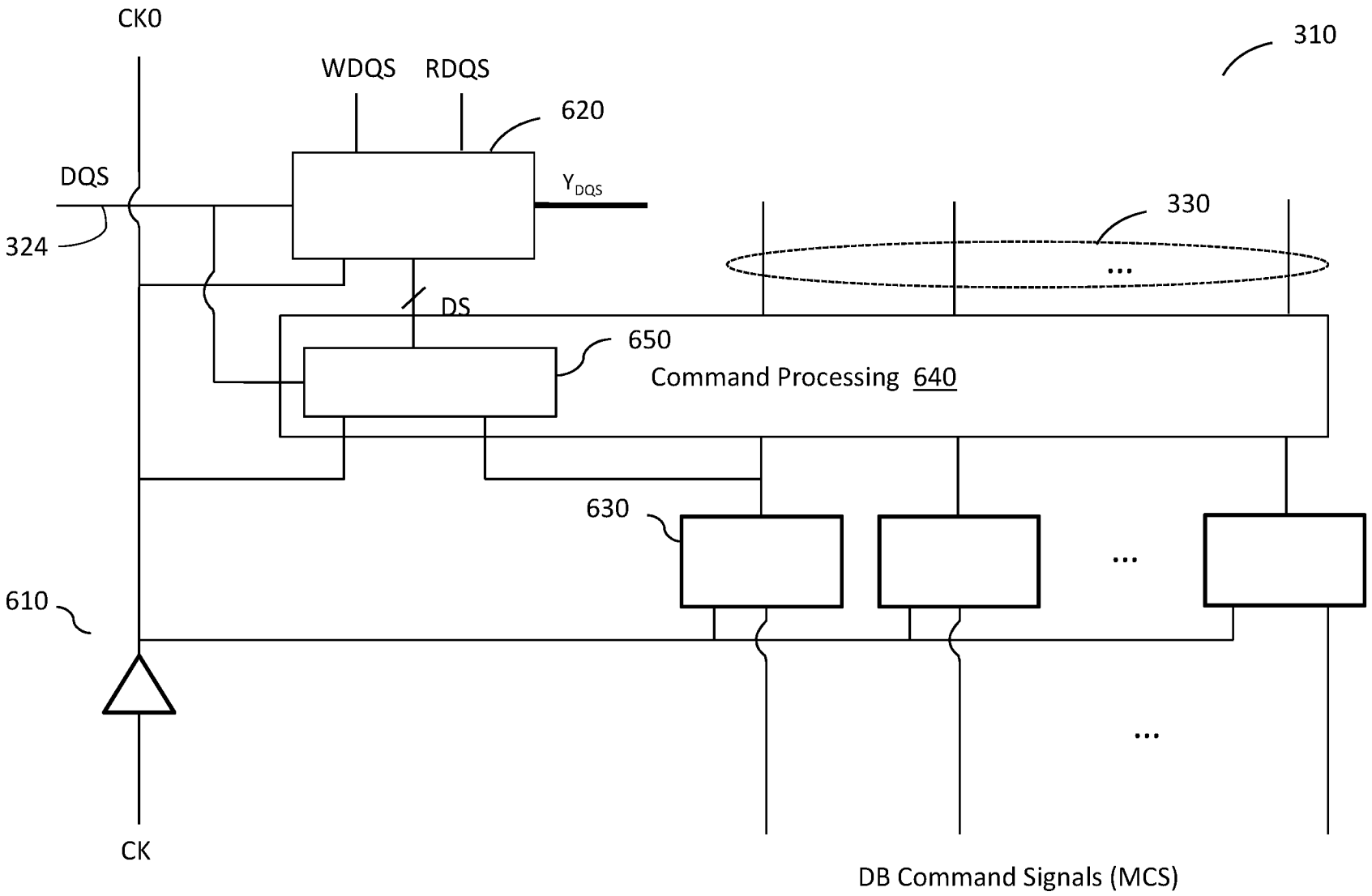
CK0
WDQS
RDQS
620
310
DQS
Y_{DQS}
330
324
...
DS
650
Command Processing 640
630
610
...
...
CK
DB Command Signals (MCS)

FIG. 6

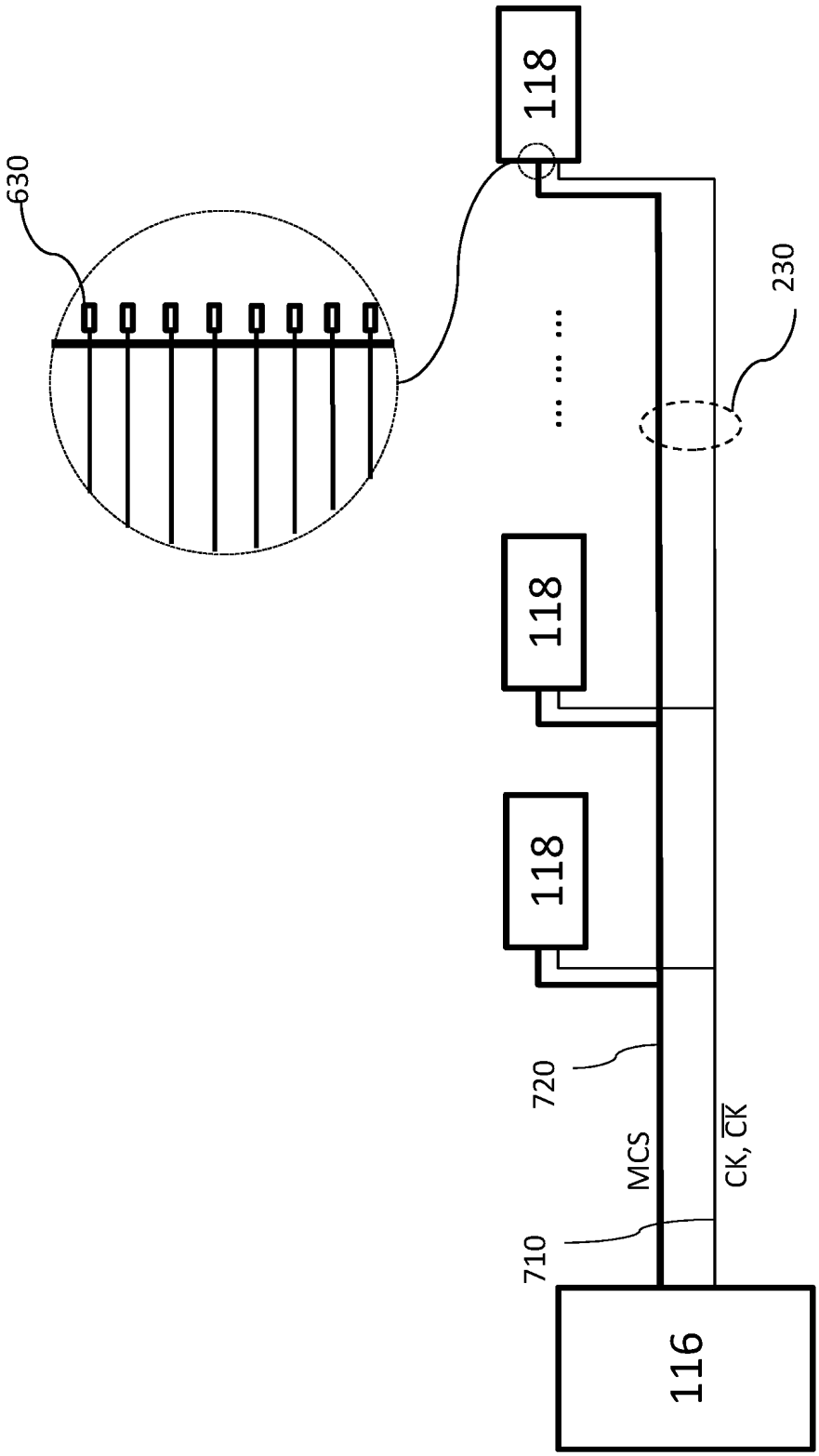

FIG. 7

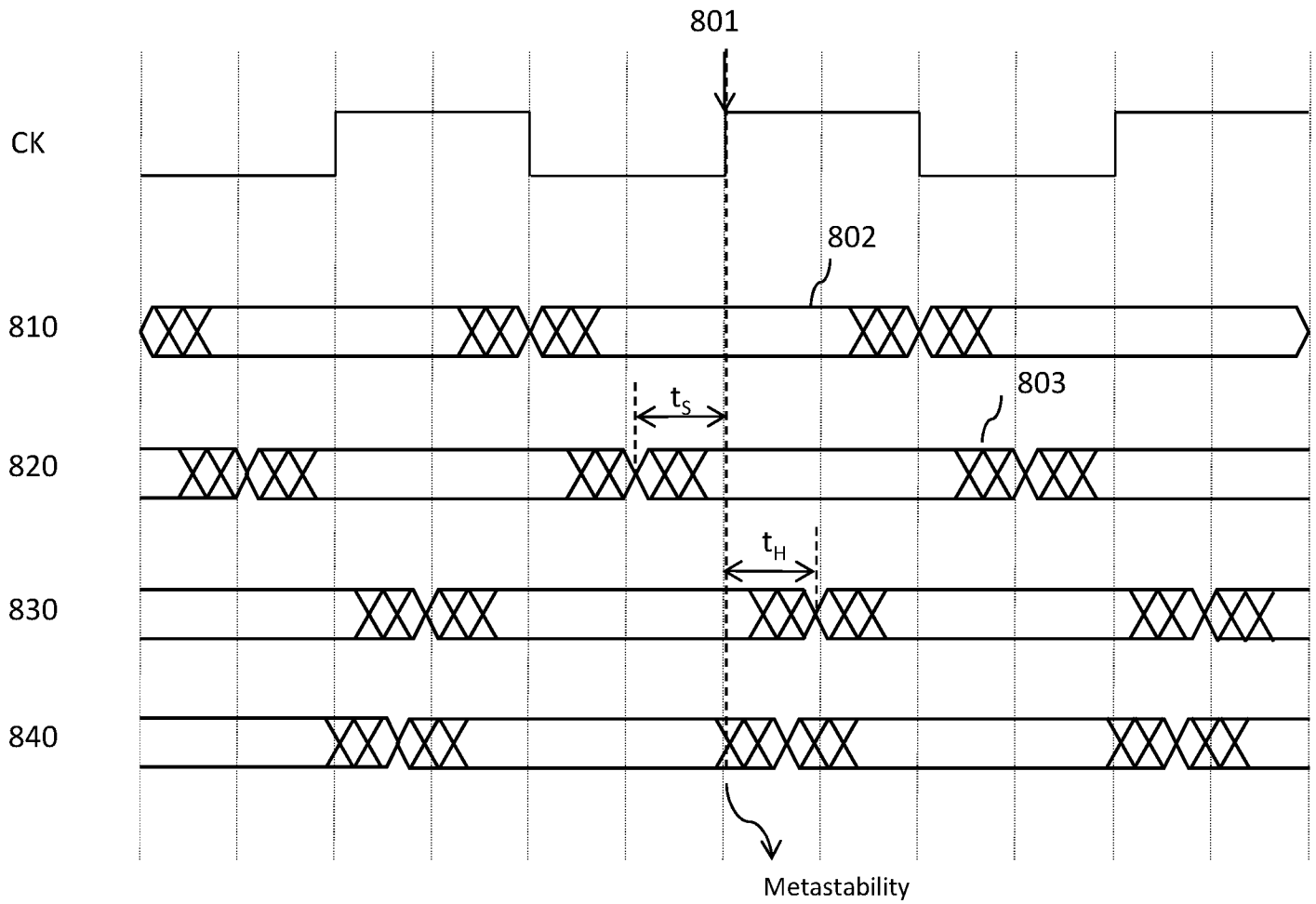

FIG. 8

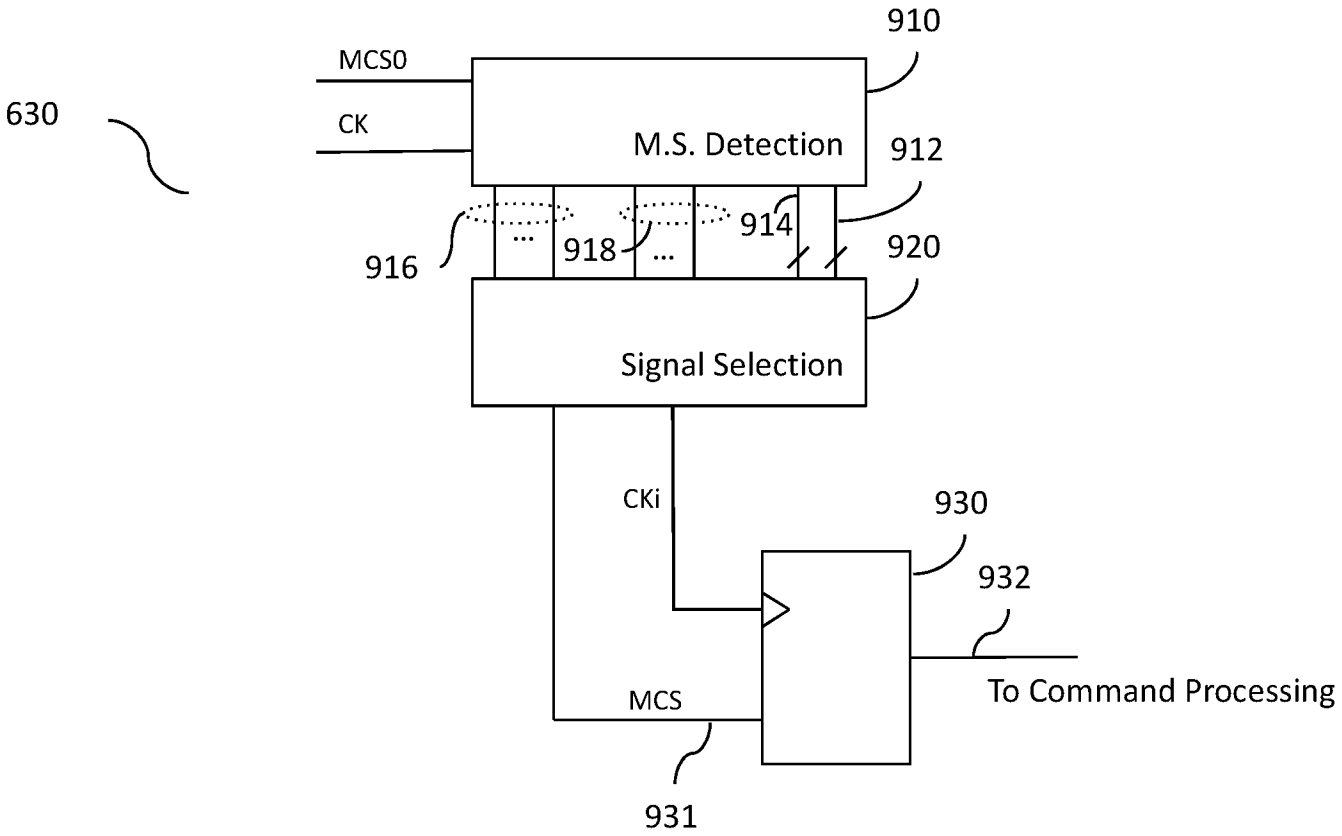
630
MCS0
CK
910
M.S. Detection
912
914
916
918
920
Signal Selection
CKi
930
932
To Command Processing
MCS
931

FIG. 9

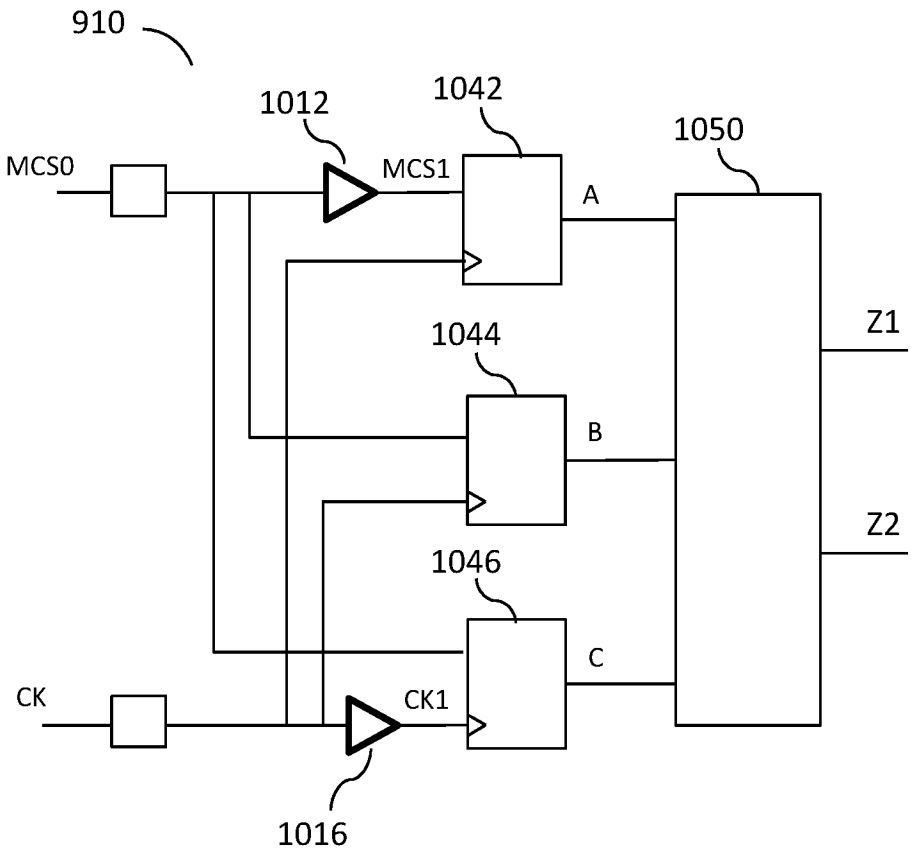

FIG. 10A

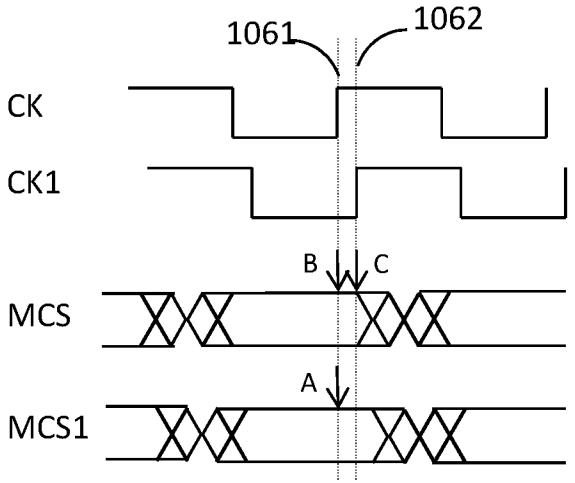

FIG. 10B

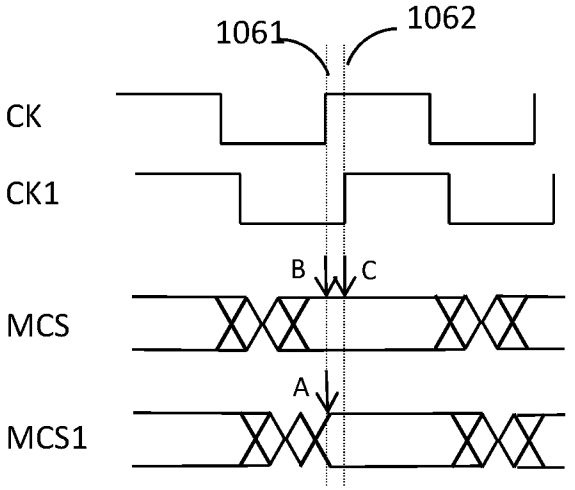

FIG. 10C

Samsung Electronics Co., Ltd.
Ex. 1002, p. 16

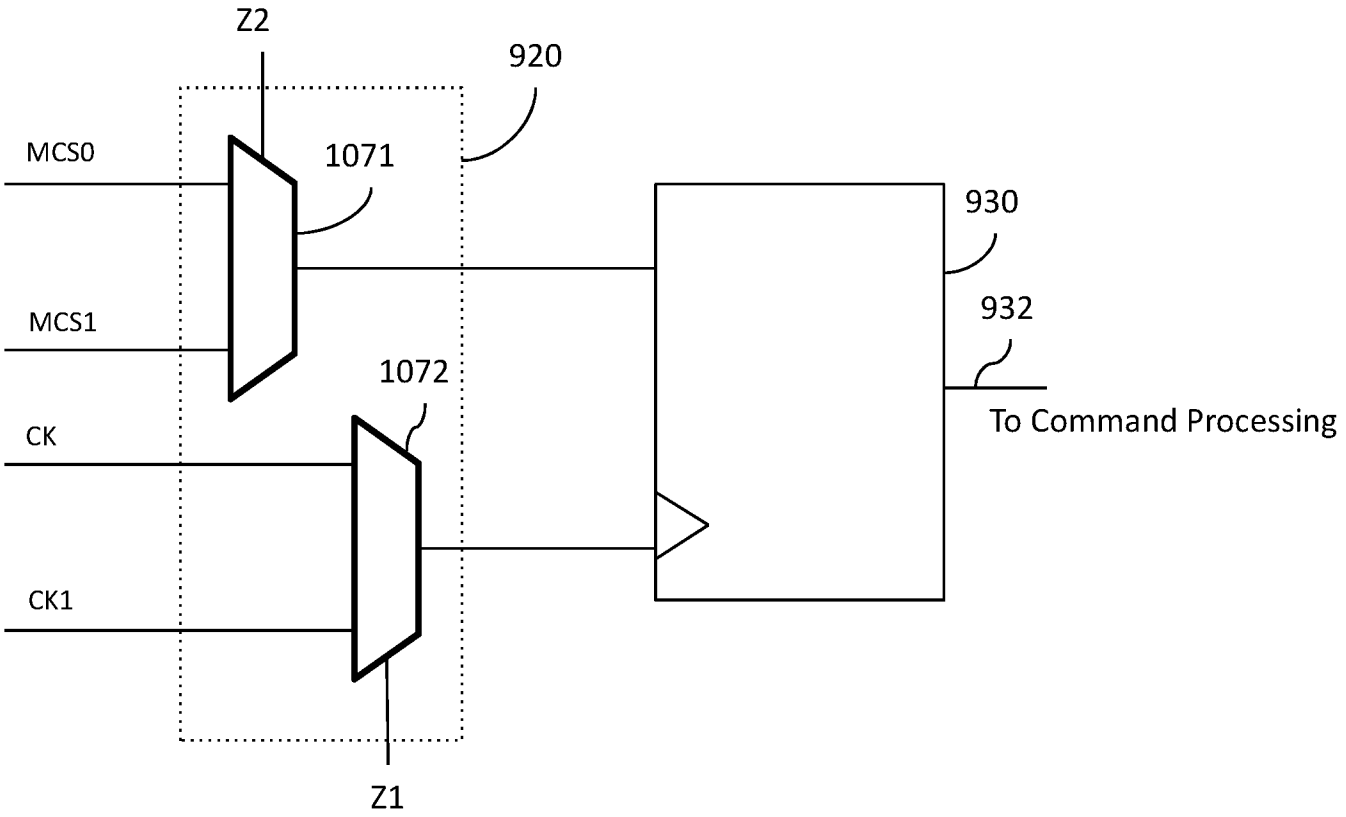
Z2
920
MCS0
1071
930
MCS1
932
1072
CK
To Command Processing
CK1
Z1

FIG. 10D

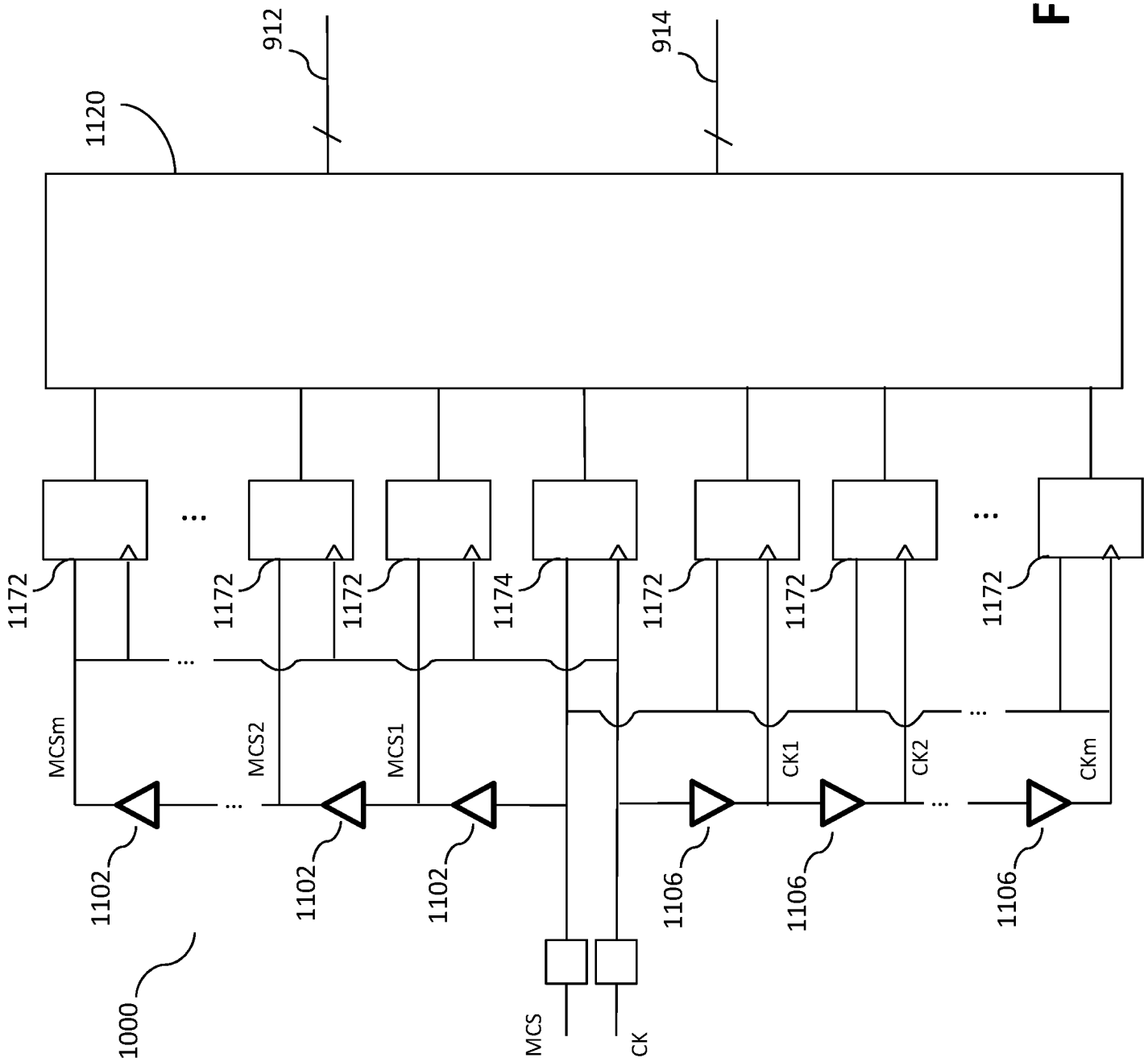
1120
912
914
1172
1174
MCSm
MCS2
MCS1
CK1
CK2
CKm
1102
1106
1000
MCS
CK

FIG. 11A

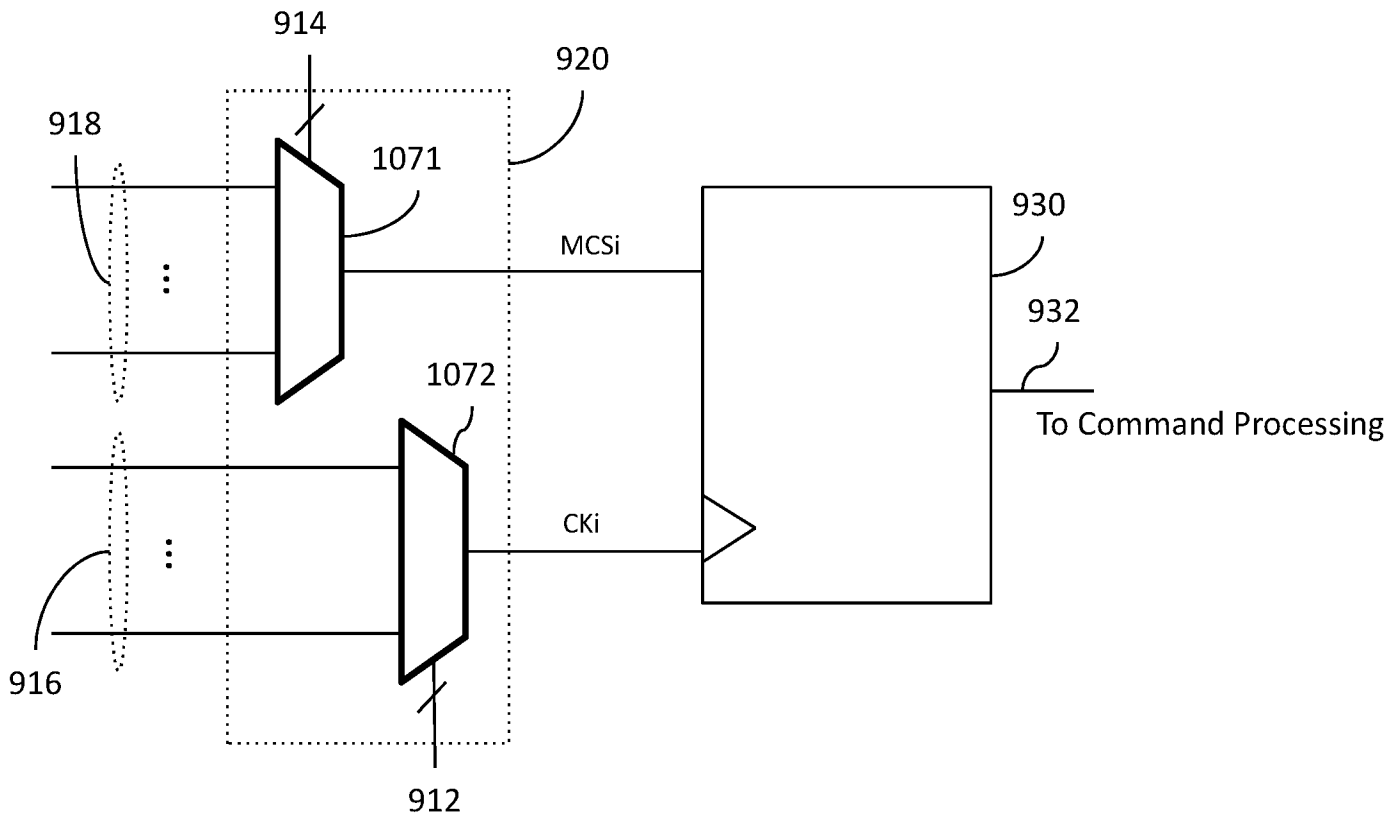
914
920
918
1071
930
MCSi
932
1072
To Command Processing
CKi
916
912

FIG. 11B

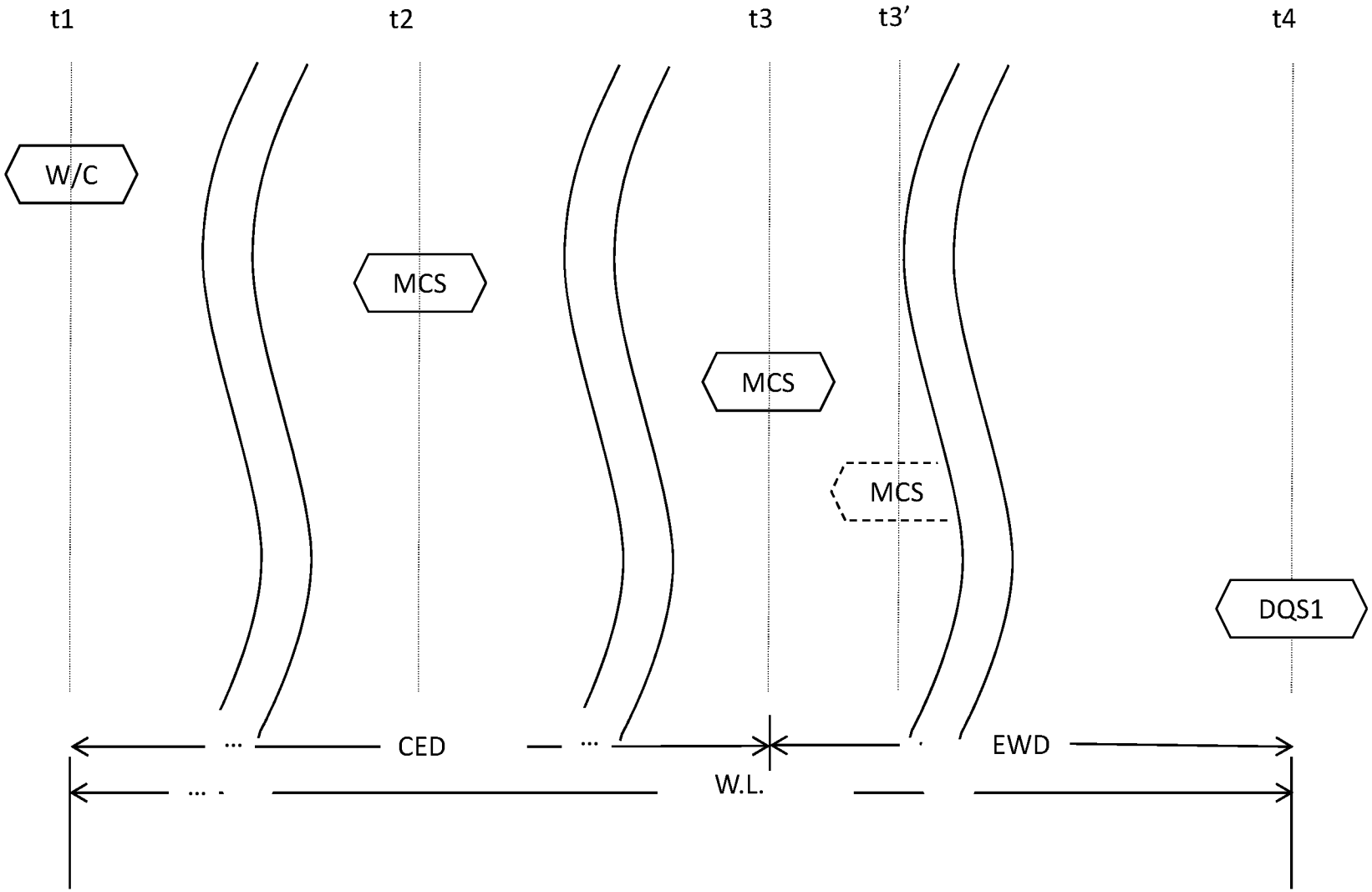

FIG. 12A

Samsung Electronics Co., Ltd.
Ex. 1002, p. 20

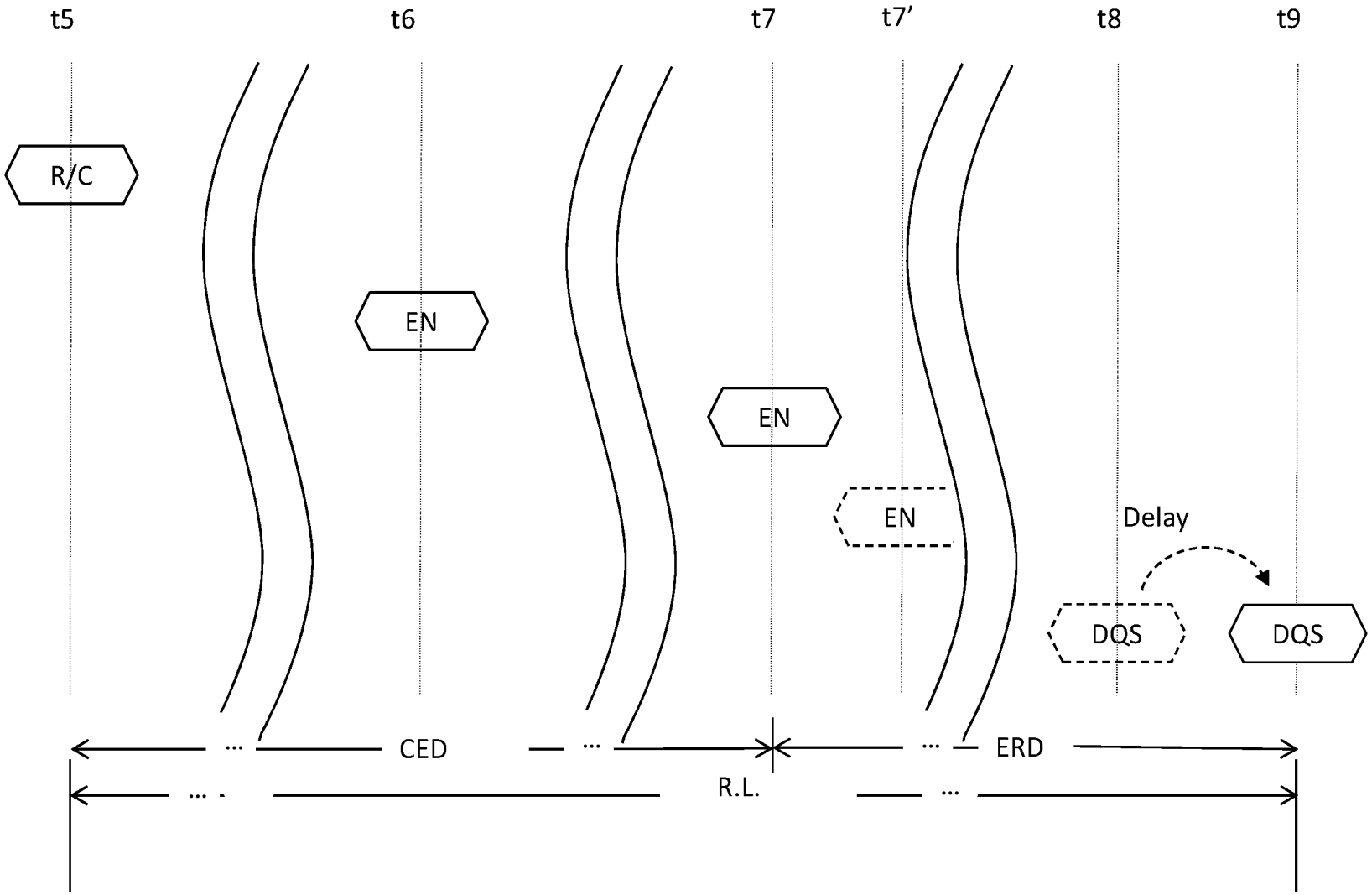

FIG. 12B

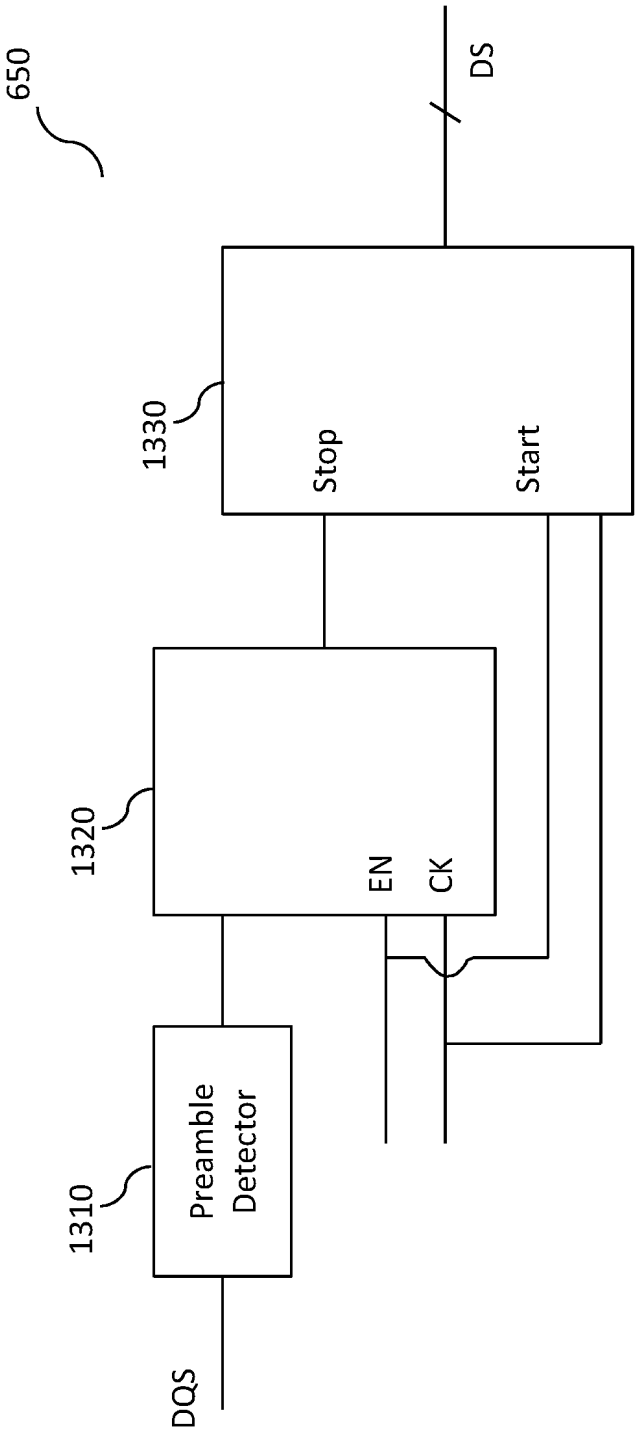

FIG. 13

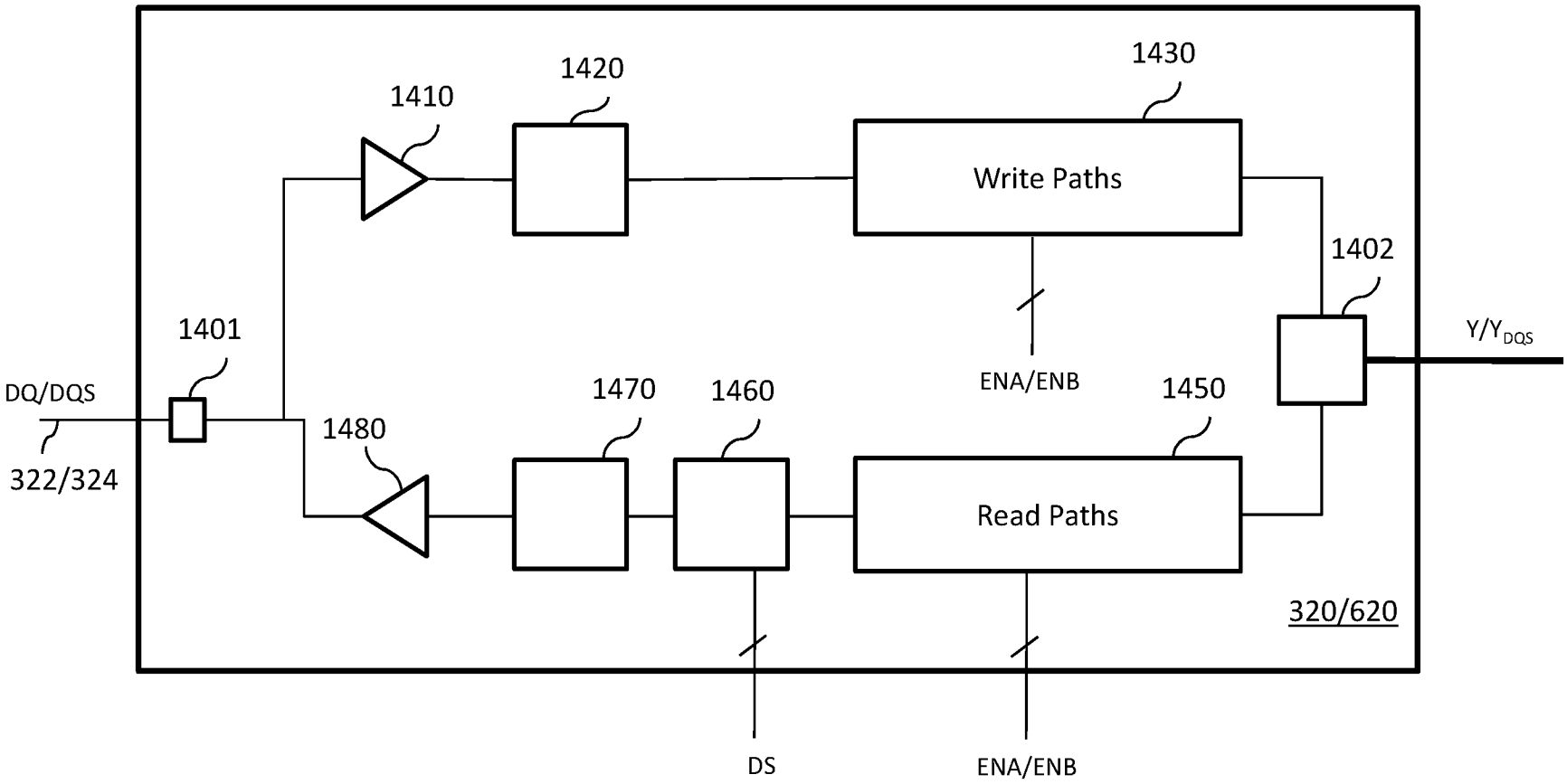

FIG. 14

Samsung Electronics Co., Ltd.
Ex. 1002, p. 23

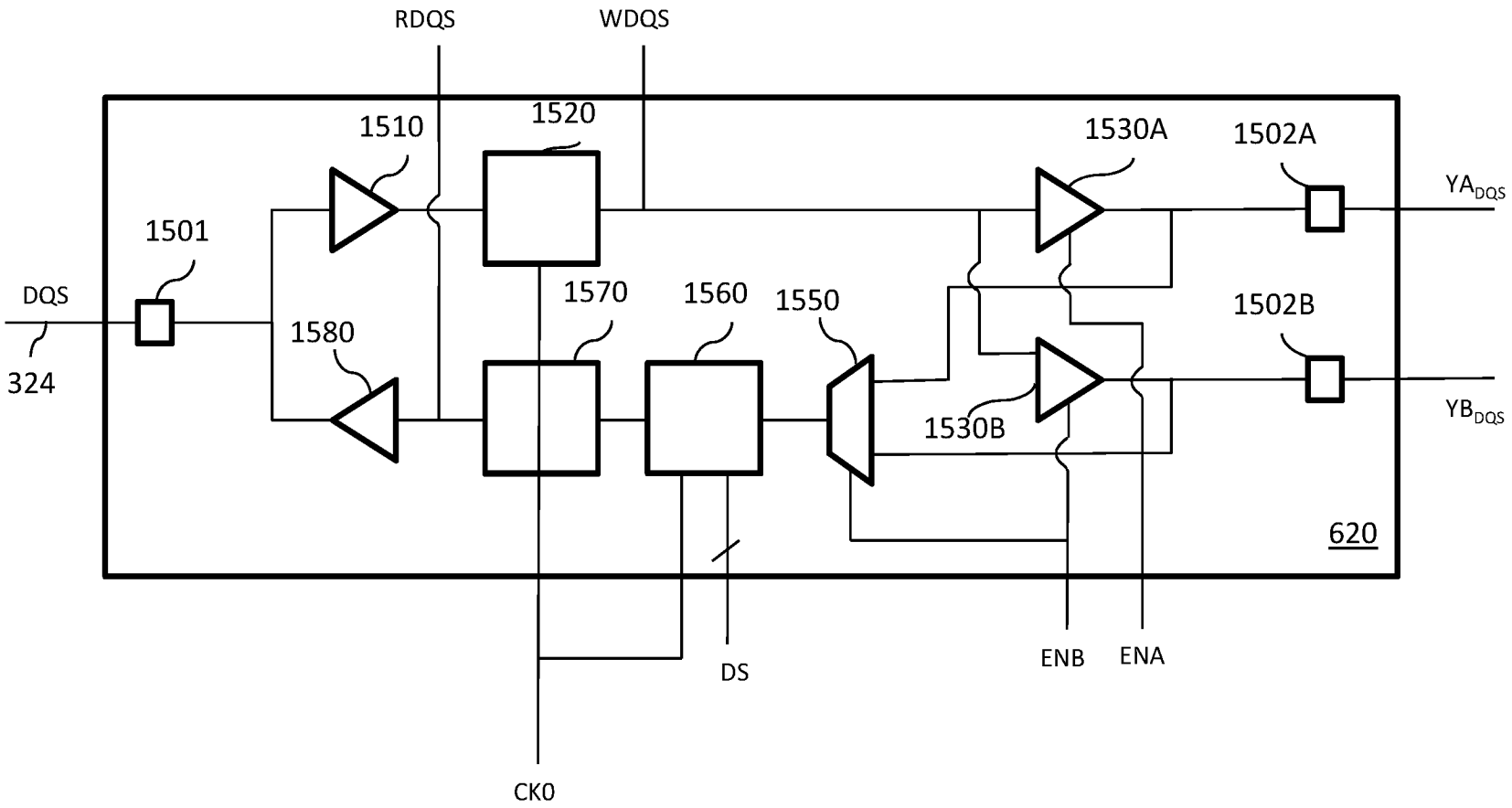

FIG. 15

Samsung Electronics Co., Ltd.
Ex. 1002, p. 24

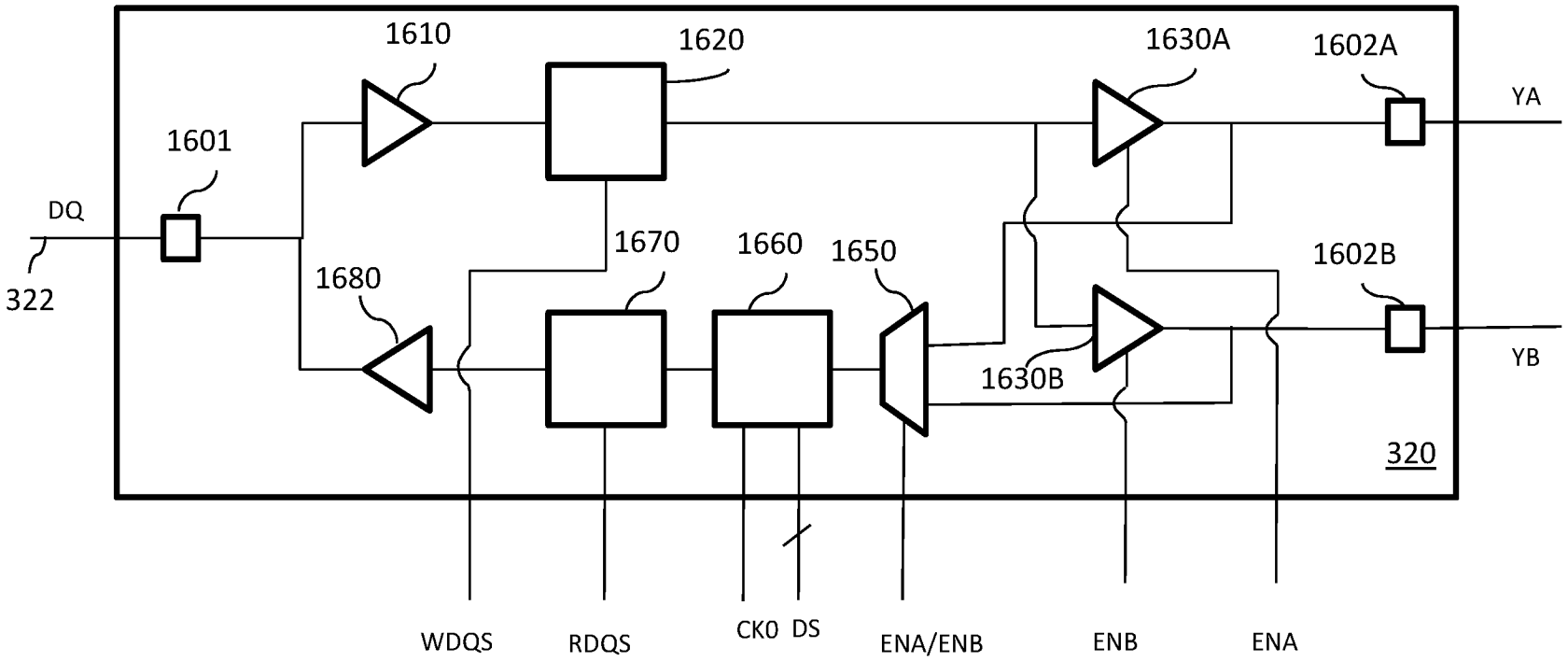
1610
1620
1630A
1602A
YA
1601
DQ
322
1670
1660
1650
1602B
1680
1630B
YB
320
WDQS
RDQS
CK0
DS
ENA/ENB
ENB
ENA

FIG. 16

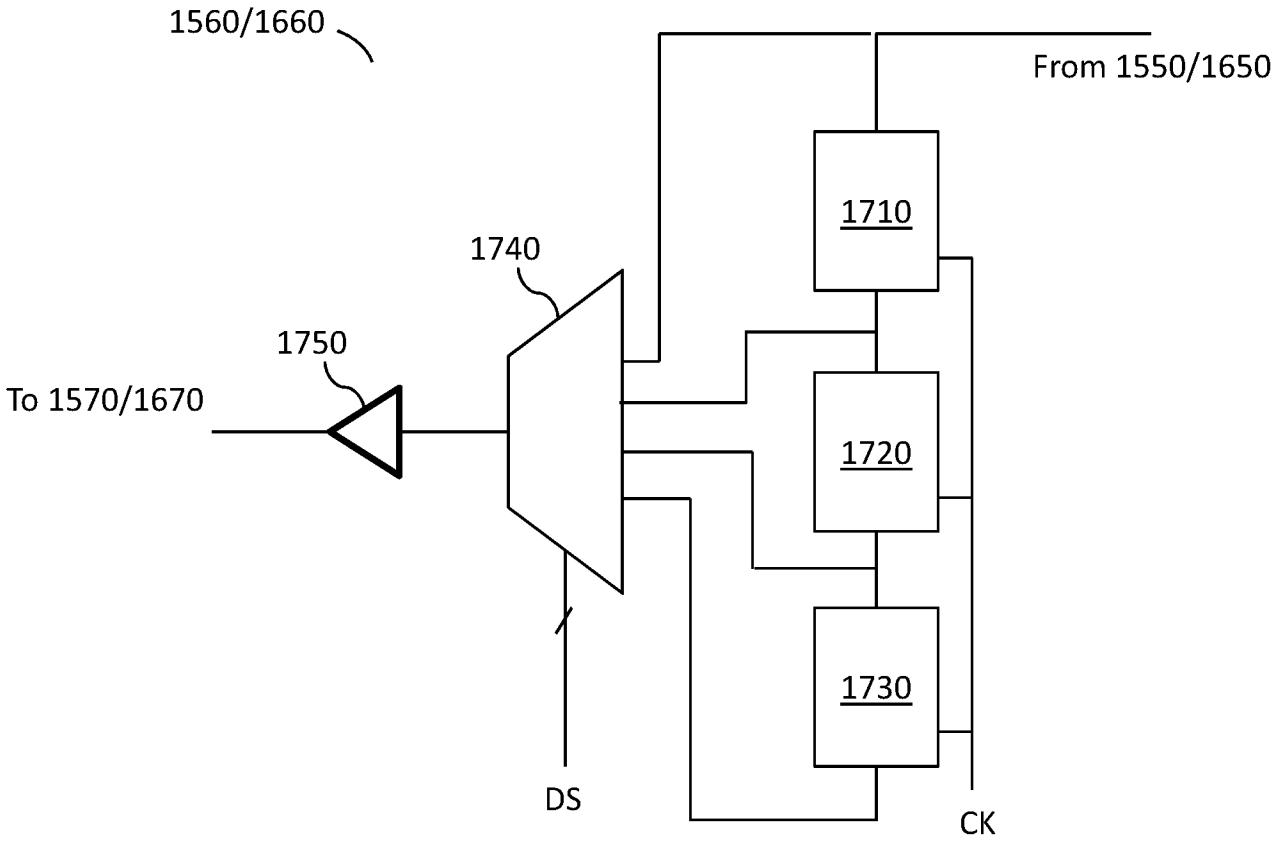
1560/1660
From 1550/1650
1710
1740
1750
To 1570/1670
1720
1730
DS
CK

FIG. 17

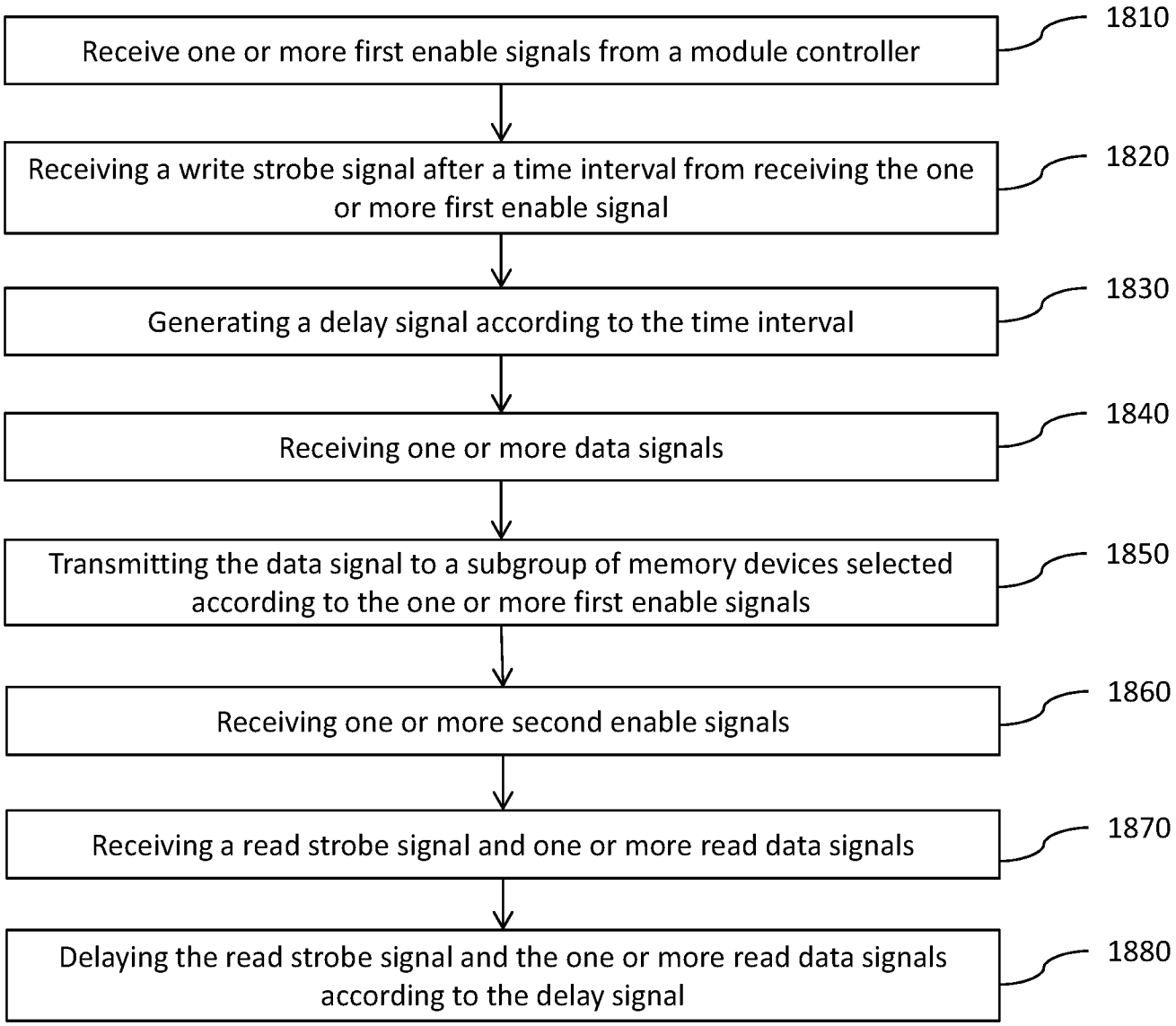

FIG. 18

Samsung Electronics Co., Ltd.
Ex. 1002, p. 27

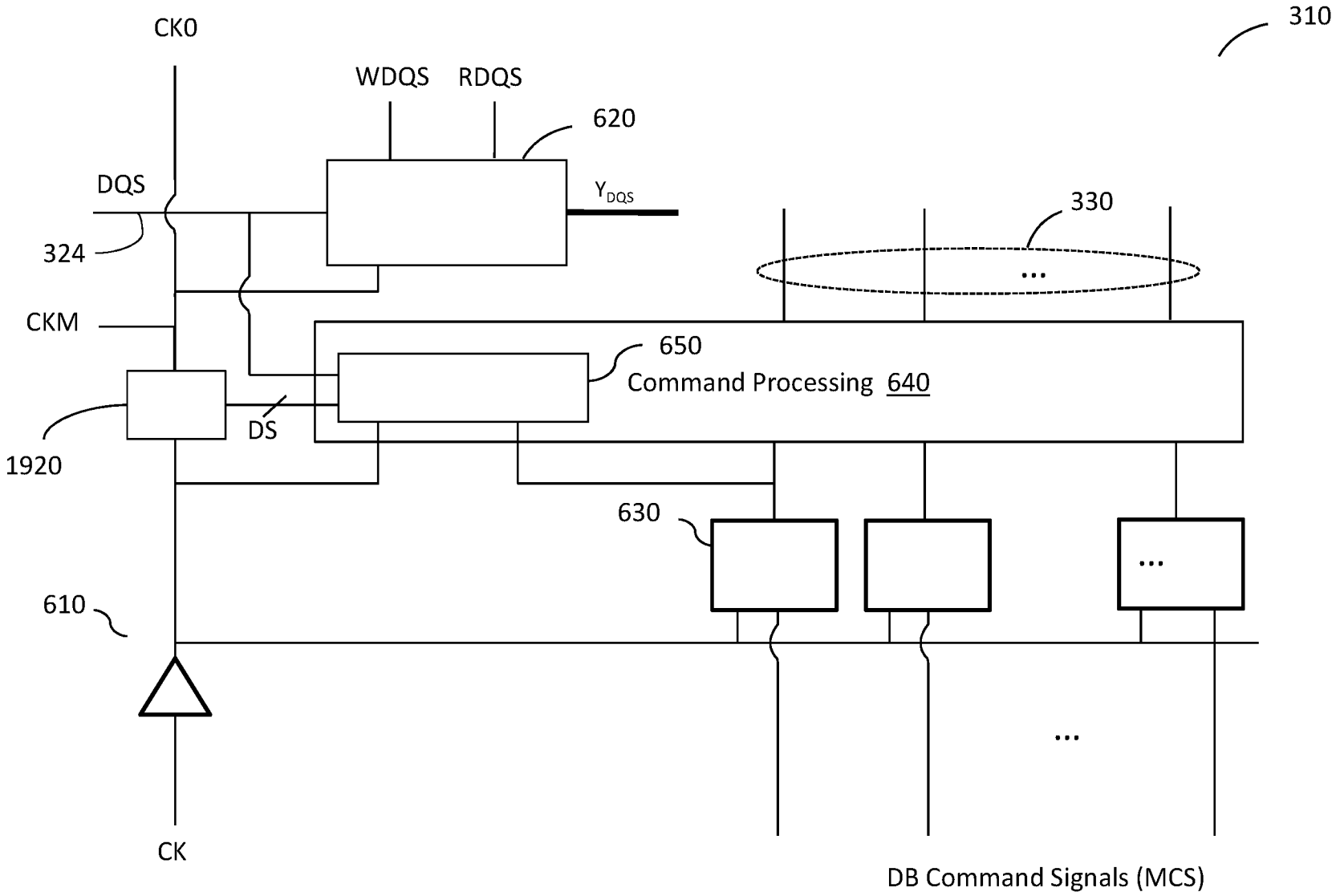
CK0
310
WDQS
RDQS
620
DQS
Y_{DQS}
330
324
...
CKM
650
Command Processing 640
DS
1920
630
610
...
...
CK
DB Command Signals (MCS)

FIG. 19

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/Brian Gonzalez
Attorney Docket Number:	N3044.10009US05

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	31020295
Application Number:	15820076
International Application Number:	
Confirmation Number:	8866
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10009US05
Receipt Date:	21-NOV-2017
Filing Date:	
Time Stamp:	17:46:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1600
RAM confirmation Number	112217INTEFSW17472000
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	138179 1a045b1a3eaa2401931dc30c50de464a8348aa07	no	8
Warnings:					
Information:					
2		2017-11-21_Continuation-Application_N3044-10009US05.pdf	1437523 dd3bd9f2272e69c8958adde0292440ea8d1ecd1f	yes	32
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	30	
	Claims		31	31	
	Abstract		32	32	
Warnings:					
Information:					
3	Oath or Declaration filed	2017-11-21_Parent-Declaration-Assignment_N3044-10009US05.pdf	101281 e6ec692b4cd11992b13cd164ebbdcc6c187c1faa	no	2
Warnings:					
Information:					
4	Power of Attorney	2017-11-21_POA_N3044-10009US05.pdf	165143 747045a492cb8ee2878efb0004ec40ea3a2cbfb5	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

5	Drawings-only black and white line drawings	2017-11-21_Figures_N3044-10009US05.pdf	1096465 9376cca4b609b1482498a2ffbab623600ecc807a	no	26

Warnings:

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Information:

6	Fee Worksheet (SB06)	fee-info.pdf	35340 b7bd2049d40a51a6ee8193dbaffdb1476389bc0c	no	2

Warnings:

Information:

Total Files Size (in bytes):	2973931

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10009US05
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10009US05
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

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For further information see 37 CFR 1.33(a).

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Customer Number	79141		
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Application Information:

Title of the Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS		
Attorney Docket Number	N3044.10009US05	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	26	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	N3044.10009US05
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Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

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Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
	Continuation of	15426064	2017-02-07	9824035	2017-11-21

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15426064	Continuation of	14846993	2015-09-07	9563587	2017-02-07

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14846993	Continuation of	13952599	2013-07-27	9128632	2015-09-08

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13952599	Claims benefit of provisional	61676883	2012-07-27

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Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

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1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

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	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

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Phone Number		Fax Number	
Email Address			

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	Application Number	
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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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	Application Number	
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Signature:

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/JAMIE J. ZHENG/			Date (YYYY-MM-DD)	
First Name	Jamie	Last Name	Zheng	Registration Number	51167

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MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DATA BUFFERS

CLAIM OF PRIORITY

[0001] The present application is a continuation of U.S. Pat. App. No. 15/426,064, to be issued as U.S. Pat. No. 9,824,035, which is a continuation of U.S. Pat. App. No. 14/846,993, now U.S. Pat. No. 9,563,587, which is a continuation of U.S. Pat. App. No. 13/952,599, filed July 27, 2013, issued as U.S. Pat. No. 9,128,632, which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on July 27, 2012. Each of the above applications is incorporated herein by reference in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] The present application is related to commonly-owned U.S. Pat. App. No. 14/715,486, filed on May 18, 2015; U.S. Pat. App. No. 13/970,606, filed on August 20, 2013; U.S. Pat. App. No. 12/504,131, filed on July 16, 2009, now U.S. Pat. No. 8,417,870; U.S. Pat. App. No. 12/761,179, filed on April 15, 2010, now U.S. Pat. No. 8,516,185; U.S. Pat. App. No. 13/287,042, filed on November 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. Pat. App. No. 13/287,081, filed on November 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

FIELD

[0003] The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

BACKGROUND

[0004] With recent advancement of information technology and widespread use of the

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Internet to store and process information, more and more demands are placed on the acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

[0005] The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

[0006] The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

[0007] In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

[0008] For memory devices in such as a memory module to be properly accessed,

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distribution of control signals and a control clock signal in the memory module is subject to strict constraints. In some conventional memory modules, control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

[0009] In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram illustrating a memory system including at least one memory module according to one embodiment.

[0011] FIGS. 2A-2D are each a diagrams illustrating interactions among components in a a memory module according to certain embodiments.

[0012] FIG. 3 is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

[0013] FIGS. 4A-4B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

[0014] FIGS. 5A-5B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

[0015] FIG. 6 is a diagram illustrating a control circuit in a data buffer according to

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certain embodiments.

[0016] FIG. 7 is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

[0017] FIG. 8 is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

[0018] FIG. 9 is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

[0019] FIGS. 10A-10C are diagrams illustrating a metastability detection circuit according to certain embodiments.

[0020] FIGS. 10D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

[0021] FIGS. 11A-11B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

[0022] FIGS. 12A-12B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

[0023] FIG. 13 is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

[0024] FIG. 14 is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

[0025] FIG. 15 a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

[0026] FIG. 16 a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

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[0027] FIG. 17 is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.

[0028] FIG. 18 is a flowchart illustrating a method for data edge alignment according to embodiments.

[0029] FIG. 19 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

DESCRIPTION OF EMBODIMENTS

[0030] A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

[0031] The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective

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groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

[0032] In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

[0033] Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

[0034] FIG. 1 shows a system 100 including a memory controller (MCH) 101 and one or more memory modules 110 coupled to the MCH by a memory bus 105, according to one embodiment. As shown, the memory bus includes C/A signal lines 120 and groups of system data/strobe signal lines 130. Also as shown, each memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114. Each memory module 110 further includes a module control circuit (module controller or module control

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device) 116 coupled to the MCH 101 via the C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to the MCH 101 via respective groups of system data/strobe signal lines 130. In one embodiment, the memory devices 112, the module control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119.

[0035] In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module 110 may vary. For example, as shown, each memory module 110 may include four ranks of memory devices 112. In another embodiment, the memory module 110 may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices 112.

[0036] In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices 112. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

[0037] Furthermore, the memory devices 112 may include any type of memory devices. For example, in one embodiment, the memory devices 112 may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module 110 may include a dual in-line memory module (DIMM).

[0038] Referring to FIG. 2A, which illustrates one memory module 110 according to an embodiment, the module control device 116 receives system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal

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lines 120 and generates module command signals and module control signals based on memory commands from the system. The module control device 116 also received a system clock MCK and generates a module clock signal CK in response to the system clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{\text{MCK}}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{\text{CK}}$.

[0039] Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

[0040] Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

[0041] Examples of module control signals include, but are not limited to a mode signal

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(MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices 118 via respective module control signal lines 230. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices 118 via the module control signal lines and decoded/processed at the isolation devices.

[0042] Module control device 116 transmits the module command signals to the memory devices 112 via module C/A signal lines 220. The memory devices 112 operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices 118 via module control signal lines 230. As shown in FIG. 2, at least some of the memory devices in a same rank share a same set of module C/A signal lines 220, and at least some of the isolation devices 118 share a same set of module control signal lines 230.

[0043] As shown n FIGS. 2A and 2B, each rank 114 includes N memory devices, where N is an integer larger than one. For example, a first rank includes memory devices M_{11}, …, M_{i1}, $M_{i+1,1}$, …, M_N, a second rank includes memory devices M_{12}, …, M_{i2}, $M_{i+1,2}$, …, $M_{N,2}$, and so on. In one embodiment, the memory devices 112 are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines 130 and including at least one memory device from each rank. For example, memory devices M_{11}, M_{12}, M_{13}, and M_{14} form a first group of memory devices, memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} form an i^{th} group of memory devices, and so on.

[0044] As shown, the isolation devices 118 are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines 130 and the respective groups of memory devices. For example, isolation device ID-1

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among the isolation devices 118 is associated with the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14} and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices, isolation devices ID-*i* among the isolation devices 118 is associated with the i^{th} group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} and is coupled between the group of system data/strobe signal lines 130-i and the *i^{th} group* of memory devices, and so on.

[0045] In one embodiment, each group or sets of memory devices are coupled to the associated isolation device 118 via a set of module data/strobe lines 210. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device 118 via a same set of module data/strobe lines 210 (as shown in FIG. 2A) or via respective subsets of module data/strobe lines 210 (as shown in FIG. 2B). For example, as shown in FIG. 2B, in the first group of memory devices, memory devices M_{11} and/or M_{13} form a first subgroup, and memory devices M_{12} and/or M_{14} form a second subgroup; in the i^{th} group of memory devices, memory devices M_{i1} and/or M_{i3} form a first subgroup, and memory devices M_{i2} and/or M_{i4} form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device 118 via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices M_{11} and/or M_{13} form the first subgroup are/is coupled to the isolation device ID-1 via the corresponding first subset of module data/strobe lines YA-1, and memory devices M_{12} and/or M_{14} form the second subgroup are/is coupled to the isolation device ID-1 via the corresponding second subset of module data/strobe lines YA-2.

[0046] In one embodiment, the isolation devices 118 are in the data paths between the MCH 101 and the memory module 110 and include data buffers between the MCH 101 and the respective groups of memory devices. In one embodiment, each isolation device 118 is configured to select a subgroup in the respective group of memory devices to communicate

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data with the MCH 101 in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH 101. Further, each isolation devices 118 is configured to isolate unselected subgroup(s) of memory devices from the MCH 101 during write operations, so that the MCH sees a load on each data line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

[0047] In one embodiment, the isolation devices 118 are distributed across the memory module 110 or the module board 119 in positions corresponding to the respective groups of memory devices. For example, isolation device ID-1 is disposed in a first position corresponding to the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and isolation device ID-*i* is disposed in an i^{th} position separate from the first position and corresponding to the i^{th} group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4}. In one embodiment, the first position is between the first group of memory devices and an edge 201 of the module board 119 where connections (not shown) to the data/strobe signal lines 130 are placed, and i^{th} position is between the i^{th} group of memory devices and the edge 201 of the module board 119. In one embodiment, the isolation devices 118 are distributed along the edge 201 of the memory module 110. In one embodiment, each isolation device 118 is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines 210, the module C/A signal lines 220, and the module control signal lines 230 include signal traces formed on and/or in the module board 119.

[0048] As an option, memory module 110 may further include a serial-presence detect (SPD) device 240, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module 110. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory module 110, a memory density per rank, a number of memory device on the memory module 110, and a memory density per memory device, etc. A basic input/output system

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(BIOS) of system 100 can be informed of these attributes of the memory module 110 by reading from the SPD 240 and can use such data to configure the MCH 101 properly for maximum reliability and performance.

[0049] In certain embodiments, the SPD 240 and/or the control circuit 116 store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit 116, input and output signals electrical and logical level control information for the control circuit 116, etc. In certain embodiments, the SPD 240 contains a system view of the module 110 which can be different from an actual physical construction of the module 110. For example, the SPD 240 stores at least one memory operation parameter that is different from a correspondng memory operation parameter in a system memory controller setting. The SPD 240 may also store at least on data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

[0050] Thus, in certain embodiment, in the memory module 110, C/A signals representing a memory command are received and buffered by the module control circuit 116, so that the MCH sees only the module control circuit 116 as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130. Thus, MCH 101 does not directly operate or control the memory devices 112. As far as data/strobe signals are concerned, the MCH 101 mainly sees the isolation devices 118, and the system 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101.

[0051] In certain embodiments, the memory module 110 is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM). In certain embodiments, the control circuit 116 includes a DDR register, and logic for memory space translation between a system memory domain and a

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module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.

[0052] As shown in FIG. 2C, in certain embodiments, the control circuit 116 transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices 118, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

[0053] For example, load reduction mechanism in the isolation devices 118 would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller 101. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller 101 over the interface between the memory devices 112 and the associated isolation devices 118. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller 101, which may cause silent system failure.

[0054] Moreover, clock skew amongst the memory devices 112 and the associated isolation devices 118 due to the distributed architecture of the memory module 110 can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

[0055] To address at least some of the above issues, in certain embodiments, as shown in

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FIG. 2D, the control circuit 116 transmits registered C/A signals to the memory devices 112, and transmits the module control signals and the module clock signal to the data buffers 118, in a fly-by arrangement. The memory devices 112 do not receive the module clock signal from the control circuit 116. Instead, each data buffer 118 regenerates the clock that is used by the respective set of memory devices 112. Each Data buffer 118 is thus responsible for providing a correct data timing interface between the respective set of memory devices 112 and the system memory controller 101. Each data buffer 118 is also responsible for providing the correct control signal timing between the control circuit 116 and the respective set of memory devices 112.

[0056] Thus, the memory module 110 in FIG. 2D allows a locally synchronized operation for each respective set of memory devices 112, which can correspond to a nibble or a byte of a DDR data bus between the memory module 110 and the system memory controller 101. Also, signal interface between each data buffer 118 and the respective set of memory devices 112 can be synchronized. In one embodiment, each data buffer 118 has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices 112, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller 101, programmable phase adjustment related to at least one control signal that is coupled to the control circuit 116. The locally synchronized operation also makes it easier for each data buffer 118 to perform self-testing of the associated set of memory devices 112, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Patent 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

[0057] In certain embodiments, operations of the isolation devices 118 are controlled by the module control signals from the module control circuit 116, which generates the module control signals according to the C/A signals received from the MCH. Thus, the module control signals need to be properly received by the isolation devices 118 to insure their proper operation. In one embodiment, the module control signals are transmitted

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together with the module clock signal CK, which is also generated by the module control circuit 116 based on the system clock signal MCK. The isolation circuits 118 buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices 118 are distributed across the memory module, the module control signal lines 230 can stretch across the memory module 110, over a distance of several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits 118 includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

[0058] Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n-1) in the exemplary configuration shown in FIG. 2. In other words, a same set of module control signals may reach different isolation devices 118 at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

[0059] With the isolation devices 118 receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to

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time the transmission of read data signals to the MCH 101 from the isolation devices 118. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100, as explained in more detail below.

[0060] More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0061] In one embodiment, as shown in FIG. 3, each group of signal lines 130 include a set of *n* data (DQ) signal lines 322 each for transmitting one of a set of data signals DQ_0, DQ_1, ..., DQ_{n-1}, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of *n* module data signal lines Y_0, Y_1, ..., Y_{n-1} and at least one module strobe signal line Y_{DQS}. When the subsets of memory devices are coupled to the associated isolation device 118 via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. 2B. Each subset of module data/strobe lines YA include a set of *n* first module data lines YA_0, YA_1, ..., YA_n and at least one first module strobe signal line YA_{DQS}; and each subset of module data/strobe lines YB include a set of *n* second module data lines YB_0, YB_1, ..., YB_n and at least one second module strobe signal line YB_{DQS}.

[0062] Each isolation device 118 includes a set of DQ routing circuits 320 coupled on one side to respective ones of the set of *n* DQ signal lines 322, and on another side to respective

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ones of the respective set of *n* module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines YA_0, YA_1, ..., YA_n and the second module data lines YB_0, YB_1, ..., YB_n. Each isolation device 118 further includes an ID control circuit 310 coupled on one side to the at least one DQS signal line 324, on another side to the one or more module strobe signal lines Y_{DQS}, or the first module strobe signal line YA_{DQS} and second module strobe signal line YB_{DQS}. The ID control circuit 310 also receives the module clock signal CK and the module control signals via the module control signal lines 230, and outputs ID control signals 330 to the DQ routing circuits 320, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module control signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK0. Each DQ routing circuit 320 is configured to enable data communication between the respective DQ signal line 322 with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

[0063] In certain embodiments, the ID control circuit 310 also provides a delay signal DS, which is used by the DQ routing circuits 320 to align read data output by the isolation device 118 with read data output by the other isolation devices 118, as explained in further detail below. In certain embodiments, the ID control circuit 310 regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK0 and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

[0064] The memory devices 112 are coupled to the isolation devices 118 via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. 4A, memory devices M_{11}, M_{12}, M_{13}, and M_{14} in the first group of memory devices can be coupled to the isolation device ID-1 via a same set of module data lines $Y\text{-}1_0$, $Y\text{-}1_1$, ..., $Y\text{-}1_{n-1}$ and module strobe line $Y\text{-}1_{DQS}$. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which

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can be different with respect to different subgroups of memory devices.

[0065] Alternatively, as shown in FIG. 4B, memory devices M_{11} and M_{13}, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines YA-1_0, YA-1_1, ..., YA-1_n and module strobe line YA-1_{DQS} and memory devices M_{12} and M_{14}, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines YB-1_0, YB-1_1, ..., YB-1_n and module strobe line YB-1_{DQS}. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board 119. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards 119, or stacked over each other, and/or over the associated isolation device.

[0066] Multiple memory devices having a data width that is less than a data width of the isolation devices 118 may be used in place of one of the memory devices 112, which has the same data width as that of the isolation devices. For example, as shown in FIG. 5A, two memory devices M_{11-1} and M_{11-2} may be used in place of the memory device M_{11}. Each of the two memory devices M_{11-1} and M_{11-2} has a data width of 4, and together they act like a memory device M_{11} of a data width of 8. Thus, memory device M_{11-1} is coupled to the isolation device ID-1 via module data lines YA-1_0, ..., YA-1_3 and module strobe line YA-1_{DQS-1} while memory circuit M_{11-2} is coupled to the isolation device ID-1 via module data lines YA-1_4, ..., YA-1_7 and module strobe line YA-1_{DQS-2}.

[0067] In another embodiment, as shown in FIG. 5B, four memory devices M_{11-1} to M_{11-4} may be used as the memory device M_{11}. Each of the four memory devices M_{11-1} to M_{11-4} has a data width of 4, and together they act like a memory device M_{11} of a data width of 16. Thus, memory device M_{11-1} is coupled to the isolation device ID-1 via module data lines YA-1_0, ..., YA-1_3 and module strobe line YA-1_{DQS-1} while memory device M_{11-2} is coupled to the isolation device ID-1 via module data lines YA-1_4, ..., YA-1_7 and module strobe line YA-1_{DQS-2}, and so on.

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[0068] FIG. 6 illustrates the ID control circuit 310 in an isolation device 118. As shown, the ID control circuit 310 includes a clock buffer 610 to receive the module clock signal CK from the module control device 116, and to output a module clock signal CK0. The ID control circuit 310 further includes a strobe routing circuit 620 that are coupled on one side to the corresponding system DQS signal line 324 and on another side to the corresponding module DQS signal lines YA_{DQS} and YB_{DQS}. The ID control circuit 310 further includes a receiver circuit 630 with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit 310 further includes a command processing circuit 640 that provides the received, decoded, and/or otherwise processed module control signals 330 to the DQ routing circuits 320 and the strobe routing circuit 620 either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits 320 and the strobe routing circuit 620 to selectively enabling data communication between the MCH 101 and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

[0069] The strobe routing circuit 620 also buffers strobe signals received from either the MCH 101 or the memory devices 112, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits 320. In one embodiment, the ID control circuit 310 further includes a delay control circuit 650 that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit 320 and the strobe routing circuit 620. The delay amount is provided to the DQ routing circuit 320 and the strobe routing circuit in a delay signal DS.

[0070] In a receiver circuit 630, the respective MCS is received in accordance with the module clock signal CK0. In one embodiment, receiver circuit 630 samples the respective MCS using rising (or falling) edges of the module clock CK0. Since the isolation devices 118 are distributed across the memory module 110 at positions corresponding to the respective groups of memory devices, the module control signal lines 230 that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as

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shown in FIG. 7. As the MCS and CK0 travel along their respective module control signal lines 710 and 720, they can become misaligned with each other when they reach the input pins 730 of an isolation device 118.

[0071] For example, a module control signal, like the MCS 810 shown in FIG. 8, can be perfectly aligned with the module clock signal CK, with a rising edge 801 of the module clock signal CK being at a center of a data eye 802, when the MCS signal and the clock signal leave the module control circuit 116. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS 820 with respect to the CK signal, i.e., the rising edge 801 of the clock signal is near a left edge of a data eye of the MCS 820, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS 830, can be shifted with respect to the module clock signal such that a rising edge 801 of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS 840, can be so shifted with respect to the module clock signal such that a rising edge 801 of the clock signal falls in the glitches 803 at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

[0072] In one embodiment, as shown in FIG. 9, a receiver circuit 630 includes a metastability detection circuit (MDC) 910 to determine a metastability condition in a corresponding module control signal MCS0. In one embodiment, the MDC 910 generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS0. The MDC 910 also generates one or more metastability indicators and outputs the one or more metastability indicators via lines 912 and/or 914.

[0073] The receiver circuit 630 further includes a signal selection circuit 920 that receives the module clock CK and the at least one delayed version of the module clock via signal lines 916. The signal selection circuit 920 also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines 918. The signal selection circuit 920 selects a clock signal CK_i from among the module clock CK and the at

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least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit 920 may also select an MCS signal MCS_i from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.

[0074] The receiver circuit 630 further includes a sampler or register circuit 930 that samples the selected module control signal MCS_i according to the selected clock signal CK_i and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit 640 for further processing (if needed) before being provided to the DQ routing circuits 320 and DQS routing circuit 620.

[0075] FIG. 10A illustrates an MDC 910 according to one embodiment. As shown, the MDC 910 includes a delay circuit 1012 that generates a delayed version MCS1 of the corresponding MCS0 by adding a predetermined amount of delay (e.g., 10ps) to MCS0. MDC 910 also includes a delay circuit 1016 that generates a delayed version CK1 of the clock signal CK0 by adding a predetermined amount of delay to CK0. In one embodiment, CK1 is delayed from CK0 by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC 910 further includes a sampler circuit 1042 that samples MCS1 according to CK0 and outputs a sampled result A, a sampler circuit 1044 that samples MCS0 according to CK0 and outputs a sampled result B, and a sampler circuit 1046 that samples MCS0 according to CK1 and outputs a sampled result C. The MDC 910 further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z1 and Z2 based on the sampled results A, B, and C.

[0076] In one embodiment, Z1 is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., $Z1 = \overline{A \oplus B}$, and Z2 is the result of another logic operation on the sampled results, e.g., $Z2 = \overline{B \oplus C}$. Thus, as shown in FIG. 10B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge 1061 of CK0 is close to the right side of a data eye where gliches at the edges of the data eyes can make C unpredicatable, A and B can be in agreement (i.e., Z1 is true) while B and C are likely not in agreement (i.e., Z2 is false). FIG. 10 C illustrates a metastability condition

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when there is insufficient set-up time. As shown in FIG. 10C and Table 1 below, a rising clock edge 1061 of CK0 is close to the left side of a data eye where gliches at the edges of the data eyes can make A unpredicatable. Thus, A and B can be in disagreement so Z1 is false while B and C can be in agreement so Z2 is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge 1061 of CK0 and the rising clock edge 1062 of CK1 are near the middle of an MCS0 data eye so there is no metastability issues and both Z1 and Z2 are true, as shown in Table 1.

[0077] FIG. 10D illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1071 that selects between CK0 and CK1 based on the metastability indicator Z1, and a second multiplexor 1072 that selects between MCS0 and MCS1 based on the metastability indicator Z2. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, Z1=1 and Z2=0, and MCS1 is output from multiplexor 1071 while CK0 is output from multiplexor 1072. Sampler 930 thus samples MCS1 according to the rising edges of CK0. Thus, more hold time is provided to mitigate the metastability condition since MCS1 is shifted from MCS0 toward the right.

[0078] On the other hand, where a metastability condition of insufficient set-up time occurs, Z1=0 and Z2=1, and CK1 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. Sampler 930 thus samples MCS0 according to the rising edges of CK1. Since CK1 is shifted from CK0 toward the right, more set-up time is provided to mitigate the metastability condition.

Table 1 Metastability Detection and Signal Selection

Sampler Output			MS Indicators		MS Condition	Signal Selection	
A	B	C	Z1	Z2		CK	MCS
D1	D1	D2	1	0	insufficient hold time	CK0	MCS1
D1	D2	D2	0	1	insufficient set-up time	CK1	MCS0
D1	D1	D1	1	1	no metastability	CK0	MCS0

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[0079] In the case when no metastability is detected, Z1=1 and Z2=1, and CK0 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

[0080] FIGS. 10A-10D illustrate a relatively simple implementation of the metastability detection circuit (MDC) 910 where only three different sample points are provided to detect metastability condition in the module control signal. In general, the MDC 910 may generate more delayed versions of the module clock signal CK0 and/or the corresponding module control signal MCS0, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. 11A, the MDC 910 can include a plurality of delay circuits 1102 that generate *m* delayed versions of MCS0, e.g., MCS1, MCS2, ... MCS*m*, and *m* delayed versions of CK0, e.g., CK1, CK2, ..., CK*m*. The MDC 910 can include sampler circuits 1104 that sample MCS0 according to CK0, CK1, ..., CK*m*, respectively, and sampler circuits 1104 that sample MCS0, MCS1, MCS2, ... MCS*m* according to CK0, respectively. The outputs of the samplers 1104 are provided to a logic circuit 1120, which determines a metastability condition in MCK0 based on the sampler outputs using, for example, a majority decision logic. The logic circuit 1120 outputs a first metastability indicator on line(s) 912 and a second metastability indicator on line(s) 914.

[0081] FIG. 11B illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1171 that selects between CK0, CK1, ..., CK*m* based on the metastability indicator provided on line(s) 912, and a second multiplexor 1172 that selects between MCS0, MCS1, ..., MCS*m* based on the metastability indicator provided on line(s) 914, such that the rising edges of the selected clock signal, e.g., Ck*i*, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCS*i*. The selected signals MCS*i* and Ck*i* are provided to the sampler 930, which samples MCS*i* according to the rising edges of CK*i*.

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[0082] As stated above, in certain embodiments, since the isolation devices 118 are in the data paths between the MCH 101 and the respective groups of memory devices 112, the MCH 101 does not have direct control of the memory devices 112. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation, as discussed further below.

[0083] FIG. 12A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit 116 at time t1, the module control circuit 116 outputs one or more enable signals EN at time t2 in response to the write commands. The one or more enable signals are received by an isolation device 118 at time t3, which afterwards receives one or more strobe signal DQS from the MCH 101 at time t4. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system 100, and is controllable by the MCH 101 and knowable to the isolation device 118. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device 118 since both these signals are received by the isolation device. Based on such determination, the isolation device 118 can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device 118 to properly time transmission of read data to the MCH, as explained further below.

[0084] FIG. 12B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit 116 at time t5, the module control circuit 116 outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device 118 at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective

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group of memory devices. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices 118.

[0085] With knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101 via the respective group of data/strobe signal lines 130, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system 100.

[0086] The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit 650 in the ID control circuit 310, as shown in FIG. 6. According to one embodiment, as shown in FIG. 13, the delay control circuit 650 includes a peramble detector 1310 to detect a write preamble in the DQS, a flip-flop circuit 1320 having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK0, and a counter circuit 1330 having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit 1320. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

[0087] FIG. 14 illustrates a DQ or DQS routing circuit 320 or 620 according to an embodiment. As shown, the DQ/DQS routing circuit 320/620 includes a DQ/DQS pin 1401 that is coupled to the corresponding DQ/DQS signal line 322/324, a set of one or more DQS pins 1402 that is coupled to a corresponding module DQ/DQS line(s) Y/Y_{DQS}, or YA/YA_{DQS} and YB/YB_{DQS}. The DQ/DQS routing circuit 320/620 further includes a write strobe buffer 1410 that buffers write data/strobe, and a write data/strobe receiver 1420 that samples the write data/strobe. The DQ/DQS routing circuit 320/620 further includes a

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plurality of write paths 1430 that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

[0088] The DQS routing circuit further includes a plurality of read paths 1450 that are selectable by the one or more of the module control signals. Output from the seleted read path is delayed in a delay circuit 1460 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1470. The sampled read data/strobe is transmitted by transmitter 1480 onto the corresponding data/strobe signal line 322/324 via the DQ/DQS pin 1401.

[0089] FIG. 15 illustrates a DQS routing circuit 620 according to an embodiment. As shown, the DQS routing circuit 620 includes a first DQS pin 1501 that is coupled to a corresponding DQS signal line 324, a second DQS pin 1502A that is coupled to a corresponding module DQS line YA_{DQS}, a third DQS pin 1502B that is coupled to a corresponding module DQS line YB_{DQS}. The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe path includes a write strobe buffer 1510 that buffers a write strobe, a write strobe receiver 1520 that samples the write strobe according to the buffered module signal CK0. The sampled write strobe is provided to the DQ routing circuits 320 as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter 1530A that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YA_{DQS}. The second write strobe path includes the write strobe buffer 1510, the write strobe receiver 1520, and a second write strobe transmitter 1530B that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YB_{DQS}. The first and second write strobe transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0090] The DQS routing circuit further includes a read strobe path coupled between the

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first DQS pin 1501 and a selected one of the second and third DQS pins 1502A and 1502B. In the read strobe path, a select circuit 1550 (e.g., a multiplexor) selects either a read strobe signal received via DQS pin 1502A or a read strobe signal received via DQS pin 1502B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0. The sampled read strobe is provided to the DQ routing circuits 320 as the read strobe RDQS and is transmitted by transmitter 1580 onto the corresponding strobe signal line 324 via the first DQS pin 1501.

[0091] FIG. 16 illustrates a DQ routing circuit 320 according to an embodiment. As shown, the DQ routing circuit 320 includes a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line YA_{DQ}, a third DQ pin 1602B that is coupled to a corresponding module DQ line YB_{DQ}. The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer 1610, a write data receiver 1620 that samples write data according to the write strobe WDQS from the DQS routing circuit 620, and a first write data transmitter 1630A that transmits the write data to one or more memory devices 112 coupled to the module data line YA_{DQ}. The second write data path includes the write data buffer 1610, the write data receiver 1620, and a second write data transmitter 1630B that transmits the write data to one or more memory devices 112 coupled to the module data line YB_{DQ}. The first and second write data transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0092] The DQ routing circuit further includes a read data path coupled between the first DQ pin 1601 and a selected one of the second and third DQ pins 1602A and 1602B. In the read data path, a select circuit 1650 (e.g., a multiplexor) selects either a read data signal

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received via DQ pin 1602A or a read data signal received via DQ pin 1602B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.

[0093] FIG. 17 illustrate a delay circuit 1560 or 1660 according to an embodiment. As shown, the delay circuit 1560 or 1660 includes a plurality of delay stages, such as delay stages 1710, 1720, and 1730, each delaying a read data or read strobe signal from the select circuit 1550/1650 by a predetermined amount. The delay circuit 1560 or 1660 further includes a select circuit 1740 (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit 1740, is provided to the sampler circuit 1570 or 1670, either directly or after being buffered by a buffer circuit 1750.

[0094] Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device 118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

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[0095] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.

[0096] As shown in FIG. 18, a delay signal DS is generated according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.

[0097] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100.

[0098] In certain embodiments, especially the embodiments shown in FIG. 2D, the delay circuits 1560 and 1660 shown in FIGS. 15 and 16 are not needed to provide alignment of the read data. As shown in FIG. 19, the ID control circuit 310 includes a clock regeneration

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circuit 1920 that regenerates the clock signal CK received from the control circuit 116, according to the delay signal DS. The regenerated clock signals CK0 and CKM each includes a proper amount of delay as compared to the clock signal CK. The clock CK0 is provided to the strobe routing circuit 620 so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer 118 and the respective set of memory devices are locally synchronized.

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WE CLAIM:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

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MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN A PLURALITY OF DATA BUFFERS

ABSTRACT OF THE DISCLOSURE

A memory module is operable in a memory system with a memory controller. The memory module comprises memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data/strobe signal lines in a data bus and respective sets of the memory devices. Each respective buffer circuit includes a data path corresponding to each data signal line in the corresponding set of data/strobe signal lines, and a command processing circuit configured to decode module control signals from the module control circuit and to control the data path in accordance with the module control signals. The data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

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Customer No. 79141
Attorney Docket No.: NT003US

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/952,599 filed on July 27, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.
(Name of Assignee)

of **51 Discovery, Suite #150, Irvine, CA 92618**
(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 10/9/2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date: 10/14/2013

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DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 15820076 Document Date: 11/21/2017

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

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Form Revision Date: August 26, 2013

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/820,076

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/820,076	11/21/2017	2139	1600	N3044.10009US05	1	1

CONFIRMATION NO. 8866

FILING RECEIPT

79141
Jamie J. Zheng, Ph.D Esq.
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1389 Center Drive
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Date Mailed: 12/26/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/426,064 02/07/2017 PAT 9824035
which is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

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If Required, Foreign Filing License Granted: 12/20/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/820,076**

Projected Publication Date: 04/05/2018

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	N3044.10009US05	8866

79141 7590 01/25/2018

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
01/25/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

Office Action Summary	Application No. 15/820,076	Applicant(s) LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/21/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/21/2017* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Continuation filed on 11/21/2017.

Claim 1 is pending for this examination.

Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the

scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of

copending Application No. 13/952,599, now US Patent No. 9,128,632, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 13/952,599, now US Patent No. 9,128,632**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in	Independent claim 1	A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals; memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and a plurality of buffer circuits to receive the module control signals, each respective buffer

	response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module		circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

	control signals.		
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

Claims	**Instant Application**	Claims	**copending Application No. 15/426,064, now US Patent No. 9,824,035**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus; a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory

	control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module		command signals; and memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory' devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory

	clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.		operation and to control timing of the data and strobe signals on the subset of the data paths in accordance with the timing information.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035, and as such would be rendered obvious over the already allowed claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

Claims	**Instant Application**	Claims	**copending Application No. 14/846,993, now US Patent No. 9,563,587**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board including edge connections for connecting to respective ones of the signal lines in the memory bus;

	a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and. a respective set of memory devices, and configured to receive the module control signals and the module clock,		memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals; wherein the each respective buffer circuit is configured to respond to one or more first control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation;

	the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.		wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

Allowable Subject Matter

Claim 1 is allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724. The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 15/820,076	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0029370 A1	01-2014	KOSHIZUKA; Atsuo	G11C7/1051	365/233.13
*	B	US-2006/0077731 A1	04-2006	Ware; Frederick A.	G11C5/04	365/194
*	C	US-2007/0217559 A1	09-2007	Stott; Bret G.	G11C7/1051	375/355
*	D	US-2010/0271092 A1	10-2010	Zerbe; Jared L.	G06F13/4243	327/161
*	E	US-8,214,616 B2	07-2012	Ware; Frederick A.	G06F13/1684	711/104
*	F	US-8,949,519 B2	02-2015	Rajan; Suresh Natarajan	G11C5/02	365/189.2
*	G	US-2002/0039323 A1	04-2002	Tokutome, Hiroto	G11C7/1066	365/233.12
*	H	US-2008/0037412 A1	02-2008	Geile; Michael J.	G06F17/14	370/208
*	I	US-7,884,619 B1	02-2011	Chong; Yan	G01R31/3016	324/601
*	J	US-2012/0256639 A1	10-2012	Pausini; Marco	G01R31/31709	324/613
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/19/2018								
	1	✓								

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

CPC- SEARCHED		
Symbol	Date	Examiner
limited search of G06F 1/12	1/19/2018	MS
limited search of G06F 13/1689	1/19/2018	MS
limited search of G06F 12/0246	1/19/2018	MS
limited search of G06F 13/1694	1/19/2018	MS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search - see attached	1/19/2018	MS
Inventor Search - see attached EAST Search	1/19/2018	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	1/19/2018	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	1/19/2018	MS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S220	5002	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S221	2082	S220 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S222	210	S221 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S223	75	S222 AND (((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S224	75	S223 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S225	75	S224 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S226	75	S225 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S227	46	S226 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:15
S228	9	S227 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S229	4703	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/01/19 09:16

			IBM_TDB			
S230	110	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S231	584308	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S232	58299	S231 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S233	130	S231 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S234	51	S233 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:16
S235	761	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S236	1	S235 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S237	5899	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S238	966	S237 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S239	38	S238 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S240	8	S239 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:19
S241	175648	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/01/19 09:20

			IBM_TDB			
S242	2113	S241 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:20
S243	1739	S242 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:20
S244	1710	S243 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:20
S245	337	S244 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:20
S246	68	S245 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:20
S247	8092	memory module and buffer and tim$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:22
S248	1694	S247 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:22
S249	1272	S248 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:22
S250	361	S249 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:22
S251	10	S250 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:22
S252	10	S251 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/19 09:22
S253	7	S252 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/01/19 09:22

			IBM_TDB			
S254	427	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25
S255	315	S254 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25
S256	156	S255 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25
S257	137	S256 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25
S258	49	S257 and tim$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25
S259	14	S258 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/01/19 09:25

EAST Search History (Interference)

< This search history is empty>

1/ 19/ 2018 10:52:45 AM
C:\ Users\ msun\ Documents\ EAST\ Workspaces\ 15820076.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/820,076	11/21/2017	Hyun Lee	N3044.10009US05

CONFIRMATION NO. 8866

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

PUBLICATION NOTICE

Title:MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

Publication No.US-2018-0095908-A1
Publication Date:04/05/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Samsung Electronics Co., Ltd.
Ex. 1002, p. 101

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15820076
Filing Date	21-Nov-2017
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5049US
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
NETLIST, INC.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9128632

9563587

9824035

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Samsung Electronics Co., Ltd.
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- (●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.
- ( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ( ) Small Entity
- ( ) Micro Entity
- (●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 51167

- ( ) A sole inventor
- ( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ( ) A joint inventor; all of whom are signing this request

Signature	/ Jamie J. Zheng /
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15820076
Filing Date:	21-Nov-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15820076

Filing Date: 21-Nov-2017

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on May 24, 2018

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	32709570
Application Number:	15820076
International Application Number:	
Confirmation Number:	8866
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5049US
Receipt Date:	24-MAY-2018
Filing Date:	21-NOV-2017
Time Stamp:	16:49:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	052518INTEFSW00006558500310
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33939 d7670317605b4606b6f8dfedabb09ccd67f23036	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30555 31e09c79bc9115c45ed945f21d613a0bd4260599	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64494		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed May 24, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	8866
Serial No.:	15/820,076	Art Unit:	2184
Filed:	November 21, 2017	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS*	Attorney Docket No.:	129980-5049-US
		Date:	May 24, 2018

RESPONSE TO OFFICE ACTION & INTERVIEW SUMMARY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Office Action dated January 25, 2018 for the above identified patent application.

Petition for Extension of Time under 37 CFR 1.136. It is respectfully requested that the time for responding to the Office Action dated January 25, 2018 be extended for a period of one month from April 25, 2018 to May 25, 2018.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

McKesson Statement starts on page 2 of this paper.
Amendment to the Claims starts on Page 3 of this paper.
Remarks start on Page 6 of this paper.

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McKesson Statement

In view of *McKesson Information Solutions v. Bridge Medical* (Fed. Cir. 2007), Applicant wishes to inform the Examiner that the prosecution history of the following US Patent Application(s) may contain information relevant to the pending application:

(1) U.S. Application Serial No. 13/970,606, filed August 20, 2013. This application issued as U.S. Patent No. 9,606,907.

(2) U.S. Application Serial No. 15,470,856, filed March 27, 2017.

The Examiner is encouraged to review the art made of record, office actions and the notice(s) of allowance, if any, in the above-mentioned applications, all of which are available on PAIR.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 110

Electronic Patent Application Fee Transmittal

Application Number:	15820076
Filing Date:	21-Nov-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt

EFS ID:	32717177
Application Number:	15820076
International Application Number:	
Confirmation Number:	8866
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5049US
Receipt Date:	24-MAY-2018
Filing Date:	21-NOV-2017
Time Stamp:	16:51:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$200
RAM confirmation Number	052518INTEFSW00006893500310
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5049US_AMEND.pdf	153831 d717c2f44d898950d3aeba123b6b6ec6de188217	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	6	7
	Claims	3	5
	Amendment/Req. Reconsideration-After Non-Final Reject	1	2

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30970 ffbb6099932af06fbb9c18725a85759bb5193e13	no	2

Warnings:

Information:

Total Files Size (in bytes):	184801

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

This amendment responds to the office action mailed January 25, 2018. In the office action, the Examiner:

A. rejected claim 1 on the ground of nonstatutory obviousness-type double patenting.

REMARKS CONCERNING CLAIMS

Claim 1 has been amended for minor issues.

Claims 2-12 have been added.

No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 1-12.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

A. Rejection of claim 1 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d), which should overcome the nonstatutory obviousness-type double patenting rejction over claims 1-22 of US Patent No. 9,824,035; claims 1-20 of US Patent No. 9,563,587; and claims 1-20 of US Patent No. 9,128,632.

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CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the Examiner, Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In particular, Applicant's filing of the terminal disclaimer is for the sole purpose of expediting prosecution. It should not be understood as implying that Applicant agrees with the rejection of claim 1 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-7249, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 24, 2018

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-7249

DB2/ 33351823.1

Samsung Electronics Co., Ltd.
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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive command signals for memory operations ~~a first operation~~ via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the memory operations ~~first operation~~ in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes at least one ~~a~~ tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount

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determined by the command processing circuit in response to at least one of the module control signals.

2. (New) The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.

3. (New) The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.

4. (New) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

5. (New) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

6. (New) The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a

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metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

7. (New) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

8. (New) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

9. (New) The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

10. (New) The memory module of claim 9, wherein the data paths include a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

11. (New) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

12. (New) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/820,076	Filing Date 11/21/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **05/24/2018**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X $100 =	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $460 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
VIOLA ROGERS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 07/03/2018

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 07/03/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	10/03/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	10/03/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2184	710-310000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

79141 7590 07/03/2018

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 07/03/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Notice of Allowability	Application No. 15/820,076	Applicant(s) LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's Amendment filed 5/24/2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-12*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Samsung Electronics Co., Ltd.
Ex. 1002, p. 126

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Amendment filed 5/24/2018.

Claims 1-12 are pending for this examination.

Claim 1 was amended.

Claims 2-12 were added.

Terminal Disclaimer

The terminal disclaimer filed on 5/24/2018 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 9,128,632; US Patent No. 9,563,587; and US Patent No. 9,824,035 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module

system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724. The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 15/820,076	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0029370 A1	01-2014	KOSHIZUKA; Atsuo	G11C7/1051	365/233.13
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC						
Symbol					**Type**	**Version**
G06F		13	/	1673	F	2013-01-01
G06F		3	/	0659	I	2013-01-01
G11C		16	/	00	I	2013-01-01
G11C		5	/	04	I	2013-01-01
G11C		7	/	1006	I	2013-01-01
G11C		7	/	1066	I	2013-01-01
G11C		7	/	109	A	2013-01-01
G11C		7	/	1093	I	2013-01-01
G11C		8	/	12	A	2013-01-01
G06F		1	/	10	I	2013-01-01
G06F		3	/	0613	I	2013-01-01
G06F		3	/	0647	I	2013-01-01
G06F		3	/	0683	I	2013-01-01
G06F		13	/	28	I	2013-01-01
G06F		13	/	4027	I	2013-01-01
G06F		3	/	0656	I	2013-01-01
G06F		13	/	1642	I	2013-01-01
G11C		8	/	18	I	2013-01-01
G11C		7	/	20	A	2013-01-01
G11C		29	/	023	I	2013-01-01
G11C		29	/	028	I	2013-01-01
H05K		999	/	99	I	2013-01-01
G11C		2029	/	0407	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 12	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 (Primary Examiner)	06/23/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
710	5

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	6	7			
711	1	2	3	4	154
711	155				

INTERNATIONAL CLASSIFICATION					
CLAIMED					**NON-CLAIMED**
G	0	6	F	3 / 00 (2006.01.01)	
G	0	6	F	12 / 00 (2006.01.01)	
G	0	6	F	13 / 00 (2006.01.01)	

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184	06/23/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														
7	7														
8	8														
9	9														
10	10														
11	11														
12	12														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184	06/23/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Samsung Electronics Co., Ltd.
Ex. 1002, p. 133

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S260	5100	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S261	2127	S260 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S262	213	S261 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S263	76	S262 AND (((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S264	76	S263 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S265	76	S264 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S266	76	S265 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S267	46	S266 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S268	9	S267 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S269	4852	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/06/23 06:30

			IBM_TDB			
S270	113	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:30
S271	603648	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:31
S272	60216	S271 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:31
S273	139	S271 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:31
S274	58	S273 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:31
S275	793	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:32
S276	1	S275 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:32
S277	6213	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:33
S278	988	S277 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:33
S279	41	S278 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:33
S280	9	S279 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:33
S281	180115	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/06/23 06:35

			IBM_TDB			
S282	2169	S281 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:35
S283	1781	S282 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:35
S284	1751	S283 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:35
S285	354	S284 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:35
S286	72	S285 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:35
S287	8353	memory module and buffer and tim$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:36
S288	1737	S287 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:36
S289	1302	S288 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:36
S290	372	S289 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:36
S291	10	S290 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:36
S292	10	S291 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/06/23 06:36
S293	7	S292 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/06/23 06:36

			IBM_TDB			
S294	440	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37
S295	323	S294 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37
S296	160	S295 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37
S297	141	S296 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37
S298	51	S297 and tim$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37
S299	14	S298 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/06/23 06:37

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S300	4730	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory).clm. and (buffer).clm.	US-PGPUB; USPAT	ADJ	ON	2018/06/23 13:54
S301	417	S300 and (delay or time interval).clm.	US-PGPUB; USPAT	ADJ	ON	2018/06/23 13:54
S302	275	S301 and (read or write).clm.	US-PGPUB; USPAT	ADJ	ON	2018/06/23 13:54
S303	3	S302 and (time transmitting or time transmission).clm.	US-PGPUB; USPAT	ADJ	ON	2018/06/23 13:54

6/23/2018 2:02:47 PM
C:\Users\msun\Documents\EAST\Workspaces\15820076.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15820076	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

CPC- SEARCHED		
Symbol	Date	Examiner
limited search of G06F 1/12	6/23/2018	MS
limited search of G06F 13/1689	6/23/2018	MS
limited search of G06F 12/0246	6/23/2018	MS
limited search of G06F 13/1694	6/23/2018	MS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Updated EAST Search - see attached	6/23/2018	MS
Inventor Search - see attached EAST Search	6/23/2018	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	6/23/2018	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	6/23/2018	MS
Google Scholar Search - search terms used: (memory module and buffering); (memory and buffer and tristate buffer); (memory and tristate buffer and delay)	6/23/2018	MS

INTERFERENCE SEARCH

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
710	limited search of subclasses 5, 6, and 7	6/23/2018	MS
711	limited search of subclasses 1, 2, 3, 4, 154, and 155	6/23/2018	MS
G06F	limited search of 1/12, 13/1689, 12/0246, and 13/1694	6/23/2018	MS

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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Ex. 1002, p. 139

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 8866

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/820,076	11/21/2017	710	2184	129980-5049US

APPLICANTS

Netlist, Inc., Irvine, CA;

INVENTORS

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 15/426,064 02/07/2017 PAT 9824035
which is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/20/2017

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/MICHAEL SUN/ Examiner's Signature	Initials	CA	26	4 → 12	1

ADDRESS

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

TITLE

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Electronically filed	October 3, 2018
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	Sun, Michael
Attorney Docket No.	129980-5049-US

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. Submission required under 37 C.F.R. § 1.114

NOTE: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission.
   - i. ☐ Request for non-entry of amendment: Please **do not** entered the amendment submitted on _____
   - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed _____
   - iii. ☐ Other _____

b. ☒ Enclosed
   - i. ☐ Amendment/Reply
   - ii. ☐ Affidavit(s)/Declaration(s)
   - iii. ☒ Information Disclosure Statement (IDS)
   - iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)

b. ☐ Other _____

3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).
   - i. ☒ (1st request) RCE fee required under 37 C.F.R. § 1.17(e)(1), estimated to be $1300 (large entity) or $650 (small entity)
   - ii. ☐ (2nd or subsequent request) RCE fee required under 37 C.F.R. § 1.17(e)(2), estimated to be $1900 (large entity) or $950 (small entity)
   - iii. ☐ Extension of time fee required under 37 C.F.R. §§ 1.136 and 1.17, estimated to be $ for a month(s) extension, the request for which is being made herewith
   - iv. ☐ Other _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Jamie J. Zheng	*Registration No. (Attorney/Agent)*	51,167
Signature		*Date*	October 3, 2018

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or by facsimile transmitted to fax no. 1-703- to the U.S. Patent and Trademark Office on the date indicated below.

Name (Print/Type)		*Registration No. (Attorney/Agent)*	
Signature		*Date*	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 141

Electronically filed October 3, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Lee et al.	Confirmation No.:	8866
Serial No.:	15/820,076	Art Unit:	2184
Filed:	November 21, 2017	Examiner:	Sun, Michael
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	Attorney Docket No.:	129980-5049-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language

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abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account

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No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. **15/426,064**, filed on **February 7, 2017**; **14/846,993**, filed on **September 7, 2015** and **13/952,599**, filed on **July 27, 2013**, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

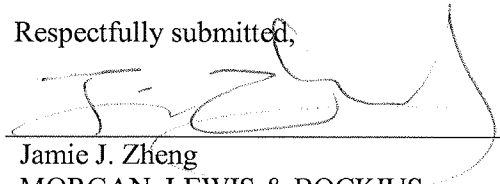
9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: October 3, 2018



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | 1 | of | 18

Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049-US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (If known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4218740	08-19-1980	MOTOROLA INC	
	2.	4249253	02-03-1981	Gentili et al.	
	3.	4368515	01-11-1983	Nielsen	
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	41.	5764590	06-09-1998	Mitsubishi Electric Corp	
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	102	6658509	12-02-2003	Bonella et al.	
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	138	7007175	02-28-2006	Chang et al.	
	139	7046538	05-16-2006	Kinsley et al.	
	140	7047361	05-16-2006	Phison Electronic	
	141	7054179	05-30-2006	Cogdill et al.	
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	143	7072231	07-04-2006	Pax	
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	171	7532537	05-12-2009	Solomon et al.	
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Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.1	Document Number / Number-Kind Code 2 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures
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Examiner Name	SUN, Michael
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	229.	13/970,606	8/20/20	Netlist,	Entire Prosecution
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First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.aov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where oublished.	T'
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	14	of	18	Attorney Docket Number	*129980-5049-US*

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	18.	W099/30240	6-17-1999	Intel Corporation		

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Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	15	of	18	Attorney Docket Number	*129980-5049-US*

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	26.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Objections to Evidence, filed February 29, 2016
	27.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Reply, filed May 19, 2016
	28.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016
	29.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
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	31.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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Examiner's Signature		Date Considered	

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				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	18	of	18	Attorney Docket Number	*129980-5049-US*

	91.	Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	92.	Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015
	93.	Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
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	95.	Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
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	98.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
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	101.	Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	102.	Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
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Examiner's Signature		Date Considered	

Electronically filed October 3, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Lee et al.	Confirmation No.:	8866
Serial No.:	15/820,076	Art Unit:	2184
Filed:	November 21, 2017	Examiner:	Sun, Michael
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	Attorney Docket No.:	129980-5049-US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 470 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on commonly-owned U.S. Pat. App. Nos. 15/470,856, filed March 27, 2017; 13/970,606, filed August 20, 2013; 12/761,179, filed April 15, 2010, and 12/504,131, filed July 16, 2009, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 164

This Information Disclosure Statement is being filed with the filing of a Request for Continued Examination, and presumably no fee is required. The Commissioner is authorized to charge any required fees to Deposit Account No. 50-0310 (order no. 129980-5049-US).

Respectfully submitted,

Date: October 3, 2018

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NON PATENT LITERATURE DOCUMENTS

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Examiner's Signature		Date Considered	

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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	***15/820,076***
				Filing Date	***November 21, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2184***
				Examiner Name	***SUN, Michael***
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				Application Number	*15/820,076*
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				First Named Inventor	*Hyun Lee*
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
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				Art Unit	*2184*
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Art Unit	*2184*
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		Non-Final Action mailed October 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579)
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		Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed Oct. 20, 2010, 17 pages.
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		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Complaint For Patent Infringement, filed Sept. 22, 2009 in 10 pages.

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	22	of	29	Attorney Docket Number	*129980-5049-US*

		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant lnphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages.
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		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant lnphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages.
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	23	of	29	Attorney Docket Number	*129980-5049-US*

		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Netlist, lnc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages.
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	24	of	29	Attorney Docket Number	*129980-5049-US*

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		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, lnc.'s Reply Claim Construction Brief, filed Aug. 16, 2010 in 17 pages.
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		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc's Opening Claim Construction Brief, filed Jul. 16, 2010 in 162 pages.
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		Vogt, Pete, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity," Intel, Feb. 18, 2004, 33 pages.

US PATENT APPLICATIONS					
Examiner Initials	Cite No.	Application Number	Filing Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	25	of	29	Attorney Docket Number	*129980-5049-US*

		Reexam Appl. No. 95/000,546 for U.S. Pat. No. 7,289,386	05/11/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,578 for U.S. Pat. No. 7,619,912	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912	10/21/2010	Netlist, Inc.	Entire File History
		Reexam App. No. 95/001,337 for U.S. Pat. No. 7,636,274	06/04/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,381 for U.S. Pat. No. 7,532,537	06/09/2010	Netlist, Inc.	Entire File History
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	26	of	29	Attorney Docket Number	*129980-5049-US*

		12/577,682	10/12/2009	Netlist, Inc.	Entire Prosecution History
		12/954,492	11/24/2010	Netlist, Inc.	Entire Prosecution History
		12/912,623	10/26/2010	Netlist, Inc.	Entire Prosecution History
		11/335,875	01/19/2006	Netlist, Inc.	Entire Prosecution History
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	27	of	29	Attorney Docket Number	*129980-5049-US*

		14/229,844	03/29/2014	Netlist, Inc.	Entire Prosecution History
		12/504,131	07/16/2009	Netlist, Inc.	Entire Prosecution History
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		13/952,599	07/27/2013	Netlist, Inc.	Entire Prosecution History

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	28	of	29	Attorney Docket Number	*129980-5049-US*

PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		CN102576565B	09-30-2015	Netlist, Inc.		

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
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		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of *Inter Partes* Review, filed August 6, 2018
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Examiner's Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	***15/820,076***
				Filing Date	***November 21, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2184***
				Examiner Name	***SUN, Michael***
Sheet	29	of	29	Attorney Docket Number	***129980-5049-US***

		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of *Inter Partes* Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

Examiner's Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	15820076
Filing Date:	21-Nov-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Gary Scott Williams/Edith Fuentes
Attorney Docket Number:	129980-5049US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt

EFS ID:	33912832
Application Number:	15820076
International Application Number:	
Confirmation Number:	8866
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Gary Scott Williams/Edith Fuentes
Filer Authorized By:	Gary Scott Williams
Attorney Docket Number:	129980-5049US
Receipt Date:	03-OCT-2018
Filing Date:	21-NOV-2017
Time Stamp:	20:36:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1300
RAM confirmation Number	100418INTEFSW00006576500310
Deposit Account	
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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79141 7590 11/19/2018

Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 11/19/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	02/19/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 200

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 11/19/2018
Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	02/19/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Electronics Co., Ltd.
Ex. 1002, p. 201

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

79141 7590 11/19/2018

Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 11/19/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Ex. 1002, p. 202

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/820,076	Applicant(s) Lee et al.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Applicant's RCE filed 10/03/2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/03/2018; 10/03/2018.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Samsung Electronics Co., Ltd.
Ex. 1002, p. 204

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Request for Continued Examination filed 10/03/2018.

Claims 1-12 are pending for this examination.

Information Disclosure Statement

The information disclosure statements (IDSs) submitted on 10/03/2018; and 10/03/2018 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Examiner notes that in both IDSs filed 10/03/2018, there were many Non-Patent Literature Documents and Foreign Patent Documents that were listed throughout without any corresponding copy of these documents attached to review. As such, these listings were not considered as Examiner had no copy of these documents to review.

Allowable Subject Matter

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module

systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724. The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/820,076	Lee et al.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC								
Symbol							**Type**	**Version**
G06F	/	13	/	1673			F	2013-01-01
G06F	/	3	/	0659			I	2013-01-01
G11C	/	16	/	00			I	2013-01-01
G11C	/	5	/	04			I	2013-01-01
G11C	/	7	/	1006			I	2013-01-01
G11C	/	7	/	1066			I	2013-01-01
G11C	/	7	/	1093			I	2013-01-01
G06F	/	1	/	10			I	2013-01-01
G06F	/	3	/	0613			I	2013-01-01
G06F	/	3	/	0647			I	2013-01-01
G06F	/	3	/	0683			I	2013-01-01
G06F	/	13	/	28			I	2013-01-01
G06F	/	13	/	4027			I	2013-01-01
G06F	/	3	/	0656			I	2013-01-01
G06F	/	13	/	1642			I	2013-01-01
G11C	/	8	/	18			I	2013-01-01
G11C	/	29	/	023			I	2013-01-01
G11C	/	29	/	028			I	2013-01-01
G11C	/	7	/	109			A	2013-01-01
G11C	/	8	/	12			A	2013-01-01
G11C	/	7	/	20			A	2013-01-01
G11C	/	2029	/	0407			A	2013-01-01

CPC Combination Sets								
Symbol							**Type**	**Set**	**Ranking**	**Version**
	/		/							

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/MICHAEL SUN/ Primary Examiner, Art Unit 2184	15 October 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20181015

Samsung Electronics Co., Ltd.
Ex. 1002, p. 208

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/820,076	Lee et al.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F	/	3	/	00
G06F	/	12	/	00
G06F	/	13	/	00

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
710	5

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					
710	6	7				
711	1	2	3	4	154	
711	155					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 12	
/MICHAEL SUN/ Primary Examiner, Art Unit 2184 (Primary Examiner)	15 October 2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Samsung Electronics Co., Ltd.
Ex. 1002, p. 209

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/820,076	Lee et al.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10												
2	2	11	11												
3	3	12	12												
4	4														
5	5														
6	6														
7	7														
8	8														
9	9														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/MICHAEL SUN/ Primary Examiner, Art Unit 2184	15 October 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20181015

Samsung Electronics Co., Ltd.
Ex. 1002, p. 210

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/820,076	Lee et al.
	Examiner	Art Unit
	MICHAEL SUN	2184

CPC - Searched*		
Symbol	**Date**	**Examiner**
limited search of G06F 1/12	10/14/2018	MS
limited search of G06F 13/1689	10/14/2018	MS
limited search of G06F 12/0246	10/14/2018	MS
limited search of G06F 13/1694	10/14/2018	MS

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Updated EAST Search - see attached	10/14/2018	MS
Inventor Search - see attached EAST Search	10/14/2018	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	10/14/2018	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	10/14/2018	MS
Google Scholar Search - search terms used: (memory module and buffering); (memory and buffer and tristate buffer); (memory and tristate buffer and delay)	10/14/2018	MS

/MICHAEL SUN/ Primary Examiner, Art Unit 2184	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 211

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/820,076	Lee et al.
	Examiner	Art Unit
	MICHAEL SUN	2184

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
710	limited search of subclasses 5, 6, and 7	10/14/2018	MS
711	limited search of subclasses 1, 2, 3, 4, 154, and 155	10/14/2018	MS
G06F	limited search of 1/12, 13/1689, 12/0246, and 13/1694	10/14/2018	MS

/MICHAEL SUN/ Primary Examiner, Art Unit 2184	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 212

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 8866

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/820,076	11/21/2017	710	2184	129980-5049US

APPLICANTS

Netlist, Inc., Irvine, CA;

INVENTORS

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 15/426,064 02/07/2017 PAT 9824035
which is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/20/2017

Foreign Priority claimed	❑ Yes ☑ No	❑ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	❑ Yes ☑ No					
Verified and Acknowledged	/MICHAEL SUN/ Examiner's Signature	Initials	CA	26	~~1~~ 12	1

ADDRESS

Morgan Lewis Bockius LLP (PA)-J. Zheng
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

TITLE

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	1	of	29	Attorney Docket Number	*129980-5049-US*

PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S/		5,784,705	07-21-1998	Leung	
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Examiner's Signature	/MICHAEL SUN/	Date Considered	10/26/2018

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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
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				Examiner Name	*SUN, Michael*
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Examiner Signature	/MICHAEL SUN/	Date Considered	10/15/2018

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				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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				First Named Inventor	*Hyun Lee*
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				Examiner Name	*SUN, Michael*
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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/M.S/		Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386	10/20/2010	Netlist, Inc.	Entire File History
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/M.S/		Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912	10/21/2010	Netlist, Inc.	Entire File History
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/M.S/		11/075,395	03/07/2005	Netlist, Inc.	Entire Prosecution History
/M.S/		11/173,175	07/01/2005	Netlist, Inc.	Entire Prosecution History
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				Art Unit	*2184*
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/M.S/		12/577,682	10/12/2009	Netlist, Inc.	Entire Prosecution History
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/M.S/		14/229,844	03/29/2014	Netlist, Inc.	Entire Prosecution History
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/M.S/		13/411,344	03/02/2012	Netlist, Inc.	Entire Prosecution History
/M.S/		13/952,599	07/27/2013	Netlist, Inc.	Entire Prosecution History

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		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018

Examiner's Signature	/MICHAEL SUN/	Date Considered	10/15/2018

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	29	of	29	Attorney Docket Number	*129980-5049-US*

		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of *Inter Partes* Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

Examiner's Signature	/MICHAEL SUN/	Date Considered	10/15/2018

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S304	5199	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S305	2176	S304 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S306	214	S305 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S307	79	S306 AND (((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S308	79	S307 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S309	79	S308 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S310	79	S309 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S311	46	S310 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S312	9	S311 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S313	4967	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/10/14 14:28

			IBM_TDB			
S314	114	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:28
S315	617831	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:30
S316	61717	S315 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:30
S317	145	S315 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:30
S318	62	S317 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:30
S319	805	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:31
S320	1	S319 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:31
S321	6524	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S322	998	S321 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S323	43	S322 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S324	9	S323 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S325	183274	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/10/14 14:33

			IBM_TDB			
S326	2205	S325 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S327	1810	S326 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S328	1778	S327 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S329	360	S328 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S330	74	S329 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:33
S331	8541	memory module and buffer and tim$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:34
S332	1759	S331 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:34
S333	1313	S332 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:34
S334	375	S333 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:34
S335	10	S334 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:34
S336	10	S335 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2018/10/14 14:34
S337	7	S336 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2018/10/14 14:34

			IBM_TDB			
S338	448	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37
S339	329	S338 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37
S340	161	S339 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37
S341	142	S340 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37
S342	51	S341 and tim$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37
S343	14	S342 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2018/10/14 14:37

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S344	4877	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory).clm. and (buffer).clm.	US-PGPUB; USPAT	ADJ	ON	2018/10/14 14:39
S345	434	S344 and (delay or time interval).clm.	US-PGPUB; USPAT	ADJ	ON	2018/10/14 14:39
S346	288	S345 and (read or write).clm.	US-PGPUB; USPAT	ADJ	ON	2018/10/14 14:39
S347	3	S346 and (time transmitting or time transmission).clm.	US-PGPUB; USPAT	ADJ	ON	2018/10/14 14:39

10/15/2018 7:20:47 AM
C:\Users\msun\Documents\EAST\Workspaces\15820076.wsp

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet | 1 | of | 18

Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049-US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (If known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S/	1.	4218740	08-19-1980	MOTOROLA INC	
/M.S/	2.	4249253	02-03-1981	Gentili et al.	
/M.S/	3.	4368515	01-11-1983	Nielsen	
/M.S/	4.	4392212	07-05-1983	Miyasaka et al.	
/M.S/	5.	4571676	02-18-1986	Mantellina et al.	
/M.S/	6.	4592011	05-27-1986	Mantellina et al.	
/M.S/	7.	4633429	12-30-1986	Lewandowski et al.	
/M.S/	8.	4670748	06-02-1987	Williams	
/M.S/	9.	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
/M.S/	10.	4866603	09-02-1989	Chiba	
/M.S/	11.	4958322	09-18-1990	Kosugi et al.	
/M.S/	12.	4961172	10-02-1990	Shubat et al.	
/M.S/	13.	4961204	10-02-1990	Hitachi Ltd	
/M.S/	14.	4980850	12-25-1990	Morgan	
/M.S/	15.	5060188	10-22-1991	Zulian et al.	
/M.S/	16.	5247643	09-21-1993	Shottan	
/M.S/	17.	5272664	12-21-1993	Silicon Graphics	
/M.S/	18.	5345412	09-06-1994	Shiratsuchi	
/M.S/	19.	5357478	10-18-1994	Mitsubishi Electric Corp	
/M.S/	20.	5388072	02-07-1995	IBM	
/M.S/	21.	5388240	02-01-1995	IBM Corporation	
/M.S/	22.	5392252	02-21-1995	Visi Technology	
/M.S/	23.	5426753	06-20-1995	Moon	
/M.S/	24.	5463590	10-31-1995	Watanabe	
/M.S/	25.	5483497	01-09-1996	Mochizuki et al.	
/M.S/	26.	5485589	01-16-1996	Dell Usa Lp	
/M.S/	27.	5495435	02-27-1996	Sugahara	
/M.S/	28.	5513135	04-30-1996	Dell et al.	
/M.S/	29.	5532954	07-02-1996	Bechtolsheim et al.	
/M.S/	30.	5541448	07-30-1996	Carpenter	
/M.S/	31.	5572691	11-05-1996	Koudmani	
/M.S/	32.	5581498	12-03-1996	Ludwig et al.	
/M.S/	33.	5590071	12-31-1996	Kolor et al.	

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Sheet | 2 of | 18

Complete if Known	
Application Number	15/820,076
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First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S/	34.	5602999	02-11-1997	Hyatt; Gilbert P.	
/M.S/	35.	5638534	06-10-1997	Samsung Electronics	
/M.S/	36.	5655153	08-05-1997	EMC CORP	
/M.S/	37.	5699542	12-16-1997	Mehta et al.	
/M.S/	38.	5702984	12-30-1997	Bertin et al.	
/M.S/	39.	5703826	12-30-1997	Hush et al.	
/M.S/	40.	5745914	04-28-1998	Connolly et al.	
/M.S/	41.	5764590	06-09-1998	Mitsubishi Electric Corp	
/M.S/	42.	5784705	07-21-1998	Leung, Wingyu	
/M.S/	43.	5784705	07-21-1998	Jr Albert Pesak	
/M.S/	44.	5802395	09-01-1998	Connolly et al.	
/M.S/	45.	5805520	09-08-1998	Anglada et al.	
/M.S/	46.	5822251	10-13-1998	Bruce et al.	
/M.S/	47.	5909388	06-01-1999	Siemens Ag	
/M.S/	48.	5926827	07-20-1999	Dell et al.	
/M.S/	49.	5926839	07-20-1999	IBM	
/M.S/	50.	5953215	09-14-1999	Karabatsos, Chris	
/M.S/	51.	5953280	09-14-1999	Matsui	
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/M.S/	53.	5959930	09-28-1999	Sakurai	
/M.S/	54.	5963464	10-05-1999	Dell et al.	
/M.S/	55.	5966736	10-12-1999	Gittinger et al.	
/M.S/	56.	5974493	10-26-1999	Mitsubishi Electric Corp	
/M.S/	57.	6011710	01-04-2000	Wiggers	
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/M.S/	59.	6044032	03-28-2000	Li	
/M.S/	60.	6070217	05-30-2000	Connolly et al.	
/M.S/	61.	6070227	05-30-2000	Rokicki	
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/M.S/	63.	6108745	08-22-2000	Gupta et al.	
/M.S/	64.	6115278	09-05-2000	Deneroff et al.	
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/M.S/	66.	6151271	11-21-2000	Lee	

EXAMINER /MICHAEL SUN/ **DATE CONSIDERED** 10/15/2018

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Application Number	15/820,076
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First Named Inventor	Hyun Lee
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Examiner Name	SUN, Michael
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/M.S/	67.	6154418	11-28-2000	Li	
/M.S/	68.	6154419	11-28-2000	Shakkarwar	
/M.S/	69.	6185654	02-06-2001	Van Doren	
/M.S/	70.	6188641	02-13-2001	Uchida	
/M.S/	71.	6205516	03-20-2001	Usami	
/M.S/	72.	6209074	03-01-2001	Dell et al.	
/M.S/	73.	6226709	05-01-2001	Goodwin et al.	
/M.S/	74.	6226736	05-01-2001	Niot	
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/M.S/	76.	6247088	06-12-2001	Seo et al.	
/M.S/	77.	6317352	11-13-2001	Halbert et al.	
/M.S/	78.	6349051	02-19-2002	Micron Technology Inc	
/M.S/	79.	6400637	06-18-2002	Akamatsu et al.	
/M.S/	80.	6408356	06-18-2002	Dell	
/M.S/	81.	6414868	07-02-2002	Wong et al.	
/M.S/	82.	6415374	07-02-2002	Faue et al.	
/M.S/	83.	6438062	08-20-2002	Karabatsos (Curtis)	
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/M.S/	92.	6526473	02-25-2003	Kim	
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/M.S/	95.	6553450	04-22-2003	Dodd et al.	
/M.S/	96.	6618320	09-09-2003	Hasegawa et al.	
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/M.S/	98.	6625081	09-23-2003	Roohparvar et al.	
/M.S/	99.	6625687	09-23-2003	Halbert et al.	
/M.S/	100	6636935	10-21-2003	Ware et al.	
/M.S/	101	6646949	11-11-2003	Ellis et al.	

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First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

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/M.S/	102	6658509	12-02-2003	Bonella et al.	
/M.S/	103	6674684	01-06-2004	Shen	
/M.S/	104	6681301	01-20-2004	Mehta et al.	
/M.S/	105	6683372	01-27-2004	Wong et al.	
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/M.S/	107	6705877	03-16-2004	Li et al.	
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/M.S/	111	6738880	05-18-2004	Lai et al.	
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/M.S/	113	6754797	06-22-2004	Wu et al.	
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/M.S/	115	6788592	09-07-2004	Nakata et al.	
/M.S/	116	6807125	10-19-2004	Coteus et al.	
/M.S/	117	6807650	10-19-2004	Lamb et al.	
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/M.S/	121	6834014	12-21-2004	Yoo et al.	
/M.S/	122	6854042	02-08-2005	Karabatsos	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

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Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

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First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
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US PATENT APPLICATIONS

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T'
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First Named Inventor	Hyun Lee
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Examiner Name	SUN, Michael
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/M.S/	249.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
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/M.S/	252.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
/M.S/	253.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
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Art Unit	2184
Examiner Name	SUN, Michael
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				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
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	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016
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Examiner's Signature	/MICHAEL SUN/	Date Considered	10/15/2018

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	17	of	18	Attorney Docket Number	*129980-5049-US*

/M.S/	68.	Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016
/M.S/	69.	Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015
/M.S/	70.	Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016
	71.	Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015
	72.	Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	73.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015
	74.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3,2015
	75.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	76.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015
	77.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	78.	Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	79.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015
	80.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
	81.	Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015
	82.	Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015
	83.	Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002
	84.	Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10
	85.	U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages
	86.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411
	87.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265
	88.	Selected Entries in Oxford English Dictionary, Oxford University Press 2014,http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid
	89.	Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select& searchBin=Search
	90.	Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015

Examiner's Signature	/MICHAEL SUN/	Date Considered	10/15/2018

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 3, 2018*	
				Application Number	*15/820,076*
				Filing Date	*November 21, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2184*
				Examiner Name	*SUN, Michael*
Sheet	18	of	18	Attorney Docket Number	*129980-5049-US*

	91.	Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	92.	Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015
	93.	Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	94.	Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	95.	Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
	96.	Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	97.	Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	98.	Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
	99.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
	100.	Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015
	101.	Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	102.	Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
	103.	Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	104.	Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	105.	Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015
	106.	Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	107.	Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	108.	Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
	109.	Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015

Examiner's Signature	/MICHAEL SUN/	Date Considered	10/15/2018

Electronically filed February 19, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	8866
Serial No.:	15/820,076	Art Unit:	2184
Filed:	November 21, 2017	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS*	Attorney Docket No.:	129980-5049-US

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The enclosed Amendment is filed after a Notice of Allowance dated November 19, 2018, and is filed under 37 C.F.R. § 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

1. (Currently Amended) A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

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Ex. 1002, p. 266

2. (Previously Presented) The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.

3. (Previously Presented) The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.

4. (Previously Presented) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

5. (Previously Presented) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

6. (Previously Presented) The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

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Ex. 1002, p. 267

7. (Previously Presented) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

8. (Previously Presented) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

9. (Previously Presented) The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

10. (Currently Amended) The memory module of claim 9, wherein the each respective buffer circuit includes ~~data paths include~~ a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

11. (Previously Presented) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

12. (Previously Presented) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

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REMARKS

Claims 1 and 10 have been amended to address antecedent basis issues. Entry of the amendments is respectfully requested under 37 C.F.R. § 1.312. No new matter has been added.

The Commissioner is hereby authorized to charge any additional fees associated with this paper communication or credit any overpayment to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

Respectfully submitted,

Date: February 19, 2019

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Samsung Electronics Co., Ltd.
Ex. 1002, p. 269

Electronic Patent Application Fee Transmittal

Application Number:	15820076
Filing Date:	21-Nov-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5049US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	35194107
Application Number:	15820076
International Application Number:	
Confirmation Number:	8866
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049US
Receipt Date:	19-FEB-2019
Filing Date:	21-NOV-2017
Time Stamp:	20:22:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	022019INTEFSW00007252500310
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	129980_5049US_Issue_Fee.pdf	112611 760114880aa5d3c7e32ad335baa4bec7ac4f8bcc	no	1
Warnings:					
Information:					
2		129980_5049US_AMEND.pdf	116575 e7a7e161b4605054252eef864c5c4e09336d65f9	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30507 89c18ece49754f540c985015c4073dc93f73474a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	259693		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Electronically filed February 19, 2019

Complete and send this form with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advanced orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing below can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049-US	8866

TITLE OF INVENTION **MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	02/19/2019

EXAMINER	ART UNIT	CLASS-SUB CLASS
SUN, MICHAEL	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed

1. **Morgan, Lewis & Bockius LLP**
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY) Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☐ Advanced Order - # of Copies ____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above.**)

☐ A check in the amount of the fee(s) enclosed

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0310 (order no. 129980-5049-US).

5. **Change in Small Entity Status** (from status indicated above)

☐ a. Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature / Jamie J. Zheng/ Date: February 19, 2019

Printed Name: Jamie J. Zheng Registration No. 51,167

UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	11/21/2017	Hyun Lee	129980-5049US	8866

79141 7590 02/28/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
02/28/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 276

Response to Rule 312 Communication	Application No.	Applicant(s)	
	15/820,076	Lee et al.	
	Examiner	Art Unit	AIA Status
	MICHAEL SUN	2184	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 19 February 2019 under 37 CFR 1.312 has been considered, and has been:

a) ☑ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Electronically filed February 19, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	8866
Serial No.:	15/820,076	Art Unit:	2184
Filed:	November 21, 2017	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS*	Attorney Docket No.:	129980-5049-US

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The enclosed Amendment is filed after a Notice of Allowance dated November 19, 2018, and is filed under 37 C.F.R. § 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

OK TO ENTER: /M.S/ 02/22/2019

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. 0MB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid 0MB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | 5 | of | 18

Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

Change(s) applied to document, /G.D./ 3/8/2019

US PATENT DOCUMENTS					
Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S/	138	7007175	02-28-2006	Chang et al.	
/M.S/	139	7046538	05-16-2006	Kinsley et al.	
/M.S/	140	7047361	05-16-2006	~~Phison Electronic~~ Chong, et al.	
/M.S/	141	7054179	05-30-2006	Cogdill et al.	
/M.S/	142	7065626	06-20-2006	Schumacher et	
/M.S/	143	7072231	07-04-2006	Pax	
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/M.S/	157	7200021	04-03-2007	Raghuram	
/M.S/	158	7227910	06-05-2007	Lipka	
/M.S/	159	7266639	09-04-2007	Raghuram	
/M.S/	160	7272709	09-18-2007	Zitlaw et al.	
/M.S/	161	7281079	10-09-2007	Bains et al.	
/M.S/	162	7286436	10-23-2007	Bhakta et al.	
/M.S/	163	7289386	10-30-2007	Bhakta et al.	
/M.S/	164	7346750	03-18-2008	Ishikawa	
/M.S/	165	7356639	04-08-2008	Perego et al.	
/M.S/	166	7370238	05-06-2008	Billick et al.	
/M.S/	167	7437591	10-14-2008	Wong	
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Sheet | 4 of | 18

Complete if Known	
Application Number	15/820,076
Filing Date	November 21, 2017
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures
/M.S/	102	6658509	12-02-2003	Bonella et al.	
/M.S/	103	6674684	01-06-2004	Shen	
/M.S/	104	6681301	01-20-2004	Mehta et al.	
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/M.S/	108	6717885	04-06-2004	Lai	
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3/8/2019

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Sheet | 3 of | 18

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First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	129980-5049US

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/M.S/	35.	5638534	06-10-1997	~~Samsung Electronics~~	Mote, Jr.
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/M.S/	1.	4218740	08-19-1980	~~MOTOROLA INC~~	Bennett, et al.
/M.S/	2.	4249253	02-03-1981	Gentili et al.	
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/820,076	04/23/2019	10268608	129980-5049US	8866

79141 7590 04/03/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Netlist, Inc., Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. ƒ 290 and/or 15 U.S.C. ƒ 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. ƒ 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:21-cv-00431	4/28/2021	Western District of Texas

PLAINTIFF	DEFENDANT
Netlist, Inc.	Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,489,314	11/26/2019	Netlist, Inc.
2	9,824,035	11/21/2017	Netlist, Inc.
3	10,268,608	4/23/2019	Netlist, Inc.
4			
5			

In the above´ entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1			
2			
3			
4			
5			

In the above´ entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1´ Upon initiation of action, mail this copy to Director Copy 3´ Upon termination of action, mail this copy to Director
Copy 2´ Upon filing document adding patent(s), mail this copy to Director Copy 4´ Case file copy

Trials@uspto.gov
571-272-7822

Paper 15
Entered: July 19, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00237
Patent 10,268,608 B2

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–5 ("the challenged claims") of U.S. Patent No. 10,268,608 B2 ("the '608 patent," Ex. 1001). The Petition challenges the patentability of claims 1–5 of the '608 patent. Netlist, Inc. ("Patent Owner") timely filed a Preliminary Response (Paper 12, "Prelim. Resp.").

An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on any of the challenged claims of the '608 patent. Accordingly, we do not institute an *inter partes* review as to the challenged claims of the '608 patent.

B. Related Proceedings

The parties identify the following matter as related to this case: *Netlist, Inc. v. Micron Technology, Inc., et al.*, Case No. 6:21-cv-00431-ADA (W.D. Tex.). Pet. 70; Paper 6, 1. Patent Owner states that matter was subsequently "transferred from the U.S. District Court for the Western District of Texas, Waco Division to the U.S. District Court for the Western District of Texas, Austin Division and docketed as" *Netlist, Inc. v. Micron Technology, Inc., et al.*, 1:22-cv-00136-LY (W.D. Tex.). Paper 6, 1.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 287

Petitioner also identifies IPR2022-00236 as involving the parent of the '608 patent. Pet. 70. Petitioner further identifies IPR2017-00730 as involving a patent related to the '608 patent. *Id.*

C. The '608 Patent (Ex. 1001)

The '608 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 2:43–45, 4:65–66.

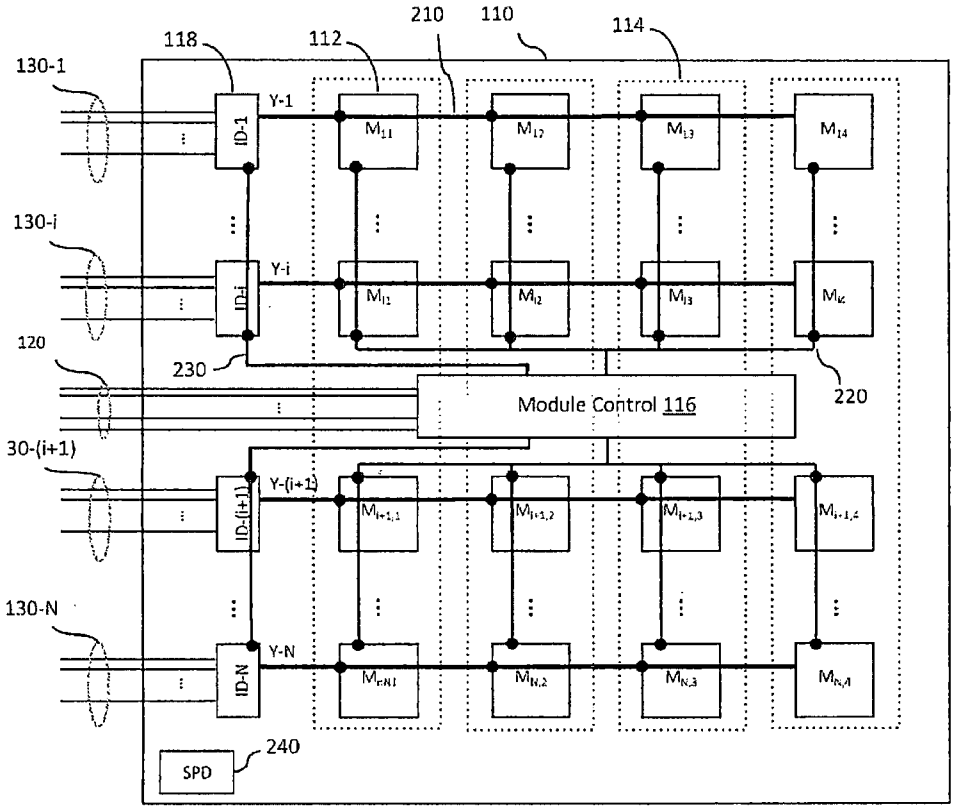

FIG. 2A

As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:65–66, 6:4–5. Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller

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(MCH) (not shown). *Id.* at 4:20–23, 4:67–5:4. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, e.g., group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:23–25; *see id.* at 6:20–25. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. For example, as shown along the top of memory module 110, isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)." Ex. 1001, 3:29–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:32–34, 4:66–5:3. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:63–65. And, "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the '608 patent explains, there are "unbalanced" lengths of control wires to respective memory devices which causes a "variation of the timing" of signals due to the variation in wire length. *See* Ex. 1001, 2:20–31; *see also id.* at 8:22–55. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "providing the correct control signal

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timing." *Id.* at 8:56–9:3. In particular, "isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation." *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to "properly time transmission" of a later read operation. *Id.* at 15:45–50.

D. Illustrative Claims

Claim 1, the sole independent claim of the '608 patent, is reproduced below with limitation identifiers in brackets corresponding to corresponding claim analysis headings in the Petition. *See* Pet. 20–41.

> 1. [a] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> [b] a module board having edge connections for coupling to respective signal lines in the memory bus;
>
> [c] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
>
> [d] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, [e] the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

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> [f] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, [g] coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, [h] the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and [i] a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and [j] a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ex. 1001, 19:14–55.

E. Evidence

The Petition relies on the following references:

Reference	**Exhibit No.**
US 2010/0312925A1; filed June 3, 2010; published Dec. 9, 2010 ("Osanai").	1005
US 8,020,022B2; filed Sept. 12, 2008; issued Sept. 13, 2011 ("Tokuhiro").	1006
US 8,713,379B2; filed Nov. 22, 2011; issued Apr. 29, 2014 ("Takefman")	1007

Petitioner also relies on the Declaration of Donald Alpert, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

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F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–5 would have been unpatentable on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 4	102[1]	Osanai
2	1–5	103(a)	Osanai, Tokuhiro
3	1–5	103(a)	Osanai, Tokuhiro, Takefman

II. ANALYSIS

A. Principles of Law

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Because the '608 patent claims priority before this date, the pre-AIA version of §§ 102 and 103 applies.

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1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368–69 (Fed. Cir. 2003) ("'[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." (second and third alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

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B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation marks and citation omitted).

Petitioner's declarant, Dr. Alpert, opines that:

> a person of ordinary skill in the art in the field of the Challenged Patent would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers . . . an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

Ex. 1003 ¶ 42; *see* Pet. 5.

Patent Owner states that it "disputes Petitioners' definition of the level of a person of ordinary skill in the art," but does not present arguments in support of its assertion at this stage in the proceeding. Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill, except that we find that the phrase "at least" in Petitioner's proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in

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electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and three years working in the field.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner proposes we "use Patent Owner's proposed constructions" from the related proceedings. Pet. 12; *see* Ex. 1019.

Patent Owner states that it "does not propose that the Board construe any claims." Prelim. Resp. 12.

We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

D. Anticipation by Osanai (Ground 1)

Petitioner argues claims 1 and 4 of the '608 patent are anticipated by Osanai. Pet. 20–45. Below we provide a brief overview of the prior art

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references and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Osanai (Ex. 1005)

Osanai relates to a memory module having memory chips and data register buffers arranged in a manner which shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is a schematic diagram of a configuration of a memory module." *Id.* ¶ 20.

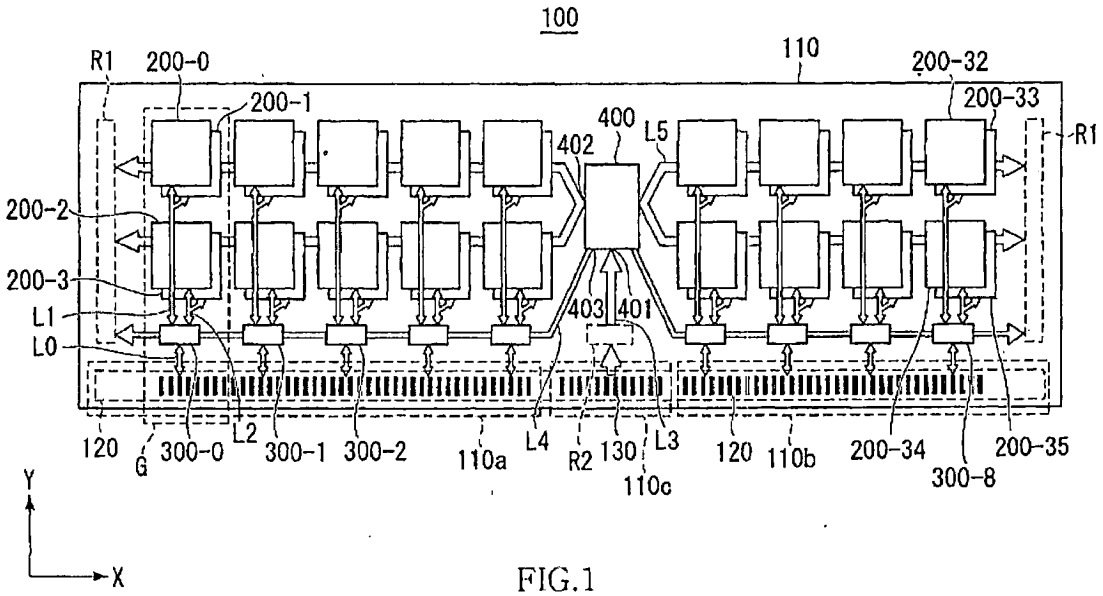

FIG.1

As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. *Id.* ¶ 51. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 52. Still further, memory module 100 includes "data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" ellectrically connected to the connectors. *Id.* ¶¶ 53–54 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connectors

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120 and the memory chips 200." *Id.* ¶ 109. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 26.

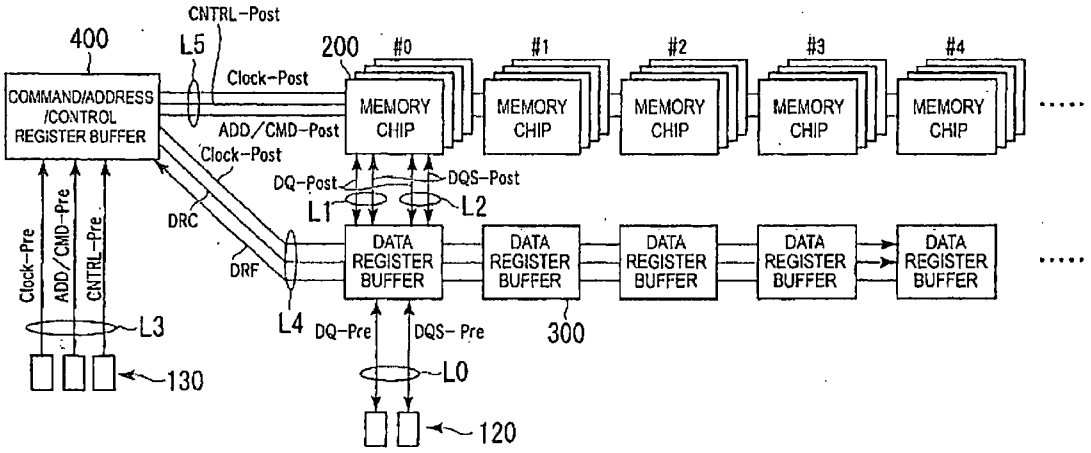

FIG.7

As shown in Figure 7, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 109. "[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post." Ex. 1005 ¶ 110. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Osanai "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 146. The write leveling and read leveling operations are provided via write leveling and

read leveling circuits in the data register buffer, as shown in Figure 5, which is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 89.

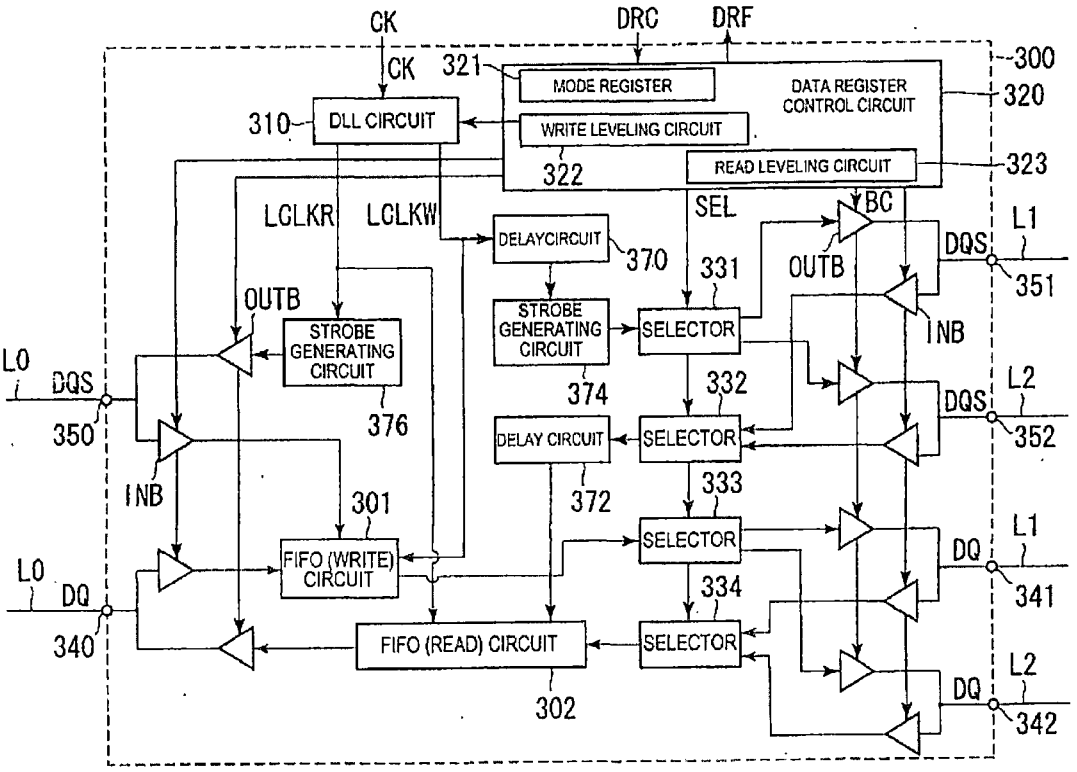

FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 151, 153. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a signal." *Id.* For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 149. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 151.

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An exemplary read leveling operation also adjusts signal timing for a read operation. *See* Ex. 1005 ¶¶ 153–157. For example,

> read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 157.

2. Analysis of Claim 1

a) Preamble and Undisputed Limitations 1[a]–1[i]

Petitioner provides detailed analysis demonstrating that Osanai discloses the preamble and limitations 1[b]–1[i]. Pet. 20–33. Petitioner supports its arguments with citations to Osanai and to the testimony of Dr. Alpert. *Id.* Patent Owner does not separately dispute Petitioner's contentions regarding the preamble and these limitations. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Osanai teaches the preamble and limitations 1[b]–1[i] for the reasons provided by Petitioner.

For example, for the preamble, Petitioner identifies Osanai's memory module 100 as the recited "memory module" and the memory control hub 12 as the recited "memory controller." Pet. 20 (citing Ex. 1005 ¶¶ 69–71). Petitioner argues that memory module 100 and control hub 12 communicate using line 23, which the Petitioner identifies as the recited "memory bus." *Id.* at 21–23 (citing Ex. 1005 ¶¶ 54–55, 75, Figs. 1, 3; Ex. 1003 ¶¶ 76–78). Petitioner argues that line 23 connects signal lines L0 and L3, which are the

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recited "data/strobe signal lines" and "control/address signal lines," respectively. *Id.* at 24 (citing Ex. 1005 ¶¶ 54–55, 75; Ex. 1003 ¶ 80).

For limitation 1[b], Petitioner argues that Osanai's memory module 100 includes data connectors 120 and 130 which, together, disclose the recited "module board having edge connections." Pet. 24–25 (citing Ex. 1005 ¶ 54, Fig. 1; Ex. 1003 ¶ 83).

For limitation 1[c], Petitioner identifies command/address/control register buffer 400 as the recited "module control device mounted on the module board." Pet. 25–26 (citing Ex. 1005 ¶¶ 66, 101–103). Petitioner argues that Osanai's memory controller 12 sends command/address/control signals (the recited "system command signals") to register buffer 400 and in response the register buffer 400 outputs "module command signals" and "module control signals," such as ADD, CMD, CTRL, and CK signals as well as control signal DRC. *Id.* at 26 (citing Ex. 1005 ¶¶ 53, 102; Ex. 1003 ¶ 87). Petitioner further argues Osanai's register buffer 400 receives Clock-Pre Signal and outputs Clock-Post signal, which Petitioner argues are the recited "system clock signal" and "module clock signal" respectively. *Id.* at 28 (citing Ex. 1005 ¶ 114, Fig. 6–7; Ex. 1003 ¶¶ 89–90).

For limitation 1[d] Petitioner identifies Osanai's memory chips 200 as the recited "memory devices" and argues that they perform memory operations, such as read and write operations, as instructed by receiving CNTRL-Post signals and Clock-post signals, which Petitioner identifies as the recited "module command signals" and "clock signals" respectively. Pet. 29–30 (Ex. 1005 ¶¶ 60, 101–114, Figs. 6, 7; Ex. 1003 ¶ 93).

For limitation 1[e] Petitioner argues Osanai's memory chips 200 are grouped into sets making "a plurality of sets of memory devices," and each

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group has its own respective set of data/strobe signal lines. Pet. 30–31 (citing Ex. 1003 ¶¶ 96–97; Ex. 1005 ¶¶ 58, 109, Figs. 5, 7).

For limitation 1[f] Petitioner identifies Osanai's data register buffers 300 mounted on memory module 100 as the recited "plurality of buffer circuits" and argues that the register buffers 300 are each paired with a set of the memory chips and L0 data lines. Pet. 31–33 (citing Ex. 1003 ¶¶ 100–101; Ex. 1005 ¶¶ 52, 61–62, 109, Figs. 1, 7).

For limitation 1[g] Petitioner argues that each data register buffer ("buffer circuit") is mounted on the module between L0 data lines ("data/strobe signal lines") and its respective memory chip group ("set of memory devices"). Pet. 33–34 (citing Ex. 1005 ¶ 109, Figs. 1, 7). Petitioner further argues that Osanai's command/address/control register buffer 400 ("module control device") outputs Clock-Post signal ("module clock signal") and DRC ("module control signals") to the buffer circuits 300. *Id.* at 34–35 (citing Ex. 1005 ¶¶ 93, 104, 112–114, 154, 157, 164, Figs. 6–7; Ex. 1003 ¶ 107).

For limitation 1[h] Petitioner argues that each data register buffer 300 has data paths that correspond to each data signal line L1 and L2, connected to each memory chip group. Pet. 36 (citing Ex. 1005 ¶ 109, Fig. 7). Petitioner argues that these data paths include circuitry components in the data register buffer 300 that connect each L0 data lines ("respective set of data/strobe signal lines"). *Id.* at 36–38 (citing Ex. 1003 ¶¶ 110–112; Ex. 1005 ¶ 109, Figs. 1, 5, 7).

For limitation 1[i] Petitioner identifies the data register control circuit 320 and DLL circuit 310 in the data register buffer 300 as the recited "command processing circuit" and argues that this circuitry uses the received DRC signals and clock signals to select the appropriate data path

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("to control the data path in accordance with the module control signals and the module clock signal"). Pet. 38–40 (citing Ex. 1005, ¶¶ 94, 96, 97, 105, 132, 158, 163, Figs. 2, 5; Ex. 1003 ¶ 115). Petitioner further argues that any data path selected by Osanai's data register control circuit 320 includes a "tristate buffer" such as Osanai's OUTB buffers. *Id.* at 40–41 (citing Ex. 1005 ¶¶ 90–94, 97–98, 105–106, 129–136, Figs. 5, 11; Ex. 1003 ¶ 116).

b) Disputed limitation 1[j]

Petitioner argues that Osanai's control circuit 320 includes read leveling and write leveling circuits 322 and 323 and Dr. Alpert testifies that these circuits compensate for propagation delays caused by some memory chips being placed farther away from their respective data register buffers. Pet. 41–42 (citing Ex. 1005 ¶ 146, Fig. 5; Ex. 1003 ¶¶ 120–121). Petitioner argues that the write leveling circuitry 322 delays the output timing of the DQS sent from the data register buffer 300, thus creating DQS-Post and that the read leveling circuitry similarly delays signals. Pet. 43 (citing Ex. 1005 ¶¶ 151–157; Ex. 1003 ¶ 123). Petitioner argues that these delays were "in response to at least one of the module control signals" because the delays depend on whether the DRC mode represents a read operation or write operation and alternatively because read and write leveling circuitry uses the module clock signal. *Id.* at 44 (citing Ex. 1005 ¶¶ 94, 132, 154–157, 164, Fig. 7; Ex. 1003 ¶ 124).

Patent Owner argues that Petitioner fails to clearly identify any claimed delay circuit configured to delay a signal, arguing that although Petitioner makes remarks regarding Osanai's write leveling circuit and read leveling circuit, Petitioner never expressly identifies either as the recited "delay circuit." Prelim. Resp. 15. Patent Owner further argues that Petitioner fails to identify any data path that includes Osanai's write leveling

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circuitry 322. *Id.* at 16. Patent Owner further argues that Petitioner does not identify a signal that is delayed through the recited data path. *Id.* at 17–19. Specifically, Patent Owner argues that Osanai's write leveling circuit 322 performs any delay before the DQS signals, which Petitioner relies on as the recited delayed signal, are even generated. *Id.* at 19. Patent Owner argues that "a signal cannot be '*delay[ed]*' as claimed unless it exists." *Id.* (alteration in original).

We do not agree with Petitioner's contentions. Specifically, we agree with Patent Owner that Petitioner has not identified a data path that includes Osanai's write leveling circuit 322. Claim 1 recites "wherein the data path . . . includes at least one tristate buffer . . . and a delay circuit configured to delay a signal through the data path." Thus, claim 1 requires that the data path include two elements: (1) at least one tristate buffer and (2) a delay circuit. We first examine Petitioner's contentions with respect to the "data path" limitation and then analyze whether Petitioner has sufficiently identified a delay circuit that is included in the aforementioned data path.

With respect to the "data path," Petitioner argues that "each data register buffer 300 has '*data paths*' that correspond to each data signal line, L1 and L2 data lines, connected to each memory chip group." Pet. 36 (citing Ex. 1005 ¶ 109, Fig. 7). Petitioner argues that "these data paths include circuitry components in the data register buffer 300 that connect each L0 data lines ('*respective set of data/strobe signal lines*') at terminals 340 and 350." Pet. 36–38 (citing Ex. 1003 ¶¶ 110–112; Ex. 1005 ¶ 109, Figs. 1, 5, 7). Initially, we note, that while Petitioner states that data register buffer 300 has data path<u>s</u>, Petitioner does not, even by way of example, identify any single one of those data paths as disclosing the recited "data path." Moreover, Petitioner does not specifically identify which circuitry

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components of data register buffer 300 are included in any one of the data paths cited by Petitioner.

With respect to the "delay circuit" Petitioner identifies Osanai's write level circuitry 322 and read leveling circuitry 323[2] and argues that the write level circuitry 322 delays the output timing of the DQS sent from the data register buffer 300, thus creating DQS-Post and that the read leveling circuitry similarly delays signals. Pet. 43 (citing Ex. 1005 ¶¶ 151–157; Ex. 1003 ¶ 123). Petitioner does not, however, state, or otherwise make a showing, that the write and read leveling circuitry are included in any one of the data paths that are relied upon by Petitioner. Nor does Petitioner show how these circuits would be included in the recited data path.

In contrast, with respect to the "tristate buffer," Petitioner explicitly states that "[a]ny data path selected by Osanai's data register control circuit 320 includes a 'tristate buffer'" and identifies Osanai's OUTB buffers as disclosing these tristate buffers. Pet. 40 (citing Ex. 1005 ¶ 94, Fig. 5; 1003 ¶ 116). Petitioner, however, does not make a similar statement regarding the delay circuit being included in the data path. Instead Petitioner contends that the "buffer circuits 300 include 'a delay circuit . . . .' *Id.* at 41. The claim, however, requires more than just the buffer circuit include the delay circuit. The claim requires the *data path* include the delay circuit. Based on our

[2] Patent Owner argues that Petitioner does not clearly and expressly identify any claimed delay circuit configured to delay a signal. Prelim. Resp. 15. We determine, however, that Petitioner relies on Osanai's write leveling circuitry 322 and read leveling circuitry 323 as disclosing the recited "delay circuit." *See* Pet. 43 (stating that the write and read leveling circuitry as the components that "delay a signal through the data path by an amount determined by the command processing circuit.")

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review of Petitioner's contentions it appears Petitioner does not demonstrate this to be the case.

3. Conclusion – Anticipation by Osanai (Ground 1)

Accordingly, having considered the arguments and evidence, we are not persuaded that Petitioner has demonstrated a reasonable likelihood that Osanai anticipates claim 1, or claim 4, which depends from claim 1.

E. Obviousness over Osanai and Tokuhiro (Ground 2) and Obviousness over Osanai, Tokuhiro, and Takefman (Ground 3)

Petitioner argues claims 1–5 of the '608 patent would have been obvious over Osanai and Tokuhiro (Pet. 45–61) and over Osanai, Tokuhiro, and Takefman (Pet. 62–65). Petitioner relies on Tokuhiro for independent claim 1 as disclosing "delay[ing] a signal through the data path by an amount determined . . . in response to . . . control signals." *Id.* at 45–52. Petitioner relies on Takefman as disclosing the recited "tristate buffer." *Id.* at 62–65. Petitioner's contentions regarding Tokuhiro or Takefman do not address or remedy the deficiencies discussed above with respect to Ground 1.[3] Specifically, Petitioner does not rely on Tokuhiro or Takefman as disclosing that the delay circuit is included in the recited data path, as required by claim 1.

Claims 2–5 depend from claim 1. Accordingly, having considered the arguments and evidence, we are not persuaded that Petitioner has

[3] As with Ground 1, Petitioner recognizes in Ground 3 that claim 1 requires the recited "tristate buffer" to be included in the recited "data path" and, accordingly, provides reasoning why Takefman's tristate buffer would have been incorporated into Osanai's data paths. *See* Pet. 62–63. Petitioner does not recognize, or at least does not address, that claim 1 also requires the same of the recited "delay circuit" and thus does not address whether the relied upon references teach a delay circuit that is included in the recited data path.

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demonstrated a reasonable likelihood that claims 1–5 would have been obvious over Osanai and Tokuhiro or would have been obvious over Osanai, Tokuhiro, and Takefman.

III. CONCLUSION

Petitioner has not demonstrated a reasonable likelihood of prevailing in showing the unpatentability of the challenged claims of the '608 patent.

IV. ORDER

For the foregoing reasons, it is

ORDERED that the Petition is *denied*, and no trial is instituted.

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