(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 August 2002 (15.08.2002)

PCT

(10) International Publication Number
WO 02/063804 A2

(51) International Patent Classification[7]: H04J 3/00

(21) International Application Number: PCT/US01/49772

(22) International Filing Date:
21 December 2001 (21.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/750,735 28 December 2000 (28.12.2000) US

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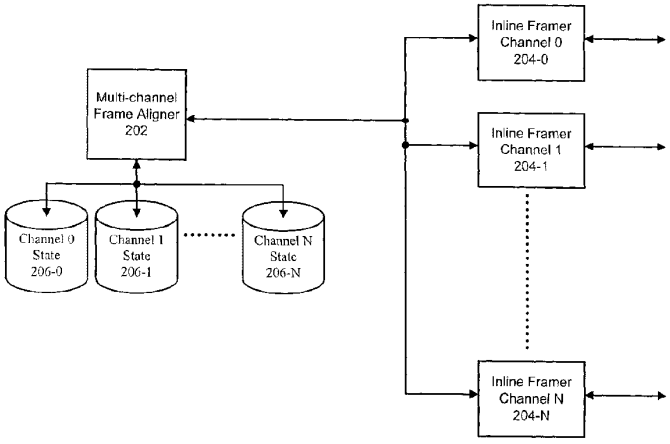
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN (utility model), CO, CR, CU, CZ, DE (utility model), DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP (utility model), KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: SCALABLE MULTI-CHANNEL FRAME ALIGNER



(57) Abstract: An offline frame alignment circuit can simultaneously achieve frame alignment for a large number of TDM streams (i.e. channels) within a required amount of time (e.g. 15 ms for ESF). The Multi-channel Frame Aligner (MCFA) uses a high speed system clock independent of the individual line clocks to perform frame alignment for each of the channels. The MCFA includes a framer memory to store the alignment states of all possible framing bit candidates for all channels. The MCFA polls each channel to determine if frame alignment is requested, and if so, if data from the associated channel is available. A state machine in the MCFA compares the received data with the expected framing bits and adjusts the stored alignment states accordingly. All framing bit candidates are processed in parallel leading to fast alignment times. The MCFA architecture can be adapted for any of a plurality of channels and framing formats merely by adjusting the speed of the MCFA system clock and capacity and arrangement of data states in the framer memory.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SCALABLE MULTI-CHANNEL FRAME ALIGNER

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FIELD OF THE INVENTION

This invention relates generally to frame alignment in a digital communications system, and more particularly, to a method and apparatus for performing frame alignment for a scalable plurality of communications channels.

BACKGROUND OF THE INVENTION

The demand for telecommunications services continues to grow. With this growing demand for services comes the need for increased capacity, and telecommunications companies are scrambling to keep up. One way to handle increased capacity is to multiplex a plurality of communications channels onto higher-bandwidth channels. Thus, by adding a single high-bandwidth channel, many individual communications channels can be added and services can be increased dramatically.

FIG. 1 is a block diagram illustrating a conventional communications system. As shown in FIG. 1, for transmission over a high-capacity transmission media 102 such as a fiber optic cable or trunk line (and generally over long distances), transmit side 104 includes components for multiplexing multiple DS0 channels (each capable of carrying a separate PSTN voice call, for example). As shown in this example, multiple DS0 channels are multiplexed onto a DS1 channel by channel banks 106, and multiple DS1 channels can be further multiplexed onto higher order channels (e.g. DS3 and higher) by mutliplexers 108 for transmission over the media. Where necessary, further conversion and processing may be performed for different types of media (e.g. conversion to optical media and formats such as OC-3 to OC-192). Receive side 110 includes components 112, 114 for demultiplexing the received higher order channels onto DS1 channels and then further into DS0 channels, respectively.

Generally, time division multiplexing (TDM) techniques are used to multiplex the multiple DS0 channels onto higher order channels such as DS1. In a time division multiplexed scheme, each DS1 bit stream is serially transmitted in frames, with each frame containing a plurality of bits for each DS0 channel. Frame synchronization or frame

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alignment is the process that forces the transmitter and receiver to agree on the timing between the two systems, and thus allows the receiver to de-multiplex the individual DS0 channels from the received DS1 bit stream. Framing is performed on the transmit side by inserting one or more framing bits into the bit stream at predetermined intervals. A typical example is found in the North American 24 channel DS1 extended superframe format (ESF). In DS1 ESF framing, one frame bit is inserted for every 192 data bits (i.e. 8 bits x 24 DS0 channels) at a frame rate of 8 kHz. A predetermined sequence of a frame bit pattern is transmitted at some or all of the Frame Bit positions. In the receiver, a frame alignment circuit detects this frame bit sequence and uses the frame alignment to recover the data bits for the individual DS0 channels from the data stream.

According to ANSI T.107 (Digital Hierarchy- Formats and Specifications) Standards, an extended DS1 framing format (ESF) is defined in which the frame bits are used for cyclic redundancy check bits and a maintenance channel, as well as for frame synchronization. In the extended framing format, the framing bits containing the framing pattern sequence (FPS) are sent only once in every fourth frame, every 772 bits. Six successive framing bits forming the FPS (e.g. the sequence 001011) are thus transmitted over 24 frames called superframes. The superframe interval repeats every 3 milliseconds.

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The framing bits and their positions in the superframe are shown in Table 1.

Frame No.	Bit No.	FPS	CRC	FDL
1	0	-	-	M1
2	193	-	C1	-
3	386	-	-	M2
4	579	0	-	-
5	772	-	-	M3
6	965	-	C2	-
7	1158	-	-	M4
8	1351	0	-	-
9	1544	-	-	M5
10	1737	-	C3	-
11	1930	-	-	M6
12	2123	1	-	-
13	2316	-	-	M7
14	2509	-	C4	-
15	2702	-	-	M8
16	2895	0	-	-
17	3088	-	-	M9
18	3281	-	C5	-
19	3474	-	-	M10
20	3667	1	-	-
21	3860	-	-	M11
22	4053	-	C6	-
23	4246	-	-	M12
24	4439	1	-	-

Table 1. DS1 Extended Superframe Format.

FPS - Frame Pattern Sequence

CRC - Cyclic Redundancy Check

FDL - Facility Data Link

Thus, frame alignment requires detection of the frame pattern sequence (FPS) in each of the above bit positions spaced apart by 772 bits in a data stream. Since the data stream is subjected to bit errors during transmission, however, reliable frame detection may require the detection of framing bits over several frames or superframes. A further requirement is that the frame aligner should reliably align in the presence of data errors that may also affect the frame bit pattern. A common requirement for ESF is that frame alignment should be achieved within 15 ms. Since there is always a finite probability of random data mimicking the frame alignment pattern, the requirement is usually stated in terms of finding a frame alignment within a certain amount of time and probability of

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correctness, for example, within 15 ms and a 99% probability that no data errors are present. A confirmation process often follows the frame alignment process, where the frame alignment is confirmed by additional checks before being accepted as the correct alignment. A common confirmation technique used with the ESF format is to calculate the CRC with the provisional alignment and compare the calculated CRC with the actual CRC bits C1-C6 transmitted over the DS1 frame bits.

Once frame alignment is achieved, the framer continues to check the frame alignment pattern for correctness. If errors exceed a certain threshold, an Out of Frame (OOF) signal is declared and a search for a fresh alignment is started. It is often observed that OOF conditions are declared due to burst errors subjected on the data stream and not due to a genuine change in the frame alignment. To avoid frequent frame alignments that can cause a disruption in the data processing, an offline frame aligner is often used. The inline framer, on detecting an OOF condition, requests the offline framer for a fresh search for frame alignment. The inline framer continues with the old alignment. If the offline frame aligner detects the same alignment as earlier, the inline framer will not be disturbed. Thus only genuine changes or loss in alignment will affect the inline framer.

Conventional circuits used to implement inline and offline framers suffer from many problems. For example, to detect the frame pattern sequence (FPS) spread over 4632 bits, the data is clocked one bit at a time through a shift register, and a check is made at each bit position for the frame pattern sequence in bit positions spaced at 772 bits. A large shift register capable of storing several frames would be required to reliably and quickly detect the frame pattern sequence. However, implementing large shift registers on integrated circuits requires substantial chip area and leads to other difficulties.

The above problems are exacerbated when multiple channels are required. For example, handling multiple channels using conventional approaches requires completely duplicating the amount of circuitry required for one channel for each of the multiple channels. A scalable approach would be preferred.

SUMMARY OF THE INVENTION

The present invention relates to an architecture and methodology for performing frame alignment that is scalable for any of a plurality of multiplexed channels, and is adaptable for any of a variety of framing formats.

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In accordance with an aspect of the invention, an offline frame alignment circuit can simultaneously achieve frame alignment for a large number of TDM streams (i.e. channels) within a required amount of time (e.g. 15 ms for ESF). The Multi-channel Frame Aligner (MCFA) uses a high speed system clock independent of the individual line clocks to perform frame alignment for each of the channels. The MCFA includes a framer memory to store the alignment states of all possible framing bit candidates for all channels. The MCFA polls each channel to determine if frame alignment is requested, and if so, if data from the associated channel is available. A state machine in the MCFA compares the received data with the expected framing bits and adjusts the stored alignment states accordingly. All framing bit candidates are processed in parallel leading to fast alignment times. The MCFA architecture can be adapted for any of a plurality of channels and framing formats merely by adjusting the speed of the MCFA system clock and capacity and arrangement of data states in the framer memory.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures, wherein:

FIG. 1 is a block diagram illustrating a multiplexing scheme in a conventional communications system;

FIG. 2 is a block diagram of an example frame alignment architecture in accordance with an embodiment of the present invention;

FIG. 3 illustrates a framing scheme in a data stream that can be detected by the frame alignment architecture of the present invention;

FIG. 4 is a functional block diagram illustrating an example frame alignment method that can be implemented by the frame alignment architecture of the present invention;

FIG. 5 is a structural block diagram illustrating an example implementation of the frame alignment architecture of the present invention in accordance with an ESF framing scheme;

FIG. 6 is a state transition diagram illustrating an example of a state transition scheme that can be implemented by the frame aligner of the present invention;

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FIG. 7 illustrates an example of data structures that can be used to implement storage of channel and data state information for a plurality of channels for which frame alignment can be performed by the frame aligner of the present invention;

FIG. 8 is a block diagram further illustrating an example of a frame alignment engine that can be included in the frame alignment architecture of the present invention illustrated in FIG. 5;

FIG. 9 is a state diagram illustrating an example of the processing flow in the frame alignment engine illustrated in FIG. 8 in accordance with an embodiment of the present invention; and

FIG. 10 is a block diagram further illustrating an example of a RAM interface block that can be included in the frame alignment engine illustrated in FIG. 8 in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail with reference to the drawings, which are provided as illustrative examples of the invention so as to enable those skilled in the art to practice the invention. Notably, the implementation of certain elements of the present invention may be accomplished using software, hardware or any combination thereof, as would be apparent to those of ordinary skill in the art, and the figures and examples below are not meant to limit the scope of the present invention. Moreover, where certain elements of the present invention can be partially or fully implemented using known components, only those portions of such known components that are necessary for an understanding of the present invention will be described, and detailed descriptions of other portions of such known components will be omitted so as not to obscure the invention. Further, the present invention encompasses present and future known equivalents to the known components referred to herein by way of illustration.

FIG. 2 is a block diagram illustrating an example architecture including a Multi-channel Frame Aligner (MCFA) in accordance with an embodiment of the present invention.

As shown in FIG. 2, MFCA 202 communicates with inline framers 204 for each channel 1 to N. MFCA 202 further maintains a state table 206 for each channel 1 to N. In operation, inline framers 204 continuously monitor the data stream for a corresponding channel for an out of frame (OOF) condition. When such a condition occurs, framers 204

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request MCFA 202 to detect the presence of the framing pattern sequence (FPS) in the corresponding channel 1 to N. After receiving a request from a framer 204, MCFA 202 begins to collect data from the requesting channel. MCFA 202 then compares the collected data with the FPS to update a state maintained for that channel, and when frame alignment is detected, it is reported back to the requesting framer 204.

An advantage of the architecture of FIG. 2 is that the single MCFA 202 can simultaneously perform frame alignment for a plurality of channels 1 to N. In other words, even though channels 1 to N and framers 204 are operating independently of each other, the MCFA 202, by maintaining state tables for all of them, can identify and maintain a frame alignment state for each channel simultaneously and independently. A further advantage is that the number of channels that can be processed by the single MCFA 202 can be easily extended by adding additional state tables, and also perhaps by increasing a processor clock speed, as will be described in more detail below. Further, the present architecture can be used to perform frame alignment for a variety of framing formats, such as DS1 SF, DS1 DDS, DS1 SLC-96, ITU-T G.704 based E1, which formats can be either pre-programmed or adjusted dynamically.

FIG. 3 further illustrates the data stream for a given channel. As shown in FIG. 3, within the data the entire FPS (comprising FPS bits FPS_1 to FPS_n) will be repeated once per FPS interval. Generally, the FPS interval will coincide with an extended frame for the given frame format (e.g. six frames = an extended frame in the ESF format). FIG. 3 shows m iterations (FPS Iteration 1 to FPS Iteration m) of the FPS in a data stream for a given channel. For an unaligned data stream, the location of the FPS in the data stream is unknown. Accordingly, each bit of the FPS occurs at an arbitrary FPS bit offset within the data stream. However, it is known that a FPS bit will occur repeatedly at that same FPS bit offset after a known FPS bit interval in the data stream. For example, in an ESF framing scheme, a FPS bit will occur once every 772 bits in a data stream. Accordingly, for a given number of bits in an FPS bit interval, an FPS bit will occur at a constant FPS bit offset in each consecutive FPS bit interval of the data stream. It should be further apparent that an entire FPS will be received after n FPS bit intervals of the data stream have been received, although perhaps not beginning with the first FPS bit in the sequence.

As should be thus apparent from the above, one way to perform frame alignment is to determine the FPS bit offset, given an arbitrary starting point of collecting data from a data stream for a given channel. It should be further apparent that it may not be sufficient to

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simply collect data corresponding to one iteration of the FPS, because the starting bit in the FPS will be an arbitrary one of the FPS bits FPS_1 to FPS_n. Accordingly, MCFA 202 collects data for m iterations of an FPS sequence, where m is selected to yield a frame alignment determination within a given probability of correctness (e.g. 99%).

It should be noted that the FPS need not be comprised of single bits at each bit offset, but that the FPS may include multiple bits at each bit offset.

A general operation of MCFA 202 for detecting the FPS bit offset in a data stream for a given channel will now be described with reference to FIG. 4. Although the following describes a frame alignment operation for only one channel for ease of illustration, it is an aspect of the invention that MCFA 202 includes the ability to simultaneously perform frame alignment for up to all channels associated with the MCFA 202 (e.g. by maintaining state tables for all channels). Such aspects of the invention will be described in more detail in following sections of the present specification.

When MCFA 202 receives a request for frame alignment from an inline framer 204, it will set up a state table for the corresponding channel. As shown in FIG. 4, the table 402 includes p entries, one for each bit in a frame bit interval (e.g. 772 for an ESF framing scheme). Each of the entries is initialized to 0, as is the bit offset counter.

Data received from the corresponding channel is examined one bit at a time (in an example where the FPS is comprised of individual bits at each frame bit interval). The comparator 404 compares the received data bit to the FPS bit indicated by the FPS bit interval counter 406. The FPS bit interval counter 406 contains the value of the entry in table 402 pointed to by the bit offset counter 408 plus one (i.e. the next expected bit in the FPS sequence 410). For example, when the first bit is received at each bit offset, the value in the entry corresponding to each bit will be zero, so the received bit is compared to the first FPS bit. Whenever the received data bit matches the expected FPS bit, the entry in state table 402 corresponding to the value of the bit offset counter is incremented. Otherwise, the entry is reset to 0. For example, if the first bit received (i.e. Bit 0) matches the first FPS bit (i.e. 0 plus one), the Bit 0 entry in the table 402 is incremented to 1.

After each received data bit is processed, the bit offset counter 408 is incremented, and after p data bits are received and processed, the bit offset counter is reset. Thus, when the p-th data bit (i.e. Bit p-1) is received, the value of the bit offset counter 408 will be p-1. Accordingly, if the p-th received data bit matches the first FPS bit, the Bit p-1 entry in the table 402 is incremented to 1. After the p-th data bit is processed, the bit offset counter 408

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resets to 0. The next received data bit will thus be compared to the next FPS bit in the sequence after the value in the table entry for Bit 0, and if it matches, the Bit 0 entry in table 402 will be incremented by 1. Otherwise, the Bit 0 entry in table 402 will be cleared (i.e. reset to 0).

MCFA 202 thus, in this example of the invention, maintains a running total of the number of sequential matches with the FPS at each bit (or collection of bits) in an FPS bit interval. When the value of any entry in table 402 reaches n, this indicates that one entire FPS was present at the FPS bit offset corresponding to that entry, and the bit offset is reported to the inline framer.

It should be noted, however, that it may take data corresponding to several FPS intervals to be received and processed (i.e. several multiples of, or FPS bit matches greater than, n) for only a single entry to exhibit a frame alignment match due to bit errors and mimics, for example. It should be further noted that the state maintained for a channel can be different than a running total, and may implement other state transition schemes, as will be described in more detail below. It should be even further noted that each channel may simultaneously use different framing schemes, or that all channels may use the same framing scheme, and the MCFA 202 can include the ability to simultaneously detect the same or different framing sequences in a number of channels using the same or different framing schemes.

The present invention will now be described in more detail in connection with an example implementation illustrated in FIG. 5. In this example of the invention, ESF is assumed as the framing scheme for all channels. However, those skilled in the art will understand how to extend the principles of the invention to other and/or simultaneously different framing schemes after being taught by the foregoing example, and so the example should not be construed as limiting.

The frame alignment architecture illustrated in FIG. 5 can be implemented, for example, in a portion of an integrated circuit (i.e. channel bank), perhaps along with, or in addition to, other channel and frame processing circuitry, which integrated circuit can be included in a physical layer device coupled to T1 lines, for example. As should be apparent, such a frame alignment architecture and physical layer device can find uses in a variety of applications in association with various points of aggregation including a central office, a digital loop carrier, channel bank, DSU/CSU, Digital Access Cross Connects(DACS), PBX, multiplexors etc.

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As shown in FIG. 5, in this example of the invention, multi-channel frame alignment engine (MFAE) 502 is adapted to perform off-line frame alignment for 28 inline framers 504-1 to 504-28. As further shown in FIG. 5, inline framer 504 includes an OOF Detector 506, frame registers 508, serial-in-parallel-out (SIPO) block 510 and line counter 512.

Each inline framer 504 receives a receive line data signal, *rx_line_data* containing a DS1 time division multiplexed signal. Associated with each line data signal is an *rx_line_clk* signal that is recovered from the corresponding line data signal using a clock recovery circuit (not shown). At each active edge of *rx_line_clk*, the *rx_line_data* signal is serially clocked into serial-in-parallel-out (SIPO) register 510. Each SIPO 510 can be comprised, for example, of two registers of 16 bits each so that while one register is being written, the other is available for reading. SIPO 510 generates a *sipo_full* signal once all 16 bits are written into the register.

Line counter 512 is comprised of a simple counter that increments from 0 to 771 on each *rx_line_clk* pulse. It resets to zero after 772 pulses have been received, or when a *frame_req* signal has been generated by OOF detector 506.

OOF Detector 506, when in frame alignment, monitors the framing bits for bit errors. If the frame bit errors exceed the OOF criteria, a *frame_req* signal is generated, requesting a fresh frame realignment. For example, given a current frame alignment (i.e. a detected FPS at a given bit offset), OOF detector 506 monitors the continued presence of the FPS at the expected bit offsets. If a certain number of bits in the data stream do not match the FPS at the expected bit offsets over a certain number of repetitions of the FPS, an out of frame condition is assumed. The *frame_req* signal also resets the line counter 512 to 0.

Frame registers 508 store the frame location (i.e. the bit offset for the FPS) for the associated channel. Frame registers 508 also latch the *frame_req* signal generated by the OOF detector 506 so that it can be detected by MFAE 502.

Multi-channel Frame Aligner Engine (MFAE) 502 continuously polls all channels sequentially for *frame_req* and *sipo_full* conditions. This is achieved through the FAE control bus 520 using the *fae_addr[4:0]*, *fae_rd* and *fae_wr* signals. These signals generated by MFAE 502 and, generally, all signals on buses 520, 522 and 524, are synchronous to the high speed system clock *fae_clk*. In order to read or write into an inline framer 504, MFAE 502 uses the word *fae_addr[4:0]* to output the address of the channel along with a *fae_rd* or *fae_wr* signal for one clock cycle on bus 520. Data is read out from

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an addressed inline framer 504 on read bus 522 via the word *fae_data_in[15:0]*. Data can be written to an inline framer 504 on write bus 524 via the word *fae_data_out[9:0]*.

An active *frame_req* signal generated by an inline framer 504 causes MFAE 502 to initiate a search for frame alignment for that channel. The signal is also used to initialize a frame bit counter associated with each channel in the MFAE 502 and maintained in framer RAM . This counter is used to keep track of all 772 frame bit candidates. Because the *frame_req* signal also resets the line counter 512, the frame bit counter in the MFAE 502 is thus synchronized to the line counter 512 in the corresponding inline framer 504. Once the request for frame alignment is registered for a channel, polling for the *sipo_full* for that channel is started. An active *sipo_full* condition indicates that 16 bits of data are available for processing. The data bits are read out from the requesting inline framer 504 by addressing the channel through *fae_addr* and simultaneously asserting *fae_rd* on control bus 520. The addresses on the *fae_addr* lines are compared to a hard-wired *fae_id* signal in each of the inline framers 504. The *fae_id* signal in each framer 504 has a unique value ranging from binary 0 to binary 27. If the address on *fae_addr* matches that of *fae_id* for a channel, the data bits stored in SIPO 510 for the channel are driven on read bus 522 via the *fae_data_in* word.

The *sipo_full* signal is asserted by each inline framer 504 once every 16 cycles of the associated *rx_line_clk*. Since the nominal *rx_line_clock* rate is 1.544 MHz for DS1, the *sipo_full* signal will be independently asserted by each inline framer 504 every 10.36 microseconds. To accommodate jitter and frequency variations, which is estimated to be a maximum of 2 UI in 16 clocks, the MFAE 502 should be able to read out data from the SIPO 510 at least once every 9.06 microseconds to avoid SIPO overflow and data loss. In one example implementation of the invention that will be described in more detail below, processing of 16 bits of data by MFAE 502 takes 17 *fae_clk* cycles. In the worst case, all 28 channels may request for frame alignment, and so 28 x 17 *fae_clk* cycles may need to elapse before the next *sipo_full* indication from the same inline framer 504 can be serviced. Thus, the maximum *fae_clk* period can be estimated as 9.06/(28 x 17) = 19.03 nanoseconds. In other words, the *fae_clk* must have a frequency greater than 52.5 MHz in order to process data for all channels in such a worst case scenario without losing data. If the number of channels to be handled is 84 rather than 27 (as in a DS3 framing scheme, for example), then the *fae_clk* frequency will have to be greater than 158 MHz.

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Referring back to FIG. 5, MFAE 502 further communicates with framer RAM 514 and state machines 516-1 and 516-2. Two state machines operate in parallel in this example of the invention for reasons that will be explained in more detail below. However, the invention is not limited to this example, and one or more than two parallel operating state machines may be implemented. The following will describe the operation of one state machine 516, which description will also apply to the other state machine. Further, those skilled in the art will be able to implement the logical structure of state machine 516 after being taught by the following descriptions and the attached drawings.

State machine 516 receives a framing bit candidate's previous state from framer RAM 514 and updates the previous state based on a comparison between the current received data bit and the FPS bit expected to be received (i.e. the next bit in the FPS sequence corresponding to the stored state). For example, if the current stored state indicates that three bits in the FPS sequence have been correctly and sequentially received at that bit position (i.e. a sequence of 001 has already been received in the last three FPS bit intervals at that bit position), then the next expected bit should have a value of 0. Thus, state machine 516 will receive the current stored state and the current received data bit. If the current received data bit has a value of 0, the state machine will output an updated state indicating that four bits in the FPS sequence have been correctly and sequentially received at that bit position. Otherwise, it will output an updated state indicating that the comparison failed.

An example of a state transition scheme that can be implemented by state machines 516 is shown in FIG. 6. The state transition diagram is shown for a single bit position in a single channel. As shown in FIG. 6, in this example of the invention, the state for a given bit offset can transition from states S0 to S23. The states S18 to S23 correspond to frame aligned states.

Initially on receipt of a *frame_req* signal, the default state for each bit position of that channel is S0. The state machine 516 advances the stored state by one state each time a bit received at that bit position corresponds to the expected bit pattern in the FPS (e.g. the ESF Frame pattern sequence of 001011). For example, immediately after starting to collect data for a channel, MFAE 502 causes state machine 516 to start looking for the first bit in the ESF sequence, which is 0. Accordingly, when the first bit for each of the 772 possible bit positions is received, if the value of the received bit is 1 rather than 0, the state for that bit position stays at S0; otherwise, the state for that bit position advances to S1. In the next

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FPS bit interval of the received data for that channel (i.e. after all other 772 bits have been received and processed for that channel), the next expected bit in the FPS is 0, regardless of whether the state was advanced to S1 or remained at S0. When each subsequent bit is received, state machine 516 also receives the stored state for the corresponding bit offset (either S0 or S1). As shown in FIG. 6, a received data bit of 0 will cause the state machine to advance the corresponding bit position to the next state from both states S0 and S1. Accordingly, if the next received bit for the bit position has a value of 0, the state for that bit position transitions to state S1 or S2 (depending on whether the last received bit had a value of 0 also); otherwise, the state returns to S0 (from either S0 or S1).

After all 6 bits in the FPS have been received correctly in sequence at a given bit position, the stored state for that bit position will have been advanced by state machine 516 to S6. However, in one example of the invention shown in FIG. 6, a further 12 bits having the sequence of 001011001011 must be received correctly to declare a frame alignment at that bit position. Thus, a total of 18 bits must be received correctly and the state for that bit position must have advanced to S18 in order to declare a frame alignment (indicated by the signal SF from state S18). This is because the number of frames required for a 99 % correct probability of alignment is 17 for a frame word length n = 1 and frame content alpha = 0.129 %. (Frame content alpha is defined as the fraction of frame alignment word to the total frame capacity. Since there are 6 FPS bits over a frame of 4632 bits in the ESF mode, alpha = 6x100/4632 = 0.129 %).

Since each ESF frame bit is separated by 772 bits, the frame length refers to the number of 772 bit frames as sub frames (i.e. the FPS bit interval). Each one of the 772 bits can be a framing bit candidate. Hence state machine 516 compares each received bit with the next FPS bit corresponding to the state stored for the previous 772 frame bit candidate (e.g. if the stored state is S0, S6, S12 or S18, the first FPS bit is compared with the received bit). This is done in parallel by state machines 516-1 and 516-2 for all 772 bit candidates by maintaining 772 states in framer RAM 514. Assuming the worst case condition where the *frame_req* signal is generated at a bit position one clock after the frame bit position, and that the frame sequence starts at 010110 instead of 001011, a maximum of 24 sub-frames may be required to be received and processed for declaring a frame alignment with the necessary probability of correctness. The frame bit interval corresponds to 772 line clock periods, which is equal to 0.5 ms. This leads to a time (referred to as MART - maximum average reframe time) of 12 ms for frame alignment, which is well within the desired time of 15 ms.

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FIG. 6 further illustrates how the state machines 516 can implement a state transition scheme that leads to more rapid frame alignment. In principle, the state transition scheme illustrated in FIG. 6 does always not require a return to state S0 when an unexpected bit is encountered at every other state. Rather, the state returns to a previous state in accordance with a strength of the match with the FPS at that state. For example, as shown in FIG. 6, when the state for a bit position has advanced to S6 (i.e. an entire sequence of the FPS has been received at that bit position), a subsequent non-matching bit causes the state to be returned to S1. However, when the state for a bit position has advanced to S18 (i.e. three entire sequences of the FPS have been consecutively received at that bit position), a subsequent non-matching bit causes the state to only be returned to S7. Thus, only two additional sequences of the FPS need be consecutively received at that bit position for a frame alignment to be declared.

It should be apparent that the state transition scheme illustrated in FIG. 6 is only an example, and that other schemes may be implemented. For example, a strict state transition scheme where all non-matching conditions require a return to state S0 may be implemented. Alternatively, more forgiving state transition schemes may be implemented wherein only a return to a state corresponding to a previous FPS interval is required upon a non-matching condition, for example. Moreover, it should be further apparent that the number of states and the number of iterations of the FPS that must be received for frame alignment can be changed depending on the framing scheme used.

Framer RAM 514 is, for example, a single port burst mode RAM that is organized as 5432 words, each word having 32 bits. This desired capacity is determined from the number of channels that can be aligned in this example implementation (i.e. 28), as well as the number of possible data states that are stored for each framing bit candidate (i.e. 24), as will become more apparent from the descriptions below. It should be noted, however, that the desired capacity of the RAM can be easily designed for different state transition schemes, numbers of channels, and framing schemes, for example, after those skilled in the art are taught by the following descriptions for the present example implementation. It should be further noted that, although a single RAM is used to store the alignment states for all channels in this example implementation, that this is not necessary for the invention.

An example of a data structure 700 that can be stored in RAM 514 for maintaining channel frame alignment state information is shown in FIGs. 7A to 7C. As shown in FIG. 7A, block 702 comprises the first twenty-eight words in RAM 514 which are used to store

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each channel's state variables. An example of the structure of a data word 706 that can be used to store one channel's state variables is shown in FIG. 7B. As shown in FIG. 7B, the state variables maintained for each channel include *frm_align_on*, *frm_status[1:0]*, *frm_ctr[3:0]*, *frm_bit_ctr[8:0]*, *init_ram* and *ram_addr_ctr[12:0]*. The state variable *frm_align_on* is used to store the current frame alignment status for that channel (e.g. a value of 1 indicates that the channel is in frame alignment). The state variable *frm_status[1:0]* is used to store the number of FPS patterns detected in a data stream (i.e. the number of entries having a state of 24; this can be more than one due to the possibility of mimics in the data stream). The state variable *frm_ctr[3:0]* is used to store the number of superframes that have been processed from a data stream. The state variable *frm_bit_ctr[8:0]* is used to store the number of bits received for a channel, modulo 772. The state variable *init_ram* is used to store a value of 1 for the first 772 bits received for a channel after a *frame_req* signal has been received. This is used to cause the state machines to use a hard-wired initial state rather than the stored state so that the RAM need not be re-written with zeroes. The state variable *ram_addr_ctr[12:0]* is used to store the current RAM index into the data states for the associated data channel from the beginning offset for that channel.

As further shown in FIG. 7A, the remainder of the RAM is divided into 28 blocks 704-0 to 704-27, each block 704 having 193 words for storing the data states for every bit in a respective one of the 28 channels. An example of a data state word structure 708 is shown in FIG. 7C. As shown in FIG. 7C, four data states each having 5 bits are stored in one word. Thus 772 data states (193 x 4) are stored in memory for each channel. Each data state represents the current ESF frame alignment state of that candidate bit. Since 5 bits are stored for each data bit, up to 32 state conditions can be stored. However, in an example of the invention where the state machines 516 described above are implemented, only 24 state conditions (i.e. S0 to S23) are stored, with a stored value of 0 corresponding to the state S0 up to a stored value of 23 corresponding to state S23.

Although FIGs. 7A through 7C illustrate an example of data structures that can be used to implement storage of alignment states for a predetermined number of channels (e.g. 28) and a predetermined framing format (e.g. ESF), those skilled in the art will be able to understand how to implement storage of alignment states for variable numbers of channels and/or framing formats after being taught by the present example, and so the invention is not limited to these illustrative descriptions.

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FIG. 8 is a block diagram illustrating an example of MFAE 502 in more detail. As shown in FIG. 8, MFAE 502 includes an engine controller 802, a data buffer 804, a multiplexer 806, a RAM interface 808 , a frame detection block 810 and a channel counter 812.

Generally, engine controller 802 receives and operates at the *fae_clk* to coordinate the task of performing frame alignment for each of inline framers 504 that has requested alignment. Engine controller 802 cycles through each of the 28 channels in accordance with channel counter 812 (which cycles from 1 to 28). For each channel, engine controller 802 determines whether frame alignment has been requested and if data is available (e.g. by checking the *frame_req* and *sipo_full* signals for that channel). If so, sixteen bits of data are read from the inline framer on *fae_data_in[15:0]* from read bus 522 and latched into buffer 804 (e.g. a 16 bit shift register). The received data bits are then serially shifted out two bits at a time. Even bits are diverted to state machine 516-1 and odd bits to state machine 516-2 using the multiplexer 806. Thus for every clock cycle *fae_clk*, engine controller 802 causes the two state machines 516-1 and 516-2 to receive the previous state in *state_in[4:0]* from the RAM interface 808 and the data candidate bit from data buffer 804.

Frame detection block 810 monitors the state machines for an indication that a frame alignment has been detected, and generates a *frame_sync* signal to the associated channel in that case. A *frame_bit_ctr* maintained in the framer RAM 514 for each channel increments from 0 to 771, which tracks which candidates bit or bits frame detection block 810 provides along with *frame_sync* signal.

Engine controller 802 can be implemented substantially by a state machine. An example of the operation of engine controller 802 is further illustrated in FIG. 9. Those skilled in the art will be able to implement engine controller 802 based on the following and foregoing operational descriptions.

As shown in FIG. 9, in sequence, engine controller 802 may cycle through up to seven MFAE states for each of the 28 channels in 17 cycles of the *fae_clk* per channel. In the FAE_RD state, the engine controller 802 reads the SIPO status and data from the channel indicated by channel counter 812. Only if a valid *frame_req* and *sipo_full* is received as determined in the FAE_CH state, will the engine controller cycle through the remaining states for that channel. Otherwise, the cycle is aborted, the channel counter is incremented (e.g. from 0 to 27, modulo 28) and the FAE_RD state commences for the next channel.

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If valid *frame_req* and *sipo_full* signals are received, engine controller 802 causes RAM interface 808 to fetch the channel's previous state variables from the RAM 514's state variable area 702 during the ST_RD state. In the ST_RAM_RD state, engine controller 802 causes the data states for the current 16 bits to be fetched from the data state locations 704 for the associated channel in RAM 514. In the ST_PROCESS state, engine controller 802 causes the ESF state processing to be performed by state machines 516-1 and 516-2 two bits at a time, so as to reduce the number of clock cycles needed to process all 16 bits. Hence two instances of ESF state machines are used in this example of the invention. The updated states from the ESF state machine are stored back into the RAM in the ST_RAM_WR state. Finally, in the ST_WR state, the channel state variables are stored back into the cannel state location in the RAM 514. If frame alignment is achieved, then frame detection block 810 writes the status and frame bit location back into the inline framer 504 via the write bus 524 and word *frame_loc*. As shown in FIG. 8, engine controller 802 can allow for some overlap of functions between states, thus allowing all 16 bits of received data to be processed in 17 *fae_clks*.

An example of RAM Interface 808 is further shown in FIG. 10. As shown in FIG. 10, it includes address multiplexer 1002, data state address generator 1004, RAM address lookup table 1006, input buffer 1008, output buffer 1010, RAM pointer 1012, buffer counter 1014, input multiplexers 1016, 1018 and output multiplexers 1020, 1022. Generally, RAM interface 808 receives the MFAE states generated by engine controller 802, along with the current channel being processed as indicated by channel counter 812, and controls the writing and reading of channel and data states between framer RAM 514 and state machines 516-1 and 516-2 based on those received inputs. It should be noted that RAM interface 808 preferably also includes circuitry for reading, updating and writing channel state variables from and to the channel state area 702 of RAM 514. However, such circuitry is not shown here for ease of illustration of the present invention.

Referring to FIG. 10, it can be seen that the 13 bit wide *ram_addr* signals can address either the channel state area or the data state area in the framer RAM 514. More particularly, address multiplexer 1002 selects the channel address generated by channel counter 812 during the ST_RD and SR_WR states (i.e. for addressing the appropriate channel in channel state area 702) and the data state address generator 1004 in other states (i.e. for addressing the appropriate set of data states in data state areas 704). The channel counter increments from 0 to 27 and indicates the current channel or framer being

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processed. The data state address generator 1004 generates the address for the individual data states located in the data state area of the RAM. The generated address will be a combination of the index into the appropriate data state area obtained from the *ram_addr_ctr* of the channel state word stored in the RAM as shown in FIG. 7B and the starting address for the channel, *ram_start_addr*, obtained from RAM address look up table 1006. The data state address generator 1004 will increment the address by one word for every four candidate data bits that are processed. Once 193 words have been read out for a particular channel, the value of *ram_addr_ctr* will be reset to zero and the value of *ram_start_addr* from the look up table will be used as the starting address.

In this example implementation of the invention, 16 data bits for each channel are processed at a time. Accordingly, 4 words from the framer RAM 514 are read out in one burst during the ST_RAM_RD cycle. The data state address generation is repeated two times -- once in the ST_RAM_RD and once in the ST_RAM_WR cycles. In the ST_RAM_WR cycle the current data states for the 16 bits are written back into the data state area of the memory from the state machines 516-1 and 516-2. In the last MFAE state, ST_WR, the current *ram_addr_ctr* is stored back into the channel state word as shown in FIG. 7B. Thus for the next cycle of the channel, the data state address generator 1004 will continue to generate addresses from the last accessed location.

RAM interface 808 also generates signals for controlling the reading and writing of data states to RAM 514 depending upon the current MFAE state as provided by the engine controller 802. The RAM output enable signal, *ram_oe,* is kept permanently enabled. The RAM memory enable signal, *ram_me*, is driven during ST_RD, ST_WR, ST_RAM_RD, and ST_RAM_WR states. The RAM write enable signal, *ram_we*, is kept at logic 1 during ST_RAM_WR and ST_WR states when data is being written into the RAM.

The four data state words read out from the RAM beginning at the address generated by the data state address generator 1004 are stored into a 16 location deep and 5 bit wide register array, input buffer 1008, during the ST_RAM_RD state. Four individual 5 bit data states are arranged in each 32 bit data word as shown in FIG. 7C. As shown, the lower 5 bits of each byte in each 32 bit data word contain the data state for a respective candidate bit (e.g. bit 0 to 771 for each channel). The data states read from the RAM during the ST_RAM_RD state are written into a location in input buffer 1008 in accordance with the value of the RAM pointer 1012. The pointer is incremented by 4 every clock during the ST_RAM_RD state. Thus, the first four data states read from the RAM (i.e. from the first

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data state word addressed by the data state address generator 1014) are written into a first column of the input buffer 1008 on the first clock, the next four data states read from the RAM (i.e. from the second data state word addressed by the data state address generator 1014) are written into a second column of the input buffer 1008 on the second clock, and so on.

Data is read out from input buffer 1008 in a first-in-first-out fashion two data states at a time. Input multiplexers 1016, 1018 redirect five bits of data from an appropriate location in input buffer 1008 into either state machine 516-1 or 516-2. All even data bit states (i.e. states corresponding to Bit 0, Bit 2, Bit 4, etc.) are sent to state machine 516-1 through the *state_in_0[4:0]* signals, while all odd data bit states (i.e. states corresponding to Bit 1, Bit 3, Bit 5, etc.) are sent to state machine 516-2 through the *state_in_1[4:0]* signals. The reading of the data states out to the state machines is controlled by *st_buffer_ctr* 1014 which increments from 0 to 7 during the ST_RAM_RD and ST_RAM_WR states. For example, when *st_buffer_ctr* is 0, input multiplexer 1016 selects a first entry in a first column (i.e. entry 0) to be provided from input buffer 1008 on the *state_in_0[4:0]* signals, while input multiplexer 1018 selects a second entry in the first column (i.e. entry 1) to be provided from input buffer 1008 on the *state_in_1[4:0]* signals. Next, when *st_buffer_ctr* is 1, input multiplexer 1016 selects a second entry in a first column (i.e. entry 3) to be provided from input buffer 1008 on the *state_in_0[4:0]* signals, while input multiplexer 1018 selects a fourth entry in the first column (i.e. entry 4) to be provided from input buffer 1008 on the *state_in_1[4:0]* signals. Then, when *st_buffer_ctr* increments to 2, input multiplexer 1016 selects a first entry in a second column (i.e. entry 4) to be provided from input buffer 1008 on the *state_in_0[4:0]* signals, while input multiplexer 1018 selects a second entry in the second column (i.e. entry 5) to be provided from input buffer 1008 on the *state_in_1[4:0]* signals. It should be apparent that this scheme can allow for data to be written into certain locations of input buffer 1008 while data is read out from certain other locations of input buffer 1008.

The processed data states from the two state machines 516-1 and 516-2 are received and written back into RAM 514 by RAM interface 808 in substantially the reverse manner as described above. The processed data states are supplied by state machines 516-1 and 516-2 on the *state_out0* and *state_out1* signals, respectively. These are stored in output buffer 1010 via output multiplexers 1020, 1022. Output multiplexers 1020, 1022 cause processed data states received via the *state_out0* signals to be written into the even locations

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in the columns of output buffer 1010 while data states received on the *state_out1* signals are written into odd locations in the columns of output buffer 1010. During the ST_RAM_WR state, four five-bit data states at a time are written back into RAM 514. The *ram_ptr* points to the next location to be read from output buffer 1010 and increments by 4 every clock cycle. The four data states are formatted into one 32 bit word as shown in FIG. 7C and written back into the data state area of the RAM 514.

It should be noted that the above descriptions of the timings of operations of various components of RAM interface 808 with respect to the MFAE processing states received from engine controller 802 are given for ease of illustration. However, those skilled in the art will understand that more complex timing schemes may need to be implemented for proper sequence and/or pipelining of operations.

Frame detection block 810 monitors the *frame_sync* signals from both state machines 516-1 and 516-2 and latches the *frame_bit_ctr* value into a *frame_location[9:0]* register if a valid *frame_sync* signal is received. To avoid framing to a pattern that is random data mimicking the frame alignment pattern, frame detection block 810 is inactive until a minimum number of frames (e.g. 24) have been processed for the channel (as indicated by the *frm_ctr* word in the channel state variable, for example).

After the requisite number of frames have been processed for a given channel, frame detection block 810 will begin operation after each set of 16 data bits are received from the associated channel. At that time, three scenarios are possible:

1. No *frame_sync* signal has been generated. The search for a frame alignment is thus continued in the subsequent frames until the first frame alignment is found. This state is saved by setting *frm_status[1:0]* equal to a value of 0.

2. Only one *frame_sync* was detected in the entire range of 772 candidate bits. In this case, frame detection block 810 will set *frm_status* to a value of 1 and assert the *frm_align* signal. *Frame_location[9:0]* will indicate the position of the frame bit with respect to the *frame_req* signal.

3. More than one *frame_sync* signals is detected within a frame period of 772 bits. This indicates the presence of one or more mimic pattern and is indicated by *frm_status* having a value of 2. In this case the frame search is continued in subsequent frames until the mimic pattern dies out and only one frame alignment is obtained.

During each cycle in the ST_WR state, a check is made on the *frm_status* signals. If it has a value of 1, indicating a successful alignment, the *frame_location* value is written

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through the common bus *fae_data_out[9:0]* using the *fae_addr[4:0]* and *fae_wr* signals to the corresponding inline framer 504. The inline framer can then use this value to decode all other relevant data bits in the frame.

Although the present invention has been particularly described with reference to the preferred embodiments thereof, it should be readily apparent to those of ordinary skill in the art that changes and modifications in the form and details may be made without departing from the spirit and scope of the invention. It is intended that the appended claims include such changes and modifications.

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What is claimed is:

1. An apparatus for simultaneously determining a respective frame alignment in each of a plurality of channels, the apparatus comprising:

means for simultaneously storing a frame alignment state for a plurality of frame bit candidates for each of the plurality of channels;

means for receiving data from the plurality of channels;

means for updating the stored frame alignment state for each of the plurality of frame bit candidates in accordance with the received data; and

means for declaring the respective frame alignment in accordance with the updated frame alignment state for a certain one of the plurality of frame bit candidates for each of the plurality of channels.

2. An apparatus according to claim 1, wherein the updating means includes:

means for retrieving the frame alignment state for certain of the frame bit candidates associated with the received data;

means for comparing the received data with expected framing data based on the retrieved frame alignment states;

means for advancing the retrieved frame alignment states upon a successful comparison of the received data with the expected framing data;

means for withholding advancing of the retrieved frame alignment states upon a failed comparison of the received data with the expected framing data; and

means for replacing the retrieved frame alignment states with the updated frame alignment states in the storing means.

3. An apparatus according to claim 2, wherein the withholding means is operative to reset the retrieved frame alignment states to less advanced states in accordance with current frame alignment strengths indicated by the retrieved frame alignment states.

4. An apparatus according to claim 1, further comprising :

means for polling the plurality of channels for frame alignment requests; and

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means for controlling the operation of the receiving means, the updating means and the declaring means for certain of the plurality of channels based on the polled frame alignment requests.

5. An apparatus according to claim 4, wherein each of the plurality of channels includes an inline framer, the inline framer comprising:

means for generating the frame alignment request; and

means for processing channel data using an old frame alignment simultaneously while the respective frame alignment is being determined.

6. An apparatus according to claim 1, wherein the respective frame alignment for a first one of the plurality of channels is in accordance with a first framing scheme, and wherein the respective frame alignment for a second one of the plurality of channels is in accordance with a second framing scheme, the first and second framing schemes both being one of DS1 SF, DS1 DDS, DS1 SLC-96, and ITU-T G.704 based E1.

7. An apparatus according to claim 1, wherein the respective frame alignment for a first one of the plurality of channels is in accordance with a first framing scheme, and wherein the respective frame alignment for a second one of the plurality of channels is in accordance with a second framing scheme, the first and second framing schemes each being a different one of DS1 SF, DS1 DDS, DS1 SLC-96, and ITU-T G.704 based E1.

8. A method for simultaneously determining a respective frame alignment in each of a plurality of channels, the apparatus comprising:

simultaneously storing a frame alignment state for a plurality of frame bit candidates for each of the plurality of channels;

receiving data from the plurality of channels;

updating the stored frame alignment state for each of the plurality of frame bit candidates in accordance with the received data; and

declaring the respective frame alignment in accordance with the updated frame alignment state for a certain one of the plurality of frame bit candidates for each of the plurality of channels.

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9. A method according to claim 8, wherein the updating step includes:

retrieving the frame alignment state for certain of the frame bit candidates associated with the received data;

comparing the received data with expected framing data based on the retrieved frame alignment states;

advancing the retrieved frame alignment states upon a successful comparison of the received data with the expected framing data;

withholding advancing of the retrieved frame alignment states upon a failed comparison of the received data with the expected framing data; and

replacing the retrieved frame alignment states with the updated frame alignment states.

10. A method according to claim 9, wherein the withholding step includes resetting the retrieved frame alignment states to less advanced states in accordance with current frame alignment strengths indicated by the retrieved frame alignment states.

11. A method according to claim 8, further comprising :

polling the plurality of channels for frame alignment requests; and

controlling performance of the receiving step, the updating step and the declaring step for certain of the plurality of channels based on the polled frame alignment requests.

12. A method according to claim 11, wherein each of the plurality of channels includes an inline framer, the method further comprising:

processing channel data at the inline framer using an old frame alignment simultaneously while the respective frame alignment is being determined.

13. A method according to claim 8, wherein the respective frame alignment for a first one of the plurality of channels is in accordance with a first framing scheme, and wherein the respective frame alignment for a second one of the plurality of channels is in accordance with a second framing scheme, the first and second framing schemes both being one of DS1 SF, DS1 DDS, DS1 SLC-96, and ITU-T G.704 based E1.

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14. A method according to claim 8, wherein the respective frame alignment for a first one of the plurality of channels is in accordance with a first framing scheme, and wherein the respective frame alignment for a second one of the plurality of channels is in accordance with a second framing scheme, the first and second framing schemes each being a different one of DS1 SF, DS1 DDS, DS1 SLC-96, and ITU-T G.704 based E1.

15. An apparatus, comprising:

a frame alignment engine coupled to a bus for commonly receiving data from a plurality of channels, the received data from each of the plurality of channels including a framing pattern embedded at a frame bit offset with respect to an arbitrary starting bit of a stream of data respectively associated with each of the plurality of channels;

a memory coupled to the frame alignment engine, the memory having a plurality of channel state entries respectively corresponding to the plurality of channels, each of the channel state entries including a counter referenced to the arbitrary starting bit, the memory further having a plurality of data state entries for each of the plurality of channels, the plurality of data state entries respectively corresponding to a plurality of frame bit candidates, the frame alignment engine being responsive to data received from a requesting one of the channels so as to retrieve the counter for the requesting channel, and to retrieve certain of the data state entries corresponding to the received data from the requesting channel based on the counter; and

a state machine coupled to the frame alignment engine, the state machine including a comparator that is adapted to compare the data received from the requesting channel with the framing pattern and to update the certain data state entries based on the comparison.

16. An apparatus according to claim 15, wherein each of the plurality of channels includes an inline framer, the inline framer comprising:

a frame register for storing an old frame bit offset;

an out of frame detector coupled to the frame register for processing the respective stream of data using the old frame bit offset simultaneously while the respective frame bit offset is being determined.

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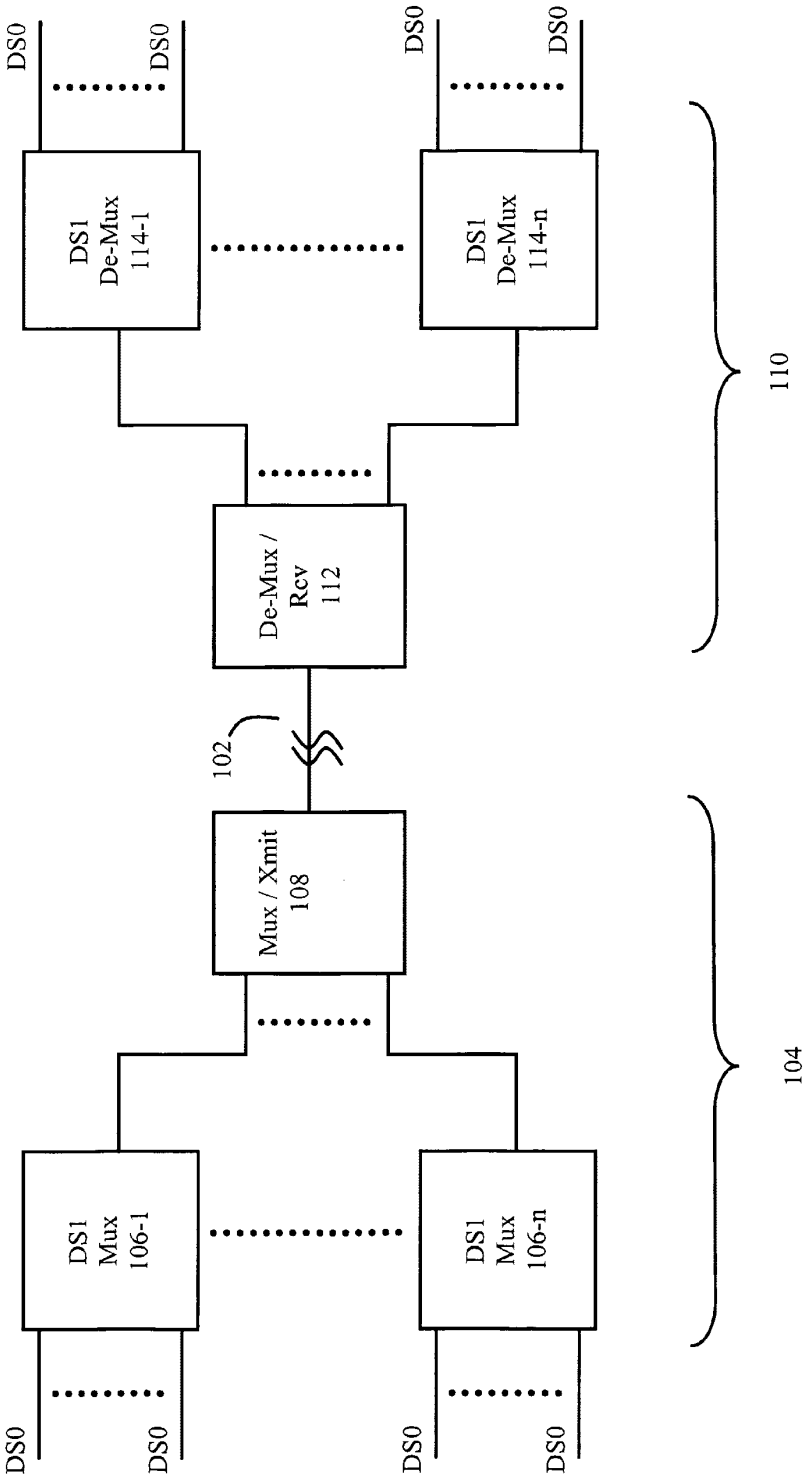

FIG. 1
(PRIOR ART)

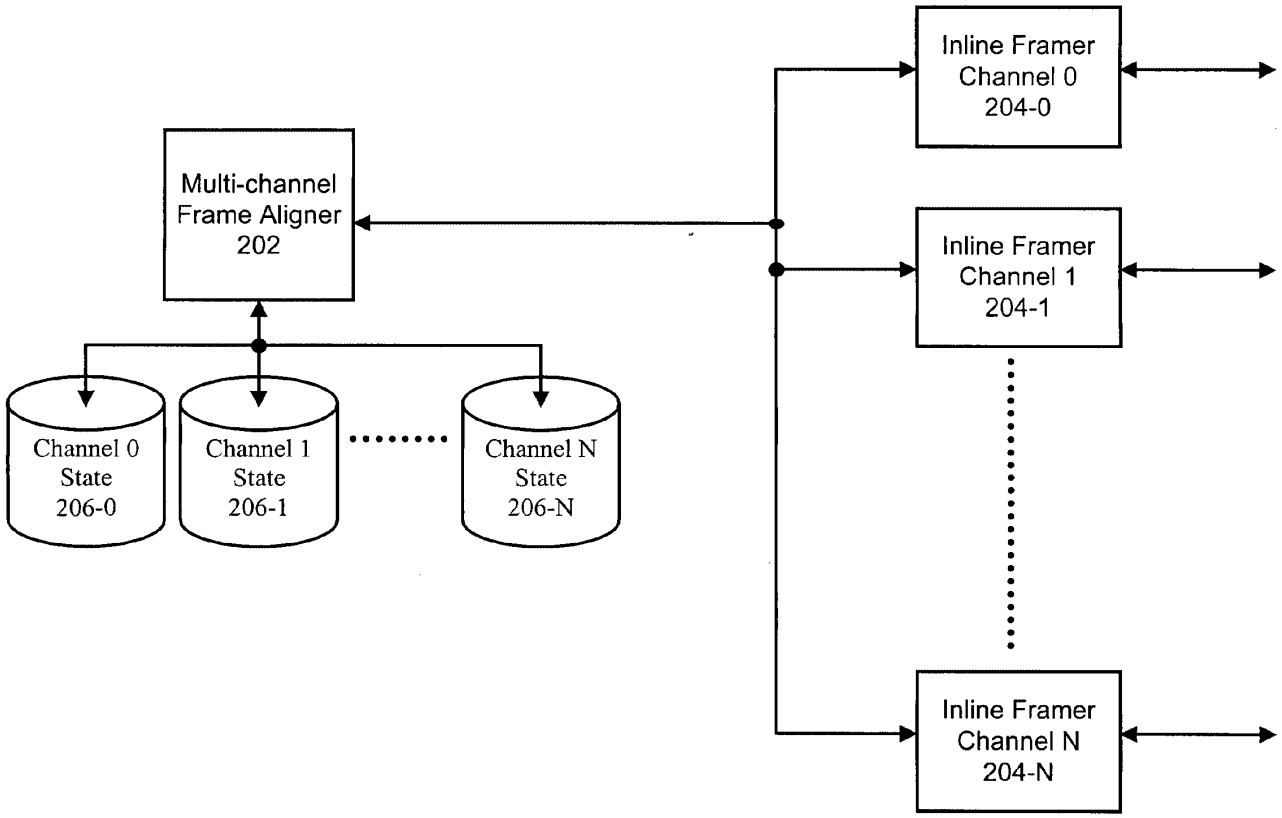
Multi-channel
Frame Aligner
202
Channel 0
State
206-0
Channel 1
State
206-1
Channel N
State
206-N
Inline Framer
Channel 0
204-0
Inline Framer
Channel 1
204-1
Inline Framer
Channel N
204-N

FIG. 2

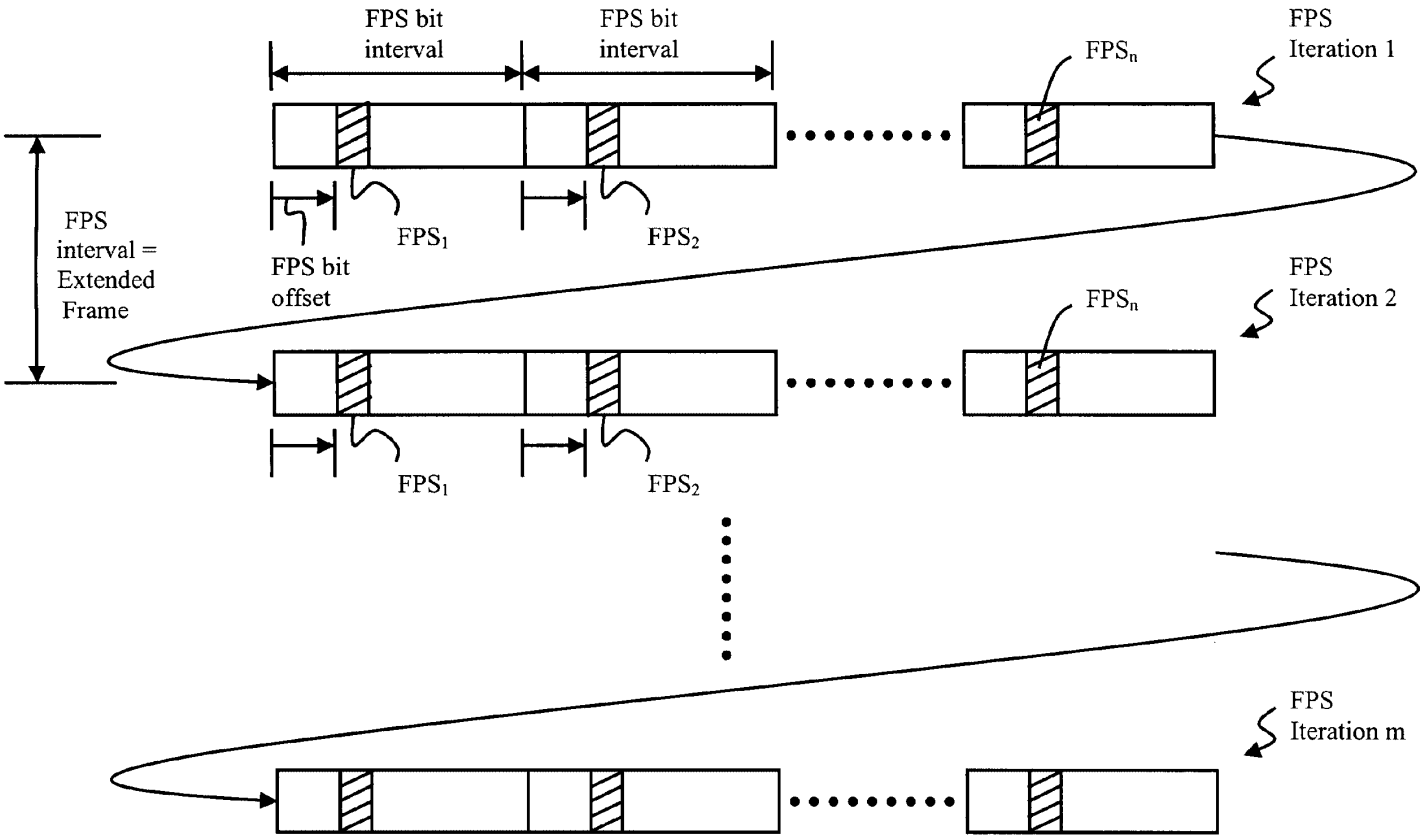

FIG. 3

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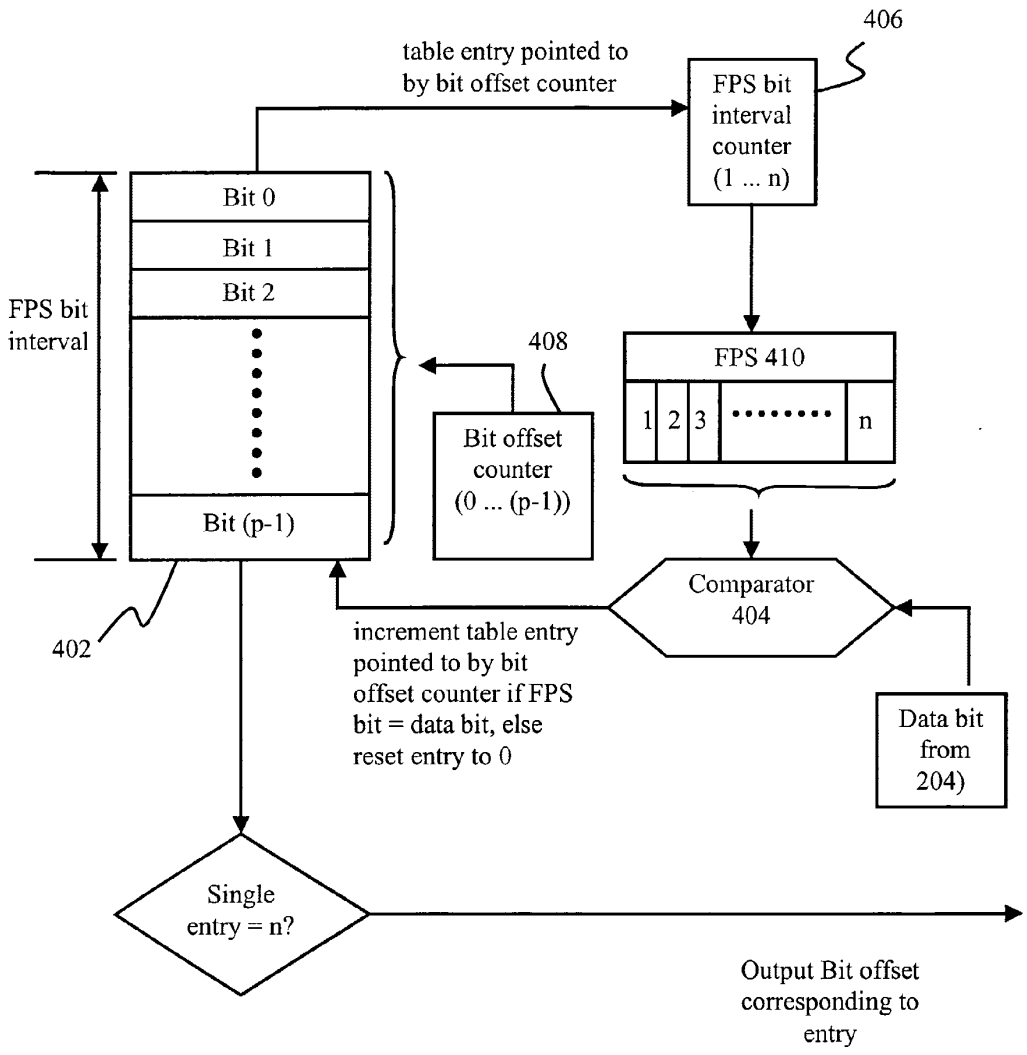
406
table entry pointed to by bit offset counter
FPS bit interval counter (1 ... n)
Bit 0
Bit 1
Bit 2
Bit (p-1)
FPS bit interval
408
Bit offset counter (0 ... (p-1))
FPS 410
1 2 3 n
Comparator 404
402
increment table entry pointed to by bit offset counter if FPS bit = data bit, else reset entry to 0
Data bit from 204)
Single entry = n?
Output Bit offset corresponding to entry

FIG. 4

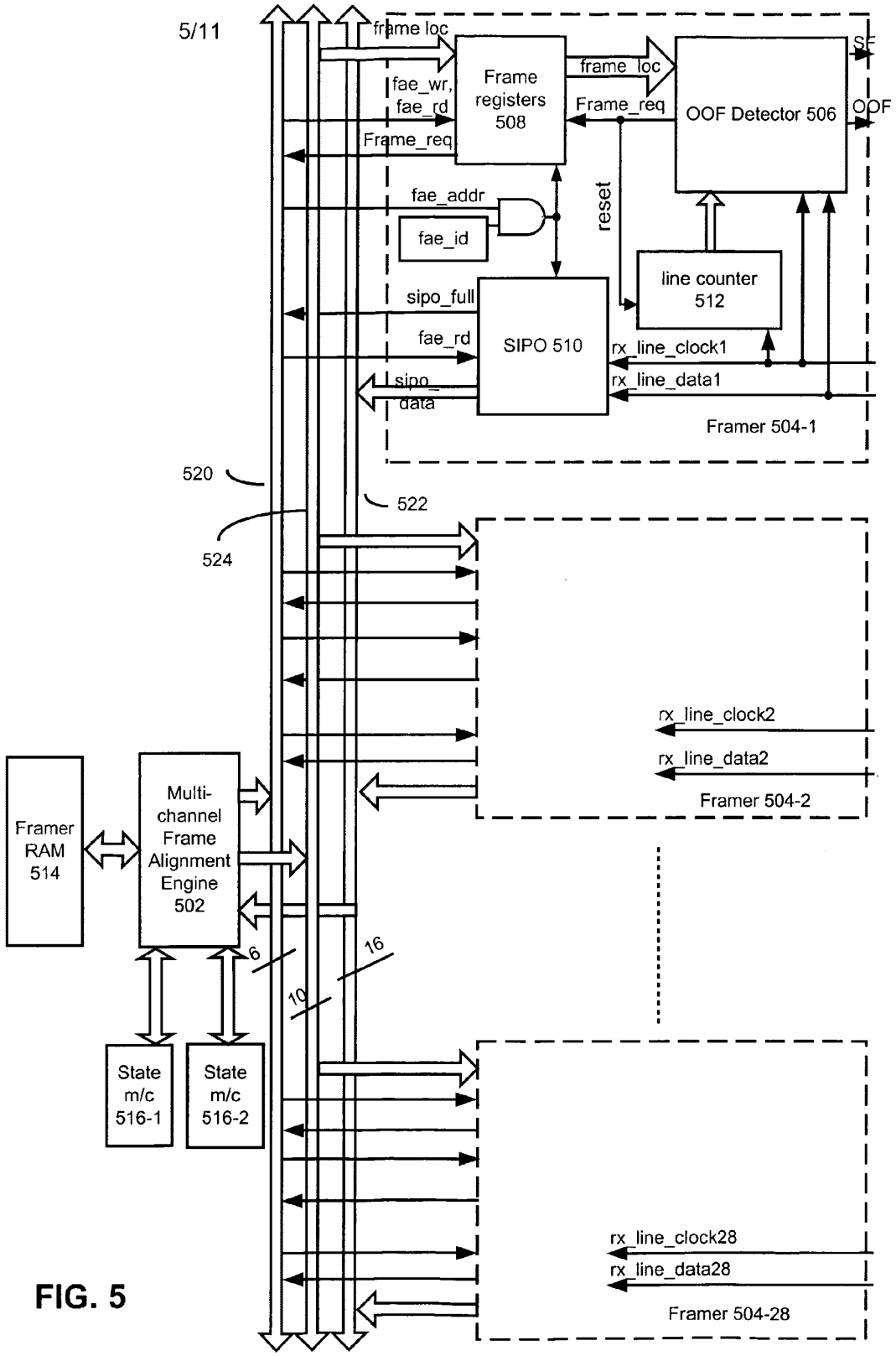
frame loc
fae_wr,
fae_rd
Frame_req
Frame registers 508
frame_loc
Frame_req
OOF Detector 506
SF
OOF
fae_addr
fae_id
reset
line counter 512
sipo_full
fae_rd
SIPO 510
rx_line_clock1
rx_line_data1
sipo_ data
Framer 504-1
520
522
524
rx_line_clock2
rx_line_data2
Framer 504-2
Framer RAM 514
Multi-channel Frame Alignment Engine 502
6
16
10
State m/c 516-1
State m/c 516-2
rx_line_clock28
rx_line_data28
Framer 504-28

FIG. 5

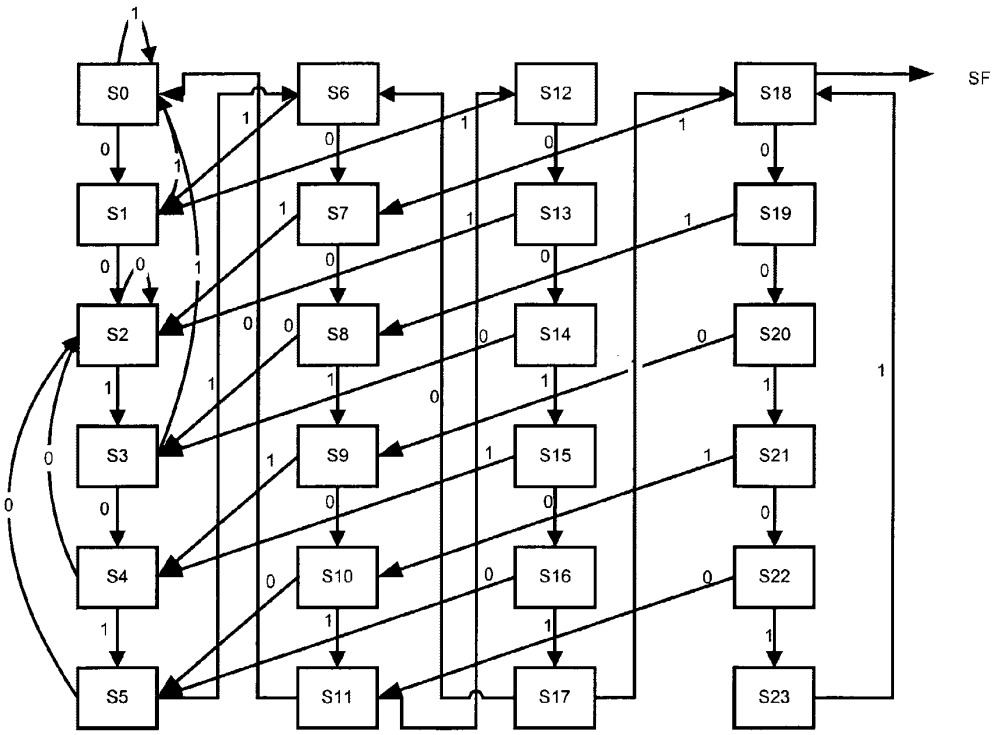
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
SF

FIG. 6

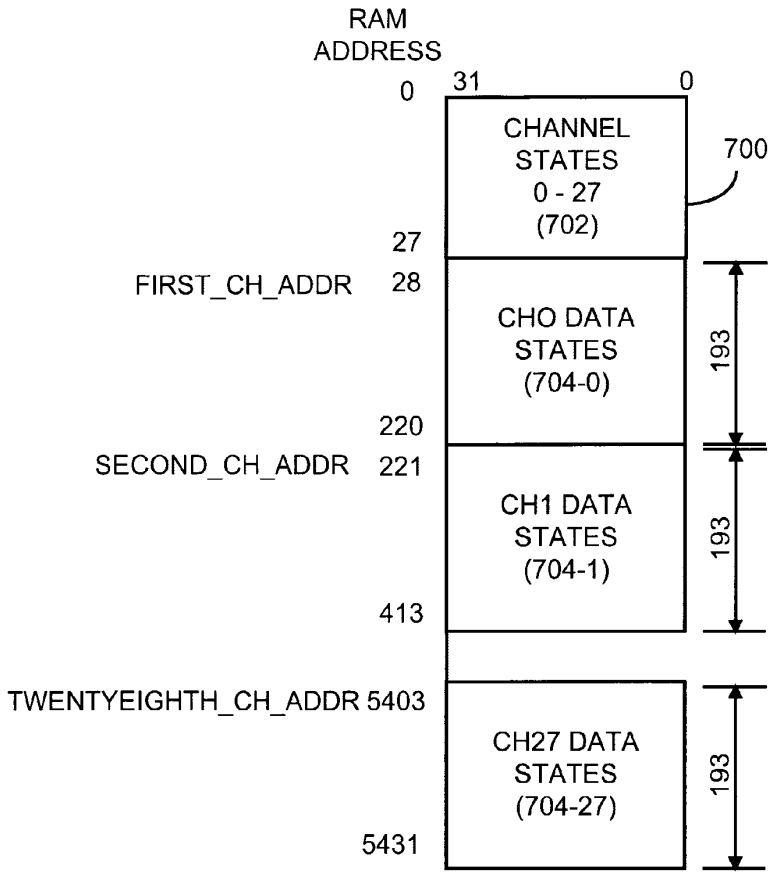
RAM
ADDRESS
0
31
0
CHANNEL
STATES
0 - 27
(702)
700
27
FIRST_CH_ADDR
28
CHO DATA
STATES
(704-0)
193
220
SECOND_CH_ADDR
221
CH1 DATA
STATES
(704-1)
193
413
TWENTYEIGHTH_CH_ADDR
5403
CH27 DATA
STATES
(704-27)
193
5431

FIG. 7A

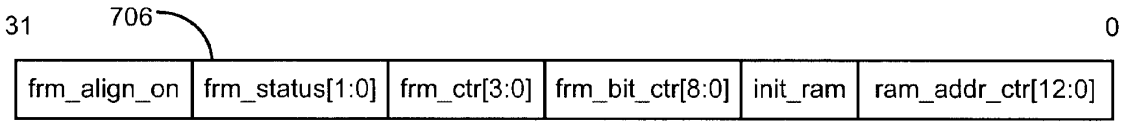
31
706
0
frm_align_on
frm_status[1:0]
frm_ctr[3:0]
frm_bit_ctr[8:0]
init_ram
ram_addr_ctr[12:0]

FIG. 7B

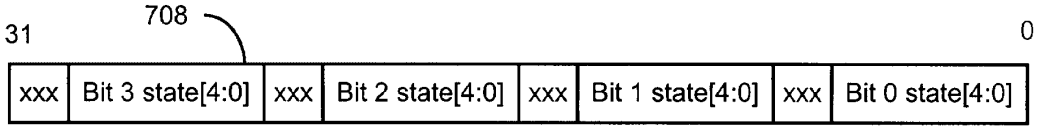
31
708
0
xxx
Bit 3 state[4:0]
xxx
Bit 2 state[4:0]
xxx
Bit 1 state[4:0]
xxx
Bit 0 state[4:0]

FIG. 7C

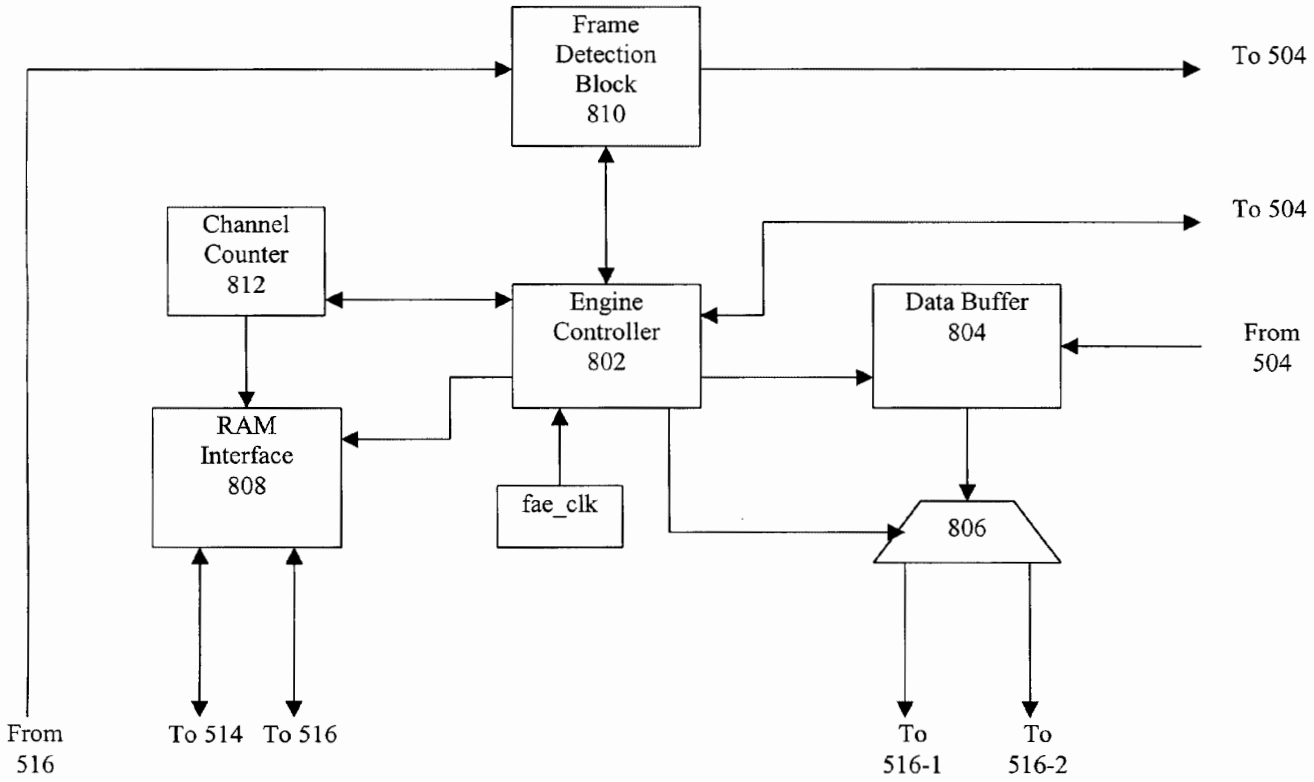
Frame
Detection
Block
810
To 504
To 504
Channel
Counter
812
Engine
Controller
802
Data Buffer
804
From
504
RAM
Interface
808
fae_clk
806
From
516
To 514
To 516
To
516-1
To
516-2

FIG. 8

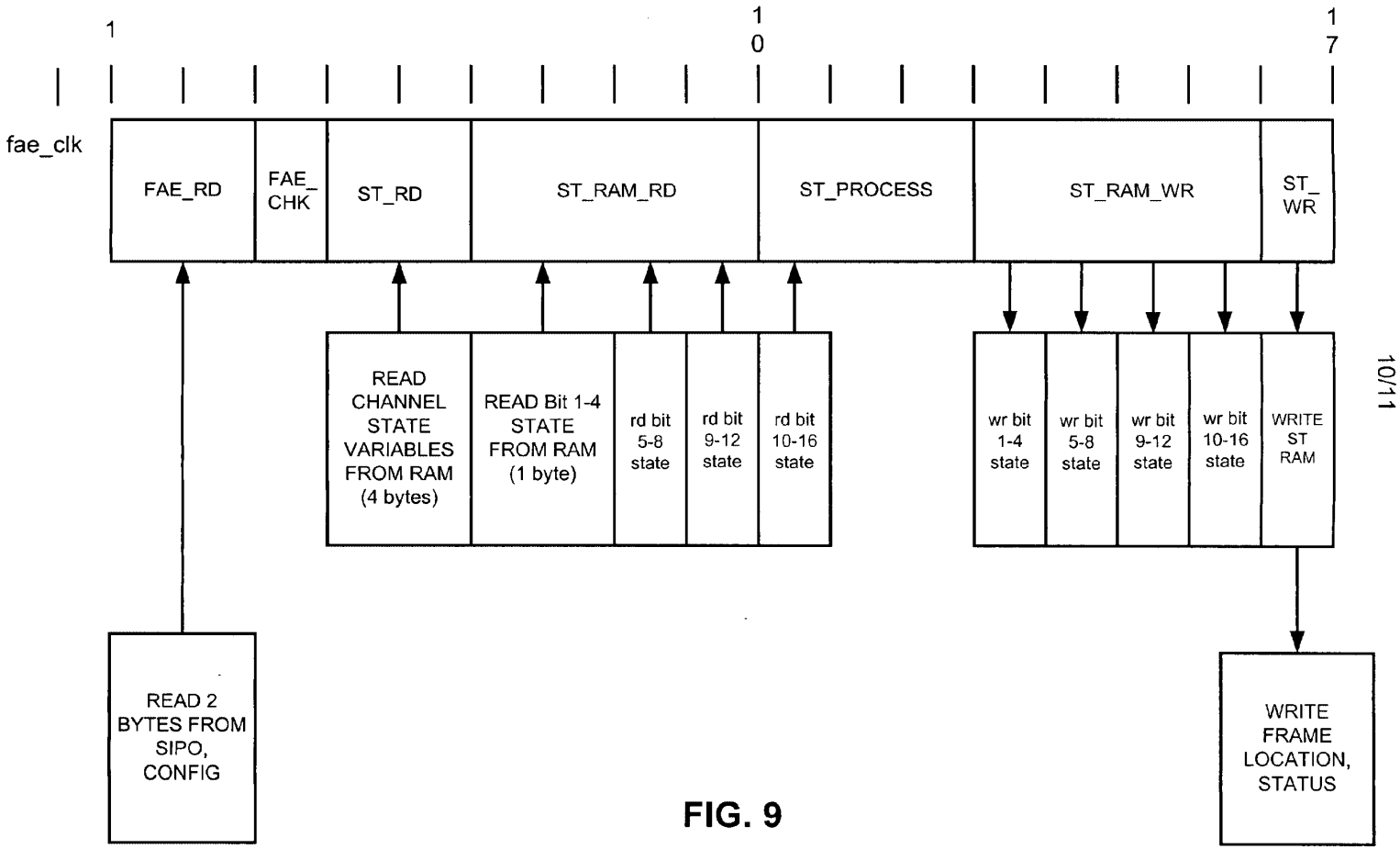
1
10
17
fae_clk
FAE_RD
FAE_ CHK
ST_RD
ST_RAM_RD
ST_PROCESS
ST_RAM_WR
ST_ WR
READ CHANNEL STATE VARIABLES FROM RAM (4 bytes)
READ Bit 1-4 STATE FROM RAM (1 byte)
rd bit 5-8 state
rd bit 9-12 state
rd bit 10-16 state
wr bit 1-4 state
wr bit 5-8 state
wr bit 9-12 state
wr bit 10-16 state
WRITE ST RAM
READ 2 BYTES FROM SIPO, CONFIG
WRITE FRAME LOCATION, STATUS

FIG. 9

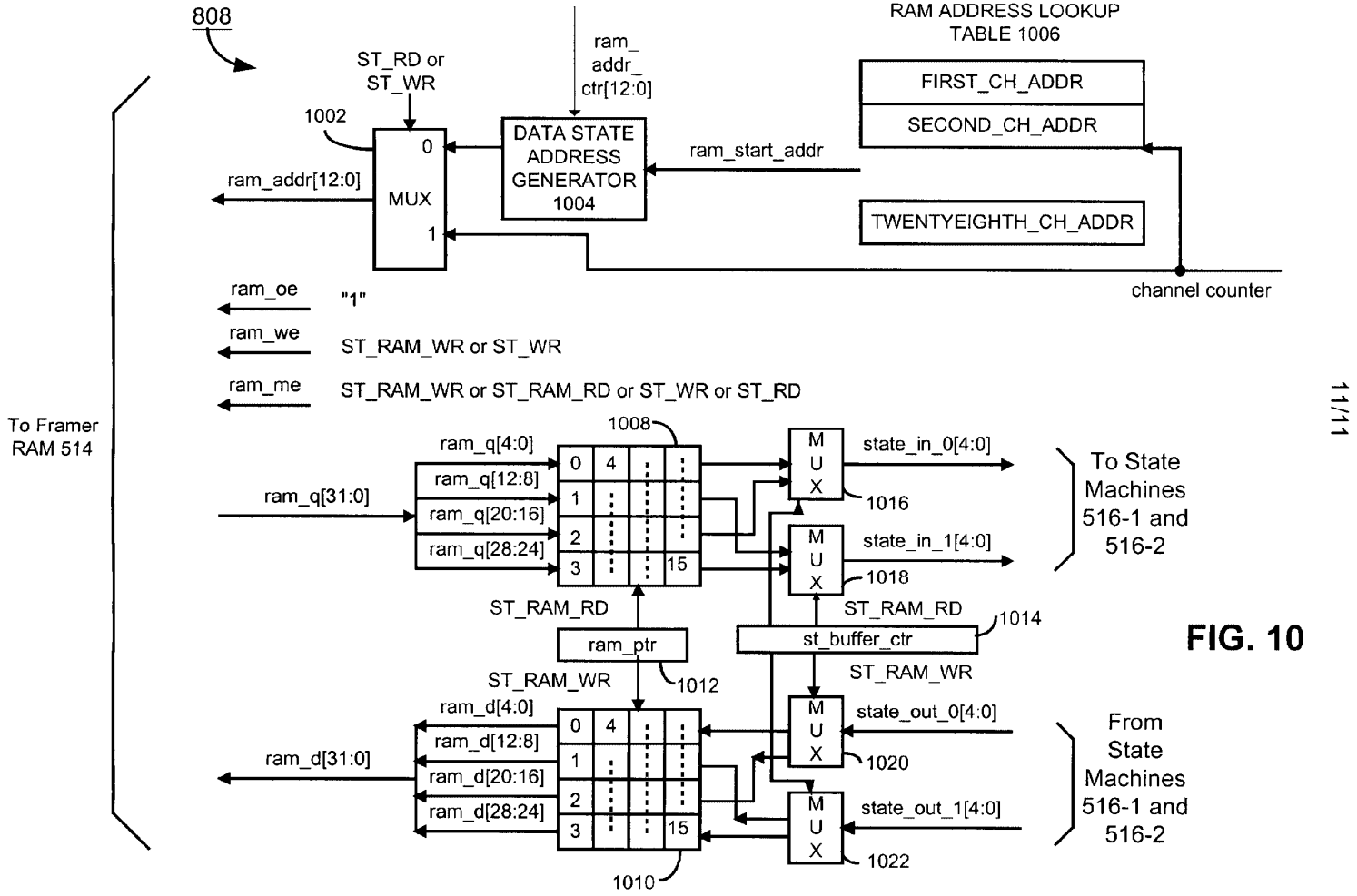

FIG. 10

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 February 2003 (27.02.2003)

PCT

(10) International Publication Number
WO 03/017283 A1

(51) International Patent Classification[7]: G11C 16/08, 8/06

(21) International Application Number: PCT/US02/25583

(22) International Filing Date: 13 August 2002 (13.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/928,621 13 August 2001 (13.08.2001) US

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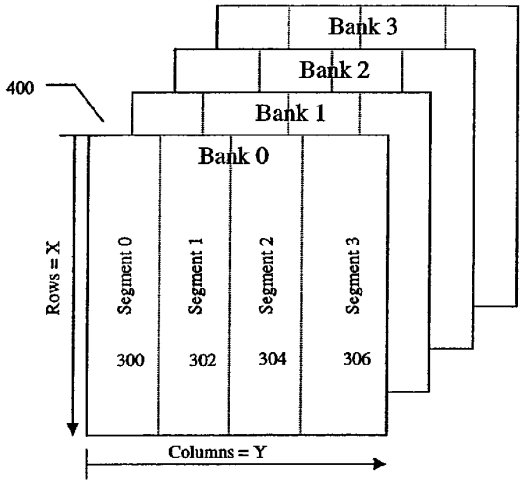
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: SYNCHRONOUS FLASH MEMORY WITH VIRTUAL SEGMENT ARCHITECTURE



(57) Abstract: An improved memory device and architecture has been detailed that enhances a Flash memory device that has an SDRAM compatible interface. The memory device employs a virtual paging scheme that allows the memory to have an efficient Flash internal structure, while logically re-mapping this architecture externally to a compatible virtual SDRAM architecture. This allows for access and operation of the improved memory device with a compatible SDRAM controller device, while Flash specific functions can be performed with an SDRAM command sequence. Internal to the memory, memory array banks are divided into four equal segments by row range and logically re-mapped by placing the segments virtually beside each other. This forms a virtual memory bank structure of equivalent rows and columns as a comparable SDRAM device. Additionally, the improved memory device may also have an extended interface that allows for direct access to the internal Flash memory architecture without logical abstraction.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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SYNCHRONOUS FLASH MEMORY WITH VIRTUAL SEGMENT ARCHITECTURE

Technical Field of the Invention

The present invention relates generally to non-volatile memory devices and in particular the present invention relates to synchronous non-volatile flash memory with virtual segment architecture.

Background of the Invention

Memory devices are typically provided as internal storage areas in the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. There are several different types of memory used in modern electronics, one common type is RAM (random-access memory). RAM is characteristically found in use as main memory in a computer environment. RAM refers to read and write memory; that is, you can both write data into RAM and read data from RAM. This is in contrast to ROM, which permits you only to read data. Most RAM is volatile, which means that it requires a steady flow of electricity to maintain its contents. As soon as the power is turned off, whatever data was in RAM is lost.

Computers almost always contain a small amount of read-only memory (ROM) that holds instructions for starting up the computer. Unlike RAM, ROM cannot be written to. An EEPROM (electrically erasable programmable read-only memory) is a special type non-volatile ROM that can be erased by exposing it to an electrical charge. Like other types of ROM, EEPROM is traditionally not as fast as RAM. EEPROM comprise a large number of memory cells having electrically isolated gates (floating gates). Data is stored in the memory cells in the form of charge on the floating gates. Charge is transported to or removed from the floating gates by programming and erase operations, respectively.

Yet another type of non-volatile memory is a Flash memory. A Flash memory is a type of EEPROM that can be erased and reprogrammed in blocks instead of one byte at a time. Many modern PCs have their BIOS stored on a flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a flash BIOS. Flash memory is also popular in modems because it enables the modem manufacturer to support new protocols as they become standardized.

A typical Flash memory comprises a memory array, which includes a large number of memory cells. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge in the floating gate.

Both RAM and ROM random access memory devices have memory cells that are typically arranged in an array of rows and columns. During operation, a row (page) is accessed and then memory cells can be randomly accessed on the page by providing column addresses. This access mode is referred to as page mode access. To read or write to multiple column locations on a page requires the external application of multiple column addresses. To increase access time, a burst mode access has been implemented. The burst mode uses an internal column address counter circuit to generate additional column addresses. The address counter begins at an externally provided address and advances in response to an external clock signal or a column address strobe signal.

A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ or 133 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. An extended form of SDRAM that can transfer a data value on the rising and falling edge of the clock signal is called double data rate SDRAM (DDR SDRAM, or simply, DDR). SDRAM's can be accessed quickly, but are volatile. Many computer systems are designed to operate using SDRAM, but would benefit from non-volatile memory. A synchronous Flash memory has been designed that allows for a non-volatile memory device with an SDRAM interface. Although knowledge of the function and internal structure of a synchronous Flash memory is not essential to understanding the present invention, a detailed discussion is included in United States Patent Application Serial No. 09/627,682 filed July 28, 2000 and titled, "Synchronous Flash Memory," which is commonly assigned and incorporated by reference.

In general, the goal of synchronous Flash is to mimic the architecture of SDRAM. It has an SDRAM interface which is compatible to SDRAM for read operation to the synchronous Flash memory. Programming, erasing, block protection and other flash specific

function differ from SDRAM and are performed with a three cycle SDRAM command sequence. Unfortunately, the general internal architecture of conventional SDRAM memory is not the most efficient architecture for non-volatile memories and for Flash memory specifically.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a non-volatile memory device that can operate in a manner similar to SDRAM operation and maintain an internal architecture that is more applicable to non-volatile memory device access and power efficiencies.

Summary of the Invention

The above-mentioned problems with memory devices and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

In one embodiment, a synchronous flash memory device comprises a first memory array with a first memory array dimensionality, a control circuit, and a synchronous memory interface, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality.

In another embodiment, a synchronous non-volatile memory device comprises a memory array with a plurality of array banks, each array bank having a first number of rows and a first number of columns, a control circuit, and a synchronous memory interface, wherein, for each array bank of the plurality of array banks, the control circuit logically adapts the first number of rows and the first number of columns to a second number of rows and a second number of columns.

In a further embodiment, a synchronous flash memory device comprises a first memory array with a first memory array dimensionality, a control circuit, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality, and a synchronous memory interface. Wherein the synchronous memory interface comprises, an address interface, a data interface, and a control interface.

In yet another embodiment, a synchronous flash memory device comprises a first memory array with a plurality of array banks, each having a first row dimension and a first column dimension, a control circuit, wherein the control circuit logically adapts the first row

dimension and the first column dimension of each of the plurality of banks to a second row dimension and a second column dimension, and a synchronous memory interface. Wherein the synchronous memory interface comprises, an address interface, an extended address interface, a data interface, and a control interface.

A method of operating a synchronous flash memory device comprises dividing a memory array with a first memory array dimensionality into a plurality of sections, and logically adapting the plurality of sections of the memory array to form an emulated virtual second memory array dimensionality.

Another method of operating a synchronous flash memory device comprises dividing a memory array with a first memory array dimensionality into a plurality of array banks, dividing each array bank of the plurality of array banks into a plurality of segments, logically adapting the plurality of array banks and plurality of segments of the first memory array dimensionality of the memory array to form an emulated virtual second memory array dimensionality, wherein accessing the emulated virtual second memory array dimensionality occurs through a synchronous memory interface, and allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface.

In yet another method of logically mapping a synchronous non-volatile memory device comprises forming a first memory array with a first plurality of banks, dividing each bank of the first plurality of banks into a plurality of segments, and logically mapping the plurality of segments to appear as a second memory array with a second plurality of segments.

In a further embodiment, a synchronous flash memory device comprises a memory array with a first set of four array banks, such that each array bank has a first number of rows and a first number of columns and each array bank is divided into four segments by row range, a latch circuit, a control circuit, and an SDRAM compatible synchronous memory interface. Wherein the control circuit logically maps the latch circuit and the four segments in each of the four array banks to appear as an emulated virtual SDRAM memory device of an equal memory size with a second virtual set of four array banks, such that the first number of rows and the first number of columns of each array bank of the memory array map to a second number of rows, that is one fourth the first number of rows, and a second number of

columns, that is four times the first number of columns, of the second virtual set of four array banks of the emulated virtual SDRAM memory device.

In another method of making a synchronous flash memory device comprises forming a non-volatile memory array with a plurality of array banks, each array bank having a first number of rows and a first number of columns, forming a control circuit, and forming a synchronous interface, wherein the control circuit logically adapts the first number of rows and the first number of columns of each array bank of the plurality of array banks to a second number of rows and a second number of columns.

In another embodiment, a system comprises a synchronous memory controller, and a synchronous flash memory device. Wherein the synchronous flash memory device comprises, a memory array with a first memory array dimensionality, a control circuit, and a synchronous memory interface, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality.

Brief Description of the Drawings

Figure 1 illustrates a prior art SDRAM memory array with four banks of memory within the array.

Figure 2 illustrates a virtual synchronous flash memory array of the present invention with four banks of memory within the array.

Figures 3 and 4 illustrate a virtual synchronous Flash memory array of the present invention subdivided into segments and the segments being mapped into a virtual SDRAM memory array.

Figure 5 illustrates a block diagram example of a 4Mx32 virtual synchronous Flash memory, showing address, control and data interfaces.

Figure 6 is a diagram of a memory address for a virtual synchronous Flash, showing bank address, additional virtual synchronous Flash addresses, row address, and column address.

Figure 7 illustrates a bank of virtual synchronous Flash memory array of the present invention showing mapping of a segment to other segment positions within the bank.

Figure 8 is a block diagram of a virtual synchronous Flash memory device coupled to an external processor.

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Detailed Description of the Invention

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

A conventional synchronous Flash memory matches the internal architecture and simulates the operation of an SDRAM memory quite closely. In contrast, a virtual synchronous flash memory of the present invention changes the internal architecture, while maintaining a compatible conventional SDRAM interface. This allows it to better match the efficiencies of the underlying memory technology. The resulting memory structure of a virtual synchronous Flash internal memory array is then logically reassembled to simulate an SDRAM configuration for the purposes of interfacing to a standard SDRAM compatible memory controller, processor, or other compatible external device. The virtual synchronous Flash memory of the present invention allows for additional memory address pins to be added to the external address interface so as to enable external devices with the appropriate capability to access the internal architecture of the virtual synchronous Flash memory directly.

Figure 1 is a simplified diagram of a prior art SDRAM memory array architecture. SDRAM memory arrays generally consist of a sequence of memory array banks that have rows and columns. The SDRAM memory arrays, upon being accessed with a bank, row, and column address, load an internal data latch circuit with a defined number of bits. The SDRAM memory array 100 of Figure 1 has four array banks 102, 104, 106, and 108. Each of the four banks 102, 104, 106, and 108 in turn has X rows 110 and Y columns 112. When a bank and row are selected by an input row address, the contents of a row of memory cells are placed on column bit lines coupled to sense amplifiers (not shown) and the bit values of the memory cells are detected. The selected memory array row, and therefore the contents of the

sense amplifiers, is generally called the active row page. The values detected by the sense amplifiers are latched in latch circuit 114. An input column address to the SDRAM, which defines the column page, selects from the latches of the latch circuit 114, and thus from the columns of the active row page, the Z number of bit values to be latched by an internal data buffer (not shown). The Z data bits are held in the internal data buffer for transfer from the SDRAM memory device through the data interface (not shown). An example of a common SDRAM memory is a 4Mx32 SDRAM, which has 4 banks, 4,096 rows, 256 columns, and 32 bits. However, SDRAM memories come in multiple densities and bus widths, for example 8Mx8, 4Mx16, 4Mx32, 2Mx32, and 8Mx16 to list a few.

An SDRAM memory read operation generally starts with an "ACTIVE" command that sets the bank and row address, by reading in an address placed on the address interface to the SDRAM memory device. The "ACTIVE" command thus activates the active row page and places it on the internal sense amplifiers to be read and latched by internal latch circuits. The column address is read in from the address interface by a following "READ" command that sets the column page by selecting columns from the latch circuits to place in an internal data buffer in the SDRAM memory device. The SDRAM command sequence is then finished on the next clock cycle with a data word transfer from the internal data buffer.

In an SDRAM compatible command sequence, before any READ or WRITE commands can be issued to a bank within the synchronous flash memory, a row in that bank must be "opened." This is accomplished via an ACTIVE command, which is used to open (or activate) a row in a particular array bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A11 selects the row. This row remains active for accesses until the next ACTIVE command, power-down or RESET.

A subsequent ACTIVE command to a different row in the same bank can be issued without having to close a previous active row, provided the minimum time interval between successive ACTIVE commands to the same bank is met. A subsequent ACTIVE command to another bank can also be issued while the first bank is being accessed, which results in a reduction of total row access overhead.

After an ACTIVE command to activate a row in the memory, the READ command is used to initiate a read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column

location. Read data appears on data outputs, the DQs (not shown) of the data interface (not shown) subject to the logic level on the data mask (DQM) input that is sometimes used to mask data DQ outputs and values not needed for the current memory access operation.

During READ bursts, the valid data-out element from the starting column address is available following a specified latency after the READ command. In SDRAM compatible memory, each subsequent data-out element is valid by the next positive clock edge. Upon completion of a burst, assuming no other commands have been initiated, all data outputs go as to a high impedance state. A full page burst continues until terminated. (At the end of the page, it wraps to column 0 and continue.) Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst, or the last desired data element of a longer burst that is being truncated. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed, random read accesses within a page can be performed, or each subsequent READ may be performed to a different bank.

A fixed-length or full-page READ burst can be truncated with either ACTIVE TERMINATE (may or may not be bank specific) or BURST TERMINATE (not bank specific) commands. Data from any READ burst may also be truncated with a subsequent WRITE command (WRITE commands must be preceded by WRITE SETUP), and data from a fixed-length READ burst may be immediately followed by data from a subsequent WRITE command (subject to bus turnaround limitations). The WRITE may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided.

As stated above, a virtual synchronous flash memory of the present invention changes the internal architecture, while maintaining a compatible conventional SDRAM interface. This allows it to better match the efficiencies of the underlying memory technology. Figure 2 details a simplified diagram of a memory array of a virtual synchronous Flash of the present invention. The resulting memory structure of a virtual synchronous Flash internal memory array is then logically reassembled to simulate an SDRAM configuration for the purposes of interfacing to a standard SDRAM compatible memory controller, processor, or other compatible external device. The virtual synchronous Flash

memory of the present invention allows for additional memory address pins to be added to the external address interface so as to enable external devices with the appropriate capability to access the internal architecture of the virtual synchronous Flash memory directly.

To accomplish this goal, the virtual synchronous Flash memory of the present invention internally reduces the effective column length of a memory array bank to one-fourth the column length of a corresponding SDRAM memory device. In addition, the number of rows of a memory array bank is increased to four times the number of rows of a corresponding SDRAM memory device, maintaining the same overall memory density. It is noted that other internal memory array configurations are possible and would be apparent to those skilled in the art.

The virtual synchronous Flash memory array 200 of Figure 2 is shown with four array banks 202, 204, 206, and 208. Each of the four banks 202, 204, 206, and 208 in the memory array in turn has 4(X) rows 210 and Y/4 columns 212. When a bank and row are selected by an input row address, the contents of a row of memory cells is placed on column bit lines coupled to sense amplifiers (not shown) and the bit values of the memory cells are detected. The selected memory array row, and contents of the sense amplifiers, is called the active row page. The values detected by the sense amplifiers are latched in by latch circuit 214. An input column address to the virtual synchronous Flash, which defines the column page, selects from the latches of the latch circuit 214, and thus from the columns of the active row page, the Z number of bit values to be latched by an internal data buffer (not shown). The Z data bits are held in the internal data buffer for transfer from the virtual synchronous Flash memory device through the data interface (not shown). From the above example, a 4Mx32 SDRAM, which has 4 banks, 4,096 rows, 256 columns, and 32 bits, would correspond to a 4Mx32 virtual synchronous Flash that internally has 4 banks, 16,384 rows, 64 columns, and 32 bits.

A process for logically reassembling the internal rows and columns of the virtual synchronous Flash of Figure 2 to map to a comparable conventional SDRAM configuration is shown in Figures 3 and 4. In Figure 3, each of the four banks 308, 310, 312, and 314 of the internal memory array 316 of the virtual synchronous Flash of Figure 2, which has 4(X) rows and Y/4 columns, is shown in Figure 3. As detailed in Figure 2, each of the virtual synchronous Flash internal memory array banks is divided by row range into four segments 300, 302, 304, and 306. The number of rows in each separate segment of Figure 3 is equal to

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the overall X number of rows in the SDRAM that the virtual synchronous Flash is compatible with. The segments 300, 302, 304, and 306 of each separate bank of the virtual synchronous Flash are then logically mapped by arranging them in a virtual manner side by side into a corresponding virtual memory bank 400 that is X rows long and Y columns wide, as shown in Figure 4, matching a corresponding compatible SDRAM device. It is noted that other methods of logically mapping a virtual synchronous Flash memory to match an SDRAM are possible and would be apparent to those skilled in the art with the benefit of the present disclosure.

In the example previously given of a 4Mx32 memory device, a 4Mx32 virtual synchronous Flash using the technique of Figures 3 and 4 internally has 4 banks, 16,384 rows, 64 columns, and 32 bits. Each bank is logically divided into 4 segments of 4,096 rows and 64 columns each. The segments of each bank are logically mapped to form a virtual bank of 4,096 rows and 256 columns. This procedure can be used on each bank to allow the 4Mx32 virtual synchronous Flash to simulate a 4Mx32 synchronous SDRAM compatible memory device, which has 4 banks, 4,096 rows, 256 columns, and 32 bits.

Figure 5 is a simplified external diagram of a 4Mx32 virtual synchronous Flash memory device 500 of an embodiment of the present invention, showing external connections, major interfaces, and extended virtual synchronous Flash address lines. The virtual synchronous Flash memory device 500 of Figure 5 includes bank address lines BA0-BA1 502, address lines A0-A15 504, data interface 506, and control line interface 508. The bank address lines BA0-BA1 502 select the desired memory array bank for a subsequent access. The data interface 506 transfers data to and from the virtual synchronous Flash memory device 500. The control line interface 508 contains the signal lines necessary to control the virtual synchronous Flash memory device 500 in its operation, such as, but not limited to, CS, DQS, clock, CAS, RAS, and WE. Depending on the SDRAM command being issued the values placed on the address lines A0-A15 504 select the row or column of the memory array for an access. The address lines A0-A15 are additionally split into two separate subsections, A0-A11 510 and A12-A15 512. The addresses in subsection A0-A11 510 allow standard SDRAM compatible row and column memory address accesses to the virtual synchronous Flash memory device 500. The additional address lines in subsection A12-A15 512 are not necessary for SDRAM compatible memory access, but if used by an extended capability SDRAM control device, address lines A12-A15 512 allow access to

extended virtual synchronous Flash capabilities and internal architecture. The virtual synchronous Flash uses address lines A12-A13 for access to the extended internal Flash memory array row addresses. Address lines A14-A15 are used to set the extended internal Flash memory array segment address.

A virtual synchronous Flash of the present invention is compatible with conventional SDRAM interfaces and commands, such as detailed above. In addition, virtual synchronous Flash supports extended operations to allow Flash specific operations and to allow direct access to the extended rows and columns of the internal memory array architecture. Direct access to the extended rows and columns without logical re-mapping of the rows and columns to a compatible SDRAM configuration is enabled by the additional address interface lines optionally fitted to the virtual synchronous Flash memory device, such as A12-A15 512 of Figure 5.

An example of a virtual synchronous Flash address space 600 is shown in Figure 6. The virtual synchronous Flash address space of Figure 6 matches the address space of the SDRAM it is compatible with and contains a row address 606, a column address 608, a word address 610, and bank address 612. In addition, the virtual synchronous Flash address space 600 contains extended addresses for segment addressing 602 and row addressing 604 that allow for the direct access of the virtual synchronous Flash without logical mapping by compatible host controllers.

In the example 4Mx32 virtual synchronous Flash of Figure 5, address lines A12-A13 are used for extended row accesses into four times as many physical rows (16,384 rows) that a virtual synchronous Flash has as compared to a compatible conventional 4Mx32 SDRAM (4,096 rows). Address lines A14-A15 are used for selecting which segment section of four (i.e., 300, 302, 304, and 306 of Figure 3) of the virtual synchronous Flash's currently active memory array bank (i.e., 308 of Figure 3) are accessed in the operation.

A virtual synchronous Flash memory device's capability to set its segment address allows for full segment association within the bank as shown in Figure 7. In Figure 7 is shown a bank of virtual synchronous Flash memory 700 with four segments 702, 704, 706, and 708 that has been logically re-mapped to an SDRAM configuration. A row of the segment zero 710 is shown being logically repositioned by an access that includes an extended virtual synchronous Flash segment address to appear as if it was placed in one of the other three segments of the current memory bank (segment one 712, segment two 714, or

segment three 716). The ability of full segment association allows any row selected in a bank to be addressed to any of the four segments in that bank. This has the effect of logically shifting the address space by that number of segments for a subsequent memory access.

In operation, a virtual synchronous Flash memory reduces the active page of the internal memory array bank by one-fourth. This reduces the number of sense amplifiers activating by one-fourth, saving power and complexity. In the example 4Mx32 virtual synchronous Flash, the memory device only activates 2K sense amplifiers versus 8K sense amplifiers for an SDRAM or synchronous Flash memory device. In addition, because sixteen segments are available for the virtual synchronous Flash memory device versus four segments for an SDRAM, when each of the four banks has their respective four segments activated, there is a higher hit rate for READs without activating new rows. The increased granularity of a virtual synchronous Flash memory device decreases power usage, and in addition, decreases memory access latency. Therefore effectively increasing bandwidth to the virtual synchronous Flash over that of a conventional synchronous Flash component.

Figure 8 shows an illustration of a virtual synchronous Flash memory system, wherein a 4Mx32 virtual synchronous Flash memory device 800 of an embodiment of the present invention is coupled to an external processor 802. It is noted that the virtual synchronous Flash memory system of Figure 8 is only shown as an example, and other systems and embodiments of the present invention can include multiple types of other integrated circuits (i.e., a memory controller, a field programmable gate array (FPGA), a volatile memory device, an application specific integrated circuit (ASIC), etc.). Systems containing memory devices are well known in the prior art and the following description is intended only to be an overview of their operation and provide an example of their operation with an embodiment of the present invention.

In the system of Figure 8, address values for the virtual synchronous Flash memory 800 are received from the processor 802 on the external address bus connections 804 and bank address lines 806. The received address values are stored internal to the memory device and utilized to select the memory cells in the internal memory array (not shown). In a conventional SDRAM compatible operation, the processor 802, with an ACTIVE command, inputs a row and bank address on address lines A0-A11 808 and bank address lines BA0 and BA1 806 activating an internal virtual row page (not shown) in the virtual synchronous Flash memory device 800. The row and bank address is followed by a READ command with a

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column address placed on address lines A0-A8 (a subset of address lines A0-A11 808) by the processor 802. Internal to the virtual synchronous Flash memory device 800, data values from the bank segments (not shown) are captured in latch circuits, logically re-mapped to form an SDRAM compatible data format, and readied for transfer from the virtual synchronous Flash memory device 800. Data transfer from the virtual synchronous Flash memory device 800 begins on the following clock cycle received and transmitted on the bi-directional data word interface 810 to the processor 802. Control of the virtual synchronous Flash memory device 800 for operations is actuated by the internal control circuitry (not shown). The control circuitry operates in response external control signals received from the processor 802 on control signal external interface connections 820 and to internal events.

Extended access to the virtual synchronous Flash memory device 800 is accomplished utilizing the extended virtual synchronous Flash address lines, A12-A15 814. The processor 802, with an ACTIVE command, inputs a row on address lines A0-A11 808, extended row and segment address lines A12-A15 814, and bank address lines BA0 and BA1 806. The ACTIVE command directly activates a bank and internal row page and/or segment of the internal memory array (not shown) in the virtual synchronous Flash memory device 800 for further operations. The row, extended row, and bank address is followed by a READ command with a column address placed on address lines A0-A8 (a subset of address lines A0-A15 804) by the processor 802. Internal to the virtual synchronous Flash memory device 800, data values from the bank segments (not shown) are readied for transfer from the virtual synchronous Flash memory device 800 by being copied into internal latch circuits (not shown). Data transfer from or to the virtual synchronous Flash memory device 800 begins on the following clock cycle received and transmitted on the bi-directional data word interface 810 to the processor 802. Control of the virtual synchronous Flash memory device 800 for operations is actuated by the internal control circuitry (not shown). The control circuitry operates in response external control signals received from the processor 802 on control signal external interface connections 820 and to internal events.

Conclusion

An improved memory device and architecture has been detailed that enhances a Flash memory device that has an SDRAM compatible READ interface. The memory device employs a virtual paging scheme that allows for the architecture of the memory to implement

an efficient Flash memory structure internally. Externally, the memory logically maps the internal Flash architecture to an SDRAM compatible interface and virtual architecture, allowing for memory access and operation with a compatible SDRAM controller device. Programming, erasing, block protection, and other Flash specific functions differ from SDRAM and are performed with an SDRAM command sequence.

In one embodiment, a memory device has four times as many rows in a memory array bank as a comparable SDRAM device, but only one fourth as many columns. This reduces the number of sense amplifiers activating, therefore saving power and complexity in the memory device. Internal to the memory, memory array banks are divided into four equal segments by row range and logically re-mapped by placing the segments virtually beside each other. This logically re-mapped memory bank forming a virtual memory bank structure of equivalent rows and columns as the comparable SDRAM device.

In another embodiment, a memory device with an extended memory interface with additional address lines was detailed, allowing for direct access to the internal Flash memory architecture without the abstraction of logical re-mapping the internal memory array. Additionally, the extended interface allows for full bank association and mapping of a segment row of an activated virtual row page to any segment of the bank for a subsequent memory access.

More segments are available for the memory device versus a comparable SDRAM. Therefore, a memory has a higher hit rate for READs without necessitating activation of further new rows. This increases the memory array granularity and has the effect of decreasing power and latency. The improved latency effectively increases the available bandwidth of the memory device.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

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What is claimed is:

1. A synchronous flash memory device comprising:
a first memory array with a first memory array dimensionality;
a control circuit; and
a synchronous memory interface, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality.

2. The synchronous flash memory device of claim 1, wherein the memory array further comprises a plurality of array banks.

3. The synchronous flash memory device of claim 2, wherein the plurality of array banks each have a first row dimension and a first column dimension.

4. The synchronous flash memory device of claim 3, wherein the control circuit logically adapts the first row dimension and the first column dimension of each array bank to a second row dimension and a second column dimension.

5. The synchronous flash memory device of claim 4, wherein the second row dimension and the second column dimension are the same as a SDRAM memory device or a DDR memory device.

6. The synchronous flash memory device of claim 2, wherein each array bank of the plurality of array banks further comprise a plurality of segments.

7. The synchronous flash memory device of claim 6, wherein each array bank of the plurality of array banks comprise four segments.

8. The synchronous flash memory device of claim 1, wherein the synchronous memory interface further comprises one of a SDRAM or a DDR compatible interface.

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9. A synchronous non-volatile memory device comprising:
a memory array with a plurality of array banks, each array bank having a first number of rows and a first number of columns;
a control circuit; and
a synchronous memory interface, wherein, for each array bank of the plurality of array banks, the control circuit logically adapts the first number of rows and the first number of columns to a second number of rows and a second number of columns.

10. The synchronous flash memory device of claim 9, wherein the plurality of array banks equal four array banks.

11. The synchronous flash memory device of claim 9, wherein each array bank of the plurality of array banks further comprise a plurality of segments.

12. The synchronous flash memory device of claim 11, wherein the plurality of segments are divided by a row range.

13. The synchronous flash memory device of claim 11, wherein each array bank of the plurality of array banks comprises four segments.

14. The synchronous flash memory device of claim 9, wherein the second number of rows and the second number of columns matches that of a SDRAM or a DDR memory.

15. A synchronous flash memory device comprising:
a first memory array with a first memory array dimensionality;
a control circuit, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality; and
a synchronous memory interface, wherein the synchronous memory interface comprises,
an address interface,
a data interface, and
a control interface.

16. The synchronous flash memory device of claim 15, wherein the address interface further comprises an extended address interface, wherein the extended address interface allows extended access to the synchronous flash memory device.

17. The synchronous flash memory device of claim 16, wherein the extended address interface further allows access to the first memory dimensionality.

18. A synchronous flash memory device comprising:
a first memory array with a plurality of array banks, each having a first row dimension and a first column dimension;
a control circuit, wherein the control circuit logically adapts the first row dimension and the first column dimension of each of the plurality of banks to a second row dimension and a second column dimension; and
a synchronous memory interface, wherein the synchronous memory interface comprises,

an address interface,
an extended address interface,
a data interface, and
a control interface.

19. The synchronous flash memory device of claim 18, wherein the extended address interface further allows access to the first row dimension.

20. The synchronous flash memory device of claim 18, wherein the extended address interface further allows access to the first column dimension.

21. The synchronous flash memory device of claim 18 wherein the extended address interface further comprises an additional address interface to the first row dimension of the synchronous flash memory device.

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22. The synchronous flash memory device of claim 21, wherein the additional address interface has two address lines for access into the first row dimension of the synchronous flash memory device.

23. The synchronous flash memory device of claim 18, wherein the plurality of array banks further comprise a plurality of segments, and wherein the extended address interface further comprises an additional address interface to select a segment of an active bank of the synchronous flash memory device.

24. The synchronous flash memory device of claim 23, wherein the additional address interface has two address lines for selection of the segment of the active bank of the synchronous flash memory device.

25. The synchronous flash memory device of claim 23, wherein the additional address interface allows associating an active row of a selected segment with any other segment in the active bank of the synchronous flash memory device.

26. A method of operating a synchronous flash memory device comprising:
dividing a memory array with a first memory array dimensionality into a plurality of sections; and
logically adapting the plurality of sections of the memory array to form an emulated virtual second memory array dimensionality.

27. The method of claim 26, wherein dividing the memory array into a plurality of sections further comprises dividing the memory array into a plurality of array banks.

28. The method of claim 27, wherein dividing the memory array into the plurality of array banks further comprises dividing the memory array into a plurality of array banks such that the array banks have a first row dimension and a first column dimension.

29. The method of claim 28, wherein logically adapting the plurality of sections of the

memory array to form the emulated virtual second memory array dimensionality further comprise logically adapting the first row dimension and the first column dimension of each array bank to a second row dimension and a second column dimension.

30. The method of claim 29, wherein the second row dimension and the second column dimension of each array bank of the plurality of array banks are the same as a SDRAM memory device or a DDR memory device.

31. The method of claim 27, wherein dividing the memory array into the plurality of array banks further comprises dividing each array bank into a plurality of segments.

32. The method of claim 26, further comprising coupling to one of a SDRAM or a DDR compatible interface.

33. A method of operating a synchronous flash memory device comprising:
dividing a memory array with a first memory array dimensionality into a plurality of array banks;
dividing each array bank of the plurality of array banks into a plurality of segments;
logically adapting the plurality of array banks and plurality of segments of the first memory array dimensionality of the memory array to form an emulated virtual second memory array dimensionality, wherein accessing the emulated virtual second memory array dimensionality occurs through a synchronous memory interface; and
allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface.

34. The method of claim 33, wherein the extended interface is an extended address interface.

35. The method of claim 33, wherein the extended interface operates in conjunction with the synchronous memory interface.

36. The method of claim 33, wherein the extended interface allows access to the first row dimension of each array bank.

37. The method of claim 36, wherein the extended interface allows extended access to the first column dimension of each array bank of the plurality of array banks.

38. The method of claim 34, wherein the extended address interface further comprises two address lines to allow access into the first row dimension of the synchronous flash memory device.

39. The method of claim 36, wherein the extended interface further comprises an additional address interface to allow selection of a segment of an active bank of the synchronous flash memory device.

40. The method of claim 39, wherein forming the additional address interface further comprises forming two address lines for selection of the segment of the active bank of the synchronous flash memory device.

41. The method of claim 39, wherein the additional address interface allows associating an active row of a selected segment with any other segment in the active bank of the synchronous flash memory device.

42. A method of logically mapping a synchronous non-volatile memory device comprising:
forming a first memory array with a first plurality of banks;
dividing each bank of the first plurality of banks into a plurality of segments; and
logically mapping the plurality of segments to appear as a second memory array with a second plurality of segments.

43. A synchronous flash memory device comprising:
a memory array with a first set of four array banks, such that each array bank has a

first number of rows and a first number of columns and each array bank is divided into four segments by row range;

a latch circuit;

a control circuit; and

an SDRAM compatible synchronous memory interface, wherein the control circuit logically maps the latch circuit and the four segments in each of the four array banks to appear as an emulated virtual SDRAM memory device of an equal memory size with a second virtual set of four array banks, such that the first number of rows and the first number of columns of each array bank of the memory array map to a second number of rows, that is one fourth the first number of rows, and a second number of columns, that is four times the first number of columns, of the second virtual set of four array banks of the emulated virtual SDRAM memory device.

44. A method of making a synchronous flash memory device comprising:

forming a non-volatile memory array with a plurality of array banks, each array bank having a first number of rows and a first number of columns;

forming a control circuit; and

forming a synchronous interface, wherein the control circuit logically adapts the first number of rows and the first number of columns of each array bank of the plurality of array banks to a second number of rows and a second number of columns.

45. A system comprising:

a synchronous memory controller; and

a synchronous flash memory device, wherein the synchronous flash memory device comprises,

a memory array with a first memory array dimensionality,

a control circuit, and

a synchronous memory interface, wherein the control circuit logically adapts the first memory array dimensionality to a second memory array dimensionality.

46. The system of claim 45, wherein the synchronous memory controller further

comprises one of a processor, an ASIC, or an FPGA.

47. The system of claim 45, wherein the synchronous memory controller further comprises a SDRAM or a DDR compatible controller.

48. The system of claim 45, wherein the synchronous memory controller further comprises an extended virtual synchronous Flash compatible controller.

49. The system of claim 45, wherein the synchronous memory controller further comprises an extended synchronous Flash compatible controller.

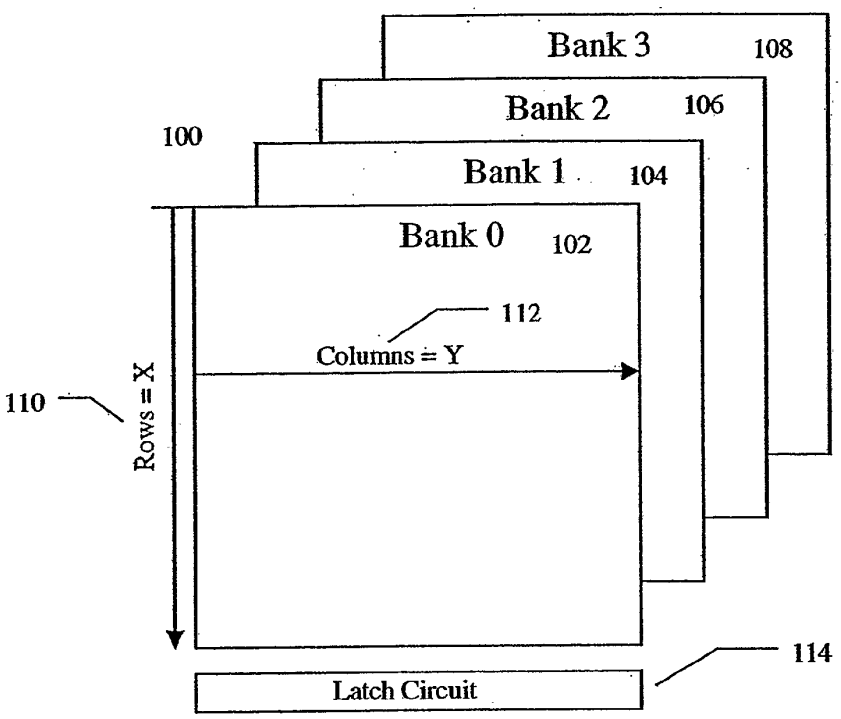

FIG. 1
Prior Art

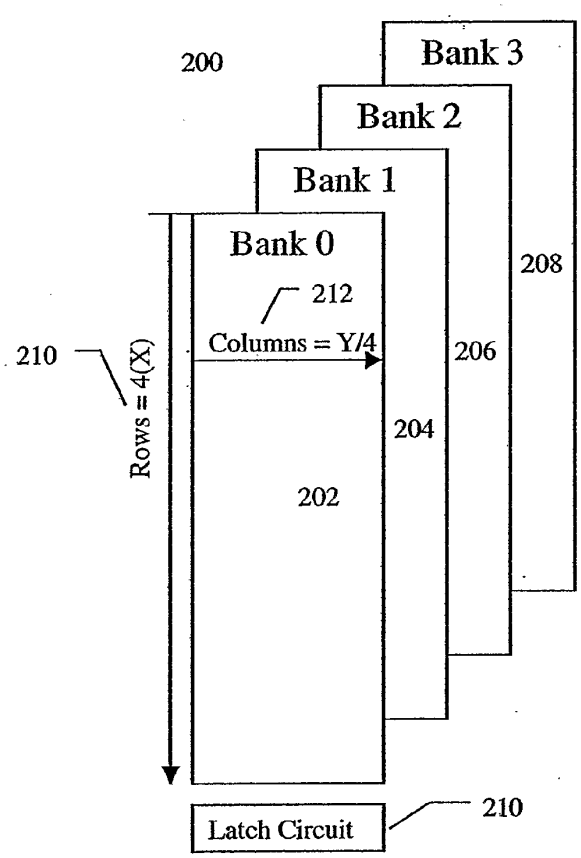
200
Bank 3
Bank 2
Bank 1
Bank 0
208
212
Columns = Y/4
210
206
Rows = 4(X)
204
202
210
Latch Circuit

FIG. 2

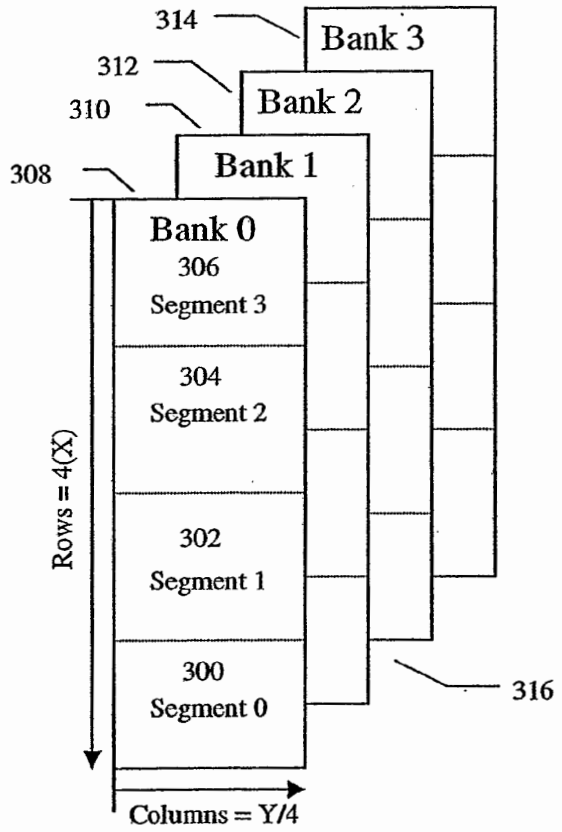
314
Bank 3
312
Bank 2
310
Bank 1
308
Bank 0
306
Segment 3
304
Segment 2
302
Segment 1
300
Segment 0
316
Rows = 4(X)
Columns = Y/4

FIG. 3

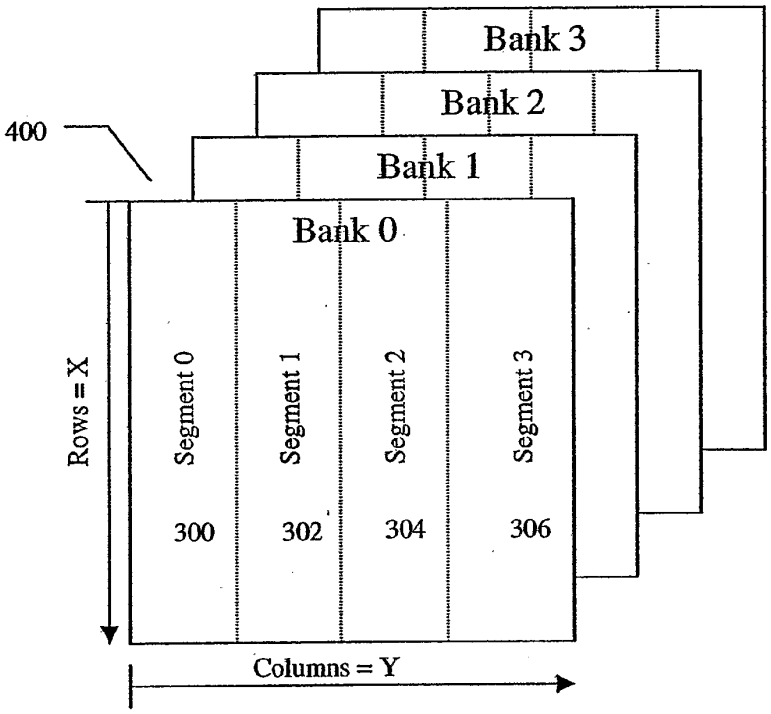
Bank 3
Bank 2
Bank 1
Bank 0
400
Rows = X
Segment 0
Segment 1
Segment 2
Segment 3
300
302
304
306
Columns = Y

FIG. 4

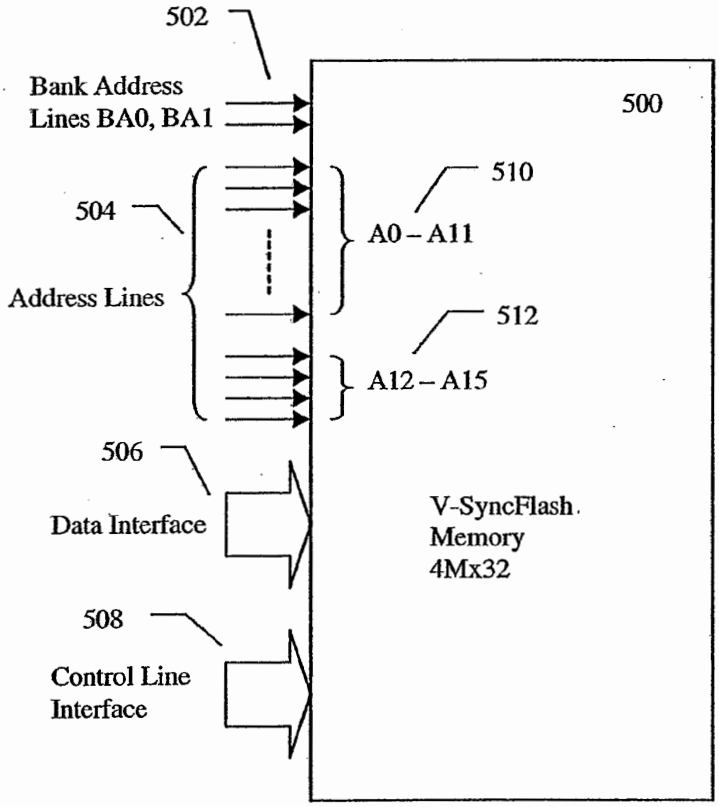
502
Bank Address
Lines BA0, BA1
500
510
504
A0 – A11
Address Lines
512
A12 – A15
506
Data Interface
V-SyncFlash
Memory
4Mx32
508
Control Line
Interface

FIG. 5

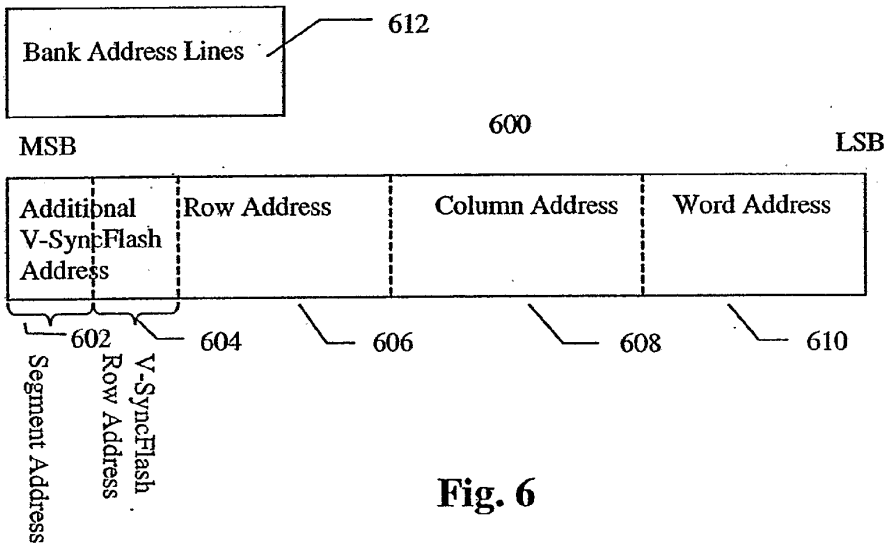
Bank Address Lines
612
600
MSB
LSB
Additional V-Sync Flash Address
Row Address
Column Address
Word Address
602
604
606
608
610
Segment Address
Row Address
V-SyncFlash

Fig. 6

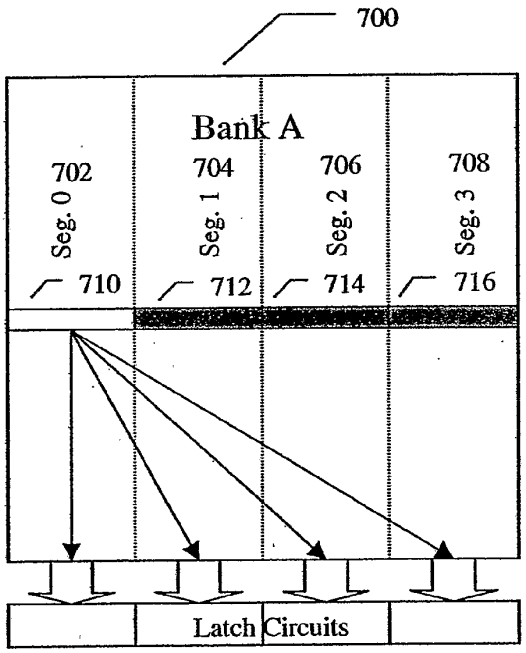
700
Bank A
702
Seg. 0
704
Seg. 1
706
Seg. 2
708
Seg. 3
710
712
714
716
Latch Circuits

FIG. 7

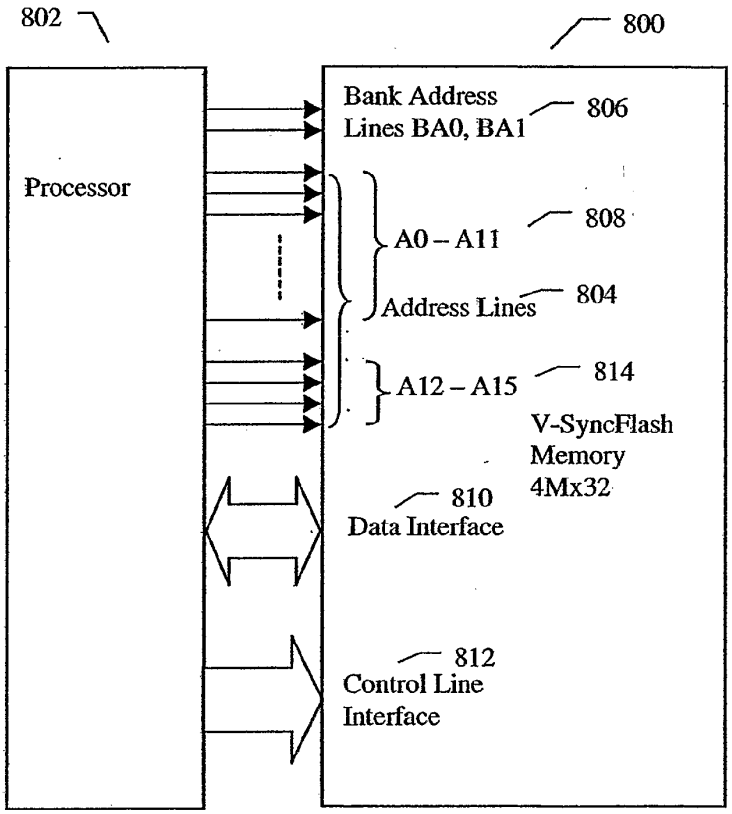
802
800
Processor
Bank Address
Lines BA0, BA1
806
A0 – A11
808
Address Lines
804
A12 – A15
814
V-SyncFlash
Memory
4Mx32
810
Data Interface
812
Control Line
Interface

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/25583

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C16/08 G11C8/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 246 626 B1 (ROOHPARVAR FRANKIE F) 12 June 2001 (2001-06-12) column 3, line 53 -column 9, line 25; figures 1A,19	1-49
X	EP 1 063 652 A (SILICON STORAGE TECH INC) 27 December 2000 (2000-12-27) abstract paragraph '0021! - paragraph '0022! figures 2-4	1-49
X	US 6 026 465 A (PASHLEY RICHARD D ET AL) 15 February 2000 (2000-02-15) abstract column 20, line 60 -column 29, line 17; figures 1,3,8,12,14,15	1-49

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 December 2002	17/12/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ríos Báez, A

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/25583

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 108 745 A (GUPTA ANURAG ET AL) 22 August 2000 (2000-08-22) abstract column 4, line 56 -column 5, line 18; figures 1,2,4,9	1-49
A	WO 00 67128 A (CENTENNIAL TECHNOLOGIES INC ;COLLINS LARRY (US); MERRY DAVID (US);) 9 November 2000 (2000-11-09) abstract page 2, line 20 - line 24 page 6, line 1 - line 16; claims 1,2; figures 1,2A,2B	1-49
A	US 5 732 029 A (SEOK YONG-SIK ET AL) 24 March 1998 (1998-03-24) column 1, line 15 - line 67	1-49
P,X	WO 01 75897 A (MICRON TECHNOLOGY INC) 11 October 2001 (2001-10-11) cited in the application figure 1	1-49

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 02/25583

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6246626 B1	12-06-2001	US 2002036941 A1	28-03-2002
EP 1063652 A	27-12-2000	EP 1063652 A2	27-12-2000
		JP 2001023382 A	26-01-2001
US 6026465 A	15-02-2000	US 5696917 A	09-12-1997
		AU 2765895 A	04-01-1996
		BR 9507911 A	12-08-1997
		EP 0765498 A2	02-04-1997
		WO 9534030 A2	14-12-1995
		US 6385688 B1	07-05-2002
US 6108745 A	22-08-2000	JP 11265315 A	28-09-1999
WO 0067128 A	09-11-2000	AU 4686900 A	17-11-2000
		EP 1210666 A1	05-06-2002
		WO 0067128 A1	09-11-2000
US 5732029 A	24-03-1998	KR 145222 B1	17-08-1998
		JP 2738526 B2	08-04-1998
		JP 8321200 A	03-12-1996
WO 0175897 A	11-10-2001	AU 4787101 A	15-10-2001
		AU 4968601 A	15-10-2001
		AU 4968701 A	15-10-2001
		AU 5112101 A	15-10-2001
		AU 5116801 A	15-10-2001
		AU 5116901 A	15-10-2001
		AU 5582501 A	15-10-2001
		AU 8929101 A	15-10-2001
		WO 0175895 A2	11-10-2001
		WO 0175896 A2	11-10-2001
		WO 0175890 A2	11-10-2001
		WO 0175897 A2	11-10-2001
		WO 0175898 A2	11-10-2001
		WO 0175892 A2	11-10-2001
		WO 0175623 A2	11-10-2001
		WO 0175893 A2	11-10-2001
		US 6314049 B1	06-11-2001

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 August 2003 (21.08.2003)

PCT

(10) International Publication Number
WO 03/069484 A2

(51) International Patent Classification[7]: G06F 13/00

(21) International Application Number: PCT/US03/02610

(22) International Filing Date: 29 January 2003 (29.01.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/073,740 11 February 2002 (11.02.2002) US

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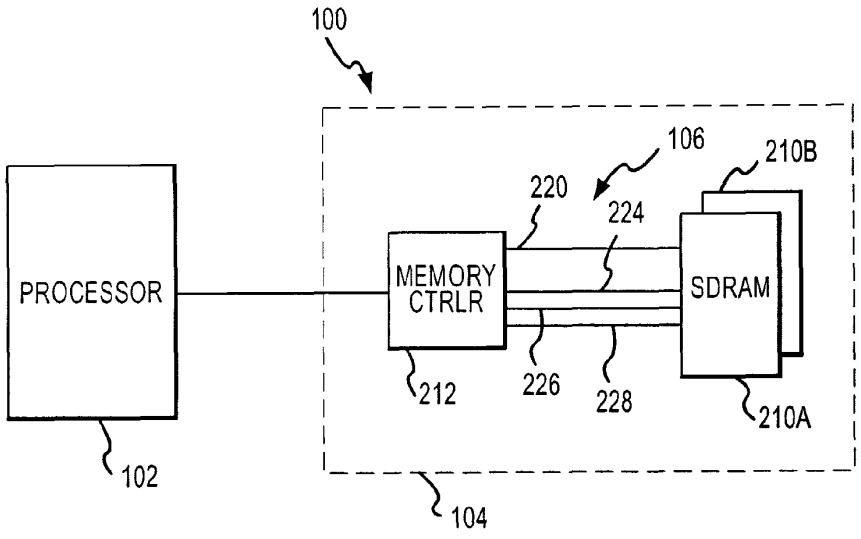
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND APPARATUS FOR SUPPLEMENTARY COMMAND BUS



(57) Abstract: An electronic system according to various aspects of the present invention includes a memory having a location-specific command interface and a general command interface. The memory communicates with other components in the system via a main command bus configured to transfer address-specific commands and a supplementary command bus configured to transfer general commands. Commands may be received by the memory simultaneously at the respective interfaces.

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METHOD AND APPARATUS FOR SUPPLEMENTARY COMMAND BUS

Field of Invention

The invention relates to integrated circuits and semiconductor systems, and more particularly, to accessing data.

Background of the Invention

Many electronic systems use memory to store information. Memory devices include an interface to communicate with other elements of the system. An ordinary interface provides several inputs and outputs, including various bus connections to accommodate multi-bit transfers in parallel. In particular, memory devices typically include a command bus and an address bus that transmit command and address information from a controller to the memory device.

For example, many existing DRAM devices include a command/address bus having three command signals, ordinarily row address strobe (RAS), column address strobe (CAS), and write enable (WE), and several address signals, including row/column address (A[X:0]), bank address (BA[1:0]), and chip select (CS). The command signals decode yielding several commands, such as ACTIVATE ROW, COLUMN SELECT with WRITE/READ, PRECHARGE ROW, PRECHARGE ALL, AUTO REFRESH, SELF REFRESH, WAKE, LOAD MODE, and LOAD EXTENDED MODE.

Certain access processes saturate the command/address bus, limiting the throughput/bandwidth of the memory device. For example, referring to Figure 9 illustrating a simplified memory access process, if the addressing patterns dictate all page misses, each burst transfer operation 900 of data to/from the memory devices requires one ACTIVATE command 910 for the row address 911 and one READ or WRITE command 912 corresponding to the column address data 913. Bank selection data is transferred via a bank selection bus 924. A PRECHARGE command 914 for the selected bank 915 is then asserted to close the selected bank. If the burst size does not allow time for three commands, however, the data transfer rate is throttled. A common example is a burst size of four data bus transfers 916A-D with the data bus 920 running at double the rate of the command/address bus 922. This is a simplified, illustrative example, for memory accesses typically utilize interleaved commands to the various banks to optimize the operation of the memory system, but it serves to illustrate that each data bus burst transfer operation 900

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provides two command/address slots 910, 912. Because three commands are required to effect the transfer, however, the data bus efficiency may be reduced to two-thirds of its capacity.

Summary of the Invention

An electronic system according to various aspects of the present invention includes a memory having a location-specific command interface and a general command interface. The memory communicates with other components in the system via a main command bus configured to transfer address-specific commands and a supplementary command bus configured to transfer general commands. Commands may be received by the memory simultaneously at the respective interfaces. For example, a PRECHARGE command may be received on the general command interface while a memory access is received on the location-specific interface.

Brief Description of the Drawings

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the following illustrative Figures, which may not be to scale. In the following Figures, like reference numbers refer to similar elements throughout the Figures.

Figure 1 is a block diagram of an electronic system according to various aspects of the present invention;

Figure 2 is a block diagram of a memory interface and a bus system;

Figure 3 is a block diagram of a main control bus and a supplementary control bus;

Figure 4 is a timing diagram for consecutive memory accesses;

Figure 5 is a block diagram of an alternative embodiment of a main control bus and a supplementary control bus;

Figure 6 is another alternative embodiment of a main control bus and a supplementary control bus;

Figure 7 is a timing diagram for providing a secondary command indicator;

Figure 8 is a timing diagram for providing a tertiary command indicator; and

Figure 9 is a timing diagram for a simplified, illustrative prior art memory access.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the

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figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description

The present invention may be described in terms of functional block components and various processing steps. Such functional blocks may be realized by any number of hardware and software components configured to perform specified functions. For example, the present invention may employ various components, e.g., memory elements, interface elements, logic elements, buses, package connections, and the like, which may carry out a variety of functions under the control of one or more processors or other control devices. In addition, the present invention may be practiced in conjunction with any number of storage systems and data transmission media and protocols and the systems described are merely exemplary applications of the invention. Further, the present invention may employ any number of conventional techniques for data transmission, signaling, data processing, bus control, and the like.

Referring to Figure 1, an electronic system 100 according to various aspects of the present invention may include a processor 102 and a memory system 104. The present electronic system 100 comprises a system using a memory, such as a personal computer system. The electronic system 100 may comprise, however, any suitable electronic system, such as a communication system, computing system, entertainment system, control system, portable electronic device, audio component, appliance, or factory control system, and the various components may differ according to the particular system and environment. The processor 102 generally controls operation of the electronic system 100, and may comprise any appropriate processor or controller, such as an Intel, Motorola, or Advanced Micro Devices microprocessor. In some applications, the processor 102 may be replaced by other devices, such as logic circuits or ASICs, or omitted altogether.

The memory system 104 comprises a storage system for storing data. The memory system 104 may comprise any appropriate memory system for storing data and transferring data between the memory system 104 and the processor 102 or another component. In the present embodiment, the memory system 104 includes one or more memory modules 210A, B, a memory controller 212, and a bus system 106. The memory controller 212 controls access to, including data transfers to and from, the memory modules 210, and may perform further functions and operations as well. The memory controller 212 may comprise any

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suitable memory controller for controlling access to the memory modules 210. In some embodiments, the memory controller 212 may be omitted and/or have its functions performed by other system components.

The memory modules 210 may comprise any system for storing data, such as a ROM, SRAM, DRAM, SDRAM, or any other suitable storage system. In the present embodiment, the memory modules 210 comprise double data rate synchronous dynamic random access memory (DDR SDRAM) modules from Micron. For example, each memory module 210 suitably comprises a high-speed CMOS SDRAM internally configured as four banks of DRAMs. The memory modules 210, however, may comprise any appropriate memory or configuration, such as an individual memory chip, a multi-component device, or another type of storage device altogether. The memory modules 210 interface with the rest of the electronic system 100 through any suitable interface, such as a plurality of connections comprising pins, solder, conductive connections, optical couplings, or any other suitable coupling.

The bus system 106 connects the components of the memory system 104. The memory system 104, including the bus system 106, may utilize any appropriate signals, including optical or electric signals. The bus system 106 may comprise any suitable medium for transferring information, such as a plurality of wires, optical fibers, or other communication medium. In the present embodiment, the medium comprises an electronic bus, such as a serial bus or multi-bit bus, to which the memory system 104 and other components may be attached.

Communications with the memory system 104 may be controlled in any suitable manner and by any suitable component, such as using the processor 102, the memory controller 212, or other circuit or system to control communications. In the present embodiment, communications with the memory module 210 are suitably controlled by the memory controller 212.

The bus 106 and the connected components may communicate using any appropriate communication techniques and/or protocols. For example, the components may communicate via the bus 106 using a selected conventional protocol, such as those described in specifications for Micron SDRAMs. The bus 106 is also suitably configured to communicate with the memory modules 210. For example, referring to Figure 2, each memory module 210 includes an interface 250 having a data bus connection 320, address bus connection 324, main command bus connection 326, and supplementary command bus

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connection 328. The bus 106 may be configured accordingly to facilitate communication, such as including a data bus 220, an address bus 224, a main control bus 226, and a supplementary control bus 228.

The memory interface 250 and the bus 106 provide one or media for transferring information to and from the memory module 210. Each bus component 220, 224, 226, 228 ordinarily transfers a selected type of information, i.e., address selection information on the address bus 224, data on the data bus 220, and command signals on the main control bus 226 and the supplementary control bus 228. Further, each bus may be suitably configured to transfer the relevant information. For example, each bus may be configured to handle a selected number of bits.

More particularly, the data bus interface 320 of the present embodiment comprises a multibit, such as 4-, 8-, or 16-bit, connection for transferring information to and from the data bus 220. The address bus interface 324 of the present embodiment comprises a 13-bit connection for, among other things, receiving row and column address information to select one location out of the memory array 210 in a selected bank. The data bus 220 and address bus 224 are suitably configured to interface with the memory module 210 via the corresponding interfaces 320, 324.

Signals on the main control bus 226 and the supplementary control bus 228 define commands, and may further identify the chips and/or banks to which the commands apply. The commands may be any set of commands for operation of the memory module 210. In the present embodiment, the supplementary control bus 228 is used to provide a first selected subset of commands and the main control bus 226 to provide a second selected subset or, alternatively, the entire set of commands. For example, the supplementary control bus 228 may be used for general commands, i.e., commands that relate to large blocks of memory locations (like the entire module or an entire bank). The main control bus 226 handles location-specific commands, i.e., that relate to specific individual locations or groups of locations in the memory module 210, as well as other commands in various embodiments. The memory location relating to the location-specific command may be indicated in any suitable manner, such as by signals on the address bus 224. Thus, the main control bus 226 is used for commands using row and/or column information, typically provided via the address bus 224, and the supplementary control bus 228 is used for commands that are not associated with row or column information, and thus do not utilize the address bus 224.

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Command signals may be divided between the main control bus 226 and the supplementary control bus 228 in any suitable manner; similarly, the main control bus 226 and the supplementary control bus 228 may be configured in any suitable manner to accommodate the command signals. For example, in one embodiment illustrated in Figure 3, the main control bus 226 comprises a main command bus 410 having three main command bits (M-CMD), a main chip select bus bit 412 having one bit (M-CS), and a main bank selection bus 414 having two bits (M-BA). The three main command bits are suitably designated as a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE). In the present embodiment, the main bank selection bus 222 comprises a two-bit bus which defines the bank to which a command is to be applied, and the one-bit main chip select bus 412 identifies the relevant chip for the corresponding operation.

Similarly, the supplementary control bus 228 may be configured in any suitable manner to accommodate the relevant command set. For example, the supplementary control bus 228 suitably comprises a supplementary command bus 416 (S-CMD), a supplementary chip select bus 418 (S-CS), and a supplementary bank selection bus 420 (S-BA). In one embodiment, the supplementary control bus 228 solely facilitates PRECHARGE operations. PRECHARGE operations may comprise operations to deactivate open rows in a particular bank or all banks of the memory, though the PRECHARGE operation may comprise any appropriate process for preparing a memory or portion of memory for access or restoring a memory to a selected state following an access.

In the present dedicated PRECHARGE embodiment, the supplementary command bus 416 is a one-bit signal such that assertion of the supplementary command bit signals the memory module 210 to execute a PRECHARGE command on the bank 310A indicated by the supplementary chip select bus 418 and supplementary bank selection bus 420. Alternatively, because PRECHARGE is the only command controlled by the supplementary control bus 228, the supplementary command bus 416 may be omitted altogether, so that the supplementary chip select bus operates as the PRECHARGE signal. Activation of the supplementary chip select causes a PRECHARGE operation on the indicated chip in the bank designated by the supplementary bank selection bus 420.

Thus, the ACTIVE and subsequent READ or WRITE commands may be asserted using the main control bus 226 in conjunction with the address bus 224 to retrieve or store data. The next ACTIVE command or other command may then be asserted via the main control bus 226 on another bank 310B concurrently with assertion of a PRECHARGE

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command on the original bank 310A via the supplementary control bus 228. Accordingly, the PRECHARGE commands may be asserted without using the main control bus 226, thus relieving congestion on the main control bus 226 and tending to improve the performance of the memory module 210.

More particularly, an electronic system 100 and method according to various aspects of the present invention may use the main control bus 226 to activate rows and select columns for memory access operations and the supplementary control bus 228 to close banks of memory. For example, referring to Figure 4, an initial memory access may be performed by identifying the relevant bank on the main bank selection bus 414, the relevant chip on the main chip select bus 412, and the relevant memory row on the address bus 224, and providing the ACTIVE signal on the main command bus 410 at a first time T1. At substantially the same time, the supplementary control bus 228 receives a NOP command to prevent any unwanted command from being registered on the supplementary control bus 228.

Following the initial memory access, a second memory access operation may be initiated at a second memory location on a different bank. Accordingly, the second memory location may be identified on the main chip select bus 412, main bank select bus 414, and address bus 224, and the ACTIVE and READ or WRITE commands may be successively provided via the main command bus 410 at times T3 and T4. Meanwhile, the supplementary control bus 228 may provide a PRECHARGE command to a previously accessed bank to close the still-active row from the preceding memory access operation. For example, the previously accessed bank and chip are identified on the supplementary bank selection bus 420 and supplementary chip select bus 418, respectively, at time T3. The PRECHARGE command is provided on the supplementary command bus 416 to initiate the precharge of the previously accessed bank while the second bank is being accessed via the main control bus 226.

The command set may be apportioned and/or shared by the main control bus 226 and the supplementary control bus 228 in any suitable manner. For example, the commands may be shared such that all of the commands requiring the address bus 224 are asserted via the main control bus 226, and all of the commands that do not require the address bus 224 may be asserted via either the supplementary control bus 228 or the main control bus 226. Thus, the device providing the commands, such as the memory controller 212, may select which control bus 226, 228 on which to provide a command according to any selected criteria.

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Alternatively, the commands may be restricted to assertion on either the main control bus 226 or the supplementary control bus 228, or the commands may be apportioned such that one set of commands is asserted only on the main control bus 226, a second set is asserted only on the supplementary control bus 228, while a third set may be asserted on either bus 226, 228.

Similarly, memory module interface 250, the main control bus 226, and the supplementary control bus 228 may be configured in any suitable manner to facilitate assertion of the commands as apportioned or shared. In the embodiment in which all commands not requiring the address bus 224 may be asserted on either the main control bus 226 or the supplementary control bus 228, the respective control buses 226, 228 are suitably configured with sufficient bits to accommodate the relevant command set. For example, referring to Figure 5, the memory module 210 may accommodate nine commands such that three commands require the address bus 224 (such as ACTIVE, READ, and WRITE) and six commands do not (such as DESELECT, NO OPERATION, BURST TERMINATE, PRECHARGE, AUTO REFRESH, and LOAD MODE REGISTER). To accommodate all nine commands, the main control bus 226 may be configured with four command bits. Similarly, the supplementary control bus 228 is suitably configured with three command bits to accommodate the six commands that do not use the address bus 224.

In alternative embodiments, the number of pins may be reduced by reconfiguring the command set and the main and supplementary command buses 226, 228 and the interface 250. For example, the commands may be apportioned such that commands not requiring the address bus 224 are asserted only on the supplementary control bus 228. Thus, in the present embodiment, the main control bus 226 may be configured to handle only three commands (ACTIVE, READ, and WRITE), requiring only two command bits, as illustrated in Figure 6.

In another embodiment, the number of bits required by the supplementary control bus 228 may be reduced by packetizing various commands. Packetizing comprises sending consecutive signals for a single command, such as for lower priority commands. For example, referring to Figure 7, the supplementary control bus 228 may be configured with two supplementary command bits 416 as well as the supplementary chip select 418 and supplementary bank select bits 420. The supplementary command bits 416 may receive one of four main commands. Three commands are suitably executable commands, such as PRECHARGE, AUTO REFRESH, and NOP. The fourth command may be a secondary

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command indicator 620, referred to in this embodiment as EXTEND1. EXTEND1 designates a secondary command 622 following, for example, in the next cycle. Thus, if EXTEND1 is transmitted, the next cycle contains the secondary command 622. The secondary commands may comprise any appropriate commands, such as SELF REFRESH, WAKE, or LOAD MODE. In the present embodiment, the secondary commands comprise commands that are lower priority than the main commands. The main and secondary command sets may be selected, however, according to any desired criteria.

Further, referring to Figure 8, the secondary command 622 may indicate another command following, such as in the next cycle, by asserting a tertiary command indicator 724 (EXTEND2). The tertiary command 726 may then be asserted in the following cycle. Additional command capability may be provided using additional sub-command indicators if desired. Thus, many low priority commands may be added without adding additional command bits.

It should be appreciated that the particular implementations shown and described herein are illustrative of the invention and its best mode and are not intended to otherwise limit the scope of the present invention in any way. Indeed, for the sake of brevity, conventional signal processing, data transmission, and other functional aspects of the systems (and components of the individual operating components of the systems) may not be described in detail herein. Furthermore, the connecting lines shown in the various figures contained herein are intended to represent exemplary functional relationships and/or physical couplings between the various elements. It should be noted that many alternative or additional functional relationships or physical connections may be present in a practical communication system.

The present invention has been described above with reference to a preferred embodiment. However, those skilled in the art having read this disclosure will recognize that changes and modifications may be made to the preferred embodiment without departing from the scope of the present invention. These and other changes or modifications are intended to be included within the scope of the present invention, as expressed in the following claims.

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Claims

1. An electronic system, comprising:

a processor;

a memory having more than one memory location; and

a bus connecting the processor to the memory, wherein the bus comprises:

a data bus for transmitting data;

an address bus for identifying a first memory location;

a main command bus for transferring a first command that relates to the first memory location; and

a supplementary command bus for transferring a second command, wherein the second command does not relate to the first memory location.

2. An electronic system according to claim 1, wherein the second command is a PRECHARGE command, and wherein the supplementary command bus comprises a one-bit bus.

3. An electronic system according to claim 1, wherein:

the main command bus transfers location-specific commands; and

the supplementary command bus transfers only general commands.

4. An electronic system according to claim 1, wherein:

the second command is a secondary command indicator; and

the supplementary command bus transfers a third command after the second command.

5. An electronic system, comprising:

a processor;

a memory having more than one memory location; and

a bus connecting the processor to the memory, wherein the bus comprises:

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a main command bus configured to transfer an address-specific command; and

a supplementary command bus configured to transfer a general command.

6. An electronic system according to claim 5, wherein the general command is a PRECHARGE command.

7. An electronic system according to claim 5, wherein:

the general command is a secondary command indicator; and

the supplementary command bus is further configured to transfer a third command after the second command.

8. A memory having an interface, wherein the interface comprises:

a location-specific command interface configured to receive location-specific commands; and

a general command interface configured to receive only one or more general commands.

9. A memory according to claim 8, wherein the general command interface is configured to receive a PRECHARGE command.

10. A memory according to claim 8, wherein the location-specific command interface is configured to receive location-specific commands and general commands.

11. A memory having an interface, wherein the interface comprises a general command interface configured to receive a general command.

12. A memory according to claim 11, wherein the general command is a PRECHARGE command.

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13. A memory according to claim 11, wherein the memory includes more than one bank, and the interface further comprises a general bank select interface configured to receive bank address information for the general command.

14. A memory including a one-bit PRECHARGE input dedicated to receiving a PRECHARGE command.

15. A memory according to claim 14, wherein the memory includes more than one bank, further including a general bank select interface configured to receive bank address information for the PRECHARGE command.

16. A memory system, comprising:

a memory controller; and

a memory in communication with the memory controller, wherein the memory includes an interface, comprising:

a main control interface for receiving a location-specific command; and

a supplementary control interface for receiving a general command.

17. A memory system according to claim 16, wherein the general command is a PRECHARGE command.

18. A memory system according to claim 16, wherein:

the general command is a secondary command indicator; and

the supplementary control interface is configured to transfer a secondary command after the secondary command indicator.

19. An electronic system, comprising:

a processor; and

a memory system connected to the processor, comprising:

a memory controller connected to the processor; and

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a memory connected to the memory controller and having an interface, comprising:

an address interface for receiving an address signal;

a main control interface, comprising:

a main command bus for receiving a first command signal relating to a memory location specified by the address signal; and

a main bank select bus for receiving a first bank select signal specifying a first bank corresponding to the first command signal; and

a supplementary control interface, comprising:

a supplementary command bus for receiving a second command signal, wherein the second command signal corresponds to a general command; and

a supplementary bank select bus for receiving a second bank signal specifying a second bank corresponding to the second command signal.

20. A method of accessing a memory, comprising:

in a first time slot, requesting activation of a first row;

in a second time slot, requesting an access of a memory location in the first row;

in a third time slot, requesting activation of a second row and requesting closure the first row.

21. A method according to claim 20, further comprising:

providing a main command bus, wherein the requesting activation of the second row occurs on the main command bus; and

providing a supplementary command bus, wherein the requesting closure of the first row occurs on the supplementary command bus.

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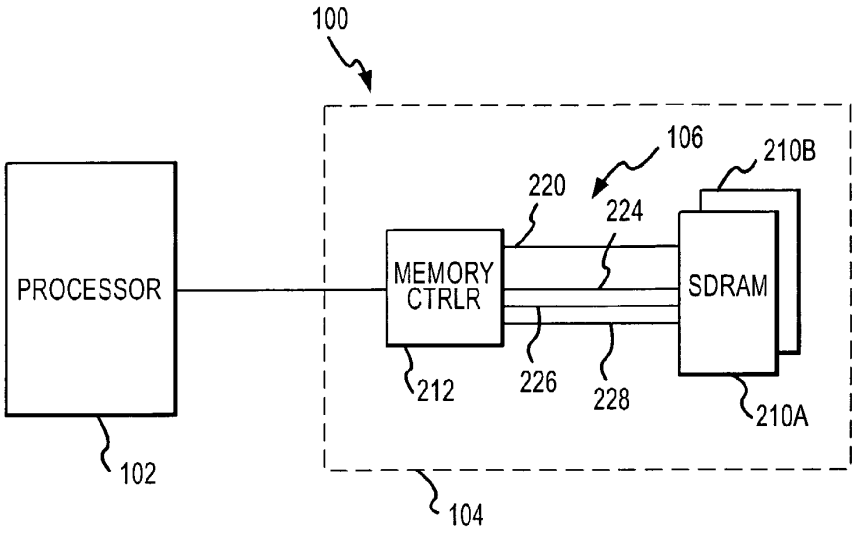
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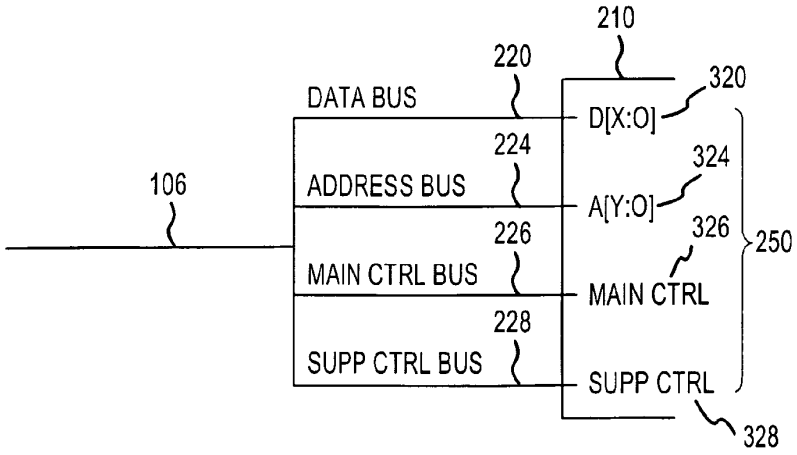
212
226
228
210A
102
104

FIG.1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SUPP CTRL
328

FIG.2

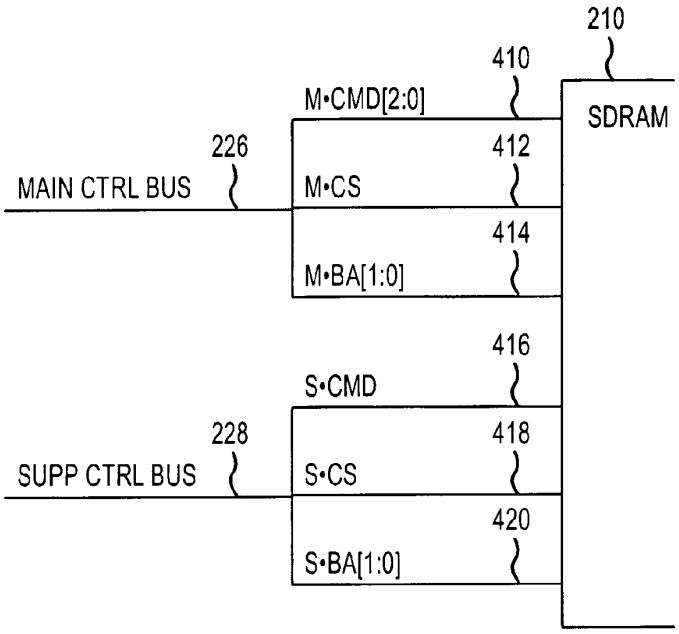
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FIG.3

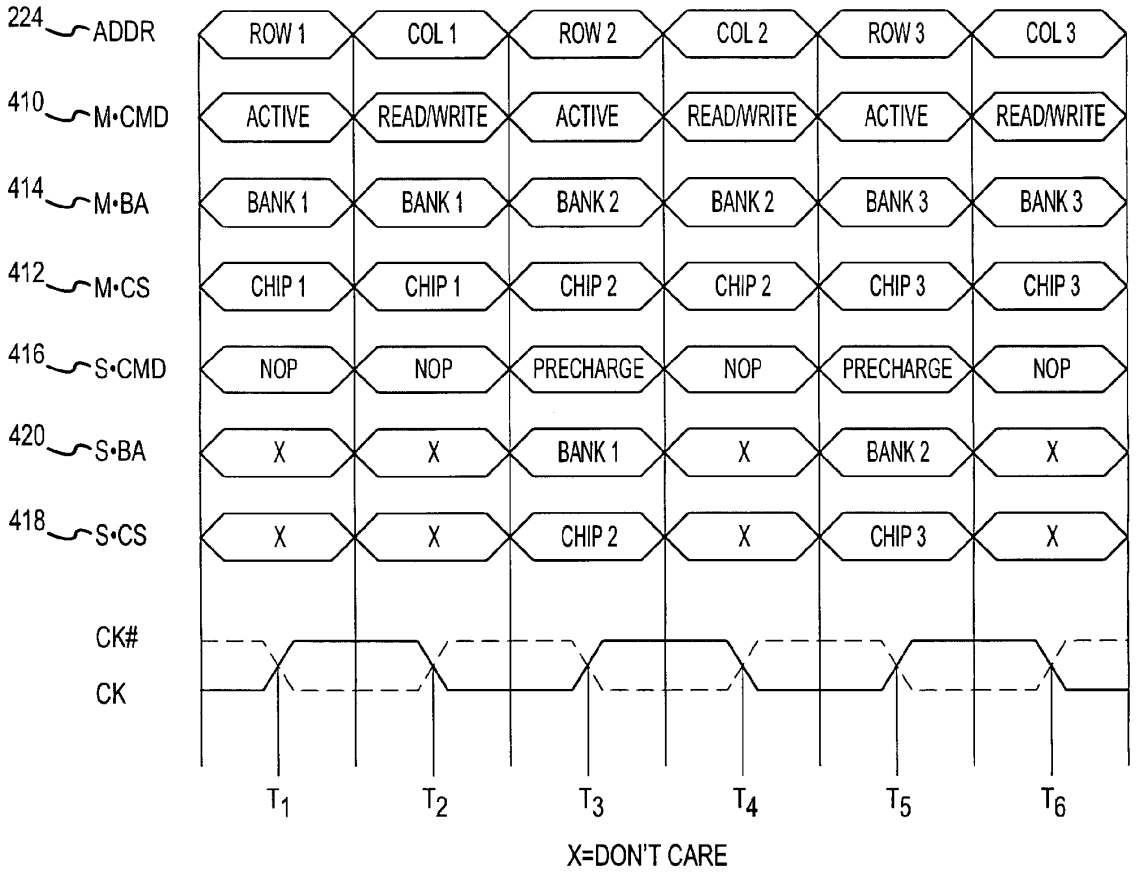

FIG.4

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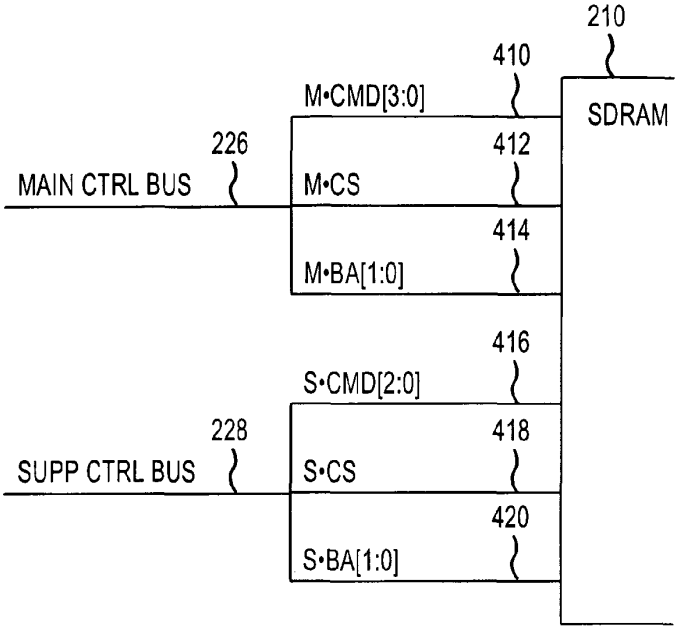
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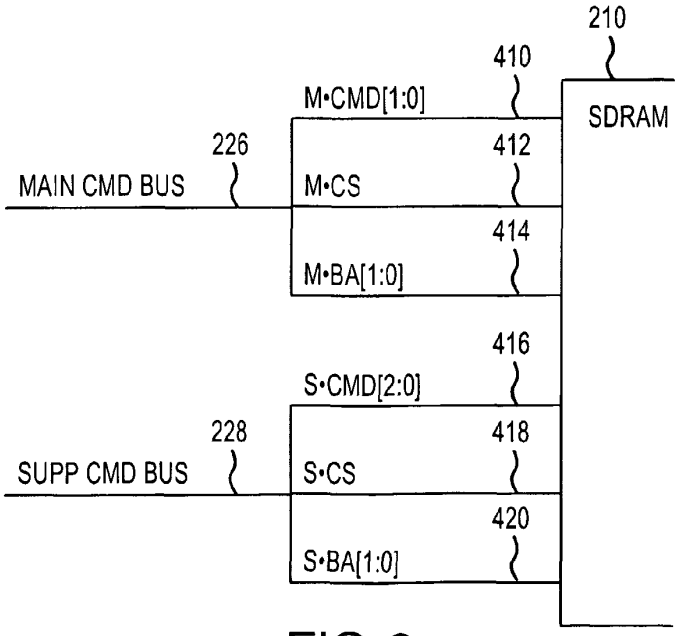
FIG.5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S•CS
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S•BA[1:0]

FIG.6

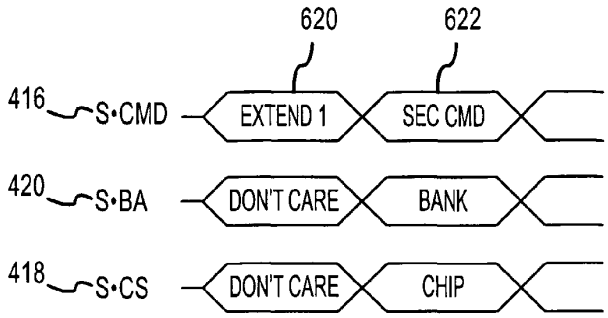

620
622
416
S•CMD
EXTEND 1
SEC CMD
420
S•BA
DON'T CARE
BANK
418
S•CS
DON'T CARE
CHIP

FIG.7

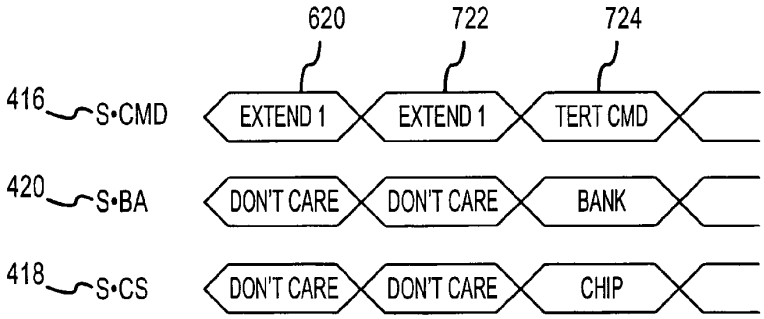
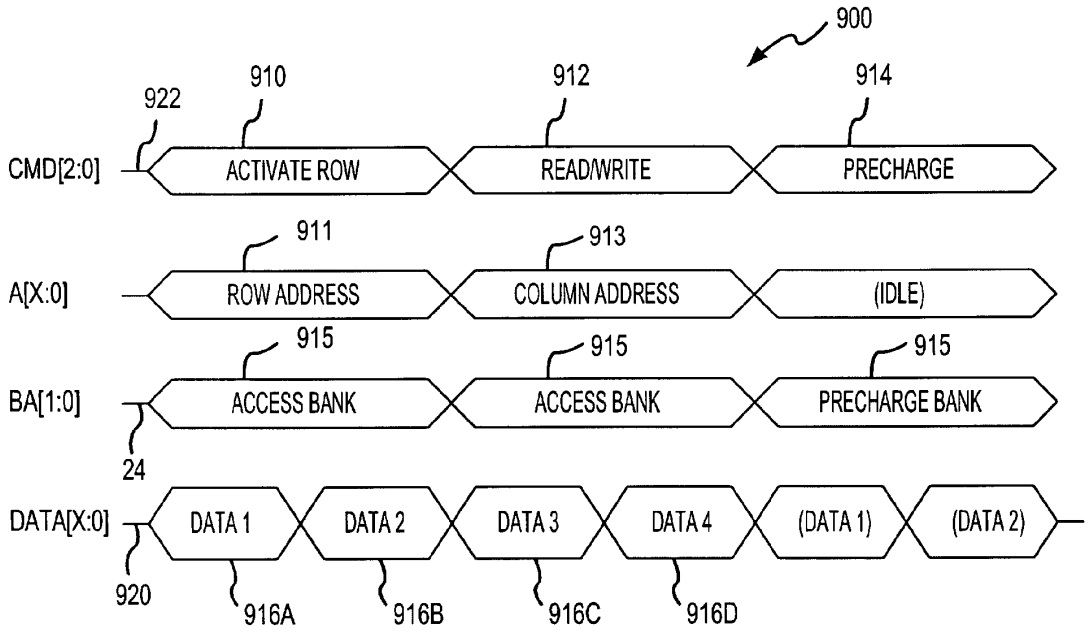

620
722
724
416
S•CMD
EXTEND 1
EXTEND 1
TERT CMD
420
S•BA
DON'T CARE
DON'T CARE
BANK
418
S•CS
DON'T CARE
DON'T CARE
CHIP

FIG.8



(PRIOR ART)

FIG.9

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 May 2006 (26.05.2006)

PCT

(10) International Publication Number
WO 2006/055497 A2

(51) International Patent Classification:
G06F 13/40 (2006.01) *G11C 7/00* (2006.01)
G11C 5/06 (2006.01)

(21) International Application Number:
PCT/US2005/041199

(22) International Filing Date:
10 November 2005 (10.11.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/992,953 18 November 2004 (18.11.2004) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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(54) Title: COMMAND CONTROLLING DIFFERENT OPERATIONS IN DIFFERENT CHIPS

(57) Abstract: Abstract of the Disclosure In some embodiments, the invention includes a chip having a register to include an operation type signal. The chip also includes control circuitry to receive a first command and in response to the first command to cause the chip to perform a first operation if the operation type signal has a first value and to cause the chip to perform a second operation if the operation type signal has a second value. The chip may be a memory chip in a memory system. Other embodiments are described and claimed.

COMMAND CONTROLLING DIFFERENT OPERATIONS IN DIFFERENT CHIPS

BACKGROUND

TECHNICAL FIELD

The present invention relates to semiconductor chips and, more particularly, to chips in which a command causes different operations in different chips.

BACKGROUND ART:

Conductors are typically terminated through resistive structures, such as resistive materials and transistors. The terminations have been positioned in various places. Examples of the location of terminations include on motherboards or other circuit boards or cards. Other examples of locations of terminations include on a chip that transmits a signal and/or on a chip that receives a signal. Terminations on the chip are commonly referred to as on die terminations (ODTs).

Some Dynamic Random Access Memories (DRAM) chips have registers referred to as a mode register set (MRS) which includes bits to control functions of the DRAM chips. One or more bits in the MRS may control particular functions of the DRAM chips. Extended MRSs (such as EMRS0, EMRS1 etc.) may provide additional bits for use.

DRAM chips are typically included in memory modules, some of which are dual in-line memory modules (DIMMS). The term rank refers to a group of memory chips that are selected together, for example, through a shared chip select signal or through some other way. Some modules include only one rank per module and some include more than one rank per module. Some ranks include chips on more than one module.

In some two rank memory systems, for best electrical performance, the ODT is enabled on the DRAM chips that are not receiving the data for write operations.

The JEDEC Solid State Technology Association has provided standards for DDR2 (dual date rate 2 or double data rate 2) DRAM chips. In DDR2 DRAM chips, the ODTs are controlled by using discrete signals per rank. In some two rank-1 DIMM systems, two ODT pins are used on the controller and the DIMM. Two pins may also used per DRAM chip to support stacking solutions. As used in this disclosure, the word "pin" means traditional pins or other connections to die pads.

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In GDDR3 (graphics DDR3) and also DDR3/DDR2 proposals, the command bus may be shared between two ranks. The DRAM can monitor or snoop the command bus for a write transaction. If it sees a write cycle and no CS# asserted then, it can turn its ODT on. The write command may target the other rank. (CS# are rank or device specific). The term "2N timing" refers to a situation in which it takes an extra clock cycle for sampling as compared to a 1N timing. The sampling may be of a signal, such as an address signal. Snooping may work well for 1N timings, but not for 2N timings (with an additional clock cycle before sampling) because snooping may cause additional clock cycles in turnaround cycles and in leadoff write cycles.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

FIG. 1 is a block diagram representation of a system including a memory controller and a memory module including memory chips according to some embodiments of the invention.

FIG. 2 is a block diagram representation of further details of the memory controller and memory chips of FIG. 1 according to some embodiments of the invention.

FIG. 3 is a representation of a register according to some embodiments of the invention.

FIG. 4 is a block diagram representation of further details of a memory chip of FIGS. 1 and 2 according to some embodiments of the invention.

FIG. 5 is a block diagram representation of a system including a memory controller and a memory module according to some embodiments of the invention.

FIG. 6 is a block diagram representation of a system including a memory controller and memory modules according to some embodiments of the invention.

FIG. 7 is a timing diagram illustrating operation of the memory controller and memory chips of FIG. 5 according to some embodiments of the invention.

FIG. 8 is a block diagram representation of the memory controller of FIGS. 1, 2, 5, and 6 being included in the same die as a processor.

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FIG. 9 is a block diagram representation of the memory controller of FIGS. 1, 2, 5, and 6 being included in the same die as a memory controller hub of a chipset.

FIG. 10 is a system showing a program to provide values to the registers of FIG. 2.

DETAILED DESCRIPTION

Referring to FIG. 1, a memory controller 12 provides various signals including command signals (hereinafter called commands) to a memory chip MC0 and to a memory chip MC1 on a support 16. A memory module 18 includes chips MC0 and MC1 and a support 16 and may include additional chips not illustrated in FIG. 1. Various signals, including commands, pass through interconnects 14 between memory controller 12 and MC0 and MC1. Data, addresses, commands, and chip select signals may be on different conductors or may be shared on at least some of the same conductors. Signals of different types may be carried on different interconnects or the signals may be fully or partially packetized or time multiplexed over the same conductors in interconnects 14.

Chip MC0 responds to a particular command by performing one operation and chip MC1 responds to the same command by performing another operation. For example, chip MC0 may respond to a command, for example, called command A, by performing a write operation while chip MC1 responds to command A by turning on an ODT. Stated another way, chip MC0 may interpret command A as being a write command while chip MC1 interprets command A as being a turn on ODT command. In some embodiments, there is a second command, for example, called command B, for which chip MC0 responds by turning on an ODT while MC1 responds by performing a write operation. As another example, chip MC0 may respond to a command, for example, called command C, by performing a read operation while chip MC1 responds to command C by performing a refresh operation. Likewise, there may be a second command, for example, called command D, for which chip MC0 responds by performing a refresh operation while MC1 responds by performing a read operation. Still other different operations may be performed in response to a command. Note that the labels A, B, C, and D are arbitrary.

There are many ways in which chips MC0 and MC1 may be implemented. FIG. 2 illustrates some example implementations (embodiments), but the invention is not limited to the details of FIG. 2 and the following description of it. The invention may be implemented in various embodiments that are different from FIG. 2 and the description of

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it. Further, the embodiments of FIG. 2 may include additional components not illustrated in FIG. 2.

Referring to FIG. 2, memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20, a data bus 22, and an address bus 24. Chip select (CS) signals are provided to chips MC0 and MC1 through buses 26 and 28. Chip select signals are sometimes active low and designated CS#. In the case of FIG. 2, the chip select signals are CS0# for chip MC0 and CS1# for chip MC1. Chip select signals are sometimes referred to as device select signals.

The commands referred to in this disclosure may be provided from memory controller 12 to chips MC0 and MC1 through various ways. In some embodiments, the commands described herein are provided only through control bus 20. In other embodiments, the commands are provided through a combination of control bus 20 and address bus 24. In still other embodiments, the data bus is also used to communicate commands. Control circuitry 32 in chip MC0 and control circuitry 42 receive the commands from controller 12, although the signal including the commands may be modified or otherwise changed between the controller 12 and controller circuitry 32 and 42.

Chip MC0 includes a register 30 and chip MC1 includes a register 40. Registers 30 and 40 include operation type signals to control how chips MC0 and MC1 interpret at least some commands. The operation type signals may be in one or more than one bits. As an example, registers 30 and 40 each may be included in a MRS or EMRS using previously unused bits or new bits. However, it is not required that registers 30 and 40 be in an MRS or EMRS.

As an example (called example 1), an operation type signal in register 30 has a first value because, for example, a particular bit in register 30 has a first voltage state. The same operation type signal in register 40 has a second value because the corresponding bit in register 40 has a second voltage state. In example 1, there are commands called commands A and B. Chip MC0 responds to command A as a write command, meaning that control circuitry 32 causes certain data bits on data bus 22 to be stored in core 36 of chip MC0. Chip MC1 responds to command A by turning on ODT 48. More particularly control circuitry 42 turns on ODT 48. Conversely, chip MC0 responds to command B by turning on ODT 38 and chip MC1 responds to command B as a write command. More

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particularly, in response to command B, control circuitry 32 turns on ODT 38 and control circuitry 42 causes data on bus 22 to be stored in core 46. In some embodiments, if the values of the operation type signals in registers 30 and 40 were reversed, then chip MC0 would respond to command A by turning on ODT 38 and to command B by performing a write operation; and chip MC1 would respond to command A by performing a write operation and to command B by performing an ODT operation.

As another example (called example 2), there are commands called commands C and D. An operation type signal in registers 30 and 40 could be set with particular values such that chip MC0 responds to command C as a read command and to a command D as a refresh command, whilst chip MC1 responds to command C as a refresh command and to command D as a read command. The values of the operation type signal can be set by the states (voltages) of one or more bits in registers 30 and 40. There can be only one or more than one operation type signal in a register. In some embodiments, chips MC0 and MC1 have the features of both examples 1 and 2, whilst in other embodiments, chips MC0 and MC1 have the features of example 1, but not example 2, and in still other embodiments, chips MC0 and MC1 have the features of example 2, but not example 1.

FIG. 3 illustrates a register with one or more bits for "write or ODT on" and one or more bits for "read or refresh." The register of FIG. 3 may represent register 30 or 40, although registers 30 and 40 are not required to include bits for both "write or ODT on" and "read or refresh." In FIG. 3, different bits are shown to control "write or ODT on" and "read or refresh." Alternatively, the same bit(s) can control both. For example, if the operation type signal has a first value, then the chip may respond to command A as a write request and command C as a read request, and if the operation type signal as a second value, the chip responds to command B as an ODT on command and command D as a refresh request. Even other information can be encoded in the operation type signal.

In examples 1 and 2, the first state could be a logical high voltage and the second state a logical low voltage, but that is not required. For example, the first state could be a logical low voltage and the second state could be a logical high voltage. In other embodiments, more than two states (voltages) can be included in a register bit(s).

There are various ways in which an ODT may be constructed and this invention is not limited to any particular way. FIG. 4 illustrates an implementation of ODT 38 in chip MC0, but the invention is not limited to these details. Indeed, various other types of ODT

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may be used. Further, some embodiments do not include any ODT. Referring to FIG. 4, resistive structures R1-D ... RN-D are between a data node 50 and switches Sw1-D ... SwN-D, respectively, which in turn are coupled to a supply voltage node VDDQ. Resistive structures R1-S ... RM-S are between data node 50 and switches Sw1-S ... SwM-S, respectively, which in turn are coupled to a ground voltage node VSSQ. The numbers "N" and "M" may be the same or different and may have different values in different implementations. Control circuitry 32 controls the switches and hence whether ODT 38 is "on." The number of switches closed may determine the amount of resistance in the termination. For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance. In FIG. 4, data node 50 is between a pin (pad) and an input buffer 52. Some chips do not include traditional pins, but may include pads.

In current typical implementations, more than one memory chip is included in a module. The chips are typically grouped in ranks. For example, FIG. 5 illustrates memory controller 12 being coupled to memory chips in a memory module 64, which has two ranks of chips supported by support 62. A first rank (rank 0) includes memory chips MC0-0 .... MC0-N (where N is not necessarily the same as in FIG. 4). A second rank (rank 1) includes memory chips MC1-0 .... MC1-N. The two ranks may have the same number of chips or a different number. FIG. 5 illustrates each chip in a rank being selected by the same chip select signal (CS0 for the chips of rank 0 and CS1 for the chips of rank 1). The chip select signal could be provided on its own multi-drop bus as illustrated in FIG. 5 or through other ways such as a multiplexed or packetized signal.

In FIG. 6, memory controller 12 is coupled to a first memory module 68 with a first rank of chips (MC0-0 ... MC0-N) and a second rank of chips (MC1-0 ... MC1-N) supported by a support 66 and to a second memory module 74 with a third rank of chips (MC2-0 ... MC2-N) and a fourth rank of chips (MC3-0 ... MC3-N) supported by a support 72. Chip select signals CS0, CS1, CS2, and CS3 are used to select the chips in the corresponding ranks. Accordingly, chip select signals CS0 is used for all the chips of the first rank (rank 0), CS1 is used for all the chips of the second rank (rank 1) and so forth. The chip select signals in FIG. 6 could include a "#" symbol.

Various alternatives may be used. For example, in some embodiments, each module has only one rank. In this example, FIG. 6 could be modified so that all the chips

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in module 68 were in one rank and all the chips in module 74 were in another rank. As another alternative, each module could have two ranks, but the system would include only two ranks. In this example, FIG. 6 could be modified so that chips MC0-0 ... MC0-N and MC2-0 ... MC2-N would be in one rank and chips MC1-0 ... MC1-N and MC3-0 ... MC3-N would be in the other rank. There could be more than two ranks per module and more than four ranks per system.

As illustrated in FIGS. 5 and 6, each of the memory chips are on the same side of supports 62, 66, and 72. In practice, the chips of one rank may be on one side of the support and the chips of another rank may be on the other side of support, or some other arrangement may be used. In some embodiments, chips from the same rank are on different sides of the support.

FIG. 7 provides an illustrative timing diagram for operation of the system of FIG. 5, although the invention is not limited to these details.

During clock cycle 0, command A is issued with CS0# and CS1# asserted.

During clock cycle 3, the ODT in each of chips MC1-0 ... MC1-N (rank 1) is turned on after a delay of tAOND.

During clock cycles 4-7, data is written to chips MC0-0 ... MC0-N (rank 0) on the bus after a delay of tWL. As an example, a DDR3 memory chip may be used with a burst length (BL) of 8 and data double pumped (also called dual data rate or double data rate), meaning data is transmitted or received once each half clock cycle. Note that there is some time between the time the ODT is turned on in the chips of rank 1 and the time data is on the bus for the chips of rank 0.

During clock cycle 5, command B is issued with CS0# and CS1# asserted.

During clock cycle 8, the ODT in chips MC1-0 ... MC1-N (rank 1) are turned off automatically (without a separate command) after a fixed delay based on a burst length of 8. (In some other embodiments, the ODTs are not turned off automatically.) During clock cycle 8, the ODT in chips MC0-0 ... MC0-N (rank 0) is turned on after a delay tAOND in response to command B.

During clock cycles 9-12, data is written to chips MC1-0 ... MC1-N (rank 1) on the bus after a delay of tWL.

During clock cycle 13, the ODT in chips MC0-0 ... MC0-N (rank 0) are turned off automatically after a fixed delay based on a burst length of 8.

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In some embodiments, if only one CS# is asserted then the second rank may ignore the command.

Although memory controller 12 is illustrated in different figures, it is not necessary that a memory controller according to the different embodiments of the invention have the ability to operate in each of the different systems.

FIG. 8 illustrates memory controller 12 as being in a processor 84, such as a microprocessor. FIG. 9 illustrates memory controller 12 as being in a memory controller hub 86 in a chipset.

Although FIGS. 2, 5 and 6 are illustrated with multi-drop bus configurations, point to point interconnects may be used. For example, interconnect 14 in FIG. 1 could be multi-drop, point-to-point or a combination of them. A command that is responded to differently by different chips can be received simultaneously by the chips or it can be received a different times by the chips.

Although the memory chips MC0 and MC1 are illustrated, the invention may be used with chips whose primary purpose is not memory storage.

The command may include multiple bits in parallel, in series or in a combination of parallel and series. The command may be packetized with other signals.

The states of the bits in registers 30 and 40 may be set at boot up (turning on the system that includes chips MC0 and MC1) or after boot up. For example, the state might be changed depending on various things that could happen after boot up. In some embodiments (different from those of the example 1), the state of the bits in registers 30 and 40 are changed so that the chips MC0 and MC1 respond to the same command as being sometimes a write command and other times a turn on ODT command. In this case, simply using command A would be sufficient and command B would not be used as it is in example 1.

FIG. 10 is the same as FIG. 2, except that system circuitry 90 interfaces between a program 92 in memory 94. In some embodiments, program 92 may be BIOS, an operating system or other software. Among other things, program 92 may control at least part of the contents of registers 30 and 40 including how chips MC0 and MC1 respond to commands, such as in examples 1 and 2. In other embodiments, program 92 does not control the contents of those parts of registers 30 and 40 that control how chips MC0 and MC1 respond to the commands, such as in examples 1 and 2. For example, memory controller

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12 may decide what is to be those contents of registers 30 and 40 based on internal logic of controller 12 independent of control of program 92.

By using a command to control the ODTs, it is not necessary to have a pin (pad) to control the ODTs, although there may be a pin to control the ODTs in some embodiments. In some embodiments, the ODTs are controlled only by commands, not pins. This results in reduction of pins compared to a system with pins used to control the ODTs. In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.

By using commands to control ODTs, it does not matter whether a 1N or 2N timing is used. As noted, a 2N timing involves one extra clock cycle to sample a signal.

The term "control" means to at least partially control. The term "cause" means to at least partially cause.

In the disclosure and claims, the use of the word "first" is just for convenience in distinguishing. It does not imply a temporal, spatial, or importance order. For example, reference to a first operational type signal does not mean the first operational type signal is first in a temporal, spatial, or importance order with respect to a second operational type signal. Likewise, reference to a first command does not mean that the first command is first in a temporal, spatial, or importance order with respect to other commands. Similarly, the words "second," "third," and "fourth" are merely labels without implying a temporal, spatial, or importance order.

An embodiment is an implementation or example of the invention. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

If the specification states a component, feature, structure, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or

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claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

The invention are not restricted to the particular details described herein. Indeed, many other variations of the foregoing description and drawings may be made within the scope of the present invention. Accordingly, it is the following claims including any amendments thereto that define the scope of the invention.

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CLAIMS

What is claimed is:

1. A chip comprising:

a register to include an operation type signal;

control circuitry to receive a first command and in response to the first command to cause the chip to perform a first operation if the operation type signal has a first value and to cause the chip to perform a second operation if the operation type signal has a second value.

2. The chip of claim 1, further comprising:

a memory core; and

an on die termination, and wherein the first operation is to turn on the on die termination and the second operation is to cause data to be written into the memory core.

3. The chip of claim 1, wherein the control circuitry is to receive a second command and to cause the chip to perform the second operation if the operation type signal has the first value and to cause the chip to perform the first operation if the operation type signal has the second value.

4. The chip of claim 1, wherein the operation type signal is a first operation type signal and the register also is to include a second operation type signal and the control circuitry is to receive a third command and to cause the chip to perform a third operation if the second operation type signal has a first value and to cause the chip to perform a fourth operation if the second operation type signal has a second value.

5. A system comprising:

a first chip to provide a first command; and

a second chip and a third chip to receive the first command, wherein the first chip responds to the first command by performing a first operation and wherein the second chip responds to the first command by performing a second operation.

6. The system of claim 5, wherein the first chip is a memory controller, the second chip is in a first rank of memory chips and the second chip is in a second rank of memory chips.

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7. The system of claim 5, wherein the first and second chips further comprising:

a memory core; and

an on die termination, and wherein the first operation is to turn on the on die termination and the second operation is to cause data to be written into the memory core.

8. A system comprising:

a first chip to provide a first command; and

a second chip including a register to include an operation type signal having a first value; and

a third chip including a register to include an operation type signal having a second value, and wherein in response to the first command and the operation type signals, the second chip performs a first operation and the third chip performs a second operation.

9. The system of claim 8, wherein the first chip is a memory controller, the second chip is in a first rank of memory chips and the second chip is in a second rank of memory chips.

10. The system of claim 8, wherein in response to receiving a second command, the second chip performs the second operation and the third chip performs the first operation.

11. The system of claim 8, wherein in response to receiving a third command, the second chip performs a third operation and the third chip performs a fourth operation.

12. The system of claim 8, wherein the command is simultaneously received by the second and third chips.

13. The system of claim 8, wherein the command is received at different times by the second and third chips.

14. A system comprising:

a memory controller to provide a first command;

a first group of memory chips each including a register to include an operation type signal having a first value; and

a second group of memory chips each including a register to include an operation type signal having a second value, and wherein in response to the first command and the values of the operation type signals, the chips of the first group each perform a first operation and the chips of the second group each perform a second operation.

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15. The system of claim 14, wherein each chip in the first group responds to a second command by performing the second operation and wherein each of the chips in the second group responds to the second command by performing the first operation.

16. The system of claim 14, wherein the operation type signals are a first operation type signal and the registers are also to include a second operation type signal and wherein in response to the a third command and the values of the second operation type signals, the chips of the first group of each perform a third operation and the chips of the second group each perform a fourth operation.

17. The system of claim 14, wherein the first operation is a write operation and the second operation is to turn on an on die termination in the chip performing the operation.

18. The system of claim 14, wherein the first operation is to turn on an on die termination in the chip performing the first operation and the second operation is a write operation.

19. The system of claim 14, wherein the first operation is a read operation and the second operation is a refresh operation.

20. The system of claim 14, wherein the first operation is a refresh operation and the second operation is a read operation.

21. The system of claim 14, wherein the first group of memory chips is in a first rank and the second group of memory chips is in a second rank.

22. The system of claim 14, further including system circuitry to interface between a program and the memory controller to control the state of the at least one bit in the chips.

23. The system of claim 14, wherein the program includes BIOS.

24. The system of claim 14, wherein the program includes an operating system.

25. The system of claim 14, wherein the memory controller provides signals to the memory chips to set the operation type signals in the registers.

26. The system of claim 25, wherein a value of the operation type signal is set when the chip becomes operational.

27. The system of claim 25, wherein a value of the operation type signal may change after the chip becomes operational.

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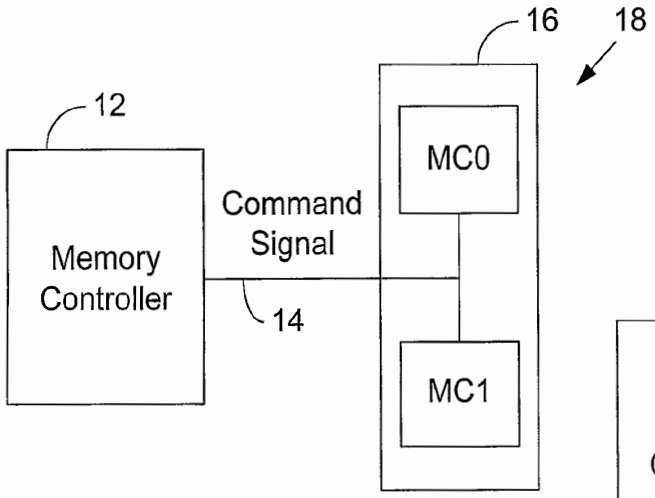

FIG. 1

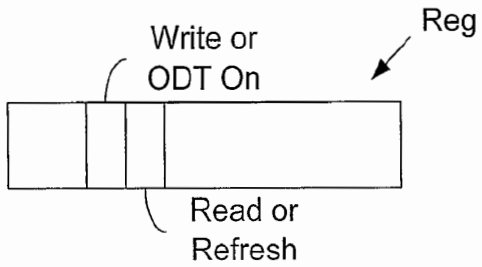

FIG. 3

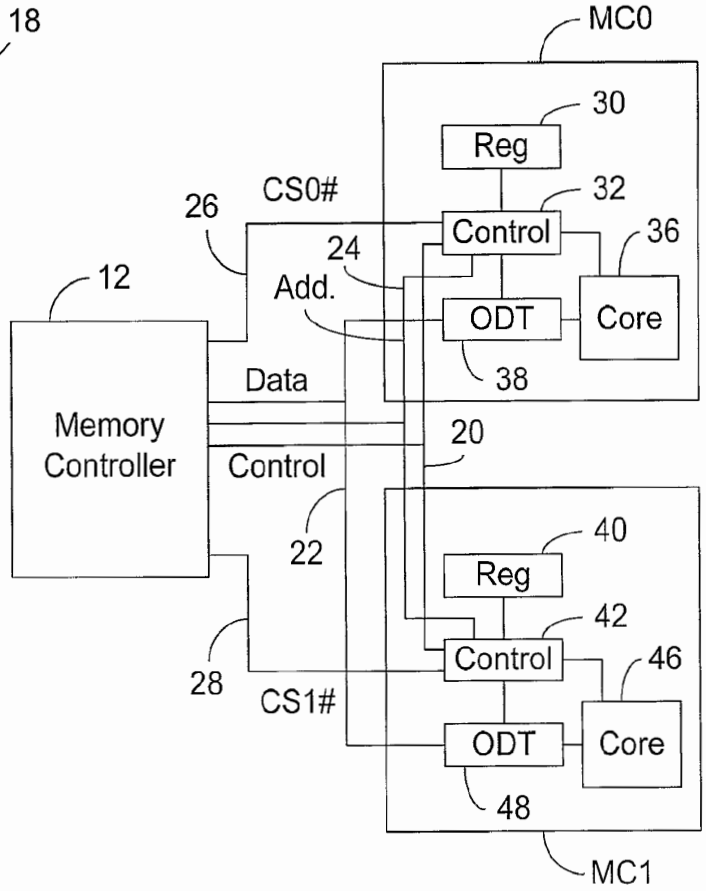

FIG. 2

Samsung Electronics Co., Ltd.
Ex. 1010, p. 762

Samsung Electronics Co., Ltd.
Ex. 1010, p. 763

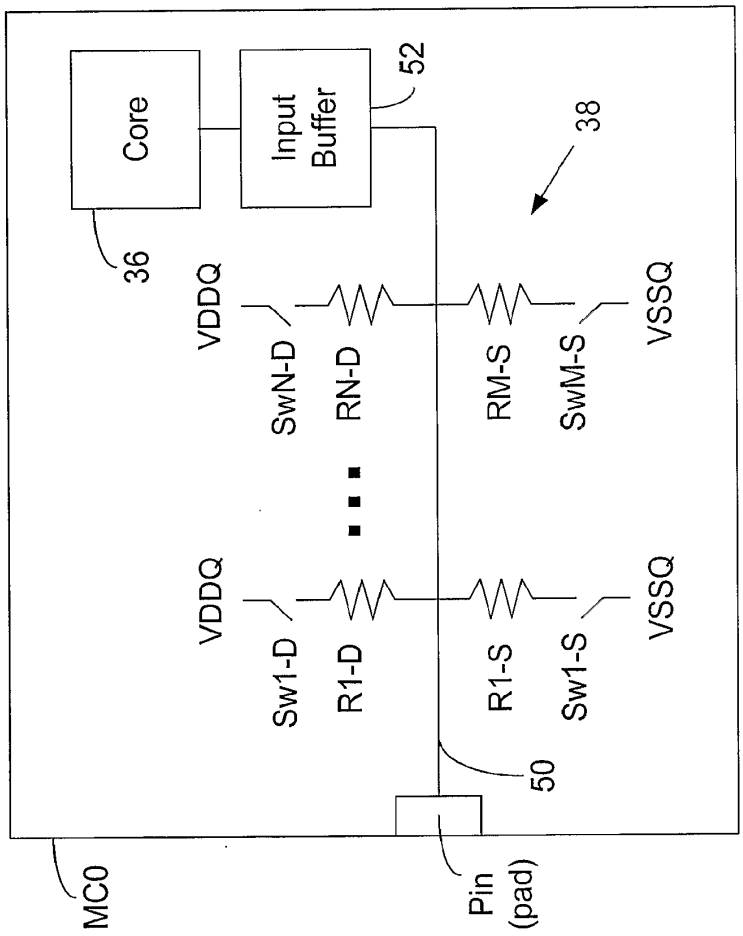

FIG. 4

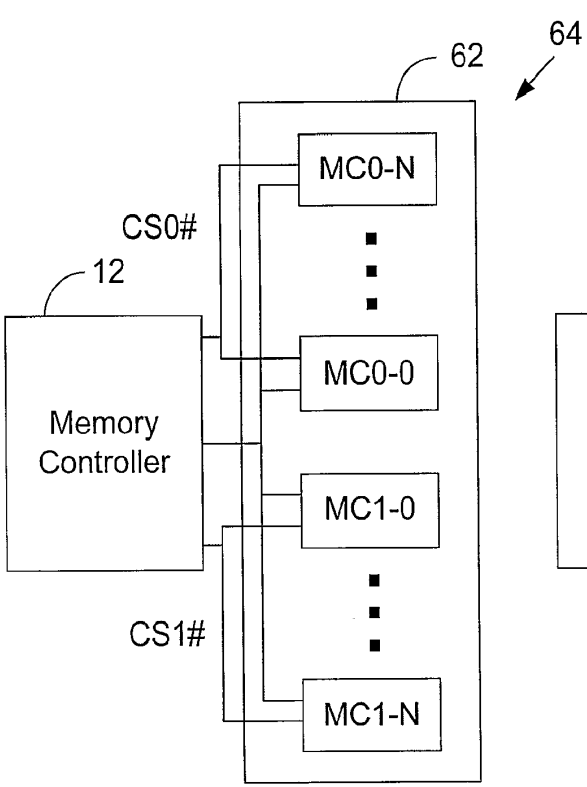

FIG. 5

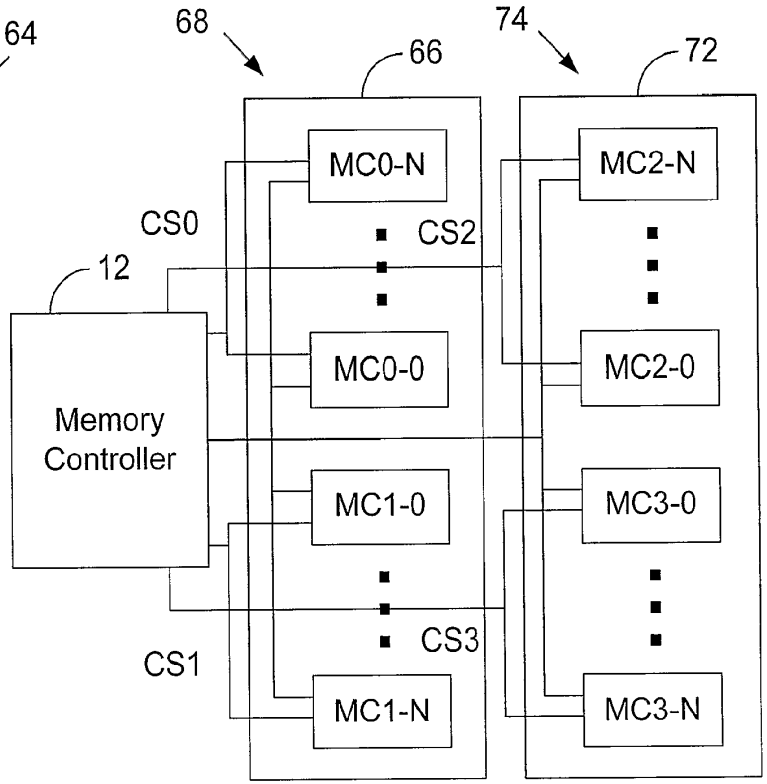

FIG. 6

Samsung Electronics Co., Ltd.
Ex. 1010, p. 764

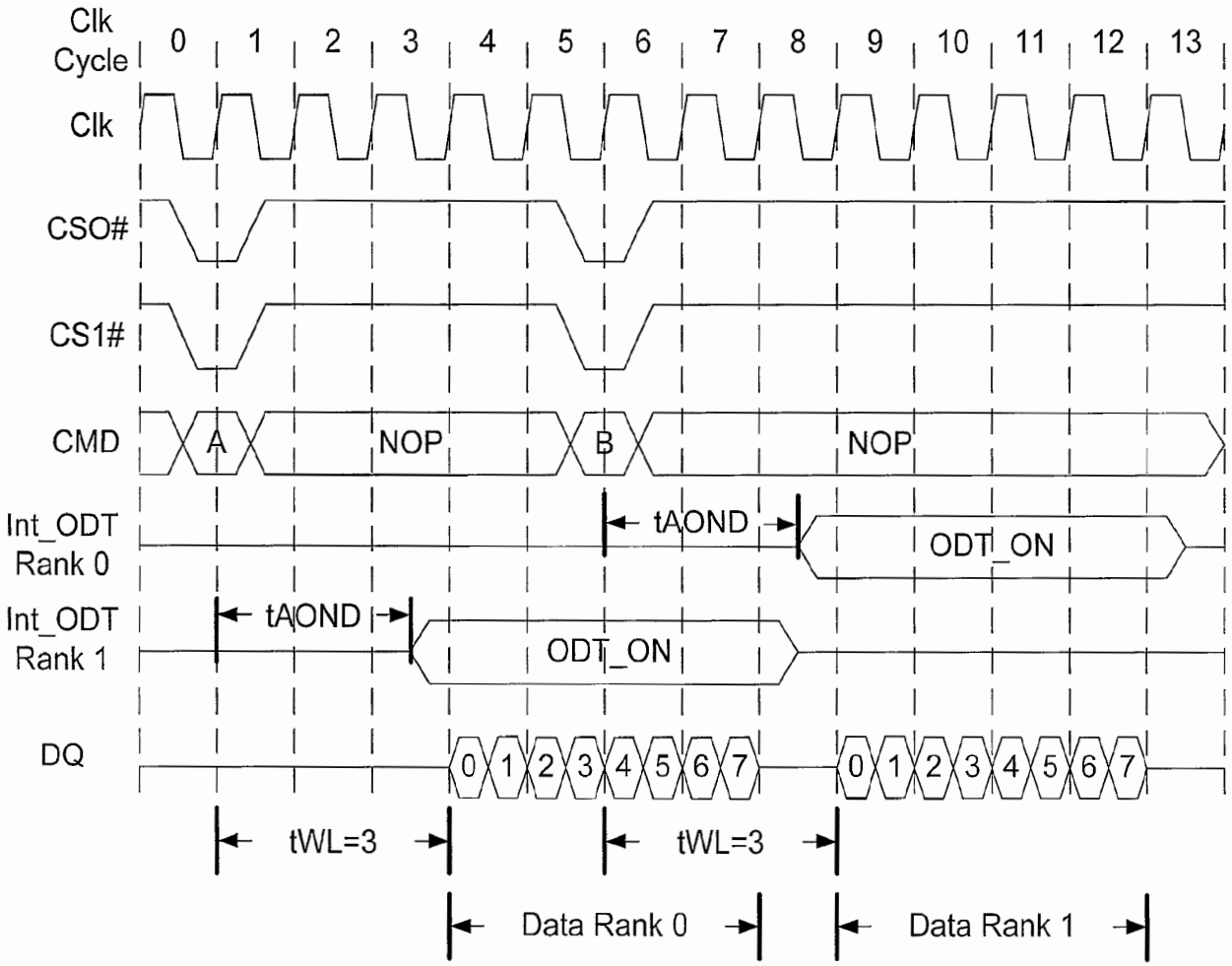

FIG. 7

Samsung Electronics Co., Ltd.
Ex. 1010, p. 765

FIG. 8

FIG. 9

Samsung Electronics Co., Ltd.
Ex. 1010, p. 766

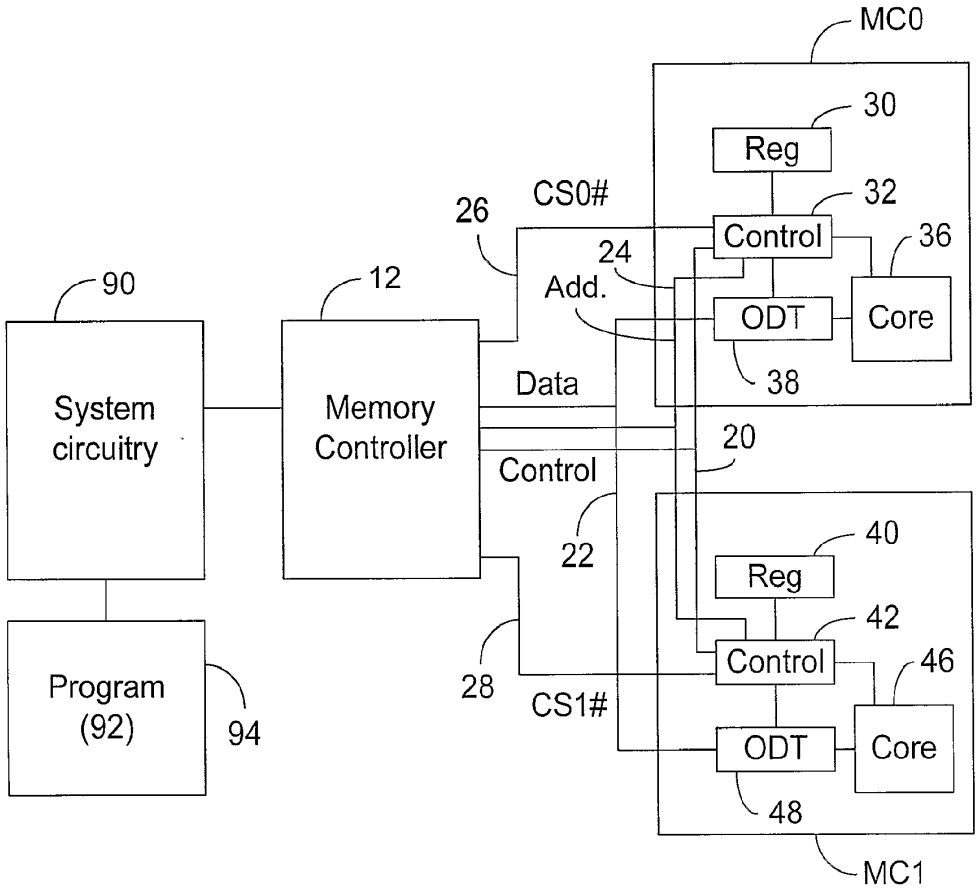

FIG. 10

Samsung Electronics Co., Ltd.
Ex. 1010, p. 767

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
Delaney, Karoline A.
KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, CA 92614
ETATS-UNIS D'AMERIQUE

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 27 September 2010 (27-09-2010)
Applicant's or agent's file reference NETL048VPC	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2010/040826	International filing date *(day/month/year)* 1 July 2010 (01-07-2010)
Applicant NETLIST, INC.	

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	VOYé-PICCOLI, Alexandra Tel: +49 (0)89 2399-8003

Form PCT/ISA/220 (July 2009) *(See notes on accompanying sheet)*

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InvineINT
SEP 29 2010
Knobbe, Martens

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Annex B).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, International Phase, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet or sheets containing a complete set of claims in replacement of all the claims previously filed must be submitted.

Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively in Arabic numerals (Section 205(a)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

BNSDOCID: <XS_____201006011P4_I_>

Samsung Electronics Co., Ltd.
Ex. 1010, p. 770

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide*, National Chapters.

BNSDOCID: <XS_____201006011P4_!_>

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
NETL048VPC		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2010/040826	01/07/2010	16/07/2009
Applicant		
NETLIST, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [ ] the text is approved as submitted by the applicant
   [X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 3a
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

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International application No.
PCT/US2010/040826

INTERNATIONAL SEARCH REPORT

Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A memory system and method utilizing one or more memory modules is provided. The memory module (400) includes a plurality of memory devices (412) and a controller (430) configured to receive control information (440) from a system memory controller (420) and to produce module control signals (442). The memory module further includes a plurality of circuits, for example byte-wise buffers (416), which are configured to selectively isolate the plurality of memory devices from the system memory controller. The circuits are operable, in response to the module control signals, to drive write data from the system memory controller to the plurality of memory devices and to merge read data from the plurality of memory devices to the system memory controller. The circuits are distributed at corresponding positions separate from one another.

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/040826

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C5/02 G11C5/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2006/262586 A1 (SOLOMON JEFFREY C [US] ET AL) 23 November 2006 (2006-11-23) the whole document	1-10, 18-44 11-17
X	US 2008/162790 A1 (IM JEON-TAEK [KR]) 3 July 2008 (2008-07-03) paragraphs [0069] - [0088]; figures 11,12	1-5, 10-21, 23-31, 34-44
A		6-9,22, 32,33
X	US 2009/103387 A1 (SHAU JENG-JYE [US]) 23 April 2009 (2009-04-23) paragraphs [0026] - [0032]	1,18,28, 39

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2010	27/09/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Trifonov, Antoniy

Form PCT/ISA/210 (second sheet) (April 2005)

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Ex. 1010, p. 774

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/040826

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006262586 A1	23-11-2006	US 2009201711 A1	13-08-2009
		US 2010128507 A1	27-05-2010
US 2008162790 A1	03-07-2008	CN 101221809 A	16-07-2008
		KR 20080062174 A	03-07-2008
US 2009103387 A1	23-04-2009	NONE	

Form PCT/ISA/210 (patent family annex) (April 2005)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/040826	01.07.2010	16.07.2009

International Patent Classification (IPC) or both national classification and IPC
INV. G11C5/02 G11C5/06

Applicant
NETLIST, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Trifonov, Antoniy Telephone No. +49 89 2399-7168

Form PCT/ISA/237 (Cover Sheet) (July 2009)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed

   ☐ together with the international application in electronic form

   ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1-44
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-44
Industrial applicability (IA)	Yes:	Claims	1-44
	No:	Claims	

2. Citations and explanations

see separate sheet

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Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Samsung Electronics Co., Ltd.
Ex. 1010, p. 778

Re Item V.

1 Reference is made to the following documents:

D1 US 2006/262586 A1 (SOLOMON JEFFREY C [US] ET AL) 23 November 2006 (2006-11-23)

D2 US 2008/162790 A1 (IM JEON-TAEK [KR]) 3 July 2008 (2008-07-03)

D3 US 2009/103387 A1 (SHAU JENG-JYE [US]) 23 April 2009 (2009-04-23)

2 A plurality of claims in the present application attempt to define the subject-matter by merging a plurality of data signals from the memory devices and driving the merged data signal to the computer system memory controller. However, the term merging is not correctly used since an impression could be conveyed of some kind of "twisting" of the data connections or even driving/ multiplexing signals from different ranks into one single data line, e.g. as shown on Fig. 4B lines 452 (0:3&4-7) being driven onto the lines 450 (0:3). For the purpose of further examination therefore the merging will be considered as nothing but a "logical" combination of two independent transmission data circuits, each driving its own connection lines (in the case of Fig. 4B, the left half of 416 drives all and only lines 0-3 and the right half drives only lines 4-7).

3 Independent claim 39 specifies a "load reducing switching circuit". Since no technical features for supporting said "load reducing" are included in the claim, this term will not be considered for further examination.

4 The present application does not meet the criteria of Article 33(1) PCT, for the following reasons:

4.1 Document D1 discloses a memory module comprising:
- at least one printed circuit board (10);

- a plurality of memory devices mechanically coupled to the at least one printed circuit board (32);

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- a control circuit (a part of 40 , e.g. 122 generating control signals for switching circuits 120) mechanically coupled to the at least one printed circuit board, the control circuit configurable to receive control signals from a system memory controller and to transmit module control signals to the plurality of memory devices (see Fig. 9A); and

- a plurality of data transmission circuits (120, 120a, 120b) mechanically coupled to the at least one printed circuit board and distributed at corresponding positions relative to the at least one printed circuit board, the plurality of data transmission circuits configurable to be operatively coupled to the system memory controller and configurable to receive module control signals from the control circuit,

wherein at least one first data transmission circuit (see 120a on Fig. 4A and par. [0052], wherein the line 102a represents a set of data lines coupled to the plurality of memory devices 30) of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices (30), at least one second data transmission circuit (120b) of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices (30),

wherein the at least one first data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller and at least one selected memory device of the at least two memory devices operatively coupled to the at least one first data transmission circuit, and the at least one second data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller and at least one selected memory device of the at least two memory devices operatively coupled to the at least one second data transmission circuit (the circuits 120a and 120b isolate the data lines 102a and 102b of respectively ranks 32a and 32b from the common data line(s) 112, see also par. [0054]).

D2 discloses also (see Fig. 12) a memory module comprising a printed circuit board (510), a plurality of memory devices (511), a control circuit (513, 514, 516) and a plurality of data transmission circuits (515) connected as required in claim 1 in the present application.

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Claim 1 is therefore not new in the sense of Article 33(2) PCT.

4.2 Since the data transmission circuits (or equivalent "switching circuits") of D1 and D2 are used for:
- isolating one or more of the loads of the memory devices from the computer system (see D1: pars.[0040, 41] and D2: par. [0072]),
- for bidirectional data transfer between a memory controller and memory devices (i.e. for read and write operations), and for
- "merging" read data (see Figs. 1 and 4A in D1, wherein the circuit 40 comprises a plurality of sub-circuits for multiplexing/de-multiplexing of lines (102) onto common lines (112). If the memory devices' output bus is 4 bit wide and the module output bus 64 bit, the data from the memory devices can be considered as "merged" on the memory module data bus),
the subject-matter of claims 18, 28 and 39 is also not new compared to the prior art of D1 and D2.

4.3 The memory devices in D1 can have different configurations (par. [0108]), e.g. 128Mx8bit or 128Mx4bit and the memory module can operate as a data path rank buffer (par. [0055]). Accordingly, the data transmission circuit of D1 comprises a byte-wise buffer as required in claim 25 in the present application. This and the remaining technical features of claim 25 could therefore be found in D1.

5 The remaining dependent claims 2-17, 19-24, 26, 27, 29-38, 40-44 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/ or inventive step (Article 33(2) and (3) PCT).

Re Item VII.

6 The independent claims are not in the two-part form in accordance with Rule 6.3(b) PCT.

7 Reference signs are not inserted in parentheses in the claims in accordance with Rule 6.2(b) PCT.

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8 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in documents D1 - D3 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII.

9 The various definitions of the invention given in the independent claims are such that the claims as a whole are not concise so that the requirements of Article 6 PCT are not met.

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Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

BNSDOCID: <XS_____200704010CK_I_>

US 20060262586A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0262586 A1**

Solomon et al. (43) **Pub. Date: Nov. 23, 2006**

(54) **MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION**

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(21) Appl. No.: **11/335,875**

(22) Filed: **Jan. 19, 2006**

Related U.S. Application Data

(63) Continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, and which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004. Provisional application No. 60/550,668, filed on Mar. 5, 2004. Provisional application No. 60/575,595, filed on May 28, 2004. Provisional application No. 60/590,038, filed on Jul. 21, 2004. Provisional application No. 60/645,087, filed on Jan. 19, 2005.

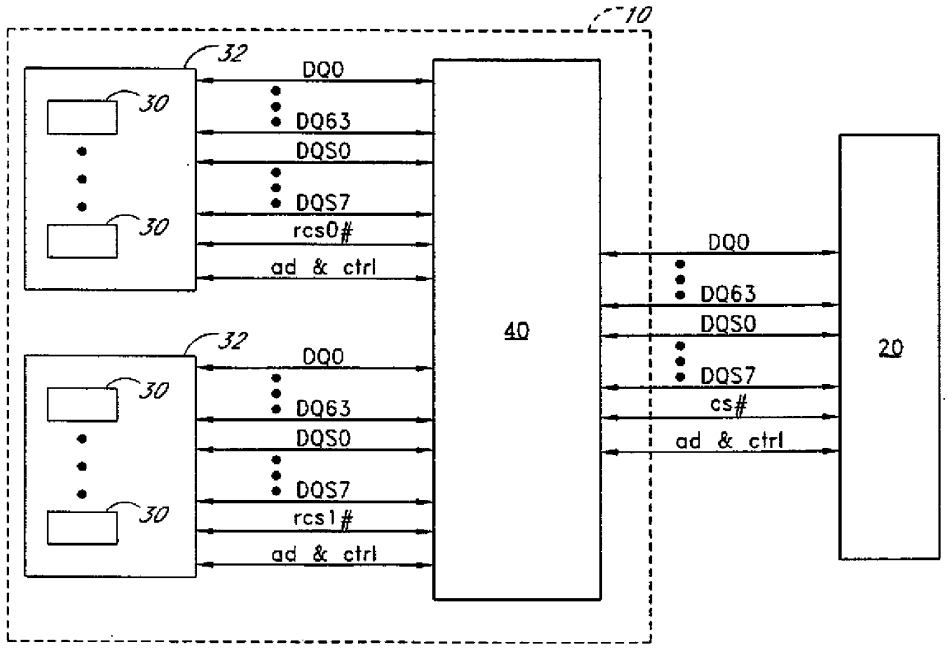
Publication Classification

(51) **Int. Cl.**
G11C 5/06 (2006.01)

(52) **U.S. Cl.** **365/63**

(57) **ABSTRACT**

A memory module includes a plurality of memory devices and a circuit. Each memory device has a corresponding load. The circuit is electrically coupled to the plurality of memory devices and is configured to be electrically coupled to a memory controller of a computer system. The circuit selectively isolates one or more of the loads of the memory devices from the computer system. The circuit comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.



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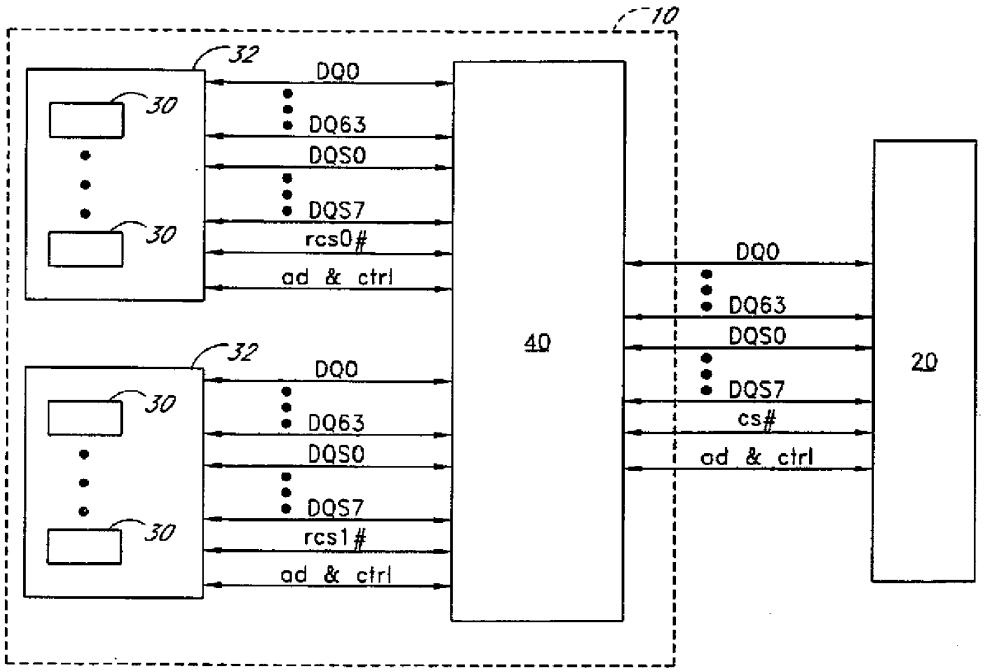

FIG. 1

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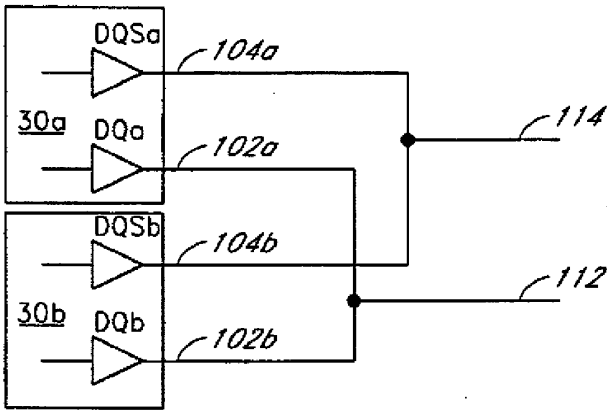

FIG. 2

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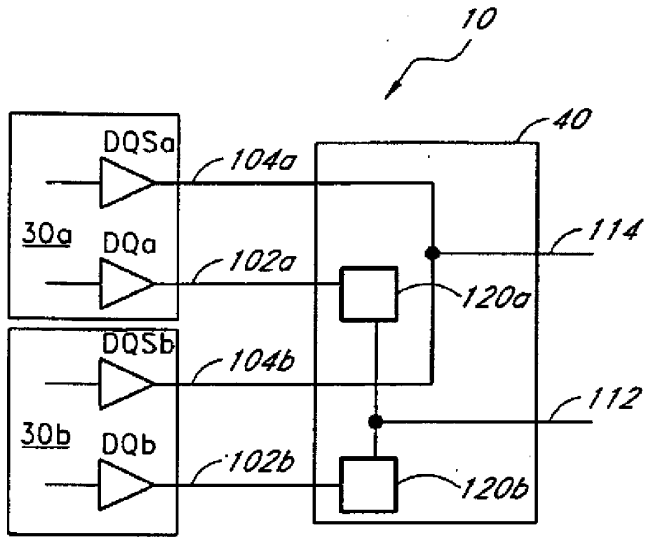

FIG. 3A

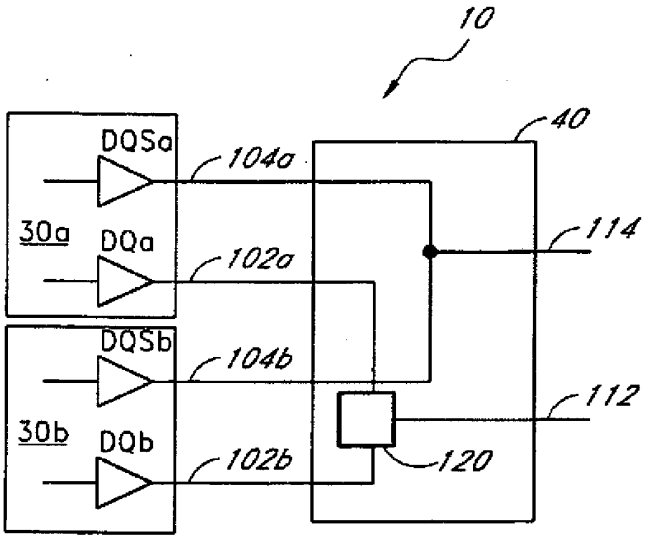

FIG. 3B

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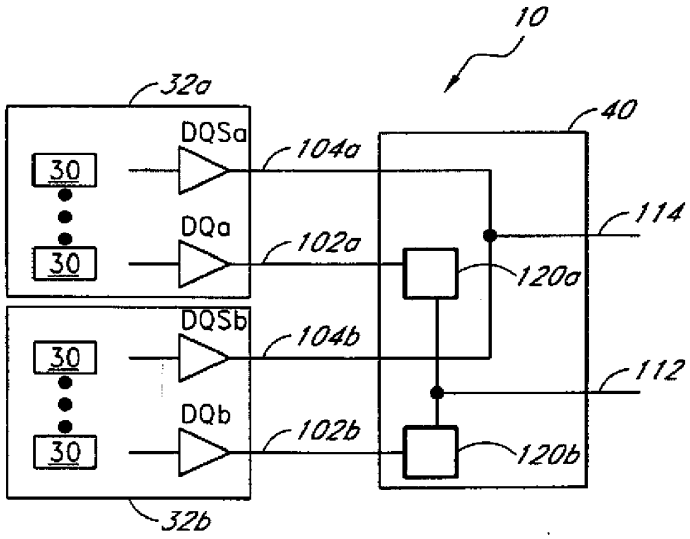

FIG. 4A

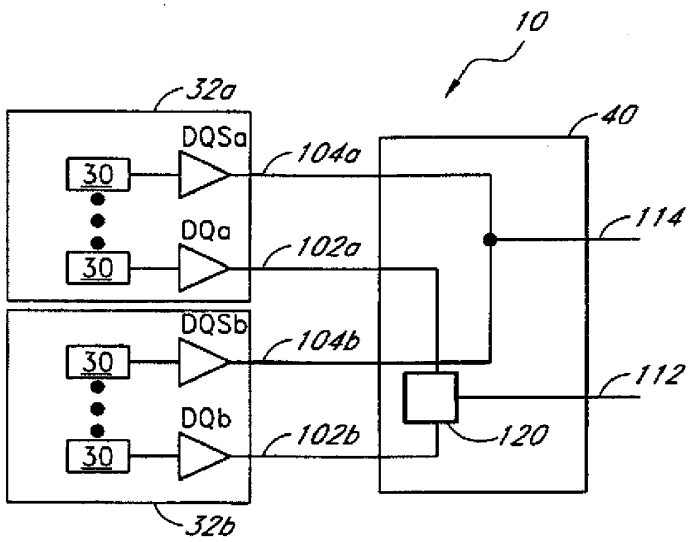

FIG. 4B

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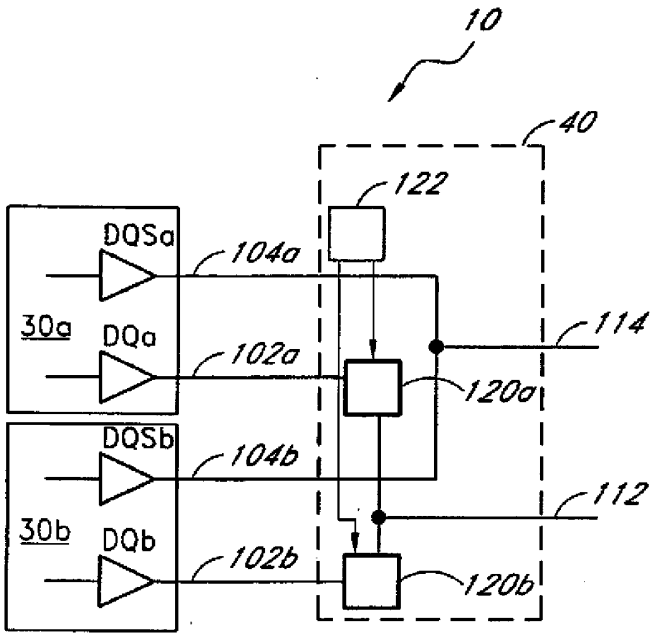

FIG. 5A

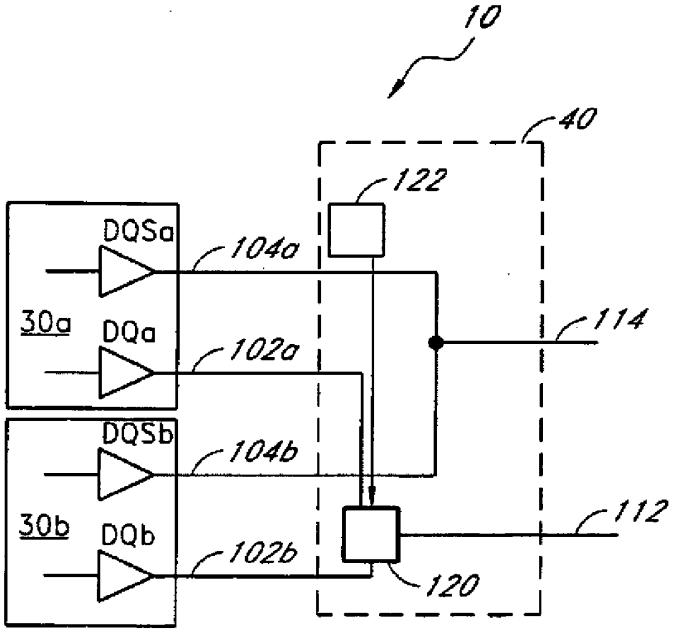

FIG. 5B

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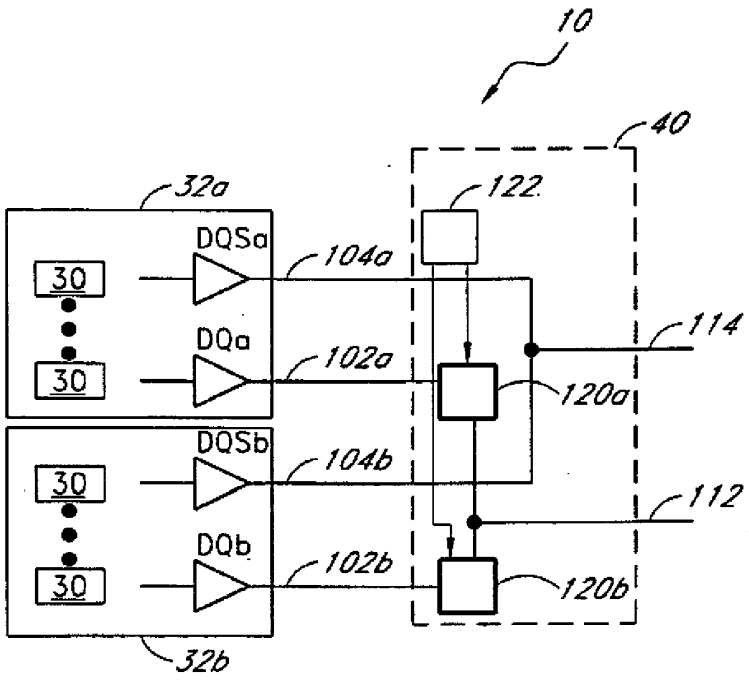

FIG. 5C

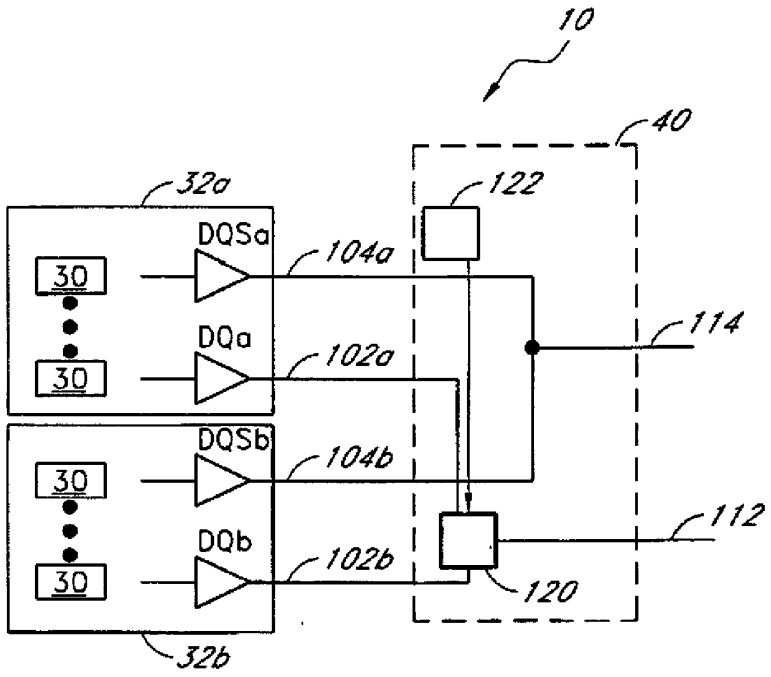

FIG. 5D

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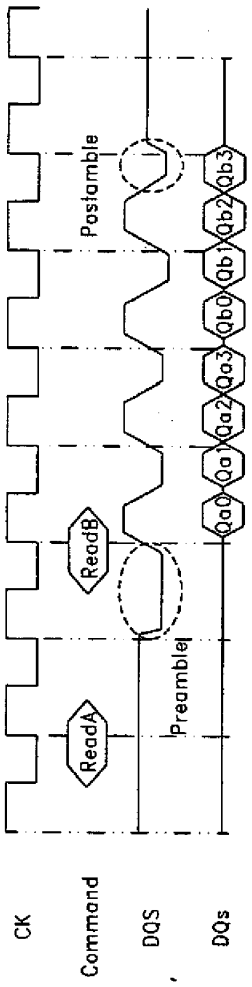

FIG. 6A

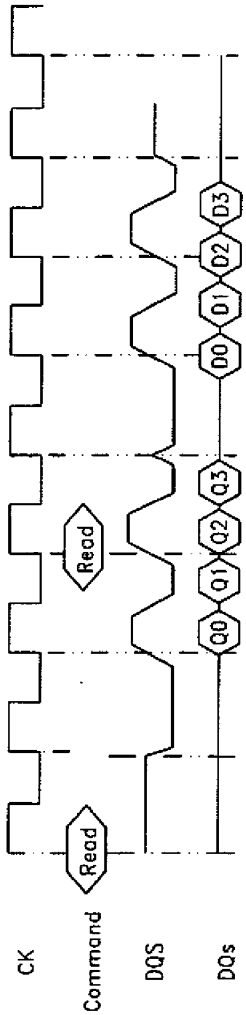

FIG. 6B

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BNSDOCID: <US____20060262586A1_I_>

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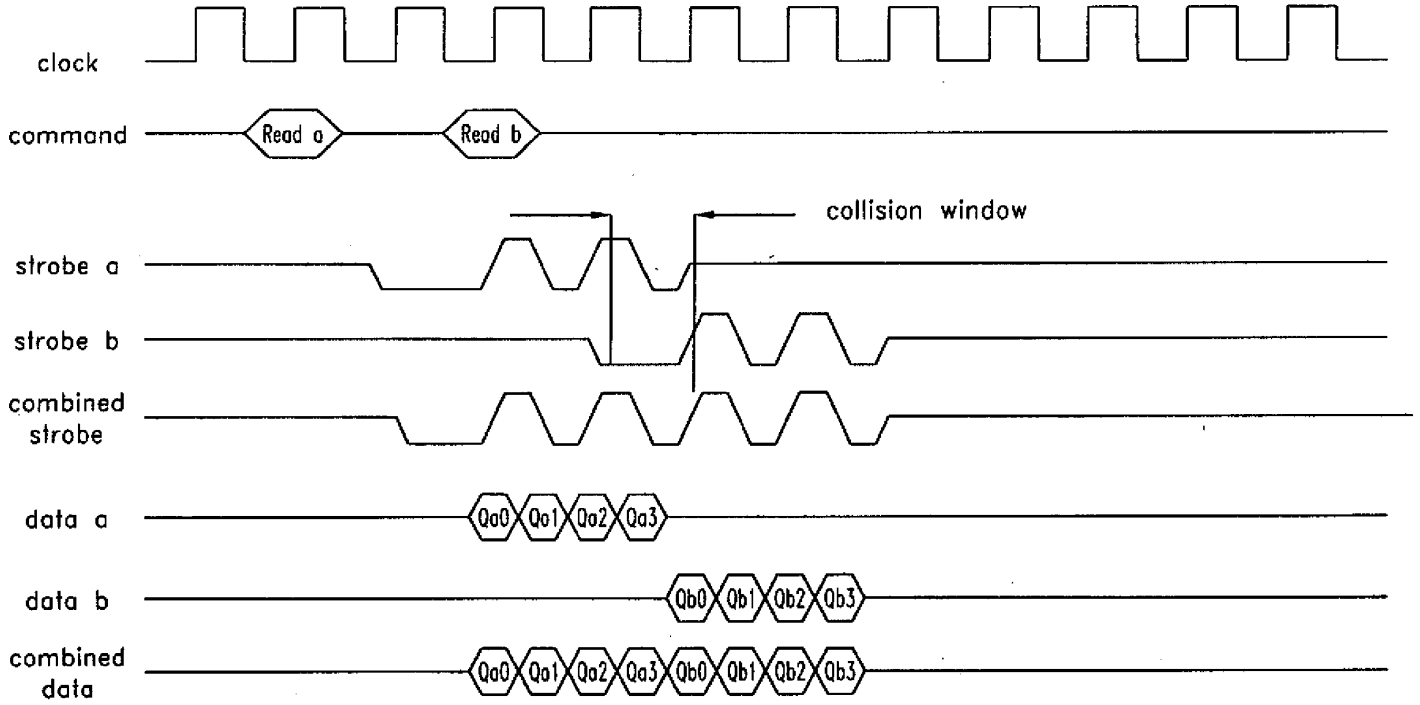

FIG. 7

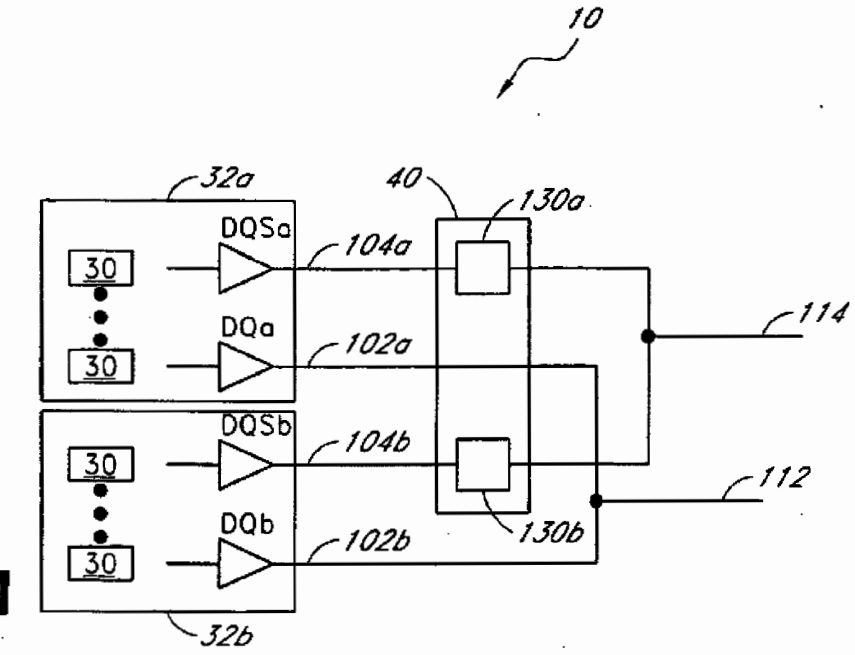

FIG. 8A

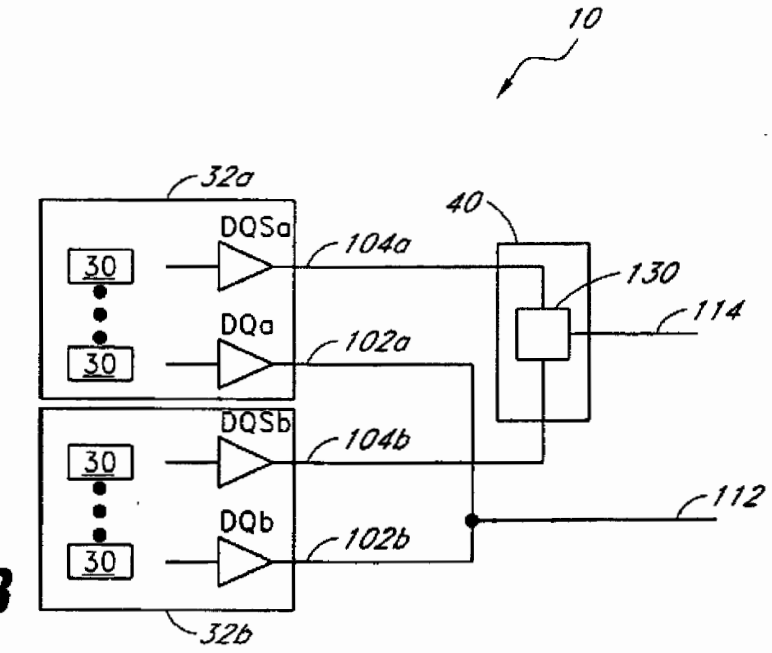

FIG. 8B

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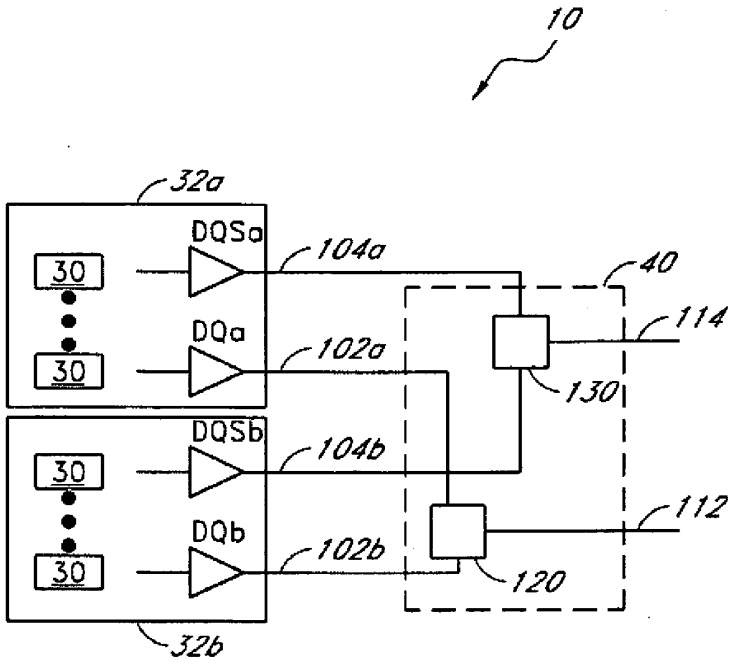

FIG. 8C

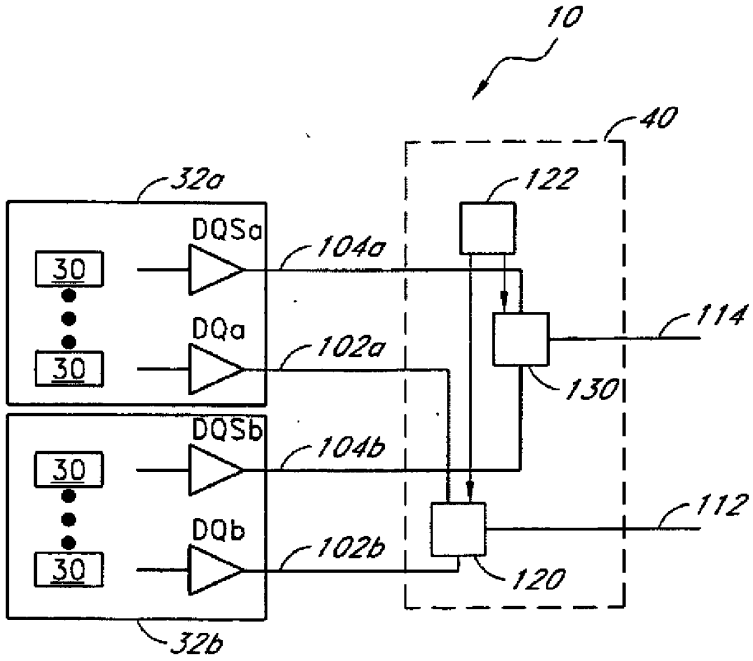

FIG. 8D

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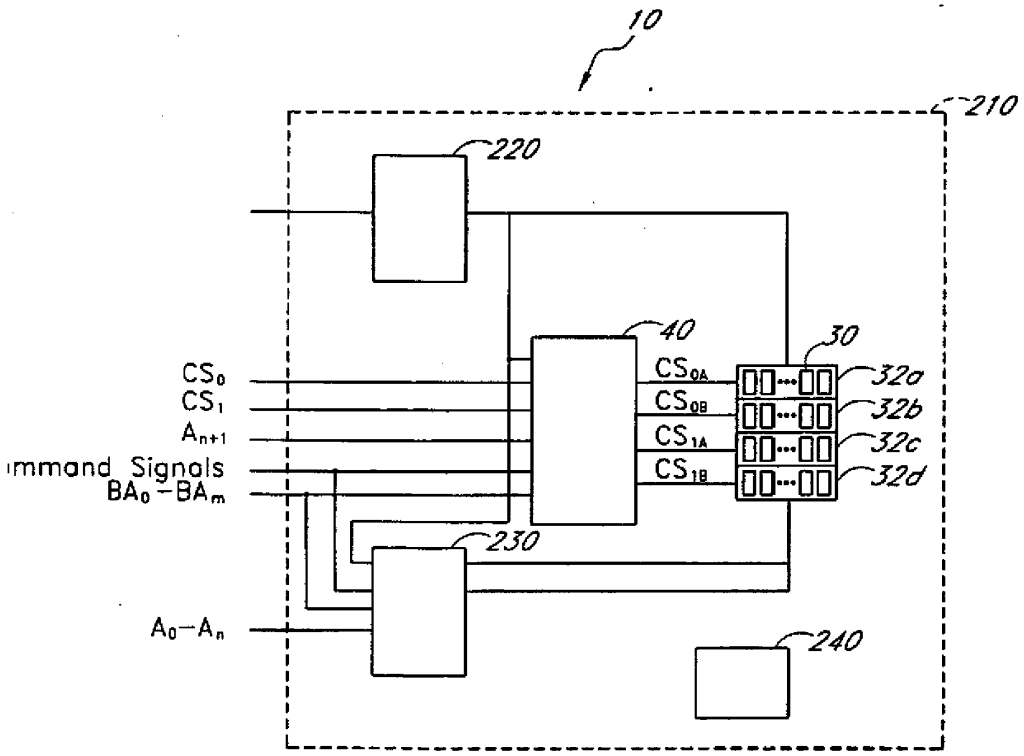

FIG. 9A

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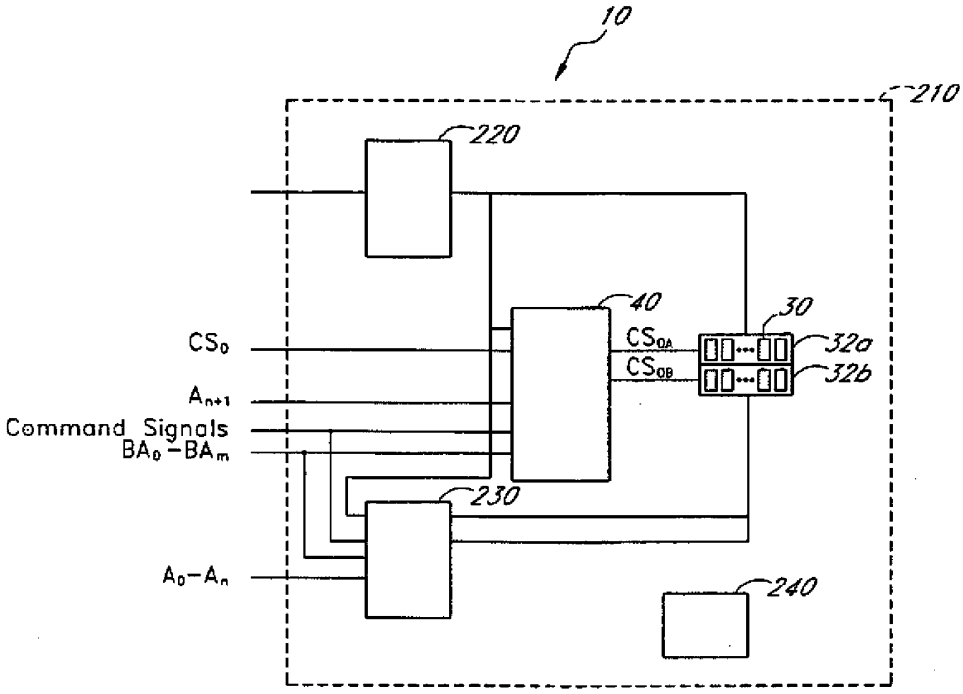

FIG. 9B

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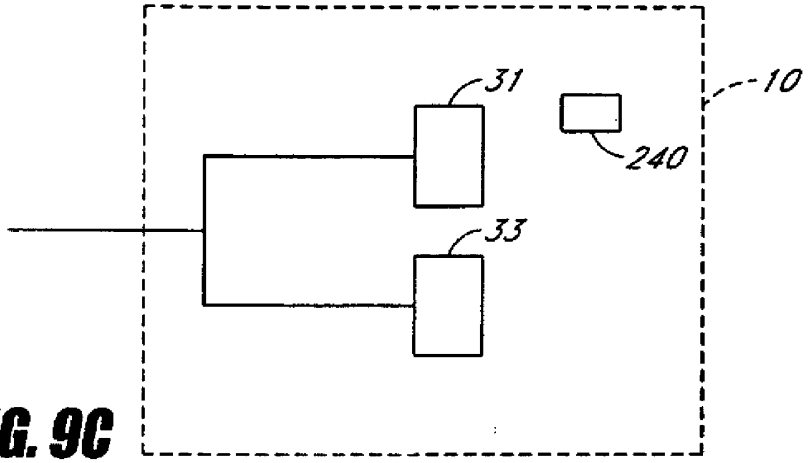

FIG. 9C

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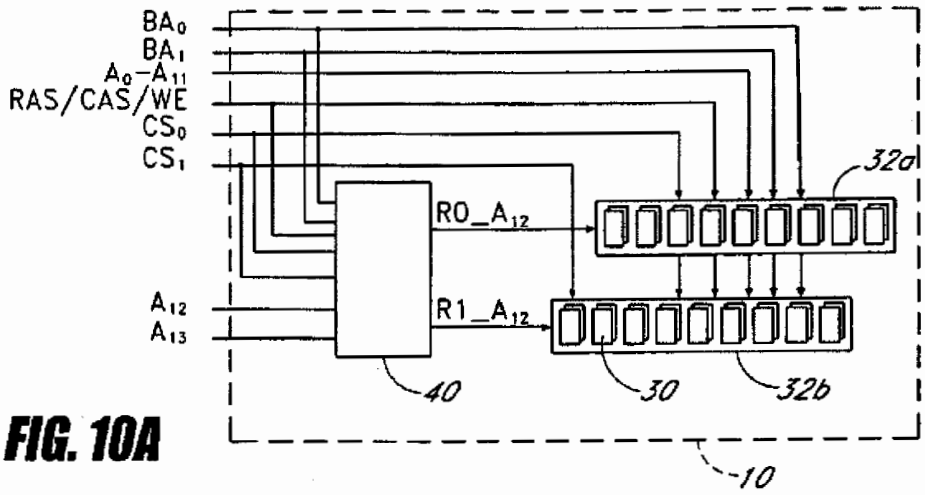

FIG. 10A

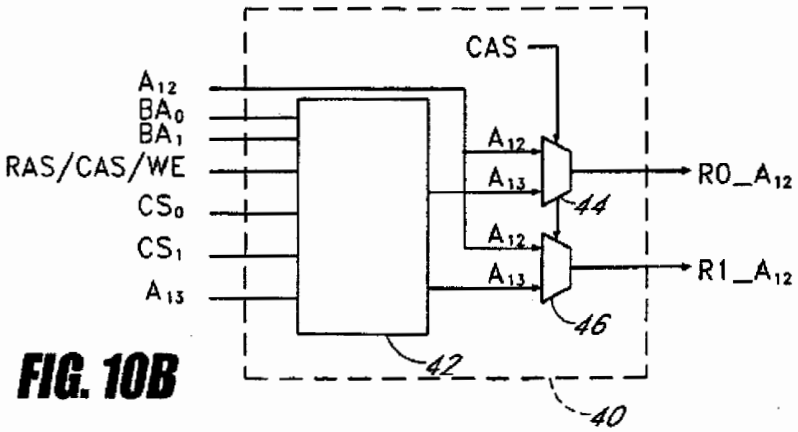

FIG. 10B

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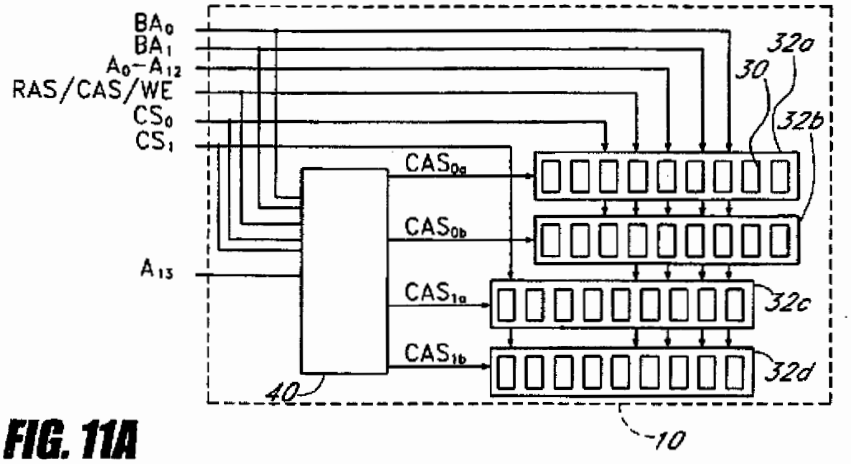

FIG. 11A

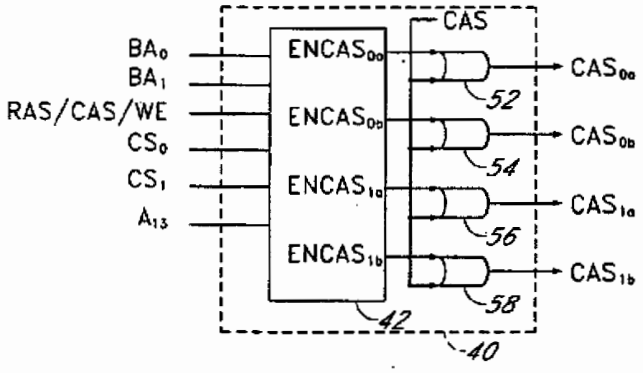

FIG. 11B

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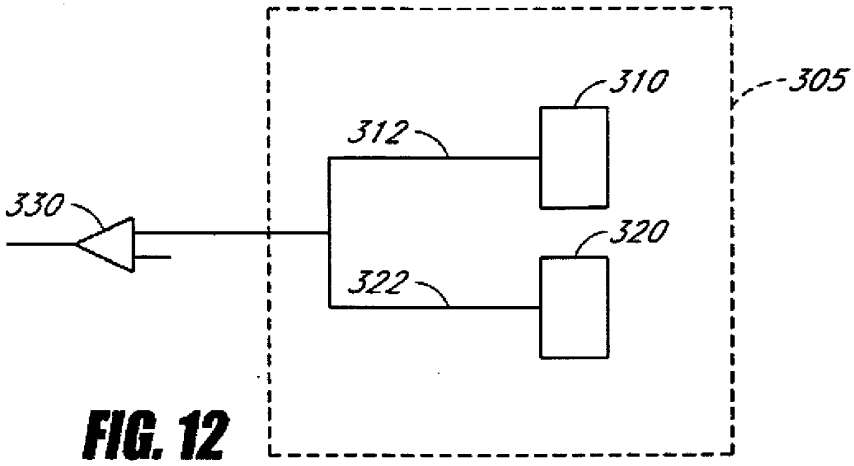

FIG. 12

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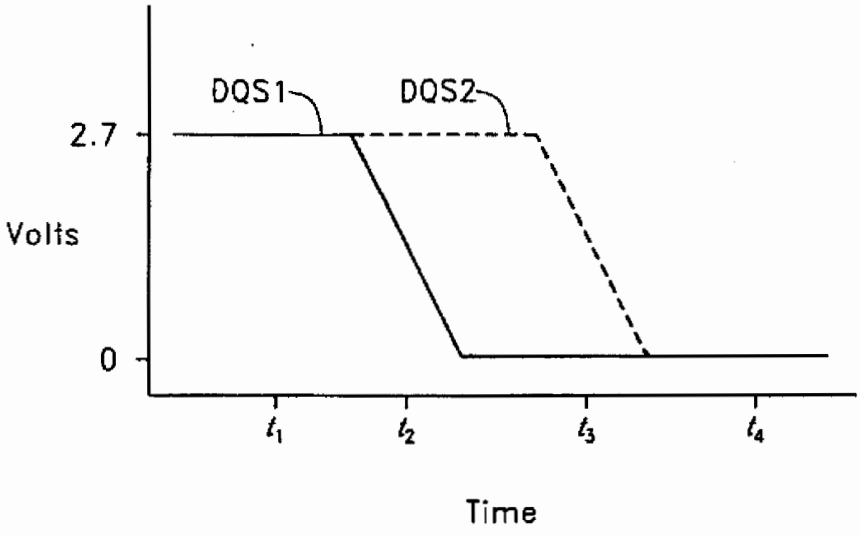

FIG. 13

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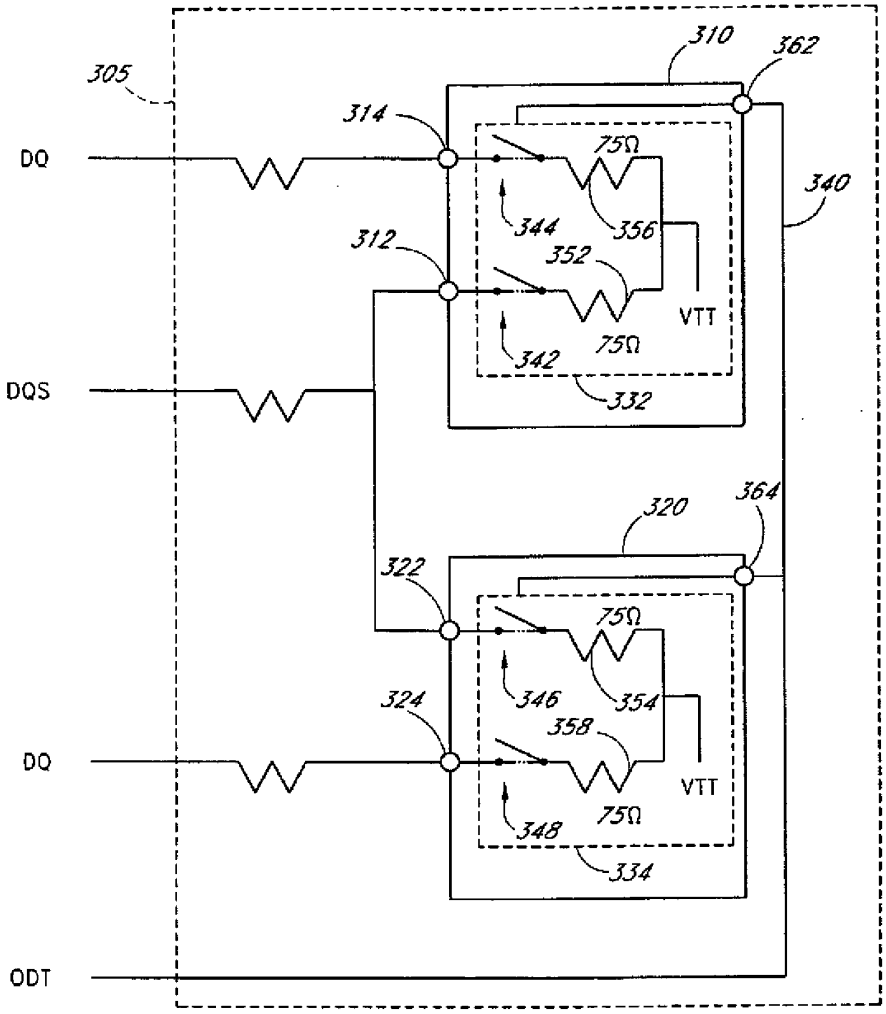

FIG. 14

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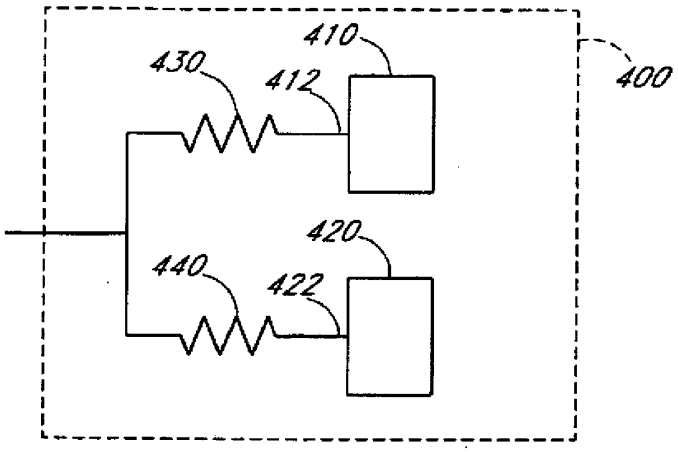

FIG. 15A

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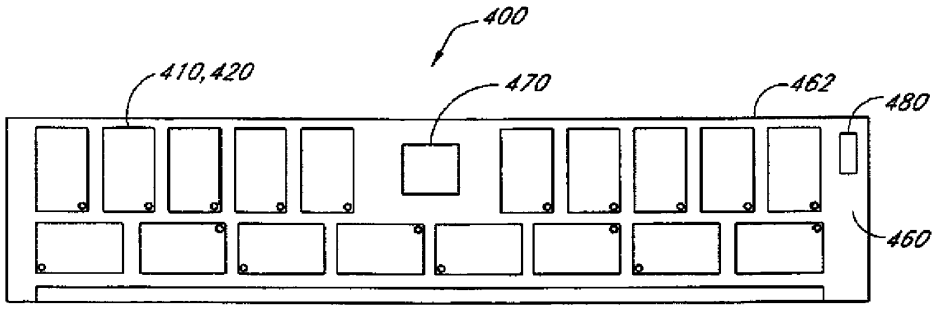

FIG. 16A

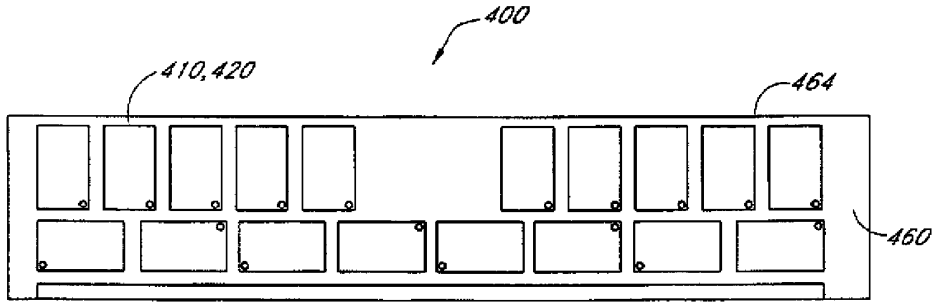

FIG. 16B

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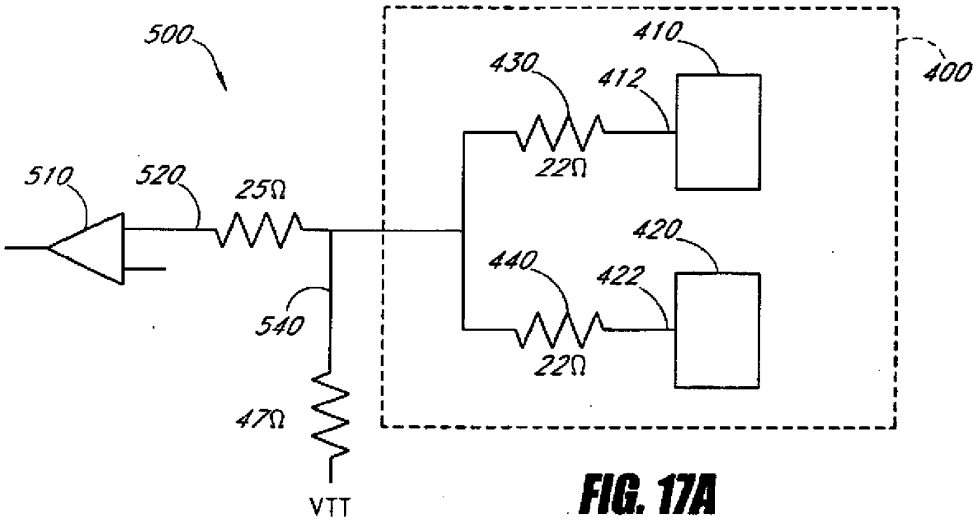

FIG. 17A

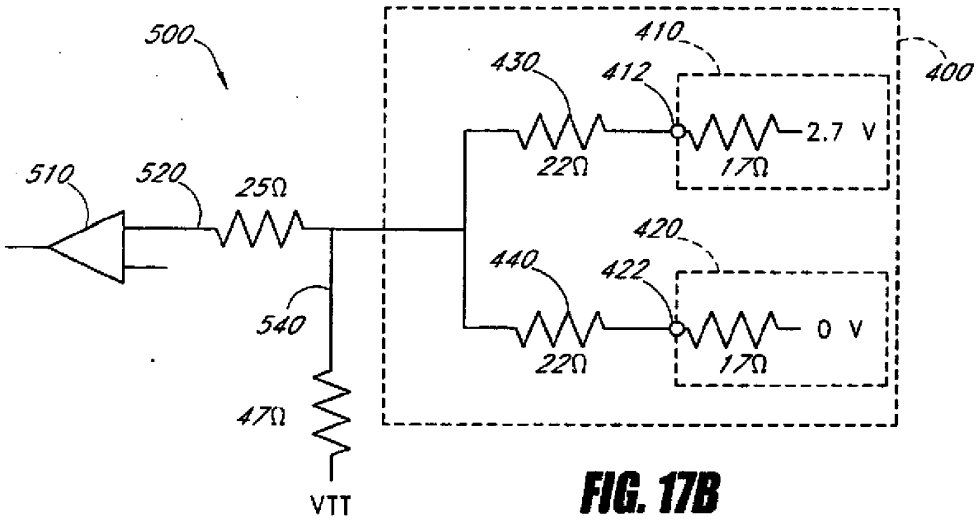

FIG. 17B

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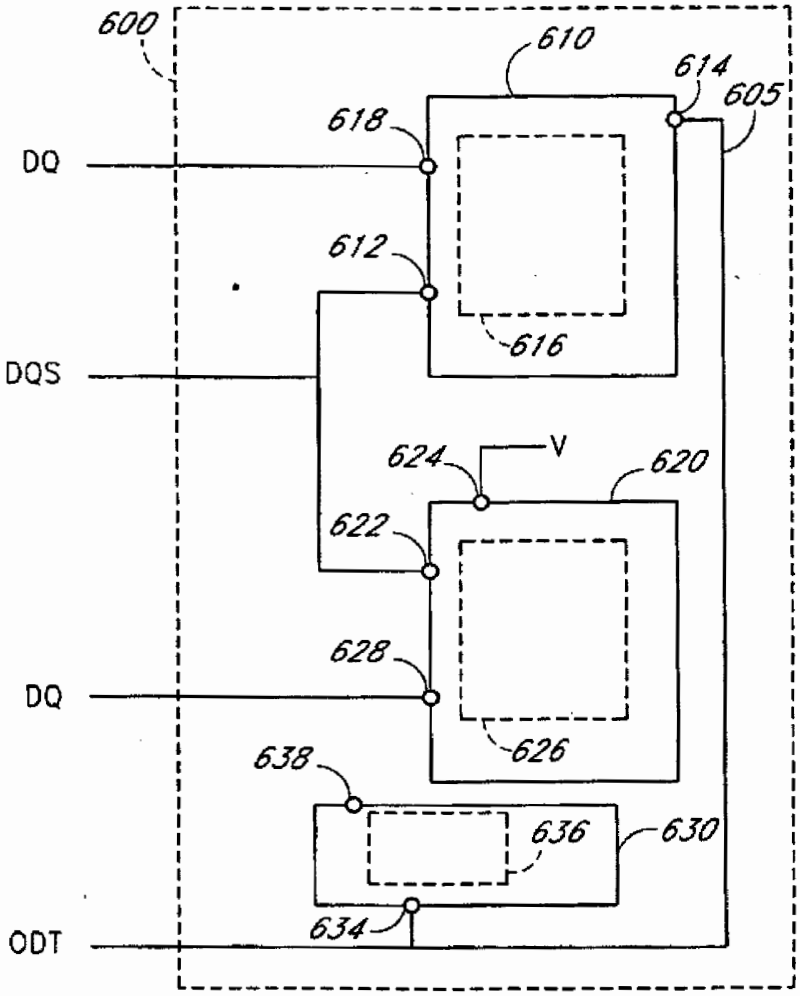

FIG. 18

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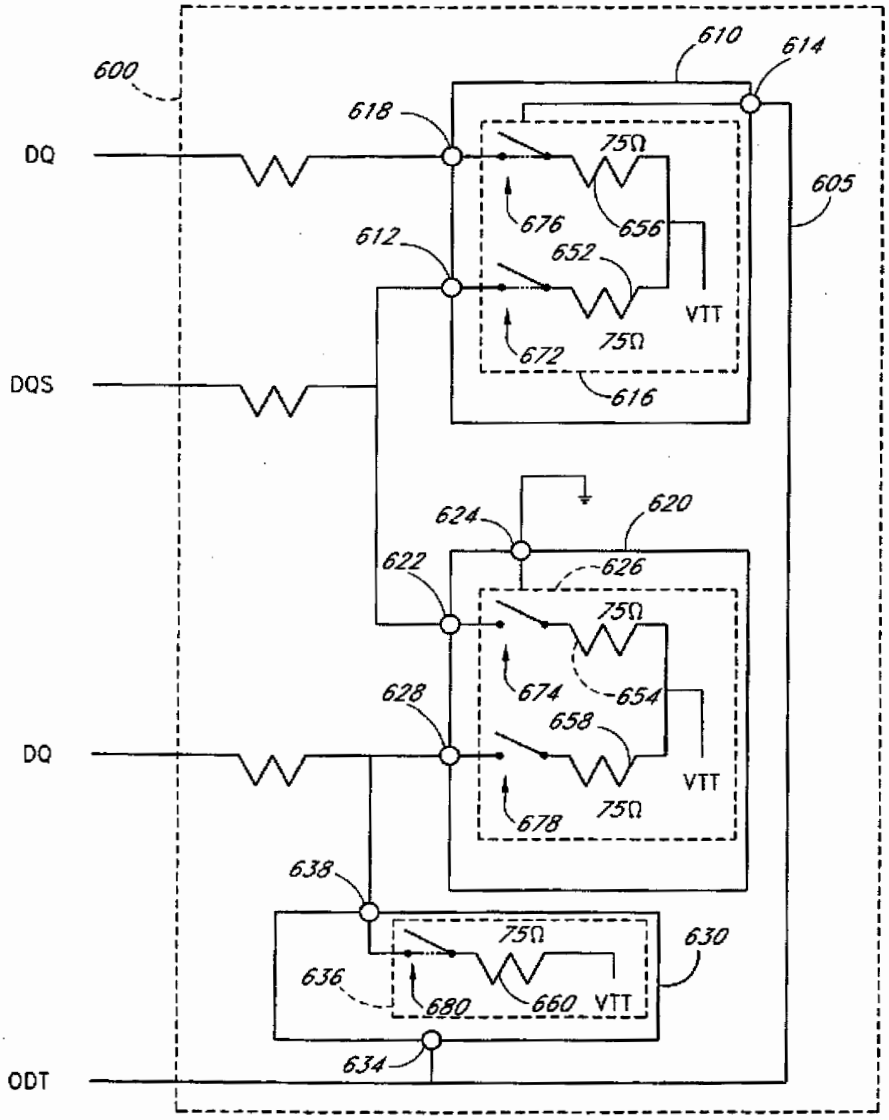

FIG. 19

BNSDOCID: <US____20060262586A1_I_>

MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation-in-part of U.S. patent application Ser. No. 11/173,175, filed Jul. 1, 2005, which claims the benefit of U.S. Provisional Application No. 60/588,244, filed Jul. 15, 2004 and which is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005, which claims the benefit of U.S. Provisional Application No. 60/550,668, filed Mar. 5, 2004, U.S. Provisional Application No. 60/575,595, filed May 28, 2004, and U.S. Provisional Application No. 60/590,038, filed Jul. 21, 2004. U.S. patent application Ser. Nos. 11/173,175 and 11/075,395, and U.S. Provisional Application Nos. 60/588,244, 60/550,668, 60/575,595, and 60/590,038 are each incorporated in its entirety by reference herein. The present application also claims the benefit of U.S. Provisional Application No. 60/645,087, filed Jan. 19, 2005, which is incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

[0004] 2. Description of the Related Art

[0005] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0006] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in fourbanks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64M×8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M×8-byte" configuration or a "64M×64-bit" configuration, with a depth of 64M and a width of 8 bytes or 64 bits.

[0007] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128M×8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M×8-byte" configuration or a "128M×64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0008] The commercially-available 512-MB (64M×8-byte) memory modules and the 1-GB (128M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

[0009] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

[0010] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a: memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0011] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0012] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0013] In certain embodiments, a memory module comprises a plurality of memory devices and a circuit. Each memory device has a corresponding load. The circuit is electrically coupled to the plurality of memory devices and is configured to be electrically coupled to a memory controller of a computer system. The circuit selectively isolates one or more of the loads of the memory devices from the computer system. The circuit comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

[0014] In certain embodiments, a method of using a memory module with a computer system is provided. The method comprises providing a memory module having a plurality of memory devices and a circuit. The circuit is electrically coupled to the plurality of memory devices. The circuit is configured to be electrically coupled to a computer system. Each memory device has a corresponding load. The method further comprises electrically coupling the memory module to the computer system. The method further comprises activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module.

[0015] In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The device selectively electrically couples the first data signal line to the common data signal line and selectively electrically couples the second data signal line to the common data signal line. The device comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIG. 1** schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0017] **FIG. 2** schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0018] **FIGS. 3A and 3B** schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

[0019] **FIGS. 4A and 4B** schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0020] **FIGS. 5A-5D** schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0021] **FIG. 6A** shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0022] **FIG. 6B** shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0023] **FIG. 7** shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0024] **FIGS. 8A-8D** schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0025] **FIG. 9A** schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0026] **FIG. 9B** schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0027] **FIG. 9C** schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0028] **FIG. 10A** schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0029] **FIG. 10B** schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] **FIG. 11A** schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0031] **FIG. 11B** schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0032] **FIG. 12** schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0033] **FIG. 13** is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0034] **FIG. 14** schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0035] **FIG. 15** schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0036] **FIGS. 16A and 16B** schematically illustrate a first side and a second side, respectively, of a memory module

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with eighteen 64M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0037] **FIGS. 17A and 17B** schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0038] **FIG. 18** schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0039] **FIG. 19** schematically illustrates a particular embodiment of the memory module schematically illustrated by **FIG. 18**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

[0040] **FIG. 1** schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0041] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes,-without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0042] Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0043] Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein ale available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

[0044] In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

[0045] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by **FIG. 1**. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

[0046] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0047] In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic

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element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

[0048] **FIG. 2** schematically illustrates a circuit diagram of two memory devices **30***a*, **30***b* of a conventional memory module showing the interconnections between the DQ data signal lines **102***a*, **102***b* of the memory devices **30***a***30***b* and the DQS data strobe signal lines **104***a*, **104***b* of the memory devices **30***a*, **30***b*. Each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, **FIG. 2** only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b*. The DQ data signal lines **102***a*, **102***b* and the DQS data strobe signal lines **104***a*, **104***b* are typically conductive traces etched on the printed circuit board of the memory module. As shown in **FIG. 2**, each of the memory devices **30***a*, **30***b* has their DQ data signal lines **102***a*, **102***b* electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104***a*, **104***b* electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30***a*, **30***b* concurrently.

[0049] In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

[0050] As schematically illustrated by **FIGS. 3A and 3B**, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102***a*, **102***b* of the two memory devices **30***a*, **30***b* from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102** a of the first memory device **30***a* or a second DQ data signal from the DQ data signal line **102***b* of the second memory device **30***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of **FIGS. 3A and 3B** which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0051] For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** a, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by **FIG. 3A**. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by **FIG. 3B**. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **10***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ signal lines **102***a*, **102***b* to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, **FIGS. 3A and 3B** only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b* for simplicity. The configurations schematically illustrated by **FIGS. 3A and 3B** can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

[0052] In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in **FIGS. 4A and 4B**, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of **FIGS. 4A and 4B** comprises two ranks **32***a*, **32***b*, with each rank **32***a*, **32***b* having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, **FIGS. 4A and 4B** illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

[0053] The circuit **40** of **FIG. 4A** selectively isolates one or more of the DQ data signal lines **102***a*, **102***b* of the two ranks **32***a*, **32***b* from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32***a*, **32***b* via the DQ data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102***a* of the first rank **32***a* and a second DQ data signal from the DQ data signal line **102***b* of the second rank **32***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120***a*, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by **FIG. 4A**. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. In certain other

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embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by **FIG. 4B**. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

[0054] In the example embodiments schematically illustrated by **FIGS. 3A, 3B, 4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by **FIGS. 5A-5D**. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

[0055] In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0056] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0057] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0058] An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

EXAMPLE 1

[0059]

```
//========================== declarations
    reg         rasN_R, casN_R, weN_R;
    wire        actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
    wire        xfr_cmd_R,mrs_cmd,rd_cmd_R;
//------------------------- DDR 2 FET
    reg         brs0N_R;                    // registered chip sel
    reg         brs1N_R;                    // registered chip sel
    reg         brs2N_R;                    // registered chip sel
    reg         brs3N_R;                    // registered chip sel
    wire        sel;
    wire        sel_01;
    wire        sel_23;
    wire        rd_R1;
    wire        wr_cmd_R,wr_R1;
```

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-continued

```
    reg                         rd_R2,rd_R3,rd_R4,rd_R5;
    reg                         wr_R2,wr_R3,wr_R4,wr_R5;
    reg                         enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
    wire                        wr_01_R1,wr_23_R1;
    reg                         wr_01_R2,wr_01_R3,wr_01_R4;
    reg                         wr_23_R2,wr_23_R3,wr_23_R4;
    wire                        rodt0_a,rodt0_b;
//------------------------------ logic
    always @(posedge clk_in)
                begin
                    brs0N_R <= brs0_in_N;   // cs0
                    brs1N_R <= brs1_in_N;   // cs1
                    brs2N_R <= brs2_in_N;   // cs2
                    brs3N_R <= brs3_in_N;   // cs3
                    rasN_R <= brras_in_N ;
                    casN_R <= brcas_in_N ;
                    weN_R <= bwe_in_N ;
                end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R;     // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;    // pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;              // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;     // rnd reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;      // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ;     // write cmd
//-----------------------------------------
assign   rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign   wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1
//-----------------------------------------
    always @(posedge clk_in)
                begin
                    rd_R2 <= rd_R1 ;
                    rd_R3 <= rd_R2;
                    rd_R4 <= rd_R3;
                    rd_R5 <= rd_R4;
//                  rd0_o_R6 <= rd0_o_R5;
                    wr_R2 <= wr_R1 ;
                    wr_R3 <= wr_R2;
                    wr_R4 <= wr_R3;
                    wr_R5 <= wr_R4;
                end
//-----------------------------------------
assign   wr_01_R1 = sel_01 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
assign   wr_23_R1 = sel_23 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
    always @(posedge clk_in)
                begin
                    wr_01_R2 <= wr_01_R1 ;
                    wr_01_R3 <= wr_01_R2;
                    wr_01_R4 <= wr_01_R3;
                    wr_23_R2 <= wr_23_R1 ;
                    wr_23_R3 <= wr_23_R2;
                    wr_23_R4 <= wr_23_R3;
                end
assign   rodt0_ab = (rodt0)             // odt cmd from sys
                    | (wr_23_R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                    | (wr_23_R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                    | (wr_23_R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                    ;
assign   rodt1_ab = (rodt1)             // odt cmd from sys
                    | (wr_01_R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                    | (wr_01_R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                    | (wr_01_R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                    ;
//-----------------------------------------
    always @(posedge clk_in)
                begin
    if (
        | (rd_R2)                           // pre-am rd
        | (rd_R3)                           // 1st cyc of rd brst (cl3)
        | (rd_R4)                           // 2nd cyc of rd brst (cl3)
        | (wr_R1)                           // pre-am wr
        | (wr_R2)                           // wr brst 1st cyc
        | (wr_R3)                           // wr brst 2nd cyc
         ) begin
```

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-continued

```
                enfet1 <= 1'b1;          // enable fet
                enfet2 <= 1'b1;          // enable fet
                enfet3 <= 1'b1;          // enable fet
                enfet4 <= 1'b1;          // enable fet
                enfet5 <= 1'b1;          // enable fet
                enfet6 <= 1'b1;          // enable fet
        end
else
        begin
                enfet1 <= 1'b0;          // disable fet
                enfet2 <= 1'b0;          // disable fet
                enfet3 <= 1'b0;          // disable fet
                enfet4 <= 1'b0;          // disable fet
                enfet5 <= 1'b0;          // disable fet
                enfet6 <= 1'b0;          // disable fet
        end
end
```

Back-to-Back Adjacent Read Commands

[0060] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. **FIG. 6A** shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0061] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of **FIG. 6B** for successive read accesses from different memory devices.

[0062] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0063] In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in **FIG. 7**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0064] **FIGS. 8A-8D** schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104***a*, **104***b* of two ranks **32***a*, **32***b* from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104***a*, **104***b* of **FIGS. 8A-8D** correspond to two ranks **32***a*, **32***b* of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104***a*, **104***b* corresponding to two individual memory devices **30***a*, **30***b*.

[0065] **FIG. 8A** schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104***a*, **104***b* from one another during the transition from the first read data burst of one rank **32***a* of memory devices **30** to the second read data burst of another rank **32***b* of memory devices **30**.

[0066] In certain embodiments, as schematically illustrated by **FIG. 8A**, the circuit **40** comprises a first switch **130** a electrically coupled to a first DQS data strobe signal line **104***a* of a first rank **32***a* of memory devices **30** and a second switch **130***b* electrically coupled to a second DQS data strobe signal line **104***b* of a second rank **32***b* of memory devices **30**. In certain embodiments, the time for switching the first switch **130***a* and the second switch **130***b* is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32***a* and before the first DQS data strobe of the read data burst of the second rank **32***b*). During the read data burst for the first rank **32***a*, the first switch **130***a* is enabled. After the last DQS data strobe

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of the first rank **32***a* and before the first DQS data strobe of the second rank **32***b*, the first switch **130***a* is disabled and the second switch **130***b* is enabled.

[0067] As shown in **FIG. 8A**, each of the ranks **32***a*, **32***b* otherwise involved in a BBARX collision have their DQS data strobe signal lines **104***a*, **104***b* selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104***a*, **104***b* of the two ranks **32***a*, **32***b* of memory devices **30** from one another to avoid a BBARX collision.

[0068] In certain embodiments, as schematically illustrated by **FIG. 8B**, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104***a*, **104***b* from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104***a*, to the second DQS data strobe signal line **104***b*, or to both DQS data strobe signal lines **104***a*, **104***b*. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32***a* of memory devices **30** and a second DQS data strobe signal from a second rank **32***b* of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

[0069] In certain embodiments, the circuit **40** also provides the load isolation described above in reference to **FIGS. 1-5**. For example, as schematically illustrated by **FIG. 8C**, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102***a*, **102***b* and the switch **130** for the DQS data strobe signal lines **104***a*, **104***b*. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by **FIG. 8D**. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

[0070] The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104***a*, **104***b* by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104***a*, **104***b* to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102***a*, **102***b* to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

[0071] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64Mx8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64Mx4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0072] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0073] **FIG. 9A** schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality-of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

[0074] In certain embodiments, as schematically illustrated in **FIG. 9A**, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230**. The register **230**

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receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

[0075] In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0076] In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

[0077] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32***a*, **32***b*, **32***c*, **32***d*, as schematically illustrated by **FIG. 9A**. In certain other embodiments, the memory devices **30** are arranged in two ranks **32***a*, **32***b*, as schematically illustrated by **FIG. 9B**. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

[0078] As schematically illustrated by **FIGS. 9A and 9B**, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

[0079] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by **FIG. 9A**, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of **FIG. 9B**, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0080] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by **FIG. 9A**. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by **FIG. 9B**.

[0081] In the exemplary embodiment schematically illustrated by **FIG. 9A**, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0-CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0082] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

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[0083] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. Cs_{0A} is pulled low, thereby selecting Rank 0.

[0084] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

[0085] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

[0086] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

[0087] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

[0088] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

[0089] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0090] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0091] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0092] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0093] Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0094] For example, for a commercially-available 512-MB (64M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

[0095] Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

[0096] Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

[0097] Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M×8-bit) memory device].

[0098] Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M×8-bit) memory device].

[0099] Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

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[0100] In a further example, for a commercially-available 1-GB (128M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

[0101] Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

[0102] Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

[0103] Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M×8-bit) memory device].

[0104] Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M×8-bit) memory device].

[0105] Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0106] In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0107] **FIG. 9C** schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory-locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0108] In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0109] For example, to fabricate a 1-GB (128M×8-byte) memory module, sixteen 512-Mb (128M×4-bit) memory devices can be used. The sixteen 512-Mb (128M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

[0110] Byte 3: 13 row address bits.

[0111] Byte 4: 12 column address bits.

[0112] Byte 13: 8 bits wide for the primary virtual 1-Gb (128M×8-bit) memory device.

[0113] Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M×8-bit) memory device.

[0114] Byte 17: 4 banks.

[0115] In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have the same values as they would have for a 512-MB (128M×4-byte) memory module utilizing 512-Mb (128M×4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to **8**, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0116] In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a

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set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[0117] Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[0118] Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

[0119] In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

[0120] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[0121] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128Mx4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128Mx4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256Mx4-bit to the computer system.

[0122] In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

[0123] Table 3 A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February **2004**, and incorporated in its entirety by reference herein.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x4"configuration	11	11	12	12
Number of column address bits for "x8"configuration	10	10	11	11
Number of column address bits for "x16"configuration	9	9	10	10

[0124] As described by Table 3A, 512-Mb (128Mx4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128Mx8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128Mx8-byte) memory module using sixteen 512-Mb (128Mx4-bit) DRAM devices.

[0125] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

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TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

[0126] Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[0127] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[0128] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank **2**) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[0129] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[0130] The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[0131] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

EXAMPLE 2

[0132]

```
always @(posedge clk_in)
    begin
                rs0N_R <= rs0_in_N;    // cs0
                rasN_R <= ras_in_N;
                casN_R <= cas_in_N;
                weN_R <= we_in_N;
    end
// Gated Chip Selects
assign          pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)          // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                    // ref exit, pwr dn
```

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-continued

```
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)          // pchg all
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)  // pchg single bnk
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ~ba2_in)  // activate
                    | (~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)     // xfr
                    ;
assign              pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                   // ref,md reg set
                    | (~rs0_in_N & ras_in_N & cas_in_N)                             // ref exit, pwr dn
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)        // pchg all
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)  // pchg single bnk
                    | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ba2_in)   // activate
                    | (~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                    ;
//-------------------------------
 always @(posedge clk_in)
    begin
                a4_r <= a4_in ;
                a5_r <= a5_in ;
                a6_r <= a6_in ;
                a10_r <= a10_in ;
                ba0_r <= ba0_in ;
                ba1_r <= ba1_in ;
                ba2_r <= ba2_in ;
                q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                   & !rs0N_R
                   & (!ba0_r & !ba1_r)
                   ;    // md reg set cmd
    always @(posedge clk_in)
        if (~reset_N)    // lmr
                cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1) // load mode reg cmd
      begin
                cl3 <= (~a6_r & a5_r & a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)          // reset
                cl2 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1) // load mode reg cmd
      begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)          // reset
                cl4 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1) // load mode reg cmd
      begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
      end
 always @(posedge clk_in)
        if (~reset_N)          cl5 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1) // load mode reg cmd
      begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
      end
assign              pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)  // wr brst cl3 preamble
                    ;
assign              pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)             // rd brst cl3 preamble
                                   | (wr_cmd_cyc2 & cl3)             // wr brst cl3 1st pair
                                   | (wr_cmd_cyc2 & cl4)             // wr brst cl4 preamble
                                   ;
assign              pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)             // wr brst cl3 2nd pair
                                   | (wr_cmd_cyc3 & cl4)             // wr brst cl4 1st pair
                                   | (rd_cmd_cyc3 & cl3)             // rd brst cl3 1st pair
                                   | (rd_cmd_cyc3 & cl4)             // rd brst cl4 preamble
                                   ;
assign              pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)             // rd brst cl3 2nd pair
                                   | (wr_cmd_cyc4 & cl4)             // wr brst cl4 2nd pair
                                   | (rd_cmd_cyc4 & cl4)             // rd brst cl4 1st pair
                                   ;
// dq
assign              pre_dq_cyc = pre_cyc2_enfet
                    | pre_cyc3_enfet
```

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-continued

```
                    | pre_cyc4_enfet
                    | pre_cyc5_enfet
                    ;
assign              pre_dq_ncyc = enfet_cyc2
                    | enfet_cyc3
                    | enfet_cyc4
                    | enfet_cyc5
                    ;
// dqs
assign              pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                    | (pre_cyc3_enfet & ~ba2_cyc2)
                    | (pre_cyc4_enfet & ~ba2_cyc3)
                    | (pre_cyc5_enfet & ~ba2_cyc4)
                    ;
assign              pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                    | (pre_cyc3_enfet & ba2_cyc2)
                    | (pre_cyc4_enfet & ba2_cyc3)
                    | (pre_cyc5_enfet & ba2_cyc4)
                    ;
assign              pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                    | (enfet_cyc3 & ~ba2_cyc3)
                    | (enfet_cyc4 & ~ba2_cyc4)
                    | (enfet_cyc5 & ~ba2_cyc5)
                    ;
assign              pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                    | (enfet_cyc3 & ba2_cyc3)
                    | (enfet_cyc4 & ba2_cyc4)
                    | (enfet_cyc5 & ba2_cyc5)
                    ;
always @(posedge clk_in)
    begin
        acs_cyc2 <= acs_cyc1 ;      // cs active
        ba2_cyc2 <= ba2_r ;
        ba2_cyc3 <= ba2_cyc2 ;
        ba2_cyc4 <= ba2_cyc3 ;
        ba2_cyc5 <= ba2_cyc4 ;
        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
        rd_cmd_cyc7 <= rd_cmd_cyc6 ;
        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
    end
always @(negedge clk_in)
    begin
        dq_ncyc <= dq_cyc;
        dqs_ncyc_a <= dqs_cyc_a;
        dqs_ncyc_b <= dqs_cyc_b;
    end
// DQ FET enables
assign              enq_fet1 = dq_cyc | dq_ncyc          ;
assign              enq_fet2 = dq_cyc | dq_ncyc ;
assign              enq_fet3 = dq_cyc | dq_ncyc          ;
assign              enq_fet4 = dq_cyc | dq_ncyc ;
assign              enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign              ens_fet1a = dqs_cyc_a | dqs_ncyc_a   ;
assign              ens_fet2a = dqs_cyc_a | dqs_ncyc_a   ;
assign              ens_fet3a = dqs_cyc_a | dqs_ncyc_a   ;
assign              ens_fet1b = dqs_cyc_b | dqs_ncyc_b   ;
assign              ens_fet2b = dqs_cyc_b | dqs_ncyc_b   ;
assign              ens_fet3b = dqs_cyc_b | dqs_ncyc_b   ;
```

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[0133] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

EXAMPLE 3

[0134]

```
// latched a13 flags cs0, banks 0-3
    always @(posedge clk_in)
        if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R) // activate
        begin
                1_a13_00 <= a13_r ;
        end
    always @(posedge clk_in)
        if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)  // activate
        begin
                1_a13_01 <= a13_r ;
        end
    always @(posedge clk_in)
        if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)  // activate
        begin
                1_a13_10 <= a13_r ;
        end
    always @(posedge clk_in)
        if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)   // activate
        begin
                1_a13_11 <= a13_r ;
        end
// gated cas
assign cas_i = ~(casN_R);
assign cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00   & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_01   & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & 1_a13_10   & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & 1_a13_11   & bnk1_R & bnk0_R & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R; // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R; // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd cyc
    always @(posedge clk_in)
        begin
                rd0_o_R2 <= rd0_o_R1 ;
                rd0_o_R3 <= rd0_o_R2;
                rd0_o_R4 <= rd0_o_R3;
                rd0_o_R5 <= rd0_o_R4;
                rd1_o_R2 <= rd1_o_R1 ;
                rd1_o_R3 <= rd1_o_R2;
                rd1_o_R4 <= rd1_o_R3;
                rd1_o_R5 <= rd1_o_R4;
                wr0_o_R2 <= wr0_o_R1 ;
                wr0_o_R3 <= wr0_o_R2;
                wr0_o_R4 <= wr0_o_R3;
                wr1_o_R2 <= wr1_o_R1 ;
                wr1_o_R3 <= wr1_o_R2;
                wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                          // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                        // 1st cyc of rd brst
            | rd0_o_R4                                        // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)              // post-rd cyc if no ped on rnk 1
```

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-continued

```
        | (wr0_o_R1)                                                    // pre-am wr
        | wr0_o_R2 | wr0_o_R3                                          // wr brst 1st & 2nd cyc
        | (wr0_o_R4)                                                   // post-wr cyc (chgef9)
        | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4                    // rank 1 (chgef9)
        )
                        en_fet_a <= 1'b1;                              // enable fet
    else
                        en_fet_a <= 1'b0;                              // disable fet
    end
always @(posedge clk_in)
        begin
        if (
                (rd1_o_R2 & ~rd0_o_R4)
                | rd1_o_R3
                | rd1_o_R4
                | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                               // (chgef8)
            | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                         // post-wr cyc      (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                          // rank 0 (chgef9)
                )
                        en_fet_b <= 1'b1;                              //
        else
                        en_fet_b <= 1'b0;
        end
```

[0135] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

[0136] **FIG. 10A** schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a* and a second rank **32***b*. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured in pairs, and the memory devices **30** of the second rank **32***b* are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32***b* are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32***a* and the second rank **32***b*.

[0137] The first rank **32***a* of **FIG. 10A** has 18 memory devices **30** and the second rank **32***b* of **FIG. 10A** has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b* are also compatible with embodiments described herein.

[0138] In the embodiment schematically illustrated by **FIG. 10A**, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of **FIG. 10A** has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of **FIG. 10A** have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128M×4-bit memory devices has the same memory density as a 1-Gb 128M×8-bit memory device.

[0139] For two "×4 " memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[0140] For example, a 1-Gb 128M×8-bit DDR-1 DRAM memory device uses row addresses A_{12}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M×8 memory module **10** comprising pairs of the 512-Mb 128M×4 memory devices **30** supplies the address and command signals including the extra row

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address (A_{13}) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

[0141] **FIG. 10B** schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by **FIG. 10B**, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32***a* of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32***b* of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

[0142] In the exemplary circuit **40** of **FIG. 10B**, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32***a* as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32***b* as the A_{12} address. The first rank **32***a* and the second rank **32***b* thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0143] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0144] **FIG. 11A** schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a*, a second rank **32***b*, a third rank **32***c*, and a fourth rank **32***d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32***a*, the second rank **32***b*, the third rank **32***c*, and the fourth rank **32***d*.

[0145] Each rank **32***a*, **32***b***32***c*, **32***d* of **FIG. 11A** has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b*, **32***c*, **32***d* are also compatible with embodiments described herein.

[0146] In the embodiment schematically illustrated by **FIG. 11A**, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of **FIG. 11A** has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M×8-byte memory module with 36 512-Mb 128M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M×8-byte memory module with 18 512-Mb 128M×8-bit-memory devices (arranged in two ranks).

[0147] To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by **FIG. 11A**. **FIG. 11B** schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32***a*, **32***b*, **32***c*, **32***d* of memory devices **30**.

[0148] In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

[0149] In the embodiment schematically illustrated by **FIG. 11B**, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32***a*, **32***b*, **32***c*, **32***d* is active.

[0150] In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated

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CAS signals which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*.

Tied Data Strobe Signal Pins

[0151] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64Mx4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64Mx8-bit configuration (e.g., as a 1-GB memory module with 128Mx8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0152] **FIGS. 12 and 13** schematically illustrate a problem which may arise from tying together two output signal pins. **FIG. 12** schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

[0153] **FIG. 13** is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by **FIG. 13**, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

[0154] A second problem may also arise from tying together two output signal pins. **FIG. 14** schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of **FIG. 14** are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, **FIG. 14** only shows one DQ pin for each memory device **310**, **320**.

[0155] Each of the memory devices **310**, **320** of **FIG. 14** utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in **FIG. 14** by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in **FIG. 14** by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of **FIG. 14** are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

[0156] Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[0157] In certain configurations, as schematically illustrated by **FIG. 14**, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly,

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in certain configurations, as schematically illustrated by **FIG. 14**, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by **FIG. 14**, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

[0158] When connecting the first memory device **310** and the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are, enabled at the sametime (egg., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in **FIG. 14**, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of **FIG. 14**, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[0159] **FIG. 15** schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

[0160] In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). **FIGS. 16A and 16B** schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

[0161] In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

[0162] In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0163] **FIGS. 17A and 17B** schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by **FIG. 17A**, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in **FIGS. 17A and 17B**) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[0164] **FIG. 17B** schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first

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memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of **FIG. 13**, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0165] In certain embodiments, as schematically illustrated by **FIG. 17B**, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of **FIG. 17B** is approximately zero.

[0166] The voltage at the second DQS pin **422** in **FIG. 17B** is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of **FIGS. 17A and 17B** advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[0167] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

[0168] For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[0169] **FIG. 18** schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610** having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

[0170] **FIG. 19** schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by **FIG. 18**. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in **FIG. 14** by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

[0171] The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in **FIG. 14** by the switches **674**, **678** which are opened.

[0172] The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the

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ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in **FIG. 19** by the switch **680** which is either closed (dash-dot line) or opened (solid line).

[0173] In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

[0174] Certain embodiments of the memory module **600** schematically illustrated by **FIG. 19** advantageously avoid the problem schematically illustrated by **FIG. 12** of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to **FIG. 14**, **FIGS. 18 and 19** only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of **FIG. 18** are schematic representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

[0175] The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in **FIG. 19**). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

[0176] The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by **FIG. 19** provides external or off-chip termination of the second memory device **620**.

[0177] Certain embodiments of the memory module **600** schematically illustrated by **FIG. 19** advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

[0178] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[0179] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0180] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. A memory module comprising:

a plurality of memory devices, each memory device having a corresponding load; and

a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, the circuit selectively isolating one or more of the loads of the memory devices from the computer system, the circuit comprising logic which translates between a system

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memory domain of the computer system and a physical memory domain of the memory module.

2. The memory module of claim 1, wherein the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD).

3. The memory module of claim 2, wherein the circuit further comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

4. The memory module of claim 1, wherein the plurality of memory devices has a first number of memory devices, and the circuit selectively isolates the loads of a second number of the memory devices from the computer system, the second number less than the first number.

5. The memory module of claim 4, wherein the first number of memory devices are configured in a plurality of ranks, and wherein the second number of memory devices are configured as one rank of the plurality of ranks.

6. The memory module of claim 1, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

7. The memory module of claim 1, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects.

8. The memory module of claim 1, wherein the system memory domain is compatible to a first memory density, and the physical memory domain is compatible with a second memory density equal to twice the first memory density.

9. The memory module of claim 1, wherein the plurality of memory devices are arranged in two or more ranks of memory devices.

10. The memory module of claim 9, wherein the circuit comprises a data path multiplexer/demultiplexer which isolates the ranks of memory devices from one another.

11. The memory module of claim 1, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

12. The memory module of claim 1, wherein the memory module comprises a dual inline memory module.

13. The memory module of claim 12, wherein the memory module comprises a rank-buffered dual inline memory module.

14. The memory module of claim 1, wherein the memory module comprises a DDR 2 SDRAM memory array.

15. The memory module of claim 1, wherein the circuit selectively isolates the loads of the memory devices from the computer system in response to a command or address signal received from the computer system.

16. A method of using a memory module with a computer system, the method comprising:

providing a memory module having a plurality of memory devices and a circuit electrically coupled to the plurality of memory devices, the circuit configured to be electrically coupled to a computer system, each memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module.

17. The method of claim 16, wherein the plurality of memory devices comprises a first number of memory devices and activating the circuit selectively isolates the loads of a second number of memory devices from the computer system, the second number less than the first number.

18. The method of claim 17, wherein the first number of memory devices are arranged in two or more ranks of memory devices, and wherein the second number of memory devices are arranged as one rank of the two or more ranks.

19. The method of claim 18, wherein the circuit comprises a data path multiplexer/demultiplexer which isolates the ranks of memory devices from one another.

20. The method of claim 16, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

21. The method of claim 16, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

22. The method of claim 16, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects.

23. The method of claim 16, wherein the system memory domain is compatible to a first memory density, and the physical memory domain is compatible with a second memory density equal to twice the first memory density.

24. The method of claim 16, wherein the memory module comprises a dual inline memory module.

25. A memory module connectable to a computer system, the memory module comprising:

a first memory device having a first data signal line and a first data strobe signal line;

a second memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the device selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the device comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

26. The memory module of claim 25, wherein the device comprises a logic element.

27. The memory module of claim 26, wherein the device further comprises one or more switches selectively electri-

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cally coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

28. The memory module of claim 26, wherein the logic element is selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

29. The memory module of claim 25, wherein the memory module further comprises a common data strobe signal line connectable to the computer system, the device electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the common data strobe signal line, the device selectively electrically coupling the first data strobe signal line to the common data strobe signal line and selectively electrically coupling the second data strobe signal line to the common data strobe signal line.

30. The memory module of claim 29, wherein the device comprises a logic element and one or more switches selectively electrically coupling the first data strobe signal line to the common data strobe signal line and selectively electrically coupling the second data strobe signal line to the common data strobe signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.

* * * * *

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US 20080162790A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2008/0162790 A1**

(43) **Pub. Date: Jul. 3, 2008**

IM

(54) **NAND FLASH MEMORY HAVING C/A PIN AND FLASH MEMORY SYSTEM INCLUDING THE SAME**

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(21) Appl. No.: **11/757,121**

(22) Filed: **Jun. 1, 2007**

(30) **Foreign Application Priority Data**

Dec. 29, 2006 (KR) 10-2006-0137629

Publication Classification

(51) **Int. Cl.**
G06F 13/28 (2006.01)

(52) **U.S. Cl.** **711/103**

(57) **ABSTRACT**

A NAND flash memory in which a command/address pin is separated from a data input/output pin. The NAND flash memory includes a memory cell array used for storing data, a command/address pin through which a command and an address are received for transmitting data in the memory cell array, and a data input/output pin through which data are transmitted in the memory cell array. The command/address pin is separated from the data input/output pin in the NAND flash memory. Data input/output speed is increased. Furthermore, the NAND flash memory can perform a bank interleaving operation with a minimal delay time.

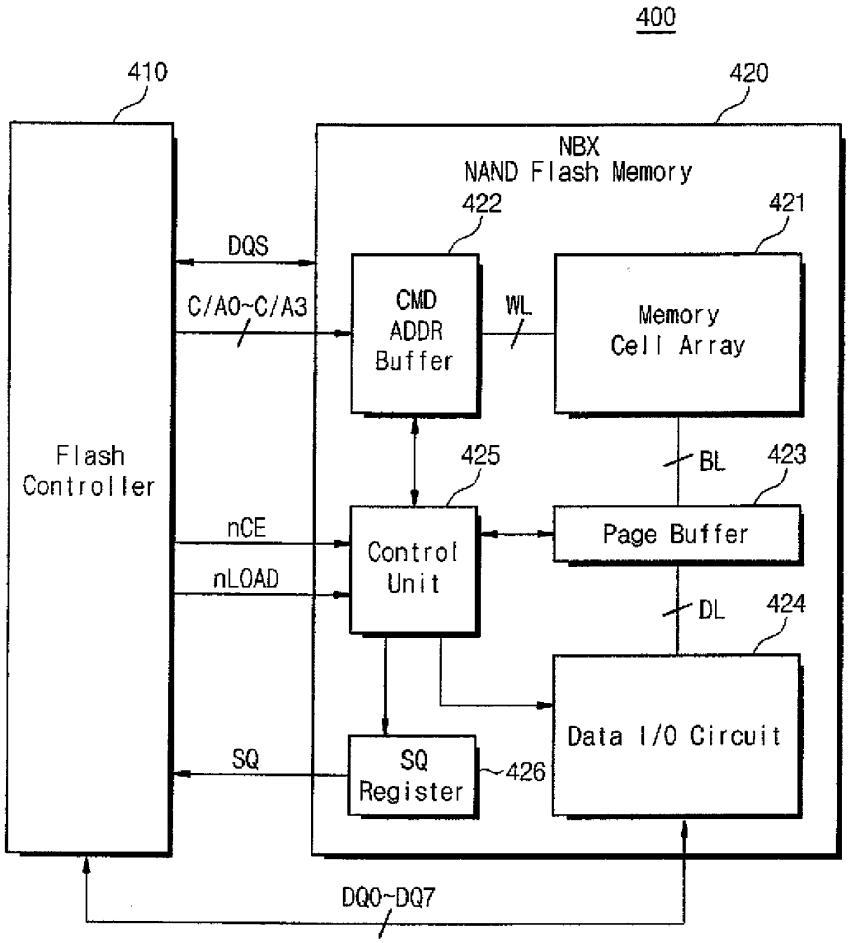

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Fig. 1

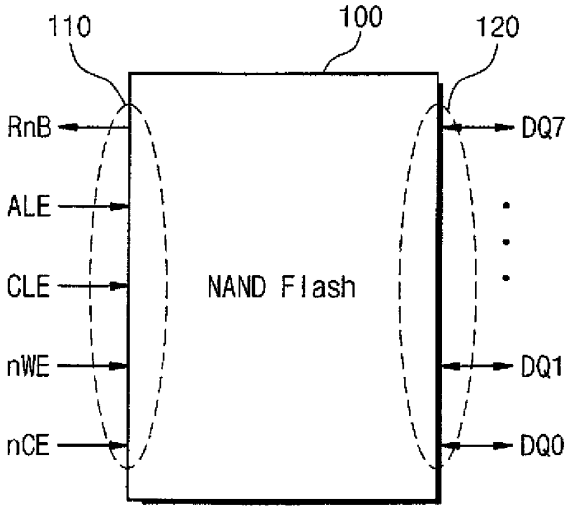

Fig. 2

Pin Name	Description
RnB	Ready, Busy Status Out
nRE	Read Enable
nCE	Chip Enable
Vcc	Power Supply
Vss	Ground
CLE	Command Latch Enable
ALE	Address Latch Enable
nWE	Write Enable
nWP	Write Protection
DQ0~DQ7	Data Input & Output

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Fig. 3

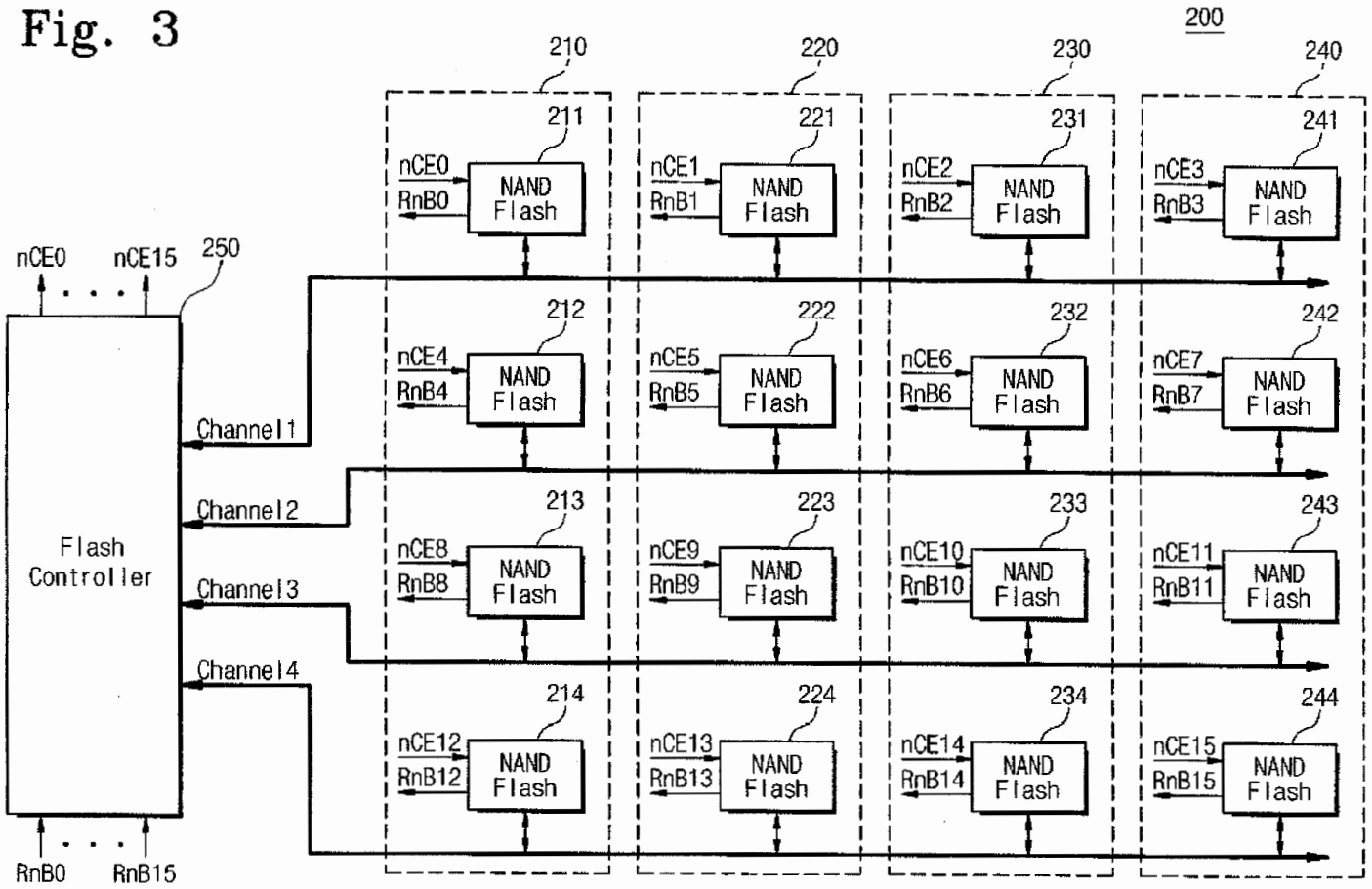

Fig. 4

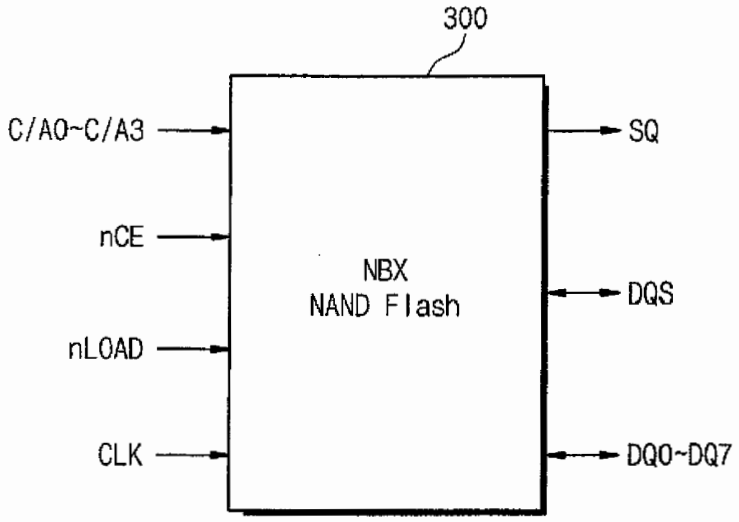

Fig. 5

Pin Name	Description
C/A0~C/A3	Command/Address Mux
nLOAD	Load Command or Address
nCE	Chip Enable
CLK	Clock
Vcc	Power Supply
Vss	Ground
SQ	Status Out
DQS	Strobe for Data I/O
DQ0~DQ7	Data Input & OutPut

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Fig. 6

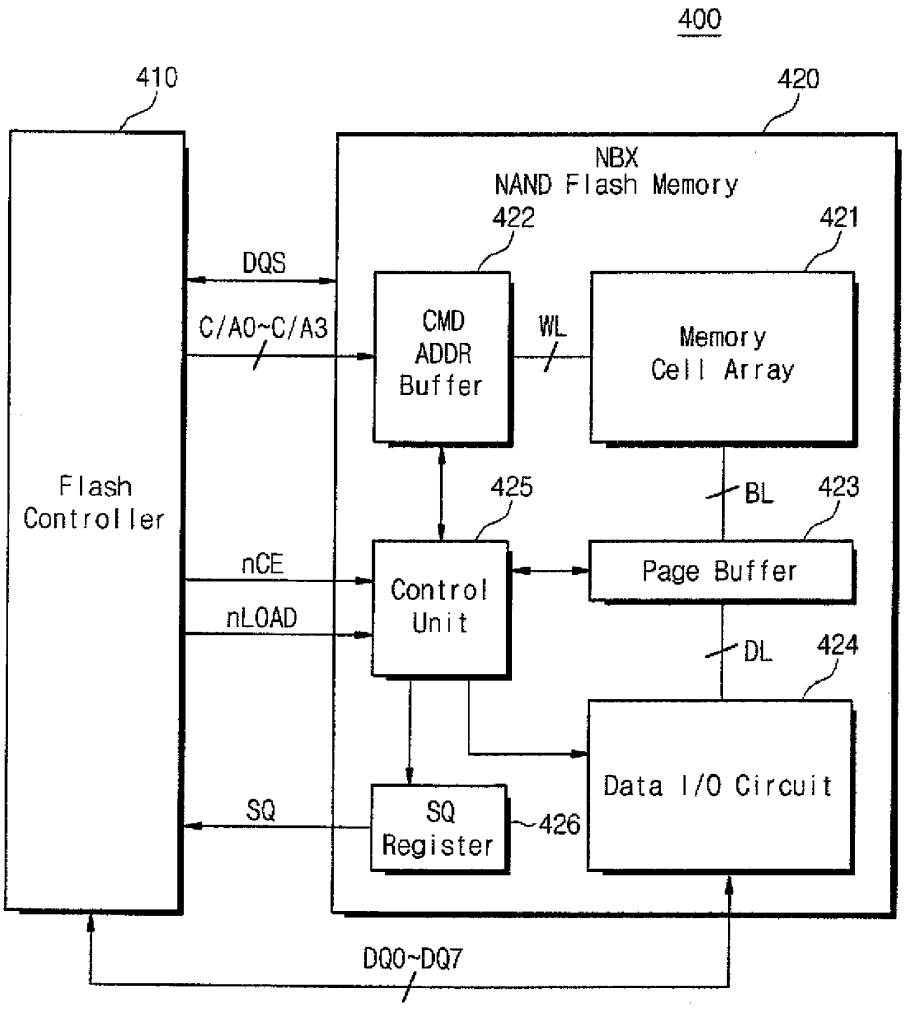

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Fig. 7

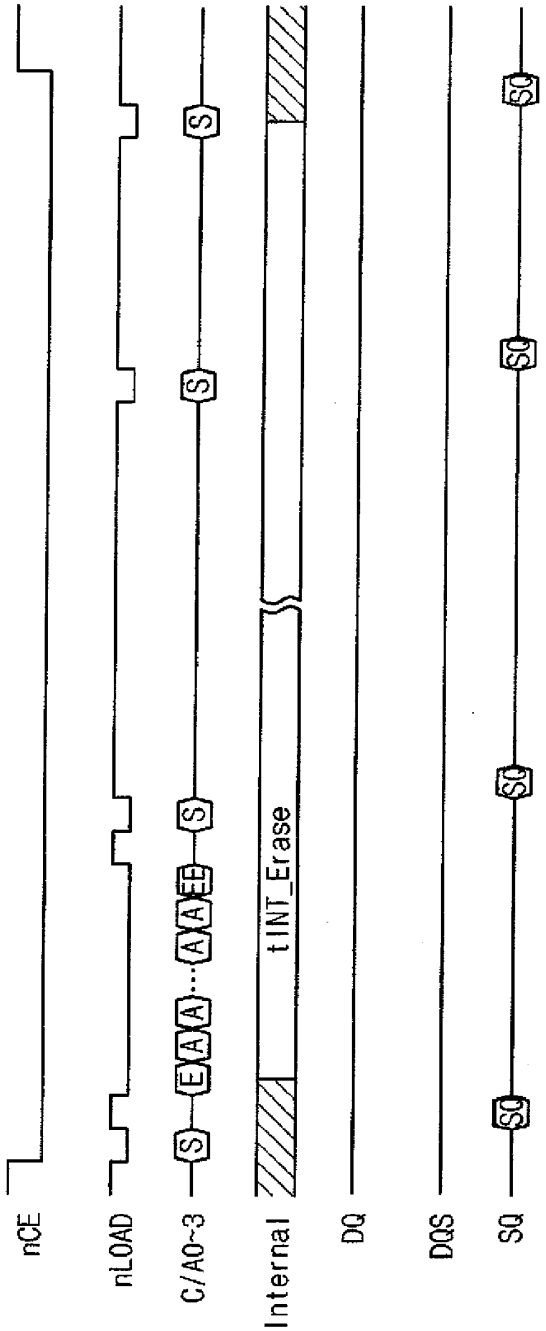

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Fig. 8

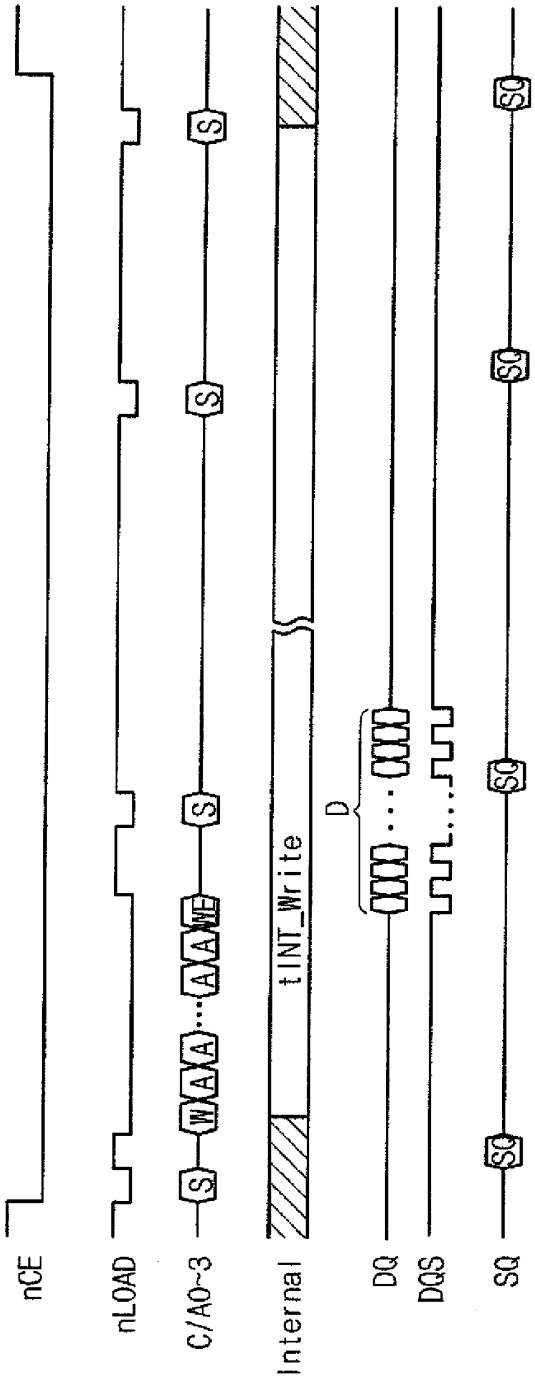

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Fig. 9

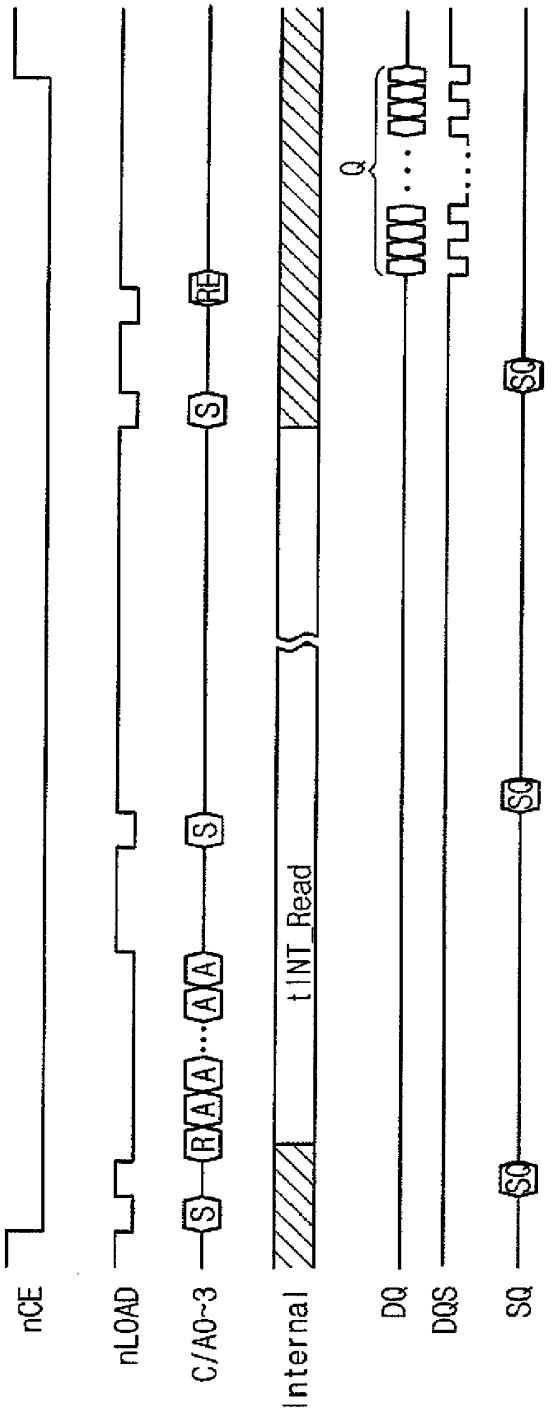

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Fig. 10

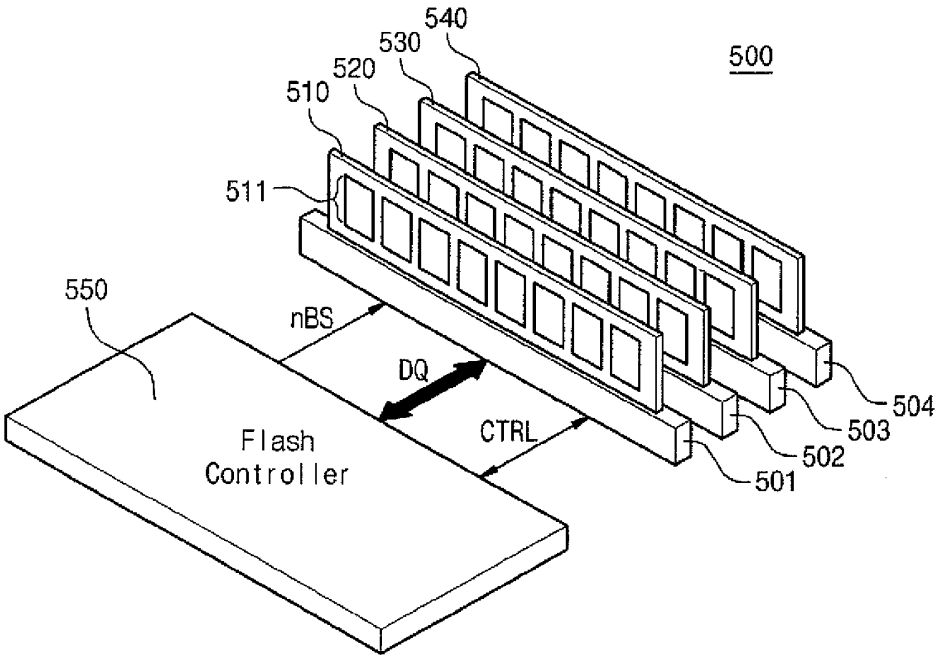

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Fig. 11

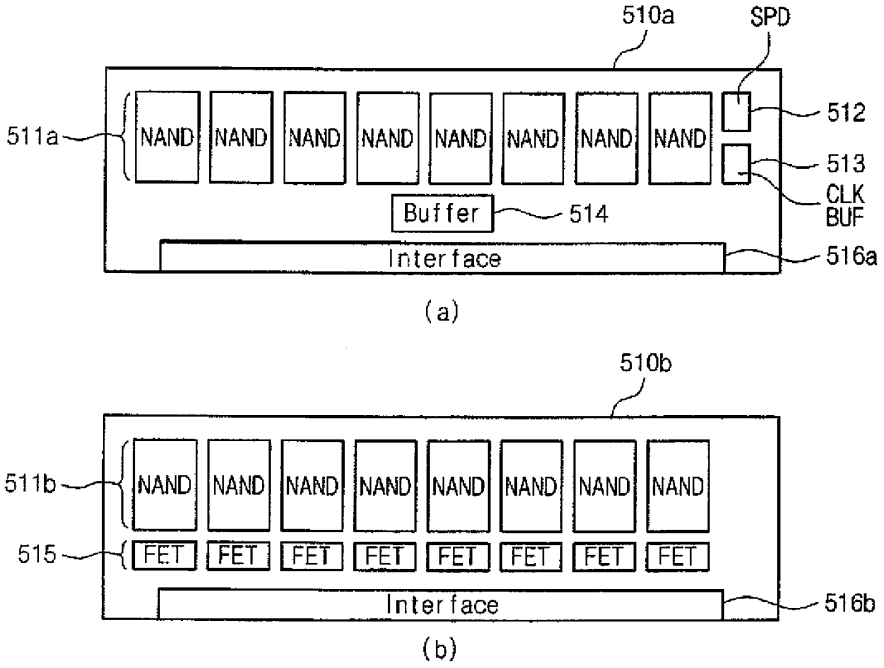

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Fig. 12

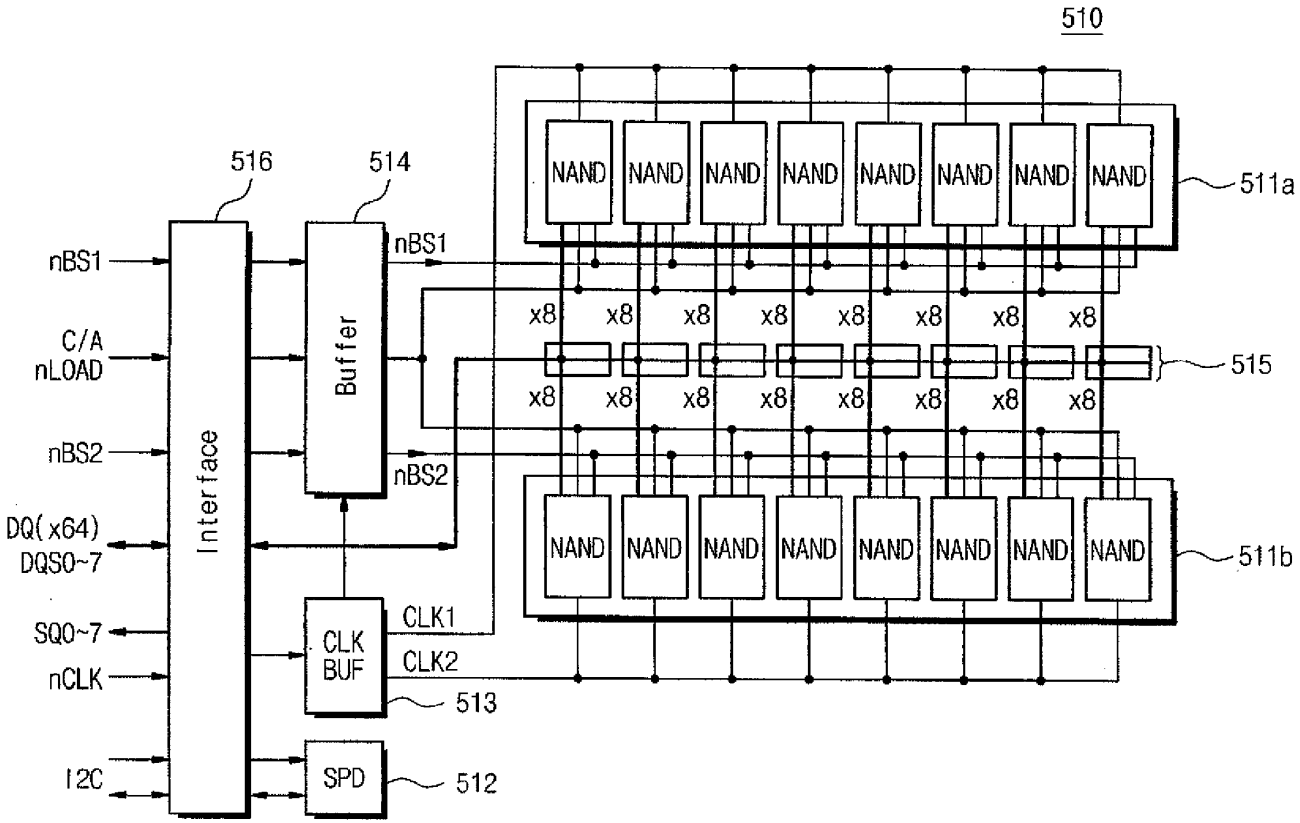

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Fig. 13

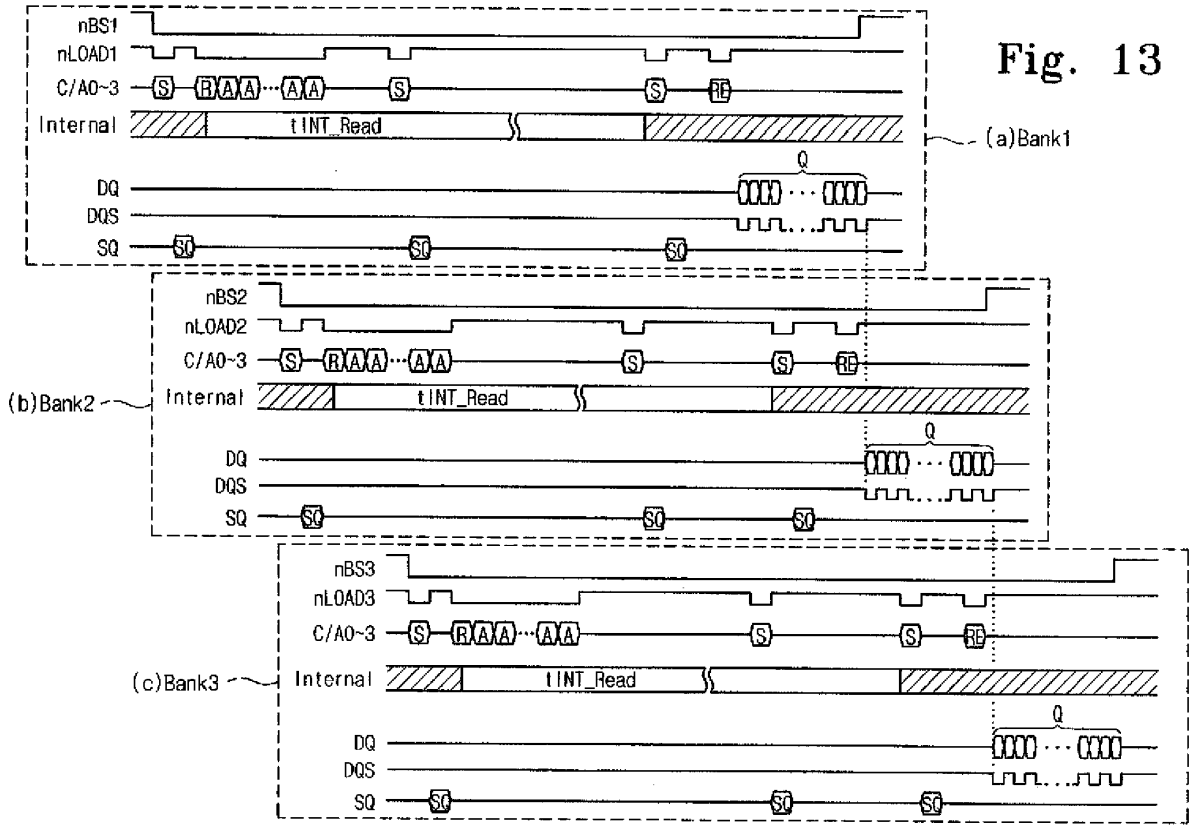

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Fig. 14

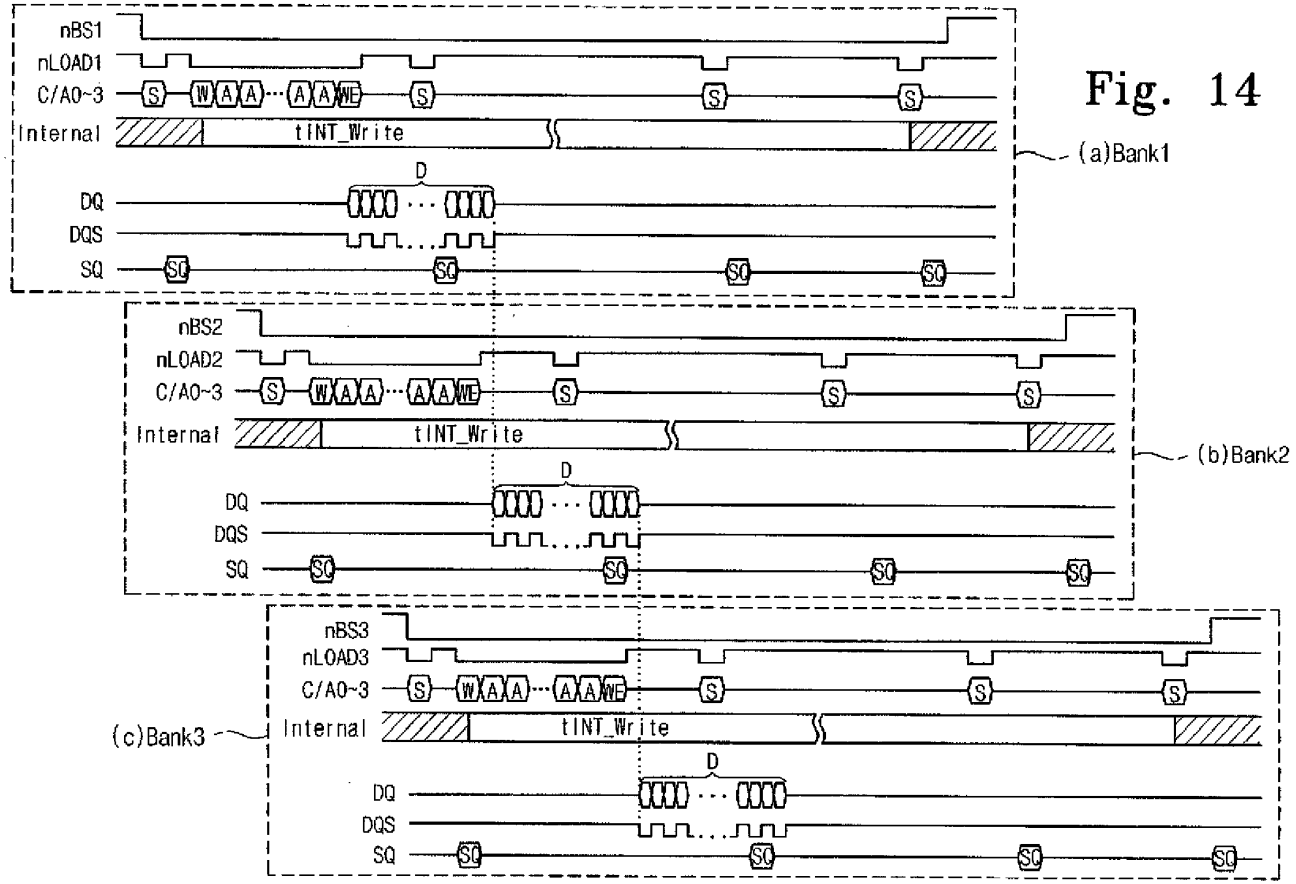

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Fig. 15

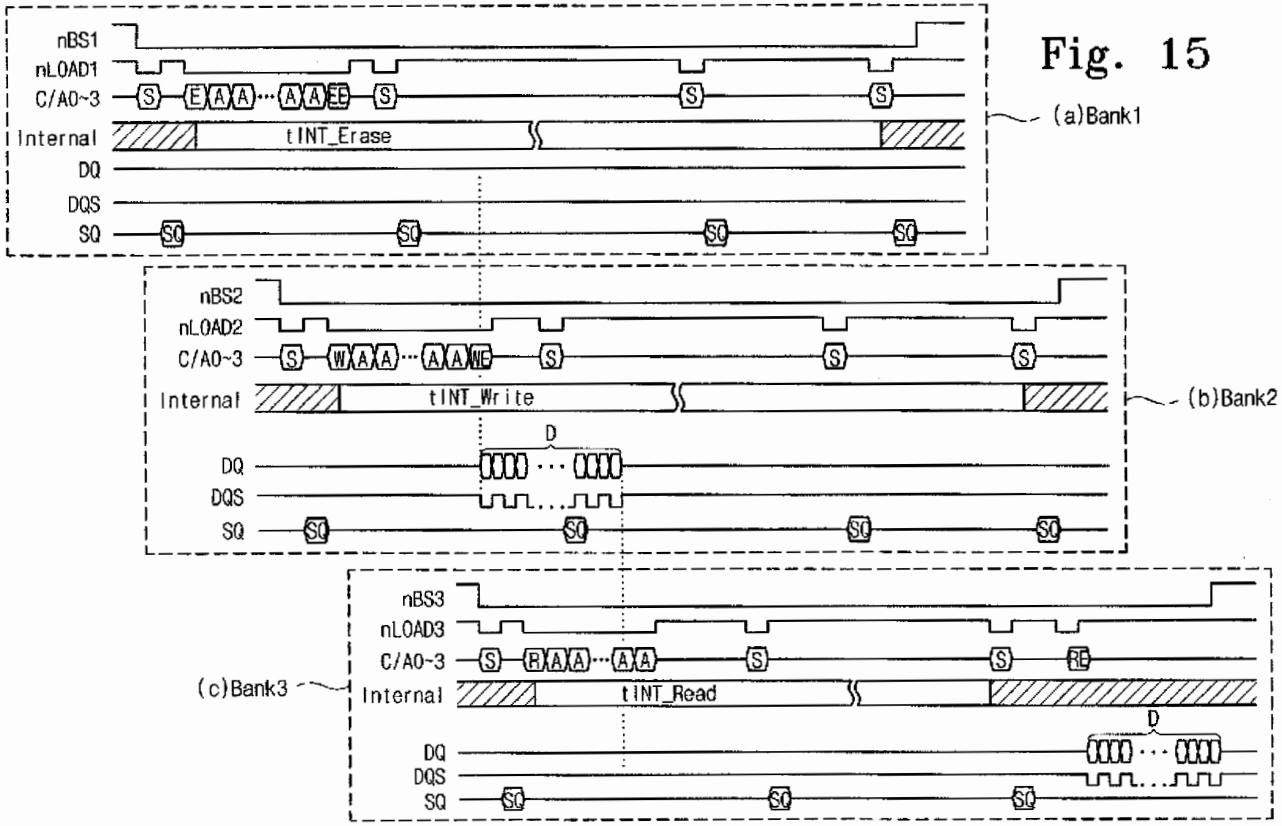

Fig. 16

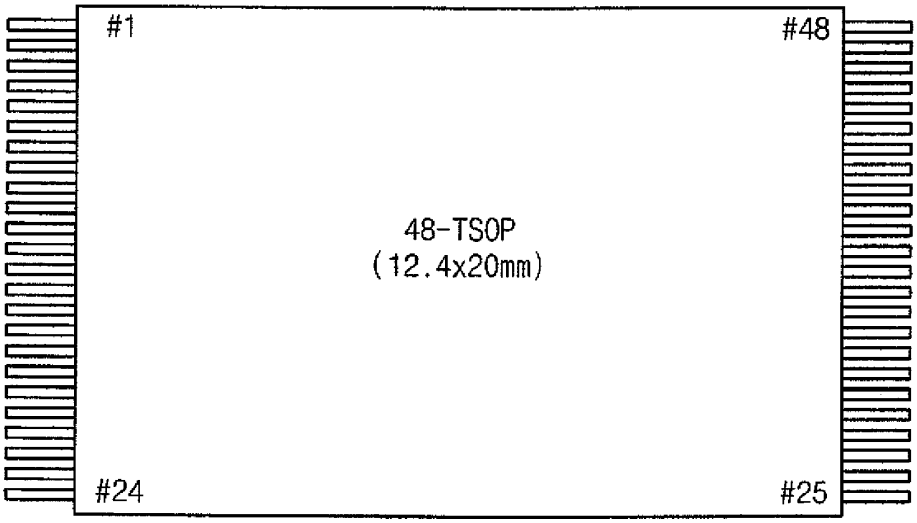

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Fig. 17

Pin	Name	Description
#1	C/A3	Command/Address Mux
#2	C/A2	Command/Address Mux
#3	C/A1	Command/Address Mux
#4	C/A0	Command/Address Mux
#5	nLOAD	Load Command or Address
#6	nCE	Chip Enable
#7	CK	Clock
#8	VSS	Ground for Core
#9	NC	No Connection
#10	DQ7	Data Input & OutPut
#11	DQ6	Data Input & OutPut
#12	DQ5	Data Input & OutPut
#13	DQ4	Data Input & OutPut
#14	VDDQ	Power Supply for DQ
#15	DQS	Strobe for Data Input & Output
#16	VSSQ	Ground for DQ
#17	DQ3	Data Input & OutPut
#18	DQ2	Data Input & OutPut
#19	DQ1	Data Input & OutPut
#20	DQ0	Data Input & OutPut
#21	VDD	Power Supply for DQ
#22	SQ	Status Out(Not DDR, Clock to Data Out)
#23	nCKE	Clock Enable(Clock Stop When High)
#24	WP	Write Protection

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NAND FLASH MEMORY HAVING C/A PIN AND FLASH MEMORY SYSTEM INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2006-0137629, filed on Dec. 29, 2006, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] The present disclosure relates to a memory device, and more particularly, to a NAND flash memory having a command/address (C/A) pin and a flash memory system including the same.

[0004] 2. Discussion of the Related Art

[0005] Semiconductor memory devices are storage devices for storing data. Semiconductor memory devices can be classified as a random access memory (RAM) and a read only memory (ROM). A RAM is a volatile memory device that requires power to maintain stored data. A ROM is a nonvolatile memory device that can maintain stored data even when not powered.

[0006] Examples of RAMs include a dynamic RAM (DRAM) and a static RAM (SRAM). Examples of ROMs include a programmable ROM (PROM), an erasable programmable ROM (EPROM), an electrically erasable programmable ROM (EEPROM), and a flash memory. Examples of flash memories include a NOR flash memory and a NAND flash memory. NAND flash memories are widely used for mobile communication terminals, portable media players, digital cameras, and mobile storage media.

[0007] FIG. **1** illustrates a conventional NAND flash memory **100**, and FIG. **2** is a table providing descriptions of pins of the NAND flash memory **100**. Referring to FIG. **1**, the NAND flash memory **100** includes control pins such as RnB, ALE, CLE, nWE, and nCE pins that are formed on a first surface **110** of the NAND flash memory **100**. The NAND flash memory **100** further includes data pins such as DQ0 through DQ7 pins formed on a second surface **120**.

[0008] The pin structure of the NAND flash memory **100** shown in FIG. **1** is a structure for a thin small outline package (TSOP). However, since the control pins are formed on one surface of the NAND flash memory **100**, board structure for the NAND flash memory **100** is complicated. Furthermore, when a memory module is formed using a plurality of NAND flash memories having the pin structure illustrated in FIG. **1**, the structure of a printed circuit board (PCB) for the memory module is complicated.

[0009] FIG. **3** is a block diagram illustrating a flash memory system **200** having a multi-bank architecture using the NAND flash memory **100** of FIG. **1**. Referring to FIG. **3**, the flash memory system **200** may include a flash controller **250**, first bank **210**, second bank **220**, third bank **230**, and fourth bank **240**.

[0010] Each of the banks **210**, **220**, **230**, and **240** includes four NAND flash memories. For example, the first bank **210** includes four NAND flash memories **211**, **212**, **213**, and **214**. The second bank **220** includes four NAND flash memories **221**, **222**, **223**, and **224**. The third bank **230** includes four NAND flash memories **231**, **232**, **233**, and **234**. The fourth bank **240** includes four NAND flash memories **241**, **242**, **243**, and **244**. The flash controller **250** is connected to the banks **210**, **220**, **230**, and **240** through four channels **1** through **4**. Here, each of the channels **1** through **4** connects corresponding NAND flash memories of the banks **210**, **220**, **230**, and **240**. For example, channel **1** connects NAND flash memories **211**, **221**, **231**, and **241** of the banks **210**, **220**, **230**, and **240**, respectively. Similarly, channel **2** connects NAND flash memories **212**, **222**, **232**, and **242**. Channel **3** connects NAND flash memories **213**, **223**, **233**, and **243**, Channel **4** connects NAND flash memories **214**, **224**, **234**, and **244**.

[0011] The controller **250** performs a bank interleaving operation using chip enable signals nCE0-nCEX (where X is a positive integer). In so doing, the controller **250** receives as many enable signals and read and busy signals RnB0-RnBX as there are NAND flash memories. As used herein, bank interleaving is a data reading or writing operation performed between banks of a memory system in which two or more banks share a common channel. For example, in a bank interleaving operation, the flash controller **250** reads data from and/or writes data to the NAND flash memories **211**, **221**, **231**, and **241** connected to channel **1** while moving between the NAND flash memories **211**, **221**, **231**, and **241**.

[0012] As described above, as many chip enable signals nCE0 to nCEX and ready and busy signals RnB0 to RnBX are used as the number of flash memory chips for a bank interleaving operation. Therefore, when the flash memory system **200** uses all the four channels **1** to **4**, sixteen chip enable signals nCE0 to nCE15 and sixteen read and busy signals RnB0 to RnB15 are used for a bank interleaving operation. Accordingly, the structure of the flash memory system **200** becomes more complicated as the numbers of banks and flash memory chips increase.

[0013] A conventional NAND flash memory receives address and command signals through a data input/output (DQ) pin. Therefore, when address and command signals are input to the NAND flash memory, data cannot be input to or output from the NAND flash memory. This results in a data delay time. Data input/output is especially delayed when a bank interleaving operation is performed.

[0014] Furthermore, when data is written to or read from a cell array of a conventional NAND flash memory, RnB signals are generated. In this case, a flash controller cannot perform any operation until the writing/reading operation is completed. This reduces the performance of a flash memory system.

SUMMARY OF THE INVENTION

[0015] Exemplary embodiments of the present invention provide a NAND flash memory having fast data input/output.

[0016] Exemplary embodiments of the present invention provide a flash memory system that performs a bank interleaving operation while minimizing delay time.

[0017] Exemplary mbodiments of the present invention provide NAND flash memories including a memory cell array used for storing data, a command/address pin through which a command and an address are received for inputting data to or outputting data from the memory cell array, and a data input/output pin through which data are input to or output from the memory cell array.

[0018] In some exemplary embodiments, the NAND flash memory further includes a status register receiving a status read command through the command/address pin and providing an operational status of the NAND flash memory to a flash

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controller. The flash controller sends the status read command to the NAND flash memory when the NAND flash memory operates, before the NAND flash memory operates, or after the NAND flash memory operates. The status register sends a status signal SQ to the flash controller to inform the flash controller whether the NAND flash memory is internally operational. The flash controller controls the internal operation of the NAND flash memory in response to the status signal SQ.

[0019] In some exemplary embodiments, the data is input/output through the data input/output pin depending upon the toggling of a data strobe signal DOS. The data is input/output through the data input/output pin by a DDR (double data rate) transmission method. The NAND flash memory further includes a command/address buffer receiving the command and address transmitted through command/address pin. The NAND flash memory further includes a control unit controlling the reception of the command and address. The control unit receives a chip enable signal nCE and a load signal nLOAD from a flash controller and controls the reception of the command and address

[0020] In some exemplary embodiments of the present invention, there are provided flash memory systems including a flash controller and a flash memory module formed of a plurality of NAND flash memories. Each of the NAND flash memories includes a memory cell array used for storing data, a command/address pin through which a command and an address are received from the flash controller for inputting/outputting data to/from the memory cell array and a data input/output pin through which data are input to and output from the memory cell array.

[0021] In some exemplary embodiments, each of the NAND flash memories further includes a status register receiving a status read command through the command/address pin and providing an operational status of the NAND flash memory to the flash controller. The flash controller sends the status read command to the NAND flash memory when the NAND flash memory operates, before the NAND flash memory operates or after the NAND flash memory operates. The status register sends a status signal SQ to the flash controller to inform the flash controller whether the NAND flash memory is internally operational. The flash controller controls the internal operation of the NAND flash memory in response to the status signal SQ. The data input/output through the data input/output pin is performed according to a toggling of a data strobe signal DQS. The data input/output through the data input/output pin is performed by a DDR transmission method. Each of the NAND flash memories further includes a command/address buffer receiving the command and address transmitted through command/address pin. Each of the NAND flash memories further includes a control unit controlling the reception of the command and address. The control unit receives a chip enable signal nCE and a load signal nLOAD from the flash controller and controls the reception of the command and address.

BRIEF DESCRIPTION OF THE FIGURES

[0022] The above and other features of the present disclosure will become more apparent by describing in detail exemplary embodiments of the present invention with reference to the attached drawings in which:

[0023] FIG. **1** illustrates a conventional NAND flash memory;

[0024] FIG. **2** is a table illustrating pins of the NAND flash memory of FIG. **1**;

[0025] FIG. **3** is a block diagram illustrating a flash memory system with a multi-bank architecture using the NAND flash memory of FIG. **1**;

[0026] FIG. **4** illustrates an NBX NAND flash memory according to an exemplary embodiment of the present invention;

[0027] FIG. **5** is a table providing descriptions of pins of the NBX NAND flash memory of FIG. **4**, according to an exemplary embodiment of the present invention;

[0028] FIG. **6** is a block diagram of an NBX NAND flash memory system illustrating the NBX NAND flash memory of FIG. **4**, according to an exemplary embodiment of the present invention;

[0029] FIG. **7** is a timing diagram showing how data are erased from the NBX NAND flash memory of FIG. **6**, according to an exemplary embodiment of the present invention;

[0030] FIG. **8** is a timing diagram for explaining how data are written into the NBX NAND flash memory of FIG. **6**, according to an exemplary embodiment of the present invention;

[0031] FIG. **9** is a timing diagram for explaining how data are read from the NBX NAND flash memory of FIG. **6**, according to an exemplary embodiment of the present invention;

[0032] FIG. **10** is a diagram illustrating an NBX NAND flash memory system according to an exemplary embodiment of the present invention;

[0033] FIG. **11** is a block diagram illustrating an NBX flash module of the NBX NAND flash memory system of FIG. **10**, according to an exemplary embodiment of the present invention;

[0034] FIG. **12** is a block diagram illustrating an internal structure of the NBX flash module of FIG. **11**, according to an exemplary embodiment of the present invention;

[0035] FIGS. **13** through **15** are timing diagrams illustrating a bank interleaving operation of the NBX flash memory system of FIG. **10**, according to an exemplary embodiment of the present invention;

[0036] FIG. **16** illustrates a thin small outline package (TSOP) of an NBX NAND flash memory according to an exemplary embodiment of the present invention; and

[0037] FIG. **17** is a table illustrating pins of the TSOP of FIG. **16**, according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0038] Exemplary embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. The present invention may, however, be embodied in different forms and should not be constructed as limited to the exemplary embodiments set forth herein.

[0039] FIG. **4** illustrates a NAND flash memory **300** according to an exemplary embodiment of the present invention, and FIG. **5** is a table illustrating pins of the NBX NAND flash memory **300** according to an exemplary embodiment of the present invention. The NAND flash memory **300** includes additional command/address pins C/A**0** to C/A**3**. The NAND flash memory **300** further includes a data strobe pin DQS in addition to data input/output pins DQ**0** to DQ**7** for input/output data synchronization. Input signals of the NAND flash

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memory **300** are synchronized with a clock (CLK) signal. The NAND flash memory **300** of FIG. **4** will now be referred to as a NAND bus scalable (NBX) NAND flash memory.

[0040] Referring to FIG. **5**, the command/address pins C/A**0** to C/A**3** are used for inputting command and address signals. Although four command/address pins C/A**0** to C/A**3** are shown in FIG. **5**, the number of command/address pins C/A**0** to C/A**3** can be increased. The nLOAD pin is used for loading a command or address signal to the NAND flash memory **300**. The nCE pin is a chip enable pin. The CLK pin is a clock pin. The Vcc pin is a power voltage pin, and the Vss pin is a ground voltage pin.

[0041] The SQ pin indicates which operation is being performed or is completed in the NBX NAND flash memory **300**. For example, a high SQ signal indicates that an operation is completed in the NBX NAND flash memory **300** and the NBX NAND flash memory **300** is ready for the next operation. A low SQ signal indicates that an operation is being performed in die NBX NAND flash memory **300**. The SQ signal is output in synchronization with a CLK signal. As described above, the DQS pin is a data strobe pin used for data input/output, and the DQ0 to DQ7 pins are data input/output pins.

[0042] FIG. **6** is a block diagram of an example of the NBX NAND flash memory of FIG. **4**, according to an exemplary embodiment of the present invention. The NBX NAND flash memory **420** is electrically connected to a flash controller **410**. The NBX NAND flash memory **420** receives address and command signals from the flash controller **410** through a C/A pin and receives data from and sends data to the flash controller **410** through a data input/output pin.

[0043] Referring to FIG. **6**, the NBX NAND flash memory **420** includes a memory cell array **421**, a command address buffer **422**, a page buffer **423**, a data input/output circuit **424**, a control unit **425**, and an SQ register **426**.

[0044] The memory cell array **421** includes a plurality of memory blocks (not shown). Each of the memory blocks includes a plurality of pages (not shown). Each of the pages includes a plurality of memory cells that share a word line. The size of each page may be 512 bytes, 2 KB, or 4 KB, The size of page varies according to the type of the flash memory. In the NBX NAND flash memory **420**, data are erased in units of a block, and data are read and written in units of a page.

[0045] The command address buffer **422** is connected to the memory cell array **421** through a word line WL. The command address buffer **422** receives a command or address signal from the flash controller **410**. The control unit **425** receives control signals nCE and nLOAD and controls the command address buffer **422**.

[0046] The command signal is input to the NBX NAND flash memory **420** when the control signals nCE and nLOAD are low. Table 1 shows examples of command and control signals used in the NBX NAND flash memory system **400**. In Table 1, nCKE denotes a clock enable signal.

TABLE 1

Command(4bits)	Code	nCKE	nCE	nLOAD	DQS	DQ	Clock Cycle
Chip Deselect	—	L	H	X	High-Z	High-Z	L -> H
Clock Stop	—	H	X	X	High-Z	X	X(after n cycles)
Power On	—	H	H	X	High-Z	High-Z	Stead State After n cycles
Read	0h	L	L	L	High-Z	High-Z	L -> H, 1st cycle: Read in (after that address in)
Read Enable	1h	L	L	L	Toggle	Data out	L -> H, 1st cycle: Read enable (after that read data out)
Program (White)	2h	L	L	L	High-Z	High-Z	L -> H, 1 cycle: Program Command (after that address in)
Program Enable	3h	L	L	L	Toggle	Data-in	L -> H, 1st cycle: command in (after that program the page)
Page Read Stop	4h	L	L		High-Z	High-Z	L -> H, 1 cycle
Page Write Stop	5h	L	L		High-Z	High-Z	L -> H, 1 cycle
ID Read	6h	L	L		Toggle	Data Out	L -> H, 1st cycle: cmd in
Register Configuration	7h	L	L		Toggle	Data In	L -> H, 1st cycle: cmd in (after that configuration for n cycles)
Status Read	8h	—	—		High-Z	High-Z	L -> H, 1st cycle: cmd in, 2nd cycle: status data out
Reserved	9h-Eh						
Reset	Fh	L	L		High-Z	High-Z	After n cycles

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[0047] Referring to Table 1, Read is a command for starting a read operation. Read Enable is a command for reading data. Write is a command for starting a write operation. Write Enable or Program Enable is a command for writing data into the memory cell array **421**.

[0048] Status Read is a command for checking the operation status of the NBX NAND flash memory **420**. Reset is a command for initializing the NBX NAND flash memory **420**.

[0049] For example, a read command is input to the NBX NAND flash memory **420** in one clock cycle when nCE and nLOAD signals are low. Next, an address is input to the NBX NAND flash memory **420**. Other commands are input to the NBX NAND flash memory **420** in the same manner.

[0050] Referring again to FIG. **6**, the NBX NAND flash memory **420** includes the SQ register **426**. The SQ register **426** stores the status of the NBX NAND flash memory **420**. When a status read command is input, the SQ register **426** sends a status signal SQ to the flash controller **410** under the control of the control unit **425**.

[0051] The status signal SQ is sent to the flash controller **410** to inform the flash controller **410** of the status of the NBX NAND flash memory **420**. For example, when the NBX NAND flash memory **420** does not perform any operation, the status signal SQ is high, and when the NBX NAND flash memory **420** performs an operation, the status signal SQ is low. The status signal is generated in synchronization with a CLK signal. Referring to Table 1, after a status read command is input and one cycle passes, a state signal SQ is output. The flash controller **410** can provide the status signal SQ to the flash memory at anytime.

[0052] An address is input from the first clock cycle after a command is input. The bit size of the address is determined by an nLOAD signal. Erase, write, and read operations of the NBX NAND flash memory **420** of FIG. **6** will now be described with reference to FIGS. **7** through **9**.

[0053] FIG. **7** is a timing diagram illustrating how data are erased from the NBX NAND flash memory **420** of FIG. **6**, according to an exemplary embodiment of the present invention. Referring to FIG. **7**, when an nCE signal and an nLOAD signal are low, a command or an address is input through a C/A pin.

[0054] Referring to FIG. **7**, S denotes a status read command, E denotes an erase command, A denotes an address, and EE denotes an erase enable command. The status read command S can be input regardless of whether an erase operation is performed. When the status read command S is input, the NBX NAND flash memory **420** generates a status signal SQ after one clock cycle.

[0055] The NBX NAND flash memory **420** starts a read operation in response to an erase command. When an erase command is input, an address A is input through the C/A pin. After the address is completely input, an erase enable command EE is input. The NBX NAND flash memory **420** erases data from a memory block corresponding to the address A in response to the erase enable command EE.

[0056] During the erase operation, the NBX NAND flash memory **420** generates a status signal SQ in response to a status read command S to indicate its status (erase status). After the erase operation, the NBX NAND flash memory **420** generates a status signal SQ in response to a status read command S to indicate its status (end of erase operation).

[0057] FIG. **8** is a timing diagram for explaining how data are written into the NBX NAND flash memory **420** of FIG. **6**, according to an exemplary embodiment of the present invention. Referring to **8**, when an nCE signal and an nLOAD signal are low, a command or an address is input through a C/A pin.

[0058] In FIG. **8**, W denotes a write command, A denotes an address, and WE denotes a write enable command. Here, a status read command S can be input regardless of whether a write operation is performed. When the status read command S is input, the NBX NAND flash memory **420** generates a status signal SQ after one clock cycle.

[0059] The NBX NAND flash memory **420** starts a write operation in response to a write command W. After a write command W and an address A are input, a write enable command WE is input. After that, the NBX NAND flash memory **420** receives data through a data input/output (DQ) pin according to the toggling of a data strobe (DQS) signal. Data are input to or output from the NBX NAND flash memory **420** in synchronization with the DQS signal. Referring to FIG. **8**, data are transferred twice per one period of the DQS signal by a double data rate (DDR) transmission method.

[0060] After the data are received, the NBX NAND flash memory **420** performs programming on a page corresponding to the address A using the received data. During the write operation, the NBX NAND flash memory **420** generates a status signal SQ in response to a status read command S to indicate its status (write status). After the write operation, the NBX NAND flash memory **420** generates a status signal SQ in response to a status read command S to indicate its status (end of write operation).

[0061] FIG. **9** is a timing diagram for explaining how data are read from the NBX NAND flash memory **420** of FIG. **6**, according to an exemplary embodiment of the present invention. In FIG. **9**, R denotes a read command, A denotes an address, and RE denotes a read enable command. A status read command S can be input regardless of whether a read operation is performed. When the status read command S is input, the NBX NAND flash memory **420** generates a status signal SQ after one clock cycle.

[0062] The NBX NAND flash memory **420** starts a read operation in response to a read command R. After a read command R and an address A are input, the **420** reads data from a page corresponding to the address A and stores the data in the page buffer **423** (refer to FIG. **6**). The NBX NAND flash memory **420** outputs a status signal SQ in response to a status read command S indicating that the NBX NAND flash memory **420** is ready for data transmission.

[0063] The NBX NAND flash memory **420** outputs the data stored in the page buffer **423** in response to a read enable command RE. The NBX NAND flash memory **420** outputs the data through a DQ pin according to the toggling of a DQS signal. Data are output from the NBX NAND flash memory **420** in synchronous with the DQS signal. Referring to FIG. **9**, data are read from the NBX NAND flash memory **420** at double data rate (DDR).

[0064] As explained above, the NBX NAND flash memory of the present invention includes separate C/A and DQ pins. Furthermore, the NBX NAND flash memory includes the SQ register to generate a status signal SQ whenever the flash controller sends a status read command S. Since the CA pin and the DQ pin are separate, read and write speeds can be increased. Furthermore, command and address buses can have a width different from that of a data bus.

[0065] FIG. **10** is a diagram illustrating an NBX NAND flash memory system **500** according to an exemplary embodi-

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ment of the present invention. Referring to FIG. **10**, the NBX NAND flash memory system **500** includes a flash controller **550** and a plurality of NBX flash modules **510**, **520**, **530**, and **540**. In the exemplary embodiment of FIG. **10**, four NBX flash modules are illustrated.

[0066] The NBX flash modules **510**, **520**, **530**, and **540** are connected to flash sockets **501**, **502**, **503**, and **504**, respectively, and the flash sockets **501**, **502**, **503**, and **504** are connected to the flash controller **550** through a data bus (DQ bus). The NBX flash modules **510**, **520**, **530**, and **540** receive a bank selection (nBS) signal from the flash controller **550**. Furthermore, data (DQ) and control (CTRL) signals are transmitted between the flash controller **550** and the NBX flash modules **510**, **520**, **530**, and **540**. Each of the NBX flash modules **510**, **520**, **530**, and **540** includes a plurality of NBX NAND flash memories. In the exemplary embodiment shown in FIG. **10**, each of the NBX flash modules **510**, **520**, **530**, and **540** includes sixteen NBX NAND flash memories **511**.

[0067] The flash controller **550** controls write, read, and erase operations of the NBX NAND flash memories of the NBX flash modules **510**, **520**, **530**, and **540**. Furthermore, the flash controller **550** performs bank interleaving between banks using the nBS signal.

[0068] When it is necessary to update SQ registers of the NBX NAND flash memories of the NBX flash modules **510**, **520**, **530**, and **540**, the flash controller **550** can transmit a register value that can be commonly used for all the NBX flash modules **510**, **520**, **530**, and **540**. This function of the flash controller **550** is referred to as a broadcasting function. After simultaneously enabling nBS signals for all banks, the flash controller **550** provides a register configuration command (refer to Table 1). The register configuration command is simultaneously provided to each of the NBX NAND flash memories through a C/A pin. Then, the flash controller **550** writes a register value to an SQ register using the C/A pin.

[0069] FIG. **11** is a block diagram illustrating an NBX flash module of the NBX NAND flash memory system **500** of FIG. **10**, according to an exemplary embodiment of the present invention. in FIG. **11**, reference numeral **510***a* denotes a front surface of the NBX flash module **510** of the NBX NAND flash memory system **500**, and reference numeral **510***b* denotes a back surface of the NBX flash module **510**.

[0070] Referring to FIGS. **11**(*a*) and (*b*), eight NBX NAND flash memories **511***a* are formed in the front surface **510***a* of the NBX flash module **510**, and eight NBX NAND flash memories **511***b* are formed on the back surface **510***b* of the NBX flash module **510**. The eight NBX NAND flash memories **511***a* form one bank, and the eight NBX NAND flash memories **511***b* form another bank. For example, one NBX flash module includes two banks. When each of the NBX NAND flash memories **511***a* and **511***b* has an 8-bit bus width, one bank has a 64-bit bus width.

[0071] An electrically erasable programmable read only memory (EEPROM) **512** for status presence detection (SPD), a clock buffer **513**, a buffer **514** for C/A and control signals, and an interface **516***a* are formed on the front surface **510***a* of the NBX flash module **510**. The EEPROM **512** is used to store data (SPD data) necessary for the flash controller **550** (refer to FIG. **10**) to access the NBX flash module **510**. The clock buffer **513** is used for distributing a clock signal to the NBX NAND flash memories **511***a* and **511***b*. The buffer **514** is used for distributing command, address, and control signals to the NBX NAND flash memories **511***a* and **511***b*.

[0072] Fast enable transfer (FET) switches **515** and an interface **516***b* are formed on the back surface **510***b* of the NBX flash module **510**. The FET switches **515** are used to reduce loads on data buses, thereby enabling high-speed data transmission. Since a DDR transmission method is used for the NBX NAND flash memories **511***a* and **511***b*, the FET switches **515** are used to facilitate the use of the DDR transmission method. Each of the FET switches **515** can latch 10 bits: 8 bits for data (DQ), 1 bit for a DQS signal, and 1 bit for a SQ signal. When assembled, the interfaces **516***a* and **516***b* of the NBX flash module **510** are connected to the flash socket **510** (refer to FIG. **10**).

[0073] FIG. **12** is a block diagram illustrating an internal structure of the NBX flash module **510** of FIG. **11**, according to an exemplary embodiment of the present invention. As illustrated in FIG. **11**, the NBX flash module **510** includes the NBX NAND flash memories **511***a* and **511***b* (first and second banks), the EEPROM **512** for SPD, the clock buffer **513**, the buffer **514** for C/A and control signals, the FET switches **515**, and the interface **516**.

[0074] The interface **516** receives a command, an address, data, first and second bank selection signals nBS1 and nBS2, and an nLOAD signal from the flash controller **550** (refer to FIG. **10**). Here, the nBS1 signal is used for selecting the first bank **511***a*, and the nBS2 signal is used for selecting the second bank **511***b*.

[0075] The nBS1 signal is provided as a chip enable signal nCE for the NBX NAND flash memories of the first bank **511***a*. The nBS2 signal is provided as a chip nCE signal for the NBX NAND flash memories of the second bank **511***b*. The buffer **514** for C/A and control signals is used to temporarily store a command, an address, and an nLOAD signal and sends them to a selected bank.

[0076] The clock buffer **513** receives a clock signal nCLK and generates first and second clock signals CLK1 and CLK2. The first clock signal CLK1 is provided to the first bank **511***a*, and the second clock signal CLK2 is provided to the second bank **511***b*. Furthermore, the clock buffer **513** provides a clock signal for the buffer **514** for C/A and control signals. The buffer **514** is operated in synchronization with a clock signal.

[0077] The EEPROM **512** for SPD stores SPD information necessary for the flash controller to access the NBX flash module **510** For example, the EEPROM **512** for SPD stores information about internal delay time necessary for writing data to or reading data from the NBX NAND flash memories of the first and second banks **511***a* and **511***b*. In read or write operation, the flash controller **550** reads the internal delay time information from the EEPROM **512** and outputs signals and data according to the read information for read or write operation.

[0078] NBX NAND flash memories included in a given bank have the same page size. Information about this page size is stored in the EEPROM **512**. The page size of a NBX NAND flash memory may vary from one bank to another bank and/or from one NBX flash module to another NBX flash module. The EEPROM **512** for SPD stores this page information. When accessing a NBX flash module, the flash controller **550** reads the page information from the EEPROM **512** and operates according to the read page information.

[0079] Banks included in one NBX flash module can have different storage capacities. In addition, NBX NAND flash memories included in one bank can have different storage capacities. The EEPROM **512** for SPD stores information

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about the bank capacities of banks. When accessing a NBX flash module, the flash controller **550** reads the bank capacity information from the EEPROM **512** and operates according to the read bank capacity information. That is, the flash controller **550** reads SPD information from the EEPROM **512** and sets itself using the SPD information.

[0080] FIGS. **13** through **15** are timing diagrams for explaining a bank interleaving operation of the NBX NAND flash memory system **500** of FIG. **10**, according to an exemplary embodiment of the present invention. Bank interleaving is a read, write, or erase operation that is performed alternately on banks. FIG. **13** illustrates an interleaving operation between banks for reading data from the banks. FIG. **14** illustrates an interleaving operation between banks for writing data to the banks. FIG. **15** illustrates an interleaving operation between banks for erasing, writing, and reading.

[0081] Referring to FIG. **13**, a first bank is enabled by a first bank selection signal nBS1. For example, when the first bank selection signal nBS1 is at a low level, data are read from the first bank. Reading data from the first bank starts in response to a read command R. After the read command R and an address A is input, data are read from a selected page and transmitted to a page buffer. When data corresponding to one page is stored in the page buffer, an NBX NAND flash memory outputs a status signal SQ in response to a status read command S to indicate that it is ready to output data.

[0082] The NBX NAND flash memory outputs the data stored in the page buffer in response to a read enable command RE. Here, the NBX NAND flash memory outputs the data through a data input/output pin DQ according to the toggling of a data strobe signal DQS.

[0083] When a second bank selection signal nBS2 is changed to a low level during the reading operation for the first bank, data are read from a second bank. Similarly, when a third bank selection signal nBS3 is changed to a low level during the reading operations for the first and second banks, data are read from a third bank. The reading operations for the second and third banks are performed in the same manner as that for the first bank.

[0084] After data are output from the first bank, data are output from the second bank without a delay time. Similarly, after data are output from the second bank, data are output from the first bank.

[0085] Referring to FIG. **14**, when a first bank selection signal nBS1 is at a low level, data are written into a first bank. Writing data into the first bank starts in response to a write command W. After the write command W and an address A are input, a write enable command WE is input. An NBX NAND flash memory receives data through a data input/output pin DQ according to the toggling of a data strobe signal DQS. The received data are stored in a page buffer.

[0086] After data are stored in the page buffer, the NBX NAND flash memory performs internal programming on a page of the address A using the stored data. The NBX NAND flash memory outputs a status signal SQ in response to a status read command S to indicate the end of the write operation.

[0087] When second and third bank selection signals are changed to a low level during the write operation for the first bank, data are written into second and third banks. The write operations for the second and third banks are performed in the same manner as that for the first bank.

[0088] Referring to FIG. **14**, after data are completely loaded from a flash controller to a page buffer of the first bank, data are loaded from the flash controller to a page buffer of the second bank without a delay time. Similarly, after the data are loaded to the page buffer of the second bank, data are loaded from the flash controller to a page buffer of the third bank.

[0089] Referring to FIG. **15**, an erase operation is performed on a first bank, a write operation is performed on a second bank, and a read operation is performed on a third bank. During the erase operation for the first bank, the write operation for the second bank is performed. In addition, during the erase and write operations for the first and second banks, the read operation for the third bank is performed.

[0090] Since a conventional NAND flash memory uses a data input/output pin DQ for receiving command and address signals as well as data, a data stream in a data bus or channel is often interrupted. Furthermore, a conventional NAND flash memory module has a long data delay time during an bank interleaving operation. However, as illustrated in FIGS. **13** through **15**, the NBX flash module of exemplary embodiments of the present invention can perform an interleaving operation for data input/output without a data delay time, so that data can be read from and written to the NBX flash module at a high speed.

[0091] FIG. **16** illustrates a thin small outline package (TSOF) of an NBX NAND flash memory according to an exemplary embodiment of the present invention, and FIG. **17** is a table providing descriptions of pins of the TSOP of FIG. **16**, according to an exemplary embodiment of the present invention. Referring to FIG. **16**, the NBX NAND flash memory has 48 pins. The 1st to 24th pins are formed on the left side, and the 25th to 48th pins are formed on the right side. Referring to FIG. **17**, all control functions are assigned to the left-side pins. According to exemplary embodiments of the present invention, the number of pins can be decreased, and the NBX NAND flash memory can be designed to have all controls pins on one side. Therefore, the NBX NAND flash memory can have a simple structure.

[0092] As described above, in the NAND flash memory of exemplary embodiments of the present invention, the C/A pin is separated from the data input/output pin. Therefore, data input/output speed can be improved. Furthermore, the NAND flash memory can perform a bank interleaving operation with less delay time.

[0093] The above-disclosed subject matter is to be considered illustrative, and not restrictive. It will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention.

What is claimed is:

1. A NAND flash memory comprising:
- a memory cell array storing data;
- a command/address pin through which a command and an address are received for transmitting data; and
- a data input/output pin through which data are transmitted in the memory cell array.

2. The NAND flash memory of claim **1**, further comprising a status register receiving a status read command through the command/address pin and providing an operational status of the NAND flash memory to a flash controller.

3. The NAND flash memory of claim **2**, wherein the flash controller sends the status read command to the NAND flash memory.

4. The NAND flash memory of claim **2**, wherein the status register sends a status signal SQ to the flash controller to inform the flash controller whether the NAND flash memory is internally operational.

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5. The NAND flash memory of claim 4, wherein the flash controller controls the internal operation of the NAND flash memory in response to the status signal SQ.

6. The NAND flash memory of claim 1, wherein the data transmitted through the data input/output pin is transmitted according to a toggling of a data strobe signal DQS.

7. The NAND flash memory of claim 6, wherein the data transmitted through the data input/output pin is transmitted by a DDR (double data rate) transmission method.

8. The NAND flash memory of claim 1, further comprising a command/address buffer receiving the command and address received through command/address pin.

9. The NAND flash memory of claim 8, further comprising a control unit controlling the reception of the command and address.

10. The NAND flash memory of claim 9, wherein the control unit receives a chip enable signal nCE and a load signal nLOAD from a flash controller and controls the reception of the command and address.

11. A flash memory system comprising:

a flash controller, and

a flash memory module comprising a plurality of NAND flash memories,

wherein each of the NAND flash memories comprises:

a memory cell array storing data;

a command/address pin through which a command and an address are received from the flash controller for transmitting data in the memory cell array; and

a data input/output, pin through which data is transmitted in the memory cell array.

12. The flash memory system of claim 11, wherein each of the NAND flash memories further comprises a status register receiving a status read command through the command/address pin and providing an operational status of the NAND flash memory to the flash controller.

13. The flash memory system of claim 12, wherein the flash controller sends the status read command to the NAND flash memory.

14. The flash memory system of claim 12, wherein the status register sends a status signal SQ to the flash controller to inform the flash controller whether the NAND flash memory is internally operational.

15. The flash memory system of claim 14, wherein the flash controller controls the internal operation of the NAND flash memory in response to the status signal SQ.

16. The flash memory system of claim 11, wherein the data transmitted through the data input/output pin is transmitted according to a toggling of a data strobe signal DQS.

17. The flash memory system of claim 16, wherein the data transmitted through the data input/output pin is transmitted by a DDR (double data rate) transmission method.

18. The flash memory system of claim 1, wherein each of the NAND flash memories further comprises a command/address buffer receiving the command and address received through command/address pin.

19. The flash memory system of claim 18, wherein each of the NAND flash memories further comprises a control unit controlling the reception of the command and address.

20. The flash memory system of claim 19, wherein the control unit receives a chip enable signal nCE and a load signal nLOAD from the flash controller and controls the reception of the command and address.

* * * * *

BNSDOCID: <US____20080162790A1_I_>

US 20090103387A1

(19) **United States**

(12) **Patent Application Publication**

Shau

(10) **Pub. No.: US 2009/0103387 A1**

(43) **Pub. Date: Apr. 23, 2009**

(54) **HIGH PERFORMANCE HIGH CAPACITY MEMORY SYSTEMS**

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(21) Appl. No.: **11/874,914**

(22) Filed: **Oct. 19, 2007**

Publication Classification

(51) **Int. Cl.**
G11C 8/00 (2006.01)
H05K 3/00 (2006.01)

(52) **U.S. Cl.** **365/230.02**; 29/829

(57) **ABSTRACT**

The present invention provides memory system architectures developed to increase the capacity of memory systems. Typically applications including the main memory of computers. Memory systems of the present invention can achieve capacities larger than prior art systems by one or two orders of magnitudes without significant degradation in performance while using system interfaces that are compatible with existing memory systems with no or minimal modifications.

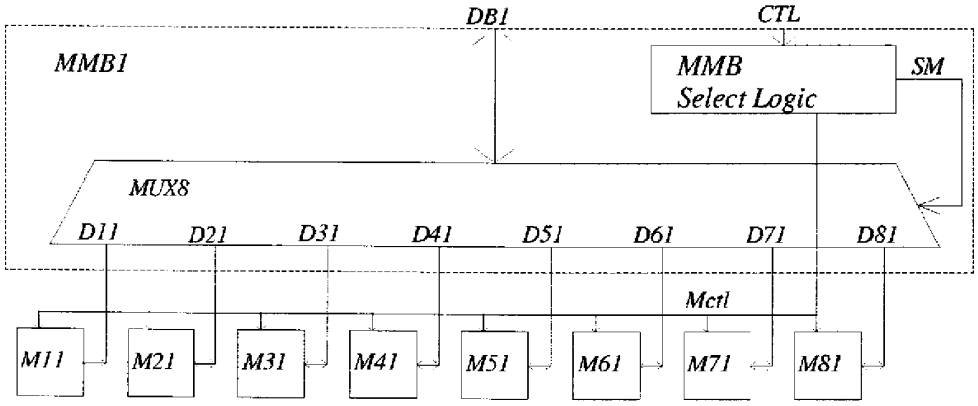

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FIG. 1(a) Prior art

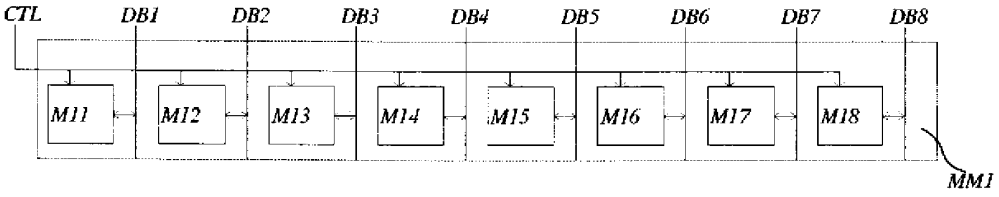

FIG. 1(b) Prior art

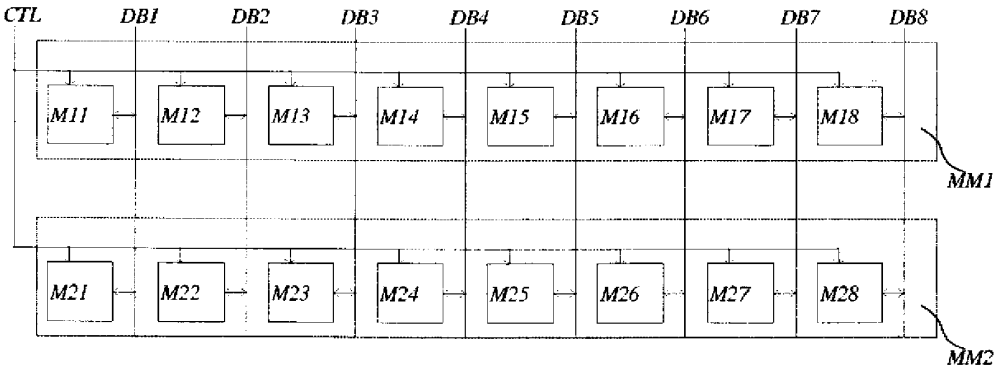

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FIG. 1(c) Prior art

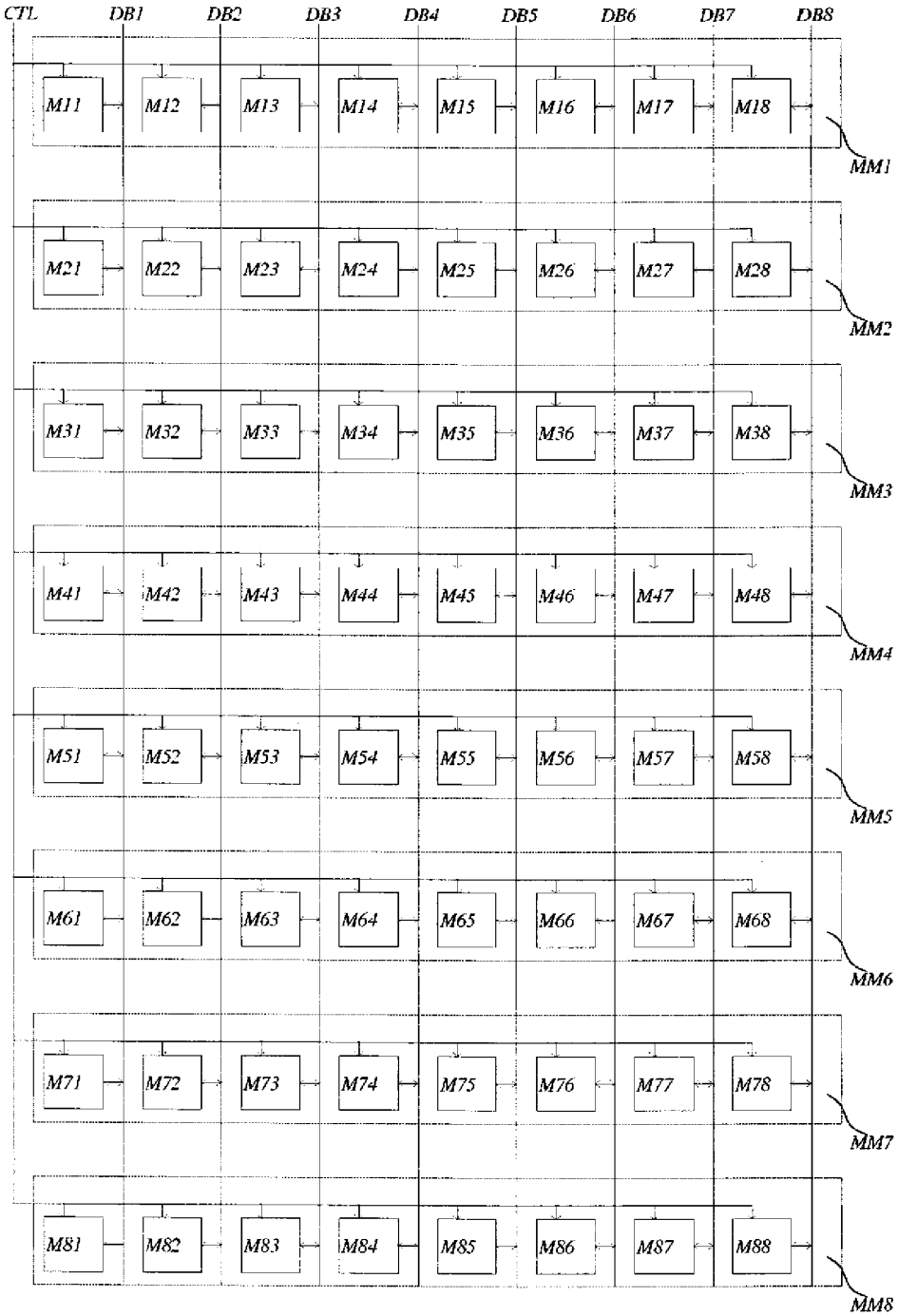

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FIG. 2(a) Prior art

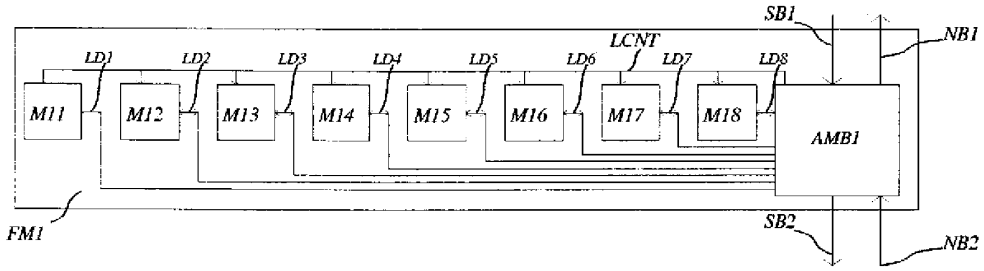

FIG. 2(b) Prior art

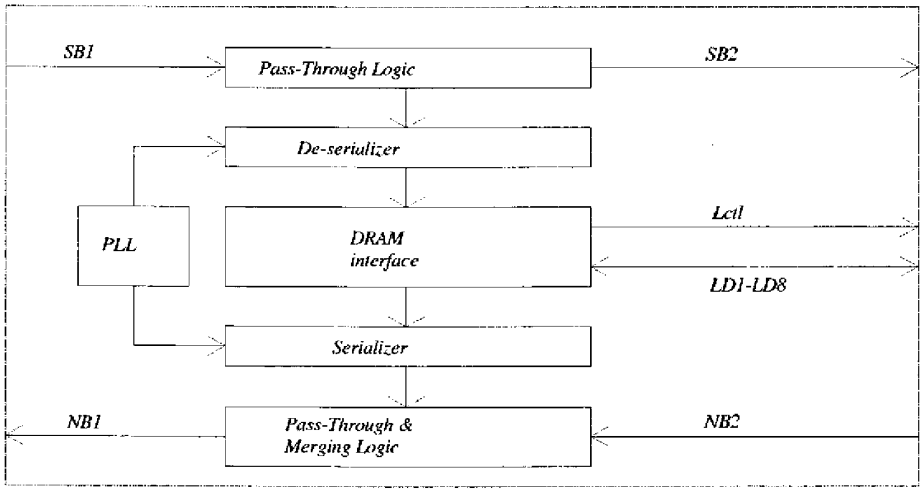

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FIG. 2(c) Prior art

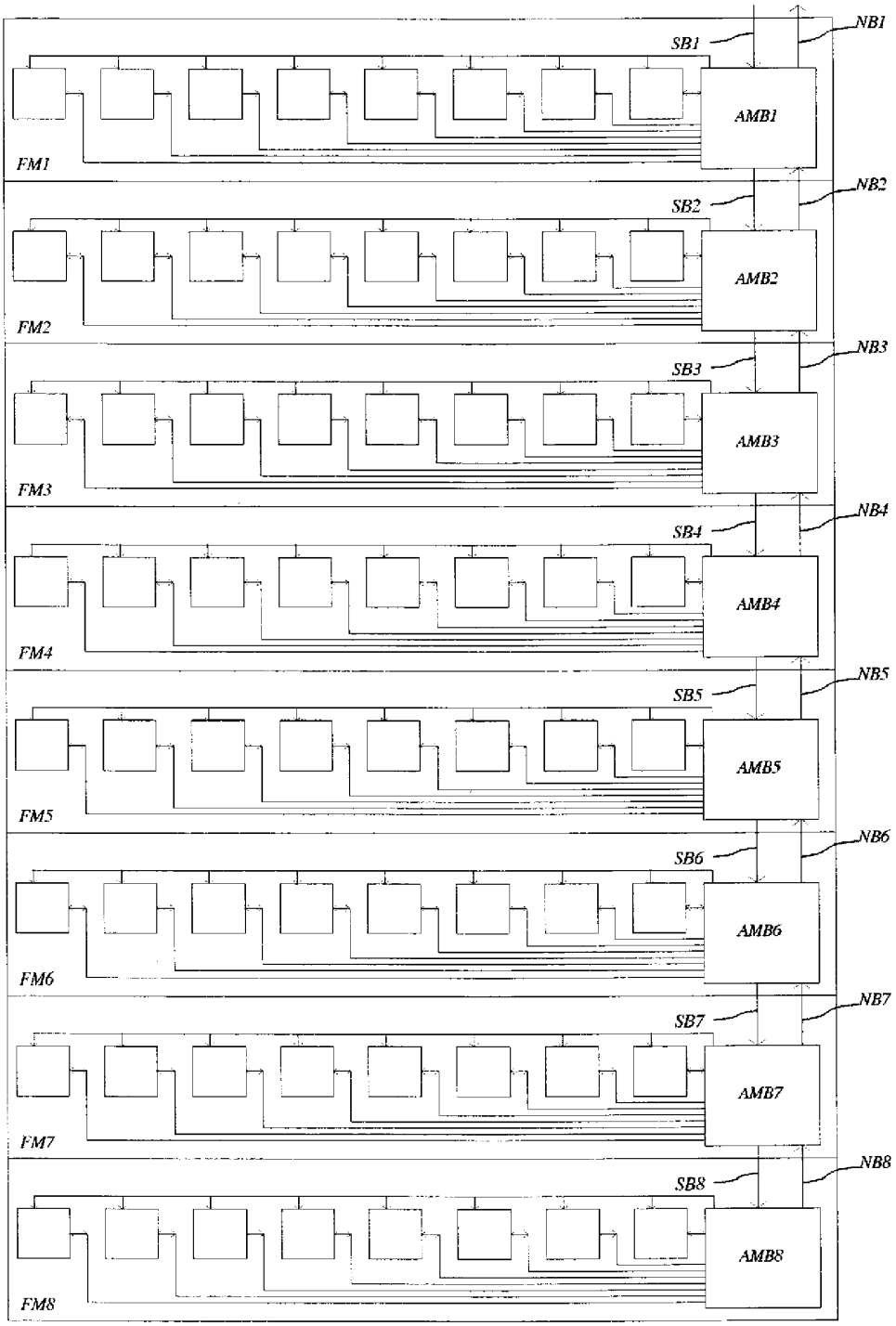

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FIG. 3(a)

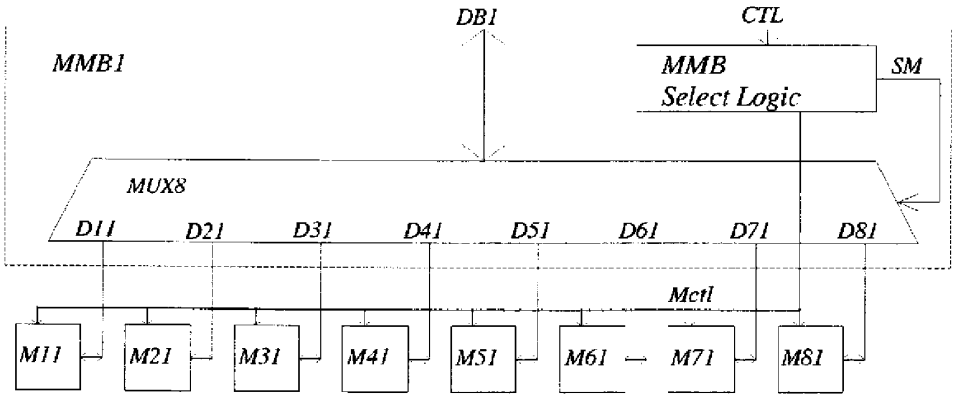

FIG. 3(b)

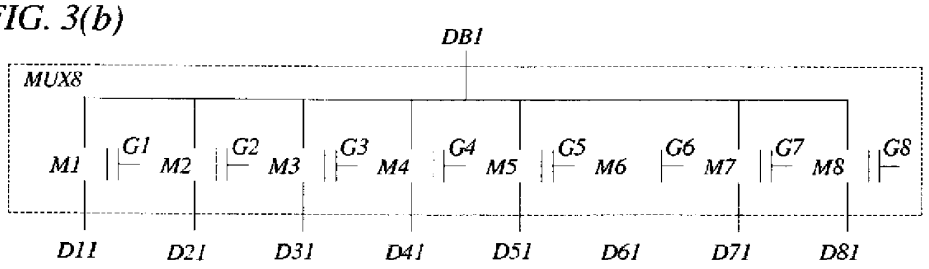

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FIG. 3(c)

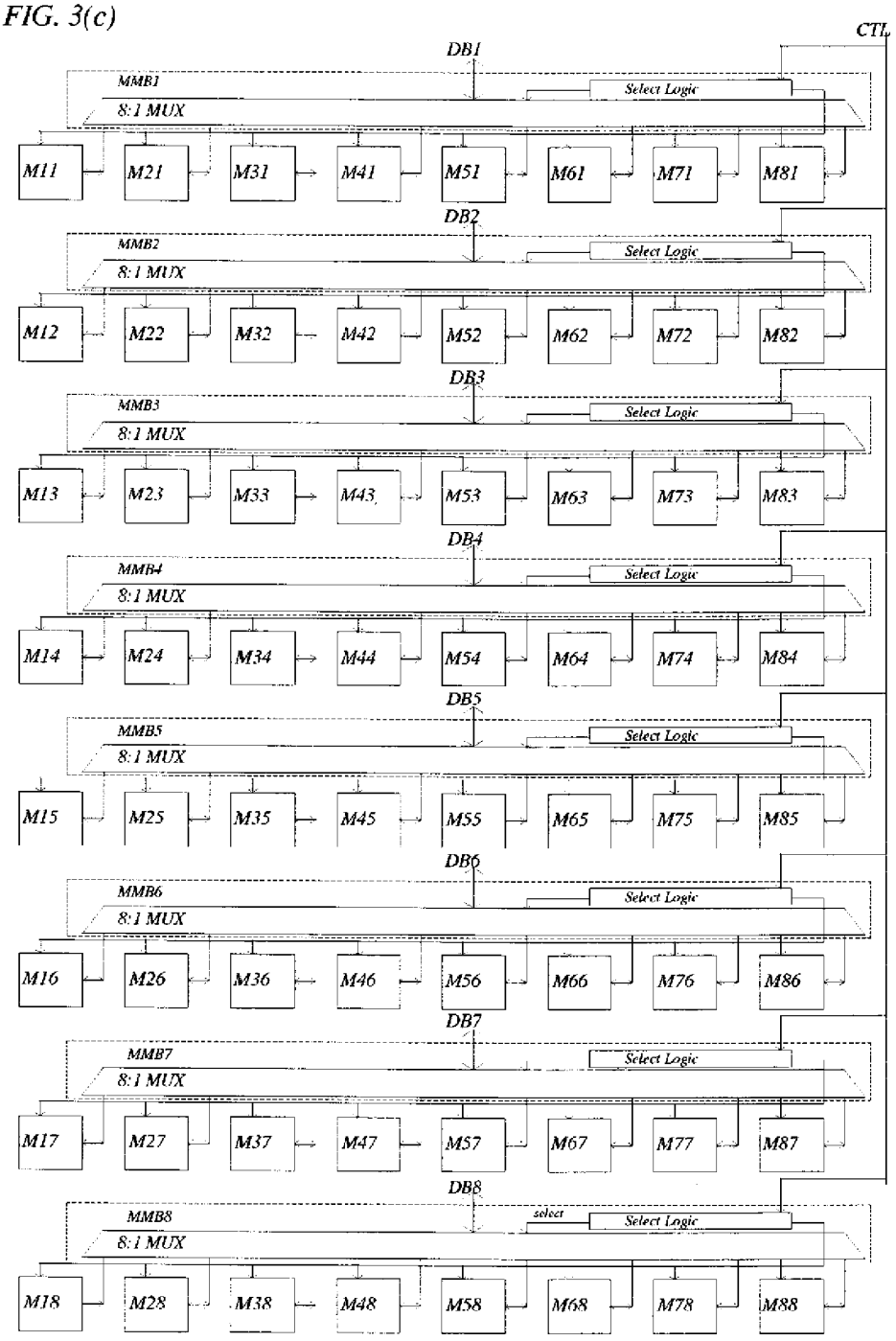

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FIG. 4(a)

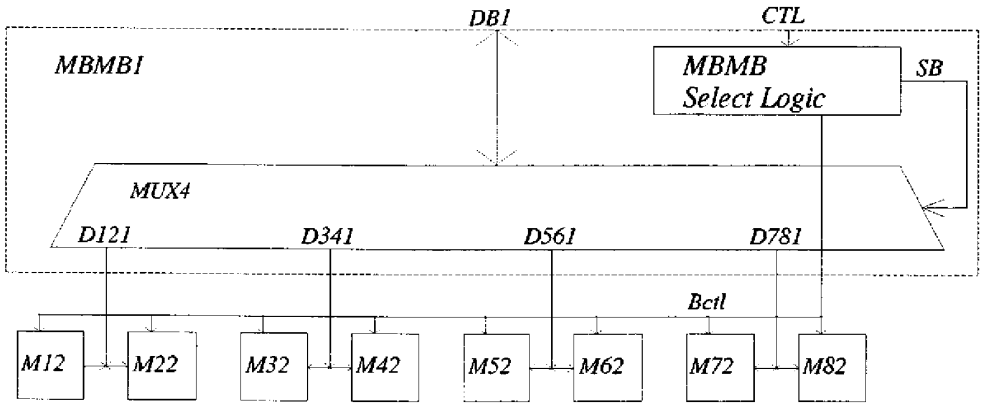

FIG. 4(b)

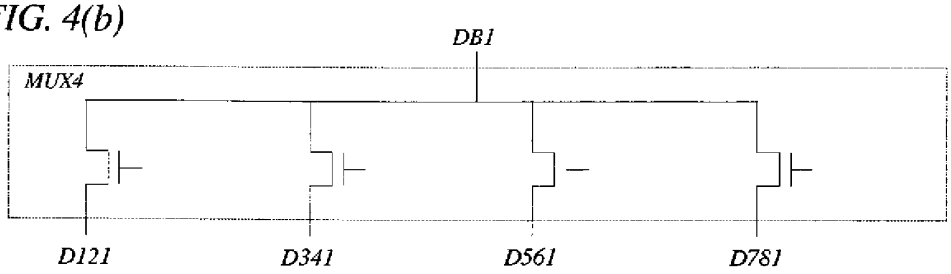

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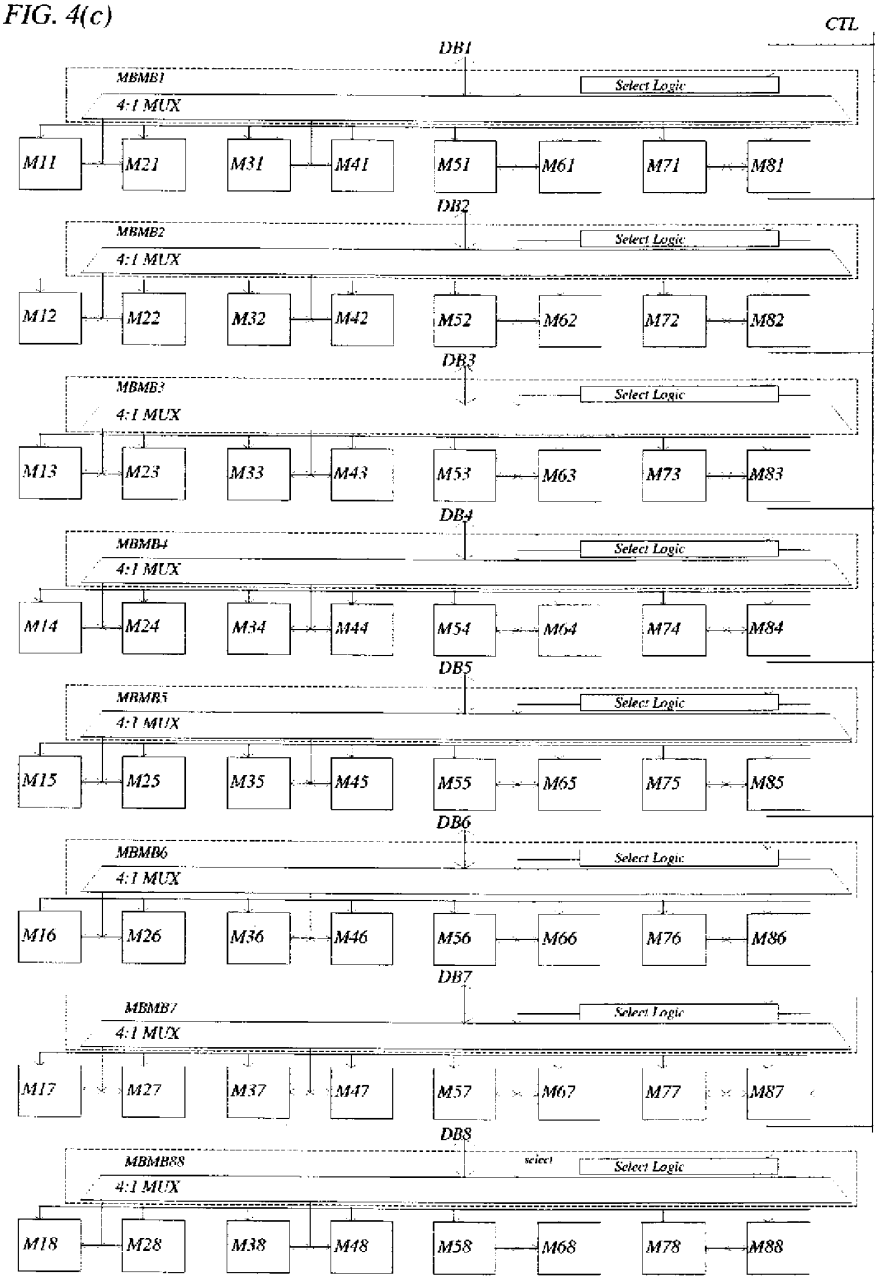
FIG. 4(c)



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HIGH PERFORMANCE HIGH CAPACITY MEMORY SYSTEMS

BACKGROUND OF THE INVENTION

[0001] The present invention relates to structures and methods designed to increase the capacity of high performance memory systems.

[0002] The present invention is applicable to most types of memories such as dynamic random access memory (DRAM), static random access memory (SRAM), nonvolatile memories, etc. Among the wide varieties of possible applications, the most well known applications are the main memory in computers. We will focus on computer main memory using double data rate version 2 (DDR2) dynamic random access memory (DRAM) as examples to demonstrate the basic principles of the present invention. The scope of the present invention is certainly not limited to particular types of memory or particular types of applications used in our examples.

[0003] A "memory system" defined in this patent application is board level circuits supporting memory operation of memory chips. A "memory module" is defined as a subcircuit of a memory system. A "system level signal" is defined as an electrical signal used to communicate with circuits external to a memory system. A "chip level signal" is defined as an electrical signal used to communicate with memory chips.

[0004] It is well known that the performance of a computer is strongly dependent on both the performance as well as the capacity of its main memory. Ideally, a computer wants to have high performance system memory at as large capacity as possible. In reality, high performance and high capacity have conflicting requirements that can become limiting factors. We will discuss key factors on those limitations using typical personal computer memory systems as examples.

[0005] The most common memory chip used for computer system memory is DRAM. Table 1 lists typical chip level interface signals for a current art 1 G (2^{30}) bit DDR2 synchronized DRAM integrated circuit chip.

TABLE 1

Standard 1G-bit DDR2 DRAM Interface signals

Name	Type	Descriptions
DQ0-DQ7	In/out	8-bit data Bidirectional bus
DQS, DQS#	In/out	Bidirectional data strobe
DM	input	Input data mask
A0-A12	input	Addresses
BA0-BA2	input	Bank addresses
CK, CK#	input	Differential clocks
CKE	input	Clock enable
CS#	input	Chip select
RAS#, CAS#, WE#	input	Command inputs; alone with CS# define commands
ODT	input	On-die termination
Vref	input	Reference voltage
VDD, VDDQ, VDDL, VSS, VSSQ, VSSL	power	Power and ground lines for core, I/O, and DLL

[0006] DRAM chips are typically mounted on small printed circuit board (PCB) called Single-In-line Memory Module (SIMM) or Dual-In-line Memory Module (DIMM); a DIMM is equivalent to two SIMM modules placed into one PCB utilizing both sides of the circuit board. The SIMM or DIMM memory modules provide the flexibility to expand the capacity of computer main memory. The memory controller in chipset typically has the flexibility to support 8 SIMM or 4 DIMM modules. A personal computer typically starts with one installed DIMM module while providing additional empty sockets. A user who wants to improve the performance of computer can insert additional modules into the expandable sockets. To support such expandable memory systems, personal computers typically support a system level memory interface with signals listed in Table 2.

TABLE 2

Standard personal computer system memory interface signals

Name	Type	Descriptions
DQ0-DQ63	In/out	64-bit data Bidirectional bus, supported by eight 8-bit data bus. 8 more data (DQ64-DQ71) can be added for parity or error correction code (ECC).
DQS0-DQS7, DQS0#-DQS7#	In/out	Bidirectional data strobe, one pair for each 8-bit data bus. One more pair (DQS8, DQS8#) can be added for parity or ECC.
DM0-DM7.	input	Input data mask. One for each 8-bit data bus. One more (DM8) can be added for parity or ECC.
A0-A13	input	Addresses, may have more or less address bits.
BA0-BA2	input	Bank addresses, may have only two bank address bits.
CK, CK#	input	Differential clocks, may have separated clocks for different modules
CKE0-CKE7	input	Clock enable, one fore each memory module
CS#0-CS#7	input	Chip select signals, one for each memory module.
RAS#, CAS#, WE#	input	Command inputs.
ODT0-ODT7	input	On-die termination, one for each memory module
RESET#	input	Reset
PAR_IN	input	Parity bit for address and control
PAR_ERR	output	Parity error found in address and control
SCL, SA0-SA2	input	EEPROM clock and addresses
SDA	In/out	EEPROM data
Vref	input	Reference voltage

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TABLE 2-continued

Standard personal computer system memory interface signals

Name	Type	Descriptions
VDD, VDDQ, VDDL, VDDE, VSS, VSSQ, VSSL	power	Power and ground lines for core, I/O, and DLL

[0007] If we draw all these signals in our figures, the resulting figures will be very busy, making it less clear in demonstrating the key points of the present invention. Therefore, in our figures the interface signals are simplified into two groups, namely data signals and control signals. Data signals (DB) are signals directly related to data transfers while following the same signal transfer protocols, including the data bus (DQ), data strobe (DQS and #DQS), and input data mask (DM) signals. Control signals (CTL) are signals used to determine operation states of the memory chips, including the addresses, bank addresses, clocks signals (CK, CK#, CKE), chip select signal (CS#), and command inputs (RAS#, CAS#, WE#). We will not show DC or slow signals such as power lines, reference voltage signals, EEPROM signals, and on-die-termination signals because those connections are not related to the key factors of the present invention. To facilitate clear understanding of the present invention, there is no need to show those details that are well known to people skilled in the art; we will focus on the key elements related to the present invention—the data and control signals of memory chips. For simplicity, the optional parity/ECC data signals are also not included in our discussion because a person with ordinary skill in the art would understand how to apply the present invention on the parity/ECC signals upon disclosure of our examples. The simplified representations of memory interface signals used in our discussions are listed in Table 3.

TABLE 3

Simplified representation of memory interface signals

meaning	representation	Corresponding signals in Table 2
Data signal bus 1	DB1	DQ0-DQ7, DQS0, DQS#0, DM0
Data signal bus 2	DB2	DQ8-DQ15, DQS1, DQS#1, DM1
Data signal bus 3	DB3	DQ16-DQ23, DQS2, DQS#2, DM2
Data signal bus 4	DB4	DQ24-DQ31, DQS3, DQS#3, DM3
Data signal bus 5	DB5	DQ32-DQ39, DQS4, DQS#4, DM4
Data signal bus 6	DB6	DQ40-DQ47, DQS5, DQS#5, DM5
Data signal bus 7	DB7	DQ48-DQ53, DQS6, DQS#6, DM6
Data signal bus 8	DB8	DQ54-DQ63, DQS7, DQS#7, DM7
Control signals	CTL	A0-A13, BA0-BA2, CK, CK#, CS#0-CS#7, CKE0-CKE7, RAS#, CAS#, WE#
Not shown		DQ64-DQ71, DQS8, DQS#8, DM8, ODT0-ODT8, RESET#, PAR_IN, PAR_ERR, SCL, SA0-SA2, Vref, VDD, VDDQ, VDDL, VDDE, VSS, VSSQ, VSSL

[0008] Using the simplified representations in Table 3, the architectures of typical prior art memory systems can be illustrated by FIGS. **1**(*a-c*). FIGS. **1**(*a*) is the simplified schematic block diagrams for a typical prior art memory module (MM**1**). This memory module comprises a plurality of memory chips (M**11**-M**18**) that shares the same control signals (CTL). The data signals of memory chips are connected in parallel: the first memory chip (M**11**) supports data signal bus **1** (DB**1**); the second memory chip (M**12**) supports data signal bus **2** (DB**2**); the third memory chip (M**13**) supports data signal bus **3** (DB**3**); the forth memory chip (M**14**) supports data signal bus **4** (DB**4**); the fifth memory chip (M**15**) supports data signal bus **5** (DB**5**); the sixth memory chip (M**16**) supports data signal bus **6** (DB**6**); the seventh memory chip (M**17**) supports data signal bus **7** (DB**7**); the eighth memory chip (M**18**) supports data signal bus **8** (DB**8**). The width of module level data bus is therefore the combined width of all memory chips (M**11**-M**18**) on the same module (MM**1**). We will call such connection as "parallel data connection" in the following discussions.

[0009] A common prior art method to increase the capacity of a memory system is to use DIMM modules instead of SIMM modules. FIG. **1**(*b*) shows the simplified schematic block diagram for a DIMM module. A DIMM module comprises one additional memory module (MM**2**) that is typically placed on the other side of the same print circuit board used to place the first memory module (MM**1**). The memory chips (M**21**-M**28**) of the second memory module (MM**2**) are connected in the same way as that of the first memory module (MM**1**). Since both memory modules (MM**1**, MM**2**) share the same data signals (DB**1**-DB**8**) in a shared bus structure, each memory module must use different chip select signals (part of CTL but not shown separately in figures for simplicity) to avoid driver conflicts: typically, different modules are also connected to different clock enable signals (not shown). Other than chip enable and clock enable signals, typically all other control signals are the same for all memory modules. The two memory modules (MM**1**, MM**2**) on the same DIMM module often can share most of signal lines so that the increase in loading is typically less than twice of a single module. Using DIMM module is therefore an efficient prior art method to increase the capacity of memory systems.

[0010] If we want to have larger capacity than a DIMM module, we need to add more memory modules to the system. FIG. **1**(*c*) shows the simplified schematic block diagram for a memory system that has **6** additional memory modules. The memory chips (M**31**-M**38**) of the third memory module (MM**3**) are connected in the same way as that of the first memory module (MM**1**). The memory chips (M**41**-M**48**) of the forth memory module (MM**4**) are connected in the same way as that of the first SIMM module (MM**1**). The memory chips (M**51**-M**58**) of the fifty memory module (MM**5**) are connected in the same way as that of the first memory module (MM**1**). The memory chips (M**61**-M**68**) of the sixth memory module (MM**6**) are connected in the same way as that of the first SIMM module (MM**1**). The memory chips (M**71**-M**78**) of the seventh memory module (MM**7**) are connected in the same way as that of the first memory module (MM**1**). The memory chips (M**81**-M**88**) of the eighth memory module (MM**8**) are connected in the same way as that of the first

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SIMM module (MM1). All the memory modules in the same system share the same data signals (DB1-DB8) in a shared bus structure. Therefore, each memory module must use different chip select signals (part of CTL but not shown separately in figures for simplicity) to avoid driver conflicts; typically, different modules are also connected to different clock enable signals (not shown). Other than chip enable and clock enable signals, typically all other control signals are the same for all memory modules.

[0011] The capacity of the memory system in FIG. **1**(*c*) is four times the capacity of the memory system in FIG. **1**(*b*). However, when the number of memory modules is increased, the loading on the shared data signals (DB1-DB8) and control signals (CTL) also increases. The "Loading" on a signal is the non-ideal factors that can slow down signals performances such as leakage currents, parasitic capacitances, inductances, or resistances. The loadings for the system in FIG. **1**(*c*) are about four times that of the system in FIG. **1**(*b*). Increase in loading typically means degradation in performance and/or stability. This problem is especially significant for prior art DDR2 synchronized DRAM with data rate higher than 600 millions of bits per second (MPS) per pin. DDR2 DRAM uses Stub Series Terminated Logic (SSTL) buses with on-chip terminal resistors so that each memory chip (even when it is not active) is sinking currents through terminal resistors, making it impractical to connect large number of prior art memory modules. It is well known that using multiple DDR2 DIMM modules would degrade performance significantly, especially at data rate higher than 600 millions of bits per second (MPS) per pin. Increasing capacity by adding more and more prior art memory modules is therefore not practical. It is therefore strongly desirable to provide methods that can increase the capacity of a memory system without increasing the loading of data and control signals.

[0012] One prior art solution to solve the loading problem is to use phase locked loop (PLL) to generate local clock signals, and use buffers to generate local control signals. Such methods reduce the loading on control signals, but the loading problems in data signals are not solved.

[0013] Another prior art solution for the loading problem is the JEDEC standard "Fully Buffered DIMM" (FBDIMM) approach. An FBDIMM uses an integrated circuit (IC) chip called "Advanced Memory Buffer (AMB)" to control all the interface signals to all memory chips on the module. The loadings on memory chip data and control signals are therefore completely isolated from other memory modules. FIG. **2**(*a*) is a simplified schematic block diagrams for an FBDIMM (FM1). The memory chips (M11-M18) on the FBDIMM (FM1) are arranged in parallel data connection while the data signals (LD1-LD8) and control signals (LCTL) of the memory chips are internal signals controlled by an advanced memory buffer (AMB1). FIG. **2**(*b*) is a simplified schematic block diagram for prior art AMB. The inputs of an AMB come from south bound signal transfer lanes (SB1) that typically comprise 10 pairs of high speed differential signal transfer lines. Currently, each pair of the differential signal transfer lines is capable of transferring signals at 4.8 billion bits per second (GPS). The input signals on SB1 are latched and analyzed by pass-through logic circuits. If the inputs request operations to other FBDIMM, the input signals are passed to the next FBDIMM through another south bound signal transfer lanes (SB2). If the inputs request operations on the same FBDIMM, the input signals are sent to a de-serializer, then to a DRAM interface logic circuitry that translates the input signals into control signals (LCTL) to memory chips. The data (LD1-LD8) signals returned from memory chips on the same module received by the DRAM interface are sent to a serializer. The serializer converts the data into proper format and sends the output data to pass-through and merging (P&M) circuits. The P&M logic circuits transfer outputs through north bound signal transfer lanes (NB1) that typically comprise 14 pairs of high speed differential signal transfer lines. Output signals from other FBDIMM modules from another north bound signal transfer lanes (NB2) are also latched and processed by the P&M circuits before sending to NB1. Those high speed signal transfer lanes (SB1, SB2, NB1, NB2) are synchronized by phase-locked loop (PLL) circuits. FIG. **2**(*b*) is a simplified block diagram emphasizing features related to key points of the present invention. Please refer to the data sheets of existing AMB products such as Intel 6400 or NEC P720901 for further details. Those existing AMB products are typically complex high cost integrated circuits (IC) comprise more than 600 interface signals.

[0014] To increase the capacity of an FBDIMM system, multiple FBDIMM modules (FM1-FM8) are connected in daisy-chained bus architecture as illustrated in FIG. **2**(*c*). The system input (SB1) is connected to the south bound signal transfer lanes (SB1) of the first module (FM1). The system output is connected to the north bound signal transfer lanes (NB1) of the first module (FM1). The inputs to the second module (FM2) are supported by south bound signal transfer lanes (SB2) that are provided by AMB1 in FM1. The outputs from the module (FM2) are supported by north bound signal transfer lanes (NB2) to AMB1 in FM1. The inputs to the third module (FM3) are supported by south bound signal transfer lanes (SB3) that are provided by AMB2 in FM2. The outputs from the module (FM3) are supported by north bound signal transfer lanes (NB3) to AMB2 in FM2. The inputs to the forth module (FM4) are supported by south bound signal transfer lanes (SB4) that are provided by AMB3 in FM3. The outputs from the module (FM4) are supported by north bound signal transfer lanes (NB4) to AMB3 in FM3. The inputs to the fifth module (FM5) are supported by south bound signal transfer lanes (SB5) that are provided by AMB4 in FM4. The outputs from the module (FM5) are supported by north bound signal transfer lanes (NB5) to AMB4 in FM4. The inputs to the sixth module (FM6) are supported by south bound signal transfer lanes (SB6) that are provided by AMB5 in FM5. The outputs from the module (FM6) are supported by north bound signal transfer lanes (NB6) to AMB5 in FM5. The inputs to the seventh module (FM7) are supported by south bound signal transfer lanes (SB7) that are provided by AMB6 in FM6. The outputs from the module (FM7) are supported by north bound signal transfer lanes (NB7) to AMB6 in FM6. The inputs to the eighth module (FM8) are supported by south bound signal transfer lanes (SB8) that are provided by AMB7 in FM7. The outputs from the module (FM8) are supported by north bound signal transfer lanes (NB8) to AMB7 in FM7. The capacity of the memory system in FIG. **2**(*c*) is the same as that of the memory system in FIG. **1**(*c*) while the loadings on all data and controls signals are about the same of a single module in FIG. **1**(*a*). In addition, the loading on all signals lines remain the same no matter how many FBDIMM modules are connected in the memory system, effectively solving the loading problems. However, the memory access latency is increase by the need to transfer signals serially through the AMBs connected in daisy chain architecture. For example, if we want to access the memory chips in the seventh module (FM7), we need to

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add 7 sound bound signal transfer cycles, 7 north bound signal transfer cycles, plus delays caused by AMB logic processing as the overhead in timing. The worst delay time increases linearly with the number of FBDIMM modules linked in the daisy chain, limiting the capability to increase capacity. In addition, the FBDIMM modules are by far more expensive than conventional memory modules, and they are not compatible with conventional memory interfaces, limiting their application on high cost server or work stations. FBDIMM saves power by isolating memory chips in different modules, but the power consumed by overhead in AMB is significant.

[0015] It is therefore highly desirable to provide other solutions that can increase total capacity of memory systems without the drawbacks of existing solutions such as FBDIMM approaches.

SUMMARY OF THE INVENTION

[0016] The primary objective of this invention is, therefore, to provide high capacity memory systems without increasing the loading of data signals. The other primary objective of this invention is to achieve the above objective with minimum overhead in performance and in cost. Another objective is to achieve the above objectives while using interfaces that are compatible with conventional memory systems. These and other objectives are achieved by using multiplexing to isolate loadings on data signals. The resulting memory systems are capable of achieving high capacity with basically the same performance and power of a single conventional memory. The interface signals also can be compatible with conventional memory systems.

[0017] While the novel features of the invention are set forth with particularly in the appended claims, the invention, both as to organization and content, will be better understood and appreciated, along with other objects and features thereof, from the following detailed description taken in conjunction with the drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIGS. **1**(*a-c*) are simplified schematic block diagrams for prior art conventional memory systems;

[0019] FIGS. **2**(*a-c*) are simplified schematic block diagrams for prior art FBDIMM systems;

[0020] FIG. **3**(*a*) is a simplified schematic block diagram for one example of the Multiplexed Memory Buffer (MMB) module of the present invention;

[0021] FIG. **3**(*b*) is a simplified symbolic diagram for the bidirectional multiplexer in FIG. **3**(*a*);

[0022] FIG. **3**(*c*) is a simplified schematic block diagram for one example of the MMB memory system of the present invention;

[0023] FIG. **4**(*a*) is a simplified schematic block diagram for one example of the Multiplexed Bus Memory Buffer (MBMB) module of the present invention;

[0024] FIG. **4**(*b*) is a simplified symbolic diagram for the bidirectional multiplexer in FIG. **4**(*a*); and

[0025] FIG. **4**(*c*) is a simplified schematic block diagram for MBMB one example of the memory system of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] FIG. **3**(*a*) is a simplified schematic block diagram for one example of the Multiplexed Memory Buffer (MMB) module of the present invention. In this example, the MMB memory module (MMB1) comprises 8 memory chips (M11, M21, M31, M41, M51, M61, M71, M81). Comparing to the prior art memory module in FIG. **1**(*a*), the key difference is that the memory chips (M11-M18) in the prior art memory module is arranged in parallel data connection to support a complete set of system data signals (DB1-DB8). In contrast, the memory chips (M11, M21, M31, M41, M51, M61, M71, M81) in memory modules of the present invention is arranged to support a sub set (DB1) of the system data signals, while the first memory chip (M11) supports DB1, the second memory chip (M21) supports DB1, . . . , and the eighth memory chip (M81) also supports DB1. In other words, all those memory chips (M11, M21, M31, M41, M51, M61, M71, M81) are arranged to support the same data signals (DB1). The functions of those memory chips are equivalent to the functions of the memory chips in one vertical column of the prior art memory system in FIG. **1**(*c*). Therefore, we call such architecture as "vertical data connection". We will call the memory chips (M11, M21, M31, M41, M51, M61, M71, M81) in a MMB module as an "MMB group". Under vertical data connection, at any given time no more than one of the memory chips in the MMB group is allowed to access the system data signal (DB1) under normal operation conditions, making it possible to isolate the loadings of different chips by multiplexing. As shown in FIG. **3**(*a*), the chip level data signals (D11, D21, D31, D41, D51, D61, D71, D81) are connected to the branch entries of bidirectional multiplexers (MUX8), while the system level data signals (DB1) are connected to the root entries of the bidirectional multiplexers (MUX8). FIG. **3**(*a*) uses the symbolic view of a multiplexer to represent a plurality of bi-directional multiplexers because we need one bi-directional multiplexer for each bit of system level data signal (DB1). An MMB select logic circuitry analyzes the system control signal (CTL) and calculates the select signals (SM) for the bidirectional multiplexers (MUX8). This MMB select logic circuitry also serves as buffers to provide chip level control signals (Mctl) to memory chips.

[0027] Since data signals of memory chips are typically bi-direction signals (with possible exceptions such as input data masks), the multiplexers (MUX8) in MMB modules actually need to have both multiplexing and de-multiplexing functions. We will call such circuitry as "bidirectional multiplexer" in our discussions. A person with ordinary skill in circuit design would be able to design bidirectional multiplexers in wide varieties of configurations. FIG. **3**(*b*) shows one of the simplest implementations of bidirectional multiplexers useful for applications of the present invention. For this example, the chip level data signals (D11, D21, D31, D41, D51, D61, D71, D81) are connected to the sources of MOS transistors (M1-M8), while the drains of those transistors are all connected to the same system level data signal (DB1). By controlling the gate signals (G1-G8) we can select chip level signals that are allowed to communicate with the system level signal, and isolate the loadings on unselected signals. There are many other ways to implement bidirectional multiplexers. A typical example is to use a pair of p-channel and n-channel pass gate transistors to control one entry. Combinational logic gates also can form equivalent circuitry. The scope of the present invention is not limited by particular implementations of the detailed circuit designs. A "bidirectional multiplexer" defined in the present invention is a circuitry that provides multiplexing as well as de-multiplex-

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ing functions for bidirectional signal communication: A "bidirectional multiplexer" has one "root entry" and a plurality of "branch entries". Using FIG. 3(*b*) as an example, the transistor sources connected to signals D11, D21, D31, D41, D51, D61, D71, D81 are "branch entries" while the transistor drains connected to signal DB1 is the "root entry" defined in this patent application. In our definition, bidirectional multiplexers used in the present invention must be able to isolate loadings on unselected data signals. "Isolate loadings from a signal" means significantly reduce the effective loading caused by the signal. During normal operation conditions, one or no branch entry of a bidirectional multiplexer is selected to communicate with the "root entry" while the loadings of unselected branch entries are isolated from the root entry. However "bidirectional multiplexer" used for the present invention allows exceptions. For example, we may want to simultaneously select multiple entries in special modes. For another example, during the time to switch from one entry to another entry, we may have both entries turned on for a short period of time. We also want to have the capability to turn off all branch entries. Therefore, unlike the strictly defined logic function of multiplexers, the bidirectional multiplexers used by the present invention does not always guaranteed to have only one selected entry at all time.

[0028] FIG. 3(*c*) is the simplified schematic block diagram for an MMB memory system that has the same capacity as the prior art memory system in FIG. 1(*c*). In this example, the memory system comprises 8 MMB modules (MMB1-MMB8). Each MMB module comprises 8 memory chips. Each MMB module is equipped with eight-entry bidirectional multiplexers. Each MMB module support one set of the system level data signals: MMB1 supports DB1, MMB2 supports DB2, MMB3 supports DB3, MMB4 supports DB4, MMB5 supports DB5, MMB6 supports DB6, MMB7 supports DB7, and MMB8 supports DB8. This MMB memory system has the same interface signals, the same capacity, and the same functions as the prior art system in FIG. 1(*c*); while the loading is equivalent to the loading of one prior art module in FIG. 1(*a*). Using such architecture is therefore able to support roughly 8 times more capacity than the architecture in FIG. 1(*c*).

[0029] It is well known that a properly controlled bidirectional multiplexer is able to isolate the loadings on unselected branches. The bidirectional multiplexer itself introduces additional loading, but such loading can be designed to be insignificant relative to overall loading. The bidirectional multiplexer also introduced additional delay, but such additional delay can be designed to be insignificant relative to overall delay. The selection logic signal (SM) of the bidirectional multiplexer (MUX8) is determined from system level control signals (CTL) by the MMB Select logic circuitry. The MMB Select logic circuitry can isolate the loading seen by the system level control signals (CTL), but it also introduces additional delays. However, the buffer delay can be designed to be insignificant. In many cases, we may not need to buffer the control signals. The logic function of the MMB Select logic circuitry is similar to DRAM data bus control logic circuits that are well known to the industry. An MMB is certainly by far less complex than a prior art AMB. Upon disclosure of the present invention, a person with ordinary skill in the art will certainly be able to design the MMB in wide varieties of ways so that there is no need to discuss in further details.

[0030] The MMB memory systems have many advantages comparing to prior art systems. It has identical functions and identical interface signals (DB1-DB8, CTL) as the prior art system in FIG. 1(*c*). MMB systems can be fully compatible with existing systems with no or minimal modifications. While the loadings on the data and control signals are equivalent to the loadings of a single module in FIG. 1(*a*) plus small overhead added by the MMB circuits, the MMB overhead typically can be designed to be insignificant relative to the system loading. Using MMB architectures, it is very common to be able to increase system capacity by 4 to 16 times or more. The timing overhead is typically much less than that of FBDIMM systems. The MMB systems are by far more cost efficient than prior art AMB systems. The power consumed by MMB systems is by far less than prior art systems with equivalent capacities.

[0031] While specific embodiments of the invention have been illustrated and described herein, it is realized that other modifications and changes will occur to those skilled in the art. Upon disclosure of the present invention, those skilled in the art will be able to develop wide varieties of circuits to implement the elements of the present invention. For example, there are many ways in designing the bidirectional multiplexer and supporting selection logic circuits. For another example, the chip select signals connected to memory chips in the same MMB group can be defined in many different ways. If each memory chip in the same MMB group has separated chip select signal, then the function of an MMB system is equivalent to the function of many conventional modules. If all the memory chips in the same MMB group are connected to the same chip select signal, then the function of a MMB group is equivalent to a memory chip of the combined capacity of all memory chips in the group. We certainly can use combinations of the above two chip selection methods. For another example, we can modify the data signal connection methods to define a variation of the MMB architecture called "Multiplexed Bus Memory Buffer" (MBMB) architecture as illustrated by FIGS. 4(*a-c*).

[0032] For the MMB example in FIG. 3(*a*), each entry of a bidirectional multiplexer is connected to a single memory chip. For MBMB modules, each entry of a bidirectional multiplexer can be shared by multiple memory chips. The MBMB example in FIG. 4(*a*) illustrates the option when each entry of a multiplexer is shared by two memory chips. Memory chips M11 and M21 are sharing the same data signals (D121) in a bus structure, memory chips M31 and M41 are sharing another set of data signals (D341) in a bus structure, Memory chips M51 and M61 are sharing the same data signals (D561) in a bus structure, while memory chips M71 and M81 are sharing another set of data signals (D781) in a bus structure. Using such configuration, we only need 4-entry bidirectional multiplexers (MUX4) instead of 8-entry bidirectional multiplexers. FIG. 4(*b*) shows one of the simplest implementation of bidirectional multiplexer useful for applications of the present invention. For this example, the shared data entries (D121, D341, D561, D781) are connected to the sources of MOS transistors (M12, M34, M56, M78), while the drains of those transistors are all connected to the same system level data signal (DB1). By controlling the gate signals (G12, G34, G56, G78) we can select chip level signals that are allowed to communicate with the system level signal, and isolate the loadings on unselected signals.

[0033] FIG. 4(*c*) is the simplified schematic block diagram for an MBMB memory system that has the same capacity as

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the prior art memory system in FIG. 1(*c*). In this example, the memory system comprises 8 MBMB modules (MBMB1-MBMB8). Each MBMB module comprises 8 memory chips. Each MBMB is equipped with four-entry bidirectional multiplexers to select one set of data signals from one of the eight memory chips in the same MBMB module (with the helps of chip select signals that are not shown separately), while every pair of memory chips share one entry of the MBMB bidirectional multiplexer. The MBMB system in FIG. 4(*c*) can serve the same function as the prior art system in FIG. 1(*c*) as well as the MMB system in FIG. 3(*c*). The signal loadings of the MBMB system are equivalent to that of two memory modules in FIG. 1(*b*), which is higher than the loading of the MMB system in FIG. 3(*a*). In the mean time, MBMB modules are more cost efficient than MMB modules due to less entries in bidirectional multiplexers and lower pin counts in MMB chips. The optimum selection is determined by system requirements.

[0034] While specific embodiments of the invention have been illustrated and described herein, it is realized that other modifications and changes will occur to those skilled in the art. For example, each entry of MBMB multiplexer certainly can support more than 2 memory chips by trading higher loading to achieve lower costs. Different number of memory chips can be connected to different entries of multiplexers. The number of branch entries of each bidirectional multiplexer can be any number larger or equal to 2, not limited to 4 or 8 entries. We certainly can connect more modules to the MMB or MBMB systems. It is also possible to link MMB or MBMB modules with FBDIMM architectures to achieve very large capacity.

[0035] The present invention is a board level architecture developed to increase the total capacity of memory systems while isolating the loading of data signals by multiplexing. Comparing to prior art memory modules, the loadings of an MMB system of the present invention are equivalent to a prior art SIMM module. The variation of MMB system called MBMB system allows multiple memory chips to share the same entry of a bidirectional multiplexer in a bused connection. When each entry of a bidirectional multiplexer is shared by two memory chips, the equivalent loadings are about the same as a prior art DIMM module. Using MMB or MBMB architectures, we can achieve memory capacity much higher than prior art memory systems without significant degradation in system performance. The memory systems of the present invention can be fully compatible with prior art memory systems. The costs of MMB or MBMB systems are by far lower than the cost of prior art FBDIMM systems.

[0036] Prior art memory systems typically fit one memory module into one printed circuit board. That is not necessary the case for memory modules of the present invention. We often fit multiple modules into a single printed circuit board. It is even possible to fit the whole memory system into a single printed circuit board. The memory systems of the present invention can have identical system level interface as prior art systems. It is therefore possible to design printed circuit boards of the present invention that can use existing DIMM sockets with no or minimal modifications. The printed circuit boards of the present invention sometimes do not use all the interface signals on a conventional DIMM socket, and sometimes we may need more signals such as chip select signals and clock enable signals in other sockets. We may need to use additional board level connectors or small modifications in board interface to design circuit boards of the present invention that fit into prior art DIMM sockets.

[0037] A "memory system" is defined as board level circuits supporting memory operations. A "memory module" is defined as separable sub circuits of a memory system. A "system level signal" is defined as an electrical signal used to communicate with circuits external to a memory system. A "chip level signal" is defined as an electrical signal used to communicate with memory chips. The "Loading" on a signal is the non-ideal factors that can slow down performances such as leakage currents, parasitic capacitances, inductances, or resistances. A "bidirectional multiplexer" defined in the present invention is a circuitry that provides multiplexing as well as de-multiplexing functions for bidirectional signal communication; A "bidirectional multiplexer" has one "root entry" and a plurality of "branch entries"; During normal operation conditions, one or no branch entry of a bidirectional multiplexer is selected to communicate with the "root entry" while the loadings of unselected branch entries are isolated from the root entry; However "bidirectional multiplexer" allows exceptions, such as transitional operations or special mode operations, to have conditions when multiple branch entries are selected simultaneously. "Isolate loadings from a signal" means significantly reduce the effective loading caused by the signal. An "IC chip" is defined as packed integrated circuit or integrated circuit bare die that is ready to be placed on printed circuit board. A "memory chip" is defined as packaged IC memories or bare die memory integrated circuit that is ready to be placed on printed circuit board.

[0038] While specific embodiments of the invention have been illustrated and described herein, it is realized that other modifications and changes will occur to those skilled in the art. It is therefore to be understood that the appended claims are intended to cover all modifications and changes as fall within the true spirit and scope of the invention.

What is claimed is:

1. A memory system or a memory module comprising:

A plurality of integrated circuit memory chips placed on printed circuit boards;

System level data signals for data communication to circuits external to said memory system or memory module;

Chip level data signals for data communication to said memory chips;

Integrated circuit chip(s) comprising a plurality of bidirectional multiplexers;

Wherein a plurality of system level data signals are connected to the root entries of said bidirectional multiplexers, while the chip level data signals supporting said system level data signals are connected to the branch entries of said bidirectional multiplexers for selective isolation of loadings.

2. The memory chips in claim **1** are dynamic random access memory chips.

3. The dynamic random access memory chips in claim **2** are synchronized dynamic random access memory integrated circuit with data transfer rate higher than 600 million bits per second per signal.

4. The dynamic random access memory chips in claim **2** supports double data rate operations.

5. The memory system in claim **1** is compatible with JEDEC standard DIMM interface with no or minimal modifications.

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6. The memory system in claim 1 is compatible with JEDEC standard SIMM interface with no or minimal modifications.

7. One branch entry of the bidirectional multiplexers in claim 1 is connected to one data signal of one memory chip.

8. One branch entry of the bidirectional multiplexers in claim 1 is shared by data signals from multiple memory chips.

9. A method to manufacture a memory system or a memory module comprising the steps of:

Placing a plurality of integrated circuit memory chips on printed circuit board(s);

Providing system level data signals for data communication to circuits external to said memory system or memory module;

Providing chip level data signals for data communication to said memory chips;

Providing integrated circuit chip(s) comprising a plurality of bidirectional multiplexers;

Wherein a plurality of system level data signals are connected to the root entries of said bidirectional multiplexers, while the chip level data signals supporting said system level data signals are connected to the branch entries of said bidirectional multiplexers for selective isolation of loadings.

10. The method in claim 9 comprising the step of placing a plurality of memory chips on printed circuit board(s) using dynamic random access memory chips.

11. The method in claim 10 comprising the step of placing a plurality of dynamic random access memory chips on printed circuit board(s) using synchronized dynamic random access memory with data transfer rate higher than 600 million bits per second per signal.

12. The method in claim 9 comprising the step of placing a plurality of dynamic random access memory chips on printed circuit board(s) using dynamic random access memory chips that supports double data rate operations.

13. The method in claim 9 provides a memory system that is compatible with JEDEC standard DIMM interface with no or minimal modifications.

14. The method in claim 9 provides a memory system that is compatible with JEDEC standard SIMM interface with no or minimal modifications.

15. The method in claim 9 comprises the step of connecting one data signal of one memory chip to one branch entry of the bidirectional multiplexers in claim 9.

16. The method in claim 9 comprises the step of connecting data signals from multiple memory chips to share one branch entry of the bidirectional multiplexers in claim 9.

* * * * *

BNSDOCID: <US____20090103387A1_I_>

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, CA 92614
ETATS-UNIS D'AMERIQUE

PCT

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

(PCT Rule 66)

Date of mailing *(day/month/year)*	24.10.2011
Applicant's or agent's file reference: NETL.048VPC	**REPLY DUE** within 1 month(s) from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/040826	01.07.2010	16.07.2009

International Patent Classification (IPC) or both national classification and IPC
INV. G11C5/02

Applicant
Netlist, Inc.

1. ☒ The written opinion established by the International Searching Authority:
   ☒ is ☐ is not
   considered to be a written opinion of the International Preliminary Examining Authority.

2. This second opinion contains indications relating to the following items:
   - ☒ Box No. I Basis of the opinion
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☒ Box No. V Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☒ Box No. VII Certain defects in the international application
   - ☒ Box No. VIII Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

   When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(e).
   How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 55.3 and 66.8.
   Also: For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4*bis*. For an informal communication with the examiner, see Rule 66.6. For an additional opportunity to submit amendments, see Rule 66.4.
   If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary report on patentability (Chapter II of the PCT) must be established according to Rule 69.2 is: 16.11.2011

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	Trifonov, Antoniy Telephone No. +49 89 2399-7168

Form PCT/IPEA/408 (Cover Sheet) (July 2011)

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OCT 28 2011

KNOBBE, MARTENS,
OLSON & BEAR,LLP

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

International application No.
PCT/US2010/040826

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3(a) and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4(a))
   - ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a) and (b))

2. With regard to the elements of the international application, this opinion has been established on the basis of *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed")*:

Description, Pages

1-26 as originally filed

Claims, Numbers

1-55 filed with telefax on 14-05-2011

Drawings, Sheets

1-13 filed with the letter of 19-08-2010

☐ a sequence listing - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:

4. ☐ This opinion has been established as if (some of) the amendments listed below had not been made, since either they are considered to go beyond the disclosure as filed, or they were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in the Supplemental Box (Rules 70.2(c) and (c-bis)):
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:

5. ☐ This opinion has been established:
   - ☐ taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 66.1(d-bis)).
   - ☐ without taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 66.4bis).

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6. ☐ Supplementary international search report(s) from Authority(ies) have been received and taken into account in drawing up this opinion (Rule 45bis.8(b) and (c)).

Box No. V Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-5, 10-17, 19-26, 29-33, 35-38, 43, 46-51, 55
Inventive step (IS)	Claims	1-5, 10-17, 19-27, 29-33, 35-38, 43, 45-51, 55
Industrial applicability (IA)	Claims	

2. Citations and explanations:

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

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Re Item V.

1 Reference is made to the following documents:

D1 US 2006/262586 A1 (SOLOMON JEFFREY C [US] ET AL) 23 November 2006 (2006-11-23)

D2 US 2008/162790 A1 (IM JEON-TAEK [KR]) 3 July 2008 (2008-07-03)

D3 US 2009/103387 A1 (SHAU JENG-JYE [US]) 23 April 2009 (2009-04-23)

2 The term "merge" or "merging", as used in a plurality of claims in the present application, is not clear (Article 6 PCT).

3 The present application does not meet the criteria of Article 33(1) PCT, for the following reasons:

3.1 Document D2 discloses (see Figs. 11, 12) a memory module comprising:
- at least one printed circuit board (510, 520, 530, 540);

- a plurality of memory devices (511a) mechanically coupled to the at least one printed circuit board;

- a control circuit (516a,516b) mechanically coupled to the at least one printed circuit board, the control circuit configurable to receive control signals from a system memory controller (550) and to transmit module control signals to the plurality of memory devices (see Fig. 12); and

- a plurality of data transmission circuits (fast enable transfer switches 515) mechanically coupled to the at least one printed circuit board and distributed at corresponding positions relative to the at least one printed circuit board, the plurality of data transmission circuits configurable to be operatively coupled to the system memory controller (through the interface 516) and configurable to receive module control signals from the control circuit (DQS and SQ signals, see par. [0072]),

wherein at least one first data transmission circuit of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices (see Fig. 12, wherein one first circuit 515 is coupled to at least two memory devices, 511a and 511b), at least one second data transmission circuit (one second circuit 515) of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices.

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The plurality of data transmission circuits are obviously configured to response to the module control signals, since they have multiplexing and latching functionalities, e.g. the fast enable transfer switches (FET switches) are controlled by the control circuit to store/latch and multiplex data from/to at least two memory devices. The FETs are therefore responsible for inhibition/ driving of data to/from the memory devices (i.e. the FETs are coupled to the read/write paths of the memory devices).

The independent claims 1, 21, 37 are therefore not new in the sense of Article 33(2) PCT.

3.2 Independent method claims 31 and 48 contain each, respectively defined in method terms, the technical features of at least one of the independent apparatus claims 1, 21, 37 and additionally the following definitions:
- the data transmission circuits comprising a byte-wise data buffer; and
- the data transmission circuits being load reducing switching circuits.
Since the additional definitions are directly disclosed in D2 (see par. [0072]), the subject-matter of claims 31 and 48 is not new compared to the prior art of D2.

4 The technical features of dependent claims 2-5, 10 can be directly found in D2 (see par. [0072 and Figs. 11,12]).

5 The alignment of the data transmission circuits, the connector and the memory devices in D2 is shown on Figs. 10 and 11 and is done in accordance with the requirements of claims 11-17 in the present application.

6 The technical features of claims 19, 20, 22-26, 29, 30, 35, 36, 38, 43, 46, 47, 49-51, 55 can be directly found in D2, see par. [0072].

7 Since the FET switches in D2 switch data to/from at least two memory devices, these are considered as driven by the controller circuit in accordance with the currently running operation, as required by dependent claims 32 and 33.

8 The data transmission circuits and the memory devices in D2 are not specified as having different bit widths as required by claims 6-9 in the present application.

9 A tristate buffer, as defined in claims 18, 28, 34, 54, is not disclosed in the prior art of D2.

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10 The memory module in D2 does not comprise DRAM memory devices, as required in claims 27, 45 in the present application.

11 The technical features of dependent claims 39-42,44, 52, 53 are not disclosed in D2.

Re Item VII.

12 The independent claims are not in the two-part form in accordance with Rule 6.3(b) PCT.

13 Reference signs are not inserted in parentheses in the claims in accordance with Rule 6.2(b) PCT.

14 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in documents D1 - D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII.

15 The various definitions of the invention given in the independent claims are such that the claims as a whole are not concise so that the requirements of Article 6 PCT are not met.

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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To:
Christensen, Michael R.
KNOBBE, MARTENS, OLSON & BEAR LLP
2040 Main Street, 14th Floor
Irvine, CA 92614
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*	30 January 2013 (30-01-2013)
Applicant's or agent's file reference NETL071WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2011/059209	International filing date *(day/month/year)* 3 November 2011 (03-11-2011)
Applicant NETLIST, INC.	

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	PITARD, Jacqueline Tel: +49 (0)89 2399-2562

Form PCT/ISA/220 (July 2010)

Received Orange County Docketing

FEB 05 2013

Knobbe Martens Olson & Bear LLP

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
NETL071WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/059209	03/11/2011	03/11/2010
Applicant		
NETLIST, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 6 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [X] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title**,
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 2
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

Samsung Electronics Co., Ltd.
Ex. 1010, p. 880

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/059209

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/059209

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C5/06 G11C7/10 G11C7/18
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/025137 A1 (RAJAN SURESH NATARAJAN [US] ET AL) 31 January 2008 (2008-01-31) paragraph [0051]; figures 2b,2c	1-28
A	US 2006/233012 A1 (SEKIGUCHI TOMONORI [JP] ET AL) 19 October 2006 (2006-10-19) paragraph [0138]; figure 16	1-28
X	EP 1 816 570 A2 (RAMBUS INC [US]) 8 August 2007 (2007-08-08) paragraph [0019] - paragraph [0022]; figures 2,3 paragraph [0109] - paragraph [0112]; figure 15	29-34

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2013	30/01/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lindquist, Jim

4

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/059209

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008025137 A1	31-01-2008	US 2008025137 A1	31-01-2008
		US 2009285031 A1	19-11-2009
US 2006233012 A1	19-10-2006	CN 1841551 A	04-10-2006
		JP 4309368 B2	05-08-2009
		JP 2006277870 A	12-10-2006
		US 2006233012 A1	19-10-2006
EP 1816570 A2	08-08-2007	DE 1022642 T1	11-01-2001
		DE 00100018 T1	29-12-2005
		DE 02000378 T1	29-12-2005
		DE 06125946 T1	22-11-2007
		DE 06125954 T1	22-11-2007
		DE 06125958 T1	22-11-2007
		DE 69132121 D1	25-05-2000
		DE 69132121 T2	21-09-2000
		DE 69132501 D1	08-02-2001
		DE 69132501 T2	23-08-2001
		DE 69132721 D1	11-10-2001
		DE 69132721 T2	29-05-2002
		DE 69133500 T2	27-07-2006
		DE 69133550 T2	11-01-2007
		DE 69133565 T2	05-07-2007
		DE 69133572 T2	14-02-2008
		EP 0525068 A1	03-02-1993
		EP 1022642 A1	26-07-2000
		EP 1197830 A2	17-04-2002
		EP 1640847 A2	29-03-2006
		EP 1816569 A2	08-08-2007
		EP 1816570 A2	08-08-2007
		EP 1830241 A1	05-09-2007
		IL 96808 A	31-03-1996
		JP 3404383 B2	06-05-2003
		JP 3414393 B2	09-06-2003
		JP 3550143 B2	04-08-2004
		JP H05507374 A	21-10-1993
		JP 2001273765 A	05-10-2001
		JP 2003203008 A	18-07-2003
		US 5319755 A	07-06-1994
		US 5408129 A	18-04-1995
		US 5473575 A	05-12-1995
		US 5499385 A	12-03-1996
		US 5513327 A	30-04-1996
		US 5606717 A	25-02-1997
		US 5638334 A	10-06-1997
		US 5657481 A	12-08-1997
		US 5809263 A	15-09-1998
		US 5841580 A	24-11-1998
		US 5841715 A	24-11-1998
		US 5915105 A	22-06-1999
		US 5928343 A	27-07-1999
		US 5954804 A	21-09-1999
		US 5983320 A	09-11-1999
		US 6032214 A	29-02-2000
		US 6032215 A	29-02-2000
		US 6034918 A	07-03-2000
		US 6035365 A	07-03-2000
		US 6038195 A	14-03-2000

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Ex. 1010, p. 883

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/059209

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 6044426 A	28-03-2000
		US 6049846 A	11-04-2000
		US 6067592 A	23-05-2000
		US 6070222 A	30-05-2000
		US 6085284 A	04-07-2000
		US 6101152 A	08-08-2000
		US 6128696 A	03-10-2000
		US 6182184 B1	30-01-2001
		US 6185644 B1	06-02-2001
		US 6260097 B1	10-07-2001
		US 6266285 B1	24-07-2001
		US 6304937 B1	16-10-2001
		US 6314051 B1	06-11-2001
		US 6415339 B1	02-07-2002
		US 6598171 B1	22-07-2003
		US 2001030904 A1	18-10-2001
		US 2002001253 A1	03-01-2002
		US 2002004867 A1	10-01-2002
		US 2002015351 A1	07-02-2002
		US 2002016876 A1	07-02-2002
		US 2002046314 A1	18-04-2002
		US 2002091890 A1	11-07-2002
		US 2002141281 A1	03-10-2002
		US 2004114454 A1	17-06-2004
		US 2005030802 A1	10-02-2005
		US 2005033903 A1	10-02-2005
		US 2005141332 A1	30-06-2005
		WO 9116680 A1	31-10-1991

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-28

   To arrange die die interconnects (e.g. data paths) to interconnect the control die to a plurality of array dies, to minimize loads.

   ---

2. claims: 29-34

   Modes to operate the data path control circuit, to either transport data bits or command/address information, thus maximizing the use of the data path.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/059209	03.11.2011	03.11.2010

International Patent Classification (IPC) or both national classification and IPC
INV. G11C5/06 G11C7/10 G11C7/18

Applicant
NETLIST, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Lindquist, Jim Telephone No. +49 89 2399-2727

Form PCT/ISA/237 (Cover Sheet) (July 2009)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/059209

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Samsung Electronics Co., Ltd.
Ex. 1010, p. 887

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has, within the applicable time limit:

   ☒ paid additional fees

   ☐ paid additional fees under protest and, where applicable, the protest fee

   ☐ paid additional fees under protest but the applicable protest fee was not paid

   ☐ not paid additional fees

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☐ all parts.

   ☒ the parts relating to claims Nos. 1-34

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1-34
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-34
Industrial applicability (IA)	Yes:	Claims	1-34
	No:	Claims	

2. Citations and explanations

   see separate sheet

Samsung Electronics Co., Ltd.
Ex. 1010, p. 888

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

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Ex. 1010, p. 889

V. Citations and Explanations

1 The following documents are cited in this Written Opinion:

D1 US 2008/025137 A1 (RAJAN SURESH NATARAJAN [US] ET AL) 31 January 2008 (2008-01-31)

D2 EP 1 816 570 A2 (RAMBUS INC [US]) 8 August 2007 (2007-08-08)

2 The subject matter of claim 1 lacks novelty so that the criteria of Articles 33(1) and (2) PCT are not met.

In comparison to claim 1, D1 (fig.2B, para.0051) discloses a memory package, comprising:

a plurality of array dies (206A-D) having data ports;

at least a first die interconnect (Data) and a second die interconnect (Data), the first die interconnect (Data) in electrical communication with at least one data port of a first array die (206A) of the plurality of array dies and at least one data port of a second array die (206C) of the plurality of array dies and not in electrical communication with the data ports of at least a third array die (206B,206D) of the plurality of array dies, the second die interconnect (Data) in electrical communication with at least one data port of the third array die (206B) and not in electrical communication with the data ports of the first array die (206A) and the data ports of the second array die (206C); and

a control die (202) comprising at least a first data conduit (right Data connection to 202) configured to transmit a data signal to the first die interconnect (right Data) and to not transmit the data signal to the second die interconnect (left Data), and at least a second data conduit (left Data connection to 202) configured to transmit the data signal to the second die interconnect (left Data) and to not transmit the data signal to the first die interconnect (right Data).

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3 Independent claims 11 and 20 contains substantially the same features as claim 1 only differently worded. The subject-matter of these claims therefore lacks novelty for the same reasons as those set out here above.

4 The subject-matter of claim 29 lacks novelty so that Articles 33(1) and (2) PCT are not met.

In comparison to claim 29, D2 (para.0109-0112, fig.2,3,15) discloses a memory module comprising:

a register device (19) configured to receive command/address signals (20) from a memory control hub (19) and to generate data path control signals (18); and

a plurality of DRAM packages (15,16,17), each DRAM package comprising:

a control die (para.0111, in part. p.16,l.53) comprising a plurality of command/address buffers and a data path control circuit configured to control command/address time slots and data bus time slots (para.0020), the control die configured to receive data signals from the register device, and command/address signals from the register device (para.0021); and

a plurality of DDR DRAM dies (150-157, para.0109) operatively coupled to the control die to receive the data signals from the control die,

wherein the memory module is selectively configurable into at least two operational modes comprising:

a first operational mode (para.0111) in which the register device generates the data path control signals, and the control die uses the data path control signals to operate the data path control circuit (para.0111); and

a second operational mode (0020) in which the control die operate the data path control circuit to provide the command/address signals to the plurality of DDR DRAM dies without decoding the command/address signals (para.0111).

5 The features of the dependent claims are either known from D1 or D2, or derivable therefrom in an obvious manner.

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Ex. 1010, p. 891

VII. Certain Defects

5.1 The independent claims are not drafted in two-part form delimited against D1, contrary to Rule 6.3.(b) PCT.

5.2 Reference signs are not inserted in the claims contrary to Rule 6.2.(b) PCT.

5.3 Contrary to the requirements of Rule 5.1(a)(ii) PCT, documents D1 and D2 are not identified in the description and the relevant background art disclosed therein is not discussed.

5.4 With regard to the phrase "hereby incorporated by reference" throughout the description, according to Rule 4.14 PCT, if there is a wish to treat the international application as a continuation-in-part of another application, this application must be indicated in the PCT request of the international application.

5.5 The description also contains references to documents not retrievable by the public, e.g. application numbers. These references must either be replaced by retrievable references or they must be removed.

5.6 And finally, the reference to the spirit of the present invention in page 37 is not allowed, since it wrongly makes the impression that the extent of protection is expanded beyond the contents of the claims (see Chapter III, 4.3a of the PCT Preliminary Examination Guidelines).

VIII. Certain Observations

6 The set of claims contains too many independent claims. The various definitions of the invention given in the independent claims 1, 11, 20 and 29 are such that the claims as a whole are not clear and concise, contrary to Article 6 PCT, since it is not clear for which matter protection is sought. To meet the criteria of this article the claims may only include one independent claim in each category, with dependent claims as appropriate (Rule 6.4(a)-(c) PCT).

7 Dependent claims 30-32 are not clear, because the meaning of the term "rank multiplication" is not clear. This term must be clarified to make any positive contribution to the patentability of the previous subject-matter.

Samsung Electronics Co., Ltd.
Ex. 1010, p. 892

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/ WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

US 20080025137A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2008/0025137 A1**

Rajan et al. (43) **Pub. Date: Jan. 31, 2008**

(54) **SYSTEM AND METHOD FOR SIMULATING AN ASPECT OF A MEMORY CIRCUIT**

(75) Inventors: **Suresh Natarajan Rajan**, San Jose, CA (US); **Keith R. Schakel**, San Jose, CA (US); **Michael John Sebastian Smith**, Palo Alto, CA (US); **David T. Wang**, San Jose, CA (US); **Frederick Daniel Weber**, San Jose, CA (US)

Correspondence Address:
ZILKA-KOTAB, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

(73) Assignee: **METARAM, INC.**

(21) Appl. No.: **11/461,427**

(22) Filed: **Jul. 31, 2006**

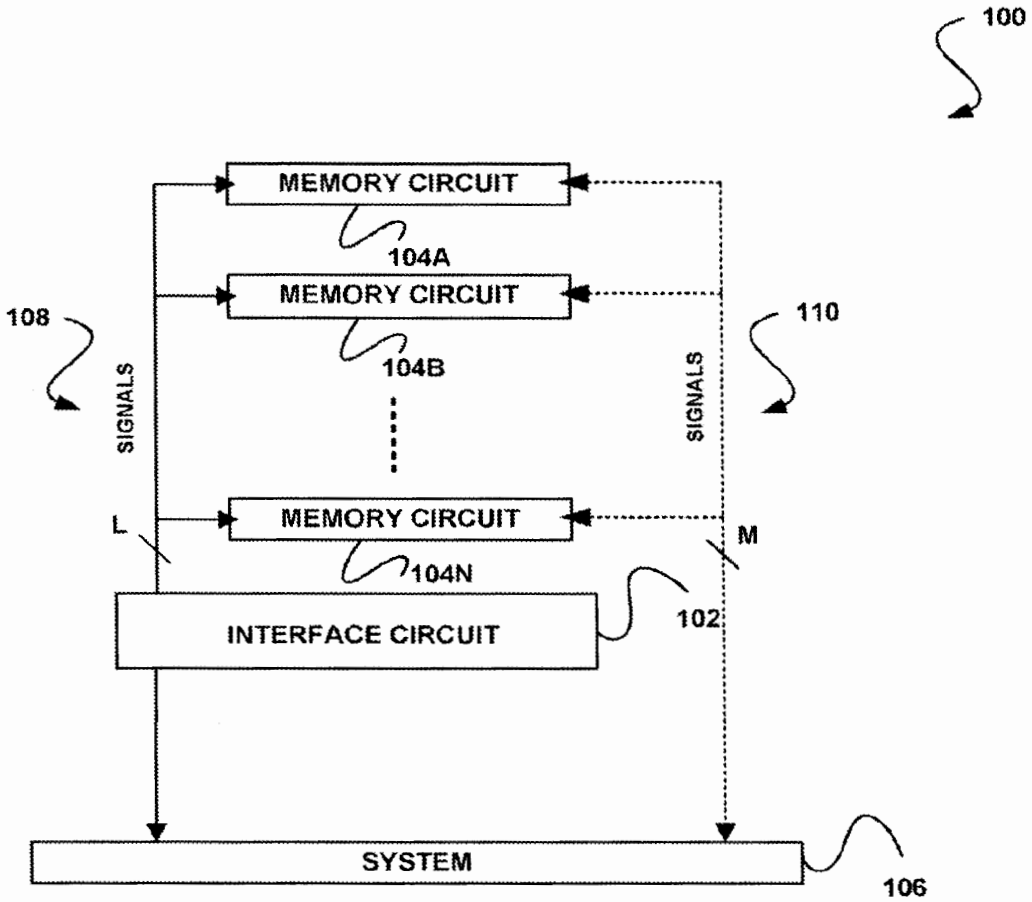
Publication Classification

(51) **Int. Cl.**
G11C 8/00 (2006.01)

(52) **U.S. Cl.** **365/239**

(57) **ABSTRACT**

A system and method are provided for simulating an aspect of a memory circuit. Included is an interface circuit that is in communication with a plurality of memory circuits and a system. Such interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of memory circuits. In accordance with various embodiments, such aspect may include a signal, a capacity, a timing, and/or a logical interface.



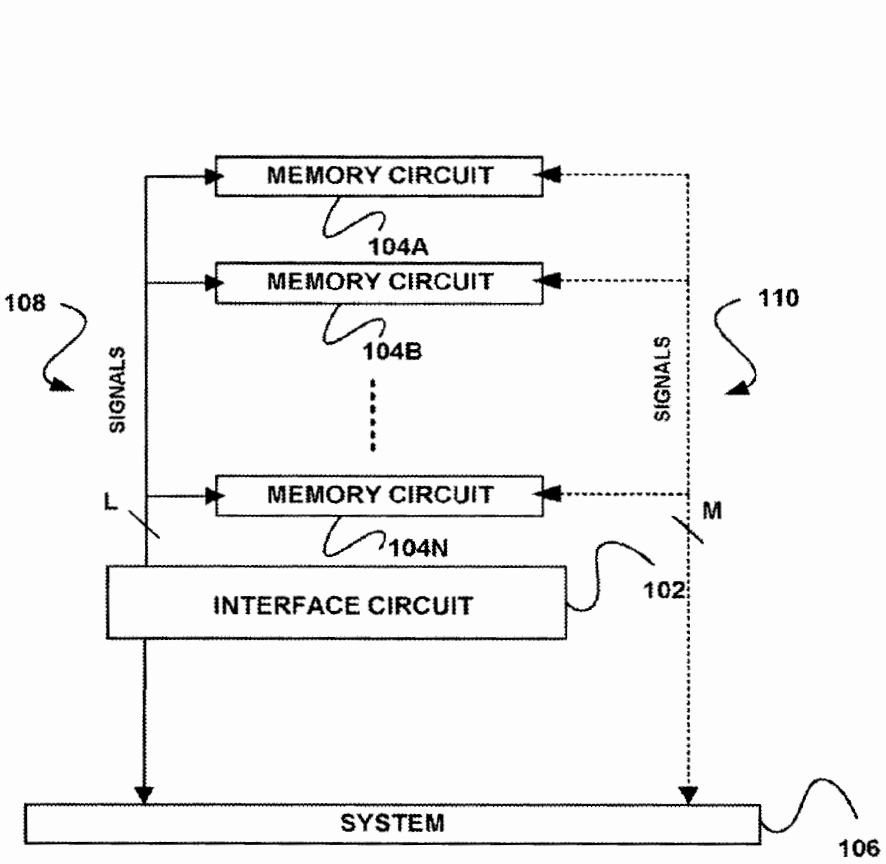

100
MEMORY CIRCUIT
104A
MEMORY CIRCUIT
108
SIGNALS
104B
110
SIGNALS
MEMORY CIRCUIT
L
M
104N
INTERFACE CIRCUIT
102
SYSTEM
106

FIGURE 1

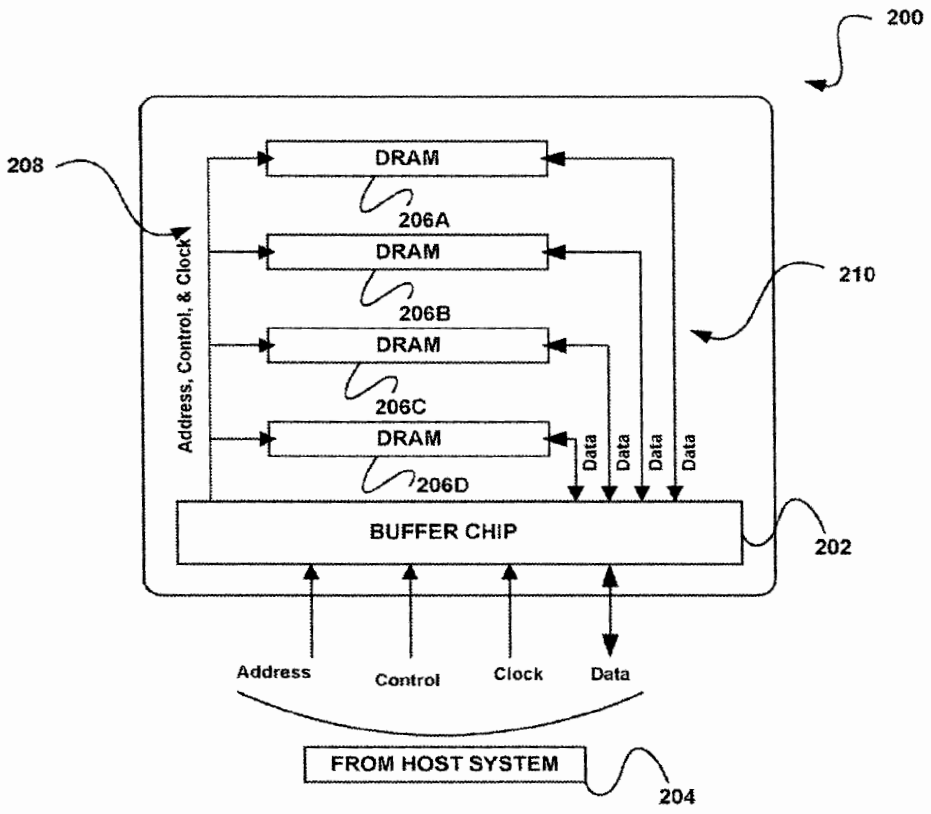


FIGURE 2A

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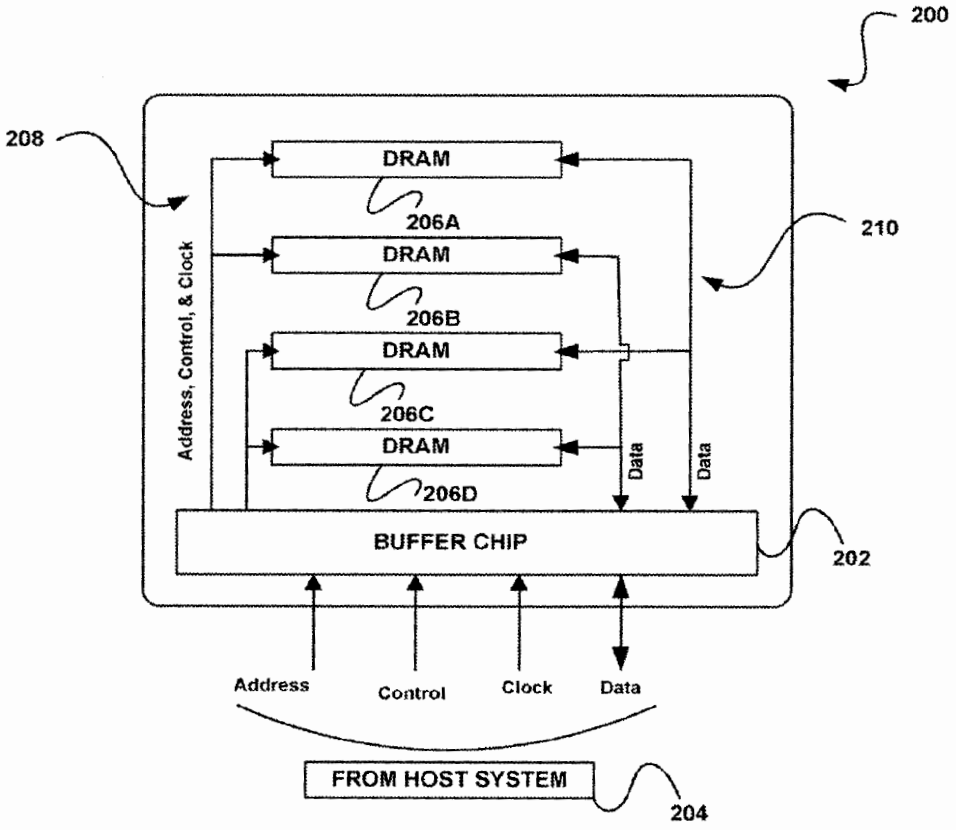
200
208
DRAM
206A
DRAM
206B
DRAM
206C
DRAM
206D
210
Address, Control, & Clock
Data
Data
BUFFER CHIP
202
Address
Control
Clock
Data
FROM HOST SYSTEM
204

FIGURE 2B

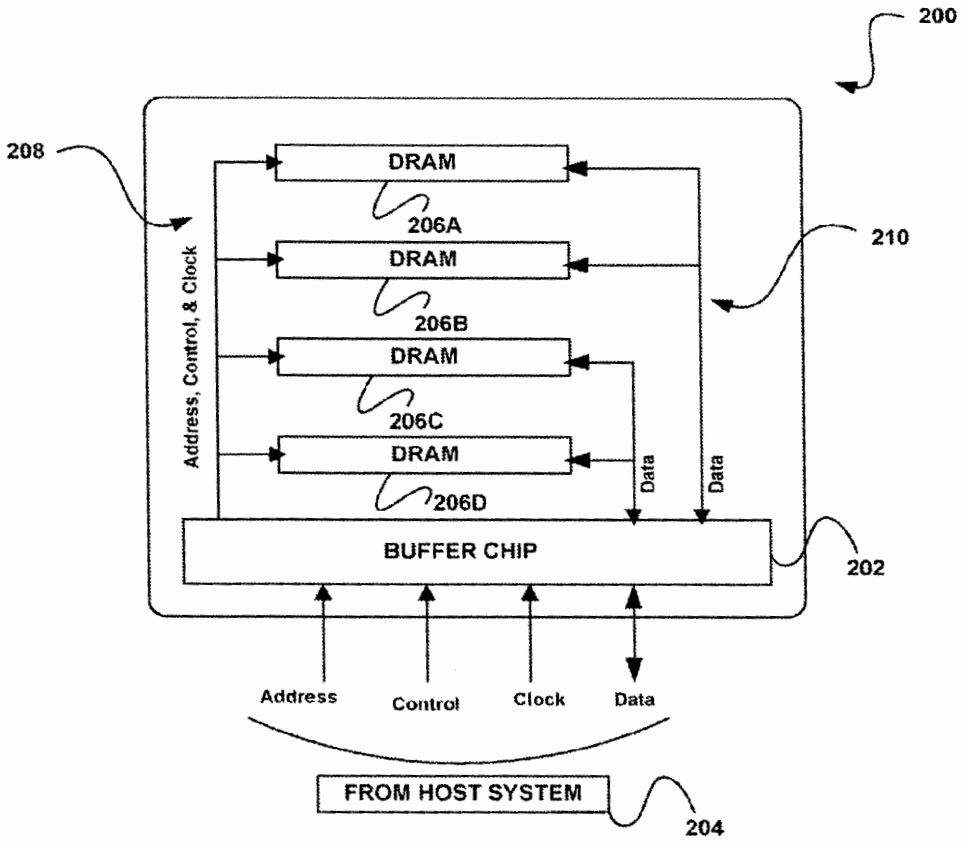

FIGURE 2C

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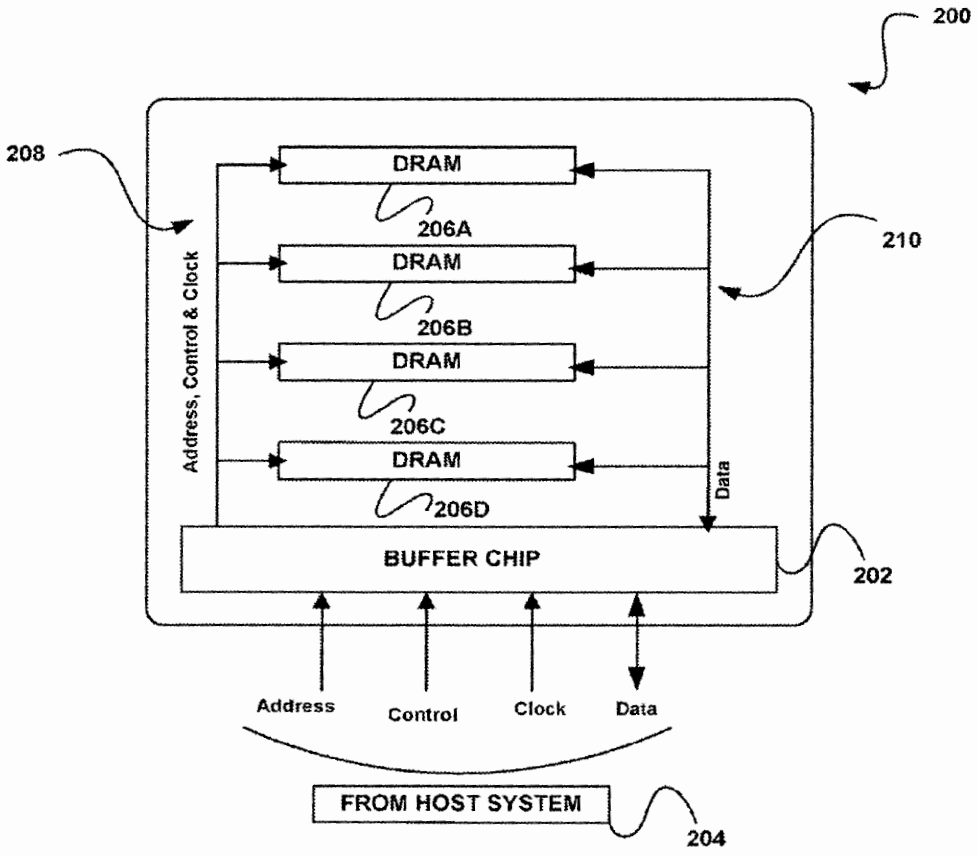
200
208
DRAM
206A
DRAM
206B
DRAM
206C
DRAM
206D
210
Address, Control & Clock
Data
BUFFER CHIP
202
Address
Control
Clock
Data
FROM HOST SYSTEM
204

FIGURE 2D

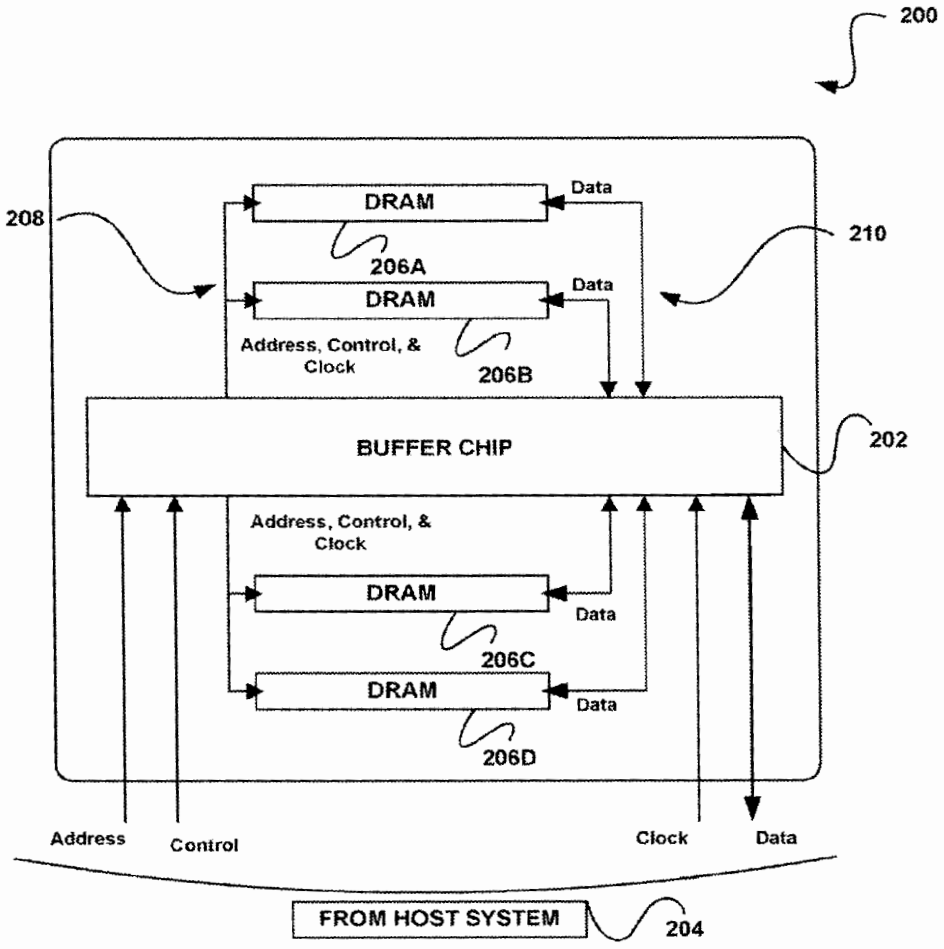

FIGURE 2E

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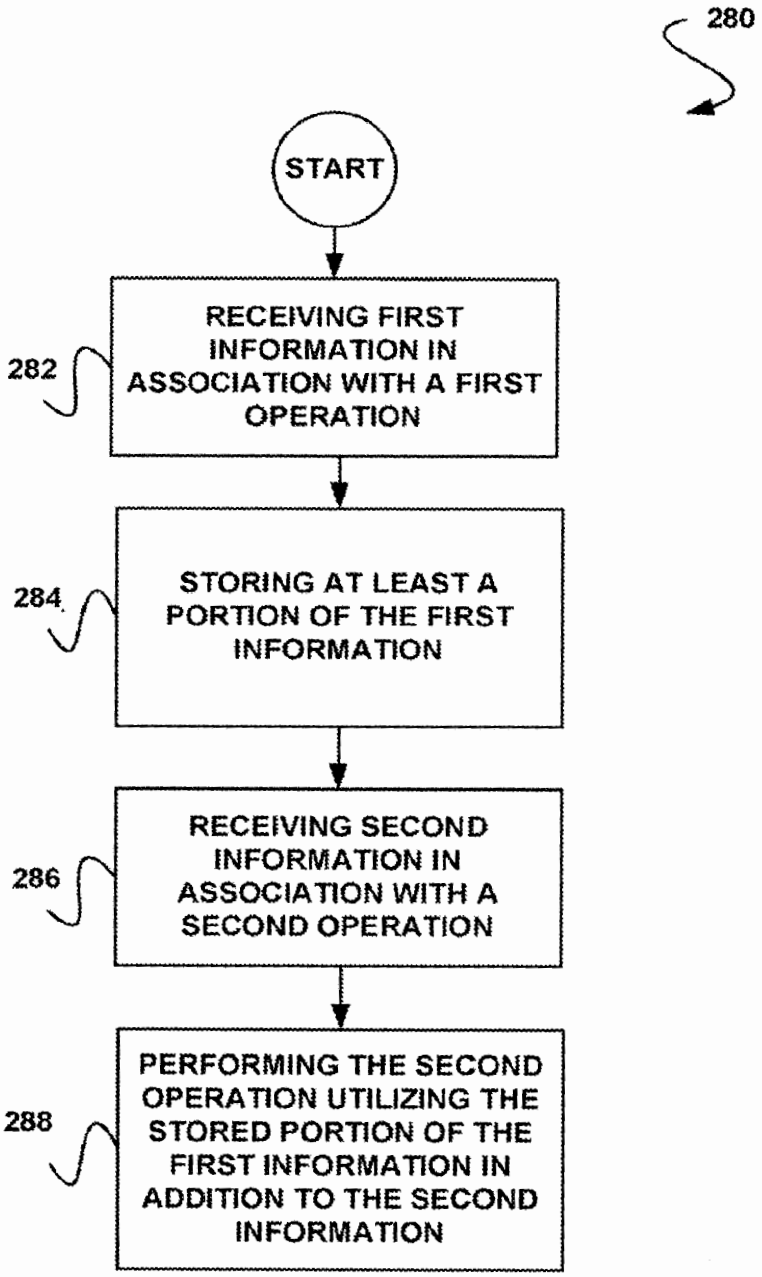
280
START
RECEIVING FIRST INFORMATION IN ASSOCIATION WITH A FIRST OPERATION
282
STORING AT LEAST A PORTION OF THE FIRST INFORMATION
284
RECEIVING SECOND INFORMATION IN ASSOCIATION WITH A SECOND OPERATION
286
PERFORMING THE SECOND OPERATION UTILIZING THE STORED PORTION OF THE FIRST INFORMATION IN ADDITION TO THE SECOND INFORMATION
288

FIGURE 2F

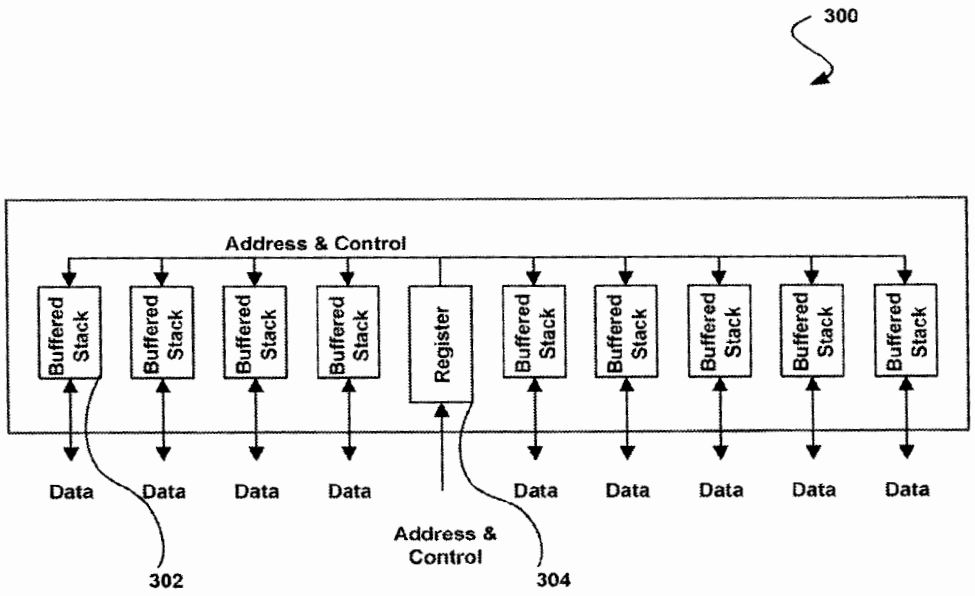
300
Address & Control
Buffered Stack
Buffered Stack
Buffered Stack
Buffered Stack
Register
Buffered Stack
Buffered Stack
Buffered Stack
Buffered Stack
Buffered Stack
Data
Data
Data
Data
Data
Data
Data
Data
Address & Control
302
304

FIGURE 3

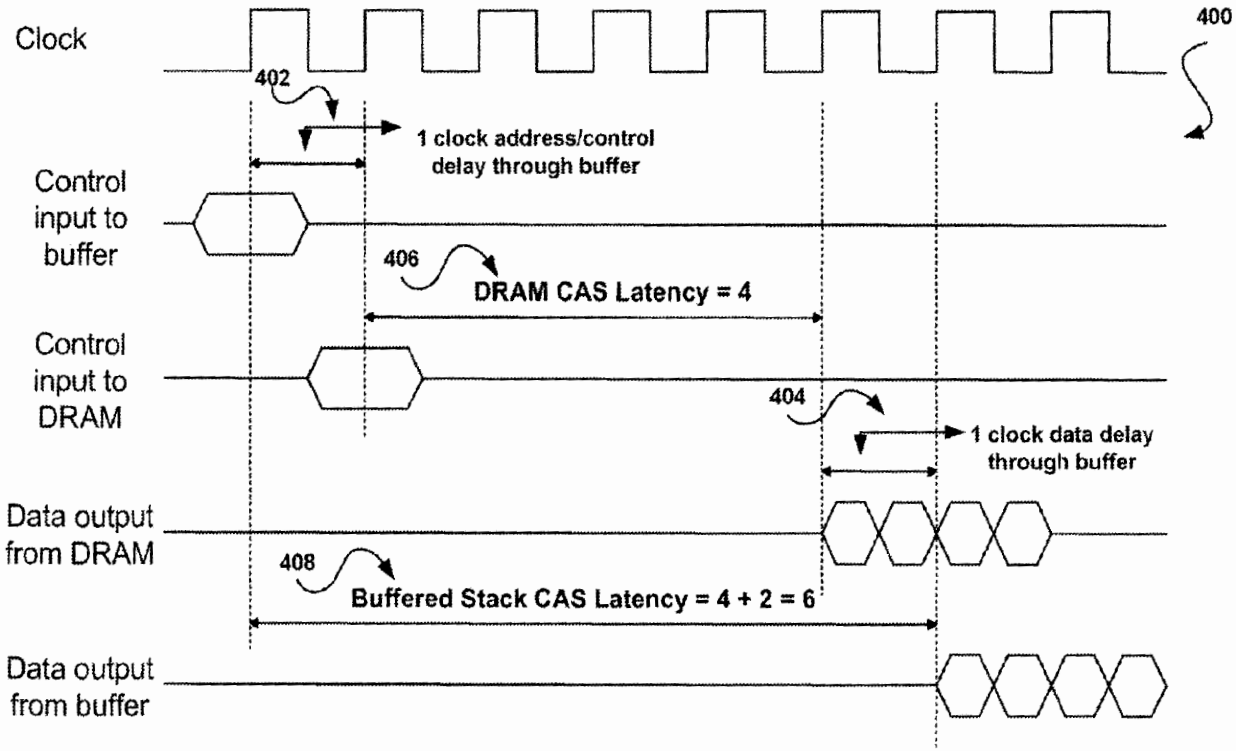
Clock
400
402
1 clock address/control delay through buffer
Control input to buffer
406
DRAM CAS Latency = 4
Control input to DRAM
404
1 clock data delay through buffer
Data output from DRAM
408
Buffered Stack CAS Latency = 4 + 2 = 6
Data output from buffer

FIGURE 4

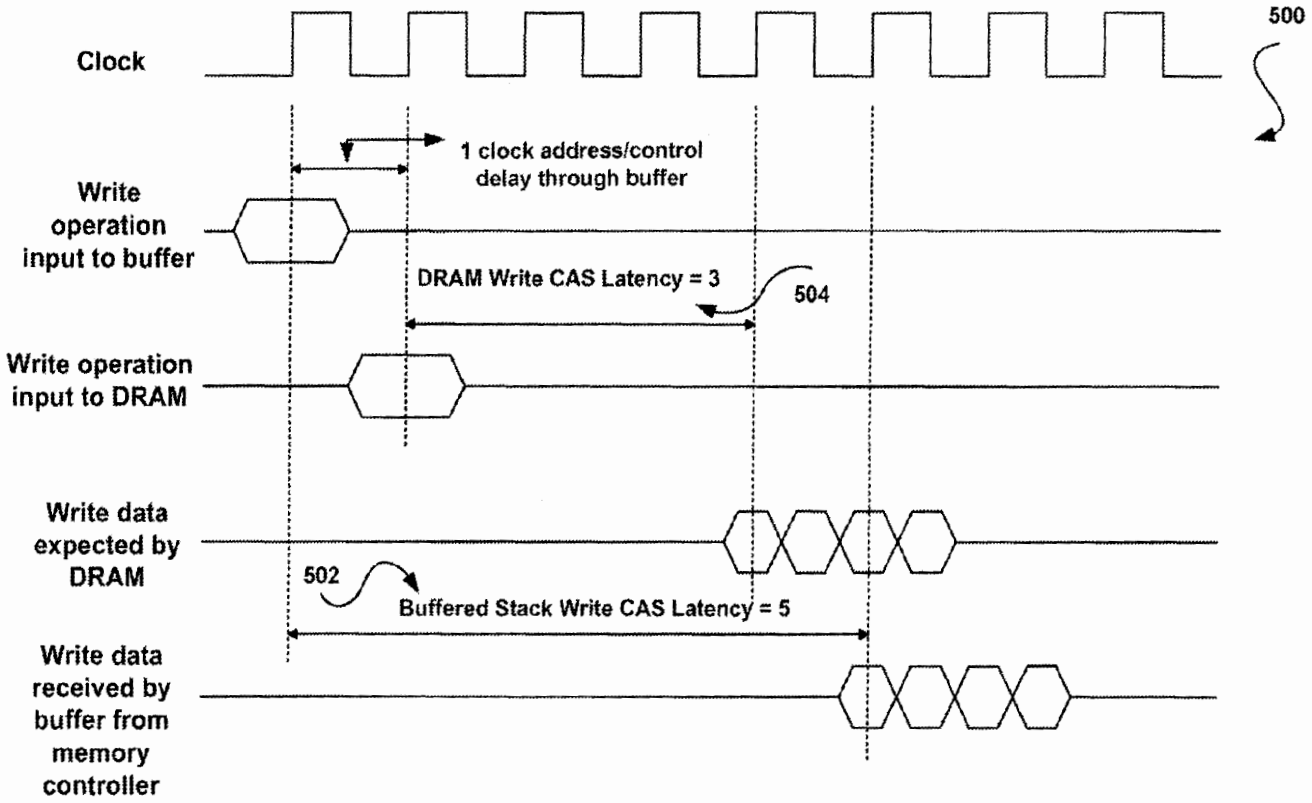
Clock
500
1 clock address/control delay through buffer
Write operation input to buffer
DRAM Write CAS Latency = 3
504
Write operation input to DRAM
Write data expected by DRAM
502
Buffered Stack Write CAS Latency = 5
Write data received by buffer from memory controller

FIGURE 5

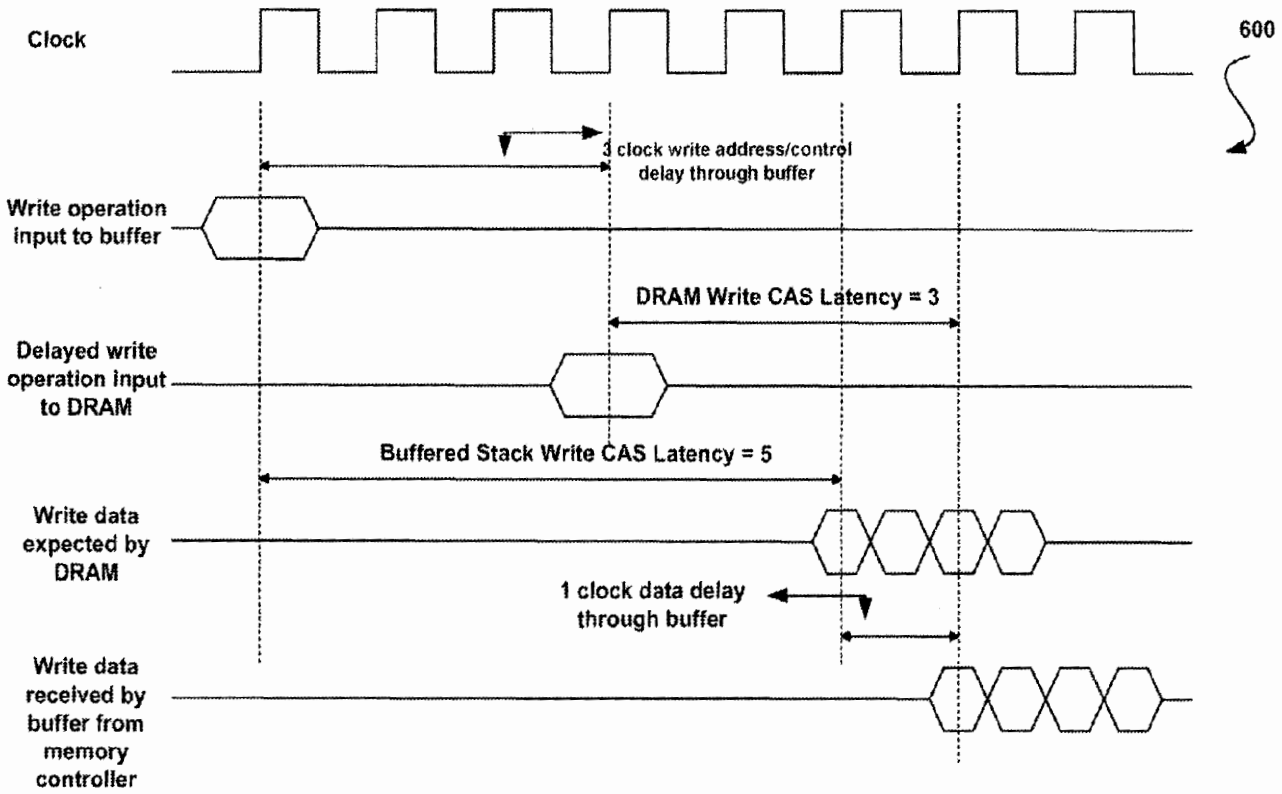
Clock
600
3 clock write address/control delay through buffer
Write operation input to buffer
DRAM Write CAS Latency = 3
Delayed write operation input to DRAM
Buffered Stack Write CAS Latency = 5
Write data expected by DRAM
1 clock data delay through buffer
Write data received by buffer from memory controller

FIGURE 6

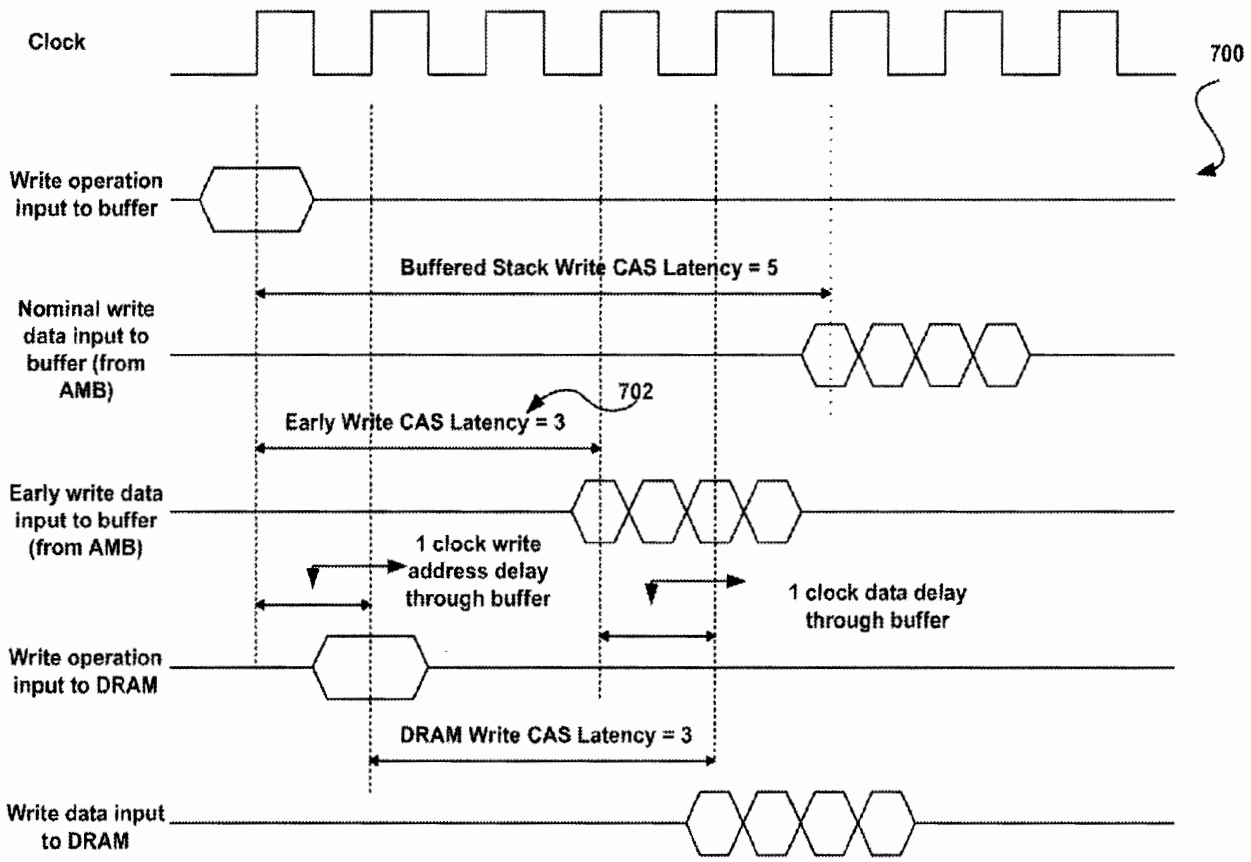
Clock
700
Write operation input to buffer
Buffered Stack Write CAS Latency = 5
Nominal write data input to buffer (from AMB)
702
Early Write CAS Latency = 3
Early write data input to buffer (from AMB)
1 clock write address delay through buffer
1 clock data delay through buffer
Write operation input to DRAM
DRAM Write CAS Latency = 3
Write data input to DRAM

FIGURE 7

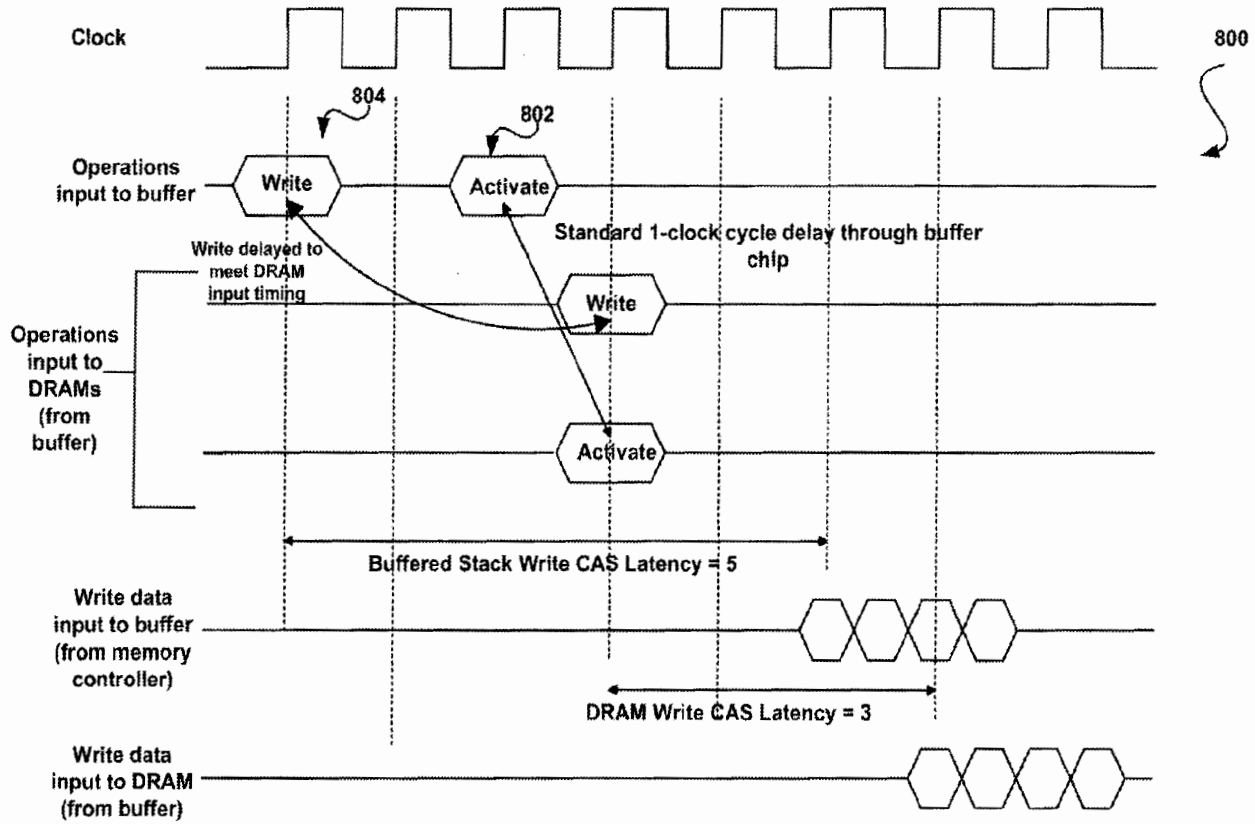
Clock
800
804
802
Operations input to buffer
Write
Activate
Standard 1-clock cycle delay through buffer chip
Write delayed to meet DRAM input timing
Write
Operations input to DRAMs (from buffer)
Activate
Buffered Stack Write CAS Latency = 5
Write data input to buffer (from memory controller)
DRAM Write CAS Latency = 3
Write data input to DRAM (from buffer)

FIGURE 8

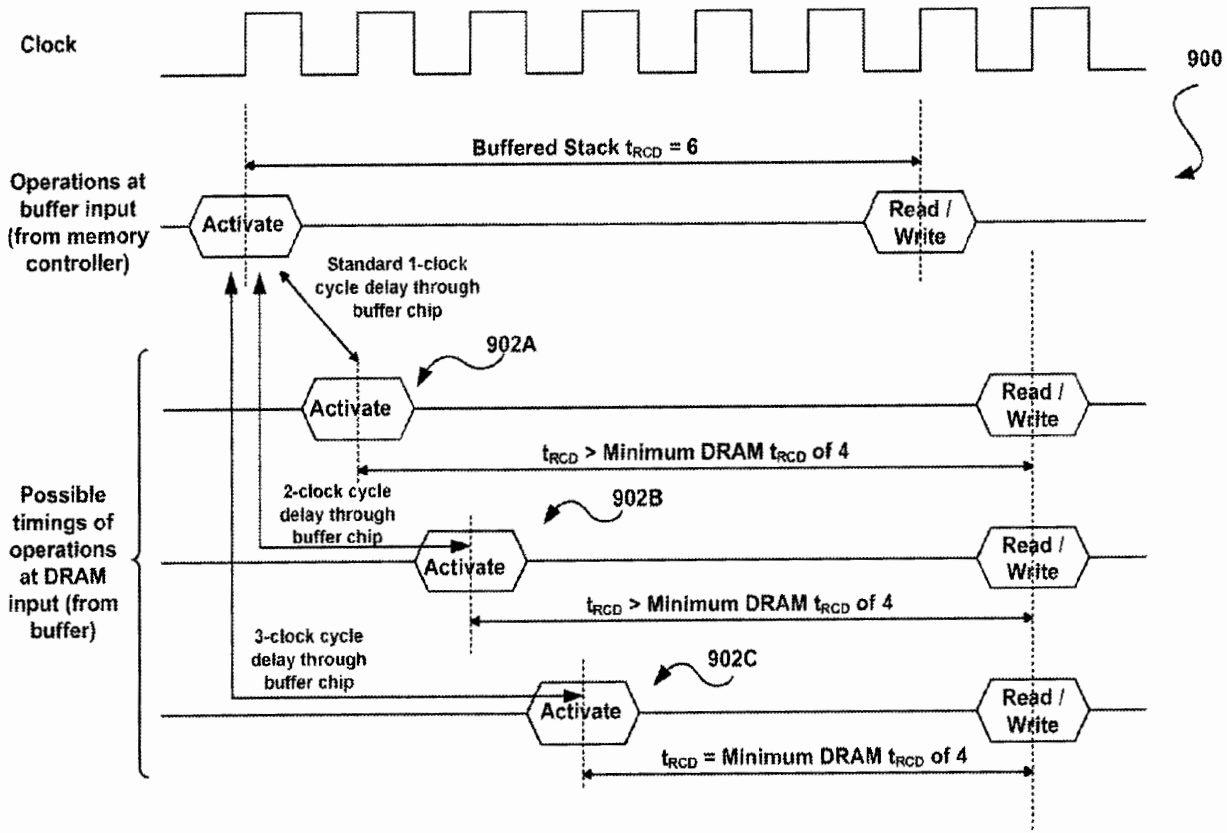
Clock
900
Buffered Stack t_{RCD} = 6
Operations at buffer input (from memory controller)
Activate
Read / Write
Standard 1-clock cycle delay through buffer chip
902A
Activate
Read / Write
t_{RCD} > Minimum DRAM t_{RCD} of 4
Possible timings of operations at DRAM input (from buffer)
2-clock cycle delay through buffer chip
902B
Activate
Read / Write
t_{RCD} > Minimum DRAM t_{RCD} of 4
3-clock cycle delay through buffer chip
902C
Activate
Read / Write
t_{RCD} = Minimum DRAM t_{RCD} of 4

FIGURE 9A

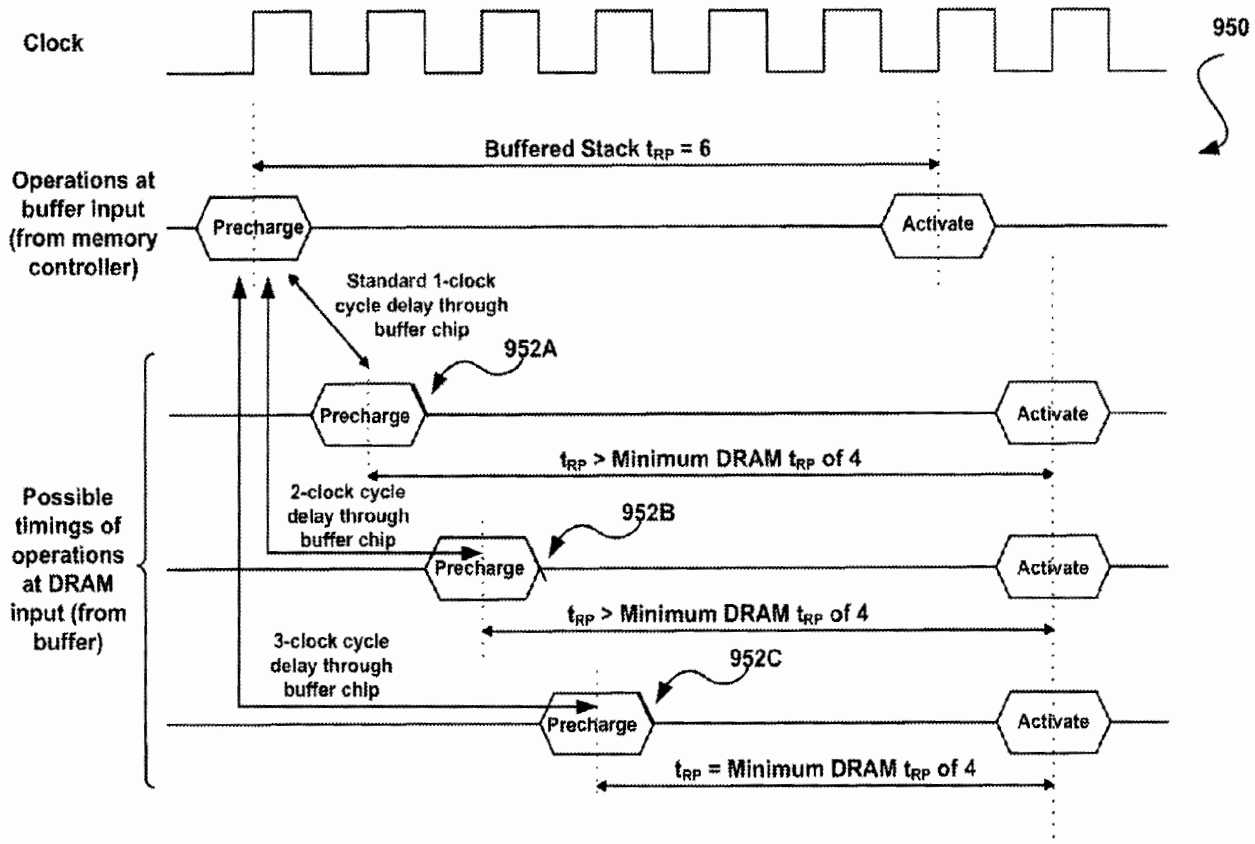
Clock
950
Buffered Stack t_{RP} = 6
Operations at buffer input (from memory controller)
Precharge
Activate
Standard 1-clock cycle delay through buffer chip
952A
Precharge
Activate
t_{RP} > Minimum DRAM t_{RP} of 4
Possible timings of operations at DRAM input (from buffer)
2-clock cycle delay through buffer chip
952B
Precharge
Activate
t_{RP} > Minimum DRAM t_{RP} of 4
3-clock cycle delay through buffer chip
952C
Precharge
Activate
t_{RP} = Minimum DRAM t_{RP} of 4

FIGURE 9B

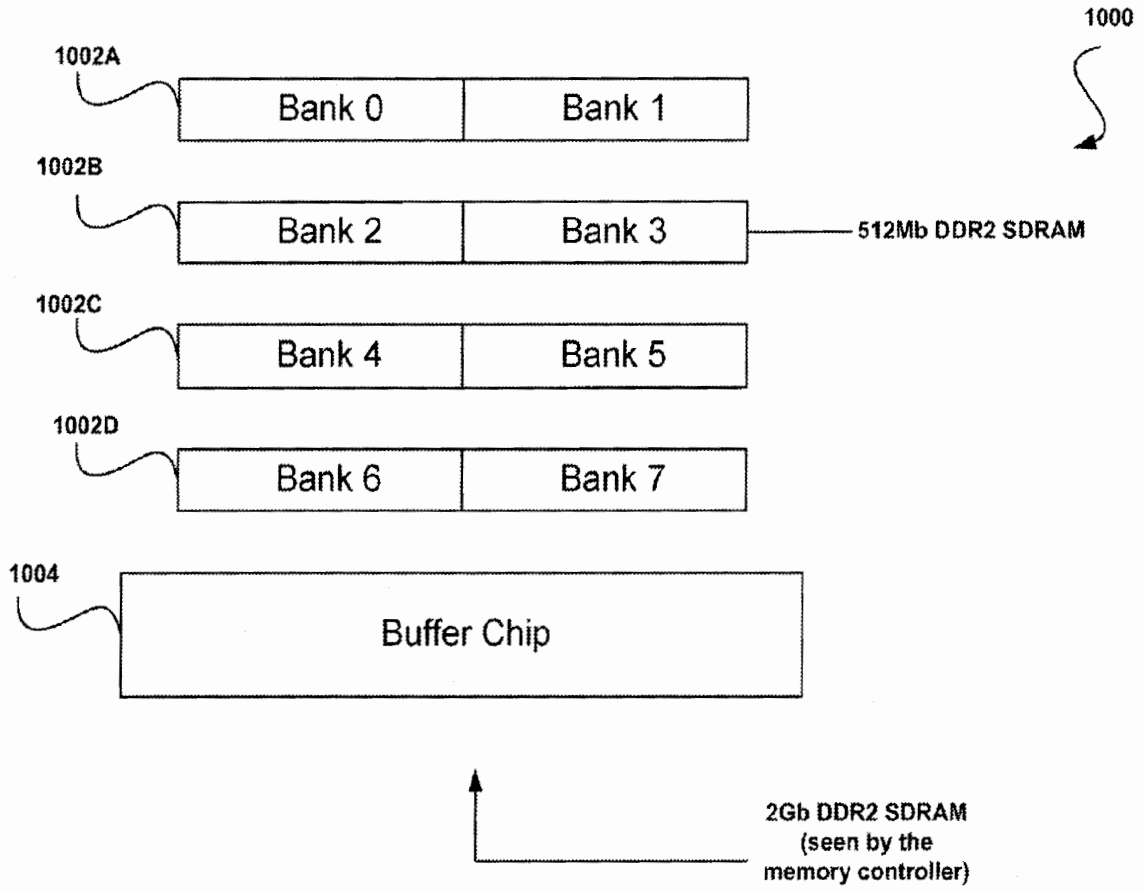

FIGURE 10

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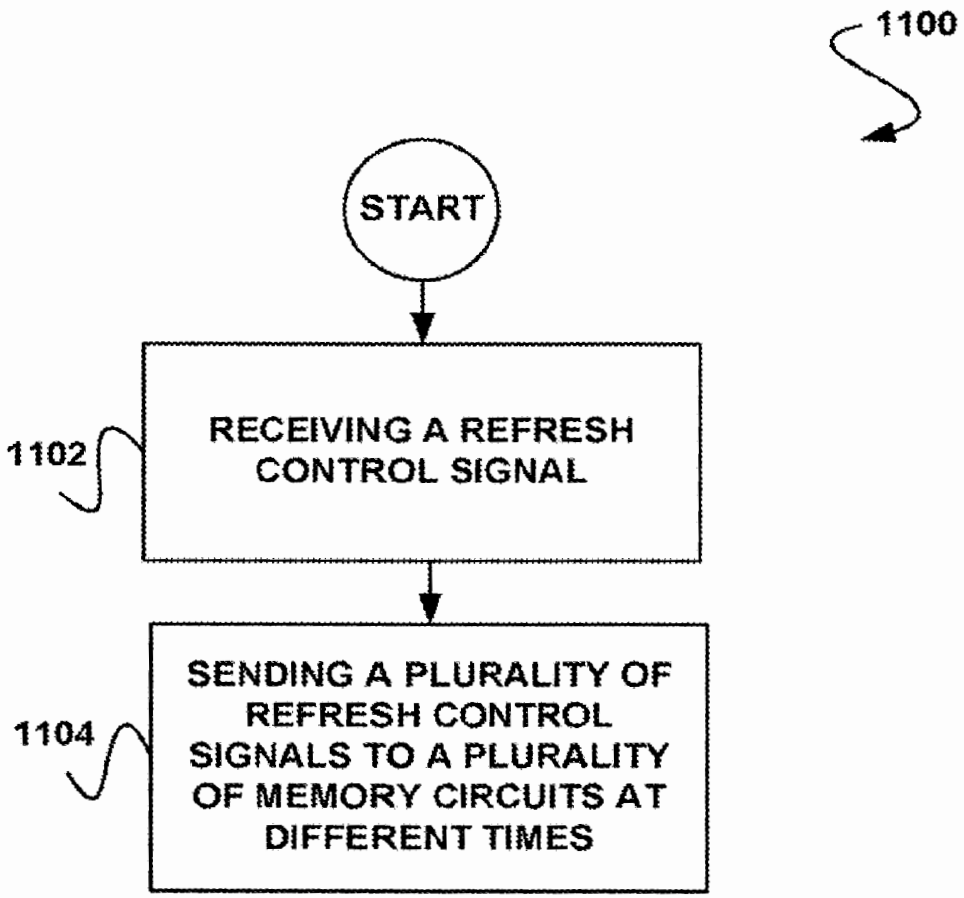
1100
START
1102
RECEIVING A REFRESH CONTROL SIGNAL
1104
SENDING A PLURALITY OF REFRESH CONTROL SIGNALS TO A PLURALITY OF MEMORY CIRCUITS AT DIFFERENT TIMES

FIGURE 11

SYSTEM AND METHOD FOR SIMULATING AN ASPECT OF A MEMORY CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention relates to memory, and more particularly to multiple-memory circuit systems.

BACKGROUND

[0002] The memory capacity requirements of computers in general, and servers in particular, are increasing rapidly due to various trends such as 64-bit processors and operating systems, multi-core processors, virtualization, etc. However, other industry trends such as higher memory bus speeds and small form factor machines, etc. are reducing the number of memory module slots in such systems. Thus, a need exists in the industry for large capacity memory circuits to be used in such systems.

[0003] However, there is also an exponential relationship between a capacity of monolithic memory circuits and a price associated therewith. As a result, large capacity memory modules may be cost prohibitive. To this end, the use of multiple smaller capacity memory circuits is a cost-effective approach to increasing such memory capacity.

SUMMARY

[0004] A system and method are provided for simulating an aspect of a memory circuit. Included is an interface circuit that is in communication with a plurality of memory circuits and a system. Such interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of memory circuits. In accordance with various embodiments, such aspect may include a signal, a capacity, a timing, and/or a logical interface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** illustrates a multiple memory circuit framework, in accordance with one embodiment.

[0006] FIGS. **2A-2E** show various configurations of a buffered stack of dynamic random access memory (DRAM) circuits with a buffer chip, in accordance with various embodiments.

[0007] FIG. **2F** illustrates a method for storing at least a portion of information received in association with a first operation for use in performing a second operation, in accordance with still another embodiment.

[0008] FIG. **3** shows a high capacity dual in-line memory module (DIMM) using buffered stacks, in accordance with still yet another embodiment.

[0009] FIG. **4** shows a timing design of a buffer chip that makes a buffered stack of DRAM circuits mimic longer column address strobe (CAS) latency DRAM to a memory controller, in accordance with another embodiment.

[0010] FIG. **5** shows the write data timing expected by DRAM in a buffered stack, in accordance with yet another embodiment.

[0011] FIG. **6** shows write control signals delayed by a buffer chip, in accordance with still yet another embodiment.

[0012] FIG. **7** shows early write data from an advanced memory buffer (AMB), in accordance with another embodiment.

[0013] FIG. **8** shows address bus conflicts caused by delayed write operations, in accordance with yet another embodiment.

[0014] FIGS. **9A-B** show variable delays of operations through a buffer chip, in accordance with another embodiment.

[0015] FIG. **10** shows a buffered stack of four 512 Mb DRAM circuits mapped to a single 2 Gb DRAM circuit, in accordance with yet another embodiment.

[0016] FIG. **11** illustrates a method for refreshing a plurality of memory circuits, in accordance with still yet another embodiment.

DETAILED DESCRIPTION

[0017] FIG. **1** illustrates a multiple memory circuit framework **100**, in accordance with one embodiment. As shown, included are an interface circuit **102**, a plurality of memory circuits **104**A, **104**B, **104**N, and a system **106**. In the context of the present description, such memory circuits **104**A, **104**B, **104**N may include any circuit capable of serving as memory.

[0018] For example, in various embodiments, one or more of the memory circuits **104**A, **104**B, **104**N may include a monolithic memory circuit. For instance, such monolithic memory circuit may take the form of dynamic random access memory (DRAM). Such DRAM may take any form including, but not limited to synchronous (SDRAM), double data rate synchronous (DDR DRAM, DDR2 DRAM, DDR3 DRAM, etc.), quad data rate (QDR DRAM), direct RAM-BUS (DRDRAM), fast page mode (FPM DRAM), video (VDRAM), extended data out (EDO DRAM), burst EDO (BEDO DRAM), multibank (MDRAM), synchronous graphics (SGRAM), and/or any other type of DRAM. Of course, one or more of the memory circuits **104**A, **104**B, **104**N may include other types of memory such as magnetic random access memory (MRAM), intelligent random access memory (IRAM), distributed network architecture (DNA) memory, window random access memory (WRAM), flash memory (e.g. NAND, NOR, or others, etc.), pseudostatic random access memory (PSRAM), wetware memory, and/or any other type of memory circuit that meets the above definition.

[0019] In additional embodiments, the memory circuits **104**A, **104**B, **104**N may be symmetrical or asymmetrical. For example, in one embodiment, the memory circuits **104**A, **104**B, **104**N may be of the same type, brand, and/or size, etc. Of course, in other embodiments, one or more of the memory circuits **104**A, **104**B, **104**N may be of a first type, brand, and/or size; while one or more other memory circuits **104**A, **104**B, **104**N may be of a second type, brand, and/or size, etc. Just by way of example, one or more memory circuits **104**A, **104**B, **104**N may be of a DRAM type, while one or more other memory circuits **104**A, **104**B, **104**N may be of a flash type. While three or more memory circuits **104**A, **104**B, **104**N are shown in FIG. **1** in accordance with one embodiment, it should be noted that any plurality of memory circuits **104**A, **104**B, **104**N may be employed.

[0020] Strictly as an option, the memory circuits **104**A, **104**B, **104**N may or may not be positioned on at least one dual in-line memory module (DIMM) (not shown). In various embodiments, the DIMM may include a registered DIMM (R-DIMM), a small outline-DIMM (SO-DIMM), a fully buffered-DIMM (FB-DIMM), an un-buffered DIMM,

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etc. Of course, in other embodiments, the memory circuits **104**A, **104**B, **104**N may or may not be positioned on any desired entity for packaging purposes.

[0021] Further in the context of the present description, the system **106** may include any system capable of requesting and/or initiating a process that results in an access of the memory circuits **104**A, **104**B, **104**N. As an option, the system **106** may accomplish this utilizing a memory controller (not shown), or any other desired mechanism. In one embodiment, such system **106** may include a host system in the form of a desktop computer, lap-top computer, server, workstation, a personal digital assistant (PDA) device, a mobile phone device, a television, a peripheral device (e.g. printer, etc.). Of course, such examples are set forth for illustrative purposes only, as any system meeting the above definition may be employed in the context of the present framework **100**.

[0022] Turning now to the interface circuit **102**, such interface circuit **102** may include any circuit capable of indirectly or directly communicating with the memory circuits **104**A, **104**B, **104**N and the system **106**. In various optional embodiments, the interface circuit **102** may include one or more interface circuits, a buffer chip, etc. Embodiments involving such a buffer chip will be set forth hereinafter during reference to subsequent figures. In still other embodiments, the interface circuit **102** may or may not be manufactured in monolithic form.

[0023] While the memory circuits **104**A, **104**B, **104**N, interface circuit **102**, and system **106** are shown to be separate parts, it is contemplated that any of such parts (or portions thereof) may or may not be integrated in any desired manner. In various embodiments, such optional integration may involve simply packaging such parts together (e.g. stacking the parts, etc.) and/or integrating them monolithically. Just by way of example, in various optional embodiments, one or more portions (or all, for that matter) of the interface circuit **102** may or may not be packaged with one or more of the memory circuits **104**A, **104**B, **104**N (or all, for that matter). Different optional embodiments which may be implemented in accordance with the present multiple memory circuit framework **100** will be set forth hereinafter during reference to FIGS. **2**A-**2**E, and **3** et al.

[0024] In use, the interface circuit **102** may be capable of various functionality, in the context of different embodiments. More illustrative information will now be set forth regarding such optional functionality which may or may not be implemented in the context of such interface circuit **102**, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. For example, any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0025] For instance, in one optional embodiment, the interface circuit **102** interfaces a plurality of signals **108** that are communicated between the memory circuits **104**A, **104**B, **104**N and the system **106**. As shown, such signals may, for example, include address/control/clock signals, etc. In one aspect of the present embodiment, the interfaced signals **108** may represent all of the signals that are communicated between the memory circuits **104**A, **104**B, **104**N and the system **106**. In other aspects, at least a portion of signals **110** may travel directly between the memory circuits **104**A, **104**B, **104**N and the system **106** or component thereof [e.g. register, advanced memory buffer (AMB), memory controller, or any other component thereof, where the term component is defined hereinbelow]. In various embodiments, the number of the signals **108** (vs. a number of the signals **110**, etc.) may vary such that the signals **108** are a majority or more (L>M), etc.

[0026] In yet another embodiment, the interface circuit **102** may be operable to interface a first number of memory circuits **104**A, **104**B, **104**N and the system **106** for simulating at least one memory circuit of a second number. In the context of the present description, the simulation may refer to any simulating, emulating, disguising, transforming, converting, and/or the like that results in at least one aspect (e.g. a number in this embodiment, etc.) of the memory circuits **104**A, **104**B, **104**N appearing different to the system **106**. In different embodiments, the simulation may be electrical in nature, logical in nature, protocol in nature, and/or performed in any other desired manner. For instance, in the context of electrical simulation, a number of pins, wires, signals, etc. may be simulated, while, in the context of logical simulation, a particular function may be simulated. In the context of protocol, a particular protocol (e.g. DDR3, etc.) may be simulated.

[0027] In still additional aspects of the present embodiment, the second number may be more or less than the first number. Still yet, in the latter case, the second number may be one, such that a single memory circuit is simulated. Different optional embodiments which may employ various aspects of the present embodiment will be set forth hereinafter during reference to FIGS. **2**A-**2**E, and **3** et al.

[0028] In still yet another embodiment, the interface circuit **102** may be operable to interface the memory circuits **104**A, **104**B, **104**N and the system **106** for simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of the memory circuits **104**A, **104**B, **104**N. In accordance with various aspects of such embodiment, such aspect may include a signal, a capacity, a timing, a logical interface, etc. Of course, such examples of aspects are set forth for illustrative purposes only and thus should not be construed as limiting, since any aspect associated with one ore more of the memory circuits **104**A, **104**B, **104**N may be simulated differently in the foregoing manner.

[0029] In the case of the signal, such signal may refer to a control signal (e.g. an address signal; a signal associated with an activate operation, precharge operation, write operation, read operation, a mode register write operation, a mode register read operation, a refresh operation; etc.), a data signal, a logical or physical signal, or any other signal for that matter. For instance, a number of the aforementioned signals may be simulated to appear as fewer or more signals, or even simulated to correspond to a different type. In still other embodiments, multiple signals may be combined to simulated another signal. Even still, a length of time in which a signal is asserted may be simulated to be different.

[0030] In the case of protocol, such may, in one exemplary embodiment, refer to a particular standard protocol. For example, a number of memory circuits **104**A, **104**B, **104**N that obey a standard protocol (e.g. DDR2, etc.) may be used to simulate one or more memory circuits that obey a different protocol (e.g. DDR3, etc.). Also, a number of memory circuits **104**A, **104**B, **104**N that obey a version of protocol (e.g. DDR2 with 3-3-3 latency timing, etc.) may be

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used to simulate one or more memory circuits that obey a different version of the same protocol (e.g. DDR2 with 5-5-5 latency timing, etc.).

[0031] In the case of capacity, such may refer to a memory capacity (which may or may not be a function of a number of the memory circuits **104**A, **104**B, **104**N; see previous embodiment). For example, the interface circuit **102** may be operable for simulating at least one memory circuit with a first memory capacity that is greater than (or less than) a second memory capacity of at least one of the memory circuits **104**A, **104**B, **104**N.

[0032] In the case where the aspect is timing-related, the timing may possibly relate to a latency (e.g. time delay, etc.). In one aspect of the present embodiment, such latency may include a column address strobe (CAS) latency, which refers to a latency associated with accessing a column of data. Still yet, the latency may include a row address to column address latency (tRCD), which refers to a latency required between the row address strobe (RAS) and CAS. Even still, the latency may include a row precharge latency (tRP), which refers a latency required to terminate access to an open row, and open access to a next row. Further, the latency may include an activate to precharge latency (tRAS), which refers to a latency required to access a certain row of data between an activate operation and a precharge operation. In any case, the interface circuit **102** may be operable for simulating at least one memory circuit with a first latency that is longer (or shorter) than a second latency of at least one of the memory circuits **104**A, **104**B, **104**N. Different optional embodiments which employ various features of the present embodiment will be set forth hereinafter during reference to FIGS. **2**A-**2**E, and **3** et al.

[0033] In still another embodiment, a component may be operable to receive a signal from the system **106** and communicate the signal to at least one of the memory circuits **104**A, **104**B, **104**N after a delay. Again, the signal may refer to a control signal (e.g. an address signal; a signal associated with an activate operation, precharge operation, write operation, read operation; etc.), a data signal, a logical or physical signal, or any other signal for that matter. In various embodiments, such delay may be fixed or variable (e.g. a function of the current signal, the previous signal, etc.). In still other embodiments, the component may be operable to receive a signal from at least one of the memory circuits **104**A, **104**B, **104**N and communicate the signal to the system **106** after a delay.

[0034] As an option, the delay may include a cumulative delay associated with any one or more of the aforementioned signals. Even still, the delay may result in a time shift of the signal forward and/or back in time (with respect to other signals). Of course, such forward and backward time shift may or may not be equal in magnitude. In one embodiment, this time shifting may be accomplished by utilizing a plurality of delay functions which each apply a different delay to a different signal. In still additional embodiments, the aforementioned shifting may be coordinated among multiple signals such that different signals are subject to shifts with different relative directions/magnitudes, in an organized fashion.

[0035] Further, it should be noted that the aforementioned component may, but need not necessarily take the form of the interface circuit **102** of FIG. **1**. For example, the component may include a register, an AMB, a component positioned on at least one DIMM, a memory controller, etc. Such register may, in various embodiments, include a Joint Electron Device Engineering Council (JEDEC) register, a JEDEC register including one or more functions set forth herein, a register with forwarding, storing, and/or buffering capabilities, etc. Different optional embodiments which employ various features of the present embodiment will be set forth hereinafter during reference to FIGS. **4**-**7**, and **9**A-B et al.

[0036] In a power-saving embodiment, at least one of a plurality of memory circuits **104**A, **104**B, **104**N may be identified that is not currently being accessed by the system **106**. In one embodiment, such identification may involve determining whether a page [i.e. any portion of any memory (s), etc.] is being accessed in at least one of the plurality of memory circuits **104**A, **104**B, **104**N. Of course, any other technique may be used that results in the identification of at least one of the memory circuits **104**A, **104**B, **104**N that is not being accessed.

[0037] In response to the identification of the at least one memory circuit **104**A, **104**B, **104**N, a power saving operation is initiated in association with the at least one memory circuit **104**A, **104**B, **104**N. In one optional embodiment, such power saving operation may involve a power down operation and, in particular, a precharge power down operation. Of course, however, it should be noted that any operation that results in at least some power savings may be employed in the context of the present embodiment.

[0038] Similar to one or more of the previous embodiments, the present functionality or a portion thereof may be carried out utilizing any desired component. For example, such component may, but need not necessarily take the form of the interface circuit **102** of FIG. **1**. In other embodiments, the component may include a register, an AMB, a component positioned on at least one DIMM, a memory controller, etc. One optional embodiment which employs various features of the present embodiment will be set forth hereinafter during reference to FIG. **10**.

[0039] In still yet another embodiment, a plurality of the aforementioned components may serve, in combination, to interface the memory circuits **104**A, **104**B, **104**N and the system **106**. In various embodiments, two, three, four, or more components may accomplish this. Also, the different components may be relatively configured in any desired manner. For example, the components may be configured in parallel, serially, or a combination thereof. In addition, any number of the components may be allocated to any number of the memory circuits **104**A, **104**B, **104**N.

[0040] Further, in the present embodiment, each of the plurality of components may be the same or different. Still yet, the components may share the same or similar interface tasks and/or perform different interface tasks. Such interface tasks may include, but are not limited to simulating one or more aspects of a memory circuit, performing a power savings/refresh operation, carrying out any one or more of the various functionalities set forth herein, and/or any other task relevant to the aforementioned interfacing. One optional embodiment which employs various features of the present embodiment will be set forth hereinafter during reference to FIG. **3**.

[0041] Additional illustrative information will now be set forth regarding various optional embodiments in which the foregoing techniques may or may not be implemented, per the desires of the user. For example, an embodiment is set forth for storing at least a portion of information received in

association with a first operation for use in performing a second operation. See FIG. **2**F. Further, a technique is provided for refreshing a plurality of memory circuits, in accordance with still yet another embodiment. See FIG. **11**.

[0042] It should again be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0043] FIGS. **2**A-**2**E show various configurations of a buffered stack of DRAM circuits **206**A-D with a buffer chip **202**, in accordance with various embodiments. As an option, the various configurations to be described in the following embodiments may be implemented in the context of the architecture and/or environment of FIG. **1**. Of course, however, they may also be carried out in any other desired environment (e.g. using other memory types, etc.). It should also be noted that the aforementioned definitions may apply during the present description.

[0044] As shown in each of such figures, the buffer chip **202** is placed electrically between an electronic host system **204** and a stack of DRAM circuits **206**A-D. In the context of the present description, a stack may refer to any collection of memory circuits. Further, the buffer chip **202** may include any device capable of buffering a stack of circuits (e.g. DRAM circuits **206**A-D, etc.). Specifically, the buffer chip **202** may be capable of buffering the stack of DRAM circuits **206**A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system **204**. In this way, the stack of DRAM circuits **206**A-D may appear as a smaller quantity of larger capacity DRAM circuits to the host system **204**.

[0045] For example, the stack of DRAM circuits **206**A-D may include eight 512 Mb DRAM circuits. Thus, the buffer chip **202** may buffer the stack of eight 512 Mb DRAM circuits to resemble a single 4 Gb DRAM circuit to a memory controller (not shown) of the associated host system **204**. In another example, the buffer chip **202** may buffer the stack of eight 512 Mb DRAM circuits to resemble two 2 Gb DRAM circuits to a memory controller of an associated host system **204**.

[0046] Further, the stack of DRAM circuits **206**A-D may include any number of DRAM circuits. Just by way of example, a buffer chip **202** may be connected to 2, 4, 8 or more DRAM circuits **206**A-D. Also, the DRAM circuits **206**A-D may be arranged in a single stack, as shown in FIGS. **2**A-**2**D.

[0047] The DRAM circuits **206**A-D may be arranged on a single side of the buffer chip **202**, as shown in FIGS. **2**A-**2**D. Of course, however, the DRAM circuits **206**A-D may be located on both sides of the buffer chip **202** shown in FIG. **2**E. Thus, for example, a buffer chip **202** may be connected to 16 DRAM circuits with 8 DRAM circuits on either side of the buffer chip **202**, where the 8 DRAM circuits on each side of the buffer chip **202** are arranged in two stacks of four DRAM circuits.

[0048] The buffer chip **202** may optionally be a part of the stack of DRAM circuits **206**A-D. Of course, however, the buffer chip **202** may also be separate from the stack of DRAM circuits **206**A-D. In addition, the buffer chip **202** may be physically located anywhere in the stack of DRAM circuits **206**A-D, where such buffer chip **202** electrically sits between the electronic host system **204** and the stack of DRAM circuits **206**A-D.

[0049] In one embodiment, a memory bus (not shown) may connect to the buffer chip **202**, and the buffer chip **202** may connect to each of the DRAM circuits **206**A-D in the stack. As shown in FIGS. 2A-D, the buffer chip **202** may be located at the bottom of the stack of DRAM circuits **206**A-D (e.g. the bottom-most device in the stack). As another option, and as shown in FIG. **2**E, the buffer chip **202** may be located in the middle of the stack of DRAM circuits **206**A-D. As still yet another option, the buffer chip **202** may be located at the top of the stack of DRAM circuits **206**A-D (e.g. the top-most device in the stack). Of course, however, the buffer chip **202** may be located anywhere between the two extremities of the stack of DRAM circuits **206**A-D.

[0050] The electrical connections between the buffer chip **202** and the stack of DRAM circuits **206**A-D may be configured in any desired manner. In one optional embodiment; address, control (e.g. command, etc.), and clock signals may be common to all DRAM circuits **206**A-D in the stack (e.g. using one common bus). As another option, there may be multiple address, control and clock busses. As yet another option, there may be individual address, control and clock busses to each DRAM circuit **206**A-D. Similarly, data signals may be wired as one common bus, several busses or as an individual bus to each DRAM circuit **206**A-D. Of course, it should be noted that any combinations of such configurations may also be utilized.

[0051] For example, as shown in FIG. **2**A, the stack of DRAM circuits **206**A-D may have one common address, control and clock bus **208** with individual data busses **210**. In another example, as shown in FIG. **2**B, the stack of DRAM circuits **206**A-D may have two address, control and clock busses **208** along with two data busses **210**. In still yet another example, as shown in FIG. **2**C, the stack of DRAM circuits **206**A-D may have one address, control and clock bus **208** together with two data busses **210**. In addition, as shown in FIG. **2**D, the stack of DRAM circuits **206**A-D may have one common address, control and clock bus **208** and one common data bus **210**. It should be noted that any other permutations and combinations of such address, control, clock and data buses may be utilized.

[0052] These configurations may therefore allow for the host system **204** to only be in contact with a load of the buffer chip **202** on the memory bus. In this way, any electrical loading problems (e.g. bad signal integrity, improper signal timing, etc.) associated with the stacked DRAM circuits **206**A-D may (but not necessarily) be prevented, in the context of various optional embodiments.

[0053] FIG. **2**F illustrates a method **280** for storing at least a portion of information received in association with a first operation for use in performing a second operation, in accordance with still yet another embodiment. As an option, the method **280** may be implemented in the context of the architecture and/or environment of any one or more of FIGS. **1**-**2**E. For example, the method **280** may be carried out by the interface circuit **102** of FIG. **1**. Of course, however, the method **280** may be carried out in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0054] In operation **282**, first information is received in association with a first operation to be performed on at least one of a plurality of memory circuits (e.g. see the memory circuits **104**A, **104**B, **104**N of FIG. **1**, etc.). In various embodiments, such first information may or may not be received coincidently with the first operation, as long as it is

associated in some capacity. Further, the first operation may, in one embodiment, include a row operation. In such embodiment, the first information may include address information (e.g. a set of address bits, etc.).

[0055] For reasons that will soon become apparent, at least a portion of the first information is stored. Note operation **284**. Still yet, in operation **286**, second information is received in association with a second operation. Similar to the first information, the second information may or may not be received coincidently with the second operation, and may include address information. Such second operation, however, may, in one embodiment, include a column operation.

[0056] To this end, the second operation may be performed utilizing the stored portion of the first information in addition to the second information. See operation **288**. More illustrative information will now be set forth regarding various optional features with which the foregoing method **280** may or may not be implemented, per the desires of the user. Specifically, an example will be set for illustrating the manner in which the method **280** may be employed for accommodating a buffer chip that is simulating at least one aspect of a plurality of memory circuits.

[0057] In particular, the present example of the method **280** of FIG. **2**F will be set forth in the context of the various components (e.g. buffer chip **202**, etc.) shown in the embodiments of FIGS. **2**A-**2**E. It should be noted that, since the buffered stack of DRAM circuits **206**A-D may appear to the memory controller of the host system **204** as one or more larger capacity DRAM circuits, the buffer chip **202** may receive more address bits from the memory controller than are required by the DRAM circuits **206**A-D in the stack. These extra address bits may be decoded by the buffer chip **202** to individually select the DRAM circuits **206**A-D in the stack, utilizing separate chip select signals to each of the DRAM circuits **206**A-D in the stack.

[0058] For example, a stack of four ×4 1 Gb DRAM circuits **206**A-D behind a buffer chip **202** may appear as a single ×4 4 Gb DRAM circuit to the memory controller. Thus, the memory controller may provide sixteen row address bits and three bank address bits during a row (e.g. activate) operation, and provide eleven column address bits and three bank address bits during a column (e.g. read or write) operation. However, the individual DRAM circuits **206**A-D in the stack may require only fourteen row address bits and three bank address bits for a row operation, and eleven column address bits and three bank address bits during a column operation.

[0059] As a result, during a row operation in the above example, the buffer chip **202** may receive two address bits more than are needed by each DRAM circuit **206**A-D in the stack. The buffer chip **202** may therefore use the two extra address bits from the memory controller to select one of the four DRAM circuits **206**A-D in the stack. In addition, the buffer chip **202** may receive the same number of address bits from the memory controller during a column operation as are needed by each DRAM circuit **206**A-D in the stack.

[0060] Thus, in order to select the correct DRAM circuit **206**A-D in the stack during a column operation, the buffer chip **202** may be designed to store the two extra address bits provided during a row operation and use the two stored address bits to select the correct DRAM circuit **206**A-D during the column operation. The mapping between a system address (e.g. address from the memory controller, including the chip select signal(s)) and a device address (e.g. the address, including the chip select signals, presented to the DRAM circuits **206**A-D in the stack) may be performed by the buffer chip **202** in various manners.

[0061] In one embodiment, a lower order system row address and bank address bits may be mapped directly to the device row address and bank address inputs. In addition, the most significant row address bit(s) and, optionally, the most significant bank address bit(s), may be decoded to generate the chip select signals for the DRAM circuits **206**A-D in the stack during a row operation. The address buts used to generate the chip select signals during the row operation may also be stored in an internal lookup table by the buffer chip **22** for one or more clock cycles. During a column operation, the system column address and bank address bits may be mapped directly to the device column address and bank address inputs, while the stored address bits may be decoded to generate the chip select signals.

[0062] For example, addresses may be mapped between four 512 Mb DRAM circuits **206**A-D that simulate a single 2 Gb DRAM circuits utilizing the buffer chip **202**. There may be 15 row address bits from the system **204**, such that row address bits **0** through **13** are mapped directly to the DRAM circuits **206**A-D. There may also be 3 bank address bits from the system **204**, such that bank address bits **0** through **1** are mapped directly to the DRAM circuits **206**A-D.

[0063] During a row operation, the bank address bit **2** and the row address bit **14** may be decoded to generate the 4 chip select signals for each of the four DRAM circuits **206**A-D. Row address bit **14** may be stored during the row operation using the bank address as the index. In addition, during the column operation, the stored row address bit **14** may again used with bank address bit **2** to form the four DRAM chip select signals.

[0064] As another example, addresses may be mapped between four 1 Gb DRAM circuits **206**A-D that simulate a single 4 Gb DRAM circuits utilizing the buffer chip **202**. There may be 16 row address bits from the system **204**, such that row address bits **0** through **14** are mapped directly to the DRAM circuits **206**A-D. There may also be 3 bank address bits from the system **204**, such that bank address bits **0** through **3** are mapped directly to the DRAM circuits **206**A-D.

[0065] During a row operation, row address bits **14** and **15** may be decoded to generate the 4 chip select signals for each of the four DRAM circuits **206**A-D. Row address bits **14** and **15** may also be stored during the row operation using the bank address as the index. During the column operation, the stored row address bits **14** and **15** may again be used to form the four DRAM chip select signals.

[0066] In various embodiments, this mapping technique may optionally be used to ensure that there are no unnecessary combinational logic circuits in the critical timing path between the address input pins and address output pins of the buffer chip **202**. Such combinational logic circuits may instead be used to generate the individual chip select signals. This may therefore allow the capacitive loading on the address outputs of the buffer chip **202** to be much higher than the loading on the individual chip select signal outputs of the buffer chip **202**.

[0067] In another embodiment, the address mapping may be performed by the buffer chip **202** using some of the bank address signals from the memory controller to generate the individual chip select signals. The buffer chip **202** may store

the higher order row address bits during a row operation using the bank address as the index, and then may use the stored address bits as part of the DRAM circuit bank address during a column operation. This address mapping technique may require an optional lookup table to be positioned in the critical timing path between the address inputs from the memory controller and the address outputs, to the DRAM circuits **206**A-D in the stack.

[0068] For example, addresses may be mapped between four 512 Mb DRAM circuits **206**A-D that simulate a single 2 Gb DRAM utilizing the buffer chip **202**. There may be 15 row address bits from the system **204**, where row address bits **0** through **13** are mapped directly to the DRAM circuits **206**A-D. There may also be 3 bank address bits from the system **204**, such that bank address bit **0** is used as a DRAM circuit bank address bit for the DRAM circuits **206**A-D.

[0069] In addition, row address bit **14** may be used as an additional DRAM circuit bank address bit. During a row operation, the bank address bits **1** and **2** from the system may be decoded to generate the 4 chip select signals for each of the four DRAM circuits **206**A-D. Further, row address bit **14** may be stored during the row operation. During the column operation, the stored row address bit **14** may again be used along with the bank address bit **0** from the system to form the DRAM circuit bank address.

[0070] In both of the above described address mapping techniques, the column address from the memory controller may be mapped directly as the column address to the DRAM circuits **206**A-D in the stack. Specifically, this direct mapping may be performed since each of the DRAM circuits **206**A-D in the stack, even if of the same width but different capacities (e.g. from 512 Mb to 4 Gb), may have the same page sizes. In an optional embodiment, address A[**10**] may be used by the memory controller to enable or disable auto-precharge during a column operation. Therefore, the buffer chip **202** may forward A[10] from the memory controller to the DRAM circuits **206**A-D in the stack without any modifications during a column operation.

[0071] In various embodiments, it may be desirable to determine whether the simulated DRAM circuit behaves according to a desired DRAM standard or other design specification. A behavior of many DRAM circuits is specified by the JEDEC standards and it may be desirable, in some embodiments, to exactly simulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals that a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals. For example, the JEDEC specification for a DDR2 DRAM is known as JESD79-2B.

[0072] If it is desired, for example, to determine whether a JEDEC standard is met, the following algorithm may be used. Such algorithm checks, using a set of software verification tools for formal verification of logic, that protocol behavior of the simulated DRAM circuit is the same as a desired standard or other design specification. This formal verification is quite feasible because the DRAM protocol described in a DRAM standard is typically limited to a few control signals (e.g. approximately 15 control signals in the case of the JEDEC DDR2 specification, for example).

[0073] Examples of the aforementioned software verification tools include MAGELLAN supplied by SYNOPSYS, or other software verification tools, such as INCISIVE supplied by CADENCE, verification tools supplied by JASPER, VERIX supplied by REAL INTENT, 0-IN supplied by MENTOR CORPORATION, and others. These software verification tools use written assertions that correspond to the rules established by the DRAM protocol and specification. These written assertions are further included in the code that forms the logic description for the buffer chip. By writing assertions that correspond to the desired behavior of the simulated DRAM circuit, a proof may be constructed that determines whether the desired design requirements are met. In this way, one may test various embodiments for compliance with a standard, multiple standards, or other design specification.

[0074] For instance, an assertion may be written that no two DRAM control signals are allowed to be issued to an address, control and clock bus at the same time. Although one may know which of the various buffer chip/DRAM stack configurations and address mappings that have been described herein are suitable, the aforementioned algorithm may allow a designer to prove that the simulated DRAM circuit exactly meets the required standard or other design specification. If, for example, an address mapping that uses a common bus for data and a common bus for address results in a control and clock bus that does not meet a required specification, alternative designs for buffer chips with other bus arrangements or alternative designs for the interconnect between the buffer chips may be used and tested for compliance with the desired standard or other design specification.

[0075] FIG. **3** shows a high capacity DIMM **300** using buffered stacks of DRAM circuits **302**, in accordance with still yet another embodiment. As an option, the high capacity DIMM **300** may be implemented in the context of the architecture and environment of FIGS. **1** and/or **2**A-F. Of course, however, the high capacity DIMM **300** may be used in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0076] As shown, a high capacity DIMM **300** may be created utilizing buffered stacks of DRAM circuits **302**. Thus, a DIMM **300** may utilize a plurality of buffered stacks of DRAM circuits **302** instead of individual DRAM circuits, thus increasing the capacity of the DIMM. In addition, the DIMM **300** may include a register **304** for address and operation control of each of the buffered stacks of DRAM circuits **302**. It should be noted that any desired number of buffered stacks of DRAM circuits **302** may be utilized in conjunction with the DIMM **300**. Therefore, the configuration of the DIMM **300**, as shown, should not be construed as limiting in any way.

[0077] In an additional unillustrated embodiment, the register **304** may be substituted with an AMB (not shown), in the context of an FB-DIMM.

[0078] FIG. **4** shows a timing design **400** of a buffer chip that makes a buffered stack of DRAM circuits mimic longer CAS latency DRAM to a memory controller, in accordance with another embodiment. As an option, the design of the buffer chip may be implemented in the context of the architecture and environment of FIGS. **1-3**. Of course, however, the design of the buffer chip may be used in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0079] In use, any delay through a buffer chip (e.g. see the buffer chip **202** of FIGS. **2**A-E, etc.) may be made transparent to a memory controller of a host system (e.g. see the

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host system **204** of FIGS. **2**A-E, etc.) utilizing the buffer chip. In particular, the buffer chip may buffer a stack of DRAM circuits such that the buffered stack of DRAM circuits appears as at least one larger capacity DRAM circuit with higher CAS latency.

[0080] Such delay may be a result of the buffer chip being located electrically between the memory bus of the host system and the stacked DRAM circuits, since most or all of the signals that connect the memory bus to the DRAM circuits pass through the buffer chip. A finite amount of time may therefore be needed for these signals to traverse through the buffer chip. With the exception of register chips and advanced memory buffers (AMB), industry standard protocols for memory [e.g. (DDR SDRAM), DDR2 SDRAM, etc.] may not comprehend the buffer chip that sits between the memory bus and the DRAM. Industry standard protocols for memory [e.g. (DDR SDRAM), DDR2 SDRAM, etc.] narrowly define the properties of chips that sit between host and memory circuits. Such industry standard protocols define the properties of a register chip and AMB but not the properties of the buffer chip **202**, etc. Thus, the signal delay through the buffer chip may violate the specifications of industry standard protocols.

[0081] In one embodiment, the buffer chip may provide a one-half clock cycle delay between the buffer chip receiving address and control signals from the memory controller (or optionally from a register chip, an AMB, etc.) and the address and control signals being valid at the inputs of the stacked DRAM circuits. Similarly, the data signals may also have a one-half clock cycle delay in traversing the buffer chip, either from the memory controller to the DRAM circuits or from the DRAM circuits to the memory controller. Of course, the one-half clock cycle delay set forth above is set forth for illustrative purposes only and thus should not be construed as limiting in any manner whatsoever. For example, other embodiments are contemplated where a one clock cycle delay, a multiple clock cycle delay (or fraction thereof), and/or any other delay amount is incorporated, for that matter. As mentioned earlier, in other embodiments, the aforementioned delay may be coordinated among multiple signals such that different signals are subject to time-shifting with different relative directions/magnitudes, in an organized fashion.

[0082] As shown in FIG. **4**, the cumulative delay through the buffer chip (e.g. the sum of a first delay **402** of the address and control signals through the buffer chip and a second delay **404** of the data signals through the buffer chip) is j clock cycles. Thus, the buffer chip may make the buffered stack appear to the memory controller as one or more larger DRAM circuits with a CAS latency **408** of i+j clocks, where i is the native CAS latency of the DRAM circuits.

[0083] In one example, if the DRAM circuits in the stack have a native CAS latency of 4 and the address and control signals along with the data signals experience a one-half clock cycle delay though the buffer chip, then the buffer chip may make the buffered stack appear to the memory controller as one or more larger DRAM circuits with a CAS latency of 5 (i.e. 4+1). In another example, if the address and control signals along with the data signals experience a 1 clock cycle delay through the buffer chip, then the buffer chip may make the buffered stack appear as one or more larger DRAM circuits with a CAS latency of 6 (i.e. 4+2).

[0084] FIG. **5** shows the write data timing **500** expected by a DRAM circuit in a buffered stack, in accordance with yet another embodiment. As an option, the write data timing **500** may be implemented in the context of the architecture and environment of FIGS. **1-4**. Of course, however, the write data timing **500** may be carried out in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0085] Designing a buffer chip (e.g. see the buffer chip **202** of FIGS. **2**A-E, etc.) so that a buffered stack appears as at least one larger capacity DRAM circuit with higher CAS latency may, in some embodiments, create a problem with the timing of write operations. For example, with respect to a buffered stack of DDR2 SDRAM circuits with a CAS latency of 4 that appear as a single larger DDR2 SDRAM with a CAS latency of 6 to the memory controller, the DDR2 SDRAM protocol may specify that the write CAS latency is one less than the read CAS latency. Therefore, since the buffered stack appears as a DDR2 SDRAM with a read CAS latency of 6, the memory controller may use a write CAS latency of 5 (see **502**) when scheduling a write operation to the buffered stack.

[0086] However, since the native read CAS latency of the DRAM circuits is 4, the DRAM circuits may require a write CAS latency of 3 (see **504**). As a result, the write data from the memory controller may arrive at the buffer chip later than when the DRAM circuits require the data. Thus, the buffer chip may delay such write operations to alleviate any of such timing problems. Such delay in write operations will be described in more detail with respect to FIG. **6** below.

[0087] FIG. **6** shows write operations **600** delayed by a buffer chip, in accordance with still yet another embodiment. As an option, the write operations **600** may be implemented in the context of the architecture and environment of FIGS. **1-5**. Of course, however, the write operations **600** may be used in any desired environment. Again, it should also be noted that the aforementioned definitions may apply during the present description.

[0088] In order to be compliant with the protocol utilized by the DRAM circuits in the stack, a buffer chip (e.g. see the buffer chip **202** of FIGS. **2**A-E, etc.) may provide an additional delay, over and beyond the delay of the address and control signals through the buffer chip, between receiving the write operation and address from the memory controller (and/or optionally from a register and/or AMB, etc.), and sending it to the DRAM circuits in the stack. The additional delay may be equal to j clocks, where j is the cumulative delay of the address and control signals through the buffer chip and the delay of the data signals through the buffer chip. As another option, the write address and operation may be delayed by a register chip on a DIMM, by a AMB, or by the memory controller.

[0089] FIG. **7** shows early write data **700** from an AMB, in accordance with another embodiment. As an option, the early write data **700** may be implemented in the context of the architecture and environment of FIGS. **1-5**. Of course, however, the early write data **700** may be used in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0090] As shown, an AMB on an FB-DIMM may be designed to send write data earlier to buffered stacks instead of delaying the write address and operation, as described in reference to FIG. **6**. Specifically, an early write latency **702** may be utilized to send the write data to the buffered stack.

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Thus, correct timing of the write operation at the inputs of the DRAM circuits in the stack may be ensured.

[0091] For example, a buffer chip (e.g. see the buffer chip **202** of FIGS. **2**A-E, etc.) may have a cumulative latency of 2, in which case, the AMB may send the write data 2 clock cycles earlier to the buffered stack. It should be noted that this scheme may not be possible in the case of registered DIMMs since the memory controller sends the write data directly to the buffered stacks. As an option, a memory controller may be designed to send write data earlier so that write operations have the correct timing at the input of the DRAM circuits in the stack without requiring the buffer chip to delay the write address and operation.

[0092] FIG. **8** shows address bus conflicts **800** caused by delayed write operations, in accordance with yet another embodiment. As mentioned earlier, the delaying of the write addresses and operations may be performed by a buffer chip, or optionally a register, AMB, etc., in a manner that is completely transparent to the memory controller of a host system. However, since the memory controller is unaware of this delay, it may schedule subsequent operations, such as for example activate or precharge operations, which may collide with the delayed writes on the address bus from the buffer chip to the DRAM circuits in the stack. As shown, an activate operation **802** may interfere with a write operation **804** that has been delayed. Thus, a delay of activate operations may be employed, as will be described in further detail with respect to FIG. **9**.

[0093] FIGS. **9**A-B show variable delays **900** and **950** of operations through a buffer chip, in accordance with another embodiment. As an option, the variable delays **900** and **950** may be implemented in the context of the architecture and environment of FIGS. **1-8**. Of course, however, the variable delays **900** and **950** may be carried out in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0094] In order to prevent conflicts on an address bus between the buffer chip and its associated stack(s), either the write operation or the precharge/activate operation may be delayed. As shown, a buffer chip (e.g. see the buffer chip **202** of FIGS. **2**A-E, etc.) may delay the precharge/activate operations **952**A-C/**902**A-C. In particular, the buffer chip may make the buffered stack appear as one or more larger capacity DRAM circuits that have longer tRCD (RAS to CAS delay) and tRP (i.e. precharge time) parameters.

[0095] For example, if the cumulative latency through a buffer chip is 2 clock cycles while the native read CAS latency of the DRAM circuits is 4 clock cycles, then in order to hide the delay of the address/control signals and the data signals through the buffer chip, the buffered stack may appear as one or more larger capacity DRAM circuits with a read CAS latency of 6 clock cycles to the memory controller. In addition, if the tRCD and tRP of the DRAM circuits is 4 clock cycles each, the buffered stack may appear as one or more larger capacity DRAM circuits with tRCD of 6 clock cycles and tRP of 6 clock cycles in order to allow a buffer chip (e.g., see the buffer chip **202** of FIGS. **2**A-E, etc.) to delay the activate and precharge operations in a manner that is transparent to the memory controller. Specifically, a buffered stack that uses **4-4-4** DRAM circuits (i.e. CAS latency=4, tRCD=4, tRP=4) may appear as one or at least one larger capacity DRAM circuits with 6-6-6 timing (i.e. CAS latency=6, tRCD=6, tRP=6).

[0096] Since the buffered stack appears to the memory controller as having a tRCD of 6 clock cycles, the memory controller may schedule a column operation to a bank 6 clock cycles after an activate (e.g. row) operation to the same bank. However, the DRAM circuits in the stack may actually have a tRCD of 4 clock cycles. Thus, the buffer chip may have the ability to delay the activate operation by up to 2 clock cycles in order to avoid any conflicts on the address bus between the buffer chip and the DRAM circuits in the stack while still ensuring correct read and write timing on the channel between the memory controller and the buffered stack.

[0097] As shown, the buffer chip may issue the activate operation to the DRAM circuits one, two, or three clock cycles after it receives the activate operation from the memory controller, register, or AMB. The actual delay of the activate operation through the buffer chip may depend on the presence or absence of other DRAM operations that may conflict with the activate operation, and may optionally change from one activate operation to another.

[0098] Similarly, since the buffered stack may appear to the memory controller as at least one larger capacity DRAM circuit with a tRP of 6 clock cycles, the memory controller may schedule a subsequent activate (e.g. row) operation to a bank a minimum of 6 clock cycles after issuing a precharge operation to that bank. However, since the DRAM circuits in the stack actually have a tRP of 4 clock cycles, the buffer chip may have the ability to delay issuing the precharge operation to the DRAM circuits in the stack by up to 2 clock cycles in order to avoid any conflicts on the address bus between the buffer chip and the DRAM circuits in the stack. In addition, even if thee are no conflicts on the address bus, the buffer chip may still delay issuing a precharge operation in order to satisfy the tRAS requirement of the DRAM circuits.

[0099] In particular, if the activate operation to a bank was delayed to avoid an address bus conflict, then the precharge operation to the same bank may be delayed by the buffer chip to satisfy the tRAS requirement of the DRAM circuits. The buffer chip may issue the precharge operation to the DRAM circuits one, two, or three clock cycles after it receives the precharge operation from the memory controller, register, or AMB. The actual delay of the precharge operation through the buffer chip may depend on the presence or absence of address bus conflicts or tRAS violations, and may change from one precharge operation to another.

[0100] FIG. **10** shows a buffered stack **1000** of four 512 Mb DRAM circuits mapped to a single 2 Gb DRAM circuit, in accordance with yet another embodiment. As an option, the buffered stack **1000** may be implemented in the context of the architecture and environment of FIGS. **1-9**. Of course, however, the buffered stack **1000** may be carried out in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0101] The multiple DRAM circuits **1002**A-D buffered in the stack by the buffer chip **1004** may appear as at least one larger capacity DRAM circuit to the memory controller. However, the combined power dissipation of such DRAM circuits **1002**A-D may be much higher than the power dissipation of a monolithic DRAM of the same capacity. For example, the buffered stack may consist of four 512 Mb DDR2 SDRAM circuits that appear to the memory controller as a single 2 Gb DDR2 SDRAM circuit.

[0102] The power dissipation of all four DRAM circuits **1002**A-D in the stack may be much higher than the power dissipation of a monolithic 2 Gb DDR2 SDRAM. As a result, a DIMM containing multiple buffered stacks may dissipate much more power than a standard DIMM built using monolithic DRAM circuits. This increased power dissipation may limit the widespread adoption of DIMMs that use buffered stacks.

[0103] Thus, a power management technique that reduces the power dissipation of DIMMs that contain buffered stacks of DRAM circuits may be utilized. Specifically, the DRAM circuits **1002**A-D may be opportunistically placed in a precharge power down mode using the clock enable (CKE) pin of the DRAM circuits **1002**A-D. For example, a single rank registered DIMM (R-DIMM) may contain a plurality of buffered stacks of DRAM circuits **1002**A-D, where each stack consists of four ×4 512 Mb DDR2 SDRAM circuits **1002**A-D and appears as a single ×4 2 Gb DDR2 SDRAM circuit to the memory controller. A 2 Gb DDR2 SDRAM may generally have eight banks as specified by JEDEC. Therefore, the buffer chip **1004** may map each 512 Mb DRAM circuit in the stack to two banks of the equivalent 2 Gb DRAM, as shown.

[0104] The memory controller of the host system may open and close pages in the banks of the DRAM circuits **1002**A-D based on the memory requests it receives from the rest of the system. In various embodiments, no more than one page may be able to be open in a bank at any given time. For example, with respect to FIG. **10**, since each DRAM circuit **1002**A-D in the stack is mapped to two banks of the equivalent larger DRAM, at any given time a DRAM circuit **1002**A-D may have two open pages, one open page, or no open pages. When a DRAM circuit **1002**A-D has no open pages, the power management scheme may place that DRAM circuit **1002**A-D in the precharge power down mode by de-asserting its CKE input.

[0105] The CKE inputs of the DRAM circuits **1002**A-D in a stack may be controlled by the buffer chip **1004**, by a chip on an R-DIMM, by an AMB on a FB-DIMM, or by the memory controller in order to implement the power management scheme described hereinabove. In one embodiment, this power management scheme may be particularly efficient when the memory controller implements a closed page policy.

[0106] Another optional power management scheme may include mapping a plurality of DRAM circuits to a single bank of the larger capacity DRAM seen by the memory controller. For example, a buffered stack of sixteen ×4 256 Mb DDR2 SDRAM circuits may appear to the memory controller as a single ×4 4 Gb DDR2 SDRAM circuit. Since a 4 Gb DDR2 SDRAM circuit is specified by JEDEC to have eight banks, each bank of the 4 Gb DDR2 SDRAM circuit may be 512 Mb. Thus, two of the 256 Mb DDR2 SDRAM circuits may be mapped by the buffer chip **1004** to a single bank of the equivalent 4 Gb DDR2 SDRAM circuit seen by the memory controller.

[0107] In this way, bank **0** of the 4 Gb DDR2 SDRAM circuit may be mapped by the buffer chip to two 256 Mb DDR2 SDRAM circuits (e.g. DRAM A and DRAM B) in the stack. However, since only one page can be open in a bank at any given time, only one of DRAM A or DRAM B may be in the active state at any given time. If the memory controller opens a page in DRAM A, then DRAM B may be placed in the precharge power down mode by de-asserting its CKE input. As another option, if the memory controller opens a page in DRAM B, DRAM A may be placed in the precharge power down mode by de-asserting its CKE input. This technique may ensure that if p DRAM circuits are mapped to a bank of the larger capacity DRAM circuit seen by the memory controller, then p-1 of the p DRAM circuits may continuously (e.g. always, etc.) be subjected to a power saving operation. The power saving operation may, for example, comprise operating in precharge power down mode except when refresh is required. Of course, power-savings may also occur in other embodiments without such continuity.

[0108] FIG. **11** illustrates a method **1100** for refreshing a plurality of memory circuits, in accordance with still yet another embodiment. As an option, the method **1100** may be implemented in the context of the architecture and environment of any one or more of FIGS. **1-10**. For example, the method **1100** may be carried out by the interface circuit **102** of FIG. **1**. Of course, however, the method **1100** may be carried out in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0109] As shown, a refresh control signal is received in operation **1102**. In one optional embodiment, such refresh control signal may, for example, be received from a memory controller, where such memory controller intends to refresh a simulated memory circuit(s).

[0110] In response to the receipt of such refresh control signal, a plurality of refresh control signals are sent to a plurality of the memory circuits (e.g. see the memory circuits **104**A, **104**B, **104**N of FIG. **1**, etc.), at different times. See operation **1104**. Such refresh control signals may or may not each include the refresh control signal of operation **1102** or an instantiation/copy thereof. Of course, in other embodiments, the refresh control signals may each include refresh control signals that are different in at least one aspect (e.g. format, content, etc.).

[0111] During use of still additional embodiments, at least one first refresh control signal may be sent to a first subset (e.g. of one or more) of the memory circuits at a first time and at least one second refresh control signal may be sent to a second subset (e.g. of one or more) of the memory circuits at a second time. Thus, in some embodiments, a single refresh control signal may be sent to a plurality of the memory circuits (e.g. a group of memory circuits, etc.). Further, a plurality of the refresh control signals may be sent to a plurality of the memory circuits. To this end, refresh control signals may be sent individually or to groups of memory circuits, as desired.

[0112] Thus, in still yet additional embodiments, the refresh control signals may be sent after a delay in accordance with a particular timing. In one embodiment, for example, the timing in which the refresh control signals are sent to the memory circuits may be selected to minimize a current draw. This may be accomplished in various embodiments by staggering a plurality of refresh control signals. In still other embodiments, the timing in which the refresh control signals are sent to the memory circuits may be selected to comply with a tRFC parameter associated with each of the memory circuits.

[0113] To this end, in the context of an example involving a plurality of DRAM circuits (e.g. see the embodiments of FIGS. **1-2**E, etc.), DRAM circuits of any desired size may receive periodic refresh operations to maintain the integrity

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of data therein. A memory controller may initiate refresh operations by issuing refresh control signals to the DRAM circuits with sufficient frequency to prevent any loss of data in the DRAM circuits. After a refresh control signal is issued to a DRAM circuit, a minimum time (e.g. denoted by tRFC) may be required to elapse before another control signal may be issued to that DRAM circuit. The tRFC parameter may therefore increase as the size of the DRAM circuit increases.

[0114] When the buffer chip receives a refresh control signal from the memory controller, it may refresh the smaller DRAM circuits within the span of time specified by the tRFC associated with the emulated DRAM circuit. Since the tRFC of the emulated DRAM circuits is larger than that of the smaller DRAM circuits, it may not be necessary to issue refresh control signals to all of the smaller DRAM circuits simultaneously. Refresh control signals may be issued separately to individual DRAM circuits or may be issued to groups of DRAM circuits, provided that the tRFC requirement of the smaller DRAM circuits is satisfied by the time the tRFC of the emulated DRAM circuits has elapsed. In use, the refreshes may be spaced to minimize the peak current draw of the combination buffer chip and DRAM circuit set during a refresh operation.

[0115] While various embodiments have been described above, it should be understood that they have been presented by way of example only, and not limitation. For example, any of the network elements may employ any of the desired functionality set forth hereinabove. Thus, the breadth and scope of a preferred embodiment should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A sub-system, comprising:

an interface circuit in communication with a plurality of memory circuits and a system, the interface circuit operable to interface the memory circuits and the system for simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of memory circuits;

wherein the at least one aspect is selected from the group consisting of a signal, a capacity, a timing, and a logical interface.

2. The sub-system of claim **1**, wherein the at least one aspect includes the signal.

3. The sub-system of claim **2**, wherein the signal is selected from the group consisting of an address signal, a control signal, and a data signal.

4. The sub-system of claim **1**, wherein the at least one aspect includes the capacity.

5. The sub-system of claim **4**, wherein the capacity includes a memory capacity.

6. The sub-system of claim **5**, wherein memory capacity relates to a number of the memory circuits.

7. The sub-system of claim **5**, wherein the interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with a first memory capacity that is greater than a second memory capacity of at least one of the plurality of memory circuits.

8. The sub-system of claim **1**, wherein the at least one aspect includes the timing.

9. The sub-system of claim **8**, wherein the timing relates to a latency.

10. The sub-system of claim **9**, wherein the latency includes a column address strobe (CAS) latency.

11. The sub-system of claim **10**, wherein the interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with a first CAS latency that is longer than a second CAS latency of at least one of the plurality of memory circuits.

12. The sub-system of claim **9**, wherein the latency includes a row address strobe (RAS) to CAS latency (tRCD).

13. The sub-system of claim **12**, wherein the interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with a first tRCD that is longer than a second tRCD of at least one of the plurality of memory circuits.

14. The sub-system of claim **9**, wherein the latency includes a row precharge latency (tRP).

15. The sub-system of claim **14**, wherein the interface circuit is operable to interface the memory circuits and the system for simulating at least one memory circuit with a first tRP that is longer than a second tRP of at least one of the plurality of memory circuits.

16. The sub-system of claim **9**, wherein the latency includes an activate to precharge latency (tRAS).

17. The sub-system of claim **1**, wherein the at least one aspect includes the logical interface.

18. The sub-system of claim **1**, wherein the memory circuits each include dynamic random access memory (DRAM).

19. A method, comprising:

interfacing a plurality of memory circuits and a system; and

simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of memory circuits;

wherein the at least one aspect is selected from the group consisting of a signal, a capacity, a timing, and a logical interface.

20. A sub-system, comprising:

an interface circuit in communication with a plurality of memory circuits and a system, the interface circuit operable to interface the memory circuits and the system for simulating at least one memory circuit with at least one aspect that is different from at least one aspect of at least one of the plurality of memory circuits;

wherein the interface circuit interfaces a majority of address or control signals of the memory circuits.

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US 20060233012A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0233012 A1**

Sekiguchi et al. (43) **Pub. Date: Oct. 19, 2006**

(54) **SEMICONDUCTOR STORAGE DEVICE HAVING A PLURALITY OF STACKED MEMORY CHIPS**

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(21) Appl. No.: **11/392,805**

(22) Filed: **Mar. 30, 2006**

(30) **Foreign Application Priority Data**

Mar. 30, 2005 (JP) 2005-098027

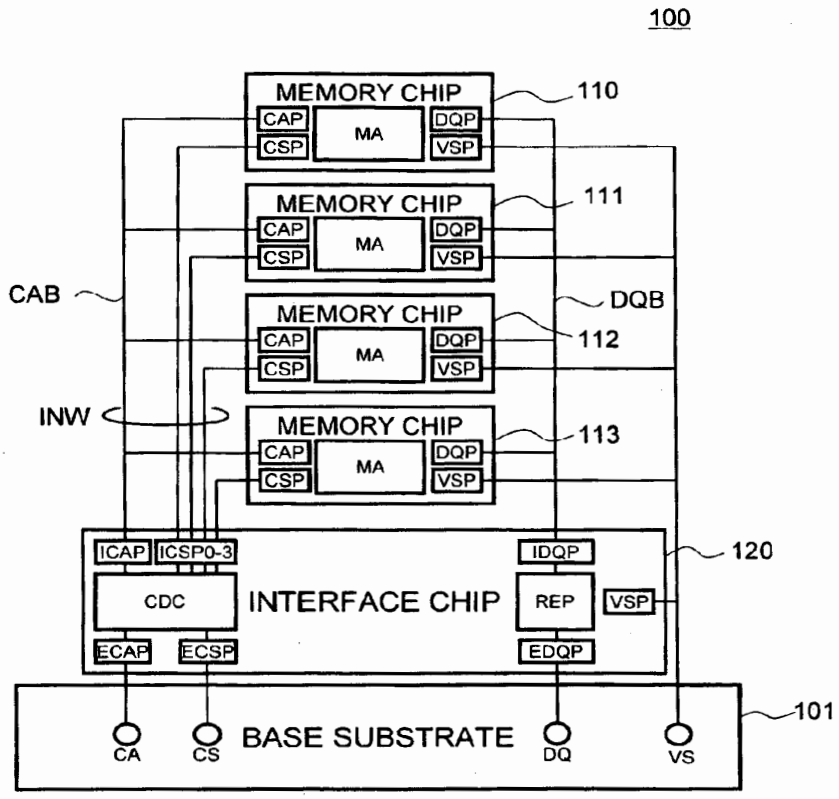
Publication Classification

(51) **Int. Cl.**
G11C 5/02 (2006.01)

(52) **U.S. Cl.** **365/51**

(57) **ABSTRACT**

A semiconductor storage employs a base substrate (**101**) having a command/address external terminal group (CA), a data input/output external terminal group (DQ), and a single chip select external terminal (CS), and also comprises a plurality of memory chips (**110**) to (**113**) mounted on a base substrate (**101**), each of which can individually carry out read and write operations. The terminals (CA), (DQ), and (CS) are connected to an interface chip (**120**). The interface chip (**120**) has a chip select signal generation circuit that can individually activate a plurality of memory chips (**110**) to (**113**) on the basis of an address signal fed by way of the terminal (CA) and on the basis of a chip select signal fed by way of the terminal (CS).



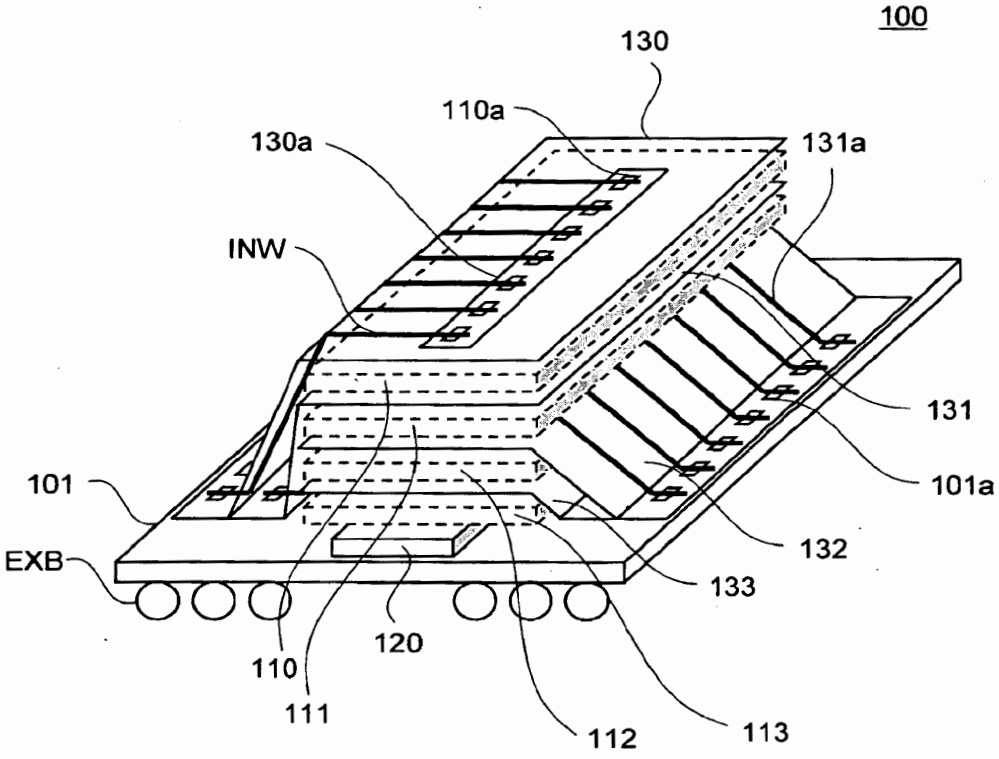

100
130
110a
130a
131a
INW
131
101a
101
132
EXB
133
120
110
111
112
113

FIG.1

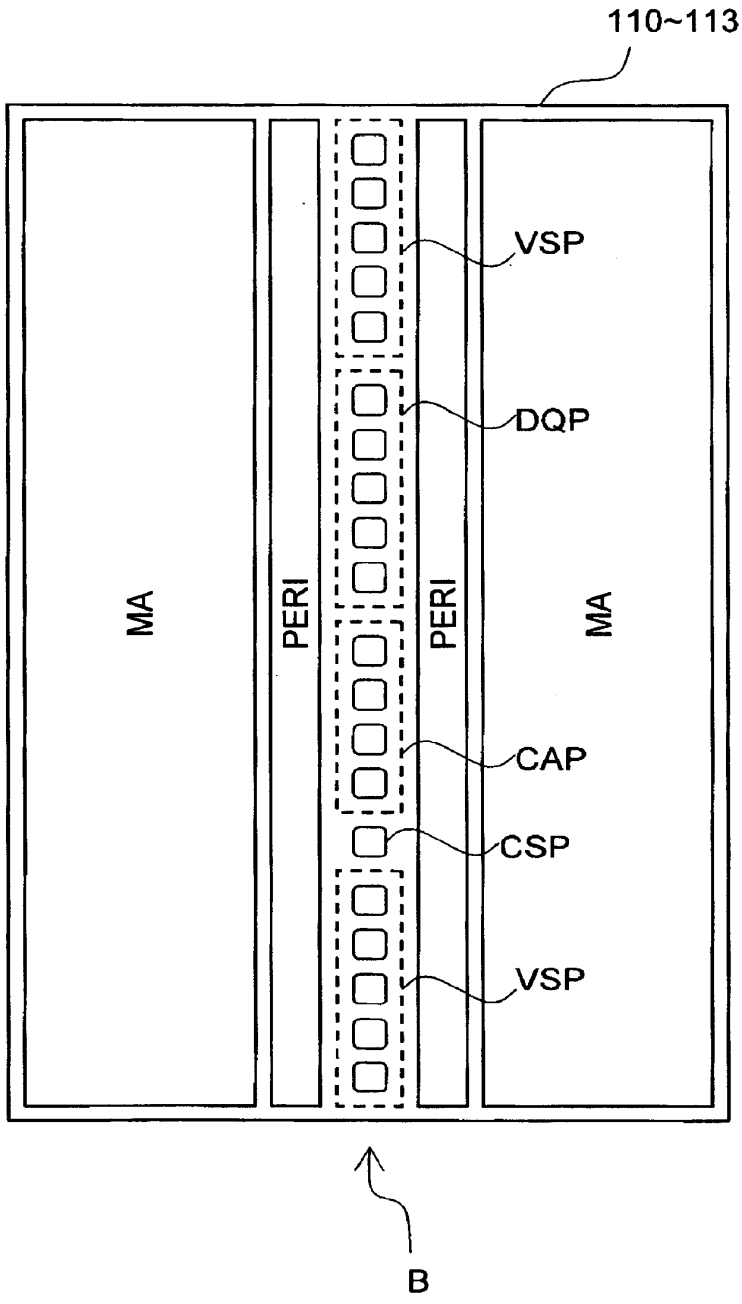


FIG.2

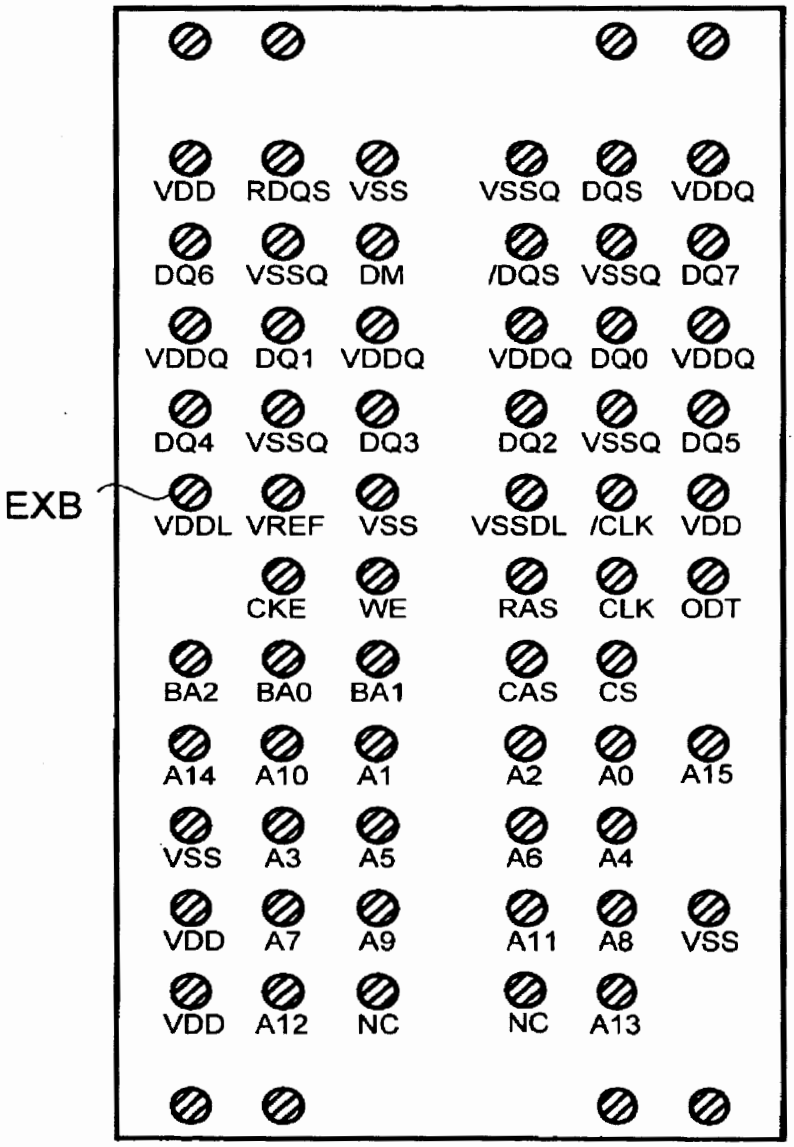

EXB
VDD RDQS VSS VSSQ DQS VDDQ
DQ6 VSSQ DM /DQS VSSQ DQ7
VDDQ DQ1 VDDQ VDDQ DQ0 VDDQ
DQ4 VSSQ DQ3 DQ2 VSSQ DQ5
VDDL VREF VSS VSSDL /CLK VDD
CKE WE RAS CLK ODT
BA2 BA0 BA1 CAS CS
A14 A10 A1 A2 A0 A15
VSS A3 A5 A6 A4
VDD A7 A9 A11 A8 VSS
VDD A12 NC NC A13

FIG.3

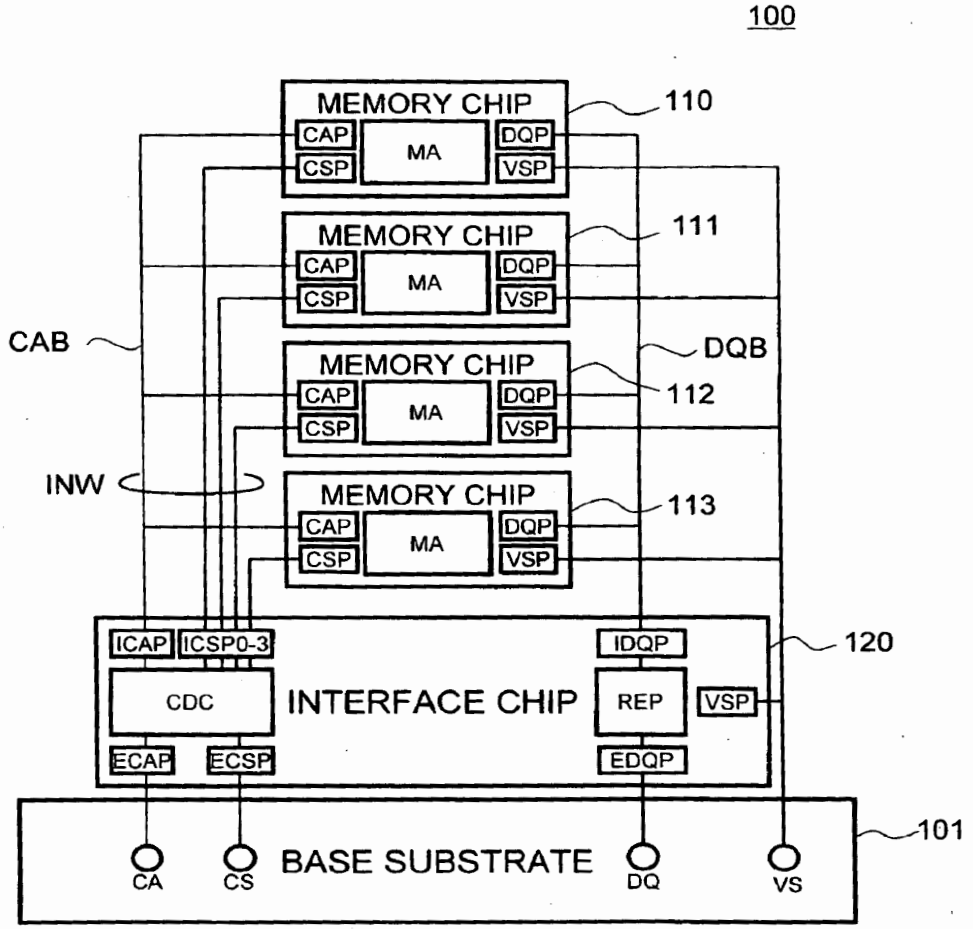


FIG.4

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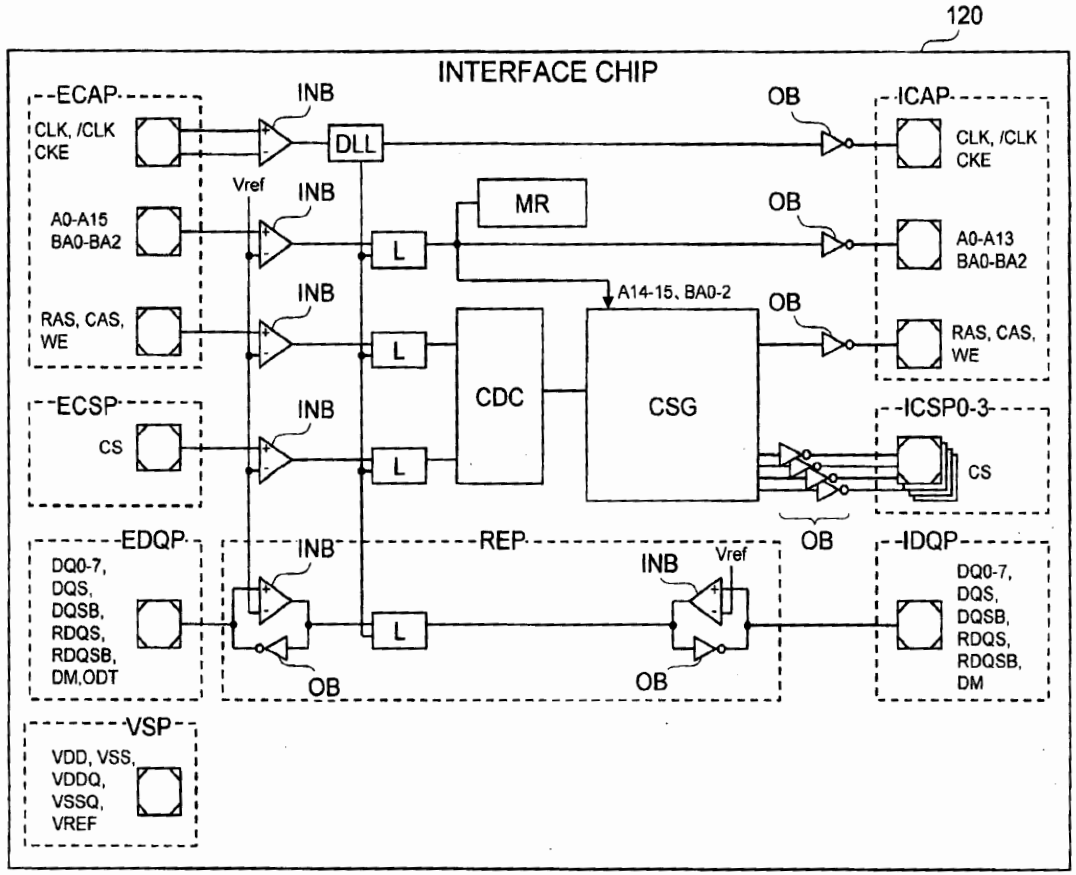
120
INTERFACE CHIP
ECAP
CLK, /CLK
CKE
A0-A15
BA0-BA2
RAS, CAS,
WE
ECSP
CS
EDQP
DQ0-7,
DQS,
DQSB,
RDQS,
RDQSB,
DM,ODT
VSP
VDD, VSS,
VDDQ,
VSSQ,
VREF
INB
Vref
DLL
MR
L
CDC
CSG
A14-15, BA0-2
OB
REP
ICAP
CLK, /CLK
CKE
A0-A13
BA0-BA2
RAS, CAS,
WE
ICSP0-3
CS
IDQP
DQ0-7,
DQS,
DQSB,
RDQS,
RDQSB,
DM

FIG.5

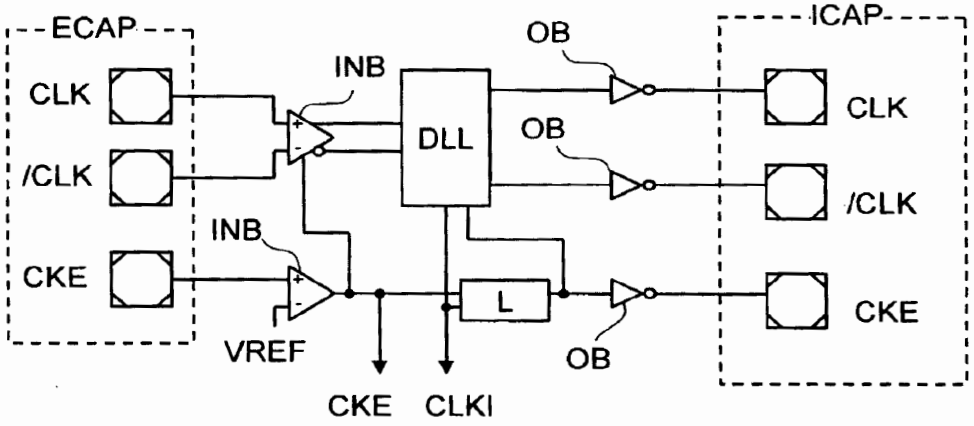

FIG.6

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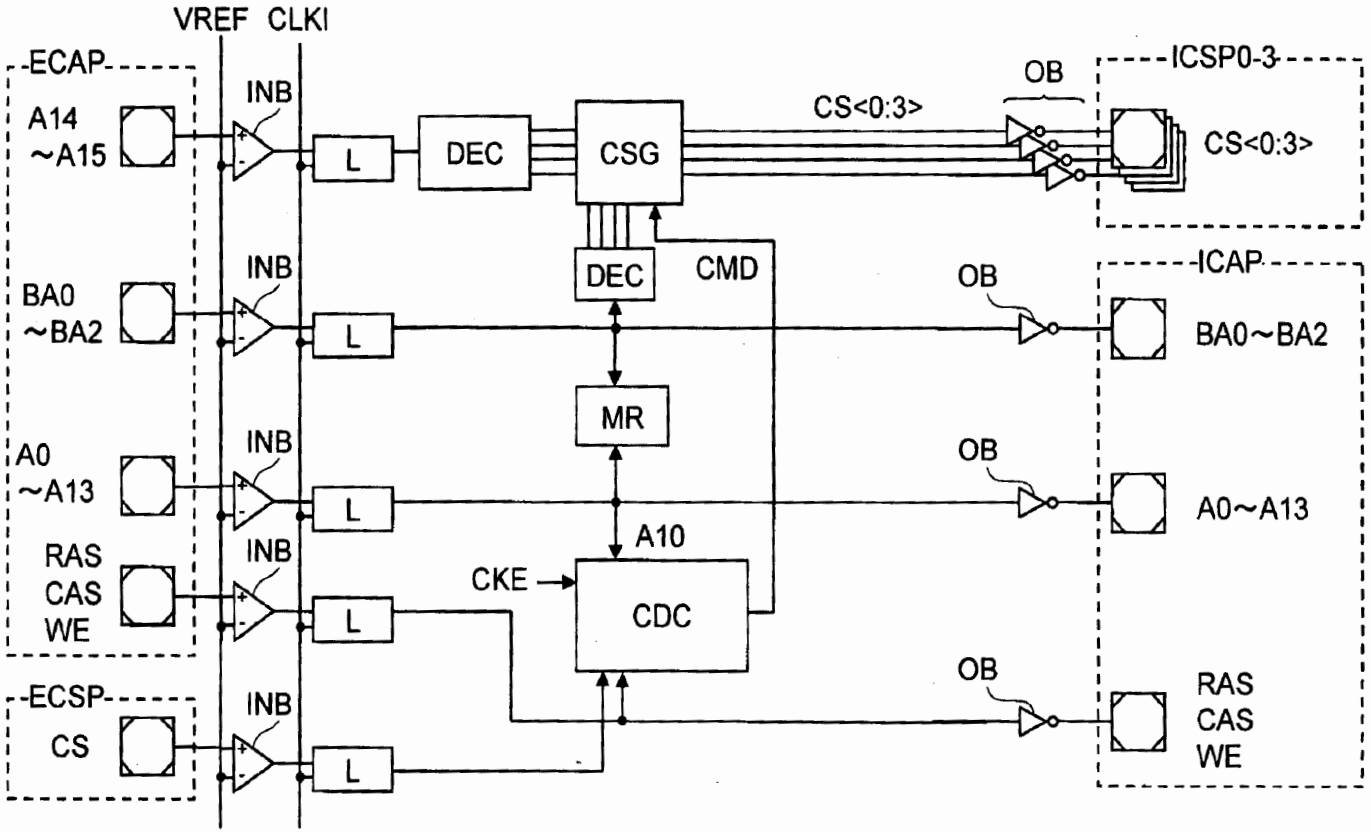
VREF
CLKI
ECAP
A14
~A15
BA0
~BA2
A0
~A13
RAS
CAS
WE
ECSP
CS
INB
L
DEC
CSG
CS<0:3>
OB
ICSP0-3
CS<0:3>
CMD
ICAP
BA0~BA2
MR
A0~A13
A10
CKE
CDC
RAS
CAS
WE

FIG.7

	COMMAND	SYMBOL	CS PUBLICATION METHOD
INITIALIZATION	Mode register set	MRS	Simultaneously activate all CS
	Extended mode register set	EMRS	
ROW SYSTEM	Auto refresh	REF	Sequentially activate with phase difference
	Self refresh entry	SELF	
	Self refresh exit	SELFX	Simultaneously activate all CS
	Single bank precharge	PRE	Activate CS stored in the active bank register
	Precharge all banks	PALL	
	Bank activate	ACT	Select CS by decoding A14, 15 and store in active bank register
COLUMN SYSTEM	Write	WRIT	Activate CS stored in the active bank register
	Write with auto precharge	WRITA	
	Read	READ	
	Read with auto precharge	READA	
OTHER	No operation	NOP	Simultaneously activate all CS
	Device deselect	DESL	
	Power down mode entry	PDEN	
	Power down mode exit	PDEX	

FIG.8

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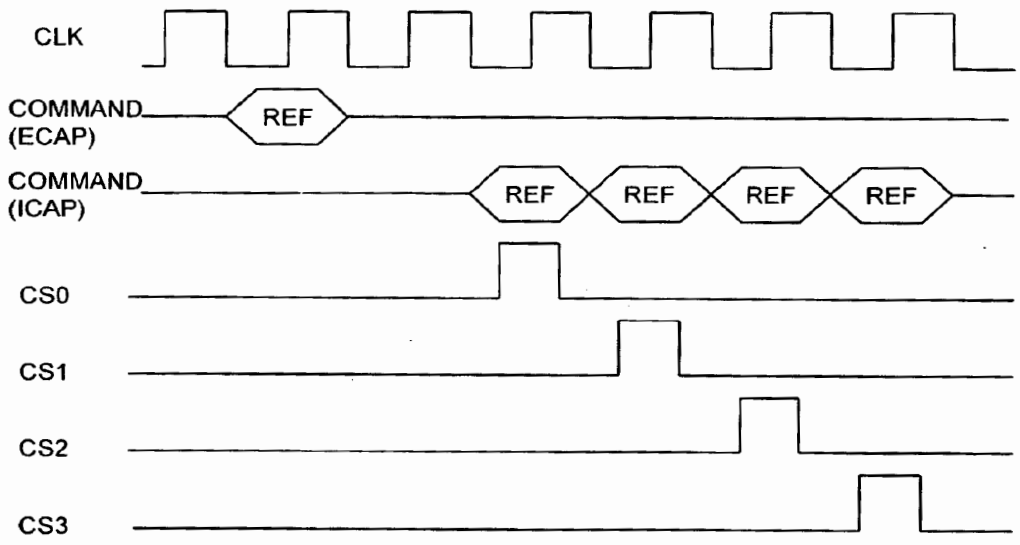
CLK
COMMAND (ECAP)
REF
COMMAND (ICAP)
REF
REF
REF
REF
CS0
CS1
CS2
CS3

FIG.9

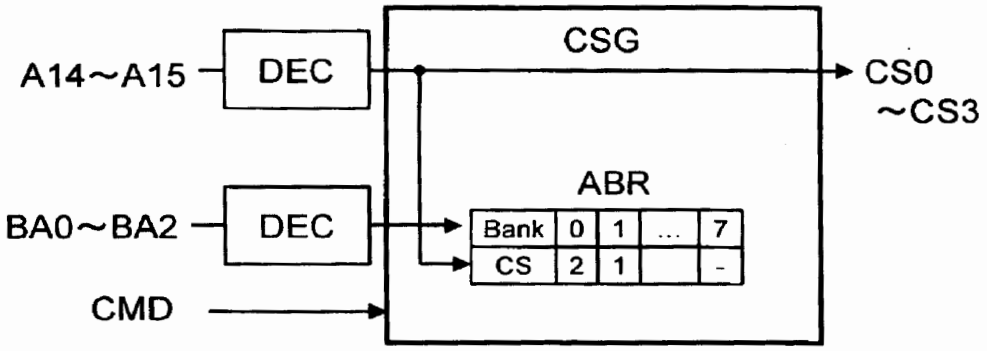

FIG.10A

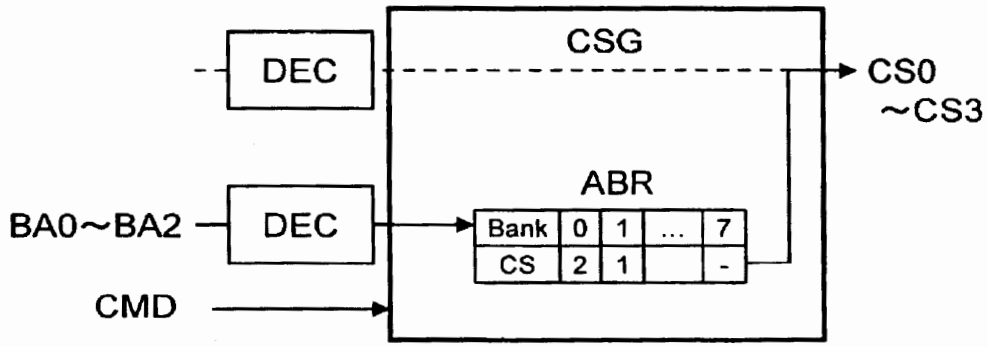

FIG.10B

FIG.11

IDQP
REP
EDQP
DM
DQ0 ~DQ7
/DQS
DQS
ODT
OB
INB
VREF
OBV
DQSI
DSG
L
RT
CLKI
ROV
VREF
RTV

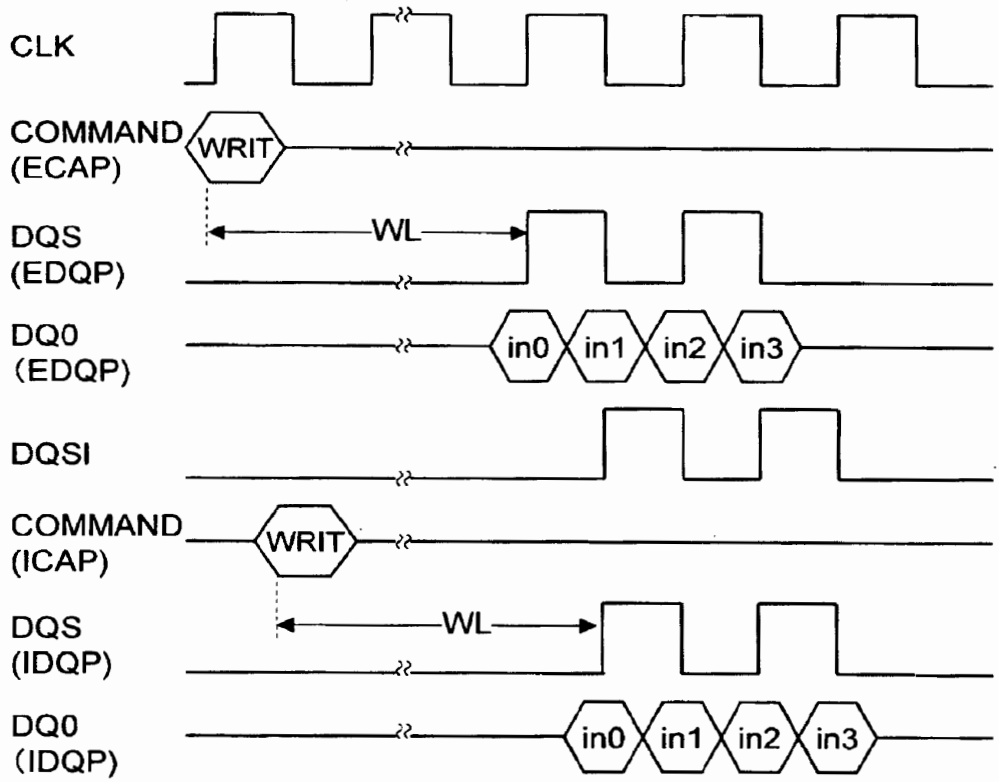
CLK
COMMAND
(ECAP)
WRIT
DQS
(EDQP)
WL
DQ0
(EDQP)
in0
in1
in2
in3
DQSI
COMMAND
(ICAP)
WRIT
DQS
(IDQP)
WL
DQ0
(IDQP)
in0
in1
in2
in3

FIG.12

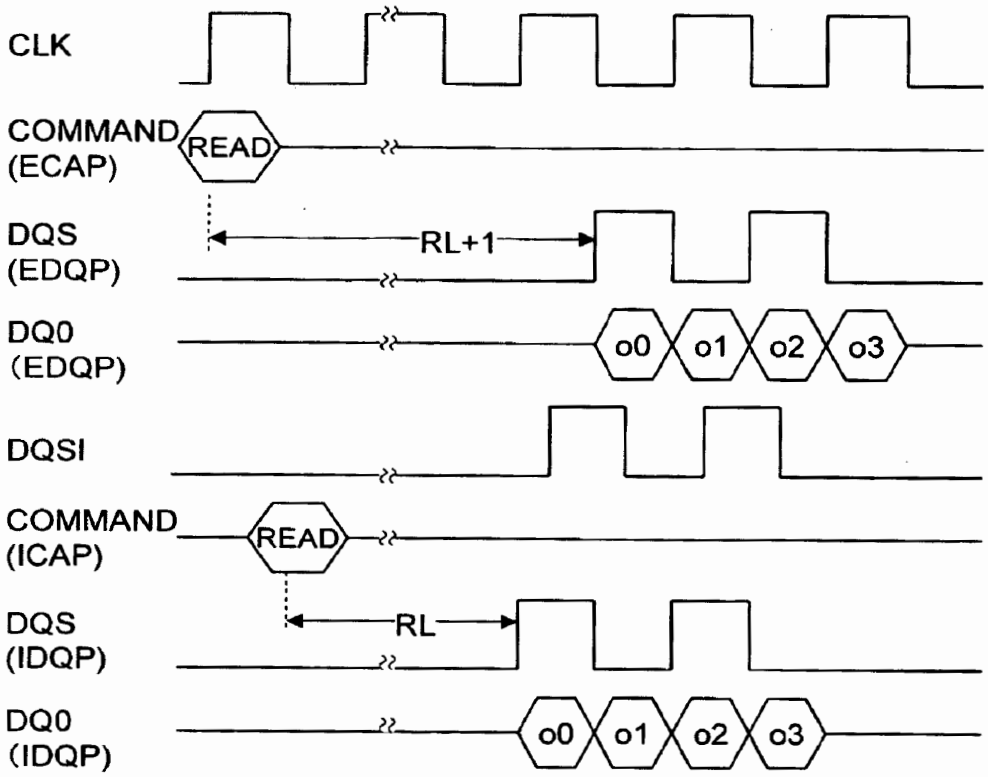
CLK
COMMAND
(ECAP)
READ
DQS
(EDQP)
RL+1
DQ0
(EDQP)
o0
o1
o2
o3
DQSI
COMMAND
(ICAP)
READ
DQS
(IDQP)
RL
DQ0
(IDQP)
o0
o1
o2
o3

FIG.13

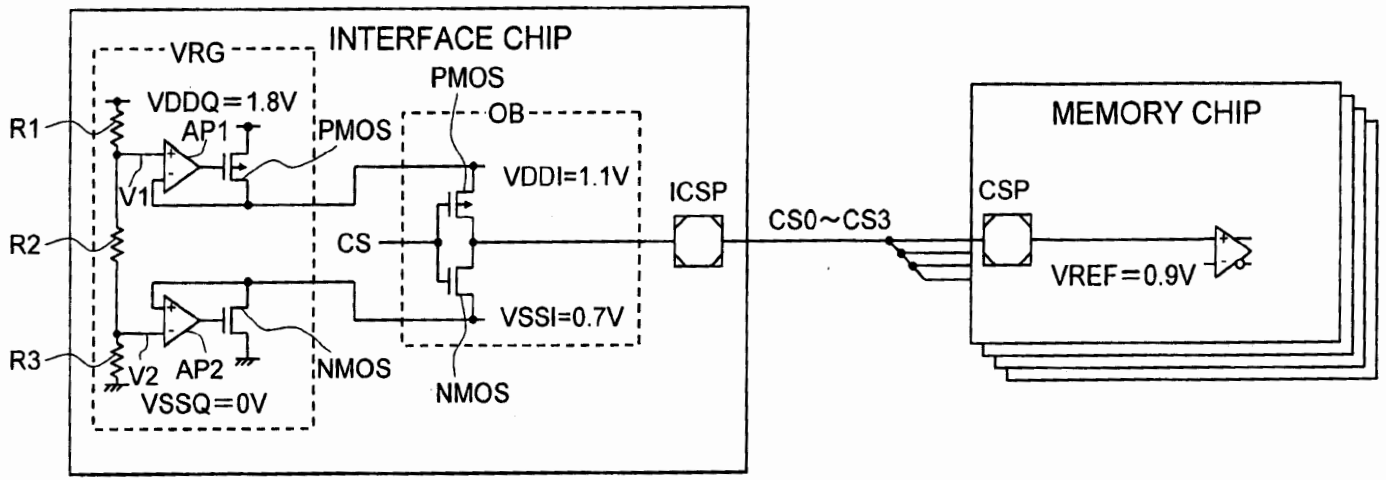

FIG.14

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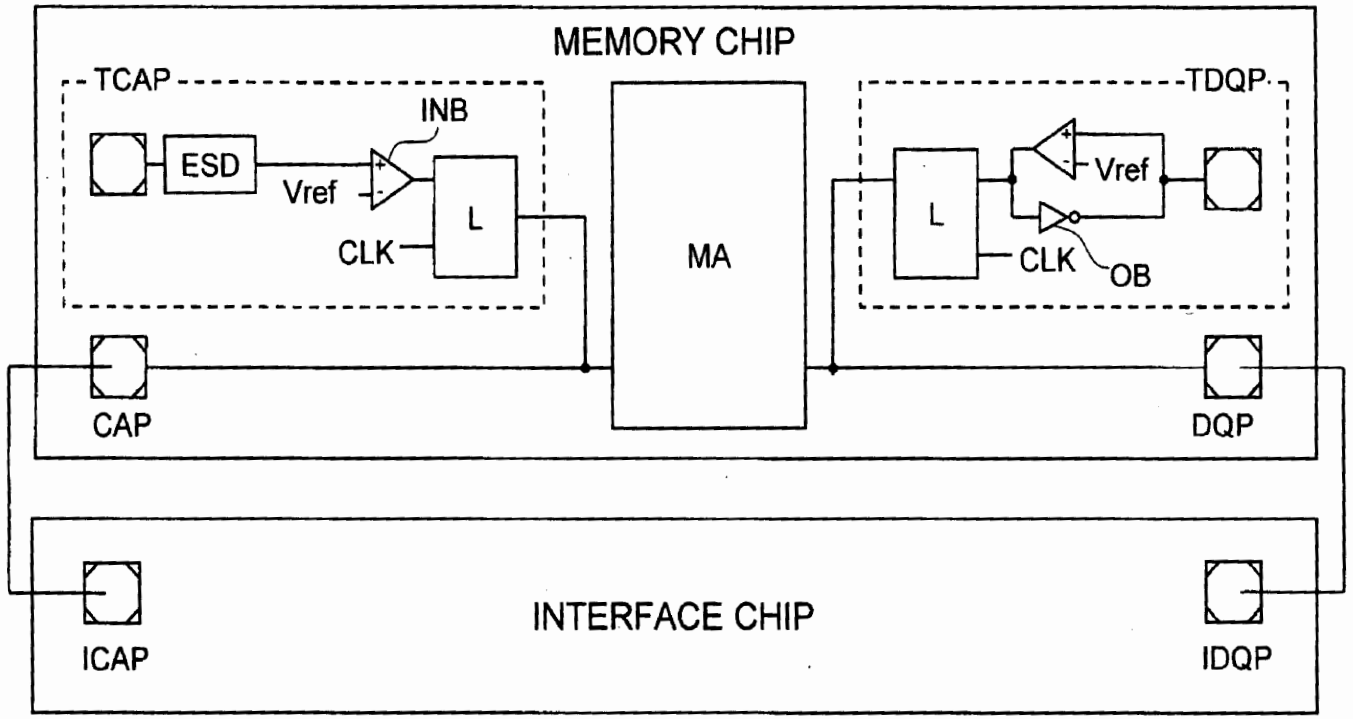
MEMORY CHIP
TCAP
INB
ESD
Vref
L
CLK
MA
TDQP
L
Vref
CLK
OB
CAP
DQP
ICAP
INTERFACE CHIP
IDQP

FIG.15

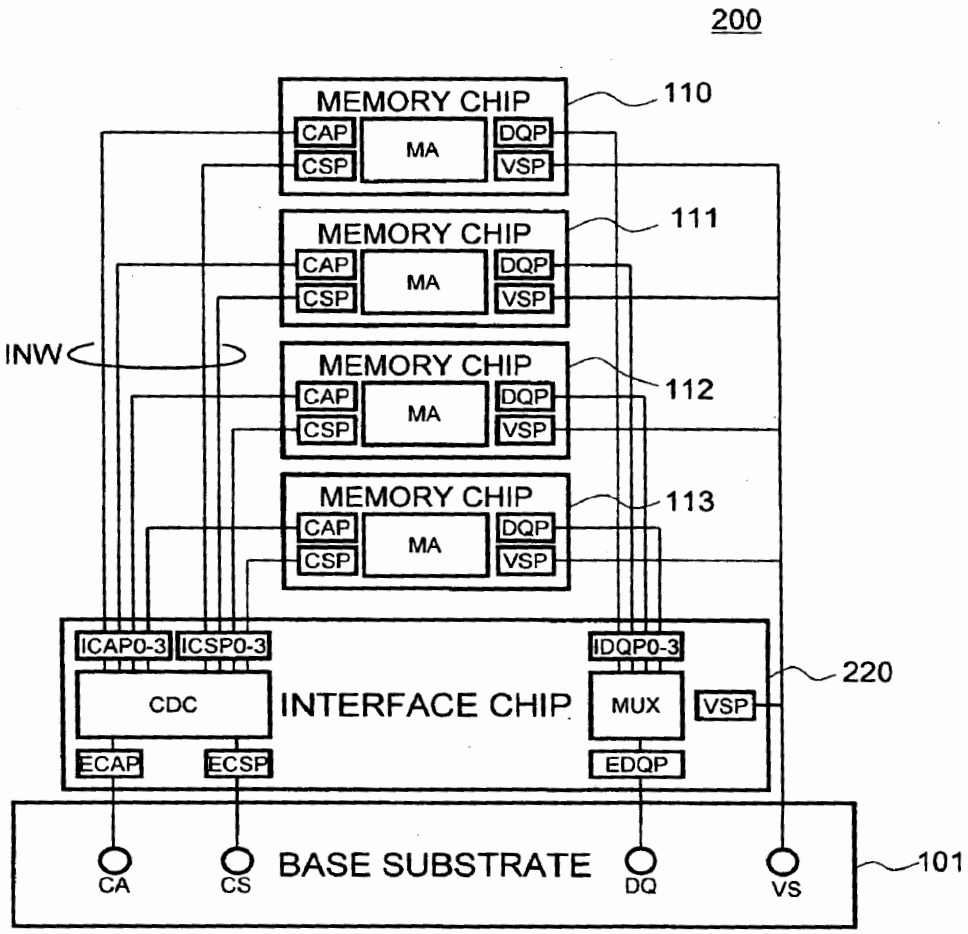

FIG.16

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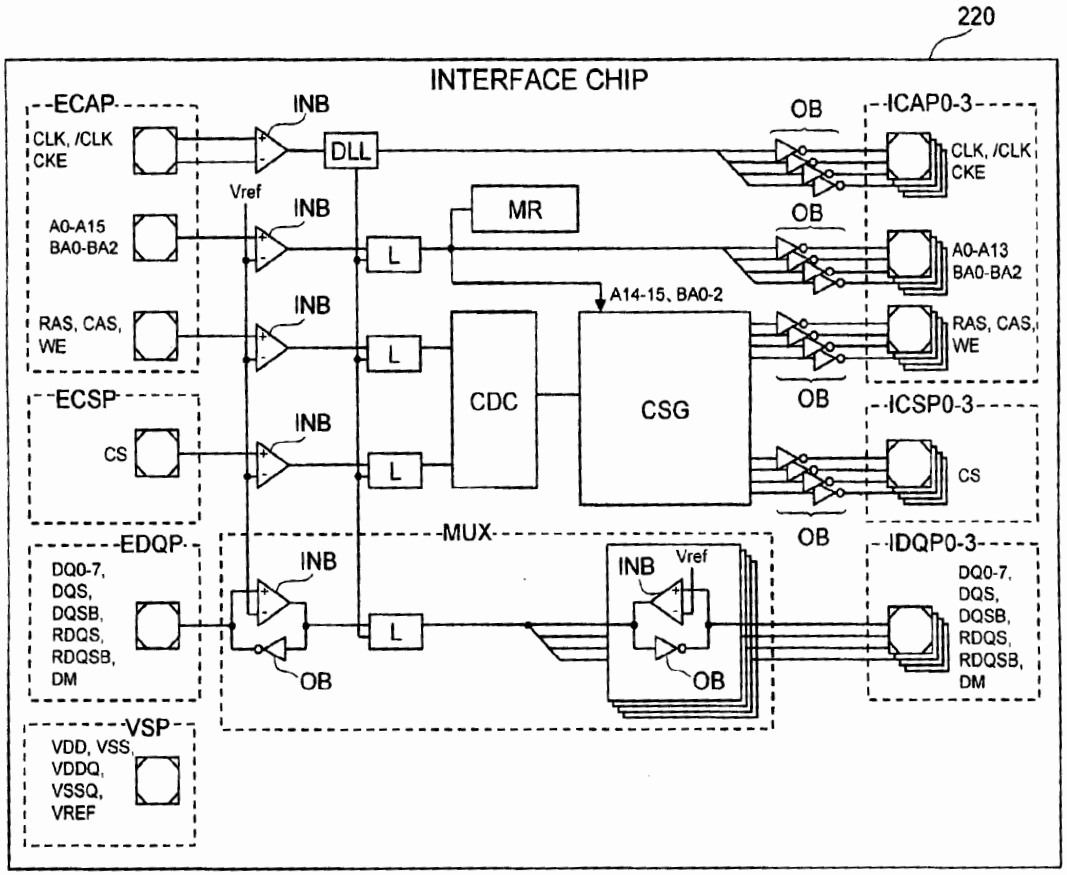
220
INTERFACE CHIP
ECAP
CLK, /CLK
CKE
A0-A15
BA0-BA2
RAS, CAS,
WE
ECSP
CS
EDQP
DQ0-7,
DQS,
DQSB,
RDQS,
RDQSB,
DM
VSP
VDD, VSS,
VDDQ,
VSSQ,
VREF
INB
Vref
DLL
MR
L
CDC
CSG
A14-15, BA0-2
MUX
OB
ICAP0-3
CLK, /CLK
CKE
A0-A13
BA0-BA2
RAS, CAS,
WE
ICSP0-3
CS
IDQP0-3
DQ0-7,
DQS,
DQSB,
RDQS,
RDQSB,
DM

FIG.17

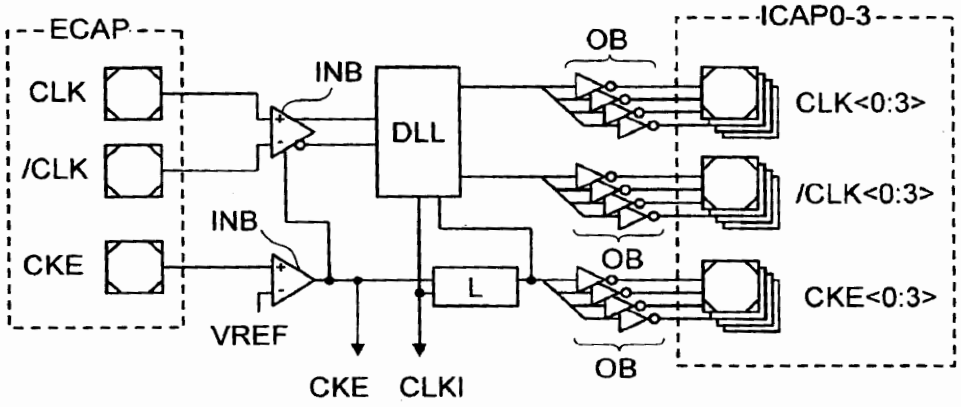

FIG.18

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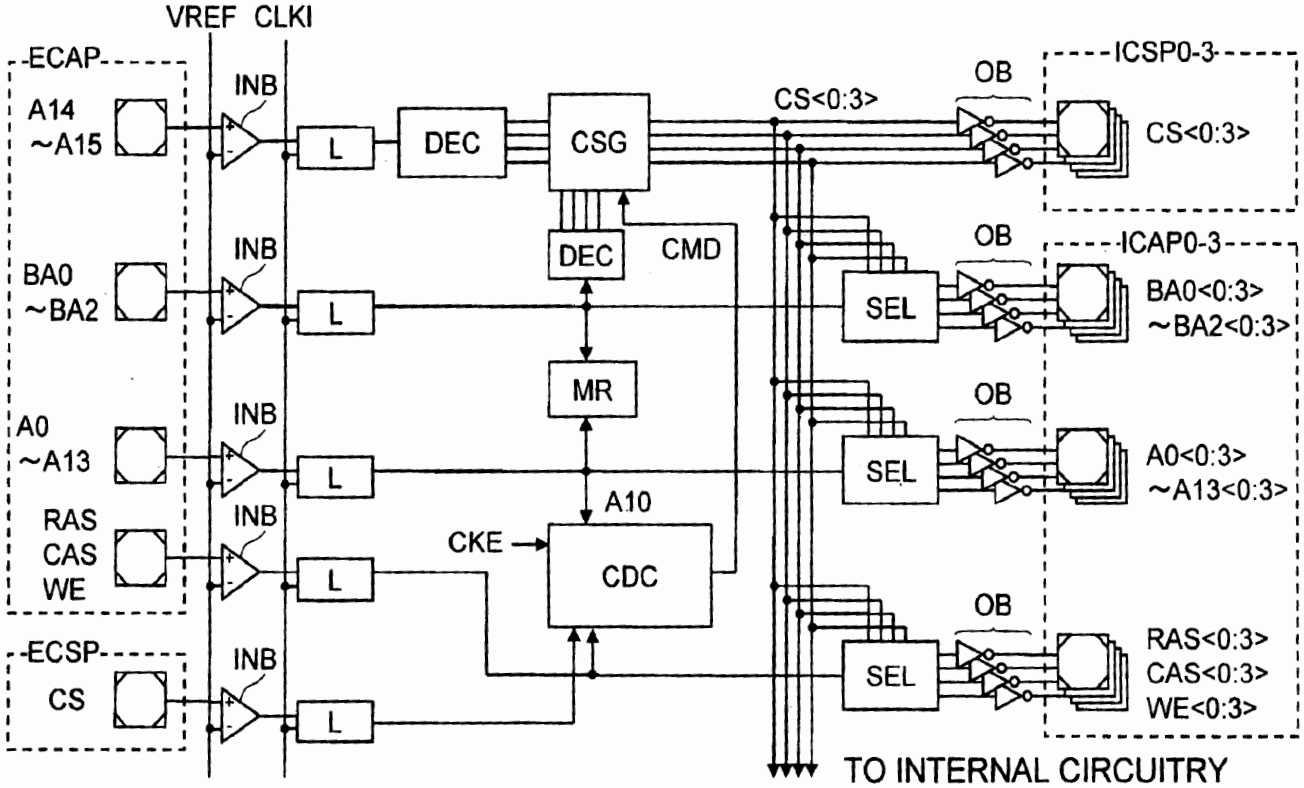

FIG.19

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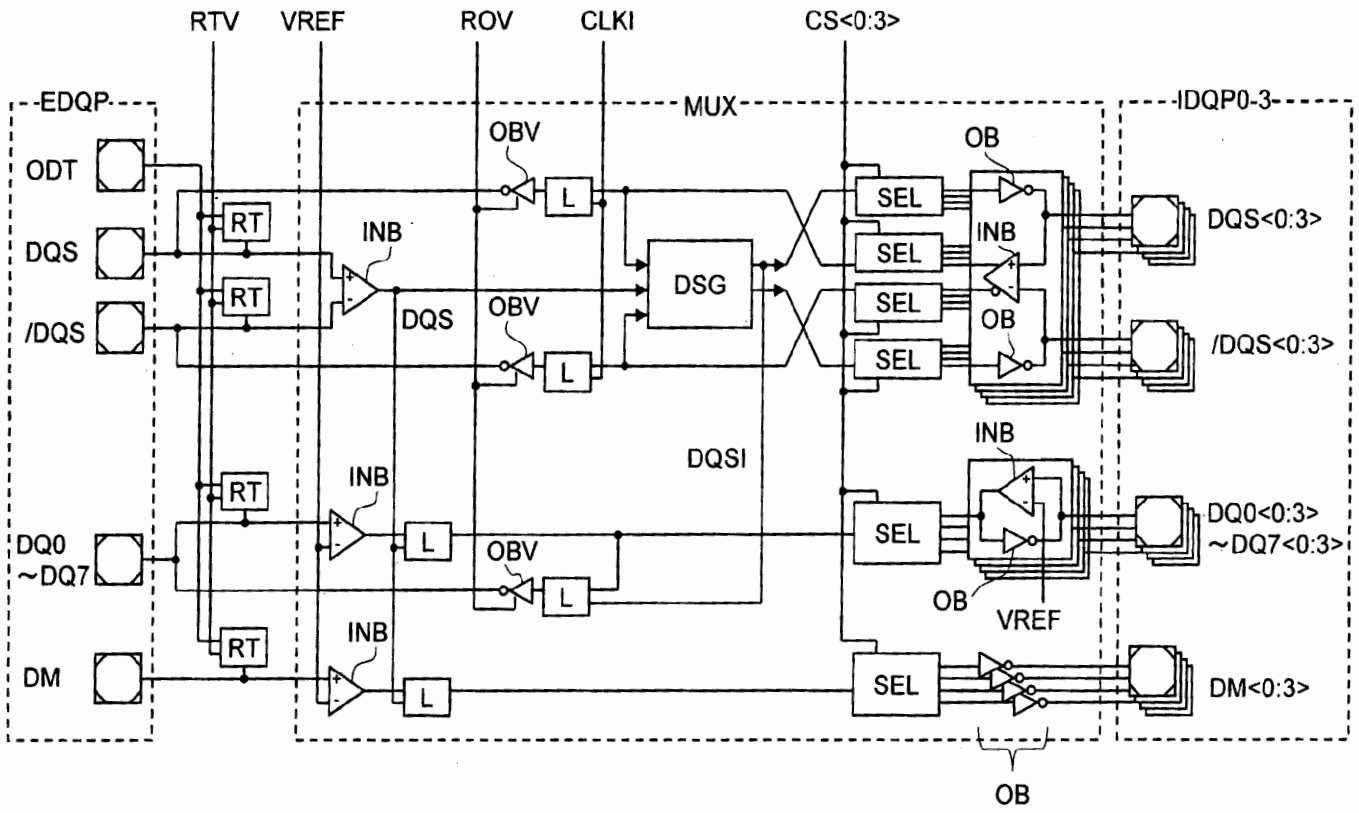
RTV
VREF
ROV
CLKI
CS<0:3>
EDQP
MUX
IDQP0-3
ODT
DQS
/DQS
DQ0
~DQ7
DM
RT
INB
OBV
L
DSG
DQS
DQSI
SEL
OB
DQS<0:3>
/DQS<0:3>
DQ0<0:3>
~DQ7<0:3>
DM<0:3>
VREF

FIG.20

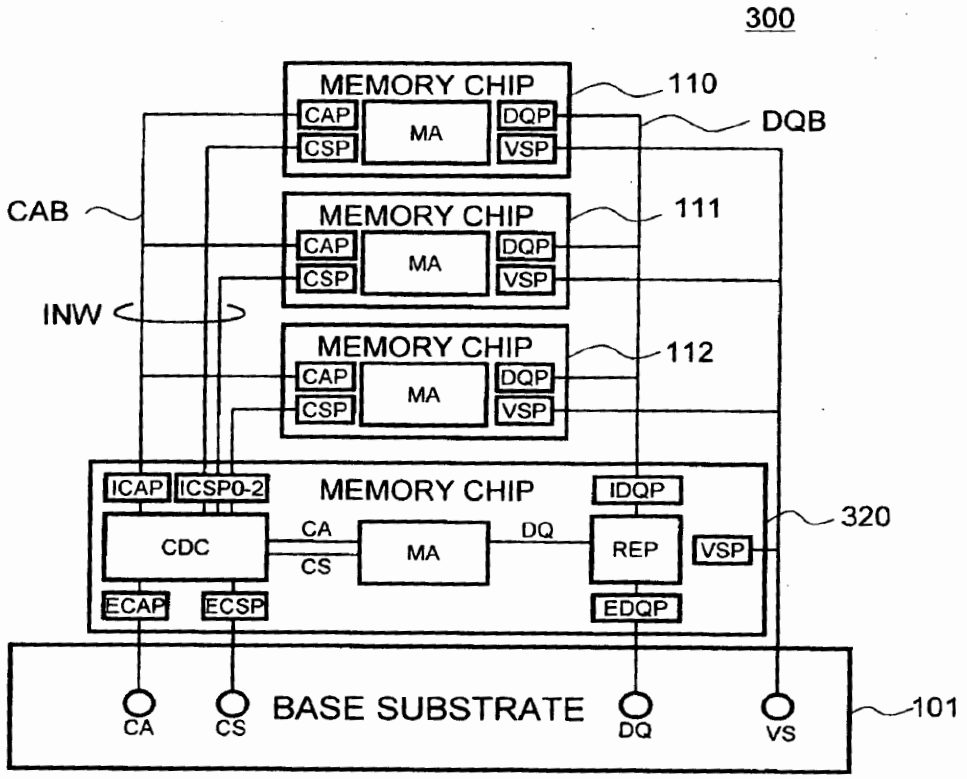
300
MEMORY CHIP
110
CAP
MA
DQP
CSP
VSP
DQB
CAB
MEMORY CHIP
111
INW
MEMORY CHIP
112
ICAP
ICSP0-2
MEMORY CHIP
IDQP
320
CDC
CA
CS
MA
DQ
REP
VSP
ECAP
ECSP
EDQP
BASE SUBSTRATE
101
CA
CS
DQ
VS

FIG.21

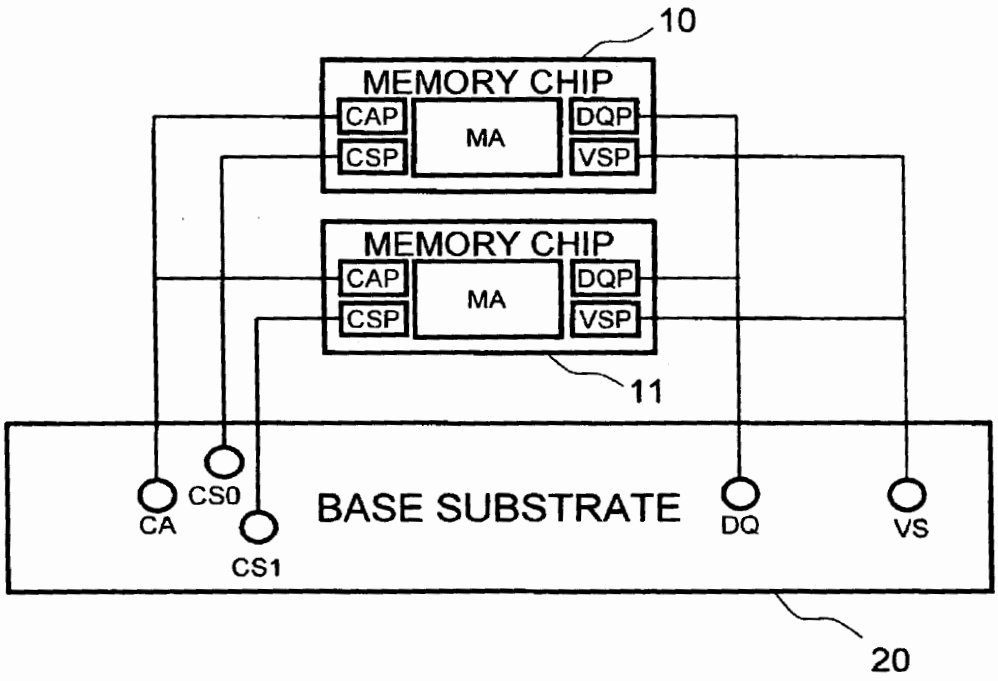

FIG.22

PRIOR ART

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SEMICONDUCTOR STORAGE DEVICE HAVING A PLURALITY OF STACKED MEMORY CHIPS

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor storage device, and more specifically relates to a semiconductor storage device that has a plurality of stacked memory chips.

BACKGROUND OF THE INVENTION

[0002] Semiconductor storage devices typified by DRAM (Dynamic Random Access Memory) are widely used as the main memory of servers and other computers, but with the increase in hardware speed and software complexity, the storage capacity required in main memory continues to increase. For this reason, it is difficult to meet the storage capacity needs required in main memory by using only a single memory chip, and a module referred as DIMM (Dual Inline Memory Module) in which a plurality of memory chips are mounted on a module substrate is ordinarily used.

[0003] However, the number of memory chips that can be mounted is low and the resulting storage capacity is limited when the memory chip is disposed in a flat configuration on a module substrate. Methods have been proposed in which a plurality of memory chips are three-dimensionally stacked and packaged, and the memory chips are mounted on a module substrate. See Japanese Patent Application Laid-Open Nos. H2-290048, 2001-110978, 2001-273755, and 2004-327474.

[0004] **FIG. 22** is a schematic diagram of a conventional semiconductor storage device that is three-dimensionally stacked and packaged. The semiconductor storage device shown in **FIG. 22** has a structure in which two memory chips **10** and **11** are stacked on the base substrate **20**, and the base substrate **20** is mounted on a module substrate (not shown). Each of the memory chips **10** and **11** has a memory array MA, a command/address pad CAP to which commands and addresses are supplied, a chip select signal pad CSP to which a chip select signal is supplied, a data input/output pad DQP for inputting and outputting data, and a power pad VSP for supplying power.

[0005] The command/address pad CAP, data input/output pad DQP, and power pad VSP each have a shared connection with the memory chip **10** and memory chip **11**, and are brought together in the command/address external terminal group CA, data input/output external terminal group DQ, and power supply external terminal group VS, respectively, on the base substrate **20**. On the contrary, the chip select signal pad CSP does not share a connection, and the chip select signal pad CSP of the memory chip **10** is connected to the chip select signal external terminal CS0, and the chip select signal pad CSP of the memory chip **11** is connected to the chip select signal external terminal CS1. The purpose of this configuration is to allow the memory chips. **10** and **11** to be selectively activated.

[0006] Another method has recently been proposed whereby the core unit in which the memory cell is formed and the interface unit in which the peripheral circuit for the memory cell is formed are each placed in a separate chip, and higher storage capacity and higher speeds are made possible by stacking these chips. This means that semiconductor storage devices that are conventionally composed of a single chip are divided into a plurality of chips. This method therefore allows the capacity of the chip (core chip) in which the core unit is formed to be increased, and makes it possible to obtain a very large storage capacity by furthermore stacking the core chips.

[0007] However, since the semiconductor storage device shown in **FIG. 22** is configured so that the command/address external terminal group CA and data input/output external terminal group DQ are connected to the memory chips **10** and **11**, there is a problem in that the parasitic capacitance of the command/address external terminal group CA and the data input/output external terminal group DQ is considerable in comparison with ordinary semiconductor storage devices in which only a single chip has been packaged.

[0008] Since such parasitic capacitance is the cause of signal waveform disturbance, there is a possibility that an adequate operating margin cannot be assured when the interface speed is very high, that is, when the clock speed exceeds 1 GHz, for example. This problem makes it difficult to make the capacity sufficiently large by using the method shown in **FIG. 22** because the problem is made more conspicuous as the number of memory chips to be stacked increases.

[0009] Also, since the semiconductor storage device shown in **FIG. 22** is different from an ordinary semiconductor storage device in which only a single chip has been packaged in the sense that two chip select signal external terminals are provided (CS0, CS1) compatibility with ordinary semiconductor storage devices is therefore lost. For this reason, a special-purpose memory controller must be designed in order to use the semiconductor storage device shown in **FIG. 22**, and the overall cost of the system is liable to increase.

[0010] Using the method described in Japanese Patent Application Laid-Open No. 2004-327474 appears to be able to solve the above-described problems, but this configuration is fundamentally different from the type of semiconductor storage device in which memory chips that are capable of independently carrying out read and write operations are stacked, and is rather a configuration in which core chips that are not capable of independently carrying out read and write operations are stacked, as shown in **FIG. 22**.

[0011] Therefore, an ordinary memory chip naturally cannot be used and a special-purpose chip must be newly designed. Also, with the configuration described in Japanese Patent Application Laid-Open No. 2004-327474, a through-electrode must be formed in the chips, and other advanced manufacturing techniques that are not sufficiently established must be used. It is therefore believed that manufacturing such chips at low cost under current conditions is difficult.

SUMMARY OF THE INVENTION

[0012] The present invention was contrived in order to solve such problems, and an object of the present invention is to reduce the parasitic capacitance of the command/address external terminal group and the data input/output external terminal group to an amount that is equal to that of a single chip component in a semiconductor storage device having a plurality of stacked memory chips.

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[0013] Another object of the present invention is to assure compatibility with ordinary semiconductor storage devices in which a single chip is packaged, in a semiconductor storage device having a plurality of stacked memory chips.

[0014] Yet another object of the present invention is to implement the objects described above with low cost by using memory chips that are each individually capable of read and write operations.

[0015] The above and other objects of the present invention can be accomplished by a semiconductor storage device comprising: a base substrate having a command/address external terminal group to which command signals and address signals are supplied, a data input/output external terminal group for inputting and outputting data signals, and a single chip select external terminal; and a plurality of memory chips that are stacked on the base substrate and are each individually capable of reading and writing operations, wherein a plurality of terminals constituting said command/address external terminal group, a plurality of terminals constituting said data input/output external terminal group, and said single chip select external terminal are connected to a single chip that has an interface function; and the single chip that has the interface function further has at least a chip select signal generation circuit that can individually activate said plurality of memory chips based on said address signals supplied via said command/address external terminal group and based on said chip select signal supplied via said chip select external terminal.

[0016] In accordance with the present invention, since the command/address external terminal group and other external terminals are connected to a single chip, the parasitic capacitance of the terminals can be reduced to an amount that is about equal to that of a single chip component. Also, since the semiconductor storage device of the present invention is provided with only a single chip select external terminal, it is possible to assure compatibility with ordinary semiconductor storage devices in which a single chip is packaged, even though the semiconductor storage device is provided with a plurality of stacked memory chips.

[0017] In addition, the stacked memory chips are memory chips that are individually capable of read and write operations. It is therefore possible to use so-called general-purpose memory, and hence to manufacture these chips at relatively low cost.

[0018] In the present invention, the single chip that has an interface function may be an interface chip that is different than the plurality of memory chips, or may be any one of the plurality of memory chips. With the former, it is possible to use the exact same chip as the memory chip that is used, and with the latter, it is possible to reduce the number of stacked chips by one.

[0019] The command signals, address signals, and data signals may be transmitted among the plurality of memory chips and the single chip that has an interface function by way of wiring with a shared connection to the plurality of memory chips, or may be carried out by way of wiring that is individually connected to the plurality of memory chips. The former allows the number of wires to be reduced, and the latter allows the wiring capacitance to be reduced.

[0020] Thus, in accordance with the present invention, it is possible to reduce the parasitic capacitance of the interface unit of a semiconductor storage device having a plurality of stacked memory chips to an amount equal to that of a single chip component. The input/output frequency of the command signal, address signal, and data signal can thereby be increased to that equivalent to a single chip component. Also, since the memory chips are three-dimensionally stacked in the present invention, the mounting surface area can be made equal to that of a single chip component.

[0021] Furthermore, since only a single chip select external terminal is provided, it is possible to assure compatibility with ordinary semiconductor storage devices in which a single chip is packaged. For this reason, there is no requirement that a special-purpose memory controller or the like be designed, and cost increases for the entire system can be held in check.

[0022] Since the stacked memory chips are furthermore ordinary memory chips (general-purpose DRAM, for example) that are each individually capable of read and write operations, formation of a through-electrode or other special steps are not required, and an increase in manufacturing costs can be inhibited.

[0023] Since it is also possible to individually activate the plurality of memory chips by using a chip select signal generation circuit, the power consumption of the entire package can also be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, wherein:

[0025] **FIG. 1** is a simplified perspective view that schematically shows a structure of the semiconductor storage device according to the first embodiment of the present invention;

[0026] **FIG. 2** is a simplified planar view of the memory chips shown in **FIG. 1**;

[0027] **FIG. 3** is a layout drawing of ball electrodes disposed on the reverse side of the base substrate shown in **FIG. 1**;

[0028] **FIG. 4** is a schematic diagram that describes the connection configuration between the memory chips and the interface chip in the first embodiment;

[0029] **FIG. 5** is a simplified circuit diagram showing the circuit configuration of the interface chip used in the first embodiment;

[0030] **FIG. 6** is a diagram showing in greater detail the circuit configuration of the clock system circuitry contained in the interface chip shown in **FIG. 5**;

[0031] **FIG. 7** is a diagram showing in greater detail the circuit configuration of the command/address system circuitry contained in the interface chip shown in **FIG. 5**;

[0032] **FIG. 8** is a list showing the commands and symbols that are output by the command decoder shown in **FIG. 7**, and the methods for issuing a chip select signal CS when the commands are executed;

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[0033] **FIG. 9** is a timing chart showing the issue timing of the refresh command to each memory chip;

[0034] **FIG. 10A** is a diagram for describing the function of the active bank register in the case where an activation command is issued;

[0035] **FIG. 10B** is a diagram for describing the function of the active bank register in the case where a column system command is issued;

[0036] **FIG. 11** is a diagram showing in greater detail the circuit configuration of the principal components of the data system circuitry contained in the interface chip shown in **FIG. 5**;

[0037] **FIG. 12** is a timing chart showing the write operation of the semiconductor storage device according to the first embodiment;

[0038] **FIG. 13** is a timing chart showing the read operation of the semiconductor storage device according to the first embodiment;

[0039] **FIG. 14** is a schematic diagram that describes the method for reducing the amplitude of the inter-chip interface between the memory chips and the interface chip;

[0040] **FIG. 15** is a diagram for describing an improved method for connecting the pads and the memory array in the memory chips;

[0041] **FIG. 16** is a schematic diagram of the connection configuration between the memory chips and the interface chip of the second embodiment;

[0042] **FIG. 17** is a simplified circuit diagram showing the circuit configuration of the interface chip shown in **FIG. 16** used in the second embodiment;

[0043] **FIG. 18** is a diagram showing in greater detail the circuit configuration of the clock system circuit contained in the interface chip shown in **FIG. 17**;

[0044] **FIG. 19** is a diagram showing in greater detail the circuit configuration of the command/address system circuit contained in the interface chip shown in **FIG. 17**;

[0045] **FIG. 20** is a diagram showing in greater detail the circuit configuration of the data system circuit contained in the interface chip shown in **FIG. 17**;

[0046] **FIG. 21** is a schematic diagram that describes the connection configuration between the memory chips and the memory chip in the semiconductor storage device of the third embodiment of the present invention; and

[0047] **FIG. 22** is a schematic diagram of a conventional semiconductor storage device that is three-dimensionally stacked and packaged.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0048] Preferred embodiments of the present invention will now be explained in detail with reference to the drawings.

[0049] **FIG. 1** is a simplified perspective view that schematically shows the structure of the semiconductor storage device **100** according to the first embodiment of the present invention.

[0050] The semiconductor storage device **100** of the present embodiment is provided with a base substrate **101**, four memory chips **110** to **113** stacked on the base substrate **101**, and an interface chip **120** disposed between the base substrate **101** and memory chips **110** to **113**, as shown in **FIG. 1**. In the present embodiment, DRAM is selected as the memory chips **110** to **113**, although this selection imposes no particular limitation. The memory chips **110** to **113** are chips having mutually the same configuration, and are DRAM chips that are individually capable of read and write operations, that is to say, the chips are ordinary general-purpose DRAM chips.

[0051] **FIG. 2** is a simplified planar view of the memory chips **110** to **113**.

[0052] The surface of the memory chips **110** to **113** can be largely classified into a memory array area MA, a peripheral circuit area PERI, and a bonding pad area B, as shown in **FIG. 2**. The bonding pad area B is disposed in a single direction in the center of the memory chip so as to be disposed between the two peripheral circuit areas PERI, and this area includes power supply pads VSP, a data input/output pad DQP, a command/address pad CAP, and a chip select signal pad CSP.

[0053] The power supply pads VSP have a peripheral circuit operating power supply VDD, a peripheral circuit ground power supply VSS, an output circuit operating power supply VDDQ, an output circuit ground power supply VSSQ, an interface reference power supply VREF, and the like. The data input/output pad DQP has data input/output pads DQ**0** to DQ**7** (the same applies to the case of ×8 components) a data strobe signal pad DQS, a data mask signal pad DM, and the like. The command/address pad CAP has a clock pad CLK, a clock enable pad CKE, a row address strobe pad RAS, a column address strobe pad CAS, a write enable pad WE, a bank address pads BA**0** to BA**2**, an address pads A**0** to A**13**, and the like.

[0054] The pads disposed on the memory chips **110** to **113** are connected to the pads **10**la disposed on the base substrate **101** by way of tapes **130** to **133** on which wiring INW is formed, as shown in **FIG. 1**. More specifically, pads **110***a* disposed on the memory chip **110** and pads **101***a* disposed on the base substrate **101** are connected by tape **130** that is disposed so as to cover the memory chip **110**, and pads disposed on the memory chips **111** to **113** and the pads **101***a* disposed on the base substrate **101** are similarly connected by tapes **131** to **133** that are disposed so as to cover the memory chips **111** to **113**, respectively.

[0055] Wiring (not shown) is formed on the base substrate **101**, and the pads **10**la and the pads (not shown) on the memory chip side of interface chip **120** are connected by the wiring. Pads (not shown) on the external circuit side of the interface chip **120** are connected to ball electrodes EXB disposed on the reverse side (mounting side) of the base substrate **101** by way of other wiring (not shown) disposed on the base substrate **101**. The ball electrodes EXB are external terminals of the semiconductor storage device **100** of the present embodiment.

[0056] **FIG. 3** is a layout drawing of ball electrodes EXB disposed on the reverse side of the base substrate **101**.

[0057] Other than the addition of address external terminals A**14** and A**15**, the types of ball electrodes EXB (which

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is an external terminal group of the semiconductor storage device **100**) match the types of pads disposed on the memory chips **110** to **113**, as shown in **FIG. 3**. Therefore, the chip select signal external terminal CS is always a single terminal. The ball electrodes EXB can be classified into a power supply external terminal group (VS), a data input/output external terminal group (DQ), a command/address external terminal group (CA), and a chip select signal external terminal (CS).

[0058] The peripheral circuit operating power supply VDD, peripheral circuit ground power supply VSS, output circuit operating power supply VDDQ, output circuit ground power supply VSSQ, interface reference power supply VREF, and the like constitute the power external terminal group (VS) in the same manner as the pads disposed on the memory chips **110** to **113**. The data input/output terminals DQ**0** to DQ7, data strobe signal terminal DQS, data mask signal terminal DM, and the like constitute the data input/output external terminal group (DQ). The clock terminal CLK, clock enable terminal CKE, row address strobe terminal RAS, column address strobe terminal CAS, write enable terminal WE, bank address terminals BA**0** to BA**2**, address terminals A**0** to A**13**, and the like constitute the command/address external terminal group (CA).

[0059] **FIG. 4** is a schematic diagram that describes the connection configuration between the memory chips **110** to **113** and the interface chip **120** in the present embodiment.

[0060] In the present embodiment, only the chip select signals are connected in a one-to-one relationship between the memory chips **110** to **113** and the interface chip **120**, as shown in **FIG. 4**. The other signals, that is to say, the command/address signals and data signals, are bus-connected by the command/address bus CAB and the data bus DQB. The power supply is also bus-connected.

[0061] As used herein, the term "one-to-one connection" refers to a connection in which the pads of the memory chips **110** to **113** and the pads of the interface chip **120** are individually connected for each memory chip, and the term "bus-connected" refers to a connection in which the pads of the memory chips **110** to **113** and the pads of the interface chip **120** share connections. Therefore, in the present embodiment, in the set of signals transmitted between the memory chips **110** to **113** and the interface chip **120**, only the chip select signal is a signal that is individually provided to the memory chips **110** to **113**.

[0062] Described more specifically, the command/address external terminal group CA and the chip select signal external terminal CS are connected to the command/address pad ECAP and the chip select signal pad ECSP, respectively, on the interface chip **120** by way of the ball electrodes EXB on the base substrate **101**. These signals are supplied to the command decoder CDC, and the output signals of the decoder are supplied to the command/address pad ICAP and chip select signal pad ICSP, respectively.

[0063] The signals (commands and addresses) that are output to the command/address pad ICAP are supplied in a shared configuration to the command/address pads CAP of the four memory chips **110** to **113** by way of the command/address bus CAB. On the other hand, four chip select signals that are output to the chip select signal pad ICSP are connected in a one-to-one relationship between the interface chip **120** and each of the memory chips **110** to **113**.

[0064] The data input/output external terminal group DQ is connected once to the data input/output pad EDQP on the interface chip **120** by way of the ball electrodes EXB on the base substrate **101**. The data input/output signals are input to a bidirectional repeater REP, and are connected to the data input/output pads DQP of the memory chips **110** to **113** by way of the data input/output pad IDQP. The data input/output pad IDQP and the data input/output pads DQP of the four memory chips. **110** to **113** are connected by a data bus DQB in the form of a 1:4 bus.

[0065] The power supply external terminal group VS is connected to the power supply pads VSP of the memory chips **110** to **113** and to the interface chip **120** directly by way of the ball electrodes EXB on the base substrate **101**.

[0066] Thus, in the semiconductor storage device **100** of the present embodiment, the connections between the ball electrodes EXB on the base substrate **101** and the memory chips **110** to **113** (excluding the power supply) are all carried out by way of the interface chip **120**. The chip connected to the data input/output external terminal group DQ and the command/address external terminal group CA is only the interface chip **120**. Thus, the parasitic capacitance of the external terminals can be reduced to an amount equal to that of a single chip component, and the frequency of the command/address and data input/output can be increased to a level equivalent to that of a single chip component.

[0067] In the present embodiment, since the command/address signals and data input/output signals are connected in the form of a bus inside a package, the number of wires inside the package can be kept low and manufacturing costs can thereby be held in check.

[0068] **FIG. 5** is a simplified circuit diagram showing the circuit configuration of the interface chip **120** used in the present embodiment.

[0069] The command/address pad ECAP on the interface chip **120** has pads for three systems: the clock system signals CLK, /CLK, and CKE; address system signals A**0** to A-**15** and BA**0** to BA**2**; and command system signals RAS, CAS, and WE, as shown in **FIG. 5**. The clock system signals CLK, /CLK, and CKE are supplied from outside of the semiconductor storage device **100** and are supplied to a clock regeneration circuit DLL by way of an input buffer INB. The output of the clock regeneration circuit DLL is supplied to terminals that output, respectively, the clock signals CLK, /CLK, and CKE of the command/address pad ICAP by way of the output buffer OB. The output of the clock regeneration circuit DLL is distributed within the interface chip **120** in order to latch other input signals in the latch circuits L.

[0070] The address system signals A**0** to A**15** and BA**0** to BA**2** are latched in the latch circuits L by way of the input buffers INB. The timing signals of the latch circuits L are supplied by the clock regeneration circuit DLL described above. The output of the latch circuits L is supplied to the terminals that output the address signals A**0** to A**13** and BA**0** to BA**2** of the command/address pad ICAP by way of the output buffer OB.

[0071] Here, the address signals A**0** to A**13** and BA**0** to BA**2** of the address signals A**0** to A**15** and BA**0** to BA**2** that are supplied from the exterior are directly fed to the command/address pad ICAP. The address signals A**14** and A**15** are not supplied to the command/address pad ICAP, but are

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rather fed to the chip select signal generation circuit CSG together with the output of the mode register MR and the bank addresses BA0 to BA2. The chip select signal generation circuit CSG is a circuit that activates any or all of the four chip select signal terminals CS supplied to the memory chips **110** to **113**.

[0072] The command system signals RAS, CAS, and WE are supplied to the command decoder CDC by way of the input buffers INB and latch circuits L. The output of the command decoder CDC is supplied to the chip select signal generation circuit CSG. The exact same signals as those fed to a general-purpose DRAM can be used as the command system signals RAS, CAS, and WE.

[0073] The chip select signal pad ECSP on the interface chip **120** is a single pad as described above. Therefore, the same chip select signal CS as used in a general-purpose DRAM may be supplied from outside of the semiconductor storage device **100** without consideration for the number of (four) stacked layers of memory chips **110** to **113**. The chip select signal CS supplied to the chip select signal pad ECSP is input to the command decoder CDC by way of the input buffer INB and latch circuits L. As described above, the chip select signal generation circuit CSG activates any or all of the four chip select signals CS on the basis of the address signals A14 and A15, the bank addresses BA0 to BA2, and the output of the command decoder CDC.

[0074] The data input/output pad EDQP on the interface chip **120** is a terminal for inputting and outputting the data signals DQ0 to DQ7, data strobe signal DQS, data mask signal DM, and other signals, and is connected to the data input/output pad IDQP by way of the bidirectional repeater REP, as described above.

[0075] In this case, when the memory chips **110** to **113** to be stacked are the double data rate (DDR-**800**) type, a signal with speed of 400 Mbps is transferred over the command/address external terminal group CA and the command/address bus CAB inside the package. On the other hand, a signal with speed of 800 Mbps is transferred over the on the data input/output external terminal group DQ and the data bus DQB inside the package.

[0076] Described next in greater detail is the circuit configuration of the interface chip **120** used in the present embodiment.

[0077] **FIG. 6** is a diagram showing in greater detail the circuit configuration of the clock system circuitry contained in the interface chip **120**.

[0078] The complimentary clock signals CLK and /CLK supplied from the command/address pad ECAP are input to a differential amp input buffer INB, as shown in **FIG. 6**. The input buffer INB is activated by the output of the differential amp input buffer INB that receives the clock enable signal CKE and the reference voltage VREF. The output of the input buffer INB that receives the complimentary clock signals CLK and /CLK is supplied to the clock regeneration circuit DLL, and the output of the regeneration circuit is supplied to the complimentary clock signals CLK and /CLK of the command/address pad ICAP by way of the output buffers OB. The clock regeneration circuit DLL generates an internal clock signal CLKI, and the internal clock signal CLKI is supplied to the internal circuitry of the interface chip **120**.

[0079] The output of the input buffer INB that receives the clock enable signal CKE is latched by the latch circuit L (which uses internal clock signal CLKI as a timing signal), and is supplied to the clock enable terminal CKE of the command/address pad ICAP by way of the output buffer OB. The clock enable signal CKE buffered by the input buffer INB is also supplied to the internal circuitry of interface chip **120**. The clockenable signal CKE is fed to the clock regeneration circuit DLL, and when the clock enable signal CKE is activated, the clock feed to the memory chips **110** to **113** is stopped.

[0080] Thus, in this present embodiment, since a clock regeneration circuit DLL is provided inside the interface chip **120**, the phase difference between the input and output clocks is reduced and the timing margin of the latch circuits L is increased. The operating margin can therefore be adequately assured even when the operating frequency is higher. When the clock enable signal CKE is deactivated, the operation of the clock regeneration circuit DLL is stopped, and since the clock feed to the memory chips **110** to **113** and the internal circuitry of the interface chip **120** is stopped, the power consumption during standby can be reduced.

[0081] **FIG. 7** is a diagram showing in greater detail the circuit configuration of the command/address system circuitry contained in the interface chip **120**.

[0082] The command/address system signals A0 to A15, BA0 to BA2, RAS, CAS, and WE are input from outside of the semiconductor storage device **100** to input buffers INB by way of the command/address pad ECAP, as shown in **FIG. 7**.

[0083] The chip select signal CS is supplied from outside of the semiconductor storage device **100** to an input buffer INB by way of the chip select signal pad ECSP. The input buffers INB are differential amp input buffers in which the reference voltage VREF is used, and the outputs of the buffers are supplied to corresponding latch circuits L. The latch circuits L synchronize with the internal clock signal CLKI generated by the clock regeneration circuit DLL (refer to **FIG. 6**), and accept the output of the corresponding input buffer INB.

[0084] The address signals A14 and A15 of the address signals A0 to A15 are decoded in the decoder DEC, and decoder output is supplied to the chip select signal generation circuit CSG. The bank addresses BA0 to BA2 are supplied to the command/address pad ICAP and are also supplied to the chip select signal generation circuit CSG and the mode register MR. The address signals A0 to A13 are supplied to the command/address pad ICAP and are also supplied to the mode register MR. The address signal A10 of the address signals A0 to A13 is also supplied to the command decoder CDC together with the command system signals RAS, CAS, and WE, as well as the chip select signal CS and clock enable signal CKE. The command decoder CDC decodes the signals in the same manner as a general-purpose DRAM, and generates a command signal CMD on the basis of the decoding result.

[0085] The command system signals RAS, CAS, and WE are directly supplied to the command/address pad ICAP, and an activate command (Bank activate), read command (Read) write command (Write), precharge command (Precharge), refresh command (Refresh), and other commands are presented to the memory chips **110** to **113**.

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[0086] The chip select signal generation circuit CSG receives a command signal CMD fed by the command decoder CDC and determines the operating mode. Any or all of the four chip select signals CSO to CS3 are activated based on the operating mode thus determined. The chip select signals CSO to CS3 are supplied to the corresponding chip select signal pads ICSP, respectively, by way of output buffers OB.

[0087] Thus, in the present embodiment, since the higher bits A14 and A15 of the address signals are decoded and the chip select signals CSO to CS3 are activated based on the decoded signals, the memory chip appears from outside of the semiconductor storage device **100** as a single, large memory chip, and only one of the four memory chips **110** to **113** is activated in ordinary operation inside the semiconductor storage device **100**. For this reason, an increase in power consumption can be held in check while assuring compatibility with general-purpose DRAM.

[0088] **FIG. 8** is a list showing the commands and symbols that are output by the command decoder CDC, and the methods for issuing a chip select signal CS when the commands are executed.

[0089] Commands are input to the command decoder CDC by using the clock system signal CKE, chip select signal CS, address signal A10, and command system signals RAS, CAS, and WE fed from outside the semiconductor storage device **100**, and the command decoder CDC generates a command signal CMD by using a combination of the signals. The chip select signal generation circuit CSG that receives the command signal CMD activates the chip select signals CS0 to CS3 as described below in accordance with the type of command.

[0090] First, when a mode set command "Mode register set (MRS)" or "Extended mode register set (EMRS)" classified as an "Initialization" command has been input, all the chip select signals CS0 to CS3 are simultaneously activated.

[0091] When a refresh command "Auto refresh (REF)" or "Self refresh entry (SELF)" classified as a "Row system" command has been input, the chip select signals CS0 to CS3 are sequentially activated with a phase difference. In other words, when synchronization is made with the clock signal CLK from outside the semiconductor storage device **100** and a refresh command (REF or SELF) is input, the interface chip **120** continuously issues a refresh command (REF or SELF) to the memory chips **110** to **113** by way of the command/address pad ICAP, and sequentially activates the chip select signals CS0 to CS3, as shown in **FIG. 9**.

[0092] The same refresh command (REF or SELF) is thereby sequentially input with a prescribed phase difference to the four memory chips **110** to **113**. The phase difference is a single clock cycle as shown in the example of **FIG. 9**, but no limitation is imposed thereby, and the phase difference may be a plurality of clock cycles.

[0093] Thus, the reason that refresh commands (REF or SELF) are sequentially issued with a phase difference to the memory chips **110** to **113** is that a greater amount of electric current temporarily flows during a refresh operation than during ordinary read and write operations. In other words, when refresh commands (REF and SELF) are simultaneously issued to all the memory chips **110** to **113**, the four memory chips **110** to **113** are simultaneously refreshed. As a result, a considerable amount of electric current flows, and the power supply potential and ground potential are liable to fluctuate.

[0094] In the case that return from self refresh is instructed, that is to say, in the case that a "Self refresh exit (SELFX)" command has been issued, all of the chip select signals CS0 to CS3 are simultaneously activated. Inputting a precharge command "Single bank precharge (PRE)" or "Precharge all banks (PALL)" activates the chip select signals CS0 to CS3, which correspond to the chip numbers (#0 to #3) stored in the active bank register ABR.

[0095] When an activation command "Back activate (ACT)" has been input, any one of the chip select signals CS0 to CS3 is activated based on the address signals A14 and A15, and the relationship between the activated chip select signal (CS0 to CS3) and the selected bank number (#0 to #7) is stored in the active bank register ABR shown in **FIG. 10A**. The active bank register ABR is a circuit disposed inside the chip select signal generation circuit CSG, and this register is made up of a group of registers that hold the relationship between the chip numbers (#0 to #3) specified by the higher two bits A14 and A15 of the row address, and the bank numbers (#0 to #7) specified by the bank addresses BA0 to BA2.

[0096] The reason for providing such an active bank register ABR is that since chip selection is carried out by the higher bits A14 and A15 of the row address A0 to A15 and only the bank address BA0 to BA2 and the column address A0 to A9 are fed when a column system command is input, it cannot be determined which chip select signals CS0 to CS3 should be activated when a column system command has been input if the above-described relationship is not stored using the active bank register ABR. However, provided that the bank address is expanded to five bits (BA0 to BA4) in lieu of the row address A14 and A15, that the chip is selected by using the higher two bits (BA0 and BA1), and that the bank inside the chip selected by the lower three bits (BA2 to BA4) is selected, such a problem is solved because the relationship between the bank address and the chip to be selected is fixed.

[0097] Nevertheless, in order to maintain compatibility with common general-purpose DRAM having an 8-bank configuration, the bank address is preferably given a three-bit configuration (BA0 to BA2) and a portion (A14 and A15) of the row address is used rather than the bank address to select a chip, as in the present embodiment. It is for this reason that an active bank register ABR is provided in the present embodiment.

[0098] When a write command "Write (WRIT)" or "Write with auto precharge (WRITA)" classified as a "column system" command, or a read command "Read (READ)" or "Read with auto precharge (READA)" classified as a "column system" command has been input, the bank address BA0 to BA2 is decoded in the decoder DEC, as shown in **FIG. 10B**, and the chip select signals CS0 to CS3, which correspond to the chip numbers (#0 to #3) stored in the active bank register ABR, are activated.

[0099] When a "No operation (NOP)" command, "Device deselect (DESL)" command, "Power down mode entry (PDEN)" command, or "Power down mode exit (PDEX)" command classified as "another" command has been input, all of the chip select signals CS0 to CS3 are simultaneously activated.

[0100] Thus, in the present embodiment, since the chip number to be activated is stored in the active bank register ABR when an activation command "Bank activate (ACT)" has been input, data can be accessed from outside the semiconductor storage device **100** by inputting to the interface chip **120** only the bank address BA**0** to BA**2** and the column address A**0** to A**9** when a read command or write command is input.

[0101] The same address input method as that used for a general-purpose DRAM can therefore be used and compatibility can be assured. Since commands are issued with a phase difference to the memory chips **110** to **113** when a refresh operation is carried out, the peak electric current that flows at the instant the memory chips **110** to **113** carry out a refresh operation can be staggered and power supply noise can be reduced.

[0102] **FIG. 11** is a diagram showing in greater detail the circuit configuration of the principal components of the data system circuitry contained in the interface chip **120**. In **FIG. 11**, the RDQS and /RDQS included in the signals of the data system are omitted.

[0103] The data system signals ODT, DQS, /DQS, DQ**0** to DQ**7**, and DM are supplied from outside the semiconductor storage device **100** by way of the data input/output pad EDQP, as shown in **FIG. 11**. The on-chip resistance activation signal ODT is supplied to terminating resistors RT connected to the terminals, and the resistance value data RTV issued by the mode register is supplied to the terminating resistors RT in a shared configuration.

[0104] The data system signals have a higher frequency than the command/address system signals, and the signal waveform is therefore more easily distorted, but signal reflection can be reduced by carrying out termination inside the chip without any terminating resistance on the substrate. The distortion of the signal waveform can thereby be inhibited, resulting in an increased operating margin. In an ordinary DRAM, a terminating resistance is used inside the memory chip, but in the semiconductor storage device **100** of the present embodiment, a terminating resistance is used inside the interface chip **120**.

[0105] The data system signals DQS, /DQS, DQ**0** to DQ**7**, and DM are supplied to the data input/output pad IDQP by way of a bidirectional repeater REP. More specifically, the data signals DQ**0** to DQ**7** and DM that are input from outside the semiconductor storage device **100** during a write operation are amplified by differential input buffers INB that make a comparison with the reference voltage VREF and are latched in the latch circuits L. The data strobe signals DQS and /DQS input from outside the semiconductor storage device **100** during a write operation are amplified by differential input buffers INB. When signals are output to the memory chips **110** to **113**, an internal strobe signal DQSI that is offset in phase by 90° with respect to the data signals DQ**0** to DQ**7** is applied. The internal strobe signal DQSI is generated by a strobe signal generation circuit DSG.

[0106] Therefore, the data strobe signal DQS on the data input/output pad EDQP is offset in phase by 90° with respect to the data in**0**, in**1**, in**2**, and in**3** that are continuously input during a write operation, as shown in **FIG. 12**. Accordingly, the latch circuits L synchronize with the rise and fall of the data strobe signal DQS, and the data in**0**, in**1**, in**2**, and in**3** can be sequentially received. Also, the data in**0**, in**1**, in**2**, and in**3** sequentially received in this manner synchronize with the data strobe signal DQS on the data input/output pad IDQP, and are output to the memory chips **110** to **113** selected the chip select signals CS**0** to CS**3**.

[0107] More specifically, synchronization is made with the rising edge of the clock signal CLK during a write operation, as shown in **FIG. 12**; a write command (WRIT) is input to the command/address pad ECAP; and after a prescribed write latency WL has elapsed, the data signals DQ**0** to DQ7 are input to the data input/output pad EDQP. Only a single data DQ**0** of the data signals DQ**0** to DQ**7** is shown in **FIG. 12**. The data strobe signal DQS (which is offset in phase by 90°) is also input to the data input/output pad EDQP simultaneously with the data signals DQ**0** to DQ**7** to be written.

[0108] A write command (WRIT) is supplied to the interface chip **120**, after which synchronization is made with the subsequent falling clock signal CLK, and the same command (WRIT) is output to the memory chips **110** to **113** by way of the command/address pad ICAP. The data signals DQ**0** to DQ**7** and data strobe signal DQS are also output from the data input/output pad IDQP after a prescribed write latency WL has elapsed. The write latency WL is a value that is set in advance in the mode register on the memory chips **110** to **113** and on the interface chip **120**. In the case of a write operation, the write latency WL is set to the same value in the interface chip **120** and the memory chips **110** to **113**.

[0109] The data signals DQ**0** to DQ**7** output from the memory chips **110** to **113** during a read operation synchronize with the internal strobe signal DQSI that is generated by the strobe signal generation circuit DSG inside the interface chip **120**, are received by the latch circuits L, and are output to the outside of the semiconductor storage device **100**. Since the data strobe signal DQS fed from the memory chips **110** to **113** during a read operation match the phase of the data signals DQ**0** to DQ**7**, as shown in **FIG. 13**, the data signals DQ**0** to DQ**7** cannot be directly received in synchronization with the data strobe signal DQS.

[0110] In view of the above, an internal strobe signal DQSI that is offset in phase by 90° from the data strobe signal DQS is generated by the strobe signal generation circuit DSG, and the read data is received in synchronization with the internal strobe signal. The data signals DQ**0** to DQ**7** thus received are synchronized with the internal clock signal CLKI (not shown) and output to an impedance variable output buffer OBV. The impedance of the impedance variable output buffer OBV is controlled by the impedance setting value ROV issued from the mode register MR.

[0111] More specifically, the read command (READ) is input to the command/address pad ECAP of the interface chip **120** at the rising edge of the clock signal CLK during a read operation, as shown in **FIG. 13**. The read command (READ) is thereafter output to the memory chips **110** to **113** at the subsequent falling edge of the clock signal CLK by way of the command/address pad ICAP. After a prescribed read latency RL has elapsed, data signals DQ**0** to DQ**7** and DQS are output from the memory chips **110** to **113**.

[0112] The interface chip **120** receives the data signals by way of the data input/output pad IDQP, synchronizes the signals with the subsequent clock signal CLK, and outputs

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the signals to the outside of the semiconductor storage device **100** by way of the data input/output pad EDQP. Since the data strobe signal DQS matches the phase of the data signals DQ**0** to DQ**7** during a read operation, the signal is directly matched with the clock and is output from the data input/output pad EDQP.

[0113] As viewed from outside of the semiconductor storage device **100**, the overall read latency is a value in which a single clock cycle has been added (which is the latency of the interface chip **120** itself) to the read latency RL of the memory chips **110** to **113**, that is to say, a value that is equal to RL+1, as shown in **FIG. 13**. Therefore, the value obtained by adding the latency of the interface chip **120** as such to the value of the mode register of the memory chips **110** to **113** is set as the read latency RL in the mode register MR on the interface chip **120**.

[0114] Thus, the present embodiment involves receiving data that uses an internal strobe signal DQSI generated by the strobe signal generation circuit DSG, allowing an adequate operating margin to be assured even when the operating frequency is high. Since the value of the terminating resistance and the impedance of the output buffer canbe controlled, distortion of the data transfer waveform is controlled, and, as a result, the operating margin can be expanded.

[0115] Next, the signal amplitude between the memory chips **110** to **113** and the interface chip **120** is described.

[0116] **FIG. 14** is a schematic diagram that describes the method for reducing the amplitude of the inter-chip interface between the memory chips **110** to **113** and the interface chip **120**. As an example, the case is shown in which the amplitude of the chip select signals CS**0** to CS**3** is reduced, but the same method may be adopted for the other signals as well.

[0117] In the present example, in the output buffer OB contained in the interface chip **120**, an inverter with a CMOS structure is used as the output buffer for providing output to the memory chips **110** to **113**, as shown in **FIG. 14**. An internal power supply voltage VDDI on the high level side of the inverter is kept at a lower level than the externally supplied power supply VDDQ, and the internal power supply voltage VSSI on the low level side is kept at a higher level than the externally supplied power supply VSSQ. If, for example, the VDDQ is 1.8 V, the VDDI may be set to about 1.1 V. Also, if the VSSQ is 0 V, the VSSI may be set to about 0.7 V.

[0118] When a signal (the chip select signal CS in **FIG. 14**) to be output is input to the input terminal of an inverter in which such internal power supply voltages VDDI and VSSI are used, the signal output has reduced amplitude. In this case, the threshold value of the NMOS and PMOS that constitute the inverter is preferably set to be lower than that of an ordinary device in order to increase speed. When set in this fashion, the amplitude of the data signals can be reduced without providing a terminating resistance in the wiring.

[0119] The internal power supply voltages VDDI and VSSI can be generated by a step-down circuit VRG. The step-down circuit VRG is composed of resistors R1 to R**3** that produce reference voltages V**1** and V**2**; differential amps AP**1** and AP**2** in which the reference voltages V**1** and V**2** are supplied to a non-inverted input terminal (+) and an inverted input terminal (−) respectively; and a PMOS and NMOS in which the outputs of the differential amps AP**1** and AP**2** are fed to the gates, respectively. The drains of the PMOS and NMOS are connected to the inverted input terminal (−) of the differential amp AP**1** and the non-inverted input terminal (+) of the differential amp AP**2**, respectively; and the electric potentials are the internal power supply voltages VDDI and VSSI, respectively.

[0120] If such a low-amplitude output buffer is used, the charge and discharge power can be considerably reduced by charging and discharging the parasitic capacitance of the wiring INW and the bonding pad when a command/address or data is transferred.

[0121] Another feature of in the present embodiment is that since four memory chips **110** to **113** are mounted in a single package, there may be a problem in that the temperature inside the package may increase due to the power consumption of the memory chips **110** to **113**, but if the power consumption due to signal transfer between the chips is reduced by using a low-amplitude output buffer, the temperature increase inside the package can be inhibited, and, as a result, the data retention time of the memory chips **110** to **113** can be extended.

[0122] The low-amplitude output buffer may be used not only on the interface chip **120** side, but also on the memory chips **110** to **113** side.

[0123] As described above, the semiconductor storage device **100** of the present embodiment has a configuration in which a plurality of memory chips **110** to **113** that are capable of independently carrying out read and write operations are stacked, and the plurality of memory chips **110** to **113** are externally connected by way of an interface chip **120**. For this reason, the chip connected to the command/address external terminal group CA and the data input/output external terminal group DQ is a single chip (interface chip **120**), and parasitic capacitance of the external terminals can be reduced to an amount that is about equal to that of a single chip component.

[0124] The frequency of the command/address and data input/output can be increased thereby to an amount that is equal to about that of a single chip component. Additionally, since the memory chips **110** to **113** are three-dimensionally stacked, the mounting surface area can be reduced to an amount equal to a single chip component.

[0125] As viewed from external circuitry, the interface chip **120** can be handled as an ordinary general-purpose DRAM, making it possible to assure compatibility with ordinary semiconductor storage devices that are packaged in only a single chip. For this reason, there is no need to design a special-purpose memory controller or the like, and an increase in the cost of the system overall can be held in check.

[0126] Since the stacked memory chips **110** to **113** are ordinary memory chips (general-purpose DRAM) that are each independently capable of read and write operations, a special step for forming a through-electrode or carrying out other processes is not required. For this reason, it is also possible to hold down increases in manufacturing costs.

[0127] In the present embodiment, the command/address signals and data input/output signals are connected in the

form of a bus inside the package, making it possible to keep the number of wires inside the package low and thereby to hold manufacturing costs in check. Since any one of the chip select signals CS0 to CS3 is activated by decoding the higher bits A14 and A15 of the row address during read and write operations, the interface chip **120** can selectively activate the memory chips **110** to **113**, and the overall power consumption of the stacked package can be reduced.

[0128] In the embodiment described above, common, general-use DRAM is used for the memory chips **110** to **113**, but the data transfer speed between the memory chips **110** to **113** and the interface chip **120** can be further increased by separating the pads for normal use and the pads for testing as the pads of the memory chips **110** to **113**. This method is described in **FIG. 15**.

[0129] **FIG. 15** is a diagram for describing an improved method for connecting the pads and the memory array MA in the memory chips **110** to **113**. For the sake of simplicity, only the command/address pad CAP and the data input/output pad DQP are depicted, but the chip select signal pad CSP may also be handled in the same manner as the command/address pad CAP.

[0130] In the present example, in addition to being provided with the command/address pad CAP and the data input/output pad DQP for normal use, the memory chips **110** to **113** are also provided with a test command/address pad TCAP and a test data input/output pad TDQP, as shown in **FIG. 15**. Although not depicted, a test pad that corresponds to the chip select signal pad CSP is also provided.

[0131] The test command/address pad TCAP has an electrostatic protection element ESD, an input buffer INB, and a latch circuit L. The test data input/output pad TDQP has an output buffer OB, an input buffer INB, and a latch circuit L. In contrast to this configuration, the command/address pad CAP and data input/output pad DQP for normal use are not connected to such circuitry and are essentially directly connected to the memory array MA, as shown in **FIG. 15**.

[0132] The test command/address pad TCAP and the test data input/output pad TDQP are pads that are used when the memory chips **110** to **113** are tested. More specifically, since the parasitic capacitance of the wiring is considerable, a tester used for testing the memory chips **110** to **113** requires an output buffer with a relatively high driving force, an input buffer with high sensitivity, and an electrostatic protection element.

[0133] In contrast, the chip connections are made with very short distance wires in terms of practical use, and since the parasitic capacitance is very low in comparison with the tester, the driving force of the output buffer OB may be fairly low, and there is no requirement that an input buffer INB with such a high sensitivity be used. Also, the necessity to provide an electrostatic protection element ESD is also low. Considering this point, in the present example, the electrostatic protection element ESD, the input buffer INB, and the like are bypassed, and the pads and memory array MA are essentially directly connected.

[0134] Testing can thereby be correctly carried out during the testing procedure, the data transfer speed between the memory chips **110** to **113** and the interface chip **120** can be increased during actual use, and power consumption can be reduced.

[0135] A second preferred embodiment of the present invention is described next.

[0136] The semiconductor storage device **200** of the second embodiment of the present invention is exactly the same as the semiconductor storage device **100** of the first embodiment described above in terms of the external appearance and the memory chips **110** to **113** that are used, but are different in terms of the interface chip that is used and the manner in which the memory chips **110** to **113** and the interface chip are connected. For this reason, a duplicative description of the portions that are the same as the first embodiment is omitted.

[0137] **FIG. 16** is a schematic diagram of the connection configuration between the memory chips **110** to **113** and the interface chip **220** of the present embodiment.

[0138] In the present embodiment, all of the signals are connected in a one-to-one relationship between the memory chips **110** to **113** and the interface chip **220**, as shown in **FIG. 16**. In other words, not only are the chip select signals connected in a one-to-one relationship, but the command/address signals and data signals are also connected in such a relationship. The power supply is bus connected. Therefore, in the present embodiment, all of the signals transferred between the memory chips **110** to **113** and the interface chip **220** are individual signals for each memory chips **110** to **113**.

[0139] Described more specifically, the command/address external terminal group CA and chip select signal external terminal CS are connected, respectively, to the command/address pad ECAP and the chip select signal pad ECSP on the interface chip **220** by way of the ball electrodes EXB on the base substrate **101**. These signals are input to the command decoder CDC, and the four outputs of the decoder are output, respectively, to the command/address pads ICAP0 to ICAP3 and chip select signal pads ICSP0 to ICSP3, which are individually assigned to the memory chips **110** to **113**.

[0140] The signals (command and address) output to the command/address pads ICAP0 to ICAP3 are individually fed to the command/address pad CAP of the four memory chips **110** to **113**. The four chip select signals that are output to the chip select signal pads ICSP0 to ICSP3 are also connected in a one-to-one relationship between the interface chip **220** and memory chips **110** to **113**, respectively.

[0141] The data input/output external terminal group DQ is connected to the data input/output pad EDQP on the interface chip **220** by way of the ball electrodes EXB on the base substrate **101**. The data input/output signals are input to a bidirectional multiplexer MUX, and are connected to the data input/output pad DQP of the memory chips **110** to **113**, respectively, by way of the data input/output pads IDQP0 to IDQP3 that are individually assigned to the memory chips **110** to **113**.

[0142] To be written to the memory chips **110** to **113**, the data is input to the interface chip **220** from outside the semiconductor storage device **100** by way of the data input/output external terminal group DQ, and write data is sent to only one of the memory chips **110** to **113** selected by way of the bidirectional multiplexer MUX. When data is read from the memory chips **110** to **113**, the read data from the selected chip of the memory chips **110** to **113** is input to

the interface chip **220** and is output to the data input/output external terminal group DQ by way of the bidirectional multiplexer.

[0143] The power supply external terminal group VS is connected directly to the power supply pads VSP of the memory chips **110** to **113** and the interface chip **220** by way of the ball electrodes EXB on the base substrate **101**.

[0144] Thus, in the present embodiment, since the command/address signals and data input/output signals are connected in a one-to-one relationship inside the package, only the input/output circuits of two transmitting and receiving channels are connected to the wiring INW inside the package. For this reason, the parasitic capacitance of the wiring INW can be reduced, and the charging and discharging electric current of the parasitic capacitance (which is a problem when high speed signals are transmitted) can be reduced.

[0145] **FIG. 17** is a simplified circuit diagram showing the circuit configuration of the interface chip **220** used in the present embodiment.

[0146] The interface chip **220** used in the present embodiment, as shown **FIG. 17**, is different from the interface chip **120** shown in **FIG. 5** in that command/address pads ICAP are individually provided to the memory chips **110** to **113** (ICAP**0** to ICAP**3**), output buffers OB are individually provided in a corresponding relationship, data input/output pads IDQP are individually provided to the memory chips **110** to **113** (IDQP**0** to IDQP**3**), and bidirectional repeaters are substituted for the bidirectional multiplexer MUX in a corresponding relationship. Other than the above, the configuration is the same as the interface chip **120** shown in **FIG. 5**.

[0147] **FIG. 18** is a diagram showing in greater detail the circuit configuration of the clock system circuit contained in the interface chip **220**.

[0148] The clock system circuit contained in the interface chip **220**, as shown in **FIG. 18**, is different than the clock system circuit of the interface chip **120** shown in **FIG. 6** in that the pads for feeding the complimentary clock signals CLK and /CLK and the clock enable signal CKE are individually provided to the memory chips **110** to **113** (ICAPO to ICAP**3**), and output buffers OB are independently provided in a corresponding relationship. Other than the above, the configuration is the same as the clock system circuit shown in **FIG. 6**.

[0149] **FIG. 19** is a diagram showing in greater detail the circuit configuration of the command/address system circuit contained in the interface chip **220**.

[0150] The command/address system circuit contained in the interface chip **220**, as shown in **FIG. 19**, is different than the command/address system circuit of the interface chip **120** shown in **FIG. 7** in that command/address pads ICAP are individually provided to the memory chips **110** to **113** (ICAP**0** to ICAP**3**), output buffers OB are individually provided in a corresponding relationship, and selectors SEL for selectively activating the output buffers are also provided. Chip select signals CS**0** to CS**3** are fed to the selectors SEL, and the selectors SEL feed a signal only to the output buffers OB that correspond to the activated chip select signals CS**0** to CS**3**. Therefore, commands and addresses are not fed to the unselected memory chips **110** to **113**.

[0151] **FIG. 20** is a diagram showing in greater detail the circuit configuration of the data system circuit contained in the interface chip **220**.

[0152] The data system circuit contained in the interface chip **220**, as shown in **FIG. 20**, is different than the data system circuit of the interface chip **120** shown in **FIG. 11** in that data input/output pads IDQP are individually provided to the memory chips **110** to **113** (IDQPO to IDQP**3**), input buffers INB and output buffers OB are individually provided in a corresponding relationship, and selectors SEL that selectively activate the output buffers are also provided.

[0153] In the same manner as the command/address system circuit, chip select signals CS**0** to CS**3** are fed to the selectors SEL, the selectors SEL feed a signal only to the output buffers OB that correspond to the activated chip select signals CS**0** to CS**3**, and only the output of the input buffers INB corresponding to the activated chip select signals CS**0** to CS**3** are allowed to pass. Therefore, data is not fed to the unselected memory chips **110** to **113**.

[0154] The semiconductor storage device **200** of the present embodiment can achieve substantially the same effects as the semiconductor storage device **100** of the first embodiment described above, and since the command/address signals and data input/output signals are connected in a one-to-one relationship inside the package, the parasitic capacitance of the wiring INW inside the package can be reduced. The charging and discharging electric current of the parasitic capacitance (which is a problem when high speed signals are transmitted) can thereby be reduced.

[0155] In the present embodiment, both the command/address signals and data input/output signals are connected in a one-to-one relationship, but since the speed of the command/address signals is half the speed of the data input/output signals in a DDR-type DRAM, power consumption does not always become a large problem for command/address signals. Considering this point, the command/address signals are bus-connected in the same manner as in the first embodiment, and the data input/output signals may be connected in a one-to-one relationship. According to this configuration, it is possible to reduce power consumption while keeping the number of wires inside the chip low.

[0156] A third preferred embodiment of the present invention is described next.

[0157] **FIG. 21** is a schematic diagram that describes the connection configuration between the memory chips **110** to **112** and the memory chip **320** in the semiconductor storage device **300** of the third embodiment of the present invention.

[0158] In the present embodiment, the special-purpose interface chip is dispensed with. Instead, an interface chip function is provided to the memory chip **320** that is most proximate to the base substrate **101**, as shown in **FIG. 21**. Other than the above, the configuration is the same as the semiconductor storage device **100** of the first embodiment described above. Signals other than the chip select signals CS**0** to CS**2** are bus-connected using the command/address bus CAB and the data bus DQB between the memory chips **110** to **112** and the memory chip **320**. According to the present invention, the number of chips can be reduced by

one, and the thickness of the entire package can therefore be reduced. Also, since the number of wires and the load of the internal wiring INW can be reduced, power consumption can be further lowered.

[0159] In the present embodiment, both the command/address signals and the data input/output signals are bus-connected in the same manner as the semiconductor storage device **100** of the first embodiment, although it is also possible to connect both the command/address signals and the data input/output signals in a one-to-one relationship as in the semiconductor storage device **200** of the second embodiment. Another option is to bus-connect the command/address signals as in the first embodiment, and to connect the data input/output signals in a one-to-one relationship.

[0160] The present invention is in no way limited to the aforementioned embodiments, but rather various modifications are possible within the scope of the invention as recited in the claims, and naturally these modifications are included within the scope of the invention.

[0161] In the embodiments described above, four memory chips were used as an example, but the number of memory chips that may be used is not limited to four, and any number of memory chips may be used as long as this number is two or more.

[0162] In the embodiments described above, DRAM was used as the memory chip, but the present invention is not limited to this type of chip alone, and other types of memory chips may also be used as long as the memory chips are each independently capable of read operations and write operations.

What is claimed is:

1. A semiconductor storage device comprising:

a base substrate having a command/address external terminal group to which command signals and address signals are supplied, a data input/output external terminal group for inputting and outputting data signals, and a single chip select external terminal; and

a plurality of memory chips that are stacked on the base substrate and are each individually capable of reading and writing operations, wherein

a plurality of terminals constituting said command/address external terminal group, a plurality of terminals constituting said data input/output external terminal group, and said single chip select external terminal are connected to a single chip that has an interface function; and

the single chip that has the interface function further has at least a chip select signal generation circuit that can individually activate said plurality of memory chips based on said address signals supplied via said command/address external terminal group and based on said chip select signal supplied via said chip select external terminal.

2. The semiconductor storage device as claimed in claim 1, wherein said single chip that has the interface function is an interface chip that is different from said plurality of memory chips.

3. The semiconductor storage device as claimed in claim 1, wherein said single chip that has the interface function is any one chip from among said plurality of memory chips.

4. The semiconductor storage device as claimed in claim 1, wherein at least one of the signals selected from said command signals, said address signals, and said data signals are transmitted between said plurality of memory chips and said single chip that has the interface function by way of wiring with a shared connection to said plurality of memory chips.

5. The semiconductor storage device as claimed in claim 1, wherein at least one of the signals selected from said command signals, said address signals, and said data signals are transmitted between said plurality of memory chips and said single chip that has the interface function by way of wiring that is individually connected to the plurality of memory chips.

6. The semiconductor storage device as claimed in claim 1, wherein said chip select signal generation circuit activates one of said plurality of memory chips based on a portion of said address signals supplied via said command/address external terminal group which is different from a bank address when an activation command is issued.

7. The semiconductor storage device as claimed in claim 6, wherein said chip select signal generation circuit has an active bank register for storing the relationship between the selected bank and the memory chip that is to be activated, and activates one of said plurality of memory chips by referencing said active bank register when a read command or a write command is issued together with said bank address via said command/address external terminal group.

8. The semiconductor storage device as claimed in claim 1, wherein said chip select signal generation circuit sequentially activates said plurality of memory chips when a refresh command is issued.

9. The semiconductor storage device as claimed in claim 1, wherein said single chip that has the interface function further has a clock regeneration circuit, and a clock regenerated by said clock regeneration circuit is supplied to said plurality of memory chips.

10. The semiconductor storage device as claimed in claim 1, wherein said single chip that has the interface function further has a strobe signal generation circuit, and said chip that has the interface function outputs a data signal that is read from said memory chip via said data input/output external terminal group in synchronism with an output of said strobe signal generation circuit.

11. The semiconductor storage device as claimed in claim 1, wherein said single chip that has the interface function has a terminating resistance that is connected to said data input/output external terminal group.

12. The semiconductor storage device as claimed in claim 1, wherein each of said plurality ofmemory chips has a bonding pad area, and said plurality of memory chips are connected to said base substrate by way of tape on which wiring is formed.

13. The semiconductor storage device as claimed in claim 1, wherein a first internal power supply voltage that is lower than an externally supplied high-level-side power supply voltage is applied as a high-level-side power supply voltage, and a second internal power supply voltage that is higher than the externally supplied low-level-side power supply voltage is applied as a low-level-side power supply voltage to an output buffer that is designed to provide output to said

plurality of memory chips and is selected from the output buffers included in said single chip that has the interface function.

14. The semiconductor storage device as claimed in claim 1, wherein said plurality of memory chips have a test pad in addition to an ordinary pad designed for actual use, said test pad is connected to a memory array at least via a buffer circuit, and said ordinary pad bypasses said buffer circuit and connects to said memory array.

15. A semiconductor storage device comprising:

a base substrate having a command/address external terminal group to which command signals and address signals are supplied and a single chip select external terminal to which a chip select signal is supplied;

an interface chip that is mounted on the base substrate and is connected to the command/address external terminal group and the chip select external terminal; and

a plurality of memory chips that are stacked on the base substrate and are each individually capable of reading and writing operations,

wherein said interface chip can individually activate said plurality of memory chips based on said address signals and said chip select signal.

16. The semiconductor storage device as claimed in claim 15, wherein at least one of the signals selected from said command signals and said address signals are transmitted between said plurality of memory chips and said interface chip via wiring with a shared connection to said plurality of memory chips.

17. The semiconductor storage device as claimed in claim 15, wherein at least one of the signals selected from said command signals and said address signals are transmitted between said plurality of memory chips and said interface chip via wiring that is individually connected to the plurality of memory chips.

18. A semiconductor storage device comprising:

a base substrate having a command/address external terminal group to which command signals and address signals are supplied and a single chip select external terminal to which a chip select signal is supplied; and

a plurality of memory chips that are stacked on the base substrate and are each individually capable of reading and writing operations,

wherein one of said plurality of memory chips is connected to the command/address external terminal group and the chip select external terminal and can individually activate said plurality of memory chips based on said address signals and said chip select signal.

19. The semiconductor storage device as claimed in claim 18, wherein at least one of the signals selected from said command signals and said address signals are transmitted between said one of said plurality of memory chips and a remaining memory chips via wiring with a shared connection to said remaining memory chips.

20. The semiconductor storage device as claimed in claim 18, wherein at least one of the signals selected from said command signals and said address signals are transmitted between said one of said plurality of memory chips and a remaining memory chips via wiring that is individually connected to the remaining memory chips.

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 816 570 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
08.08.2007 Bulletin 2007/32

(51) Int Cl.:
G06F 13/16 *(2006.01)*

(21) Application number: **06125954.5**

(22) Date of filing: **16.04.1991**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **18.04.1990 US 510898**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
00100018.1 / 1 022 641
91908374.1 / 0 525 068

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This application was filed on 12 - 12 - 2006 as a divisional application to the application mentioned under INID code 62.

(54) Integrated circuit I/O using a high performance bus interface

(57) The present invention includes a semiconductor device, the semiconductor device comprising connection means adapted to connect the semiconductor device to an external bus which is a part of a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data, control and device select information needed by the semiconductor device for communication with substantially every other semiconductor device connected to the external bus, and wherein the external bus has substantially fewer bus lines than the number of bits in a single address, wherein each said bus line is a terminated transmission line, and wherein the external bus carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to the semiconductor device, a bus line driver capable of producing a low-voltage-swing signal on one of said terminated transmission lines, wherein the semiconductor device is a semiconductor transceiver device to interface multiple units to the bus, wherein the multiple units are DRAMs.

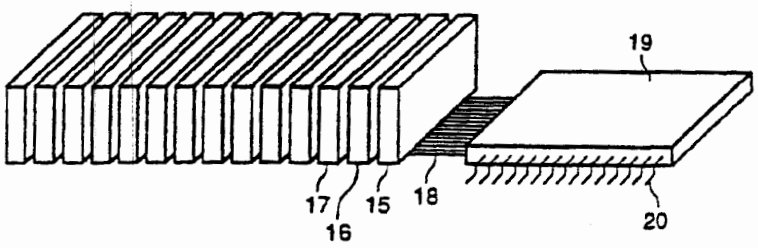

FIG. 3

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Printed by Jouve, 75001 PARIS (FR)

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Description

FIELD OF THE INVENTION

[0001] An integrated circuit bus interface for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described.

BACKGROUND OF THE INVENTION

[0002] Semiconductor computer memories have traditionally been designed and structured to use one memory device for each bit, or small group of bits, of any individual computer word, where the word size is governed by the choice of computer. Typical word sizes range from 4 to 64 bits. Each memory device typically is connected in parallel to a series of address lines and connected to one of a series of data lines. When the computer seeks to read from or write to a specific memory location, an address is put on the address lines and some or all of the memory devices are activated using a separate device select line for each needed device. One or more devices may be connected to each data line but typically only a small number of data lines are connected to a single memory device. Thus data line 0 is connected to device(s) 0, data line 1 is connected to device(s) 1, and so on. Data is thus accessed or provided in parallel for each memory read or write operation. For the system to operate properly, every single memory bit in every memory device must operate dependably and correctly.

[0003] To understand the concept of the present invention, it is helpful to review the architecture of conventional memory devices. Internal to nearly all types of memory devices (including the most widely used Dynamic Random Access Memory (DRAM), Static RAM (SRAM) and Read Only Memory (ROM) devices), a large number of bits are accessed in parallel each time the system carries out a memory access cycle. However, only a small percentage of accessed bits which are available internally each time the memory device is cycled ever make it across the device boundary to the external world.

[0004] Referring to Fig. 1, all modern DRAM, SRAM and ROM designs have internal architectures with row (word) lines 5 and column (bit) lines 6 to allow the memory cells to tile a two dimensional area 1. One bit of data is stored at the intersection of each word and bit line. When a particular word line is enabled, all of the corresponding data bits are transferred onto the bit lines. Some prior art DRAMs take advantage of this organization to reduce the number of pins needed to transmit the address. The address of a given memory cell is split into two addresses, row and column, each of which can be multiplexed over a bus only half as wide as the memory cell address of the prior art would have required.

COMPARISON WITH PRIOR ART

[0005] Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Patent No. 3,821,715 (Hoff et. al.), was issued to Intel Corporation for the earliest 4-bit micro-processor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element is permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

[0006] In U.S. Patent No. 4,315,308 (Jackson), a bus connecting a single CPU to a bus interface unit is described. The invention uses multiplexed address, data, and control information over a single 16-bit wide bus. Block-mode operations are defined, with the length of the block sent as part of the control sequence. In addition, variable access-time operations using a "stretch" cycle signal are provided. There are no multiple processing elements and no capability for multiple outstanding requests, and again, not all of the interface signals are bused.

[0007] In U.S. Patent No. 4,449,207 (Kung, et. al.), a DRAM is described which multiplexes address and data on an internal bus. The external interface to this DRAM is conventional, with separate control, address and data connections.

[0008] In U.S. Patent Nos. 4,764,846 and 4,706,166 (Go), a 3-D package arrangement of stacked die with connections along a single edge is described. Such packages are difficult to use because of the point-to-point wiring required to interconnect conventional memory devices with processing elements. Both patents describe complex schemes for solving these problems. No attempt is made to solve the problem by changing the interface.

[0009] In U.S. Patent No. 3,969,706 (Proebsting, et. al.), the current state-of-the-art DRAM interface is described. The address is two-way multiplexed, and there are separate pins for data and control (RAS, CAS, WE, CS). The number of pins grows with the size of the DRAM, and many of the connections must be made point-to-point in a memory system using such DRAMs.

[0010] There are many backplane buses described in the prior art, but not in the combination described or having the

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features of this invention. Many backplane buses multiplex addresses and data on a single bus (e.g., the NU bus). ELXSI and others have implemented split-transaction buses (U.S. Patent No. 4,595,923 and 4,481,625 (Roberts)). ELXSI has also implemented a relatively low-voltage-swing current-mode ECL driver (approximately 1 V swing). Address-space registers are implemented on most backplane buses, as is some form of block mode operation.

[0011] Nearly all modern backplane buses implement some type of arbitration scheme, but the arbitration scheme used in this invention differs from each of these. U.S. Patent Nos. 4,837,682 (Culler), 4,818,985 (Ikeda), 4,779,089 (Theus) and 4,745,548 (Blahut) describe prior art schemes. All involve either log N extra signals, (Theus, Blahut), where N is the number of potential bus requestors, or additional delay to get control of the bus (Ikeda, Culler). None of the buses described in patents or other literature use only bused connections. All contain some point-to-point connections on the backplane. None of the other aspects of this invention such as power reduction by fetching each data block from a single device or compact and low-cost 3-D packaging even apply to backplane buses.

[0012] The clocking scheme used in this invention has not been used before and in fact would be difficult to implement in backplane buses due to the signal degradation caused by connector stubs. U.S. Patent No. 4,247,817 (Heller) describes a clocking scheme using two clock lines, but relies on ramp-shaped clock signals in contrast to the normal rise-time signals used in the present invention.

[0013] In U.S. Patent No. 4,646,279 (Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

[0014] One object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner.

[0015] Another object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices.

[0016] Another object of this invention is to allow mapping out defective memory devices or portions of memory devices.

[0017] Another object of this invention is to provide a method for distinguishing otherwise identical devices by assigning a unique identifier to each device.

[0018] Yet another object of this invention is to provide a method for transferring address, data and control information over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously.

[0019] Another object of this invention is to provide a method of distributing a high-speed memory cache within the DRAM chips of a memory system which is much more effective than previous cache methods.

[0020] Another object of this invention is to provide devices, especially DRAMs, suitable for use with the bus architecture of the invention.

SUMMARY OF INVENTION

[0021] The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

[0022] Referring to Fig. 2, a standard DRAM 13, 14, ROM (or SRAM) 12, microprocessor CPU 11, I/O device, disk controller or other special purpose device such as a high speed switch is modified to use a wholly bus-based interface rather than the prior art combination of point-to-point and bus-based wiring used with conventional versions of these devices. The new bus includes clock signals, power and multiplexed address, data and control signals. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide. Persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. The new bus is used to connect elements such as memory, peripheral, switch and processing units.

[0023] In the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus. Each memory device contains only a single bus interface with no other signal pins. Other devices that may be included in the system can connect to the bus and other non-bus lines, such as input/output lines. The bus supports large data block transfers and split transactions to allow a user to achieve high bus utilization. This ability to rapidly read or write a large block of data to one single device at a time is an important advantage of this invention.

[0024] The DRAMs that connect to this bus differ from conventional DRAMs in a number of ways. Registers are

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provided which may store control information, device identification, device-type and other information appropriate for the chip such as the address range for each independent portion of the device. New bus interface circuits must be added and the internals of prior art DRAM devices need to be modified so they can provide and accept data to and from the bus at the peak data rate of the bus. This requires changes to the column access circuitry in the DRAM, with only a minimal increase in die size. A circuit is provided to generate a low skew internal device clock for devices on the bus, and other circuits provide for demultiplexing input and multiplexing output signals.

[0025] High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The bus lines are controlled-impedance, doubly-terminated lines. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5 - 2 nH. Each device 15, 16, 17, shown in Figure 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

[0026] A primary result of the architecture of this invention is to increase the bandwidth of DRAM access. The invention also reduces manufacturing and production costs, power consumption, and increases packing density and system reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027]

Figure 1 is a diagram which illustrates the basic 2-D organization of memory devices.
Figure 2 is a schematic block diagram which illustrates the parallel connection of all bus lines and the serial Reset line to each device in the system.
Figure 3 is a perspective view of a system of the invention which illustrates the 3-D packaging of semiconductor devices on the primary bus.
Figure 4 shows the format of a request packet.
Figure 5 shows the format of a retry response from a slave.
Figure 6 shows the bus cycles after a request packet collision occurs on the bus and how arbitration is handled.
Figure 7 shows the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.
Figure 8 shows the connection and timing between bus clocks and devices on the bus.
Figure 9 is a perspective view showing how transceivers can be used to connect a number of bus units to a transceiver bus. Figure 10 is a block and schematic diagram of input/output circuitry used to connect devices to the bus.
Figure 11 is a schematic diagram of a clocked sense-amplifier used as a bus input receiver.
Figure 12 is a block diagram showing how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines.
Figure 13 is a timing diagram showing the relationship of signals in the block diagram of Figure 12.
Figure 14 is timing diagram of a preferred means of implementing the reset procedure of this invention.
Figure 15 is a diagram illustrating the general organization of a 4 Mbit DRAM divided into 8 subarrays.

DETAILED DESCRIPTION

[0028] The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. The invention can also be used to connect processing devices and other devices, such as I/O interfaces or disk controllers, with or without memory devices on the bus. The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024 bytes) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation).

[0029] Virtually all of the signals needed by a computer system can be sent over the bus. Persons skilled in the art recognize that certain devices, such as CPUs, may be connected to other signal lines and possibly to independent buses, for example a bus to an independent cache memory, in addition to the bus of this invention. Certain devices, for

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example cross-point switches, could be connected to multiple, independent buses of this invention. In the preferred implementation, memory devices are provided that have no connections other than the bus connections described herein and CPUs are provided that use the bus of this invention as the principal, if not exclusive, connection to memory and to other devices on the bus.

[0030] All modern DRAM, SRAM and ROM designs have internal architectures with row (word) and column (bit) lines to efficiently tile a 2-D area. Referring to Fig. 1, one bit of data is stored at the intersection of each word line 5 and bit line 6. When a particular word line is enabled, all of the corresponding data bits are transferred onto the bit lines. This data, about 4000 bits at a time in a 4 MBit DRAM, is then loaded into column sense amplifiers 3 and held for use by the I/O circuits.

[0031] In the invention presented here, the data from the sense amplifiers is enabled 32 bits at a time onto an internal device bus running at approximately 125 MHz. This internal device bus moves the data to the periphery of the devices where the data is multiplexed into an 8-bit wide external bus interface, running at approximately 500 MHz.

[0032] The bus architecture of this invention connects master or bus controller devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and slave devices, such as DRAM, SRAM or ROM memory devices. A slave device responds to control signals; a master sends control signals. Persons skilled in the art realize that some devices may behave as both master and slave at various times, depending on the mode of operation and the state of the system. For example, a memory device will typically have only slave functions, while a DMA controller, disk controller or CPU may include both slave and master functions. Many other semiconductor devices, including I/O devices, disk controllers, or other special purpose devices such as high speed switches can be modified for use with the bus of this invention.

[0033] Each semiconductor device contains a set of internal registers, preferably including a device identification (device ID) register, a device-type descriptor register, control registers and other registers containing other information relevant to that type of device. In a preferred implementation, semiconductor devices connected to the bus contain registers which specify the memory addresses contained within that device and access-time registers which store a set of one or more delay times at which the device can or should be available to send or receive data.

[0034] Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset. During the initialization sequence each device on the bus is assigned a unique device ID number, which is stored in the device ID register. A bus master can then use these device ID numbers to access and set appropriate registers in other devices, including access-time registers, control registers, and memory registers, to configure the system. Each slave may have one or several access-time registers (four in a preferred embodiment). In a preferred embodiment, one access-time register in each slave is permanently or semi-permanently programmed with a fixed value to facilitate certain control functions. A preferred implementation of an initialization sequence is described below in more detail.

[0035] All information sent between master devices and slave devices is sent over the external bus, which, for example, may be 8 bits wide. This is accomplished by defining a protocol whereby a master device, such as a microprocessor, seizes exclusive control of the external bus (i.e., becomes the bus master) and initiates a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus. An address can consist of 16 to 40 or more bits according to the teachings of this invention. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. The requesting master may also need to transact certain internal processes before the bus transaction begins. After a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus. More than one access time can be provided to allow different types of responses to occur at different times.

[0036] A request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses. Thus multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data. Transfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block.

Device Address Mapping

[0037] Another unique aspect of this invention is that each memory device is a complete, independent memory sub-system with all the functionality of a prior art memory board in a conventional backplane-bus computer system. Individual memory devices may contain a single memory section or may be subdivided into more than one discrete memory section. Memory devices preferably include memory address registers for each discrete memory section. A failed memory device (or even a subsection of a device) can be "mapped out" with only the loss of a small fraction of the memory, maintaining essentially full system capability. Mapping out bad devices can be accomplished in two ways, both compatible with this

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invention.

[0038] The preferred method uses address registers in each memory device (or independent discrete portion thereof) to store information which defines the range of bus addresses to which this memory device will respond. This is similar to prior art schemes used in memory boards in conventional backplane bus systems. The address registers can include a single pointer, usually pointing to a block of known size, a pointer and a fixed or variable block size value or two pointers, one pointing to the beginning and one to the end (or to the "top" and "bottom") of each memory block. By appropriate settings of the address registers, a series of functional memory devices or discrete memory sections can be made to respond to a contiguous range of addresses, giving the system access to a contiguous block of good memory, limited primarily by the number of good devices connected to the bus. A block of memory in a first memory device or memory section can be assigned a certain range of addresses, then a block of memory in a next memory device or memory section can be assigned addresses starting with an address one higher (or lower, depending on the memory structure) than the last address of the previous block.

[0039] Preferred devices for use in this invention include device-type register information specifying the type of chip, including how much memory is available in what configuration on that device. A master can perform an appropriate memory test, such as reading and writing each memory cell in one or more selected orders, to test proper functioning of each accessible discrete portion of memory (based in part on information like device ID number and device-type) and write address values (up to 40 bits in the preferred embodiment, 10^{12} bytes), preferably contiguous, into device address-space registers. Non-functional or impaired memory sections can be assigned a special address value which the system can interpret to avoid using that memory.

[0040] The second approach puts the burden of avoiding the bad devices on the system master or masters. CPUs and DMA controllers typically have some sort of translation look-aside buffers (TLBs) which map virtual to physical (bus) addresses. With relatively simple software, the TLBs can be programmed to use only working memory (data structures describing functional memories are easily generated). For masters which don't contain TLBs (for example, a video display generator), a small, simple RAM can be used to map a contiguous range of addresses onto the addresses of the functional memory devices.

[0041] Either scheme works and permits a system to have a significant percentage of non-functional devices and still continue to operate with the memory which remains. This means that systems built with this invention will have much improved reliability over existing systems, including the ability to build systems with almost no field failures.

Bus

[0042] The preferred bus architecture of this invention comprises 11 signals: BusData[0:7]; AddrValid; Clkl and Clk2; plus an input reference level and power and ground lines connected in parallel to each device. Signals are driven onto the bus during conventional bus cycles. The notation "Signal[i:j]" refers to a specific range of signals or lines, for example, BusData[0:7] means BusData0, BusData1, ..., BusData7. The bus lines for BusData[0:7] signals form a byte-wide, multiplexed data/address/control bus. AddrValid is used to indicate when the bus is holding a valid address request, and instructs a slave to decode the bus data as an address and, if the address is included on that slave, to handle the pending request. The two clocks together provide a synchronized, high speed clock for all the devices on the bus. In addition to the bused signals, there is one other line (ResetIn, ResetOut) connecting each device in series for use during initialization to assign every device in the system a unique device ID number (described below in detail).

[0043] To facilitate the extremely high data rate of this external bus relative to the gate delays of the internal logic, the bus cycles are grouped into pairs of even/odd cycles. Note that all devices connected to a bus should preferably use the same even/odd labeling of bus cycles and preferably should begin operations on even cycles. This is enforced by the clocking scheme.

Protocol and Bus Operation

[0044] The bus uses a relatively simple, synchronous, split-transaction, block-oriented protocol for bus transactions. One of the goals of the system is to keep the intelligence concentrated in the masters, thus keeping the slaves as simple as possible (since there are typically many more slaves than masters). To reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase. The time for this bus access phase is known to all devices on the bus - each master being responsible for making sure that the bus will be free when the bus access begins. Thus the slaves never worry about arbitrating for the bus. This approach eliminates arbitration in single master systems, and also makes the slave-bus interface simpler.

[0045] In a preferred implementation of the invention, to initiate a bus transfer over the bus, a master sends out a request packet, a contiguous series of bytes containing address and control information. It is preferable to use a request packet containing an even number of bytes and also preferable to start each packet on an even bus cycle.

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[0046] The device-select function is handled using the bus data lines. AddrValid is driven, which instructs all slaves to decode the request packet address, determine whether they contain the requested address, and if they do, provide the data back to the master (in the case of a read request) or accept data from the master (in the case of a write request) in a data block transfer. A master can also select a specific device by transmitting a device ID number in a request packet. In a preferred implementation, a special device ID number is chosen to indicate that the packet should be interpreted by all devices on the bus. This allows a master to broadcast a message, for example to set a selected control register of all devices with the same value.

[0047] The data block transfer occurs later at a time specified in the request packet control information, preferably beginning on an even cycle. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers. The timing of data for reads and writes is preferably the same; the only difference is which device drives the bus. For reads, the slave drives the bus and the master latches the values from the bus. For writes the master drives the bus and the selected slave latches the values from the bus.

[0048] In a preferred implementation of this invention shown in Figure 4, a request packet 22 contains 6 bytes of data -- 4.5 address bytes and 1.5 control bytes. Each request packet uses all nine bits of the multiplexed data/address lines (AddrValid 23 + BusData[0:7] 24) for all six bytes of the request packet. Setting 23 AddrValid = 1 in an otherwise unused even cycle indicates the start of an request packet (control information). In a valid request packet, AddrValid 27 must be 0 in the last byte. Asserting this signal in the last byte invalidates the request packet. This is used for the collision detection and arbitration logic (described below). Bytes 25-26 contain the first 35 address bits, Address[0:35]. The last byte contains AddrValid 27 (the invalidation switch) and 28, the remaining address bits, Address[36:39], and BlockSize [0:3] (control information).

[0049] The first byte contains two 4 bit fields containing control information, AccessType[0:3], an op code (operation code) which, for example, specifies the type of access, and Master[0:3], a position reserved for the master sending the packet to include its master ID number. Only master numbers 1 through 15 are allowed - master number 0 is reserved for special system commands. Any packet with Master[0:3] = 0 is an invalid or special packet and is treated accordingly.

[0050] The AccessType field specifies whether the requested operation is a read or write and the type of access, for example, whether it is to the control registers or other parts of the device, such as memory. In a preferred implementation, AccessType[0] is a Read/Write switch: if it is a 1, then the operation calls for a read from the slave (the slave to read the requested memory block and drive the memory contents onto the bus); if it is a 0, the operation calls for a write into the slave (the slave to read data from the bus and write it to memory). AccessType[1:3] provides up to 8 different access types for a slave. AccessType[1:2] preferably indicates the timing of the response, which is stored in an access-time register, AccessRegN. The choice of access-time register can be selected directly by having a certain op code select that register, or indirectly by having a slave respond to selected op codes with pre-selected access times (see table below). The remaining bit, AccessType[3] may be used to send additional information about the request to the slaves.

[0051] One special type of access is control register access, which involves addressing a selected register in a selected slave. In the preferred implementation of this invention, AccessType[1:3] equal to zero indicates a control register request and the address field of the packet indicates the desired control register. For example, the most significant two bytes can be the device ID number (specifying which slave is being addressed) and the least significant three bytes can specify a register address and may also represent or include data to be loaded into that control register. Control register accesses are used to initialize the access-time registers, so it is preferable to use a fixed response time which can be preprogrammed or even hard wired, for example the value in AccessReg0, preferably 8 cycles. Control register access can also be used to initialize or modify other registers, including address registers.

[0052] The method of this invention provides for access mode control specifically for the DRAMs. One such access mode determines whether the access is page mode or normal RAS access. In normal mode (in conventional DRAMS and in this invention), the DRAM column sense amps or latches have been precharged to a value intermediate between logical 0 and 1. This precharging allows access to a row in the RAM to begin as soon as the access request for either inputs (writes) or outputs (reads) is received and allows the column sense amps to sense data quickly. In page mode (both conventional and in this invention), the DRAM holds the data in the column sense amps or latches from the previous read or write operation. If a subsequent request to access data is directed td the same row, the DRAM does not need to wait for the data to be sensed (it has been sensed already) and access time for this data is much shorter than the normal access time. Page mode generally allows much faster access to data but to a smaller block of data (equal to the number of sense amps). However, if the requested data is not in the selected row, the access time is longer than the normal access time, since the request must wait for the RAM to precharge before the normal mode access can start. Two access-time registers in each DRAM preferably contain the access times to be used for normal and for page-mode accesses, respectively.

[0053] The access mode also determines whether the DRAM should precharge the sense amplifiers or should save the contents of the sense amps for a subsequent page mode access. Typical settings are "precharge after normal

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access" and "save after page mode access" but "precharge after page mode access" or "save after normal access" are allowed, selectable modes of operation. The DRAM can also be set to precharge the sense amps if they are not accessed for a selected period of time.

[0054] In page mode, the data stored in the DRAM sense amplifiers may be accessed within much less time than it takes to read out data in normal mode (~10-20 nS vs. 40-100 nS). This data may be kept available for long periods. However, if these sense amps (and hence bit lines) are not precharged after an access, a subsequent access to a different memory word (row) will suffer a precharge time penalty of about 40-100 nS because the sense amps must precharge before latching in a new value.

[0055] The contents of the sense amps thus may be held and used as a cache, allowing faster, repetitive access to small blocks of data. DRAM-based page-mode caches have been attempted in the prior art using conventional DRAM organizations but they are not very effective because several chips are required per computer word. Such a conventional page-mode cache contains many bits (for example, 32 chips x 4Kbits) but has very few independent storage entries. In other words, at any given point in time the sense amps hold only a few different blocks or memory "locales" (a single block of 4K words, in the example above). Simulations have shown that upwards of 100 blocks are required to achieve high hit rates (>90% of requests find the requested data already in cache memory) regardless of the size of each block. *See, for* example, Anant Agarwal, et. al., "An Analytic Cache Model," ACM Transactions on Computer Systems, Vol. 7 (2), pp. 184-215 (May 1989).

[0056] The organization of memory in the present invention allows each DRAM to hold one or more (4 for 4MBit DRAMS) separately- addressed and independent blocks of data. A personal computer or workstation with 100 such DRAMs (i.e. 400 blocks or locales) can achieve extremely high, very repeatable hit rates (98-99% on average) as compared to the lower (50-80%), widely varying hit rates using DRAMS organized in the conventional fashion. Further, because of the time penalty associated with the deferred precharge on a "miss" of the page-mode cache, the conventional DRAM-based page-mode cache generally has been found to work less well than no cache at all.

[0057] For DRAM slave access, the access types are preferably used in the following way:

AccessType[1:3]	Use	AccessTime
0	Control Register Access	Fixed, 8[AccessReg0]
1	Unused	Fixed, 8[AccessReg0]
2-3	Unused	AccessReg1
4-5	Page Mode DRAM access	AccessReg2
6-7	Normal DRAM access	AccessReg3

Persons skilled in the art will recognize that a series of available bits could be designated as switches for controlling these access modes. For example:

AccessType[2] = page mode/normal switch

AccessType[3] = precharge/save-data switch

BlockSize[0:3] specifies the size of the data block transfer. If BlockSize[0] is 0, the remaining bits are the binary representation of the block size (0-7). If BlockSize[0] is 1, then the remaining bits give the block size as a binary power of 2, from 8 to 1024. A zero-length block can be interpreted as a special command, for example, to refresh a DRAM without returning any data, or to change the DRAM from page mode to normal access mode or vice-versa.

BlockSize[0:2]	Number of Bytes in Block
0-7	0-7 respectively
8	8
9	16
10	32
11	64
12	128
13	256
14	512
15	1024

Persons skilled in the art will recognize that other block size encoding schemes or values can be used.

[0058] In most cases, a slave will respond at the selected access time by reading or writing data from or to the bus over bus lines BusData[0:7] and AddrValid will be at logical 0. In a preferred embodiment, substantially each memory

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access will involve only a single memory device, that is, a single block will be read from or written to a single memory device.

Retry Format

[0059] In some cases, a slave may not be able to respond correctly to a request, e.g., for a read or write. In such a situation, the slave should return an error message, sometimes called a N(o)ACK(nowledge) or retry message. The retry message can include information about the condition requiring a retry, but this increases system requirements for circuitry in both slave and masters. A simple message indicating only that an error has occurred allows for a less complex slave, and the master can take whatever action is needed to understand and correct the cause of the error.

[0060] For example, under certain conditions a slave might not be able to supply the requested data. During a page-mode access, the DRAM selected must be in page mode and the requested address must match the address of the data held in the sense amps or latches. Each DRAM can check for this match during a page-mode access. If no match is found, the DRAM begins precharging and returns a retry message to the master during the first cycle of the data block (the rest of the returned block is ignored). The master then must wait for the precharge time (which is set to accommodate the type of slave in question, stored in a special register, PreChargeReg), and then resend the request as a normal DRAM access (AccessType = 6 or 7).

[0061] In the preferred form of the present invention, a slave signals a retry by driving AddrValid true at the time the slave was supposed to begin reading or writing data. A master which expected to write to that slave must monitor AddrValid during the write and take corrective action if it detects a retry message. Figure 5 illustrates the format of a retry message 28 which is useful for read requests, consisting of 23 AddrValid=1 with Master[0:3] = 0 in the first (even) cycle. Note that AddrValid is normally 0 for data block transfers and that there is no master 0 (only 1 through 15 are allowed). All DRAMs and masters can easily recognize such a packet as an invalid request packet, and therefore a retry message. In this type of bus transaction all of the fields except for Mastery[0:3] and AddrValid 23 may be used as information fields, although in the implementation described, the contents are undefined. Persons skilled in the art recognize that another method of signifying a retry message is to add a DataInvalid line and signal to the bus. This signal could be asserted in the case of a NACK.

Bus Arbitration

[0062] In the case of a single master, there are by definition no arbitration problems. The master sends request packets and keeps track of periods when the bus will be busy in response to that packet. The master can schedule multiple requests so that the corresponding data block transfers do not overlap.

[0063] The bus architecture of this invention is also useful in configurations with multiple masters. When two or more masters are on the same bus, each master must keep track of all the pending transactions, so each master knows when it can send a request packet and access the corresponding data block transfer. Situations will arise, however, where two or more masters send a request packet at about the same time and the multiple requests must be detected, then sorted out by some sort of bus arbitration.

[0064] There are many ways for each master to keep track of when the bus is and will be busy. A simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free.

[0065] With two or more masters on the bus, masters will occasionally transmit independent request packets during the same bus cycle. Those multiple requests will collide as each such master drives the bus simultaneously with different information, resulting in scrambled request information and neither desired data block transfer. In a preferred form of the invention, each device on the bus seeking to write a logical 1 on a BusData or AddrValid line drives that line with a current sufficient to sustain a voltage greater than or equal to the high-logic value for the system. Devices do not drive lines that should have a logical 0; those lines are simply held at a voltage corresponding to a low-logic value. Each master tests the voltage on at least some, preferably all, bus data and the AddrValid lines so the master can detect a logical '1' where the expected level is '0' on a line that it does not drive during a given bus cycle but another master does drive.

[0066] Another way to detect collisions is to select one or more bus lines for collision signalling. Each master sending a request drives that line or lines and monitors the selected lines for more than the normal drive current (or a logical value of ">1"), indicating requests by more than one master. Persons skilled in the art will recognize that this can be implemented with a protocol involving BusData and AddrValid lines or could be implemented using an additional bus line.

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[0067] In the preferred form of this invention, each master detects collisions by monitoring lines which it does not drive to see if another master is driving those lines. Referring to Fig. 4, the first byte of the request packet includes the number of each master attempting to use the bus (Master[0:3]). If two masters send packet requests starting at the same point in time, the master numbers will be logical "or"ed together by at least those masters, and thus one or both of the masters, by monitoring the data on the bus and comparing what it sent, can detect a collision. For instance if requests by masters number 2 (0010) and 5 (0101) collide, the bus will be driven with the value Master[0:3]=7 (0010 + 0101 = 0111). Master number 5 will detect that the signal Master[2] = 1 and master 2 will detect that Master[1] and Master[3] = 1, telling both masters that a collision has occurred. Another example is masters 2 and 11, for which the bus will be driven with the value Master[0:3]=11 (0010 + 1011 = 1011), and although master 11 can't readily detect this collision, master 2 can. When any collision is detected, each master detecting a collision drives the value of AddrValid 27 in byte 5 of the request packet 22 to 1, which is detected by all masters, including master 11 in the second example above, and forces a bus arbitration cycle, described below.

[0068] Another collision condition may arise where master A sends a request packet in cycle 0 and master B tries to send a request packet starting in cycle 2 of the first request packet, thereby overlapping the first request packet. This will occur from time to time because the bus operates at high speeds, thus the logic in a second-initiating master may not be fast enough to detect a request initiated by a first master in cycle 0 and to react fast enough by delaying its own request. Master B eventually notices that it wasn't supposed to try to send a request packet (and consequently almost surely destroyed the address that master A was trying to send), and, as in the example above of a simultaneous collision, drives a 1 on AddrValid during byte 5 of the first request packet 27 forcing an arbitration. The logic in the preferred implementation is fast enough that a master should detect a request packet by another master by cycle 3 of the first request packet, so no master is likely to attempt to send a potentially colliding request packet later than cycle 2.

[0069] Slave devices not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid. A request packet with Master[0:3] equal to 0 (a retry signal) is ignored and does not cause a collision. The subsequent bytes of such a packet are ignored.

[0070] To begin arbitration after a collision, the masters wait a preselected number of cycles after the aborted request packet (4 cycles in a preferred implementation), then use the next free cycle to arbitrate for the bus (the next available even cycle in the preferred implementation). Each colliding master signals to all other colliding masters that it seeks to send a request packet, a priority is assigned to each of the colliding masters, then each master is allowed to make its request in the order of that priority.

[0071] Figure 6 illustrates one preferred way of implementing this arbitration. Each colliding master signals its intent to send a request packet by driving a single BusData line during a single bus cycle corresponding to its assigned master number (1-15 in the present example). During two-byte arbitration cycle 29, byte 0 is allocated to requests 1-7 from masters 1-7, respectively, (bit 0 is not used) and byte 1 is allocated to requests 8-15 from masters 8-15, respectively. At least one device and preferably each colliding master reads the values on the bus during the arbitration cycles to determine and store which masters desire to use the bus. Persons skilled in the art will recognize that a single byte can be allocated for arbitration requests if the system includes more bus lines than masters. More than 15 masters can be accommodated by using additional bus cycles.

[0072] A fixed priority scheme (preferably using the master numbers, selecting lowest numbers first) is then used to prioritize, then sequence the requests in a bus arbitration queue which is maintained by at least one device. These requests are queued by each master in the bus-busy data structure and no further requests are allowed until the bus arbitration queue is cleared. Persons skilled in the art will recognize that other priority schemes can be used, including assigning priority according to the physical location of each master.

System Configuration/Reset

[0073] In the bus-based system of this invention, a mechanism is provided to give each device on the bus a unique device identifier (device ID) after power-up or under other conditions as desired or needed by the system. A master can then use this device ID to access a specific device, particularly to set or modify registers of the specified device, including the control and address registers. In the preferred embodiment, one master is assigned to carry out the entire system configuration process. The master provides a series of unique device ID numbers for each unique device connected to the bus system. In the preferred embodiment, each device connected to the bus contains a special device-type register which specifies the type of device, for instance CPU, 4 MBit memory, 64 MBit memory or disk controller. The configuration master should check each device, determine the device type and set appropriate control registers, including access-time registers. The configuration master should check each memory device and set all appropriate memory address registers.

[0074] One means to set up unique device ID numbers is to have each device to select a device ID in sequence and store the value in an internal device ID register. For example, a master can pass sequential device ID numbers through shift registers in each of a series of devices, or pass a token from device to device whereby the device with the token

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reads in device ID information from another line or lines. In a preferred embodiment, device ID numbers are assigned to devices according to their physical relationship, for instance, their order along the bus.

[0075] In a preferred embodiment of this invention, the device ID setting is accomplished using a pair of pins on each device, ResetIn and ResetOut. These pins handle normal logic signals and are used only during device ID configuration. On each rising edge of the clock, each device copies ResetIn (an input) into a four-stage reset shift register. The output of the reset shift register is connected to ResetOut, which in turn connects to ResetIn for the next sequentially connected device. Substantially all devices on the bus are thereby daisy-chained together. A first reset signal, for example, while ResetIn at a device is a logical 1, or when a selected bit of the reset shift register goes from zero to non-zero, causes the device to hard reset, for example by clearing all internal registers and resetting all state machines. A second reset signal, for example, the falling edge of ResetIn combined with changeable values on the external bus, causes that device to latch the contents of the external bus into the internal device ID register (Device[0:7]).

[0076] To reset all devices on a bus, a master sets the ResetIn line of the first device to a "1" for long enough to ensure that all devices on the bus have been reset (4 cycles times the number of devices -- note that the maximum number of devices on the preferred bus configuration is 256 (8 bits), so that 1024 cycles is always enough time to reset all devices.) Then ResetIn is dropped to "0" and the BusData lines are driven with the first followed by successive device ID numbers, changing after every 4 clock pulses. Successive devices set those device ID numbers into the corresponding device ID register as the falling edge of ResetIn propagates through the shift registers of the daisy-chained devices. Figure 14 shows ResetIn at a first device going low while a master drives a first device ID onto the bus data lines BusData[0:3]. The first device then latches in that first device ID. After four clock cycles, the master changes BusData[0:3] to the next device ID number and ResetOut at the first device goes low, which pulls ResetIn for the next daisy-chained device low, allowing the next device to latch in the next device ID number from BusData[0:3]. In the preferred embodiment, one master is assigned device ID 0 and it is the responsibility of that master to control the ResetIn line and to drive successive device ID numbers onto the bus at the appropriate times. In the preferred embodiment, each device waits two clock cycles after ResetIn goes low before latching in a device ID number from BusData[0:3].

[0077] Persons skilled in the art recognize that longer device ID numbers could be distributed to devices by having each device read in multiple bytes from the bus and latch the values into the device ID register. Persons skilled in the art also recognize that there are alternative ways of getting device ID numbers to unique devices. For instance, a series of sequential numbers could be clocked along the ResetIn line and at a certain time each device could be instructed to latch the current reset shift register value into the device ID register.

[0078] The configuration master should choose and set an access time in each access-time register in each slave to a period sufficiently long to allow the slave to perform an actual, desired memory access. For example, for a normal DRAM access, this time must be longer than the row address strobe (RAS) access time. If this condition is not met, the slave may not deliver the correct data. The value stored in a slave access-time register is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request. Thus an access time value of '1' would indicate that the slave should not access the bus until at least two cycles after the last byte of the request packet has been received. The value of AccessReg0 is preferably fixed at 8 (cycles) to facilitate access to control registers.

[0079] The bus architecture of this invention can include more than one master device. The reset or initialization sequence should also include a determination of whether there are multiple masters on the bus, and if so to assign unique master ID numbers to each. Persons skilled in the art will recognize that there are many ways of doing this. For instance, the master could poll each device to determine what type of device it is, for example, by reading a special register then, for each master device, write the next available master ID number into a special register.

ECC

[0080] Error detection and correction ("ECC") methods well known in the art can be implemented in this system. ECC information typically is calculated for a block of data at the time that block of data is first written into memory. The data block usually has an integral binary size, e.g. 256 bits, and the ECC information uses significantly fewer bits. A potential problem arises in that each binary data block in prior art schemes typically is stored with the ECC bits appended, resulting in a block size that is not an integral binary power.

[0081] In a preferred embodiment of this invention, ECC information is stored separately from the corresponding data, which can then be stored in blocks having integral binary size. ECC information and corresponding data can be stored, for example, in separate DRAM devices. Data can be read without ECC using a single request packet, but to write or read error-corrected data requires two request packets, one for the data and a second for the corresponding ECC information. ECC information may not always be stored permanently and in some situations the ECC information may be available without sending a request packet or without a bus data block transfer.

[0082] In a preferred embodiment, a standard data block size can be selected for use with ECC, and the ECC method will determine the required number of bits of information in a corresponding ECC block. RAMs containing ECC information

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can be programmed to store an access time that is equal to: (1) the access time of the normal RAM (containing data) plus the time to access a standard data block (for corrected data) minus the time to send a request packet (6 bytes); or (2) the access time of a normal RAM minus the time to access a standard ECC block minus the time to send a request packet. To read a data block and the corresponding ECC block, the master simply issues a request for the data immediately followed by a request for the ECC block. The ECC RAM will wait for the selected access time then drive its data onto the bus right after (in case (1) above)) the data RAM has finished driving out the data block. Persons skilled in the art will recognize that the access time described in case (2) above can be used to drive ECC data before the data is driven onto the bus lines and will recognize that writing data can be done by analogy with the method described for a read. Persons skilled in the art will also recognize the adjustments that must be made in the bus-busy structure and the request packet arbitration methods of this invention in order to accommodate these paired ECC requests.

[0083] Since this system is quite flexible, the system designer can choose the size of the data blocks and the number of ECC bits using the memory devices of this invention. Note that the data stream on the bus can be interpreted in various ways. For instance the sequence can be 2^n data bytes followed by 2^m ECC bytes (or vice versa), or the sequence can be 2^k iterations of 8 data bytes plus 1 ECC byte. Other information, such as information used by a directory-based cache coherence scheme, can also be managed this way. See, for example, Anant Agarwal, et al., "Scaleable Directory Schemes for Cache Consistency," 15th International Symposium on Computer Architecture, June 1988, pp. 280-289. Those skilled in the art will recognize alternative methods of implementing ECC schemes that are within the teachings of this invention.

Low Power 3-D Packaging

[0084] Another major advantage of this invention is that it drastically reduces the memory system power consumption. Nearly all the power consumed by a prior art DRAM is dissipated in performing row access. By using a single row access in a single RAM to supply all the bits for a block request (compared to a row-access in each of multiple RAMs in conventional memory systems) the power per bit can be made very small. Since the power dissipated by memory devices using this invention is significantly reduced, the devices potentially can be placed much closer together than with conventional designs.

[0085] The bus architecture of this invention makes possible an innovative 3-D packaging technology. By using a narrow, multiplexed (time-shared) bus, the pin count for an arbitrarily large memory device can be kept quite small - on the order of 20 pins. Moreover, this pin count can be kept constant from one generation of DRAM density to the next. The low power dissipation allows each package to be smaller, with narrower pin pitches (spacing between the IC pins). With current surface mount technology supporting pin pitches as low as 20 mils, all off-device connections can be implemented on a single edge of the memory device. Semiconductor die useful in this invention preferably have connections or pads along one edge of the die which can then be wired or otherwise connected to the package pins with wires having similar lengths. This geometry also allows for very short leads, preferably with an effective lead length of less than 4 mm. Furthermore, this invention uses only bused interconnections, i.e., each pad on each device is connected by the bus to the corresponding pad of each other device.

[0086] The use of a low pin count and an edge-connected bus permits a simple 3-D package, whereby the devices are stacked and the bus is connected along a single edge of the stack. The fact that all of the signals are bused is important for the implementation of a simple 3-D structure. Without this, the complexity of the "backplane" would be too difficult to make cost effectively with current technology. The individual devices in a stack of the present invention can be packed quite tightly because of the low power dissipated by the entire memory system, permitting the devices to be stacked bumper-to-bumper or top to bottom. Conventional plastic-injection molded small outline (SO) packages can be used with a pitch of about 2.5 mm (100 mils), but the ultimate limit would be the device die thickness, which is about an order of magnitude smaller, 0.2-0.5 mm using current wafer technology.

Bus Electrical Description

[0087] By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The bus of a preferred embodiment of the present invention consists of a set of resistor-terminated controlled impedance transmission lines which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity about $c/4$ (c = the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to leave 1 ns for the setup and hold time of the input receivers (described below) plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm for maximum performance. Lower performance systems may have much longer lines, e.g. a 4 ns bus

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may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

[0088] In the preferred embodiment, the bus uses current source drivers. Each output must be able to sink 50 mA, which provides an output swing of about 500 mV or more. In the preferred embodiment of this invention, the bus is active low. The unasserted state (the high value) is preferably considered a logical zero, and the asserted value (low state) is therefore a logical 1. Those skilled in the art understand that the method of this invention can also be implemented using the opposite logical relation to voltage. The value of the unasserted state is set by the voltage on the termination resistors, and should be high enough to allow the outputs to act as current sources, while being as low as possible to reduce power dissipation. These constraints may yield a termination voltage about 2V above ground in the preferred implementation. Current source drivers cause the output voltage to be proportional to the sum of the sources driving the bus.

[0089] Referring to Fig.7, although there is no stable condition where two devices drive the bus at the same time, conditions can arise because of propagation delay on the wires where one device, A 41, can start driving its part of the bus 44 while the bus is still being driven by another device, B 42 (already asserting a logical 1 on the bus). In a system using current drivers, when B 42 is driving the bus (before time 46), the value at points 44 and 45 is logical 1. If B 42 switches off at time 46 just when A 41 switches on, the additional drive by device A 41 causes the voltage at the output 44 of A 41 to drop briefly below the normal value. The voltage returns to its normal value at time 47 when the effect of device B 42 turning off is felt. The voltage at point 45 goes to logical 0 when device B 42 turns off, then drops at time 47 when the effect of device A 41 turning on is felt. Since the logical 1 driven by current from device A 41 is propagated irrespective of the previous value on the bus, the value on the bus is guaranteed to settle after one time of flight (t_f) delay, that is, the time it takes a signal to propagate from one end of the bus to the other. If a voltage drive was used (as in ECL wired-ORing), a logical 1 on the bus (from device B 42 being previously driven) would prevent the transition put out by device A 41 being felt at the most remote part of the system, e.g., device 43, until the turnoff waveform from device B 42 reached device A 41 plus one time of flight delay, giving a worst case settling time of twice the time of flight delay.

Clocking

[0090] Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks. Referring to Figure 8, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 from left to right, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far end to the origin, propagating from right to left. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.

[0091] Figure 8b illustrates how each device 51, 52 receives each of the two bus clock signals at a different time (because of propagation delay along the wires), with constant midpoint in time between the two bus clocks along the bus. At each device 51, 52, the rising edge 55 of Clock1 53 is followed by the rising edge 56 of Clock2 54. Similarly, the falling edge 57 of Clock1 53 is followed by the falling edge 58 of Clock2 54. This waveform relationship is observed at all other devices along the bus. Devices which are closer to the clock generator have a greater separation between Clock1 and Clock2 relative to devices farther from the generator because of the longer time required for each clock pulse to traverse the bus and return along line 54, but the midpoint in time 59, 60 between corresponding rising or falling edges is fixed because, for any given device, the length of each clock line between the far end of the bus and that device is equal. Each device must sample the two bus clocks and generate its own internal device clock at the midpoint of the two.

[0092] Clock distribution problems can be further reduced by using a bus clock and device clock rate equal to the bus cycle data rate divided by two, that is, the bus clock period is twice the bus cycle period. Thus a 500 MHz bus preferably uses a 250 MHz clock rate. This reduction in frequency provides two benefits. First it makes all signals on the bus have the same worst case data rates -- data on a 500 MHz bus can only change every 2 ns. Second, clocking at half the bus cycle data rate makes the labeling of the odd and even bus cycles trivial, for example, by defining even cycles to be those when the internal device clock is 0 and odd cycles when the internal device clock is 1.

Multiple Buses

[0093] The limitation on bus length described above restricts the total number of devices that can be placed on a single bus. Using 2.5 mm spacing between devices, a single 8 cm bus will hold about 32 devices. Persons skilled in the art will recognize certain applications of the present invention wherein the overall data rate on the bus is adequate but memory or processing requirements necessitate a much larger number of devices (many more than 32). Larger systems can easily be built using the teachings of this invention by using one or more memory subsystems, designated primary

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bus units, each of which consists of two or more devices, typically 32 or close to the maximum allowed by bus design requirements, connected to a transceiver device.

Referring to Figure 9, each primary bus unit can be mounted on a single circuit board 66, sometimes called a memory stick. Each transceiver device 19 in turn connects to a transceiver bus 65, similar or identical in electrical and other respects to the primary bus 18 described at length above. In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on primary bus units. In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primay bus unit. Other devices, generically referred to as peripheral devices, including disk controllers, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

[0094] The transceivers are quite simple in function. They detect request packets on the transceiver bus and transmit them to their primary bus unit. If the request packet calls for a write to a device on a transceiver's primary bus unit, that transceiver keeps track of the access time and block size and forwards all data from the transceiver bus to the primary bus unit during that time. The transceivers also watch their primary bus unit, forwarding any data that occurs there to the transceiver bus. The high speed of the buses means that the transceivers will need to be pipelined, and will require an additional one or two cycle delay for data to pass through the transceiver in either direction. Access times stored in masters on the transceiver bus must be increased to account for transceiver delay but access times stored in slaves on a primary bus unit should not be modified.

[0095] Persons skilled in the art will recognize that a more sophisticated transceiver can control transmissions to and from primary bus units. An additional control line, TrncvrRW can be bused to all devices on the transceiver bus, using that line in conjunction with the AddrValid line to indicate to all devices on the transceiver bus that the information on the data lines is: 1) a request packet, 2) valid data to a slave, 3) valid data from a slave, or 4) invalid data (or idle bus). Using this extra control line obviates the need for the transceivers to keep track of when data needs to be forwarded from its primary bus to the transceiver bus - all transceivers send all data from their primary bus to the transceiver bus whenever the control signal indicates condition 2) above. In a preferred implementation of this invention, if AddrValid and TrncvrRW are both low, there is no bus activity and the transceivers should remain in an idle state. A controller sending a request packet will drive AddrValid high, indicating to all devices on the transceiver bus that a request packet is being sent which each transceiver should forward to its primary bus unit. Each controller seeking to write to a slave should drive both AddrValid and TrncvrRW high, indicating valid data for a slave is present on the data lines. Each transceiver device will then transmit all data from the transceiver bus lines to each primary bus unit. Any controller expecting to receive information from a slave should also drive the TrncvrRW line high, but not drive AddrValid, thereby indicating to each transceiver to transmit any data coming from any slave on its primary local bus to the transceiver bus. A still more sophisticated transceiver would recognize signals addressed to or coming from its primary bus unit and transmit signals only at requested times.

[0096] An example of the physical mounting of the transceivers is shown in Figure 9. One important feature of this physical arrangement is to integrate the bus of each transceiver 19 with the original bus of DRAMs or other devices 15, 16, 17 on the primary bus unit 66. The transceivers 19 have pins on two sides, and are preferably mounted flat on the primary bus unit with a first set of pins connected to primary bus 18. A second set of transceiver pins 20, preferably orthogonal to the first set of pins, are oriented to allow the transceiver 19 to be attached to the transceiver bus 65 in much the same way as the DRAMs were attached to the primary bus unit. The transceiver bus can be generally planar and in a different plane, preferably orthogonal to the plane of each primary bus unit. The transceiver bus can also be generally circular with primary bus units mounted perpendicular and tangential to the transceiver bus.

[0097] Using this two level scheme allows one to easily build a system that contains over 500 slaves (16 buses of 32 DRAMs each). Persons skilled in the art can modify the device ID scheme described above to accommodate more than 256 devices, for example by using a longer device ID or by using additional registers to hold some of the device ID. This scheme can be extended in yet a third dimension to make a second-order transceiver bus, connecting multiple transceiver buses by aligning transceiver bus units parallel to and on top of each other and busing corresponding signal lines through a suitable transceiver. Using such a second-order transceiver bus, one could connect many thousands of slave devices into what is effectively a single bus.

Device Interface

[0098] The device interface to the high-speed bus can be divided into three main parts. The first part is the electrical interface. This part includes the input receivers, bus drivers and clock generation circuitry. The second part contains the address comparison circuitry and timing registers. This part takes the input request packet and determines if the request

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is for this device, and if it is, starts the internal access and delivers the data to the pins at the correct time. The final part, specifically for memory devices such as DRAMs, is the DRAM column access path. This part needs to provide bandwidth into and out of the DRAM sense amps greater than the bandwidth provided by conventional DRAMs. The implementation of the electrical interface and DRAM column access path are described in more detail in the following sections. Persons skilled in the art recognize how to modify prior-art address comparison circuitry and prior-art register circuitry in order to practice the present invention.

Electrical Interface - Input/Output Circuitry

[0099] A block diagram of the preferred input/output circuit for address/data/control lines is shown in Figure 10. This circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus. To further reduce the performance requirements for device input receivers, each device pin, and thus each bus line, is connected to two clocked receivers, one to sample the even cycle inputs, the other to sample the odd cycle inputs. By thus de-multiplexing the input 70 at the pin, each clocked amplifier is given a full 2 ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal. Persons skilled in the art will recognize that additional clocked input receivers can be used within the teachings of this invention. For example, four input receivers could be connected to each device pin and clocked by a modified internal device clock to transfer sequential bits from the bus to internal device circuits, allowing still higher external bus speeds or still longer settling times to amplify the bus low-voltage-swing signal into a full value CMOS logic signal.

[0100] The output drivers are quite simple, and consist of a single NMOS pulldown transistor 76. This transistor is sized so that under worst case conditions it can still sink the 50 mA required by the bus. For 0.8 micron CMOS technology, the transistor will need to be about 200 microns long. Overall bus performance can be improved by using feedback techniques to control output transistor current so that the current through the device is roughly 50 mA under all operating conditions, although this is not absolutely necessary for proper bus operation. An example of one of many methods known to persons skilled in the art for using feedback techniques to control current is described in Hans Schumacher, et al., "CMOS Subnanosecond True-ECL Output Buffer," J. Solid State Circuits, Vol. 25 (1), pp. 150-154 (Feb. 1990). Controlling this current improves performance and reduces power dissipation. This output driver which can be operated at 500 MHz, can in turn be controlled by a suitable multiplexer with two or more (preferably four) inputs connected to other internal chip circuitry, all of which can be designed according to well known prior art.

[0101] The input receivers of every slave must be able to operate during every cycle to determine whether the signal on the bus is a valid request packet. This requirement leads to a number of constraints on the input circuitry. In addition to requiring small acquisition and resolution delays, the circuits must take little or no DC power, little AC power and inject very little current back into the input or reference lines. The standard clocked DRAM sense amp shown in Figure 11 satisfies all these requirements except the need for low input currents. When this sense amp goes from sense to sample, the capacitance of the internal nodes 83 and 84 in Figure11 is discharged through the reference line 68 and input 69, respectively. This particular current is small, but the sum of such currents from all the inputs into the reference lines summed over all devices can be reasonably large.

[0102] The fact that the sign of the current depends upon on the previous received data makes matters worse. One way to solve this problem is to divide the sample period into two phases. During the first phase, the inputs are shorted to a buffered version of the reference level (which may have an offset). During the second phase, the inputs are connected to the true inputs. This scheme does not remove the input current completely, since the input must still charge nodes 83 and 84 from the reference value to the current input value, but it does reduce the total charge required by about a factor of 10 (requiring only a 0.25V change rather than a 2.5V change). Persons skilled in the art will recognize that many other methods can be used to provide a clocked amplifier that will operate on very low input currents.

[0103] One important part of the input/output circuitry generates an internal device clock based on early and late bus clocks. Controlling clock skew (the difference in clock timing between devices) is important in a system running with 2 ns cycles, thus the internal device clock is generated so the input sampler and the output driver operate as close in time as possible to midway between the two bus clocks.

[0104] A block diagram of the internal device clock generating circuit is shown in Figure 12 and the corresponding timing diagram in Figure 13. The basic idea behind this circuit is relatively simple. A DC amplifier 102 is used to convert the small-swing bus clock into a full-swing CMOS signal. This signal is then fed into a variable delay line 103. The output of delay line 103 feeds three additional delay lines: 104 having a fixed delay; 105 having the same fixed delay plus a second variable delay; and 106 having the same fixed delay plus one half of the second variable delay. The outputs 107, 108 of the delay lines 104 and 105 drive clocked input receivers 101 and 111 connected to early and late bus clock inputs 100 and 110, respectively. These input receivers 101 and 111 have the same design as the receivers described

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above and shown in Fig. 11. Variable delay lines 103 and 105 are adjusted via feedback lines 116, 115 so that input receivers 101 and 111 sample the bus clocks just as they transition. Delay lines 103 and 105 are adjusted so that the falling edge 120 of output 107 precedes the falling edge 121 of the early bus clock, Clock1 53, by an amount of time 128 equal to the delay in input sampler 101. Delay line 108 is adjusted in the same way so that falling edge 122 precedes the falling edge 123 of late bus clock, Clock2 54, by the delay 128 in input sampler 111.

[0105] Since the outputs 107 and 108 are synchronized with the two bus clocks and the output 73 of the last delay line 106 is midway between outputs 107 and 108, that is, output 73 follows output 107 by the same amount of time 129 that output 73 precedes output 108, output 73 provides an internal device clock midway between the bus clocks. The falling edge 124 of internal device clock 73 precedes the time of actual input sampling 125 by one sampler delay. Note that this circuit organization automatically balances the delay in substantially all device input receivers 71 and 72 (Fig. 10), since outputs 107 and 108 are adjusted so the bus clocks are sampled by input receivers 101 and 111 just as the bus clocks transition.

[0106] In the preferred embodiment, two sets of these delay lines are used, one to generate the true value of the internal device clock 73, and the other to generate the complement 74 without adding any inverter delay. The dual circuit allows generation of truly complementary clocks, with extremely small skew. The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125. The true and complement internal device clocks are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits, which means that the new data always will be driven on the bus slightly after the old data has been sampled.

DRAM Column Access Modification

[0107] A block diagram of a conventional 4 MBit DRAM 130 is shown in Figure 15. The DRAM memory array is divided into a number of subarrays 150-157, for example, 8. Each subarray is divided into arrays 148, 149 of memory cells. Row address selection is performed by decoders 146. A column decoder 147A, 147B, including column sense amps on either side of the decoder, runs through the core of each subarray. These column sense amps can be set to precharge or latch the most-recently stored value, as described in detail above. Internal I/O lines connect each set of sense-amps, as gated by corresponding column decoders, to input and output circuitry connected ultimately to the device pins. These internal I/O lines are used to drive the data from the selected bit lines to the data pins (some of pins 131-145), or to take the data from the pins and write the selected bit lines. Such a column access path organized by prior art constraints does not have sufficient bandwidth to interface with a high speed bus. The method of this invention does not require changing the overall method used for column access, but does change implementation details. Many of these details have been implemented selectively in certain fast memory devices, but never in conjunction with the bus architecture of this invention.

[0108] Running the internal I/O lines in the conventional way at high bus cycle rates is not possible. In the preferred method, several (preferably 4) bytes are read or written during each cycle and the column access path is modified to run at a lower rate (the inverse of the number of bytes accessed per cycle, preferably 1/4 of the bus cycle rate). Three different techniques are used to provide the additional internal I/O lines required and to supply data to memory cells at this rate. First, the number of I/O bit lines in each subarray running through the column decoder 147 is increased, for example, to 16, eight for each of the two columns of column sense amps and the column decoder selects one set of columns from the "top" half 148 of subarray 150 and one set of columns from the "bottom" half 149 during each cycle, where the column decoder selects one column sense amp per I/O bit line. Second, each column I/O line is divided into two halves, carrying data independently over separate internal I/O lines from the left half 147A and right half 147B of each subarray (dividing each subarray into quadrants) and the column decoder selects sense amps from each right and left half of the subarray, doubling the number of bits available at each cycle. Thus each column decode selection turns on *n* column sense amps, where n equals four (top left and right, bottom left and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each x 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

[0109] The multiple, gated input receivers described above allow high speed input from the device pins onto the internal I/O lines and ultimately into memory. The multiplexed output driver described above is used to keep up with the data flow available using these techniques. Control means are provided to select whether information at the device pins should be treated as an address, and therefore to be decoded, or input or output data to be driven onto or read from the internal I/O lines.

[0110] Each subarray can access 32 bits per cycle, 16 bits from the left subarray and 16 from the right subarray. With

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8 I/O lines per sense-amplifier column and accessing two subarrays at a time, the DRAM can provide 64 bits per cycle. This extra I/O bandwidth is not needed for reads (and is probably not used), but may be needed for writes. Availability of write bandwidth is a more difficult problem than read bandwidth because over-writing a value in a sense-amplifier may be a slow operation, depending on how the sense amplifier is connected to the bit line. The extra set of internal I/O lines provides some bandwidth margin for write operations.

[0111] Persons skilled in the art will recognize that many variations of the teachings of this invention can be practiced that still fall within the claims of this invention which follow.

[0112] It follows a list of further embodiments of the invention:

Embodiment 1. A memory subsystem comprising
two memory devices connected in parallel to a bus,
said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices,
said control information including device-select information,
said bus containing substantially fewer bus lines than the number of bits in a single address, and
said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices.

Embodiment 2. The memory subsystem with the features of embodiment 1 wherein said bus contains at least 8 bus lines adapted to carry at least 16 address bits and at least 8 data bits.

Embodiment 3. The memory subsystem with the features of embodiment 1 wherein said bus also includes parallel lines for clock and power.

Embodiment 4. A system comprising
a memory subsystem with the features of embodiment 1 wherein each bus of said memory subsystem is connected to its own transceiver device,
a transceiver bus connecting said transceiver devices, and
a means for transferring information between each of said buses of said memory subsystems and said transceiver bus, whereby memory subsystems may be integrated into a larger system having more memory than an individual memory subsystem.

Embodiment 5. The system with the features of embodiment 4 having a plurality of memory subsystems.

Embodiment 6. The system with the features of embodiment 4 further comprising a master device connected to said transceiver bus.

Embodiment 7. The system with the features of embodiment 6 wherein said master device is selected from the group consisting of a central processing unit, a floating point unit and a direct memory access unit.

Embodiment 8. The system with the features of embodiment 4 further comprising a peripheral device connected to the transceiver bus, said peripheral device adapted for connection to other devices not on the bus.

Embodiment 9. The system with the features of embodiment 8 wherein said peripheral device is selected from the group consisting of an I/O interface port, a video controller and a disk controller.

Embodiment 10. The system with the features of embodiment 5 wherein said transceiver bus is in a different plane than the plane of the bus of each of said memory subsystems.

Embodiment 11. The system with the features of embodiment 5 wherein the bus of each memory subsystem lies substantially in a subsystem bus plane and said transceiver bus lies substantially in a plane orthogonal to said subsystem bus plane.

Embodiment 12. The system with the features of embodiment 4 having at least two transceiver buses, each transceiver bus having a plurality of memory subsystem buses connected through a first transceiver to said transceiver bus,
each of said transceiver buses being further connected to a second transceiver adapted to interface to a second-order transceiver bus, whereby each transceiver bus is connected through said second transceiver to form a second-order transceiver bus unit.

Embodiment 13. A semiconductor subsystem bus for interconnecting semiconductor devices comprising
a plurality of semiconductor devices connected in parallel to a bus, at least one of said semiconductor devices being a memory device or a transceiver device which in turn is connected to a memory subsystem,
said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor devices,
said control information including semiconductor device-select information,
said bus containing substantially fewer bus lines than the number of bits in a single address, and
said bus carrying device-select information without the need for separate device-select lines connected directly to individual semiconductor devices, and
at least one modifiable register in each of the semiconductor devices on said bus, said modifiable registers being accessible from said bus, whereby the subsystem can be configured using signals transmitted on said bus.

Embodiment 14. The semiconductor subsystem bus with the features of embodiment 13 wherein one type of modifiable

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register is an access-time register designed to store a time delay after which a device may take some specified action on said bus.

Embodiment 15. The semiconductor subsystem bus with the features of embodiment 13 further comprising a semiconductor device having at least two access-time registers and

one of said access-time registers is permanently programmed to contain a fixed value and at least one of said access-time registers can be modified by information carried on said bus.

Embodiment 16. The semiconductor subsystem bus with the features of embodiment 13 further comprising a memory device having at least one discrete memory section and also having a modifiable address register adapted to store memory address information which corresponds to each said discrete memory section.

Embodiment 17. The semiconductor subsystem bus with the features of embodiment 16 wherein said memory address information comprises a pointer to said discrete memory section.

Embodiment 18. The semiconductor subsystem bus with the features of embodiment 16 wherein said discrete memory section has a top and a bottom and said memory address information comprises pointers to said top and said bottom.

Embodiment 19. The semiconductor subsystem bus with the features of embodiment 16 wherein said memory address information comprises

a pointer to said discrete memory section and

a range value indicating the size of said discrete memory section.

Embodiment 20. The semiconductor subsystem bus with the features of embodiment 16 wherein said address registers of each of said discrete memory sections of each of said memory devices connected to said bus are set to contain memory address information that is different for each discrete memory section and such that the highest memory address in each discrete memory section is one less than the lowest memory address in another discrete memory section, whereby memory may be organized into one or a small number of contiguous memory blocks.

Embodiment 21. The semiconductor subsystem bus with the features of embodiment 16 further comprising a means for testing each of said discrete memory sections of each of said memory devices for proper function, and

for each non-functional discrete memory section, a means for setting at least one address register which corresponds to said discrete memory section to indicate that said discrete memory section is non-functional,

for each functional discrete memory section, a means for setting at least one address register which corresponds to said discrete memory section to contain such corresponding address information.

Embodiment 22. The semiconductor subsystem bus with the features of embodiment 21 wherein said address registers corresponding to said discrete memory sections are set to provide one contiguous memory block within the subsystem.

Embodiment 23. The semiconductor subsystem bus with the features of embodiment 13 wherein one of said modifiable registers is a device identification register which can be modified to contain a value unique to that semiconductor device.

Embodiment 24. The semiconductor subsystem bus with the features of embodiment 23 wherein said device identification register is set to contain a unique value which is a function of the physical position of that semiconductor device either along said bus or in relationship to other semiconductor devices or said bus.

Embodiment 25. A bus subsystem comprising

two semiconductor devices connected in parallel to a bus, wherein one of said semiconductor devices is a master device, said master device including a means for initiating bus transactions,

said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said devices,

said control information including device-select information,

said bus containing substantially fewer lines than the number of bits in a single address, and

said bus carrying device-select information without the need for separate device-select lines connected directly to individual devices on said bus, whereby said master device initiates bus transactions which transfer information between said semiconductor devices on said bus.

Embodiment 26. The bus subsystem with the features of embodiment 25 wherein one of said semiconductor devices is a memory device connected to said bus, said memory device having at least one discrete memory section and also having a modifiable address register adapted to store memory address information which corresponds to each said discrete memory section.

Embodiment 27. The bus subsystem with the features of embodiment 26 wherein one of said semiconductor devices comprises a transceiver device connected in parallel to said bus and connected in parallel to a memory device on a bus other than said bus.

28. The bus subsystem with the features of embodiment 26 further including a means Embodiment for said master device to request said memory device to prepare for a bus transaction by sending a request packet along said bus, said memory device and said master device each having a device-internal means to prepare to begin said bus transaction during a device-internal phase and further having a bus access means to effect said bus transaction during a bus access phase, said request packet including

a sequence of bytes containing address and control information,

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said control information including information about the requested bus transaction and about the access time, which corresponds to a number of bus cycles, which needs to intervene before beginning said bus-access phase, and said address information pointing to at least one memory location within one of said discrete memory sections of said memory device.

Embodiment 29. The bus subsystem with the features of embodiment 28 wherein said memory device includes a means to read said control information and initiate said device-internal means at a time so as to complete said device-internal phase within said access time and begin said bus access phase after said number of bus cycles.

Embodiment 30. The bus subsystem with the features of embodiment 28 wherein said control information comprises an op code.

Embodiment 31. The bus subsystem with the features of embodiment 30 wherein said memory device includes sense amplifiers adapted to hold a bit of information or to precharge after a selected time and a means to transfer a data block during a data block transfer either reading data from said memory device or writing data into said memory device, and wherein said op code instructs said memory device to activate a response means, said response means including a means to

initiate a data block transfer,
select the size of said data block,
select the time to initiate said data block transfer,
access a control register, including reading from or writing to said control register,
precharge said sense amplifiers after each of said data block transfers is complete,
hold a bit of information in each of said sense amplifiers after each of said data block transfers is complete, or
select normal or page-mode access.

Embodiment 32. The bus subsystem with the features of embodiment 31 wherein said data block transfer comprises a read from or a write to memory within a single memory device.

Embodiment 33. The bus subsystem with the features of embodiment 28 further comprising a means for said master device to send control information to a specific one of said semiconductor devices on said bus by including in said request packet a device identification number unique to said semiconductor device.

Embodiment 34. The bus subsystem with the features of embodiment 28 further comprising a means for said master device to send control information to a selected one of said discrete memory portions by including in said request packet a specific memory address.

Embodiment 35. The bus subsystem with the features of embodiment 28 further comprising a means for said master device to send control information to substantially all semiconductor devices on said bus by including in said request packet a special device identification number which is recognized by said semiconductor devices.

Embodiment 15 36. The bus subsystem with the features of embodiment 28 wherein said control information specifies directly or indirectly the number of bus cycles for said master device and said memory device to wait before beginning said bus access phase.

Embodiment 37. The bus subsystem with the features of embodiment 36 wherein, for a data block transfer, said master device and said memory device use the same access time and same data block size regardless of whether said data block transfer is a read or write operation.

Embodiment 38. The bus subsystem with the features of embodiment 28 wherein said control information further includes a block-size value that encodes and specifies the size of the block of data to be transferred.

Embodiment 39. The bus subsystem with the features of embodiment 38 wherein said block-size value is encoded as a linear value for relatively small block sizes values and is encoded as a logarithmic value for relatively larger block sizes.

Embodiment 40. The bus subsystem with the features of embodiment 38 wherein said block-size value is encoded using four bits, and where the encoded value is

Encoded Value	Block Size (Bytes)
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	16

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(continued)

Encoded Value	Block Size (Bytes)
10	32
11	64
12	128
13	256
14	512
15	1024

Embodiment 41. The bus subsystem with the features of embodiment 26 wherein said memory device is a DRAM device containing
a plurality of sense amplifiers,
a means to hold said sense amplifiers in an unmodified state after a read or write operation, leaving the device in page mode,
a means to precharge said sense amplifiers and
a means for selecting whether to precharge said sense amplifiers or to hold said sense amplifiers in an unmodified state.
Embodiment 42. The bus subsystem with the features of embodiment 28 wherein said request packet comprises an even number of bytes.
Embodiment 43. The bus subsystem with the features of embodiment 28 further including a means for generating and controlling a plurality of bus cycles, during which said bus carries said address, data and control information, and wherein alternate said bus cycles are designated odd cycles and even cycles, respectively, and wherein said request packet begins only on an even cycle.
Embodiment 44. The bus subsystem with the features of embodiment 28 further including a means for generating ECC information corresponding to a block of data and a means for using said ECC information to correct errors in storing or reading said block of data, wherein said ECC information may be stored separately from said block of data.
Embodiment 45. The bus subsystem with the features of embodiment 44 further comprising at least two of said memory devices wherein said ECC information and said corresponding block of data are stored in a first and a second said memory device, respectively, and said master device includes a means to write or read said block of data with error correction by sending separate ones of said request packets for said ECC information and for said corresponding block of data.
Embodiment 46. A bus subsystem comprising
a memory device and a master device connected in parallel on a bus,
a means for said master device to send a request packet and initiate a bus transaction and
a means for said master device to keep track of current and pending bus transactions,
said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices,
said bus containing substantially fewer lines than the number of bits in a single address, and
said bus carrying device-select information without the need for separate device-select lines connected directly to individual devices on said bus, whereby said master device initiates bus transactions which transfer information between devices on said bus and collisions on said bus are avoided because said master device avoids initiating bus transactions which would conflict with current or pending bus transactions.
Embodiment 47. The bus subsystem with the features of embodiment 46 having at least two of said master devices and including
a collision detecting means whereby a first said master device sending a first said request packet can detect a second said master device sending one of said colliding request packets, where one of said said colliding request packet may be sent simultaneous with the initial sending of or overlapping the sending of said first request packet, and
an arbitration means whereby said first and said second master devices select a priority order in which each of said master devices will be allowed to access said bus sequentially .
Embodiment 48. The bus subsystem with the features of embodiment 47 wherein each of said master devices has a master ID number and each of said request packets includes a master ID position which is a predetermined number of bits in a predetermined position in said request packet, and wherein said collision detection means comprises
a means included in each master device for sending a request packet including said master ID number of said master device in said master ID position of said request packet and
a means to detect a collision and invoke said arbitration means if any master device detects any other master ID number in said master ID position.
Embodiment 49. The bus subsystem with the features of embodiment 47 wherein each of said master devices includes

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a means for sending a request packet,
a means for driving a selected bus line or lines during at least one selected bus cycle while said request packet is being sent,
a means for monitoring said selected bus line or lines to see if a said master device is sending a colliding request packet and
a means for informing all other master devices that a collision has occurred and for invoking said arbitration means.

Embodiment 50. The bus subsystem with the features of embodiment 47 wherein each of said master devices includes
a means, when sending a request packet, to drive a selected bus line or lines with a certain current during at least one selected bus cycle,
a means for monitoring said selected bus line or lines for a greater than normal current to see if another master device is driving that line or lines,
a means for detecting said greater than normal current, and
a means for informing all said master devices that a collision has occurred and for invoking said arbitration means.

Embodiment 51. The bus subsystem with the features of embodiment 47 wherein said arbitration means comprises
a means for initiating an arbitration cycle,
a means for allocating a single bus line to each master device during at least one selected bus cycle relative to the start of said arbitration cycle,
a means for allocating each master device to a single bus line during one of said selected bus cycles if there are more master devices than available bus lines,
a means for each of said master devices which sent a colliding request packet to drive said bus line allocated to said master device during said selected bus cycle, and
a means in at least one of said master devices for storing information about which master devices sent a colliding request packet,
whereby said master devices can monitor selected bus lines during said arbitration cycle and identify each said master device which sent a colliding request packet.

Embodiment 52. The bus subsystem with the features of embodiment 47 wherein said arbitration means comprises
a means included in a first one of said master devices which sent colliding request packets for identifying each of said master devices which sent colliding request packets,
a means for assigning a priority to each said master device which sent a colliding request packet, and
a means for allowing each said master device which sent a colliding request packet to access the bus sequentially according to that priority.

Embodiment 53. The bus subsystem with the features of embodiment 52 wherein said priority is based on the physical location of each of said master devices.

Embodiment 54. The bus subsystem with the features of embodiment 52 wherein said priority is based on said master ID number of said master devices.

Embodiment 55. The bus subsystem with the features of embodiment 52 wherein each of said master devices includes
a means, when sending a colliding request packet, for deciding which master device can send the next request packet in what order or at what time, whereby no master device may send a new request packet until responses to each pending request packet have been completed or scheduled.

Embodiment 56. A bus subsystem comprising
a plurality of semiconductor devices connected in parallel to a bus,
said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor devices,
said control information including device-select information,
said bus containing substantially fewer lines than the number of bits in a single address,
said bus carrying said device-select information without the need for separate device-select lines connected directly to individual semiconductor devices,
said semiconductor devices including a reset means having an input and an output, the output of the reset means of one semiconductor device being connected to the input of the reset means of the next semiconductor device in series.

Embodiment 57. The bus subsystem with the features of embodiment 56 further including system reset means comprising
a means for generating a first and a second reset signal,
a means for passing said first reset signal to a first of said semiconductor devices and then to subsequent ones of said semiconductor devices in series and
a means for passing a second reset signal to said first semiconductor device and then to said subsequent semiconductor devices in series,
said bus subsystem including one of said semiconductor devices containing
a device identification register adapted to contain a number unique to said semiconductor device within said bus subsystem,
a device identification register setting means, and
a device reset means for resetting said semiconductor device to some desired, known reset state in response to said

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first reset signal and for setting said device identification register in response to said second reset signal,
whereby said bus subsystem can be reset to a known reset state with a unique device identification value in said device identification register of each of said semiconductor devices.
Embodiment 58. The bus subsystem with the features of embodiment 57 wherein said desired, known reset state is where all registers in the semiconductor device are cleared and the state machines are reset.
Embodiment 59. The bus subsystem with the features of embodiment 57 wherein said device identification register setting means comprises
a means for detecting said second reset signal,
a means for reading a device identification number from said bus lines at a specific time relative to said second reset signal and
a means for storing said device identification number in said device identification register of said semiconductor device.
Embodiment 60. The bus subsystem with the features of embodiment 57 wherein said second reset signal comprises multiple pulse sequences and wherein said device identification setting means includes
a means for interpreting said pulse sequences as a device identification number and
a means for storing said device identification number in said device identification register of said semiconductor device.
Embodiment 61. The bus subsystem with the features of embodiment 57 wherein said device reset means comprises an n-stage shift register capable of storing n-bit values, wherein said device reset means interprets a specific value in said shift register as said first reset signal and interprets a specific value in said shift register as said second reset signal.
Embodiment 62. The bus subsystem with the features of embodiment 57 wherein one of said semiconductor devices is a master device, said master device including a means for generating said first and said second reset signals.
Embodiment 63. The bus subsystem with the features of embodiment 57 wherein one of said semiconductor devices is a master device, said master device including
a master ID register,
a means for assigning a master ID number to said master device and
a means for storing said master ID number in said master ID register.
Embodiment 64. The bus subsystem with the features of embodiment 63 further comprising a second one of said master devices, and a means for a first one of said master devices to assign a master ID number to substantially all other said master devices, whereby said first master device assigns one of said master ID numbers to each of said master devices on said bus subsystem and each said master device stores said assigned master ID number in said master ID register.
Embodiment 65. The bus subsystem with the features of embodiment 57 wherein one of said semiconductor devices includes a device-type register adapted to contain an identifier characteristic of that type of semiconductor device, and one or more modifiable registers, at least one of which is an access-time register adapted for storing access times.
Embodiment 66. The bus subsystem with the features of embodiment 65 wherein one of said semiconductor devices is a master device having
a means for selecting a semiconductor device,
a means for reading said device-type register of said selected semiconductor device,
a means for determining the device type of said selected semiconductor device,
a means for determining access-time values appropriate for said selected semiconductor device and for storing said access-time values in said access-time registers of said selected semiconductor device, and
a means for selecting and storing other values appropriate for said selected semiconductor device in corresponding registers of said selected semiconductor device,
whereby said master device can select a semiconductor device, determine what type it is, and set said access-time and other registers to contain appropriate values.
Embodiment 67. The bus subsystem with the features of embodiment 66 further comprising a memory device having at least one discrete memory section and at least one modifiable address register adapted to store memory address information which corresponds to each of said discrete memory sections, and
said master device further comprising a means for selecting and testing each of said discrete memory sections and a means for storing address information in said address registers corresponding to each of said discrete memory sections,
whereby said master device can test all said discrete memory sections and assign unique address values thereto.
Embodiment 68. A bus subsystem comprising
two semiconductor devices connected in parallel to a bus, one of said semiconductor devices being a master device,
said bus including a plurality of bus data lines for carrying substantially all address, data and control information needed by said semiconductor devices,
said control information including device-select information,
said bus containing substantially fewer of said bus data lines than the number of bits in a single address, and
said bus carrying device-select information without the need for separate device-select lines connected directly to individual semiconductor devices,
wherein all of said bus data lines are terminated transmission lines and all of said address, data and control information

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is carried on said bus data lines as a sequential series of bits in the form of low-voltage-swing signals.

Embodiment 69. The bus subsystem with the features of embodiment 68 further comprising a semiconductor device including a current-mode driver connected to drive one of said bus data lines.

Embodiment 70. The bus subsystem with the features of embodiment 69 further comprising a semiconductor device having a means to measure the voltage of said low-voltage-swing signals on a selected one of said bus data lines, whereby said semiconductor device can determine whether zero, one, or more than one of said current-mode drivers are driving said selected bus data line.

Embodiment 71. The bus subsystem with the features of embodiment 70 further comprising a semiconductor device having

a plurality of input receivers connected to one of said bus data lines, and

a selection means for selecting said input receivers one by one to sense and store, one at a time, the bits of said sequential series of bits.

Embodiment 72. The bus subsystem with the features of embodiment 70 further comprising a semiconductor device having two input receivers connected to one of said bus data lines.

Embodiment 73. A bus subsystem comprising

two semiconductor devices connected in parallel to a bus having a first and a second end, said bus including a bus clock line, said bus clock line having first and second ends corresponding to said first and second ends of said bus, respectively,

a clock generator connected to said first end of said bus clock line to generate early bus clock signals with a normal rise time, and

signal return means at said second end of said bus clock line to return said early bus clock signals to said first end of said bus as corresponding late bus clock signals,

whereby each of said early bus clock signals will propagate from said clock generator along said clock line starting from said first end to said second end of said bus and then return at a later time to said first end of said bus as a corresponding late bus clock signal, whereby each semiconductor device on said bus can detect said early bus clock signals and said corresponding late bus clock signals.

Embodiment 74. The bus subsystem with the features of embodiment 73 further comprising a first and a second said bus clock line having first and second ends at said first and said second ends of said bus, respectively, wherein said signal return means directly connects said second ends of said first and said second bus clock lines whereby each of said early bus clock signals will propagate from said clock generator at said first end of said bus along said first bus clock line to said second end of said bus and then return on said second bus clock line to said first end of said bus as one of said corresponding late bus clock signals.

Embodiment 75. The bus subsystem with the features of embodiment 73 wherein said signal return means comprises said first bus clock line without a line terminator at said second end thereof whereby each of said early bus clock signals reaching said second end of said first bus clock line will be reflected back along said first bus clock line as said corresponding late bus clock signals.

Embodiment 76. The bus subsystem with the features of embodiment 73 further comprising

a means for operating said bus in bus cycles timed to have a certain bus cycle frequency and a corresponding bus cycle period and

a means for operating said clock generator with a period of twice the bus cycle period.

Embodiment 77. The bus subsystem with the features of embodiment 76 wherein said bus cycle frequency is greater than approximately 50 MHz and less than or equal to approximately 500 MHz.

Embodiment 78. The bus subsystem with the features of embodiment 73 further including a semiconductor device having an internal device clock generating means to derive the midpoint time between said early and corresponding late bus clock signals and to generate an internal device clock synchronized to said midpoint time.

Embodiment 79. The bus subsystem with the features of embodiment 73 further including a semiconductor device having a low-skew clock generator circuit comprising

a first delay line having an input, an output and a basic delay and means for synchronizing the output of said first delay line with said early bus clock signal,

a second delay line having said basic delay plus a variable delay, said second delay line having an output and a means for synchronizing the output of said second delay line with said late bus clock signal, and

a third delay line having a third delay and a means to set said third delay midway between the delays of said first and second delay lines, said third delay line having an output which provides an internal device clock signal synchronized to a time halfway between said early and said late bus clock signals.

Embodiment 80. The bus subsystem with the features of embodiment 73 wherein said early and said late bus clock signals are low-voltage-swing signals that transition cyclically between low and high logical values, and further including a semiconductor device having a low-skew clock generator circuit comprising

a DC amplifier to convert said early and said late bus clock signals into full-swing logic signals,

a first variable delay line having a first variable delay and an input and an output, the input of said first variable delay

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line being connected to said DC amplifier
a first, a second and a third additional delay line, each having an input and an output, the input of each of said additional delay lines being connected to the output of said first delay line,
said first additional delay line having a fixed delay,
said second additional delay line having said fixed delay plus a second variable delay, and
said third additional delay line having said fixed delay plus one half of said second variable delay,
a first clocked input receiver connected to sample said early bus clock signal and gated by said output of said first additional delay line,
a means for adjusting said first variable delay so said first clocked input receiver samples said early bus clock signal just as said early bus clock signal transitions,
a second clocked input receiver connected to sample said late bus clock signal and gated by said output of said second additional delay line,
a means for adjusting said second variable delay so said second clocked input receiver samples said late bus clock signal just as said late bus clock signal transitions,
whereby said output of said third additional delay line is synchronized to a time halfway between said outputs of said first and said second additional delay lines, and said output of said third additional delay line provides an internal device clock signal.

Embodiment 81. The bus subsystem with the features of embodiment 80 further comprising a semiconductor device having
a first one of said low-skew clock generator circuits which generates a "true" internal device clock signal and
a second one of said low-skew clock generator circuits connected to generate a "complement" internal device clock signal synchronized with but opposite in logical value to said "true" internal device clock signal.

Embodiment 82. A DRAM device designed to be connected to an external bus having a plurality of bus lines for carrying substantially all address, data and control information needed by said DRAM device as a sequential series of bits, said control information including device-select information, said external bus containing substantially fewer said bus lines than the number of bits in a single address, and said bus carrying device-select information without the need for separate device-select lines connected directly to said DRAM device, said DRAM device comprising
an array of memory cells connected in rows and columns, each of said memory cells adapted to store one of said bits,
a row address selection means for selecting one of said rows,
a column sense amp connected to each of said columns, each of said column sense amps adapted to latch one of said bits as a binary logical value or to precharge to a selected state,
a column decoding means connected to each of said column sense amps for selecting a plurality of said column sense amps for inputting one of said bits to or outputting one of said bits from said memory cells,
an internal I/O bus having a plurality of internal I/O lines wherein each of said internal I/O lines is connected to a plurality of said column sense amps, and
a plurality of bus connection means designed to connect said internal I/O lines to said external bus,
whereby a selected bit of said sequential series of bits can be transferred from said external bus to a selected one of said memory cells or said bit contained in a selected one of said memory cells can be transferred to said external bus.

Embodiment 83. The DRAM device with the features of embodiment 82 further comprising
an output driver connected to one said bus connection means,
an output multiplexer having an output connected to said output driver and a plurality of inputs, each of said inputs being connected to one of said internal I/O lines, and
a control means to select whether said output driver can drive said external bus,
whereby a plurality of memory cells are selected using said row address selection means and said column decoding means and a plurality of bits contained in said plurality of memory cells are output through said column sense amps to said internal I/O bus to said output multiplexer to said output driver to said external bus.

Embodiment 84. The DRAM device with the features of embodiment 82 further comprising
a plurality of input receivers connected to one of said bus data lines and to said internal I/O bus,
a selection means for selecting said input receivers one by one to sense and store, one at a time, the bits of said sequential series of bits, and
a control means to select whether an input receiver can drive said internal I/O bus, whereby a bit of said sequential series of bits is input from said external bus through one of said input receivers to one of said internal I/O lines to one of said column sense amps to one of said memory cells.

Embodiment 85. The DRAM device with the features of embodiment 82 further comprising
a first and a second half-array of said memory cells wherein each said row of said array of said memory cells is subdivided into two parts,
a first and a second one of said internal I/O buses connected to said column sense amps in said first and said second half-arrays, respectively, and

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a column decoder means to gate selected ones of said column sense amps connected to said memory cells in a selected row of said first and said second half-arrays simultaneously.

Embodiment 86. The DRAM device with the features of embodiment 85 wherein said column decoder means selects sixteen column sense amps at a time.

Embodiment 87. The DRAM device with the features of embodiment 82 wherein said external bus operates at a certain speed and wherein said DRAM device includes four of said internal I/O buses, each of which operates at one-fourth the speed of said external bus.

Embodiment 88. The DRAM device with the features of embodiment 82 further comprising

a means for precharging one of said column sense amps to a precharged state from which a binary logical value can quickly be loaded into said column sense amp,

if said column sense amp contains a binary logical value, a means for latching the logical value currently contained in said column sense amp and

a means for instructing said DRAM device to precharge said column sense amp or latch said binary logical value in said column sense amp.

Embodiment 89. The DRAM device with the features of embodiment 88 further comprising a means for instructing said DRAM device to precharge said column sense amp without further instruction whenever said row address selection means selects a different one of said rows.

Embodiment 90. The DRAM device with the features of embodiment 88 further comprising a means for instructing said DRAM device to precharge said column sense amp without further instruction at a first or a second preselected time after latching the latest said binary logical value, said first preselected time being long enough for said DRAM to latch said binary logical value into said column sense amp and transfer said binary logical value into memory or onto one of said internal I/O lines, and said second preselected time being a variable which can be stored in said DRAM device whereby said DRAM can latch a binary logical value into said column sense amp for transferring said binary logical value into or out of a selected said memory cell, then precharge to allow a faster subsequent read or write.

Embodiment 91. A package containing

a semiconductor die having a side, circuitry and a plurality of connecting areas positioned along or near said side, spaced at a selected pitch and connected to said circuitry,

said package comprising a plurality of bus connecting means for connecting to a plurality of external bus lines, each of said external bus lines corresponding to one of said connecting areas, each of said bus connecting means being positioned on a first side of said package,

connected to one said external bus line and to said corresponding connecting area on said semiconductor die, and spaced at a pitch substantially identical to said selected pitch of said connecting areas,

whereby each of said external bus lines can be connected to said corresponding connecting area on said semiconductor die by bus connection means positioned along a single side of said package.

Embodiment 92. The package with the features of embodiment 91 further comprising a plurality of said bus connecting means wherein each of said bus connecting means includes

a pin adapted for connection to one of said external bus lines and

a wire connecting said pin to one of said connecting areas on said semiconductor die,

said wire having an effective lead length less than about 4 millimeters and wherein the effective lead length of said wire of each of said bus connection means for said package is approximately equal.

Embodiment 93. A plurality of packages with the features of embodiment 91 wherein at least two of said semiconductor die are memory devices, each of said packages being generally flat, having a top and a bottom, and wherein

said packages are physically secured adjacent and parallel to each other in a stack,

where a first one of said packages is adjacent to a second one of said packages in said stack, said top of said first package is substantially aligned with said bottom of said second package, and

said bus connecting means of each of said packages are substantially aligned and are lying substantially in a plane.

Embodiment 94. The plurality of packages with the features of embodiment 93 further comprising a plurality of stacks wherein each of said bus connecting means can be electrically connected to corresponding said bus connecting means in each of said stacks.

Embodiment 95. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

at least one modifiable identification register accessible to said bus through said connection means, whereby data may

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be transmitted to said register via said bus and enable said device thereafter to be uniquely identified.

Embodiment 96. The semiconductor device with the features of embodiment 95 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 97. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and at least one modifiable register to hold device address information, said modifiable register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which enables said device thereafter to respond to a predetermined range of addresses.

Embodiment 98. The semiconductor device with the features of embodiment 97 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 99. The semiconductor device with the features of embodiment 98 wherein said memory device has at least one discrete memory section and also has at least one modifiable address register adapted to store memory address information which corresponds to each said discrete memory section.

Embodiment 100. The semiconductor device with the features of embodiment 99 wherein said memory address information comprises a pointer to said discrete memory section.

Embodiment 101. The semiconductor device with the features of embodiment 100 wherein said discrete memory section has a top and a bottom and said memory address information comprises pointers to said top and said bottom.

Embodiment 102. The semiconductor device with the features of embodiment 100 wherein said memory address information comprises

a pointer to said discrete memory section and

a range value indicating the size of said discrete memory section.

Embodiment 103. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

at least one modifiable access-time register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request.

Embodiment 104. The semiconductor device with the features of embodiment 103 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 105. The semiconductor device with the features of embodiment 103 further comprising at least two access-time registers and one of said access-time registers is permanently programmed to contain a fixed value and at least one of said access-time registers can be modified by information carried on said bus.

Embodiment 106. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, and wherein each said bus line is a terminated transmission line, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

a bus line driver capable of producing a low-voltage-swing signal on one of said terminated transmission lines.

Embodiment 107. The semiconductor device with the features of embodiment 106 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 108. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying

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substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said bus further including at least one bus clock line for carrying early and late bus clock signals, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

an internal device clock generating means which generates an internal device clock synchronized to a time halfway between said early and said late bus clock signals.

embodiment 109. The semiconductor device with the features of embodiment 108 wherein said bus further includes a first and a second one of said bus clock lines, said first bus clock line carries said early bus clock signal and said second bus clock line carries said late bus clock signal, said semiconductor device further comprising a means to detect said early bus clock signal on said first bus clock line and a means to detect said late bus clock signal on said second bus clock line.

Embodiment 110. The semiconductor device with the features of embodiment 109 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 111. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying as a sequential series of bits substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus,

a plurality of input receivers connected to one of said bus data lines and

a selection means for selecting said input receivers one by one to sense and store, one at a time, the bits of said sequential series of bits.

Embodiment 112. The semiconductor device with the features of embodiment 111 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 113. The semiconductor device with the features of embodiment 112 wherein two input receivers are connected to one of said bus lines.

Embodiment 114. A semiconductor device capable of use in an architecture for a semiconductor system bus including a plurality of semiconductor devices connected in parallel to a bus wherein said bus system includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said system bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said system bus,

an internal input/output bus within said semiconductor device having more lines than said system bus, and

a means for multiplexing the lines of said internal bus to the lines of said system bus, whereby said system bus can run at a higher speed than said internal bus.

Embodiment 115. The semiconductor device with the features of embodiment 114 wherein said semiconductor device is a memory device which connects substantially only to said system bus and sends and receives substantially all address, data and control information over said system bus.

Embodiment 116. A semiconductor device capable of use in an architecture for a semiconductor system bus including a plurality of semiconductor devices connected in parallel to a bus wherein said system bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said system bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said system bus,

an internal input/output bus within said semiconductor device having more lines than said system bus,

a means for multiplexing the lines of said internal bus to the lines of said system bus, whereby said system bus can run at a higher speed than said internal bus, and

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at least one modifiable identification register accessible to said system bus through said connection means, whereby data may be transmitted to said register via said system bus and which enables said device thereafter to be uniquely identified.

Embodiment 117. The semiconductor device with the features of embodiment 116 wherein said semiconductor device is a memory device which connects substantially only to said system bus and sends and receives substantially all address, data and control information over said system bus.

Embodiment 118. A semiconductor device capable of use in an architecture for a semiconductor system bus including a plurality of semiconductor devices connected in parallel to a bus wherein said system bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said system bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said system bus,

an internal input/output bus within said semiconductor device having more lines than said system bus,

a means for multiplexing the lines of said internal bus to the lines of said system bus, whereby said system bus can run at a higher speed than said internal bus, and

at least one modifiable register to hold device address information, said modifiable register accessible to said system bus through said connection means, whereby data may be transmitted to said register via said system bus which enables said device thereafter to respond to a predetermined range of addresses.

Embodiment 119. The semiconductor device with the features of embodiment 118 wherein said semiconductor device is a memory device which connects substantially only to said system bus and sends and receives substantially all address, data and control information over said system bus.

Embodiment 120. The semiconductor device with the features of embodiment 119 wherein said memory device has at least one discrete memory section and also has at least one modifiable address register adapted to store memory address information which corresponds to each said discrete memory section.

Embodiment 121. A semiconductor device capable of use in an architecture for a semiconductor system bus including a plurality of semiconductor devices connected in parallel to a bus wherein said system bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said system bus, and has substantially fewer bus lines than the number of bits in a single address, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said system bus,

an internal input/output bus within said semiconductor device having more lines than said system bus,

a means for multiplexing the lines of said internal bus to the lines of said system bus, whereby said system bus can run at a higher speed than said internal bus, and

at least one modifiable access-time register accessible to said system bus through said connection means, whereby data may be transmitted to said register via said system bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said system bus in response to a request.

Embodiment 122. The semiconductor device with the features of embodiment 121 wherein said semiconductor device is a memory device which connects substantially only to said system bus and sends and receives substantially all address, data and control information over said system bus.

Embodiment 123. The semiconductor device with the features of embodiment 121 further comprising at least two access-time registers and one of said access-time registers is permanently programmed to contain a fixed value and at least one of said access-time registers can be modified by information carried on said system bus.

Embodiment 124. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, wherein said address, data, control and device-select information is carried over said bus in the form of request packets and bus transactions, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus,

a means to receive said request packets over said bus,

a means to decode information in said request packets, and

a means to respond to said information in said request packets.

Embodiment 125. The semiconductor device with the features of embodiment 124 wherein said means to decode information in said request packet further comprises

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a means to identify and decode said control information in said request packet,
a means to identify and decode said device-select information in said request packet,
a means to identify and decode said address information in said request packet and
a means to determine whether said control information or said address information instructs said semiconductor device to begin a response.

Embodiment 126. The semiconductor device with the features of embodiment 124 wherein each of said bus transactions is carried out in response to said address and said control information in one of said request packets, and wherein said means to identify and decode information in said request packets includes a means to identify a sequence of bytes on said bus as one of said request packets containing said address and said control information, said control information including information about the type of said bus transaction being requested and the access time which needs to intervene before beginning said bus transaction over said bus and said address and said control information includes device-select information instructing one or more said semiconductor devices to respond to said address and said control information.

Embodiment 127. The semiconductor device with the features of embodiment 124 further comprising
a plurality of sense amplifiers adapted to precharge to a selected state or to latch a bit of information,
a means to hold said sense amplifiers in an unmodified state after latching one of said bits of information,
a means to precharge said sense amplifiers and
a means for selecting whether said semiconductor device should precharge said sense amplifiers or should hold said sense amplifiers in an unmodified state.

Embodiment with the features of embodiment 128. The semiconductor device 124 wherein said means to respond to said information, where said information is control information, further comprises a means to
transfer a data block during a data block transfer, further including a means to
read data from said semiconductor device and
write data into said semiconductor device, and
initiate a data block transfer,
transfer a data block of a selected size,
transfer a data block at a selected time,
access a control register, including a means to read from or write to said control register, or
select normal or page-mode access.

Embodiment 129. The semiconductor device with the features of embodiment 124 further comprising a means to respond to said information in said request packet if said information includes a device identification number unique to said semiconductor device.

Embodiment 130. The semiconductor device with the features of embodiment 124 further comprising a means to respond to said information in said request packet if said information includes a special device identification number which calls for said semiconductor device to respond.

Embodiment 131. The semiconductor device with the features of embodiment 124 further comprising a means to respond to said information in said request packet if said information includes an address unique to said semiconductor device.

Embodiment 132. The semiconductor device with the features of embodiment 124 further comprising a means to interpret said control information and decode the time to wait before beginning said bus transaction over said bus.

Embodiment 133. The semiconductor device with the features of embodiment 124 further comprising a means to interpret said control information and decode the size of a data block to transfer during one of said bus transactions.

Embodiment 134. The semiconductor device with the features of embodiment 124, 125, 126, 127, 128, 129, 130, 131, 132 or 133 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus.

Embodiment 135. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data, control and device-select information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, and carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to said individual semiconductor device, wherein said address, data, control and device-select information is carried over said bus in the form of request packets and bus transactions, said semiconductor device comprising
connection means adapted to connect said semiconductor device to said bus,
a means to encode address and control information in said request packets and
a means to send said request packets over said bus.

Embodiment 136. The semiconductor device 135 further comprising a means to request a bus transaction wherein each of said bus transactions is carried out in response to said address and said control information in one of said request packets, and wherein said means to encode information in said request packets includes a means to mark a sequence

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of bytes on said bus as one of said request packets, said control information including information about the type of said bus transaction being requested and the access time which needs to intervene before beginning said bus transaction over said bus and said address and said control information includes device-select information instructing one or more said semiconductor devices to respond to said address and said control information.

Embodiment 137. The semiconductor device with the features of embodiment 135 wherein one or more of said plurality of semiconductor devices has a unique device identification number, said semiconductor device further comprising a means to send control information to a specific one of said plurality of semiconductor devices by including in said request packet a selected said device identification number.

Embodiment 138. The semiconductor device with the features of embodiment 135 wherein each of said plurality of semiconductor devices is adapted to respond to a special device identification number, said semiconductor device further comprising a means to send control information to each of said plurality of semiconductor devices by including in said request packet said special device identification number.

Embodiment 139. The semiconductor device with the features of embodiment 135 wherein one or more of said plurality of semiconductor devices is a memory device having a plurality of addresses, said semiconductor device further comprising a means to send control information to a specific address or range of addresses in one of said plurality of semiconductor devices by including said specific address or range of addresses in said request packet.

Embodiment 140. The semiconductor device with the features of embodiment 135 wherein at least one of said request packets is a request packet requesting a bus transaction which is followed by a corresponding one of said bus transactions, said semiconductor device further comprising a means to encode said control information to specify directly or indirectly the time between the end of said request packet requesting a bus transaction and said corresponding bus transaction over said bus.

Embodiment 141. The semiconductor device with the features of embodiment 140 wherein one type of said bus transactions is a transfer of a data block, said semiconductor device further comprising a means to encode said control information to specify the size of said data block to transfer.

Embodiment 142. The semiconductor device with the features of embodiment 140 further comprising a means to keep track of current and pending bus transactions, whereby collisions on said bus are avoided because said semiconductor device avoids initiating bus transactions which would conflict with current or pending bus transactions.

Embodiment 143. The semiconductor device with the features of embodiment 135 wherein said semiconductor device is a first master device and one of said plurality of semiconductor devices is a second master device, further comprising a collision detecting means whereby said first master device when sending a first one of said request packets can detect said second master device sending a colliding one of said request packets, where said colliding request packet may be sent simultaneous with the initial sending of or overlapping the sending of said first request packet, and

an arbitration means whereby said first and said second master devices select a priority order in which each of said master devices will be allowed to access said bus sequentially.

Embodiment 144. The semiconductor device with the features of embodiment 143 wherein said semiconductor device is a master device and at least one of said plurality of semiconductor devices is a master device, each of said master devices has a master ID number and each of said request packets includes a master ID position which is a predetermined number of bits in a predetermined position in said request packet, and wherein said collision detection means comprises a means for said semiconductor device to send its master ID number in said request packet and

a means to detect a collision and invoke said arbitration means if said semiconductor device detects any other master ID number in said master ID position.

Embodiment 145. The semiconductor device with the features of embodiment 144 wherein said system bus architecture includes a means for carrying information on said bus during bus cycles, said semiconductor device further comprising a means for driving a selected bus line or lines during at least one selected bus cycle while sending each said request packet,

a means for monitoring said selected bus line or lines to see if another said master device is sending one of said colliding request packets and

a means for informing all said master devices that a collision has occurred and for invoking said arbitration means.

Embodiment 146. The semiconductor device with the features of embodiment 145 further comprising

a means, when sending a request packet, for driving a selected bus line or lines with a certain current during at least one selected bus cycle,

a means for monitoring said selected bus line or lines for a greater than normal current to see if another said master device is driving that line or lines,

a means for detecting said greater than normal current, and

a means for informing all said master devices that a collision has occurred and for invoking said arbitration means.

Embodiment 147. The semiconductor device with the features of embodiment 143 wherein said arbitration means comprises

a means for initiating an arbitration cycle,

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a means for allocating a single bus line to each said master device during at least one selected bus cycle relative to the start of said arbitration cycle,
a means for allocating each said master device to a single bus line during one of said selected bus cycles if there are more master devices than available bus lines,
a means for each of said master devices which sent one of said colliding request packets to drive said bus line allocated to said master device during said selected bus cycle, and
a means in at least one of said master devices for storing information about which master devices sent one of said colliding request packets,
whereby said master devices can monitor selected bus lines during said arbitration cycle and identify each said master device which sent one of said colliding request packets.
Embodiment 148. The semiconductor device with the features of embodiment 143 wherein said arbitration means comprises
a means for identifying each of said master devices which sent one of said colliding request packets,
a means for assigning a priority to each said master device which sent one of said colliding request packets, and
a means for allowing each said master device which sent one of said colliding request packets to access the bus sequentially according to that priority.
Embodiment 149. The semiconductor device with the features of embodiment 143 wherein said priority is based on the physical location of each of said master devices.
Embodiment 150. The semiconductor device with the features of embodiment 143 wherein said priority is based on said master ID number of said master devices.

Claims

1. A semiconductor device, the semiconductor device comprising:

connection means adapted to connect the semiconductor device to an external bus which is a part of a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data, control and device select information needed by the semiconductor device for communication with substantially every other semiconductor device connected to the external bus, and wherein the external bus has substantially fewer bus lines than the number of bits in a single address, wherein each bus line of the plurality of bus lines is a terminated transmission line, and wherein the external bus carries device-select information for the semiconductor device without the need for a separate device-select line connected directly to the semiconductor device,
a bus line driver capable of producing a low-voltage-swing signal on one of the terminated transmission lines,

wherein the semiconductor device is a semiconductor transceiver device to interface multiple units to the bus, wherein the multiple units are DRAMs.

2. The semiconductor device of claim 1,
wherein the bus line driver is capable of producing a low-voltage-swing signal having a voltage swing of not more than 1 Volt on one of said terminated transmission lines.

3. The semiconductor device of claim 1 or 2,
wherein the bus line driver is capable of producing a low-voltage-swing signal having a voltage swing of at least 500 mV on one of said terminated transmission lines.

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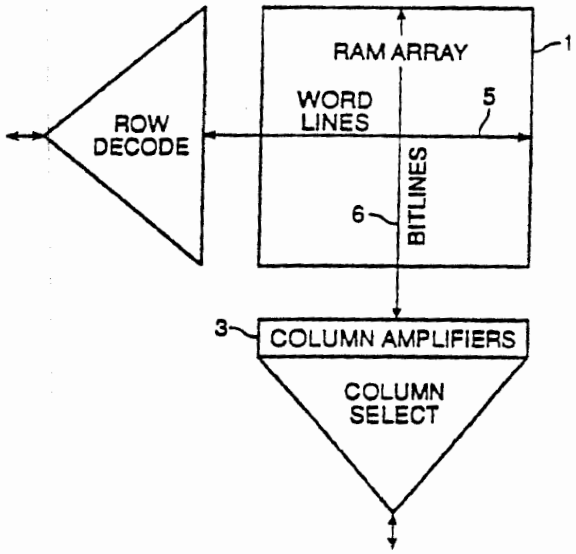

FIG. 1

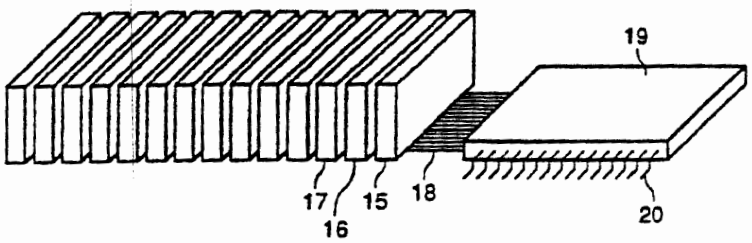

FIG. 3

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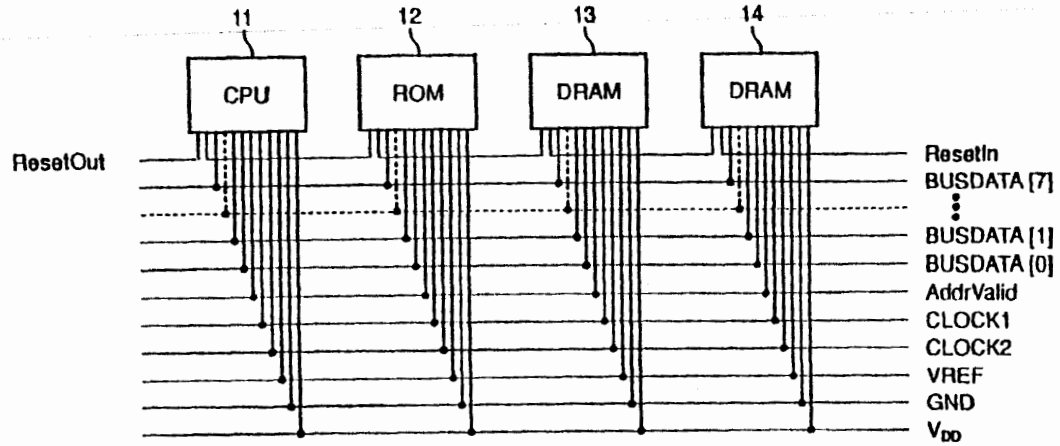

FIG. 2

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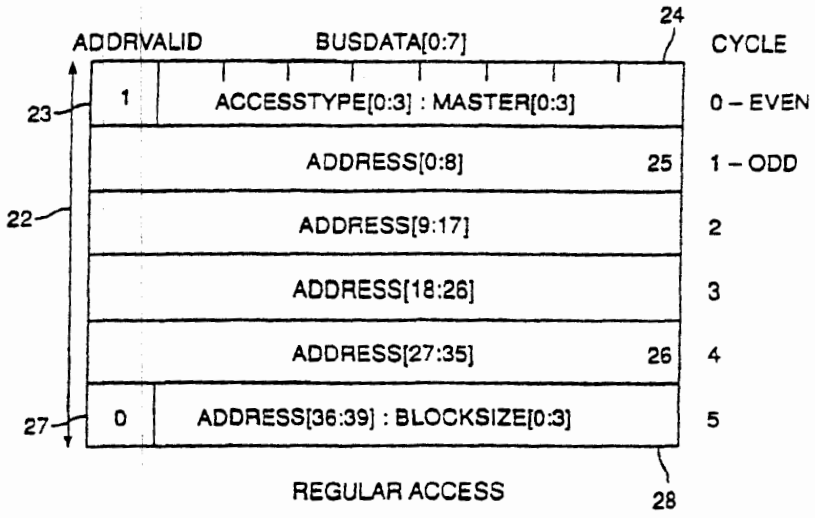

FIG. 4

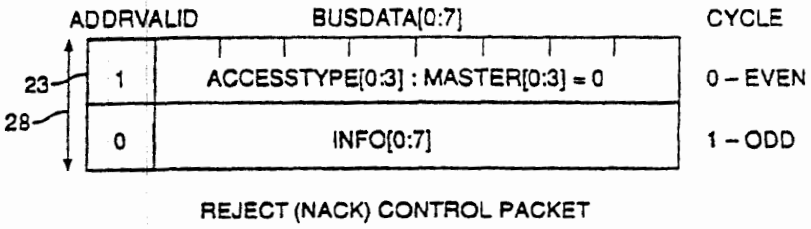

FIG. 5

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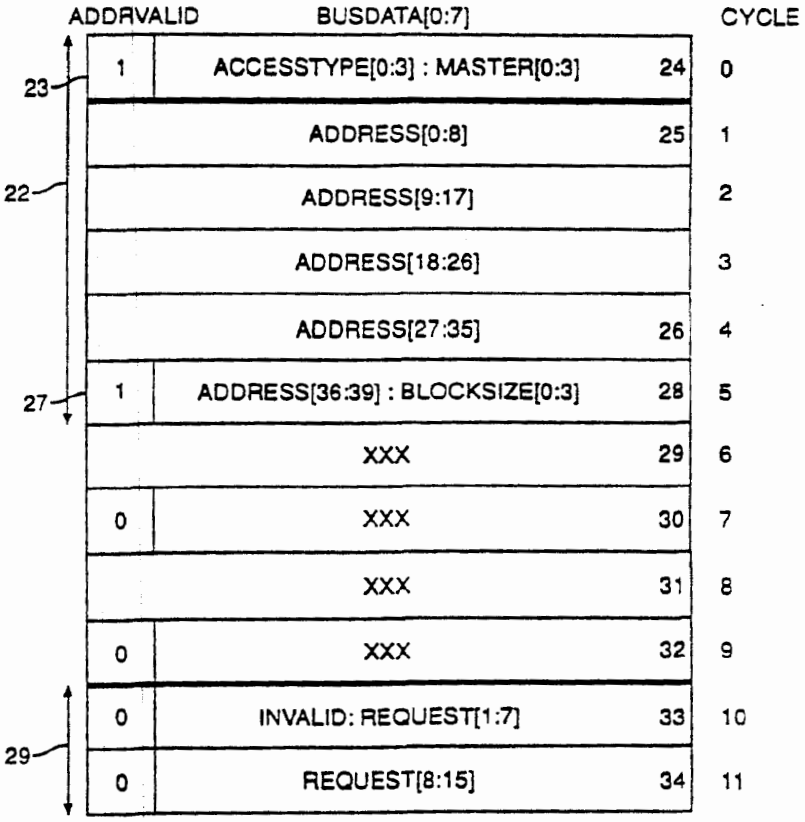

FIG. 6

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FIG. 7a

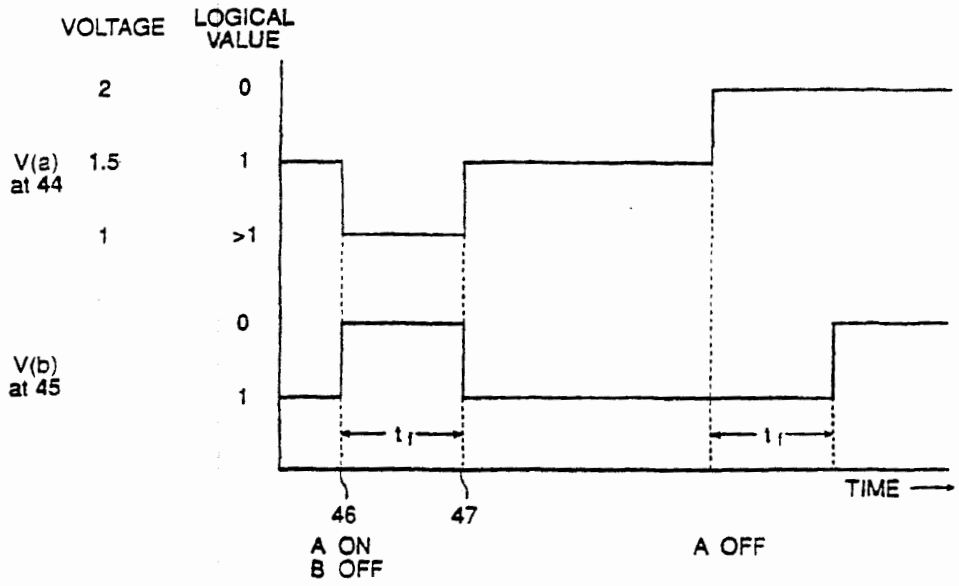

FIG. 7b

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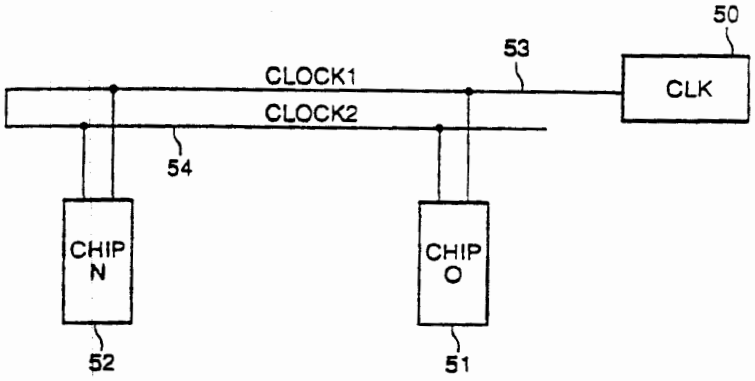

FIG. 8a

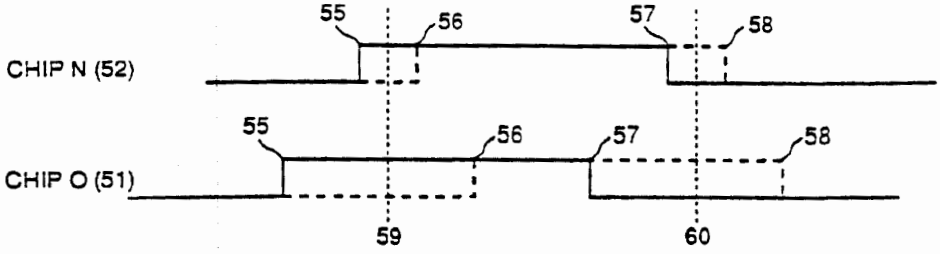

FIG. 8b

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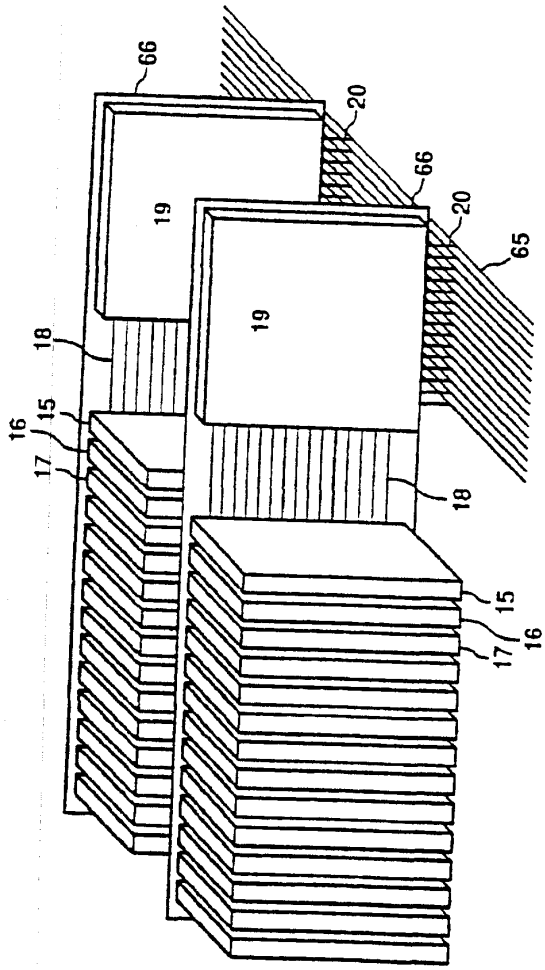

FIG. 9

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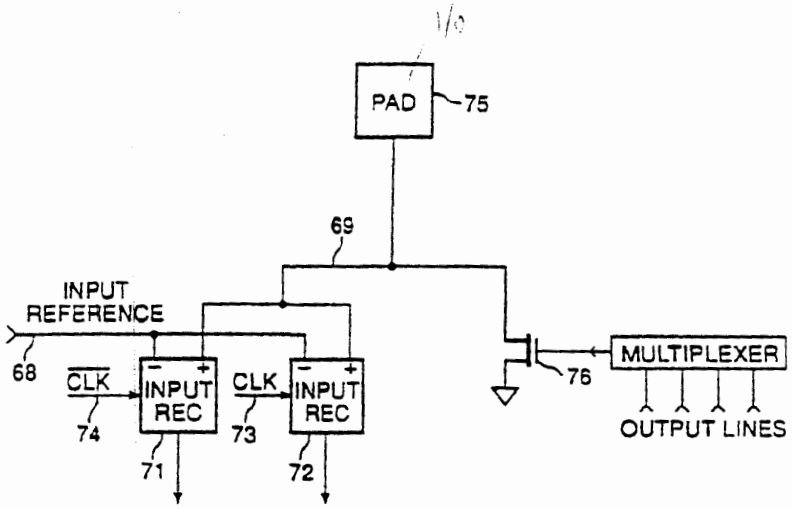

FIG. 10

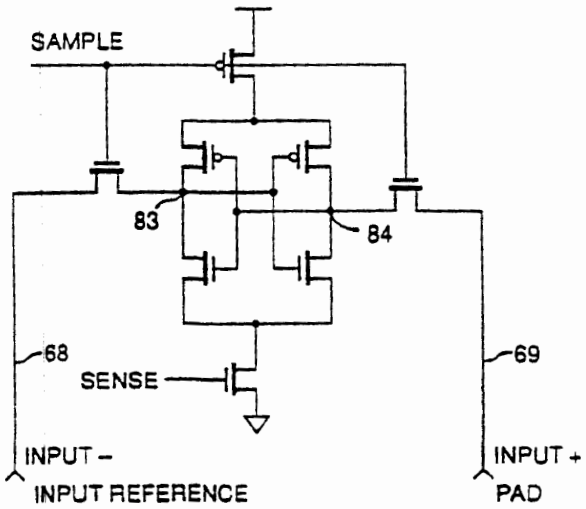

FIG. 11

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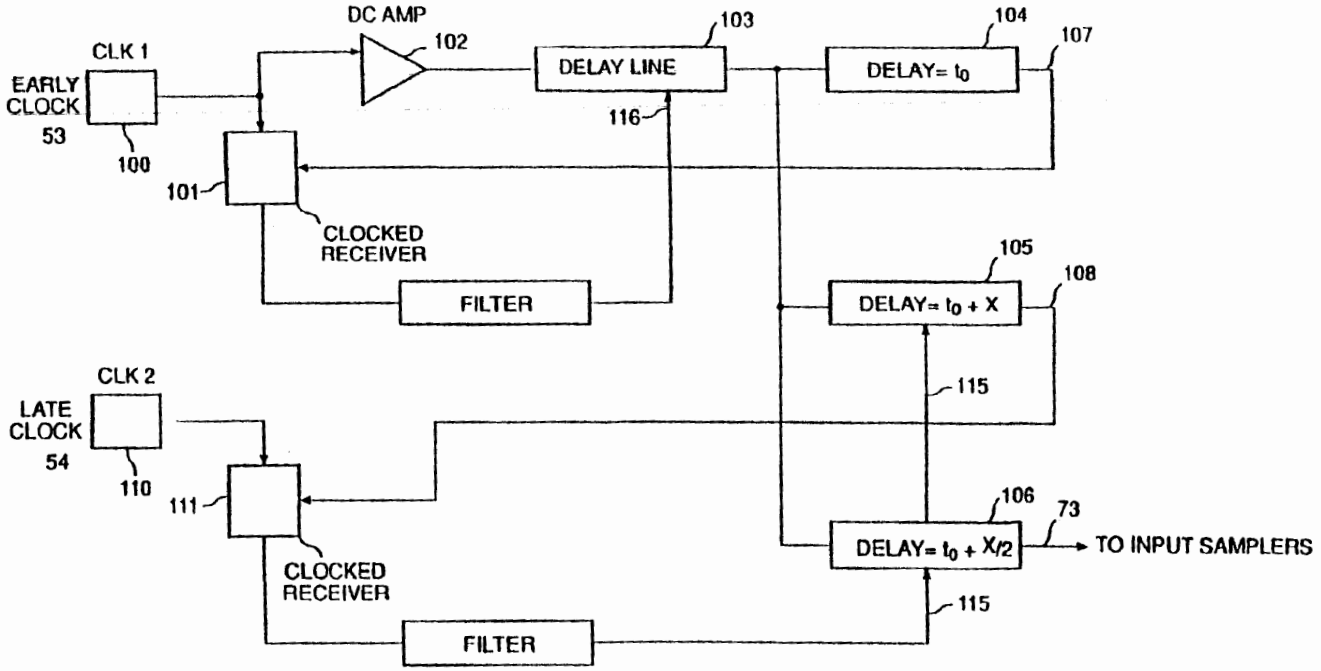

FIG. 12

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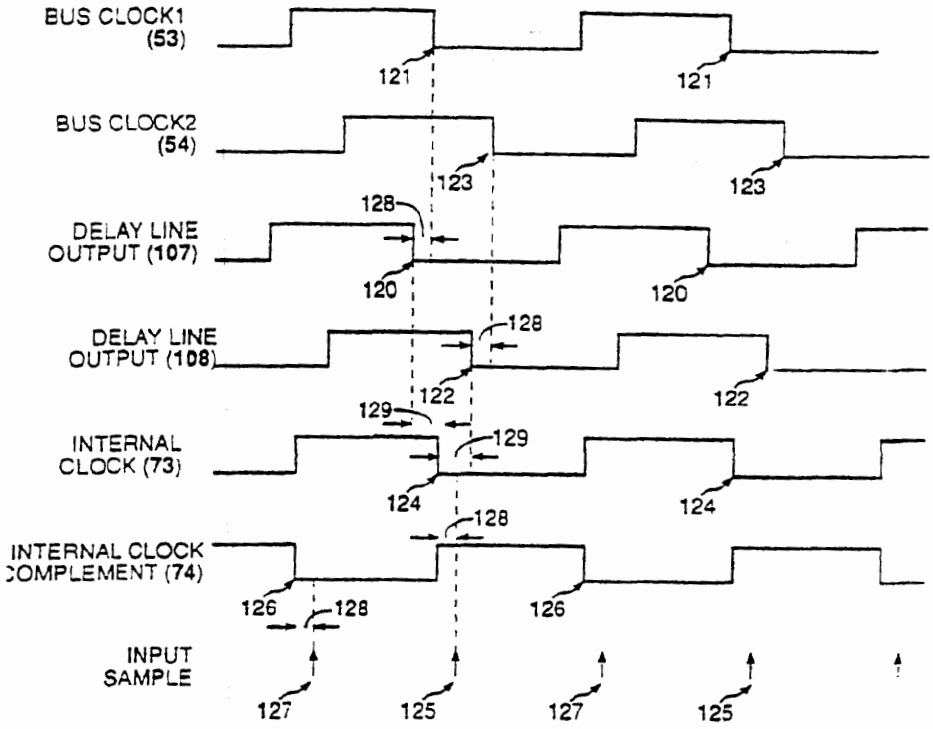

FIG. 13

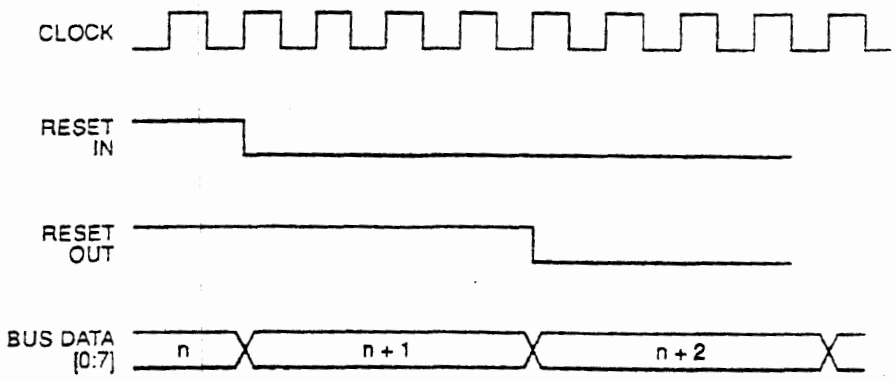

FIG. 14

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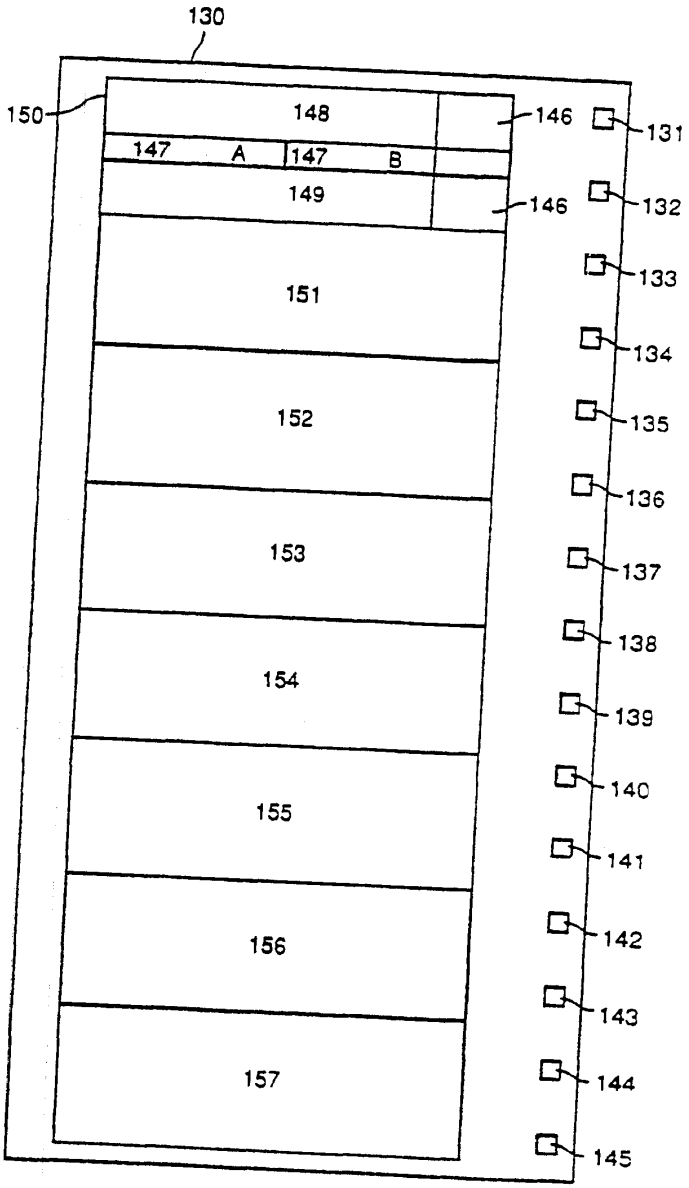

FIG. 15

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 3821715 A, Hoff **[0005]**
- US 4315308 A, Jackson **[0006]**
- US 4449207 A, Kung **[0007]**
- US 4764846 A **[0008]**
- US 4706166 A, Go **[0008]**
- US 3969706 A, Proebsting **[0009]**
- US 4595923 A **[0010]**
- US 4481625 A, Roberts **[0010]**
- US 4837682 A, Culler **[0011]**
- US 4818985 A, Ikeda **[0011]**
- US 4779089 A, Theus **[0011]**
- US 4745548 A, Blahut **[0011]**
- US 4247817 A, Heller **[0012]**
- US 4646279 A, Voss **[0013]**

Non-patent literature cited in the description

- **ANANT AGARWAL.** An Analytic Cache Model. *ACM Transactions on Computer Systems,* May 1989, vol. 7 (2), 184-215 **[0055]**
- **ANANT AGARWAL et al.** Scaleable Directory Schemes for Cache Consistency. *15th International Symposium on Computer Architecture,* June 1988, 280-289 **[0083]**
- **HANS SCHUMACHER et al.** CMOS Subnanosecond True-ECL Output Buffer. *J. Solid State Circuits,* February 1990, vol. 25 (1), 150-154 **[0100]**

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1000

(19) Europäisches Patentamt
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Office européen des brevets

(11) EP 1 816 570 A3

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
15.08.2007 Bulletin 2007/33

(43) Date of publication A2:
08.08.2007 Bulletin 2007/32

(21) Application number: **06125954.5**

(22) Date of filing: **16.04.1991**

(51) Int Cl.:
G06F 1/04 *(2006.01)* ***G06F 1/12*** *(2006.01)*
G06F 13/00 *(2006.01)* ***G06F 13/16*** *(2006.01)*
G06F 13/36 *(2006.01)* ***G06F 13/38*** *(2006.01)*
G11C 7/00 *(2006.01)* ***G11C 8/00*** *(2006.01)*
G11C 8/04 *(2006.01)*

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **18.04.1990 US 510898**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
00100018.1 / 1 022 641
91908374.1 / 0 525 068

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(54) **Integrated circuit I/O using a high performance bus interface**

(57) The present invention includes a semiconductor device, the semiconductor device comprising connection means adapted to connect the semiconductor device to an external bus which is a part of a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data, control and device select information needed by the semiconductor device for communication with substantially every other semiconductor device connected to the external bus, and wherein the external bus has substantially fewer bus lines than the number of bits in a single address, wherein each said bus line is a terminated transmission line, and wherein the external bus carries device-select information for said semiconductor device without the need for a separate device-select line connected directly to the semiconductor device, a bus line driver capable of producing a low-voltage-swing signal on one of said terminated transmission lines, wherein the semiconductor device is a semiconductor transceiver device to interface multiple units to the bus, wherein the multiple units are DRAMs.

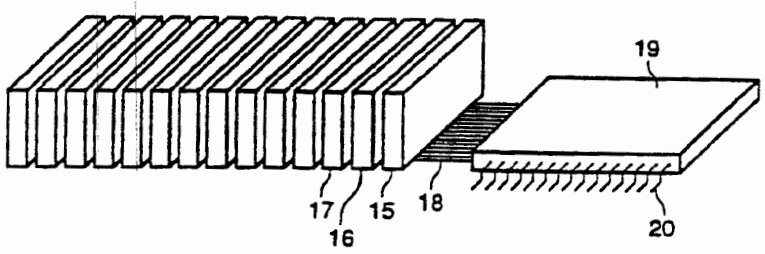

FIG. 3

EP 1 816 570 A3

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 06 12 5954

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	GB 1 262 691 A (BURROUGHS CORP [US]) 2 February 1972 (1972-02-02) * page 2, line 56 - line 82 * * page 5, line 104 - line 119 * -----	1-3	INV. G06F1/04 G06F1/12 G06F13/00 G06F13/16
A	US 4 630 193 A (KRIS BRYAN) 16 December 1986 (1986-12-16) * column 1, line 58 - column 2, line 4 * * column 2, line 40 - column 5, line 33 * * abstract; figure 1 * -----	1-3	G06F13/36 G06F13/38 G11C7/00 G11C8/00 G11C8/04
			TECHNICAL FIELDS SEARCHED (IPC)
			G06F G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	10 July 2007	NGUYEN XUAN HIEP, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

4

FPO FORM 1503 03.82 (P04C01)

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 06 12 5954

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

10-07-2007

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 1262691 A	02-02-1972	BE 741528 A	16-04-1970
		DE 1956515 A1	11-06-1970
		FR 2023120 A5	07-08-1970
		JP 52041604 B	19-10-1977
US 4630193 A	16-12-1986	EP 0077328 A1	27-04-1983
		WO 8203931 A1	11-11-1982

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, CA 92614
ETATS-UNIS D'AMERIQUE

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	28.11.2011

Applicant's or agent's file reference	IMPORTANT NOTIFICATION
NETL.048VPC	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2010/040826	01.07.2010	16.07.2009

Applicant
Netlist, Inc.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary report on patentability and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary report on patentability. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

The applicant's attention is drawn to Article 33(5), which provides that the criteria of novelty, inventive step and industrial applicability described in Article 33(2) to (4) merely serve the purposes of international preliminary examination and that "any Contracting State may apply additional or different criteria for the purposes of deciding whether, in that State, the claimed inventions is patentable or not" (see also Article 27(5)). Such additional criteria may relate, for example, to exemptions from patentability, requirements for enabling disclosure, clarity and support for the claims.

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	Slater, Sharon Tel. +49 89 2399-2565

Form PCT/IPEA/416 (January 2004)

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DEC 05 2011

KNOBBE, MARTENS,
OLSON & BEAR,LLP

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference NETL.048VPC	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/US2010/040826	International filing date *(day/month/year)* 01.07.2010	Priority date *(day/month/year)* 16.07.2009

International Patent Classification (IPC) or national classification and IPC
INV. G11C5/02

Applicant
Netlist, Inc.

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 6 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *(sent to the applicant and to the International Bureau)* a total of 26 sheets, as follows:
      - ☒ sheets of the description, claims and/or drawings which have been amended and/or sheets containing rectifications authorized by this Authority, unless those sheets were superseded or cancelled, and any accompanying letters (see Rules 46.5, 66.8, 70.16, 91.2, and Section 607 of the Administrative Instructions).
      - ☐ sheets containing rectifications, where the decision was made by this Authority not to take them into account because they were not authorized by or notified to this Authority at the time when this Authority began to draw up this report, and any accompanying letters (Rules 66.4bis, 70.2(e), 70.16 and 91.2).
      - ☐ superseded sheets and any accompanying letters, where this Authority either considers that the superseding sheets contain an amendment that goes beyond the disclosure in the international application as filed, or the superseding sheets were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in item 4 of Box No. I and the Supplemental Box (see Rule 70.16(b)).

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see paragraph 3*bis* of Annex C of the Administrative Instructions).

4. This report contains indications relating to the following items:
   - ☒ Box No. I Basis of the report
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☒ Box No. VII Certain defects in the international application
   - ☒ Box No. VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
14.05.2011	28.11.2011
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Fax: +49 89 2399 - 4465	Authorized officer Trifonov, Antoniy Telephone No. +49 89 2399-7168

Form PCT/IPEA/409 (Cover Sheet) (July 2011)

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/US2010/040826

Box No. I Basis of the report

1. With regard to the **language**, this report is based on

☒ the international application in the language in which it was filed

☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
- ☐ international search (under Rules 12.3(a) and 23.1(b))
- ☐ publication of the international application (under Rule 12.4(a))
- ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a) and (b))

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1-26	as originally filed	

Claims, Numbers

1-57	filed with telefax on 15-11-2011	

Drawings, Sheets

1-13	filed with the letter of	19-08-2010

☐ a sequence listing - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:
- ☐ the description, pages
- ☐ the claims, Nos.
- ☐ the drawings, sheets/figs
- ☐ the sequence listing *(specify)*:
- ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since either they are considered to go beyond the disclosure as filed, or they were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in the Supplemental Box (Rules 70.2(c) and (c-bis)):
- ☐ the description, pages
- ☐ the claims, Nos.
- ☐ the drawings, sheets/figs
- ☐ the sequence listing *(specify)*:

5. ☐ This report has been established:
- ☐ taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rules 66.1(d-bis) and 70.2(e)).
- ☐ without taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91(Rules 66.4bis and 70.2(e)).

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6. ☐ Supplementary international search report(s) from Authority(ies) has/have been received and taken into account in establishing this report (Rule 45bis.8(b) and (c)).

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	6-12, 18, 21-36, 41, 42, 45, 54, 56, 57
	No:	Claims	1-5, 13-17, 19, 20, 37-40, 43, 44, 46-53, 55
Inventive step (IS)	Yes:	Claims	6-12, 18, 21-36, 41, 42, 45, 54, 56, 57
	No:	Claims	1-5, 13-17, 19, 20, 37-40, 43, 44, 46-53, 55
Industrial applicability (IA)	Yes:	Claims	1-57
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

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Re Item V.

1 Reference is made to the following documents:

D1 US 2006/262586 A1 (SOLOMON JEFFREY C [US] ET AL) 23 November 2006 (2006-11-23)

D2 US 2008/162790 A1 (IM JEON-TAEK [KR]) 3 July 2008 (2008-07-03)

D3 US 2009/103387 A1 (SHAU JENG-JYE [US]) 23 April 2009 (2009-04-23)

2 The present application does not meet the criteria of Article 33(1) PCT, for the following reasons:

2.1 Document D2 discloses (see Figs. 6, 11, 12) a memory module comprising:
- at least one printed circuit board (510, 520, 530, 540);

- a plurality of memory devices (511a on Fig. 11, 420 on Fig. 6) mechanically coupled to the at least one printed circuit board;

- a control circuit (425, 516a, 516b) mechanically coupled to the at least one printed circuit board, the control circuit configurable to receive control signals from a system memory controller (410, 550) and to transmit module control signals to the plurality of memory devices (see Figs. 6, 12); and

- a plurality of data transmission circuits. The data transmission circuits in D1 are shown on Figs. 6 (page buffer 423) and 12 (fast enable transfer switches 515) and are mechanically coupled to the at least one printed circuit board and distributed at corresponding positions relative to the at least one printed circuit board. The plurality of data transmission circuits are further operatively coupled to the system memory controller (410) through the interface 516, receive module control signals from the control circuit (see the control unit 425 on Fig. 6), and are also used to latch (see pars. [0063, 0072]) the data written into or read out of the memory devices (e.g. the data transferred through the interface circuit 424). For the reason that they are used to latch both the input/ output data and are obviously time controlled by the control circuit 425, the data transmission circuits are considered to include read/write buffer- and drive/inhibit data- transmission functionality.

Further, at least one first data transmission circuit of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices (see Fig. 12, wherein one first circuit 515 is

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coupled to at least two memory devices, 511a and 511b), at least one second data transmission circuit (one second circuit 515) of the plurality of data transmission circuits is operatively coupled to at least two memory devices of the plurality of memory devices.

Independent claim 1 is therefore not new in the sense of Article 33(2) PCT.

2.2 Independent claim 21 periphrases and generalises the subject-matter of claim 1 by renaming the "data transmission circuits" in "circuits" and by removing the previously defined first and second data transmission circuits. On the other side claim 21 specifies that each of the plurality of circuits and the respectively coupled to each of them memory devices have different bit widths (understand that the respective read/write I/O data paths connected to the data transmission circuits have "bit widths") and thereby provides a feature, which is not disclosed in D2.
The subject-matter of independent claim 21 is therefore new over the prior art of D2.

2.3 Independent claim 31 corresponds to claim 21 in method terms and is also considered new over the prior art of D2.

2.4 Independent claims 37 and 48 respectively correspond to independent claims 21 and 31. The difference between the subject-matter of these claims is in that the plurality of data transmission circuits (in claim 21) or simply circuits (in claim 31) are replaced by a switching circuit (in claim 37) respectively a data load switching circuit (in claim 48). For a single switching circuit, which is coupled to a plurality of memory devices is, however, obvious to have a greater bit width than a single memory device (see in D2, wherein all the switches 515 build a switching circuit, which is coupled to all memory devices having each lower bit width).

Accordingly, the technical feature in claims 21 and 31, which makes a difference over the closest prior art of D2, is not considered to provide the same or even any difference between claims 37, 48 and said prior art.

The subject-matter of independent claims 37 and 48 is therefore not new over the prior art of D2.

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3 The data transmission circuits and the memory devices in D2 are not specified as having different bit widths as required by claims 6-9, 21-36 in the present application.

4 A tristate buffer, as defined in claims 18, 41, 42, 54, is not disclosed in the prior art of D2.

5 The memory module in D2 does not comprise SDRAM memory devices, as required by claims 10-12, 45, 56, 57 in the present application.

6 The features of the remaining dependent claims can either directly be found in the prior art or concern an obvious modification of the prior art and add nothing new or inventive to the independent claims.

Re Item VII.

7 The independent claims are not in the two-part form in accordance with Rule 6.3(b) PCT.

8 Reference signs are not inserted in parentheses in the claims in accordance with Rule 6.2(b) PCT.

9 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in documents D1 - D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII.

10 The various definitions of the invention given in the independent claims are such that the claims as a whole are not concise so that the requirements of Article 6 PCT are not met.

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November 14, 2011

VIA FACSIMILE (49.89.2933.4465)

International Preliminary Examining Authority
Attn: Authorized Officer Antoniy Trifonov
THE EUROPEAN PATENT OFFICE
D-80298 Munich
GERMANY

Re: **WRITTEN REPLY, UNDER RULE 66.3, TO WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY**
Title: SYSTEM AND METHOD UTILIZING DISTRIBUTED BYTE-WISE BUFFERS ON A MEMORY MODULE
Application No.: PCT/US2010/040826
Applicant: NETLIST, Inc.
Our Reference No.: NETL.048VPC

Dear Examiner Trifonov:

This letter is in response to the "Written Opinion of the International Preliminary Examining Authority" mailed October 24, 2011. With this response, the Applicant submits the following amendments and remarks.

The Applicant provides herewith an amended claim set on Replacement Pages 27-35 including Replacement Claims 1-57 which replace Claims 1-55 as previously filed on May 13, 2011. Additionally, for the Examiner's convenience, the Applicant includes a marked-up copy of the amended claim set showing the changes as compared to the previously-filed claims (Appendix A). The Applicant has amended Replacement Claims 10, 11, 15, 21, 25, 31, 33, 35-37, 40, 48, 50, 51, and 55, and has added new Claims 56 and 57.

The amendment to Claim 10 and the new Claims 56 and 57 recite that "the plurality of memory devices comprise one or more synchronous dynamic random access memory devices" and are supported by the application as originally filed, including but not limited to paragraph [0046].

The amendments to Claim 11 clarify the claim by using proper antecedent basis and do not add new matter to Claim 11. The amendments to Claim 50 clarify the claim by including the word "the" and do not add new matter to Claim 50.

The amendment to Claim 15 corrects a typographical error in its dependency and does not add new matter to Claim 15.

At least some of the amendments to Claims 21, 31, 37, and 48 recite the relationship between the bit width of the circuits and the bit widths of the memory devices and are supported by the application as originally filed, including but not limited to paragraph [0056].

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At least some of the amendments to Claims 21, 31, 37, and 48 and the amendments to Claims 25, 33, 35, 36, 40, 51, and 55 remove the terms "merge," "merges," and "merged" and instead refer to data being received. These amendments are supported by the application as originally filed, including but not limited to paragraphs [0055], [0056], and [0064].

The Applicant acknowledges that the Written Opinion has been established on the basis of previously-filed Claims 1-55. The Written Opinion indicates that each of these claims has industrial applicability. The Written Opinion also appears to indicate that (i) Claims 6-9, 18, 27, 28, 34, 39-42, 44, 45, and 52-54 also satisfy the criteria of novelty and inventive step, and that (ii) Claims 1-5, 10-17, 19-27, 29-33, 35-38, 43, 45-51, and 55 do not. The Applicant respectfully traverses each of the pending rejections. However, as discussed, the Applicant has amended certain Replacement Claims in order to advance prosecution.

Claim 1

Claim 1 was rejected as not being new in the sense of Article 33(2) PCT in view of U.S. Patent Application Publication No. 2008/0162790 ("D2"). The Applicant respectfully submits, however, that D2 fails to identically disclose every feature of Claim 1, so Claim 1 satisfies the criteria of novelty and inventive step over D2.

For example, D2 fails to disclose or render obvious, among other things:

> a plurality of data transmission circuits ... configurable to receive module control signals from the control circuit, ...
>
> wherein **the at least one first data transmission circuit is configurable to respond to the module control signals** by selectively driving or inhibiting data transmission between the system memory controller and at least one selected memory device..., and wherein **the at least one second data transmission circuit is configurable to respond to the module control signals** by selectively driving or inhibiting data transmission between the system memory controller and at least one selected memory device

(emphasis added).

In section 3.1, the Written Opinion identifies the "interfaces 516a and 516b" of D2 as the control circuit, the "fast enable transfer switches 515" of D2 as the data transmission circuits, and the DQS and SQ signals of D2 as the "module control signals." However, nowhere does D2 disclose or suggest that the "fast enable transfer switches 515" are configurable to respond to the DQS and SQ signals "by selectively driving or inhibiting data transmission between the system memory controller and at least one selected memory device," as is recited by Claim 1.

The only discussion of the operation of the "fast enable transfer switches 515" is found in paragraph [0072] of D2, which merely discloses that the "fast enable transfer switches 515" are "used to reduce loads on data buses, thereby enabling high-speed data transmission" and "are used to facilitate the use of the DDR transmission method" (D2 at ¶[0072]). Instead of responding to the DQS or SQ signals, the "fast enable transfer switches 515" of D2 appear to only pass the received DQS signals onto the "NBX NAND flash memories 511a and 511b" to which the switches 515 are connected (see, e.g., Fig. 12 of D2). Therefore, the "fast enable transfer switches 515" cannot be interpreted to be the data

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Received at the EPO on Nov 15, 2011 01:38:04. Page 3 of 25

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transmission circuits recited by Claim 1, and the DQS signals cannot be interpreted to be the "module control signals" recited by Claim 1.

Furthermore, the SQ signals of D2 also cannot be interpreted to be the "module control signals" of Claim 1. The SQ signals are produced by the memory devices and are not received by the switches 515 from the interface 516a, 516b (see, e.g., the single-headed arrow for SQ0~7 pointing away from the interface 516 in Fig. 12 of D2). Therefore, D2 does not disclose or suggest all the features of Claim 1.

In addition, the Written Opinion fails to identify any disclosure of D2 to correspond to "the plurality of data transmission circuits each comprising **at least one write buffer** configured to drive data onto at least two data paths to at least two corresponding memory devices of the plurality of memory devices and **at least one read buffer** configured to drive data from the corresponding at least two memory devices onto a data line to the system memory controller," as recited by Claim 1 (emphasis added).

While D2 describes at paragraph [0072] that "each of the FET switches 515 can latch 10 bits: 8 bits for data (DQ), 1 bit for a DQS signal, and 1 bit for a SQ signal," this passage does not disclose or suggest that the FET switches 515 comprise "at least one write buffer...and at least one read buffer," as recited by Claim 1. Instead, this passage is merely referring to the well-known technique of latching data lines by pulling them to their last valid logic level to keep the data bus stable (also known as "bus holding" or "bus keeping"). This interpretation is bolstered by Figs. 8 and 13 of D2, which show timing diagrams for the operation of the module of D2. These timing diagrams show DQ and DQS being toggled substantially immediately after the write enable (WE) command (see, Fig. 8 of D2) and substantially immediately after the read enable (RE) command (see, Fig. 13 of D2). None of these timing diagrams show the values of DQ or DQS being latched and then outputted some clock cycles later. Thus, the disclosure of D2 is not consistent with the interpretation being relied upon by the Written Opinion in rejecting Claim 1 that "the FETs are therefore responsible for inhibition/driving of data to/from the memory devices."

At least for the above reasons, the Applicant respectfully submits that D2 does not identically disclose or render obvious every feature of Claim 1, so Claim 1 is patentably distinguished from D2.

Independent Claims 21, 31, 37, and 48

Claims 21, 31, 37, and 48 were also rejected for not being new in view of D2. The Applicant respectfully submits, however, that these claims are patentably distinguished from D2, at least for reasons similar to those set forth with respect to Claim 1.

Claim 21 has been amended to recite "a plurality of circuits each having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit with smaller than the first bit width." The Applicant submits that this feature is not disclosed or suggested by D2, so at least for this additional reason, Claim 21 is patentably distinguished over D2.

Claim 31 has been amended to recite that "the received data signals each having a bit width less than a bit width of the data transmission circuit." The Applicant submits that this

ation: 15.11.2011 01:33:10 - 15.11.2011 01:38:04. This page 4 of 25 was completed at 15.11.2011 01:34:06
Received at the EPO on Nov 15, 2011 01:38:04. Page 4 of 25

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feature is not disclosed or suggested by D2, so at least for this additional reason, Claim 31 is patentably distinguished over D2.

Claim 37 has been amended to recite "a switching circuit configured to transmit data to and from the plurality of memory devices, the switching circuit having a first bit width and ... a memory device of the plurality of memory devices has a second bit width less than the first bit width." The Applicant submits that this feature is not disclosed or suggested by D2, so at least for this additional reason, Claim 37 is patentably distinguished over D2.

Claim 48 has been amended to recite "the load-reducing switching circuit having a first bit width ..., the memory devices each having a second bit width less than the first bit width." The Applicant submits that this feature is not disclosed or suggested by D2, so at least for this additional reason, Claim 48 is patentably distinguished over D2.

Dependent Claims 2-20, 22-30, 32-36, 38-47, and 49-55

In the Written Opinion, dependent Claims 6-9, 18, 27, 28, 34, 39-42, 44, 45, and 52-54 were found to satisfy the novelty and inventive step criteria, and dependent Claims 2-5, 10-17, 19, 20, 22-26, 29, 30, 32, 33, 35, 36, 38, 43, 46, 47, 49-51, and 55 were rejected in view of D2. Each of Claims 2-5, 10-17, 19, 20, 22-26, 29, 30, 32, 33, 35, 36, 38, 43, 46, 47, 49-51, and 55 is dependent upon one of Claims 1, 21, 31, 37, and 48. Therefore, each of Claims 2-5, 10-17, 19, 20, 22-26, 29, 30, 32, 33, 35, 36, 38, 43, 46, 47, 49-51, and 55 is patentably distinguished from the references for at least the reasons set forth with respect to its corresponding independent claim, based on its dependency and for its additional features.

New Dependent Claims 56 and 57

New dependent Claim 56 is dependent from Claims 31 and 48 and new dependent Claim 57 is dependent upon Claim 37. Therefore, each of Claims 56 and 57 is patentably distinguished from the references for at least the reasons set forth with respect to its corresponding independent claim, based on its dependency and for its additional features.

CONCLUSION

The Applicant submits that the present claims meet the requirements of PCT Articles 33(2) and 33(3). Nevertheless, if any undeveloped issues remain or if any issues require clarification, the Examiner is invited to contact the undersigned.

Sincerely,

Daniel E. Altman

Enclosures

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WHAT IS CLAIMED IS:

1. A memory module comprising:

at least one printed circuit board;

a plurality of memory devices mechanically coupled to the at least one printed circuit board;

a control circuit mechanically coupled to the at least one printed circuit board, the control circuit configurable to receive control signals from a system memory controller and to transmit module control signals to the plurality of memory devices; and

a plurality of data transmission circuits mechanically coupled to the at least one printed circuit board and distributed at corresponding positions relative to the at least one printed circuit board, the plurality of data transmission circuits configurable to be operatively coupled to the system memory controller and configurable to receive module control signals from the control circuit, the plurality of data transmission circuits each comprising at least one write buffer configured to drive data onto at least two data paths to at least two corresponding memory devices of the plurality of memory devices and at least one read buffer configured to drive data from the corresponding at least two memory devices onto a data line to the system memory controller,

wherein at least one first data transmission circuit of the plurality of data transmission circuits is operatively coupled to a first at least two memory devices of the plurality of memory devices, at least one second data transmission circuit of the plurality of data transmission circuits is operatively coupled to a second at least two memory devices of the plurality of memory devices,

wherein the at least one first data transmission circuit is configurable to respond to the module control signals by selectively driving or inhibiting data transmission between the system memory controller and at least one selected memory device of the first at least two memory devices operatively coupled to the at least one first data transmission circuit, and wherein the at least one second data transmission circuit is configurable to respond to the module control signals by selectively driving or inhibiting data transmission between the system memory controller and at least one

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selected memory device of the second at least two memory devices operatively coupled to the at least one second data transmission circuit.

2. The memory module of Claim 1, wherein the at least one first data transmission circuit comprises a byte-wise buffer.

3. The memory module of Claim 2, wherein the at least one second data transmission circuit comprises a byte-wise buffer.

4. The memory module of Claim 1, wherein the at least one first data transmission circuit has the same bit width as does each of the first at least two memory devices to which the at least one first data transmission circuit is operatively coupled.

5. The memory module of Claim 4, wherein the at least one second data transmission circuit has the same bit width as does each of the second at least two memory devices to which the at least one second data transmission circuit is operatively coupled.

6. The memory module of Claim 1, wherein the at least one first data transmission circuit has a first bit width and each of the first at least two memory devices to which the at least one first data transmission circuit is operatively coupled has a second bit width which is less than the first bit width.

7. The memory module of Claim 6, wherein the at least one first data transmission circuit is operatively coupled to two memory devices per rank, and the first bit width is twice the second bit width.

8. The memory module of Claim 6, wherein the at least one second data transmission circuit has a third bit width and each of the second at least two memory devices to which the at least one second data transmission circuit is operatively coupled has a fourth bit width which is less than the third bit width.

9. The memory module of Claim 8, wherein the at least one second data transmission circuit is operatively coupled to two memory devices per rank, and the third bit width is twice the fourth bit width.

10. The memory module of Claim 1, wherein the plurality of memory devices comprise one or more synchronous dynamic random access memory devices.

11. The memory module of Claim 10, wherein the corresponding positions of the at least one first data transmission circuit and the at least one second data transmission circuit are along an edge of the at least one printed circuit board such that the at least one first data transmission circuit is located substantially between the edge and at least some of the first at

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least two memory devices operatively coupled to the at least one first data transmission circuit and the at least one second data transmission circuit is located substantially between the edge and at least some of the second at least two memory devices operatively coupled to the at least one second data transmission circuit.

12. The memory module of Claim 11, wherein the at least one printed circuit board comprises a connector comprising a plurality of electrical contacts which are positioned on the edge of the at least one printed circuit board and are configured to be releasably coupled to corresponding contacts of a computer system socket.

13. The memory module of Claim 1, wherein a package containing the at least one first data transmission circuit is at a location spaced from a location of a package containing the at least one second data transmission circuit.

14. The memory module of Claim 13, wherein a position of the at least one first data transmission circuit is generally aligned with one or more of the first at least two memory devices operatively coupled to the at least one first data transmission circuit.

15. The memory module of Claim 14, wherein the at least one first data transmission circuit and the first at least two memory devices operatively coupled to the at least one first data transmission circuit are positioned generally along a line that is substantially perpendicular to an edge of the at least one printed circuit board.

16. The memory module of Claim 13, wherein a position of the at least one first data transmission circuit is generally offset from a line defined by the positions of the first at least two memory devices operatively coupled to the at least one first data transmission circuit.

17. The memory module of Claim 16, wherein the line is substantially perpendicular to an edge of the at least one printed circuit board and the at least one first data transmission circuit is offset from the line in a direction generally along the edge.

18. The memory module of Claim 1, wherein the at least one write buffer comprises at least one tristate buffer and the at least one read buffer comprises at least one tristate buffer.

19. The memory module of Claim 1, wherein the at least one write buffer regenerates data signals from the system memory controller and wherein the at least one read buffer regenerates data signals from the memory devices.

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20. The memory module of Claim 1, wherein read data that is selectively driven by the first data transmission circuit is transmitted through the at least one read buffer of the first data transmission circuit, and wherein write data that is driven by the first data transmission circuit is transmitted through the at least one write buffer of the first data transmission circuit, and wherein read data that is selectively driven by the second data transmission circuit is transmitted through the at least one read buffer of the second data transmission circuit, and wherein write data that is selectively driven by the second data transmission circuit is transmitted through the at least one write buffer of the second data transmission circuit.

21. A memory module comprising:

a plurality of memory devices;

a controller configured to receive control information from a system memory controller and to produce module control signals; and

a plurality of circuits each having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit width smaller than the first bit width and comprising at least one write buffer and at least one read buffer, the plurality of circuits configured to selectively isolate the plurality of memory devices from the system memory controller, wherein the circuits are operable, in response to the module control signals, to actively drive write data from the system memory controller to the plurality of memory devices through the at least one write buffer and to receive and drive read data from the plurality of memory devices to the system memory controller through the at least one read buffer, wherein the circuits are distributed at corresponding positions separate from one another.

22. The memory module of Claim 21, wherein the plurality of circuits is contained in a plurality of packages at locations spaced from one another.

23. The memory module of Claim 22, wherein the plurality of memory devices, the controller, and the plurality of circuits are mechanically coupled to a printed circuit board having an edge, wherein the packages are positioned along the edge and between the edge and the plurality of memory devices.

24. The memory module of Claim 21, wherein the circuits comprise byte-wise buffers.

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25. The memory module of Claim 21, wherein the each circuit of the plurality of circuits comprises:

a data terminal configurable to be operatively coupled to the system memory controller;

a first memory terminal configurable to be operatively coupled to a first group of the plurality of memory devices; and

a second memory terminal configurable to be operatively coupled to a second group of the plurality of memory devices;

wherein, when the circuit actively drives write data, the data terminal is operatively coupled to one of the first memory terminal and the second memory terminal; and

wherein, when the circuit receives and drives read data, one of the first memory terminal and the second memory terminal is operatively coupled to the data terminal.

26. The memory module of Claim 21, wherein the memory module is a dual in-line memory module.

27. The memory module of Claim 21, wherein the plurality of memory devices comprise one or more synchronous dynamic random access memory devices.

28. The memory module of Claim 21, wherein the at least one write buffer of each of the plurality of circuits comprises at least one tristate buffer and the at least one read buffer of the plurality of circuits comprises at least one tristate buffer.

29. The memory module of Claim 21, wherein the at least one write buffer of each of the plurality of circuits regenerates data signals from the system memory controller.

30. The memory module of Claim 21, wherein the at least one read buffer of each of the plurality of circuits regenerates data signals from the memory devices.

31. A method of operating a memory module comprising a plurality of memory devices, the method comprising:

providing a data transmission circuit on a data line between a computer system memory controller and the plurality of memory devices of the memory module, the data transmission circuit comprising a byte-wise data buffer comprising at least one write buffer and at least one read buffer;

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during a write operation, enabling the data transmission circuit to drive a data signal from the computer system memory controller on one of a plurality of paths to the memory devices of the memory module through the at least one write buffer; and

during a read operation, enabling the data transmission circuit to receive a plurality of data signals from the memory devices of the memory module and to drive the received data signals to the computer system memory controller through the at least one read buffer, the received data signals each having a bit width less than a bit width of the data transmission circuit.

32. The method of Claim 31, further comprising providing a controller configured to receive control information from the computer system memory controller and to produce at least one module control signal in response to the control information, wherein enabling the data transmission circuit to drive a data signal comprises transmitting the at least one module control signal from the controller to the data transmission circuit.

33. The method of Claim 31, further comprising providing a controller configured to receive control information from the computer system memory controller and to produce at least one module control signal in response to the control information, wherein enabling the data transmission circuit to receive the plurality of data signals comprises transmitting the at least one module control signal from the controller to the data transmission circuit.

34. The method of Claim 31, wherein the at least one write buffer comprises at least one tristate buffer and the at least one read buffer comprises at least one tristate buffer.

35. The method of Claim 31, wherein, during a write operation, the byte-wise data buffer regenerates the data signal from the computer system memory controller and drives the regenerated data signal to the memory devices of the memory module, and wherein, during a read operation, the byte-wise data buffer regenerates the received data signals and drives the regenerated received data signals to the computer system memory controller.

36. The method of Claim 31, wherein during a write operation, the data signal is regenerated and driven by the at least one write buffer to the memory devices of the memory module, and during a read operation, the received data signals are regenerated and driven by the at least one read buffer to the computer system memory controller.

37. A memory module comprising:

a plurality of memory devices;

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a controller configured to receive control information from a system memory controller and produce module control signals; and

a switching circuit configured to transmit data to and from the plurality of memory devices, the switching circuit having a first bit width and comprising at least one write buffer and at least one read buffer, the switching circuit configured to isolate the plurality of memory devices from the system memory controller, wherein the switching circuit is operable, in response to the module control signals, to drive write data from the system memory controller to the plurality of memory devices through the at least one write buffer and to receive read data from the plurality of memory devices, wherein a memory device of the plurality of memory devices has a second bit width less than the first bit width, the received read data transmitted to the system memory controller through the at least one read buffer.

38. The memory module of claim 37, wherein the plurality of memory devices comprises a first group of the plurality of memory devices in a first rank and a second group of the plurality of memory devices in a second rank.

39. The memory module of claim 38, wherein the plurality of memory devices further comprises a third group of the plurality of memory devices in a third rank and a fourth group of the plurality of memory devices in a fourth rank, and where data lines of the first rank are connected to data lines of the first rank and to the switching circuit, and data lines of the second rank are connected to data lines of the fourth rank and to the switching circuit.

40. The memory module of claim 37, wherein the switching circuit comprises:

a data terminal for coupling to the system memory controller;

a first memory terminal coupled to the first group of the plurality of memory devices; and

a second memory terminal coupled to the second group of the plurality of memory devices;

wherein, when the switching circuit drives write data, the data terminal is coupled to one of the first memory terminal and the second memory terminal through the at least one write buffer; and

wherein, when the switching circuit receives read data from the plurality of memory devices, one of the first memory terminal and the second memory terminal is coupled to the data terminal through the at least one read buffer.

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41. The memory module of claim 40, wherein the at least one write buffer further comprises:

a first tristate buffer configured to conditionally drive the first memory terminal; and

a second tristate buffer configured to conditionally drive the second memory terminal.

42. The memory module of claim 41, wherein the at least one read buffer further comprises a multiplexer configured to receive data signals from the first memory terminal and data signals from the second memory terminal and supply data signals selected from the data signals received from the first memory terminal and the data signals received from the second memory terminal to the at least one read buffer.

43. The memory module of claim 37, wherein the memory module is a dual in-line memory module.

44. The memory module of claim 38, wherein the memory module is configured to combine the first rank and the second rank into one logical memory rank.

45. The memory module of claim 37, wherein the memory devices comprise synchronous dynamic random access memories.

46. The memory module of claim 37, wherein the switching circuit is configured to reshape a signal waveform.

47. The memory module of claim 37, wherein the controller comprises a register for latching address and control signals from the memory controller.

48. A method of operating a memory module comprising a plurality of memory devices, the method comprising:

providing a load-reducing switching circuit on a data line between a computer system memory controller and the plurality of memory devices of the memory module, the load-reducing switching circuit having a first bit width;

during a write operation, enabling the load-reducing switching circuit to drive a data signal from the computer system memory controller on one of a plurality of paths through at least one write buffer of the load-reducing switching circuit to the memory devices of the memory module; and

during a read operation, enabling the load-reducing switching circuit to receive a plurality of data signals from the memory devices of the memory module,

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the memory devices each having a second bit width less than the first bit width, and driving the received data signals through at least one read buffer of the load-reducing switching circuit to the computer system memory controller.

49. The method of claim 48, wherein the enabling of the load-reducing switching circuit comprises extracting control information from the computer system memory controller to provide an enable control signal to the load-reducing switching circuit.

50. The method of claim 48, wherein during a write operation, the enabling of the load-reducing switching circuit to drive a data signal from the computer system memory controller on one of a plurality of paths to the memory devices of the memory module comprises regenerating the data signal using the at least one write buffer.

51. The method of claim 48, wherein during a read operation, the enabling of the load-reducing switching circuit to receive the plurality of data signals from the memory devices of the memory module and driving the received data signals to the computer system memory controller comprises performing a multiplex function on data signals from the memory devices of the memory module.

52. The method of claim 48, further comprising combining two or more physical memory ranks into one logical memory rank.

53. The method of claim 52, wherein the two or more physical memory ranks are accessible with a single chip select signal from the computer system memory controller.

54. The method of claim 48, wherein the at least one write buffer comprises at least one tristate buffer and the at least one read buffer comprises at least one tristate buffer.

55. The method of claim 48, wherein during a read operation, the enabling of the load-reducing switching circuit to receive the plurality of data signals from the memory devices of the memory module and driving the received data signals to the computer system memory controller comprises regenerating the received data signals using the at least one read buffer.

56. The method of Claim 31 or Claim 48, wherein the plurality of memory devices comprises one or more synchronous dynamic random access memory devices.

57. The memory module of Claim 37, wherein the plurality of memory devices comprises one or more synchronous dynamic random access memory devices.

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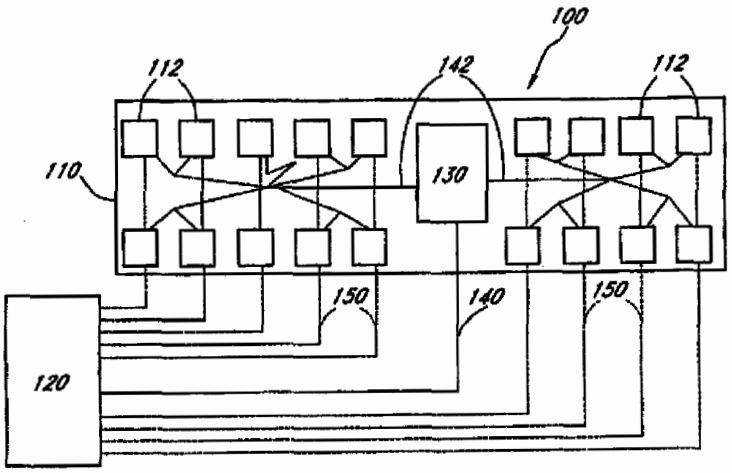

FIG. 1A
(Prior Art)

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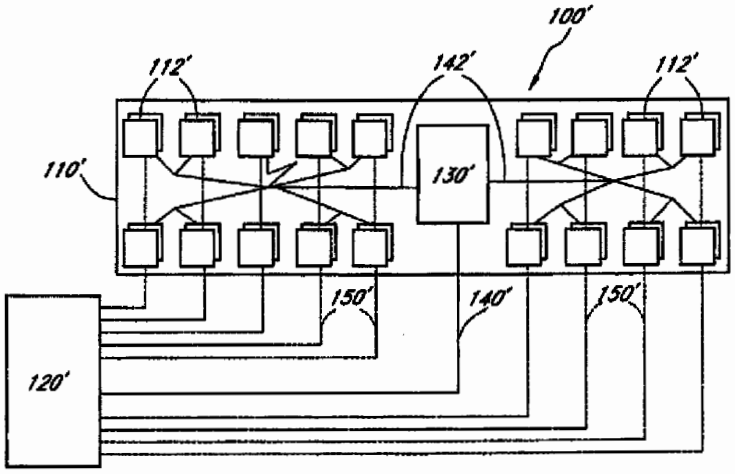

FIG. 1B
(Prior Art)

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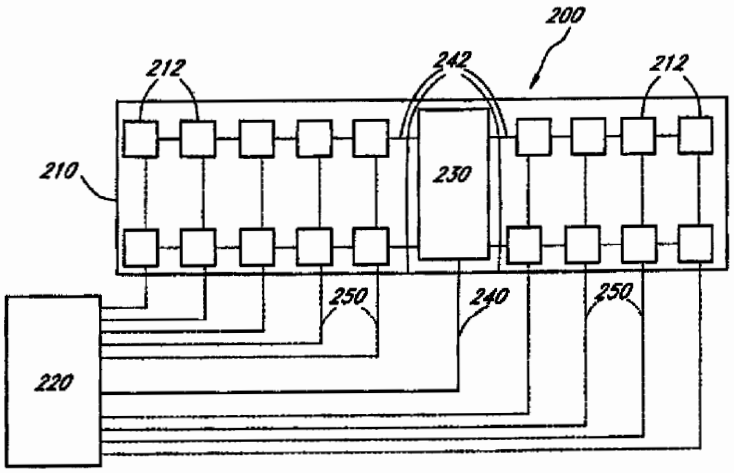

FIG. 2A
(Prior Art)

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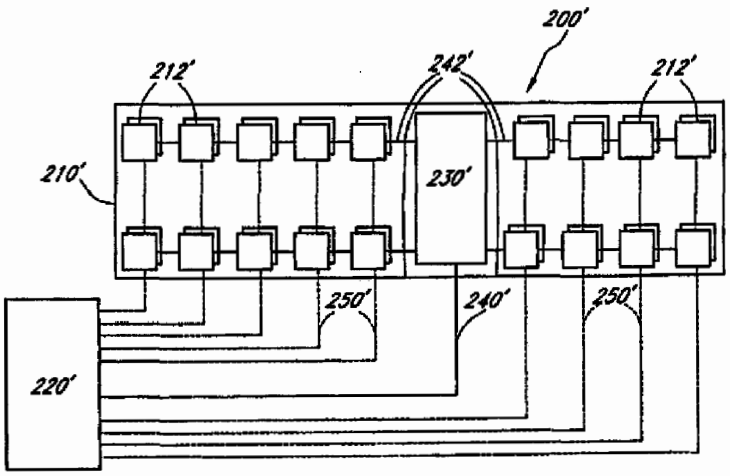

FIG. 2B
(Prior Art)

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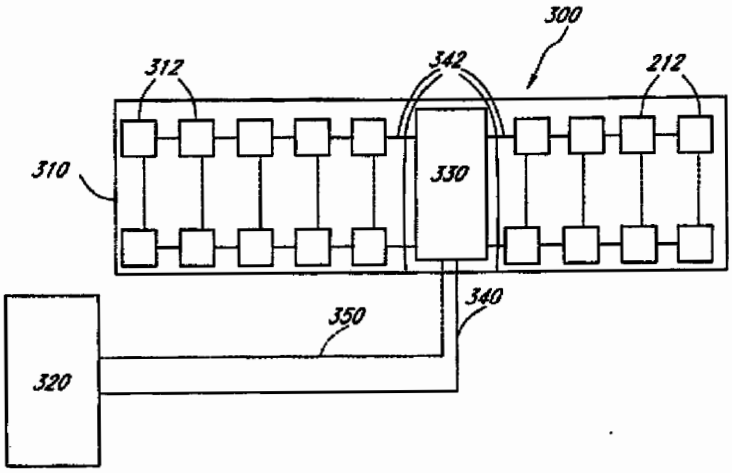

FIG. 2C
(Prior Art)

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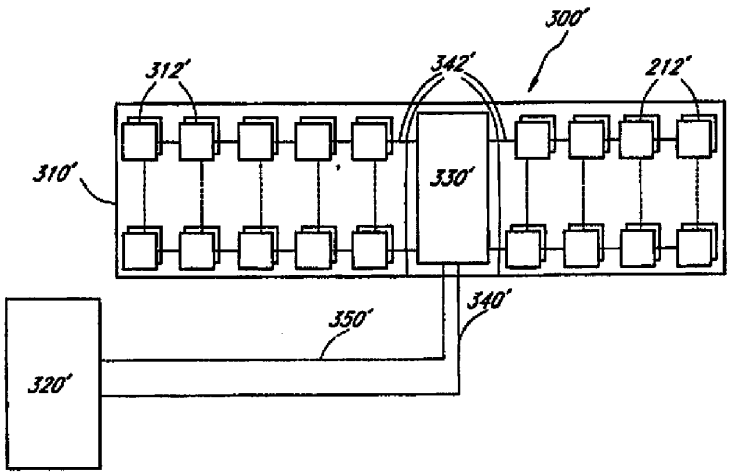

FIG. 2B
(Prior Art)

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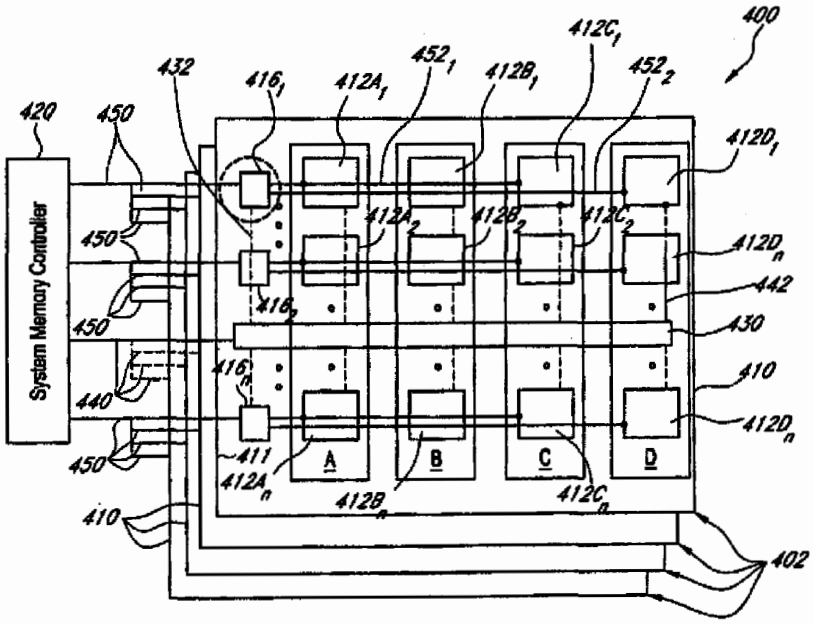

FIG. 3A

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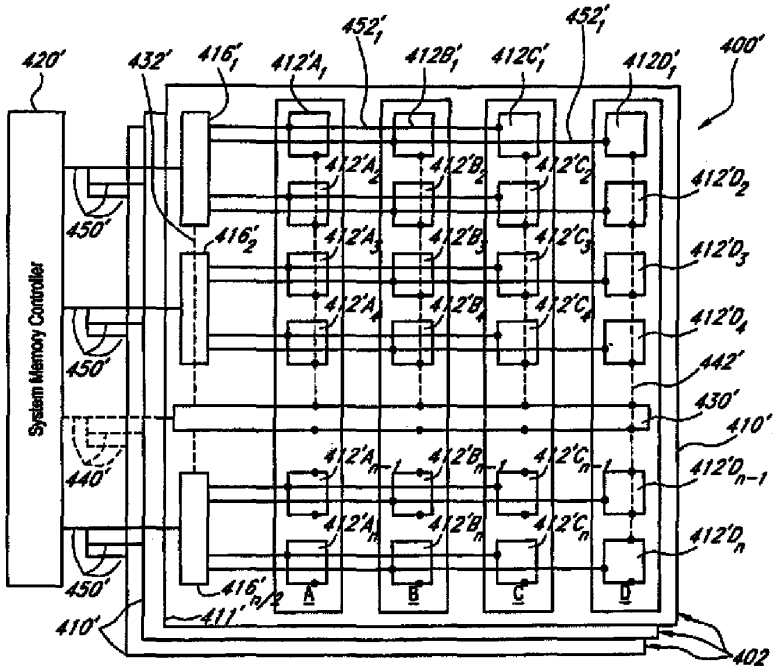

FIG. 3B

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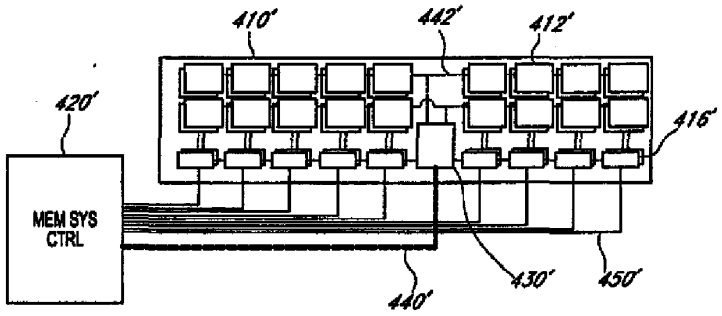

FIG. 3C

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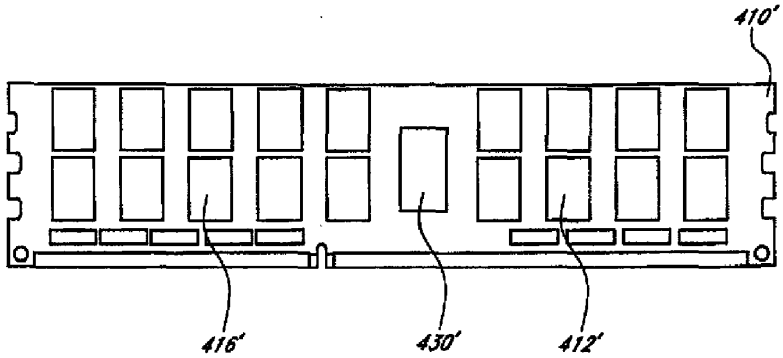

FIG. 3D

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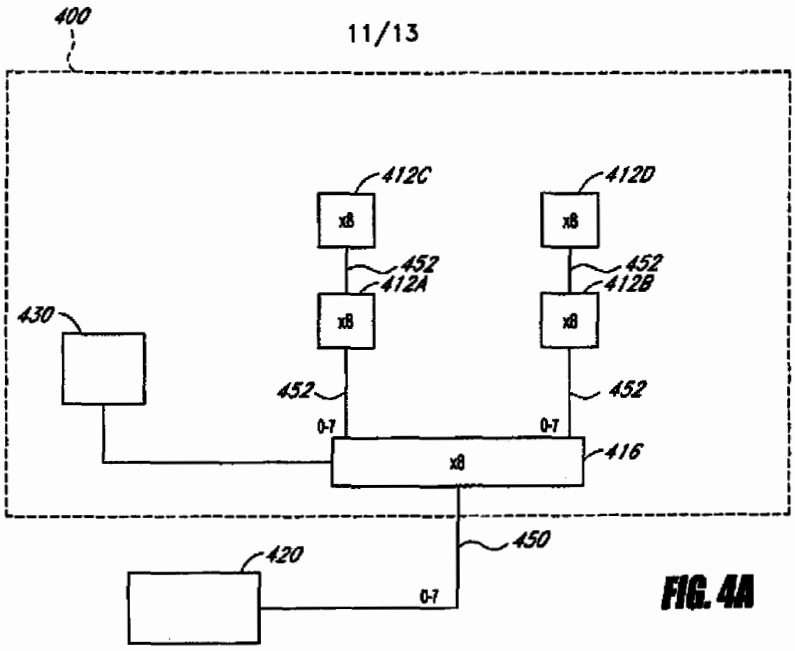

FIG. 4A

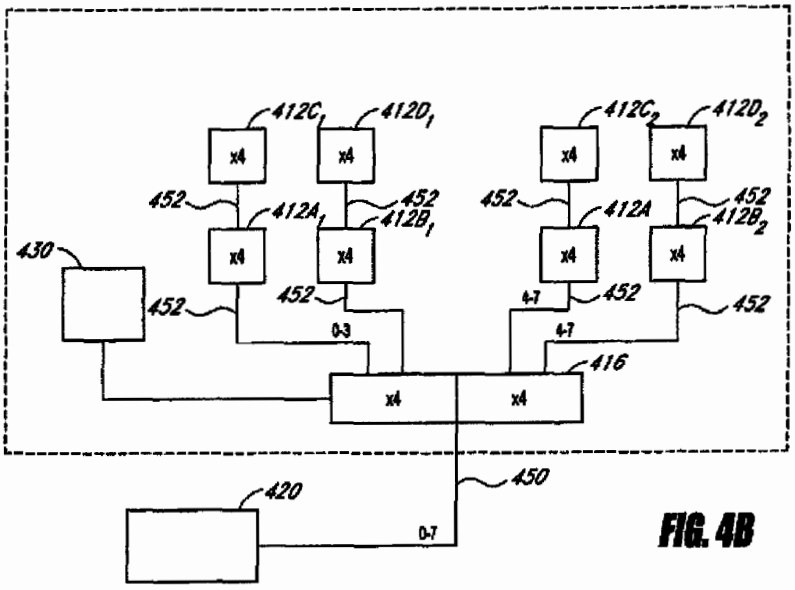

FIG. 4B

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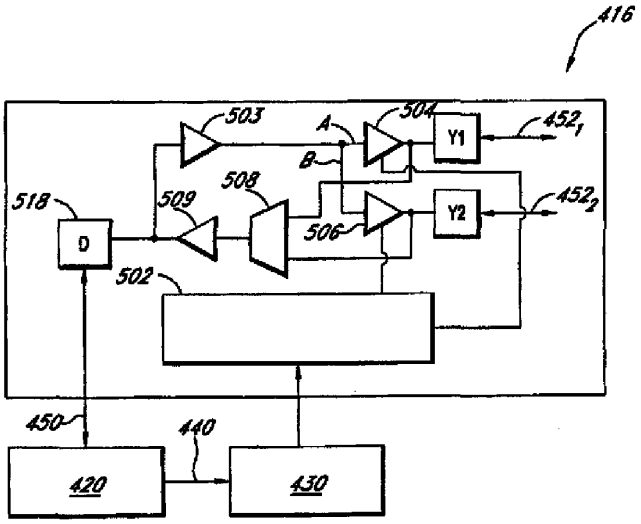

FIG. 5

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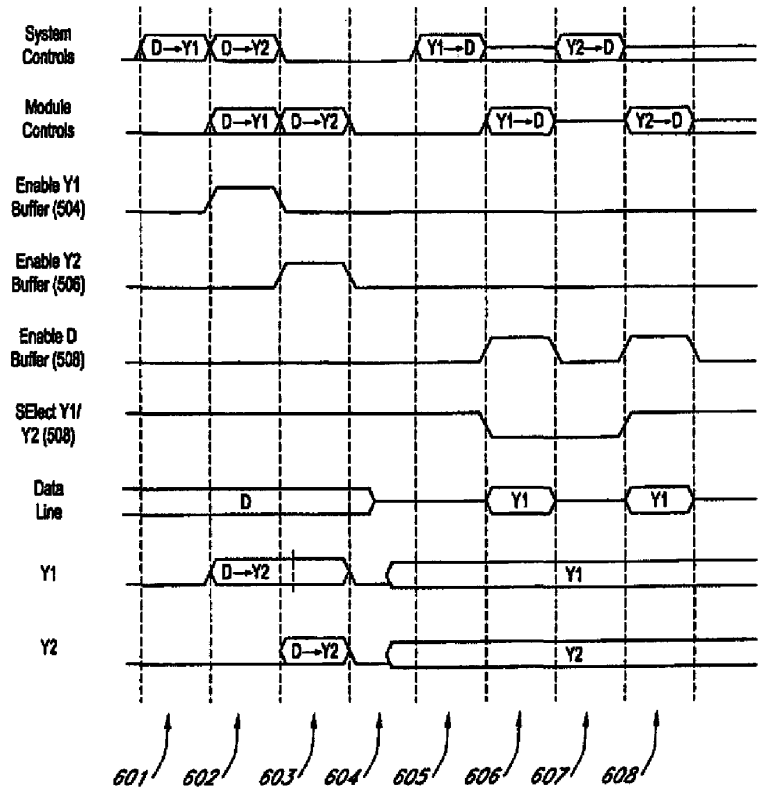

FIG. 6

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Electronic Acknowledgement Receipt

EFS ID:	21124728
Application Number:	13952599
International Application Number:	
Confirmation Number:	6784
Title of Invention:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NT003US
Receipt Date:	06-JAN-2015
Filing Date:	27-JUL-2013
Time Stamp:	01:46:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	2007-08-08_EP1816570.pdf	2964754 92a7814f6c8df013c5e8b56c77fee9f2221650c2	no	43

Warnings:	
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10	Foreign Reference	2002-07-25_WO_02-058069-A2.pdf	1499332 881e0785be275d5deaa043c38e0869f694762b45	no	30
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Information:					

11	Foreign Reference	2002-08-15_WO_02063804_A2.pdf	1449300 0770796bf0a9759fec57af199414fe3150f61108	no	38
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Information:					
12	Foreign Reference	2003-02-27_WO_03-017283_A1.pdf	1358193 6d0e561c314eb5974036a7d106200dce0317184d	no	35
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13	Foreign Reference	2003-08-21_WO_03-069484_A2.pdf	733234 f5c92e171afbc47d746e326d53635fb5b25496db	no	20
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Information:					
14	Foreign Reference	2006-05-26_WO_2006-055497_A2.pdf	780966 64a60a27371955ebc5e2112f63d28d9c7f782854	no	20
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Information:					
15	Non Patent Literature	2010-09-27_ISA_NETL048VPC.pdf	3697704 14a028fbcf203d0058e8fb17e39fcabd3f0d5819	no	103
Warnings:					
Information:					
16	Non Patent Literature	2011-10-24_Written_Opinion_NETL048VPC.pdf	193206 698efd293f375cddb6073a3b39b5f2bd5cd1b230	no	7
Warnings:					
Information:					
17	Non Patent Literature	2013-01-30_PCT_Search_Report_Written_Opinion-NETL071WO.pdf	7352527 5e385e1e2b51f31def4d74023769a0af67e82849	no	127
Warnings:					
Information:					
18	Non Patent Literature	2013-02-12_Notice_of_Allowance_048A.pdf	2287416 0c5794115a0cd49f569c122cc0850ba4169798a5	no	52
Warnings:					
Information:					
19	Non Patent Literature	2012-09-13_NFOA_NETL048CP1.pdf	751902 7d30827ade262f6794bdc2c155d261510ee87f5a	no	20
Warnings:					
Information:					

20	Non Patent Literature	2013-03-13_Rsps_to_non-final_OA_NETL_048CP1.pdf	301199 06f84c4aa58f1d9a0273f382ae492be0c9f81869	no	16
Warnings:					
Information:					
21	Non Patent Literature	2013-07-11_NOA_NETL048CP1.pdf	2197715 61bc8befc653a672386156ee28961a053c03b599	no	37
Warnings:					
Information:					
22	Non Patent Literature	2014-06-24_Petition_IPR2014-01029.pdf	995769 5f532e07581069892a1ca0f985e08ec811c3dade	no	64
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Information:					
23	Non Patent Literature	2011-11-28_IPRP_NETL048VPC.pdf	2829935 0f7b0b2a3c1d583ae89047b17dc9ace6e7273f3c	no	34
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24	Non Patent Literature	Exhibit-1008.pdf	3815500 f78bf592ac00ef2763330ada32e48e7ffb184678	no	173
Warnings:					
Information:					
25	Non Patent Literature	2014-07-23_Supp_Petition_IPR2014-01029.pdf	1058145 12b230bca6dbf7f1e89206150d7ba6fc10dbf2be	no	65
Warnings:					
Information:					
26	Non Patent Literature	2014-10-17_Prelim_Rsps_IPR2014-01029.pdf	3272498 de4f42dccc84d138ce64e88f09df639d62db5988	no	56
Warnings:					
Information:					
27	Non Patent Literature	2014-12-16_decision_denying_Institution.pdf	672087 c4cff0575c18a15433ae803328bede744a08e537	no	22
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Information:					
28	Non Patent Literature	2014-09-22_Corrected_Petition_IPR2014-01369.pdf	912271 db81c4f9f7c8d687e8a242440bc7084a9a7c5c8c	no	66
Warnings:					
Information:					

29	Non Patent Literature	2014-09-22_Bagherzadeh_Decl_IPR2014-01369.pdf	9565317 7441d826caca8489a47bec3be76aa7cc703e7204	no	396
Warnings:					
Information:					
30	Non Patent Literature	2014-09-22_Exhibit-1013.pdf	1716301 f98f2639ee453b16d439416ea5935d6c108ad156	no	6
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Information:					
31	Non Patent Literature	2014-09-22_Exhibit-1014.pdf	2001462 e75d557231316ea02a8d5912e06741f6351e938e	no	5
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Information:					
32	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR2014400882.pdf	5916394 ca7955bd18406ea9f2e6a8ef2a1589895a9b43a4	no	67
Warnings:					
Information:					
33	Non Patent Literature	Exhibit_1007_Declaration_IPR201400882.pdf	23268956 d5246ffbde107498b9ef92db0dcff1b8260eb27a	no	392
Warnings:					
Information:					
34	Non Patent Literature	preliminary_response_00882.pdf	2565336 09849b7c0ebed5bc8e16e07aa3c7f6bcc8622d43	no	60
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Information:					
35	Non Patent Literature	institution_decision_00882.pdf	1039322 bb3172e918ca8d935eb711d76a14c9d1e8926b30	no	34
Warnings:					
Information:					
36	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR2014400883.pdf	6432014 d0e71763e1fea5859087c84c1ee77fcc75618896	no	68
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Information:					
37	Non Patent Literature	Exhibit_1011_IPR201400883.pdf	14560728 fb06579024a277e530bb09684f84c99d8bad6f29	no	266
Warnings:					
Information:					

38	Non Patent Literature	preliminary_response_00883.pdf	2381661 e987bf2019f017ddc8eedcc402681f32012a084e	no	56
Warnings:					
Information:					
39	Non Patent Literature	institution_decision_00883.pdf	916263 f37827a35a9c0307408f73270c78a89a47547468	no	27
Warnings:					
Information:					
40	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR20 1401011.pdf	6392456 7ac563fe82a2624343712ca50ac41363d6c50fe3	no	68
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Information:					
41	Non Patent Literature	Exhibit_1007_IPR201401011.pdf	22195027 22ced863be84aa0f3b07817daab99e721096c01e	no	392
Warnings:					
Information:					
42	Non Patent Literature	preliminary_response_01011.pdf	2875716 9b7e44610d7ab045113fa3e8561b4513572d3c64	no	62
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Information:					
43	Non Patent Literature	institution_decision_01011.pdf	903751 56c0309df8f7babb1cc544ee91b4036b8b1ddb9e	no	31
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Information:					
44	Non Patent Literature	Exhibit-3001.pdf	902406 e357e8723caa0a5b86ae1bc9abc1a080ef5e7493	no	63
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45	Non Patent Literature	Exhibit-3002.pdf	2525056 7db2e7e7374fa995780d3676ac75e787c351802c	no	133
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46	Non Patent Literature	Exhibit-3003.pdf	283811 2fee627ab3350b948eff30ae20dc6c3ca5b05107	no	1
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47	Non Patent Literature	Exhibit-3004.pdf	266334 3c5bba2f090727ef8b8212b3f715b448dad3c53a	no	1
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Information:					
48	Non Patent Literature	McCluskey_1986.pdf	2063520 65a221b1bdf55ee1a8405d71c7abad8727c74168	no	9
Warnings:					
Information:					
49	Non Patent Literature	20140606_Smart_Storage_Invalidity_Contentions.pdf	13104462 83f1b654d7f616ae16cad08de6f4a383f0f23f7b	no	85
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Information:					
50	Non Patent Literature	SSS_Inv_Cont_Exh_E1-E4.pdf	19588217 36ef069bffef590c8a2c24abf3992f2abb1b5bd1	no	122
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Information:					
51	Non Patent Literature	SSS_Inv_Cont_Exh_E5-E7.pdf	14371632 9ca9401a280e47bc201747138cb24482a9f231ae	no	82
Warnings:					
Information:					
52	Non Patent Literature	Exhibit_F.pdf	2358744 9d1eef457c9c36d7ca24b6cf55b8044d6b370205	no	178
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53	Non Patent Literature	Exhibit_G.pdf	1201560 d2cc352a3768ba3172145adbea8b7b0147a8ca58	no	137
Warnings:					
Information:					
54	Non Patent Literature	Exhibit_H_Smart_Storage.pdf	452099 b3c4e028d034619877cbee4afa57879e9dbfb613	no	3
Warnings:					
Information:					
55	Non Patent Literature	20140606_DIABLO_Invalidity_Contentions.pdf	1703900 ed2e5f223734481110116 61f8139988b2fca4464	no	41
Warnings:					
Information:					

56	Non Patent Literature	Diablo_EXHIBIT_D1-D6.pdf	4503878 846616191878fef35456447c0ccb84fc865a3ddf	no	145
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57	Non Patent Literature	Exhibit_F1_F5.pdf	2996579 6dd1be41b8dd93ee6334946c9a6217b76c857dce	no	154
Warnings:					
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58	Non Patent Literature	Exhibit_G1_G6.pdf	814795 f3816f131e664f7c7386b336a28043f2ba245fa3	no	79
Warnings:					
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59	Non Patent Literature	Exhibit_H_Diablo.pdf	45048 81f1e4da57ee373a3d87d4c1e42a28642560bda9	no	3
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4218740	08-19-1980	MOTOROLA INC	
	2.	4249253	02-03-1981	Gentili et al.	
	3.	4368515	01-11-1983	Nielsen	
	4.	4392212	07-05-1983	Miyasaka et al.	
	5.	4571676	02-18-1986	Mantellina et al.	
	6.	4592011	05-27-1986	Mantellina et al.	
	7.	4633429	12-30-1986	Lewandowski et al.	
	8.	4670748	06-02-1987	Williams	
	9.	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
	10.	4866603	09-02-1989	Chiba	
	11.	4958322	09-18-1990	Kosugi et al.	
	12.	4961172	10-02-1990	Shubat et al.	
	13.	4961204	10-02-1990	Hitachi Ltd	
	14.	4980850	12-25-1990	Morgan	
	15.	5060188	10-22-1991	Zulian et al.	
	16.	5247643	09-21-1993	Shottan	
	17.	5272664	12-21-1993	Silicon Graphics Inc	
	18.	5345412	09-06-1994	Shiratsuchi	
	19.	5357478	10-18-1994	Mitsubishi Electric Corp	
	20.	5388072	02-07-1995	IBM	
	21.	5388240	02-01-1995	IBM Corporation	
	22.	5392252	02-21-1995	Visi Technology Inc	
	23.	5426753	06-20-1995	Moon	
	24.	5463590	10-31-1995	Watanabe	
	25.	5483497	01-09-1996	Mochizuki et al.	
	26.	5485589	01-16-1996	Dell Usa Lp	
	27.	5495435	02-27-1996	Sugahara	
	28.	5513135	04-30-1996	Dell et al.	
	29.	5532954	07-02-1996	Bechtolsheim et al.	
	30.	5541448	07-30-1996	Carpenter	
	31.	5572691	11-05-1996	Koudmani	
	32.	5581498	12-03-1996	Ludwig et al.	
	33.	5590071	12-31-1996	Kolor et al.	

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Sheet 2 of 13

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	34.	5602999	02-11-1997	Hyatt; Gilbert P.	
	35.	5638534	06-10-1997	Samsung Electronics Co Ltd	
	36.	5655153	08-05-1997	EMC CORP	
	37.	5699542	12-16-1997	Mehta et al.	
	38.	5702984	12-30-1997	Bertin et al.	
	39.	5703826	12-30-1997	Hush et al.	
	40.	5745914	04-28-1998	Connolly et al.	
	41.	5764590	06-09-1998	Mitsubishi Electric Corp	
	42.	5784705	07-21-1998	Leung, Wingyu	
	43.	5784705	07-21-1998	Jr Albert Pesak	
	44.	5802395	09-01-1998	Connolly et al.	
	45.	5805520	09-08-1998	Anglada et al.	
	46.	5822251	10-13-1998	Bruce et al.	
	47.	5909388	06-01-1999	Siemens Ag	
	48.	5926827	07-20-1999	Dell et al.	
	49.	5926839	07-20-1999	IBM	
	50.	5953215	09-14-1999	Karabatsos, Chris	
	51.	5953280	09-14-1999	Matsui	
	52.	5958025	09-01-1999	Nippon Electric Co	
	53.	5959930	09-28-1999	Sakurai	
	54.	5963464	10-05-1999	Dell et al.	
	55.	5966736	10-12-1999	Gittinger et al.	
	56.	5974493	10-26-1999	Mitsubishi Electric Corp	
	57.	6011710	01-04-2000	Wiggers	
	58.	6018787	01-25-2000	Ip	
	59.	6044032	03-28-2000	Li	
	60.	6070217	05-30-2000	Connolly et al.	
	61.	6070227	05-30-2000	Rokicki	
	62.	6097652	08-01-2000	Roh	
	63.	6108745	08-22-2000	Gupta et al.	
	64.	6115278	09-05-2000	Deneroff et al.	
	65.	6134638	10-17-2000	Olarig et al.	
	66.	6151271	11-21-2000	Lee	

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	67.	6154418	11-28-2000	Li	
	68.	6154419	11-28-2000	Shakkarwar	
	69.	6185654	02-06-2001	Van Doren	
	70.	6188641	02-13-2001	Uchida	
	71.	6205516	03-20-2001	Usami	
	72.	6209074	03-01-2001	Dell et al.	
	73.	6226709	05-01-2001	Goodwin et al.	
	74.	6226736	05-01-2001	Niot	
	75.	6233650	05-15-2001	Johnson et al.	
	76.	6247088	06-12-2001	Seo et al.	
	77.	6317352	11-13-2001	Halbert et al.	
	78.	6349051	02-19-2002	Micron Technology Inc	
	79.	6400637	06-18-2002	Akamatsu et al.	
	80.	6408356	06-18-2002	Dell	
	81.	6414868	07-02-2002	Wong et al.	
	82.	6415374	07-02-2002	Faue et al.	
	83.	6438062	08-20-2002	Karabatsos (Curtis)	
	84.	6446158	09-03-2002	Karabatsos	
	85.	6446184	09-03-2002	Dell et al.	
	86.	6453381	09-17-2002	Yuan et al.	
	87.	6470417	10-22-2002	Kolor et al.	
	88.	6480439	11-12-2002	Tokutome et al.	
	89.	6487102	11-26-2002	Halbert et al.	
	90.	6502161	12-31-2002	Perego et al.	
	91.	6518794	02-11-2003	Coteus et al.	
	92.	6526473	02-25-2003	Kim	
	93.	6530007	03-04-2003	Olarig et al.	
	94.	6530033	03-04-2003	Raynham et al.	
	95.	6553450	04-22-2003	Dodd et al.	
	96.	6618320	09-09-2003	Hasegawa et al.	
	97.	6621496	09-16-2003	Ryan	
	98.	6625081	09-23-2003	Roohparvar et al.	
	99.	6625687	09-23-2003	Halbert et al.	
	100.	6636935	10-21-2003	Ware et al.	
	101.	6646949	11-11-2003	Ellis et al.	

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Application Number	13/952,599
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First Named Inventor	Hyun Lee
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	102.	6658509	12-02-2003	Bonella et al.	
	103.	6674684	01-06-2004	Shen	
	104.	6681301	01-20-2004	Mehta et al.	
	105.	6683372	01-27-2004	Wong et al.	
	106.	6697888	02-24-2004	Halbert et al.	
	107.	6705877	03-16-2004	Li et al.	
	108.	6717885	04-06-2004	Lai	
	109.	6721843	04-13-2004	Lexar Media Inc	
	110.	6721860	04-13-2004	Klein	
	111.	6738880	05-18-2004	Lai et al.	
	112.	6742098	05-25-2004	Halbert et al.	
	113.	6754797	06-22-2004	Wu et al.	
	114.	6785189	08-31-2004	Jacobs et al.	
	115.	6788592	09-07-2004	Nakata et al.	
	116.	6807125	10-19-2004	Coteus et al.	
	117.	6807650	10-19-2004	Lamb et al.	
	118.	6813196	11-02-2004	Park et al.	
	119.	6832284	12-14-2004	Perego et al.	
	120.	6832303	12-14-2004	Tanaka	
	121.	6834014	12-21-2004	Yoo et al.	
	122.	6854042	02-08-2005	Karabatsos	
	123.	6880094	04-12-2005	LaBerge	
	124.	6889304	05-03-2005	Perego et al.	
	125.	6912615	06-28-2005	Nicolai	
	126.	6912628	06-28-2005	Wicki et al.	
	127.	6925028	08-02-2005	Hosokawa et al.	
	128.	6944694	09-13-2005	Pax	
	129.	6950366	09-27-2005	Lapidus et al.	
	130.	6954281	10-11-2005	Fukuda et al	
	131.	6961281	11-01-2005	Wong et al.	
	132.	6981089	12-27-2005	Dodd et al.	
	133.	6982892	01-03-2006	Lee et al.	
	134.	6982893	01-03-2006	Jakobs	
	135.	6990043	01-24-2006	Kuroda et al.	
	136.	6996686	02-07-2006	Doblar et al.	
	137.	7007130	02-28-2006	Holman	

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Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	138.	7007175	02-28-2006	Chang et al.	
	139.	7046538	05-16-2006	Kinsley et al.	
	140.	7047361	05-16-2006	Phison Electronics Corp	
	141.	7054179	05-30-2006	Cogdill et al.	
	142.	7065626	06-20-2006	Schumacher et al.	
	143.	7072231	07-04-2006	Pax	
	144.	7073041	07-04-2006	Dwyer et al.	
	145.	7078793	07-18-2006	Ruckerbauer et al.	
	146.	7093066	08-15-2006	Klein	
	147.	7120727	10-10-2006	Lee et al.	
	148.	7124260	10-17-2006	LaBerge et al.	
	149.	7127584	10-24-2006	Thompson et al.	
	150.	7130952	10-31-2006	Nanki et al.	
	151.	7133960	11-07-2006	Thompson et al.	
	152.	7133972	11-07-2006	Jeddeloh	
	153.	7142461	11-28-2006	Janzen	
	154.	7149841	12-12-2006	LaBerge	
	155.	7167967	01-23-2007	Bungo et al.	
	156.	7181591	02-20-2007	Tsai	
	157.	7200021	04-03-2007	Raghuram	
	158.	7227910	06-05-2007	Lipka	
	159.	7266639	09-04-2007	Raghuram	
	160.	7272709	09-18-2007	Zitlaw et al.	
	161.	7281079	10-09-2007	Bains et al.	
	162.	7286436	10-23-2007	Bhakta et al.	
	163.	7289386	10-30-2007	Bhakta et al.	
	164.	7346750	03-18-2008	Ishikawa	
	165.	7356639	04-08-2008	Perego et al.	
	166.	7370238	05-06-2008	Billick et al.	
	167.	7437591	10-14-2008	Wong	
	168.	7461182	12-02-2008	Fukushima et al.	
	169.	7464225	12-09-2008	Tsern	
	170.	7471538	12-30-2008	Hofstra	
	171.	7532537	05-12-2009	Solomon et al.	
	172.	7619912	11-17-2009	Bhakta et al.	

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Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

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	173.	7636274	12-22-2009	Solomon et al.	
	174.	7864627	01-04-2011	Bhakta et al.	
	175.	7865674	01-04-2011	Gower et al.	
	176.	7881150	02-01-2011	Solomon et al.	
	177.	7916574	03-29-2011	Solomon et al.	
	178.	8001434	08-16-2011	Lee et al.	
	179.	8089795	01-03-2012	Rajan	
	180.	8130560	03-06-2012	Rajan	
	181.	8189328	05-29-2012	Kanapathippillai	
	182.	8233303	07-31-2012	Best	
	183.	8250295	08-21-2012	Amidi et al.	
	184.	8417870	04-09-2013	Lee et al.	
	185.	8516185	08-20-2013	Lee et al.	
	186.	8516188	08-20-2013	Solomon et al.	
	187.	8756364	06-17-2014	Bhakta et al.	
	188.	20010008006	07-12-2001	Klein	
	189.	20050257109	11-17-2005	Averbuj	
	190.	20060179206	08-10-2006	Brittain et al.	
	191.	20060233012	10-19-2006	Sekiguchi et al. (Tomonori et al.)	
	192.	20060259711	11-16-2006	Oh	
	193.	20060267172	11-30-2006	Nguyen et al.	
	194.	20060277355	12-07-2006	Ellsberry et al.	
	195.	20070058409	03-15-2007	Ruckerbauer	
	196.	20070070669	03-29-2007	Tsern	
	197.	20080025137	01-31-2008	Natarajan et al.	
	198.	20080046631	02-21-2008	Takaku et al.	
	199.	20080104352	05-01-2008	Talbot	
	200.	20080162790	07-03-2008	IM Jeon-Taek	
	201.	20090103387	04-23-2009	Shau Jen-Jye	
	202.	20100070690	03-18-2010	Amer et al.	
	203.	20100091540	04-15-2010	Bhakta et al.	
	204.	20110016250	01-20-2011	Lee et al.	
	205.	20110016269	01-20-2011	Lee et al.	
	206.	20110090749	04-21-2011	Bhakta et al.	
	207.	20110125966	05-26-2011	Amidi et al.	

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Sheet	7	of	13

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Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

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	208.	2008/0104352	05-01-2008	Talbot	
	209.	RE36229	06-15-1999	Cady	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	210.	EP1816570 A2	08-08-2007	Rambus, Inc.		
	211.	JP2000311485	10-13-2000	Fujitsu Ltd.	Translation of Abstract	
	212.	JP09237492	09-09-1997	Toshiba Corp.	Machine Translation	
	213.	JP2000285674	10-13-2000	Fujitsu Ltd.	Translation of Abstract	
	214.	JP2002184176	06-28-2002	NEC Tohoku Ltd.		
	215.	JP2003007963	01-10-2003	Hitachi, Ltd.	Machine Translation	
	216.	JP2008046989	02-28-2008	Fujitsu Ltd.	Translation of Abstract Only	
	217.	JP10-092169	10-04-1998	IBM Corp.	Translation of Abstract	
	218.	JPH10-320270	12-04-1998	Matsushita Electric Inc. Co.	Translation	
	219.	WO1992/002879	02-20-1992	Du Pont Pixel Systems Limited		
	220.	WO1994/007242	03-31-1994	Atmel Corporation		
	221.	WO1995/034030	12-14-1995	Intel Corporation		
	222.	WO1999/000734	01-07-1999	Hitachi, Ltd.		
	223.	WO2002/058069	07-25-2002	Honeywell International Inc.		
	224.	WO2002/063804	08-15-2002	Centillium Communications Inc		
	225.	WO2003/017283	02-27-2003	Micron Technology Inc		
	226.	WO2003/069484	08-21-2003	Micron Technology Inc		

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Sheet	8	of	13

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Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

	227.	WO2006/055497	05-26-2006	Intel Corporation		

US PATENT APPLICATIONS

Examiner Initials *	Cite No.[1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	228.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	229.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	230.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	231.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	232.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	233.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	234.	International Search Report and Written Opinion, PCT/US2010/040826, September 27, 2010	
	235.	Written Opinion of the International Preliminary Examining Authority, PCT/US2010/040826, October 24, 2011	
	236.	International Preliminary Report on Patentability, PCT/US2010/040826, November 28, 2011	
	237.	International Search Report and Written Opinion, PCT/US2011/059209, January 30, 2013	
	238.	Notice of Allowance issued on February 12, 2013, for U.S. Patent Application No. 12/504,131 filed July 16, 2009, 52 pages.	
	239.	Non-Final Office Action mailed September 13, 2012, for U.S. Patent Application No. 12/761,179 filed April 15, 2010, 20 pages.	
	240.	Response to Non-Final Office Action mailed September 13, 2012, for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages.	
	241.	Notice of Allowance issued on July 11, 2013, for U.S. Patent Application No. 12/761,179 filed April 15, 2010, 37 pages.	
	242.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	243.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	244.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
	245.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
	246.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/952,599
				Filing Date	July 27, 2013
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	SUN, Michael
Sheet	9	of	13	Attorney Docket Number	NT003US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	247.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	248.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	249.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
	250.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
	251.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	252.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
	253.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	254.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	255.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.	
	256.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.	
	257.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	258.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	259.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Corrected Petition for Inter Partes Review ofU.S. Patent No. 7,881,150, filed on July 8, 2014.	
	260.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter PartesReview, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.	
	261.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	262.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	

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				Examiner Name	SUN, Michael
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	263.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	264.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	265.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	266.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	267.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	268.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	269.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	270.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	271.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	272.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	273.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	274.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	275.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/952,599
				Filing Date	July 27, 2013
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	SUN, Michael
Sheet	11	of	13	Attorney Docket Number	NT003US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	276.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	277.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibit H to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	278.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
	279.	Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages	
	280.	Huang et al, "An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers," VLSI Design 2011, p. 379	
	281.	Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.	
	282.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7, October, 2001	
	283.	JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family, June 1997	
	284.	JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25, May 2003	
	285.	JEDEC Standard, "Fully Buffered DIMM (FBDIMM): DFx Design for Validation and Test," JESD82-28, February 2008	
	286.	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
	287.	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
	288.	Non-final office action, U.S. Patent Application No. 13/411,344, July 7, 2014, 19 pages	
	289.	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
	290.	Non-final office action, U.S. Patent Application No. 13/288,850, October 11, 2013, 24 pages	
	291.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	
	292.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
	293.	Response to non-final office action dated October 11, 2013 for U.S. Patent Application No. 13/288,850, filed January 13, 2014, 15 pages	
	294.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
	295.	Notice of Allowance, U.S. Pat. App. 12/504,131, February 12, 2013, 52 pages	
	296.	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042, filed November 1, 2011, 42 pages	
	297.	Response to Non-Final Office Action dated January 2, 2014, filed April 2, 2004, for U.S. Pat. App. No. 13/287,042, filed November 1, 2011, 12 pages	

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				Filing Date	July 27, 2013
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	SUN, Michael
Sheet	12	of	13	Attorney Docket Number	NT003US

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	298.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	
	299.	Miles J. Murdocca et al., "Principles of Computer Architecture" , Prentice Hall, 2000, pp. 249-251	
	300.	Intel® 6400/6402 Advanced Memory Buffer Datasheet, published October 2006.	
	301.	Micron "Synchronous DRAM Module MT18LSDT472," 1998, Micron Technology, Inc., 17 pages.	
	302.	PC133 SDRAM Registered DIMM Design Specification, Revision 1.1, Aug. 1999, 62 pages.	
	303.	Micron DDR SDRAM DIMM Module 256MB, 512 MB, 03/2002, 26 pages	
	304.	Reese, "Introduction to Logic Synthesis using Verilog HDL," Morgan&Claypool Publishers, 2006, pp. 1-28	
	305.	64 & 72 Pin Zip/Simm Sram Module, JEDEC, Standard No. 21-C, www.jedec.com/download/search/4.sub.--04.sub.--01.pdf, Jun. 1997 pp. 4.4.1-1	
	306.	Distributed Memory Mapping, IP.com, IPCOM000014788D, 2000	
	307.	Intel Corporation, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, Feb. 1999.	
	308.	Intel Corporation, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, Oct. 1998.	
	309.	JEDEC "JEDEC Standard: Double Data Rate (DDR) SDRAM Specification", JESD79C Mar. 2003.	
	310.	JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, Feb. 2002.	
	311.	Jedec Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002	
	312.	Jedec Standard, "Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL.sub.--2 Registered Buffer for Stacked DDR DIMM Applications," JESD82-4B, May 2003.	
	313.	Jin et al. "Embedded Memory in System-On-Chip Design: Architecture and Prototype Implementation," CCECE, 2003, pp. 141-146.	
	314.	Jin et al. "Prototype Implementation and Evaluation of a Multibank Embedded Memory Archtecture in Programmable Logic," IEEE, 2003, pp. 13-16.	
	315.	Lee et al. "A banked-promotion translation lookaside buffer system," Journal of Systems Architecture, vol. 47, 2002, pp. 1065-1078.	
	316.	Lee et al. "An on-chip cache compression technique to reduce decompression overhead and design complexity." Journal of Systems Architecture, vol. 46, 2000, pp. 1365-1382.	
	317.	Micron "DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB," 2002 Micron Technology, Inc. 20 pages.	
	318.	Sunaga et al. "Continuous RAS Access Method in Multiple-bank DRAM Chip," IP.com, IPCOM000123375D, 1998	
	319.	Takai et al. "250 Mbyte/s Synchronous DRAM Using a 3-Stage- Pipelined Architecture," IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, p. 426-431, dated April 1994.	

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	320.	Toal et al. "A 32-Bit SoPC Implementation of a P5." Proceedings of the Eighth IEEE International Symposium on Computers and Communications, 2003, pp. 1530-1346	
	321.	Tudruj, Marek. "Dynamically reconfigurable heterogenous multi-processor systems with transputer-controlled communication," Journal of Systems Architecture, vol. 43, 1997, pp. 27-32	
	322.	JEDEC Standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published Jan. 2004 (Feb. 2004)	
	323.	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification JEDEC, Standard No. 21-C, Revision 1.3, Jan. 2002, pages 4.20.4-1	

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Electronic Patent Application Fee Transmittal

Application Number:	13952599
Filing Date:	27-Jul-2013
Title of Invention:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NT003US

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	2806	1	90	90
		Total in USD ($)		**90**

Electronic Acknowledgement Receipt

EFS ID:	21125338
Application Number:	13952599
International Application Number:	
Confirmation Number:	6784
Title of Invention:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NT003US
Receipt Date:	06-JAN-2015
Filing Date:	27-JUL-2013
Time Stamp:	03:16:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$90
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Information:					
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Information:					
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Warnings:					
Information:					
49	Transmittal Letter	2015-01-03_IDS_Cover_NT003US.pdf	61397 210a1f9ed856603f9df5a7f52d8ac5461a17270e	no	2
Warnings:					
Information:					
50	Information Disclosure Statement (IDS) Form (SB08)	2015-01-05_IDS_NT003US.pdf	413693 dd880ac17fdf20f15bebef38bf11d70c1e4adf97	no	13
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
51	Fee Worksheet (SB06)	fee-info.pdf	30597 c3f2d7b9bc0d0ba8212d7833e9ec834ab5476548	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	116469647

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	13/952,599
Filed	:	July 27, 2013
For	:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	6784
Docket No.	:	NT003US

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 323 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

The Commissioner is authorized to charge any required fees to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: January 5, 2015

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1071

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 04/22/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 04/22/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/952,599	07/27/2013	Hyun Lee	NT003US	6784

TITLE OF INVENTION: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/22/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1072

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 04/22/2015
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/952,599	07/27/2013	Hyun Lee	NT003US	6784

TITLE OF INVENTION: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1073

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/952,599	07/27/2013	Hyun Lee	NT003US	6784

79141 7590 04/22/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
SUN, MICHAEL	
ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 04/22/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Ex. 1010, p. 1074

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/952,599	Applicant(s) LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's response filed 12/31/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/06/2015
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1076

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Amendment filed 12/31/2014.

Claims 1-20 are pending for this examination.

Claims 1, 2, 4-6, 8, 12-14, and 18-20 were amended.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/06/2015 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Informal Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Claim 8 of the application has been amended as follows:

In claim 8, line 7, "delayin at least one signal" has been amended to --delaying at least one signal--.

Allowable Subject Matter

Claims 1-20 are allowed.

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims. Applicant argues these limitations on Pages 7-11 of Applicant's Remarks filed 12/31/2014. These limitations find support in Applicant's Specification on Pages 6-29. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Sun whose telephone number is 571-270-1724. The examiner can normally be reached on Mondays to Thursdays from 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai, can be reached at (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 13/952,599	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,214,616	07-2012	Ware et al.	711/167
*	B	US-8,949,519	02-2015	Rajan et al.	711/105
*	C	US-2002/0039323	04-2002	Tokutome et al.	365/233
*	D	US-2008/0037412	02-2008	Geile et al.	370/208
*	E	US-7,884,619	02-2011	Chong et al.	324/601
*	F	US-2012/0256639	10-2012	Pausini et al.	324/613
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1080

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13952599	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

CPC- SEARCHED		
Symbol	Date	Examiner
limited search of G06F 1/12	4/13/2015	MS
limited search of G06F 13/1689	4/13/2015	MS
limited search of G06F 12/0246	4/13/2015	MS
limited search of G06F 13/1694	4/13/2015	MS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Updated EAST Search - see attached	4/13/2015	MS
Inventor Search - see attached EAST Search	4/09/2015	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	4/09/2015	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	4/09/2015	MS
Google Scholar Search - search terms used: (buffered memory module); (memory module with buffers that time signal transmissions respective to each individual buffer)	4/15/2015	MS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
710	limited search of subclasses 5, 6, and 7	4/13/2015	MS
711	limited search of subclasses 1, 2, 3, 4, 154, and 155	4/13/2015	MS
G06F	limited search 1/12, 13/1689, 12/0246, and 13/1694	4/13/2015	MS

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 6784

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/952,599	07/27/2013	710	2184	NT003US

APPLICANTS
Netlist, Inc., Irvine, CA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS
Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************
This appln claims benefit of 61/676,883 07/27/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
08/12/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MICHAEL SUN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	26	20	3

ADDRESS

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306
UNITED STATES

TITLE

MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

FILING FEE RECEIVED		
800	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S23	2944	(710/5).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S24	762	(710/6).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S25	438	(710/7).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S26	822	(711/1).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S27	514	(711/2).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S28	1033	(711/3).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S29	1182	(711/4).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S30	8473	(711/154).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S31	582	(711/155).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/04/09 15:10
S32	1223	(S23 or S24 or S25 or S26 or S27 or S28 or S29 or S30 or S31) and memory module and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S33	887	S32 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S34	832	S33 and read and write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S35	652	S34 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S36	375	S35 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S37	18	S36 and (align$4 with read data)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10

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S38	3505	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S39	90	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:10
S40	4051	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:39
S41	835	S40 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:39
S42	22	S41 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:39
S43	2	S42 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/09 15:39
S44	4235	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:46
S45	1691	S44 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:46
S46	193	S45 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:46
S47	59	S46 AND ((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:47
S48	59	S47 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:48
S49	59	S48 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:48

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S50	59	S49 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:48
S51	31	S50 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:48
S52	3	S51 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:48
S53	462563	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:53
S54	45977	S53 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:54
S55	99	S53 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:54
S56	33	S55 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 08:55
S57	0	(determining or calculating) with (time interval or delay) with (signal near5 memory controller) with (signal near5 memory bus)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 13:58
S58	620	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 13:59
S59	1	S58 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2015/04/13 14:00

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S60	18562	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/04/13 15:00

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S61	3795	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory).clm. and (buffer).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/04/13 15:01
S62	335	S61 and (delay or time interval).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/04/13 15:06
S63	218	S62 and (read or write).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/04/13 15:06
S64	3	S63 and (time transmitting or time transmission).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2015/04/13 15:06

4/ 15/ 2015 2:20:06 PM
C:\ Users\ msun\ Documents\ EAST\ Workspaces\ 13952599.wsp

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Ex. 1010, p. 1086

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13952599	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC						
Symbol					**Type**	**Version**
G06F		3	/	0659	F	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 (Primary Examiner)	04/15/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

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Ex. 1010, p. 1087

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13952599	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
710	5	G	0	6	F	3 / 00 (2006.01.01)					
CROSS REFERENCE(S)		G	0	6	F	12 / 00 (2006.01.01)					
		G	0	6	F	13 / 00 (2006.01.01)					

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	6	7			
711	1	2	3	4	154
711	155				

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 20	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 (Primary Examiner) (Date)	04/15/2015	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No. 20150415

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13952599	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5														
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8	8														
9	9														
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12	12														
13	13														
14	14														
15	15														
16	16														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184	04/15/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	1.	4218740	08-19-1980	MOTOROLA INC	
/M.S./	2.	4249253	02-03-1981	Gentili et al.	
/M.S./	3.	4368515	01-11-1983	Nielsen	
/M.S./	4.	4392212	07-05-1983	Miyasaka et al.	
/M.S./	5.	4571676	02-18-1986	Mantellina et al.	
/M.S./	6.	4592011	05-27-1986	Mantellina et al.	
/M.S./	7.	4633429	12-30-1986	Lewandowski et al.	
/M.S./	8.	4670748	06-02-1987	Williams	
/M.S./	9.	4706214	11-10-1987	Mitsubishi Denki Kabushiki Kaisha	
/M.S./	10.	4866603	09-02-1989	Chiba	
/M.S./	11.	4958322	09-18-1990	Kosugi et al.	
/M.S./	12.	4961172	10-02-1990	Shubat et al.	
/M.S./	13.	4961204	10-02-1990	Hitachi Ltd	
/M.S./	14.	4980850	12-25-1990	Morgan	
/M.S./	15.	5060188	10-22-1991	Zulian et al.	
/M.S./	16.	5247643	09-21-1993	Shottan	
/M.S./	17.	5272664	12-21-1993	Silicon Graphics Inc	
/M.S./	18.	5345412	09-06-1994	Shiratsuchi	
/M.S./	19.	5357478	10-18-1994	Mitsubishi Electric Corp	
/M.S./	20.	5388072	02-07-1995	IBM	
/M.S./	21.	5388240	02-01-1995	IBM Corporation	
/M.S./	22.	5392252	02-21-1995	Visi Technology Inc	
/M.S./	23.	5426753	06-20-1995	Moon	
/M.S./	24.	5463590	10-31-1995	Watanabe	
/M.S./	25.	5483497	01-09-1996	Mochizuki et al.	
/M.S./	26.	5485589	01-16-1996	Dell Usa Lp	
/M.S./	27.	5495435	02-27-1996	Sugahara	
/M.S./	28.	5513135	04-30-1996	Dell et al.	
/M.S./	29.	5532954	07-02-1996	Bechtolsheim et al.	
/M.S./	30.	5541448	07-30-1996	Carpenter	
/M.S./	31.	5572691	11-05-1996	Koudmani	
/M.S./	32.	5581498	12-03-1996	Ludwig et al.	
/M.S./	33.	5590071	12-31-1996	Kolor et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 13

Complete if Known	
Application Number	13/952,599
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Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

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/M.S./	34.	5602999	02-11-1997	Hyatt; Gilbert P.	
/M.S./	35.	5638534	06-10-1997	Samsung Electronics Co Ltd	
/M.S./	36.	5655153	08-05-1997	EMC CORP	
/M.S./	37.	5699542	12-16-1997	Mehta et al.	
/M.S./	38.	5702984	12-30-1997	Bertin et al.	
/M.S./	39.	5703826	12-30-1997	Hush et al.	
/M.S./	40.	5745914	04-28-1998	Connolly et al.	
/M.S./	41.	5764590	06-09-1998	Mitsubishi Electric Corp	
/M.S./	42.	5784705	07-21-1998	Leung, Wingyu	
/M.S./	43.	5784705	07-21-1998	Jr Albert Pesak	
/M.S./	44.	5802395	09-01-1998	Connolly et al.	
/M.S./	45.	5805520	09-08-1998	Anglada et al.	
/M.S./	46.	5822251	10-13-1998	Bruce et al.	
/M.S./	47.	5909388	06-01-1999	Siemens Ag	
/M.S./	48.	5926827	07-20-1999	Dell et al.	
/M.S./	49.	5926839	07-20-1999	IBM	
/M.S./	50.	5953215	09-14-1999	Karabatsos, Chris	
/M.S./	51.	5953280	09-14-1999	Matsui	
/M.S./	52.	5958025	09-01-1999	Nippon Electric Co	
/M.S./	53.	5959930	09-28-1999	Sakurai	
/M.S./	54.	5963464	10-05-1999	Dell et al.	
/M.S./	55.	5966736	10-12-1999	Gittinger et al.	
/M.S./	56.	5974493	10-26-1999	Mitsubishi Electric Corp	
/M.S./	57.	6011710	01-04-2000	Wiggers	
/M.S./	58.	6018787	01-25-2000	Ip	
/M.S./	59.	6044032	03-28-2000	Li	
/M.S./	60.	6070217	05-30-2000	Connolly et al.	
/M.S./	61.	6070227	05-30-2000	Rokicki	
/M.S./	62.	6097652	08-01-2000	Roh	
/M.S./	63.	6108745	08-22-2000	Gupta et al.	
/M.S./	64.	6115278	09-05-2000	Deneroff et al.	
/M.S./	65.	6134638	10-17-2000	Olarig et al.	
/M.S./	66.	6151271	11-21-2000	Lee	

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Sheet 3 of 13

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First Named Inventor	Hyun Lee
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/M.S./	67.	6154418	11-28-2000	Li	
/M.S./	68.	6154419	11-28-2000	Shakkarwar	
/M.S./	69.	6185654	02-06-2001	Van Doren	
/M.S./	70.	6188641	02-13-2001	Uchida	
/M.S./	71.	6205516	03-20-2001	Usami	
/M.S./	72.	6209074	03-01-2001	Dell et al.	
/M.S./	73.	6226709	05-01-2001	Goodwin et al.	
/M.S./	74.	6226736	05-01-2001	Niot	
/M.S./	75.	6233650	05-15-2001	Johnson et al.	
/M.S./	76.	6247088	06-12-2001	Seo et al.	
/M.S./	77.	6317352	11-13-2001	Halbert et al.	
/M.S./	78.	6349051	02-19-2002	Micron Technology Inc	
/M.S./	79.	6400637	06-18-2002	Akamatsu et al.	
/M.S./	80.	6408356	06-18-2002	Dell	
/M.S./	81.	6414868	07-02-2002	Wong et al.	
/M.S./	82.	6415374	07-02-2002	Faue et al.	
/M.S./	83.	6438062	08-20-2002	Karabatsos (Curtis)	
/M.S./	84.	6446158	09-03-2002	Karabatsos	
/M.S./	85.	6446184	09-03-2002	Dell et al.	
/M.S./	86.	6453381	09-17-2002	Yuan et al.	
/M.S./	87.	6470417	10-22-2002	Kolor et al.	
/M.S./	88.	6480439	11-12-2002	Tokutome et al.	
/M.S./	89.	6487102	11-26-2002	Halbert et al.	
/M.S./	90.	6502161	12-31-2002	Perego et al.	
/M.S./	91.	6518794	02-11-2003	Coteus et al.	
/M.S./	92.	6526473	02-25-2003	Kim	
/M.S./	93.	6530007	03-04-2003	Olarig et al.	
/M.S./	94.	6530033	03-04-2003	Raynham et al.	
/M.S./	95.	6553450	04-22-2003	Dodd et al.	
/M.S./	96.	6618320	09-09-2003	Hasegawa et al.	
/M.S./	97.	6621496	09-16-2003	Ryan	
/M.S./	98.	6625081	09-23-2003	Roohparvar et al.	
/M.S./	99.	6625687	09-23-2003	Halbert et al.	
/M.S./	100.	6636935	10-21-2003	Ware et al.	
/M.S./	101.	6646949	11-11-2003	Ellis et al.	

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Sheet 4 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	102.	6658509	12-02-2003	Bonella et al.	
/M.S./	103.	6674684	01-06-2004	Shen	
/M.S./	104.	6681301	01-20-2004	Mehta et al.	
/M.S./	105.	6683372	01-27-2004	Wong et al.	
/M.S./	106.	6697888	02-24-2004	Halbert et al.	
/M.S./	107.	6705877	03-16-2004	Li et al.	
/M.S./	108.	6717885	04-06-2004	Lai	
/M.S./	109.	6721843	04-13-2004	Lexar Media Inc	
/M.S./	110.	6721860	04-13-2004	Klein	
/M.S./	111.	6738880	05-18-2004	Lai et al.	
/M.S./	112.	6742098	05-25-2004	Halbert et al.	
/M.S./	113.	6754797	06-22-2004	Wu et al.	
/M.S./	114.	6785189	08-31-2004	Jacobs et al.	
/M.S./	115.	6788592	09-07-2004	Nakata et al.	
/M.S./	116.	6807125	10-19-2004	Coteus et al.	
/M.S./	117.	6807650	10-19-2004	Lamb et al.	
/M.S./	118.	6813196	11-02-2004	Park et al.	
/M.S./	119.	6832284	12-14-2004	Perego et al.	
/M.S./	120.	6832303	12-14-2004	Tanaka	
/M.S./	121.	6834014	12-21-2004	Yoo et al.	
/M.S./	122.	6854042	02-08-2005	Karabatsos	
/M.S./	123.	6880094	04-12-2005	LaBerge	
/M.S./	124.	6889304	05-03-2005	Perego et al.	
/M.S./	125.	6912615	06-28-2005	Nicolai	
/M.S./	126.	6912628	06-28-2005	Wicki et al.	
/M.S./	127.	6925028	08-02-2005	Hosokawa et al.	
/M.S./	128.	6944694	09-13-2005	Pax	
/M.S./	129.	6950366	09-27-2005	Lapidus et al.	
/M.S./	130.	6954281	10-11-2005	Fukuda et al	
/M.S./	131.	6961281	11-01-2005	Wong et al.	
/M.S./	132.	6981089	12-27-2005	Dodd et al.	
/M.S./	133.	6982892	01-03-2006	Lee et al.	
/M.S./	134.	6982893	01-03-2006	Jakobs	
/M.S./	135.	6990043	01-24-2006	Kuroda et al.	
/M.S./	136.	6996686	02-07-2006	Doblar et al.	
/M.S./	137.	7007130	02-28-2006	Holman	

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Sheet 5 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	138.	7007175	02-28-2006	Chang et al.	
/M.S./	139.	7046538	05-16-2006	Kinsley et al.	
/M.S./	140.	7047361	05-16-2006	Phison Electronics Corp	
/M.S./	141.	7054179	05-30-2006	Cogdill et al.	
/M.S./	142.	7065626	06-20-2006	Schumacher et al.	
/M.S./	143.	7072231	07-04-2006	Pax	
/M.S./	144.	7073041	07-04-2006	Dwyer et al.	
/M.S./	145.	7078793	07-18-2006	Ruckerbauer et al.	
/M.S./	146.	7093066	08-15-2006	Klein	
/M.S./	147.	7120727	10-10-2006	Lee et al.	
/M.S./	148.	7124260	10-17-2006	LaBerge et al.	
/M.S./	149.	7127584	10-24-2006	Thompson et al.	
/M.S./	150.	7130952	10-31-2006	Nanki et al.	
/M.S./	151.	7133960	11-07-2006	Thompson et al.	
/M.S./	152.	7133972	11-07-2006	Jeddeloh	
/M.S./	153.	7142461	11-28-2006	Janzen	
/M.S./	154.	7149841	12-12-2006	LaBerge	
/M.S./	155.	7167967	01-23-2007	Bungo et al.	
/M.S./	156.	7181591	02-20-2007	Tsai	
/M.S./	157.	7200021	04-03-2007	Raghuram	
/M.S./	158.	7227910	06-05-2007	Lipka	
/M.S./	159.	7266639	09-04-2007	Raghuram	
/M.S./	160.	7272709	09-18-2007	Zitlaw et al.	
/M.S./	161.	7281079	10-09-2007	Bains et al.	
/M.S./	162.	7286436	10-23-2007	Bhakta et al.	
/M.S./	163.	7289386	10-30-2007	Bhakta et al.	
/M.S./	164.	7346750	03-18-2008	Ishikawa	
/M.S./	165.	7356639	04-08-2008	Perego et al.	
/M.S./	166.	7370238	05-06-2008	Billick et al.	
/M.S./	167.	7437591	10-14-2008	Wong	
/M.S./	168.	7461182	12-02-2008	Fukushima et al.	
/M.S./	169.	7464225	12-09-2008	Tsern	
/M.S./	170.	7471538	12-30-2008	Hofstra	
/M.S./	171.	7532537	05-12-2009	Solomon et al.	
/M.S./	172.	7619912	11-17-2009	Bhakta et al.	

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Sheet 6 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	173.	7636274	12-22-2009	Solomon et al.	
/M.S./	174.	7864627	01-04-2011	Bhakta et al.	
/M.S./	175.	7865674	01-04-2011	Gower et al.	
/M.S./	176.	7881150	02-01-2011	Solomon et al.	
/M.S./	177.	7916574	03-29-2011	Solomon et al.	
/M.S./	178.	8001434	08-16-2011	Lee et al.	
/M.S./	179.	8089795	01-03-2012	Rajan	
/M.S./	180.	8130560	03-06-2012	Rajan	
/M.S./	181.	8189328	05-29-2012	Kanapathippillai	
/M.S./	182.	8233303	07-31-2012	Best	
/M.S./	183.	8250295	08-21-2012	Amidi et al.	
/M.S./	184.	8417870	04-09-2013	Lee et al.	
/M.S./	185.	8516185	08-20-2013	Lee et al.	
/M.S./	186.	8516188	08-20-2013	Solomon et al.	
/M.S./	187.	8756364	06-17-2014	Bhakta et al.	
/M.S./	188.	20010008006	07-12-2001	Klein	
/M.S./	189.	20050257109	11-17-2005	Averbuj	
/M.S./	190.	20060179206	08-10-2006	Brittain et al.	
/M.S./	191.	20060233012	10-19-2006	Sekiguchi et al. (Tomonori et al.)	
/M.S./	192.	20060259711	11-16-2006	Oh	
/M.S./	193.	20060267172	11-30-2006	Nguyen et al.	
/M.S./	194.	20060277355	12-07-2006	Ellsberry et al.	
/M.S./	195.	20070058409	03-15-2007	Ruckerbauer	
/M.S./	196.	20070070669	03-29-2007	Tsern	
/M.S./	197.	20080025137	01-31-2008	Natarajan et al.	
/M.S./	198.	20080046631	02-21-2008	Takaku et al.	
/M.S./	199.	20080104352	05-01-2008	Talbot	
/M.S./	200.	20080162790	07-03-2008	IM Jeon-Taek	
/M.S./	201.	20090103387	04-23-2009	Shau Jen-Jye	
/M.S./	202.	20100070690	03-18-2010	Amer et al.	
/M.S./	203.	20100091540	04-15-2010	Bhakta et al.	
/M.S./	204.	20110016250	01-20-2011	Lee et al.	
/M.S./	205.	20110016269	01-20-2011	Lee et al.	
/M.S./	206.	20110090749	04-21-2011	Bhakta et al.	
/M.S./	207.	20110125966	05-26-2011	Amidi et al.	

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Sheet 7 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

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/M.S./	208.	2008/0104352	05-01-2008	Talbot	
/M.S./	209.	RE36229	06-15-1999	Cady	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]
/M.S./	210.	EP1816570 A2	08-08-2007	Rambus, Inc.		
/M.S./	211.	JP2000311485	10-13-2000	Fujitsu Ltd.	Translation of Abstract	
/M.S./	212.	JP09237492	09-09-1997	Toshiba Corp.	Machine Translation	
/M.S./	213.	JP2000285674	10-13-2000	Fujitsu Ltd.	Translation of Abstract	
/M.S./	214.	JP2002184176	06-28-2002	NEC Tohoku Ltd.		
/M.S./	215.	JP2003007963	01-10-2003	Hitachi, Ltd.	Machine Translation	
/M.S./	216.	JP2008046989	02-28-2008	Fujitsu Ltd.	Translation of Abstract Only	
/M.S./	217.	JP10-092169	10-04-1998	IBM Corp.	Translation of Abstract	
/M.S./	218.	JPH10-320270	12-04-1998	Matsushita Electric Inc. Co.	Translation	
/M.S./	219.	WO1992/002879	02-20-1992	Du Pont Pixel Systems Limited		
/M.S./	220.	WO1994/007242	03-31-1994	Atmel Corporation		
/M.S./	221.	WO1995/034030	12-14-1995	Intel Corporation		
/M.S./	222.	WO1999/000734	01-07-1999	Hitachi, Ltd.		
/M.S./	223.	WO2002/058069	07-25-2002	Honeywell International Inc.		
/M.S./	224.	WO2002/063804	08-15-2002	Centillium Communications Inc		
/M.S./	225.	WO2003/017283	02-27-2003	Micron Technology Inc		
/M.S./	226.	WO2003/069484	08-21-2003	Micron Technology Inc		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 8 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

/M.S./	227.	WO2006/055497	05-26-2006	Intel Corporation		

US PATENT APPLICATIONS

Examiner Initials *	Cite No.[1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	228.	13/411,344	3/2/2012	Lee	Entire Prosecution History
/M.S./	229.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
/M.S./	230.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
/M.S./	231.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
/M.S./	232.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
/M.S./	233.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/M.S./	234.	International Search Report and Written Opinion, PCT/US2010/040826, September 27, 2010	
/M.S./	235.	Written Opinion of the International Preliminary Examining Authority, PCT/US2010/040826, October 24, 2011	
/M.S./	236.	International Preliminary Report on Patentability, PCT/US2010/040826, November 28, 2011	
/M.S./	237.	International Search Report and Written Opinion, PCT/US2011/059209, January 30, 2013	
/M.S./	238.	Notice of Allowance issued on February 12, 2013, for U.S. Patent Application No. 12/504,131 filed July 16, 2009, 52 pages.	
/M.S./	239.	Non-Final Office Action mailed September 13, 2012, for U.S. Patent Application No. 12/761,179 filed April 15, 2010, 20 pages.	
/M.S./	240.	Response to Non-Final Office Action mailed September 13, 2012, for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages.	
/M.S./	241.	Notice of Allowance issued on July 11, 2013, for U.S. Patent Application No. 12/761,179 filed April 15, 2010, 37 pages.	
/M.S./	242.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
/M.S./	243.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
/M.S./	244.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
/M.S./	245.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
/M.S./	246.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/952,599
				Filing Date	July 27, 2013
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	SUN, Michael
Sheet	9	of	13	Attorney Docket Number	NT003US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/M.S./	247.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
/M.S./	248.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
/M.S./	249.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
/M.S./	250.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
/M.S./	251.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
/M.S./	252.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
/M.S./	253.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
/M.S./	254.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
/M.S./	255.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.	
/M.S./	256.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.	
/M.S./	257.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
/M.S./	258.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
/M.S./	259.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Corrected Petition for Inter Partes Review ofU.S. Patent No. 7,881,150, filed on July 8, 2014.	
/M.S./	260.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter PartesReview, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.	
/M.S./	261.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
/M.S./	262.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	

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(Use as many sheets as necessary)

Sheet 10 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/M.S./	263.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
/M.S./	264.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
/M.S./	265.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
/M.S./	266.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
/M.S./	267.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
/M.S./	268.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
/M.S./	269.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	270.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	271.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	272.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	273.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
/M.S./	274.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	275.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Sheet 11 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

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/M.S./	277.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibit H to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
/M.S./	278.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
/M.S./	279.	Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages	
/M.S./	280.	Huang et al, "An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers," VLSI Design 2011, p. 379	
/M.S./	281.	Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.	
/M.S./	282.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7, October, 2001	
/M.S./	283.	JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family, June 1997	
/M.S./	284.	JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25, May 2003	
/M.S./	285.	JEDEC Standard, "Fully Buffered DIMM (FBDIMM): DFx Design for Validation and Test," JESD82-28, February 2008	
/M.S./	286.	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
/M.S./	287.	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
/M.S./	288.	Non-final office action, U.S. Patent Application No. 13/411,344, July 7, 2014, 19 pages	
/M.S./	289.	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
/M.S./	290.	Non-final office action, U.S. Patent Application No. 13/288,850, October 11, 2013, 24 pages	
/M.S./	291.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	
/M.S./	292.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
/M.S./	293.	Response to non-final office action dated October 11, 2013 for U.S. Patent Application No. 13/288,850, filed January 13, 2014, 15 pages	
/M.S./	294.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
/M.S./	295.	Notice of Allowance, U.S. Pat. App. 12/504,131, February 12, 2013, 52 pages	
/M.S./	296.	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042, filed November 1, 2011, 42 pages	
/M.S./	297.	Response to Non-Final Office Action dated January 2, 2014, filed April 2, 2004, for U.S. Pat. App. No. 13/287,042, filed November 1, 2011, 12 pages	

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Sheet 12 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

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/M.S./	298.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	
/M.S./	299.	Miles J. Murdocca et al., "Principles of Computer Architecture" , Prentice Hall, 2000, pp. 249-251	
/M.S./	300.	Intel® 6400/6402 Advanced Memory Buffer Datasheet, published October 2006.	
/M.S./	301.	Micron "Synchronous DRAM Module MT18LSDT472," 1998, Micron Technology, Inc., 17 pages.	
/M.S./	302.	PC133 SDRAM Registered DIMM Design Specification, Revision 1.1, Aug. 1999, 62 pages.	
/M.S./	303.	Micron DDR SDRAM DIMM Module 256MB, 512 MB, 03/2002, 26 pages	
/M.S./	304.	Reese, "Introduction to Logic Synthesis using Verilog HDL," Morgan&Claypool Publishers, 2006, pp. 1-28	
/M.S./	305.	64 & 72 Pin Zip/Simm Sram Module, JEDEC, Standard No. 21-C, www.jedec.com/download/search/4.sub.--04.sub.--01.pdf, Jun. 1997 pp. 4.4.1-1	
/M.S./	306.	Distributed Memory Mapping, IP.com, IPCOM000014788D, 2000	
/M.S./	307.	Intel Corporation, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, Feb. 1999.	
/M.S./	308.	Intel Corporation, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, Oct. 1998.	
/M.S./	309.	JEDEC "JEDEC Standard: Double Data Rate (DDR) SDRAM Specification", JESD79C Mar. 2003.	
/M.S./	310.	JEDEC Standard No. 21-C, 4.20-2-168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, Feb. 2002.	
/M.S./	311.	Jedec Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002	
/M.S./	312.	Jedec Standard, "Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL.sub.--2 Registered Buffer for Stacked DDR DIMM Applications," JESD82-4B, May 2003.	
/M.S./	313.	Jin et al. "Embedded Memory in System-On-Chip Design: Architecture and Prototype Implementation," CCECE, 2003, pp. 141-146.	
/M.S./	314.	Jin et al. "Prototype Implementation and Evaluation of a Multibank Embedded Memory Archtecture in Programmable Logic," IEEE, 2003, pp. 13-16.	
/M.S./	315.	Lee et al. "A banked-promotion translation lookaside buffer system," Journal of Systems Architecture, vol. 47, 2002, pp. 1065-1078.	
/M.S./	316.	Lee et al. "An on-chip cache compression technique to reduce decompression overhead and design complexity." Journal of Systems Architecture, vol. 46, 2000, pp. 1365-1382.	
/M.S./	317.	Micron "DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB," 2002 Micron Technology, Inc. 20 pages.	
/M.S./	318.	Sunaga et al. "Continuous RAS Access Method in Multiple-bank DRAM Chip," IP.com, IPCOM000123375D, 1998	
/M.S./	319.	Takai et al. "250 Mbyte/s Synchronous DRAM Using a 3-Stage- Pipelined Architecture," IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, p. 426-431, dated April 1994.	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/952,599
				Filing Date	July 27, 2013
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	SUN, Michael
Sheet	13	of	13	Attorney Docket Number	NT003US

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/M.S./	320.	Toal et al. "A 32-Bit SoPC Implementation of a P5." Proceedings of the Eighth IEEE International Symposium on Computers and Communications, 2003, pp. 1530-1346	
/M.S./	321.	Tudruj, Marek. "Dynamically reconfigurable heterogenous multi-processor systems with transputer-controlled communication," Journal of Systems Architecture, vol. 43, 1997, pp. 27-32	
/M.S./	322.	JEDEC Standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published Jan. 2004 (Feb. 2004)	
/M.S./	323.	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification JEDEC, Standard No. 21-C, Revision 1.3, Jan. 2002, pages 4.20.4-1	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13952599	07/27/2013	Hyun Lee	NT003US	6784

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS

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1 JAMIE J. ZHENG, Ph.D, Esq.
2
3

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(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Netlist, Inc.	Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ■ Corporation or other private group entity ☐ Government

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☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/952,599
Filed	:	July 27, 2013
For	:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	6784
Docket No.	:	NT003US

CERTIFICATE OF EFS WEB TRANSMISSION

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July 22, 2015

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby submits the following amendment under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 7 of this paper.

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AMENDMENTS TO THE CLAIMS

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1. (Currently Amended) A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to ~~each of~~ the memory command signals;

memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and

a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and

wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and

wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

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2. (Previously Presented) The memory module of claim 1, wherein each module control signal arrives at the plurality of buffer circuits at different points in time across more than one clock cycle of the system clock, and wherein the each respective buffer circuit is configured to align the respective set of read data signals such that different sets of read data signals corresponding to the memory read operation are transmitted by the different buffer circuits onto different sets of data/strobe signal lines in the memory bus within one system clock cycle.

3. (Original) The memory module of claim 1, wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal, and wherein each buffer circuit further includes at least one signal adjustment circuit to adjust one or more the module control signals to mitigate any metastability condition in the module control signals.

4. (Previously Presented) The memory module of claim 1, wherein the module control device further receives the system clock from the system memory controller and transmits a registered clock signal to the plurality of buffer circuits, and wherein the each respective buffer circuit regenerates one or more clock signals from the registered clock signal and provides a regenerated clock signal to the respective group of memory devices.

5. (Previously Presented) The memory module of claim 1, wherein the respective buffer circuit comprises:

a time interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first signal and the second signal;

a delay circuit to delay the respective set of read data signals received from the respective group of memory devices according to the delay signal.

6. (Previously Presented) A method of operating a memory module in a memory system having a memory controller, the memory module being coupled to the memory controller via a memory bus, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module including memory devices and a module controller coupled to the memory controller via the set of control/address signal lines, the method comprising:

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receiving a read command from the memory controller via the set of control/address signal lines;

generating module command signals and module control signals in response to the read command;

producing read data from the memory devices in response to the module command signals;

controlling a plurality of sets data paths in a plurality of data buffers using the module control signals such that each respective set of the plurality of sets of data paths receive and conduct a respective portion of the read data; and

outputting read data from the plurality of data paths onto the memory bus, wherein a first set of the plurality of data paths output a first portion of the read data onto a first set of data/strobe signal lines in accordance with a first time interval, wherein a second set of the plurality of data paths output a second portion of the read data onto a second set of data/strobe signal lines in accordance with a second time interval different from the first time interval, the first time interval and the second time interval having been determined during a prior write operation performed in the memory system.

7. (Original) The method of claim 6, further comprising:

determining a metastability condition associated with a respective module control signal at each of the plurality of data buffers; and

adjusting the respective module control signal based on the metastability condition.

8. (Currently Amended) The method of claim 6, further comprising, in the each data buffer:

receiving at least one first module control signal generated in the memory module in response to a write command associated with the prior write operation;

determining a time interval between receiving the at least one first module control signal and receiving a write signal associated with the write command from the memory controller, the write signal being one of a write data signal and a write strobe signal; and

delaying ~~delayin~~ at least one signal in the respective data buffer according to the time interval.

9. (Original) The method of claim 8 wherein the at least one signal is a clock signal.

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10. (Original) The method of claim 8 wherein the at least one signal is at least one of a read data signal and a read strobe signal.

11. (Original) The method of claim 8, wherein the write signal is a write strobe signal, the method further comprising:

detecting a preamble of the write strobe signal to determine the time interval.

12. (Previously Presented) A buffer circuit for use in a memory module coupled to a memory controller via a memory bus, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module including a plurality of memory devices organized in groups and a module controller coupled to the memory controller via the set of control/address signal lines, comprising:

a time interval determination circuit to determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory bus; and

a delay circuit to time transmission of data/strobe signals received from a respective group of the plurality of memory devices to the memory controller via a respective set of the plurality of sets of data/strobe signal lines according to the time interval.

13. (Previously Presented) The buffer circuit of claim 12 wherein the buffer further comprises receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal.

14. (Previously Presented) The buffer circuit of claim 12 wherein the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more the module control signals to mitigate metastability condition in the module control signals.

15. (Original) The buffer circuit of claim 12, wherein the first signal is an enable signal to enable a write data path in the buffer circuit.

16. (Original) The buffer circuit of claim 15, wherein the second signal is a write strobe signal.

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17. (Original) The buffer circuit of claim 15, wherein the second signal has a preamble, and wherein the time interval determination circuit includes a preamble detector to detect the preamble of the second signal.

18. (Previously Presented) The buffer circuit of claim 15, wherein the time interval determination circuit further includes a counter to count a number of clock cycles between receipt of the first signal and detection of the preamble of the second signal.

19. (Previously Presented) The buffer circuit of claim 12, further comprising:

a clock regeneration circuit to receive a clock signal from the module controller and to regenerate a regenerated clock signal according to the time interval.

20. (Previously Presented) The buffer circuit of claim 12, wherein the buffer circuit is coupled to a respective group of the plurality of memory devices on the memory module, and wherein the buffer circuit further comprises a clock regeneration circuit to receive a clock signal from the module controller and to provide a regenerated clock signal to the respective group of the plurality of memory devices.

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REMARKS

This amendment responds to the Notice of Allowance dated April 22, 2015.

Claims 1 and 8 are amended to correct minor errors. No new matter is added.

The Examiner is invited to call the undersigned at (650) 273-6008 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: July 22, 2015

By: /Jamie J. Zheng/
Jamie J. Zheng
Registration No. 51,167
Customer No. 79,141

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1111

Electronic Patent Application Fee Transmittal

Application Number:	13952599
Filing Date:	27-Jul-2013
Title of Invention:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NT003US

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt

EFS ID:	22996471
Application Number:	13952599
International Application Number:	
Confirmation Number:	6784
Title of Invention:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NT003US
Receipt Date:	22-JUL-2015
Filing Date:	27-JUL-2013
Time Stamp:	19:21:30
Application Type:	Utility under 35 USC 111(a)

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1	Issue Fee Payment (PTO-85B)	2015-07-21_Issue_Fee_Transmittal_NT003US.pdf	74192 5f154fc83f125e814f54ad70b92cc383cb893b58	no	2
Warnings:					
Information:					
2	Amendment after Notice of Allowance (Rule 312)	2015-07-22_312_Amendment_NT003US.pdf	92184 d2a85858c67aca145fc548383b99c00d51d32f1c	no	7
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30353 b4aaef5fb686f3438573cf7017f7ecfe00846087	no	2
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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NT003US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/952,599
Filed	:	July 27, 2013
For	:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	6784
Docket No.	:	NT003US

CERTIFICATE OF EFS WEB TRANSMISSION

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July 22, 2015

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby submits the following amendment under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 7 of this paper.

OK TO ENTER: /M.S./ 08/06/2015

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Ex. 1010, p. 1116

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/952,599	07/27/2013	Hyun Lee	NT003US	6784

79141 7590 08/11/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
08/11/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com
eofficeaction@appcoll.com

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1117

Response to Rule 312 Communication	Application No.	Applicant(s)
	13/952,599	LEE ET AL.
	Examiner	Art Unit
	MICHAEL SUN	2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *22 July 2015* under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Samsung Electronics Co., Ltd.
Ex. 1010, p. 1118

PTO/SB/08a/b(07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	4	of	13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	102.	6658509	12-02-2003	Bonella et al.	
/M.S./	103.	6674684	01-06-2004	Shen	
/M.S./	104.	6681301	01-20-2004	Mehta et al.	
/M.S./	105.	6683372	01-27-2004	Wong et al.	
/M.S./	106.	6697888	02-24-2004	Halbert et al.	
/M.S./	107.	6705877	03-16-2004	Li et al.	
/M.S./	108.	6717885	04-06-2004	Lai	
/M.S./	109.	6721843	04-13-2004	~~Lexar Media Inc.~~	Estakhri
/M.S./	110.	6721860	04-13-2004	Klein	
/M.S./	111.	6738880	05-18-2004	Lai et al.	
/M.S./	112.	6742098	05-25-2004	Halbert et al.	
/M.S./	113.	6754797	06-22-2004	Wu et al.	
/M.S./	114.	6785189	08-31-2004	Jacobs et al.	
/M.S./	115.	6788592	09-07-2004	Nakata et al.	
/M.S./	116.	6807125	10-19-2004	Coteus et al.	
/M.S./	117.	6807650	10-19-2004	Lamb et al.	
/M.S./	118.	6813196	11-02-2004	Park et al.	
/M.S./	119.	6832284	12-14-2004	Perego et al.	
/M.S./	120.	6832303	12-14-2004	Tanaka	
/M.S./	121.	6834014	12-21-2004	Yoo et al.	
/M.S./	122.	6854042	02-08-2005	Karabatsos	
/M.S./	123.	6880094	04-12-2005	LaBerge	
/M.S./	124.	6889304	05-03-2005	Perego et al.	
/M.S./	125.	6912615	06-28-2005	Nicolai	
/M.S./	126.	6912628	06-28-2005	Wicki et al.	
/M.S./	127.	6925028	08-02-2005	Hosokawa et al.	
/M.S./	128.	6944694	09-13-2005	Pax	
/M.S./	129.	6950366	09-27-2005	Lapidus et al.	
/M.S./	130.	6954281	10-11-2005	Fukuda et al	
/M.S./	131.	6961281	11-01-2005	Wong et al.	
/M.S./	132.	6981089	12-27-2005	Dodd et al.	
/M.S./	133.	6982892	01-03-2006	Lee et al.	
/M.S./	134.	6982893	01-03-2006	Jakobs	
/M.S./	135.	6990043	01-24-2006	Kuroda et al.	
/M.S./	136.	6996686	02-07-2006	Doblar et al.	
/M.S./	137.	7007130	02-28-2006	Holman	

Change(s) applied to document, /K.S.S./ 5/13/2015

EXAMINER	/Michael Sun/	DATE CONSIDERED	04/15/2015

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	67.	6154418	11-28-2000	Li	
/M.S./	68.	6154419	11-28-2000	Shakkarwar	
/M.S./	69.	6185654	02-06-2001	Van Doren	
/M.S./	70.	6188641	02-13-2001	Uchida	
/M.S./	71.	6205516	03-20-2001	Usami	
/M.S./	72.	6209074	03-01-2001	Dell et al.	
/M.S./	73.	6226709	05-01-2001	Goodwin et al.	
/M.S./	74.	6226736	05-01-2001	Niot	
/M.S./	75.	6233650	05-15-2001	Johnson et al.	
/M.S./	76.	6247088	06-12-2001	Seo et al.	
/M.S./	77.	6317352	11-13-2001	Halbert et al.	
Change(s) applied to document, /K.S.S./ 5/13/2015 /M.S./	78.	6349051	02-19-2002	~~Micron Technology Inc~~ Klein	
/M.S./	79.	6400637	06-18-2002	Akamatsu et al.	
/M.S./	80.	6408356	06-18-2002	Dell	
/M.S./	81.	6414868	07-02-2002	Wong et al.	
/M.S./	82.	6415374	07-02-2002	Faue et al.	
/M.S./	83.	6438062	08-20-2002	Karabatsos (Curtis)	
/M.S./	84.	6446158	09-03-2002	Karabatsos	
/M.S./	85.	6446184	09-03-2002	Dell et al.	
/M.S./	86.	6453381	09-17-2002	Yuan et al.	
/M.S./	87.	6470417	10-22-2002	Kolor et al.	
/M.S./	88.	6480439	11-12-2002	Tokutome et al.	
/M.S./	89.	6487102	11-26-2002	Halbert et al.	
/M.S./	90.	6502161	12-31-2002	Perego et al.	
/M.S./	91.	6518794	02-11-2003	Coteus et al.	
/M.S./	92.	6526473	02-25-2003	Kim	
/M.S./	93.	6530007	03-04-2003	Olarig et al.	
/M.S./	94.	6530033	03-04-2003	Raynham et al.	
/M.S./	95.	6553450	04-22-2003	Dodd et al.	
/M.S./	96.	6618320	09-09-2003	Hasegawa et al.	
/M.S./	97.	6621496	09-16-2003	Ryan	
/M.S./	98.	6625081	09-23-2003	Roohparvar et al.	
/M.S./	99.	6625687	09-23-2003	Halbert et al.	
/M.S./	100.	6636935	10-21-2003	Ware et al.	
/M.S./	101.	6646949	11-11-2003	Ellis et al.	

EXAMINER /Michael Sun/ **DATE CONSIDERED** 04/15/2015

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

Change(s) applied to document, /K.S.S./ 5/13/2015

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	34.	5602999	02-11-1997	Hyatt; Gilbert P.	
/M.S./	35.	5638534	06-10-1997	~~Samsung Electronics Co Ltd~~	Mote, Jr.
/M.S./	36.	5655153	08-05-1997	~~EMC CORP~~	Sandorfi
/M.S./	37.	5699542	12-16-1997	Mehta et al.	
/M.S./	38.	5702984	12-30-1997	Bertin et al.	
/M.S./	39.	5703826	12-30-1997	Hush et al.	
/M.S./	40.	5745914	04-28-1998	Connolly et al.	
/M.S./	41.	5764590	06-09-1998	~~Mitsubishi Electric Corp~~	Iwamoto , et al.
/M.S./	42.	5784705	07-21-1998	Leung, Wingyu	
/M.S./	43.	5784705	07-21-1998	~~Jr Albert Pesak~~	Leung
/M.S./	44.	5802395	09-01-1998	Connolly et al.	
/M.S./	45.	5805520	09-08-1998	Anglada et al.	
/M.S./	46.	5822251	10-13-1998	Bruce et al.	
/M.S./	47.	5909388	06-01-1999	~~Siemens Ag~~	Mueller
/M.S./	48.	5926827	07-20-1999	Dell et al.	
/M.S./	49.	5926839	07-20-1999	~~IBM~~	Katayama
/M.S./	50.	5953215	09-14-1999	Karabatsos, Chris	
/M.S./	51.	5953280	09-14-1999	Matsui	
/M.S./	52.	5958025	09-01-1999	~~Nippon Electric Co~~	Sonobe
/M.S./	53.	5959930	09-28-1999	Sakurai	
/M.S./	54.	5963464	10-05-1999	Dell et al.	
/M.S./	55.	5966736	10-12-1999	Gittinger et al.	
/M.S./	56.	5974493	10-26-1999	~~Mitsubishi Electric Corp~~	Okumura , et al.
/M.S./	57.	6011710	01-04-2000	Wiggers	
/M.S./	58.	6018787	01-25-2000	Ip	
/M.S./	59.	6044032	03-28-2000	Li	
/M.S./	60.	6070217	05-30-2000	Connolly et al.	
/M.S./	61.	6070227	05-30-2000	Rokicki	
/M.S./	62.	6097652	08-01-2000	Roh	
/M.S./	63.	6108745	08-22-2000	Gupta et al.	
/M.S./	64.	6115278	09-05-2000	Deneroff et al.	
/M.S./	65.	6134638	10-17-2000	Olarig et al.	
/M.S./	66.	6151271	11-21-2000	Lee	

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Sheet 1 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

Change(s) applied to document, /K.S.S./ 5/13/2015

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	1.	4218740	08-19-1980	~~MOTOROLA INC~~	Bennett, et al.
/M.S./	2.	4249253	02-03-1981	Gentili et al.	
/M.S./	3.	4368515	01-11-1983	Nielsen	
/M.S./	4.	4392212	07-05-1983	Miyasaka et al.	
/M.S./	5.	4571676	02-18-1986	Mantellina et al.	
/M.S./	6.	4592011	05-27-1986	Mantellina et al.	
/M.S./	7.	4633429	12-30-1986	Lewandowski et al.	
/M.S./	8.	4670748	06-02-1987	Williams	
/M.S./	9.	4706214	11-10-1987	~~Mitsubishi Denki Kabushiki Kaisha~~	Kassai
/M.S./	10.	4866603	09-02-1989	Chiba	
/M.S./	11.	4958322	09-18-1990	Kosugi et al.	
/M.S./	12.	4961172	10-02-1990	Shubat et al.	
/M.S./	13.	4961204	10-02-1990	~~Hitachi Ltd~~	Tanaka, et al.
/M.S./	14.	4980850	12-25-1990	Morgan	
/M.S./	15.	5060188	10-22-1991	Zulian et al.	
/M.S./	16.	5247643	09-21-1993	Shottan	
/M.S./	17.	5272664	12-21-1993	~~Silicon Graphics Inc~~	Alexander, et al.
/M.S./	18.	5345412	09-06-1994	Shiratsuchi	
/M.S./	19.	5357478	10-18-1994	~~Mitsubishi Electric Corp~~	Kikuda, et al.
/M.S./	20.	5388072	02-07-1995	~~IBM~~	Matick, et al.
/M.S./	21.	5388240	02-01-1995	~~IBM Corporation~~	Olderdissen, et al.
/M.S./	22.	5392252	02-21-1995	~~Visi Technology Inc~~	Rimpo, et al.
/M.S./	23.	5426753	06-20-1995	Moon	
/M.S./	24.	5463590	10-31-1995	Watanabe	
/M.S./	25.	5483497	01-09-1996	Mochizuki et al.	
/M.S./	26.	5485589	01-16-1996	~~Dell Usa Lp~~	Kocis, et al.
/M.S./	27.	5495435	02-27-1996	Sugahara	
/M.S./	28.	5513135	04-30-1996	Dell et al.	
/M.S./	29.	5532954	07-02-1996	Bechtolsheim et al.	
/M.S./	30.	5541448	07-30-1996	Carpenter	
/M.S./	31.	5572691	11-05-1996	Koudmani	
/M.S./	32.	5581498	12-03-1996	Ludwig et al.	
/M.S./	33.	5590071	12-31-1996	Kolor et al.	

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Sheet 5 of 13

Complete if Known	
Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

Change(s) applied to document, /K.S.S./ 5/14/2015

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/M.S./	138.	7007175	02-28-2006	Chang et al.	
/M.S./	139.	7046538	05-16-2006	Kinsley et al.	
/M.S./	140.	7047361	05-16-2006	~~Phison Electronics Corp.~~ Chong, et al.	
/M.S./	141.	7054179	05-30-2006	Cogdill et al.	
/M.S./	142.	7065626	06-20-2006	Schumacher et al.	
/M.S./	143.	7072231	07-04-2006	Pax	
/M.S./	144.	7073041	07-04-2006	Dwyer et al.	
/M.S./	145.	7078793	07-18-2006	Ruckerbauer et al.	
/M.S./	146.	7093066	08-15-2006	Klein	
/M.S./	147.	7120727	10-10-2006	Lee et al.	
/M.S./	148.	7124260	10-17-2006	LaBerge et al.	
/M.S./	149.	7127584	10-24-2006	Thompson et al.	
/M.S./	150.	7130952	10-31-2006	Nanki et al.	
/M.S./	151.	7133960	11-07-2006	Thompson et al.	
/M.S./	152.	7133972	11-07-2006	Jeddeloh	
/M.S./	153.	7142461	11-28-2006	Janzen	
/M.S./	154.	7149841	12-12-2006	LaBerge	
/M.S./	155.	7167967	01-23-2007	Bungo et al.	
/M.S./	156.	7181591	02-20-2007	Tsai	
/M.S./	157.	7200021	04-03-2007	Raghuram	
/M.S./	158.	7227910	06-05-2007	Lipka	
/M.S./	159.	7266639	09-04-2007	Raghuram	
/M.S./	160.	7272709	09-18-2007	Zitlaw et al.	
/M.S./	161.	7281079	10-09-2007	Bains et al.	
/M.S./	162.	7286436	10-23-2007	Bhakta et al.	
/M.S./	163.	7289386	10-30-2007	Bhakta et al.	
/M.S./	164.	7346750	03-18-2008	Ishikawa	
/M.S./	165.	7356639	04-08-2008	Perego et al.	
/M.S./	166.	7370238	05-06-2008	Billick et al.	
/M.S./	167.	7437591	10-14-2008	Wong	
/M.S./	168.	7461182	12-02-2008	Fukushima et al.	
/M.S./	169.	7464225	12-09-2008	Tsern	
/M.S./	170.	7471538	12-30-2008	Hofstra	
/M.S./	171.	7532537	05-12-2009	Solomon et al.	
/M.S./	172.	7619912	11-17-2009	Bhakta et al.	

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Sheet 6 of 13

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Application Number	13/952,599
Filing Date	July 27, 2013
First Named Inventor	Hyun Lee
Art Unit	2184
Examiner Name	SUN, Michael
Attorney Docket Number	NT003US

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/M.S./	173.	7636274	12-22-2009	Solomon et al.	
/M.S./	174.	7864627	01-04-2011	Bhakta et al.	
/M.S./	175.	7865674	01-04-2011	Gower et al.	
/M.S./	176.	7881150	02-01-2011	Solomon et al.	
/M.S./	177.	7916574	03-29-2011	Solomon et al.	
/M.S./	178.	8001434	08-16-2011	Lee et al.	
/M.S./	179.	8089795	01-03-2012	Rajan	
/M.S./	180.	8130560	03-06-2012	Rajan	
/M.S./	181.	8189328	05-29-2012	Kanapathippillai	
/M.S./	182.	8233303	07-31-2012	Best	
/M.S./	183.	8250295	08-21-2012	Amidi et al.	
/M.S./	184.	8417870	04-09-2013	Lee et al.	
/M.S./	185.	8516185	08-20-2013	Lee et al.	
/M.S./	186.	8516188	08-20-2013	Solomon et al.	
/M.S./	187.	8756364	06-17-2014	Bhakta et al.	
/M.S./	188.	20010008006	07-12-2001	Klein	
/M.S./	189.	20050257109	11-17-2005	Averbuj	
/M.S./	190.	20060179206	08-10-2006	Brittain et al.	
/M.S./	191.	20060233012	10-19-2006	Sekiguchi et al. (Tomonori et al.)	
/M.S./	192.	20060259711	11-16-2006	Oh	
/M.S./	193.	20060267172	11-30-2006	Nguyen et al.	
/M.S./	194.	20060277355	12-07-2006	Ellsberry et al.	
/M.S./	195.	20070058409	03-15-2007	Ruckerbauer	
/M.S./	196.	20070070669	03-29-2007	Tsern	
/M.S./	197.	20080025137	01-31-2008	~~Nataraja~~n et al.	Rajan
/M.S./	198.	20080046631	02-21-2008	Takaku et al.	
/M.S./	199.	20080104352	05-01-2008	Talbot	
/M.S./	200.	20080162790	07-03-2008	IM Jeon-Taek	
/M.S./	201.	20090103387	04-23-2009	Shau Jen-Jye	
/M.S./	202.	20100070690	03-18-2010	Amer et al.	
/M.S./	203.	20100091540	04-15-2010	Bhakta et al.	
/M.S./	204.	20110016250	01-20-2011	Lee et al.	
/M.S./	205.	20110016269	01-20-2011	Lee et al.	
/M.S./	206.	20110090749	04-21-2011	Bhakta et al.	
/M.S./	207.	20110125966	05-26-2011	Amidi et al.	

Change(s) applied to document, /J.M./ 5/20/2015

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/952,599	09/08/2015	9128632	NT003US	6784

79141 7590 08/19/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

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APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
13/952,599	07/27/2013	Hyun Lee	129980-5046US	67122

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/06/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jamie J. Zheng/
Name:	Jamie J. Zheng
Registration Number:	51167