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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | NT003C1 |
|---|---|---|
| | Application Number | |
| Title of Invention | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION | |

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## Application Information:

| **Title of the Invention** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION | | |
|---|---|---|---|
| **Attorney Docket Number** | NT003C1 | **Small Entity Status Claimed** ☒ | |
| **Application Type** | Nonprovisional | | |
| **Subject Matter** | Utility | | |
| **Suggested Class (if any)** | | **Sub Class (if any)** | |
| **Suggested Technology Center (if any)** | | | |
| **Total Number of Drawing Sheets (if any)** | 26 | **Suggested Figure for Publication (if any)** | 2A |

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| Prior Application Status | Pending | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) |
| | Continuation of | 13952599 | 2013-07-27 |

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| 13952599 | non provisional of | 61676883 | 2012-07-27 |
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| **Signature** | /Jamie J. Zheng/ | | | Date (YYYY-MM-DD) | 2015-09-07 |
|---|---|---|---|---|---|
| First Name | Jamie | Last Name | Zheng | Registration Number | 51167 |

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# MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

## CLAIM OF PRIORITY

[0001] The present application is a continuation of U.S. Pat. App. No. 13/952,599, filed July 27, 2013, to be issued as U.S. Pat. No. 9,128,632, which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on July 27, 2012. Each of the above applications is incorporated by reference herein in its entirety.

## CROSS REFERENCE TO RELATED APPLICATIONS

[0002] The present application is related to commonly-owned U.S. Pat. App. No. 14/715,486, filed on May 18, 2015; U.S. Pat. App. No. 13/970,606, filed on August 20, 2013; U.S. Pat. App. No. 12/504,131, filed on July 16, 2009, now U.S. Pat. No. 8,417,870; U.S. Pat. App. No. 12/761,179, filed on April 15, 2010, now U.S. Pat. No. 8,516,185; U.S. Pat. App. No. 13/287,042, filed on November 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. Pat. App. No. 13/287,081, filed on November 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

## FIELD

[0003] The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

## BACKGROUND

[0004] With recent advancement of information technology and widespread use of the Internet to store and process information, more and more demands are placed on the acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical



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information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

[0005] The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

[0006] The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

[0007] In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

[0008] For memory devices in such as a memory module to be properly accessed, distribution of control signals and a control clock signal in the memory module is subject to strict constraints. In some conventional memory modules, control wires are routed so there



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is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

[0009] In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram illustrating a memory system including at least one memory module according to one embodiment.

[0011] FIGS. 2A-2D are each a diagrams illustrating interactions among components in a a memory module according to certain embodiments.

[0012] FIG. 3 is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

[0013] FIGS. 4A-4B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

[0014] FIGS. 5A-5B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

[0015] FIG. 6 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.



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[0016] FIG. 7 is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

[0017] FIG. 8 is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

[0018] FIG. 9 is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

[0019] FIGS. 10A-10C are diagrams illustrating a metastability detection circuit according to certain embodiments.

[0020] FIGS. 10D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

[0021] FIGS. 11A-11B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

[0022] FIGS. 12A-12B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

[0023] FIG. 13 is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

[0024] FIG. 14 is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

[0025] FIG. 15 a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

[0026] FIG. 16 a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

[0027] FIG. 17 is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.



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[0028] FIG. 18 is a flowchart illustrating a method for data edge alignment according to embodiments.

[0029] FIG. 19 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

## DESCRIPTION OF EMBODIMENTS

[0030] A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

[0031] The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a



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respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

[0032] In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

[0033] Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

[0034] FIG. 1 shows a system 100 including a memory controller (MCH) 101 and one or more memory modules 110 coupled to the MCH by a memory bus 105, according to one embodiment. As shown, the memory bus includes C/A signal lines 120 and groups of system data/strobe signal lines 130. Also as shown, each memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114. Each memory module 110 further includes a module control circuit (module controller or module control device) 116 coupled to the MCH 101 via the C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to the MCH 101 via respective groups of system data/strobe signal lines 130. In one embodiment, the memory devices 112, the module



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control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119.

[0035] In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module 110 may vary. For example, as shown, each memory module 110 may include four ranks of memory devices 112. In another embodiment, the memory module 110 may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices 112.

[0036] In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices 112. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

[0037] Furthermore, the memory devices 112 may include any type of memory devices. For example, in one embodiment, the memory devices 112 may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module 110 may include a dual in-line memory module (DIMM).

[0038] Referring to FIG. 2A, which illustrates one memory module 110 according to an embodiment, the module control device 116 receives system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal lines 120 and generates module command signals and module control signals based on memory commands from the system. The module control device 116 also received a system clock MCK and generates a module clock signal CK in response to the system



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clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{MCK}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{CK}$.

[0039] Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

[0040] Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

[0041] Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory



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controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices 118 via respective module control signal lines 230. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices 118 via the module control signal lines and decoded/processed at the isolation devices.

[0042] Module control device 116 transmits the module command signals to the memory devices 112 via module C/A signal lines 220. The memory devices 112 operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices 118 via module control signal lines 230. As shown in FIG. 2, at least some of the memory devices in a same rank share a same set of module C/A signal lines 220, and at least some of the isolation devices 118 share a same set of module control signal lines 230.

[0043] As shown n FIGS. 2A and 2B, each rank 114 includes *N* memory devices, where *N* is an integer larger than one. For example, a first rank includes memory devices $M_{11}$, …, $M_{i1}$, $M_{i+1,1}$, …, $M_N$, a second rank includes memory devices $M_{12}$, …, $M_{i2}$, $M_{i+1,2}$, …, $M_{N,2}$, and so on. In one embodiment, the memory devices 112 are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines 130 and including at least one memory device from each rank. For example, memory devices $M_{11}$, $M_{12}$, $M_{13}$, and $M_{14}$ form a first group of memory devices, memory devices $M_{i1}$, $M_{i2}$, $M_{i3}$, and $M_{i4}$ form an $i^{th}$ group of memory devices, and so on.

[0044] As shown, the isolation devices 118 are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines 130 and the respective groups of memory devices. For example, isolation device ID-1 among the isolation devices 118 is associated with the first group of memory devices $M_{11}$, $M_{12}$, $M_{13}$, and $M_{14}$ and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices, isolation devices ID-*i* among the isolation



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devices 118 is associated with the $i^{th}$ group of memory devices $M_{i1}$, $M_{i2}$, $M_{i3}$, and $M_{i4}$ and is coupled between the group of system data/strobe signal lines 130-i and the $i^{th}$ *group* of memory devices, and so on.

[0045] In one embodiment, each group or sets of memory devices are coupled to the associated isolation device 118 via a set of module data/strobe lines 210. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device 118 via a same set of module data/strobe lines 210 (as shown in FIG. 2A) or via respective subsets of module data/strobe lines 210 (as shown in FIG. 2B). For example, as shown in FIG. 2B, in the first group of memory devices, memory devices $M_{11}$ and/or $M_{13}$ form a first subgroup, and memory devices $M_{12}$ and/or $M_{14}$ form a second subgroup; in the $i^{th}$ group of memory devices, memory devices $M_{i1}$ and/or $M_{i3}$ form a first subgroup, and memory devices $M_{i2}$ and/or $M_{i4}$ form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device 118 via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices $M_{11}$ and/or $M_{13}$ form the first subgroup are/is coupled to the isolation device ID-1 via the corresponding first subset of module data/strobe lines YA-1, and memory devices $M_{12}$ and/or $M_{14}$ form the second subgroup are/is coupled to the isolation device ID-1 via the corresponding second subset of module data/strobe lines YA-2.

[0046] In one embodiment, the isolation devices 118 are in the data paths between the MCH 101 and the memory module 110 and include data buffers between the MCH 101 and the respective groups of memory devices. In one embodiment, each isolation device 118 is configured to select a subgroup in the respective group of memory devices to communicate data with the MCH 101 in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH 101. Further, each isolation devices 118 is configured to isolate unselected subgroup(s) of memory devices



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from the MCH 101 during write operations, so that the MCH sees a load on each data line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

[0047] In one embodiment, the isolation devices 118 are distributed across the memory module 110 or the module board 119 in positions corresponding to the respective groups of memory devices. For example, isolation device ID-1 is disposed in a first position corresponding to the first group of memory devices $M_{11}$, $M_{12}$, $M_{13}$, and $M_{14}$, and isolation device ID-*i* is disposed in an $i^{th}$ position separate from the first position and corresponding to the $i^{th}$ group of memory devices $M_{i1}$, $M_{i2}$, $M_{i3}$, and $M_{i4}$. In one embodiment, the first position is between the first group of memory devices and an edge 201 of the module board 119 where connections (not shown) to the data/strobe signal lines 130 are placed, and $i^{th}$ position is between the $i^{th}$ group of memory devices and the edge 201 of the module board 119. In one embodiment, the isolation devices 118 are distributed along the edge 201 of the memory module 110. In one embodiment, each isolation device 118 is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines 210, the module C/A signal lines 220, and the module control signal lines 230 include signal traces formed on and/or in the module board 119.

[0048] As an option, memory module 110 may further include a serial-presence detect (SPD) device 240, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module 110. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory module 110, a memory density per rank, a number of memory device on the memory module 110, and a memory density per memory device, etc. A basic input/output system (BIOS) of system 100 can be informed of these attributes of the memory module 110 by reading from the SPD 240 and can use such data to configure the MCH 101 properly for maximum reliability and performance.



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[0049] In certain embodiments, the SPD 240 and/or the control circuit 116 store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit 116, input and output signals electrical and logical level control information for the control circuit 116, etc. In certain embodiments, the SPD 240 contains a system view of the module 110 which can be different from an actual physical construction of the module 110. For example, the SPD 240 stores at least one memory operation parameter that is different from a correspondng memory operation parameter in a system memory controller setting. The SPD 240 may also store at least on data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

[0050] Thus, in certain embodiment, in the memory module 110, C/A signals representing a memory command are received and buffered by the module control circuit 116, so that the MCH sees only the module control circuit 116 as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130. Thus, MCH 101 does not directly operate or control the memory devices 112. As far as data/strobe signals are concerned, the MCH 101 mainly sees the isolation devices 118, and the system 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101.

[0051] In certain embodiments, the memory module 110 is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM). In certain embodiments, the control circuit 116 includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.



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[0052] As shown in FIG. 2C, in certain embodiments, the control circuit 116 transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices 118, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

[0053] For example, load reduction mechanism in the isolation devices 118 would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller 101. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller 101 over the interface between the memory devices 112 and the associated isolation devices 118. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller 101, which may cause silent system failure.

[0054] Moreover, clock skew amongst the memory devices 112 and the associated isolation devices 118 due to the distributed architecture of the memory module 110 can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

[0055] To address at least some of the above issues, in certain embodiments, as shown in FIG. 2D, the control circuit 116 transmits registered C/A signals to the memory devices 112, and transmits the module control signals and the module clock signal to the data buffers 118, in a fly-by arrangement. The memory devices 112 do not receive the module clock signal from the control circuit 116. Instead, each data buffer 118 regenerates the clock that is used by the respective set of memory devices 112. Each Data buffer 118 is



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thus responsible for providing a correct data timing interface between the respective set of memory devices 112 and the system memory controller 101. Each data buffer 118 is also responsible for providing the correct control signal timing between the control circuit 116 and the respective set of memory devices 112.

[0056] Thus, the memory module 110 in FIG. 2D allows a locally synchronized operation for each respective set of memory devices 112, which can correspond to a nibble or a byte of a DDR data bus between the memory module 110 and the system memory controller 101. Also, signal interface between each data buffer 118 and the respective set of memory devices 112 can be synchronized. In one embodiment, each data buffer 118 has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices 112, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller 101, programmable phase adjustment related to at least one control signal that is coupled to the control circuit 116. The locally synchronized operation also makes it easier for each data buffer 118 to perform self-testing of the associated set of memory devices 112, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Patent 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

[0057] In certain embodiments, operations of the isolation devices 118 are controlled by the module control signals from the module control circuit 116, which generates the module control signals according to the C/A signals received from the MCH. Thus, the module control signals need to be properly received by the isolation devices 118 to insure their proper operation. In one embodiment, the module control signals are transmitted together with the module clock signal CK, which is also generated by the module control circuit 116 based on the system clock signal MCK. The isolation circuits 118 buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices 118 are distributed across the memory module, the module control signal lines 230 can stretch across the memory module 110, over a distance of



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several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits 118 includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

[0058] Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-($n$-1) in the exemplary configuration shown in FIG. 2. In other words, a same set of module control signals may reach different isolation devices 118 at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

[0059] With the isolation devices 118 receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to time the transmission of read data signals to the MCH 101 from the isolation devices 118. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a



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subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100, as explained in more detail below.

[0060] More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0061] In one embodiment, as shown in FIG. 3, each group of signal lines 130 include a set of *n* data (DQ) signal lines 322 each for transmitting one of a set of data signals $DQ_0$, $DQ_1$, …, $DQ_{n-1}$, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of *n* module data signal lines $Y_0$, $Y_1$, …, $Y_{n-1}$ and at least one module strobe signal line $Y_{DQS}$. When the subsets of memory devices are coupled to the associated isolation device 118 via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. 2B. Each subset of module data/strobe lines YA include a set of *n* first module data lines $YA_0$, $YA_1$, …, $YA_n$ and at least one first module strobe signal line $YA_{DQS}$; and each subset of module data/strobe lines YB include a set of *n* second module data lines $YB_0$, $YB_1$, …, $YB_n$ and at least one second module strobe signal line $YB_{DQS}$.

[0062] Each isolation device 118 includes a set of DQ routing circuits 320 coupled on one side to respective ones of the set of *n* DQ signal lines 322, and on another side to respective ones of the respective set of *n* module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines $YA_0$, $YA_1$, …, $YA_n$ and the second module data lines $YB_0$, $YB_1$, …, $YB_n$. Each isolation device 118 further includes an ID control circuit 310 coupled on one side to the at least one DQS signal line 324, on another side to the one or more module strobe signal lines $Y_{DQS}$, or the first module strobe



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signal line $YA_{DQS}$ and second module strobe signal line $YB_{DQS}$. The ID control circuit 310 also receives the module clock signal CK and the module control signals via the module control signal lines 230, and outputs ID control signals 330 to the DQ routing circuits 320, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module control signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK0. Each DQ routing circuit 320 is configured to enable data communication between the respective DQ signal line 322 with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

[0063] In certain embodiments, the ID control circuit 310 also provides a delay signal DS, which is used by the DQ routing circuits 320 to align read data output by the isolation device 118 with read data output by the other isolation devices 118, as explained in further detail below. In certain embodiments, the ID control circuit 310 regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK0 and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

[0064] The memory devices 112 are coupled to the isolation devices 118 via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. 4A, memory devices $M_{11}$, $M_{12}$, $M_{13}$, and $M_{14}$ in the first group of memory devices can be coupled to the isolation device ID-1 via a same set of module data lines $Y\text{-}1_0$, $Y\text{-}1_1$, …, $Y\text{-}1_{n-1}$ and module strobe line $Y\text{-}1_{DQS}$. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which can be different with respect to different subgroups of memory devices.

[0065] Alternatively, as shown in FIG. 4B, memory devices $M_{11}$ and $M_{13}$, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines $YA\text{-}1_0$, $YA\text{-}1_1$, …, $YA\text{-}1_n$ and module strobe line $YA\text{-}1_{DQS}$ and



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memory devices $M_{12}$ and $M_{14}$, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines $YB\text{-}1_0$, $YB\text{-}1_1$, …, $YB\text{-}1_n$ and module strobe line $YB\text{-}1_{DQS}$. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board 119. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards 119, or stacked over each other, and/or over the associated isolation device.

[0066] Multiple memory devices having a data width that is less than a data width of the isolation devices 118 may be used in place of one of the memory devices 112, which has the same data width as that of the isolation devices. For example, as shown in FIG. 5A, two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ may be used in place of the memory device $M_{11}$. Each of the two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ has a data width of 4, and together they act like a memory device $M_{11}$ of a data width of 8. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_0$, …, $YA\text{-}1_3$ and module strobe line $YA\text{-}1_{DQS\text{-}1}$ while memory circuit $M_{11\text{-}2}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_4$, …, $YA\text{-}1_7$ and module strobe line $YA\text{-}1_{DQS\text{-}2}$.

[0067] In another embodiment, as shown in FIG. 5B, four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ may be used as the memory device $M_{11}$. Each of the four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ has a data width of 4, and together they act like a memory device $M_{11}$ of a data width of 16. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_0$, …, $YA\text{-}1_3$ and module strobe line $YA\text{-}1_{DQS\text{-}1}$ while memory device $M_{11\text{-}2}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_4$, …, $YA\text{-}1_7$ and module strobe line $YA\text{-}1_{DQS\text{-}2}$, and so on.

[0068] FIG. 6 illustrates the ID control circuit 310 in an isolation device 118. As shown, the ID control circuit 310 includes a clock buffer 610 to receive the module clock signal CK from the module control device 116, and to output a module clock signal CK0. The ID control circuit 310 further includes a strobe routing circuit 620 that are coupled on one side to the corresponding system DQS signal line 324 and on another side to the corresponding



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module DQS signal lines $YA_{DQS}$ and $YB_{DQS}$. The ID control circuit 310 further includes a receiver circuit 630 with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit 310 further includes a command processing circuit 640 that provides the received, decoded, and/or otherwise processed module control signals 330 to the DQ routing circuits 320 and the strobe routing circuit 620 either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits 320 and the strobe routing circuit 620 to selectively enabling data communication between the MCH 101 and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

[0069] The strobe routing circuit 620 also buffers strobe signals received from either the MCH 101 or the memory devices 112, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits 320. In one embodiment, the ID control circuit 310 further includes a delay control circuit 650 that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit 320 and the strobe routing circuit 620. The delay amount is provided to the DQ routing circuit 320 and the strobe routing circuit in a delay signal DS.

[0070] In a receiver circuit 630, the respective MCS is received in accordance with the module clock signal CK0. In one embodiment, receiver circuit 630 samples the respective MCS using rising (or falling) edges of the module clock CK0. Since the isolation devices 118 are distributed across the memory module 110 at positions corresponding to the respective groups of memory devices, the module control signal lines 230 that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as shown in FIG. 7. As the MCS and CK0 travel along their respective module control signal lines 710 and 720, they can become misaligned with each other when they reach the input pins 730 of an isolation device 118.

[0071] For example, a module control signal, like the MCS 810 shown in FIG. 8, can be



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perfectly aligned with the module clock signal CK, with a rising edge 801 of the module clock signal CK being at a center of a data eye 802, when the MCS signal and the clock signal leave the module control circuit 116. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS 820 with respect to the CK signal, i.e., the rising edge 801 of the clock signal is near a left edge of a data eye of the MCS 820, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS 830, can be shifted with respect to the module clock signal such that a rising edge 801 of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS 840, can be so shifted with respect to the module clock signal such that a rising edge 801 of the clock signal falls in the glitches 803 at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

[0072] In one embodiment, as shown in FIG. 9, a receiver circuit 630 includes a metastability detection circuit (MDC) 910 to determine a metastability condition in a corresponding module control signal MCS0. In one embodiment, the MDC 910 generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS0. The MDC 910 also generates one or more metastability indicators and outputs the one or more metastability indicators via lines 912 and/or 914.

[0073] The receiver circuit 630 further includes a signal selection circuit 920 that receives the module clock CK and the at least one delayed version of the module clock via signal lines 916. The signal selection circuit 920 also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines 918. The signal selection circuit 920 selects a clock signal $CK_i$ from among the module clock CK and the at least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit 920 may also select an MCS signal $MCS_i$ from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.



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[0074] The receiver circuit 630 further includes a sampler or register circuit 930 that samples the selected module control signal $MCS_i$ according to the selected clock signal $CK_i$ and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit 640 for further processing (if needed) before being provided to the DQ routing circuits 320 and DQS routing circuit 620.

[0075] FIG. 10A illustrates an MDC 910 according to one embodiment. As shown, the MDC 910 includes a delay circuit 1012 that generates a delayed version MCS1 of the corresponding MCS0 by adding a predetermined amount of delay (e.g., 10ps) to MCS0. MDC 910 also includes a delay circuit 1016 that generates a delayed version CK1 of the clock signal CK0 by adding a predetermined amount of delay to CK0. In one embodiment, CK1 is delayed from CK0 by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC 910 further includes a sampler circuit 1042 that samples MCS1 according to CK0 and outputs a sampled result A, a sampler circuit 1044 that samples MCS0 according to CK0 and outputs a sampled result B, and a sampler circuit 1046 that samples MCS0 according to CK1 and outputs a sampled result C. The MDC 910 further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z1 and Z2 based on the sampled results A, B, and C.

[0076] In one embodiment, Z1 is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., $Z1 = \overline{A \oplus B}$, and Z2 is the result of another logic operation on the sampled results, e.g., $Z2 = \overline{B \oplus C}$. Thus, as shown in FIG. 10B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge 1061 of CK0 is close to the right side of a data eye where gliches at the edges of the data eyes can make C unpredicatable, A and B can be in agreement (i.e., Z1 is true) while B and C are likely not in agreement (i.e., Z2 is false). FIG. 10 C illustrates a metastability condition when there is insufficient set-up time. As shown in FIG. 10C and Table 1 below, a rising clock edge 1061 of CK0 is close to the left side of a data eye where gliches at the edges of the data eyes can make A unpredicatable. Thus, A and B can be in disagreement so Z1 is false while B and C can be in agreement so Z2 is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge



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1061 of CK0 and the rising clock edge 1062 of CK1 are near the middle of an MCS0 data eye so there is no metastability issues and both Z1 and Z2 are true, as shown in Table 1.

[0077] FIG. 10D illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1071 that selects between CK0 and CK1 based on the metastability indicator Z1, and a second multiplexor 1072 that selects between MCS0 and MCS1 based on the metastability indicator Z2. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, Z1=1 and Z2=0, and MCS1 is output from multiplexor 1071 while CK0 is output from multiplexor 1072. Sampler 930 thus samples MCS1 according to the rising edges of CK0. Thus, more hold time is provided to mitigate the metastability condition since MCS1 is shifted from MCS0 toward the right.

[0078] On the other hand, where a metastability condition of insufficient set-up time occurs, Z1=0 and Z2=1, and CK1 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. Sampler 930 thus samples MCS0 according to the rising edges of CK1. Since CK1 is shifted from CK0 toward the right, more set-up time is provided to mitigate the metastability condition.

[0079] In the case when no metastability is detected, Z1=1 and Z2=1, and CK0 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

Table 1 Metastability Detection and Signal Selection

| Sampler Output | | | MS Indicators | | MS Condition | Signal Selection | |
|---|---|---|---|---|---|---|---|
| A | B | C | Z1 | Z2 | | CK | MCS |
| D1 | D1 | D2 | 1 | 0 | insufficient hold time | CK0 | MCS1 |
| D1 | D2 | D2 | 0 | 1 | insufficient set-up time | CK1 | MCS0 |
| D1 | D1 | D1 | 1 | 1 | no metastability | CK0 | MCS0 |

[0080] FIGS. 10A-10D illustrate a relatively simple implementation of the metastability detection circuit (MDC) 910 where only three different sample points are provided to



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detect metastability condition in the module control signal. In general, the MDC 910 may generate more delayed versions of the module clock signal CK0 and/or the corresponding module control signal MCS0, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. 11A, the MDC 910 can include a plurality of delay circuits 1102 that generate *m* delayed versions of MCS0, e.g., MCS1, MCS2, … MCS*m*, and *m* delayed versions of CK0, e.g., CK1, CK2, …, CK*m*. The MDC 910 can include sampler circuits 1104 that sample MCS0 according to CK0, CK1, …, CK*m*, respectively, and sampler circuits 1104 that sample MCS0, MCS1, MCS2, … MCS*m* according to CK0, respectively. The outputs of the samplers 1104 are provided to a logic circuit 1120, which determines a metastability condition in MCK0 based on the sampler outputs using, for example, a majority decision logic. The logic circuit 1120 outputs a first metastability indicator on line(s) 912 and a second metastability indicator on line(s) 914.

[0081] FIG. 11B illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1171 that selects between CK0, CK1, …, CK*m* based on the metastability indicator provided on line(s) 912, and a second multiplexor 1172 that selects between MCS0, MCS1, …, MCS*m* based on the metastability indicator provided on line(s) 914, such that the rising edges of the selected clock signal, e.g., Ck*i*, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCS*i*. The selected signals MCS*i* and Ck*i* are provided to the sampler 930, which samples MCS*i* according to the rising edges of CK*i*.

[0082] As stated above, in certain embodiments, since the isolation devices 118 are in the data paths between the MCH 101 and the respective groups of memory devices 112, the MCH 101 does not have direct control of the memory devices 112. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior



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write operation, as discussed further below.

[0083] FIG. 12A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit 116 at time t1, the module control circuit 116 outputs one or more enable signals EN at time t2 in response to the write commands. The one or more enable signals are received by an isolation device 118 at time t3, which afterwards receives one or more strobe signal DQS from the MCH 101 at time t4. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system 100, and is controllable by the MCH 101 and knowable to the isolation device 118. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device 118 since both these signals are received by the isolation device. Based on such determination, the isolation device 118 can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device 118 to properly time transmission of read data to the MCH, as explained further below.

[0084] FIG. 12B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit 116 at time t5, the module control circuit 116 outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device 118 at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices 118.

[0085] With knowledge of the time interval between t7 and t5, which should be about the



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same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101 via the respective group of data/strobe signal lines 130, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system 100.

[0086] The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit 650 in the ID control circuit 310, as shown in FIG. 6. According to one embodiment, as shown in FIG. 13, the delay control circuit 650 includes a peramble detector 1310 to detect a write preamble in the DQS, a flip-flop circuit 1320 having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK0, and a counter circuit 1330 having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit 1320. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

[0087] FIG. 14 illustrates a DQ or DQS routing circuit 320 or 620 according to an embodiment. As shown, the DQ/DQS routing circuit 320/620 includes a DQ/DQS pin 1401 that is coupled to the corresponding DQ/DQS signal line 322/324, a set of one or more DQS pins 1402 that is coupled to a corresponding module DQ/DQS line(s) $Y/Y_{DQS}$, or $YA/YA_{DQS}$ and $YB/YB_{DQS}$. The DQ/DQS routing circuit 320/620 further includes a write strobe buffer 1410 that buffers write data/strobe, and a write data/strobe receiver 1420 that samples the write data/strobe. The DQ/DQS routing circuit 320/620 further includes a plurality of write paths 1430 that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

[0088] The DQS routing circuit further includes a plurality of read paths 1450 that are selectable by the one or more of the module control signals. Output from the seleted read path is delayed in a delay circuit 1460 by an amount controlled by the delay signal DS, and



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sampled by a sampler circuit 1470. The sampled read data/strobe is transmitted by transmitter 1480 onto the corresponding data/strobe signal line 322/324 via the DQ/DQS pin 1401.

[0089] FIG. 15 illustrates a DQS routing circuit 620 according to an embodiment. As shown, the DQS routing circuit 620 includes a first DQS pin 1501 that is coupled to a corresponding DQS signal line 324, a second DQS pin 1502A that is coupled to a corresponding module DQS line $YA_{DQS}$, a third DQS pin 1502B that is coupled to a corresponding module DQS line $YB_{DQS}$. The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe path includes a write strobe buffer 1510 that buffers a write strobe, a write strobe receiver 1520 that samples the write strobe according to the buffered module signal CK0. The sampled write strobe is provided to the DQ routing circuits 320 as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter 1530A that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line $YA_{DQS}$. The second write strobe path includes the write strobe buffer 1510, the write strobe receiver 1520, and a second write strobe transmitter 1530B that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line $YB_{DQS}$. The first and second write strobe transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0090] The DQS routing circuit further includes a read strobe path coupled between the first DQS pin 1501 and a selected one of the second and third DQS pins 1502A and 1502B. In the read strobe path, a select circuit 1550 (e.g., a multiplexor) selects either a read strobe signal received via DQS pin 1502A or a read strobe signal received via DQS pin 1502B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0. The



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sampled read strobe is provided to the DQ routing circuits 320 as the read strobe RDQS and is transmitted by transmitter 1580 onto the corresponding strobe signal line 324 via the first DQS pin 1501.

[0091] FIG. 16 illustrates a DQ routing circuit 320 according to an embodiment. As shown, the DQ routing circuit 320 includes a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line $YA_{DQ}$, a third DQ pin 1602B that is coupled to a corresponding module DQ line $YB_{DQ}$. The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer 1610, a write data receiver 1620 that samples write data according to the write strobe WDQS from the DQS routing circuit 620, and a first write data transmitter 1630A that transmits the write data to one or more memory devices 112 coupled to the module data line $YA_{DQ}$. The second write data path includes the write data buffer 1610, the write data receiver 1620, and a second write data transmitter 1630B that transmits the write data to one or more memory devices 112 coupled to the module data line $YB_{DQ}$. The first and second write data transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0092] The DQ routing circuit further includes a read data path coupled between the first DQ pin 1601 and a selected one of the second and third DQ pins 1602A and 1602B. In the read data path, a select circuit 1650 (e.g., a multiplexor) selects either a read data signal received via DQ pin 1602A or a read data signal received via DQ pin 1602B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.



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[0093] FIG. 17 illustrate a delay circuit 1560 or 1660 according to an embodiment. As shown, the delay circuit 1560 or 1660 includes a plurality of delay stages, such as delay stages 1710, 1720, and 1730, each delaying a read data or read strobe signal from the select circuit 1550/1650 by a predetermined amount. The delay circuit 1560 or 1660 further includes a select circuit 1740 (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit 1740, is provided to the sampler circuit 1570 or 1670, either directly or after being buffered by a buffer circuit 1750.

[0094] Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device 118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

[0095] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the



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isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.

[0096] As shown in FIG. 18, a delay signal DS is generated according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.

[0097] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100.

[0098] In certain embodiments, especially the embodiments shown in FIG. 2D, the delay circuits 1560 and 1660 shown in FIGS. 15 and 16 are not needed to provide alignment of the read data. As shown in FIG. 19, the ID control circuit 310 includes a clock regeneration circuit 1920 that regenerates the clock signal CK received from the control circuit 116, according to the delay signal DS. The regenerated clock signals CK0 and CKM each includes a proper amount of delay as compared to the clock signal CK. The clock CK0 is provided to the strobe routing circuit 620 so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer 118 and the respective



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set of memory devices are locally synchronized.



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WE CLAIM:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board including edge connections for connecting to respective ones of the signal lines in the memory bus;

memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines;

buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and

a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals;

wherein the each respective buffer circuit is configured to respond to one or more first control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation;

wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and

wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing



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information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation.

2. The memory module of claim 1, wherein the each respective buffer circuit includes a delay control circuit that determines a time interval between receiving the one or more first control signals and the write data/strobe signals during the write operation, and wherein the each respective buffer circuit times the transmission of the read data/strobe signals during the read operation based on the time interval.

3. The memory module of claim 2, wherein the delay control circuit includes a preamble detector to detect a preamble in a write strobe signal in order to determine the time interval.

4. The memory module of claim 1, wherein each buffer circuit includes receiver circuits to receive respective ones of the first control signals during the write operation, the receiver circuits including metastability detection circuits to detect metastability condition in the one or more first control signals, and wherein each buffer circuit further includes at least one signal adjustment circuit to adjust the one or more first control signals to mitigate any metastability condition in the one or more first control signals.

5. The memory module of claim 1, wherein the module control device further receives a system clock from the memory controller and transmits a registered clock signal to the plurality of buffer circuits, and wherein the each respective buffer circuit regenerates one or more clock signals from the registered clock signal and provides a regenerated clock signal to the respective group of memory devices.

6. The memory module of claim 1, wherein the respective buffer circuit comprises:

a time interval determination circuit to receive, during the write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first signal and the second signal;

a delay circuit to delay the respective set of read data signals received from the respective group of memory devices according to the delay signal.



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7. A method of operating a memory module coupled to a memory controller via a memory bus, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module including memory devices and a module controller coupled to the memory controller via the set of control/address signal lines, the method comprising:

receiving one or more first control signals from the module control device;

receiving respective sets of write data/strobe signals from respective sets of data/strobe signal lines in accordance with the one or more first control signals;

deriving timing information from receiving the one or more first control signals and receiving the respective sets of write data/strobe signals;

transmitting the respective sets of write data/strobe signals to respective groups of the memory devices in accordance with the one or more first control signals;

receiving one or more second control signals from the module control device;

receiving respective sets of read data/strobe signals from respective groups of the memory devices in accordance with the one or more second control signals;

transmitting the respective sets of read data/strobe signals to respective sets of data/strobe signal lines in accordance with the one or more second control signals and in accordance with the timing information.

8. The method of claim 7, further comprising:

determining a metastability condition associated with the one or more first control signals; and

adjusting at least one of the one or more first control signals based on the metastability condition.

9. The method of claim 7, further comprising:

determining a time interval between receiving one of the one or more first control signals and receiving one of a respective set of read data/strobe signals; and

delaying the respective set of read data/strobe signals according to the time interval.



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10. The method of claim 9 wherein one of the one or more first control signals is a clock signal.

11. The method of claim 9 wherein the one of the respective set of read data/strobe signals is a read strobe signal.

12. The method of claim 9, the method further comprising:

detecting a preamble of a write strobe signal to determine the time interval.

13. A buffer circuit for use on a memory module coupled to a memory controller via a memory bus, the memory module including memory devices and a module controller coupled to the memory controller via the set of control/address signal lines, the buffer circuit comprising:

a time interval determination circuit to determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory bus; and

a delay circuit to time transmission of data/strobe signals received from one of the memory devices to the memory controller via the data bus according to the time interval.

14. The buffer circuit of claim 13 wherein the buffer circuit further comprises receiver circuits to receive module control signals from the module control device, each receiver circuit including a metastability detection circuit to detect metastability condition in a corresponding one of the module control signals.

15. The buffer circuit of claim 13 wherein the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more of the module control signals to mitigate metastability condition in the module control signals.

16. The buffer circuit of claim 12, wherein the first signal is an enable signal to enable a write data path in the buffer circuit.

17. The buffer circuit of claim 15, wherein the second signal is a write strobe signal.



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18. The buffer circuit of claim 15, wherein the second signal has a preamble, and wherein the time interval determination circuit includes a preamble detector to detect the preamble of the second signal.

19. The buffer circuit of claim 15, wherein the time interval determination circuit further includes a counter to count a number of clock cycles between receipt of the first signal and detection of the preamble of the second signal.

20. The buffer circuit of claim 12, wherein the buffer circuit is coupled to a respective group of the plurality of memory devices on the memory module, and wherein the buffer circuit further comprises a clock regeneration circuit to receive a clock signal from the module controller and to provide a regenerated clock signal to the respective group of the plurality of memory devices.



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# MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION


## ABSTRACT OF THE DISCLOSURE

A memory module is operatable in a memory system with a memory controller. The memory module comprises a module control device to receive command signals from the memory controller and to output module command signals and module control signals. The module command signals are provided to memory devices organized in groups, each group including at least one memory device, while the module control signals are provided to a plurality of buffer circuits to control data paths in the buffer circuits. The plurality of buffer circuits are associated with respective groups of memory devices and are distributed across a surface of the memory module such that each module control signal arrives at the plurality of buffer circuits at different points in time. The plurality of buffer circuits are configured to align read data signals received from the memory devices such that the read data signals are transmitted to the memory controller from the memory module substantially aligned with each other and in accordance with a read latency parameter of the memory system.

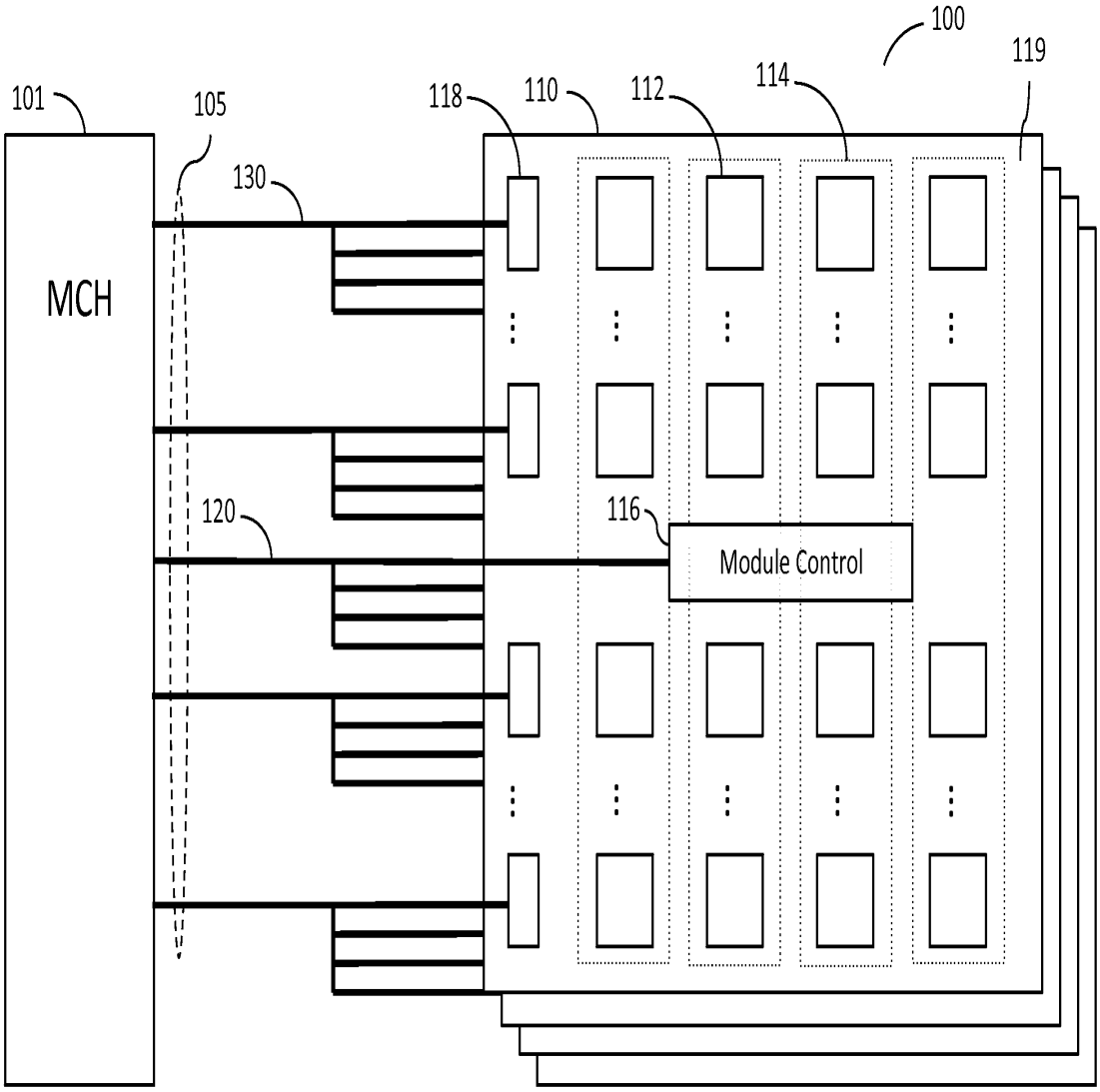


FIG. 1

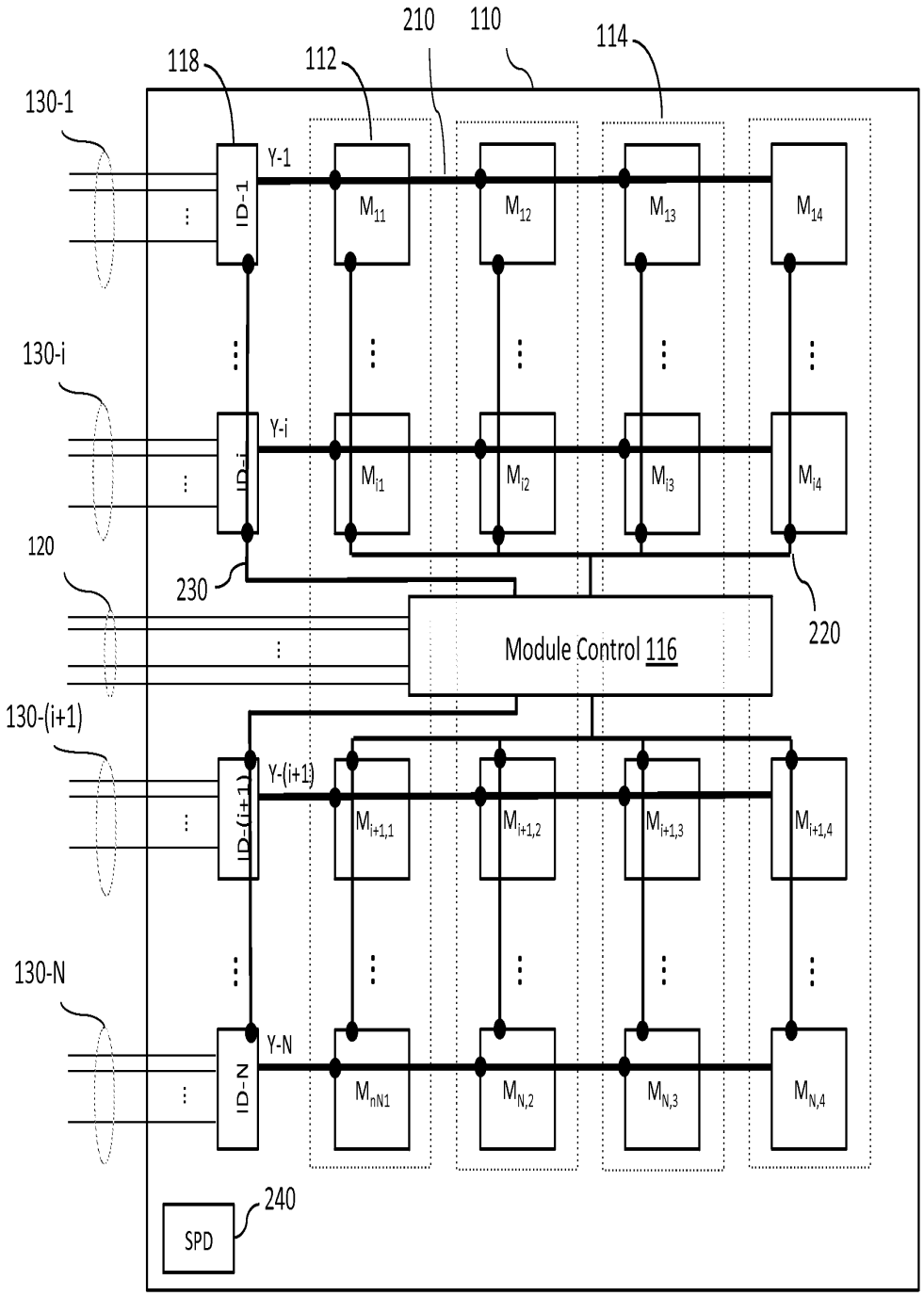
210
110
114
118
112
130-1
Y-1
ID-1
M11
M12
M13
M14
130-i
Y-i
ID-i
Mi1
Mi2
Mi3
Mi4
120
230
220
Module Control 116
130-(i+1)
Y-(i+1)
ID-(i+1)
Mi+1,1
Mi+1,2
Mi+1,3
Mi+1,4
130-N
Y-N
ID-N
MnN1
MN,2
MN,3
MN,4
240
SPD

FIG. 2A

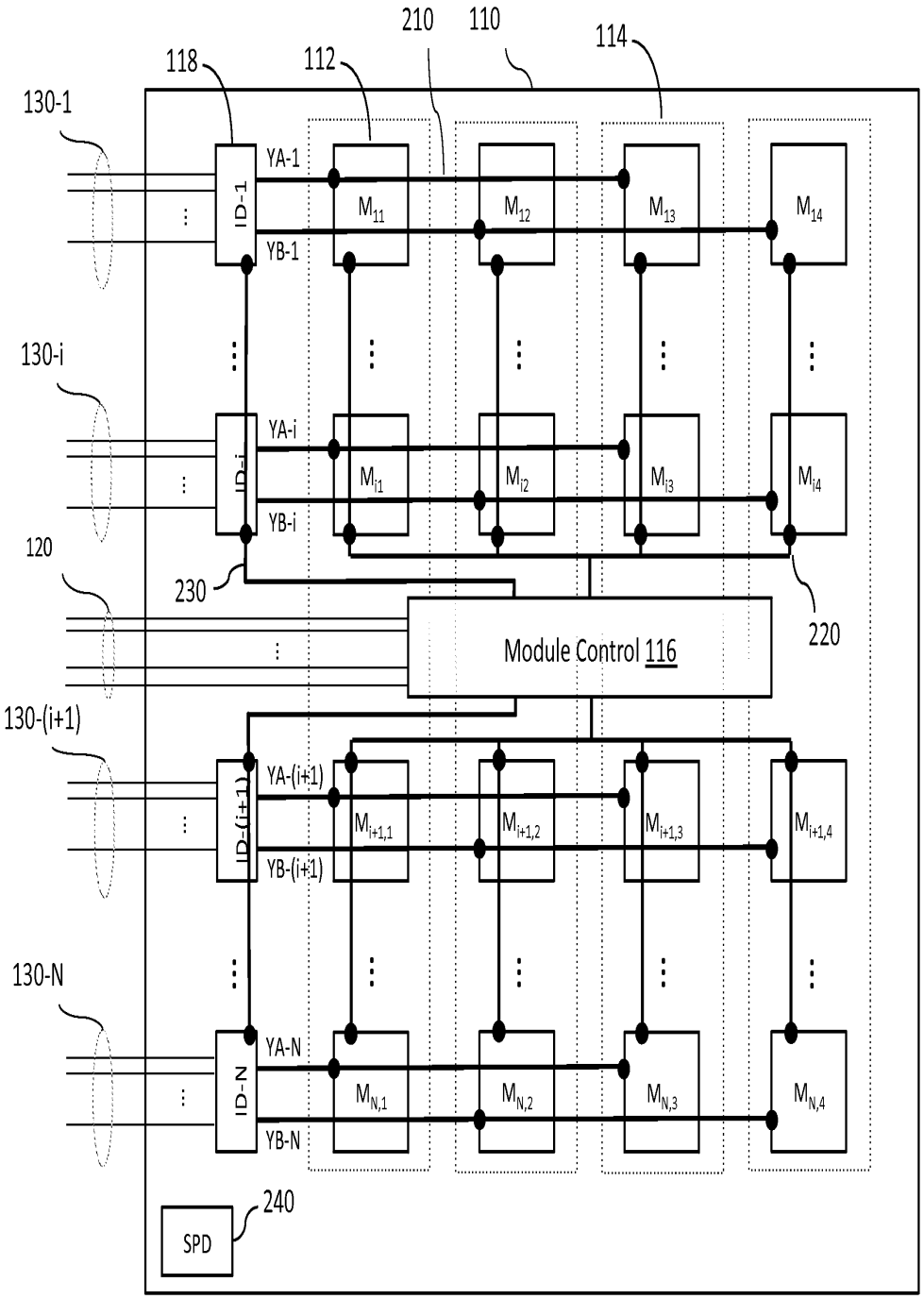
210
110
114
118
112
130-1
YA-1
ID-1
YB-1
$M_{11}$
$M_{12}$
$M_{13}$
$M_{14}$
130-i
YA-i
ID-i
YB-i
$M_{i1}$
$M_{i2}$
$M_{i3}$
$M_{i4}$
120
230
220
Module Control 116
130-(i+1)
YA-(i+1)
ID-(i+1)
YB-(i+1)
$M_{i+1,1}$
$M_{i+1,2}$
$M_{i+1,3}$
$M_{i+1,4}$
130-N
YA-N
ID-N
YB-N
$M_{N,1}$
$M_{N,2}$
$M_{N,3}$
$M_{N,4}$
240
SPD

FIG. 2B

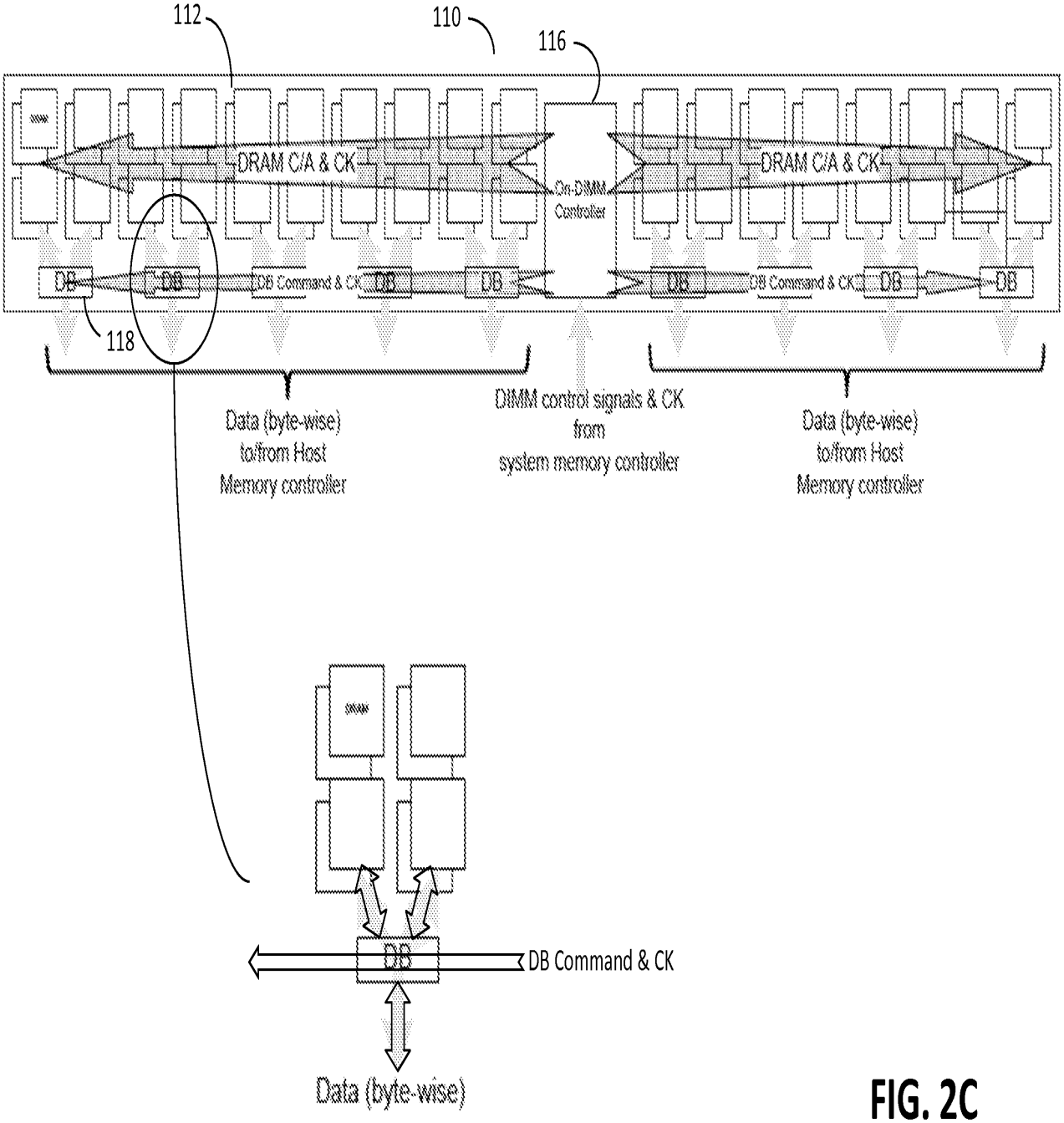
112
110
116
DRAM C/A & CK
On-DIMM Controller
DRAM C/A & CK
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
DB
DB Command & CK
Data (byte-wise)

FIG. 2C

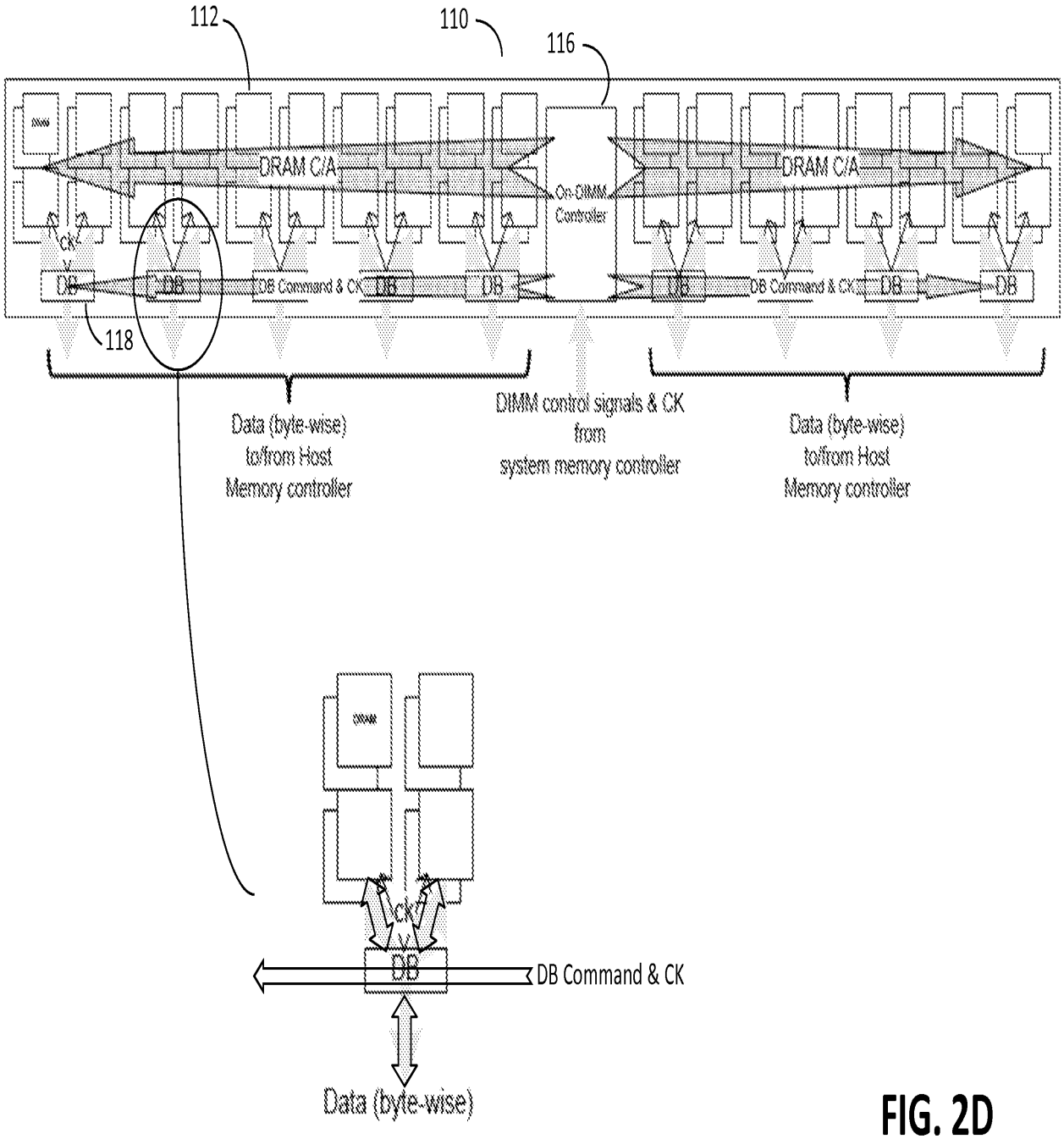
112
110
116
DRAM C/A
DRAM C/A
On-DIMM Controller
CK
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
CK
DB
DB Command & CK
Data (byte-wise)

FIG. 2D

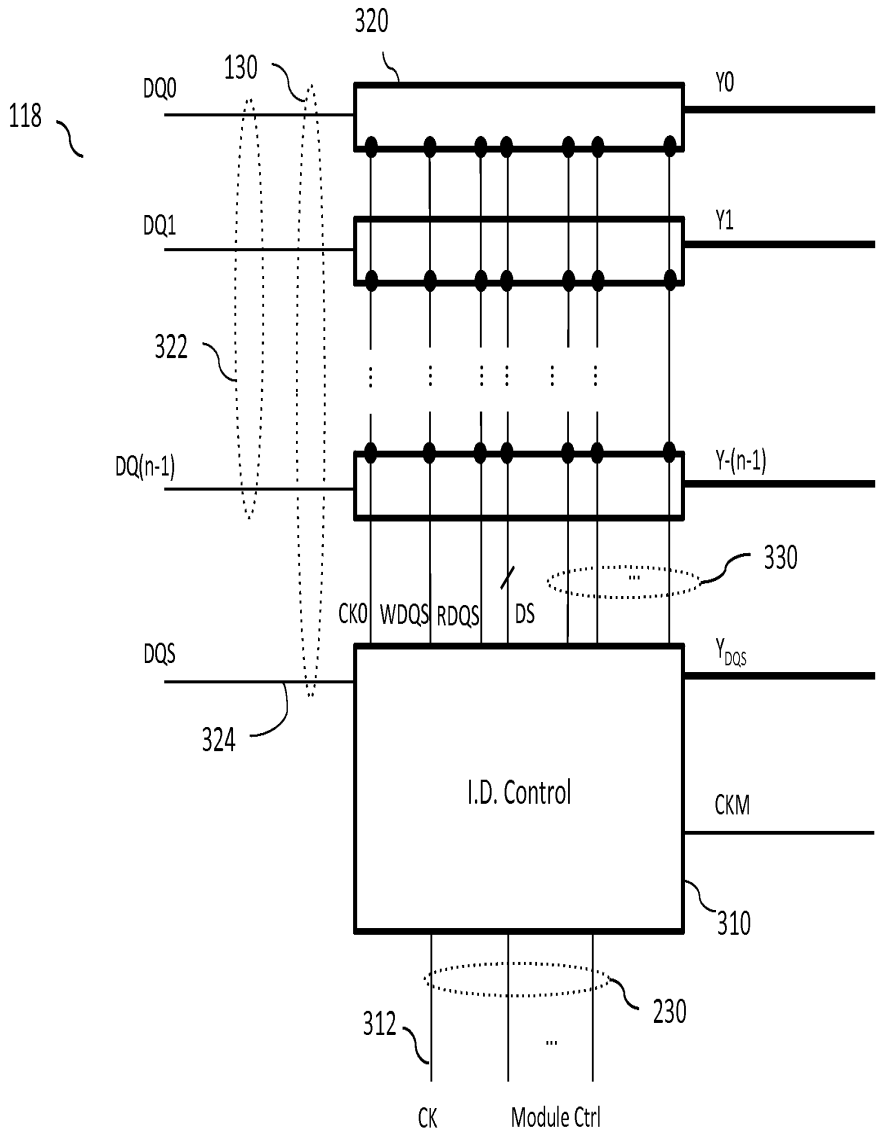
320
130
118
DQ0
Y0
DQ1
Y1
322
DQ(n-1)
Y-(n-1)
330
CK0
WDQS
RDQS
DS
DQS
$Y_{DQS}$
324
I.D. Control
CKM
310
230
312
CK
Module Ctrl

FIG. 3

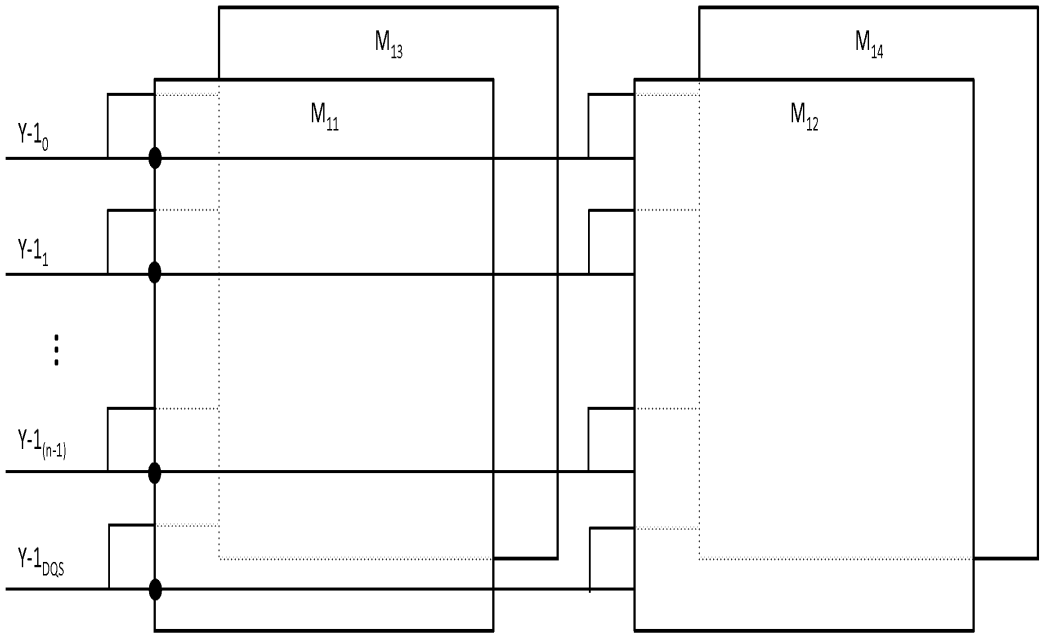


FIG. 4A

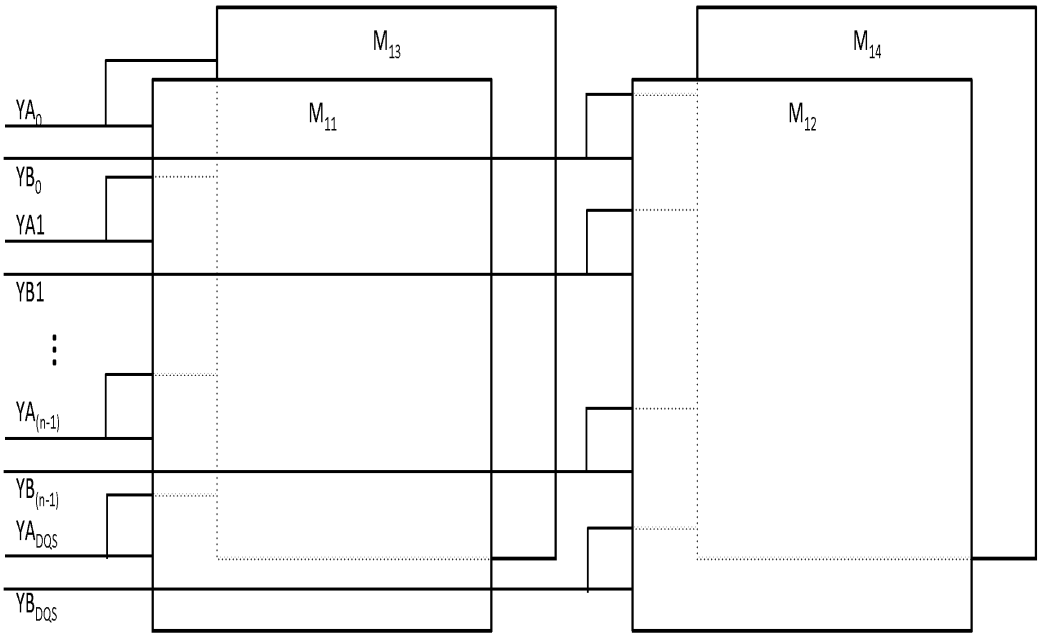


FIG. 4B

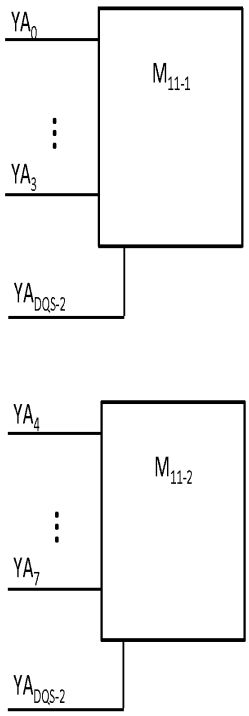
YA0
YA3
M11-1
YADQS-2
YA4
YA7
M11-2
YADQS-2

FIG. 5A

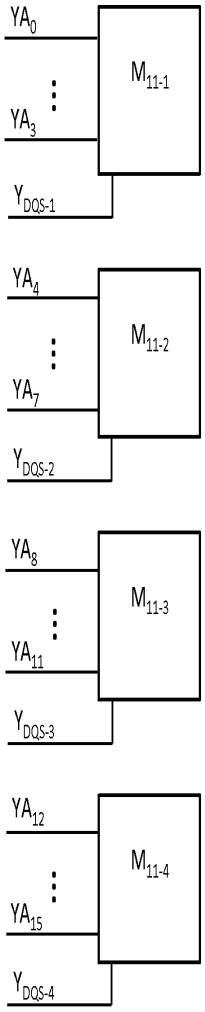
YA0
YA3
M11-1
YDQS-1
YA4
YA7
M11-2
YDQS-2
YA8
YA11
M11-3
YDQS-3
YA12
YA15
M11-4
YDQS-4

FIG. 5B

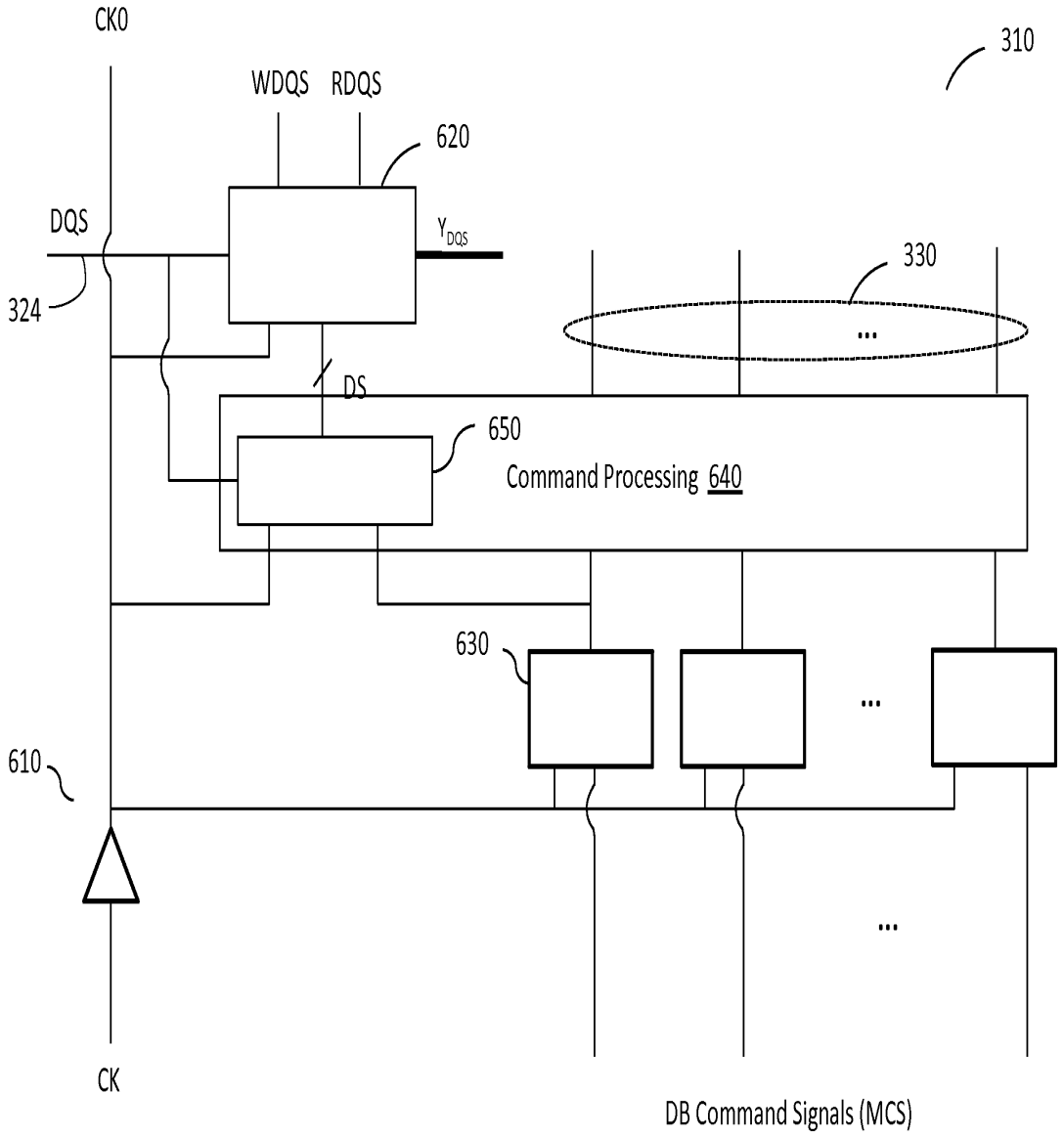
CK0
310
WDQS
RDQS
620
DQS
$Y_{DQS}$
330
324
...
DS
650
Command Processing 640
630
...
610
...
CK
DB Command Signals (MCS)

FIG. 6

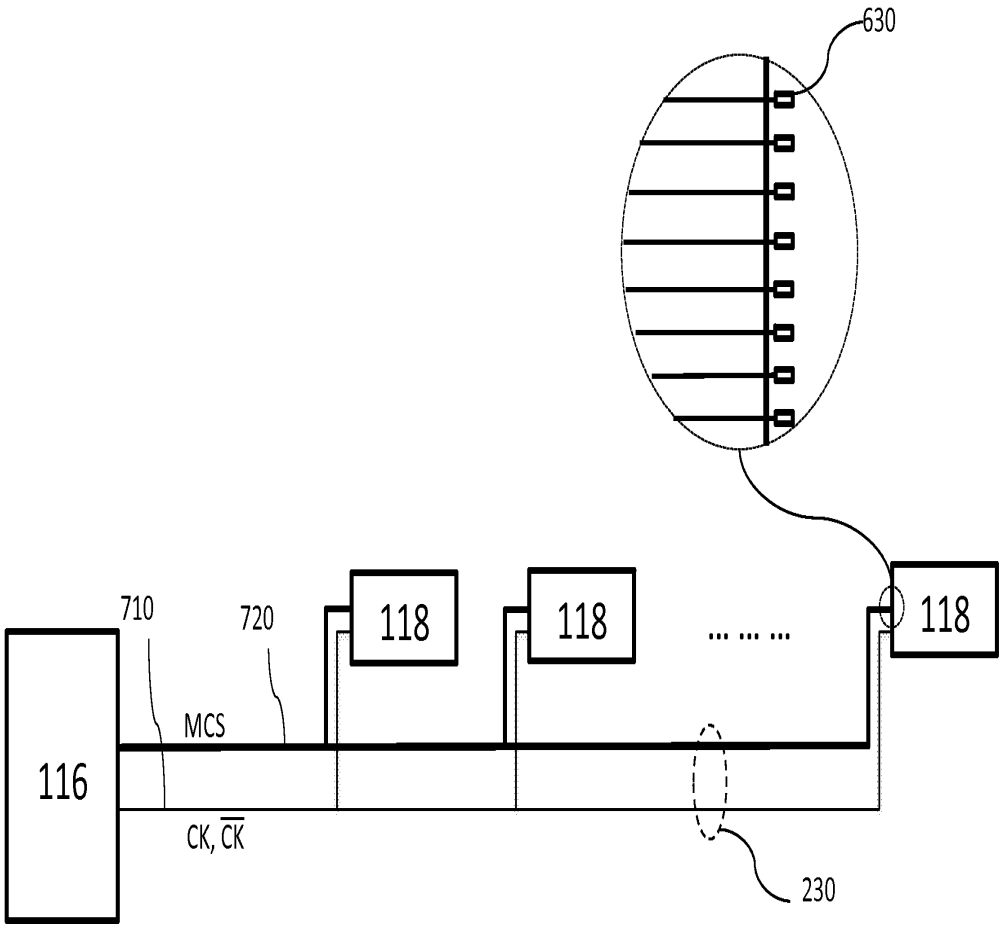


FIG. 7

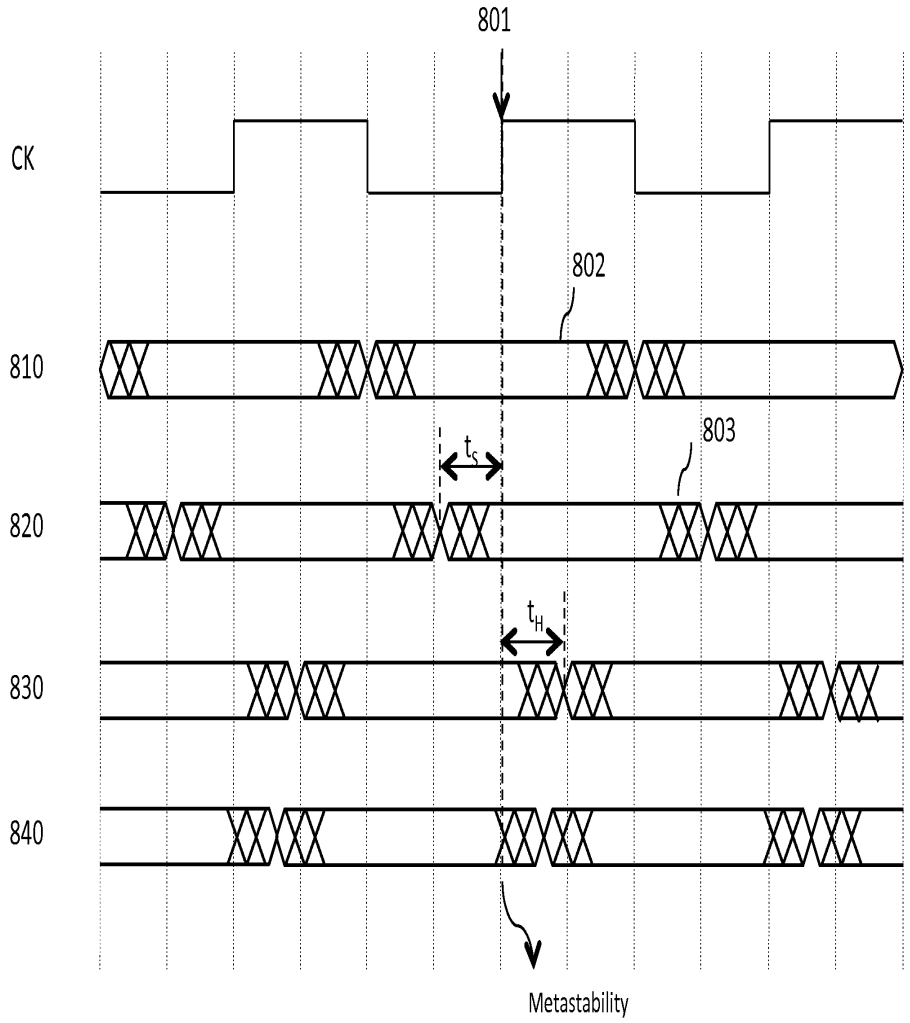


FIG. 8

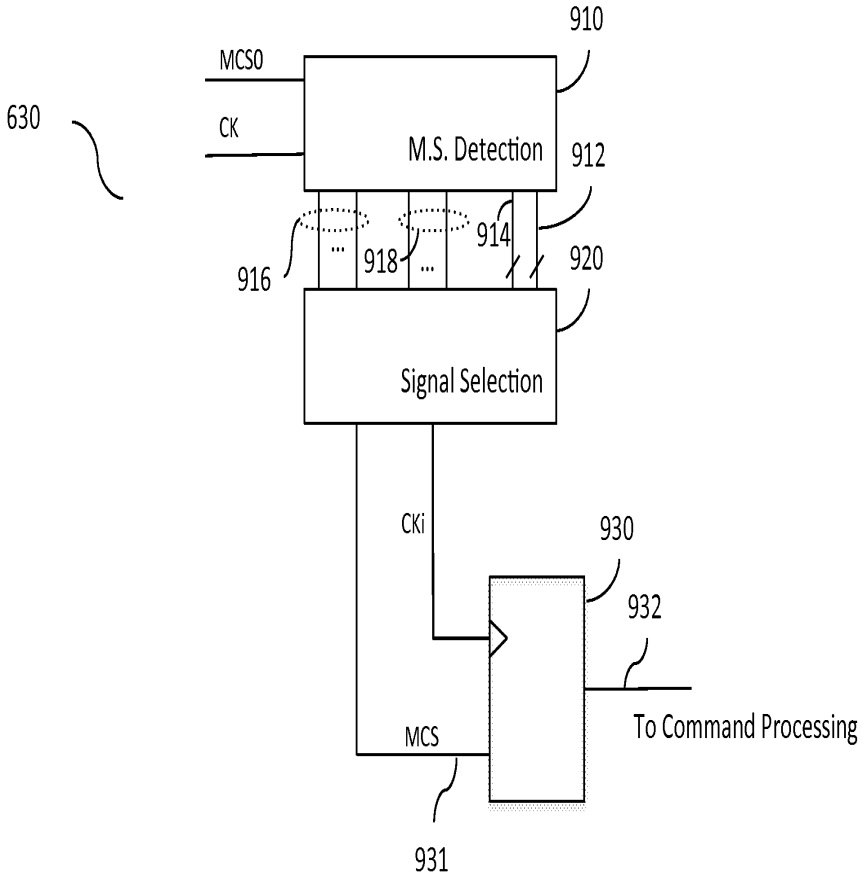
910
MCS0
630
CK
M.S. Detection
912
914
916
918
920
Signal Selection
CKi
930
932
To Command Processing
MCS
931

FIG. 9

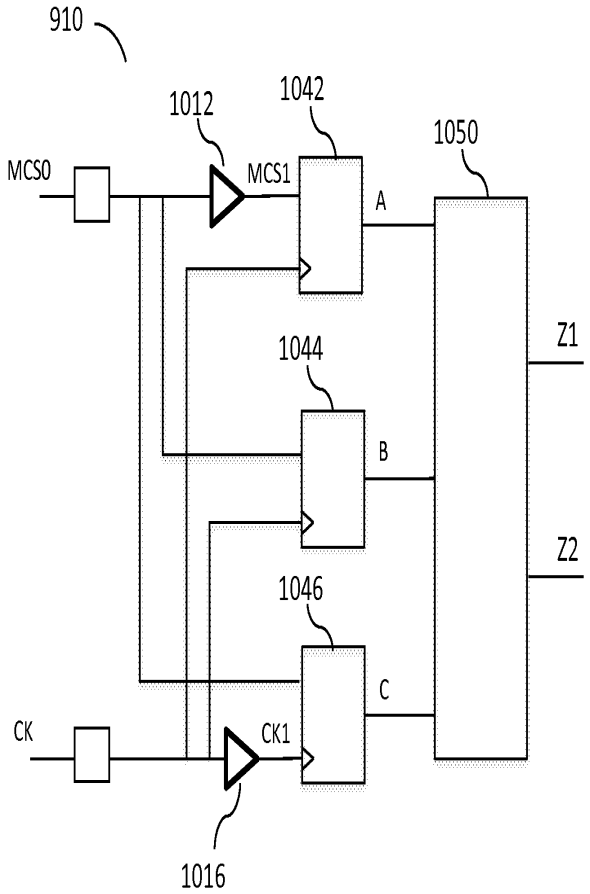


FIG. 10A

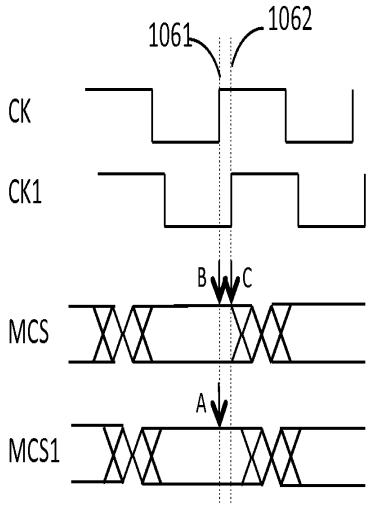


FIG. 10B

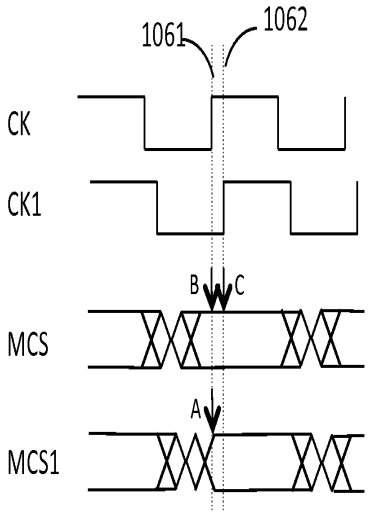


FIG. 10C

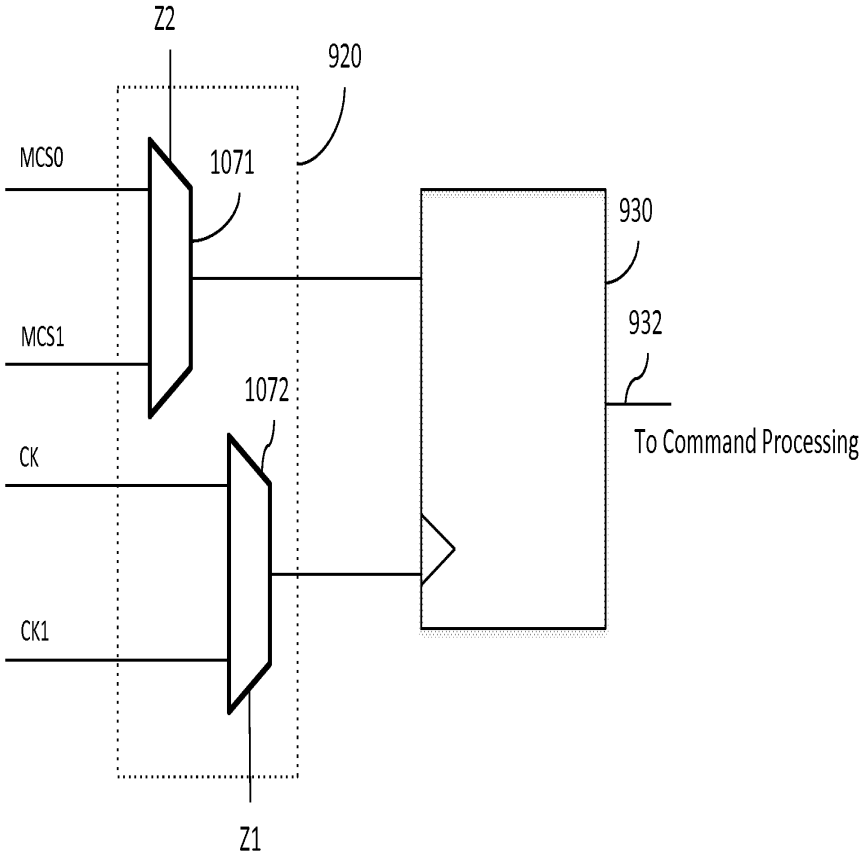
Z2
920
MCS0
1071
930
MCS1
932
1072
To Command Processing
CK
CK1
Z1

FIG. 10D

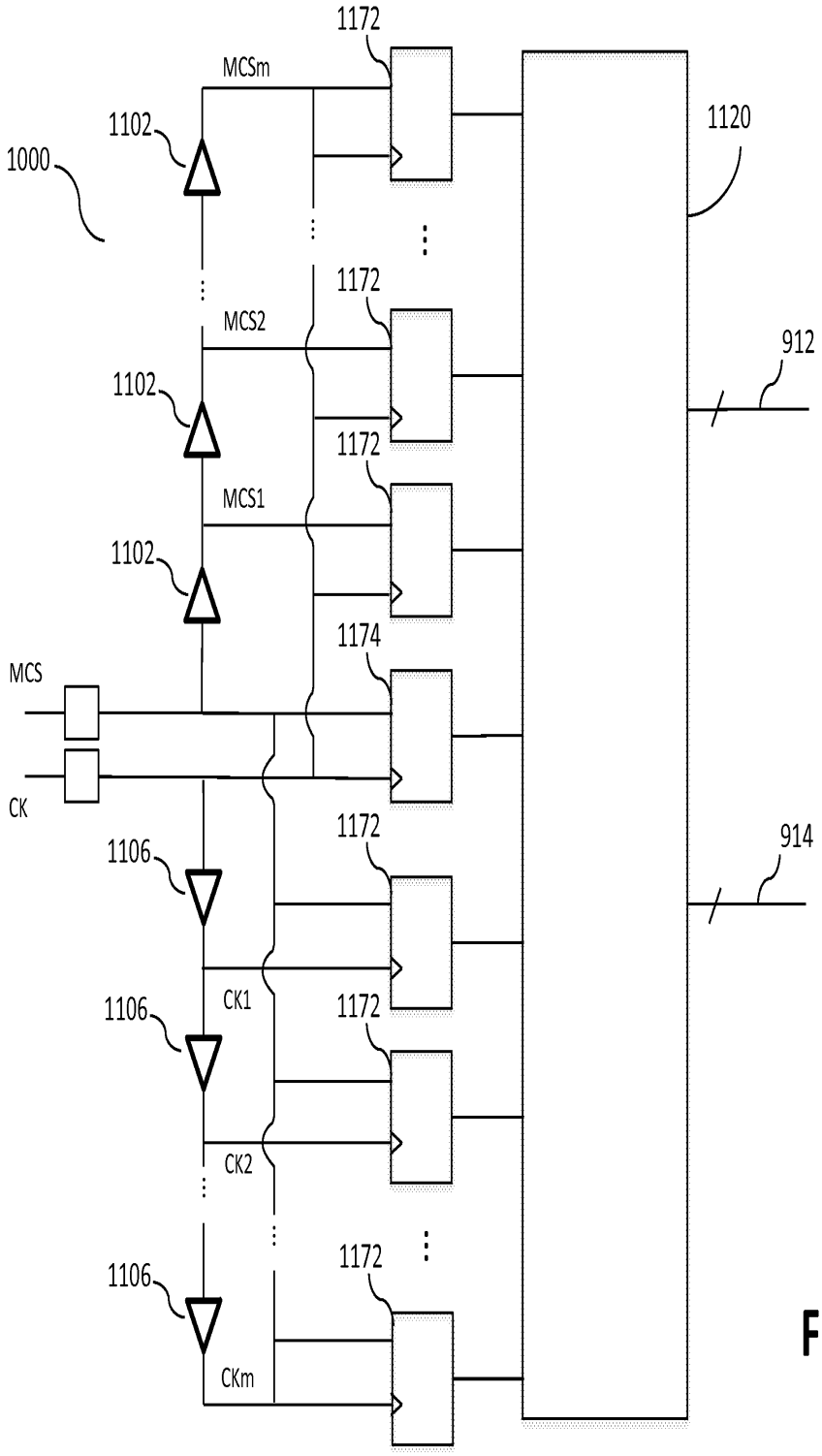
1172
MCSm
1102
1000
1120
1172
MCS2
912
1102
1172
MCS1
1102
1174
MCS
CK
1172
914
1106
CK1
1172
1106
CK2
1172
1106
CKm

FIG. 11A

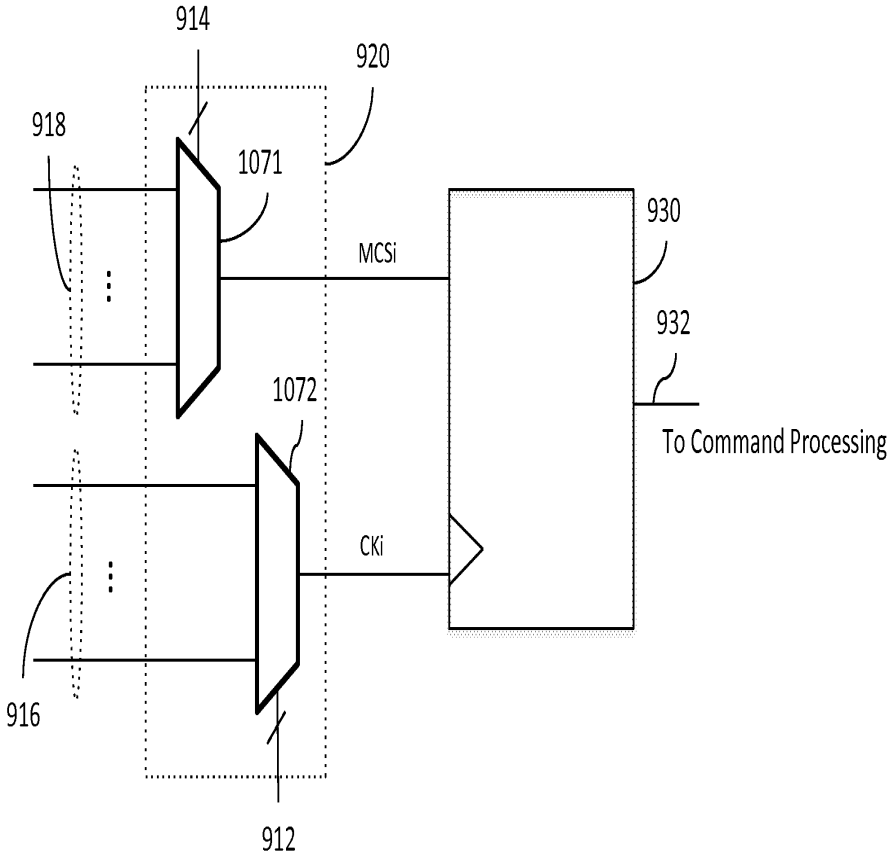
914
920
918
1071
930
MCSi
932
1072
To Command Processing
CKi
916
912

FIG. 11B

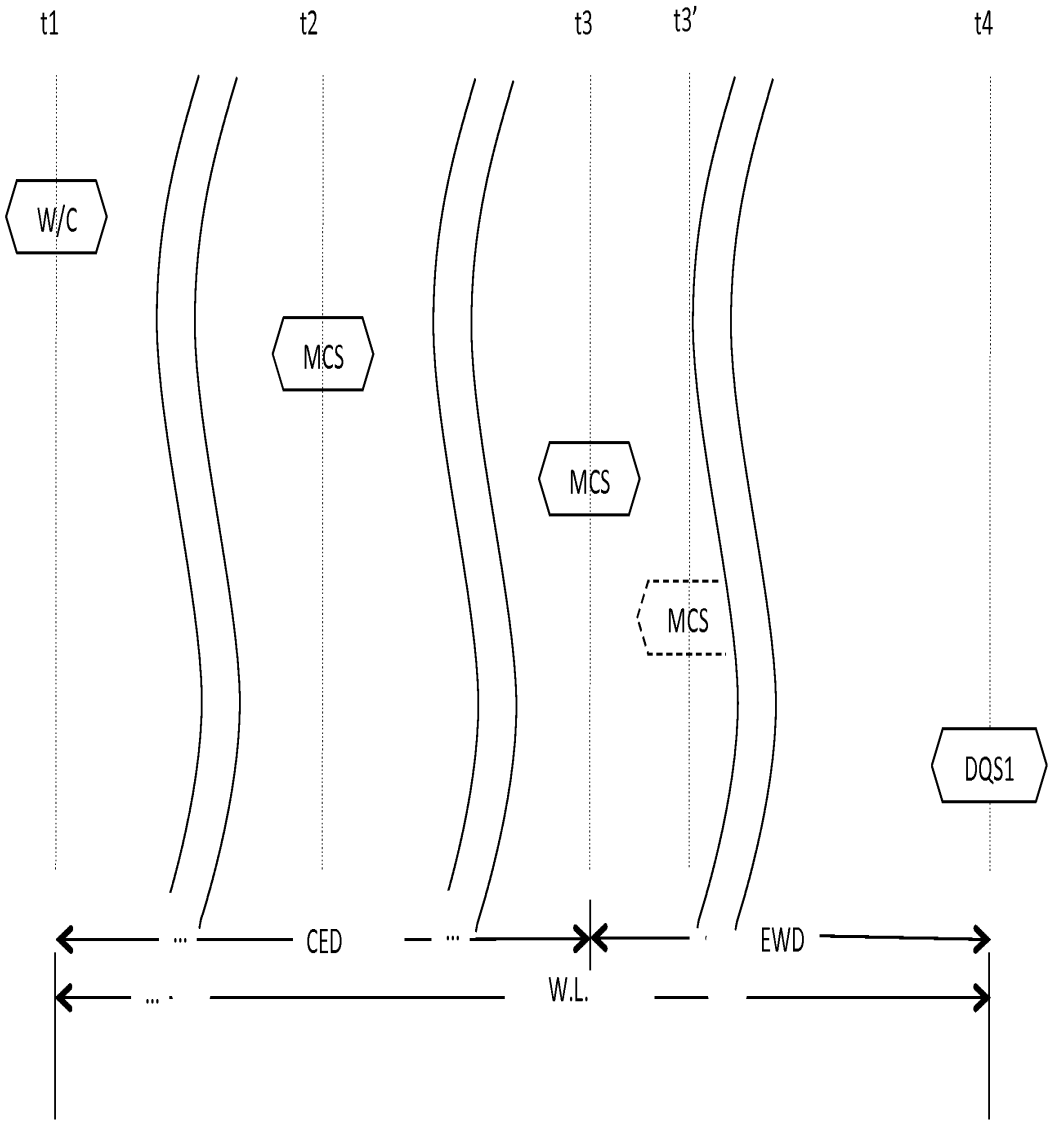


FIG. 12A

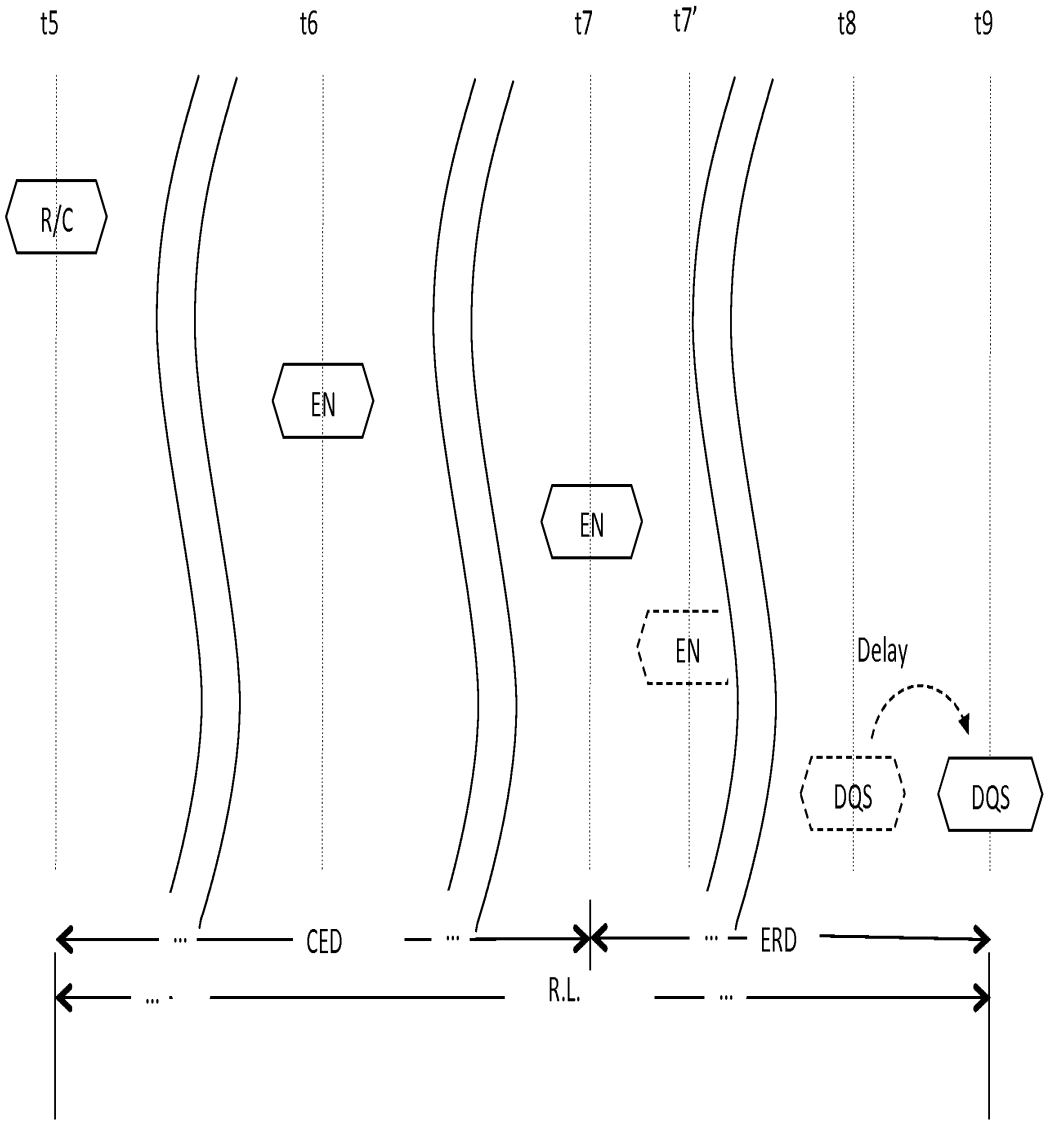


FIG. 12B

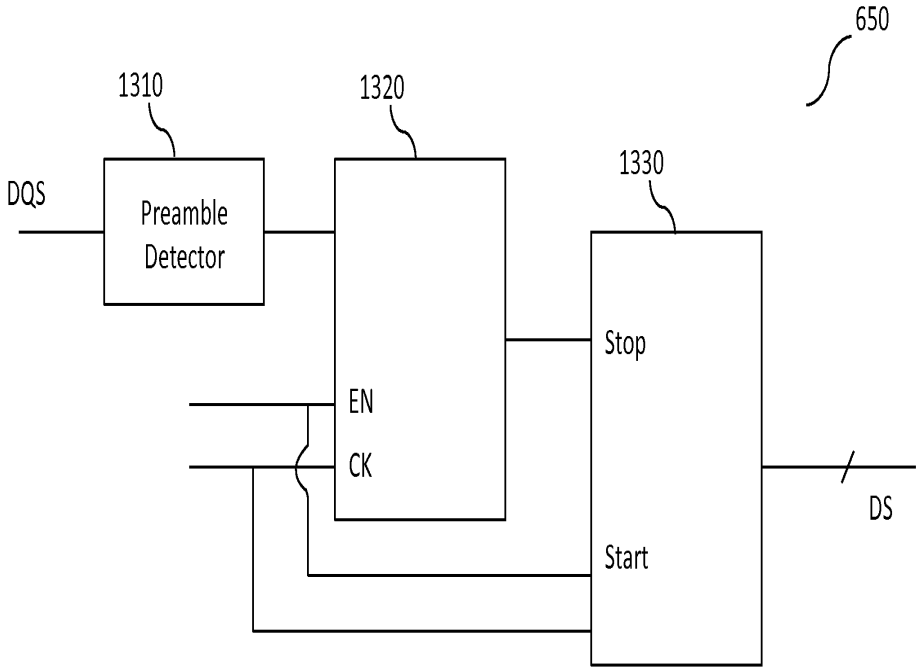


FIG. 13

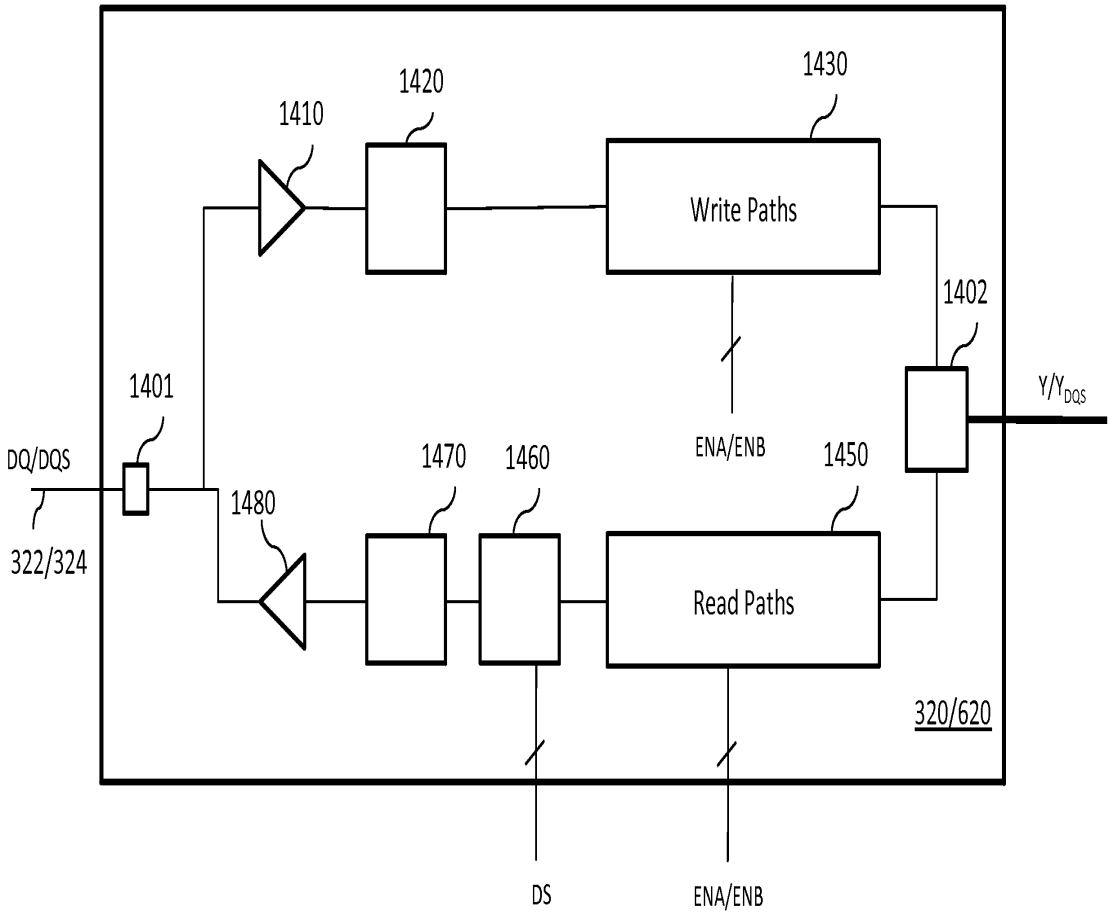
1410
1420
1430
Write Paths
1402
Y/Y_DQS
1401
DQ/DQS
322/324
ENA/ENB
1470
1460
1450
1480
Read Paths
320/620
DS
ENA/ENB

FIG. 14

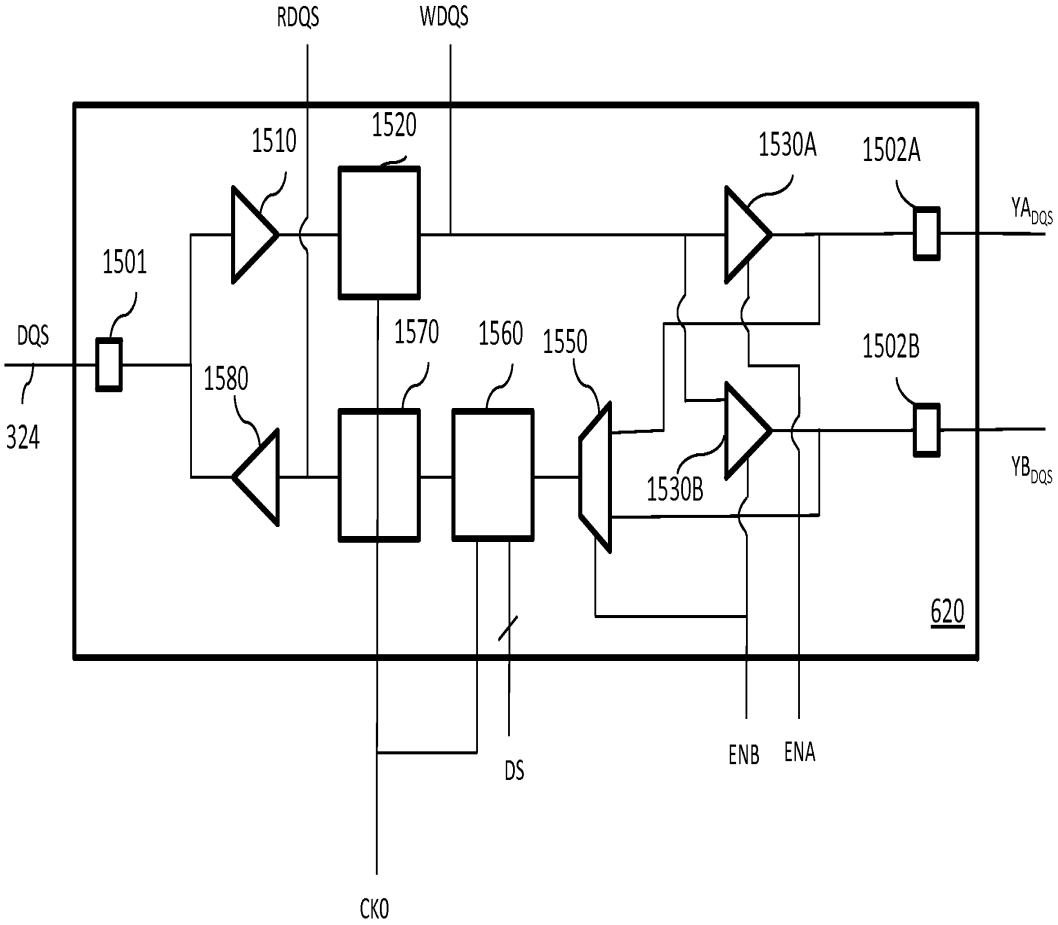
RDQS
WDQS
1510
1520
1530A
1502A
YA$_{DQS}$
1501
DQS
324
1580
1570
1560
1550
1502B
1530B
YB$_{DQS}$
620
DS
ENB
ENA
CK0

FIG. 15

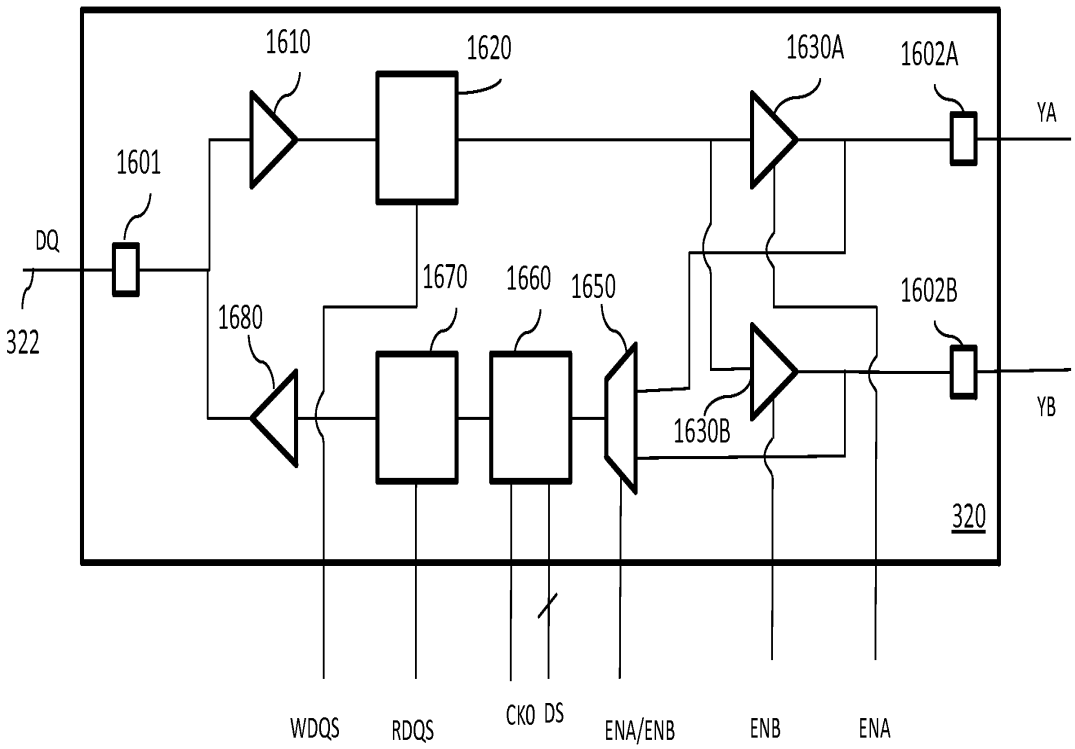
1610
1620
1630A
1602A
YA
1601
DQ
322
1680
1670
1660
1650
1602B
YB
1630B
320
WDQS
RDQS
CK0
DS
ENA/ENB
ENB
ENA

FIG. 16

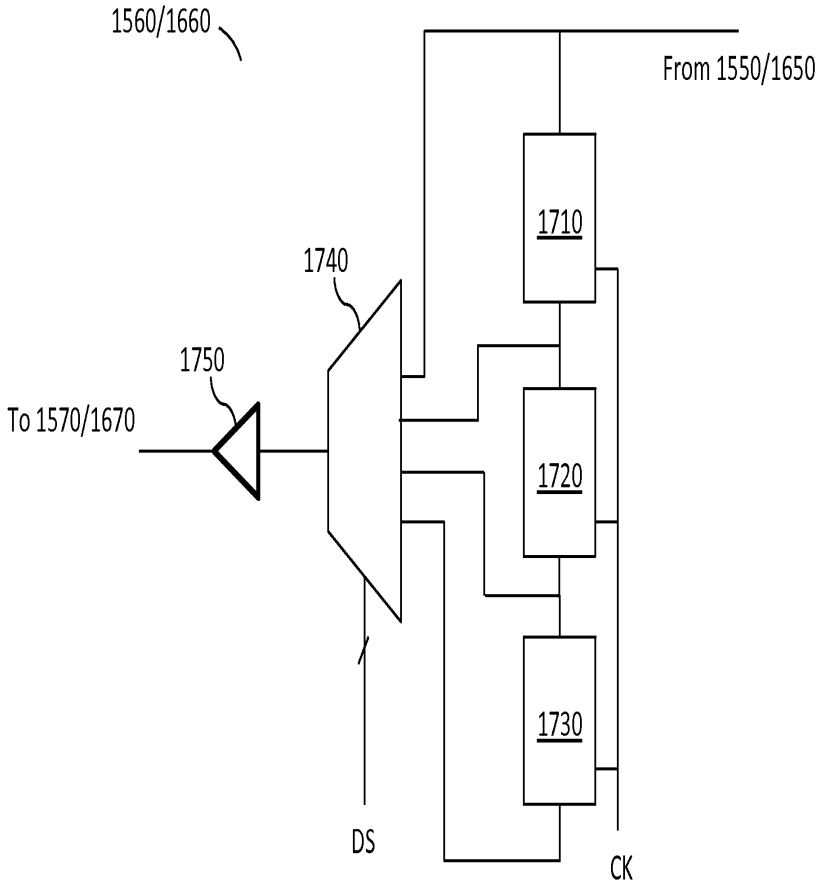
1560/1660
From 1550/1650
1710
1740
1750
To 1570/1670
1720
1730
DS
CK

FIG. 17

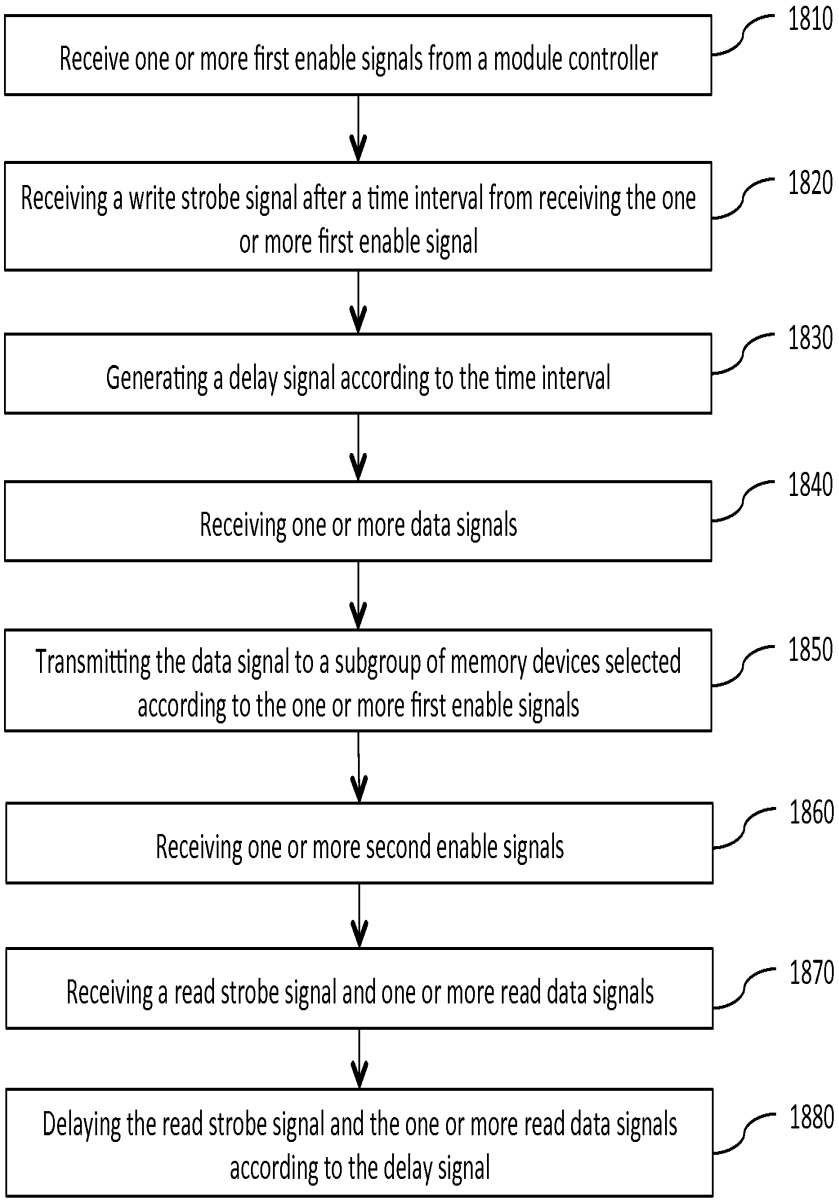
Receive one or more first enable signals from a module controller
1810
Receiving a write strobe signal after a time interval from receiving the one or more first enable signal
1820
Generating a delay signal according to the time interval
1830
Receiving one or more data signals
1840
Transmitting the data signal to a subgroup of memory devices selected according to the one or more first enable signals
1850
Receiving one or more second enable signals
1860
Receiving a read strobe signal and one or more read data signals
1870
Delaying the read strobe signal and the one or more read data signals according to the delay signal
1880

FIG. 18

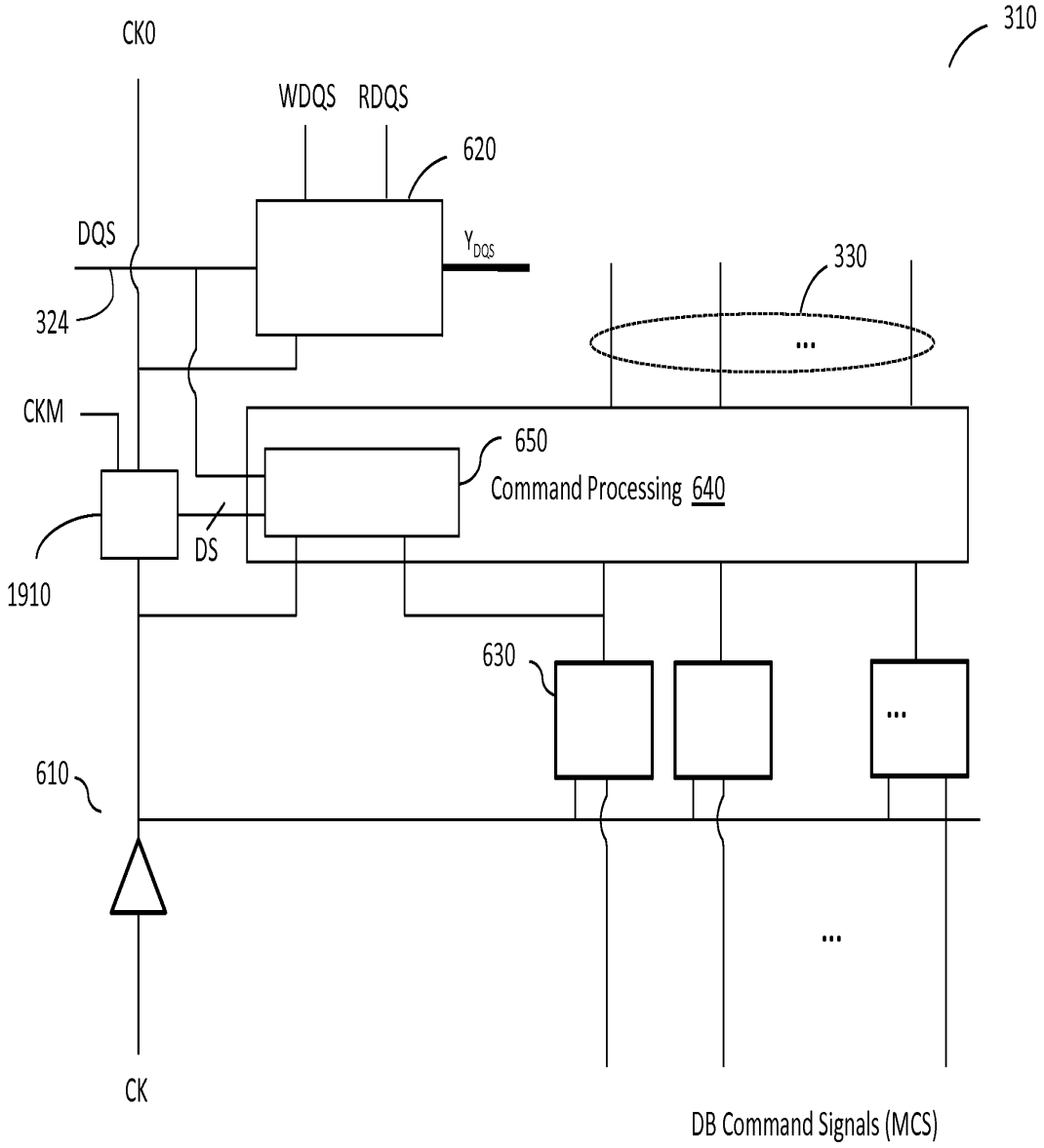
CK0
310
WDQS
RDQS
620
DQS
$Y_{DQS}$
330
324
CKM
650
Command Processing 640
DS
1910
630
610
CK
DB Command Signals (MCS)

FIG. 19

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | |
| **Filing Date:** | |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Jamie Jie Zheng |
| **Attorney Docket Number:** | NT003C1 |

Filed as Small Entity

**Filing Fees for Utility under 35 USC 111(a)**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| Utility filing Fee (Electronic filing) | 4011 | 1 | 70 | 70 |
| Utility Search Fee | 2111 | 1 | 300 | 300 |
| Utility Examination Fee | 2311 | 1 | 360 | 360 |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | | **Total in USD ($)** | **730** |

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 23418983 |
| **Application Number:** | 14846993 |
| **International Application Number:** | |
| **Confirmation Number:** | 5461 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | NT003C1 |
| **Receipt Date:** | 07-SEP-2015 |
| **Filing Date:** | |
| **Time Stamp:** | 23:29:13 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Credit Card |
| Payment was successfully received in RAM | $730 |
| RAM confirmation Number | 22423 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Application Data Sheet | 2015-09-07_ApplicationDataSheet_NT003C1.pdf | 1437292<br>25eb5a45540baf32753bc3df1865fb460572ddd0 | no | 6 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | | 2015-09-07_Specification_NT003C1.pdf | 358211<br>c576b107e09467e596834fd1d9bf112c10814fac | yes | 36 |

**Multipart Description/PDF files in .zip description**

| Document Description | Start | End |
|---|---|---|
| Specification | 1 | 30 |
| Claims | 31 | 35 |
| Abstract | 36 | 36 |

| | | | | | |
|---|---|---|---|---|---|
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 3 | Drawings-only black and white line drawings | 2015-09-07_Drawings_NT003C1.pdf | 359514<br>5c592a8b0e2af5e61e657261d00fe08c1f889900 | no | 26 |
| **Warnings:** | | | | | |
| The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing | | | | | |
| **Information:** | | | | | |
| 4 | Fee Worksheet (SB06) | fee-info.pdf | 34931<br>e0ec29fe23a7da9b585f72be325e27971d958515 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 2189948 | | |

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**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

DocCode - SCORE

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Application Number: 14846993 Document Date: 09/07/2015

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Form Revision Date: September 30, 2013

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| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | 2139 | 730 | NT003C1 | 20 | 3 |

**CONFIRMATION NO. 5461**

**FILING RECEIPT**

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000077572394

Date Mailed: 09/23/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**Applicant(s)**

Netlist, Inc., Irvine, CA;

**Power of Attorney:** None

**Domestic Priority data as claimed by applicant**

This application is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

**If Required, Foreign Filing License Granted:** 09/21/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/846,993**

**Projected Publication Date:** 12/31/2015

**Non-Publication Request:** No

**Early Publication Request:** No
**** SMALL ENTITY ****

**Title**

MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

**Preliminary Class**

711

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

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## Title 37, Code of Federal Regulations, 5.11 & 5.15

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 14/846,993 | 09/07/2015 | Hyun Lee | NT003C1 |

**CONFIRMATION NO. 5461**

**FORMALITIES LETTER**

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

*OC000000077572395*

Date Mailed: 09/23/2015

# NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

**FILED UNDER 37 CFR 1.53(b)**

***Filing Date Granted***

**Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

**SUMMARY OF FEES DUE:**

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **70** surcharge.
- $( **0**) previous unapplied payment amount.
- $ **70** TOTAL FEE BALANCE DUE.

**Items Required To Avoid Processing Delays:**

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):

Hyun Lee
Jayesh R. Bhakta

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tlo/

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>14/846,993 |
|---|---|

## APPLICATION AS FILED - PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY FEE($) |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | 70 | | N/A | |
| SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | 300 | | N/A | |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | 360 | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 20 minus 20 = | * | x 40 = | 0.00 | OR | | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 3 minus 3 = | * | x 210 = | 0.00 | | | |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | 0.00 | | | |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | 0.00 | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | 730 | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY ADDITIONAL FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT A | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| AMENDMENT A | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| AMENDMENT A | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| AMENDMENT A | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | OR | RATE($) | ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT B | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| AMENDMENT B | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| AMENDMENT B | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| AMENDMENT B | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

**Courtesy Reminder for**
**Application Serial No: 14/846,993**

Attorney Docket No: NT003C1
Customer Number: 79141
Date of Electronic Notification: 09/23/2015

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
jz@jzpatent.com
eofficeaction@appcoll.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://sportal.uspto.gov/secure/myportal/privatepair.** If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

Customer No. 79141
Attorney Docket No.: NT003US

# COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

| | |
|---|---|
| **Title of Invention** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |

## DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/952,599 filed on July 27, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

## ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid, I hereby sell and assign to

**Netlist, Inc.**
**(Name of Assignee)**

of **51 Discovery, Suite #150, Irvine, CA 92618**
**(Address of Assignee)**

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 10/9/2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date: 10/14/2013



Samsung Electronics Co., Ltd.
Ex. 1011, p. 83

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 14846993 |
| **Filing Date:** | 07-Sep-2015 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Jamie Jie Zheng |
| **Attorney Docket Number:** | NT003C1 |

Filed as Small Entity

**Filing Fees for Utility under 35 USC 111(a)**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| Late Filing Fee for Oath or Declaration | 2051 | 1 | 70 | 70 |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **70** |

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 23698238 |
| **Application Number:** | 14846993 |
| **International Application Number:** | |
| **Confirmation Number:** | 5461 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | NT003C1 |
| **Receipt Date:** | 05-OCT-2015 |
| **Filing Date:** | 07-SEP-2015 |
| **Time Stamp:** | 23:40:13 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Credit Card |
| Payment was successfully received in RAM | $70 |
| RAM confirmation Number | 8142 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Oath or Declaration filed | 2013-10-15_Declaration_Signed_NT003US.pdf | 201957<br>077e7a3e75ea46a46ebcf4c6382d25028cb4b7b3 | no | 2 |
| **Warnings:** | | | | | |
| The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 30645<br>7a21533f164eb34b9cbc1c6cc403eab66c9ee703 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 232602 | | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>14/846,993 |
|---|---|

## APPLICATION AS FILED - PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY FEE($) |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | 70 | | N/A | |
| SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | 300 | | N/A | |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | 360 | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 20 minus 20 = | * | x 40 = | 0.00 | OR | | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 3 minus 3 = | * | x 210 = | 0.00 | | | |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | 0.00 | | | |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | 0.00 | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | 730 | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY ADDITIONAL FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT A | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| AMENDMENT A | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| AMENDMENT A | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| AMENDMENT A | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | OR | RATE($) | ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT B | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| AMENDMENT B | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| AMENDMENT B | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| AMENDMENT B | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | 2111 | 800 | NT003C1 | 20 | 3 |

**CONFIRMATION NO. 5461**

**UPDATED FILING RECEIPT**

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000078049128

Date Mailed: 10/28/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**Applicant(s)**

Netlist, Inc., Irvine, CA;

**Power of Attorney:** None

**Domestic Priority data as claimed by applicant**

This application is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

**If Required, Foreign Filing License Granted:** 09/21/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/846,993**

**Projected Publication Date:** 02/04/2016

**Non-Publication Request:** No

**Early Publication Request:** No
**** SMALL ENTITY ****

**Title**

MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

**Preliminary Class**

710

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

## LICENSE FOR FOREIGN FILING UNDER

## Title 35, United States Code, Section 184

## Title 37, Code of Federal Regulations, 5.11 & 5.15

**GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 14/846,993 | 09/07/2015 | Hyun Lee | NT003C1 |

**CONFIRMATION NO. 5461**

**PUBLICATION NOTICE**

*OC000000080337325*

79141
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

**Title:**MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

**Publication No.**US-2016-0034408-A1
**Publication Date:**02/04/2016

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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| Sheet | 1 | of | 3 |
|---|---|---|---|

| Complete if Known | |
|---|---|
| Application Number | 14/846,993 |
| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

**US PATENT DOCUMENTS**

| Examiner Initials * | Cite No. [1] | Document Number Number-Kind Code [2] (if known) | Publication Date (MM-DD-YYYY) | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
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| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
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| | 6. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016 | |
| | 7. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016 | |
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| | 15. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016 | |
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| | 17. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016 | |

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| | 18. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016 | |
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| | 20. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016 | |
| | 21. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016 | |
| | 22. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016 | |
| | 23. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016 | |
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| | | | | Art Unit | 2111 |
| | | | | Examiner Name | Unknown |
| Sheet | 3 | of | 3 | Attorney Docket Number | NT003C1 |

| NON PATENT LITERATURE DOCUMENTS | | | |
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| | 39. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016 | |
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# Electronic Acknowledgement Receipt

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| **EFS ID:** | 26289746 |
| **Application Number:** | 14846993 |
| **International Application Number:** | |
| **Confirmation Number:** | 5461 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | NT003C1 |
| **Receipt Date:** | 07-JUL-2016 |
| **Filing Date:** | 07-SEP-2015 |
| **Time Stamp:** | 20:22:55 |
| **Application Type:** | Utility under 35 USC 111(a) |

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| 4 | Non Patent Literature | 2016-05-11_Eng_Trans_NGR_NT001KR.pdf | 183171<br>1bd82675735359e2c4e2487f59394991711 6f0f0 | no | 5 |
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# INFORMATION DISCLOSURE STATEMENT

| | | |
|---|---|---|
| Applicant | : | NETLIST, INC. |
| App. No. | : | 14/846,993 |
| Filed | : | September 7, 2015 |
| For | : | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| Examiner | : | UNKNOWN |
| Art Unit | : | 2111 |
| Conf No. | : | 5461 |

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Dear Sir:

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The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

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Respectfully submitted,

Dated: July 7, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
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|---|---|---|---|---|---|---|
| | 5. | WO99/30240 | 06-17-1999 | Intel Corporation | | |

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| | 8. | Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015 | |
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| | 10. | Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 11. | Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015 | |
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|---|---|---|---|
| | 16. | Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015 | |
| | 17. | Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015 | |
| | 18. | Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015 | |
| | 19. | Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015 | |
| | 20. | Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002 | |
| | 21. | Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10 | |
| | 22. | U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages | |
| | 23. | Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411 | |
| | 24. | Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265 | |
| | 25. | Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid | |
| | 26. | Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search | |
| | 27. | Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015 | |
| | 28. | Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015 | |
| | 29. | Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 30. | Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015 | |
| | 31. | Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015 | |
| | 32. | Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015 | |
| | 33. | Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015 | |
| | 34. | Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016 | |

**EXAMINER** **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

| Sheet | 3 | of | 3 |
|---|---|---|---|

| Complete if Known | |
|---|---|
| Application Number | 14/846,993 |
| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | 35. | Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015 | |
| | 36. | Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015 | |
| | 37. | Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015 | |
| | 38. | Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015 | |
| | 39. | Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 40. | Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015 | |
| | 41. | Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015 | |
| | 42. | Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015 | |
| | 43. | Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015 | |
| | 44. | Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016 | |
| | 45. | Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015 | |
| | 46. | Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015 | |

**EXAMINER** **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 26290375 |
| **Application Number:** | 14846993 |
| **International Application Number:** | |
| **Confirmation Number:** | 5461 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | NT003C1 |
| **Receipt Date:** | 08-JUL-2016 |
| **Filing Date:** | 07-SEP-2015 |
| **Time Stamp:** | 00:46:53 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | no |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Transmittal Letter | 2016-07-07_IDS_2_Cover_NT003C1.pdf | 49581<br>649a8994a73a22402fbb1936c2fd31dfb07aa25b | no | 2 |

**Warnings:**

| | | | | | |
|---|---|---|---|---|---|
| **Information:** | | | | | |
| 2 | Information Disclosure Statement (IDS) Form (SB08) | 2016-07-07_IDS_2_NETL003C1.pdf | 94385<br>a2edf1db77bc852ae4b74f0486a1fe5e29bfa0bc | no | 3 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| This is not an USPTO supplied IDS fillable form | | | | | |
| 3 | Non Patent Literature | 2015-11-23_NFOA_NETL048CPC1.pdf | 4155462<br>35b8c4f3b724d8b3e3f65fa2a1c1257016dabb25 | no | 79 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 4 | Non Patent Literature | 2016-03-23_Rsps_NFOA_NETL048CPC1.pdf | 118678<br>0f3c0dba6a043802851f4422a0b58d52f88e9d5a | no | 9 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | | **Total Files Size (in bytes):** | 4418106 | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**<u>New Applications Under 35 U.S.C. 111</u>**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**<u>National Stage of an International Application under 35 U.S.C. 371</u>**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**<u>New International Application Filed with the USPTO as a Receiving Office</u>**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

# INFORMATION DISCLOSURE STATEMENT

| | | |
|---|---|---|
| Applicant | : | NETLIST, INC. |
| App. No. | : | 14/846,993 |
| Filed | : | September 7, 2015 |
| For | : | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| Examiner | : | UNKNOWN |
| Art Unit | : | 2111 |
| Conf No. | : | 5461 |

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 46 references. Copies of some of the foreign documents and/or their translation and non-patent literature are submitted herewith. Copies of the rest of the foreign documents and/or their translation and non-patent literature have been submitted in commonly-owned U.S. Pat. Appl. No. 14/715,486 (filed May 18, 2015) on February 21, 2016, which is accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: July 7, 2016

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828



Samsung Electronics Co., Ltd.
Ex. 1011, p. 106

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

# NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 09/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

| EXAMINER |
|---|
| SUN, MICHAEL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

DATE MAILED: 09/23/2016

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | Hyun Lee | NT003C1 | 5461 |

TITLE OF INVENTION: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | SMALL | $480 | $0 | $0 | $480 | 12/23/2016 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**



PTOL-85 (Rev. 02/11)

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## PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** **Mail Stop ISSUE FEE**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, Virginia 22313-1450**
**or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

| |
|---|
| (Depositor's name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | Hyun Lee | NT003C1 | 5461 |

TITLE OF INVENTION: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | SMALL | $480 | $0 | $0 | $480 | 12/23/2016 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| SUN, MICHAEL | 2184 | 710-005000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Ex. 1011, p. 108

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | Hyun Lee | NT003C1 | 5461 |

79141 7590 09/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

| EXAMINER |
|---|
| SUN, MICHAEL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

DATE MAILED: 09/23/2016

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.



PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
Ex. 1011, p. 109

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

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The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| Notice of Allowability | Application No. 14/846,993 | Applicant(s) LEE ET AL. | |
|---|---|---|---|
| | Examiner MICHAEL SUN | Art Unit 2184 | AIA (First Inventor to File) Status No |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's Continuation filed 9/07/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   **Certified copies:**

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/07/2016; 7/08/2016
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184



Samsung Electronics Co., Ltd.
Ex. 1011, p. 111

The present application is being examined under the pre-AIA first to invent provisions.

## DETAILED ACTION

### Status of the Application

This Office Action is in response to Applicant's Continuation filed 9/07/2015.

Claims 1-20 are pending for this examination.

### Information Disclosure Statement

The information disclosure statement (IDS) submitted on 7/07/2016; and 7/08/2016 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Examiner points out that in both of the filed IDSes, many of the NPL references were not considered as Examiner could not find a copy of the cited references included in the case, the parent case, or the relevant cases, and as such without a copy of the NPL references, Examiner is unable to consider such references.

### Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however,

the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims. Applicant argues these limitations on Pages 7-11 of Applicant's Remarks filed 12/31/2014 of parent application 13/952,599. These limitations find support in Applicant's Specification on Pages 6-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

**Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Sun whose telephone number is 571-270-1724. The examiner can normally be reached on Mondays to Thursdays from 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai, can be reached at (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

| Notice of References Cited | Application/Control No. 14/846,993 | Applicant(s)/Patent Under Reexamination LEE ET AL. | |
|---|---|---|---|
| | Examiner MICHAEL SUN | Art Unit 2184 | Page 1 of 1 |

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| * | B | US-2006/0077731 A1 | 04-2006 | Ware; Frederick A. | G11C5/04 | 365/194 |
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| * | E | US-8,214,616 B2 | 07-2012 | Ware; Frederick A. | G06F13/1684 | 711/104 |
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| * | G | US-2002/0039323 A1 | 04-2002 | Tokutome, Hiroto | G11C7/1066 | 365/233.12 |
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| | J | US- | | | | |
| | K | US- | | | | |
| | L | US- | | | | |
| | M | US- | | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | CPC Classification |
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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

| Sheet | 1 | of | 3 |
|---|---|---|---|

| Complete if Known | |
|---|---|
| Application Number | 14/846,993 |
| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

**US PATENT DOCUMENTS**

| Examiner Initials * | Cite No. [1] | Document Number Number-Kind Code [2] (if known) | Publication Date (MM-DD-YYYY) | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| /M.S./ | 1. | 2002/0038405 A1 | 03-28-2002 | Leddige, M. et al. | |
| /M.S./ | 2. | 2009/0296503 A1 | 12-03-2009 | Chu, M. et al. | |
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| /M.S./ | 4. | 2008/0162790 A1 | 07-03-2008 | IM | |

**NON PATENT LITERATURE DOCUMENTS**

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | 5. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015 | |
| | 6. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016 | |
| | 7. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016 | |
| | 8. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016 | |
| | 9. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016 | |
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| | 11. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016 | |
| | 12. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016 | |
| | 13. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016 | |
| | 14. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016 | |
| | 15. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016 | |
| | 16. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016 | |
| | 17. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016 | |

**EXAMINER** /Michael Sun/ **DATE CONSIDERED** 09/18/2016

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**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**
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| Sheet | 2 | of | 3 |
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| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

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|---|---|---|---|
| | 18. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016 | |
| | 19. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016 | |
| | 20. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016 | |
| | 21. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016 | |
| | 22. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016 | |
| | 23. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016 | |
| | 24. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016 | |
| | 25. | Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016 | |
| | 26. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016 | |
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| | 33. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016 | |
| | 34. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016 | |

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| | 35. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016 | |
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| | 39. | Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016 | |
| | 40 | International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014 | |
| | 41. | Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015. | |
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| | 44. | Examination Report, European Patent Application No. 10730021.2, dated April 14, 2014. | |
| | 45. | Response to Examination Report, European Patent Application No. 10730021.2, dated June 4, 2014. | |
| | 46. | Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015. | |
| /M.S./ | 47. | Response to Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015, filed November 4, 2015. | |
| /M.S./ | 48. | English Translation of the Notice of Grounds for Rejection, Korean Patent Application No. 2012-7004038, dated May 11, 2016 | |
| /M.S./ | 49. | Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016 | |

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# BIB DATA SHEET

**CONFIRMATION NO. 5461**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 14/846,993 | 09/07/2015<br>**RULE** | 710 | 2184 | NT003C1 |

**APPLICANTS**
Netlist, Inc., Irvine, CA;

**INVENTORS**
Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************
This application is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**** FOREIGN APPLICATIONS ****************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
09/21/2015

| Foreign Priority claimed | ❑ Yes ☑ No | | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|
| 35 USC 119(a-d) conditions met | ❑ Yes ☑ No | ❑ Met after Allowance | | | | |
| Verified and Acknowledged | /MICHAEL SUN/<br>Examiner's Signature | Initials | CA | 26 | 20 | 3 |

**ADDRESS**
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306
UNITED STATES

**TITLE**
MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

| FILING FEE RECEIVED | | |
|---|---|---|
| 800 | FEES: Authority has been given in Paper<br>No._____ to charge/credit DEPOSIT ACCOUNT<br>No._____ for following: | ❑ All Fees<br>❑ 1.16 Fees (Filing)<br>❑ 1.17 Fees (Processing Ext. of time)<br>❑ 1.18 Fees (Issue)<br>❑ Other _____<br>❑ Credit |

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| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

## US PATENT DOCUMENTS

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|---|---|---|---|---|---|
| /M.S./ | 1. | 6381140 | 04-30-2002 | Liao, Sheng-Chi | |
| /M.S./ | 2. | 7254036 | 08-07-2007 | Pauley et al. | |
| /M.S./ | 3. | 20090248969 | 10-01-2009 | Wu; Larry | |
| /M.S./ | 4. | 20100125681 | 05-20-2010 | Patel; Shwetal A. | |

## FOREIGN PATENT DOCUMENTS

| Examiner Initials * | Cite No. [1] | Foreign Patent Document | Publication Date (MM-DD-YYYY) | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T[6] |
|---|---|---|---|---|---|---|
| | 5. | WO99/30240 | 06-17-1999 | Intel Corporation | | |

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| /M.S./ | 6. | Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015 | |
| /M.S./ | 7. | Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016 | |
| | 8. | Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015 | |
| | 9. | Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015 | |
| | 10. | Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 11. | Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015 | |
| | 12. | Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015 | |
| | 13. | Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015 | |
| | 14. | Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015 | |
| | 15. | Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016 | |

**EXAMINER** /Michael Sun/ **DATE CONSIDERED** 09/18/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

| Sheet | 2 | of | 3 |
|---|---|---|---|

| Complete if Known | |
|---|---|
| Application Number | 14/846,993 |
| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | 16. | Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015 | |
| | 17. | Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration, filed June 19,2015 | |
| | 18. | Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015 | |
| | 19. | Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015 | |
| | 20. | Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002 | |
| | 21. | Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10 | |
| | 22. | U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages | |
| | 23. | Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411 | |
| | 24. | Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265 | |
| | 25. | Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid | |
| | 26. | Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search | |
| | 27. | Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015 | |
| | 28. | Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015 | |
| | 29. | Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 30. | Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015 | |
| | 31. | Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015 | |
| | 32. | Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015 | |
| | 33. | Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015 | |
| | 34. | Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016 | |

**EXAMINER** /Michael Sun/ **DATE CONSIDERED** 09/18/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

| Sheet | 3 | of | 3 |
|---|---|---|---|

| Complete if Known | |
|---|---|
| Application Number | 14/846,993 |
| Filing Date | September 7, 2015 |
| First Named Inventor | Hyun Lee |
| Art Unit | 2111 |
| Examiner Name | Unknown |
| Attorney Docket Number | NT003C1 |

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | 35. | Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015 | |
| | 36. | Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015 | |
| | 37. | Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015 | |
| | 38. | Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015 | |
| | 39. | Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015 | |
| | 40. | Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015 | |
| | 41. | Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015 | |
| | 42. | Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015 | |
| | 43. | Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015 | |
| | 44. | Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016 | |
| | 45. | Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015 | |
| | 46. | Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015 | |

**EXAMINER** /Michael Sun/ **DATE CONSIDERED** 09/18/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14846993 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

| CPC | | | | | |
|---|---|---|---|---|---|
| **Symbol** | | | | **Type** | **Version** |
| G06F | | 13 | / 28 | F | 2013-01-01 |
| G06F | | 3 | / 0659 | I | 2013-01-01 |
| G11C | | 16 | / 00 | I | 2013-01-01 |
| G11C | | 5 | / 04 | I | 2013-01-01 |
| G11C | | 7 | / 1006 | I | 2013-01-01 |
| G11C | | 7 | / 1066 | I | 2013-01-01 |
| G11C | | 7 | / 109 | A | 2013-01-01 |
| G11C | | 7 | / 1093 | I | 2013-01-01 |
| G11C | | 8 | / 12 | A | 2013-01-01 |
| G06F | | 1 | / 10 | I | 2013-01-01 |
| G06F | | 3 | / 0613 | I | 2013-01-01 |
| G06F | | 3 | / 0647 | I | 2013-01-01 |
| G06F | | 3 | / 0683 | I | 2013-01-01 |
| G06F | | 13 | / 4027 | I | 2013-01-01 |
| | | | / | | |

| CPC Combination Sets | | | | | | | |
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| **Symbol** | | | | **Type** | **Set** | **Ranking** | **Version** |
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| | | | |
|---|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br>20 | |
| /MICHAEL SUN/<br>Primary Examiner.Art Unit 2184<br><br>(Primary Examiner) | 09/18/2016<br><br>(Date) | O.G. Print Claim(s)<br>1 | O.G. Print Figure<br>1 |

U.S. Patent and Trademark Office

Part of Paper No. 20160918

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14846993 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

| US ORIGINAL CLASSIFICATION | | INTERNATIONAL CLASSIFICATION | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLASS | SUBCLASS | CLAIMED | | | | | NON-CLAIMED | | | | | |
| 710 | 5 | G | 0 | 6 | F | 3 / 00 (2006.01.01) | | | | | | |
| CROSS REFERENCE(S) | | G | 0 | 6 | F | 12 / 00 (2006.01.01) | | | | | | |
| | | G | 0 | 6 | F | 13 / 00 (2006.01.01) | | | | | | |

| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
|---|---|---|---|---|---|
| 710 | 6 | 7 | | | |
| 711 | 1 | 2 | 3 | 4 | 154 |
| 711 | 155 | | | | |

| | | | |
|---|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br>20 | |
| /MICHAEL SUN/<br>Primary Examiner.Art Unit 2184<br><br>(Primary Examiner) | 09/18/2016<br><br>(Date) | O.G. Print Claim(s)<br>1 | O.G. Print Figure<br>1 |

U.S. Patent and Trademark Office

Part of Paper No. 20160918

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14846993 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
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| 2 | 2 | 18 | 18 | | | | | | | | | | | | |
| 3 | 3 | 19 | 19 | | | | | | | | | | | | |
| 4 | 4 | 20 | 20 | | | | | | | | | | | | |
| 5 | 5 | | | | | | | | | | | | | | |
| 6 | 6 | | | | | | | | | | | | | | |
| 7 | 7 | | | | | | | | | | | | | | |
| 8 | 8 | | | | | | | | | | | | | | |
| 9 | 9 | | | | | | | | | | | | | | |
| 10 | 10 | | | | | | | | | | | | | | |
| 11 | 11 | | | | | | | | | | | | | | |
| 12 | 12 | | | | | | | | | | | | | | |
| 13 | 13 | | | | | | | | | | | | | | |
| 14 | 14 | | | | | | | | | | | | | | |
| 15 | 15 | | | | | | | | | | | | | | |
| 16 | 16 | | | | | | | | | | | | | | |

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|---|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br>20 | |
| /MICHAEL SUN/<br>Primary Examiner.Art Unit 2184<br><br>(Primary Examiner) | 09/18/2016<br><br>(Date) | O.G. Print Claim(s)<br>1 | O.G. Print Figure<br>1 |

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S92 | 4621 | memory module and timing signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S93 | 1897 | S92 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S94 | 197 | S93 and operating speed | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S95 | 60 | S94 AND ( (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC. ) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S96 | 60 | S95 and buffer | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S97 | 60 | S96 and ((data or strobe) near2 signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S98 | 60 | S97 and (read or write) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S99 | 32 | S98 and memory bus | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S100 | 5 | S99 and command signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S101 | 4164 | (lee, hyun).in. | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S102 | 103 | (bhakta, jayesh).in. | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S103 | 523452 | buffer and memory and (data or strobe) and (read or write) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |

| | | | | | | |
|---|---|---|---|---|---|---|
| S104 | 52122 | S103 and ((determin$5 or calculat$3) with (time interval or delay)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S105 | 112 | S103 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S106 | 41 | S105 and (transmi$5 with (time interval or delay)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:48 |
| S107 | 691 | (determining or calculating) with (time interval or delay) with (first signal) with (second signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:49 |
| S108 | 1 | S107 and memory controller and buffer and memory bus | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:49 |
| S109 | 4929 | memory module and buffer and memory device and memory controller and control signal and command | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S110 | 912 | S109 and system clock | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S111 | 31 | S110 and (write with (different near4 time)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S112 | 5 | S111 and (align$4 with read) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S113 | 161889 | (deriving or timing or calculating) with (delay or latency) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S114 | 1921 | S113 and read and write and strobe and memory module and controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S115 | 1590 | S114 and buffer | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S116 | 1563 | S115 and ((data or strobe) near4 signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S117 | 300 | S116 and (timing with transmission) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 09:50 |
| S118 | 55 | S117 and (timing with transmission with read) with write | US-PGPUB; USPAT; USOCR; EPO; DERWENT; | ADJ | ON | 2016/09/18 09:50 |

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|---|---|---|---|---|---|---|
| | | | IBM_TDB | | | |
| S119 | 7282 | memory module and buffer and tim$3 and (control signal or address signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 12:59 |
| S120 | 1550 | S119 and time interval | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 12:59 |
| S121 | 1183 | S120 and delay | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 12:59 |
| S122 | 334 | S121 and (strobe signal and data signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 12:59 |
| S123 | 7 | S122 and (time interval with (first signal and second signal)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 13:00 |
| S124 | 7 | S123 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 13:02 |
| S125 | 4 | S124 and time transmission | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2016/09/18 13:02 |
| S126 | 390 | memory module and buffer and (control signal and address signal and data signal and strobe signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:02 |
| S127 | 286 | S126 and delay | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:03 |
| S128 | 141 | S127 and time interval | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:03 |
| S129 | 122 | S128 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:03 |
| S130 | 40 | S129 and tim$3 transmission | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:03 |
| S131 | 10 | S130 and first signal and second signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2016/09/18 13:03 |

**EAST Search History (Interference)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| S132 | 4298 | ((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC. ) and (memory).clm. and (buffer).clm. | US-PGPUB; USPAT | ADJ | ON | 2016/09/18 13:07 |
| S133 | 378 | S132 and (delay or time interval).clm. | US-PGPUB; USPAT | ADJ | ON | 2016/09/18 13:07 |
| S134 | 250 | S133 and (read or write).clm. | US-PGPUB; USPAT | ADJ | ON | 2016/09/18 13:07 |
| S135 | 3 | S134 and (time transmitting or time transmission).clm. | US-PGPUB; USPAT | ADJ | ON | 2016/09/18 13:07 |

**9/ 18/ 2016 1:17:34 PM**
**C:\ Users\ msun\ Documents\ EAST\ Workspaces\ 14846993.wsp**

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14846993 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

## CPC- SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| limited search of G06F 1/12 | 9/18/2016 | MS |
| limited search of G06F 13/1689 | 9/18/2016 | MS |
| limited search of G06F 12/0246 | 9/18/2016 | MS |
| limited search of G06F 13/1694 | 9/18/2016 | MS |

## CPC COMBINATION SETS - SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| | | |

## US CLASSIFICATION SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| | | | |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| EAST Search - see attached | 9/18/2016 | MS |
| Inventor Search - see attached EAST Search | 9/18/2016 | MS |
| limited EAST Search of class/subclasses 710/5, 6, and 7 | 9/18/2016 | MS |
| limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155 | 9/18/2016 | MS |
| Google Scholar Search - search terms used: (buffered memory module); (memory module with buffer); (memory module with buffers that time signal transmissions and delays espective to each individual buffer)v | 9/18/2016 | MS |

## INTERFERENCE SEARCH

| US Class/ CPC Symbol | US Subclass / CPC Group | Date | Examiner |
|---|---|---|---|
| 710 | limited search of subclasses 5, 6, and 7 | 9/18/2016 | MS |
| 711 | limited search of subclasses 1, 2, 3, 4, 154, and 155 | 9/18/2016 | MS |
| G06F | limited search of 1/12, 13/1689, 12/0246, and 13/1694 | 9/18/2016 | MS |

| | |
|---|---|
| | /MICHAEL SUN/<br>Primary Examiner, Art Unit 2184 |

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14846993 | 09/07/2015 | Hyun Lee | NT003C1 | 5461 |

TITLE OF INVENTION:

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | undiscounted | $960 | $0 | $0 | $960 | 12/23/2016 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| | | |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 JAMIE J. ZHENG, Ph.D, Esq.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ■ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-5963 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jamie J. Zheng/ Date December 23, 2016

Typed or printed name Jamie J. Zheng Registration No. 51,167

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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## Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 14846993 |
| **Filing Date:** | 07-Sep-2015 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Jamie Jie Zheng |
| **Attorney Docket Number:** | NT003C1 |

Filed as Large Entity

**Filing Fees for Utility under 35 USC 111(a)**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| UTILITY APPL ISSUE FEE | 1501 | 1 | 960 | 960 |
| PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL | 1504 | 1 | 0 | 0 |
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | | **Total in USD ($)** | **960** |

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 27889257 |
| **Application Number:** | 14846993 |
| **International Application Number:** | |
| **Confirmation Number:** | 5461 |
| **Title of Invention:** | MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | NT003C1 |
| **Receipt Date:** | 23-DEC-2016 |
| **Filing Date:** | 07-SEP-2015 |
| **Time Stamp:** | 02:42:45 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | CARD |
| Payment was successfully received in RAM | $960 |
| RAM confirmation Number | 122316INTEFSW02450000 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Issue Fee Payment (PTO-85B) | 2016-12-23_Issue_Fee_Transmittal_NT003C1.pdf | 74606<br>97ebbb95e2048604fbdeb2a8140c844ca8e0661a | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 32321<br>605e6aa91670f7239560a26e3c625c84da6dd6b5 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 106927 | | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

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| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/846,993 | 02/07/2017 | 9563587 | NT003C1 | 5461 |

79141 7590 01/18/2017
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

# ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Netlist, Inc., Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

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IR103 (Rev. 10/09)

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**UNITED STATES DEPARTMENT OF COMMERCE**
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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY.DOCKET NO./TITLE | REQUEST ID |
|---|---|---|---|---|
| 14/846,993 | 09/07/2015 | Netlist, Inc. | 129980-5047US | 67123 |

## Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/06/2018 has been accepted.

**CERTIFICATIONS:**

**Change of Entity Status:**

X Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

**This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).**

| | |
|---|---|
| **Signature:** | /Jamie J. Zheng/ |
| **Name:** | Jamie J. Zheng |
| **Registration Number:** | 51167 |