UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC.,
and SK HYNIX MEMORY SOLUTIONS INC.
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

U.S. Patent No. 9,128,632

Inter Partes Review No. IPR2017-00730

PATENT OWNER'S PRELIMINARY RESPONSE

la-1347448

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

II. BACKGROUND 2

III. THE ’632 PATENT 2

IV. THE ASSERTED PRIOR ART REFERENCES 5

A. Saito 6

B. Swain 21

C. Kim 22

V. CLAIM CONSTRUCTION 22

VI. RESPONSE TO GROUNDS OF CHALLENGE 23

A. Ground A – Saito In View Of Swain Fails To Render Obvious Claims 1-5, 12-14, 19 And 20 23

1. Independent Claim 1 23

2. Dependent Claim 5 47

3. Independent Claim 12 51

B. Ground B – Saito In View Of Swain and Kim Fails To Render Obvious Claims 3, 13 And 14 53

VII. THE PATENT OWNER’S FINAL COMMENTS 53

VIII. CONCLUSION 54

Exhibit List for Inter Partes Review of U.S. Patent No. 9,128,632

Exhibit Description	Exhibit #
Hewlett-Packard, "DDR3 memory technology," Technology brief, 3rd edition (April 2012). ("HP")	2001
Cooper-Balis, Elliott. *BUFFER-ON-BOARD MEMORY SYSTEM*. (Doctoral dissertation). University of Maryland, 2012. Retrieved from https://www.ece.umd.edu/~blj/papers/thesis-PhD-ecc--BOB.pdf on April 29, 2017. ("Cooper-Balis")	2002

I. INTRODUCTION

On January 20, 2017, SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. (collectively, "Hynix" or "Petitioner") submitted a Petition to institute *inter partes* review of U.S. Patent No. 9,128,632 (the "'632 Patent"), and the Petition was accompanied by an expert declaration by Dr. Trevor Mudge (Ex. 1003, "Mudge Declaration" or "Mudge Decl."). Netlist, Inc. ("Patent Owner") submits this Preliminary Response in response to the Petition.

The Board should deny Hynix's Petition. The proposed combination of Saito and Swain, in all of the grounds proposed in the Petition, relies on a deficient mapping. In particular, neither Saito nor Swain supports the Petitioner's attempt to link the Petition's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") and Petitioner's "memory write operation" (write leveling operation in the Saito-Swain combination) as required by claim 1. These distinct techniques are not linked, as evidenced by teachings in Saito itself and the state-of-the-art disclosures referenced herein. Indeed, as discussed below, the Petitioner relies on sleight-of-hand to create such a non-existent link.

Additionally, the Petition's proposed combination of Saito and Swain is deficient because the Petition's obviousness rationales are inapplicable to the proposed combination and are undercut by the actual disclosures of Saito and Swain.

Moreover, the Petition entirely fails to address certain claimed details recited in claims 5 and 12.

Accordingly, the Patent Owner respectfully requests that the Board deny *inter partes* review. 35 U.S.C. § 314(a).

II. BACKGROUND

Netlist was founded in 2000 by Chuck Hong, Christopher Lopes and Jay Bhakta (one of the named inventors on the ’632 Patent). As a result of their efforts over the past seventeen years, Netlist has become widely regarded as a pioneer in high-performance memory for servers and storage systems, with many of its innovative products being adopted by its primary customers IBM, HP and Dell.

III. THE ’632 PATENT

The Petition challenges independent claims 1 and 12 of the ’632 Patent, and their respective dependent claims 2-5, 13, 14, 19 and 20. Claim 1 is directed to a “memory module,” and claim 12 is directed to a “buffer circuit for use in a memory module.”

Claim 1 discloses that its “memory module” is “to operate in a memory system with a memory controller.” Fig. 1 below illustrates an exemplary memory module 110 in a memory system 100 with a memory controller (MCH) 101.

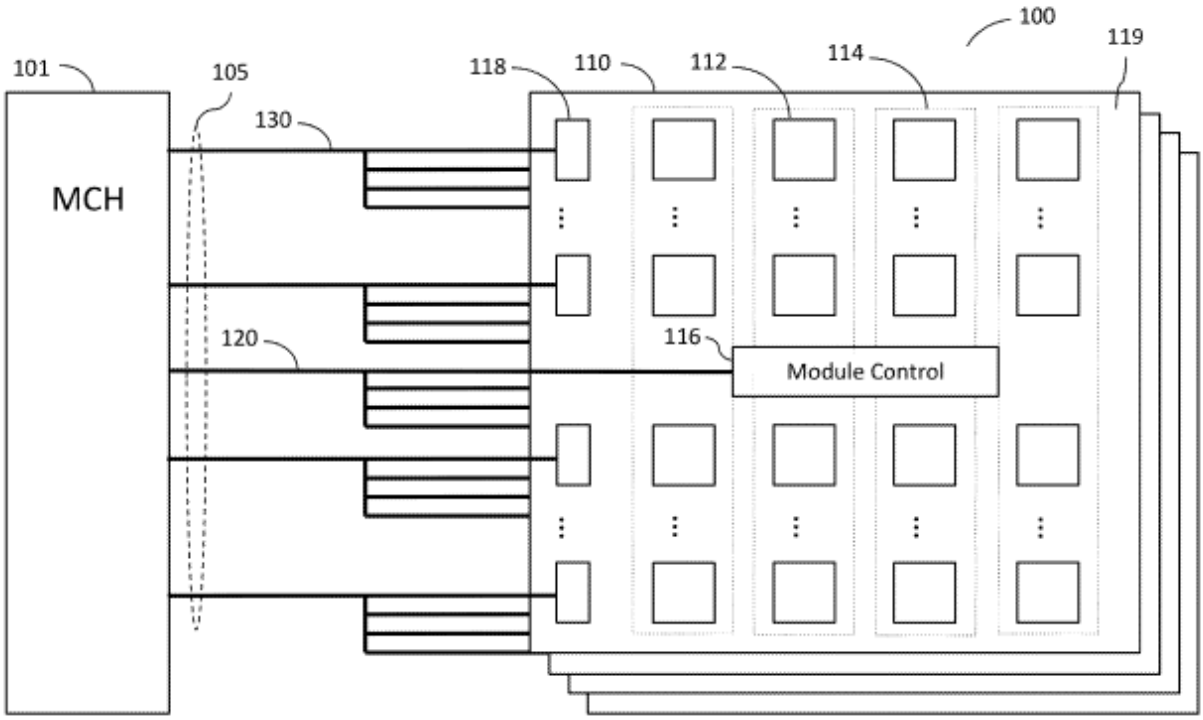


FIG. 1

Claim 1 further discloses its "memory module comprising: a module control device . . . ; memory devices organized in groups . . . ; a plurality of buffer circuits . . ." and "wherein" clauses with additional operational details. Fig. 2A below illustrates an exemplary memory module 110 comprising module control device 116, memory devices 112 organized in groups and a plurality of buffer circuits or isolation devices 118.

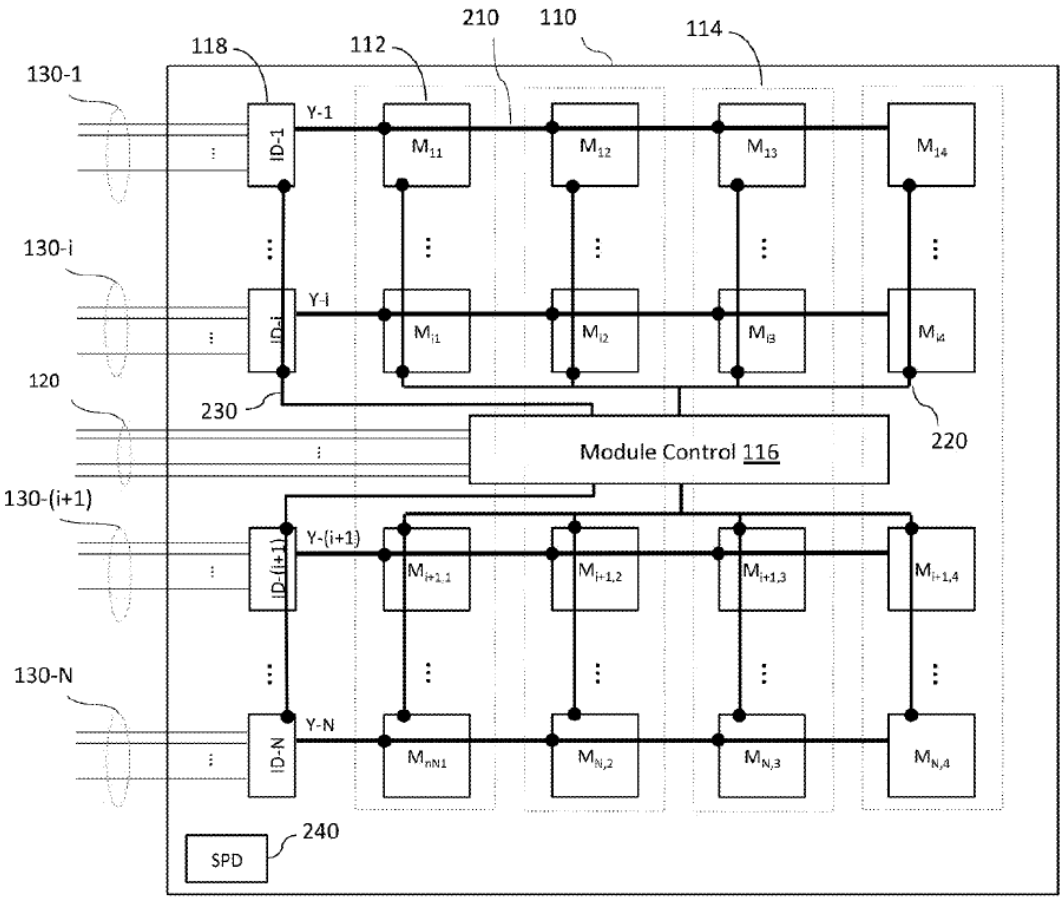


FIG. 2A

Claim 12 discloses that its "buffer circuit" is "for use in a memory module coupled to a memory controller via a memory bus." For example, Fig. 1 above illustrates an exemplary buffer circuit or isolation device 118 for use in a memory module 110 coupled to memory controller (MCH) 101 via memory bus 105.

Claim 12 further discloses its "buffer circuit . . . comprising: a time interval determination circuit . . . ; and a delay circuit . . . ." Fig. 3 below illustrates an exemplary buffer circuit or isolation device 118.

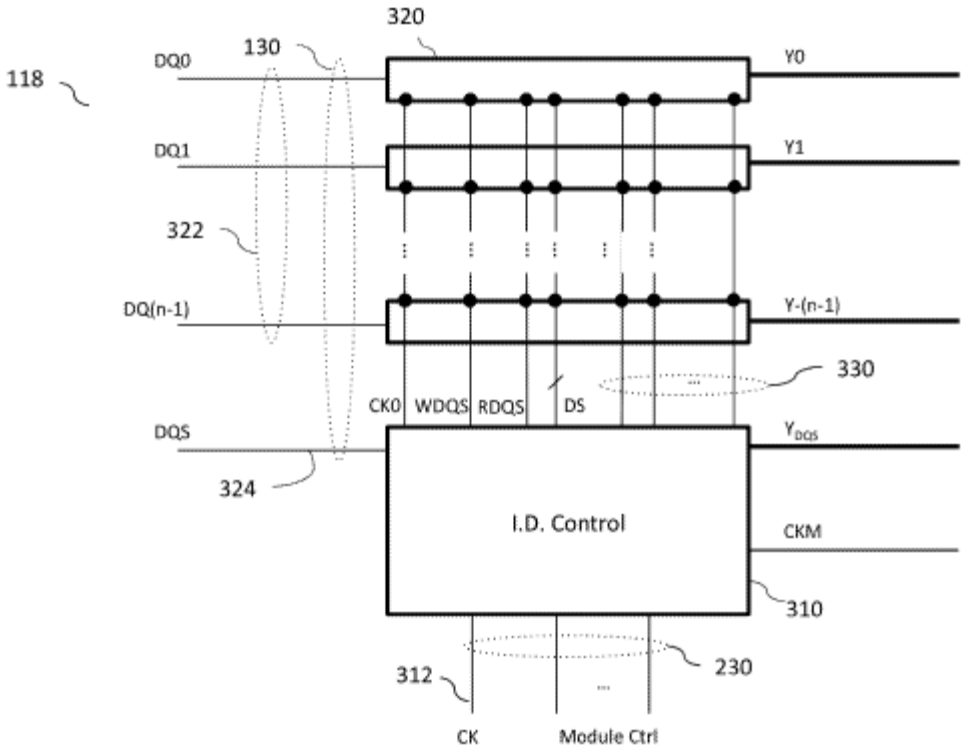


FIG. 3

Further details of an exemplary buffer circuit 118 are shown in Figs. 3, 6 and 13-17.

IV. THE ASSERTED PRIOR ART REFERENCES

The Petitioner challenges claims 1-5, 12-14, 19 and 20 of the ’632 Patent by relying on U.S. Patent Application Publication No. 2010/0309706 to Saito et al. (“Saito”) as well as secondary references U.S. Patent No. 7,808,849 to Swain et al. (“Swain”) and U.S. Patent No. 6,184,701 to Kim et al. (“Kim”).

A. Saito

Saito discloses a memory module architecture "in which a considerably high data transfer rate can be realized." (Ex. 1005, Saito, ¶ [0009].) Saito purportedly achieves this goal by including "a plurality of data register buffers" and "a command/address/control register buffer" on the memory module. (*Id.*, ¶ [0012].) Introducing the register buffers and shortening line lengths reduces the load capacity of the signal paths between the memory controller and the memory chips on the memory module to improve signal quality even at high data transfer rates. (*Id*., ¶¶ [0012], [0055], [0068].)

To understand Saito's place in the developmental history of memory module technology, helpful points of reference may be found in double data rate type three SDRAM (DDR3 SDRAM) technology and Load Reduced DIMM (LRDIMM) technology. (*See*, *e.g.*, Ex. 2001, HP, 3-4; Ex. 2002, Cooper-Balis, 12-14.)

Fig. 3 of Saito, reproduced and annotated by the Patent Owner below, illustrates a memory system in which Saito's memory module can be used.

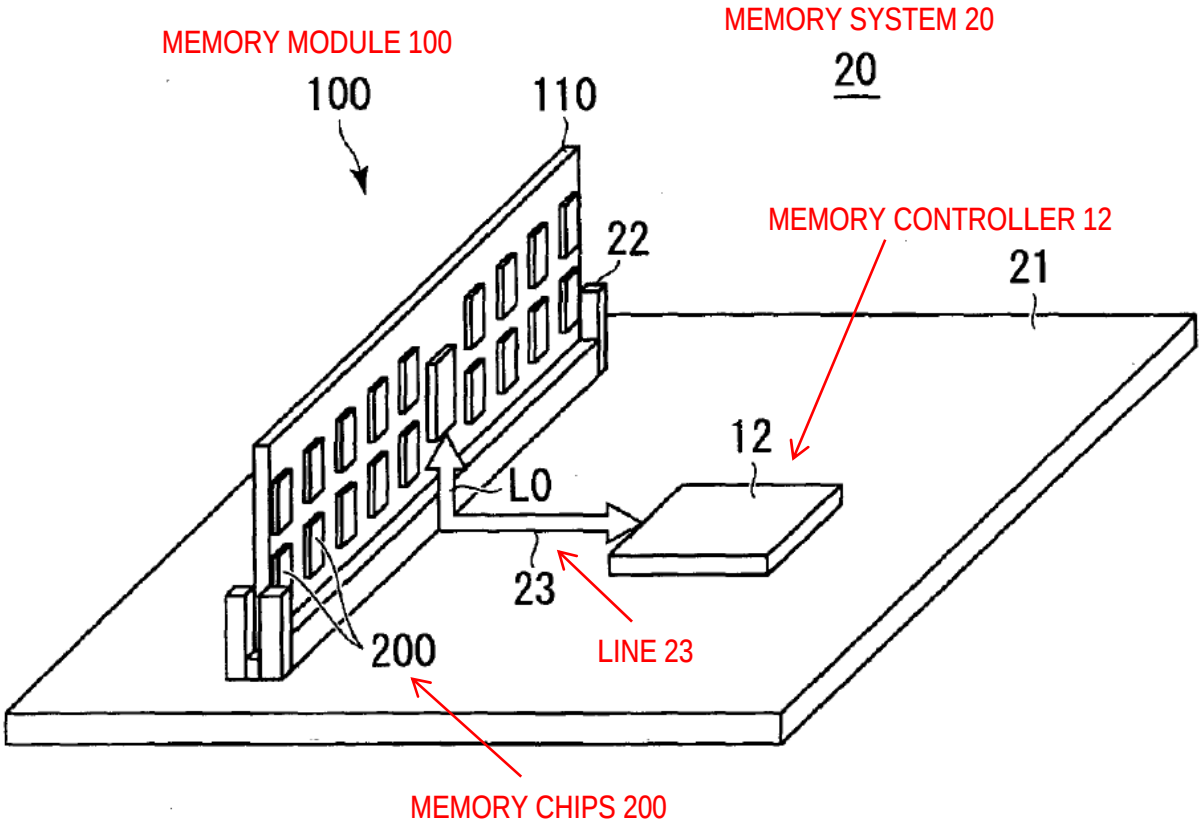


FIG.3

As illustrated in Fig. 3, memory system 20 can include a memory controller 12 and a memory module 100 inserted into memory slot 22. The memory controller 12 and memory module 100 communicate via data and command/address/control lines provided via a signal path (Line 23) between the memory controller 12 and memory module 100. (Ex. 1005, Saito, ¶ [0068].) Without including data register buffers and a command/address/control buffer, the memory controller 12 experiences the load capacitance of all of memory chips 200, preventing a high data transfer rate. (*Id.*)

Fig. 7 of Saito, which depicts a memory module that includes the plurality of data register buffers and a command/address control register buffer and is representative of Saito's operation, is reproduced and annotated by the Patent Owner, below.

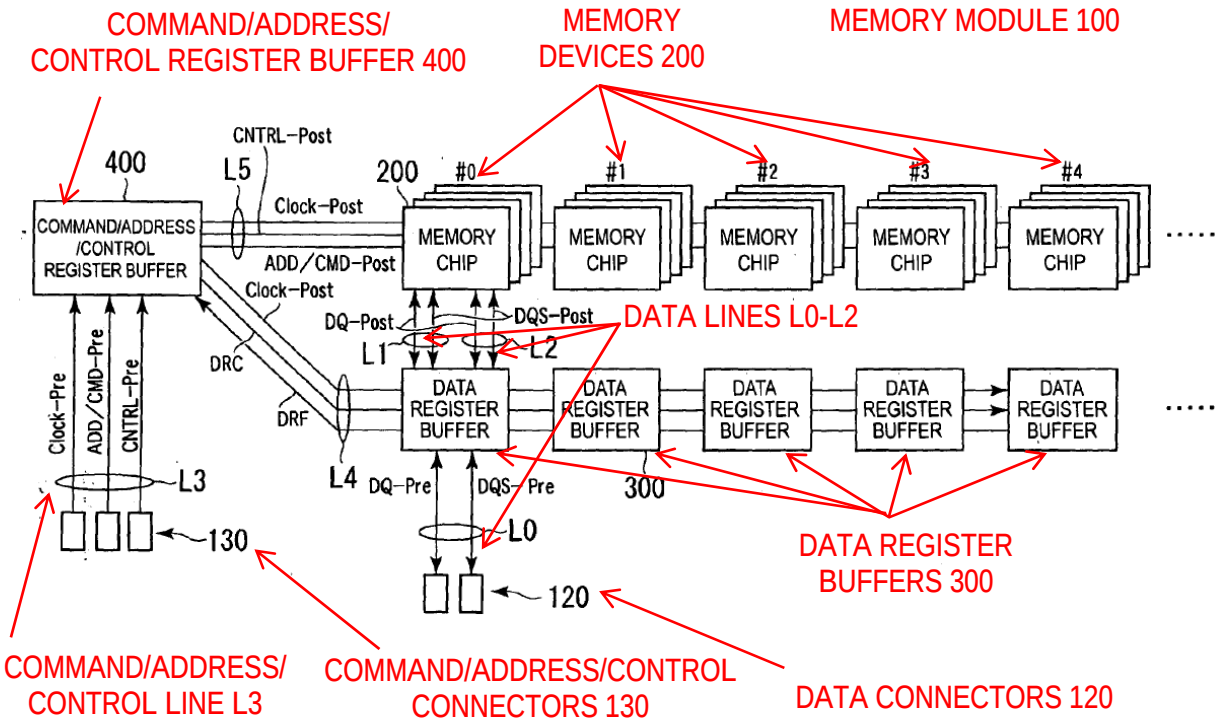


FIG.7

The memory module 100 includes a plurality of memory chips 200 arranged in 4-Rank configuration, a plurality of data register buffers 300, and a command/address/control register buffer 400. (*Id.*, ¶¶ [0044], [0049].) Data connectors 120 are connectors for exchanging write data and read data read between the memory module 100 and the off-module memory controller. (*Id.*, ¶ [0046].) The command/address/control connectors 130 are

connectors for supplying a command signal, an address signal, a control signal, and a clock signal from the off-module memory controller to the command/address/control register buffer 400. (*Id*., ¶ [0047].)

As shown in FIG. 7, the data register buffers 300 intervene between the data connectors 120 and the memory chips 200. (*Id*., ¶ [0100].) The data connectors 120 and each of the data register buffers 300 are connected via data line L0, and each of the data register buffers 300 and the corresponding memory chips 200 are connected to each other via data lines L1 or L2. (*Id*.) Data lines L0-L2 transfer data and data strobe signals between the memory controller, data register buffers 300 and memory chips 200.

Also, as shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected via the command/address/control line L3. (*Id*., ¶ [0103].) The command/address/control register buffer 400 and each of the data register buffers 300 are connected via control line L4. (*Id*.) The command/address/control register buffer 400 and the memory chips 200 are connected via a command/address/control line L5. (*Id*.)

During operation, a command/address/control signal, a control signal and a clock signal can be transferred via command/address/control line L3 from the memory controller and supplied to command/address/control register buffer 400. ((*Id*., ¶ [0052].) The command/address/control register buffer 400 buffers the

signals to the memory chips 200 and generates a control signal and clock to be supplied to data register buffers 300. (*Id*., ¶¶ [0058]-[0059].) The control signal and clock can be used to control read and write operations between the memory controller and the memory chips 200 via data register buffers 300. (*Id*., ¶ [0085].)

The placement of the data register buffer between the memory chips 200 and the memory controller affects the timing of memory read and write operations. (*Id*., ¶ [0101].) In relation to the timing for the data register buffer, Saito requires two read leveling timing adjustments and two separate write leveling timing adjustments be performed during initializing operations (before read and write operations). (*Id*., ¶ [0101].) The read leveling operations and write leveling operations are performed during an initialization operation before read and write operations. (*Id*., Fig. 13, steps S4 and S5 (reproduced below).) During initialization step S4, a read leveling operation and a write leveling operation for interface between the memory chips 200 and the data register buffers 300 are performed. (*Id*., ¶¶ [0140]-[0149].) The write and read leveling operations between a data register buffer 300 and a memory chip 200 are referred to herein as "S4-Write Leveling" and "S4-Read Leveling."

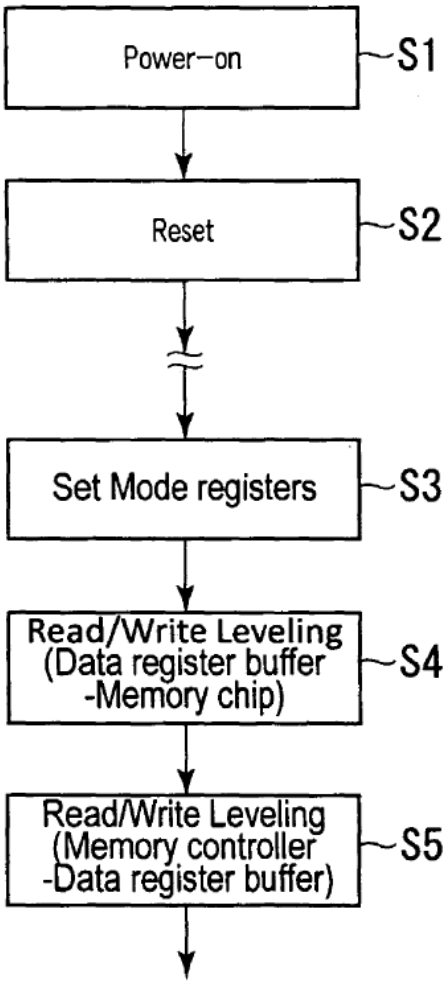


FIG.13

Additionally, during initialization step S5, a read leveling operation and a write leveling operation for the interface between the memory controller 12 and the data register buffers 300 are performed. (*Id.*, ¶¶ [0150]-[0159].) The write and read leveling operations between a data register buffer 300 and a memory controller 12 are referred to herein as "S5-Write Leveling" and "S5-Read Leveling."

As further clarified in Saito, the S4-Write Leveling and S4-Read Leveling and the S5-Write Leveling and S5-Read Leveling are performed by different circuitry in the memory system.

<u>S4 Leveling</u>

The S4-Write Leveling and S4-Read Leveling are performed by write leveling circuit 322 and read leveling circuit 323 in the data register buffer 300. (*Id.*, Fig. 5 (annotated and reproduced below).)

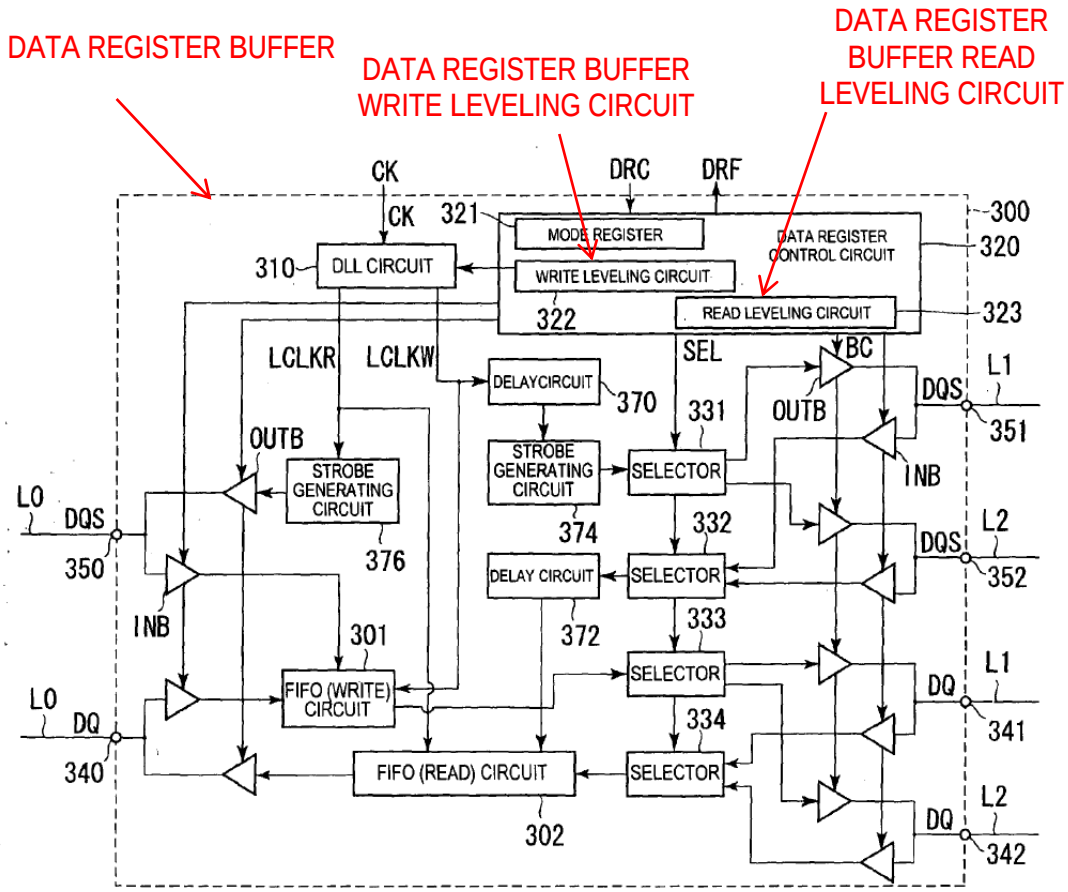


FIG.5

The S5-Write Leveling and S5-Read Leveling, in contrast, are performed by write leveling circuit 12a and read leveling circuit 12b in the memory controller 12. (*Id*., Fig. 2 (annotated and reproduced below).)

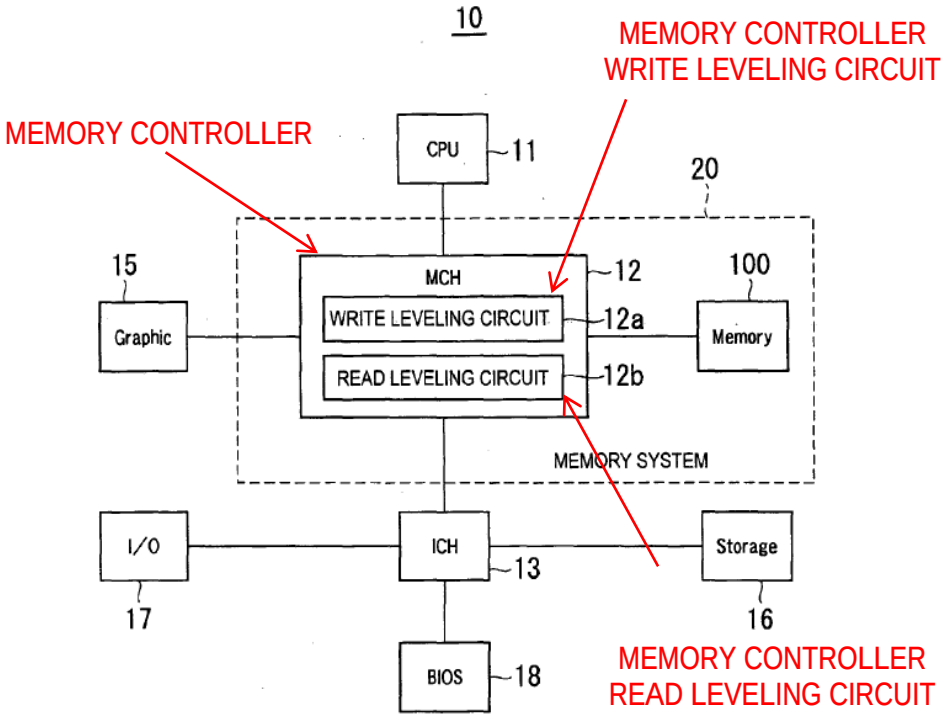
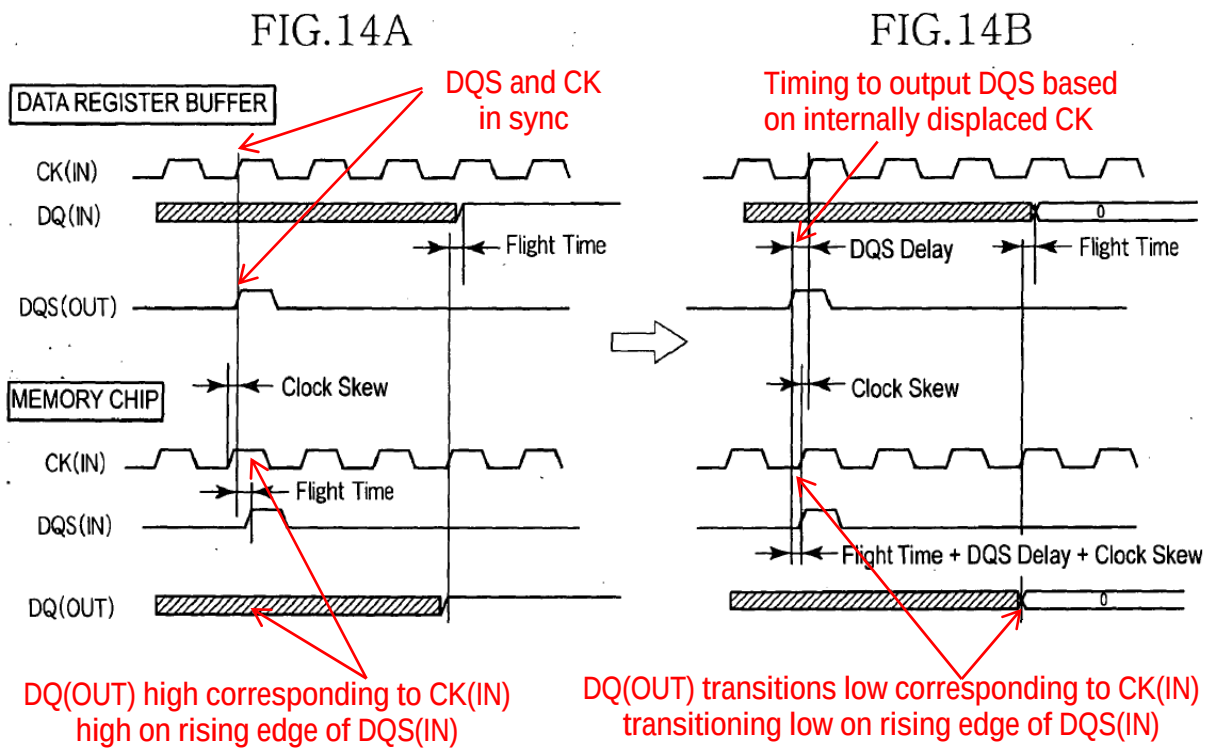


FIG.2

The details of Saito's S4-Read Leveling and S4-Write Leveling are described with reference to timing diagrams of Figs. 14A, 14B and 15 and the details of Saito's S5-Read Leveling and S5-Write Leveling are described with reference to timing diagrams of Figs. 16A, 16B and 17. These timing diagrams are presented and annotated below.

Saito's S4-Write Leveling, performed by write leveling circuit 322 in data register buffer 300, accounts for mismatch between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. (*Id*., ¶¶ [0140]-[0141].) The mismatch is due to the propagation delay of DQS generated by the data register buffer 300. (*Id*., ¶ [0141].) The clock signal is provided from the command/address/control register buffer 400 directly to the memory chip 200, as well as provided to data register buffer 300 to synchronize the generation of the DQS signal. (*Id*.) Upon completing S4-Write Leveling, the phase of the clock signal CK and the DQS signal input to the memory chip are aligned. (*Id*., ¶ [0144].)

Saito seeks to achieve the timing alignment of S4-Write Leveling by adjusting the output timing of the DQS signal by displacing the internal clock LCLKW of data register buffer 300. (*Id*., ¶ [0142].) As illustrated in Fig. 14A, to begin the data register buffer 300 generates a DQS signal, DQS(OUT), in synchronization with the CK signal, CK(IN). (*Id*.) During the write leveling operation, memory chip 200 can output a logic value on a DQ signal, DQ(OUT) corresponding to the state of clock signal received by the memory chip, CK(IN), on the rising edge of the DQS signal received by the memory chip, DQS(IN). (*Id*.)



Data register buffer 300 can displace the internal clock LCLKW in the direction of the phase shift to displace the generation of the DQS signal, DQS(OUT) with respect to the clock signal, CK(IN). (*Id.*, ¶¶ [0143]-[0144].) Eventually, as illustrated in Fig. 14B, DQ(OUT) transitions when the state of clock signal transitions on the rising edge of the DQS signal received by the memory chip. (*Id.*) The displacement of LCLKW can be stored in data register control circuit 320. (*Id.*, ¶ [0144].)

Saito's S4-Read Leveling is performed by read leveling circuit 323 of data register buffer 300. (*Id.*, ¶ [0145].) S4-Read Leveling measures a time A between receipt of a Read Command that is input as part of the control signals DRC, and the receipt of data DQ, at the data register buffer 300. (*Id.*, ¶ [0149].) Time A is

measured for each memory chip 200 corresponding to the data register buffer 300, and stored to adjust activation timing of input buffer circuit INB, for example. (*Id.*)

As illustrated in Fig. 15, S4-Read Leveling begins with the command/address/control register buffer 400 outputting the clock signal CK, the active command (ACT) and the read command (Read). (*Id.*, ¶ [0146].) The clock signal CK is supplied to the memory chip 200 and the data register buffer 300, and the Read command is supplied to the memory chip 200 and the data register buffer 300 (e.g., as a part of the control signal DRC). (*Id.*)

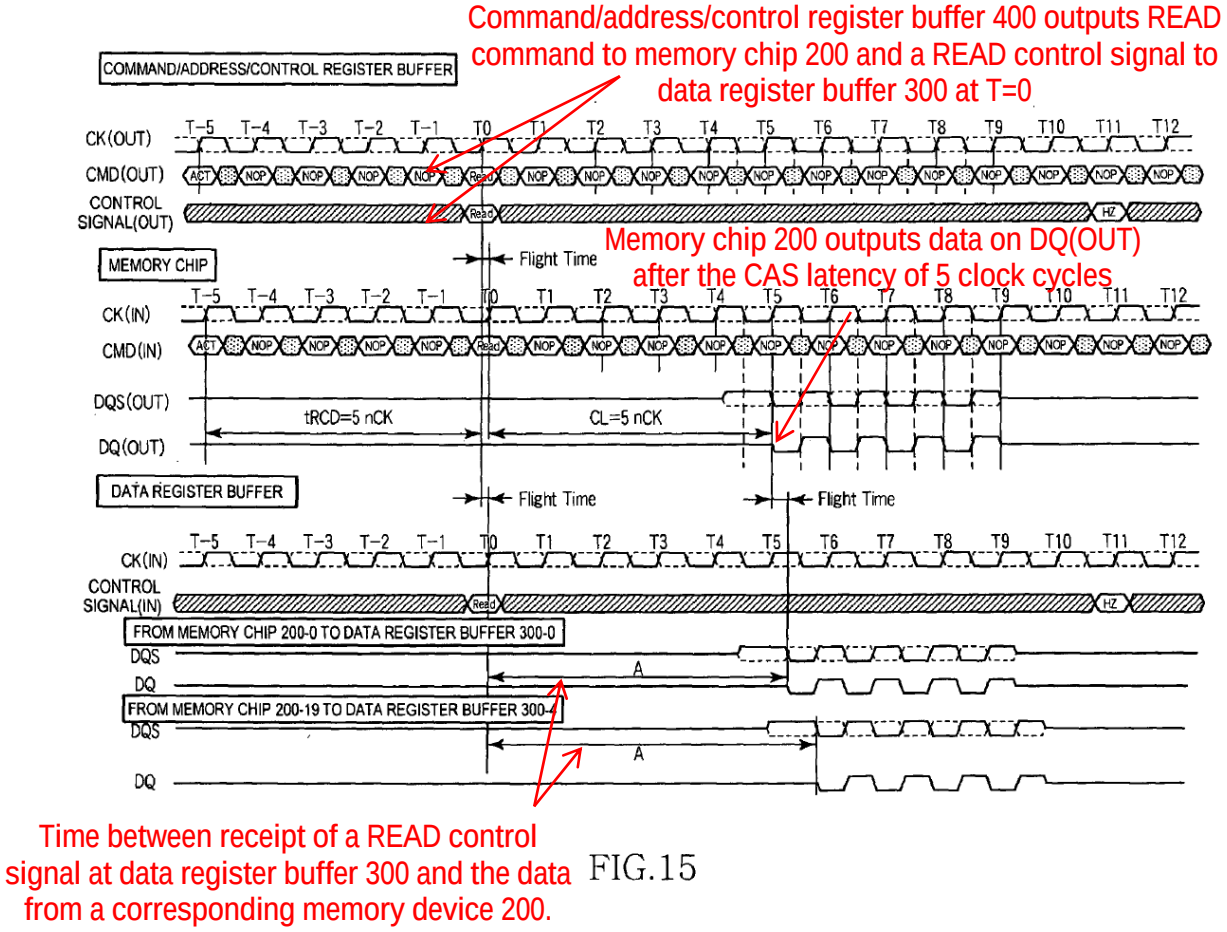


FIG.15

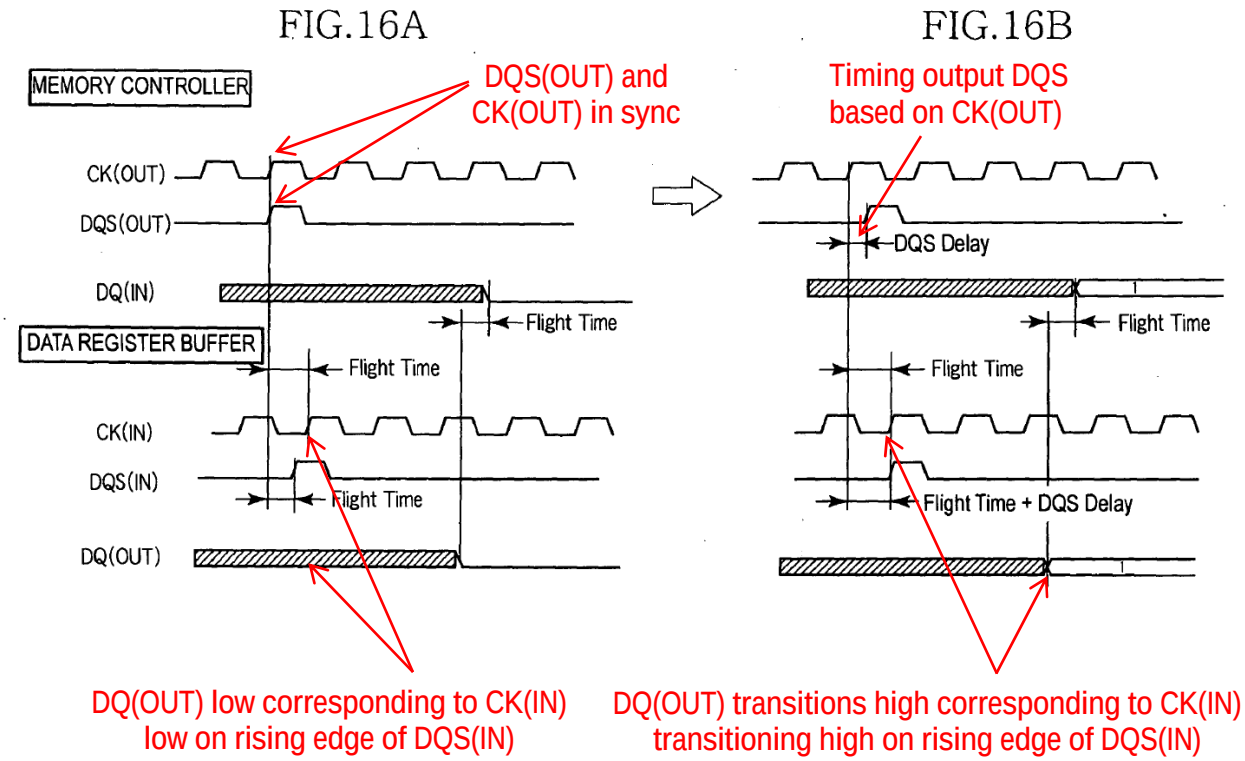
The memory chip 200 can perform a read operation in response to the Read command and output a data pattern. (*Id*., ¶ [0148].) The data output by the memory chip 200 can be received by the data register buffer 300, and used to determine time A. (*Id*., ¶ [0149].)

S5 Leveling

Saito's S5-Write Leveling, performed by the memory controller, accounts for mismatch between the time of receipt of the clock signal CK and the data strobe signal DQS at data register buffer 300. (*Id*., ¶ [0151].) The mismatch is due to the propagation delay of clock signal CK supplied the data register buffer 300. (*Id*.) The clock signal is provided from the command/address/control register buffer 400 to the data register buffer 300, but the DQS signal is supplied directly to the data register buffer from the memory controller. (*Id*.) Upon completing S5-Write Leveling, the phase of the clock signal CK and the DQS signal input to the data register buffer are aligned. (*Id*., ¶ [0154].)

Saito seeks to achieve the timing alignment of S5-Write Leveling by adjusting the output timing of the DQS signal at the memory controller in the direction of the phase shift between the clock signal CK and the DQS signal. (*Id*., ¶ [0152].) As illustrated in Fig. 16A, to begin the memory controller generates a DQS signal, DQS(OUT), in synchronization with the CK signal, CK(OUT). (*Id*.) During the write leveling operation, data register buffer 300 can output a logic

value on a DQ signal, DQ(OUT) corresponding to the state of clock signal received by the data register buffer 300, CK(IN), on the rising edge of the DQS signal received by the data register buffer 300, DQS(IN). (*Id.*)



The memory controller can displace the output timing of the DQS signal in the direction of the phase shift to displace the generation of the DQS signal, DQS(OUT) with respect to the clock signal, CK(OUT). (*Id.*, ¶ [0153].) Eventually, as illustrated in Fig. 16B, DQ(OUT) transitions when the state of clock signal transitions on the rising edge of the DQS signal received by the data register buffer 300. (*Id.*, ¶ [0154].) The displacement between the CK signal and DQS

signal output by the memory controller can be stored in internal circuitry of the memory controller. (*Id*.)

Saito's S5-Read Leveling performed by read leveling circuit 12b of the memory controller. (*Id*., ¶ [0155].) S5-Read Leveling measures a time B between issuance of a Read Command and the receipt of data DQ, at the memory controller. (*Id*., ¶ [0159].) Time B is measured for each data register buffer 300, and stored in the internal circuitry of the memory controller to adjust activation timing of input buffer circuit in the memory controller, for example. (*Id*.)

As illustrated in Fig. 17, S5-Read Leveling begins with the memory controller outputting the clock signal CK, the active command (ACT) and the read command (Read). (*Id*., ¶ [0156].) The clock signal CK is supplied to the data register buffer 300, and the Read command is supplied to the data register buffer 300 (e.g., as a part of the control signal DRC) via the command/address/control register buffer 400. (*Id*.) The data register buffer 300 can automatically generate dummy output data pattern in response to the Read command. (*Id*., ¶ [0158].) The dummy data output by the data register buffer 300 can be received by the memory controller, and used to determined time B. (*Id*., ¶ [0159].)

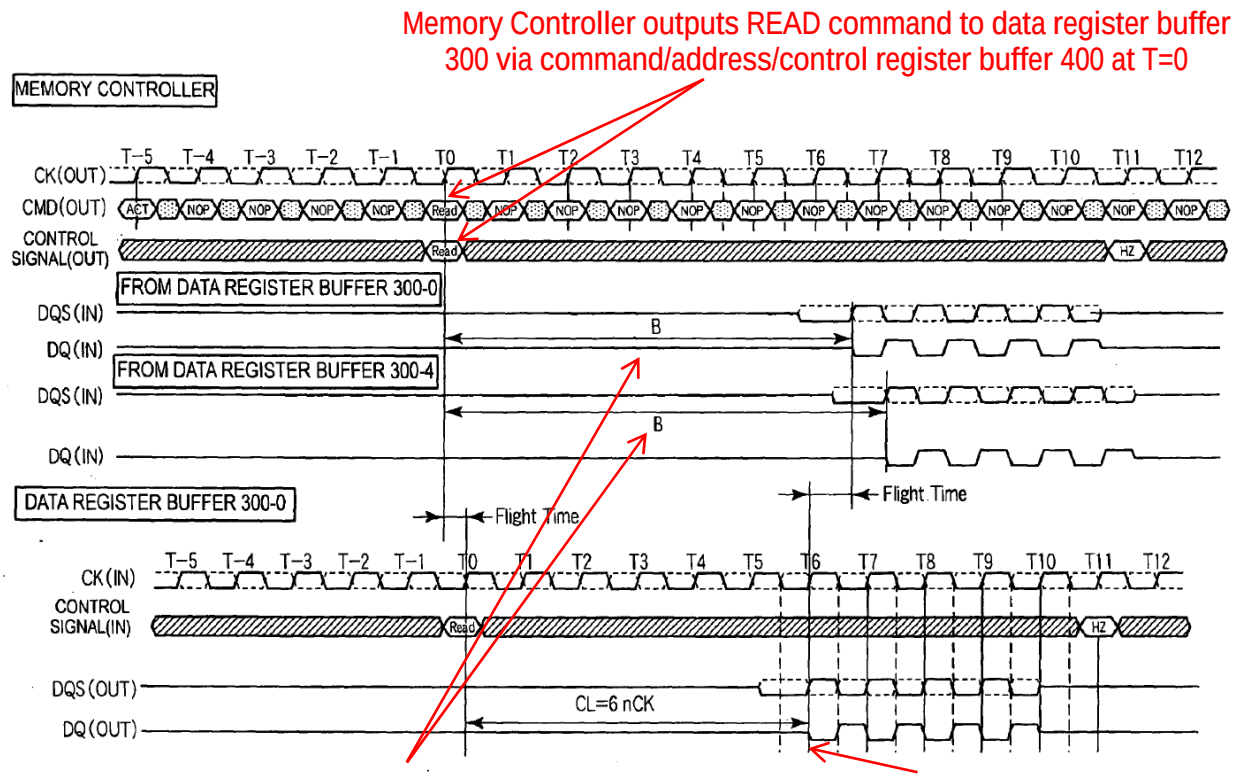


FIG.17

A characteristic flaw in the Petitioner's reliance on Saito is an incorrect characterization of Saito's timing adjustments and delays between the write and read leveling operations as being the same. (Pet., 32.) As detailed above and below, Saito expressly teaches performing separate read and write leveling operations for the data register buffer-memory chip interface and for the memory controller-data register buffer interface (S4-Read Leveling, S4-Write Leveling, S5-Read Leveling and S5-Write Leveling) and using different timing adjustments or delays based on these separate read and write leveling operations. (Saito, Ex.

1005, ¶ [0101].) The Petitioner sets forth interpretations of, and combinations with, Saito that are contrary to Saito's actual operational principles, as above.

B. Swain

Swain discloses a read leveling technique for memory devices in a sequential chained topology. (Ex. 1006, Swain, Abstract.) Swain identifies limitations of prior art read leveling techniques including 1) susceptibility to cross talk and board level noises when using a single data pattern and 2) prevention of detection of stuck-at faults. (*Id*., 5:9-18.) Swain proposes a read leveling technique illustrated in Fig. 4 and described at 5:25-6:61.

For this read leveling technique, Swain discloses a memory controller performing a first step of write leveling, according to known approaches, and then a next step of writing a data pattern containing multiple bytes into different memory locations. (*Id*., 5:44-55.) The data pattern can be selected to identify stuck-at faults, board level noise, crosstalk, etc. (*Id*., 5:55-58.) In a subsequent step of reading a data portion, the read data portion may correspond to a single byte of the written data pattern. (*Id.*, 5:66-6:2.)

Swain's memory controller can then iteratively set compensation test values and perform data reads of the previously written data pattern to search for the optimum compensation value using the test values. (*Id*., 5:59-62, 5:66-6:5.) The memory controller compares the read data with expected data according to the data

pattern. (*Id.*, 6:6-7) When there is a match, it may be concluded that the present test value is acceptable for later read operation during normal read operation. (*Id.*, 6:7-10.) More than one acceptable test value may be determined. (*Id.*, 6:11-23.)

C. Kim

Kim discloses integrated circuits having metastability detection/prevention circuits. (Ex. 1007, Kim, 2:20-57.) The Petition only cites Lee for its purported disclosure of a "metastability detection circuit" and/or "signal adjustment circuit" as claimed in the '632 Patent. (*See, e.g.*, Pet., 50.)

V. CLAIM CONSTRUCTION

During *inter partes* review, the Board gives claims their "broadest reasonable construction in light of the specification of the patent," of which they are a part. 37 C.F.R. § 42.100(b); *Cuozzo Speed Tech., LLC. v. Lee*, 136 S.Ct. 2131, 2144 (2016) (affirming the propriety of the broadest reasonable construction standard during *inter partes* review proceedings). Claim construction must be "reasonable in light of the totality of the written description." *In re Baker Hughes, Inc.*, 215 F.3d 1297, 1303 (Fed. Cir. 2000).

For the purposes of this Response, the Patent Owner submits that all claims terms should be accorded their ordinary and customary meaning as understood by one of ordinary skill in the art. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257

(Fed. Cir. 2007). The Patent Owner also submits that construction of claim terms is not required here to address the deficiencies in the Petition.

VI. RESPONSE TO GROUNDS OF CHALLENGE

A. Ground A – Saito In View Of Swain Fails To Render Obvious Claims 1-5, 12-14, 19 And 20

Under Ground A, the Petitioner asserts that claims 1-5, 12-14, 19 and 20 are unpatentable under 35 U.S.C. § 103 as obvious over Saito in view of Swain. (Pet., 15-49.) The Petitioner's proposed ground of unpatentability under § 103 based on Saito and Swain is deficient, as discussed below.

1. Independent Claim 1

The Petition's combination of Saito and Swain fails to meet claim 1 based on at least the follow recitations related to the claimed "each respective buffer circuit" and "respective time interval":

> wherein the each respective buffer circuit
>
> [(i)] is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and
>
> [(ii)] is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

As will be shown below, the Petitioner's mapping of these recitations to Saito and Swain and the Petitioner's obviousness rationales proposed to support the proposed Saito-Swain combination are deficient.

a) The Saito-Swain Combination Fails To Meet The Recitations Of Claim 1

The Petitioner's "each respective buffer circuit" is Saito's data register buffer 300. (Pet., *e.g.*, 22, 28.)

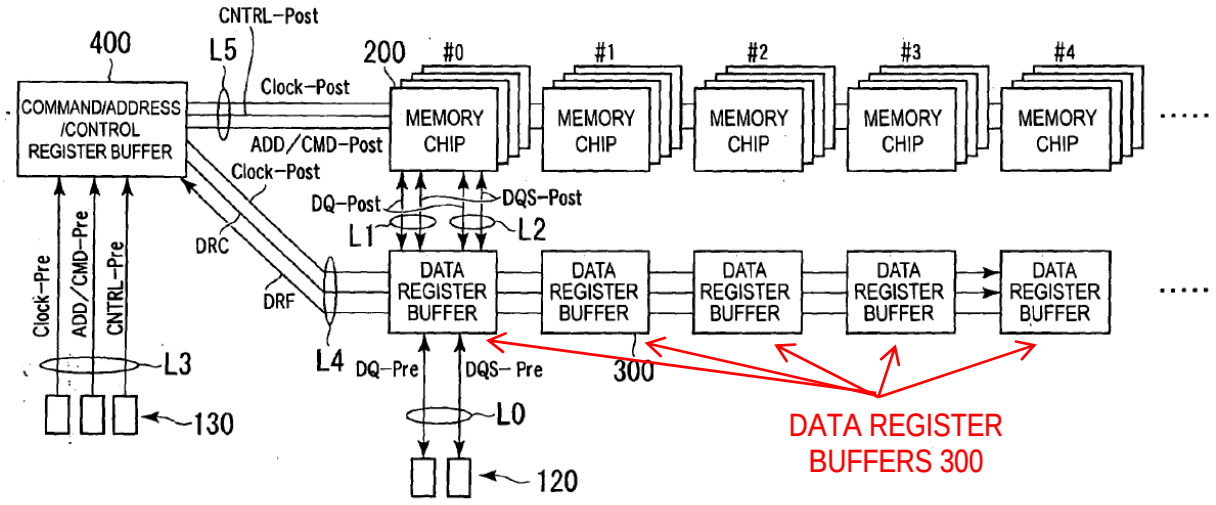


FIG.7

The Petitioner's "respective time interval" is mapped to "a re-timing . . . to convert CL into CL=6" at paragraph [0128] of Saito, as emphasized by Petitioner's expert. (Pet., 29; Ex. 1003, Mudge Decl., ¶ 127 (bold emphasizing "the data register buffer 300 performs a re-timing . . . to convert CL into CL=6" of Saito's ¶ [0128]).)

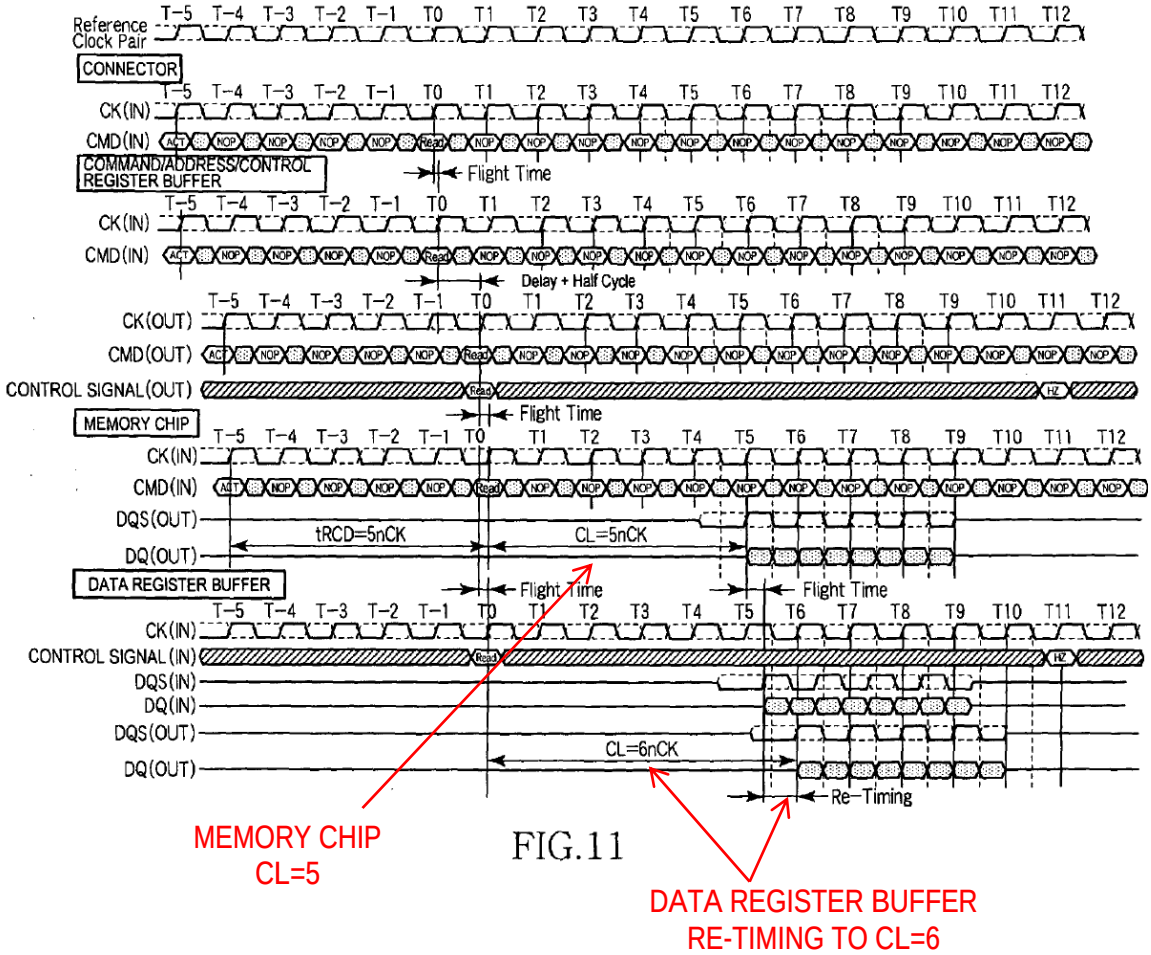

Reference Clock Pair
CONNECTOR
CK(IN)
CMD(IN)
COMMAND/ADDRESS/CONTROL REGISTER BUFFER
Flight Time
Delay + Half Cycle
CK(OUT)
CMD(OUT)
CONTROL SIGNAL(OUT)
MEMORY CHIP
DQS(OUT)
DQ(OUT)
tRCD=5nCK
CL=5nCK
DATA REGISTER BUFFER
CONTROL SIGNAL(IN)
DQS(IN)
DQ(IN)
CL=6nCK
Re-Timing
MEMORY CHIP
CL=5
DATA REGISTER BUFFER
RE-TIMING TO CL=6

FIG.11

The Petition makes the following mapping and combination of Saito and Swain:

> The data register buffers of Saito are thus "*configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation*." And the data register buffers are also "*configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with*" a time interval (determined during the read leveling operation – but not the time interval determined during the writing leveling operation), "*and a read latency parameter of the memory system during a memory read operation*." Saito thus meets the limitations of this element, but for using its time interval determined during the writing leveling operation ("*a memory write operation*") with the read latency parameter during a memory read operation. Ex. 1003 at ¶¶123-128.
>
> However, Swain discloses using the timing intervals determined during write leveling operations in the read leveling operations as well. *Id.* at ¶¶131-133.

(Pet., 29-30.)

With respect to recitation (i), the Petitioner's "memory write operation" is a writing leveling operation. (Pet., 30.) The Petitioner concedes that its "respective time interval" from Saito ("a re-timing . . . to convert CL into CL=6") is not "based on signals received by the each respective buffer circuit during" a writing leveling

operation (Petitioner's "memory write operation") from Saito alone. Instead, the Petitioner's "memory write operation" is mapped to a write leveling operation of Saito modified by Swain. (*Id.*)

With respect to recitation (ii), the Petitioner's "read latency parameter" is "a known read latency, referred to as CAS latency, that 'is set to five clock cycles (CL=5)'" attributed to Saito's paragraphs [0126] and [0148]. (*Id.*, 29.) The Petitioner's "memory read operation" is a "read operation[] during normal operation" attributed to Saito's paragraph [0126] (*id.*), which refers to the read operation in Saito's Fig. 11. Thus, according to the Petitioner's mapping, the Petitioner's "buffer circuit" (Saito's data register buffer 300) "is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with" the Petitioner's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") and the Petitioner's "read latency parameter" (Saito's "CL=5") during the Petitioner's "memory read operation" (Saito's read operation in Fig. 11).

There is, however, a technological error in the Petitioner's mapping for recitation (i). In order for the Saito-Swain combination to meet recitation (i) under the Petitioner's mapping, the Petitioner's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") should be "based on signals received by the each respective buffer circuit during" the Petitioner's "memory write operation" (write

leveling operation in the Saito-Swain combination). But neither Saito nor Swain supports such a technological relationship between a CL conversion re-timing and a write leveling operation, which would be required for the Saito-Swain combination to meet claim 1.

Saito plainly identifies the basis for this "re-timing": "to convert CL into CL=6," which even the Petitioner's expert emphasizes. (Ex., 1005, Saito, ¶ [0128]; Ex. 1003, Mudge Decl., ¶ 127.) This CL conversion is a one-clock-cycle conversion of the CAS latency ("CL=5" clock cycles to "CL=6" clock cycles). Importantly, Saito discloses this CL conversion as a read latency (at ¶ [0128]) not a write latency (disclosed as WL at ¶ [0131] of Saito). In other words, this CL conversion re-timing is directed to a read operation—not a write operation.

There is more. Saito also discloses this CL conversion re-timing as *separate* from leveling (both read and write leveling) teachings. Specifically, Saito's read and write leveling teachings are performed during an initialization operation *before* read and write operations. (Ex. 1001, Saito, Fig. 13 (reproduced below) leveling steps S4 and S5).)

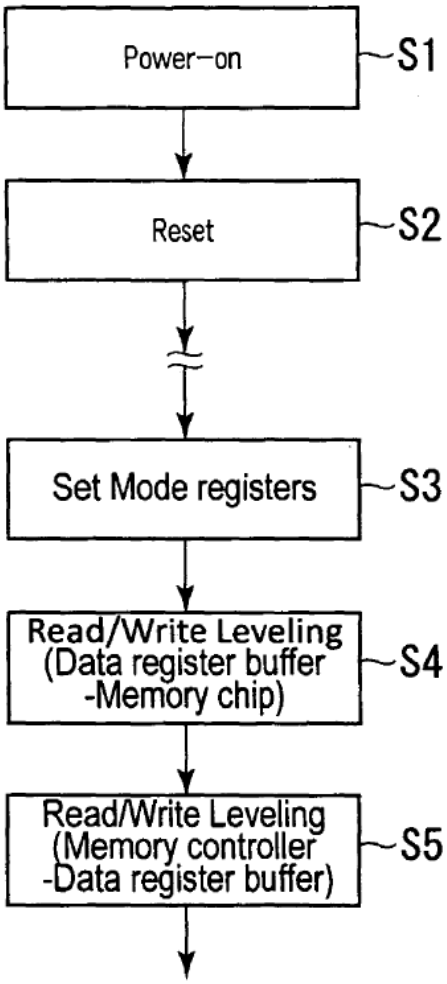


FIG.13

Indeed, Saito uses different figures to separately show CL conversion re-timing (in Fig. 11) and leveling teachings (Figs. 14A-17).

Swain lacks any mention of a CL conversion re-timing, much less any technological relationship between a CL conversion re-timing and a write leveling operation. Rather, the Petitioner merely asserts that Swain discloses some link between read leveling and write leveling. (Pet., *e.g.*, 31.) Specifically, the

Petitioner cites to a lone phrase in Swain—"parameters determined while write leveling" (Ex. 1006, Swain, 5:59-65)—to assert that "the time interval determined during write leveling is used in read leveling as well" (Pet., 31). Even assuming *arguendo* that this statement means what the Petitioner urges it to be, applying this Swain-based assertion to Saito still would not establish a technological relationship between Saito's CL conversion re-timing and Saito's write leveling. Swain would merely link Saito's read leveling and write leveling, so the write leveling teachings of the Saito-Swain combination (Petitioner's "memory write operation") would still be distinct from its CL conversion re-timing (Petitioner's "time interval").

Moreover, this kind of CL conversion re-timing in Saito (Petitioner's "time interval") was well-known and its underlying design reason was unrelated to any write leveling. Load Reduced DIMMs (LRDIMMs) are a kind of memory module that has a "memory buffer chip" (Ex. 2001, HP, 3), which is like Saito's own data register buffer 300 teachings. HP explains that the "buffering [provided by the memory buffer chip] requires adding clock cycles to memory reads and writes, increasing the latency of LRDIMMs relative to single and dual-rank RDIMMs" (*id.*), which is the same kind of CL conversion re-timing in Saito. Similar to HP's "adding clock cycles to memory reads and write, increasing the latency of LRDIMMs" (*id.*), Saito's CL conversion re-timing is a one-clock-cycle addition in the conversion of the CAS latency ("CL=5" clock cycles to "CL=6" clock cycles in

¶¶ [0126] and [0128] of Saito). In other words, the design reason for this kind of CL conversion re-timing in Saito (Petitioner's "time interval") is the buffering provided by Saito's data register buffer 300, not any write leveling (Petitioner's "memory write operation"). (*See also* Ex. 2002, Cooper-Balis, 13 ("The only noticeable difference seen to the system is a one cycle increase in latency to account for the latching signals and data before it is sent to the DRAM device of memory controller.").)

Given the underlying technological distinction between the Petitioner's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") and Petitioner's "memory write operation" (write leveling operation in the Saito-Swain combination), neither Saito nor Swain supports the Petitioner's attempt to link these distinct techniques in the manner required by claim 1: *i.e.*, the Petitioner's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") should be "based on signals received by the each respective buffer circuit during" the Petitioner's "memory write operation" (write leveling operation in the Saito-Swain combination). They are not linked, as evidenced by teachings in Saito itself and the state-of-the-art disclosures above.

Indeed, the Petitioner must rely on sleight-of-hand to create such a non-existent link. The Petitioner states:

> And the timing adjustment ("*respective time interval*") that is the result of the read leveling operation during initialization is used with that CAS latency ("*read latency*") to time transmission during read operations. *Id.* at [0128]; Ex. 1003 at ¶127.

(Pet., 29.) This is a sleight-of-hand statement by the Petitioner. As shown above, Petitioner's "time interval" is *not* "the result of the read leveling operation during initialization" (or any other leveling teaching) in Saito or Swain. Instead, Petitioner's "time interval" (Saito's "re-timing . . . to convert CL into CL=6") is a one-clock-cycle addition in the conversion of the CAS latency ("CL=5" clock cycles to "CL=6" clock cycles in ¶¶ [0126] and [0128] of Saito), which is for the buffering provided by Saito's data register buffer 300. As also discussed above, the underlying design reason for Saito's leveling is "consideration of a propagation time of a signal" (in ¶ [0138]), not buffering provided by Saito's data register buffer 300.

For at least the reasons set forth above, the Petitioner's proposed obviousness ground for independent claim 1 is deficient. Relying on its deficient analysis for claim 1 (Pet., 42-45), the Petitioner's proposed obviousness ground of unpatentability of independent claim 12 is also deficient. Accordingly, the Patent Owner respectfully requests the Board to deny *inter partes* review of the Petition's

proposed ground of unpatentability for claims 1-5, 12-14, 19 and 20 as obvious over Saito in view of Swain (Ground A) for this reason.

b) The Petition Fails To Establish A Proper Obviousness Rationale For The Saito-Swain Combination

The Petitioner asserts that the combination of Saito and Swain renders claim 1 obvious. (Pet., 31-33.) Specifically, the Petition alleges multiple rationales to support its conclusion of obviousness over its proposed combination of Saito and Swain. As discussed in more detail below, the Petition used the claim language as a hindsight roadmap to construct the Saito-Swain combination. Specifically, the proposed combination of Saito and Swain is deficient because the Petition's obviousness rationales are inapplicable to the proposed combination and undercut by the actual disclosures of Saito and Swain.

(1) Saito's Read And Write Intervals Are Not The Same

The first obviousness rationale provided by the Petition is a motivation based on an allegedly express teaching in Saito. As explained below, Saito teaches the exact opposite.

The Petition presents the first rationale as follows:

> A person of ordinary skill in the art would have been motivated to look to the read leveling operation described in Swain as utilizing the time intervals determined during the writing leveling operation when considering Saito because Saito expressly teaches that the write and

> read intervals are the same, as explained above. Ex. 1003 at ¶134. This teaching is an express suggestion in Saito to use the read leveling operation of Swain (that are based on "parameters determined while write leveling," Ex. 1006 at 5:63-64) for purposes of determining the time interval for memory read operations.

(Pet., 32 (Underline in original).) In particular, the Petition asserts that "Saito expressly teaches that the write and read intervals are the same." (*Id.*)

To support this allegedly express teaching in Saito, the Petition refers to its earlier statements:

> Given that Saito discloses that the bus line lengthens and transfer rates in its system are the same for both reads and writes, an ordinarily skilled artisan would understand that any time intervals for writes and reads should be the same for a particular portion of the system (*e.g.*, memory chip-data register buffer or data register buffer-memory controller) and time intervals for one could be used for the other, such as Swain teaches for using time intervals determined during write leveling for read leveling as well. *Id.* at ¶133. For instance, Saito teaches:
>
>> Because the data register buffer 300 only performs the buffering of the data, transfer rates of the write data and the read data that are transferred via the data line L0 and transfer rates of the write data and the read data that are transferred via the data lines L1 and L2 are equal to each other.
>
> Ex. 1005 at [0089].

(Pet., 31-32 (Underline in original).)

These above statements, however, fail to establish the Petition's allegedly express disclosure in Saito that "write and read intervals are the same." A transfer rate is not a time interval. Equal transfer rates (in Saito's ¶ [0089]) do not mean equal or same time intervals (as alleged by the Petition).

Additionally, the above statements fail to justify that "[t]his teaching is an express suggestion in Saito to use the read leveling operation of Swain." Saito's paragraph [0089] simply discloses equal transfer rates. The disclosure of equal transfer rates is not an express suggestion to use any read leveling operation, much less the read level operation of Swain.

Because the Petition's allegedly express disclosure in Saito that "write and read intervals are the same" is not actually supported by Saito, the Petition's first rationale cannot stand. Thus, a POSITA would have *not* been "motivated to look to the read leveling operation described in Swain as utilizing the time intervals determined during the writing leveling operation when considering Saito."

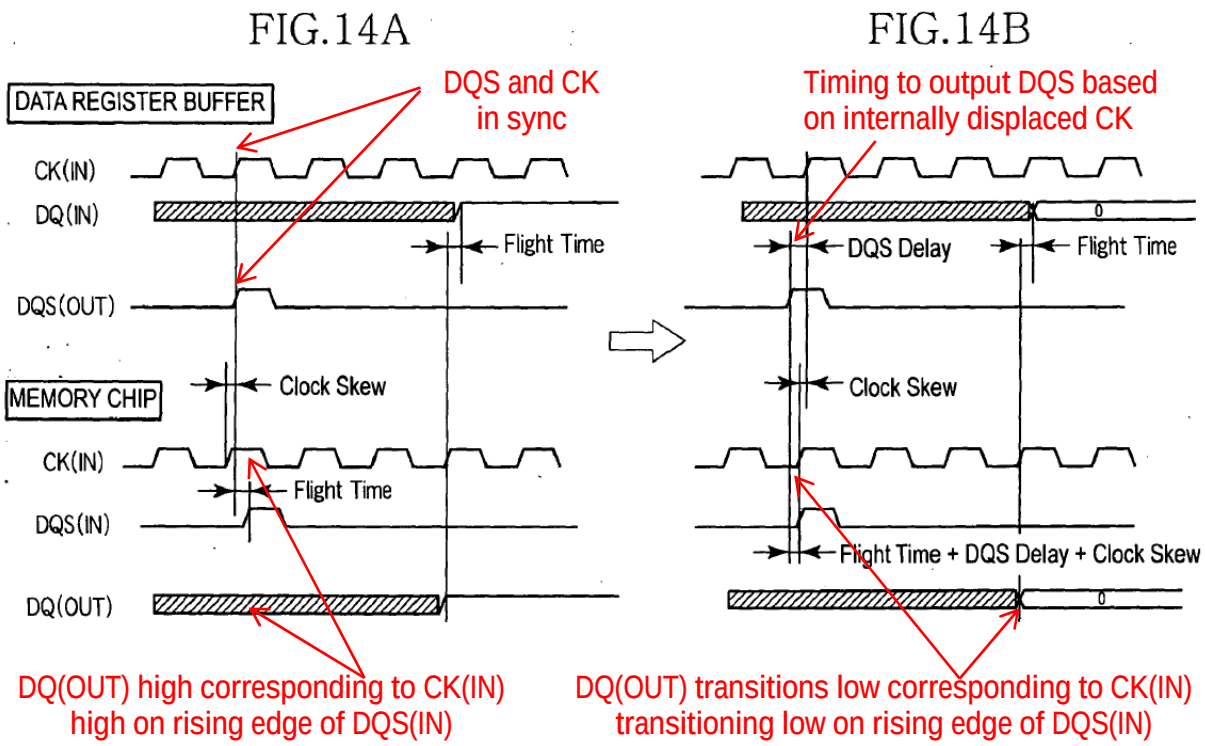
In fact, Saito teaches the opposite—recognizing that different (not same) timings are implemented for Saito's read and write leveling (Saito, ¶¶ [0101], [0140]-[0159], Figs. 14A-17)—despite the common data bus line lengths in portions of the memory system (*id.*, ¶ [0055]) and the common data transfer rates through the buffer (*id.*, ¶ [0089]) in Saito. Different read and write leveling

operations are required by Saito because read and write leveling timing parameters are not simply interchangeable, even when bus line lengths or data transfer rates through the buffer are the same. The read and write leveling operations, even in the same portion of the system, are provided to account for different timing issues and are used for different purposes.

For example, Saito's S4-Write Leveling (performed by write leveling circuit 322 in data register buffer 300), accounts for mismatch between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. (*Id*., ¶¶ [0140]-[0141].) The mismatch is due to the propagation delay of DQS generated by the data register buffer 300 with respect to the clock signal. (*Id*., ¶ [0141].) The clock signal is provided from the command/address/control register buffer 400 directly to the memory chip 200, as well as provided to data register buffer 300 to synchronize the generation of the DQS signal. (*Id*.) Upon completing S4-Write Leveling, the phase of the clock signal CK and the DQS signal input to the memory chip are aligned. (*Id*., ¶ [0144].)

Saito achieves the timing alignment of S4-Write Leveling by adjusting the output timing of the DQS signal by displacing the internal clock LCLKW of data register buffer 300. (*Id*., ¶ [0142].) As illustrated in Fig. 14A (reproduced and annotated below), to begin the data register buffer 300 generates a DQS signal, DQS(OUT), in synchronization with the clock signal, CK(IN). (*Id*.) During the

write leveling operation, memory chip 200 can output a logic value on a DQ signal, DQ(OUT) corresponding to the state of clock signal received by the memory chip, CK(IN), on the rising edge of the DQS signal received by the memory chip, DQS(IN). (*Id.*)



Data register buffer 300 can displace the internal clock LCLKW in the direction of the phase shift to displace the generation of the DQS signal, DQS(OUT) with respect to the clock signal, CK(IN). (*Id.*, ¶¶ [0143]-[0144].) Eventually, as illustrated in Fig. 14B, the logic value of the DQ signal, DQ(OUT) changes when the state of clock signal received by the memory chip, CK(IN), on the rising edge of the DQS signal received by the memory chip, DQS(IN)

changes. (*Id*.) The displacement of LCLKW can be stored in data register circuit 320. (*Id*., ¶ [0144].)

In contrast, Saito's S4-Read Leveling (performed by read leveling circuit 323 of data register buffer 300) measures a time A between receipt of a Read Command that is input as part of the control signals DRC, and the receipt of data DQ, at the data register buffer 300. (*Id*., ¶¶ [0145]-[0149].) Time A is measured for each memory chip 200 corresponding to the data register buffer 300, and stored to adjust activation timing of input buffer circuit INB, for example. (*Id*.)

As illustrated in Fig. 15 (reproduced and annotated below), S4-Read Leveling begins with the command/address/control register buffer 400 outputting the clock signal CK, the active command (ACT) and the read command (Read). (*Id*., ¶ [0146].) The clock signal CK is supplied to the memory chip 200 and the data register buffer 300, and the Read command is supplied to the memory chip 200 and the data register buffer 300 (e.g., as a part of the control signal DRC). (*Id*.) The memory chip 200 can perform a read operation in response to the Read command and output a data pattern. (*Id*., ¶ [0148].) The data output by the memory chip 200 can be received by the data register buffer 300, and used to determine time A. (*Id*., ¶ [0149].)

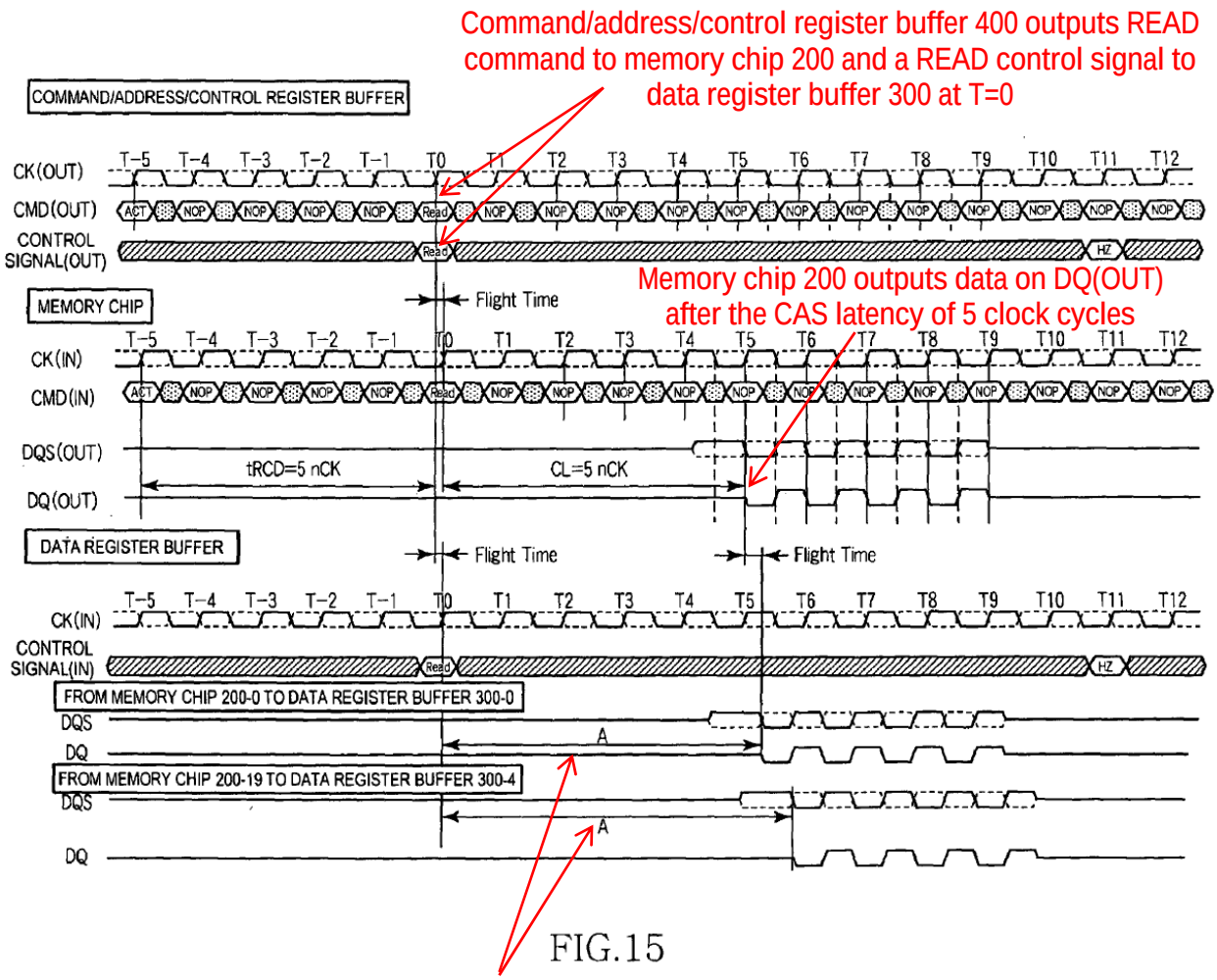


FIG.15

Time between receipt of a READ control signal at data register buffer 300 and the data from a corresponding memory device 200.

As indicated above, Saito's read and write leveling operations are not simply about data buffer transfer rates or bus line lengths. Instead, the S4-Write Leveling operation accounts for mismatch between a clock signal and a DQS signal at the input to a memory chip. The result of the operation is an adjustment of an internal clock signal LCLKW. The S4-Read Leveling operation accounts for potential mismatch involving other signals: Read commands signals and clock signals being sent to both the memory chip 200 and the data register buffer 300 in parallel. The

result of the operation is a time interval A that is used to activated input buffers of data register buffer 300.

To summarize, despite the common bus line lengths for L0-L2 and the common data transfer rates through data register buffer 300, Saito discloses different read leveling and write leveling operations that account for different signals and delays (DQS/CK vs. Read Command/DQ), include different results (adjustment of clock vs. time interval between two different signals), and impact different parts of the circuit (internal clock LCLKW vs. INB control). Thus, contrary to the Petition's allegedly express disclosure in Saito that "write and read intervals are the same," Saito actually teaches that different (not same) timings are implemented for Saito's read and write leveling.

Therefore, the basis for the Petition's first obviousness rationale—the Petition's allegedly express disclosure in Saito that "write and read intervals are the same—is unsupported by, and even opposite to, Saito's actual disclosure. Accordingly, the Petition's first rationale is inapplicable and, thus, fails to properly establish the proposed combination of Saito and Swain.

(2) Saito's Read And Write Intervals Do Not Measure The Same Period

The Petition presents a second obviousness rationale as follows:

> A skilled artisan would also have been motivated to use the write-leveling timing as a basis for read leveling in order to avoid having to measure the same period twice. Ex. 1003 at ¶134.

(Pet., 32.) This obviousness rationale is also improper for being inapplicable to the proposed combination of Saito and Swain. The only support for this alleged motivation is a conclusory statement from Petitioner's expert. (Ex. 1003, Mudge Decl., ¶ 134.) As explained below, Saito and Swain both teach the exact opposite. Neither "measure[s] the same period twice" and therefore neither could avoid measuring the same period twice as proposed by the Petition.

The Petition does not identify which period Saito or Swain measures twice, nor any indication that using write-leveling timing as a basis for read leveling would avoid measuring said period twice. Swain discloses performing a write leveling and a read leveling. (Ex. 1006, Swain, 5:44-6:23.) Petitioner asserts that Swain discloses "the time interval determined during write leveling is used in read leveling as well." (Pet., 31.) Irrespective of the source of the test values in Swain's read leveling operation, however, Swain performs a write leveling operation to determine "various delays that may be required to reliably write (stores) data" and a read leveling operation to determine a read compensation delay

based on an acceptable or optimum test value for delay. (Ex. 1006, Swain, 5:45-46, 5:59-62, 6:8-10.) Swain does not presume that the read leveling compensation delay and various write leveling delays are the same, such that measurement of a read leveling period can be avoided by relying on a write leveling delay parameter.

As discussed above with respect to the first rationale, Saito discloses read leveling operations and write leveling operations accounting for different timing issues, including different stored results, and impacting different parts of the data register buffer. Saito's S4-Read Leveling measures, for each memory chip, a time A between receipt of a Read Command from a command/address/control register buffer 400 and receipt of read data from a memory chip 200 at the corresponding data register buffer 300. Saito's S4-Write Leveling involves determining a displacement of an internal clock LCLKW to align the receipt of a clock signal (from command/address/control register buffer 400) and the receipt of a data strobe signal (from data register buffer 300) at memory chip 200. Saito does not disclose measuring any period twice or that measurement of some period twice would or could be avoided by basing read leveling operation on write leveling timing. In fact, the Petition concedes, by its reliance on Swain, that Saito does not include any suggestion that the read leveling operation should use any write leveling timing. (Pet., 30.)

Therefore, the Petition's second obviousness rationale is inapplicable, and even contrary, to the disclosure of Saito and Swain – each of which requires performing separate read leveling and write leveling operations – and is entirely unsupported by the Petition beyond a conclusory statement by its expert. Accordingly, the Petition's second rationale fails to properly establish the proposed combination of Saito and Swain.

(3) Petition's Proposed Modification Of Saito Based On Swain Does Not Simply Arrange Old Elements Performing The Same Function To Yield Predictable Results

The Petition presents a third obviousness rationale as follows:

> Moreover, when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious, which is the case here. Ex. 1005 at [0089]; Ex. 1006 at 5:54-57; Ex. 1003 at ¶135.

(Pet., 32.) As an initial matter, this rationale as presented in the body of the Petition itself is a conclusory statement without any analysis, facts or evidence. The only application of the rationale in the Petition is to say that it "is the case here." The Petition cannot meet its burden with such a conclusory rationale.

Furthermore, even the Mudge Declaration at "Ex. 1003 at ¶135" is deficient. Here, the read and write leveling operations disclosed in Saito and Swain are identified as the "old elements." There is no discussion about their specific

arrangement in combination or any analysis to support the conclusion that "it would yield no more than one would expect." Instead, the Mudge Declaration relies on the teaching alleged to be in Saito that write and read time intervals would be the same. (Ex. 1003, Mudge Decl., ¶ 135.) However, as discussed above with respect to the first obviousness rationale, Saito does not support the Petition's allegation .

As such, for similar reasons, the Petition's third obviousness rationale fails to properly establish the proposed combination of Saito and Swain.

(4) Swain's Technique Would Not Improve Saito In The Same WayAs In Swain

The Petition presents s fourth obviousness rationale as follows:

> If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. By 2012 Swain's read leveling operation based on the results of its write leveling operation was well-known. Ex. 1003 at ¶136; Ex. 1006 at 5:54-57. It was thus known to improve memory modules on which it was used. Ex. 1003 at ¶136. Further, its actual application was well within the level of ordinary skill in the art, as it was described and taught by Swain. *Id.*

(Pet., 32-33 (Underline in original).) The Petition appears to map this "technique" to "Swain's read leveling operation based on the results of its write leveling operation." The Petition, however, fails to explain why a POSITA could apply

Swain's technique to Saito in the same way. In fact, Swain's technique would not be applied in the same way to the read and write leveling operations of Saito.

In particular, Swain provides a more detailed description of its technique:

> In step 430, memory controller 190 sets the compensation delay to a test value. The test value can be a different value in each iteration of the loop of steps 430-470. The test values may be chosen to 'search' for the optimum value. In addition, any available information (e.g., parameters determined while write leveling of above) can be used in choosing the test value for different iterations.

(Ex. 1006, Swain, 5:59-65.) Swain's read leveling includes choosing test values for an iterative read leveling process, in which test values for the compensation delay can be evaluated to determine an optimum compensation delay resulting from the read leveling process. (*Id*., 5:59-6:23.) Any information, including write leveling parameters, can be used in choosing the test values. (*Id*., 5:62-65.) During the iterative read leveling process, the memory device can be read according to the test value and the read data can compared with expected data. (*Id*., 5:66-6:10.)

Saito's read leveling operations measure a time A between the time of receipt of a Read Command at a data register buffer and the time of receipt of read data at the data register buffer (for S4-Read Leveling). (Ex. 1005, Saito, ¶ [0149], Fig. 15.) Saito's read leveling operation does not involve writing or reading data

patterns, test values or an iterative process. As a result, a POSITA could not and would not implement Swain's read leveling technique in the same way in Saito's memory module. In fact, Saito's read leveling process is a simple measurement and would not achieve a benefit from using a write leveling parameter in the way Swain teaches. As described above, Saito's read leveling and write leveling operations are entirely unrelated. Accordingly, the Petition's fourth obviousness rationale is inapplicable and, thus, fails to properly establish the proposed combination of Saito and Swain.

For at least the above reasons, the Petitioner has failed to establish a proper obviousness rationale for the proposed combination of Saito and Swain. Thus, the Petitioner's proposed obviousness ground for independent claim 1 is deficient. Relying on its deficient analysis for claim 1 (Pet., 42-45), the Petitioner's proposed obviousness ground of unpatentability of independent claim 12 is also deficient. Accordingly, the Patent Owner respectfully requests the Board to deny *inter partes* review of the Petition's proposed ground of unpatentability for claims 1-5, 12-14, 19 and 20 as obvious over Saito in view of Swain (Ground A).

2. Dependent Claim 5

Dependent claim 5 further specifies that the "respective buffer circuit" of claim 1 comprises, in part:

> a time interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first and second signal.

The Petitioner asserts that Saito and Swain render this claim obvious, relying on its analysis of claim 1 and its belief that claim 5 "merely labels some of the circuitry and signals discussed above." (Pet., 42.) The Petitioner is mistaken.

More detailed than claim 1, claim 5 further requires "a time interval determination circuit . . . to generate a delay signal indicating a time interval between" "a first signal from the module controller" and "a second signal from the memory bus." The Petition makes no showing of addressing these claimed details.

The Petitioner's "time interval determination circuit" is Saito's write leveling circuit 322 (Pet., 42), which is shown in Fig. 5.

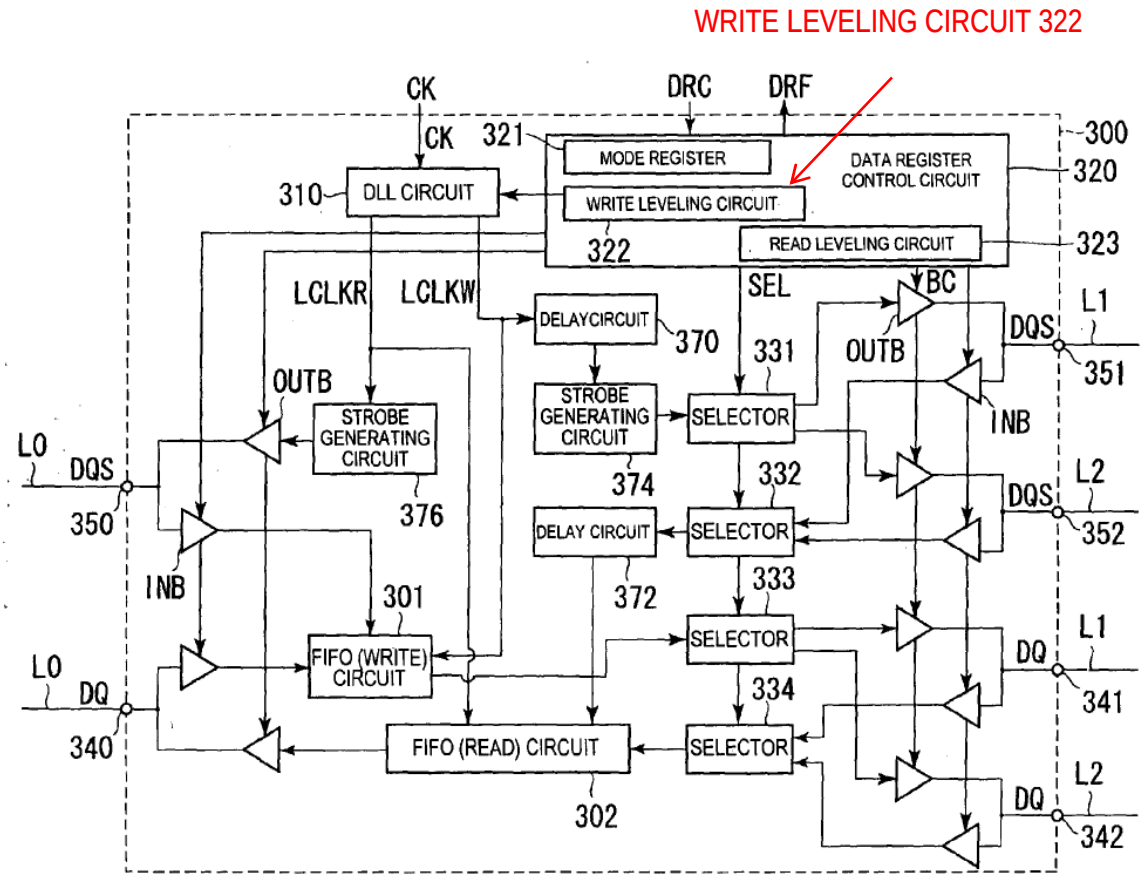


FIG.5

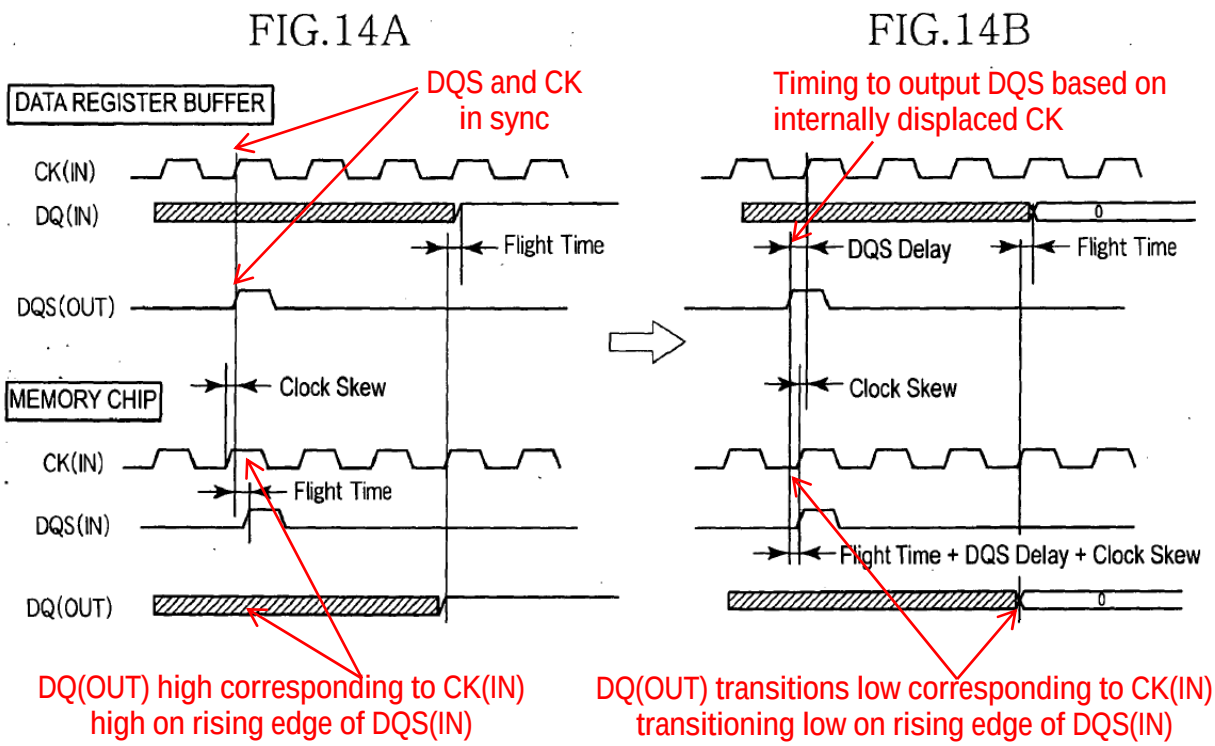
The Petitioner's "first signal from the module controller" is "the clock signal CK from the module controller" in relation to Saito's write leveling circuit 322. The Petitioner's "second signal from the memory bus" is "the data signal DQ from the memory bus" in in relation to Saito's write leveling circuit 322.

Thus, according to the Petitioner's mapping, the Petitioner's "time interval determination circuit" (Saito's write leveling circuit 322) should "generate a delay signal indicating a time interval between" the Petitioner's "first signal from the module controller" (clock signal CK from the module controller) and the

Petitioner's "second signal from the memory bus" (data signal DQ from the memory bus), but the Petition fails to address this "time interval between the first and second signal."

In an incomplete manner, the Petition only asserts that Saito's write leveling circuit 322 uses the Petitioner's "first signal" and "second signal" "to generate delay signals that the data register buffers then use during normal read operations to delay read data signals." (Pet., 42.) Nowhere here does the Petition identify a "*time interval between* the first and second signal," as required by claim 5.

Instead, as discussed above in Section VI.A.1.b and illustrated in annotated Figs. 14A-B reproduced again below, Saito discloses sending a DQS signal to a memory chip from the data register buffer in synchronization with the CK signal. The memory chip outputs a DQ signal reflecting the state of the CK signal received by the memory chip on the rising edge of the DQS signal. An internal clock, LCLKW, is displaced until the memory chip outputs a DQ signal reflecting a transition of the state of the of the CK signal received by the memory chip on the rising edge of the DQS signal. The displacement of the internal clock at this transition of DQ can be stored and represents synchronous receipt of the CK signal and DQS signal at the memory device. Saito does not disclose measuring the time difference between receipt of the DQ input from the memory bus and the CK input from the command/address/control register buffer.



Moreover, measuring the difference between the time of receipt of the CK signal and the DQ signal does not provide any meaningful information in Saito's S4-Write Leveling operation. The only timing adjustment in Saito's S4-Write Leveling is based on the *state* of the DQ signal not the *timing* of the DQ signal. Therefore, the Petition fails to demonstrate that Saito discloses that the respective buffer circuit comprises: "a time interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first and second signal," as required by claim 5.

The Petition does not rely on Swain for the recitations of claim 5. Furthermore, Swain (even in combination with Saito) is silent regarding "a time

interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first and second signal," as required by claim 5. Therefore, the Petitioner's proposed ground of unpatentability of claim 5 based on Saito and Swain is deficient.

3. Independent Claim 12

Claim 12 requires, in part:

> a time interval determination circuit to determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory bus[.]

The Petitioner asserts that Saito and Swain render this recitation obvious, relying on its analysis of claim 1 and its belief that claim 12 "merely labels some of the circuitry and signals discussed above." (Pet., 45.) The Petitioner is mistaken.

Different from claim 1, claim 12 requires determining a more specific time interval: "a time interval between a first signal received from the module controller and a second signal received from the memory bus." The Petition makes no showing that this specific time interval is determined with requisite particularity.

The Petitioner's "time interval determination circuit" is Saito's write leveling circuit 322 (Pet., 45), which is shown in Fig. 5. The Petitioner's "first signal from the module controller" is "the clock signal CK from the module

controller" in relation to Saito's write leveling circuit 322. The Petitioner's "second signal from the memory bus" is "the data signal DQ from the memory bus" in in relation to Saito's write leveling circuit 322.

Thus, according to the Petitioner's mapping, the Petitioner's "time interval determination circuit" (Saito's write leveling circuit 322) should "determine a time interval between" the Petitioner's "first signal from the module controller" (clock signal CK from the module controller) and the Petitioner's "second signal from the memory bus" (data signal DQ from the memory bus), but the Petition fails to address this "time interval between receiving a first signal . . . and a second signal."

In an incomplete manner, the Petition only asserts that Saito's write leveling circuit 322 uses the Petitioner's "first signal" and "second signal" "to generate delay signals that circuitry in the data register buffers ("*delay circuit*") then use during normal read operations to delay read data signals." (Pet., 45.) Nowhere here does the Petition identify a "*time interval between* receiving a first signal . . . and a second signal," as required by claim 12. (*See* Section VI.A.2 above.)

The Petition does not rely on Swain for the recitations of claim 12. Furthermore, Swain (even in combination with Saito) is silent regarding "a time interval determination circuit to determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory

bus," as required by claim 12. Therefore, the Petitioner's proposed ground of unpatentability of claim 12 based on Saito and Swain is deficient.

For at least the reasons set forth above, the Petitioner's proposed obviousness ground of unpatentability for claims 1-5, 12-14, 19 and 20 as being obvious over Saito and Swain is deficient, and the Patent Owner respectfully requests that the Board deny *inter partes* review based on Ground A.

B. Ground B – Saito In View Of Swain and Kim Fails To Render Obvious Claims 3, 13 And 14

The Petitioner additionally proposes Ground B for the unpatentability of claims 3, 13 and 14 over Saito in view of Swain in further view of Kim. (Pet., 49-53.) However, in this Ground, the Petitioner does not further address the recitations of claims 1 and 12 discussed above in Sections VI.A.1 and VI.A.3. For each of the reasons set forth above in Sections VI.A.1 and VI.A.3, the Petitioner's proposed grounds of unpatentability of claims 3, 13 and 14 over Saito in view of Swain are deficient, and Kim does not make up for the deficiencies of Saito and Swain. Therefore, the Petitioner's proposed ground of unpatentability of claims 3, 13 and 14 over the Saito-Swain-Kim combination is similarly deficient.

VII. THE PATENT OWNER'S FINAL COMMENTS

The Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is

instituted. Additionally, the Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

VIII. CONCLUSION

For the foregoing reasons, the Board should deny this *inter partes* review.

Dated: April 30, 2017

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Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Patent Owner's Preliminary Response has 9,150 words (as counted by the "Word Count" feature of the Microsoft Word™ word-processing system), exclusive of "a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing."

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CERTIFICATE OF SERVICE

I hereby certify that the attached Patent Owner's Preliminary Response was served as of the below date via e-mail by agreement to the following counsel of record for the Petitioner:

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