Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-12)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	Filed herewith
Filing Date	February 7, 2017
First Named Inventor	HYUN LEE
Title	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	NT003C2

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date	February 6, 2017
Name	Jamie J. Zheng	Telephone	650-521-4828
Registration Number	51,167		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/82B(07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☐ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

☐ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (*e.g.,* a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	
Name		Telephone	
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number
:

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number.**

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NT003C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1600**

Electronic Acknowledgement Receipt

EFS ID:	28281218
Application Number:	15426064
International Application Number:	
Confirmation Number:	9117
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NT003C2
Receipt Date:	07-FEB-2017
Filing Date:	
Time Stamp:	02:12:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1600
RAM confirmation Number	020717INTEFSW02140500
Deposit Account	505963
Authorized User	Jamie Zheng

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2017-02-06_ApplicationDataSheet_NT003C2.pdf	1437534 d0daf3195b52a7287d90bcefd4251b3473d52666	no	6
Warnings:					
Information:					
2		2017-02-06_Specification_NT003C2.pdf	258161 c9bd6c352f547db46740eff4a11989e79add4cf6	yes	35

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	30
Claims	31	34
Abstract	35	35

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2017-02-06_Drawings_NT003C2.pdf	316914 4df3bda8f4b6e838008259aec8a2188059870f69	no	26
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
4	Oath or Declaration filed	2013-10-15_Declaration_Signed_NT003US.pdf	201957 077e7a3e75ea46a46ebcf4c6382d25028cb4b7b3	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

5	Power of Attorney	2017-02-06_AIA82A_transmittal_POA_NT003C2.pdf	195966 ffded8c34dcb6497a03b4d9a9583c7f365d39c1f	no	3
Warnings:					
Information:					
6	Power of Attorney	AIA_General_POA_Netlist.pdf	133545 f8258889ee9edc63b1cc17705b3158faaed49e9e	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	34870 4c15ce04e4f9af2a03c5eacf91ea057bfa85c74b	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2578947	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NT003C1
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Ladera Ranch	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	21 Thalia		
Address 2			
City	Ladera Ranch	State/Province	CA
Postal Code	92694	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NT003C1
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address	jz@jzpatent.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS		
Attorney Docket Number	NT003C1	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	26	**Suggested Figure for Publication (if any)**	6

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	14846993	2015-09-07

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NT003C1
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

Prior Application Status: Patented (Remove)

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14846993	Continuation of	13952599	2013-07-27	9128632	2015-09-08

Prior Application Status: Expired (Remove)

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13952599	non provisional of	61676883	2012-07-27

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. (Add)

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

(Remove)

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Priority Claimed
			● Yes No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. (Add)

Authorization to Permit Access:

Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NT003C1
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information:			
Address 1	175 Technology, #150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address	nwhitley@netlist.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NT003C1
	Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2017-02-06
First Name	Jamie	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

CLAIM OF PRIORITY

[0001] The present application is a continuation of U.S. Pat. App. No. 14/846,993, to be issued as U.S. Pat. No. 9,563,587, which is a continuation of U.S. Pat. App. No. 13/952,599, filed July 27, 2013, issued as U.S. Pat. No. 9,128,632, which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on July 27, 2012. Each of the above applications is incorporated by reference herein in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] The present application is related to commonly-owned U.S. Pat. App. No. 14/715,486, filed on May 18, 2015; U.S. Pat. App. No. 13/970,606, filed on August 20, 2013; U.S. Pat. App. No. 12/504,131, filed on July 16, 2009, now U.S. Pat. No. 8,417,870; U.S. Pat. App. No. 12/761,179, filed on April 15, 2010, now U.S. Pat. No. 8,516,185; U.S. Pat. App. No. 13/287,042, filed on November 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. Pat. App. No. 13/287,081, filed on November 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

FIELD

[0003] The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

BACKGROUND

[0004] With recent advancement of information technology and widespread use of the Internet to store and process information, more and more demands are placed on the

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acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

[0005] The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

[0006] The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

[0007] In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

[0008] For memory devices in such as a memory module to be properly accessed, distribution of control signals and a control clock signal in the memory module is subject to

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strict constraints. In some conventional memory modules, control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

[0009] In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram illustrating a memory system including at least one memory module according to one embodiment.

[0011] FIGS. 2A-2D are each a diagrams illustrating interactions among components in a a memory module according to certain embodiments.

[0012] FIG. 3 is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

[0013] FIGS. 4A-4B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

[0014] FIGS. 5A-5B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

[0015] FIG. 6 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

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[0016] FIG. 7 is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

[0017] FIG. 8 is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

[0018] FIG. 9 is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

[0019] FIGS. 10A-10C are diagrams illustrating a metastability detection circuit according to certain embodiments.

[0020] FIGS. 10D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

[0021] FIGS. 11A-11B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

[0022] FIGS. 12A-12B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

[0023] FIG. 13 is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

[0024] FIG. 14 is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

[0025] FIG. 15 a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

[0026] FIG. 16 a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

[0027] FIG. 17 is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.

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[0028] FIG. 18 is a flowchart illustrating a method for data edge alignment according to embodiments.

[0029] FIG. 19 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

DESCRIPTION OF EMBODIMENTS

[0030] A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

[0031] The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a

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respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

[0032] In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

[0033] Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

[0034] FIG. 1 shows a system 100 including a memory controller (MCH) 101 and one or more memory modules 110 coupled to the MCH by a memory bus 105, according to one embodiment. As shown, the memory bus includes C/A signal lines 120 and groups of system data/strobe signal lines 130. Also as shown, each memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114. Each memory module 110 further includes a module control circuit (module controller or module control device) 116 coupled to the MCH 101 via the C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to the MCH 101 via respective groups of system data/strobe signal lines 130. In one embodiment, the memory devices 112, the module

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control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119.

[0035] In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module 110 may vary. For example, as shown, each memory module 110 may include four ranks of memory devices 112. In another embodiment, the memory module 110 may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices 112.

[0036] In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices 112. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

[0037] Furthermore, the memory devices 112 may include any type of memory devices. For example, in one embodiment, the memory devices 112 may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module 110 may include a dual in-line memory module (DIMM).

[0038] Referring to FIG. 2A, which illustrates one memory module 110 according to an embodiment, the module control device 116 receives system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal lines 120 and generates module command signals and module control signals based on memory commands from the system. The module control device 116 also received a system clock MCK and generates a module clock signal CK in response to the system

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clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{MCK}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{CK}$.

[0039] Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

[0040] Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

[0041] Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory

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controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices 118 via respective module control signal lines 230. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices 118 via the module control signal lines and decoded/processed at the isolation devices.

[0042] Module control device 116 transmits the module command signals to the memory devices 112 via module C/A signal lines 220. The memory devices 112 operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices 118 via module control signal lines 230. As shown in FIG. 2, at least some of the memory devices in a same rank share a same set of module C/A signal lines 220, and at least some of the isolation devices 118 share a same set of module control signal lines 230.

[0043] As shown n FIGS. 2A and 2B, each rank 114 includes *N* memory devices, where *N* is an integer larger than one. For example, a first rank includes memory devices M_{11}, ..., M_{i1}, $M_{i+1,1}$, ..., M_N, a second rank includes memory devices M_{12}, ..., M_{i2}, $M_{i+1,2}$, ..., $M_{N,2}$, and so on. In one embodiment, the memory devices 112 are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines 130 and including at least one memory device from each rank. For example, memory devices M_{11}, M_{12}, M_{13}, and M_{14} form a first group of memory devices, memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} form an ith group of memory devices, and so on.

[0044] As shown, the isolation devices 118 are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines 130 and the respective groups of memory devices. For example, isolation device ID-1 among the isolation devices 118 is associated with the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14} and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices, isolation devices ID-*i* among the isolation

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devices 118 is associated with the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} and is coupled between the group of system data/strobe signal lines 130-i and the ith *group* of memory devices, and so on.

[0045] In one embodiment, each group or sets of memory devices are coupled to the associated isolation device 118 via a set of module data/strobe lines 210. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device 118 via a same set of module data/strobe lines 210 (as shown in FIG. 2A) or via respective subsets of module data/strobe lines 210 (as shown in FIG. 2B). For example, as shown in FIG. 2B, in the first group of memory devices, memory devices M_{11} and/or M_{13} form a first subgroup, and memory devices M_{12} and/or M_{14} form a second subgroup; in the ith group of memory devices, memory devices M_{i1} and/or M_{i3} form a first subgroup, and memory devices M_{i2} and/or M_{i4} form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device 118 via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices M_{11} and/or M_{13} form the first subgroup are/is coupled to the isolation device ID-1 via the corresponding first subset of module data/strobe lines YA-1, and memory devices M_{12} and/or M_{14} form the second subgroup are/is coupled to the isolation device ID-1 via the corresponding second subset of module data/strobe lines YA-2.

[0046] In one embodiment, the isolation devices 118 are in the data paths between the MCH 101 and the memory module 110 and include data buffers between the MCH 101 and the respective groups of memory devices. In one embodiment, each isolation device 118 is configured to select a subgroup in the respective group of memory devices to communicate data with the MCH 101 in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH 101. Further, each isolation devices 118 is configured to isolate unselected subgroup(s) of memory devices

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from the MCH 101 during write operations, so that the MCH sees a load on each data line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

[0047] In one embodiment, the isolation devices 118 are distributed across the memory module 110 or the module board 119 in positions corresponding to the respective groups of memory devices. For example, isolation device ID-1 is disposed in a first position corresponding to the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and isolation device ID-*i* is disposed in an ith position separate from the first position and corresponding to the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4}. In one embodiment, the first position is between the first group of memory devices and an edge 201 of the module board 119 where connections (not shown) to the data/strobe signal lines 130 are placed, and i^{th} position is between the ith group of memory devices and the edge 201 of the module board 119. In one embodiment, the isolation devices 118 are distributed along the edge 201 of the memory module 110. In one embodiment, each isolation device 118 is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines 210, the module C/A signal lines 220, and the module control signal lines 230 include signal traces formed on and/or in the module board 119.

[0048] As an option, memory module 110 may further include a serial-presence detect (SPD) device 240, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module 110. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory module 110, a memory density per rank, a number of memory device on the memory module 110, and a memory density per memory device, etc. A basic input/output system (BIOS) of system 100 can be informed of these attributes of the memory module 110 by reading from the SPD 240 and can use such data to configure the MCH 101 properly for maximum reliability and performance.

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[0049] In certain embodiments, the SPD 240 and/or the control circuit 116 store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit 116, input and output signals electrical and logical level control information for the control circuit 116, etc. In certain embodiments, the SPD 240 contains a system view of the module 110 which can be different from an actual physical construction of the module 110. For example, the SPD 240 stores at least one memory operation parameter that is different from a correspondng memory operation parameter in a system memory controller setting. The SPD 240 may also store at least on data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

[0050] Thus, in certain embodiment, in the memory module 110, C/A signals representing a memory command are received and buffered by the module control circuit 116, so that the MCH sees only the module control circuit 116 as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130. Thus, MCH 101 does not directly operate or control the memory devices 112. As far as data/strobe signals are concerned, the MCH 101 mainly sees the isolation devices 118, and the system 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101.

[0051] In certain embodiments, the memory module 110 is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM). In certain embodiments, the control circuit 116 includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.

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[0052] As shown in FIG. 2C, in certain embodiments, the control circuit 116 transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices 118, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

[0053] For example, load reduction mechanism in the isolation devices 118 would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller 101. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller 101 over the interface between the memory devices 112 and the associated isolation devices 118. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller 101, which may cause silent system failure.

[0054] Moreover, clock skew amongst the memory devices 112 and the associated isolation devices 118 due to the distributed architecture of the memory module 110 can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

[0055] To address at least some of the above issues, in certain embodiments, as shown in FIG. 2D, the control circuit 116 transmits registered C/A signals to the memory devices 112, and transmits the module control signals and the module clock signal to the data buffers 118, in a fly-by arrangement. The memory devices 112 do not receive the module clock signal from the control circuit 116. Instead, each data buffer 118 regenerates the clock that is used by the respective set of memory devices 112. Each Data buffer 118 is thus

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responsible for providing a correct data timing interface between the respective set of memory devices 112 and the system memory controller 101. Each data buffer 118 is also responsible for providing the correct control signal timing between the control circuit 116 and the respective set of memory devices 112.

[0056] Thus, the memory module 110 in FIG. 2D allows a locally synchronized operation for each respective set of memory devices 112, which can correspond to a nibble or a byte of a DDR data bus between the memory module 110 and the system memory controller 101. Also, signal interface between each data buffer 118 and the respective set of memory devices 112 can be synchronized. In one embodiment, each data buffer 118 has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices 112, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller 101, programmable phase adjustment related to at least one control signal that is coupled to the control circuit 116. The locally synchronized operation also makes it easier for each data buffer 118 to perform self-testing of the associated set of memory devices 112, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Patent 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

[0057] In certain embodiments, operations of the isolation devices 118 are controlled by the module control signals from the module control circuit 116, which generates the module control signals according to the C/A signals received from the MCH. Thus, the module control signals need to be properly received by the isolation devices 118 to insure their proper operation. In one embodiment, the module control signals are transmitted together with the module clock signal CK, which is also generated by the module control circuit 116 based on the system clock signal MCK. The isolation circuits 118 buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices 118 are distributed across the memory module, the module control signal lines 230 can stretch across the memory module 110, over a distance of

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several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits 118 includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

[0058] Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n-1) in the exemplary configuration shown in FIG. 2. In other words, a same set of module control signals may reach different isolation devices 118 at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

[0059] With the isolation devices 118 receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to time the transmission of read data signals to the MCH 101 from the isolation devices 118. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a

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subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100, as explained in more detail below.

[0060] More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0061] In one embodiment, as shown in FIG. 3, each group of signal lines 130 include a set of *n* data (DQ) signal lines 322 each for transmitting one of a set of data signals DQ_0, DQ_1, …, DQ_{n-1}, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of *n* module data signal lines Y_0, Y_1, …, Y_{n-1} and at least one module strobe signal line Y_{DQS}. When the subsets of memory devices are coupled to the associated isolation device 118 via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. 2B. Each subset of module data/strobe lines YA include a set of *n* first module data lines YA_0, YA_1, …, YA_n and at least one first module strobe signal line YA_{DQS}; and each subset of module data/strobe lines YB include a set of *n* second module data lines YB_0, YB_1, …, YB_n and at least one second module strobe signal line YB_{DQS}.

[0062] Each isolation device 118 includes a set of DQ routing circuits 320 coupled on one side to respective ones of the set of *n* DQ signal lines 322, and on another side to respective ones of the respective set of *n* module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines YA_0, YA_1, …, YA_n and the second module data lines YB_0, YB_1, …, YB_n. Each isolation device 118 further includes an ID control circuit 310 coupled on one side to the at least one DQS signal line 324, on another side to the one or more module strobe signal lines Y_{DQS}, or the first module strobe

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signal line YA_{DQS} and second module strobe signal line YB_{DQS}. The ID control circuit 310 also receives the module clock signal CK and the module control signals via the module control signal lines 230, and outputs ID control signals 330 to the DQ routing circuits 320, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module control signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK0. Each DQ routing circuit 320 is configured to enable data communication between the respective DQ signal line 322 with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

[0063] In certain embodiments, the ID control circuit 310 also provides a delay signal DS, which is used by the DQ routing circuits 320 to align read data output by the isolation device 118 with read data output by the other isolation devices 118, as explained in further detail below. In certain embodiments, the ID control circuit 310 regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK0 and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

[0064] The memory devices 112 are coupled to the isolation devices 118 via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. 4A, memory devices M_{11}, M_{12}, M_{13}, and M_{14} in the first group of memory devices can be coupled to the isolation device ID-1 via a same set of module data lines $Y\text{-}1_0$, $Y\text{-}1_1$, …, $Y\text{-}1_{n-1}$ and module strobe line $Y\text{-}1_{DQS}$. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which can be different with respect to different subgroups of memory devices.

[0065] Alternatively, as shown in FIG. 4B, memory devices M_{11} and M_{13}, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines $YA\text{-}1_0$, $YA\text{-}1_1$, …, $YA\text{-}1_n$ and module strobe line $YA\text{-}1_{DQS}$ and

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memory devices M_{12} and M_{14}, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines $YB\text{-}1_0$, $YB\text{-}1_1$, ..., $YB\text{-}1_n$ and module strobe line $YB\text{-}1_{DQS}$. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board 119. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards 119, or stacked over each other, and/or over the associated isolation device.

[0066] Multiple memory devices having a data width that is less than a data width of the isolation devices 118 may be used in place of one of the memory devices 112, which has the same data width as that of the isolation devices. For example, as shown in FIG. 5A, two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ may be used in place of the memory device M_{11}. Each of the two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ has a data width of 4, and together they act like a memory device M_{11} of a data width of 8. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_0$, ..., $YA\text{-}1_3$ and module strobe line $YA\text{-}1_{DQS\text{-}1}$ while memory circuit $M_{11\text{-}2}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_4$, ..., $YA\text{-}1_7$ and module strobe line $YA\text{-}1_{DQS\text{-}2}$.

[0067] In another embodiment, as shown in FIG. 5B, four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ may be used as the memory device M_{11}. Each of the four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ has a data width of 4, and together they act like a memory device M_{11} of a data width of 16. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_0$, ..., $YA\text{-}1_3$ and module strobe line $YA\text{-}1_{DQS\text{-}1}$ while memory device $M_{11\text{-}2}$ is coupled to the isolation device ID-1 via module data lines $YA\text{-}1_4$, ..., $YA\text{-}1_7$ and module strobe line $YA\text{-}1_{DQS\text{-}2}$, and so on.

[0068] FIG. 6 illustrates the ID control circuit 310 in an isolation device 118. As shown, the ID control circuit 310 includes a clock buffer 610 to receive the module clock signal CK from the module control device 116, and to output a module clock signal CK0. The ID control circuit 310 further includes a strobe routing circuit 620 that are coupled on one side to the corresponding system DQS signal line 324 and on another side to the corresponding

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module DQS signal lines YA_{DQS} and YB_{DQS}. The ID control circuit 310 further includes a receiver circuit 630 with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit 310 further includes a command processing circuit 640 that provides the received, decoded, and/or otherwise processed module control signals 330 to the DQ routing circuits 320 and the strobe routing circuit 620 either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits 320 and the strobe routing circuit 620 to selectively enabling data communication between the MCH 101 and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

[0069] The strobe routing circuit 620 also buffers strobe signals received from either the MCH 101 or the memory devices 112, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits 320. In one embodiment, the ID control circuit 310 further includes a delay control circuit 650 that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit 320 and the strobe routing circuit 620. The delay amount is provided to the DQ routing circuit 320 and the strobe routing circuit in a delay signal DS.

[0070] In a receiver circuit 630, the respective MCS is received in accordance with the module clock signal CK0. In one embodiment, receiver circuit 630 samples the respective MCS using rising (or falling) edges of the module clock CK0. Since the isolation devices 118 are distributed across the memory module 110 at positions corresponding to the respective groups of memory devices, the module control signal lines 230 that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as shown in FIG. 7. As the MCS and CK0 travel along their respective module control signal lines 710 and 720, they can become misaligned with each other when they reach the input pins 730 of an isolation device 118.

[0071] For example, a module control signal, like the MCS 810 shown in FIG. 8, can be

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perfectly aligned with the module clock signal CK, with a rising edge 801 of the module clock signal CK being at a center of a data eye 802, when the MCS signal and the clock signal leave the module control circuit 116. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS 820 with respect to the CK signal, i.e., the rising edge 801 of the clock signal is near a left edge of a data eye of the MCS 820, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS 830, can be shifted with respect to the module clock signal such that a rising edge 801 of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS 840, can be so shifted with respect to the module clock signal such that a rising edge 801 of the clock signal falls in the glitches 803 at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

[0072] In one embodiment, as shown in FIG. 9, a receiver circuit 630 includes a metastability detection circuit (MDC) 910 to determine a metastability condition in a corresponding module control signal MCS0. In one embodiment, the MDC 910 generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS0. The MDC 910 also generates one or more metastability indicators and outputs the one or more metastability indicators via lines 912 and/or 914.

[0073] The receiver circuit 630 further includes a signal selection circuit 920 that receives the module clock CK and the at least one delayed version of the module clock via signal lines 916. The signal selection circuit 920 also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines 918. The signal selection circuit 920 selects a clock signal CK_i from among the module clock CK and the at least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit 920 may also select an MCS signal MCS_i from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.

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[0074] The receiver circuit 630 further includes a sampler or register circuit 930 that samples the selected module control signal MCS_i according to the selected clock signal CK_i and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit 640 for further processing (if needed) before being provided to the DQ routing circuits 320 and DQS routing circuit 620.

[0075] FIG. 10A illustrates an MDC 910 according to one embodiment. As shown, the MDC 910 includes a delay circuit 1012 that generates a delayed version MCS1 of the corresponding MCS0 by adding a predetermined amount of delay (e.g., 10ps) to MCS0. MDC 910 also includes a delay circuit 1016 that generates a delayed version CK1 of the clock signal CK0 by adding a predetermined amount of delay to CK0. In one embodiment, CK1 is delayed from CK0 by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC 910 further includes a sampler circuit 1042 that samples MCS1 according to CK0 and outputs a sampled result A, a sampler circuit 1044 that samples MCS0 according to CK0 and outputs a sampled result B, and a sampler circuit 1046 that samples MCS0 according to CK1 and outputs a sampled result C. The MDC 910 further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z1 and Z2 based on the sampled results A, B, and C.

[0076] In one embodiment, Z1 is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., $Z1 = \overline{A \oplus B}$, and Z2 is the result of another logic operation on the sampled results, e.g., $Z2 = \overline{B \oplus C}$. Thus, as shown in FIG. 10B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge 1061 of CK0 is close to the right side of a data eye where gliches at the edges of the data eyes can make C unpredicatable, A and B can be in agreement (i.e., Z1 is true) while B and C are likely not in agreement (i.e., Z2 is false). FIG. 10 C illustrates a metastability condition when there is insufficient set-up time. As shown in FIG. 10C and Table 1 below, a rising clock edge 1061 of CK0 is close to the left side of a data eye where gliches at the edges of the data eyes can make A unpredicatable. Thus, A and B can be in disagreement so Z1 is false while B and C can be in agreement so Z2 is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge

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1061 of CK0 and the rising clock edge 1062 of CK1 are near the middle of an MCS0 data eye so there is no metastability issues and both Z1 and Z2 are true, as shown in Table 1.

[0077] FIG. 10D illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1071 that selects between CK0 and CK1 based on the metastability indicator Z1, and a second multiplexor 1072 that selects between MCS0 and MCS1 based on the metastability indicator Z2. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, Z1=1 and Z2=0, and MCS1 is output from multiplexor 1071 while CK0 is output from multiplexor 1072. Sampler 930 thus samples MCS1 according to the rising edges of CK0. Thus, more hold time is provided to mitigate the metastability condition since MCS1 is shifted from MCS0 toward the right.

[0078] On the other hand, where a metastability condition of insufficient set-up time occurs, Z1=0 and Z2=1, and CK1 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. Sampler 930 thus samples MCS0 according to the rising edges of CK1. Since CK1 is shifted from CK0 toward the right, more set-up time is provided to mitigate the metastability condition.

[0079] In the case when no metastability is detected, Z1=1 and Z2=1, and CK0 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

Table 1 Metastability Detection and Signal Selection

Sampler Output			MS Indicators		MS Condition	Signal Selection	
A	B	C	Z1	Z2		CK	MCS
D1	D1	D2	1	0	insufficient hold time	CK0	MCS1
D1	D2	D2	0	1	insufficient set-up time	CK1	MCS0
D1	D1	D1	1	1	no metastability	CK0	MCS0

[0080] FIGS. 10A-10D illustrate a relatively simple implementation of the metastability detection circuit (MDC) 910 where only three different sample points are provided to

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detect metastability condition in the module control signal. In general, the MDC 910 may generate more delayed versions of the module clock signal CK0 and/or the corresponding module control signal MCS0, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. 11A, the MDC 910 can include a plurality of delay circuits 1102 that generate *m* delayed versions of MCS0, e.g., MCS1, MCS2, … MCS*m*, and *m* delayed versions of CK0, e.g., CK1, CK2, …, CK*m*. The MDC 910 can include sampler circuits 1104 that sample MCS0 according to CK0, CK1, …, CK*m*, respectively, and sampler circuits 1104 that sample MCS0, MCS1, MCS2, … MCS*m* according to CK0, respectively. The outputs of the samplers 1104 are provided to a logic circuit 1120, which determines a metastability condition in MCK0 based on the sampler outputs using, for example, a majority decision logic. The logic circuit 1120 outputs a first metastability indicator on line(s) 912 and a second metastability indicator on line(s) 914.

[0081] FIG. 11B illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1171 that selects between CK0, CK1, …, CK*m* based on the metastability indicator provided on line(s) 912, and a second multiplexor 1172 that selects between MCS0, MCS1, …, MCS*m* based on the metastability indicator provided on line(s) 914, such that the rising edges of the selected clock signal, e.g., Ck*i*, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCS*i*. The selected signals MCS*i* and Ck*i* are provided to the sampler 930, which samples MCS*i* according to the rising edges of CK*i*.

[0082] As stated above, in certain embodiments, since the isolation devices 118 are in the data paths between the MCH 101 and the respective groups of memory devices 112, the MCH 101 does not have direct control of the memory devices 112. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior

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write operation, as discussed further below.

[0083] FIG. 12A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit 116 at time t1, the module control circuit 116 outputs one or more enable signals EN at time t2 in response to the write commands. The one or more enable signals are received by an isolation device 118 at time t3, which afterwards receives one or more strobe signal DQS from the MCH 101 at time t4. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system 100, and is controllable by the MCH 101 and knowable to the isolation device 118. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device 118 since both these signals are received by the isolation device. Based on such determination, the isolation device 118 can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device 118 to properly time transmission of read data to the MCH, as explained further below.

[0084] FIG. 12B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit 116 at time t5, the module control circuit 116 outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device 118 at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. Note that the same enable signal may be received by another isolation device 118 at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices 118.

[0085] With knowledge of the time interval between t7 and t5, which should be about the

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same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101 via the respective group of data/strobe signal lines 130, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system 100.

[0086] The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit 650 in the ID control circuit 310, as shown in FIG. 6. According to one embodiment, as shown in FIG. 13, the delay control circuit 650 includes a peramble detector 1310 to detect a write preamble in the DQS, a flip-flop circuit 1320 having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK0, and a counter circuit 1330 having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit 1320. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

[0087] FIG. 14 illustrates a DQ or DQS routing circuit 320 or 620 according to an embodiment. As shown, the DQ/DQS routing circuit 320/620 includes a DQ/DQS pin 1401 that is coupled to the corresponding DQ/DQS signal line 322/324, a set of one or more DQS pins 1402 that is coupled to a corresponding module DQ/DQS line(s) Y/Y_{DQS}, or YA/YA_{DQS} and YB/YB_{DQS}. The DQ/DQS routing circuit 320/620 further includes a write strobe buffer 1410 that buffers write data/strobe, and a write data/strobe receiver 1420 that samples the write data/strobe. The DQ/DQS routing circuit 320/620 further includes a plurality of write paths 1430 that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

[0088] The DQS routing circuit further includes a plurality of read paths 1450 that are selectable by the one or more of the module control signals. Output from the seleted read path is delayed in a delay circuit 1460 by an amount controlled by the delay signal DS, and

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sampled by a sampler circuit 1470. The sampled read data/strobe is transmitted by transmitter 1480 onto the corresponding data/strobe signal line 322/324 via the DQ/DQS pin 1401.

[0089] FIG. 15 illustrates a DQS routing circuit 620 according to an embodiment. As shown, the DQS routing circuit 620 includes a first DQS pin 1501 that is coupled to a corresponding DQS signal line 324, a second DQS pin 1502A that is coupled to a corresponding module DQS line YA_{DQS}, a third DQS pin 1502B that is coupled to a corresponding module DQS line YB_{DQS}. The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe path includes a write strobe buffer 1510 that buffers a write strobe, a write strobe receiver 1520 that samples the write strobe according to the buffered module signal CK0. The sampled write strobe is provided to the DQ routing circuits 320 as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter 1530A that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YA_{DQS}. The second write strobe path includes the write strobe buffer 1510, the write strobe receiver 1520, and a second write strobe transmitter 1530B that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YB_{DQS}. The first and second write strobe transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0090] The DQS routing circuit further includes a read strobe path coupled between the first DQS pin 1501 and a selected one of the second and third DQS pins 1502A and 1502B. In the read strobe path, a select circuit 1550 (e.g., a multiplexor) selects either a read strobe signal received via DQS pin 1502A or a read strobe signal received via DQS pin 1502B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0. The

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sampled read strobe is provided to the DQ routing circuits 320 as the read strobe RDQS and is transmitted by transmitter 1580 onto the corresponding strobe signal line 324 via the first DQS pin 1501.

[0091] FIG. 16 illustrates a DQ routing circuit 320 according to an embodiment. As shown, the DQ routing circuit 320 includes a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line YA_{DQ}, a third DQ pin 1602B that is coupled to a corresponding module DQ line YB_{DQ}. The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer 1610, a write data receiver 1620 that samples write data according to the write strobe WDQS from the DQS routing circuit 620, and a first write data transmitter 1630A that transmits the write data to one or more memory devices 112 coupled to the module data line YA_{DQ}. The second write data path includes the write data buffer 1610, the write data receiver 1620, and a second write data transmitter 1630B that transmits the write data to one or more memory devices 112 coupled to the module data line YB_{DQ}. The first and second write data transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0092] The DQ routing circuit further includes a read data path coupled between the first DQ pin 1601 and a selected one of the second and third DQ pins 1602A and 1602B. In the read data path, a select circuit 1650 (e.g., a multiplexor) selects either a read data signal received via DQ pin 1602A or a read data signal received via DQ pin 1602B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.

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[0093] FIG. 17 illustrate a delay circuit 1560 or 1660 according to an embodiment. As shown, the delay circuit 1560 or 1660 includes a plurality of delay stages, such as delay stages 1710, 1720, and 1730, each delaying a read data or read strobe signal from the select circuit 1550/1650 by a predetermined amount. The delay circuit 1560 or 1660 further includes a select circuit 1740 (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit 1740, is provided to the sampler circuit 1570 or 1670, either directly or after being buffered by a buffer circuit 1750.

[0094] Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device 118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

[0095] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the

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isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.

[0096] As shown in FIG. 18, a delay signal DS is generated according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.

[0097] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100.

[0098] In certain embodiments, especially the embodiments shown in FIG. 2D, the delay circuits 1560 and 1660 shown in FIGS. 15 and 16 are not needed to provide alignment of the read data. As shown in FIG. 19, the ID control circuit 310 includes a clock regeneration circuit 1920 that regenerates the clock signal CK received from the control circuit 116, according to the delay signal DS. The regenerated clock signals CK0 and CKM each includes a proper amount of delay as compared to the clock signal CK. The clock CK0 is provided to the strobe routing circuit 620 so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer 118 and the respective

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set of memory devices are locally synchronized.

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WE CLAIM:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory command signals; and

memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the subset of the data paths in accordance with the timing information.

2. The memory module of claim 1, wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation.

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Ex. 1032, p. 46

3. The memory module of claim 2, wherein the each respective buffer circuit includes a delay control circuit that determines, during the memory write operation, a time interval between receiving a first signal from the module control device and a second signal from the memory controller, and wherein the timing information includes the time interval.

4. The memory module of claim 3, wherein the each respective buffer circuit further receives a module clock signal and further includes a clock regeneration circuit that regenerates a local clock signal having a programmable phase relationship with the module clock signal, the each respective buffer circuit outputting the local clock signal to the respective set of the plurality of sets of memory devices, the respective set of the plurality of sets of memory devices performing the first memory operation in accordance with the local clock signal.

5. The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

6. The memory module of claim 5, wherein the module command signals include chip select signals that select one memory device in each of the plurality of sets of memory devices to perform the first memory operation.

7. The memory module of claim 5, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

8. The memory module of claim 7, wherein the module command signals include chip select signals that select two memory devices in each of the plurality of sets of memory devices to perform the first memory operation.

9. The memory module of claim 1, wherein the each respective buffer circuit further receives a module clock signal from the module control device and further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

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Ex. 1032, p. 47

10. The memory module of claim 9, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

11. The memory module of claim 10, wherein the module command signals include chip select signals that select one memory device in each of the plurality of sets of memory devices to perform the first memory operation.

12. The memory module of claim 9, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

13. The memory module of claim 12, wherein the module command signals include chip select signals that select two memory devices in each of the plurality of sets of memory devices to perform the first memory operation.

14. The memory module of claim 1, wherein the each respective buffer circuit further receives a module clock signal and further includes a clock regeneration circuit that regenerates a local clock signal having a programmable phase relationship with the module clock signal, the each respective buffer circuit outputting the local clock signal to the respective set of the plurality of sets of memory devices, the respective set of the plurality of sets of memory devices performing the first memory operation in accordance with the local clock signal.

15. The memory module of claim 14, wherein the selected subset of the data paths include a first path for transmitting a strobe signal among the data and strobe signals, the first path including a sampler that samples the strobe signal in accordance with the local clock signal.

16. The memory module of claim 15, wherein the selected subset of the data paths include a second path for transmitting a data signal among the data and strobe signals, the second path including a sampler that samples the data signal in accordance with the sampled strobe signal.

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17. The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

18. The memory module of claim 17, wherein the module command signals include chip select signals that select one memory device in each of the plurality of sets of memory devices to perform the first memory operation.

19. The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

20. The memory module of claim 19, wherein the module command signals include chip select signals that select two memory devices in each of the plurality of sets of memory devices to perform the first memory operation.

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MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

A memory module is operatable in a memory system with a memory controller. The memory module comprises a module control device mounted on the module board to receive command signals from the memory controller and to output module command signals and module control signals, and memory devices mounted on the module board to perform a first memory operation in response to the module command signals. The memory module further comprises a plurality of buffer circuits distributed across a surface of the module board. Each respective buffer circuit is associated with a respective set of the memory devices and includes logic that is configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals through the each respective buffer circuit in accordance with the timing information.

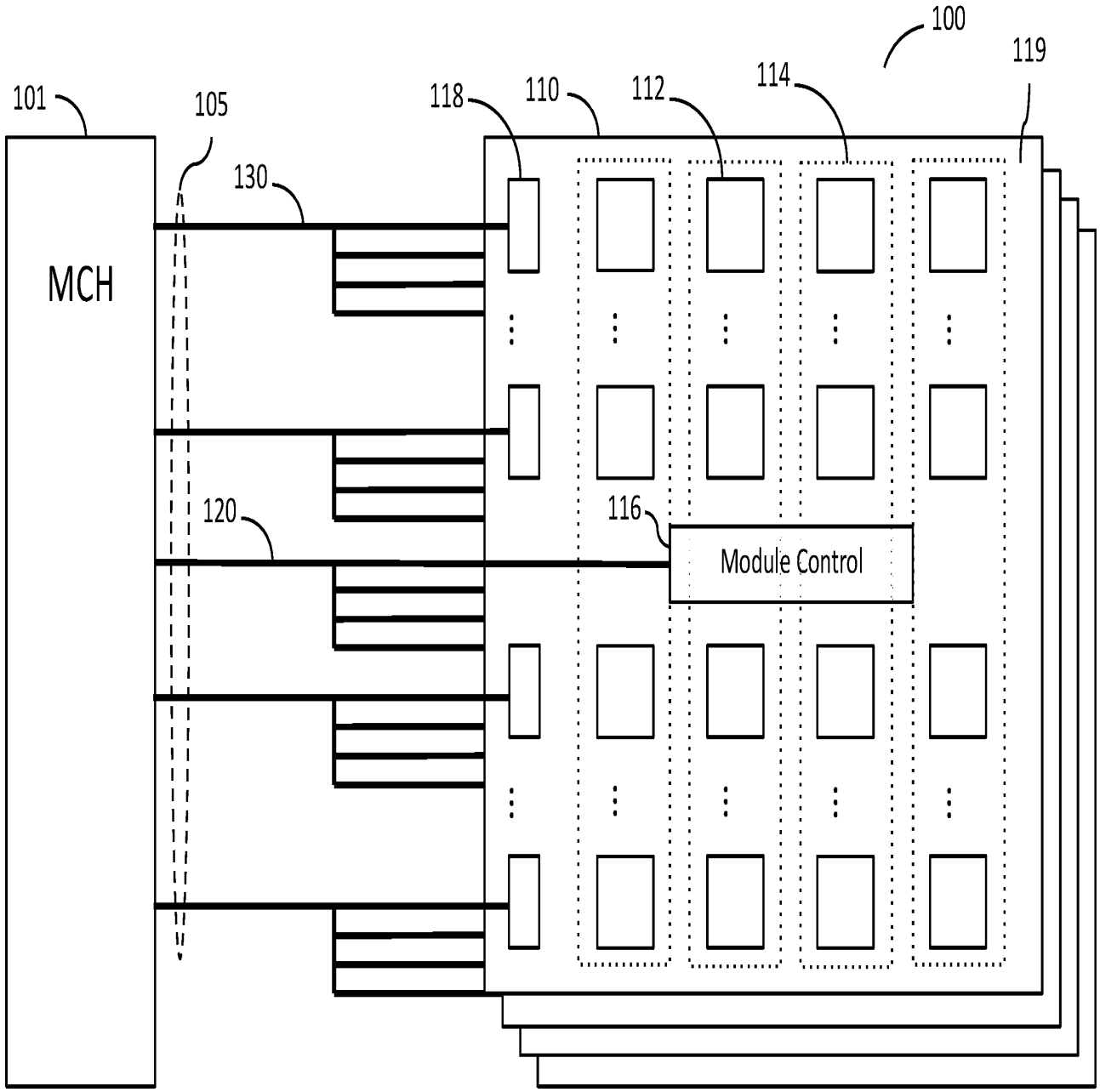

FIG. 1

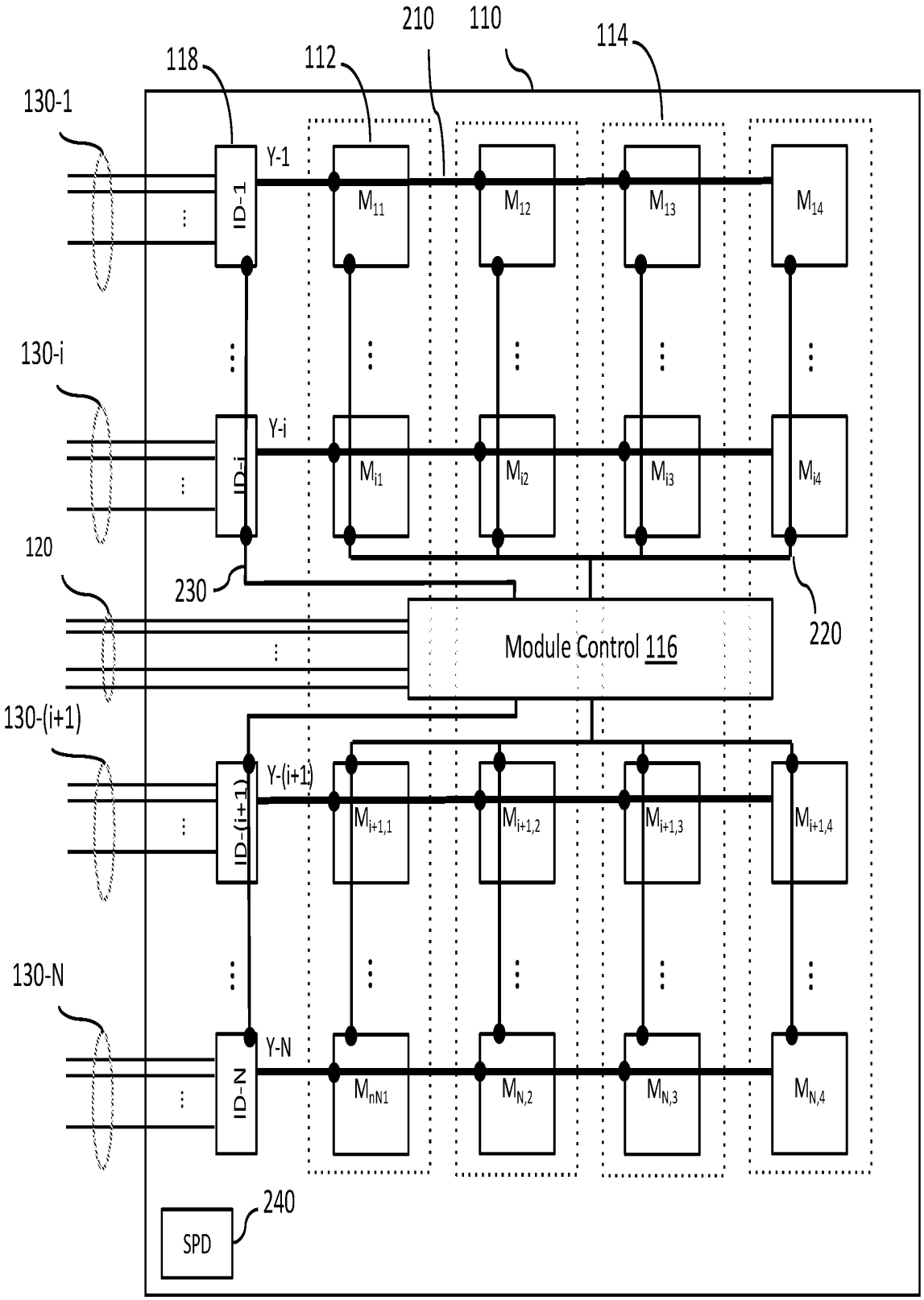
210
110
114
118
112
130-1
Y-1
ID-1
M_{11}
M_{12}
M_{13}
M_{14}
130-i
Y-i
ID-i
M_{i1}
M_{i2}
M_{i3}
M_{i4}
120
230
220
Module Control 116
130-(i+1)
Y-(i+1)
ID-(i+1)
$M_{i+1,1}$
$M_{i+1,2}$
$M_{i+1,3}$
$M_{i+1,4}$
130-N
Y-N
ID-N
M_{nN1}
$M_{N,2}$
$M_{N,3}$
$M_{N,4}$
240
SPD

FIG. 2A

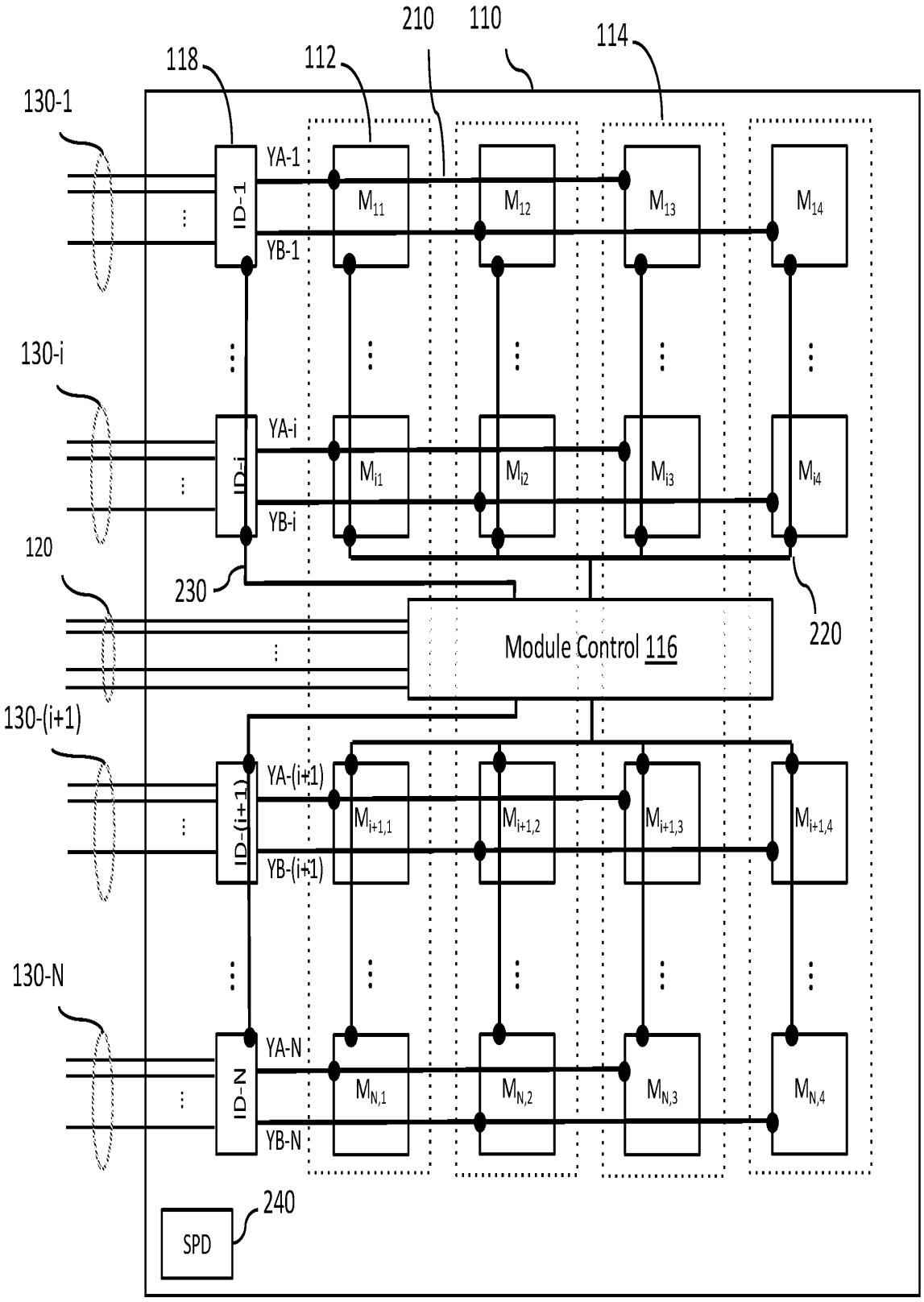
210
110
114
118
112
130-1
YA-1
ID-1
YB-1
M_{11}
M_{12}
M_{13}
M_{14}
130-i
YA-i
ID-i
YB-i
M_{i1}
M_{i2}
M_{i3}
M_{i4}
120
230
220
Module Control 116
130-(i+1)
YA-(i+1)
ID-(i+1)
YB-(i+1)
$M_{i+1,1}$
$M_{i+1,2}$
$M_{i+1,3}$
$M_{i+1,4}$
130-N
YA-N
ID-N
YB-N
$M_{N,1}$
$M_{N,2}$
$M_{N,3}$
$M_{N,4}$
240
SPD

FIG. 2B

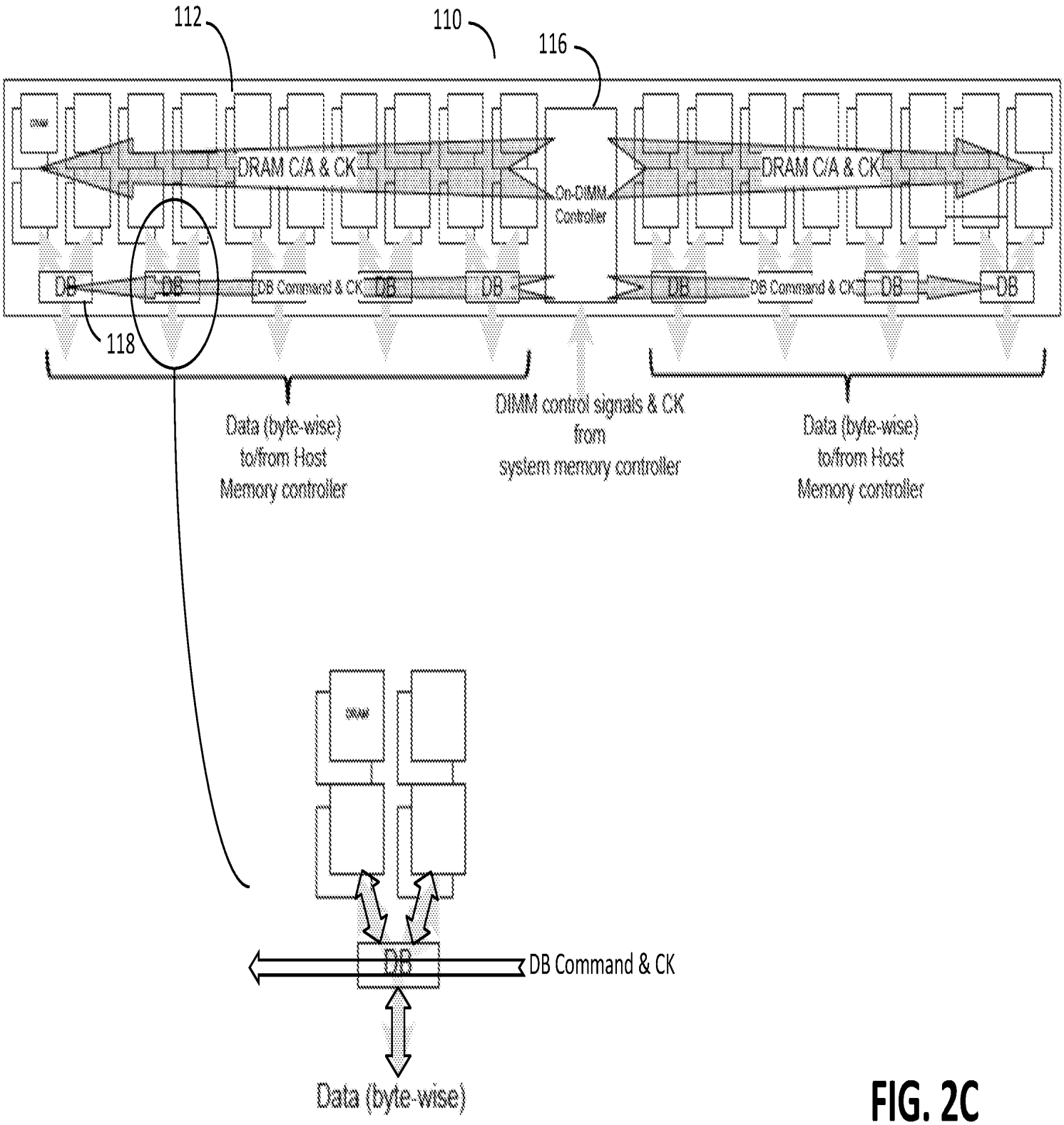
112
110
116
DRAM C/A & CK
DRAM C/A & CK
On-DIMM Controller
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
DB
DB Command & CK
Data (byte-wise)

FIG. 2C

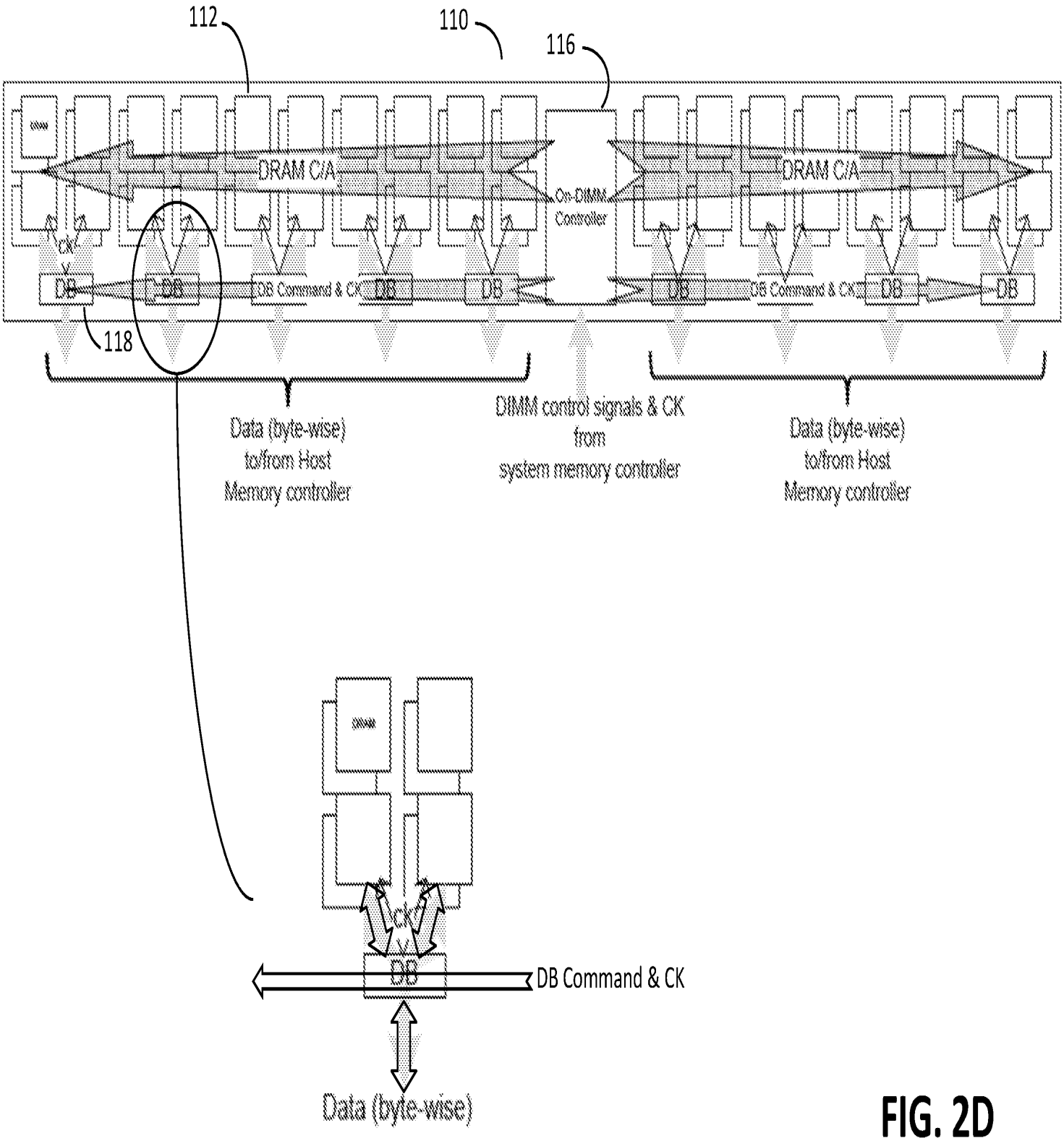
112
110
116
DRAM C/A
DRAM C/A
On-DIMM Controller
CK
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
CK
DB
DB Command & CK
Data (byte-wise)

FIG. 2D

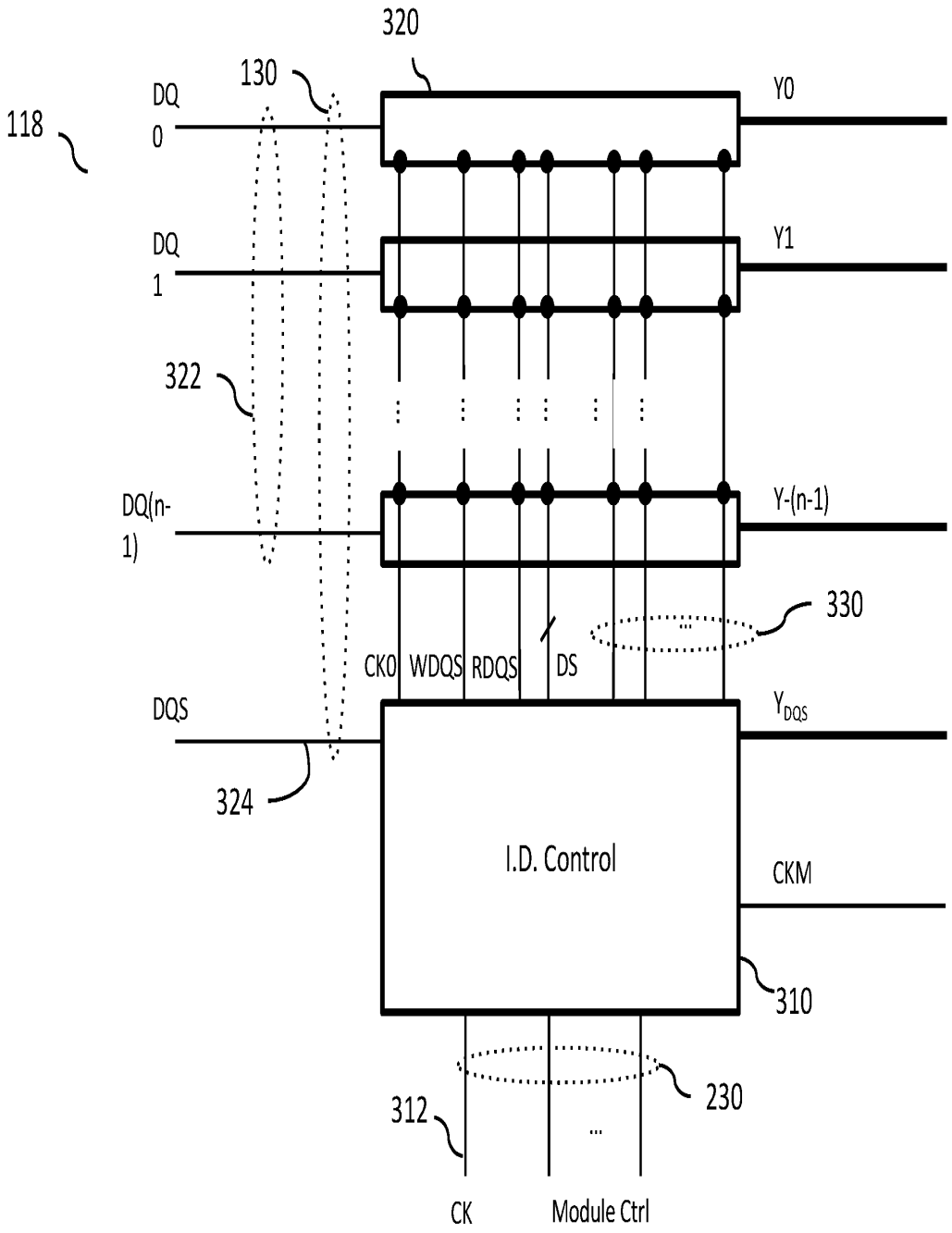
320
130
118
DQ
0
Y0
DQ
1
Y1
322
DQ(n-
1)
Y-(n-1)
330
CK0
WDQS
RDQS
DS
DQS
Y_{DQS}
324
I.D. Control
CKM
310
230
312
CK
Module Ctrl

FIG. 3

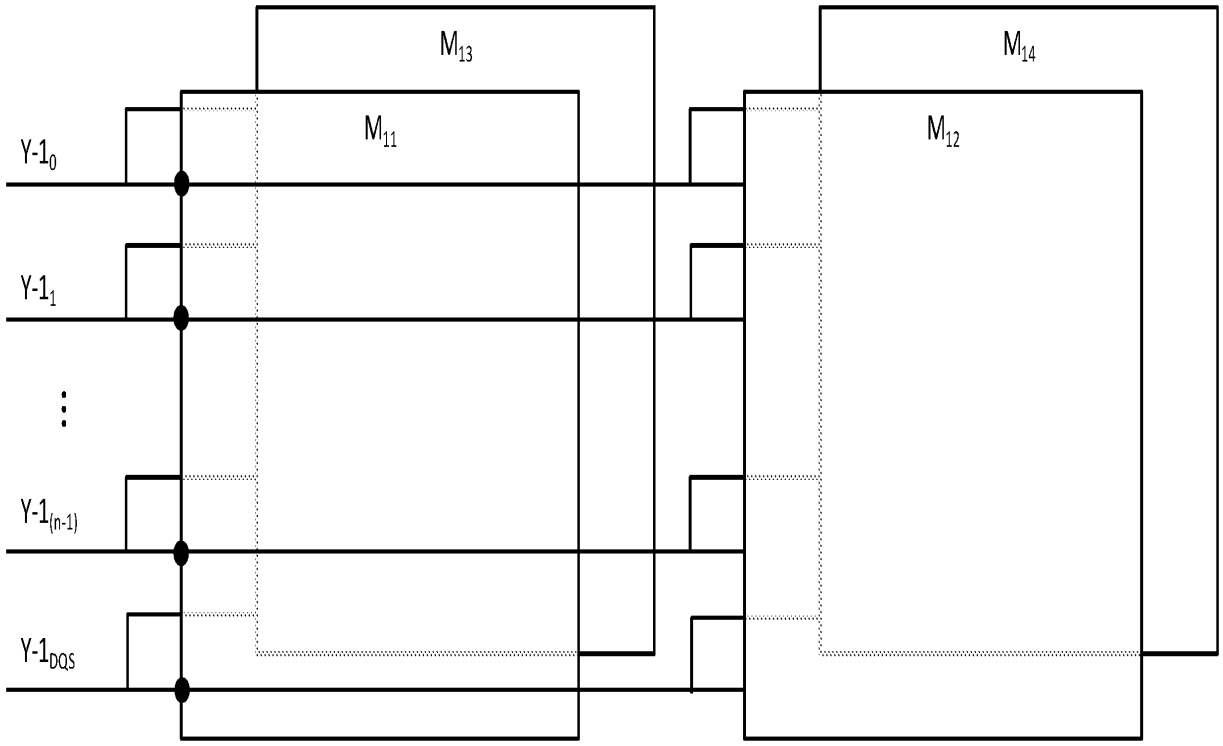

FIG. 4A

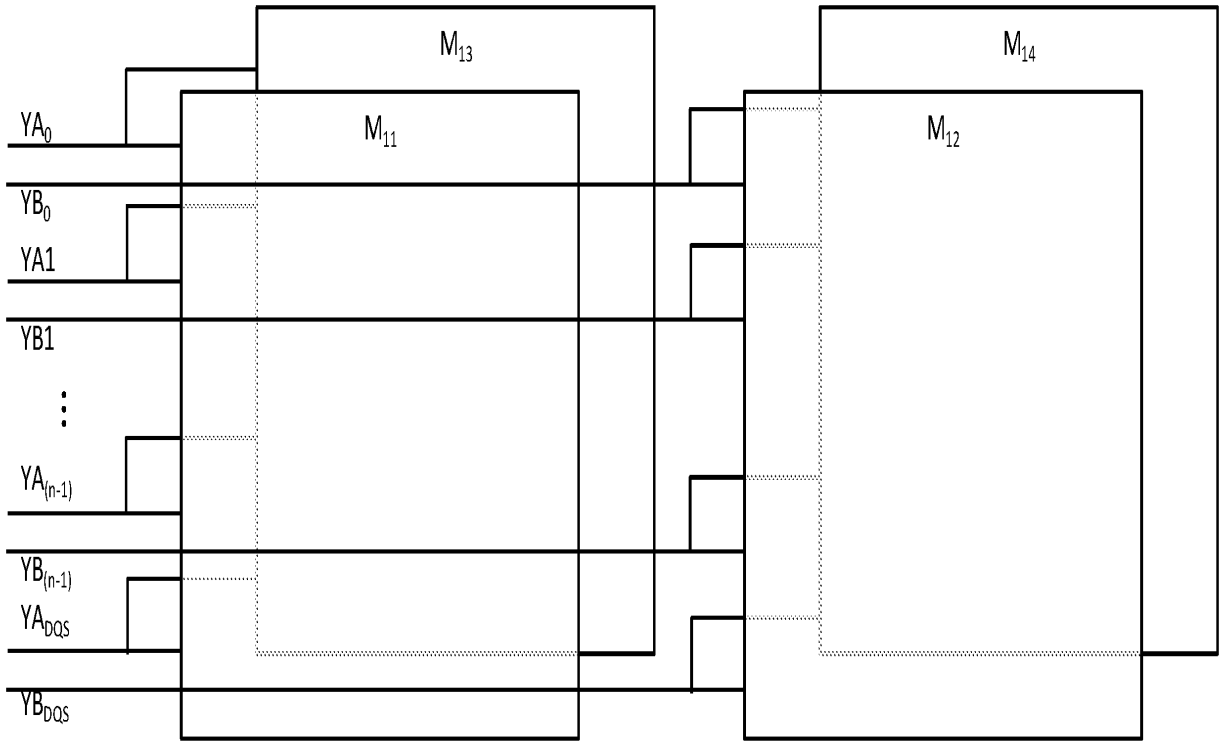

FIG. 4B

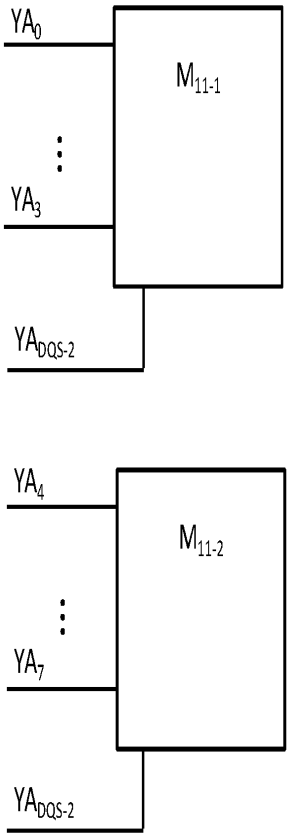
YA0
M11-1
YA3
YADQS-2
YA4
M11-2
YA7
YADQS-2

FIG. 5A

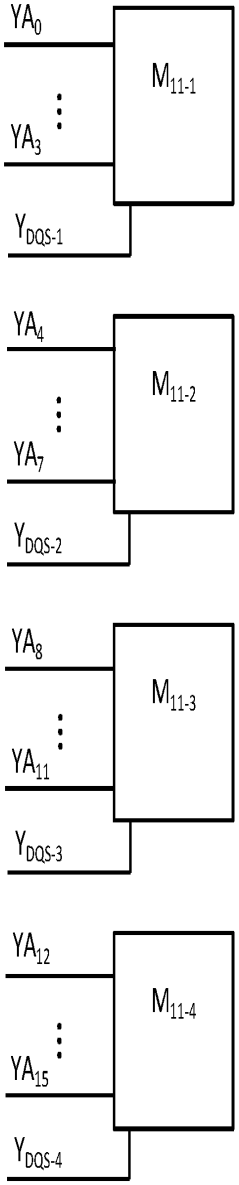
YA0
M11-1
YA3
YDQS-1
YA4
M11-2
YA7
YDQS-2
YA8
M11-3
YA11
YDQS-3
YA12
M11-4
YA15
YDQS-4

FIG. 5B

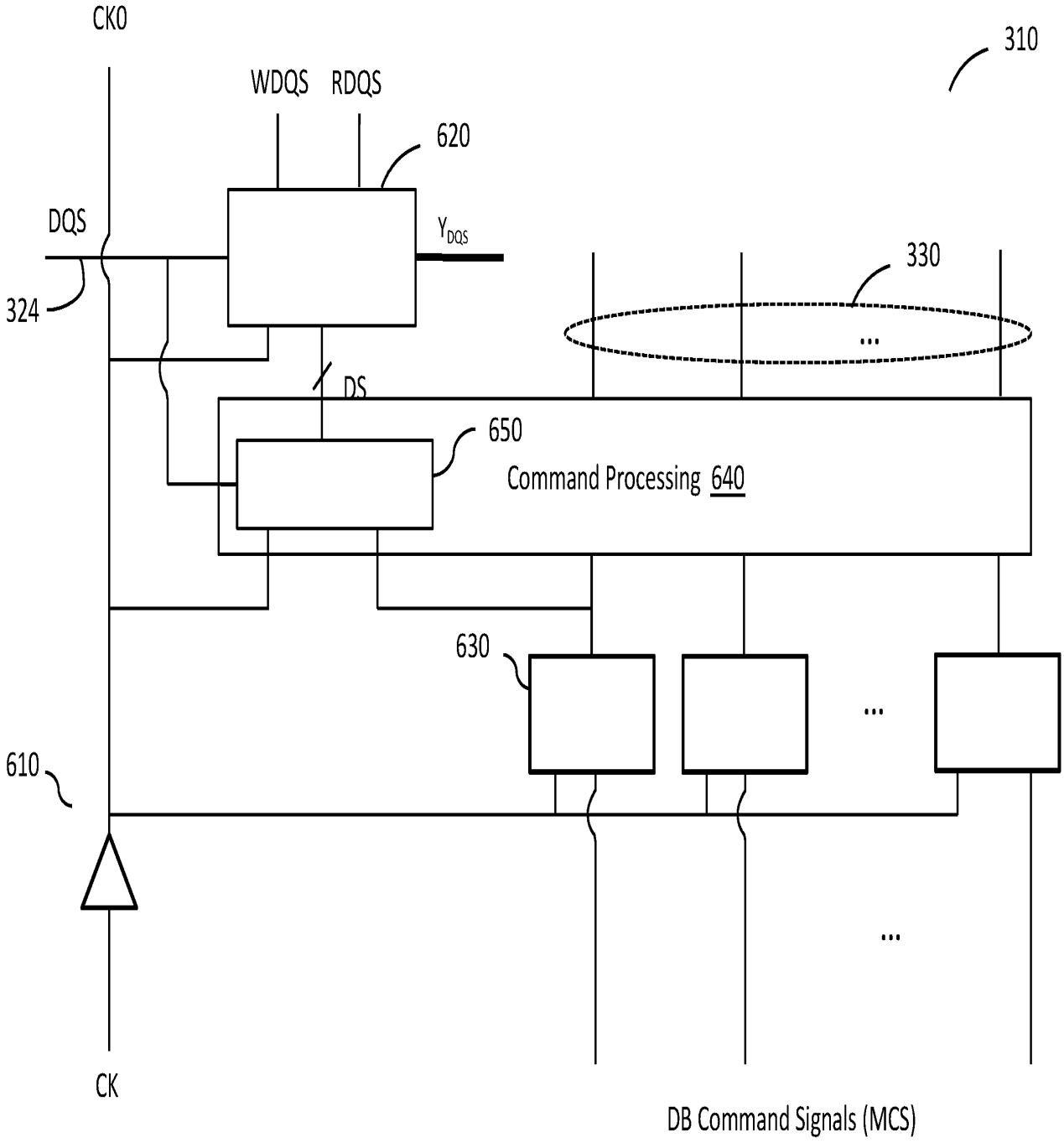
CK0
310
WDQS
RDQS
620
DQS
Y_{DQS}
330
324
...
DS
650
Command Processing 640
630
...
610
...
CK
DB Command Signals (MCS)

FIG. 6

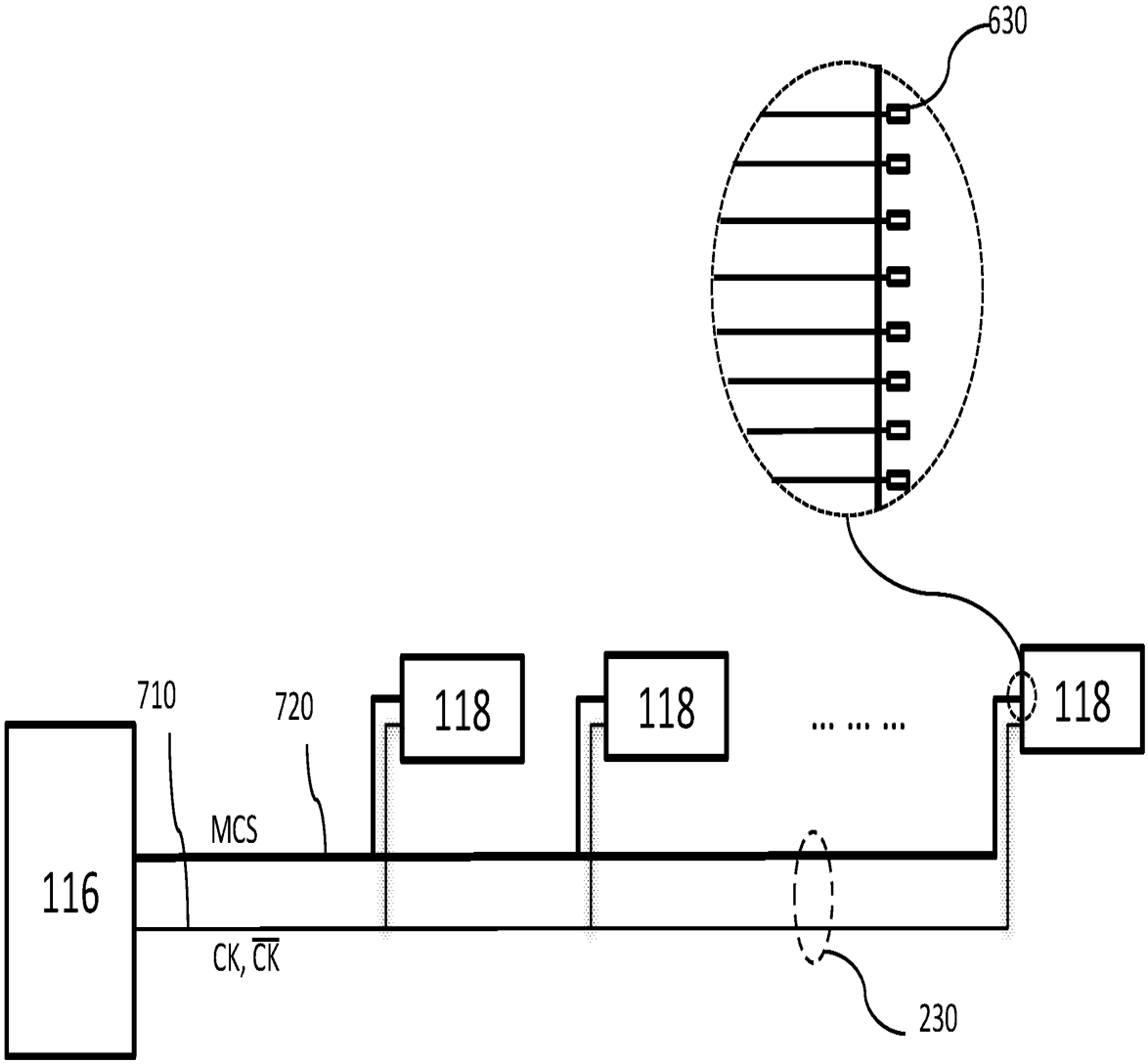

FIG. 7

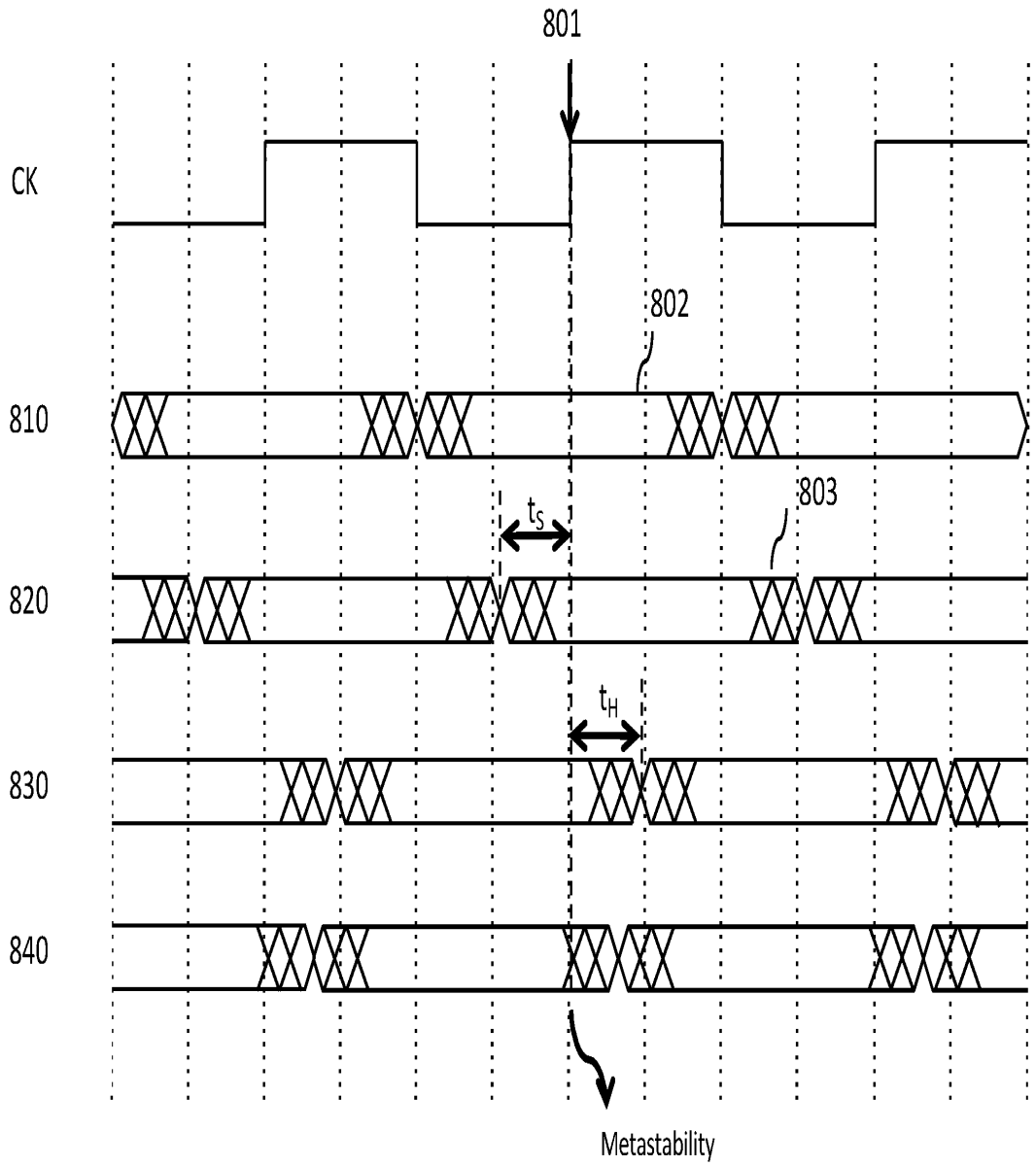

FIG. 8

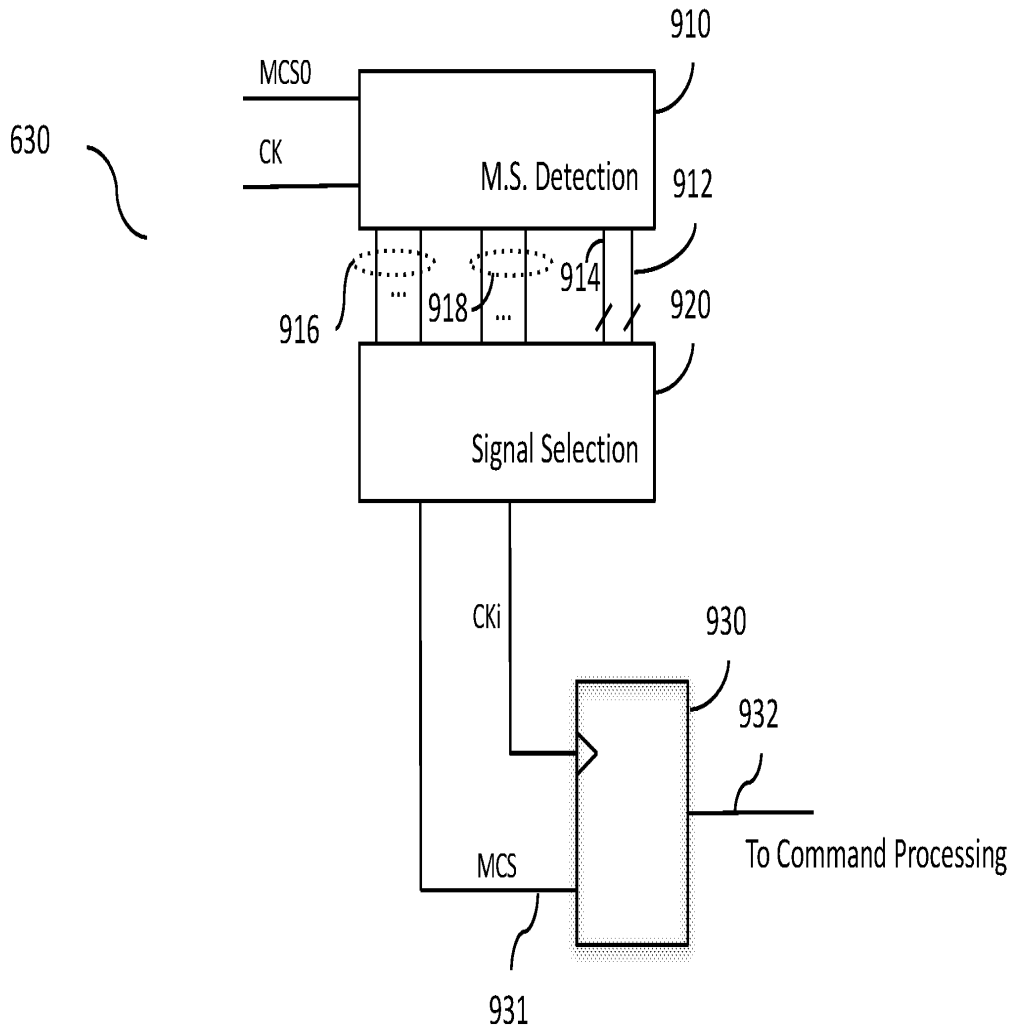
910
MCS0
630
CK
M.S. Detection
912
914
916
918
920
Signal Selection
CKi
930
932
To Command Processing
MCS
931

FIG. 9

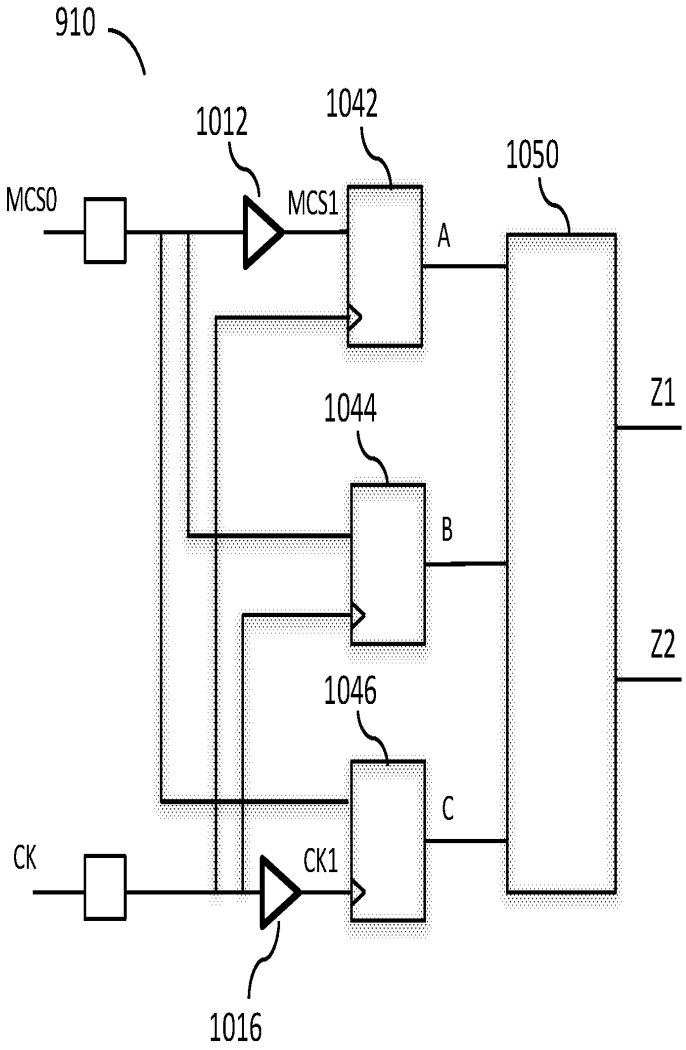

FIG. 10A

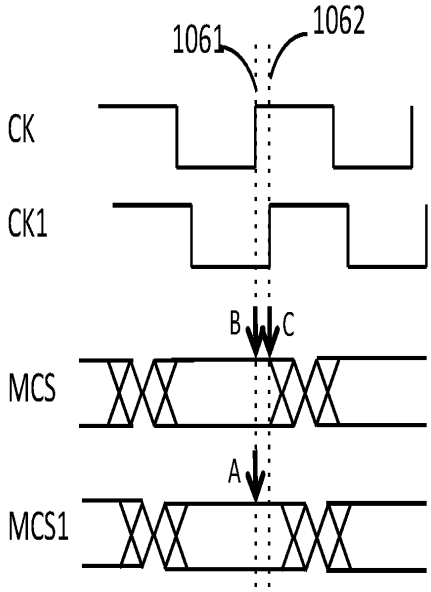

FIG. 10B

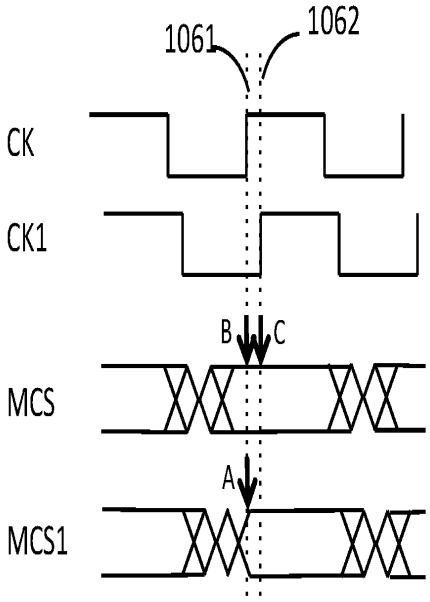

FIG. 10C

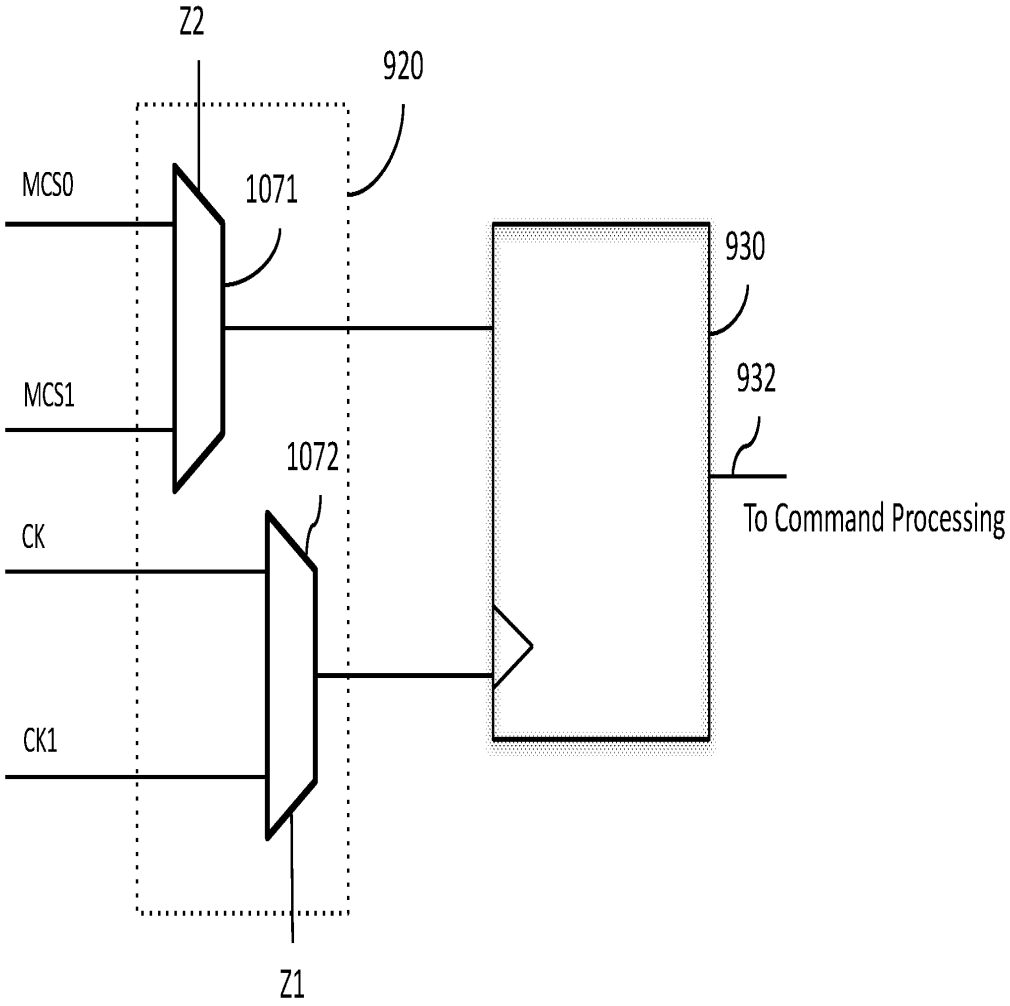
Z2
920
MCS0
1071
930
MCS1
932
1072
To Command Processing
CK
CK1
Z1

FIG. 10D

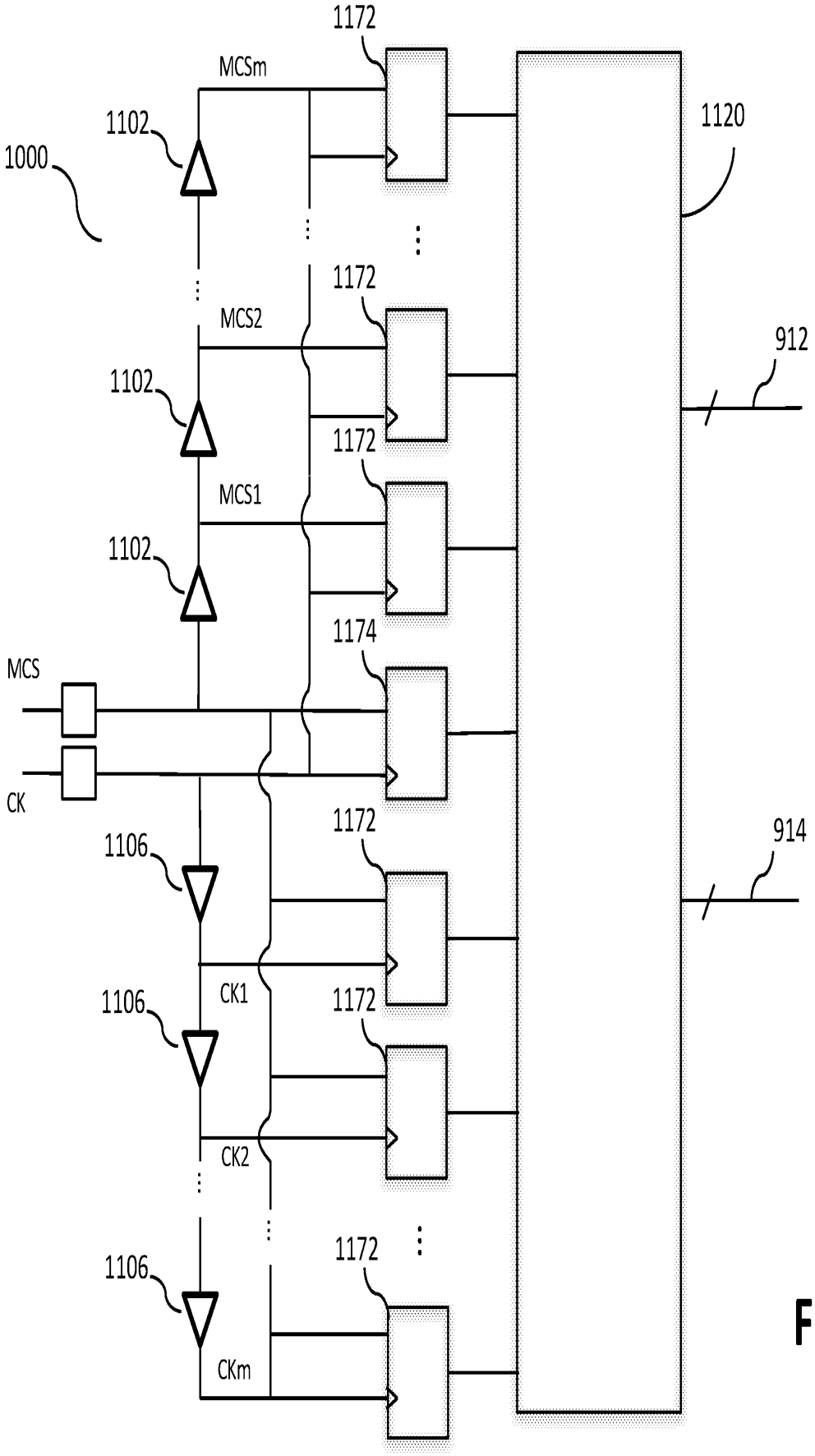
1172
MCSm
1102
1000
1120
1172
MCS2
912
1102
1172
MCS1
1102
1174
MCS
CK
1172
914
1106
CK1
1106
1172
CK2
1172
1106
CKm

FIG. 11A

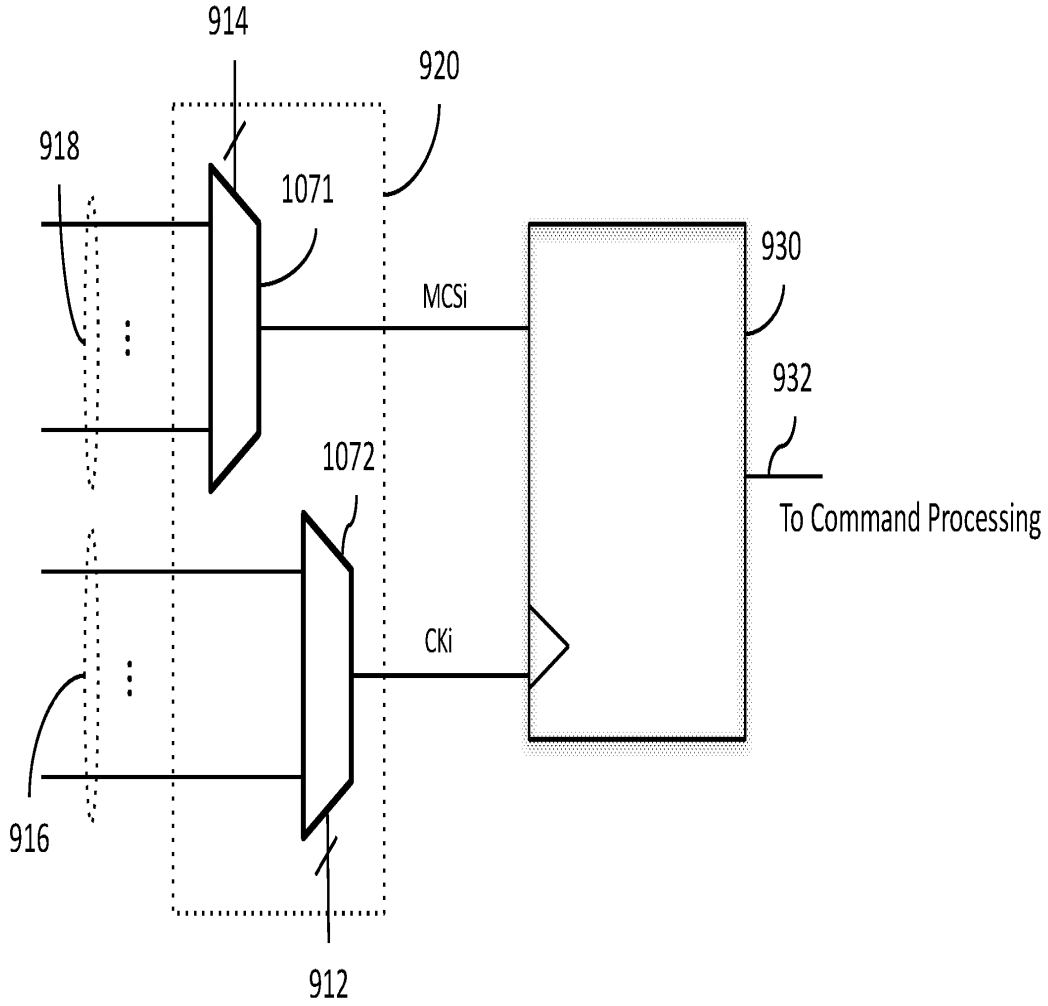
914
920
918
1071
930
MCSi
932
1072
To Command Processing
CKi
916
912

FIG. 11B

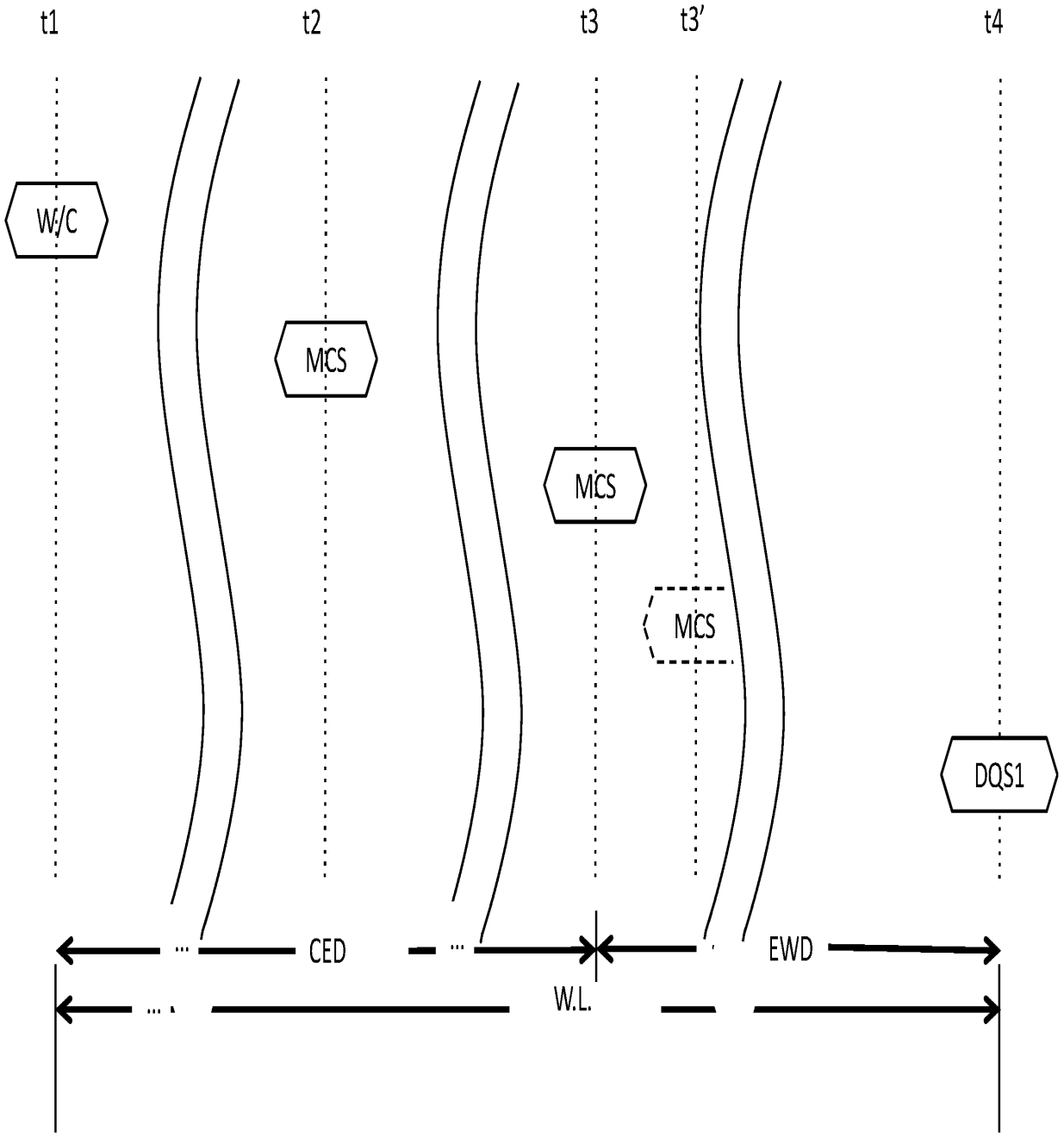

FIG. 12A

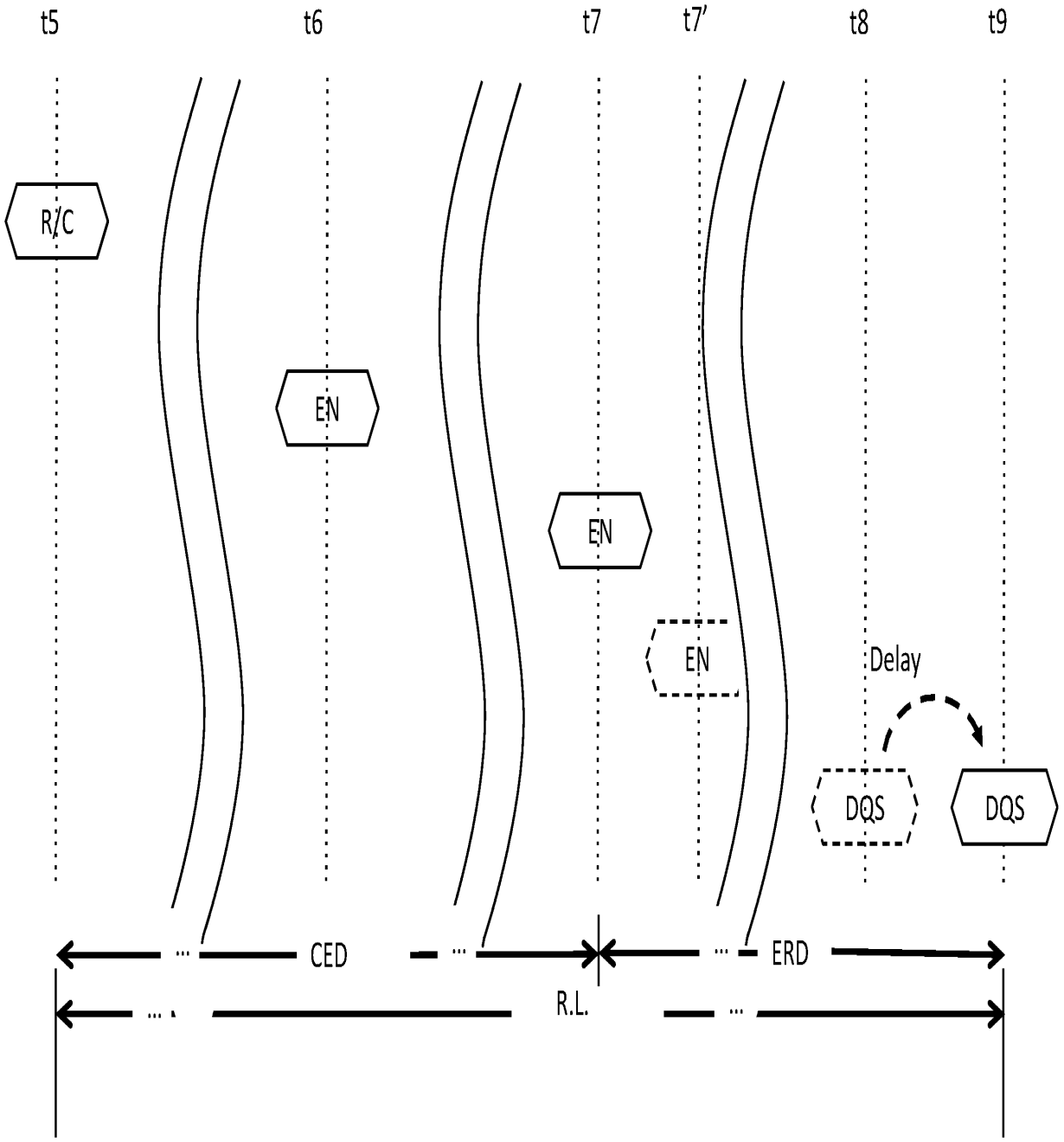

FIG. 12B

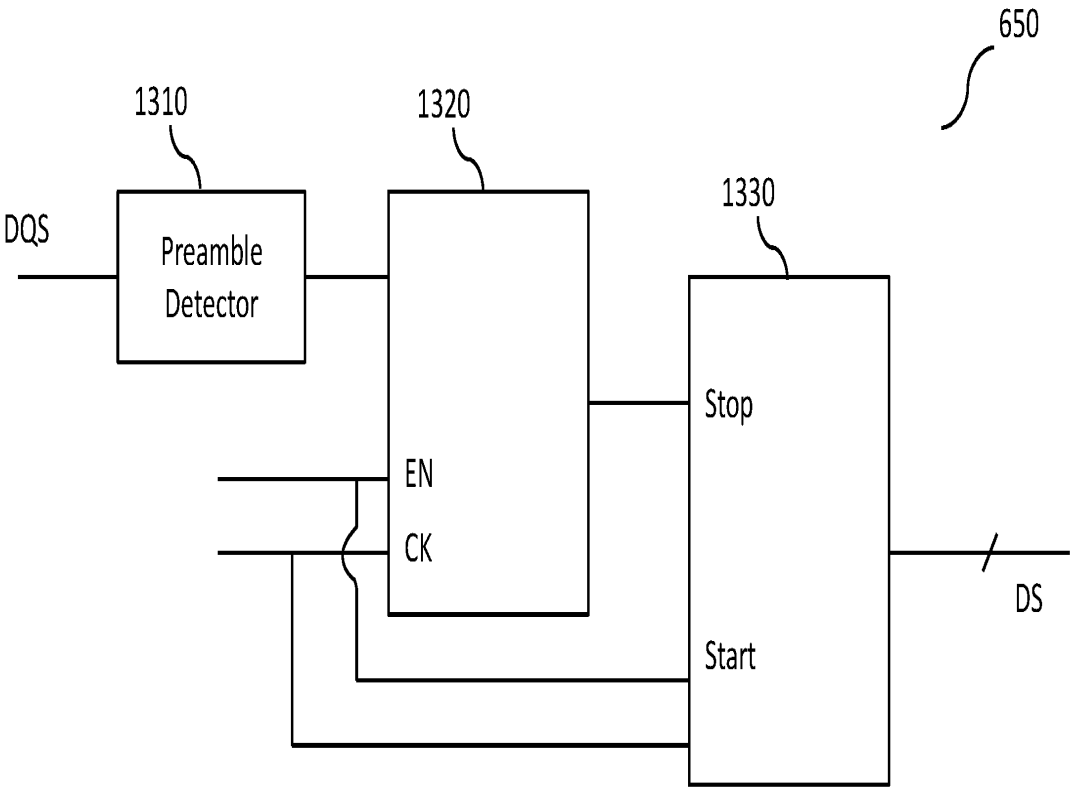

FIG. 13

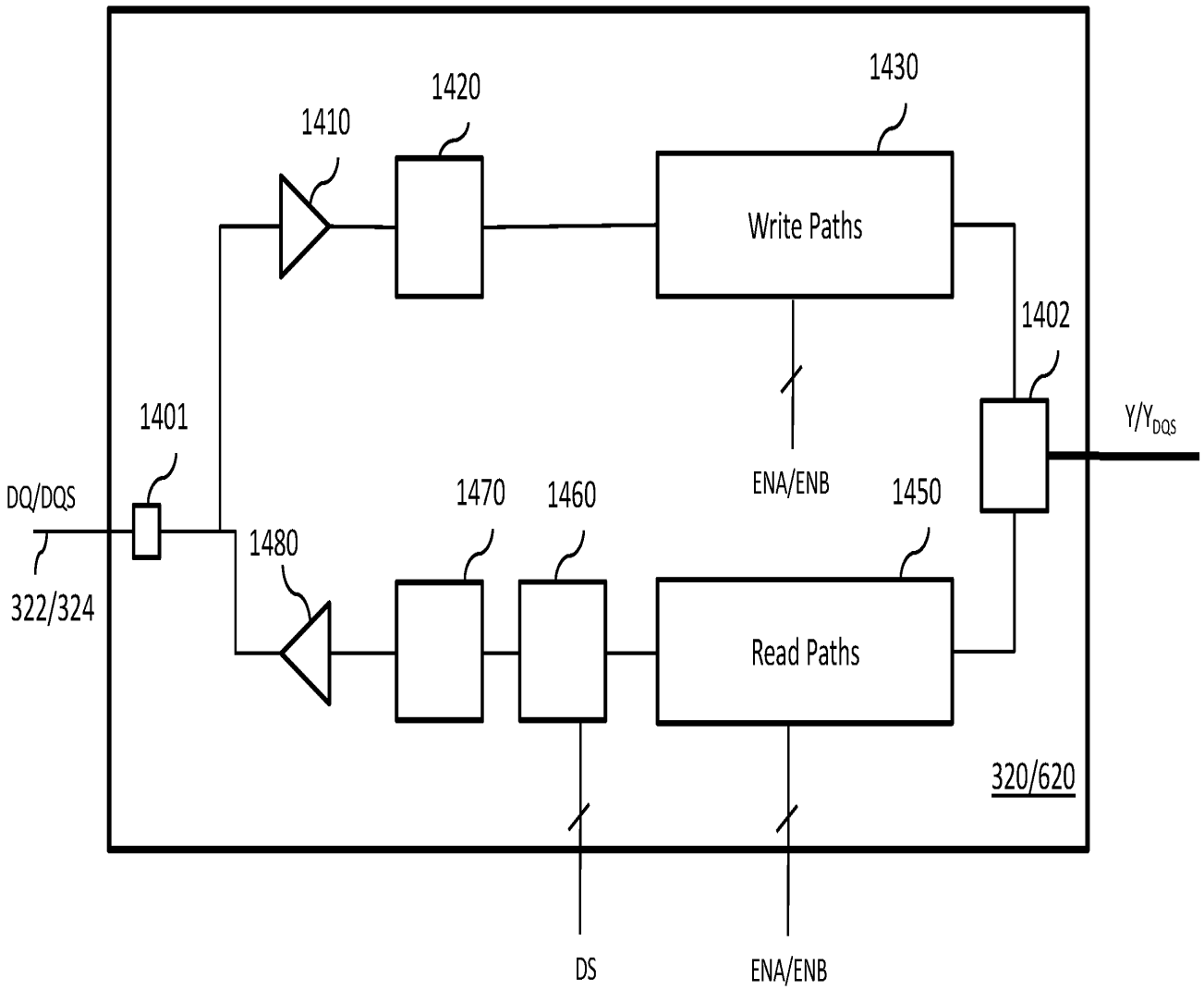
1430
1420
1410
Write Paths
1402
1401
Y/Y_DQS
DQ/DQS
1470
1460
ENA/ENB
1450
1480
322/324
Read Paths
320/620
DS
ENA/ENB

FIG. 14

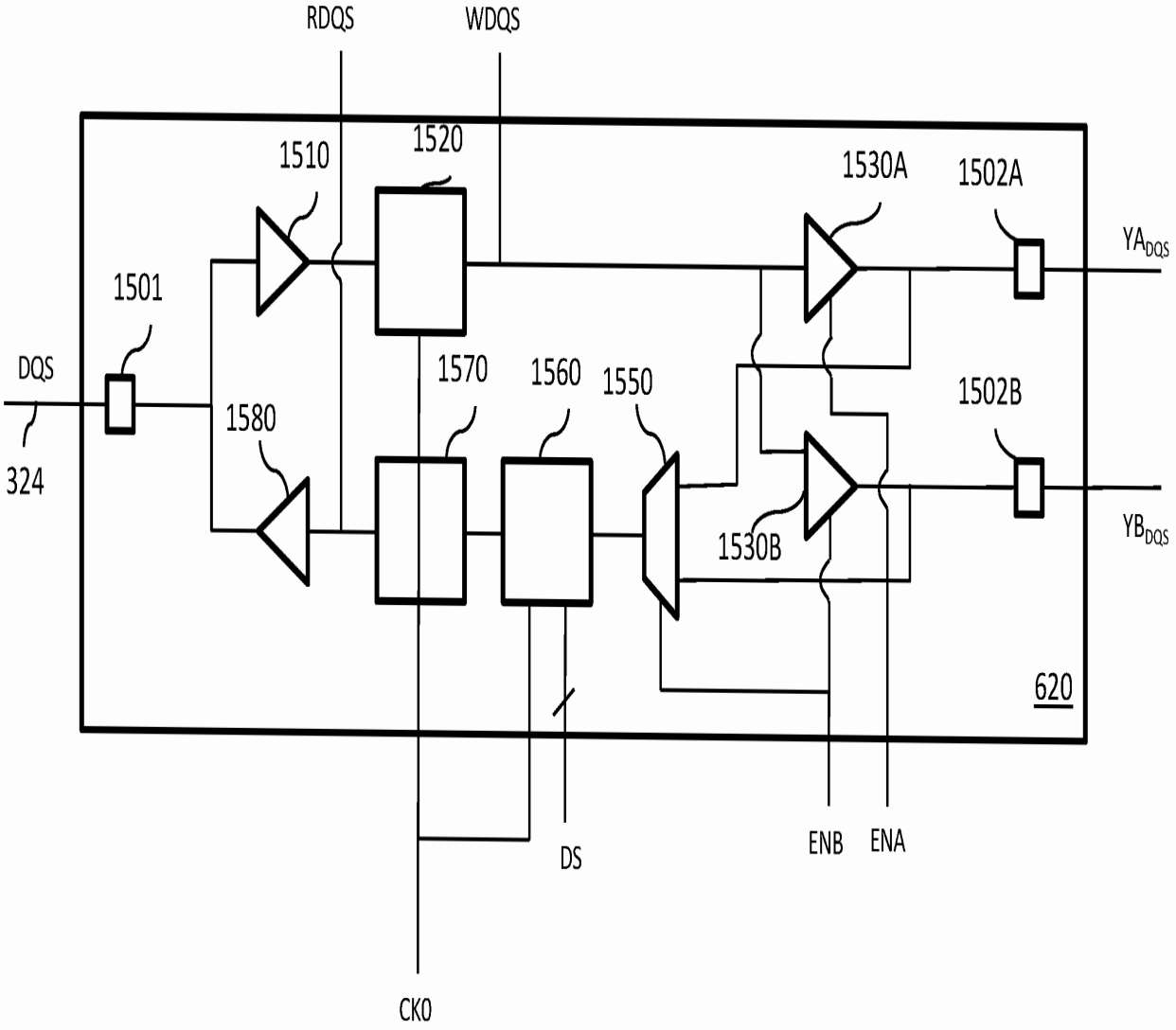
RDQS
WDQS
1510
1520
1530A
1502A
YA$_{DQS}$
1501
DQS
324
1580
1570
1560
1550
1502B
1530B
YB$_{DQS}$
620
DS
ENB
ENA
CK0

FIG. 15

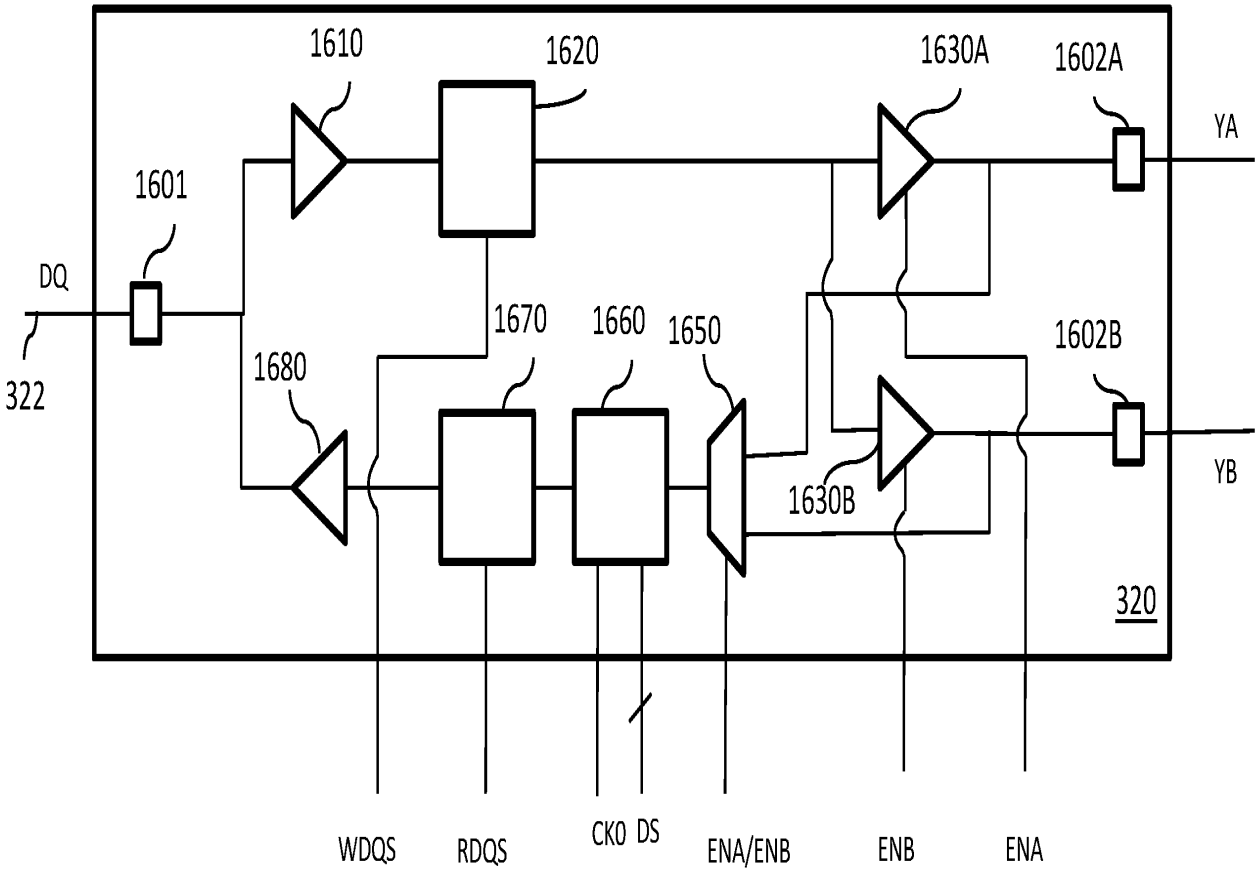
1610
1620
1630A
1602A
YA
1601
DQ
322
1670
1660
1650
1680
1602B
YB
1630B
320
WDQS
RDQS
CK0
DS
ENA/ENB
ENB
ENA

FIG. 16

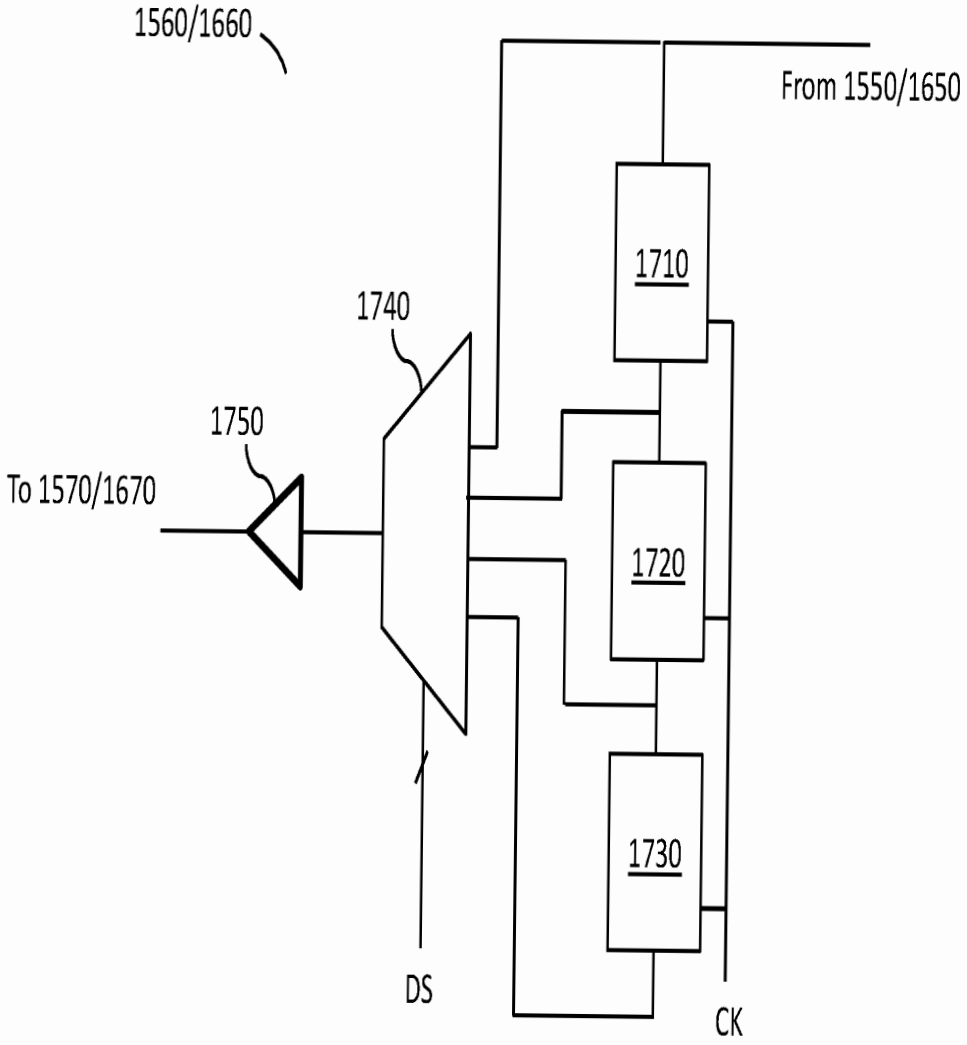
1560/1660
From 1550/1650
1710
1740
1750
To 1570/1670
1720
1730
DS
CK

FIG. 17

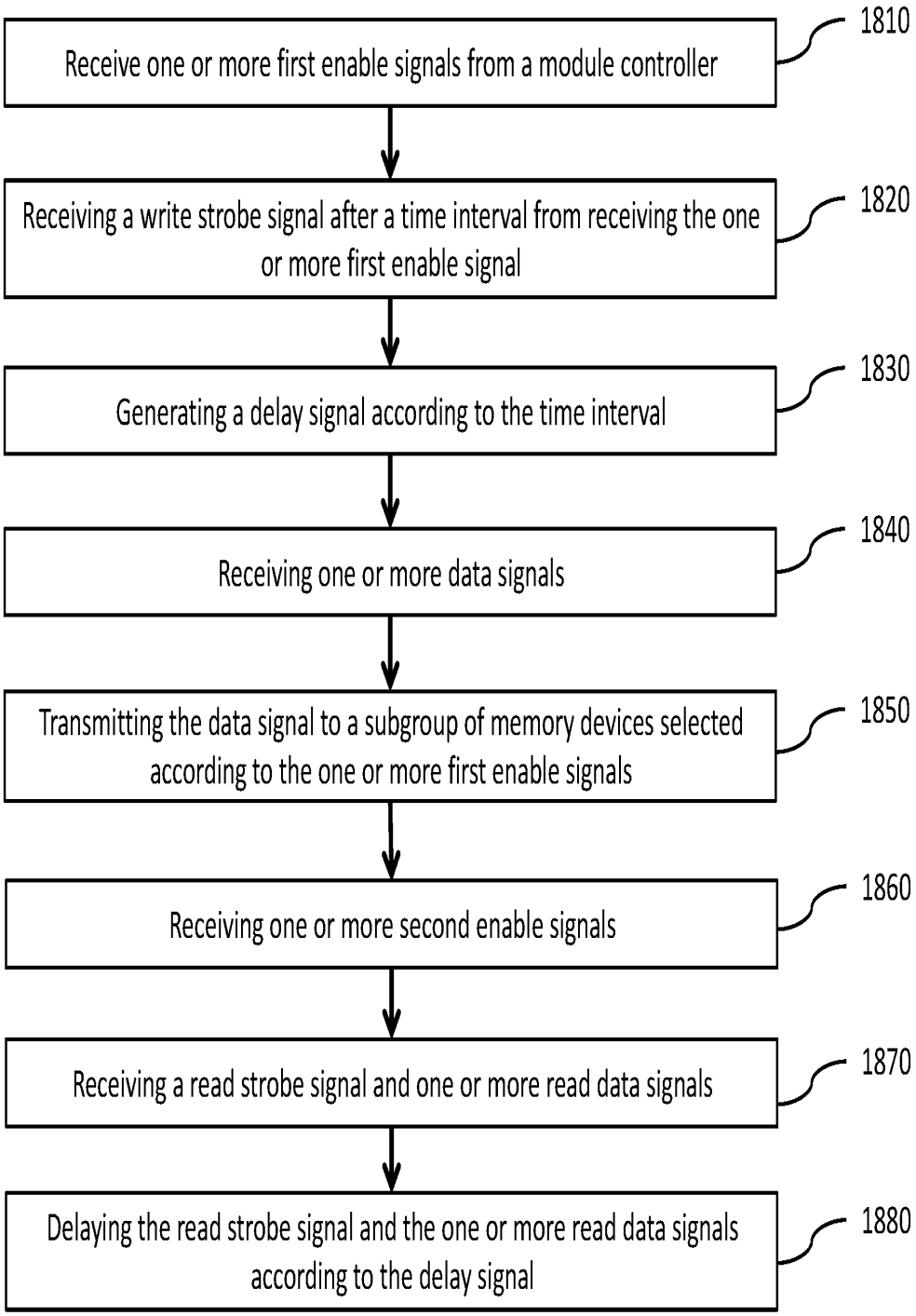
Receive one or more first enable signals from a module controller
1810
Receiving a write strobe signal after a time interval from receiving the one or more first enable signal
1820
Generating a delay signal according to the time interval
1830
Receiving one or more data signals
1840
Transmitting the data signal to a subgroup of memory devices selected according to the one or more first enable signals
1850
Receiving one or more second enable signals
1860
Receiving a read strobe signal and one or more read data signals
1870
Delaying the read strobe signal and the one or more read data signals according to the delay signal
1880

FIG. 18

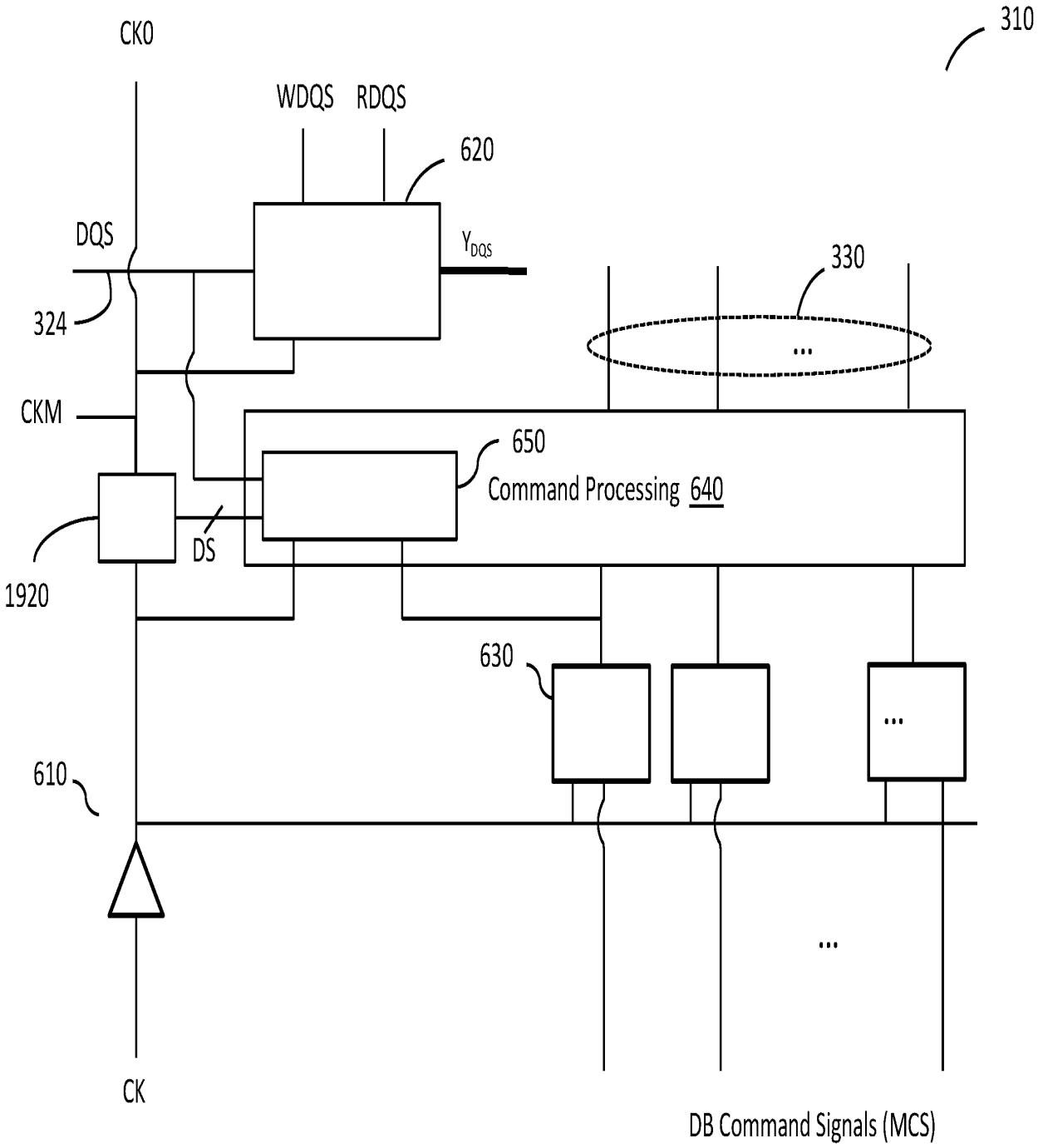
310
CK0
WDQS
RDQS
620
DQS
Y_{DQS}
330
324
CKM
650
Command Processing 640
DS
1920
630
610
CK
DB Command Signals (MCS)

FIG. 19

Customer No. 79141
Attorney Docket No.: NT003US

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/952,599 filed on July 27, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.
(Name of Assignee)

of **51 Discovery, Suite #150, Irvine, CA 92618**
(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: Date: 10/9/2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date: 10/14/2013

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Document code: WFEE

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		02	FC : 2111	300.00 OP	
		03	FC : 2311	360.00 OP	

Document code: WFEE

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01	FC : 1011	-280.00	OP
02	FC : 1111	-600.00	OP
03	FC : 1311	-720.00	OP

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CCETIN RF #30191124 Mailroom Dt: 02/14/2017 15426064

Credit Card Refund Total: $870.00

Visa XXXXXXXXXXXX5877

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
15/426,064

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/426,064	02/07/2017	2139	730	NT003C1	20	1

CONFIRMATION NO. 9117

FILING RECEIPT

OC000000089228771

79141
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Date Mailed: 02/16/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/14/2017

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/426,064**

Projected Publication Date: 05/25/2017

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04

CONFIRMATION NO. 9117

PUBLICATION NOTICE

OC000000091633814

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Title:MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

Publication No.US-2017-0147514-A1
Publication Date:05/25/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

79141 7590 06/02/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
06/02/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com

Office Action Summary	Application No. 15/426,064	Applicant(s) LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/07/2017.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) 1-20 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on 2/07/2017 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Continuation filed on 2/07/2017.

Claims 1-20 are pending for this examination.

Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the

scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-20 of instant Application, respectively contains every element of claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 14/846,993, now US Patent No. 9,563,587**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus; a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory command signals; and memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and a plurality of buffer circuits	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board including edge connections for connecting to respective ones of the signal lines in the memory bus; memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address

	mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory' devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the subset of the data paths in accordance with the timing information.		signal lines and to control the memory devices and the buffer circuits in response to the memory command signals; wherein the each respective buffer circuit is configured to respond to one or more first control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation; wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the

			write operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

Claims	**Instant Application**	Claims	**copending Application No. 13/952,599, now US Patent No. 9,128,632**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus; a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory command signals; and	Independent claim 1	A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals; memory devices organized in groups, each group including at least one memory device, the memory devices receiving the

	memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory' devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing		module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory

	of the data and strobe signals on the subset of the data paths in accordance with the timing information.		write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632.		

Likewise, the dependent claims of the above cited independent claims carry similar limitations to each other respectively.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however,

the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Sun whose telephone number is 571-270-1724. The examiner can normally be reached on Mondays to Thursdays from 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai, can be reached at (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 15/426,064	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8,565,033 B1	10-2013	Manoharajah; Valavan	G11C29/028	365/129
*	B	US-2014/0029370 A1	01-2014	KOSHIZUKA; Atsuo	G11C7/1051	365/233.13
*	C	US-2006/0077731 A1	04-2006	Ware; Frederick A.	G11C5/04	365/194
*	D	US-2007/0217559 A1	09-2007	Stott; Bret G.	G11C7/1051	375/355
*	E	US-2010/0271092 A1	10-2010	Zerbe; Jared L.	G06F13/4243	327/161
*	F	US-8,214,616 B2	07-2012	Ware; Frederick A.	G06F13/1684	711/104
*	G	US-8,949,519 B2	02-2015	Rajan; Suresh Natarajan	G11C5/02	365/189.2
*	H	US-2002/0039323 A1	04-2002	Tokutome, Hiroto	G11C7/1066	365/233.12
*	I	US-2008/0037412 A1	02-2008	Geile; Michael J.	G06F17/14	370/208
*	J	US-7,884,619 B1	02-2011	Chong; Yan	G01R31/3016	324/601
*	K	US-2012/0256639 A1	10-2012	Pausini; Marco	G01R31/31709	324/613
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/29/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC- SEARCHED

Symbol	Date	Examiner
limited search of G06F 1/12	5/28/2017	MS
limited search of G06F 13/1689	5/28/2017	MS
limited search of G06F 12/0246	5/28/2017	MS
limited search of G06F 13/1694	5/28/2017	MS

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
EAST Search - see attached	5/28/2017	MS
Inventor Search - see attached EAST Search	5/28/2017	MS
limited EAST Search of class/subclasses 710/5 and 6	5/28/2017	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	5/28/2017	MS

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S136	4815	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S137	1994	S136 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S138	206	S137 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S139	62	S138 AND ((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S140	62	S139 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S141	62	S140 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S142	62	S141 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S143	34	S142 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S144	5	S143 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S145	4446	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S146	107	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:00
S147	554514	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02

S148	55223	S147 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02
S149	124	S147 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02
S150	47	S149 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02
S151	728	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02
S152	1	S151 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:02
S153	5419	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S154	941	S153 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S155	36	S154 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S156	7	S155 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S157	168977	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S158	2026	S157 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S159	1667	S158 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S160	1640	S159 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S161	321	S160 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:04
S162	62	S161 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2017/05/28 14:04

			IBM_TDB			
S163	7700	memory module and buffer and tim$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S164	1622	S163 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S165	1229	S164 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S166	350	S165 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S167	9	S166 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S168	9	S167 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S169	6	S168 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/05/28 14:05
S170	415	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S171	304	S170 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S172	151	S171 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S173	132	S172 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S174	48	S173 and tim$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05
S175	13	S174 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/05/28 14:05

EAST Search History (Interference)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/426,064
Filed	:	February 7, 2017
For	:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	9117
Docket No.	:	N3044.100009US04

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

August 30, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the following Amendment and remarks in response to the Non-Final Office Action dated June 2, 2017 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5394.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 7 of this paper.

1. (Currently Amended) A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective ~~data/strobe~~ signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to ~~produce~~ output module command signals and module control signals in response to the memory command signals; and

memory devices mounted on the module board and configured to perform the ~~a~~ first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines~~, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines~~; and

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit ~~providing data paths~~ of the plurality of buffer circuits is coupled between a respective set of ~~the~~ data/strobe signal lines and a respective set ~~of the plurality of sets~~ of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic ~~that responds~~ configured to respond to the module control signals by enabling ~~a subset of~~ the data paths ~~for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices~~, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on ~~the subset of~~ the data paths in accordance with the timing information.

2. (Original) The memory module of claim 1, wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation.

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3. (Currently Amended) The memory module of claim 2, wherein the each respective buffer circuit includes a delay control circuit ~~that determines~~ configured to determine, during the memory write operation, a time interval between receiving a first signal from the module control device and receiving a second signal from the memory controller, and wherein the timing information includes the time interval.

4. (Currently Amended) The memory module of claim 3, wherein the each respective buffer circuit is further configured to receive ~~receives~~ a module clock signal and further includes a clock regeneration circuit configured to generate ~~that regenerates~~ a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output ~~outputting~~ the local clock signal to the respective set ~~of the plurality of sets~~ of memory devices~~, the respective set of the plurality of sets of memory devices performing the first memory operation in accordance with the local clock signal~~.

5. (Original) The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

6. (Currently Amended) The memory module of claim 2 ~~5~~, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output the respective data and strobe signals in accordance with the local clock signal ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

7. (Currently Amended) The memory module of claim 3 ~~5~~, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

8. (Currently Amended) The memory module of claim 7, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output the respective data and strobe signals in accordance with the local clock signal, the two

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memory devices being in a same rank ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

9. (Currently Amended) The memory module of claim 1, wherein the each respective buffer circuit is further configured to receive ~~receives~~ a module clock signal from the module control device and further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

10. (Original) The memory module of claim 9, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

11. (Currently Amended) The memory module of claim 10, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

12. (Original) The memory module of claim 9, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

13. (Currently Amended) The memory module of claim 12, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to receive or output the respective data and strobe signals, the two memory devices being in a same rank ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

14. (Currently Amended) The memory module of claim 1, wherein the each respective buffer circuit is further configured to receives a module clock signal and further includes a clock regeneration circuit configured to generate ~~that regenerates~~ a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is configured to output ~~outputting~~ the local clock signal to the respective set of ~~the~~

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~~plurality of sets of~~ memory devices~~, the respective set of the plurality of sets of memory devices performing the first memory operation in accordance with the local clock signal~~.

15. (Currently Amended) The memory module of claim 14, wherein the ~~selected subset of the~~ data paths include a first data path for transmitting a strobe signal among the respective data and strobe signals, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal.

16. (Currently Amended) The memory module of claim 15, wherein the ~~selected subset of the~~ data paths include a second data path for transmitting a first data signal among the data and strobe signals, the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

17. (Original) The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

18. (Currently Amended) The memory module of claim 17, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

19. (Original) The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

20. (Currently Amended) The memory module of claim 19, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal.

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the two memory devices being in a same rank ~~each of the plurality of sets of memory devices to perform the first memory operation~~.

21. (New) The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device.

22. (New) The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the memory controller.

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REMARKS

This amendment responds to the Non-Final Office Action dated June 2, 2017. In the Office Action, the Examiner:

- provisionally rejected claims 1-20 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587, and over claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632.

Claims 1, 3-4, 6-9, 11, 13-16, 18, and 20 are amended for clarity and to correct minor issues. New claims 21-22 are presented. Support for the amendments and the new claims can be found throughout the Specification. Thus, no new matter is added.

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d), which should overcome any actual or provisional rejection based on the nonstatutory obviousness-type double patenting ground over the references U.S. Patent No. No. 9,563,587 and US Patent No. 9,128,632, which are commonly owned with this application.

Applicant submits that claims 1-22 are in condition for allowance and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 to discuss any remaining issues.

Respectfully submitted,

Date: August 30, 2017

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141

Samsung Electronics Co., Ltd.
Ex. 1032, p. 111

Electronic Acknowledgement Receipt

EFS ID:	30225889
Application Number:	15426064
International Application Number:	
Confirmation Number:	9117
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/JoLin Johnson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10009US04
Receipt Date:	30-AUG-2017
Filing Date:	07-FEB-2017
Time Stamp:	17:03:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2017-08-30_Amendment_NT003C2.pdf	162264 2c28ebfdfa0b019be84ec7224e9e5a18b60a6727	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	7
Warnings:			
Information:			
	Total Files Size (in bytes):	162264	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15426064
Filing Date	07-Feb-2017
First Named Inventor	Hyun Lee
Attorney Docket Number	N3044.10009US04
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9563587

9128632

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

- [x] Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.
- [ ] I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- [x] Small Entity
- [ ] Micro Entity
- [ ] Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- [x] An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 51167

- [ ] A sole inventor
- [ ] A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- [ ] A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	/Jamie J. Zheng/

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15426064
Filing Date:	07-Feb-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/JoLin Johnson
Attorney Docket Number:	N3044.10009US04

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15426064

Filing Date: 07-Feb-2017

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on August 30, 2017

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	30226009
Application Number:	15426064
International Application Number:	
Confirmation Number:	9117
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/JoLin Johnson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10009US04
Receipt Date:	30-AUG-2017
Filing Date:	07-FEB-2017
Time Stamp:	17:06:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	083117INTEFSW17065700
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33582 619a3a9cddf98deaf7e394c10fa88a624c42efef	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30707 2011d486e9b5e6aca88a57be3717e087a241913c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64289		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 09/08/2017

DEVANS SALE #00000001 Mailroom Dt: 08/30/2017 505394 15426064
01 FC : 2202 80.00 DA

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
15/426,064	02/07/2017	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $210 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	08/30/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 20	= 2		x $40 =	80
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	80

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/Dorian Evans/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 09/21/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 09/21/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	12/21/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Ex. 1032, p. 123

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/21/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	12/21/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Electronics Co., Ltd.
Ex. 1032, p. 124

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

79141 7590 09/21/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 09/21/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/426,064	Applicant(s) LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's Amendment filed 8/30/2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-22*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Amendment filed 8/30/2017.

Claims 1-22 are pending for this examination.

Claims 1, 3, 4, 6-9, 11, 13-16, 18, and 20 were amended.

Claims 21 and 22 were added.

Terminal Disclaimer

The terminal disclaimer filed on 8/30/2017 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of copending Application No. 14/846,993, now US Patent No. 9,563,587, and copending Application No. 13/952,599, now US Patent No. 9,128,632 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

Claims 1-22 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however,

the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Sun whose telephone number is 571-270-1724. The examiner can normally be reached on Mondays to Thursdays from 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai, can be reached at (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL SUN/

Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 15/426,064	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner MICHAEL SUN	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0029370 A1	01-2014	KOSHIZUKA; Atsuo	G11C7/1051	365/233.13
*	B	US-2006/0077731 A1	04-2006	Ware; Frederick A.	G11C5/04	365/194
*	C	US-2007/0217559 A1	09-2007	Stott; Bret G.	G11C7/1051	375/355
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S176	4899	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S177	2031	S176 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S178	209	S177 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S179	64	S178 AND ((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S180	64	S179 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S181	64	S180 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S182	64	S181 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S183	36	S182 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S184	6	S183 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S185	4572	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S186	107	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:25
S187	568734	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:26

S188	56651	S187 and ((determin$5 or calculat$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:26
S189	125	S187 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:26
S190	47	S189 and (transmi$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:26
S191	741	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:27
S192	1	S191 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:27
S193	5642	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S194	951	S193 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S195	36	S194 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S196	7	S195 and (align$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S197	172008	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S198	2068	S197 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S199	1698	S198 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S200	1670	S199 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S201	328	S200 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S202	64	S201 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2017/09/16 12:28

			IBM_TDB			
S203	7890	memory module and buffer and tim$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:28
S204	1655	S203 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S205	1249	S204 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S206	355	S205 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S207	9	S206 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S208	9	S207 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S209	6	S208 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2017/09/16 12:28
S210	421	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29
S211	309	S210 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29
S212	153	S211 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29
S213	134	S212 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29
S214	48	S213 and tim$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29
S215	13	S214 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2017/09/16 12:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

S216	4561	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory).clm. and (buffer).clm.	US-PGPUB; USPAT	ADJ	ON	2017/09/16 13:29
S217	411	S216 and (delay or time interval).clm.	US-PGPUB; USPAT	ADJ	ON	2017/09/16 13:29
S218	272	S217 and (read or write).clm.	US-PGPUB; USPAT	ADJ	ON	2017/09/16 13:29
S219	3	S218 and (time transmitting or time transmission).clm.	US-PGPUB; USPAT	ADJ	ON	2017/09/16 13:29

9/ 16/ 2017 1:45:21 PM
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BIB DATA SHEET

CONFIRMATION NO. 9117

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/426,064	02/07/2017 RULE	710	2184	N3044.10009US04

APPLICANTS
Netlist, Inc., Irvine, CA;

INVENTORS
Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************
This application is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
02/14/2017

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No		CA	26	~~20~~ 22	1
Verified and Acknowledged	/MICHAEL SUN/ Examiner's Signature	Initials				

ADDRESS
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098
UNITED STATES

TITLE
MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

FILING FEE RECEIVED		
810	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC- SEARCHED

Symbol	Date	Examiner
limited search of G06F 1/12	9/16/2017	MS
limited search of G06F 13/1689	9/16/2017	MS
limited search of G06F 12/0246	9/16/2017	MS
limited search of G06F 13/1694	9/16/2017	MS

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES

Search Notes	Date	Examiner
Updated EAST Search - see attached	9/16/2017	MS
Inventor Search - see attached EAST Search	9/16/2017	MS
limited EAST Search of class/subclasses 710/5 and 6	9/16/2017	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	9/16/2017	MS
Google Scholar Search - search terms used: (memory module and signal lines and delay); (memory module with buffer that times signal transmissions and delays respective to individual buffer)	9/16/2017	MS

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
710	limited search of subclasses 5, 6, and 7	9/16/2017	MS
711	limited search of subclasses 1, 2, 3, 4, 154, and 155	9/16/2017	MS
G06F	limited search of 1/12, 13/1689, 12/0246, and 13/1694	9/16/2017	MS

	/MICHAEL SUN/ Primary Examiner, Art Unit 2184

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

CPC						
Symbol					**Type**	**Version**
G06F		13	/	1673	F	2013-01-01
G06F		3	/	0613	I	2013-01-01
G06F		3	/	0656	I	2013-01-01
G06F		3	/	0659	I	2013-01-01
G06F		3	/	0683	I	2013-01-01
G06F		13	/	1642	I	2013-01-01
G11C		8	/	18	I	2013-01-01
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CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
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NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 22	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 (Primary Examiner)	09/16/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
710	5	G	0	6	F	3 / 00 (2006.01.01)						
CROSS REFERENCE(S)		G	0	6	F	12 / 00 (2006.01.01)						
		G	0	6	F	13 / 00 (2006.01.01)						

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	6	7			
711	1	2	3	4	154
711	155				

NONE (Assistant Examiner) (Date)	Total Claims Allowed: 22	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 09/16/2017 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Samsung Electronics Co., Ltd.
Ex. 1032, p. 140

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15426064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
6	6	22	22												
7	7														
8	8														
9	9														
10	10														
11	11														
12	12														
13	13														
14	14														
15	15														
16	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 22	
/MICHAEL SUN/ Primary Examiner.Art Unit 2184 (Primary Examiner)	09/16/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Samsung Electronics Co., Ltd.
Ex. 1032, p. 141

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/426,064
Filed	:	February 7, 2017
For	:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	9117
Docket No.	:	N3044.100009US04

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

September 28, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. §1.312

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Allowance mailed September 21, 2017, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper. **Remarks** begin on page 6 of this paper.

Samsung Electronics Co., Ltd.
Ex. 1032, p. 142

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

1. (**Previously Presented**) A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and

memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

2. (**Original**) The memory module of claim 1, wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation.

3. (**Previously Presented**) The memory module of claim 2, wherein the each respective buffer circuit includes a delay control circuit configured to determine, during the memory write

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operation, a time interval between receiving a first signal from the module control device and receiving a second signal from the memory controller, and wherein the timing information includes the time interval.

4. **(Previously Presented)** The memory module of claim 3, wherein the each respective buffer circuit is further configured to receive a module clock signal and further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

5. **(Original)** The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

6. **(Currently Amended)** The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output the respective data and strobe signals ~~in accordance with the local clock signal~~.

7. **(Previously Presented)** The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

8. **(Currently Amended)** The memory module of claim 7, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include <u>two</u> ~~one~~ memory <u>devices</u> ~~device~~ from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output the respective data and strobe signals ~~in accordance with the local clock signal~~, the two memory devices being in a same rank.

9. **(Previously Presented)** The memory module of claim 1, wherein the each respective buffer circuit is further configured to receive a module clock signal from the module control device and further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

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10. **(Currently Amended)** The memory module of claim 1 [9], wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

11. **(Previously Presented)** The memory module of claim 10, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals.

12. **(Currently Amended)** The memory module of claim 1 [9], wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

13. **(Currently Amended)** The memory module of claim 12, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include ~~one~~ two memory devices ~~device~~ from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to receive or output the respective data and strobe signals, the two memory devices being in a same rank.

14. **(Previously Presented)** The memory module of claim 1, wherein the each respective buffer circuit is further configured to receives a module clock signal and further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is configured to output the local clock signal to the respective set of memory devices.

15. **(Previously Presented)** The memory module of claim 14, wherein the data paths include a first data path for transmitting a strobe signal among the respective data and strobe signals, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal.

16. **(Previously Presented)** The memory module of claim 15, wherein the data paths include a second data path for transmitting a first data signal among the data and strobe signals, the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

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17. **(Original)** The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

18. **(Previously Presented)** The memory module of claim 17, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal.

19. **(Original)** The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

20. **(Currently Amended)** The memory module of claim 19, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include ~~one~~ two memory devices ~~device~~ from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal, the two memory devices being in a same rank.

21. **(Previously Presented)** The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device.

22. **(Previously Presented)** The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the memory controller.

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REMARKS

Applicant appreciates the allowance of the claims. In this amendment under 37 C.F.R. §1.312, claims 6 and 8 are amended to correct antecedent basis issues and a minor error, claims 10 and 12 are amended to change their dependency from depending from allowed claim 9 to depending from allowed claim 1, and claims 13 and 20 are amended to correct minor errors. Applicant respectfully requests entry of the changes to these claims before the issuance and publication of the patent. In the event that Examiner finds remaining impediment to the entry of this amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 28th day of September, 2017.

Respectfully submitted,

/Jamie J. Zheng, Reg. no. 51167/

JAMIE J. ZHENG
Registration No. 51,167
Attorney for Applicant
Telephone No. (650) 521-4828

Samsung Electronics Co., Ltd.
Ex. 1032, p. 147

Electronic Acknowledgement Receipt

EFS ID:	30511970
Application Number:	15426064
International Application Number:	
Confirmation Number:	9117
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10009US04
Receipt Date:	28-SEP-2017
Filing Date:	07-FEB-2017
Time Stamp:	20:08:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2017-09-28_312-Amendment_N3044-10009US04.pdf	530826 ffd8f9de0f943cfd63887d0a8cea9b3239d2c2f0	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	6

Warnings:	
Information:	
Total Files Size (in bytes):	530826

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/21/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	12/21/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 MASCHOFF BRENNAN
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-5394 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jamie J. Zheng/ Date October 5, 2017
Typed or printed name Jamie J. Zheng Registration No. 51167

Samsung Electronics Co., Ltd.
Ex. 1032, p. 150

Electronic Patent Application Fee Transmittal

Application Number:	15426064
Filing Date:	07-Feb-2017
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/Brian Gonzalez
Attorney Docket Number:	N3044.10009US04

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	30575386
Application Number:	15426064
International Application Number:	
Confirmation Number:	9117
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10009US04
Receipt Date:	05-OCT-2017
Filing Date:	07-FEB-2017
Time Stamp:	19:23:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	100617INTEFSW19274600
Deposit Account	505394
Authorized User	Brian Gonzalez

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.20 (Post Issuance fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	2017-10-05_Comments_N3044-10009US04.pdf	226892 b3c7ab897bafec6a27ec426ab044b6c93ef29db6	no	1
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	2017-10-05_Issue-Fee_N3044-10009US04.pdf	1659876 c3fbe6988c5b6bdd130a74ac4f69617d1ce68cca	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30822 380121ec171d371bf2a671c615b1719f2108025c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1917590		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	Netlist, Inc.	
Application No.:	15/426,064	Art Unit 2184
Filed:	February 7, 2017	
Conf. No.:	9117	
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	
Examiner:	Sun, Michael	
Customer No.:	79141	
Attorney Docket No.:	N3044.10009US04	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant acknowledges Examiner's statements of Reasons for Allowance of the above-referenced patent application and agrees that the claimed subject matter is patentable. However, Applicant takes no position regarding the Reasons for Allowance presented by the Examiner other than the positions Applicant may have previously taken during prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed to Applicant as an indication of the basis for Applicant's belief that the claims are patentable. Furthermore, Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record and Applicant does not waive its rights to such arguments by not further addressing such reasons herein.

Dated this 5th day of October, 2017.

Respectfully submitted,

/Jamie J. Zheng, Reg. no. 51167/

JAMIE J. ZHENG
Registration No. 51,167
Attorney for Applicant
Telephone No. (650) 521-4828

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/426,064
Filed	:	February 7, 2017
For	:	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	9117
Docket No.	:	N3044.100009US04

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

September 28, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. §1.312

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Allowance mailed September 21, 2017, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper. **Remarks** begin on page 6 of this paper.

OK TO ENTER: /M.S/ 10/07/2017

Samsung Electronics Co., Ltd.
Ex. 1032, p. 156

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	02/07/2017	Hyun Lee	N3044.10009US04	9117

79141 7590 10/18/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
SUN, MICHAEL

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
10/18/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	15/426,064	LEE ET AL.
	Examiner	**Art Unit**
	MICHAEL SUN	2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *28 September 2017* under 37 CFR 1.312 has been considered, and has been:

   a) ☒ entered.

   b) ☐ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Samsung Electronics Co., Ltd.
Ex. 1032, p. 158

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/426,064	11/21/2017	9824035	N3044.10009US04	9117

79141 7590 11/01/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Netlist, Inc., Irvine, CA;
Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. ¨ 290 and/or 15 U.S.C. ¨ 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. ¨ 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:21-cv-00431	4/28/2021	Western District of Texas

PLAINTIFF	DEFENDANT
Netlist, Inc.	Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 10,489,314	11/26/2019	Netlist, Inc.
2 9,824,035	11/21/2017	Netlist, Inc.
3 10,268,608	4/23/2019	Netlist, Inc.
4		
5		

In the above´ entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above´ entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1´ Upon initiation of action, mail this copy to Director Copy 3´ Upon termination of action, mail this copy to Director
Copy 2´ Upon filing document adding patent(s), mail this copy to Director Copy 4´ Case file copy