

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00236
Patent 9,824,035 B2

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

KHAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1, 2, 6, 10–13, 21, and 22 (“the challenged claims”) of U.S. Patent No. 9,824,035 B2 (“the ’035 patent,” Ex. 1001). The Petition challenges the patentability of claims 1, 2, 6, 10–13, 21, and 22 of the ’035 patent. Netlist, Inc. (“Patent Owner”) timely filed a Preliminary Response (Paper 12, “Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing at least one of the challenged claims of the ’035 patent. Accordingly, we institute an *inter partes* review as to the challenged claims of the ’035 patent on all the grounds of unpatentability set forth in the Petition.

B. *Related Proceedings*

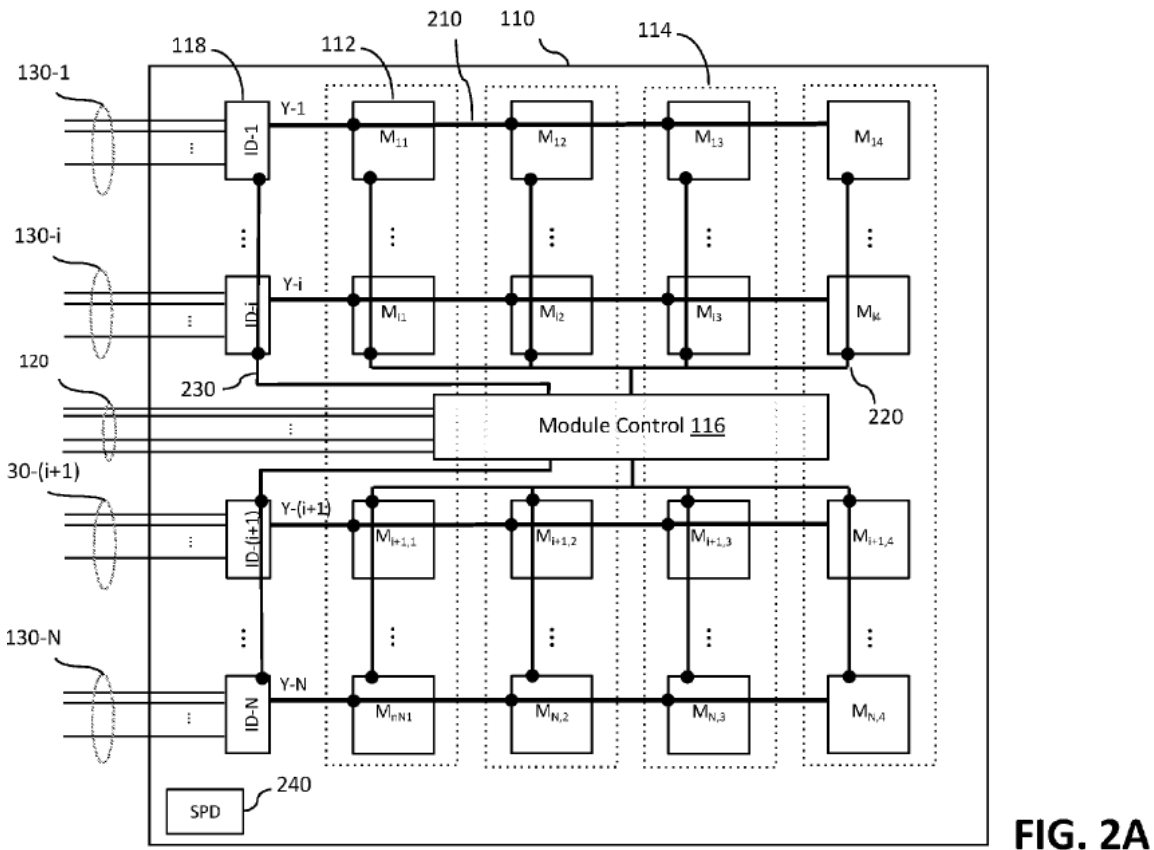
The parties identify the following matter as related to this case: *Netlist, Inc. v. Micron Technology, Inc., et al.*, Case No. 6:21-cv-00431-ADA (W.D. Tex.). Pet. 76; Paper 6, 1. Patent Owner states that matter was subsequently “transferred from the U.S. District Court for the Western District of Texas, Waco Division to the U.S. District Court for the Western District of Texas, Austin Division and docketed as” *Netlist, Inc. v. Micron*

Technology, Inc., et al., 1:22-cv-00136-LY (W.D. Tex.) (“parallel litigation”). Paper 6, 1.

Petitioner also identifies IPR2022-00237 as involving the child of the ’035 patent. Pet. 77. Petitioner further identifies IPR2017-00730 as involving the parent of the ’035 patent. *Id.* at 76.

C. The ’035 Patent (Ex. 1001)

The ’035 patent, titled “Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers,” relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 4:63–64.



As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:64–66, 6:1–5.

Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:18–23. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, e.g., group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:28–30; *see id.* at 3:25–27, 6:14–17. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:14–17, 6:27–29. For example, as shown along the top of memory module 110, isolation device ID-1 “is associated with [a] first group of memory devices M_{11} , M_{12} , M_{13} , and M_{14} , and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices” via module data/strobe lines 210. *Id.* at 6:17–21.

In operation, memory module 110 “perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.).” Ex. 1001, 3:27–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:27–32, 4:18–23, 4:64–67. For example, “[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118.” *Id.* at 7:60–63. And, “read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130.” *Id.* at 7:63–67.

As can be seen in Figure 2A, and as the '035 patent explains, there are “unbalanced” lengths of control wires to respective memory devices which causes a “variation of the timing” of signals due to the variation in wire

length. *See* Ex. 1001, 2:25–28; *see also id.* at 8:22–50. To account for timing issues, each isolation device, or data buffer, 118 is “responsible for providing a correct data timing” and “providing the correct control signal timing.” *Id.* at 8:59–65. In particular, “isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation.” *Id.* at 15:18–21. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to “properly time transmission” of a later read operation. *Id.* at 15:33–45.

D. Illustrative Claims

Claim 1, the sole independent claim of the ’035 patent, is reproduced below with limitation identifiers in brackets corresponding to claim analysis headings in the Petition. *See* Pet. 17–38.

1. [a] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

[b] a module board having edge connections for coupling to respective signal lines in the memory bus;

[c] a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and

[d] memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, [e] the memory devices including

a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

[f] a plurality of buffer circuits mounted on the module board in positions [g] corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, [h] the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and [i] logic configured to respond to the module control signals by enabling the data paths, [j] wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

Ex. 1001, 19:10–45.

E. Evidence

The Petition relies on the following references:

Reference	Exhibit No.
US 2010/0312925A1; filed June 3, 2010; published Dec. 9, 2010 (“Osanaï”).	1005
US 8,020,022B2; filed Sept. 12, 2008; issued Sept. 13, 2011 (“Tokuhiro”).	1006
US 8,713,379B2; filed Nov. 22, 2011; issued Apr. 29, 2014 (“Takefman”).	1007

Petitioner also relies on the Declaration of Donald Alpert, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1, 2, 6, 10–13, 21, and 22 would have been unpatentable on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 2, 6, 10–13, 21, 22	103(a) ¹	Osanai, Tokuhiro
2	1, 2, 6, 10–13, 21, 22	103(a)	Takefman, Tokuhiro
3	1, 2, 6, 10–13, 21, 22	103(a)	Takefman, Tokuhiro, Osanai

II. ANALYSIS

A. Discretion under 35 U.S.C. § 314(a)

Patent Owner argues that the Board should exercise its discretion under 35 U.S.C. § 314(a) and deny institution in light of the district court litigation involving the '035 patent. Prelim. Resp. 24–31. Petitioner argues the opposite. Pet. 72–74.

In assessing whether to exercise such discretion, the Board weighs six non-exclusive factors, known as the *Fintiv* factors. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv I*”). Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* On June 21, 2022, the Director of the USPTO issued a Memorandum² to clarify “the PTAB’s current application of *Fintiv* to discretionary institutions when there is

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Because the '035 patent claims priority before this date, the pre-AIA version of § 103 applies.

² Available at:

https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

parallel litigation” and “confirm[] that the precedential import of *Fintiv* is limited to the facts of that case.” Memorandum, 2. In particular, the Memorandum sets forth that: (1) the PTAB will not rely on the *Fintiv* factors to discretionarily deny institution “where a petition presents compelling evidence of unpatentability” (*id.* at 2); (2) the *Fintiv* factors do not apply to parallel U.S. International Trade Commission proceedings (*id.* at 2–3); (3) the PTAB will not discretionarily deny institution “where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB” (*id.* at 3); and (4) “the PTAB will consider the median time from filing to disposition of the civil trial for the district in which the parallel litigation resides” (*id.*). We have considered Patent Owner’s arguments in light of the *Fintiv* factors, together with Petitioner’s opposition, and we decline to exercise our discretion to deny the Petition as explained further below.

1. Factor 1: Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted

The first *Fintiv* factor requires consideration of whether the district court has stayed or will stay the proceeding pending *inter partes* review. “A district court stay of the litigation pending resolution of the PTAB trial allays concerns about inefficiency and duplication efforts.” *Fintiv*, Paper 11 at 6. Where a stay has been entered, we weigh this factor strongly against exercising discretion to deny instituting review. *Id.*

Patent Owner argues that there is no evidence that the district court would grant a stay if an IPR instituted. Prelim. Resp. 24. Petitioner contends that they do not know whether the district court will stay the case if trial is instituted. Pet. 74. Thus, based on both parties’ arguments and the

evidence submitted thus far, this factor neither weighs against nor for exercising our discretion to deny institution.

2. *Factor 2: Proximity of the Court's Trial Date to the Board's Projected Statutory Deadline*

If the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution. *Fintiv*, Paper 11 at 9. Here, the evidence submitted shows that no trial date has yet been set in the parallel litigation. *See* Ex. 2005 (Pre-Markman Scheduling Order). This factor, therefore, weighs heavily against exercising our discretion to deny institution.

3. *Factor 3: Investment in the Parallel Proceeding by the Court and Parties*

The third *Fintiv* factor considers “the amount and type of work already completed in the parallel litigation by the [district] court and the parties at the time of the institution decision.” *Fintiv*, Paper 11 at 9.

Petitioner contends that the district court in the parallel litigation “has not issued any substantive opinions regarding the scope or validity of the challenged claims, and given Petitioners' stipulations, the Court is unlikely to invest any resources on the grounds raised in this petition, either before or after the scheduled institution date.” Pet. 73. In contrast, Patent Owner argues that by the time an institution decision is rendered in this proceeding the parties will have file claim construction briefings and a claim construction hearing will have been conducted. Prelim. Resp. 25–26. Patent Owner also contends that “it is reasonable to presume that the district court will issue its claim construction decision prior to the institution deadline.” *Id.* at 26.

Having considered the record, we agree with Petitioner that the parallel proceeding is in an early stage. While claim construction briefings

have been filed, the record before us indicates that the district court has not yet considered the claim construction arguments or issued a claim construction order or any other substantive orders related to the '035 patent. “If, at the time of the institution decision, the district court has not issued orders related to the patent at issue in the petition, this fact weighs against exercising discretion to deny institution.” *Fintiv*, Paper 11 at 9–10.

Accordingly, we determine that this factor weighs against exercising our discretion to deny institution.

4. *Factor 4: Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

Petitioner argues that they “have stipulated that they will not pursue invalidity on the same grounds—or even the same references—if the Board institutes trial in this proceeding.” Pet. 72. Furthermore, Petitioner argues that “this Petition challenges claims 10–11 and 22, which are not at issue in the parallel litigation” and therefore the “claims-at-issue in both proceedings do not overlap and provide another reason that the fourth factor favors institution.” *Id.* at 72–73.

Patent Owner argues “Petitioners have asserted the exact same references against every asserted claim in the parallel litigation.” Prelim. Resp. 28 (citing Ex. 2009). Patent Owner points out that Petitioner’s stipulation is narrower than the stipulation considered by the Board in *Sotera Wireless, Inc. v. Masimo Corporation*, IPR2020-01019, Paper 12, 18–19 (PTAB Dec. 1, 2020) (precedential in relevant part), in that Petitioner only stipulates to not pursuing the same grounds presented in the Petition, rather than any ground raised or could have been raised in the Petition. *Id.* at 29. Thus, Patent Owner argues that the stipulation only marginally favors not exercising discretionary denial. *Id.*

We agree with Patent Owner and find that there is a substantial overlap of issues with the parallel litigation. *See* Ex. 2009 (identifying Osanai, Tokuhiro, and Takefman as references relied upon in the parallel litigation). However, we also find that Petitioner’s proposed stipulation, while narrower than the stipulation considered by the Board in *Sotera*, does potentially minimize duplication of effort and risk of inconsistent results at least with respect to the overlapping references and claims.

For this reason, taking into consideration the stipulation and the additional claims challenged in the Petition, we find that this factor weighs slightly against exercising our discretion to deny institution.

5. *Factor 5: Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party*

According to the fifth *Fintiv* factor, “[i]f a petitioner is unrelated to a defendant in an earlier [district] court proceeding, the Board has weighed this fact against exercising discretion to deny institution.” *See Fintiv*, Paper 11 at 13–14.

Here, Petitioner and Patent Owner are the defendant and plaintiff, respectively, in the parallel litigation. Therefore, we find that this factor weighs in favor of exercising our discretion to deny institution.

6. *Factor 6: Other Circumstances that Impact the Board’s Exercise of Discretion, Including the Merits*

As to the final *Fintiv* factor, “all the relevant circumstances,” including the merits, are considered in assessing whether to exercise discretion to deny institution of *inter partes* review. *Fintiv*, Paper 11 at 14.

Petitioner argues “the merits strongly favor institution as shown through the strength of the grounds in this petition.” Pet. 73. Patent Owner, on the other hand, argues that “Petitioners have not demonstrated a

reasonable likelihood of success due to fatal, facial flaws in the Petition.”
Prelim. Resp. 30.

As explained further below, we find Petitioner has made a reasonable, but not necessarily compelling, showing of prevailing against at least one of the challenged claims. Thus, this factor neither weighs against nor for exercising our discretion to deny institution.

7. *Balancing the Fintiv Factors*

We have considered the circumstances and facts before us in view of the *Fintiv* factors. Because our analysis is fact driven, no single factor is determinative of whether we exercise our discretion to deny institution under § 314(a). Instead, the factors considered are part of a balanced assessment of all relevant circumstances in the case. *Fintiv*, Paper 11 at 14. Here, no trial date has been set, there has been minimal investment in the parallel proceeding, and Petitioner has stipulated to not pursuing invalidity on the same grounds or the same references. Thus, factors 2, 3, and 4 weigh against exercising our discretion to deny institution, while the remaining factors are mostly neutral with factor 5 being the only factor weighing towards exercising our discretion to deny institution.

Balancing all of the factors, we determine that the circumstances presented here weigh against exercising discretion under § 314(a) to deny institution of *inter partes* review.

B. *Principles of Law*

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner’s declarant, Dr. Alpert, opines that:

a person of ordinary skill in the art in the field of the Challenged Patent would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers . . . an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

Ex. 1003 ¶ 42; *see* Pet. 4–5.

Patent Owner states that it “disputes Petitioners’ definition of the level of a person of ordinary skill in the art,” but does not present arguments in support of its assertion at this stage in the proceeding. Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, except that we find that the phrase “at least” in Petitioner’s proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor’s degree in such engineering disciplines and three years working in the field.

D. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner proposes that we “use Patent Owner’s proposed constructions” from the related proceedings. Pet. 10 (citing Ex. 1019).

Patent Owner states that it “does not propose that the Board construe any claims.” Prelim. Resp. 11.

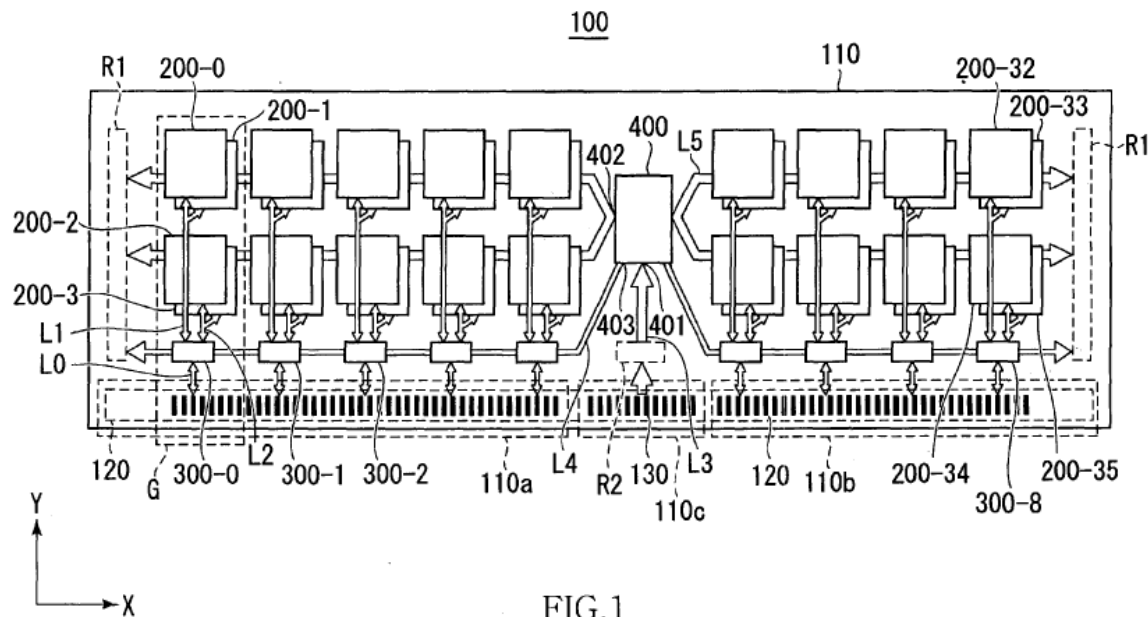
We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

E. Obviousness over Osanai and Tokuhiro (Ground 1)

Petitioner argues claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent would have been obvious over Osanai and Tokuhiko. Pet. 17–48. Below we provide a brief overview of the prior art references and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. *Osanai* (Ex. 1005)

Osanai relates to a memory module having memory chips and data register buffers arranged in a manner which shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is “a schematic diagram of a configuration of a memory module.” *Id.* ¶ 20.



As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. Ex. 1005 ¶ 51. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 52. Still further, memory module 100 includes “data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller” electrically connected to the connectors. *Id.* ¶¶ 53–54 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, “data register buffer 300 intervenes between the data connectors 120 and the memory chips 200.” *Id.* ¶ 109. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 26.

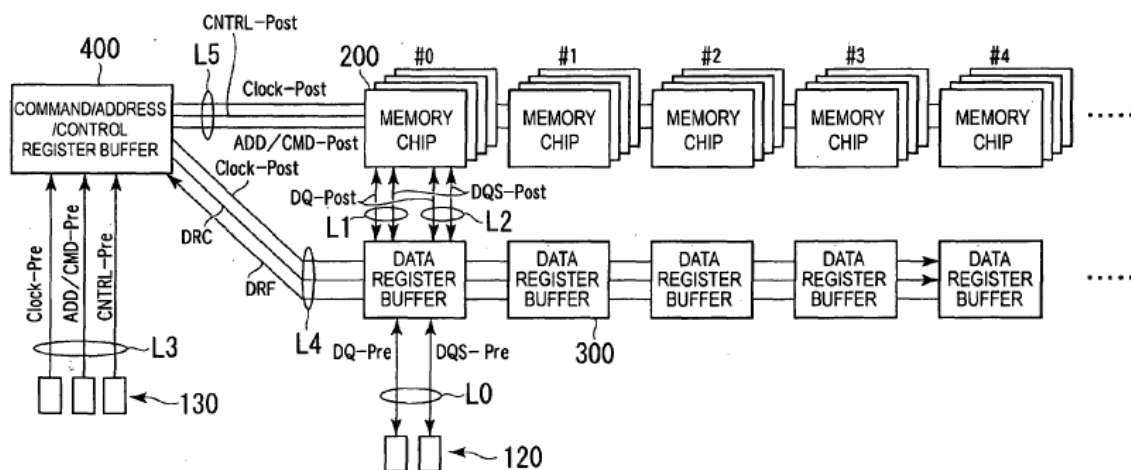


FIG. 7

As shown in Figure 7, “data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2.” Ex. 1005 ¶ 109. “[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal

DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.” *Id.*

Further, “[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post.” *Id.* ¶ 110. As such, “it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller.” *Id.* Osanai “adjust[s] a write timing or a read timing in consideration of a propagation time of a signal” via leveling operations. *Id.* ¶ 146. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 89.

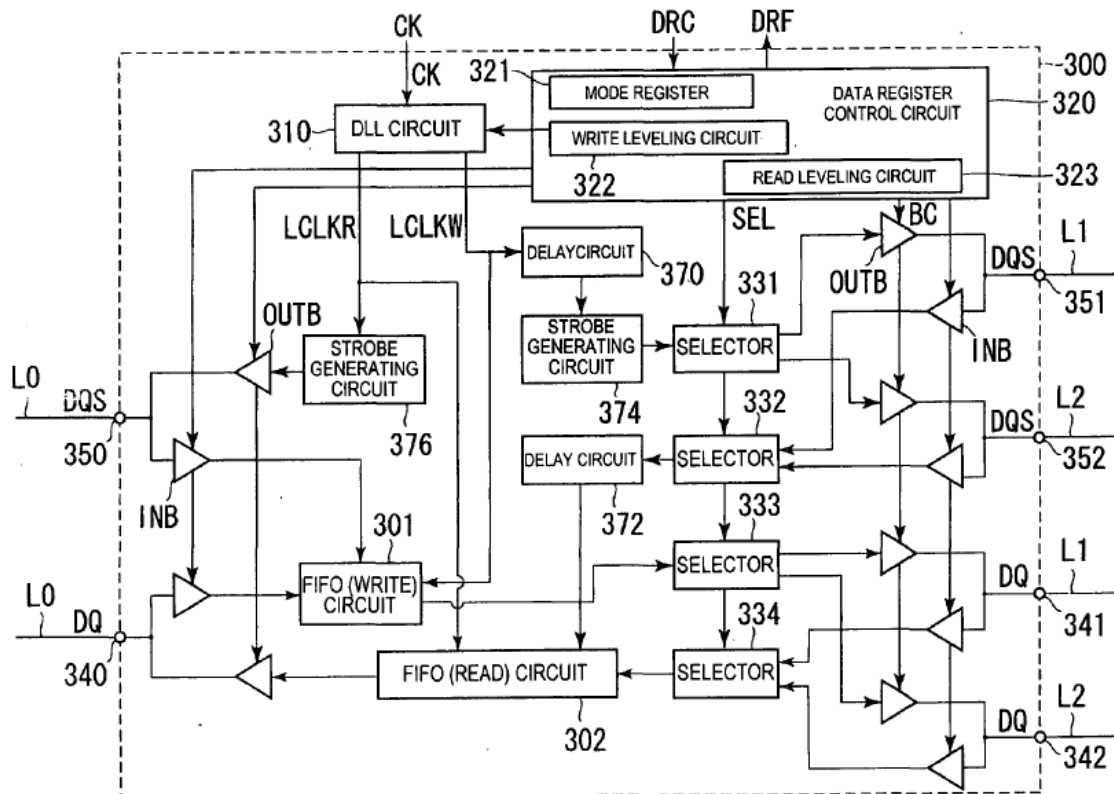


FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 151, 153. The write leveling and read leveling operations “adjust a write timing or a read timing in consideration of a propagation time of a signal.” *Id.* ¶ 146. For example, in a write operation, “[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” *Id.* ¶ 149. To compensate for that, “write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS.” *Id.* ¶ 151.

An exemplary read leveling operation also adjusts signal timing for a read operation. *See id.* ¶¶ 153–157. For example,

read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 157.

2. *Tokuhiro (Ex. 1006)*

Tokuhiro relates to a memory control circuit having “a write leveling function and control[ing] read/write operations by supplying a clock signal to a plurality of memories.” Ex. 1006, 3:16–20. Tokuhiro explains that, in memory interfaces, “a propagation delay is generated” because a “clock signal CK output from [a] memory controller 90 cannot reach all the [memory units] at the same time.” *Id.* at 1:63–2:1. Tokuhiro further explains that delay is addressed through a write leveling function for “adjusting (compensating) a delay time” of “data strobe signal DQS.” *Id.* at 2:10–18. The write level technique Tokuhiro describes “delaying, in [a] write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time.” *Id.* at 3:16–26.

In one example, “during the write operation, [a] first variable delay circuit DW delays the data strobe signal DQS output to the SDRAM by the first delay time Dt1 that has been set based on the write leveling function.” Ex. 1006, 14:66–15:2. Tokuhiro explains that a “delay time . . . calculated is provided as Delay (R)n. In other words, the second delay time Dt2 for the

data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling.” *Id.* at 16:19–23; *see id.* 16:1–18.

3. *Analysis of Claim 1*

a) *The preamble and undisputed limitations 1[b]–[i]*

Petitioner provides detailed analysis demonstrating that Osanai teaches the preamble and limitations 1[b]–1[i]. Pet. 17–33. Petitioner supports its arguments with citations to Osanai and to the testimony of Dr. Alpert. *Id.* Patent Owner does not separately dispute Petitioner’s contentions regarding any of these limitations. *See generally* Prelim. Resp. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Osanai teaches the preamble and limitations 1[b]–1[i] for the reasons provided by Petitioner.

For example, Petitioner identifies Osanai’s memory module 100, memory control hub 12, line 23, data connectors 120, and lines L0 and L3 as the respective “memory module,” “memory controller,” “memory bus,” and “signal lines” recited in the preamble. Pet. 17–21 (citing Ex. 1005 ¶¶ 54–55, 69–71, 75, 126, Figs. 1, 2; Ex. 1003 ¶¶ 73–80). Because we determine Petitioner has demonstrated that Osanai teaches the preamble, we need not decide at this juncture whether the preamble is limiting.

For limitation 1[b], Petitioner identifies data connectors 120 and 130, which Petitioner argues are located on the edge and connect the signal lines L0 and L3, as the claimed “edge connections for coupling to respective signal lines in the memory bus.” Pet. 21–22 (citing Ex. 1003 ¶ 82; Ex. 1005 ¶ 54, Fig. 1).

For limitation 1[c], Petitioner identifies Osanai’s command/address/control register buffer 400 as the claimed “module control

device.” Pet. 22–23 (citing Ex. 1005, ¶¶ 66, 101–103, Figs. 1, 6). Petitioner identifies memory controller 12 as the claimed “memory controller” and argues that it sends command/address/control signals to buffer 400. *Id.* at 23 (citing Ex. 1005 ¶¶ 53, 102). In response the register buffer 400 outputs address, command, clock, and control signals, which Petitioner argues teach the claimed “module command signal” and “module control signal.” *Id.* (citing Ex. 1005 ¶¶ 103, Fig. 6; Ex. 1003 ¶ 86).

For limitation 1[d], Petitioner identifies memory chips 200 mounted on memory module 100 as the recited “memory devices mounted on the module board.” Pet. 24 (citing Ex. 1005, Fig. 1; Ex. 1003 ¶ 90). Petitioner argues that memory chips 200 perform memory operations including read and write operations and thus “perform the first memory operation” as recited. *Id.* at 25 (citing Ex. 1005 ¶ 60, 90, 128–142; Ex. 1003 ¶ 90).

For limitation 1[e], Petitioner argues that Osanai’s memory chips 200 are grouped into sets making “a plurality of sets of memory devices,” as recited in claim 1. Pet. 25 (Ex. 1005 ¶ 58). Petitioner identifies lines L0, L1, and L2 as the recited “plurality of sets of data/strobe signal lines.” *Id.* at 26 (citing Ex. 1005 ¶ 109, Fig. 7; Ex. 1003 ¶ 94).

For limitation 1[f], Petitioner identifies Osanai’s register buffers 300 mounted in memory module 100 as the recited “plurality of buffer circuits mounted on the module board in positions.” Pet. 26–27 (citing Ex. 1005 ¶¶ 52, 61–62, 109, Fig. 1; Ex. 1003 ¶¶ 97–98).

For limitation 1[g], Petitioner argues that each data register buffer 300 is located between L0 data lines and its respective memory chip group. *Id.* at 28 (citing Ex. 1005 ¶¶ 57–58, 109, Fig. 7; Ex. 1003 ¶ 102). Thus, according to Petitioner, Osanai teaches a plurality of buffer circuits “corresponding to respective sets of the plurality of sets of data/strobe signal

lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices.” *Id.* at 28–29.

For limitation 1[h], Petitioner argues that each data register buffer 300 has data paths L1 and L2 connected to each memory chip group and that the data paths are used to transmit DQ-Post and DQS-Post signals. Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110, Figs. 1, 5, 7). Thus, according to Petitioner, Osanai teaches “each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation.” *Id.*

For limitation 1[i], Petitioner argues that Osanai’s data register control circuit 320 teaches the claimed “logic” and that this control circuit 320 enables different data paths for reading and writing operations depending on the DRC. Pet. 31–32 (citing Ex. 1005 ¶¶ 94, 96, 105, 106, 158, 163, Fig. 5; Ex. 1003 ¶ 111). According to Petitioner, a person of ordinary skill would have understood that data register control circuit 320 selects certain paths using certain signals and that this would have taught “logic configured to respond to the module control signals by enabling the data paths.” *Id.* at 32–33.

b) Disputed limitation [j]

Limitation [j] recites “wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.”

Ex. 1001, 19:39–45. Petitioner argues that the combination of Osanai and Tokuhiro teaches this limitation. Pet. 33–38 (citing Ex. 1003 ¶¶ 117–122;

Ex. 1005 ¶¶ 96, 110, 115–116, 146–164, Figs. 5, 7, 14A–17; Ex. 1006, 1:63–2:9, 2:46–49, 3:9–12, 3:16–26, 4:7–17, 16:1–28, claim 2). Petitioner acknowledges that while Osanai discloses the claimed “logic” it does not expressly disclose that the timing information is obtained during a second memory operation prior to the first memory operation. *Id.* at 33–34. Petitioner, therefore, relies on Tokuhiko for teaching this limitation.

Specifically, Petitioner argues that Osanai discloses both read and write leveling techniques that make timing adjustments by using the module clock signal. Pet. 34–36 (citing Ex. 1005 ¶¶ 96, 110, 115–116, 146–164, Figs. 5, 7; Ex. 1003 ¶¶ 117–118). Thus, Petitioner argues Osanai discloses “obtaining timing information” based on a module clock signal received by each respective buffer circuit. *Id.* at 36 (citing Ex. 1003 ¶ 118).

Petitioner argues that Tokuhiko also discloses read and write leveling techniques just as Osanai does. In addition, Petitioner argues Tokuhiko teaches a delay unit that obtains a first delay time from a write operation (i.e. “during a second memory operation”) to use in its calculation of a second delay time (“obtaining timing information”) used for a read operation. Pet. 37 (citing Ex. 1006, 3:16–26, 16:1–28; Ex. 1003 ¶ 121).

Petitioner argues that one of ordinary skill would have been motivated to use Tokuhiko’s technique in Osanai’s buffer leveling circuits for three reasons. The first is to reduce the number of steps needed to determine the read delay by basing that determination on timing information determine during write leveling. Pet. 39 (citing Ex. 1003 ¶ 126). The second is to reduce power consumption and reduce circuit area, thereby reducing costs by increasing manufacturing yield. *Id.* at 40 (citing Ex. 1006, 24:26–29, 21:15–24:42, Figs. 16–17; Ex. 1003 ¶ 127). The third reason to combine Tokuhiko with Osanai is to improve signal fidelity, decrease timing skew

among components and lower the load perceived by the memory controller. *Id.* at 40–41 (citing Ex. 1005 ¶¶ 4, 5, 75–76, 117–119, 176, 194; Ex. 1006, 1:63–2:28, 3:1–13; 3:16–26, 19:8–13, 19:25–33; Ex. 1003 ¶ 128).

Patent Owner argues that Petitioner does not show that Tokuhiko discloses “obtain[ing] timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation.” Prelim. Resp. 13–24. Specifically, Patent Owner argues that Tokuhiko does not obtain timing information during a second memory operation because during Tokuhiko’s write leveling function, no memory operations can be performed at all. *Id.* at 13. Patent Owner argues that Tokuhiko uses a known write leveling mechanism described in the Joint Electron Device Engineering Counsel (JEDEC) DDR3 standard. *Id.* at 16 (citing Ex. 1006, 1:22–26, 2:10–45). According to Patent Owner, during the write leveling mode described in the JEDEC DDR3 standard, the memory module is prohibited from performing any memory operations at the direction of the memory controller, or otherwise. *Id.* at 18–19 (citing Ex. 2003 at 38–41; Ex. 2004 at 39, 41, Fig. 14). Only after the write leveling mode ends can any memory operations resume. *Id.* at 21 (citing Ex. 2004, Fig. 16). Patent Owner argues, therefore, that any delay time set in write leveling is not timing information obtained during a memory operation because no memory operations can be performed during the write leveling function taught in Tokuhiko and the JEDEC DDR3 standard. *Id.* at 23.

As can be seen from Petitioner’s contentions and Patent Owner’s arguments summarized above, a central dispute between the parties is whether obtaining timing information during Tokuhiko’s write leveling operation teaches obtaining timing information during a second memory

operation as recited in claim 1. Specifically, Petitioner argues that Tokuhiro's write leveling operation teaches the claimed memory operation. *See* Pet. 37. We note here that Petitioner uses the phrases "write leveling operation" and "write operation" interchangeably in certain instances, implying that the write leveling operation is a write operation, and therefore a memory operation. *See id.* (explaining that "Tokuhiro teaches a delay unit that obtains a first delay time from a *write operation*" because "Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the *write level operation*." (emphases added)). Patent Owner, on the other hand, argues that no memory operations occur during Tokuhiro's write leveling operation. Prelim. Resp. 13–24.

At this stage of the proceeding, we are persuaded by Petitioner's arguments which we determine are supported by disclosures from Tokuhiro and by Dr. Alpert's unrebutted testimony. For example, Tokuhiro discloses that "the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling." Ex. 1006, 16:20–23. Tokuhiro further discloses "[A] first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time." *Id.* at 3:22–26. Dr. Alpert testifies that, based on these disclosures, a person of ordinary skill "would have recognized that, because Tokuhiro uses '*timing information*' determined during the write operation for a subsequent read operation, the write operation necessarily occurred before the read operation" (Ex. 1003 ¶ 121) and "that Tokuhiro . . . discloses that timing information determined during a write operation is used in determining a delay for subsequent read operations" (*id.* ¶ 122).

On the current record, we find Dr. Alpert's un rebutted testimony sufficient, particularly given Tokuhiro's teachings as described above. We find Patent Owner's arguments to be largely technical arguments that can be further developed at trial with the benefit of expert testimony from both sides regarding the disclosure in the JEDEC DDR3 standard and its applicability to Tokuhiro. Additionally, Patent Owner's argument does not address whether Tokuhiro's write leveling operation is a write operation as implied by Petitioner's arguments, or whether the write leveling operation itself teaches the recited "second memory operation" regardless of whether other memory operations are prohibited from being performed during the write leveling operation.

4. Analysis of 2, 6, 10–13, 21, and 22

Claims 2, 6, 10–13, 21, and 22 depend either directly or indirectly from independent claim 1. Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing that claims 2, 6, 10–13, 21, and 22 would have been obvious over the combination of Osanai and Tokuhiro. *See* Pet. 41–48. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See generally* Prelim. Resp.

5. Conclusion – Obviousness over Osanai and Tokuhiro (Ground 1)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent as obvious over Osanai and Tokuhiro.

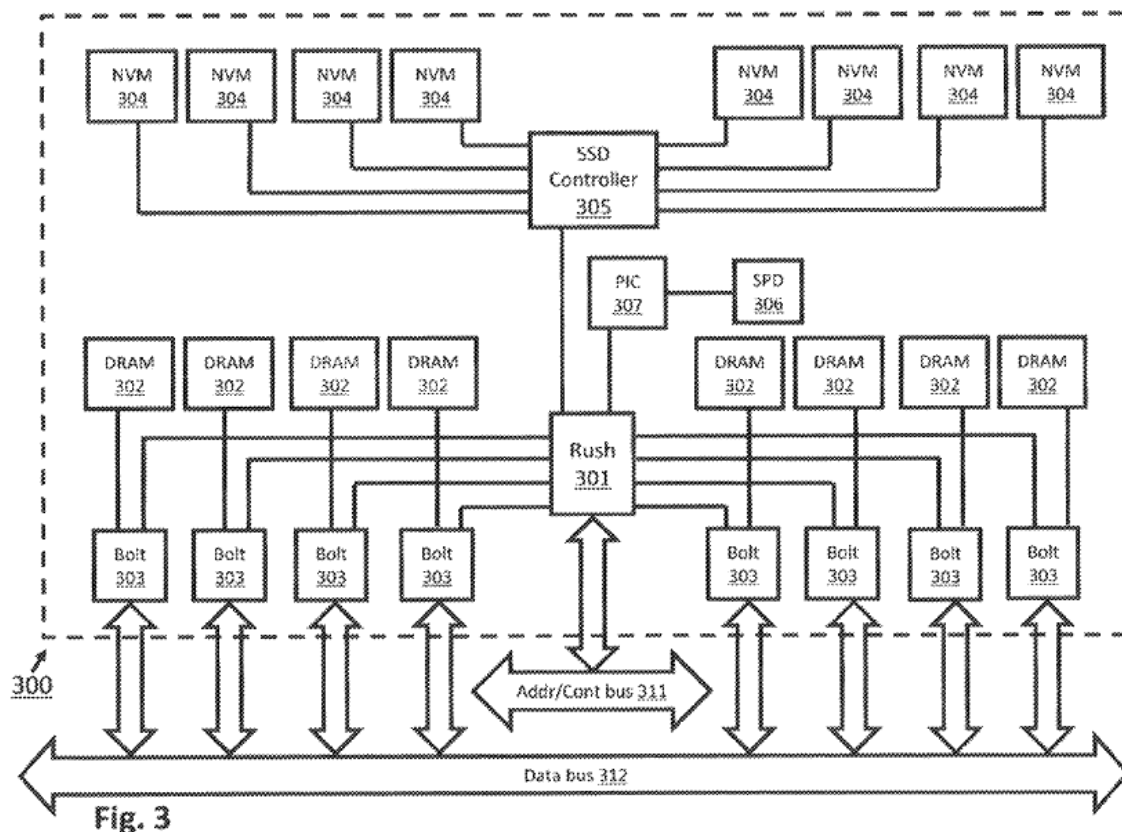
F. Obviousness over Takefman, Tokuhiro, and Osanai (Ground 3)

Petitioner argues claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent would have been obvious over Takefman, Tokuhiro and Osanai. Pet. 48–71.

Below we provide a brief overview of the prior art references and then analyze Petitioner’s contentions in light of Patent Owner’s arguments.

1. *Takefman (Ex. 1007)*

Takefman relates to a computer interface which uses a memory bus to connect a computer processing unit and a memory device. Ex. 1007, 1:48–55. Figure 3, reproduced below, is a block diagram of a “TerraDIMM,” a type of memory device. *Id.* at 2:5–6; *see id.* at 4:9, 4:27–29.



As shown in Figure 3, “TeraDIMM 300 includes an ASIC 301, herein the ‘Rush,’ a rank of DRAM devices 302, a number of data buffer devices 303, herein ‘Bolt’ devices, a rank of [non-volatile memory (NVM)] devices 304, [solid state disk (SSD)] controller 305, [serial presence detect (SPD)] 306, and a PIC microcontroller 307.” Ex. 1007, 5:53–59. Further, “address/control bus 311 is connected to the Rush 301 while the main

memory bus 312 is separated from the on-DIMM memory bus by the Bolt devices 303.” *Id.* at 5:67–6:3. Still further, “Rush 301 also includes control circuitry for the Bolt devices 303” and “SSD controller 305 manages the flow of data going to and from the NVM devices 304.” *Id.* at 5:62–66.

Takefman explains that

[e]ach of the Bolt devices include three DDR-3 ports . . . that allow the host port (connected to the memory bus) to connect to any of the three DDR-3 ports. Furthermore, each port of the DDR-3 ports can be tri-stated and can signal using DDR-3 DQ/DQS signaling. Bolt devices 303 provide retiming of data bursts from the computer system to/from the DRAM devices 302 or Rush 301. Bolt devices 303 also provide a separation that allows on-DIMM DMA (direct memory access) to occur between the DRAM devices 302 and the Rush 301.

Id. at 6:4–13.

Takefman further explains that

[o]ne aspect to the Rush 301 data interface is the inclusion of per-lane delay compensation circuits that, for instance, provide programmable launch times and lane de-skew on receive. Because of the difference in the distances between the Bolt devices 303 and the Rush 301 and the Bolt devices 303 and the DRAM devices 302, the TeraDIMM may arrange its launch time Such that its data arrives at an appropriate time.

Id. at 6:14–20.

2. Analysis of Claim 1

a) The preamble and undisputed limitations 1[b]–1[i]

Petitioner provides detailed analysis demonstrating that Takefman and Osanai teach the preamble and limitations 1[b]–1[i]. Pet. 48–64. Petitioner supports its arguments with citations to Takefman, Osanai, and to the testimony of Dr. Alpert. *Id.* Patent Owner does not separately dispute Petitioner’s contentions regarding any of these limitations. *See generally*

Prelim. Resp. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Takefman and Osanai teach the preamble and limitations 1[b]–1[i] for the reasons provided by Petitioner.

For example, with respect to the preamble, Petitioner identifies Takefman’s memory module, DRAM 302, and bolt devices 303 as the recited “memory module,” “memory units,” and “plurality of buffer circuits,” respectively. Pet. 48 (citing Ex. 1003 ¶ 154, Ex. 1007, Fig. 3). Petitioner further argues that Takefman’s address control bus 311 and data bus 312 includes a set of control/address signal lines and a plurality of set of data/strobe signal lines. *Id.* at 51 (citing Ex. 1007, 1:58–3:6, 5:67–6:3, 7:64–8:3, Fig. 3; Ex. 1003 ¶¶ 157–158). Petitioner argues that to the extent Takefman does not explicitly disclose that data bus 312 includes data/strobe signal lines, a person of ordinary skill would have known, based on the disclosure of Osanai (as discussed above with respect to Ground 1) the memory buses include data/strobe signal lines. *Id.* at 51–52 (Ex. 1003 ¶ 158). Petitioner provides testimony from Dr. Alpert that a person of ordinary skill would have found it obvious to incorporate these data/strobe signal lines into Takefman’s data bus 312 to ensure the proper timing of read and write commands. *Id.* at 52 (citing Ex. 1003 ¶ 158). Because we determine Petitioner has demonstrated that the combination of Osanai, Takefman, and Tokuhito teaches the preamble, we need not decide at this juncture whether the preamble is limiting.

For limitation 1[b], Petitioner argues that Takefman teaches “a module board having edge connections for coupling to respective signal lines in the memory bus” and provides support from Takefman’s disclosure

and from Dr. Alpert's testimony. Pet. 53 (citing Ex. 1003 ¶ 161; Ex. 1007, 4:8–29, 4:47–53, 5:53–6:26, Fig. 1).

For limitation 1[c], Petitioner identifies Rush 301 as the recited “module control device” and argues that it is configured to receive memory commands, such as read and write commands, directly from the address/control bus 311. Petitioner provides support from Takefman's disclosure and Dr. Alpert's testimony. Pet. 53–55 (citing Ex. 1003 ¶ 164; Ex. 1007, 1:58–3:6, 5:44–47, 5:67–6:3, 19:38–46, 21:11–48, 21:49–22:15, Fig. 3).

For limitation 1[d], Petitioner identifies DRAM 302 as the recited “memory devices” and memory module 300 as the recited “module board” and argues that a person of ordinary skill would have recognized DRAM 302 receives “module command signals” from Rush 301 that instruct the DRAM to perform certain operations such as a write operation. Pet. 56 (citing Ex. 1007, 19:38–46, 21:49–22:15; Ex. 1003 ¶ 168).

For limitation 1[e], Petitioner argues that Takefman teaches “memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines.” Pet. 56–57. Petitioner argues that Takefman's DRAM 302 is organized into ranks and that the memory controller selects each rank using chip-select signals. *Id.* (citing Ex. 1003 ¶ 171; Ex. 1007, 5:8–52, 5:67–6:3, Fig. 3).

For limitation 1[f], Petitioner argues Takefman teaches “*a plurality of buffer circuits mounted on the module board in positions.*” Pet. 57–58. For example, Petitioner identifies bolt devices 303 as the recited “buffer circuits” and argues that they are mounted on module board 300. *Id.* at 57–58 (citing Ex. 1003 ¶ 174; Ex. 1007, 5:60–6:26, Fig. 3).

For limitation 1[g], Petitioner further argues that the bolt devices 303 correspond to “respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices.” Pet. 58–60 (citing Ex. 1003 ¶¶ 177–178; Ex. 1007, 5:4–10, 5:12–15, 5:67–6:9, Fig. 3).

For limitation 1[h], Petitioner argues Takefman teaches that “each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation.” Pet. 60–61 (citing Ex. 1003 ¶ 181; Ex. 1007, 4:33–40, 5:44–48, 6:7–11).

For limitation 1[i], Petitioner argues Takefman teaches “logic configured to respond to the module control signals by enabling the data paths.” Pet. 61–62 (citing Ex. 1003 ¶¶ 184–185; Ex. 1007, 6:14–26, Fig. 3). Petitioner argues that based on Osanai’s disclosures discussed above with respect to Ground 1, a person of ordinary skill would have known of leveling circuits for compensating for propagation delays caused by memory chips 200 and their respective buffers 300 are located at different distances. *Id.* at 62 (citing Ex. 1005 ¶¶ 146–149; Ex. 1003 ¶ 185). Petitioner supports its arguments with Dr. Alpert’s testimony that a person of ordinary skill would be motivated to use this knowledge of read/write leveling circuits buffers to modify Takefman’s bolt devices 303 to address each individualized distances that cause propagation delays. *Id.* (citing Ex. 1003 ¶ 185). According to Petitioner a person of ordinary skill would have designed the bolt devices to include logic that both performs compensation adjustments and enables data paths. *Id.* Petitioner argues a POSITA would have been motivated to make this modification as a simple matter of the design choice in including this functionality in Rush circuitry as compared to

the individual bolt devices underlying each memory device. *Id.* According to Petitioner, a POSITA would also be motivated to make this modification to provide greater flexibility to the bolt devices in terms of allowing for a variable number of memory devices. *Id.*

b) Disputed limitation [j]

Limitation [j] recites “wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.”

Ex. 1001, 19:39–45. Petitioner argues that Takefman discloses the claimed “logic” but does not expressly disclose that the timing information is obtained “during a second memory operation prior to the first memory operation.” Pet. 63. Petitioner, therefore, relies on Tokuhiko, as it did in Ground 1, arguing that Tokuhiko teaches obtaining timing information “during a second memory operation prior to the first memory operation.” *Id.* at 63–66 (citing Ex. 1003 ¶¶ 188–191, 193–196; Ex. 1006, 1:15–20, 21:15–24:42, Figs. 16–17; Ex. 1007, 1:15–18, 6:9–11, 6:14–20, Fig. 3).

Petitioner contends that a person of ordinary skill “would have been motivated to incorporate Tokuhiko’s leveling technique in each of Takefman’s bolt devices 303, with or without being modified based on a POSITA’s knowledge, for four reasons.” Pet. 65. Specifically:

First, such a person would have recognized that this modification would implement Tokuhiko’s well-known technique in Takefman’s bolt devices 303 to achieve the same benefit achieved by Tokuhiko’s device, i.e., reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling.

Second, and as explained above, a POSITA would have been motivated to do so based on the express teaching found in Tokuhiro. *Third*, a POSITA would have been motivated to modify Takefman's bolt devices 303 to incorporate Tokuhiro's teaching to improve signal fidelity, decrease timing skew among components, and/or lower the load perceived by the memory controller. *Fourth*, and as explained above, making such a modification would be the application of a known technique to a known device (method, or product) ready for improvement to yield predictable results. *Id.* at 65–66 (citing Ex. 1003 ¶¶ 193–196; Ex. 1007, 21:15–24:42, Figs. 16–17).

Patent Owner makes the same arguments here as it does for the same limitation of claim 1 in Ground 1. Prelim. Resp. 13–24. For the same reasons explained above (*see supra* § II.E.3.b) we are persuaded by Petitioner's arguments at this stage of the proceeding.

3. Analysis of 2, 6, 10–13, 21, and 22

Claims 2, 6, 10–13, 21, and 22 depend either directly or indirectly from independent claim 1. Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing that claims 2, 6, 10–13, 21, and 22 would have been obvious over the combination of Takefman, Tokuhiro, and Osanai. *See* Pet. 66–71. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See generally* Prelim. Resp.

4. Conclusion – Obviousness over Takefman, Tokuhiro and Osanai (Ground 3)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent as obvious over Takefman, Tokuhiro, and Osani.

G. Obviousness over Takefman and Tokuhiro (Ground 2)

Petitioner argues claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent would have been obvious over Takefman and Tokuhiro. Pet. 48–70. In its contentions, Petitioner argues that several limitations, though not explicitly disclosed by Takefman (or Tokuhiro), would have been obvious nonetheless, based on the knowledge of a person of ordinary skill in the art. *Id.* As evidence of this knowledge, Petitioner relies on Osanai and supporting testimony from Dr. Alpert. *Id.* For example, as explained above in our analysis of Ground 3, Petitioner argues that to the extent Takefman does not explicitly disclose that its data bus 312 includes data/strobe signal lines, a person of ordinary skill would have understood that modifying Takefman to include these claimed lines would have been obvious in light of the teachings of Osanai. *Id.* at 51–52. Petitioner also contends that the modification would have been obvious because it would have complied with the JEDEC standards, which “necessarily include signal lines to carry DQ/DQS and CK signals.” *Id.* at 52. Similarly, Petitioner argues that to the extent Takefman does not explicitly disclose “logic configured to respond to the module control signals by enabling the data paths” that such logic would be obvious in light of the teachings of Osanai. *Id.* at 62 (citing Ex. 1005 ¶¶ 146–149).

We do not discern from our review of Takefman that it explicitly discloses the aforementioned limitations. Given that Takefman does not explicitly disclose these limitations, we have concerns about the sufficiency of Petitioner’s showing, particularly as to whether Petitioner has sufficiently articulated a reason why a person of ordinary skill in the art would have modified the Takefman and Tokuhiro combination to include the missing

limitations. At trial, if Petitioner so chooses, the record would benefit from development of these issues.

III. CONCLUSION

Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one challenged claim of the '035 patent. At this stage of the proceeding, however, we have not made a final determination with respect to the patentability of the challenged claims.

IV. ORDER

For the foregoing reasons, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '035 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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Patent 9,824,035 B2

For PETITIONER:

Matthew Hopkins
WINSTON & STRAWN LLP
mhopkins@winston.com

For PATENT OWNER:

Rex Hwang
Ryan Hargrave
Michael Ricketts
SKIERMONT DERBY LLP
rhwang@skiermontderby.com
rhargrave@skiermontderby.com
mricketts@skiermontderby.com