

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00711
Patent 10,860,506 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and
NABEEL U. KHAN, *Administrative Patent Judges*.

KHAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co. Ltd.¹ (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–20 (“the challenged claims”) of U.S. Patent No. 10,860,506 B2 (“the ’506 patent,” Ex. 1001). Netlist, Inc. (“Patent Owner”) timely filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the ’506 patent, and we institute an *inter partes* review as to the challenged claims of the ’506 patent on all the grounds of unpatentability set forth in the Petition.

B. Related Proceedings

The parties identify the following matters as related to this case:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.);
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, Case No. 2:21-cv-00463 (E.D. Tex.);
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.);

¹ Petitioner also identifies Samsung Semiconductor, Inc. as a real party-in-interest. Pet. xxiii.

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236 (PTAB);
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237 (PTAB); and
- U.S. Patent Application No. 17/114,478.

Pet. xxiii; Paper 8, 1.

C. The '506 Patent (Ex. 1001)

The '506 patent, titled “Memory Module with Timing-Controlled Data Buffering,” relates to a memory system that controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 4:65–66.

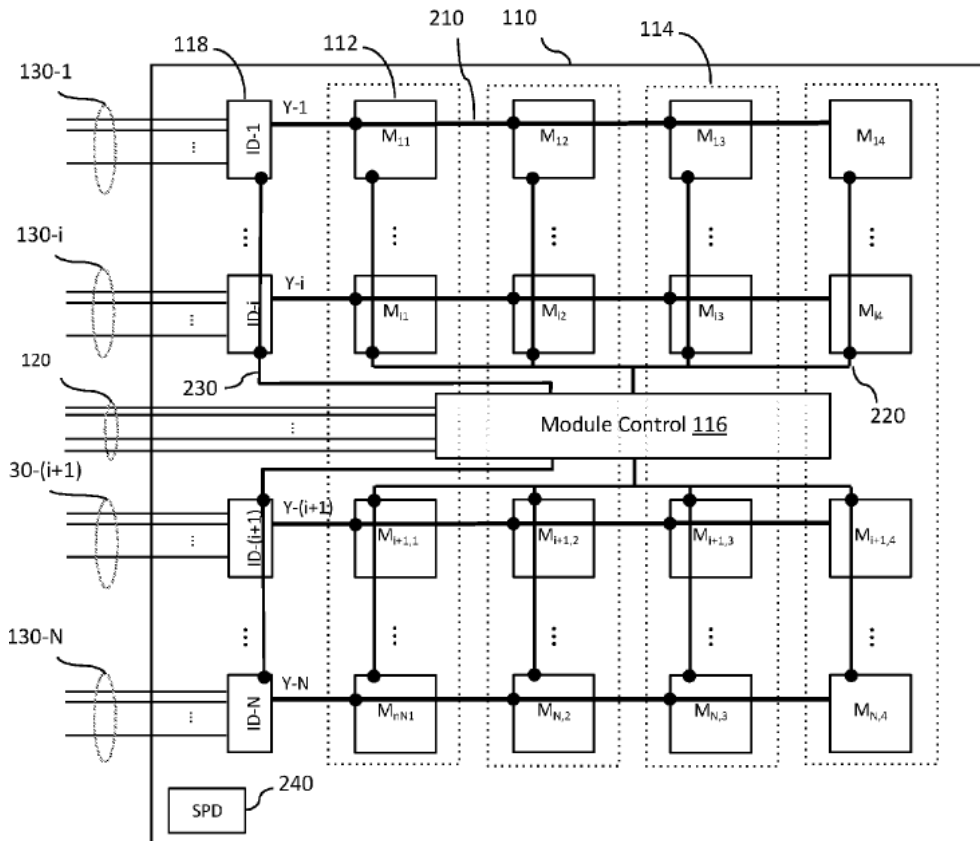


FIG. 2A

As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:65–67, 6:4–8.

Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:20–25. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, *e.g.*, group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:30–32; *see id.* at 3:27–29, 6:17–20. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. For example, as shown along the top of memory module 110, isolation device ID-1 “is associated with [a] first group of memory devices M_{11} , M_{12} , M_{13} , and M_{14} , and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices” via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 “perform[s] memory operations in response to memory commands (*e.g.*, read, write, refresh, precharge, etc.).” Ex. 1001, 3:30–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:29–34, 4:20–25, 4:65–5:1. For example, “[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118.” *Id.* at 7:63–66. And, “read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130.” *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the ’506 patent explains, there are “unbalanced” lengths of control wires to respective memory devices, which cause a “variation of the timing” of signals due to the variation in wire

length. *See* Ex. 1001, 2:20–30; *see also id.* at 8:26–55. To account for timing issues, each isolation device, or data buffer, 118 is “responsible for providing a correct data timing” and “for providing the correct control signal timing.” *Id.* at 8:64–9:3. In particular, “isolation devices 118 includes [a] signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation.” *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information that is used to “properly time transmission” of a later read operation. *Id.* at 15:42–50.

D. Illustrative Claims

Claims 1 and 14 are the independent claims of the ’506 patent. Claim 1, which is representative of the challenged claims, is reproduced below with limitation identifiers in brackets corresponding to claim analysis headings in the Petition. *See* Pet. 20–38.

1. [pre] A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:

[a] a module board having edge connections to be coupled to respective signal lines in the memory bus;

[b] a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;

[c1] memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, [c2] wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read

data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and

[d] data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and [e] wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

[f] delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

[g] sample the first section of the read data using the first delayed read strobe; and

[h] transmit the first section of the read data to a first section of the data bus;

[i] wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

Ex. 1001, 19:16–55.

E. Evidence

The Petition relies on the following references:

Reference	Exhibit No.
US 2010/0312956 A1; filed June 3, 2010; published Dec. 9, 2010 (“Hiraishi”).	1005
US 8,020,022 B2; filed Sept. 12, 2008; issued Sept. 13, 2011 (“Tokuhiko”).	1006
US 2006/0277355 A1; filed June 1, 2005; published Dec. 7, 2006 (“Ellsberry”).	1007
US 6,184,701 B1; filed May 27, 1999; issued Feb. 6, 2001 (“Kim”).	1008

Reference	Exhibit No.
US 2007/0008791 A1; filed July 7, 2005; published Jan. 11, 2007 (“Butt”).	1029

Petitioner also relies on the Declaration of Robert G. Wedig, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–20 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a) ²	Hiraishi, Butt
3, 5, 12, 16	103(a)	Hiraishi, Butt, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Kim
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt, Tokuhiro
3, 5, 12, 16	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Tokuhiro, Kim

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. For this proceeding, Petitioner assumes that the ’506 patent has an effective priority date before this date (Pet. 2) and applies the pre-AIA version of § 103.

Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner contends a person of ordinary skill in the art “would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor’s degree in such engineering disciplines and at least three years of work experience in the field.” Pet. 2 (citing Ex. 1003 ¶ 37). Patent Owner asserts it is “applying the level of ordinary skill in the art proposed by Petitioner.” Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, except that we find that the phrase “at least” in Petitioner’s proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years of work experience in the field of memory module design and operation, or a bachelor’s degree in such engineering disciplines and three years of work experience in the field.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Neither party proposes any constructions for any claim terms. *See* Prelim. Resp; *see also* Pet. 9.³ We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

D. Obviousness over Hiraishi and Butt (Ground 1)

Petitioner argues claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent would have been obvious over Hiraishi and Butt. Pet. 20–68. Below we provide a brief overview of the prior art references and analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Hiraishi (Ex. 1005)

Hiraishi relates to a memory module having memory chips and data register buffers arranged in a manner that shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is “a schematic diagram of a configuration of a memory module.” *Id.* ¶ 13.

³ Petitioner indicates that it may assert in the related District Court case that “certain terms in the '506 [p]atent are subject to § 112, ¶ 6, and indefinite for failure to disclose an adequate structure or algorithm,” but, for purposes of its Petition, “adopts Patent Owner's current position on claim construction that § 112, ¶ 6 does not apply.” Pet. 9–10.

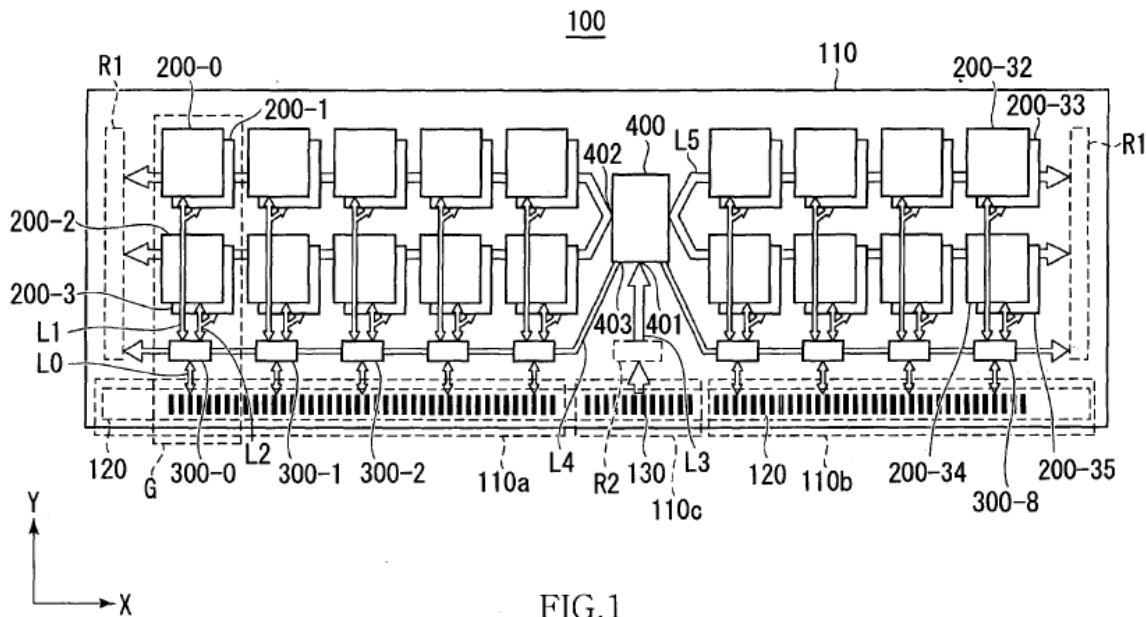


FIG. 1

As shown in Figure 1, memory module 100 includes “a plurality of memory chips 200 mounted on [a] module substrate 110.” Ex. 1005 ¶ 45. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 46. Still further, memory module 100 includes “data connectors 120[, which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller” electrically connected to the connectors. *Id.* ¶¶ 47–48 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, “data register buffer 300 intervenes between the data connectors 120 and the memory chips 200.” *Id.* ¶ 103. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 19.

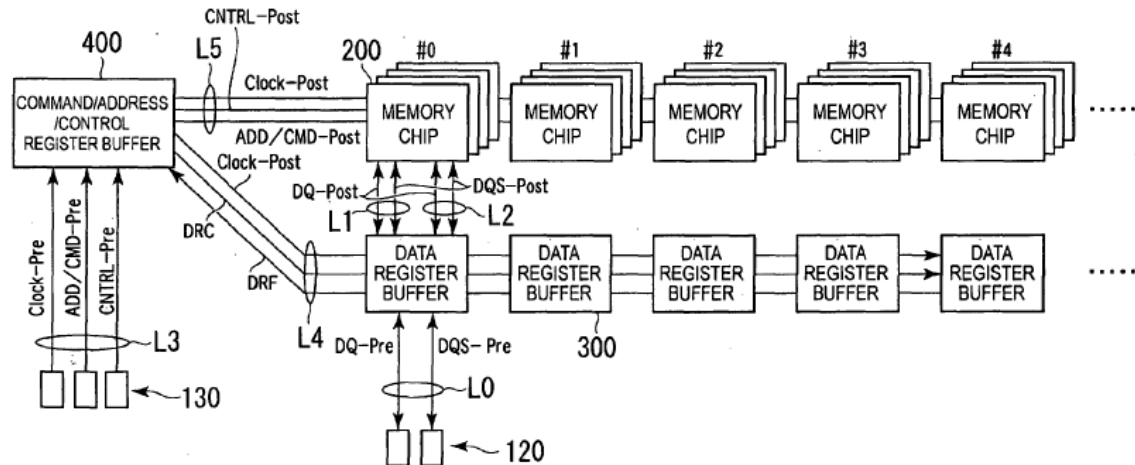


FIG. 7

As shown in Figure 7, “data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2.” Ex. 1005 ¶ 103. “[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.” *Id.*

Further, “[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post.” *Id.* ¶ 104. As such, “it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller.” *Id.* Hiraishi “adjust[s] a write timing or a read timing in consideration of a propagation time of a signal” via leveling operations. *Id.* ¶ 140. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which

is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 83.

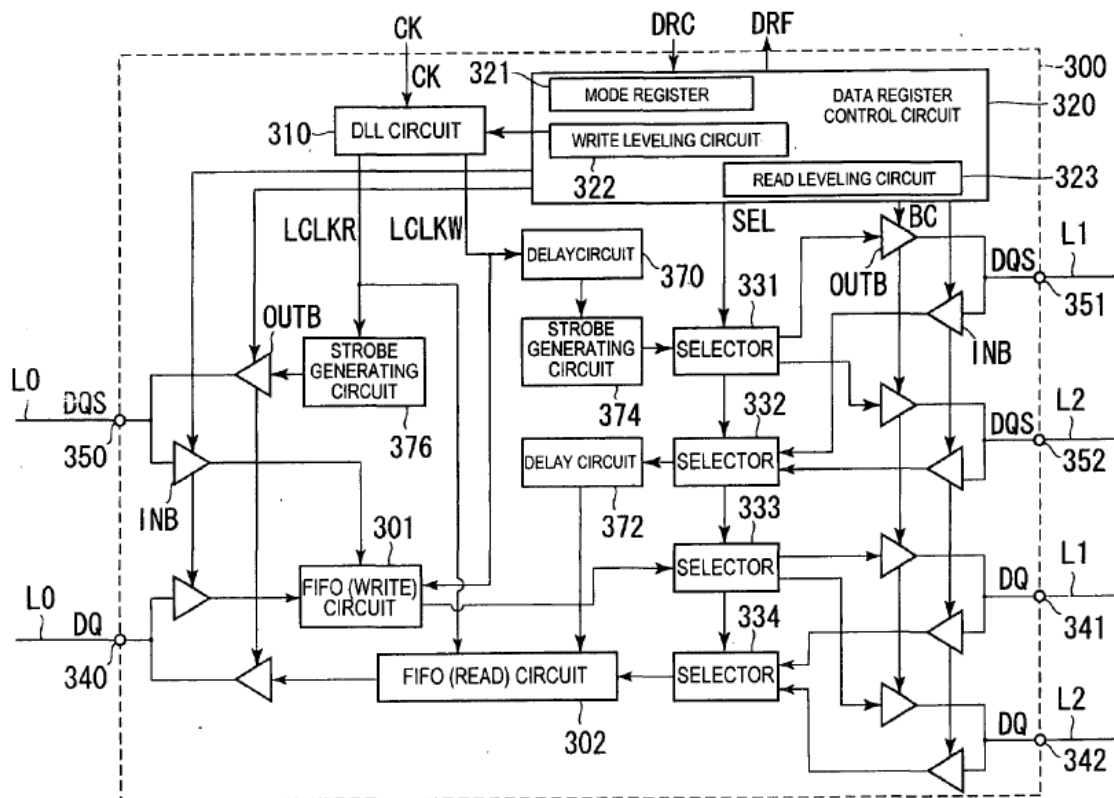


FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 90, 145, 147. The write leveling and read leveling operations “adjust a write timing or a read timing in consideration of a propagation time of a signal.” *Id.* ¶ 140. For example, in a write operation, “[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” *Id.* ¶ 143. To compensate for that, “write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS.” *Id.* ¶ 145.

An exemplary read leveling operation also adjusts signal timing for a read operation. *See* Ex. 1005 ¶¶ 147–151. For example,

read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 151.

2. *Butt* (Ex. 1029)

Butt relates to DQS strobe centering that is “suitable for a DDR memory application.” Ex. 1029 ¶ 2. Figure 2, reproduced below, is a “detailed block diagram of a read data logic and signal paths of a memory interface.” *Id.* ¶ 9.

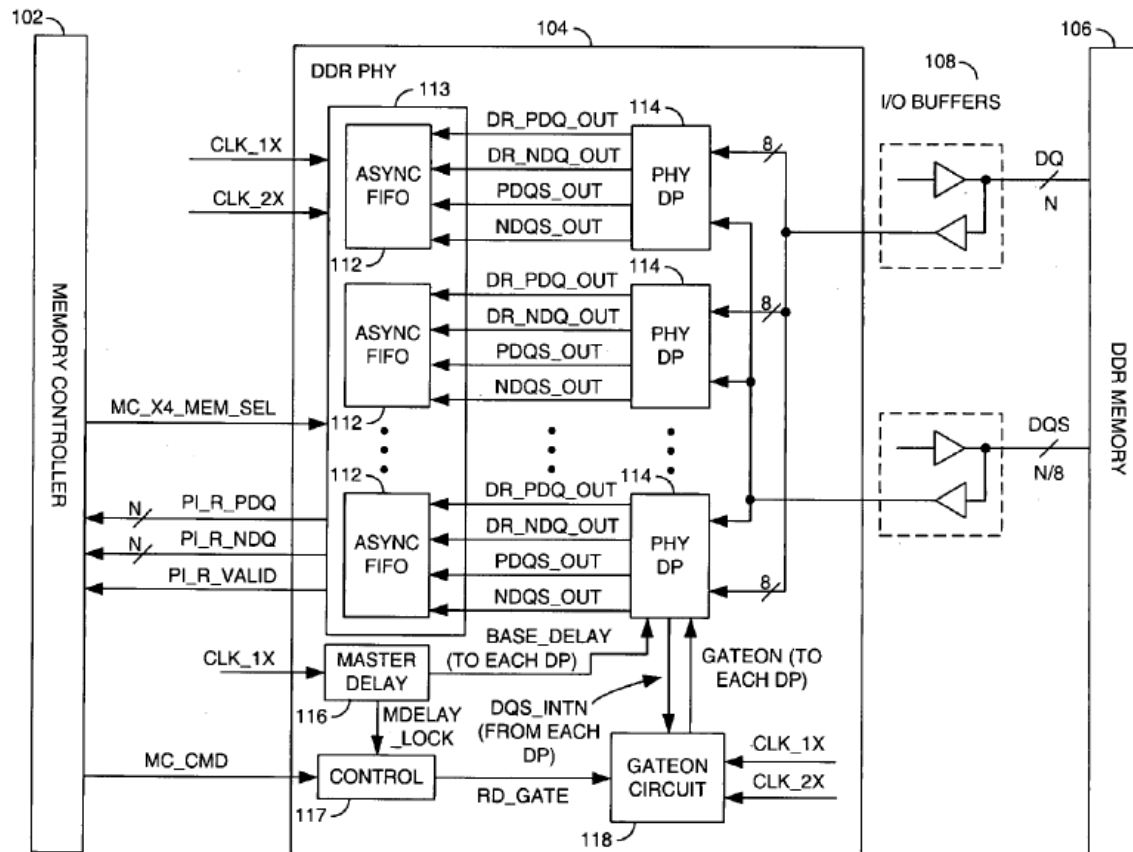


FIG. 2

As shown in Figure 2, a system includes memory controller 102, memory interface 104, and one or more double data rate (DDR) synchronous dynamic random-access memory (SDRAM) devices 106. Ex. 1029, ¶¶ 15, 17. The circuit 104 comprises “a number of asynchronous (ASYNC) first-in first-out (FIFO) buffers 112, FIFO synchronization logic 113, a number of physical read datapaths (DPs) 114, a master delay (MDELAY) logic 116, a control logic 117 and a programmable gating signal generator 118.” *Id.* ¶ 17. Each of the physical read datapaths 114 is “configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal

(e.g., GATEON) from the programmable gating signal generator 118.” *Id.* The DPs are “configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116.” *Id.* ¶ 18.

3. Analysis of Claim 1

a) Preamble and Undisputed Limitations 1[a]–1[e]

Petitioner provides detailed analysis demonstrating that Hiraishi and Butt teach the preamble and limitations 1[a]–1[e]. Pet. 21–35. Petitioner supports its arguments with citations to Hiraishi and Butt and to the testimony of Dr. Wedig. *Id.* Patent Owner does not separately dispute Petitioner’s contentions regarding the preamble and these limitations. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Hiraishi and Butt teach the preamble and limitations 1[b]–1[e] for the reasons provided by Petitioner, which we summarize below.

For example, for the preamble Petitioner identifies Hiraishi’s memory module 100 as teaching the recited “memory module,” memory control hub (MCH 12) as teaching the recited “memory controller,” and bus 23 with data lines L0 as teaching the recited “data bus.” Pet. 21 (citing Ex. 1005 ¶¶ 65, 69, Figs. 1–3; Ex. 1003 ¶¶ 101–102). Petitioner argues that Hiraishi’s memory module 100 connects to MCH 12 by a memory bus 23 and that bus 23 includes a set of control/address signal lines. *Id.* at 22–23 (citing Ex. 1005 ¶¶ 47, 49, 60, 69, 102–103, 107, Figs. 1, 3, 7; Ex. 1003 ¶¶ 102–103).

For limitation 1[a] Petitioner identifies Hiraishi’s module substrate 110 as the recited “module board,” and command/address/control connectors 130 and data connectors 120 as the recited “edge connections.” Pet. 23 (citing Ex. 1005 ¶¶ 45, 47–49, Fig. 1; Ex. 1003 ¶¶ 104–107).

For limitation 1[b] Petitioner identifies Hiraishi's command/address/control register buffer 400 as the recited "module control device on the module board." Pet. 24–25 (citing Ex. 1005 ¶¶ 59, Fig. 1; Ex. 1003 ¶¶ 108–109). Petitioner argues Hiraishi's register buffer 400 is configurable to receive C/A signals corresponding to a read operation through command/address/control connectors 130 and line L3 and to output C/A signals and control signals such as the DRC and Clock-Post signal on line L5. *Id.* at 25 (citing Ex. 1005 ¶¶ 18–19, 47, 60, 97, 99, Figs. 1, 6, 7; Ex. 1003 ¶ 110).

For limitation 1[c1] Petitioner argues that Hiraishi teaches memory devices, depicted in Figure 5 as 200-0 to 200-35, arranged in four different ranks on module board 110 and coupled to register buffer 400 by data line L5. Pet. 28–29 (citing Ex. 1005 ¶¶ 45, 50–52, 107, Figs. 1, 7; Ex. 1003 ¶¶ 114–116).

For limitation 1[c2] Petitioner argues that Hiraishi's memory devices 200 are situated in ranks and correspond to respective sets of data/strobe signal lines such as line L0 depicted in Figure 7 and are connected to data register buffers. Pet. 30 (citing Ex. 1005 ¶¶ 51–54, 56, 76, 79–80, 103, 120–129, Figs. 1, 4, 7; Ex. 1003 ¶ 119). Petitioner argues that, consistent with the JEDEC standard, read commands include a chip select signal that command all memory devices in the selected rank to perform the command together. *Id.* at 30–31 (citing Ex. 1021 at 319, 413; Ex. 1020, 13, 22, 34 n.1; Ex. 1018, 4.20.4-6, 4.20.4-10–4.20.4-16; Ex. 1003 ¶¶ 120–121).

For limitation 1[d] Petitioner argues that Hiraishi's data register buffers 300 are positioned between the set of memory devices 200 and the connectors 120 connecting to the data line L0 and that the data register buffers 300 are coupled to memory devices 200. Pet. 31 (citing Ex. 1003

¶¶ 122–126). Petitioner argues that data buffer 300 receives module command/address/control line L4 from command/address/control register buffer 400. *Id.* at 31–33 (citing Ex. 1005, Figs. 1, 5, 7; Ex. 1003 ¶¶ 122–126).

For limitation 1[e] Petitioner argues that Hiraishi teaches a first data buffer (data register buffer 300) that is coupled to the first memory device (memory devices 200) and is configurable to perform the operations further recited in limitations 1[f] to 1[i] as further explained below. Pet. 34 (citing Ex. 1005 ¶¶ 45, 55–56, 84, 99, 103, Figs. 1, 7; Ex. 1003 ¶¶ 127–128).

b) Limitations 1[f] and 1[i]

Limitations 1[f] and 1[i] require that in response to one or more of the module control signals, the first data buffer is configurable to: 1[f] “delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;” 1[i] “wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.” Ex. 1001, 19:44–55. Petitioner relies on Hiraishi alone and, in the alternative, on the combination of Hiraishi and Butt as teaching these limitations.

With respect to Hiraishi alone, Petitioner argues that Hiraishi’s data register buffers (300) include delay circuit 372 and can delay the first read strobe (DQS signal at input 351) by about 90 degrees to generate a first delayed read strobe to the FIFO (Read) Circuit 302. Pet. 35 (citing Ex. 1005 ¶ 91, Fig. 5; Ex. 1003 ¶¶ 99–100). Petitioner argues that Hiraishi’s reference to delaying the DQS signal by *about* 90 degrees is to allow for fine timing adjustments to the DQS signals by read leveling circuit 323 through a read leveling operation. *Id.* at 40 (citing Ex. 1005 ¶¶ 90–91, 140, Fig. 13; Ex. 1003 ¶¶ 137–138). Petitioner argues that read leveling in Hiraishi

includes performing a read operation which means that the amount of delay applied to the strobe signal DQS by delay circuit 372 would be based at least on signals received by the data buffer 300 during read leveling. *Id.* at 42–43 (citing Ex. 1005 ¶¶ 28, 140; Ex. 1003 ¶¶ 142–143).

Alternatively, with respect to the combination of Hiraishi and Butt, Petitioner argues that Butt discloses a delay circuit 104 that can delay read strobe signal DQS that is used to read data signal DQ. Pet. 44 (citing Ex. 1029 ¶¶ 17–18, Fig. 3A; Ex. 1003 ¶ 145). Petitioner argues that Butt describes a method of “read training” that can establish optimum DQS settings by adjusting a delay of the read data strobe signal DQS. *Id.* at 45 (citing Ex. 1029 ¶¶ 33, 35, Fig. 3A; Ex. 1003 ¶¶ 145–147). The optimum DQS settings established during read training are then used during later read operations, which Petitioner argues would teach one of skill in the art that Butt delays the data strobe signal by a predetermined amount based on signals received during a previous operation (i.e. the dummy data and strobe signals received during read training). *Id.* at 47 (citing Ex. 1003 ¶¶ 148, 150).

Petitioner argues that it would be been obvious to apply Butt’s teachings to Hiraishi to set the delay for Hiraishi’s delay circuit 372 by read leveling circuit 323 based on signals received during a prior read leveling process. Pet. 47 (citing Ex. 1003 ¶¶ 149–150). Hiraishi calls for read leveling and Butt teaches the details for performing read leveling. *Id.* According to Petitioner, “Butt provides the motivation: to ‘enable[] a reliable data read operation for high speed applications.’”⁴ *Id.* (emphasis

⁴ Petitioner emphasizes, by underline, each instance of the names of the prior art references in its Petition. Unless otherwise noted, we omit these emphases in our quotations from the Petition.

omitted, alteration by Petitioner) (quoting Ex. 1029 ¶ 36). Petitioner also argues that a person of ordinary skill would have “had a reasonable expectation of success because the combination would be a simple application of known techniques to improve similar technology in a similar way, and Butt’s calibration process 200 would offer the same benefit for Hiraishi’s delay circuit 372 as for Butt.” *Id.* at 47–48 (emphasis omitted) (citing Ex. 1003 ¶¶ 149–150).

Patent Owner argues that Petitioner fails to establish that Hiraishi alone or with Butt discloses a read strobe that is delayed based on signals received by the data buffer during a previous operation. Prelim. Resp. 30–43. With respect to Hiraishi alone, Patent Owner argues that, contrary to Petitioner’s contentions, Hiraishi describes delaying the DQS signal by a fixed 90 degrees and that there is no teaching that Hiraishi’s delay circuit 372 performs any fine timing adjustments to the DQS signal by the read leveling circuit. *Id.* at 31–32. This is because, according to Patent Owner, the delay circuit 372 is not disclosed as connected to any circuitry capable of providing any input that could alter the amount of delay applied by the delay circuit 372 to the DQS signal. *Id.* at 32–33 (citing Ex. 2005 ¶ 81); *see also id.* at 37–42 (explaining that none of the four outputs from read leveling circuit are used to adjust the delay of DQS by the delay circuit 372). Patent Owner argues that the JEDEC DDR standard allows for a delay tolerance which varies as a function of memory speed and that “Hiraishi’s reference to ‘about 90 degrees’ is meant to reflect the imprecise nature of adding fixed amounts of delay to a DQS signal.” *Id.* at 35 (citing Ex. 2005 ¶¶ 85–86; Ex. 2002, 81; Ex. 1019, 184–186; Ex. 1005 ¶ 91).

Addressing the combination of Hiraishi and Butt, Patent Owner argues that Butt cannot cure Hiraishi’s deficiency because Hiraishi’s read

leveling circuit is neither physically nor functionally connected to the delay circuit (as explained above) and the proposed combination with Butt does not change the manner in which the delay circuit is connected. Prelim. Resp. 43.

Patent Owner also argues that Petitioner fails to establish a motivation to combine Hiraishi with Butt. Prelim. Resp. 47–54. Specifically, Patent Owner argues Butt’s approach for performing read leveling would render Hiraishi incapable of performing read leveling because Butt’s read leveling approach requires DQ read data from the memory device but there is no evidence how Hiraishi’s buffer could provide DQ read data from the memory to its leveling circuitry. *Id.* According to Patent Owner, the only input to delay circuit 372 is the DQS on terminal 351 or 352, and the only input to data register control circuit 320 is the DRC, and, thus, neither the delay circuit 372 nor data register control circuit 320 have access to the DQ read data. *Id.* at 51–52 (citing Ex. 2005 ¶¶ 100–101).

Patent Owner also argues that even if Hiraishi’s read leveling could be replaced by Butt’s strobe delay adjustment, one of ordinary skill would not have been motivated to do so. Prelim. Resp. 54–56. Petitioner relies on Butt’s statement that its method would “enable[] a reliable data read operation for high speed applications.” Ex. 1029 ¶ 36, *quoted in* Pet. 47. But according to Patent Owner, “Hiraishi already claims ‘to realize a considerably high data transfer rate.’” *Id.* at 54 (citing Ex. 1005 ¶¶ 11, 69–70). Patent Owner argues “Petitioner does not explain or even suggest that the read leveling operation of Butt could make the read leveling operation in Hiraishi more reliable or otherwise better.” *Id.*

At this stage of the proceeding, we determine Petitioner has established a reasonable likelihood that one of ordinary skill would have

combined Hiraishi and Butt in the manner proposed by Petitioner and that this combination teaches the limitations 1[f] and 1[i]. Petitioner supports its contentions with evidence from the relied upon references and from the testimony of Dr. Wedig as summarized above. Specifically, we are persuaded that the combination of Hiraishi and Butt teaches delaying a first read strobe by a first predetermined amount based on signals received in a previous operation. Hiraishi teaches a delay circuit 372 that delays data strobe signals, and Butt explicitly teaches “adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window” based on previously performed read training. Ex. 1005, ¶ 91, Fig. 5; Ex. 1029 ¶¶ 33–35.

We are also persuaded by Petitioner’s arguments that there would be sufficient motivation to combine Hiraishi and Butt. Butt expressly states, in this regard, that its “invention generally enables a reliable data read operation for high speed applications.” Ex. 1029 ¶ 36. Additionally, Dr. Wedig provides credible testimony that it would have been obvious to combine Hiraishi and Butt. Ex. 1003 ¶ 149. Specifically, Dr. Wedig testifies that a person of ordinary skill “would have recognized that the calibration provided by the read training in Butt would facilitate more accurate and rapid exchanges of data by centering the data strobe signal in a valid data eye.” *Id.* (emphasis omitted).

Although Patent Owner argues that the combination would not successfully delay the read strobe signal based on previous operations due to Hiraishi’s read leveling circuit not being connected to its delay circuit and due to the combination not providing DQ read data to delay circuit 372, at this stage of the proceeding we credit Dr. Wedig’s testimony that a person of ordinary skill would have had a reasonable expectation of success in making

the combination. *Id.* For example, Dr. Wedig testifies that one of ordinary skill in the art would have been able to implement Butt's functionality in Hiraishi's delay circuit 372 and that doing so would be a simple application of known techniques to improve similar technology because Hiraishi's delay circuit 372 serves a function that is analogous to Butt's function of delaying the data strobe signal. *Id.*

c) Limitations 1[g] and 1[h]

Limitation 1[g] and 1[h] require the first data buffer is configurable to "sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus." Ex. 1001, 19:49–52. Regarding limitation 1[g], Petitioner argues that the first data buffer is configurable to sample the first section of the read data using the first delayed read strobe. Pet. 36–38. Petitioner argues that one of ordinary skill would have understood that, "when the data signal is latched in the FIFO, it necessarily is sampled (registered) and, because the delayed DQS signal acts 'as an input trigger signal' to latch the data in the FIFO (Read) circuit 302, this is necessarily done in accordance with the delayed strobe signal received from delay circuit 372." Pet. 37 (citing Ex. 1003 ¶ 132; Ex. 1005 ¶ 91).

Petitioner argues, in the alternative, that if Hiraishi alone does not teach limitation 1[g], as explained above, then the combination of Hiraishi and Butt does. Pet. 37–38. According to Petitioner, Butt discloses a method for calibrating a delayed read strobe DQS such that "data is sampled using the delayed read data strobe signals DQS." *Id.* at 37 (citing Ex. 1029 ¶¶ 18, 35). Petitioner argues that Butt's sampling operation is equivalent to Hiraishi's use of the DQS signal to trigger the FIFO Read circuit 302. *Id.* at 37–38 (citing Ex. 1029 ¶ 19).

For limitation 1[h] Petitioner argues Hiraishi's data buffer transmits the first section of the read data DQ on data line L0 via terminal 340 to a first section of the data bus line 23. Pet. 38 (citing Ex. 1003 ¶¶ 134–135).

As to limitation 1[g] Patent Owner argues Petitioner has failed to establish Hiraishi alone samples read data using the delayed read strobe. Prelim. Resp. 43–47. Patent Owner argues that Hiraishi never mentions sampling read data using the delayed strobe provided by delay circuit 372. *Id.* at 43. Patent Owner takes issue with Petitioner's argument that when data is latched in the FIFO, it necessarily is sampled because Petitioner does not articulate any basis for this assertion or provide supporting citations. *Id.* at 44–45.

Patent Owner argues that the combination of Hiraishi and Butt also does not teach limitation 1[g]. This is because Butt is incompatible with Hiraishi. Prelim. Resp. 46. As Patent Owner explains, Butt discloses that the data is sampled before it is presented to the output FIFO while the alleged sampling in Hiraishi is performed during or after the data is presented to Hiraishi's FIFO Read circuit. *Id.* at 46 (citing Ex. 1029 ¶ 18). Thus, Patent Owner argues “incorporating Butt's method in Hiraishi would not arrive at the invention, or even an operable implementation, because Hiraishi does not have any circuitry that can sample data *before* FIFO 302, as required by Butt's method, and Petitioner has not explained how that could be done.” *Id.* at 46.

Finally, Patent Owner argues Petitioner fails to present a *prima facie* case that a person of ordinary skill would have been motivated to modify Hiraishi with Butt's alleged sampling feature. Prelim. Resp. 56–58. Patent Owner points out that “[t]he only motivation provided is that ‘[t]he operation Butt describes as ‘sampling’ is *equivalent* to Hiraishi's use of the DQS

signal to trigger the FIFO (Read) circuit 302.” *Id.* at 57 (alteration in original) (citing Pet. 37–38). However, according to Patent Owner, Petitioner does not explain why a person of ordinary skill would regard Butt’s sampling as superior or preferable to Hiraishi’s existing approach. *Id.* at 57.

At this stage of the proceeding, we determine Petitioner has established a reasonable likelihood that one of ordinary skill would have combined Hiraishi and Butt in the manner proposed by Petitioner and that this combination teaches the limitations 1[g] and 1[h]. Petitioner supports its contentions with evidence from the relied upon references and from the testimony of Dr. Wedig as summarized above. Specifically, we are persuaded that the combination of Hiraishi and Butt teaches sampling the first section of the read data using the first delayed read strobe. Butt expressly teaches that “[e]ach of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO . . . after the data is sampled using the delayed read data strobe signals DQS.” Ex. 1029 ¶ 18. We also agree with Petitioner’s contention that Hiraishi transmits the first section of read data using the first delayed read strobe. *See* Ex. 1005, Fig. 5; Ex. 1003 ¶¶ 134–135.

As to Patent Owner’s argument that Butt is incompatible with Hiraishi because in Butt the data is sampled before it is presented to the FIFO while in Hiraishi the data is sampled during or after the data is presented to Hiraishi’s FIFO Read circuit, at this stage of the proceeding we determine that the one of ordinary skill in the art would have understood how to make the combination with a reasonable expectation of success, as supported by Dr. Wedig’s testimony. *See* Ex. 1003 ¶¶ 133, 149. We are also persuaded by Petitioner’s argument that one of ordinary skill would have been

sufficiently motivated to combine Butt with Hiraishi because Butt describes a method that enables a reliable data read operation for high speed applications. Ex. 1029 ¶ 36.

d) Conclusion as to Claim 1

For the aforementioned reasons we are persuaded that the combination of the Hiraishi and Butt teaches the limitations of claim 1 and that Petitioner has established a reasonable likelihood that the combination would have rendered claim 1 obvious.

4. Analysis of Claims 2, 4, 6, 7, 11, 13–15, 17, and 18

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that claims 2, 4, 6, 7, 11, 13–15, 17, and 18 would have been obvious over the combination of Hiraishi and Butt. *See* Pet. 48–68. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

5. Conclusion – Obviousness over Hiraishi and Butt (Ground 1)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent as obvious over Hiraishi and Butt.

E. Obviousness over Hiraishi, Butt, and Tokuhiro (Ground 4)

Petitioner argues claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent would have been obvious over Hiraishi, Butt, and Tokuhiro. Pet. 93–125. Below we provide a brief overview of Tokuhiro and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Tokuhiro (Ex. 1006)

Tokuhiro relates to a memory control circuit having “a write leveling function and control[ing] read/write operations by supplying a clock signal to a plurality of memories.” Ex. 1006, 3:16–20. Tokuhiro explains that, in memory interfaces, “a propagation delay is generated” because a “clock signal CK output from [a] memory controller 90 cannot reach all the [memory units] at the same time.” *Id.* at 1:63–2:1. Tokuhiro further explains that delay is addressed through a write leveling function for “adjusting (compensating) a delay time” of “data strobe signal DQS.” *Id.* at 2:10–18. For its write level technique, Tokuhiro describes “delaying, in [a] write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time.” *Id.* at 3:16–26.

In one example, “during the write operation, [a] first variable delay circuit DW delays the data strobe signal DQS output to the SDRAM by the first delay time Dt1 that has been set based on the write leveling function.” Ex. 1006, 14:66–15:2. Tokuhiro explains that a “delay time . . . calculated is provided as Delay (R)n. In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling.” *Id.* at 16:19–23; *see id.* 16:1–18.

2. Petitioner’s Proposed Combination and Reasons to Combine

Petitioner relies on Tokuhiro for its ability to delay transmission of read data based on a delay time determined during a write operation. Pet. 94. Petitioner proposes to implement the functionality of the delay

elements (DR) of Tokuhiko in the data buffers of Hiraishi. *Id.* at 103–111. Specifically, Petitioner proposes to add Tokuhiko’s read delay elements (e.g. DR-1) to Hiraishi’s data register buffer immediately after the read data from the memory is latched in Hiraishi’s FIFO Read Circuit 302. *Id.* at 107–109. Alternatively, Petitioner argues that Tokuhiko’s delay elements could be used instead of Hiraishi’s FIFO circuit for delaying read data. *Id.* at 110. Petitioner presents two different implementations of the Hiraishi, Butt, and Tokuhiko combination. The first being where the system memory controller determines the read delay. *Id.* at 112–113. The second is where the module controller determines the read delay. *Id.* at 114–119.

Petitioner provides three motivations to combine Tokuhiko with Hiraishi, including that (1) Tokuhiko teaches calculating read delays based on the delays for write operations, which is more efficient than Hiraishi’s technique of performing read leveling independent of write delays; (2) Tokuhiko provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays; and (3) Tokuhiko discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not. Pet. 95–103.

Patent Owner argues that although Petitioner relies on the combination of Hiraishi, Butt, and Tokuhiko, “each of the alleged motivations to combine . . . is directed to a proposed modification of only an *unmodified* Hiraishi with Tokuhiko, not to a proposed *further* modification of a Hiraishi-Butt combination with Tokuhiko.” Prelim. Resp. 59.

Patent Owner further argues that Petitioner does not explain how adding Tokuhiko’s delay element DR-1 reconciles with the delayed strobe provided by the delay circuit 372 which, Patent Owner argues, is delayed by

a significant 90-degrees. Prelim. Resp. 62. Patent Owner argues that Petitioner's combination cannot account for the delay introduced by delay circuit 372 because the delay from this circuit is not an input to Tokuhiro's DR-1 delay element in Petitioner's proposed combination. *Id.* at 62–63.

Patent Owner argues, with respect to Petitioner's first implementation in which the system memory controller determines the read delay (Pet. 112–113), that a person of ordinary skill in the art would not have implemented Hiraishi's S5 leveling operations to program the read delay elements added from Tokuhiro to Hiraishi's data buffer. Prelim. Resp. 64–68. This is because Hiraishi's S5 leveling accounts only for delays between the system memory controller and the data buffers, not between the data buffers and the memory devices, the latter of which, Patent Owner argues, is what the claims of the '506 patent are directed to. *Id.* at 66–67. Patent Owner also argues that Petitioner fails to establish that the first implementation would be operable because Tokuhiro's read and write leveling are performed by the computer's main CPU, not its memory controller. *Id.* at 68. According to Patent Owner, in Tokuhiro, the delay elements are connected over dedicated CPU control lines on which control signals are provided, whereas in Petitioner's proposed combination, the only inputs to delay element DR-1 are the DQS signal and the local clock signal and no evidence has been presented that the components can be modified to operate in the proposed combination. *Id.* at 71–72.

With respect to the second implementation, Patent Owner argues that Petitioner failed to identify what component in Hiraishi the module controller is and that, because of this, it is impossible to discern what the basis for Petitioner's second implementation is. Prelim. Resp. 77–78. Further, Patent Owner argues that the Petition does not identify any passage

of Hiraishi that suggests that the functionality of its memory controller can be implemented by its data register buffers, as contended by Petitioner. *Id.* at 79. Moreover, according to Patent Owner, the functionality relied on by Petitioner is implemented by Tokuhiro's main CPU, not the memory controller and thus Petitioner's motivation for the second implementation fails. *Id.* at 79–80. Finally, Patent Owner argues that although the second implementation relies on Hiraishi's time measurement technique to measure time intervals to determine the corresponding fly-by-delay, what the Petition describes is the idea of determining the time delay between the memory controller and the data register buffer, not between the data register buffer and the memory devices. *Id.* at 80.

At this stage of the proceeding, we determine Petitioner has provided a sufficient reason to combine Hiraishi, Butt, and Tokuhiro. For example, Petitioner argues that Tokuhiro's method of calculating read delays based on the delays for write operations is more efficient than Hiraishi's technique of performing read leveling independent of write delays. Pet. 95–99 (citing Ex. 1003 ¶¶ 279–288). Petitioner also argues Tokuhiro provides techniques to remove fly-by delay while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays. Pet. 100 (citing Ex. 1003 ¶¶ 289–292). Petitioner argues that Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not. Pet. 101–103 (citing Ex. 1003 ¶¶ 293–299). Petitioner supports its contentions with credible testimony from Dr. Wedig who testifies that performing the write and read leveling operations of Hiraishi would require circuitry in both the data register buffer and the memory controller but that this circuitry could be simplified by implementing Tokuhiro's technique of setting read delays based on write delays. Ex. 1003 ¶¶ 283–288. Dr. Wedig

also testifies that Tokuhiro teaches that problems arise if fly-by delays on read operations are not compensated, especially if such delays exceed the clock period, and also teaches solutions to this problem. Ex. 1003

¶¶ 293–299.

As summarized above, Patent Owner makes various arguments why one of ordinary skill would not have been motivated to combine Tokuhiro with Hiraishi and why the proposed combination would not have been operable or would have required further modification that Petitioner has not described. At this stage of the proceeding we determine Petitioner has presented sufficient evidence and reasoning supporting its proposed combination and explaining why one of ordinary skill in the art would have combined the references in the manner proposed. For example, Dr. Wedig testifies that it would have been obvious to implement Tokuhiro's delay elements in Hiraishi's data register buffers in the manner described by Petitioner, for example by applying the read delay immediately after the read data from the memory is latched. Ex. 1003 ¶¶ 300–321. Dr. Wedig also testifies that when Tokuhiro's read delay elements are added to Hiraishi's data buffer, existing delay circuit 372 would still continue to make fine timing adjustments to the phase of the strobe DQS. *Id.* ¶ 304. This testimony supports Petitioner's arguments that one of ordinary skill would have had a reasonable expectation of success in making the combination. While Patent Owner presents multiple arguments to the contrary, with support from the testimony of Dr. Khatri, we determine that the weight of Petitioner's evidence is sufficient at this stage of the proceeding.

3. Analysis of Claim 1

Petitioner relies on the same contentions made in Ground 1, over Hiraishi and Butt, for all limitations of claim 1 except limitations 1[f] and

1[i]. Pet. 119–120. Our analysis of Ground 1 above, therefore, applies for those limitations where they are applicable and will not be repeated here.

As a reminder, limitations 1[f] and 1[i] require that in response to one or more of the module control signals, the first data buffer is configurable to: 1[f] “delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;” 1[i] “wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.” Ex. 1001, 19:44–55. Petitioner argues that Tokuhiro’s delay element DR-1 added to Hiraishi’s data buffer circuit would delay the strobe signal from selector 332 and provide that delayed strobe signal to the FIFO Read Circuit 302. Pet. 120 (citing Ex. 103 ¶ 323). The delay introduced by Tokuhiro’s DR-1 delay element for the read operation would be based on an earlier write operation, according to Petitioner. *Id.* at 121–122 (citing Ex. 1006, 18:53–63, 2:13–18).

At this stage of the proceeding we are persuaded by Petitioner’s arguments which we determine are supported by disclosures from Hiraishi, Butt, and Tokuhiro and by Dr. Wedig’s testimony. Patent Owner does not make separate arguments, in addition to those discussed above, regarding these limitations.

a) Conclusion as to Claim 1

For the aforementioned reasons, we are persuaded that the combination of Hiraishi, Butt, and Tokuhiro teaches the limitations of claim 1 and that Petitioner has established a reasonable likelihood that the combination would have rendered claim 1 obvious.

4. Claims 2, 4, 6, 7, 11, 13–15, 17, and 18

Based on a review of the current record at this stage of the proceeding Petitioner has made a sufficient showing of a reasonable likelihood that

claims 2, 4, 6, 7, 11, 13–15, 17, and 18 would have been obvious over the combination of Hiraishi and Butt. *See* Pet. 122–125. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

5. *Conclusion – Obviousness over Hiraishi, Butt, and Tokuhiro (Ground 4)*

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent as obvious over Hiraishi, Butt, and Tokuhiro.

F. *Obviousness over Hiraishi, Butt, and Ellsberry (Ground 2); Obviousness over Hiraishi, Butt, and Kim (Ground 3); Obviousness over Hiraishi, Butt, Tokuhiro, and Ellsberry (Ground 5); Obviousness over Hiraishi, Butt, Tokuhiro, and Kim (Ground 6)*

Petitioner argues that claims 3, 5, 12, and 16 of the '506 patent would have been obvious over Hiraishi, Butt, and Ellsberry (Pet. 68–78); that claims 8–10, 19, and 20 of the '506 patent would have been obvious over Hiraishi, Butt, and Kim (*id.* at 79–93); that claims 3, 5, 12, and 16 of the '506 patent would have been obvious over Hiraishi, Butt, Tokuhiro, and Ellsberry (*id.* at 126–127); and that claims 8–10, 19, and 20 of the '506 patent would have been obvious over Hiraishi, Butt, Tokuhiro, and Kim (*id.* at 127).

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that the challenged claims under the aforementioned grounds would have obvious over the respective references. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

III. CONCLUSION

Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one challenged claim of the '506 patent. At this stage of the proceeding, however, we have not made a final determination with respect to the patentability of the challenged claims.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–20 of the '506 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '506 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2022-00711
Patent 10,860,506 B2

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