JEDEC STANDARD

DDR4 Data Buffer Definition (DDR4DB02)

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DDR4 DATA BUFFER DEFINITION

(From JEDEC Board Ballot, JCB-17-01, formulated under the cognizance of the JC-40.4 Subcommittee on Registered and Fully Buffered Memory Support Logic.)

1 Scope

This standard defines standard specifications for features and functionality, DC & AC interface parameters and test loading for definition of the DDR4 data buffer for driving DQ and DQS nets on DDR4 LRDIMM applications.

The purpose is to provide a standard for the DDR4DB02 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR4DB02 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

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2 Device standard

2.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V V_{DD} operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are V_{DD} terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR4DB02 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers. The buffer control word (BCW) mechanism is described in more detail in Section 2.5.

The DDR4DB02 also supports dedicated pins for ZQ calibration and for parity error alerts.

2.2 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of 200 µS in the RESET state (i.e. the BCK_t/BCK_c inputs are held LOW and the BCKE input is held HIGH). In the RESET state all other input receivers are disabled, and can be left floating. In the RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All outputs must float. In the RESET state the data buffer is in low power state and host interface or DRAM interface termination is disabled.

With a falling edge of the BCKE input, the data buffer transitions to the clock stopped power down mode. A certain period of time (t_{ACT}=16 t_{CK}) before the BCKE input is pulled LOW the reference voltage BVrefCA needs to be stable within specification.

With stable clock input signals BCK_t/BCK_c and BCKE still held LOW, the buffer transitions into the equivalent of CKE power down mode.

2.2.1 Clock Stabilization Time t_{DLLK}

During DLL stabilization time t_{DLLK} the data buffer is not fully operational. In ensure correct operation, some rules apply to the inputs of the buffer:

- BCKE must remain LOW.
- BODT is kept at a stable valid logic level.

These rules apply to any instance where stabilization time t_{DLLK} is required:

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- Exit from Reset state
- Exit from clock stop power down
- Changing clocking related registers
- Changing input clock frequency during boot or run time

Since the data buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the DLL stabilization time (t_{DLLK}) the DB must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs.

2.3 Reset Initialization with Stable Power

The timing diagram depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. The data buffer remains in the RESET state for a minimum of 16 * tCK (i.e. BCK_t/BCK_c are held LOW (i.e. below $V_{IL(static)}$) and BCKE input is held HIGH for that long).

After initialization, the host needs to write to those control registers in the RCD and DB whose contents need to be changed before it can proceed to the DRAM initialization.

2.4 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB02).

2.4.1 Control Bus Signals

Table 2 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Input clock	2
BVrefCA	Reference voltage for command and control signals	1
	Total	9

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2.4.2 Command List

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

2.4.3 Dedicated Signals

BCKE, BODT, and BCK_t/BCK_c are considered dedicated signals because they have direct control of certain commands and/or modes of operation. The following sections describe how the dedicated signals are used.

2.5 Data Buffer Power Down Modes

2.5.1 CKE Power Down with ODT enabled Entry

The data buffer enters into a power saving state when its BCKE input transitions from high to low if BC09 DA3 = 1. The DB enters CKE Power Down mode with ODT enabled if BC09 DA2 = 0. The event is captured by the data buffer device synchronously with the BCK_t/BCK_c input clock. In this power saving state, most input receivers and all output drivers in the data buffer are disabled. Similarly, any internal non-essential circuits can be powered down in this mode. The input receivers that need to remain enabled are BCK_t/BCK_c, BCKE and BODT. The data buffer device disables input receivers within tInDIS clocks after latching the BCKE inputs LOW. After tInDIS, the data buffer can tolerate floating inputs except for BCK_t/BCK_c, BODT and BCKE. Since the data buffer control signals will be terminated to V_{TT} in the DDR4 LR-DIMM board, the register device will need to disable all unused data buffer control output drivers to avoid wasting power when the data buffers are in the CKE Power Down state. It is required that data buffer clock signal (BCK_t/BCK_c) will continue toggling at a stable phase and frequency during CKE Power Down mode in order to allow the data buffer devices to remain locked to this clock.

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2.5.2 CKE Power Down with ODT disabled Entry

The data buffer enters into a power saving state when its BCKE input transitions from high to low if BC09 DA3 = 1. The DB enters CKE Power Down mode with ODT disabled if BC09 DA2 = 1.The event is captured by the data buffer device synchronously with the BCK_t/BCK_c input clock. In this power saving state, most input receivers and all output drivers in the data buffer are disabled. Similarly, any internal non-essential circuits can be powered down in this mode. The input receivers that need to remain enabled are BCK_t/BCK_c and BCKE. The BODT input receiver is disabled in this mode. The data buffer device disables input receivers within tInDIS clocks after latching the BCKE inputs LOW. After tInDIS, the data buffer can tolerate floating inputs except for BCK_t/BCK_c, and BCKE. Since the data buffer control signals will be terminated to V_{TT} in the DDR4 LR-DIMM board, the register device will need to disable all unused data buffer control output drivers to avoid wasting power when the data buffers are in the CKE Power Down state. It is required that data buffer clock signal (BCK_t/BCK_c) will continue toggling at a stable phase and frequency during CKE Power Down mode in order to allow the data buffer devices to remain locked to this clock.

2.5.3 CKE Power Down with ODT enabled Exit

When BCKE is driven from low to high by the register and the data buffer captures this event synchronously with the BCK_t/BCK_c input clock, the buffer exits its CKE Power Down mode. When BCKE is driven from LOW to HIGH by the register, it is required that valid logic levels are driven at all the data buffer inputs and that these levels be held constant for $t_{Fixedoutput}$ to allow input receivers to stabilize. During the $t_{Fixedoutput}$ window, it is required that the command driven to the data buffer is a NOP (BCOM[3:0] = 1010). After the input receivers are stabilized, the data buffer will start processing commands in its normal operation mode with the correct latency and timing.

2.5.4 CKE Power Down with ODT disabled Exit

When BCKE is driven from low to high by the register and the data buffer captures this event synchronously with the BCK_t/BCK_c input clock, the buffer exits its CKE Power Down mode. When BCKE is driven from LOW to HIGH by the register, it is required that valid logic levels are driven at all the data buffer inputs and that these levels be held constant for $t_{Fixedoutput}$ to allow input receivers to stabilize. During the $t_{Fixedoutput}$ window, it is required that the command driven to the data buffer is a NOP (BCOM[3:0] = 1010) and that the BODT signal is constantly driven LOW. After the input receivers are stabilized, the data buffer will start processing commands in its normal operation mode with the correct latency and timing. This also applies to BODT-controlled termination enable/disable events.

2.5.5 Clock Stopped Power Down Entry

To support ACPI S3 Power Management mode, the data buffer supports a Clock Stopped Power Down mode. When both inputs BCK_t and BCK_c are held at LOW (V_{IL} (static)) the data buffer device stops operation and enters low-power static and standby operation. The device will stop its internal clock circuits and it will float all outputs drivers and disable all input receivers.

To enter Clock Stopped Power Down mode, the device will first enter CKE Power Down mode. Once in CKE Power Down mode, BCKE will continue be driven to LOW, followed by BCK_t and BCK_c also driven LOW. The device is now in Clock Stopped Power Down mode. In this mode all input receivers and input termination of the data buffer will be disabled. The only input circuits that need to remain active are BCK_t/BCK_c and BCKE, which are required to detect the wake up request from the register or a RESET condition.

2.5.6 Clock Stopped Power Down Exit

To wake up the data buffer from its Clock Stopped Power Down mode, the data buffer BCKE input must continued to be driven LOW to ensure that the data buffer device goes into CKE Power Down mode immediately after exiting Clock Stopped Power Down mode. If Clock Stopped Power Down mode had been entered from CKE Power Down with the host ODT termination feature enabled, it is also necessary for BODT to be driven to LOW before the data buffer is taken out of Clock Stopped Power Down mode. After that, a frequency and phase accurate input clock signal must be applied. The state of the BCKE and BDODT input signals must not be changed before the end of the DLL

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stabilization time (tDLLK). If Clock Stopped Power Down mode had been entered from CKE Power Down with host ODT termination disabled, the host interface DQ termination is disabled until the end of tDLLK and from then on works with synchronous timing and deterministic latency. The input clock BCK_t and BCK_c must be stable for a time equal or greater than tDLLK before any access to the data buffer can take place. During DLL stabilization time the BCKE signal need to be kept at LOW level.

2.6 Data Buffer Termination

2.6.1 Host Interface ODT Termination

The DDR4DB02 supports DQ bus termination in LRDIMM applications by providing the BODT input connected to the DDR4RCD02.

Unless BODT is turned off in RCD F0RC8x bits DA[5] or DA[7], BODT is the logical OR of the RCD DODT0 and DODT1 inputs, i.e. if one or both of these inputs is asserted HIGH, the RCD BODT output is asserted HIGH.

When BODT is enabled, the host controls enabling RTT_NOM on the host interface of the data buffer through assertion of the DODT signals, which are OR'ed by the RCD, which in turn asserts BODT HIGH or LOW to the data buffer. The enabling/disabling of the on-die termination at the DRAM interface of the data buffer is independent from the BODT input control signal.

The timing for enabling RTT_NOM on the host interface in response to BODT being captured HIGH is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the BODT signal assertion than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

It is the responsibility of the host to assert the DODT signal to the RCD early enough to ensure that the host interface termination is active prior to start of the read preamble at the host interface. The duration of the data buffer's RTT_NOM termination is controlled by the host through the length of the DODT pulse.

Since the data buffer can either drive data or terminate (but not both at the same time), the data buffer disables RTT_NOM at the host interface for reads targeted to this DIMM during the duration of the read burst (including the Read Preamble).

The timing for enabling RTT_WR on the host interface in response to a WRITE command being captured on the BCOM inputs is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the WRITE command capture than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

Figure 1 shows the host interface ODT timing based on the assertion of the input signal BODT. The DDR4DB02 parameters ODTLon, ODTLoff, ODTLcnw, ODTLcwn and tADC are defined in the Electrical and Timing chapter. For simplicity this diagram shows ODT timings always aligned with rising clock edges but due to the existence of the

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fractional cycle delays DB_WL(R) and tPDM_WR or tPDM_WR_RA, this is typically not the case.

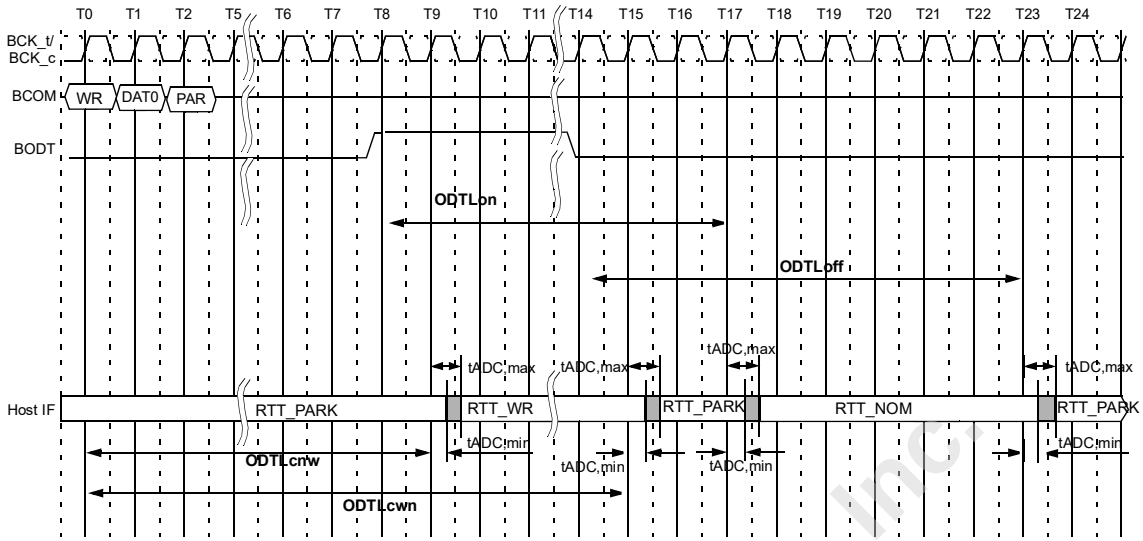

Figure 1 — Host Interface ODT Timing

DB_WL(R) = CWL + AL + PL + DWL(R)
ODTLon = DB_WL(R[1]) - tPDM_WR - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 0)
= DB_WL(R[1]) - tPDM_WR_RA - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 1)
ODTLoff = ODTLon
ODTLcnw = DB_WL(R) - tPDM_WR - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 0)
= DB_WL(R) - tPDM_WR_RA - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 1)
ODTLcwn = ODTLcnw + tWPRE + BL/2 +1; where tWPRE = 1 or 2 and BL = 4, 8 or 10 with CRC enabled

Unless DDR4RCD02 F0RC8x bit DA[7] = '1', the host also controls the QxODT signals at the DRAM interface directly through the assertion of the two DODT signals at the host interface. The host may utilize non-target termination to a rank on the same DIMM other than the target rank for read transactions. The host may also utilize non-target termination to a rank on the same DIMM other than the target rank for write transactions.

2.6.2 DRAM Interface ODT Termination

The timing for enabling disabling the on-die termination circuits at the DRAM interface of the DDR4 data buffer is independent from the BODT input control signal. Instead, the hardware in the data buffer will enable the DRAM interface termination within the clock cycle preceding the MDQS preamble during data transactions resulting from DRAM Read commands. This timing is controlled by the DB hardware using the trained DRAM interface receive enable control word settings stored in F[3:0]BC2x and F[3:0]BC3x.

2.7 Dual Frequency Support

The DDR4DB02 supports operation at a second, i.e. lower than nominal, frequency as a means to save RCD/DB and DRAM power when the memory bandwidth demand allows.

1.RTT_NOM termination without a coinciding DDR4DB02 data movement (e.g. WR) uses Rank 0 timing while RTT_NOM termination with a coinciding data movement will use the timing of the target rank, which implies that the data buffer can dynamically switch between different rank timings from one access to the next.

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To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR4DB02 can be trained twice at two different frequencies at boot up time and retain register settings associated with each of the two frequencies. See section 4.12 for a complete list of control words that are duplicated to support dual frequency context switching. The DDR4DB02 hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed.

Switching between the two frequency contexts is achieved by writing to control word BC0A bit DA3. DA3='0' selects the default frequency context 1 while DA3='1' selects frequency context 2.

Dual frequency training at boot up time requires selecting the appropriate frequency context, performing the training at that frequency and then selecting the other frequency context and performing the training at the other frequency. Subsequently, every time the operation frequency changes, the corresponding frequency context bit must be set in the DDR4DB02 via control word writes to BC0A and F0BC6x. The control word write to BC0A/F0BC6x must be the last access to the DB before the input frequency on the BCK_t/BCK_c pins changes. See section 2.7.1 for the exact sequence of steps for an input frequency change to an LRDIMM.

2.7.1 Input Clock Frequency Change

Once the DDR4DB02 is initialized, the DDR4DB02 requires the clock to be "stable" during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Clock stop power down mode. DDR4 DB02 allows two possible sequences (Sequence A and Sequence B) for input clock frequency change for the DDR4RCD02 and DDR4DB02.

The complete sequence of input clock frequency change for the DDR4RCD02 and DDR4DB02 is as follows:

Sequence A:

1. Disable CKE power down mode in RCD (i.e. write to F0RC09, bit 3 = '0').
2. Ensure CKE power down mode in DB is enabled (i.e. BC09, bit 3 ' 1').
3. Send new BC0A and F0BC6x frequency setting to DB. The DB will defer the application until the next rising edge of BCKE.
4. Put the DRAMs into Self Refresh by sending SRE commands to all ranks. After this step all DCKE inputs will be LOW but the RCD will stay active. The DB will enter CKE power down mode.
5. Send new F0RC0A and F0RC3x frequency setting to RCD without asserting CKE. The control word writes will proceed because RCD is still active. DRAMs are still in Self Refresh. No additional commands to the RCD are allowed after this step (until step 8).
6. Host changes frequency by going through Clock Stopped mode. Both CK inputs need to be driven LOW (i.e. below $V_{IL(static)}$) for a minimum of t_{CKEV} before the clock frequency may change. The DDR4DB02 input clock frequency is allowed to change only within range between the minimum and maximum application or test frequencies specified in Table 135.
7. The DCKE inputs must be held at stable LOW levels during t_{CKEV} and during the t_{STAB} time after the clock signals are restarted.
8. Assert DCKE and exit DRAM Self Refresh.
9. Wait tDLLK for DB clocks to stabilize.

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10. Depending on the new clock frequency, additional MRS commands to the DRAM may need to be issued to appropriately set CL, AL, and CWL with BCKE continuously registered high. RCD CKE power down mode may be re-enabled.

Sequence B:

1. Ensure CKE power down mode in DB is enabled (i.e. BC09, bit 3 = 1).
2. Send new BC0A and F0BC6x frequency setting to DB. The DB will defer the application until next rising edge of BCKE.
3. Send new RC0A and F0RC3x frequency setting to RCD. The RCD ensures application of the new setting at or prior to next rising edge of DCKE.
4. Put the DRAM into Self Refresh by sending SRE commands to all ranks. After this step all DCKE inputs will be LOW. The DB will enter CKE power down mode.
5. Host changes frequency by going through Clock Stopped mode. Both CK inputs need to be driven LOW (i.e. below VIL(static) for a minimum of tCKEV before the clock frequency may change. The DDR4 RCD02 input clock frequency is allowed to change only within range between the minimum and maximum application or test frequencies specified in Table 135.
6. The DCKE inputs must be held at stable LOW levels during tCKEV and during tSTAB time after the clock signals are restarted.
7. Assert CKE and exit DRAM Self Refresh.
8. Wait tDLLK for DB clocks to stabilize.
9. Depending on the new clock frequency, additional MRS commands to the DRAM may need to be issued to appropriately set CL, AL, and CWL with BCKE continuously registered high.

2.8 Command Sequences

With the exception of the NOP command, all commands require more than one clock cycle in order to send additional information needed by the buffer in the execution of the command. We call this succession of command and its corresponding data transfers a command sequence. The command sequence for Read or Write commands requires two additional cycles to transfer the rank number corresponding to the write or read command, the sequence for MRS Writes requires seven clock cycles in addition to the basic command, the sequence for the BCW Write command uses six additional clock cycles and the BCW Read command uses five additional clock cycles.

2.9 Parity Checking

Command sequences are protected by a parity checking scheme. Parity checking on the command bus signals is disabled by default, and it is necessary to enable parity checking by writing a buffer configuration bit by using a BCW instruction. The RCD always generates the parity cycles in the BCOM command sequences. Parity checking only applies to the BCOM[3:0] signals. The convention of parity is even parity, i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. . The parity bit is transmitted for each BCOM[3:0] signal in the corresponding BCOM[3:0] line during the last transfer (clock cycle) in the command sequence.

2.10 Command Sequence Error Detection

In order to keep the command bus from getting stuck in an out-of-sync situation in terms of the handling of command versus data transfers, a protection scheme is necessary.

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To implement the command sequence protection scheme, one of the command pins of the bus will be dedicated as a flag to identify the type of transfer. BCOM[3] will be used to indicate if the transfer is a command transfer (BCOM[3] = 1) or a data transfer (BCOM[3] = 0). There is only one exception where BCOM[3] looses this special meaning. That is during the cycles when the four-bit command parity word is transferred from the register to the buffers.

The data buffer will check the value of BCOM[3] every clock cycle, with the exception of parity transfers (PAR[3:0]), and it will detect any errors in the command sequences. An error in the command sequence occurs if any of the following cases is detected.

1. The buffer receives a command transfer (BCOM[3] = 1) when expecting to receive a data transfer (BCOM[3] = 0).
2. The buffer receives a data transfer (BCOM[3] = 0) when expecting to receive a command transfer (BCOM[3] = 1).

2.11 Error Handling

When a BCOM parity error is detected, the data buffer will take the following actions.

1. The data buffer logs all the bits of the erroneous command in the Error Log Register (F7BC0x .. F7BC3x) if there is no previous (parity or command sequence) error already logged in these registers and sets the parity error bit to '1'.
2. BCOM parity checking will be disabled.
3. If the parity error is detected during a configuration command (BCW Write or MRS Write), the state of the buffer configuration bits will not be modified. In other words, the configuration command will not be executed.
4. All scheduled RD/WR commands that have not yet executed are dropped
5. The data buffer will assert the ALERT_n output pin LOW for tPAR_ALERT_PW clock cycles in a similar way as the DDR4 DRAM responds to CA parity errors. If an error occurs ALERT_n is driven LOW with the third input clock edge after the corresponding incorrect data were captured on the data buffer command inputs. If BC0E DA2='1', ALERT_n goes to high impedance with the tPAR_ALERT_PW+3 input clock cycle after the parity error was detected. If BC0E DA2='0', ALERT_n continues to be driven LOW until a 'Clear Error Status' command is received. During ALERT_n assertion, RD and WR commands are ignored.
6. The 'Clear Error Status' command will re-enable BCOM parity checking. If the ALERT_n re-enable bit in BC0E is set, BCOM parity checking will be re-enabled after the expiration of the ALERT_n pulse.

When a command sequence error is detected, the data buffer will take the following actions.

1. The data buffer logs all the bits of the erroneous command in the Error Log Register (F7BC0x .. F7BC3x) if there is no previous (parity or command sequence) error already logged in these registers and sets the sequence error bit to '1'.
2. Command Sequence error checking and parity error checking will be disabled.
3. If the sequence error is detected during a configuration command (BCW Write or MRS Write), the state of the buffer configuration bits will not be modified. In other words, the configuration command will not be executed.
4. All scheduled RD/WR commands that have not yet executed are dropped
5. The data buffer will assert the ALERT_n output pin LOW for tSEQ_ALERT_PW clock cycles in a similar way as the DDR4 DRAM responds to CA parity errors. If an error occurs ALERT_n is driven LOW with the third input clock edge after the corresponding incorrect data were captured on the data buffer command inputs. If BC0E DA2='1', ALERT_n goes to high impedance with the tSEQ_ALERT_PW+3 input clock cycle after the protocol violation was detected. If BC0E DA2='0', ALERT_n continues to be driven LOW until a 'Clear Error Status' command is received. During the ALERT_n pulse, RD and WR commands are ignored.

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6. The 'Clear Error Status' command will re-enable command sequence error checking. If the ALERT_n re-enable bit in BC0E is set, sequence error checking will be re-enabled after the expiration of the ALERT_n pulse.

2.12 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

DB_WL(R)[1] = CWL + AL + PL + DWL(R)

DB_RL(R)[2] = CL + AL + PL + MRE(R) + tRPRE/2

The equations for DWL and MRE for Ranks 0 to 3 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * tCK/64

DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * tCK/64

DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * tCK/64

DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * tCK/64

DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * tCK/64

DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * tCK/64

DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * tCK/64

DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * tCK/64

MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * tCK/64

MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * tCK/64

MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * tCK/64

MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * tCK/64

MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * tCK/64

1.This equation assumes that the DDR4DB02 MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.
2.This equation assumes that the DDR4DB02 MDQS Read Delay Control Words in F[3:0]BC4x/F[3:0]BC5x are at their default power-on setting.

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MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * tCK/64

MRE[2].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * tCK/64

MRE[2].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * tCK/64

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4DB02 for all ranks and nibbles.

Timing parameters that are integer multiples of tCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tCK are shown in *red italic* letters. Timing parameters for transparent mode are shown in plain green.

For simplicity the timing diagrams only show one of the possible host interface termination modes and RTT_PARK is never shown even though it is always supported.

2.13 Write Commands

Table 5 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or '10').

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

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Figure 2 shows the timing sequence for a Write command.

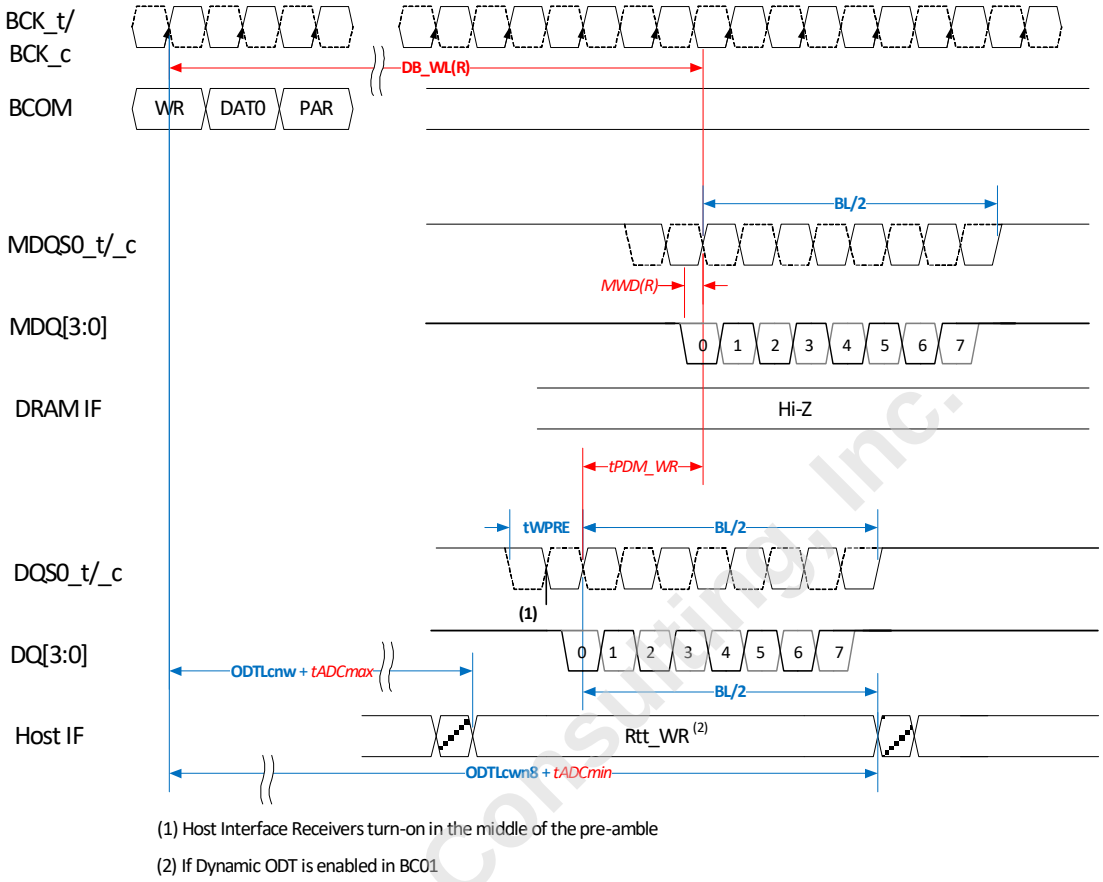

Figure 2 — WRITE Timing

2.14 Read Commands and MPR Override Reads

Table 5 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or

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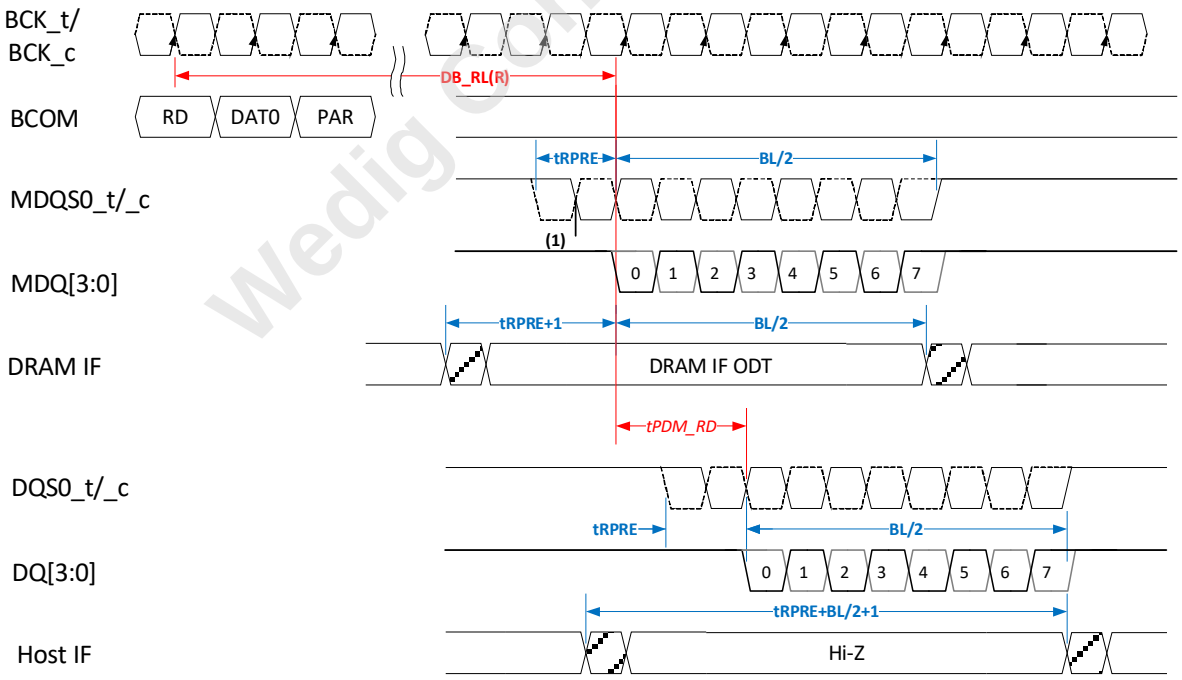
'10').

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

Figure 3 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

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Read commands can be used to access locations other than the memory array in the DDR4 DRAM devices. These special read commands are MPR override reads. The DDR4DB02 uses the Rank 0 output enable timing for these reads. By default, the only function of the data buffer during MPR reads and MRS reads is to simply forward the data received at the DRAM interface to the edge connector interface. In order to allow training of the data buffer to host segment separately from the data buffer to DRAM segment, the buffer can be configured in an override mode for MPR read commands. The override mode for MPR reads is enabled by a buffer control word, BCW, bit (F0BC1x, DA1). The power-on default values for MPR0 to MPR3 are the same as the power-on default values for the DRAM MPRs, see Table 73. When the MPR read override mode is enabled the buffer sends its own MPR data bits on the host interface instead of the data received from the DRAMs. The DB implements the equivalent of the writeable DRAM page 0 Multi Purpose Registers. The DDR4DB02 supports two modes in which MPR can be accessed for read. The two modes are serial return and parallel return. There is also an optional staggered return format described in Chapter 2.14.1, "Optional MPR Override Read Format for Staggered Returns," The following two tables illustrate the serial return and parallel return methods for MPR0 reads. Both nibbles of the DB drive identical information. In these examples the pattern programmed in the MPR0 (F5BC0x, DA[7:0]) is 0111 1111. Back to back accesses to MPR0 in serial or parallel modes return the same information.

Table 6 — MPR Override Read Format for Serial Return

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

Table 7 — MPR Override Read Format for Parallel Return

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

The DDR4DB02 supports MPR override reads using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR override reads. The DDR4DB02 supports MPR override read commands that are 4 tCK apart so that in BL8 mode a stream can be created on the data bus with no bubbles or clocks between read data.

2.14.1 Optional MPR Override Read Format for Staggered Returns

Table 8 illustrates the staggered return method. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. A read command to MPR0 will result in data being driven

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from MPR0 on DQ0, data from MPR1 on DQ1 and so forth as shown in the UI0-7 column below. For the return pattern shown in Table 8, the controller issues a 8-command sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3 resulting in a un-interrupted stream of 64UI.

Table 8 — MPR0,1,2,3,0,1,2,3 Override Read Format for Staggered Return

RD Command Staggered	MPR0 UI0-7	MPR1 UI8-15	MPR2 UI16-23	MPR3 UI24-31	MPR0 UI32-39	MPR1 UI40-47	MPR2 UI48-55	MPR3 UI56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ4	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ5	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ6	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ7	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

The DDR4DB02 can respond to back to back read commands starting with MPR1 as shown in Table 9.

Table 9 — MPR1,2,3,0,1,2,3,0 Override Read Format for Staggered Return

RD Command Staggered	MPR1 UI0-7	MPR2 UI8-15	MPR3 UI16-23	MPR0 UI24-31	MPR1 UI32-39	MPR2 UI40-47	MPR3 UI48-55	MPR0 UI56-63
DQ0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ4	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ5	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ6	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ7	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3

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The DDR4DB02 can respond to back to back read commands starting with MPR2 as shown in Table 10.

Table 10 — MPR2,3,0,1,2,3,0,1 Override Read Format for Staggered Return

RD Command Staggered	MPR2 UI0-7	MPR3 UI8-15	MPR0 UI16-23	MPR1 UI24-31	MPR2 UI32-39	MPR3 UI40-47	MPR0 UI48-55	MPR1 UI56-63
DQ0	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ1	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ2	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ3	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ4	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ5	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ6	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ7	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0

The DDR4DB02 can respond to back to back read commands starting width MPR3 as shown in Table 11.

Table 11 — MPR3,0,1,2,3,0,1,2 Override Read Format for Staggered Return

RD Command Staggered	MPR3 UI0-7	MPR0 UI8-15	MPR1 UI16-23	MPR2 UI24-31	MPR3 UI32-39	MPR0 UI40-47	MPR1 UI48-55	MPR2 UI56-63
DQ0	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ1	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ2	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ3	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ4	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ5	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ6	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ7	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1

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2.15 MRS Write Commands

The RCD only generates MRS Write commands to the data buffers for each A-side MRS command to Rank 0.

Table 13 shows the sequence for MRS Write commands.

Table 12 — Multicycle Sequence for MRS Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	MRS Write	MRS Write Command BCOM[3:0] = 1011
2	DAT0	MRS ID code BCOM[3:0] = {0, BG0, BA1, BA0}
3	DAT1	First data transfer for MRS Write command BCOM[3:0] = {0, DA2, DA1, DA0]
4	DAT2	Second data transfer for MRS Write command BCOM[3:0] = {0, DA5, DA4, DA3}
5	DAT3	Third data transfer for MRS Write command BCOM[3:0] = {0, DA8, DA7, DA6}
6	DAT4	Fourth data transfer for MRS Write command BCOM[3:0] = {0, DA11, DA10, DA9}
7	DAT5	Fifth data transfer for MRS Write command BCOM[3:0] = {0, 0, DA13, DA12}
8	PAR[3:0]	Even parity bits for MRS Write command and data PAR[x]: parity bit for 7 previous BCOM[x] transfers
9	Next Cmd	Next Command

The sequence for an MRS Write command is shown in Figure 4 below. The timing diagram shows how the MRS Write command is followed by six data transfer cycles and a parity data transfer cycle. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the MRS Write command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRS Write command also imposes a limitation on how close consecutive MRS Write commands can be issued to the data buffer.

For MRS commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in F0RC0D is set to ‘0’ (LRDIMM), the DDR4 register generates a BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer’s host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection. The DDR4DB02 will not capture any MRS bits written in PDA mode.

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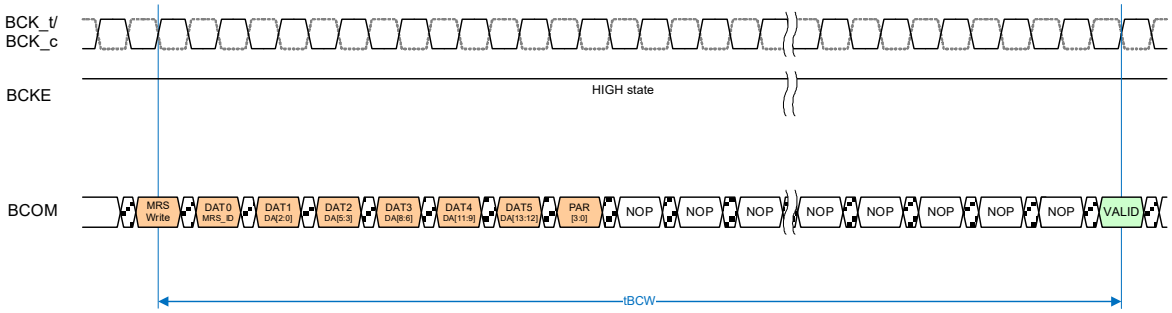

Figure 4 — MRS Write command sequence

2.16 Per DRAM Addressability Support

In order to enable the DDR4 'per DRAM addressability (PDA)' feature the data buffer will perform a "write" data transaction in each MRS Write command to transfer data from the host interface to the DRAM interface whenever the PDA mode enable bit in F0BC1x is set to 1 to indicate that this feature is enabled. This will need to be a special write mode in the data buffer because it is necessary to meet the PDA setup and hold timing parameters (tPDA_S and tPDA_H) in the DDR4 DRAMs. This special write mode will work by allowing the host to have direct control of the MDQ signals on the DRAM interface of the buffer in transparent mode. In other words, the DQ to MDQ path will work in asynchronous transparent mode. In this way, the host will be able to assert the MDQ0 lines early enough to meet tPDA_S and late enough to meet tPDA_H. The data buffer will control the data strobe (MDQS_t/MDQS_c) burst on the DRAM interface as in a normal write command.

The DB does not process regular DRAM Write commands while in PDA mode. However, the RCD needs to process DRAM MPR Write commands correctly during this time. Before entering 'per DRAM addressability (PDA)' mode, DRAM write leveling is required to be performed by the host to the DRAM.

The sequence to enter and exit PDA mode for LRDIMMs is as follows (steps 1 and 2 can be swapped if desired):

1. Send MRS command to MR3 with A4=1 to the rank to be put into PDA mode
2. Send BCW to F0BC1x with DA2=1 to enter DB PDA mode
3. Perform per DRAM MRS commands (only for the rank that was put in PDA mode in step 1)
4. Send MRS command to MR3 with A4=0 to the rank that is in PDA mode with all DRAMs selected (DQ0=0)
5. Send BCW to F0BC1x with DA2=0 to exit DB PDA mode

The timing diagram in Figure 5 shows how the data buffer will handle MRS commands in 'per DRAM addressability (PDA)' mode. The path from host DQ to DRAM interface MDQ works in (asynchronous) transparent mode in this case.

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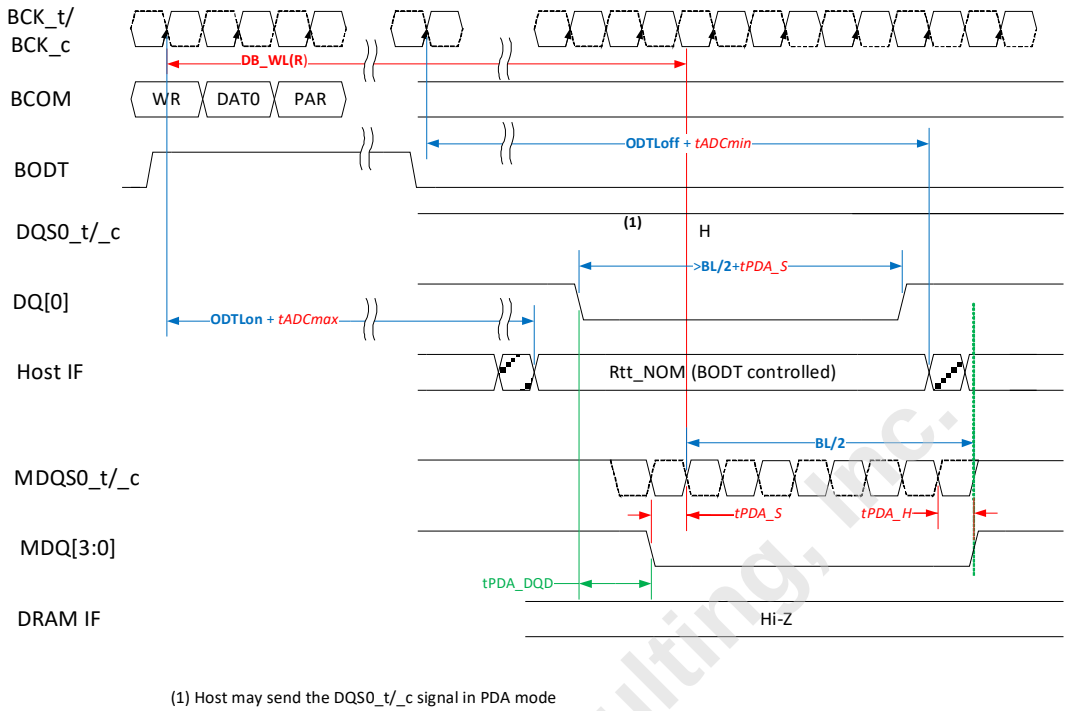

Figure 5 — Processing of DRAM MRS command by data buffer in PDA mode

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2.17 BCW Write Command

Table 13 shows the sequence for buffer control word write commands.

Table 13 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0]
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

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The sequence for a BCW Write command is shown in Figure 6 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tBCW parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

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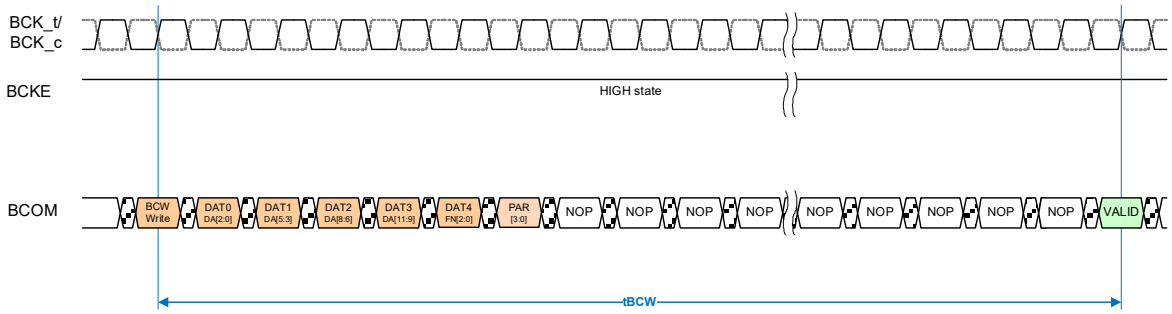

Figure 6 — Buffer Control Word Write command sequence

2.18 Per Buffer Addressability Feature

It is necessary for the data buffer to support a feature similar to per-DRAM addressability in the buffer control word access transactions. This feature will be used to allow the host controller to configure each data buffer independently from each other. This is a requirement, for example, to allow independent VrefDQ training per buffer or independent ODT impedance settings for certain buffers. The DDR4DB02 will support both BL8 and BC4 in PBA mode.

The PBA feature will be enabled by a BCW bit stored in a word that does not contain any registers that need to be programmed in per-buffer addressability mode. This is necessary so that it is possible to get the buffers in and out of PBA mode without having to modify BCW bits that have been programmed specifically per buffer. The mechanism to enable and disable BCW Write access per buffer will be very similar to the PDA mechanism, it will be based on the DQ0 host interface input signal, and it will only work once host interface write leveling training has been completed from the host controller to the data buffers. When PBA mode is enabled each buffer will use the captured DQ0 input signal level to determine if the BCW Write transaction actually applies to that particular buffer. The VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 low level in PBA mode.

The sequence for two consecutive BCW Write commands with 'per-buffer addressability (PBA)' mode enabled is shown in Figure 7 below. This sequence shows consecutive BCW Write commands. Figure 8 shows the sequence for a BCW write command with 'per-buffer addressability (PBA)' mode enabled followed by a non-BCW write command. Since in the 'per-buffer addressability (PBA)' mode only BCW Write commands are allowed, the BCW Write command shown in Figure 8 has to be used to disable (exit) the 'per-buffer addressability (PBA) mode. Before entering 'per-buffer addressability (PBA)' mode, the following buffer control words must be programmed: Host Interface RTT_NOM Control Word (BC00) and Host Interface RTT_PARK Control Word (BC02). After the Host Interface RTT_NOM and Host Interface RTT_PARK have been programmed 'per-buffer addressability (PBA)' mode can be enabled using BCW bit (F0BC1x, DA0). In the 'per-buffer addressability (PBA)' mode, all BCW Write commands are qualified with DQ0. If the value on DQ0 is 0 then the buffer executes the BCW write command. If the value on DQ0 is 1, then the buffer ignores the BCW Write command. The controller can choose to drive all the DQ bits. The per buffer control word command cycle time in PBA mode tMRD_PBA is required to complete the write operation to the mode register and is the minimum time required between two BCW Write commands, as shown in Figure 7. Remove the buffer from 'per-buffer addressability (PBA)' mode by setting the corresponding BCW bit (F0BC1x, DA0). This command will require DQ0=0.

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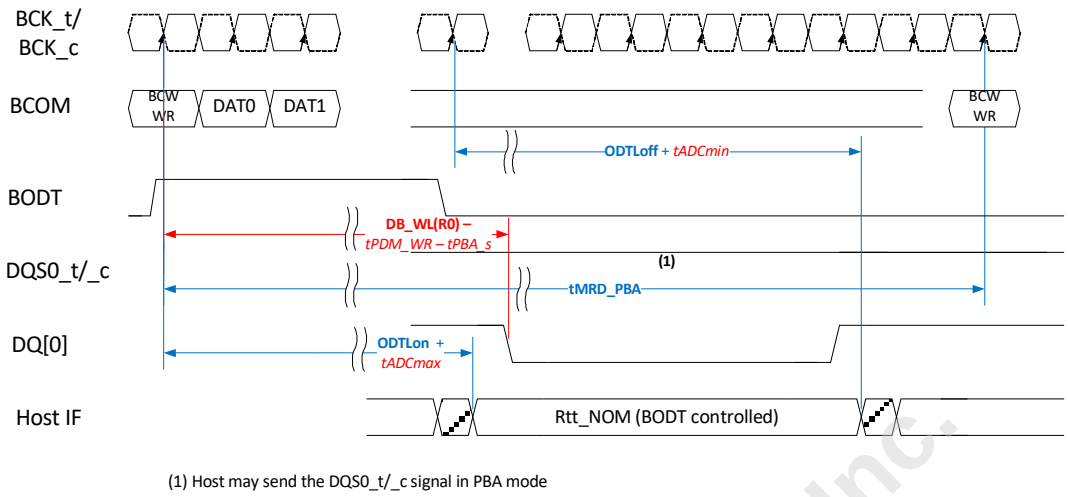

Figure 7 — BCW Write to BCW Write command sequence in PBA mode

Removing a buffer from 'per-buffer addressability (PBA)' mode will require programming the entire buffer control word when the BCW Write command is issued. The per buffer control word command update delay time tMOD_PBA is required to complete the write operation to the mode register and is the minimum time required between a BCW command and any other valid command when 'per buffer addressability (PBA)' mode is enabled, as shown in Figure 8. The data buffer uses Rank 0 write timing in PBA mode.

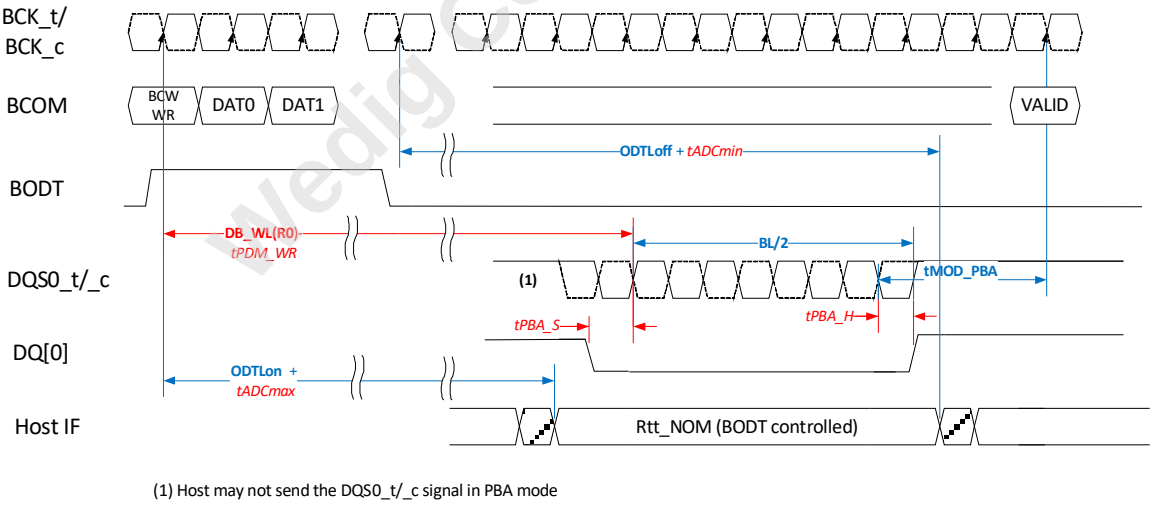

Figure 8 — BCW Write to other command sequence in PBA mode

Dynamic ODT is not supported. So extra care is required for the ODT setting. If RTT_NOM is enabled in the Host Interface RTT_NOM Control Word (BC00), the buffer data termination needs to be controlled by the BODT pin and applied with the same timing parameters as in normal operation.

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2.19 BCW Read Commands

Buffer Control Words can be read from the DDR4DB02 via BCW read commands.

Table 14 shows the sequence for BCW Read commands.

Table 14 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

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The sequence for BCW Read command is shown in Figure 9 below. The timing diagram shows how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR override read from MPR0 (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD01 will forward Read command to DRAM but DDR4DB02 will ignore read data from DRAM. After the read command that follows the BCW Read command, the DB will be back in normal operation, i.e. all subsequent reads come from the DRAM interface (unless F0BC1x DA1=1). The host is required to wait at least tBCR between issuing a BCW Read command and the following Read command.

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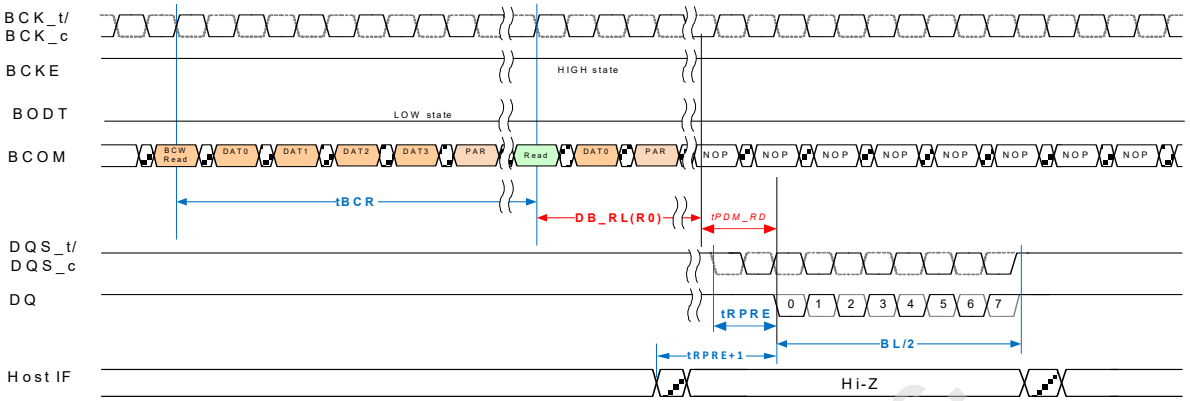

Figure 9 — BCW Read command sequence

2.19.1 BCW Read Data Format

Only the serial data format is available for Reads following a BCW Read commands - see Table 15. The data buffer is required to drive associated strobes with the read data return. Serial return implies that the same pattern is returned on all DQ lanes as shown in the table below. All undefined or reserved bits in the BCW must be driven as '0'. In this example the value programmed in BCWXx (DA[7:0]) is 0111 1111. The command issued from the register is BCW Read (BCOM[3:0] = 1101). This tells the buffer that the 8 bits from BCWXx need to be accessed serially. All BCW read transactions are done in burst length of 8 by the buffer. All BCW accesses are aligned to byte boundaries. The DB will always send two 4-bit CWs on every 4-bit CW Read command. In case of a 4-bit CW Read command with an even address in RCD F0RC6x DA[7:4], the DB will send the addressed 4-bit CW in UI0 .. UI3 and the next address 4-bit CW in UI4 .. UI7. In case of a 4-bit CW Read command with an odd address in RCD F0RC6x DA[7:4], the DB will send the addressed 4-bit CW in UI4 .. UI7 and the previous address 4-bit CW in UI0 .. UI3.

Table 15 — BCW Read Data Format

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

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2.20 Training Support Features

The DDR4DB02 does not contain self-sufficient training state machines for calibrating its timing control settings. It will instead depend on the host controller to get the timing control registers programmed with the appropriate settings that will allow the DB to work in the DDR4 LRDIMM environment. To enable the host controller in performing the training procedure in an efficient and reliable manner, the data buffer provides various training support features. The following sections describe such training support features in the DDR4DB02

The DB provides separate timing control registers for the lower and upper nibble. However, there is only one Buffer Training Mode Control Word so both nibbles are always in the same training mode.

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Table 16 below provides an overview of the buffer control words (BCW) that are involved in the timing control and timing training features of the DDR4DB02.

Table 16 — Timing and Training Control Words

Address	Description	Scope
BC0C	Training control word	Training mode enable
F0BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0	Additional cycles of DRAM Interface Receive Enable Delay and Write Leveling Delay per rank and per nibble
F0BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0	
F0BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2	
F0BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2	
F1BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1	
F1BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1	
F1BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3	
F1BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3	
F[3:0]BC2x	Lower nibble DRAM interface receive enable training control	DRAM Interface Receive Enable phase and cycle control per rank
F[3:0]BC3x	Upper nibble DRAM interface receive enable training control	
F[3:0]BC4x	Lower nibble MDQS read delay control	Input MDQS delay control per rank
F[3:0]BC5x	Upper nibble MDQS read delay control	
F[3:0]BC8x	Lower nibble MDQ-MDQS write delay control	Output MDQ signal phase control per rank
F[3:0]BC9x	Upper nibble MDQ-MDQS write delay control	
F[3:0]BCAx	Lower nibble host interface write leveling control	Host Interface write leveling phase and cycle control per rank
F[3:0]BCBx	Upper nibble host interface write leveling training control	
F5BC0x - F5BC3x F6BC0x - F6BC3x	Lower and upper nibble Multi Purpose Registers[7:0]	Store read/write data patterns for receive enable, read and write delay and host interface write training as well as MPR override mode.
F6BC4x	Buffer training configuration control word	Configuration control for certain training modes
F6BC5x	Buffer training status word	Status for certain training modes
F[7:4]BC8x	MDQ0/4-Read delay control	Input MDQS delay control per rank and per lane
F[7:4]BC9x	MDQ1/5-Read delay control	
F[7:4]BCAx	MDQ2/6-Read delay control	
F[7:4]BCBx	MDQ3/7-Read delay control	
F[7:4]BCCx	MDQ0/4-MDQS write delay control	Output MDQ signal phase control per rank and per lane
F[7:4]BCDx	MDQ1/5-MDQS write delay control	
F[7:4]BCEx	MDQ2/6-MDQS write delay control	
F[7:4]BCFx	MDQ3/7-MDQS write delay control	

Table 17 below provides a summary description of the various training support functions and features in the DDR4DB02.

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Table 17 — Summary of Training Support Features and Functions

Training Step	Features
DRAM Interface Receive Enable Phase Training (MREP)	Receiver enable phase detector on MDQS pins Phase detector output driven on host interface DQ pins
DRAM Write Leveling (DWL)	Generates MDQS but forwards MDQ to DQ.
Host Interface Write Leveling (HWL)	Write Leveling phase detector on DQS pins Phase detector output driven on host interface DQ pins
MDQS Read Delay Training (MRD)	Phase adjustment for MDQS input delay Multi Purpose Register control words Data comparator output driven to host interface DQ pins
MDQ-MDQS Write Delay Training (MWD)	Phase adjustment for MDQ-MDQS output delay Multi Purpose Register control words Data comparator output driven to host interface DQ pins
Host Interface Write Training (HIW)	Write data comparator logic Multi Purpose Register control words Data comparator output in training status word

For the training modes that utilize a data comparison between received data and expected data (stored in the data buffer MPR), the host needs to wait tCCD_CMP between commands with data movement (i.e. READ or WRITE). The DDR4DB02 does not support contiguous DQ data streams (i.e. without dead cycles between data bursts) in these training modes.

An example sequence for DDR4DB02 training is described in the flow diagram of Figure 10 below.

The host is responsible to program the Rank Presence control word BC07 to match the ranks of the particular module in training before any of the training modes are entered and this control word should not be changed from this point in time onwards (until the module is reset or retrained).

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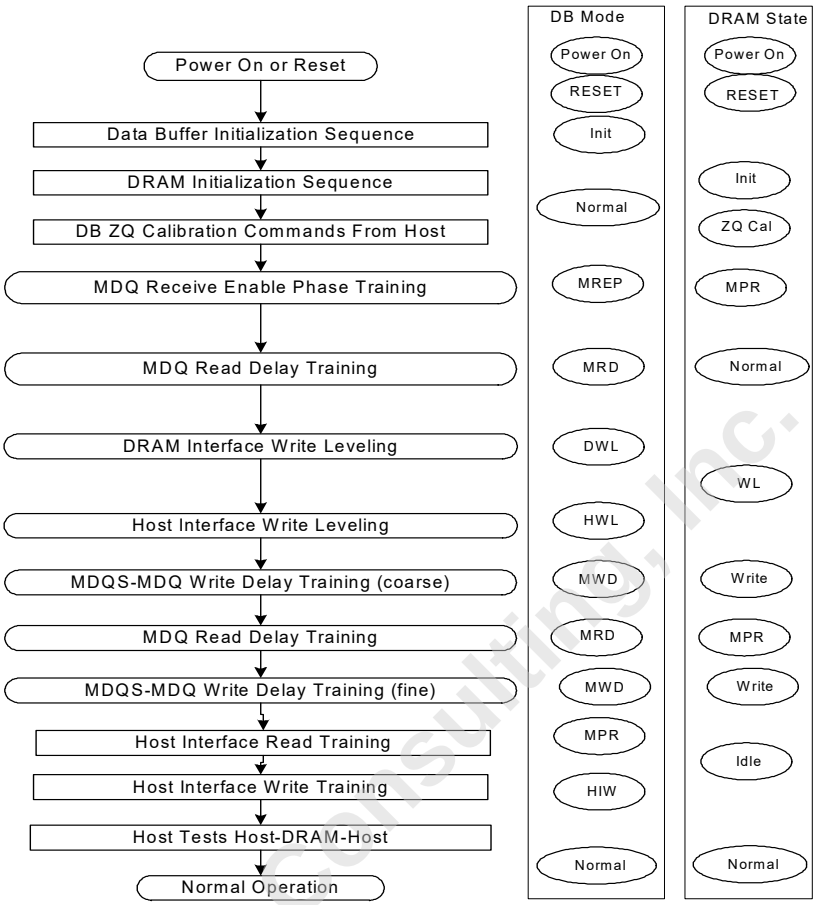

Figure 10 — Example of Training Sequence Flow Diagram

2.20.1 DRAM Interface MDQ Receive Enable Phase (MREP) Training Mode

This training mode has been defined so that it can be performed before any training has taken place between the host controller and the DDR4DB02

The DRAM interface receive enable phase timing selection is controlled in steps of 1/64 * t_{CK} by Bits DA[5:0] in F[3:0]BC2x and F[3:0]BC3x. The host controller has the ability of setting the values for this parameter by means of BCW Write commands. The problem is how to find the optimal settings that will allow the data buffer to work reliably in the LRDIMM environment. To help the host controller solve this problem, the data buffer provides a DRAM interface receive enable phase training mode. In this training mode, the data buffer uses a group of programmable delay elements and sampling circuits to capture the MDQSx_t/MDQSx_c signals received from the DRAMs. There is one delay element per nibble and per rank. When the Receive Enable training control bits (F[3:0]BC2x/F[3:0]BC3x) are all zero, the phase of the internal DRAM interface receive enable clock is aligned to the data buffer input clock signal (BCK_t/BCK_c). In this training mode, the output of each MDQ/MDQS sampling circuit is driven onto the four host interface DQ pins corresponding to each nibble. In this training mode, the DQS_t/DQS_c inputs and outputs at the host interface are disabled.

To perform receive enable phase training, the host will first enable the MDQS Receive Enable Training mode in the

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Training Control Word (BC0C). After that, and assuming that the DRAMs have already been initialized, the host will send a sequence of Read commands to the DRAMs (using the DRAMs MPR) in order to generate a continuous train of pulses in the MDQSx_t/MDQSx_c inputs of the data buffer. The data buffer will use the RANK_ID field in the Read Command sequences received through the BCOM[3:0] interface to select which receiver enable timing control register will be used during training. The DB will use F0BC2x and F0BC3x for Rank 0, F1BC2x and F1BC3x for Rank 1, and so on. Using the output of the sampling circuits available on the DQ pins, the host controller will be able to decide if it needs to increase or decrease the receive enable phase control settings in the data buffer by means of BCW Write commands. The objective is to find the end of the DRAM read preamble, i.e. first rising edge of MDQS_t. At this time, the output of the sampling circuits will change from 0 to 1. With this method, the host controller will be able to align the internal receive enable clock to the first rising edge of the incoming MDQSx_t/ MDQSx_c signals. Once this point has been found, the host controller will program the final value by applying an offset to the training result. The host must apply an offset of half clock cycle (32/64 * t_{CK}) for 1 t_{CK} read preamble mode or an offset of a full clock cycle (1*t_{CK}) for 2 tC_K read preamble mode.

The MREP training step trained the partial cycle fields in the DRAM interface receive enable control words to their correct position, aligned with the strobes coming from the DRAMs. However, in the presence of large command delay differences between DRAM and data buffer, the full cycle fields in the DRAM interface receive enable control words may also need adjustment so that the data buffer receivers are enabled in the correct cycle. To accomplish this task, the host can put the data buffer into MRD mode by a BCW write to BC0C. In MRD mode, the host writes a known pattern to the DRAM MPR registers and also into the MPR registers of the data buffer and reads it back, allowing the data buffer to compare the read data with the known pattern. See section 2.20.4 for details on MRD mode.

If the comparison shows that the data read is equal to the data written, the full cycle field in F0BCCx, F1BCCx, F0BCEx and F1BCEx is correct. If there is a mismatch, the host adjusts the full cycle field bits and repeats the READ/WRITE sequence until the comparison results show that the data written was correctly read back.

The data buffer provides only a single Read FIFO fall-through time for all ranks and for correct operation this delay cannot change. Any potential adjustments to this data buffer Read FIFO fall-through time have to be performed prior to this training step. The host is responsible for establishing and maintaining its own unique read enable timing for each rank.

The DRAM interface receive enable timing established in this training step is also used by the DB for the driver enable for the DQ/DQS outputs for Read commands (by adding an offset that corresponds to the Read FIFO flow-through time) as well as for the turn-on and turn-off timing of the DRAM interface MDQ/MDQS ODT termination.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

To allow the host to perform its own receive enable training, the host needs to exit MREP mode and put the data buffer into normal mode. In normal mode, the DB will forward the read data from the DRAM interface to the host interface and generate the associated DQS_t/DQS_c strobes. Optionally, Read Preamble Training mode (F0BC1x DA4=1) may be enabled normal mode to help the host with its own receive enable training.

2.20.2 DRAM Interface Write Leveling (DWL) Training Mode

This training mode has been defined so that it can be performed before any training has taken place between the host and the DDR4 DB.

The DRAM interface write leveling phase timing selection is controlled in steps of 1/64 * t_{CK} by Bits DA[5:0] in F[3:0]BCAx and F[3:0]BCBx. The host controller has the ability of setting the values for this parameter by means of BCW Write commands. There is one delay element per nibble and per rank. In this training mode, the data buffer drives the DRAM feedback onto the four host connector interface DQ pins corresponding to each nibble.

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To perform DRAM interface write leveling training, the host will first enable the DRAM Interface Write Leveling Training mode in the Training Control Word (BC0C). After that the host will increment the strobe timing by writes to F[3:0]BCAx/F[3:0]BCBx. The data buffer will generate a sequence of pulses on its MDQSx_t/MDQSx_c outputs (meeting the DDR4DB02 tMQSH(min) and tMQSL(min) parameters). In this training mode the DQ inputs are disabled and the DQ outputs drive the sampled MDQ inputs. The DQS_t/DQS_c inputs and outputs at the host interface are disabled. The data buffer will use the content of BC08 DA[1:0] to select which Write Leveling timing control word will be used during DRAM Write Leveling training. The DB will use F0BCAx/F0BCBx and F0BCDx for Rank 0, F1BCAx/F1BCBx and F1BCDx for Rank 1, F2BCAx/F2BCBx and F0BCFx for Rank 2 and F3BCAx/ F3BCBx and F1BCFx for Rank 3. Using the DRAM feedback available on the data buffer's DQ output pins, the host controller will be able to decide if it needs to increase or decrease the DRAM Write Leveling control settings in the data buffer by means of BCW Write commands.

The host controller can perform this procedure independently for the upper and the lower nibbles, because the data buffer provides independent controls for the upper and the lower nibbles. The host controller can also perform this procedure independently per rank because the data buffer provides independent receive enable phase timing controls per rank.

The DRAM Write Leveling training step should be followed by the host interface write leveling step by writing with a BCW to BC0C.

2.20.3 Host Interface Write Leveling (HWL) Mode

Since the DRAM write leveling timing adjustments are done by the data buffer, the host does not yet know the required strobe alignments to the clock. To help the host controller solve this problem, the data buffer provides a host interface write leveling training mode. The host controller is responsible for performing this procedure independently for each rank (and maintain its adjusted DQS delays per rank) since the buffer has the same Write FIFO fall-through times independent of the rank.

To perform write leveling phase training, the host will first enable the Host Interface Write Leveling mode in the Training Mode Control Word (BC0C). After that, and assuming that the DRAM interface write leveling training has already been performed, the host will issue DESELECT commands to the DB (targeted at the DRAMs). The host will generate one half-cycle DQSx_t/DQSx_c pulse per DESELECT command. This Host interface write leveling scheme assumes that the data buffer has only a single Write FIFO fall-through time through the data buffer and that this delay doesn't change (until the next initialization sequence) so any potential adjustments to the data buffer Write FIFO fall-through time have to be performed prior to this training step.

In this training mode, the DDR4 DB keeps the MDQ/MDQS drivers disabled. The DB will signal the strobe to clock alignment on the host connector interface DQ pins (in the same way a DRAM signals its strobe to clock alignment), i.e. the DQS_t/DQS_c inputs and the DQ outputs are enabled. Since the strobe to clock alignment has already been performed on the DRAM interface side, and the Write FIFO fall-through time is fixed, the data buffer knows the required strobe timing on the host interface for each nibble for each rank and can provide the alignment information to the host. The host controller will be able to decide if it needs to increase or decrease the DQSx_t/DQSx_c timing. The objective is to find the setting where the output of the DB DQ pins changes from '0' to '1'.

The host controller needs to perform this procedure independently for the upper and the lower nibbles, because each x4 DRAM will require a different write leveling adjustment. The host controller can also perform this procedure independently per rank because the data buffer provides independent receive enable phase timing controls per rank. The host is required to program BC08 DA[1:0] with the Rank ID of the rank being write leveled before entering HWL mode.

When the BODT input is asserted the DB provides RTT_NOM termination on DQS_t/DQS_c in this mode with the previously established host ODT timing but DQ termination is OFF. When the BODT input is de-asserted the DB provides RTT_PARK termination on DQS_t/DQS_c in this mode with the previously established host ODT timing but DQ termination is OFF. The data buffers on all LRDIMMs in a channel must be put into this mode for write leveling. The write leveling is performed one rank at a time and the data buffers on other DIMMs should have their

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DQ outputs and terminations disabled with writes to BC03, DA3='1'.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

The procedures described in the DWL and HWL training modes are used to achieve phase alignment between the DRAM strobe and the clock inputs. However, the host still does not know whether its strobe timing established in the HWL step corresponds to the correct CAS Write Latency (CWL) required by the DRAM. After the training steps are completed, the host performs a sequence of Writes followed by Reads to establish the correct cycle timing for write leveling by writing the Additional Cycles of DRAM Interface Write Leveling Delay control words (F0BCDx, F1BCDx, F0BCFx, F1BCFx).

2.20.4 DRAM-to-DB Read Delay (MRD) Training Mode

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM (either from its internal array or from the MPRs for data-preserving read training). The data buffer provides data pattern control words that are programmed with the expected read data from the DRAM and the results of the comparison is provided on the data buffers host interface.

To perform DRAM-to-DB read training, the host will first enable the MDQS read delay training mode in the Training Mode Control Word (BC0C).

The delay of the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) during read transactions is selected by buffer control word F[3:0]BC4x and F[3:0]BC5x for lower and upper nibble respectively. The nominal setting for F[3:0]BC4x/F[3:0]BC5x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into F[3:0]BC4x/F[3:0]BC5x. Since the DDR4DB02 uses the RANK ID fields in the BCOM Read Command sequences to select the correct DRAM interface receive enable timings for the reads from the DRAMs, the content of BC08 DA[1:0] is don't care while in this training mode.

In this training mode, the data buffer uses a data pattern comparator to determine if the read data arriving from the DRAMs after a Read command match an expected result. There is one data comparator per data buffer. The output of the data comparator is driven onto the eight host connector interface DQ pins corresponding. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. Bit 0 of the Buffer Training Configuration control word F6BC4x selects whether all four DQ bits within a nibble are driven to '0' if there is any mismatch in any of the 32 bits associated with that nibble or whether only the DQ bit(s) of the particular lane(s) (i.e. the series of 8 bits arriving on the same DQ bit) that had one or more mismatches are driven to '0'. The expected data pattern values are stored in the MPR control words F5BC0x through F5BC3x and F6BC0x through F6BC3x.

MPR0[7:0] will contain the expected first UI (UI0) for MDQ[7:0] and MPR7[7:0] will contain the expected last UI(UI7) for MDQ[7:0], or in a general sense: MPRx[7:0] should match UIx for MDQ[7:0].

The 64 bits contained in these data registers can support arbitrary data patterns in a single BL8 data transaction. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The DDR4DB02 is required to support fine adjustment of the phase of individual bit lanes relative to the baseline MDQS for DDR4 data rates above 2400 MT/s-. For this purpose the host controller can utilize the per lane MDQS-MDQ read delay control words F[7:4]BC8x through F[7:4]BCBx. F4BC8x controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BC9x controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS

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delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQS delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

2.20.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB02 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/ F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

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2.20.6 Host Interface Read Training

For the DB-to-host read training, the DQS delay adjustments are performed in the host so that it can correctly sample the data driven by the DB (originating from the data buffer's MPRs instead of originating from the DRAM MPRs).

To perform DB-to-host read training, the host will first enable the MPR Override mode in the Buffer Configuration Control Word (F0BC1x) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host will cause the data buffer to send the contents of the data buffer's MPR back to the host by issuing DRAM Read commands through the DDR4 register.

This mode utilizes MPR0 to MPR3 and supports the same formats as a DDR4 DRAM page 0 MPR reads (Serial, Parallel, and the Optional Staggered if supported).

The DDR4DB02 uses the Rank 0 output enable timing for MPR Override reads.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

2.20.7 Host Interface Write Training (HIW) Mode

For the host-to-DB write delay training, the DQ-DQS delay adjustments are performed in the host so that the data buffer receives the DQ and DQS signals with the optimal phase relationship. The data buffer provides data pattern control words that are programmed with the expected write data from the host and the results of the comparison is provided in the training status word (F6BC5x) and in BC0F, DA3. The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x). Read command following a BCW Read to F6BC5x command in that mode is designed to provide the content of F6BC5x[7:0] on the DQ[7:0] for a burst length of 8 in a way similar to the MPR mode with data coming from the mentioned register. The DDR4DB02 uses the Rank 0 output enable timing for these reads.

To perform host-to-DB write training, the host will first enable the host interface write training mode in the Training Mode Control Word (BC0C), followed by write commands to the RCD and DB. The DDR4DB02 uses the RANK ID field in the BCOM Write Command sequences to select the correct host interface write leveling timing. The content of BC08 DA[1:0] are don't care while in this training mode. Using the result from the data comparator available in the Training Status Word and Error Status Word, the host controller will be able to determine if it has found the correct value of DQS-DQ delay for that particular nibble or bit lane or if needs to increment or decrement its own phase delay. The host may also send one or more consecutive read commands to obtain the result from the data comparator available in the Training Status Word F6BC5x.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

After the host interface read and write training steps are completed the host may perform additional writes and read to and from DRAM to further train the host bus by adjusting its own I/O timings

2.21 Transparent Mode

Transparent mode is enabled in the DDR4DB02 by setting F0BC1x DA5 to 1. While in transparent mode, the DB does not interpret BCOM commands. For BCOM[3:0] input values of '1010' it directs the data flow from host interface to DRAM interface and it enables the on-die termination at the host interface. For BCOM[3:0] input values other than '1010', the Data Buffer directs the data flow from DRAM interface to host interface and it enables the on-die termination at the DRAM interface. The Data Buffer does not support high-speed changes in direction of data flow. The tMRD_TM parameter in the Timing Requirements section describes how often the direction in data flow can be reversed in transparent mode.

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In transparent mode the Data Buffer statically enables the input receivers of the interface that is receiving signals and it permanently enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. In this mode, the data and data strobe signals flow asynchronously through the DB. The DB needs to provide balanced (matched) propagation delay for all the signals within each DQ/DQS-MDQ/MDQS nibble.

All the clock frequencies available in normal mode in the Data Buffer will also be supported in transparent mode.

The test equipment will have direct control of the BODT signal through the DODTn inputs of the DDR4 Register. The DB supports two modes for using the BODT signal while transparent mode is enabled. The two modes are selected by F0BC1x DA6 and they are described in Table 18 below. In the first mode, the BODT input signal is ignored and the enabling of the on-die termination is determined only by the BCOM[3:0] inputs. The host interface termination is enabled for BCOM[3:0] input values of '1010', and the DRAM interface termination is enabled for BCOM[3:0] input values other than '1010'. In the second mode, the BODT signal is used as a condition, in addition to the BCOM[3:0] values, to enable or disable the on-die terminations of the DRAM interface and the host interface. In the second mode, the on-die terminations are enabled when BODT is driven HIGH, and the terminations are disabled when the BODT signal is driven LOW.

In transparent mode, the strength of the DRAM Interface termination is controlled by the MDQ RTT Buffer Control Word (BC04) and the strength of the Host Interface termination is controlled only by the RTT_NOM Buffer Control Word (BC00).

Table 18 — DB Termination Control in Transparent Mode

BCOM[3:0]	BODT	BODT Mode (F0BC1x DA6)	Host Termination	DRAM Termination
= '1010'	LOW	0	ON	OFF
		1	**OFF**	OFF
	HIGH	0	ON	OFF
		1	ON	OFF
≠ '1010'	LOW	0	OFF	ON
		1	OFF	**OFF**
	HIGH	0	OFF	ON
		1	OFF	ON

2.22 One Rank Timing Mode

The DDR4DB02 device supports a Single Rank Timing Mode feature. When enabled the DDR4DB02 uses one common MDQS/MDQ DRAM interface rank timing for all ranks instead of the default Per Rank Timing Mode. After the Host has completed training on a per rank basis, the Host will calculate one common DRAM interface MDQS/ MDQ rank timing for all ranks. The Host will then program the common rank timing values into Rank 0 of the DDR4DB02 timing control words F0BCCx, F0BCDx, F0BC2x, F0BC3x, F0BC4x, F0BC5x, F0BC8x, F0BC9x, F0BCAx, F0BCBx, F4BC8x, F4BC9x, F4BCAx, F4BCBx, F4BCCx, F4BCDx, F4BCEx, F4BCFx. The Host can then enable One Rank Timing Mode by setting F0BC1x, DA3= 1. The Host at any time can restore per rank settings and disable this feature by programming F0BC1x DA3=0.

2.23 ZQ Calibration

The DDR4DB02 performs I/O circuit calibration when it receives BC06 commands CMD1 (ZQCL) or CMD2 (ZQCS). In order to use ZQ calibration command, a 240 Ω +/- 1% resistor must be connected between the ZQCAL pin and Vss.

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Proper host interface RTT_NOM, RTT_WR, RTT_PARK DQ/DQS drive strength, DRAM interface RTT and MDQ/MDQS drive strength not guaranteed until a ZQCL calibration command is issued.

The host sends ZQCL and ZQCS calibration commands through the DDR4 register. The host needs to issue ZQ calibration commands sequentially to each package rank (i.e. wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one). No other commands that cause data transfers on the host interface DQ/DQS outputs or the DRAM interface MDQ/MDQS outputs are allowed during the tZQinit, tZQoper or tZQCS periods.

The DDR4DB02 may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands. That will depend on the behavior of the DDR4 register. If the DDR4RCD02 is configured to generate a CMD1 or CMD2 BCW sequence upon receiving ZQCL and ZQCS commands from the host, then it will cause the DB to perform the corresponding calibration command. The host also has the ability to directly issue BC06 BCW transactions to send CMD1 and CMD2 commands to the DDR4 data buffers.

2.24 Decision Feedback Equalization (DFE)

For frequencies of 2933 MT/s and above the DDR4DB02 device will support a 4 Tap decision feedback equalization (DFE) on its host-interface receivers. The host can enable 1, 2, 3 or 4 taps in a consecutive order always starting with Tap 1 as shown in Table 19. Read-only status bits F2BCEx - DA4 and F2BCEx - DA6 identify the DFE capabilities supported by each DDR4DB02 device. DFE input gain adjustment is controlled in BCW F2BCFx and DFE Tap Coefficients 1 through 4 are adjusted by control words F3BCCx through F3BCFx, respectively. These DFE control words allow programming of each parameter on a DQ I/O-specific basis, and they are intended to be trained by the host. The DDR4DB02 device does not support adaptive DFE. In order to allow Data Buffer hardware to correctly preset DFE post-cursor bit values before the start of Write data bursts, the host must ensure a high on all DQ pins during DQS preamble as shown in the DDR4DB02 WRITE timing Figure 2.

2.24.1 Tap Configurations

Table 19 — Tap Configurations

Number of Taps Enabled	F3BCC x DA6	F3BCD x DA6	F3BCE x DA6	F3BCF x DA6	Tap 1	Tap 2	Tap 3	Tap 4
0	0	x	x	x	Disabled	Disabled[1]	Disabled[1]	Disabled[1]
1	1	0	x	x	Enabled	Disabled	Disabled[2]	Disabled
2	1	1	0	x	Enabled	Enabled	Disabled	Disabled[3]
3	1	1	1	0	Enabled	Enabled	Enabled	Disabled
4	1	1	1	1	Enabled	Enabled	Enabled	Enabled

1. DDR4DB02 hardware disabled by F3BCCx DA6 = 0, F3BCDx DA6, F3BCEx DA6 and F3BCFx DA6 are don't care and ignored by Data Buffer.
2. DDR4DB02 hardware disabled by F3BCDx DA6 = 0, F3BCEx DA6 and F3BCFx DA6 are don't care and ignored by Data Buffer.
3. DDR4DB02 Hardware disabled by F3BCEx DA6 = 0, F3BCFx DA6 is a don't care and ignored by Data Buffer.

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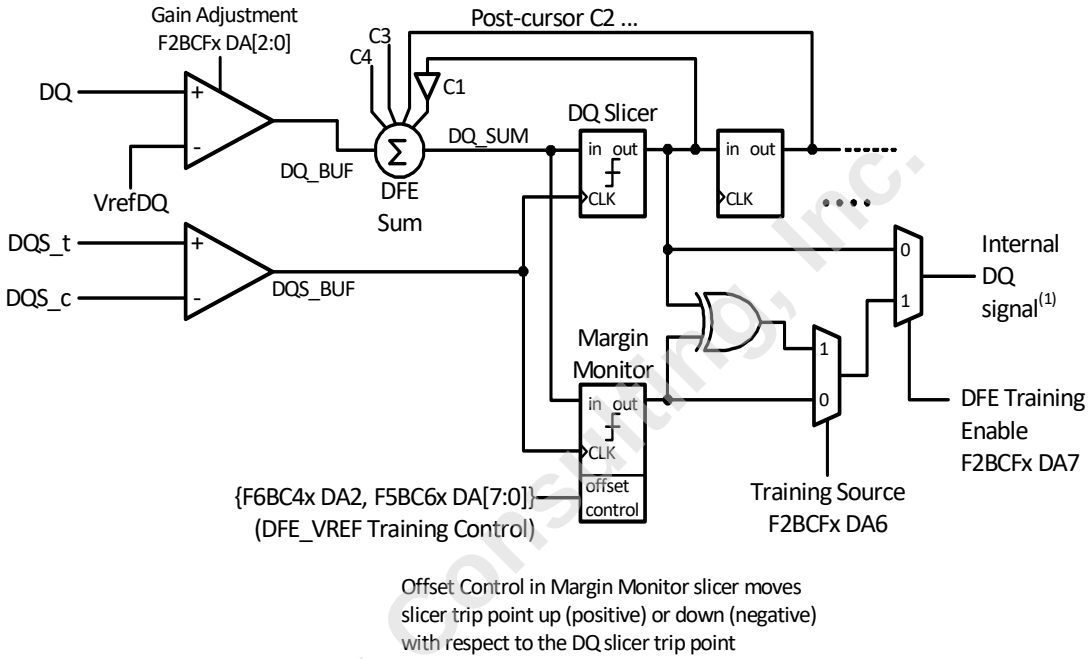
2.24.2 DFE Training Support

The DDR4DB02 device supports DFE training mode in its Host Interface input circuits. The purpose of DFE training mode is to configure input receiver and Vref generator circuits so that a DFE training reference voltage (DFE_VREF) is controlled by F5BC6x - DA[7:0] and F6BC4x - DA2 while the effective DRAM interface Vref setting is maintained at the last value programmed in F5BC6x - DA[7:0] and F6BC4x - DA2 before F2BCFx - DA7 (for any one of the DQn pins) is set to 1.



NOTE 1: This signal propagates through the Data Buffer device and supports regular DB02 features such as DRAM Data Writes and Host Interface Write Training (HIW).

Figure 11 — DFE Training Circuitry

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2.25 Optional NVDIMM Support Feature

2.25.1 NVDIMM Initialization Sequence

The recommended sequence for initializing an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. Power up.
   a. NV local controller starts with LCOM[2:0] and LCK_t/LCK_c pins disabled and LCKE pin driven LOW.
2. Check SPD.
3. Configure RCD02 and DB02 basic settings.
4. Execute DRAM initialization sequence.
5. Perform Host to RCD02/DB02/DRAM training sequences as needed.
6. Enable NVDIMM mode (Write F4RC00 – DA0 = 1).[1]
   a. LCOM[1:0] start driving static LOW (F4RC01 – DA[1:0]).
7. Host can lock NVDIMM mode enable by setting F0RC0E – DA1 = 1 before the lockout time is started in the NVDIMM (i.e., within t_{MRD_L2} = 32 t_{CK} from the RCW Write command that sets Bit DA0 in F4RC00 to 1).
8. The Host controller writes register MODULE_OPS_CONFIG-Offset 0xAA bit3 in the NV local controller (through I^2C) to enable monitoring of LCOM[1:0] asynchronous interrupt signal.
9. Wait lockout time (1 sec) for NVDIMM internal initialization.
   a. The lockout time window starts t_{MRD_L2} = 32 t_{CK} after the RCW Write command that sets Bit DA0 in F4RC00 to 1.
   b. NV local controller allowed to drive LCOM[2:0] and LCK_t/LCK_c.
   c. No activity allowed on DRAM channel during the lockout window.
   d. No activity is allowed on the I^2C bus during the lockout window excepting for the command in Step 8 above.
10. Initiate normal operation. The Host can arm the NVC at this point.

2.25.2 Save Mode Entry Sequence

The recommended sequence to enter Save Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below. According to the Byte Addressable Energy Backed Interface specification, Save operations can be initiated through the SAVE_n pin or through certain control register bits in the NV local controller. The sequence shown below applies to all Save operations regardless of the method used to initiate them.

1. Host puts DRAMs in Self Refresh.
2. RCD tracks DRAM Self Refresh state associated with DCKE0 and DCKE1 in F4RC6x.
   a. NV controller puts active DRAM ranks in Self Refresh.
3. NV local controller enables local clock LCK, masks platform clock and C/A signals (F4RC00 – DA[2:1] = 11b).
   a. NVDIMM settings configured previously (during Initialization).
4. NV local controller waits for RCD/DB clocks to stabilize (t_{STAB} + t_{DLLK}).
5. NV controller adjusts RCD02/DB02 (and DRAM) settings if needed.
6. NV local controller saves DRAM data in Non-Volatile Memory (only for ranks that were found in Self Refresh).

---

1. This step is performed by the combination of F0RC4x, F0RC5x and F0RC6x writes to execute CMD 5 CW Write Operation since the F0RC07 command features only apply to the LCOM[2:0] interface.

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2.25.3 Save Mode Exit Sequence

The recommended sequence to exit Save Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. NV controller finishes saving DRAM data in Non-Volatile Memory.
2. NV controller restores RCD02/DB02 (and DRAM) settings it has modified (as needed).
3. NV controller puts active DRAMs in Self Refresh state.
4. NV controller gives RCD control back to the Host (F4RC00 – DA[2:1] = 00b).
5. NV controller drives LCKE Low and disables LCK_t/LCK_c and LCOM[2:0] drivers.

2.25.4 Restore Mode Entry Sequence

The recommended sequence to enter Restore Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. Host controller and NV local controller complete Steps 1 through 8 of Initialization Sequence.
   a. Optional period of normal operation (i.e., Restore operation can be requested by Host controller at any time and not always immediately after Initialization).
2. Host controller checks for presence of valid image.
3. If valid image is present Host controller requests Restore operation.
   a. NV controller assumes there is no valid data in DRAMs needing to be preserved.
   b. The Host shall not toggle DCKEn signal logic levels during the following three steps of this sequence.
   c. NV controller enables local clock LCK, masks platform clock and C/A signals (F4RC00 – DA[2:1] = 11b).
      1. NVDIMM settings configured previously (during Initialization).
   d. NV local controller waits for RCD/DB clocks to stabilize ($t_{STAB} + t_{DLLK}$).
   e. NV controller adjusts RCD02/DB02 (and DRAM) settings if needed.
   f. NV local controller restores data from non-volatile memory to DRAMs.

2.25.5 Restore Mode Exit Sequence

The recommended sequence to exit Restore Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. NV controller finishes restoring data from non-volatile memory to DRAMs.
2. NV controller restores RCD02/DB02 (and DRAM) settings it has modified (as needed).
3. NV controller puts active DRAMs in Self Refresh state.
4. NV controller disables local clock LCK, enables platform clock and C/A signals in RCD02 (F4RC00 – DA[2:1] = 00b).
   a. Host controller required to drive DCKEn signals Low at this time.
5. NV controller drives LCKE Low and disables LCK_t/LCK_c and LCOM[2:0] drivers.
6. Host controller initiates Erase procedure.
7. The Host controller is allowed to start normal operation.
   a. The Host can arm the NVC after meeting the maximum erase time specified in NVC registers.

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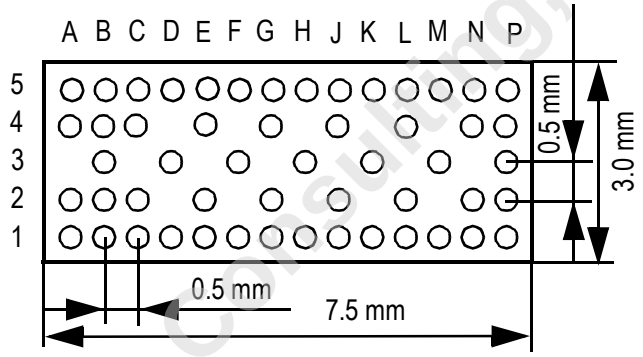
3 Mechanical Outline

Package options include a 53-ball Fine-Pitch BGA (FBGA) with 0.5mm ball pitch, 14 x 5 grid with 17 balls depopulated, 7.5mm x 3.0mm as defined in MO-276 (Issue J, Variation P7.5x3.0-KM-53M) or an alternate 56-ball Fine-Pitch BGA (FBGA) with 0.5 mm ball pitch, 15 x 5 grid with 19 balls depopulated, 8.0 mm x 3.0 mm as defined in MO-276 (Issue J, Variation P8.0x3.0-KM-56U). The device pinout options support the register link inputs on the left side columns to support easy signal routing to the DDR4 register. Corresponding host side data/strobe balls are placed in a way to match the corresponding pin location on the connector if the device is mounted on the backside of an LRDIMM on NVDIMM module. Each V_{DD} and V_{SS} is located close to an associated no ball position to allow low cost via technology combined with the small 0.5mm ball pitch.

3.1 14 x 5 Ball Configuration and Assignment



Ball diameter: 0.30 mm
Ball pitch: 0.5 mm x 0.5 mm

Figure 12 — 53 Ball Configuration 14 x5 (TOP VIEW)

Table 20 specifies the pinout for the DDR4DB02. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

Table 20 — Ball Assignment - 53-ball FBGA, 14 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
5	BCOM3	BCOM2	MDQ3	MDQ2	MDQ7	MDQ6	MDQS0_t	MDQS0_c	MDQS1_c	MDQS1_t	MDQ1	MDQ0	MDQ5	MDQ4
4	BCOM0	BCOM1	V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	ALERT_n
3		V_{DD}		V_{DD}		V_{DD}		V_{DD}		V_{DD}		V_{DD}		BVrefCA
2	BCK_t	BCKE	V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	ZQCAL
1	BCK_c	BODT	DQ3	DQ2	DQ7	DQ6	DQS0_t	DQS0_c	DQS1_c	DQS1_t	DQ1	DQ0	DQ5	DQ4

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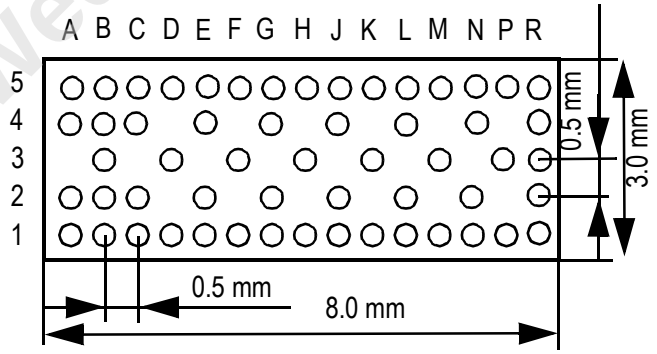
3.1.1 14 x 5 Terminal Functions

Table 21 — 14 x 5 Terminal functions

Signal Group	Signal Name	Type	Description
Data buffer control inputs	BODT	CMOS[1] V_{REF} based	Data buffer on-die termination signal
	BCKE	CMOS[1] V_{REF} based	Data buffer clock enable signal for data buffer power management
	BCOM[3:0]	CMOS[1] V_{REF} based	Register communication bus for data buffer programming and control access
Clock inputs	BCK_t, BCK_c	CMOS differential	Differential clock input pair
Host Interface	DQ[3:0] DQS0_t DQS0_c DQ[7:4] DQS1_t DQS1_c	CMOS bidirectional	Host side data lower nibble Host side data strobe for lower nibble Host side data strobe complement for lower nibble Host side data upper nibble Host side data strobe for upper nibble Host side data strobe complement for upper nibble
DRAM Interface	MDQ[3:0] MDQS0_t MDQS0_c MDQ[7:4] MDQS1_t MDQS1_c	CMOS bidirectional	DRAM side data lower nibble DRAM side data strobe for lower nibble DRAM side data strobe complement for lower nibble DRAM side data upper nibble DRAM side data strobe for upper nibble DRAM side data strobe complement for upper nibble
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the data buffer control bus inputs.
Miscellaneous pins	BVrefCA	$V_{DD}/2$	Input reference voltage for data buffer control bus receivers
	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration

1. These receivers use BVrefCA as the switching point reference

3.2 15 x 5 Alternate Package Ball Configuration and Assignments



Ball diameter: 0.30 mm

Ball pitch: 0.5 mm x 0.5 mm

Figure 13 — Alternate 56 Ball Configuration 15 x 5 (TOP VIEW)

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Table 22 specifies the alternate ballout for the DDR4DB02NV with the additional LDQS, LDQ0 and LDQ1 pins to support NVDIMM features[1].

Table 22 — Alternate Package Ball Assignments - 56 ball FBGA, 15 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
5	BCOM3	BCOM2	MDQ3	MDQ2	MDQ7	MDQ6	MDQS0_t	MDQS0_c	MDQS1_c	MDQS1_t	MDQ1	MDQ0	MDQ5	MDQ4	ALERT_n
4	BCOM0	BCOM1	V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		VSS
3		V_{DD}		V_{DD}		V_{DD}		V_{DD}		V_{DD}		V_{DD}		BVrefCA	LDQ1
2	BCK_t	BCKE	V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}		LDQ0
1	BCK_c	DQ3	DQ2	DQ7	DQ6	DQS0_t	DQS0_c	DQS1_c	DQS1_t	DQ1	DQ0	DQ5	DQ4	LDQS	ZQCAL

3.2.1 15 x 5 Terminal Functions

Table 23 — 15 x 5 Terminal functions

Signal Group	Signal Name	Type	Description
Data buffer control inputs	BCKE	CMOS[1] V_{REF} based	Data buffer clock enable signal for data buffer power management
	BCOM[3:0]	CMOS[1] V_{REF} based	Register communication bus for data buffer programming and control access
Data buffer Local Interface	LDQ[1:0]	CMOS bidirectional	Local controller data bits
	LDQS		Local controller data strobe for LDQ[1:0] data bits, single ended
Clock inputs	BCK_t, BCK_c	CMOS differential	Differential clock input pair
Host Interface	DQ[3:0] DQS0_t DQS0_c DQ[7:4] DQS1_t DQS1_c	CMOS bidirectional	Host side data lower nibble Host side data strobe for lower nibble Host side data strobe complement for lower nibble Host side data upper nibble Host side data strobe for upper nibble Host side data strobe complement for upper nibble
DRAM Interface	MDQ[3:0] MDQS0_t MDQS0_c MDQ[7:4] MDQS1_t MDQS1_c	CMOS bidirectional	DRAM side data lower nibble DRAM side data strobe for lower nibble DRAM side data strobe complement for lower nibble DRAM side data upper nibble DRAM side data strobe for upper nibble DRAM side data strobe complement for upper nibble
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the data buffer control bus inputs.
Miscellaneous pins	BVrefCA	$V_{DD}/2$	Input reference voltage for data buffer control bus receivers
	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration

1. These receivers use BVrefCA as the switching point reference

1.The alternate package and ballout are required only if optional NVDIMM features are supported.

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4 Data Buffer Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. Buffer control word (BCW) writes are sent to the DDR4 Data Buffer (DB) from the DDR4 Registering Clock Driver (RCD) as a command sequence through the buffer control bus (BCOM). Section 2.17 describes BCW write command sequences in detail. The different control words and settings are described in the following sections. Any change to the control words requires some time for the device to settle. For changes to the control word setting, the controller needs to wait t_{MRC} ($16t_{CK}$) after the last control word access before further access to the DRAM can take place. For any changes to the clock timing (including writes to BC0A/F0BC6x) this settling may take up to t_{DLLK} time. The command bus must be kept HIGH during that time (BCOM[3:0] = 1010 indicates idle, NOP, command).

The BCW space of the DB is divided into eight function spaces (F0 to F7). In F0 the DDR4 data buffer allocates decoding for 16 4-bit control words (BC00 through BC0F - see Table 24, “4-bit BCW Decoding”) and 15 8-bit control words (BC1x through BCFx). All buffer control words in F1 to F7 are 8-bit. Access to a given 4-bit control word is selected by bits DA4 through DA11 of the BCW write command sequence. The data bits to be written into the 4-bit control words are contained in bits DA0 through DA3 of the BCW write command sequence. Access to a given 8-bit control word (see Table 25, “8-bit BCW Decoding”) is selected by bits DA8 through DA11 of the BCW Write command sequence. The data bits to be written into the 8-bit control words are contained in bits DA0 through DA7 of the BCW command sequence.

For rank specific control words F0 is used for Rank 0, F1 is used for Rank 1, F2 is used for Rank 2 and F3 is used for Rank 3 (with the exception of the per bit lane control words which are in F4 to F7 for ranks 0 to 3 respectively).

During BCW Write commands, the BCKE data buffer input pin must be asserted high. If the CKE power down feature is disabled, the BCKE input is a don’t care (either HIGH or LOW). The BODT input can be either HIGH or LOW and is ignored by the data buffer for the purpose of BCW access. Control bus parity is checked during BCW write operations unless parity is disabled in the Parity Control Word. ALERT_n is asserted and the command is ignored if a parity error is detected.

Control word access must be possible in any valid frequency range in either of the two possible frequency bands.

All timing control words which are affected by a change in clock frequency need to be duplicated for the 2nd frequency context selected with BC0A, DA3.

4.1 BCW Decoding

The BCW write command sequence is initiated in the data buffer when the BCOM control bus code received at the DDR4 DB is equal to 1100b (BCOM[3:0]=1100). The BCW address and the settings are transmitted over bits DA[11:0] included in the BCW write command sequence in the six clock cycles immediately following the cycle when the 1100b BCOM command is captured. The BCW write command sequence uses one of the six data transfers just mentioned to transmit three function selection bits that select the function space targeted for that particular BCW write command. The reset default state of all control word bits (except vendor specific ones) is ‘0’. Every time the device is reset, its default state is restored. Stopping the clocks (BCK_t=BCK_c=LOW) to put the device in low-power mode will not alter the control word settings as long as BCKE is not HIGH while BCK_t and BCK_c are LOW.

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Table 24 — 4-bit BCW Decoding

BCW	FNC bits			Address Bit												Description
	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
BC00	0	0	0	0	0	0	0	0	0	0	0	setting[3:0]				Host Interface DQ RTT_NOM Control
BC01	0	0	0	0	0	0	0	0	0	0	1	setting[3:0]				Host Interface DQ RTT_WR Control
BC02	0	0	0	0	0	0	0	0	0	1	0	setting[3:0]				Host Interface DQ RTT_PARK Control
BC03	0	0	0	0	0	0	0	0	0	1	1	setting[3:0]				Host Interface DQ Driver Control Word
BC04	0	0	0	0	0	0	0	0	1	0	0	setting[3:0]				DRAM Interface MDQ RTT Control Word
BC05	0	0	0	0	0	0	0	0	1	0	1	setting[3:0]				DRAM Interface MDQ Driver Control Word
BC06	0	0	0	0	0	0	0	0	1	1	0	command[3:0]				Command Space Control Word
BC07	0	0	0	0	0	0	0	0	1	1	1	setting[3:0]				Rank Presence Control Word
BC08	0	0	0	0	0	0	0	1	0	0	0	setting[3:0]				Rank Selection Control Word
BC09	0	0	0	0	0	0	0	1	0	0	1	setting[3:0]				Power Saving Settings Control Word
BC0A	0	0	0	0	0	0	0	1	0	1	0	setting[3:0]				LRDIMM Operating Speed
BC0B	0	0	0	0	0	0	0	1	0	1	1	setting[3:0]				Operating Voltage and Host Side Output Slew Rate Control Word
BC0C	0	0	0	0	0	0	0	1	1	0	0	setting[3:0]				Buffer Training Mode Control Word
BC0D	0	0	0	0	0	0	0	1	1	0	1	setting[3:0]				LDQ Operation Control Word
BC0E	0	0	0	0	0	0	0	1	1	1	0	setting[3:0]				Parity Control Word
BC0F	0	0	0	0	0	0	0	1	1	1	1	setting[3:0]				Error Status Word

Table 25 — 8-bit BCW Decoding

BCW	FNC bits			Address Bit												Description
	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
F[7:0]BC7x	x	x	x	0	1	1	1	setting [7:0]								Function Space Selector Control Word
F0BC1x	0	0	0	0	0	0	1	setting[7:0]								Buffer Configuration Control Word
F0BC6x	0	0	0	0	1	1	0	setting[7:0]								Fine Granularity Frequency Operating Speed Control Word
F0BCCx	0	0	0	1	1	0	0	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0
F0BCDx	0	0	0	1	1	0	1	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0
F0BCEx	0	0	0	1	1	1	0	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2
F0BCFx	0	0	0	1	1	1	1	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2
F1BC1x	0	0	1	0	0	0	1	setting[7:0]								LDQ Configuration Control Word
F1BCCx	0	0	1	1	1	0	0	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1
F1BCDx	0	0	1	1	1	0	1	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1
F1BCEx	0	0	1	1	1	1	0	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3
F1BCFx	0	0	1	1	1	1	1	setting[7:0]								Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3
F2BC1x	0	1	0	0	0	0	1	setting[7:0]								LDQ Interface VREF Control Word
F2BCEx	0	1	0	1	1	1	0	setting[7:0]								Host Interface DFE Programming Control Word
F2BCFx	0	1	0	1	1	1	1	setting[7:0]								Host Interface DQ[7:0] Receiver DFE Gain Adjustment Control Word

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Table 25 — 8-bit BCW Decoding

BCW	FNC bits			Address Bit												Description
	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
F3BC1x	0	1	1	0	0	0	1	setting[7:0]								LDQ Interface Driver, ODT Control
F3BCCx	0	1	1	1	1	0	0	setting[7:0]								Host Interface DQ[7:0] Receiver DFE Tap 1 Coefficient Control Word
F3BCDx	0	1	1	1	1	0	1	setting[7:0]								Host Interface DQ[7:0] Receiver DFE Tap 2 Coefficient Control Word
F3BCEx	0	1	1	1	1	1	0	setting[7:0]								Host Interface DQ[7:0] Receiver DFE Tap 3 Coefficient Control Word
F3BCFx	0	1	1	1	1	1	1	setting[7:0]								Host Interface DQ[7:0] Receiver DFE Tap 4 Coefficient Control Word
F[3:0]BC2x	0	x	x	0	0	1	0	setting[7:0]								Lower Nibble DRAM Interface Receive Enable Training Control Word for Ranks 0 to 3
F[3:0]BC3x	0	x	x	0	0	1	1	setting[7:0]								Upper Nibble DRAM Interface Receive Enable Training Control Word for Ranks 0 to 3
F[3:0]BC4x	0	x	x	0	1	0	0	setting[7:0]								Lower Nibble MDQS Read Delay Control Word for Ranks 0 to 3
F[3:0]BC5x	0	x	x	0	1	0	1	setting[7:0]								Upper Nibble MDQS Read Delay Control Word for Ranks 0 to 3
F[3:0]BC8x	0	x	x	1	0	0	0	setting[7:0]								Lower Nibble MDQ-MDQS Write Delay Control Word for Ranks 0 to 3
F[3:0]BC9x	0	x	x	1	0	0	1	setting[7:0]								Upper Nibble MDQ-MDQS Write Delay Control Word for Ranks 0 to 3
F[3:0]BCAx	0	x	x	1	0	1	0	setting[7:0]								Lower Nibble DRAM Interface Write Leveling Control Word for Ranks 0 to 3
F[3:0]BCBx	0	x	x	1	0	1	1	setting[7:0]								Upper Nibble DRAM Interface Write Leveling Control Word for Ranks 0 to 3

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Table 25 — 8-bit BCW Decoding

BCW	FNC bits			Address Bit												Description
	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
F4BC0x	1	0	0	0	0	0	0	setting[7:0]								MRS0 Snooped Settings
F4BC1x	1	0	0	0	0	0	1	setting[7:0]								MRS1 Snooped Settings
F4BC2x	1	0	0	0	0	1	0	setting[7:0]								MRS2 Snooped Settings
F4BC3x	1	0	0	0	0	1	1	setting[7:0]								MRS3 Snooped Settings
F4BC4x	1	0	0	0	1	0	0	setting[7:0]								MRS4 Snooped Settings
F4BC5x	1	0	0	0	1	0	1	setting[7:0]								MRS5 Snooped Settings
F4BC6x	1	0	0	0	1	1	0	setting[7:0]								MRS6 Snooped Settings
F5BC0x = MPR0	1	0	1	0	0	0	0	setting[7:0]								Upper & Lower MPR bits [7:0] for UI0
F5BC1x = MPR1	1	0	1	0	0	0	1	setting[7:0]								Upper & Lower MPR bits [15:8] for UI1
F5BC2x = MPR2	1	0	1	0	0	1	0	setting[7:0]								Upper & Lower MPR bits [23:16] for UI2
F5BC3x = MPR3	1	0	1	0	0	1	1	setting[7:0]								Upper & Lower MPR bits [31:24] for UI3
F5BC4x	1	0	1	0	1	0	0	setting[7:0]								Reserved
F5BC5x	1	0	1	0	1	0	1	setting[7:0]								Host Interface Vref Control Word
F5BC6x	1	0	1	0	1	1	0	setting[7:0]								DRAM Interface Vref Control Word (& Host DFE_VREF for Training)
F6BC0x = MPR4	1	1	0	0	0	0	0	setting[7:0]								Upper & Lower MPR bits [39:32] for UI4
F6BC1x = MPR5	1	1	0	0	0	0	1	setting[7:0]								Upper & Lower MPR bits [47:40] for UI5
F6BC2x = MPR6	1	1	0	0	0	1	0	setting[7:0]								Upper & Lower MPR bits [55:48] for UI6
F6BC3x = MPR7	1	1	0	0	0	1	1	setting[7:0]								Upper & Lower MPR bits [63:56] for UI7
F6BC4x	1	1	0	0	1	0	0	setting[7:0]								Buffer Training Configuration Control Word
F6BC5x	1	1	0	0	1	0	1	setting[7:0]								Buffer Training Status Word
F7BC0x ..C3x	1	1	1	0	0	x	x	setting[7:0]								Error Log Registers
F[7:4]BC8x	1	x	x	1	0	0	0	setting[7:0]								MDQ0/4-Read Delay Control Word for Ranks 0 to 3
F[7:4]BC9x	1	x	x	1	0	0	1	setting[7:0]								MDQ1/5-Read Delay Control Word for Ranks 0 to 3
F[7:4]BCAx	1	x	x	1	0	1	0	setting[7:0]								MDQ2/6-Read Delay Control Word for Ranks 0 to 3
F[7:4]BCBx	1	x	x	1	0	1	1	setting[7:0]								MDQ3/7-Read Delay Control Word for Ranks 0 to 3
F[7:4]BCCx	1	x	x	1	1	0	0	setting[7:0]								MDQ0/4-MDQS Write Delay Control Word for Ranks 0 to 3
F[7:4]BCDx	1	x	x	1	1	0	1	setting[7:0]								MDQ1/5-MDQS Write Delay Control Word for Ranks 0 to 3
F[7:4]BCEx	1	x	x	1	1	1	0	setting[7:0]								MDQ2/6-MDQS.Write Delay Control Word for Ranks 0 to 3
F[7:4]BCFx	1	x	x	1	1	1	1	setting[7:0]								MDQ3/7-MDQS Write Delay Control Word for Ranks 0 to 3

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4.2 BC00 - Host Interface DQ RTT_NOM Termination Control Word

Table 26 — BC00: Host Interface DQ RTT_NOM Termination Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	RTT_NOM	RTT_NOM disabled
x	0	0	1		RZQ/4 (60 Ω)
x	0	1	0		RZQ/2 (120 Ω)
x	0	1	1		RZQ/6 (40 Ω)
x	1	0	0		RZQ/1 (240 Ω)
x	1	0	1		RZQ/5 (48 Ω)
x	1	1	0		RZQ/3 (80 Ω)
x	1	1	1		RZQ/7 (34 Ω)
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

4.3 BC01 - Host Interface DQ RTT_WR Termination Control Word

Table 27 — BC01: Host Interface DQ RTT_WR Termination Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	RTT_WR	Dynamic ODT Off
x	0	0	1		RZQ/4 (60 Ω)
x	0	1	0		RZQ/2 (120 Ω)
x	0	1	1		Reserved
x	1	0	0		RZQ/1 (240 Ω)
x	1	0	1		Reserved
x	1	1	0		RZQ/3 (80 Ω)
x	1	1	1		Hi-Z
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

4.4 BC02 - Host Interface DQ RTT_PARK Termination Control Word

Table 28 — BC02: Host Interface DQ RTT_PARK Termination Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	RTT_PARK	RTT_PARK disabled
x	0	0	1		RZQ/4 (60 Ω)
x	0	1	0		RZQ/2 (120 Ω)
x	0	1	1		RZQ/6 (40 Ω)
x	1	0	0		RZQ/1 (240 Ω)
x	1	0	1		RZQ/5 (48 Ω)
x	1	1	0		RZQ/3 (80 Ω)
x	1	1	1		RZQ/7 (34 Ω)
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

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4.5 BC03 - Host Interface DQ Driver Control Word

Table 29 — BC03: Host Interface DQ Driver Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Host Interface DQ/DQS Output Driver Impedance control	RZQ/6 (40 Ω)
x	0	0	1		RZQ/7 (34 Ω)
x	0	1	0		RZQ/5 (48 Ω)
x	0	1	1		RZQ/8 (30 Ω)
x	1	0	0		Reserved
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Reserved
0	x	x	x	Host Interface DQ/DQS Driver Disable	Host interface DQ/DQS drivers enabled
1	x	x	x		Host interface DQ/DQS drivers disabled

4.6 BC04 - DRAM Interface MDQ Termination Control Word

Table 30 — BC04: DRAM Interface MDQ Termination Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	DRAM Interface MDQ/MDQS ODT Strength for Data Buffer	DRAM interface ODT disabled
x	0	0	1		RZQ/4 (60 Ω)
x	0	1	0		RZQ/2 (120 Ω)
x	0	1	1		RZQ/6 (40 Ω)
x	1	0	0		RZQ/1 (240 Ω)
x	1	0	1		RZQ/5 (48 Ω)
x	1	1	0		RZQ/3 (80 Ω)
x	1	1	1		RZQ/7 (34 Ω)
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

4.7 BC05 - DRAM Interface MDQ Driver Control Word

Table 31 — BC05: DRAM Interface MDQ Driver Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	DRAM Interface MDQ/MDQS Output Driver Impedance control	RZQ/6 (40 Ω)
x	0	0	1		RZQ/7 (34 Ω)
x	0	1	0		RZQ/5 (48 Ω)
x	0	1	1		Reserved
x	1	0	0		Reserved
x	1	0	1		RZQ/4 (60 Ω)
x	1	1	0		Reserved
x	1	1	1		Reserved
0	x	x	x	DRAM Interface MDQ/MDQS Driver Disable	DRAM interface MDQ/MDQS drivers enabled
1	x	x	x		DRAM interface MDQ/MDQS drivers disabled

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4.8 BC06 - Command Space Control Word

After issuing a data buffer command via writes to BC06 waiting for t_{MRC}(16 t_{CK}) is required before the next DRAM command or BCW write can be issued.

Table 32 — BC06: Command Space Control Word

Cmd (DA[3:0])				Command No	Command Name	Result
0	0	0	0	CMD 0	Reset DLL	Reset clock DLL circuits.
0	0	0	1	CMD 1	ZQCL	Perform long I/O calibration command.
0	0	1	0	CMD 2	ZQCS	Perform short I/O calibration command.
0	0	1	1	CMD 3	Clear Error Status	Clear parity/sequence error status and re-enable parity and command sequence error checking
0	1	0	0	CMD 4	Soft Reset	Clears all internal registers and DLL. Self Clear in the next cycle.
0	1	0	1	CMD 5	Reserved	Reserved for future use
0	1	1	0	CMD 6	Reserved	Reserved for future use
0	1	1	1	CMD 7	Reserved	Reserved for future use
1	x	x	x	CMD 8-15	Reserved	Reserved for future use

4.9 BC07 - Rank Presence Control Word

This control word contains the number of package rank used on an LRDIMM. The host controller will write BC07 DA[3:0] to indicate which package ranks are used on the LRDIMM so that the DDR4DB02 can power down unnecessary logic for unused package ranks.

Table 33 — BC07: Rank Presence Control Word

Cmd (DA[3:0])				Definition	Encoding
x	x	x	0	Package Rank 0 Disable	Enabled
x	x	x	1		Disabled
x	x	0	x	Package Rank 1 Disable	Enabled
x	x	1	x		Disabled
x	0	x	x	Package Rank 2 Disable	Enabled
x	1	x	x		Disabled
0	x	x	x	Package Rank 3 Disable	Enabled
1	x	x	x		Disabled

4.10 BC08 - Rank Number & Selection Control Word

During Write Leveling the DB needs to know which package rank is being write leveled. The host is required to program bits DA[1:0] with this information prior to putting the DB into the DRAM Interface or the Host Interface Write Leveling training modes.

Table 34 — BC08: Rank Number & Selection Control Word

Cmd (DA[3:0])				Definition	Encoding
x	x	0	0	Package Rank selected for Write Leveling	Package Rank 0
x	x	0	1		Package Rank 1
x	x	1	0		Package Rank 2
x	x	1	1		Package Rank 3
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

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4.11 BC09 - Power Saving Settings Control Word

Table 35 — BC09: Power Saving Settings Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Reserved	Reserved
x	x	x	1		
x	x	0	x	Reserved	Reserved
x	x	1	x		
x	0	x	x	CKE Power Down Mode[1]	CKE power down with ODT ON, connector interface RTT is a function of BODT
x	1	x	x		CKE power down with ODT off, connector interface RTT is disabled and BODT input receiver is disabled.[2]
0	x	x	x	CKE Power Down Mode Enable[3]	Disabled
1	x	x	x		Enabled

1. The data buffer ignores CKE Power Down mode setting when CKE Power Down is disabled by BC09 - DA3.
2. If CKE power down mode is enabled in BC09 - DA3, it is legal for the BODT input signal to be floated, when CKE power down mode is invoked once BCKE is LOW.
3. CKE power down is invoked once BCKE is LOW.

4.12 BC0A - LRDIMM Operating Speed

Table 36 — BC0A: LRDIMM Operating Speed[1]

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	f ≤ 1600 MT/s	DDR4-1600
x	0	0	1	1600 MT/s < f ≤ 1867 MT/s	DDR4-1866
x	0	1	0	1867 MT/s < f ≤ 2134 MT/s	DDR4-2133
x	0	1	1	2134 MT/s < f ≤ 2400 MT/s	DDR4-2400
x	1	0	0	2400 MT/s < f ≤ 2667 MT/s	DDR4-2666
x	1	0	1	2667 MT/s < f ≤ 2933 MT/s	DDR4-2933
x	1	1	0	2933 MT/s < f ≤ 3200 MT/s	DDR4-3200
x	1	1	1	280 MT/s ≤ f < 1250 MT/s	Test frequency range[2]
0	x	x	x	Context for operation training	Default; Context 1 operation
1	x	x	x		Context 2 operation

1. The encoding value is used to inform the data buffer the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a data buffer can run.
2. Only transparent mode is supported in the test frequency range.

The following control words need to be duplicated to support dual frequency context switching:

BC00 DA[2:0]
BC01 DA[2:0]
BC02 DA[2:0]
BC03 DA[2:0]
BC04 DA[2:0]
BC05 DA[2:0]
BC0B DA0
F0BCCx DA[6:0]
F0BCDx DA[6:0]
F0BCEx DA[6:0]
F0BCFx DA[6:0]
F1BCCx DA[6:0]
F1BCDx DA[6:0]
F1BCEx DA[6:0]
F1BCFx DA[6:0]

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F[3:0]BC2x DA[5:0]
F[3:0]BC3x DA[5:0]
F[3:0]BC4x DA[4:0]
F[3:0]BC5x DA[4:0]
F[3:0]BC8x DA[4:0]
F[3:0]BC9x DA[4:0]
F[3:0]BCAx DA[5:0]
F[3:0]BCBx DA[5:0]

F5BC5x (all bits)
F5BC6x (all bits)
F6BC4x DA[2:1]
F[7:4]BC8x DA[6:4], DA[2:0]
F[7:4]BC9x DA[6:4], DA[2:0]
F[7:4]BCAx DA[6:4], DA[2:0]
F[7:4]BCBx DA[6:4], DA[2:0]
F[7:4]BCCx DA[6:4], DA[2:0]
F[7:4]BCDx DA[6:4], DA[2:0]
F[7:4]BCEx DA[6:4], DA[2:0]
F[7:4]BCFx DA[6:4], DA[2:0]

4.13 BC0B - Operating Voltage and Host Side Output Slew Rate Control Word

Table 37 — BC0B: Operating Voltage and Host Side Output Slew Rate Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Buffer V_{DD} Operating Voltage[1]	1.2 V
x	x	x	1		Reserved
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
0	0	x	x	Host DQS / DQ Output Slew Rate Control Range Settings[2]	Moderate (DQ Single-ended 5 V/ns - 7 V/ns) (DQS Differential 10 V/ns - 14 V/ns)
0	1	x	x		Strong (DQ Single-ended 6 V/ns - 8 V/ns) (DQS Differential 12 V/ns - 16 V/ns)
1	0	x	x		Very Strong (DQ Single-ended 7 V/ns - 9 V/ns) (DQS Differential 14 V/ns - 18 V/ns)
1	1	x	x		Light (DQ Single-ended 4 V/ns - 6 V/ns) (DQS Differential 8 V/ns - 12 V/ns)

1. BC0B bit DA[0] will be used to inform DDR4DB02 under what operating voltage V_{DD} it will be operating. The Data Buffer can use the information to optimize functionality and performance at voltage conditions.
2. Slew Rate Control Range functionality applies to all driver strength settings. The base range values specified in Table 37 are applicable for Ron = RZQ/7, V_{DD} = 1.2 V and 25 ^{o}C.

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4.14 BC0C - Buffer Training Control Word

Table 38 — BC0C: Buffer Training Mode Control Word

Setting (DA[3:0])				Mode Name	Function
0	0	0	0	Normal operation	Exit any of the training mode
0	0	0	1	DRAM Interface Receive Enable Phase (MREP) Training mode	MDQS receive enable phase training
0	0	1	0	Reserved	Reserved
0	0	1	1	Reserved	Reserved
0	1	0	0	DRAM Write Leveling (DWL) mode	Write level from DB to DRAM
0	1	0	1	Host Interface Write Leveling (HWL) mode	Write level from Host to data buffer
0	1	1	0	MDQS Read Delay (MRD) Training mode	DRAM interface MDQS read delay training
0	1	1	1	MDQ-MDQS Write Delay (MWD) Training mode	DRAM interface MDQ-MDQS write delay training
1	0	0	0	Host Interface Write (HIW) Training mode	Compares expected data with MPRs and provides result in training status control word
1	0	0		Reserved	Reserved
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

4.15 BC0D - LDQ Operation Control Word

This register is used by the Non Volatile controller (NVC) to change the mode of operation of the DDR4DB02.

Table 39 — BC0D: LDQ Operation Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	**LDQ Port Control**	LDQ port disabled, normal operation
x	x	0	1		LDQ enabled, input mode (RESTORE)
x	x	1	0		LDQ enabled, output mode (SAVE)
x	x	1	1		Reserved
0	0	x	x	**Save and restore frequency context select**[1]	NVC operation uses context 1[2]
0	1	x	x		NVC operation uses context 2[3]
1	0	x	x		Reserved
1	1	x	x		NVC operation uses current context[4]

1. Valid only when BC0D DA[1:0] = 01 or 10
2. Overrides setting of BC0A DA3 without modifying BC0A. DDR4DB02 functions as defined for BC0A DA3 = 0
3. Overrides setting of BC0A DA3 without modifying BC0A. DDR4DB02 functions as defined for BC0A DA3 = 1
4. Setting in BC0A is used for SAVE or RESTORE operations

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4.16 BC0E - Parity and Sequence Error Control Word

Table 40 — BC0E: Parity and Sequence Error Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Parity Checking Enable	Parity checking disabled[1]
x	x	x	1		Parity checking enabled
x	x	0	x	Sequence Checking Enable	Sequence checking disabled
x	x	1	x		Sequence checking enabled
x	0	x	x	ALERT_n Assertion[2]	ALERT_n stays asserted until Clear Error Status command has been sent.
x	1	x	x		ALERT_n pulse width according to Table 41
0	x	x	x	ALERT_n Re-enable[3]	Parity and sequence error checking remains disabled after ALERT_n pulse
1	x	x	x		Parity and sequence error checking is re-enabled after ALERT_n pulse

1. Data buffer does not check for parity including control word programming.
2. This bit affects ALERT_n assertion that is a result of a parity error or a sequence error.
3. Parity Error and Sequence Error bits in Error Status Word (BC0F) remain set until cleared by sending a 'Clear Error Status' command.

Table 41 — ALERT_n Pulse Width[1]

DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
48	96	56	112	64	128	72	144	80	160	88	176	96	192	nCK

1. Table 41 defines the ALERT_n Pulse Width for tPAR_ALERT_PW and tSEQ_ALERT_PW.

4.17 BC0F - Error Status Word

Table 42 — BC0F: Error Status Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Parity Error bit[1]	No parity error detected
x	x	x	1		Parity error detected[2]
x	x	0	x	Sequence Error bit[1]	No Sequence error detected
x	x	1	x		Sequence error deteted[2]
x	0	x	x	> 1 Error[1]	Less than one error has occurred since the error status has been cleared
x	1	x	x		More than one error has occurred since the error status has been cleared
0	x	x	x	Pass/Fail information from 64-bit data comparator	Fail, i.e. one or more bits were not matched
1	x	x	x		Pass, i.e. no data mismatches among all 64 bits

1. These bits are read-only and will get reset to '0' by a 'Clear Error Status' command
2. Detailed error information is available in the Error Log Register at F7BC0x .. F7BC3x

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4.18 F[7:0]BC7x - Function Space Selector Control Word

This control word hold the currently selected function space. All BCW Write commands that have the function space bits = 000 in DAT4 use the content of the Function Space Selector control word when decoding the full BCW address. It is optional for the BCW Read commands that have the function space bits = 000 in DAT3 to use the content of the Function Space Selector control word when decoding the full BCW address. When a non-zero function space is present in the BCW Read or Write command, it has precedence over the content of the Function Space Selector control word. Note that this control word should only be used during initialization and training and should be reset to '000' before normal operation starts. Otherwise writes to the Command Space control word (BC06) which is located in function space 0 (e.g. ZQCL or ZQCS commands snooped and forwarded by the DDR4RCD02) will not find their intended target

Table 43 — F[7:0]BC7x: Function Space Selector Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Currently Selected Function Space	Function Space 0
x	x	x	x	x	0	0	1		Function Space 1
x	x	x	x	x	0	1	0		Function Space 2
x	x	x	x	x	0	1	1		Function Space 3
x	x	x	x	x	1	0	0		Function Space 4
x	x	x	x	x	1	0	1		Function Space 5
x	x	x	x	x	1	1	0		Function Space 6
x	x	x	x	x	1	1	1		Function Space 7

4.19 F0BC1x - Buffer Configuration Control Word

This control word contains data buffer mode information that does not come from snooping of DRAM MRS commands.

Table 44 — F0BC1x: Buffer Configuration Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	Per Buffer Addressability (PBA) Mode Enable	PBA mode disabled
x	x	x	x	x	x	x	1		PBA mode enabled
x	x	x	x	x	x	0	x	MPR Override Mode Enable	MPR override mode disabled
x	x	x	x	x	x	1	x		MPR override mode enable
x	x	x	x	x	0	x	x	Per DRAM Addressability (PDA) Mode Enable	PDA mode disabled
x	x	x	x	x	1	x	x		PDA mode enabled
x	x	x	x	0	x	x	x	One Rank Timing Mode	One Rank Timing mode disabled
x	x	x	x	1	x	x	x		One Rank Timing mode enabled[1]
x	x	x	0	x	x	x	x	Read Preamble Training Mode Enable	Read preamble training mode feature disabled.
x	x	x	1	x	x	x	x		Read preamble training mode feature enabled.
x	x	0	x	x	x	x	x	Transparent Mode Enable	Transparent mode disabled
x	x	1	x	x	x	x	x		Transparent mode enabled
x	0	x	x	x	x	x	x	BODT input handling in Transparent Mode	BODT input disabled in Transparent Mode
x	1	x	x	x	x	x	x		BODT input enabled in Transparent Mode
0	x	x	x	x	x	x	x	Package Rank Timing Alignment Enable	Disabled[2]
1	x	x	x	x	x	x	x		Enabled[3]

1. Package Rank Timing Alignment mode must be disabled F0BC1x DA7=0, prior to enabling One Rank Timing mode.
2. DDR4DB02 presents different DQS timing to host for each package rank for RD operation. For WR operation, host presents un-aligned DQS timing to DDR4DB02 for each package rank as trained.
3. DDR4DB02 presents an aligned timing to host for all package ranks for RD operation (=tPDM_RD_RA). For WR operation, host presents the same identical DQS timing to DDR4DB02 for all package ranks (=tPDM_WR_RA). There are limits on how much rank-to-rank timing alignment the DDR4DB02 can provides- see tPDM_RD_RA and tPDM_WR_RA specifications in Electrical and Timing chapter.

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4.20 F0BC6x - Fine Granularity LRDIMM Operating Speed

Table 45 — F0BC6x: Fine Granularity LRDIMM Operating Speed[1]

Setting (DA[7:0])								Definition	Encoding[2]
x	0	0	0	0	0	0	0	Fine Granularity Operating Speed[3,4]	1240 MT/s < f ≤ 1260 MT/s
x	0	0	0	0	0	0	1		1260 MT/s < f ≤ 1280 MT/s
x	0	0	0	0	0	1	0		1280 MT/s < f ≤ 1300 MT/s
x	0	0	0	0	0	1	1		1300 MT/s < f ≤ 1320 MT/s
x	0	0	0	0	1	0	0		1320 MT/s < f ≤ 1340 MT/s
x	0	0	0	0	1	0	1		1340 MT/s < f ≤ 1360 MT/s
x	0	0	0	0	1	1	0		1360 MT/s < f ≤ 1380 MT/s
x	0	0	0	0	1	1	1		1380 MT/s < f ≤ 1400 MT/s
x	0	0	0	1	0	0	0		1400 MT/s < f ≤ 1420 MT/s
x	0	0	0	1	0	0	1		1420 MT/s < f ≤ 1440 MT/s
x	0	0	0	1	0	1	0		1440 MT/s < f ≤ 1460 MT/s
x	0	0	0	1	0	1	1		1460 MT/s < f ≤ 1480 MT/s
x	0	0	0	1	1	0	0		1480 MT/s < f ≤ 1500 MT/s
x	0	0	0	1	1	0	1		1500 MT/s < f ≤ 1520 MT/s
x	0	0	0	1	1	1	0		1520 MT/s < f ≤ 1540 MT/s
x	0	0	0	1	1	1	1		1540 MT/s < f ≤ 1560 MT/s
x	0	0	1	0	0	0	0		1560 MT/s < f ≤ 1580 MT/s
x	0	0	1	0	0	0	1		1580 MT/s < f ≤ 1600 MT/s
x	0	0	1	0	0	1	0		1600 MT/s < f ≤ 1620 MT/s
x	0	0	1	0	0	1	1		1620 MT/s < f ≤ 1640 MT/s
x	0	0	1	0	1	0	0		1640 MT/s < f ≤ 1660 MT/s
x	0	0	1	0	1	0	1		1660 MT/s < f ≤ 1680 MT/s
x	0	0	1	0	1	1	0		1680 MT/s < f ≤ 1700 MT/s
x	0	0	1	0	1	1	1		1700 MT/s < f ≤ 1720 MT/s
x	0	0	1	1	0	0	0		1720 MT/s < f ≤ 1740 MT/s
x	0	0	1	1	0	0	1		1740 MT/s < f ≤ 1760 MT/s
x	0	0	1	1	0	1	0		1760 MT/s < f ≤ 1780 MT/s
x	0	0	1	1	0	1	1		1780 MT/s < f ≤ 1800 MT/s
x	0	0	1	1	1	0	0		1800 MT/s < f ≤ 1820 MT/s
x	0	0	1	1	1	0	1		1820 MT/s < f ≤ 1840 MT/s
x	0	0	1	1	1	1	0		1840 MT/s < f ≤ 1860 MT/s
x	0	0	1	1	1	1	1		1860 MT/s < f ≤ 1880 MT/s
x	0	1	0	0	0	0	0		1880 MT/s < f ≤ 1900 MT/s
x	0	1	0	0	0	0	1		1900 MT/s < f ≤ 1920 MT/s
x	0	1	0	0	0	1	0		1920 MT/s < f ≤ 1940 MT/s
x	0	1	0	0	0	1	1		1940 MT/s < f ≤ 1960 MT/s
x	0	1	0	0	1	0	0		1960 MT/s < f ≤ 1980 MT/s
x	0	1	0	0	1	0	1		1980 MT/s < f ≤ 2000 MT/s
x	0	1	0	0	1	1	0		2000 MT/s < f ≤ 2020 MT/s
x	0	1	0	0	1	1	1		2020 MT/s < f ≤ 2040 MT/s
x	0	1	0	1	0	0	0		2040 MT/s < f ≤ 2060 MT/s
x	0	1	0	1	0	0	1		2060 MT/s < f ≤ 2080 MT/s
x	0	1	0	1	0	1	0		2080 MT/s < f ≤ 2100 MT/s
x	0	1	0	1	0	1	1		2100 MT/s < f ≤ 2120 MT/s
x	0	1	0	1	1	0	0		2120 MT/s < f ≤ 2140 MT/s

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4.20 F0BC6x - Fine Granularity LRDIMM Operating Speed

Table 45 — F0BC6x: Fine Granularity LRDIMM Operating Speed[1]

Setting (DA[7:0])								Definition	Encoding[2]
x	0	1	0	1	1	0	1		2140 MT/s < f ≤ 2160 MT/s
x	0	1	0	1	1	1	0		2160 MT/s < f ≤ 2180 MT/s
x	0	1	0	1	1	1	1		2180 MT/s < f ≤ 2200 MT/s
x	0	1	1	0	0	0	0		2200 MT/s < f ≤ 2220 MT/s
x	0	1	1	0	0	0	1		2220 MT/s < f ≤ 2240 MT/s
x	0	1	1	0	0	1	0		2240 MT/s < f ≤ 2260 MT/s
x	0	1	1	0	0	1	1		2260 MT/s < f ≤ 2280 MT/s
x	0	1	1	0	1	0	0		2280 MT/s < f ≤ 2300 MT/s
x	0	1	1	0	1	0	1		2300 MT/s < f ≤ 2320 MT/s
x	0	1	1	0	1	1	0		2320 MT/s < f ≤ 2340 MT/s
x	0	1	1	0	1	1	1		2340 MT/s < f ≤ 2360 MT/s
x	0	1	1	1	0	0	0		2360 MT/s < f ≤ 2380 MT/s
x	0	1	1	1	0	0	1		2380 MT/s < f ≤ 2400 MT/s
x	0	1	1	1	0	1	0		2400 MT/s < f ≤ 2420 MT/s
x	0	1	1	1	0	1	1		2420 MT/s < f ≤ 2440 MT/s
x	0	1	1	1	1	0	0		2440 MT/s < f ≤ 2460 MT/s
x	0	1	1	1	1	0	1		2460 MT/s < f ≤ 2480 MT/s
x	0	1	1	1	1	1	0		2480 MT/s < f ≤ 2500 MT/s
x	0	1	1	1	1	1	1		2500 MT/s < f ≤ 2520 MT/s
x	1	0	0	0	0	0	0		2520 MT/s < f ≤ 2540 MT/s
x	1	0	0	0	0	0	1		2540 MT/s < f ≤ 2560 MT/s
x	1	0	0	0	0	1	0		2560 MT/s < f ≤ 2580 MT/s
x	1	0	0	0	0	1	1		2580 MT/s < f ≤ 2600 MT/s
x	1	0	0	0	1	0	0		2600 MT/s < f ≤ 2620 MT/s
x	1	0	0	0	1	0	1		2620 MT/s < f ≤ 2640 MT/s
x	1	0	0	0	1	1	0		2640 MT/s < f ≤ 2660 MT/s
x	1	0	0	0	1	1	1		2660 MT/s < f ≤ 2680 MT/s
x	1	0	0	1	0	0	0		2680 MT/s < f ≤ 2700 MT/s
x	1	0	0	1	0	0	1		2700 MT/s < f ≤ 2720 MT/s
x	1	0	0	1	0	1	0		2720 MT/s < f ≤ 2740 MT/s
x	1	0	0	1	0	1	1		2740 MT/s < f ≤ 2760 MT/s
x	1	0	0	1	1	0	0		2760 MT/s < f ≤ 2780 MT/s
x	1	0	0	1	1	0	1		2780 MT/s < f ≤ 2800 MT/s
x	1	0	0	1	1	1	0		2800 MT/s < f ≤ 2820 MT/s
x	1	0	0	1	1	1	1		2820 MT/s < f ≤ 2840 MT/s
x	1	0	1	0	0	0	0		2840 MT/s < f ≤ 2860 MT/s
x	1	0	1	0	0	0	1		2860 MT/s < f ≤ 2880 MT/s
x	1	0	1	0	0	1	0		2880 MT/s < f ≤ 2900 MT/s
x	1	0	1	0	0	1	1		2900 MT/s < f ≤ 2920 MT/s
x	1	0	1	0	1	0	0		2920 MT/s < f ≤ 2940 MT/s
x	1	0	1	0	1	0	1		2940 MT/s < f ≤ 2960 MT/s
x	1	0	1	0	1	1	0		2960 MT/s < f ≤ 2980 MT/s
x	1	0	1	0	1	1	1		2980 MT/s < f ≤ 3000 MT/s
x	1	0	1	1	0	0	0		3000 MT/s < f ≤ 3020 MT/s
x	1	0	1	1	0	0	1		3020 MT/s < f ≤ 3040 MT/s
x	1	0	1	1	0	1	0		3040 MT/s < f ≤ 3060 MT/s
x	1	0	1	1	0	1	1		3060 MT/s < f ≤ 3080 MT/s
x	1	0	1	1	1	0	0		3080 MT/s < f ≤ 3100 MT/s
x	1	0	1	1	1	0	1		3100 MT/s < f ≤ 3120 MT/s
x	1	0	1	1	1	1	0		3120 MT/s < f ≤ 3140 MT/s
x	1	0	1	1	1	1	1		3140 MT/s < f ≤ 3160 MT/s
x	1	1	0	0	0	0	0		3160 MT/s < f ≤ 3180 MT/s
x	1	1	0	0	0	0	1		3180 MT/s < f ≤ 3200 MT/s
x	1	1	x	x	x	1	x		Reserved
x	1	1	x	x	1	x	x		Reserved
x	1	1	x	1	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

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1. This control word defines the frequency of the BCK_t /BCK_c input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s (i.e., 10 MHz).
2. The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.
3. The encoding value is used to inform the DDR4DB02 of the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a DB can run.
4. The host is responsible for programming F0BC6x with the settings corresponding to the input clock frequency before initiating any training procedures with the DRAMs. The host is also responsible for keeping the settings in F0BC6x and BC0A consistent with each other.

4.21 F0BCCx - Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 0

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble of Rank 0 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 0 (MDQS1_t/MDQS1_c).

Table 46 — F0BCCx: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 0

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK receive enable timing latency adder
x	x	x	x	x	0	1	0		+2 nCK receive enable timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		- 1 nCK receive enable timing latency adder
x	x	x	x	x	1	1	0		- 2 nCK receive enable timing latency adder
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK receive enable timing latency adder
x	0	1	0	x	x	x	x		+2 nCK receive enable timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		- 1 nCK receive enable timing latency adder
x	1	1	0	x	x	x	x		- 2 nCK receive enable timing latency adder
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CL, AL and PL

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4.22 F0BCDx - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 0

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank 0 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 0 (MDQS1_t/MDQS1_c).

Table 47 — F0BCDx: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 0

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK write leveling timing latency adder
x	x	x	x	x	0	1	0		+2 nCK write leveling timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		-1 nCK write leveling timing latency adder
x	x	x	x	x	1	1	0		-2 nCK write leveling timing latency adder[2]
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK write leveling timing latency adder
x	0	1	0	x	x	x	x		+2 nCK write leveling timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		-1 nCK write leveling timing latency adder
x	1	1	0	x	x	x	x		-2 nCK write leveling timing latency adder[2]
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CWL, AL and PL
2. A write leveling timing latency adder setting of -2 tCK can only be supported with write latency settings of 10 tCK or greater (for 1 tCK write preamble) or 11 tCK or greater (for 2 tCK write preamble).

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4.23 F0BCEx - Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 2

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble of Rank 2 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 2 (MDQS1_t/MDQS1_c).

Table 48 — F0BCEx: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 2

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK receive enable timing latency adder
x	x	x	x	x	0	1	0		+2 nCK receive enable timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		- 1 nCK receive enable timing latency adder
x	x	x	x	x	1	1	0		- 2 nCK receive enable timing latency adder
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK receive enable timing latency adder
x	0	1	0	x	x	x	x		+2 nCK receive enable timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		- 1 nCK receive enable timing latency adder
x	1	1	0	x	x	x	x		- 2 nCK receive enable timing latency adder
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CL, AL and PL

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4.24 F0BCFx - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 2

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank 2 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 2 (MDQS1_t/MDQS1_c).

Table 49 — F0BCFx: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 2

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK write leveling timing latency adder
x	x	x	x	x	0	1	0		+2 nCK write leveling timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		-1 nCK write leveling timing latency adder
x	x	x	x	x	1	1	0		-2 nCK write leveling timing latency adder[2]
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK write leveling timing latency adder
x	0	1	0	x	x	x	x		+2 nCK write leveling timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		-1 nCK write leveling timing latency adder
x	1	1	0	x	x	x	x		-2 nCK write leveling timing latency adder[2]
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CWL, AL and PL
2. A write leveling timing latency adder setting of -2 tCK can only be supported with write latency settings of 10 tCK or greater (for 1 tCK write preamble) or 11 tCK or greater (for 2 tCK write preamble).

4.25 F1BC1x - LDQ Configuration Control Word

This BCW configures the LDQ port operation.

Table 50 — F1BC1x: LDQ Configuration Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	LDQ Interface Vref Range	Range 1
x	x	x	x	x	x	x	1		Range 2
x	x	x	x	x	x	0	x	LDQS Pre-amble and post-amble disable[1]	Pre-amble and post-amble enabled
x	x	x	x	x	x	1	x		Pre-amble and post-amble disabled
x	x	x	x	x	0	x	x	LDQ1 Disable [2]	Both LDQ1 and LDQ0 are used for NV operations
x	x	x	x	x	1	x	x		LDQ1 is disabled and only LDQ0 is used for NV operations
x	x	x	0	0	x	x	x	LDQ Port Rate Divider[3]	BCK/16, LDQS frequency is 1/16 of the frequency of BCK
x	x	x	0	1	x	x	x		BCK/8, LDQS frequency is 1/8 of the frequency of BCK
x	x	x	1	0	x	x	x		BCK/4, LDQS frequency is 1/4 of the frequency of BCK[4]
x	x	x	1	1	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	
x	x	1	x	x	x	x	x		
x	0	x	x	x	x	x	x	Reserved	
x	1	x	x	x	x	x	x		
0	x	x	x	x	x	x	x	Reserved	
1	x	x	x	x	x	x	x		

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1. Either or both timing modes can be supported when the optional NV feature is supported. When only one of the two modes is supported F1BC1x[1] is a read only bit indicating the supported mode. If both modes are supported then F1BC1x[1] is a read/write bit with a default setting of '0'.
2. By default both pins in LDQ[1:0] port are enabled for NV operation to either improve LDQ bandwidth or to allow LDQ to operate at lower speeds. For certain applications or above certain speeds LDQ0 may be enough to satisfy bandwidth requirements. For these application the LDQ1 can be disabled by setting this bit to a 1.
3. The default setting of DA[4:3] is '01'.
4. Maximum frequency may be limited by electrical specifications LDQS.

4.26 F1BCCx - Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 1

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble of Rank 1 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 1 (MDQS1_t/MDQS1_c).

Table 51 — F1BCCx: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 1

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK receive enable timing latency adder
x	x	x	x	x	0	1	0		+2 nCK receive enable timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		- 1 nCK receive enable timing latency adder
x	x	x	x	x	1	1	0		- 2 nCK receive enable timing latency adder
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK receive enable timing latency adder
x	0	1	0	x	x	x	x		+2 nCK receive enable timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		- 1 nCK receive enable timing latency adder
x	1	1	0	x	x	x	x		- 2 nCK receive enable timing latency adder
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CL, AL and PL

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4.27 F1BCDx - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 1

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank 1 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 1 (MDQS1_t/MDQS1_c).

Table 52 — F1BCDx: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 1

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK write leveling timing latency adder
x	x	x	x	x	0	1	0		+2 nCK write leveling timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		-1 nCK write leveling timing latency adder
x	x	x	x	x	1	1	0		-2 nCK write leveling timing latency adder[2]
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK write leveling timing latency adder
x	0	1	0	x	x	x	x		+2 nCK write leveling timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		-1 nCK write leveling timing latency adder
x	1	1	0	x	x	x	x		-2 nCK write leveling timing latency adder[2]
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CWL, AL and PL
2. A write leveling timing latency adder setting of -2 tCK can only be supported with write latency settings of 10 tCK or greater (for 1 tCK write preamble) or 11 tCK or greater (for 2 tCK write preamble).

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4.28 F1BCEx - Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 3

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble of Rank 3 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 3 (MDQS1_t/MDQS1_c).

Table 53 — F1BCEx: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for Rank 3

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK receive enable timing latency adder
x	x	x	x	x	0	1	0		+2 nCK receive enable timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		- 1 nCK receive enable timing latency adder
x	x	x	x	x	1	1	0		- 2 nCK receive enable timing latency adder[2]
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay[1]	0 nCK receive enable timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK receive enable timing latency adder
x	0	1	0	x	x	x	x		+2 nCK receive enable timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		- 1 nCK receive enable timing latency adder
x	1	1	0	x	x	x	x		- 2 nCK receive enable timing latency adder[2]
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CL, AL and PL
2. A write leveling timing latency adder setting of -2 tCK can only be supported with write latency settings of 10 tCK or greater (for 1 tCK write preamble) or 11 tCK or greater (for 2 tCK write preamble).

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4.29 F1BCFx - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 3

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank 3 (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank 3 (MDQS1_t/MDQS1_c).

Table 54 — F1BCFx: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word for Rank 3

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	x	x	x	x	0	0	1		+1 nCK write leveling timing latency adder
x	x	x	x	x	0	1	0		+2 nCK write leveling timing latency adder
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		-1 nCK write leveling timing latency adder
x	x	x	x	x	1	1	0		-2 nCK write leveling timing latency adder
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay[1]	0 nCK write leveling timing latency adder.
x	0	0	1	x	x	x	x		+1 nCK write leveling timing latency adder
x	0	1	0	x	x	x	x		+2 nCK write leveling timing latency adder
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		-1 nCK write leveling timing latency adder
x	1	1	0	x	x	x	x		-2 nCK write leveling timing latency adder
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The baseline delay includes the snooped values for CWL, AL and PL

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4.30 F2BC1x - LDQ Interface VREF Control Word

Table 55 — F2BC1x: LDQ Interface VREF Control Word definition

Setting (DA[7:0])								LDQ VREF as % of V_{DD} Range 1[1]	LDQ VREF as % of V_{DD} Range 2[1]
0	0	0	0	0	0	0	0	60.0%	45.0%
0	0	0	0	0	0	0	1	60.65%	45.65%
0	0	0	0	0	0	1	0	61.30%	46.30%
0	0	0	0	0	0	1	1	61.95%	46.95%
0	0	0	0	0	1	0	0	62.60%	47.60%
0	0	0	0	0	1	0	1	63.25%	48.25%
0	0	0	0	0	1	1	0	63.90%	48.90%
0	0	0	0	0	1	1	1	64.55%	49.55%
0	0	0	0	1	0	0	0	65.20%	50.20%
0	0	0	0	1	0	0	1	65.85%	50.85%
0	0	0	0	1	0	1	0	66.60%	51.60%
0	0	0	0	1	0	1	1	67.15%	52.15%
0	0	0	0	1	1	0	0	67.80%	52.80%
0	0	0	0	1	1	0	1	68.45%	53.45%
0	0	0	0	1	1	1	0	69.10%	54.10%
0	0	0	0	1	1	1	1	69.75%	54.75%
0	0	0	1	0	0	0	0	70.40%	55.40%
0	0	0	1	0	0	0	1	71.05%	56.05%
0	0	0	1	0	0	1	0	71.70%	56.70%
0	0	0	1	0	0	1	1	72.35%	57.35%
0	0	0	1	0	1	0	0	73.00%	58.00%
0	0	0	1	0	1	0	1	73.65%	58.65%
0	0	0	1	0	1	1	0	74.30%	59.30%
0	0	0	1	0	1	1	1	74.95%	59.95%
0	0	0	1	1	0	0	0	75.60%	60.60%
0	0	0	1	1	0	0	1	76.25%	61.25%
0	0	0	1	1	0	1	0	76.90%	61.90%
0	0	0	1	1	0	1	1	77.55%	62.55%
0	0	0	1	1	1	0	0	78.20%	63.20%
0	0	0	1	1	1	0	1	78.85%	63.85%
0	0	0	1	1	1	1	0	79.50%	64.50%
0	0	0	1	1	1	1	1	80.15%	65.15%
0	0	1	0	0	0	0	0	80.80%	65.80%
0	0	1	0	0	0	0	1	81.45%	66.45%
0	0	1	0	0	0	1	0	82.10%	67.10%
0	0	1	0	0	0	1	1	82.75%	67.75%
0	0	1	0	0	1	0	0	83.40%	68.40%
0	0	1	0	0	1	0	1	84.05%	69.05%
0	0	1	0	0	1	1	0	84.70%	69.70%
0	0	1	0	0	1	1	1	85.35%	70.35%
0	0	1	0	1	0	0	0	86.00%	71.00%
0	0	1	0	1	0	0	1	86.65%	71.65%
0	0	1	0	1	0	1	0	87.30%	72.30%
0	0	1	0	1	0	1	1	87.95%	72.95%
0	0	1	0	1	1	0	0	88.60%	73.60%
0	0	1	0	1	1	0	1	89.25%	74.25%
0	0	1	0	1	1	1	0	89.90%	74.90%
0	0	1	0	1	1	1	1	90.55%	75.55%
0	0	1	1	0	0	0	0	91.20%	76.20%
0	0	1	1	0	0	0	1	91.85%	76.85%
0	0	1	1	0	0	1	0	92.50%	77.50%

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Table 55 — F2BC1x: LDQ Interface VREF Control Word definition

Setting (DA[7:0])								LDQ VREF as % of V_{DD} Range 1[1]	LDQ VREF as % of V_{DD} Range 2[1]
0	0	1	1	0	0	1	1	Reserved	Reserved
0	0	1	1	x	1	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x	Reserved	Reserved
1	0	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

1. These are target VrefLDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

4.31 F2BCEx - Host Interface DFE Programming Control Word

The host must first select DQn Write Read mode from F2BCEx before accessing Gain Adjustment or Tap Control Words.

Table 56 — F2BCEx: Host Interface DFE Programming Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Host Interface DFE Selector for BCW Write/Read operations to and from F2BCFx, F3BCCx, F3BCDx, F3BCEx, and F3BCFx	(Default) Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ0.
x	x	x	x	0	0	0	1		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ1.
x	x	x	x	0	0	1	0		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ2.
x	x	x	x	0	0	1	1		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ3.
x	x	x	x	0	1	0	0		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ4.
x	x	x	x	0	1	0	1		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ5.
x	x	x	x	0	1	1	0		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ6.
x	x	x	x	0	1	1	1		Writes broadcast to DFE registers for DQ[7:0]; Reads sourced from DFE registers for DQ7.
x	x	x	x	1	0	0	0		Writes and Reads apply to DFE registers for DQ0.
x	x	x	x	1	0	0	1		Writes and Reads apply to DFE registers for DQ1.
x	x	x	x	1	0	1	0		Writes and Reads apply to DFE registers for DQ2.
x	x	x	x	1	0	1	1		Writes and Reads apply to DFE registers for DQ3.
x	x	x	x	1	1	0	0		Writes and Reads apply to DFE registers for DQ4.
x	x	x	x	1	1	0	1		Writes and Reads apply to DFE registers for DQ5.
x	x	x	x	1	1	1	0		Writes and Reads apply to DFE registers for DQ6.
x	x	x	x	1	1	1	1		Writes and Reads apply to DFE registers for DQ7.
x	x	x	0	x	x	x	x	DFE Tap Capabilities[1]	DFE Feature not supported
x	x	x	1	x	x	x	x		DFE Feature supported
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	DFE Gain Adjustment Capability[2]	DFE Gain Adjustment Feature not supported
x	1	x	x	x	x	x	x		Supported using F2BCFx
0	x	x	x	x	x	x	x	DFE Feature Global Enable Control[3]	(Default) DFE and gain features disabled
1	x	x	x	x	x	x	x		DFE and gain features enabled

1. Read-only status bit. The hard-coded value of this status bit will be 1 in DDR4DB02 devices that support speeds higher than or equal to 2933 MT/s. This bit location is Reserved in earlier devices without DFE support and it will, by definition, read out as 0, i.e. “DFE Feature not Supported”, in those devices.
2. Read-only status bit. If F2BCEx DA6 = 0 then F2BCFx DA[2:0] will be ignored by the DDR4DB02. The hard-coded value of this status bit may be 1 in DDR4DB02 devices that support speeds higher than or equal to 2933 MT/s. This bit location is Reserved in earlier devices without Gain Adjustment support and it will, by definition, read out as 0, i.e. “DFE Gain Adjustment Feature not supported”, in those devices.

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3. This control bit enables all the capabilities declared in Bits DA6 and DA4 of F2BCEx and in the Training mode bits DA6 and DA7 of F2BCFx.

4.32 F2BCFx - Host Interface DQ[7:0] Receiver DFE Gain Adjustment and DFE Training Mode Control Word

Table 57 — F2BCFx: Host Interface DQ[7:0] Receiver DFE Gain Adjustment and DFE Training Mode Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Flat-band (DC) gain adjustment (up to the Nyquist rate) adjustment control from I/O die pad to latching element in DQn receiver selected in F2BCEx - DA[3:0][1,2,3]	Gain Adjustment = 0 dB (default)
x	x	x	x	x	0	0	1		Gain Adjustment = +2 dB
x	x	x	x	x	0	1	0		Gain Adjustment = +4 dB
x	x	x	x	x	0	1	1		Gain Adjustment = +6 dB
x	x	x	x	x	1	0	0		Gain Adjustment = 0 dB (same as default)
x	x	x	x	x	1	0	1		Gain Adjustment = -2 dB
x	x	x	x	x	1	1	0		Gain Adjustment = -4 dB
x	x	x	x	x	1	1	1		Gain Adjustment = -6 dB
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Training Source	Monitor
x	1	x	x	x	x	x	x		Monitor XOR Slicer Output
0	x	x	x	x	x	x	x	DFE Training Mode for DQn receiver selected in F2BCEx[4,5]	DFE Training Mode disabled
1	x	x	x	x	x	x	x		DFE Training Mode enabled[6,7,8]

1. If this optional feature is supported (F2BCEx DA6 = 1), the Gain Adjustment is applied to the baseline (default) inherent gain implemented in the receiver. If this feature is not supported (F2BCEx DA6 = 0), then F2BCFx DA[2:0] is ignored by the DDR4DB02 hardware.
2. Gain Adjustment values shown in Table 3 are verified by design and the measurement from device pins is TBD.
3. Allowable Differential nonlinearity (DNL) is 1 dB and the allowable Integral nonlinearity (INL) is 2.0 dB.
4. DFE Training mode cannot be enabled when Writes are broadcasted to DQ[7:0], however broadcast mode can be used to disable DFE training mode for all DQn in a single command.
5. F2BCEx - DA[2:0] determines the target DQn receiver for DFE training and F2BCEx - DA3 is ignored. Logic in DDR4DB02 ensures that only one DQn receiver is configured in training mode at any given time.
6. DFE circuits are configured into training mode.
7. Vref generator circuits are configured so that a DFE training reference voltage (DFE_VREF) is controlled by F5BC6x - DA[7:0] and F6BC4x - DA2 while the effective DRAM interface Vref value is maintained at the last setting programmed in F5BC6x - DA[7:0] and F6BC4x - DA2 before F2BCFx - DA7 (for any one of the DQn pins) is set to 1. The user must never enable DFE Training Mode while PDA or PBA modes are also enabled (i.e., when Bit DA0 or Bit DA2 are set to 1 in F0BC1x).
8. When DFE training mode is enabled for a targeted DQn receiver selected by F2BCEx - DA[2:0], the DFE Training Mode Enable bits in F2BCFx DA7 corresponding to DQn receivers other than the selected one will automatically be cleared to 0 by the DB02 hardware.

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4.33 F3BC1x - LDQ Interface Driver, ODT Control Word

This BCW configures the LDQ port driver and termination settings.

Table 58 — F3BC1x: LDQ Interface Driver, ODT Control

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	0	0	LDQ/LDQS Output Driver **Impedance Control**[1]	RZQ/6 (40 Ω)
x	x	x	x	x	x	0	1		RZQ/7 (34 Ω)
x	x	x	x	x	x	1	0		RZQ/5 (48 Ω)
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	Reserved	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	LDQ/LDQS Output Driver Disable	LDQ/LDQS output drivers enabled
x	x	x	x	1	x	x	x		LDQ/LDQS output drivers disabled
x	0	0	0	x	x	x	x	LDQ/LDQS ODT Strength[2]	ODT disabled
x	0	0	1	x	x	x	x		RZQ/4 (60 Ω)
x	0	1	0	x	x	x	x		RZQ/2 (120 Ω)
x	0	1	1	x	x	x	x		RZQ/6 (40 Ω)
x	1	0	0	x	x	x	x		RZQ/1 (240 Ω)
x	1	0	1	x	x	x	x		RZQ/5 (48 Ω)
x	1	1	0	x	x	x	x		RZQ/3 (80 Ω)
x	1	1	1	x	x	x	x		RZQ/7 (34 Ω)
0	x	x	x	x	x	x	x	**Reserved**	
1	x	x	x	x	x	x	x		

1. LDQ[1:0] drivers are only enabled in SAVE mode (BC0D DA[1:0] = 10). Only applies to LDQ1 driver if enabled (F1BC1x DA2 = 0)
2. LDQ[1:0] termination is only enabled in RESTORE mode (BC0D DA[1:0] = 01). Only applies to LDQ1 if enabled (F1BC1x DA2 = 0)

4.34 F3BCCx - Host Interface DQ[7:0] Receiver DFE Tap 1 Coefficient Control Word

Table 59 — F3BCCx: Host Interface DQ[7:0] Receiver DFE Tap 1 Coefficient Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Tap 1 Coefficient [3:0] for DQn receiver selected in F2BCEx - DA[3:0][1,2]	(Default) Tap 1 DFE bias = 0 mV
x	x	x	x	0	0	0	1		Tap 1 DFE bias = 3 mV
x	x	x	x	0	0	1	0		Tap 1 DFE bias = 6 mV
x	x	x	x	0	0	1	1		Tap 1 DFE bias = 9 mV
x	x	x	x	0	1	0	0		Tap 1 DFE bias = 12 mV
x	x	x	x	0	1	0	1		Tap 1 DFE bias = 15 mV
x	x	x	x	0	1	1	0		Tap 1 DFE bias = 18 mV
x	x	x	x	0	1	1	1		Tap 1 DFE bias = 21 mV
x	x	x	x	1	0	0	0		Tap 1 DFE bias = 24 mV
x	x	x	x	1	0	0	1		Tap 1 DFE bias = 27 mV
x	x	x	x	1	0	1	0		Tap 1 DFE bias = 30 mV
x	x	x	x	1	0	1	1		Tap 1 DFE bias = 33 mV
x	x	x	x	1	1	0	0		Tap 1 DFE bias = 36 mV
x	x	x	x	1	1	0	1		Tap 1 DFE bias = 39 mV
x	x	x	x	1	1	1	0		Tap 1 DFE bias = 42 mV
x	x	x	x	1	1	1	1		Tap 1 DFE bias = 45 mV
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Tap 1 Enable Bit for all DQ[7:0][3]	(Default) Tap 1 disabled[4]
x	1	x	x	x	x	x	x		Tap 1 enabled
0	x	x	x	x	x	x	x	Tap 1 Coefficient Sign Bit for DQn receiver selected in F2BCEx - DA[3:0]	(Default) Positive Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

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1. Tap coefficient values shown in Table 59 are verified by design and the measurement from device pins is TBD.
2. Allowable Differential nonlinearity (DNL) is 3 mV and the allowable Integral nonlinearity (INL) is 6 mV.
3. This control bit is accessed for Writes or Reads independently from the settings contained in F2BCEx - DA[3:0].
4. When Tap 1 is disabled, DB02 hardware also disables Taps 2, 3 and 4 automatically. DB02 hardware is expected to power off circuits related to DFE Taps 1, 2, 3, and 4 when F3BCCx - DA6 = 0.

4.35 F3BCDx - Host Interface DQ[7:0] Receiver DFE Tap 2 Coefficient Control Word

Table 60 — F3BCDx: Host Interface DQ[7:0] Receiver DFE Tap 2 Coefficient Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Tap 2 Coefficient [3:0] for DQn receiver selected in F2BCEx - DA[3:0][1,2]	(Default) Tap 2 DFE bias = 0 mV
x	x	x	x	0	0	0	1		Tap 2 DFE bias = 3 mV
x	x	x	x	0	0	1	0		Tap 2 DFE bias = 6 mV
x	x	x	x	0	0	1	1		Tap 2 DFE bias = 9 mV
x	x	x	x	0	1	0	0		Tap 2 DFE bias = 12 mV
x	x	x	x	0	1	0	1		Tap 2 DFE bias = 15 mV
x	x	x	x	0	1	1	0		Tap 2 DFE bias = 18 mV
x	x	x	x	0	1	1	1		Tap 2 DFE bias = 21 mV
x	x	x	x	1	0	0	0		Tap 2 DFE bias = 24 mV
x	x	x	x	1	0	0	1		Tap 2 DFE bias = 27 mV
x	x	x	x	1	0	1	0		Tap 2 DFE bias = 30 mV
x	x	x	x	1	0	1	1		Tap 2 DFE bias = 33 mV
x	x	x	x	1	1	0	0		Tap 2 DFE bias = 36 mV
x	x	x	x	1	1	0	1		Tap 2 DFE bias = 39 mV
x	x	x	x	1	1	1	0		Tap 2 DFE bias = 42 mV
x	x	x	x	1	1	1	1		Tap 2 DFE bias = 45 mV
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Tap 2 Enable Bit for all DQ[7:0][3]	(Default) Tap 2 disabled[4]
x	1	x	x	x	x	x	x		Tap 2 enabled
0	x	x	x	x	x	x	x	Tap 2 Coefficient Sign Bit for DQn receiver selected in F2BCEx - DA[3:0]	(Default) Positive Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 2 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 2 post-cursor)

1. Tap coefficient values shown in Table 60 are verified by design and the measurement from device pins is TBD.
2. Allowable Differential nonlinearity (DNL) is 3 mV and the allowable Integral nonlinearity (INL) is 6 mV.
3. This control bit is accessed for Writes or Reads independently from the settings contained in F2BCEx - DA[3:0].
4. When Tap 2 is disabled, DB02 hardware also disables Taps 3 and 4 automatically. DB02 hardware is expected to power off circuits related to DFE Taps 2, 3, and 4 when F3BCDx - DA6 = 0.

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4.36 F3BCEx - Host Interface DQ[7:0] Receiver DFE Tap 3 Coefficient Control Word

Table 61 — F3BCEx: Host Interface DQ[7:0] Receiver DFE Tap 3 Coefficient Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Tap 3 Coefficient [3:0] for DQn receiver selected in F2BCEx - DA[3:0][1,2]	(Default) Tap 3 DFE bias = 0 mV
x	x	x	x	0	0	0	1		Tap 3 DFE bias = 3 mV
x	x	x	x	0	0	1	0		Tap 3 DFE bias = 6 mV
x	x	x	x	0	0	1	1		Tap 3 DFE bias = 9 mV
x	x	x	x	0	1	0	0		Tap 3 DFE bias = 12 mV
x	x	x	x	0	1	0	1		Tap 3 DFE bias = 15 mV
x	x	x	x	0	1	1	0		Tap 3 DFE bias = 18 mV
x	x	x	x	0	1	1	1		Tap 3 DFE bias = 21 mV
x	x	x	x	1	0	0	0		Tap 3 DFE bias = 24 mV
x	x	x	x	1	0	0	1		Tap 3 DFE bias = 27 mV
x	x	x	x	1	0	1	0		Tap 3 DFE bias = 30 mV
x	x	x	x	1	0	1	1		Tap 3 DFE bias = 33 mV
x	x	x	x	1	1	0	0		Tap 3 DFE bias = 36 mV
x	x	x	x	1	1	0	1		Tap 3 DFE bias = 39 mV
x	x	x	x	1	1	1	0		Tap 3 DFE bias = 42 mV
x	x	x	x	1	1	1	1		Tap 3 DFE bias = 45 mV
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Tap 3 Enable Bit for DQ[7:0][3]	(Default) Tap 3 disabled[4]
x	1	x	x	x	x	x	x		Tap 3 enabled
0	x	x	x	x	x	x	x	Tap 3 Coefficient Sign Bit for DQn receiver selected in F2BCEx - DA[3:0]	(Default) Positive Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 3 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 3 post-cursor)

1. Tap coefficient values shown in Table 61 are verified by design and the measurement from device pins is TBD.
2. Allowable Differential nonlinearity (DNL) is 3 mV and the allowable Integral nonlinearity (INL) is 6 mV.
3. This control bit is accessed for Writes or Reads independently from the settings contained in F2BCEx - DA[3:0].
4. When Tap 3 is disabled, DB02 hardware also disables Tap 4 automatically. DB02 hardware is expected to power off circuits related to DFE Taps 3 and 4 when F3BCEx - DA6 = 0.

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4.37 F3BCFx - Host Interface DQ[7:0] Receiver DFE Tap 4 Coefficient Control Word

Table 62 — F3BCFx: Host Interface DQ[7:0] Receiver DFE Tap 4 Coefficient Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Tap 4 Coefficient [3:0] for DQn receiver selected in F2BCEx - DA[3:0][1,2]	(Default) Tap 4 DFE bias = 0 mV
x	x	x	x	0	0	0	1		Tap 4 DFE bias = 3 mV
x	x	x	x	0	0	1	0		Tap 4 DFE bias = 6 mV
x	x	x	x	0	0	1	1		Tap 4 DFE bias = 9 mV
x	x	x	x	0	1	0	0		Tap 4 DFE bias = 12 mV
x	x	x	x	0	1	0	1		Tap 4 DFE bias = 15 mV
x	x	x	x	0	1	1	0		Tap 4 DFE bias = 18 mV
x	x	x	x	0	1	1	1		Tap 4 DFE bias = 21 mV
x	x	x	x	1	0	0	0		Tap 4 DFE bias = 24 mV
x	x	x	x	1	0	0	1		Tap 4 DFE bias = 27 mV
x	x	x	x	1	0	1	0		Tap 4 DFE bias = 30 mV
x	x	x	x	1	0	1	1		Tap 4 DFE bias = 33 mV
x	x	x	x	1	1	0	0		Tap 4 DFE bias = 36 mV
x	x	x	x	1	1	0	1		Tap 4 DFE bias = 39 mV
x	x	x	x	1	1	1	0		Tap 4 DFE bias = 42 mV
x	x	x	x	1	1	1	1		Tap 4 DFE bias = 45 mV
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Tap 4 Enable Bit for DQ[7:0][3]	(Default) Tap 4 disabled[4]
x	1	x	x	x	x	x	x		Tap 4 enabled
0	x	x	x	x	x	x	x	Tap 4 Coefficient Sign Bit for DQn receiver selected in F2BCEx - DA[3:0]	(Default) Positive Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 4 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 4 post-cursor)

1. Tap coefficient values shown in Table 62 are verified by design and the measurement from device pins is TBD.
2. Allowable Differential nonlinearity (DNL) is 3 mV and the allowable Integral nonlinearity (INL) is 6 mV.
3. This control bit is accessed for Writes or Reads independently from the settings contained in F2BCEx - DA[3:0].
4. DB02 hardware is expected to power off circuits related to DFE Tap 4 when F3BCFx - DA6 = 0.

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4.38 F[3:0]BC2x/F[3:0]BC3x - Lower/Upper Nibble DRAM Interface Receive Enable Training Control Word (per rank)

There are four 8-bit control words for the trained receive enable timing on the lower nibble of the DRAM interface (MDQS0_t/MDQS0_c) and four 8-bit control words for the upper nibble (MDQS1_t/MDQS1_c). Each of the control words is located in address BC2x/BC3x of BCW Function Spaces 0 through 3. Ranks are assigned in order to each of these function spaces. That is, the control word in Function 0 (F0BC2x/F0BC3x) correspond to Rank 0, which is connected to QxCS0_n of the RCD; the control word in Function 1 (F1BC2x/F1BC3x) correspond to Rank 1, which is connected to QxCS1_n of the RCD; and so on.

Table 63 — F[3:0]BC2x: Lower Nibble DRAM Interface Receive Enable Training Control Word (per rank)

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS receive enable timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * t_{CK}
x	x	...							
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

Table 64 — F[3:0]BC3x: Upper Nibble DRAM Interface Receive Enable Training Control Word (per rank)

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS receive enable timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * t_{CK}
x	x	...							
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

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4.39 F[3:0]BC4x - Lower Nibble MDQS Read Delay Control Word

Table 65 — F[3:0]BC4x: Lower Nibble MDQS Read Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Lower Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQS by $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		Delay MDQS by $t_{CK}/4 + (1/64) * t_{CK}$
x	x	x	0	0	0	1	0		Delay MDQS by $t_{CK}/4 + (2/64) * t_{CK}$
x	x	x	0	0	0	1	1		Delay MDQS by $t_{CK}/4 + (3/64) * t_{CK}$
x	x	x	0	0	1	0	0		Delay MDQS by $t_{CK}/4 + (4/64) * t_{CK}$
x	x	x	0	0	1	0	1		Delay MDQS by $t_{CK}/4 + (5/64) * t_{CK}$
x	x	x	0	0	1	1	0		Delay MDQS by $t_{CK}/4 + (6/64) * t_{CK}$
x	x	x	0	0	1	1	1		Delay MDQS by $t_{CK}/4 + (7/64) * t_{CK}$
x	x	x	0	1	0	0	0		Delay MDQS by $t_{CK}/4 + (8/64) * t_{CK}$
x	x	x	0	1	0	0	1		Delay MDQS by $t_{CK}/4 + (9/64) * t_{CK}$
x	x	x	0	1	0	1	0		Delay MDQS by $t_{CK}/4 + (10/64) * t_{CK}$
x	x	x	0	1	0	1	1		Delay MDQS by $t_{CK}/4 + (11/64) * t_{CK}$
x	x	x	0	1	1	0	0		Delay MDQS by $t_{CK}/4 + (12/64) * t_{CK}$
x	x	x	0	1	1	0	1		Delay MDQS by $t_{CK}/4 + (13/64) * t_{CK}$
x	x	x	0	1	1	1	0		Delay MDQS by $t_{CK}/4 + (14/64) * t_{CK}$
x	x	x	0	1	1	1	1		Delay MDQS by $t_{CK}/4 + (15/64) * t_{CK}$
x	x	x	1	0	0	0	0		Delay MDQS by $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		Delay MDQS by $t_{CK}/4 - (1/64) * t_{CK}$
x	x	x	1	0	0	1	0		Delay MDQS by $t_{CK}/4 - (2/64) * t_{CK}$
x	x	x	1	0	0	1	1		Delay MDQS by $t_{CK}/4 - (3/64) * t_{CK}$
x	x	x	1	0	1	0	0		Delay MDQS by $t_{CK}/4 - (4/64) * t_{CK}$
x	x	x	1	0	1	0	1		Delay MDQS by $t_{CK}/4 - (5/64) * t_{CK}$
x	x	x	1	0	1	1	0		Delay MDQS by $t_{CK}/4 - (6/64) * t_{CK}$
x	x	x	1	0	1	1	1		Delay MDQS by $t_{CK}/4 - (7/64) * t_{CK}$
x	x	x	1	1	0	0	0		Delay MDQS by $t_{CK}/4 - (8/64) * t_{CK}$
x	x	x	1	1	0	0	1		Delay MDQS by $t_{CK}/4 - (9/64) * t_{CK}$
x	x	x	1	1	0	1	0		Delay MDQS by $t_{CK}/4 - (10/64) * t_{CK}$
x	x	x	1	1	0	1	1		Delay MDQS by $t_{CK}/4 - (11/64) * t_{CK}$
x	x	x	1	1	1	0	0		Delay MDQS by $t_{CK}/4 - (12/64) * t_{CK}$
x	x	x	1	1	1	0	1		Delay MDQS by $t_{CK}/4 - (13/64) * t_{CK}$
x	x	x	1	1	1	1	0		Delay MDQS by $t_{CK}/4 - (14/64) * t_{CK}$
x	x	x	1	1	1	1	1		Delay MDQS by $t_{CK}/4 - (15/64) * t_{CK}$
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. By default, the delay of MDQS signals received by the DDR4 buffer during read commands is $t_{CK}/4$. The F[3:0]BC4x - DA[4:0] control bits can be used by the host to adjust this lower nibble delay to a more optimal position.

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4.40 F[3:0]BC5x - Upper Nibble MDQS Read Delay Control Word

Table 66 — F[3:0]BC5x: Upper Nibble MDQS Read Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Upper Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQS by $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		Delay MDQS by $t_{CK}/4 + (1/64) * t_{CK}$
x	x	x	0	0	0	1	0		Delay MDQS by $t_{CK}/4 + (2/64) * t_{CK}$
x	x	x	0	0	0	1	1		Delay MDQS by $t_{CK}/4 + (3/64) * t_{CK}$
x	x	x	0	0	1	0	0		Delay MDQS by $t_{CK}/4 + (4/64) * t_{CK}$
x	x	x	0	0	1	0	1		Delay MDQS by $t_{CK}/4 + (5/64) * t_{CK}$
x	x	x	0	0	1	1	0		Delay MDQS by $t_{CK}/4 + (6/64) * t_{CK}$
x	x	x	0	0	1	1	1		Delay MDQS by $t_{CK}/4 + (7/64) * t_{CK}$
x	x	x	0	1	0	0	0		Delay MDQS by $t_{CK}/4 + (8/64) * t_{CK}$
x	x	x	0	1	0	0	1		Delay MDQS by $t_{CK}/4 + (9/64) * t_{CK}$
x	x	x	0	1	0	1	0		Delay MDQS by $t_{CK}/4 + (10/64) * t_{CK}$
x	x	x	0	1	0	1	1		Delay MDQS by $t_{CK}/4 + (11/64) * t_{CK}$
x	x	x	0	1	1	0	0		Delay MDQS by $t_{CK}/4 + (12/64) * t_{CK}$
x	x	x	0	1	1	0	1		Delay MDQS by $t_{CK}/4 + (13/64) * t_{CK}$
x	x	x	0	1	1	1	0		Delay MDQS by $t_{CK}/4 + (14/64) * t_{CK}$
x	x	x	0	1	1	1	1		Delay MDQS by $t_{CK}/4 + (15/64) * t_{CK}$
x	x	x	1	0	0	0	0		Delay MDQS by $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		Delay MDQS by $t_{CK}/4 - (1/64) * t_{CK}$
x	x	x	1	0	0	1	0		Delay MDQS by $t_{CK}/4 - (2/64) * t_{CK}$
x	x	x	1	0	0	1	1		Delay MDQS by $t_{CK}/4 - (3/64) * t_{CK}$
x	x	x	1	0	1	0	0		Delay MDQS by $t_{CK}/4 - (4/64) * t_{CK}$
x	x	x	1	0	1	0	1		Delay MDQS by $t_{CK}/4 - (5/64) * t_{CK}$
x	x	x	1	0	1	1	0		Delay MDQS by $t_{CK}/4 - (6/64) * t_{CK}$
x	x	x	1	0	1	1	1		Delay MDQS by $t_{CK}/4 - (7/64) * t_{CK}$
x	x	x	1	1	0	0	0		Delay MDQS by $t_{CK}/4 - (8/64) * t_{CK}$
x	x	x	1	1	0	0	1		Delay MDQS by $t_{CK}/4 - (9/64) * t_{CK}$
x	x	x	1	1	0	1	0		Delay MDQS by $t_{CK}/4 - (10/64) * t_{CK}$
x	x	x	1	1	0	1	1		Delay MDQS by $t_{CK}/4 - (11/64) * t_{CK}$
x	x	x	1	1	1	0	0		Delay MDQS by $t_{CK}/4 - (12/64) * t_{CK}$
x	x	x	1	1	1	0	1		Delay MDQS by $t_{CK}/4 - (13/64) * t_{CK}$
x	x	x	1	1	1	1	0		Delay MDQS by $t_{CK}/4 - (14/64) * t_{CK}$
x	x	x	1	1	1	1	1		Delay MDQS by $t_{CK}/4 - (15/64) * t_{CK}$
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. By default, the delay of MDQS signals received by the DDR4 buffer during read commands is $t_{CK}/4$. The F[3:0]BC5x - DA[4:0] control bits can be used by the host to adjust this upper nibble delay to a more optimal position.

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4.41 F[3:0]BC8x - Lower Nibble MDQ-MDQS Write Delay Control Word

Table 67 — F[3:0]BC8x: Lower Nibble MDQ-MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Phase Control Between Lower Nibble MDQ and MDQS During Write Transactions in Steps of (1/64) * t_{CK}[1,2]	MDQS_t to MDQ phase delay = $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (1/64) * t_{CK}$
x	x	x	0	0	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (2/64) * t_{CK}$
x	x	x	0	0	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (3/64) * t_{CK}$
x	x	x	0	0	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (4/64) * t_{CK}$
x	x	x	0	0	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (5/64) * t_{CK}$
x	x	x	0	0	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (6/64) * t_{CK}$
x	x	x	0	0	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (7/64) * t_{CK}$
x	x	x	0	1	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (8/64) * t_{CK}$
x	x	x	0	1	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (9/64) * t_{CK}$
x	x	x	0	1	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (10/64) * t_{CK}$
x	x	x	0	1	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (11/64) * t_{CK}$
x	x	x	0	1	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (12/64) * t_{CK}$
x	x	x	0	1	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (13/64) * t_{CK}$
x	x	x	0	1	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (14/64) * t_{CK}$
x	x	x	0	1	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (15/64) * t_{CK}$
x	x	x	1	0	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (1/64) * t_{CK}$
x	x	x	1	0	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (2/64) * t_{CK}$
x	x	x	1	0	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (3/64) * t_{CK}$
x	x	x	1	0	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (4/64) * t_{CK}$
x	x	x	1	0	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (5/64) * t_{CK}$
x	x	x	1	0	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (6/64) * t_{CK}$
x	x	x	1	0	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (7/64) * t_{CK}$
x	x	x	1	1	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (8/64) * t_{CK}$
x	x	x	1	1	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (9/64) * t_{CK}$
x	x	x	1	1	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (10/64) * t_{CK}$
x	x	x	1	1	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (11/64) * t_{CK}$
x	x	x	1	1	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (12/64) * t_{CK}$
x	x	x	1	1	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (13/64) * t_{CK}$
x	x	x	1	1	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (14/64) * t_{CK}$
x	x	x	1	1	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (15/64) * t_{CK}$
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. By default, the phase between the MDQ and MDQS signals driven by the DDR4 buffer during write commands is $t_{CK}/4$. The F[3:0]BC6x - DA[4:0] control bits can be used by the host to adjust the phase relationship between lower nibble MDQ and MDQS to a more optimal position.
2. MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

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4.42 F[3:0]BC9x - Upper Nibble MDQ-MDQS Write Delay Control Word

Table 68 — F[3:0]BC9x: Upper Nibble MDQ-MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Phase Control Between Upper Nibble MDQ and MDQS During Write Transactions in Steps of (1/64) * t_{CK}[1,2]	MDQS_t to MDQ phase delay = $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (1/64) * t_{CK}$
x	x	x	0	0	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (2/64) * t_{CK}$
x	x	x	0	0	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (3/64) * t_{CK}$
x	x	x	0	0	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (4/64) * t_{CK}$
x	x	x	0	0	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (5/64) * t_{CK}$
x	x	x	0	0	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (6/64) * t_{CK}$
x	x	x	0	0	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (7/64) * t_{CK}$
x	x	x	0	1	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (8/64) * t_{CK}$
x	x	x	0	1	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (9/64) * t_{CK}$
x	x	x	0	1	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (10/64) * t_{CK}$
x	x	x	0	1	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (11/64) * t_{CK}$
x	x	x	0	1	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (12/64) * t_{CK}$
x	x	x	0	1	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (13/64) * t_{CK}$
x	x	x	0	1	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 + (14/64) * t_{CK}$
x	x	x	0	1	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 + (15/64) * t_{CK}$
x	x	x	1	0	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (1/64) * t_{CK}$
x	x	x	1	0	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (2/64) * t_{CK}$
x	x	x	1	0	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (3/64) * t_{CK}$
x	x	x	1	0	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (4/64) * t_{CK}$
x	x	x	1	0	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (5/64) * t_{CK}$
x	x	x	1	0	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (6/64) * t_{CK}$
x	x	x	1	0	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (7/64) * t_{CK}$
x	x	x	1	1	0	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (8/64) * t_{CK}$
x	x	x	1	1	0	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (9/64) * t_{CK}$
x	x	x	1	1	0	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (10/64) * t_{CK}$
x	x	x	1	1	0	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (11/64) * t_{CK}$
x	x	x	1	1	1	0	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (12/64) * t_{CK}$
x	x	x	1	1	1	0	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (13/64) * t_{CK}$
x	x	x	1	1	1	1	0		MDQS_t to MDQ phase delay = $t_{CK}/4 - (14/64) * t_{CK}$
x	x	x	1	1	1	1	1		MDQS_t to MDQ phase delay = $t_{CK}/4 - (15/64) * t_{CK}$
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. By default, the phase between the MDQ and MDQS signals driven by the DDR4 buffer during write commands is $t_{CK}/4$. The F[3:0]BC7x - DA[4:0] control bits can be used by the host to adjust the phase relationship between upper nibble MDQ and MDQS to a more optimal position.
2. MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

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4.43 F[3:0]BCAx/F[3:0]BCBx - Lower/Upper Nibble DRAM Interface Write Leveling Control Word (per rank)

There are four 8-bit control words for the trained write leveling timing on the lower nibble of the DRAM interface (MDQS0_t/MDQS0_c) and four 8-bit control words for the upper nibble (MDQS1_t/MDQS1_c). Each of the control words is located in address BCAx/BCBx of BCW Function Spaces 0 through 3. Ranks are assigned in order to each of these function spaces. That is, the control word in Function 0 (F0BCAx/F0BCBx) correspond to Rank 0; the control word in Function 1 (F1BCAx/F1BCBx) correspond to Rank 1, and so on.

Table 69 — F[3:0]BCAx: Lower Nibble DRAM Interface Write Leveling Control Word (per rank)

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Control in Steps of (1/64) * t_{CK}	Delay MDQS write leveling timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * t_{CK}
x	x	...							
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

Table 70 — F[3:0]BCBx: Upper Nibble DRAM Interface Write Leveling Control Word (per rank)

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS write leveling timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * t_{CK}
x	x	...							
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

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4.44 F3BC1x - LDQ Interface Driver, ODT Control

This BCW configures the LDQ port driver and termination settings.

Table 71 — F3BC1x: LDQ Interface Driver, ODT Control

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	0	0	LDQ/LDQS Output Driver Impedance Control[1]	RZQ/6 (40 Ω)
x	x	x	x	x	x	0	1		RZQ/7 (34 Ω)
x	x	x	x	x	x	1	0		RZQ/5 (48 Ω)
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	Reserved	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	LDQ/LDQS Output Driver Disable	LDQ/LDQS output drivers enabled
x	x	x	x	1	x	x	x		LDQ/LDQS output drivers disabled
x	0	0	0	x	x	x	x	LDQ/LDQS ODT Strength[2]	ODT disabled
x	0	0	1	x	x	x	x		RZQ/4 (60 Ω)
x	0	1	0	x	x	x	x		RZQ/2 (120 Ω)
x	0	1	1	x	x	x	x		RZQ/6 (40 Ω)
x	1	0	0	x	x	x	x		RZQ/1 (240 Ω)
x	1	0	1	x	x	x	x		RZQ/5 (48 Ω)
x	1	1	0	x	x	x	x		RZQ/3 (80 Ω)
x	1	1	1	x	x	x	x		RZQ/7 (34 Ω)
0	x	x	x	x	x	x	x	Reserved	
1	x	x	x	x	x	x	x		

1. LDQ[1:0] drivers are only enabled in SAVE mode (BC0D DA[1:0] = 10). Only applies to LDQ1 driver if enabled (F1BC1x DA2 = 0)
2. LDQ[1:0] termination is only enabled in RESTORE mode (BC0D DA[1:0] = 01). Only applies to LDQ1 if enabled (F1BC1x DA2 = 0)

4.45 F4BC0x .. F4BC6x - MRS Snooped Settings

Upon receiving a DRAM MRS command, the DDR4 RCD snoops relevant bits that are needed by the DB for its operation and sends them to the DB via a MRS Write command over the BCOM bus. The data buffer stores these bit settings in BCW space. The stored snooped MRS settings can be read by means of BCW Read commands. The BCW Write command can be used to program these settings directly and override the results of any prior MRS snooping.

Table 72 — F4BC0x - F4BC6x: MRS Snooped Settings

Control Word	MRS	Control Word Bits			
		DA3/DA7	DA2/DA6	DA1/DA5	DA0/DA4
F4BC0x (DA[3:0])	MR0	CAS Latency (A12)	Reserved	BL (A1, A0)	
F4BC0x (DA[7:4])		CAS Latency (A6, A5, A4, A2)			
F4BC1x (DA[3:0])	MR1	Reserved	Additive Latency (A4, A3)		Reserved
F4BC1x (DA[7:4])		Reserved	Reserved	Reserved	Reserved
F4BC2x (DA[3:0])	MR2	Reserved	CAS Write Latency (A5:A3)		
F4BC2x (DA[7:4])		Write CRC (A12)	Reserved	Reserved	Reserved
F4BC3x (DA[3:0])	MR3	Reserved	Reserved	Geardown Mode (A3)	Reserved
F4BC3x (DA[7:4])		MPR Read Format (A12, A11)[1,2]		Reserved	Reserved
F4BC4x (DA[3:0])	MR4	CAL Mode (A8:A6)			Reserved
F4BC4x (DA[7:4])		Write Preamble (A12)	Read Preamble (A11)	Reserved	Reserved
F4BC5x (DA[3:0])	MR5	Reserved	CA Parity Latency (A2:A0)		
F4BC5x (DA[7:4])		Reserved	Reserved	Reserved	Reserved
F4BC6x (DA[3:0])	MR6	Reserved	Reserved	Reserved	Reserved
F4BC6x (DA[7:4])		Reserved	Reserved	Reserved	Reserved

1. These bits only apply to regular MPR override reads, not to the BCW read response which supports only the serial data format.
2. The DDR4DB02 supports two modes in which MPR can be accessed for read. The two modes are serial return and parallel return. There is also an optional staggered return format described in Chapter 2.1.7.3, "Optional MPR Override Read Format for Staggered Returns,"

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4.46 F5BC0x .. F5BC3x & F6BC0x .. F6BC3x - Upper and Lower Multi Purpose Registers

The control word locations F5BC0x .. F5BC3x & F6BC0x .. F6BC3x are used to store lower and upper nibble data pattern bits for various training purposes. The first four of these control words are also used as DRAM equivalent Multi Purpose Registers. In this case each 8-bit control word (DA[7:0]) applies to both lower and upper nibble in a manner compatible with the behavior of a x8 DDR4 DRAM - see section 2.14 for details.

Table 73 — F5BC0x .. F5BC3x & F6BC0x .. F6BC3x: Upper and Lower Multi Purpose Registers

Control Word	UI[1]	Upper Nibble	Lower Nibble
		Setting (DA[7:4])	Setting (DA[3:0])
F5BC0x (DA[7:0]) = MPR0	UI0	DQ[7:4] default value = 0101	DQ[3:0] default value = 0101
F5BC1x (DA[7:0]) = MPR1	UI1	DQ[7:4] default value = 0011	DQ[3:0] default value = 0011
F5BC2x (DA[7:0]) = MPR2	UI2	DQ[7:4] default value = 0000	DQ[3:0] default value = 1111
F5BC3x (DA[7:0]) = MPR3	UI3	DQ[7:4] default value = 0000	DQ[3:0] default value = 0000
F6BC0x (DA[7:0]) = MPR4	UI4	DQ[7:4] default value = 0000	DQ[3:0] default value = 0000
F6BC1x (DA[7:0]) = MPR5	UI5	DQ[7:4] default value = 0000	DQ[3:0] default value = 0000
F6BC2x (DA[7:0]) = MPR6	UI6	DQ[7:4] default value = 0000	DQ[3:0] default value = 0000
F6BC3x (DA[7:0]) = MPR7	UI7	DQ[7:4] default value = 0000	DQ[3:0] default value = 0000

1. This field defines the burst order for the data pattern used for the MRD, MWD and HIW training modes. UIx stands for Unit Interval x, where x is a number from 0 to 7. UI0 is the first half cycle and UI7 the last half cycle of a BL8 burst of data. In MPR override mode only MPR[3:0] are utilized and the data format and burst order are documented in Table 6, Table 7 and for optional staggered format Table 8, Table 9, Table 10 and Table 11.

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4.47 F5BC5x - Host Interface VREF Control Word

Table 74 — F5BC5x: Host Interface VREF Control Word definition

Cmd (DA[7:0])								DQ VREF as % of V_{DD} Range 1[1]	DQ VREF as % of V_{DD} Range 2[1]
0	0	0	0	0	0	0	0	60.0%	45.0%
0	0	0	0	0	0	0	1	60.65%	45.65%
0	0	0	0	0	0	1	0	61.30%	46.30%
0	0	0	0	0	0	1	1	61.95%	46.95%
0	0	0	0	0	1	0	0	62.60%	47.60%
0	0	0	0	0	1	0	1	63.25%	48.25%
0	0	0	0	0	1	1	0	63.90%	48.90%
0	0	0	0	0	1	1	1	64.55%	49.55%
0	0	0	0	1	0	0	0	65.20%	50.20%
0	0	0	0	1	0	0	1	65.85%	50.85%
0	0	0	0	1	0	1	0	66.60%	51.60%
0	0	0	0	1	0	1	1	67.15%	52.15%
0	0	0	0	1	1	0	0	67.80%	52.80%
0	0	0	0	1	1	0	1	68.45%	53.45%
0	0	0	0	1	1	1	0	69.10%	54.10%
0	0	0	0	1	1	1	1	69.75%	54.75%
0	0	0	1	0	0	0	0	70.40%	55.40%
0	0	0	1	0	0	0	1	71.05%	56.05%
0	0	0	1	0	0	1	0	71.70%	56.70%
0	0	0	1	0	0	1	1	72.35%	57.35%
0	0	0	1	0	1	0	0	73.00%	58.00%
0	0	0	1	0	1	0	1	73.65%	58.65%
0	0	0	1	0	1	1	0	74.30%	59.30%
0	0	0	1	0	1	1	1	74.95%	59.95%
0	0	0	1	1	0	0	0	75.60%	60.60%
0	0	0	1	1	0	0	1	76.25%	61.25%
0	0	0	1	1	0	1	0	76.90%	61.90%
0	0	0	1	1	0	1	1	77.55%	62.55%
0	0	0	1	1	1	0	0	78.20%	63.20%
0	0	0	1	1	1	0	1	78.85%	63.85%
0	0	0	1	1	1	1	0	79.50%	64.50%
0	0	0	1	1	1	1	1	80.15%	65.15%
0	0	1	0	0	0	0	0	80.80%	65.80%
0	0	1	0	0	0	0	1	81.45%	66.45%
0	0	1	0	0	0	1	0	82.10%	67.10%
0	0	1	0	0	0	1	1	82.75%	67.75%
0	0	1	0	0	1	0	0	83.40%	68.40%
0	0	1	0	0	1	0	1	84.05%	69.05%
0	0	1	0	0	1	1	0	84.70%	69.70%
0	0	1	0	0	1	1	1	85.35%	70.35%
0	0	1	0	1	0	0	0	86.00%	71.00%
0	0	1	0	1	0	0	1	86.65%	71.65%
0	0	1	0	1	0	1	0	87.30%	72.30%
0	0	1	0	1	0	1	1	87.95%	72.95%
0	0	1	0	1	1	0	0	88.60%	73.60%
0	0	1	0	1	1	0	1	89.25%	74.25%
0	0	1	0	1	1	1	0	89.90%	74.90%
0	0	1	0	1	1	1	1	90.55%	75.55%
0	0	1	1	0	0	0	0	91.20%	76.20%
0	0	1	1	0	0	0	1	91.85%	76.85%
0	0	1	1	0	0	1	0	92.50%	77.50%
0	0	1	1	0	0	1	1	Reserved	Reserved
0	0	1	1	x	1	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x	Reserved	Reserved
1	0	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

1. These are target VrefDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

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4.48 F5BC6x - DRAM Interface VREF Control Word

Table 75 — F5BC6x: DRAM Interface VREF Control Word definition

Cmd (DA[7:0])								DQ VREF as % of V_{DD} Range 1[1]	DQ VREF as % of V_{DD} Range 2[1]
0	0	0	0	0	0	0	0	60.0%	45.0%
0	0	0	0	0	0	0	1	60.65%	45.65%
0	0	0	0	0	0	1	0	61.30%	46.30%
0	0	0	0	0	0	1	1	61.95%	46.95%
0	0	0	0	0	1	0	0	62.60%	47.60%
0	0	0	0	0	1	0	1	63.25%	48.25%
0	0	0	0	0	1	1	0	63.90%	48.90%
0	0	0	0	0	1	1	1	64.55%	49.55%
0	0	0	0	1	0	0	0	65.20%	50.20%
0	0	0	0	1	0	0	1	65.85%	50.85%
0	0	0	0	1	0	1	0	66.60%	51.60%
0	0	0	0	1	0	1	1	67.15%	52.15%
0	0	0	0	1	1	0	0	67.80%	52.80%
0	0	0	0	1	1	0	1	68.45%	53.45%
0	0	0	0	1	1	1	0	69.10%	54.10%
0	0	0	0	1	1	1	1	69.75%	54.75%
0	0	0	1	0	0	0	0	70.40%	55.40%
0	0	0	1	0	0	0	1	71.05%	56.05%
0	0	0	1	0	0	1	0	71.70%	56.70%
0	0	0	1	0	0	1	1	72.35%	57.35%
0	0	0	1	0	1	0	0	73.00%	58.00%
0	0	0	1	0	1	0	1	73.65%	58.65%
0	0	0	1	0	1	1	0	74.30%	59.30%
0	0	0	1	0	1	1	1	74.95%	59.95%
0	0	0	1	1	0	0	0	75.60%	60.60%
0	0	0	1	1	0	0	1	76.25%	61.25%
0	0	0	1	1	0	1	0	76.90%	61.90%
0	0	0	1	1	0	1	1	77.55%	62.55%
0	0	0	1	1	1	0	0	78.20%	63.20%
0	0	0	1	1	1	0	1	78.85%	63.85%
0	0	0	1	1	1	1	0	79.50%	64.50%
0	0	0	1	1	1	1	1	80.15%	65.15%
0	0	1	0	0	0	0	0	80.80%	65.80%
0	0	1	0	0	0	0	1	81.45%	66.45%
0	0	1	0	0	0	1	0	82.10%	67.10%
0	0	1	0	0	0	1	1	82.75%	67.75%
0	0	1	0	0	1	0	0	83.40%	68.40%
0	0	1	0	0	1	0	1	84.05%	69.05%
0	0	1	0	0	1	1	0	84.70%	69.70%
0	0	1	0	0	1	1	1	85.35%	70.35%
0	0	1	0	1	0	0	0	86.00%	71.00%
0	0	1	0	1	0	0	1	86.65%	71.65%
0	0	1	0	1	0	1	0	87.30%	72.30%
0	0	1	0	1	0	1	1	87.95%	72.95%
0	0	1	0	1	1	0	0	88.60%	73.60%
0	0	1	0	1	1	0	1	89.25%	74.25%
0	0	1	0	1	1	1	0	89.90%	74.90%
0	0	1	0	1	1	1	1	90.55%	75.55%
0	0	1	1	0	0	0	0	91.20%	76.20%
0	0	1	1	0	0	0	1	91.85%	76.85%
0	0	1	1	0	0	1	0	92.50%	77.50%
0	0	1	1	0	0	1	1	Reserved	Reserved
0	0	1	1	x	1	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x	Reserved	Reserved
1	0	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

1. These are target VrefDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

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4.49 Host side DFE_VREF for Training

Table 76 — F5BC6x: DRAM Interface VREF Control Word (& Host DFE_VREF for Training)[1]

F5BC6x							Host DFE_VREF Training as% of Implementation Specific Maximum Sweep Voltage[2]							
							F6BC4x - DA2 = 0 (Range 1)				F6BC4x - DA2 = 1 (Range 2)			
DA7	DA6	DA5	DA4	DA3	DA2	DA[1:0]	00	01	10	11	00	01	10	11
0	0	0	0	0	0		- 0.0%	- 0.5%	- 1.0%	- 1.5%	+ 0.0%	+ 0.5%	+ 1.0%	+ 1.5%
0	0	0	0	0	1		- 2.0%	- 2.5%	- 3.0%	- 3.5%	+ 2.0%	+ 2.5%	+ 3.0%	+ 3.5%
0	0	0	0	1	0		- 4.0%	- 4.5%	- 5.0%	- 5.5%	+ 4.0%	+ 4.5%	+ 5.0%	+ 5.5%
0	0	0	0	1	1		- 6.0%	- 6.5%	- 7.0%	- 7.5%	+ 6.0%	+ 6.5%	+ 7.0%	+ 7.5%
0	0	0	1	0	0		- 8.0%	- 8.5%	- 9.0%	- 9.5%	+ 8.0%	+ 8.5%	+ 9.0%	+ 9.5%
0	0	0	1	0	1		- 10.0%	- 10.5%	- 11.0%	- 11.5%	+ 10.0%	+ 10.5%	+ 11.0%	+ 11.5%
0	0	0	1	1	0		- 12.0%	- 12.5%	- 13.0%	- 13.5%	+ 12.0%	+ 12.5%	+ 13.0%	+ 13.5%
0	0	0	1	1	1		- 14.0%	- 14.5%	- 15.0%	- 15.5%	+ 14.0%	+ 14.5%	+ 15.0%	+ 15.5%
0	0	1	0	0	0		- 16.0%	- 16.5%	- 17.0%	- 17.5%	+ 16.0%	+ 16.5%	+ 17.0%	+ 17.5%
0	0	1	0	0	1		- 18.0%	- 18.5%	- 19.0%	- 19.5%	+ 18.0%	+ 18.5%	+ 19.0%	+ 19.5%
0	0	1	0	1	0		- 20.0%	- 20.5%	- 21.0%	- 21.5%	+ 20.0%	+ 20.5%	+ 21.0%	+ 21.5%
0	0	1	0	1	1		- 22.0%	- 22.5%	- 23.0%	- 23.5%	+ 22.0%	+ 22.5%	+ 23.0%	+ 23.5%
0	0	1	1	0	0		- 24.0%	- 24.5%	- 25.0%	- 25.5%	+ 24.0%	+ 24.5%	+ 25.0%	+ 25.5%
0	0	1	1	0	1		- 26.0%	- 26.5%	- 27.0%	- 27.5%	+ 26.0%	+ 26.5%	+ 27.0%	+ 27.5%
0	0	1	1	1	0		- 28.0%	- 28.5%	- 29.0%	- 29.5%	+ 28.0%	+ 28.5%	+ 29.0%	+ 29.5%
0	0	1	1	1	1		- 30.0%	- 30.5%	- 31.0%	- 31.5%	+ 30.0%	+ 30.5%	+ 31.0%	+ 31.5%
0	1	0	0	0	0		- 32.0%	- 32.5%	- 33.0%	- 33.5%	+ 32.0%	+ 32.5%	+ 33.0%	+ 33.5%
0	1	0	0	0	1		- 34.0%	- 34.5%	- 35.0%	- 35.5%	+ 34.0%	+ 34.5%	+ 35.0%	+ 35.5%
0	1	0	0	1	0		- 36.0%	- 36.5%	- 37.0%	- 37.5%	+ 36.0%	+ 36.5%	+ 37.0%	+ 37.5%
0	1	0	0	1	1		- 38.0%	- 38.5%	- 39.0%	- 39.5%	+ 38.0%	+ 38.5%	+ 39.0%	+ 39.5%
0	1	0	1	0	0		- 40.0%	- 40.5%	- 41.0%	- 41.5%	+ 40.0%	+ 40.5%	+ 41.0%	+ 41.5%
0	1	0	1	0	1		- 42.0%	- 42.5%	- 43.0%	- 43.5%	+ 42.0%	+ 42.5%	+ 43.0%	+ 43.5%
0	1	0	1	1	0		- 44.0%	- 44.5%	- 45.0%	- 45.5%	+ 44.0%	+ 44.5%	+ 45.0%	+ 45.5%
0	1	0	1	1	1		- 46.0%	- 46.5%	- 47.0%	- 47.5%	+ 46.0%	+ 46.5%	+ 47.0%	+ 47.5%
0	1	1	0	0	0		- 48.0%	- 48.5%	- 49.0%	- 49.5%	+ 48.0%	+ 48.5%	+ 49.0%	+ 49.5%
0	1	1	0	0	1		- 50.0%	- 50.5%	- 51.0%	- 51.5%	+ 50.0%	+ 50.5%	+ 51.0%	+ 51.5%
0	1	1	0	1	0		- 52.0%	- 52.5%	- 53.0%	- 53.5%	+ 52.0%	+ 52.5%	+ 53.0%	+ 53.5%
0	1	1	0	1	1		- 54.0%	- 54.5%	- 55.0%	- 55.5%	+ 54.0%	+ 54.5%	+ 55.0%	+ 55.5%
0	1	1	1	0	0		- 56.0%	- 56.5%	- 57.0%	- 57.5%	+ 56.0%	+ 56.5%	+ 57.0%	+ 57.5%
0	1	1	1	0	1		- 58.0%	- 58.5%	- 59.0%	- 59.5%	+ 58.0%	+ 58.5%	+ 59.0%	+ 59.5%
0	1	1	1	1	0		- 60.0%	- 60.5%	- 61.0%	- 61.5%	+ 60.0%	+ 60.5%	+ 61.0%	+ 61.5%
0	1	1	1	1	1		- 62.0%	- 62.5%	- 63.0%	- 63.5%	+ 62.0%	+ 62.5%	+ 63.0%	+ 63.5%
1	0	0	0	0	0		- 64.0%	- 64.5%	- 65.0%	- 65.5%	+ 64.0%	+ 64.5%	+ 65.0%	+ 65.5%
1	0	0	0	0	1		- 66.0%	- 66.5%	- 67.0%	- 67.5%	+ 66.0%	+ 66.5%	+ 67.0%	+ 67.5%
1	0	0	0	1	0		- 68.0%	- 68.5%	- 69.0%	- 69.5%	+ 68.0%	+ 68.5%	+ 69.0%	+ 69.5%
1	0	0	0	1	1		- 70.0%	- 70.5%	- 71.0%	- 71.5%	+ 70.0%	+ 70.5%	+ 71.0%	+ 71.5%
1	0	0	1	0	0		- 72.0%	- 72.5%	- 73.0%	- 73.5%	+ 72.0%	+ 72.5%	+ 73.0%	+ 73.5%
1	0	0	1	0	1		- 74.0%	- 74.5%	- 75.0%	- 75.5%	+ 74.0%	+ 74.5%	+ 75.0%	+ 75.5%
1	0	0	1	1	0		- 76.0%	- 76.5%	- 77.0%	- 77.5%	+ 76.0%	+ 76.5%	+ 77.0%	+ 77.5%
1	0	0	1	1	1		- 78.0%	- 78.5%	- 79.0%	- 79.5%	+ 78.0%	+ 78.5%	+ 79.0%	+ 79.5%
1	0	1	0	0	0		- 80.0%	- 80.5%	- 81.0%	- 81.5%	+ 80.0%	+ 80.5%	+ 81.0%	+ 81.5%
1	0	1	0	0	1		- 82.0%	- 82.5%	- 83.0%	- 83.5%	+ 82.0%	+ 82.5%	+ 83.0%	+ 83.5%
1	0	1	0	1	0		- 84.0%	- 84.5%	- 85.0%	- 85.5%	+ 84.0%	+ 84.5%	+ 85.0%	+ 85.5%
1	0	1	0	1	1		- 86.0%	- 86.5%	- 87.0%	- 87.5%	+ 86.0%	+ 86.5%	+ 87.0%	+ 87.5%
1	0	1	1	0	0		- 88.0%	- 88.5%	- 89.0%	- 89.5%	+ 88.0%	+ 88.5%	+ 89.0%	+ 89.5%
1	0	1	1	0	1		- 90.0%	- 90.5%	- 91.0%	- 91.5%	+ 90.0%	+ 90.5%	+ 91.0%	+ 91.5%
1	0	1	1	1	0		- 92.0%	- 92.5%	- 93.0%	- 93.5%	+ 92.0%	+ 92.5%	+ 93.0%	+ 93.5%
1	0	1	1	1	1		- 94.0%	- 94.5%	- 95.0%	- 95.5%	+ 94.0%	+ 94.5%	+ 95.0%	+ 95.5%
1	1	0	0	0	0		- 96.0%	- 96.5%	- 97.0%	- 97.5%	+ 96.0%	+ 96.5%	+ 97.0%	+ 97.5%
1	1	0	0	0	1		- 98.0%	- 98.5%	- 99.0%	- 99.5%	+ 98.0%	+ 98.5%	+ 99.0%	+ 99.5%
1	1	0	0	1	0		- 100.0%	Reserved	Reserved	Reserved	+ 100.0%	Reserved	Reserved	Reserved
1	1	0	0	1	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	1		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Ex. 1058, p. 82
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1. This table is only applicable when F2BCFx - DA7 (for any one of the DQn pins) is set to 1.
2. The steps in Table 76 are vendor specific DFE training steps in percentage of the total Voltage Swing around DFE Common Mode over process, voltage and temperature, It is not a percentage of VDD, see Figure 14.

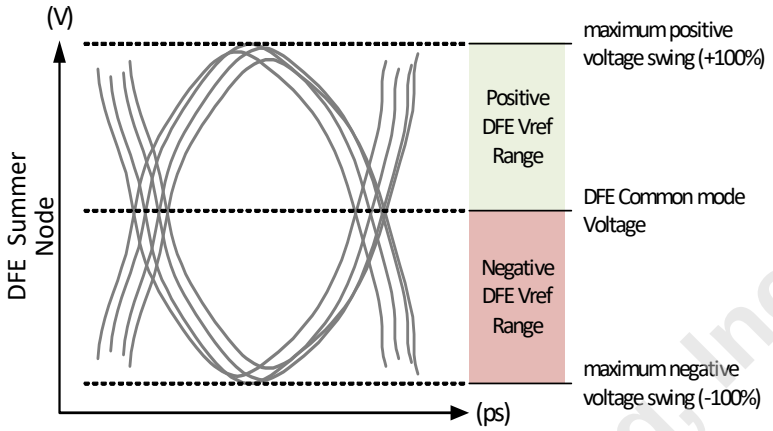

Figure 14 — Host DFE Training VREF Definition

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4.50 F6BC4x - Buffer Training Configuration Control Word

This control word configures the data buffer for the training modes MRD, MWD and HIW and affects the results in F6BC5x.

To reduce the amount of bits for the buffer training status, a subset of the results of the bitwise XNOR comparison between one burst of read or write data (=64 bits) and the 64-bit expected data in the eight MPR registers can be selected in the buffer training configuration control word.

A simple pass/fail information of the entire 64-bit compare operation is also available in BC0F, DA3.

The affected training step needs to be performed again after each change to F6BC4x for the change to become effective.

Table 77 — F6BC4x: Buffer Training Configuration Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	Status on DQ outputs	Per nibble, i.e. drive ‘0’ on all four DQ bits within nibble if any bit within a nibble burst is wrong
x	x	x	x	x	x	x	1		Per lane, i.e. drive ‘0’ only on a particular DQx output if there if any bit in that lane is wrong during a burst
x	x	x	x	x	x	0	x	Host Interface VrefDQ Training Range	Range 1
x	x	x	x	x	x	1	x		Range 2
x	x	x	x	x	0	x	x	DRAM Interface VrefDQ Training Range	Range 1
x	x	x	x	x	1	x	x		Range 2
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Select 8-bits of comparison data	Select 1 of 8 bit lanes (0 to 7) for the entire burst
x	x	x	1	x	x	x	x		Select 1 of 8 Unit Intervals (0 to 7) within a burst
0	0	0	x	x	x	x	x	Select 1 of 8 bit lanes or UIs	Bit lane 0 or UI0
0	0	1	x	x	x	x	x		Bit lane 1 or UI1
0	1	0	x	x	x	x	x		Bit lane 2 or UI2
0	1	1	x	x	x	x	x		Bit lane 3 or UI3
1	0	0	x	x	x	x	x		Bit lane 4 or UI4
1	0	1	x	x	x	x	x		Bit lane 5 or UI5
1	1	0	x	x	x	x	x		Bit lane 6 or UI6
1	1	1	x	x	x	x	x		Bit lane 7 or UI7

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4.51 F6BC5x - Buffer Training Status Word

This control word contains status information that indicates the result of certain training modes.

The state of each bit in the Buffer Training Status Word must be preserved when the DDR4DB02 enters or exits any training mode. This is needed because in most cases the data buffer needs to be taken out of training mode before the host controller can access the Buffer Training Status Word by means of BCW Read commands. The DDR4DB02 hardware should only update the state of the Buffer Training Status Word when a new result is generated by the corresponding training logic.

Table 78 — F6BC5x: Buffer Training Status Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	Bit lane 0 or UI0 status	Contains either 8 bits within one UI or 8 UIs for a given data lane based on the selection in F6BC4x, DA4
x	x	x	x	x	x	x	1		
x	x	x	x	x	x	0	x	Bit lane 1 or UI1 status	
x	x	x	x	x	x	1	x		
x	x	x	x	x	0	x	x	Bit lane 2 or UI2 status	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	Bit lane 3 or UI3 status	
x	x	x	x	1	x	x	x		
x	x	x	0	x	x	x	x	Bit lane 4 or UI4 status	
x	x	x	1	x	x	x	x		
x	x	0	x	x	x	x	x	Bit lane 5 or UI5 status	
x	x	1	x	x	x	x	x		
x	0	x	x	x	x	x	x	Bit lane 6 or UI6 status	
x	1	x	x	x	x	x	x		
0	x	x	x	x	x	x	x	Bit lane 7 or UI7 status	
1	x	x	x	x	x	x	x		

4.52 F7BC0x .. F7BC3x - Error Log Register

The control word locations F70x .. F73x function as a 32-bit error log register. Upon occurrence of a parity or protocol error the device logs the sampled offending command sequence in the Error Log Register using the bit arrangement shown in Table 79 below. The Error Log Register can be read by the host by means of the BCW read command sequence.

Table 79 — F7BC0x .. F7BC3x: Error Log Register

Control Word	Command Sequence					
	WR	RD	MRS Write	BCW Write	BCW Read	Non-Command[1]
F7BC0x (DA[3:0])	CMD[3:0][2]	CMD[3:0][3]	CMD[3:0][4]	CMD[3:0][5]	CMD[3:0][6]	DAT[3:0]
F7BC0x (DA[7:4])	DAT0[3:0]	DAT0[3:0]	DAT0[3:0]	DAT0[3:0]	DAT0[3:0]	0000
F7BC1x (DA[3:0])	PAR[3:0]	PAR[3:0]	DAT1[3:0]	DAT1[3:0]	DAT1[3:0]	0000
F7BC1x (DA[7:4])	0000	0000	DAT2[3:0]	DAT2[3:0]	DAT2[3:0]	0000
F7BC2x (DA[3:0])	0000	0000	DAT3[3:0]	DAT3[3:0]	DAT3[3:0]	0000
F7BC2x (DA[7:4])	0000	0000	DAT4[3:0]	DAT4[3:0]	PAR[3:0]	0000
F7BC3x (DA[3:0])	0000	0000	DAT5[3:0]	PAR[3:0]	0000	0000
F7BC3x (DA[7:4])	0000	0000	PAR[3:0]	0000	0000	0000

1. This sequence error occurs when a command is expected but a non-command pattern is received (i.e. BCOM3=0)
2. For WR commands the expected value of CMD[3:0] is 1000.
3. For RD commands the expected value of CMD[3:0] is 1001.
4. For MRS Write commands the expected value of CMD[3:0] is 1011.
5. For BCW Write commands the expected value of CMD[3:0] is 1100.
6. For BCW Read commands the expected value of CMD[3:0] is 1101.

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4.53 F[7:4]BC8x - MDQ0/4 Read Delay Control Word

The control word location F[7:4]BC8x is used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in F[3:0]BC4x and F[3:0]BC5x

Table 80 — F[7:4]BC8x: MDQ0/4 Read Delay Control Word.

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Phase Control Between MDQ0 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ0 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ0 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ0 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ0 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ4 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The delay of the lower/upper nibble MDQS_t/MDQS_c signals received by the DDR4 buffer during read commands is set by F[3:0]BC4x/F[3:0]BC5x. The F[7:4]BC8x - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline delay for a more optimal position.
2. The F[7:4]BC8x - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline delay for a more optimal position.

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4.54 F[7:4]BC9x - MDQ1/5 Read Delay Control Word

The control word location F[7:4]BC9x is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in F[3:0]BC4x and F[3:0]BC5x.

Table 81 — F[7:4]BC9x: MDQ1/5 Read Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Phase Control Between MDQ1 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ1 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ1 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ1 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ1 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ5 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ5with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ5with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The delay of the lower/upper nibble MDQS_t/MDQS_c signals received by the DDR4 buffer during read commands is set by F[3:0]BC4x/F[3:0]BC5x. The F[7:4]BC9x - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline delay for a more optimal position.
2. The F[7:4]BC9x - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline delay for a more optimal position.

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4.55 F[7:4]BCAx - MDQ2/6 Read Delay Control Word

The control word location F[7:4]BCAx is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in F[3:0]BC4x and F[3:0]BC5x.

Table 82 — F[7:4]BCAx: MDQ2/6 Read Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Phase Control Between MDQ2 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ2 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ2 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ2 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ2 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ6 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ6with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The delay of the lower/upper nibble MDQS_t/MDQS_c signals received by the DDR4 buffer during read commands is set by F[3:0]BC4x/F[3:0]BC5x. The F[7:4]BCAx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline delay for a more optimal position.
2. The F[7:4]BCAx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline delay for a more optimal position.

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4.56 F[7:4]BCBx - MDQ3/7 Read Delay Control Word

The control word location F[7:4]BCBx is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in F[3:0]BC4x and F[3:0]BC5x.

Table 83 — F[7:4]BCBx: MDQ3/7 Read Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Phase Control Between MDQ3 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ3 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ3 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ3 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ3 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ7 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ7 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The delay of the lower/upper nibble MDQS_t/MDQS_c signals received by the DDR4 buffer during read commands is set by F[3:0]BC4x/F[3:0]BC5x. The F[7:4]BCBx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline delay for a more optimal position.
2. The F[7:4]BCBx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline delay for a more optimal position.

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4.57 F[7:4]BCCx - MDQ0/4-MDQS Write Delay Control Word

The control word location F[7:4]BCCx is used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in F[3:0]BC8x and F[3:0]BC9x.

Table 84 — F[7:4]BCCx: MDQ0/4-MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Phase Control Between MDQ0 and Lower Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ0 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	0	0	0	1		Delay MDQ0 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	0	0	1	0		Delay MDQ0 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	0	0	1	1		Delay MDQ0 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	0	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	0	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	0	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	0	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ4 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * t_{CK} (same as default)
0	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * t_{CK}
0	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * t_{CK}
0	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The phase between the lower/upper nibble MDQ and MDQS signals driven by the DDR4 buffer during write commands is set by F[3:0]BC8x/F[3:0]BC9x. The F[7:4]BCCx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline for a more optimal position.
2. The F[7:4]BCCx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline for a more optimal position.

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4.58 F[7:4]BCDx - MDQ1/5-MDQS Write Delay Control Word

The control word location F[7:4]BCDx is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in F[3:0]BC8x and F[3:0]BC9x.

Table 85 — F[7:4]BCDx: MDQ1/5 - MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Phase Control Between MDQ1 and Lower Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ1 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	0	0	0	1		Delay MDQ1 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	0	0	1	0		Delay MDQ1 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	0	0	1	1		Delay MDQ1 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	0	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	0	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	0	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	0	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ5 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ5 with respect to baseline by -0/64 * t_{CK} (same as default)
0	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * t_{CK}
0	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * t_{CK}
0	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The phase between the lower/upper nibble MDQ and MDQS signals driven by the DDR4 buffer during write commands is set by F[3:0]BC8x/F[3:0]BC9x. The F[7:4]BCDx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline for a more optimal position.
2. The F[7:4]BCDx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline for a more optimal position.

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4.59 F[7:4]BCEx - MDQ2/6-MDQS Write Delay Control Word

The control word location F[7:4]BCEx is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in F[3:0]BC8x and F[3:0]BC9x.

Table 86 — F[7:4]BCEx: MDQ2/6 - MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Phase Control Between MDQ2 and Lower Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ2 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	0	0	0	1		Delay MDQ2 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	0	0	1	0		Delay MDQ2 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	0	0	1	1		Delay MDQ02with respect to baseline by +3/64 * t_{CK}
x	x	x	x	0	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	0	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	0	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	0	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ6 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * t_{CK} (same as default)
0	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * t_{CK}
0	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * t_{CK}
0	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The phase between the lower/upper nibble MDQ and MDQS signals driven by the DDR4 buffer during write commands is set by F[3:0]BC8x/F[3:0]BC9x. The F[7:4]BCEx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline for a more optimal position.
2. The F[7:4]BCEx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline for a more optimal position.

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4.60 F[7:4]BCFx - MDQ3/7-MDQS Write Delay Control Word

The control word location F[7:4]BCFx is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in F[3:0]BC8x and F[3:0]BC9x.

Table 87 — F[7:4]BCFx: MDQ3/7 - MDQS Write Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Phase Control Between MDQ3 and Lower Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[1]	Delay MDQ3 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	0	0	0	1		Delay MDQ3 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	0	0	1	0		Delay MDQ3 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	0	0	1	1		Delay MDQ3 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	0	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	0	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	0	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	0	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
0	0	0	0	x	x	x	x	Phase Control Between MDQ7and Upper Nibble Baseline MDQ-MDQS Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ7 with respect to baseline by +0/64 * t_{CK} (Default)
0	0	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by +1/64 * t_{CK}
0	0	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by +2/64 * t_{CK}
0	0	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by +3/64 * t_{CK}
0	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * t_{CK} (same as default)
0	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * t_{CK}
0	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * t_{CK}
0	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The phase between the lower/upper nibble MDQ and MDQS signals driven by the DDR4 buffer during write commands is set by F[3:0]BC8x/F[3:0]BC9x. The F[7:4]BCFx - DA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline for a more optimal position.
2. The F[7:4]BCFx - DA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline for a more optimal position.

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4.61 Logic Diagram

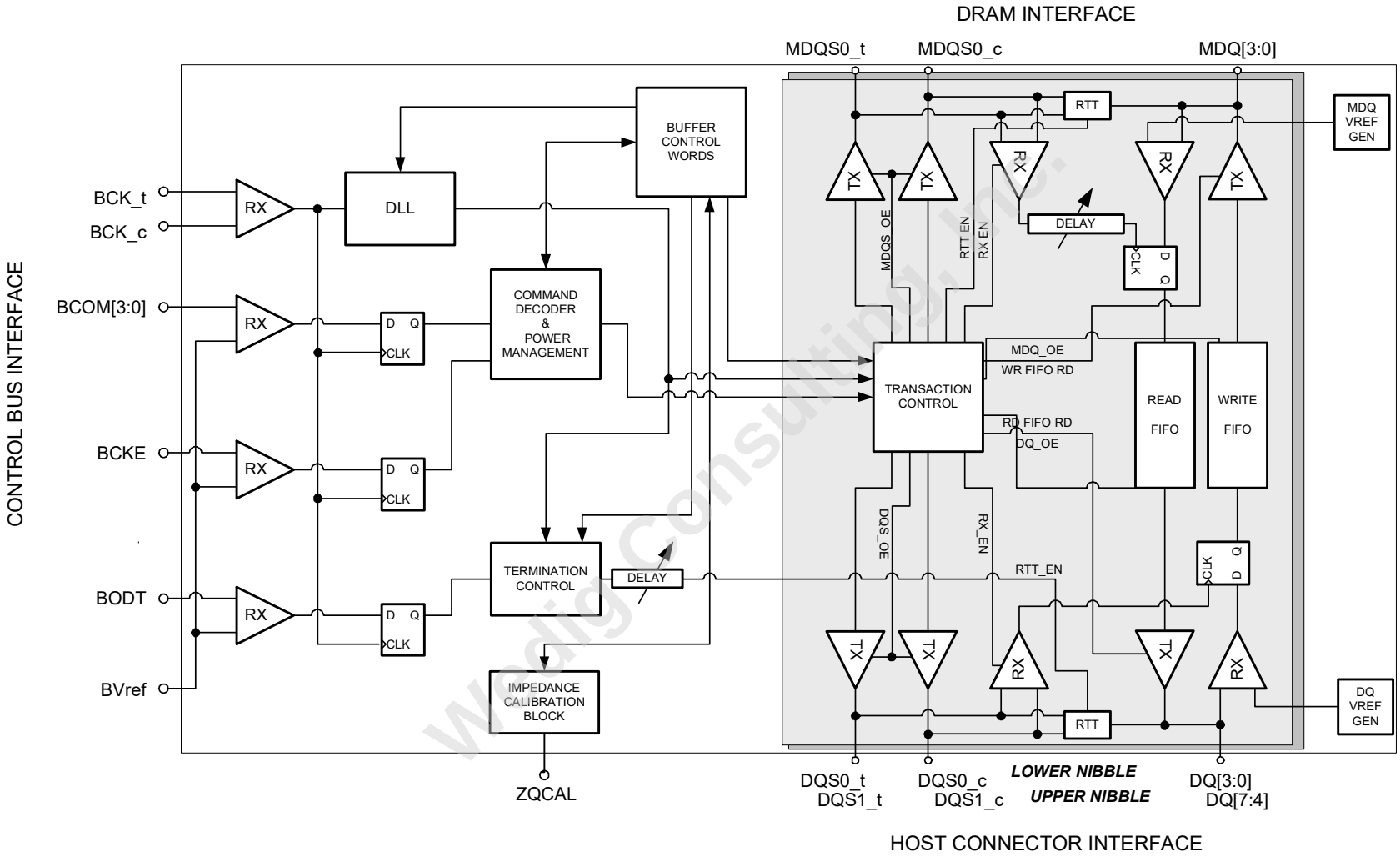

Figure 15 — Logic Diagram

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5 Absolute maximum ratings

Table 88 — Absolute maximum ratings over operating free-air temperature range [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.3	1.5	V
V_{IN}	Receiver input voltage	See Note 2 and 3	–0.3	V_{DD} + 0.5	V
BVrefCA	Reference voltage		–0.3	V_{DD} + 0.5	V
V_{OUT}	Driver output voltage	See Note 2 and 3	–0.3	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	±50	mA
I_{OUT}	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or V_{SS} pin		-	±100	mA
T_{stg}	Storage temperature		–65	+150	°C

NOTE 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3: This value is limited to 1.50 V maximum.

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6 Input AC and DC Specifications

The DDR4DB02 parametric values are specified for the device default control word settings, unless otherwise stated. The device must meet the electrical and timing characteristics with any programmed driver strength setting. Note that the BC0A setting does not affect any of the parametric values.

Table 89 — Operating Electrical Characteristics

Symbol	Parameter	Applicable Signals	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]		1.2 V Operation	1.14	1.2	1.26	V
BVrefCA	DC Reference voltage[1]			0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V
$V_{IL(static)}$	LOW-level input voltage	BCK_t, BCK_c during clock stop		0	-	0.35 x V_{DD}	V
V_{IX}(BCK)	Differential input cross point voltage range	BCK_t, BCK_c		see Table 96			
V_{IX_EX}(BCK)	Extended differential input cross point voltage range	BCK_t, BCK_c					
$V_{CM(DC)}$	Average common mode DC voltage			0.46 x V_{DD}	0.5 x V_{DD}	0.54 x V_{DD}	V
V_{SEH}	Single-ended high level			see Table 95			
V_{SEL}	Single-ended low level						
$V_{IH(AC)}$	AC input high			see Table 93			
$V_{IL(AC)}$	AC input low						
V_{IHdiff}	Differential input high						
V_{ILdiff}	Differential input low						
$V_{IHdiff(AC)}$	AC differential input high						
$V_{ILdiff(AC)}$	AC differential input low						
$V_{OH(AC)}$	AC output high	All outputs except ALERT_n		see Table 109			
$V_{OL(AC)}$	AC output low						
$V_{OH(DC)}$	DC output high						
$V_{OM(DC)}$	DC output mid						
$V_{OL(DC)}$	DC output low						
$V_{OHdiff(AC)}$	AC differential output high			see Table 110			
$V_{OLdiff(AC)}$	AC differential output low						
T_j	Junction temperature[2]			0	-	125	°C
T_{case}	Case temperature		Measurement procedure JESD51-2	-	-	103[3]	°C
T_{j_ext}	Extended junction temperature[4,5]			-40	-	125	°C
T_{case_ext}	Extended case temperature[4]		Measurement procedure JESD51-2	-40	-	103[6]	°C

1. DC bandwidth limits to 20 MHz for V_{DD} and BVrefCA.
2. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a Tj of 125 °C by the device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a device shall not be higher than 125 °C.
4. Extended temperature range support is an optional feature. Devices supporting this feature are identified by appending "X" to the device name. For example, DDR4DB02X and DDR4DB02NVX support extended temperature range while DDR4DB02 and DDR4DB02NV do not support extended temperature range.
5. For operation beyond Tj_ext min and max datasheet values are not guaranteed and may de-rate. For operation above Tj_ext max lifetime could be affected. All parametric measurements are performed at -40 °C, 25 °C and 95 °C.
6. This spec is meant to guarantee a Tj_ext of 125 °C by the DDR4RCD02. Since Tj_ext cannot be measured or observed by users, Tcase_ext is specified instead. Under all thermal condition, the Tj_ext of a device shall not be higher than 125 °C.

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6.1 Data Buffer Input Receiver Specifications

6.1.1 DQ Input Receiver Specifications

The DQ input receiver mask for voltage and timing is shown in Figure 16. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR4DB02 input receiver to successfully capture a valid input signal with BER < 1e-16. The mask is a receiver property for each pin and it is not the valid data eye.

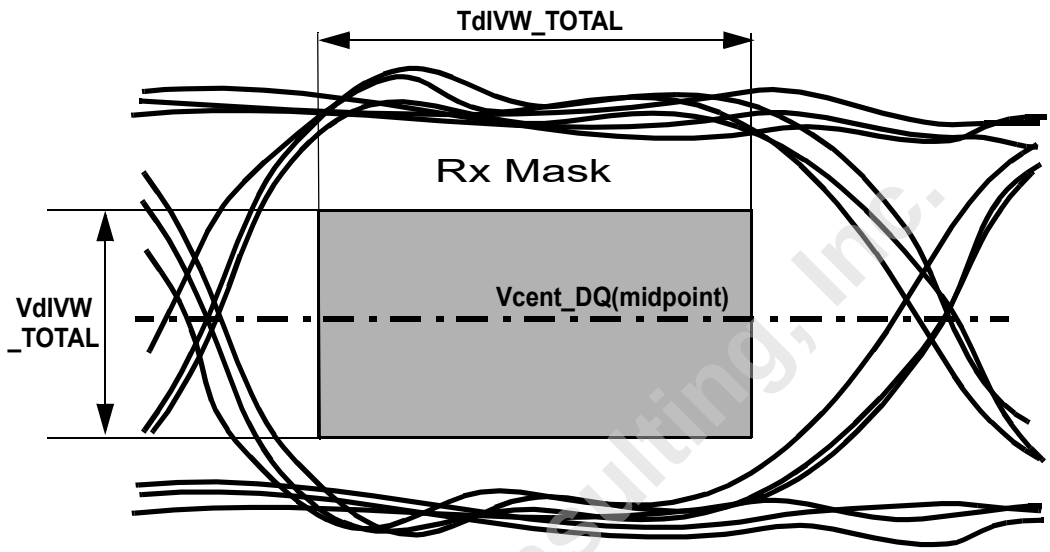

Figure 16 — DQ Receiver(Rx) mask

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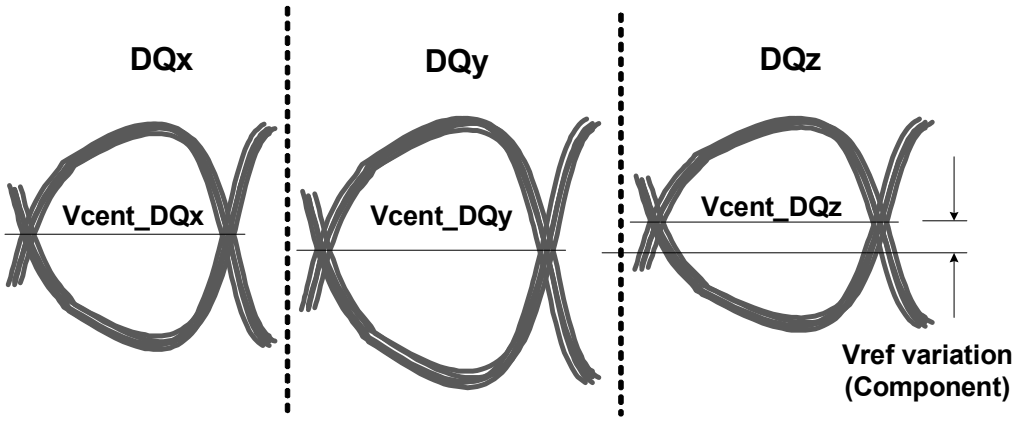

Figure 17 — Across pin Vcent_DQ voltage variation

Vcent_DQ(midpoint) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DDR4DB02 component. Each DQ pin Vcent level is defined by the center, i.e. widest opening of the cumulative data input eye as depicted in Figure 17. This clarifies that any DDR4DB02 component level variation must be accounted for within the DDR4DB02 Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

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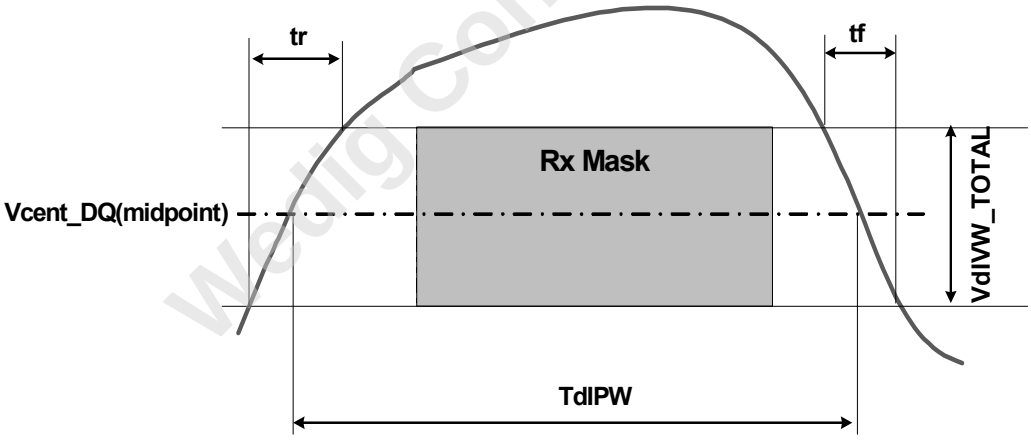

NOTE 1: SRIN_dIVW = VdIVW_TOTAL / (tr or tf)

Figure 18 — DQ TdIPW and SRIN_dIVW definition (for each input pulse)

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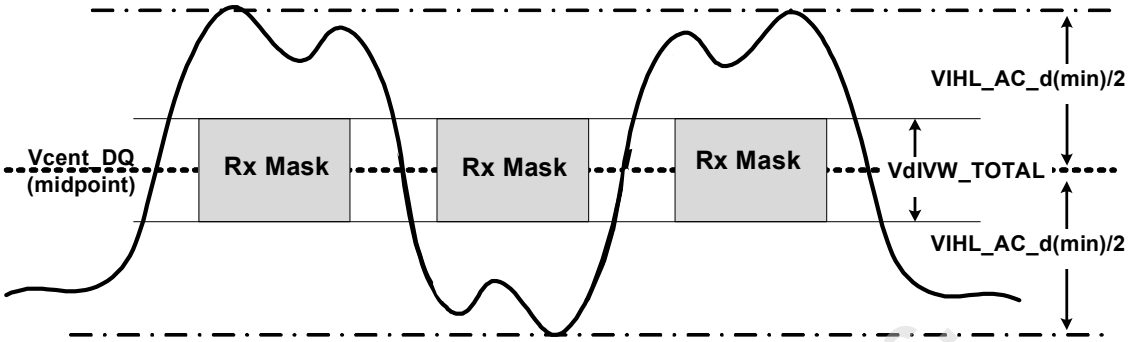

NOTE 1: The VIHL_AC_d requirement has to be met for any UI making a transition. It does not have to be met for a UI when there is no signal transition.

Figure 19 — VIHL_AC_d(min) requirement (for each input pulse)

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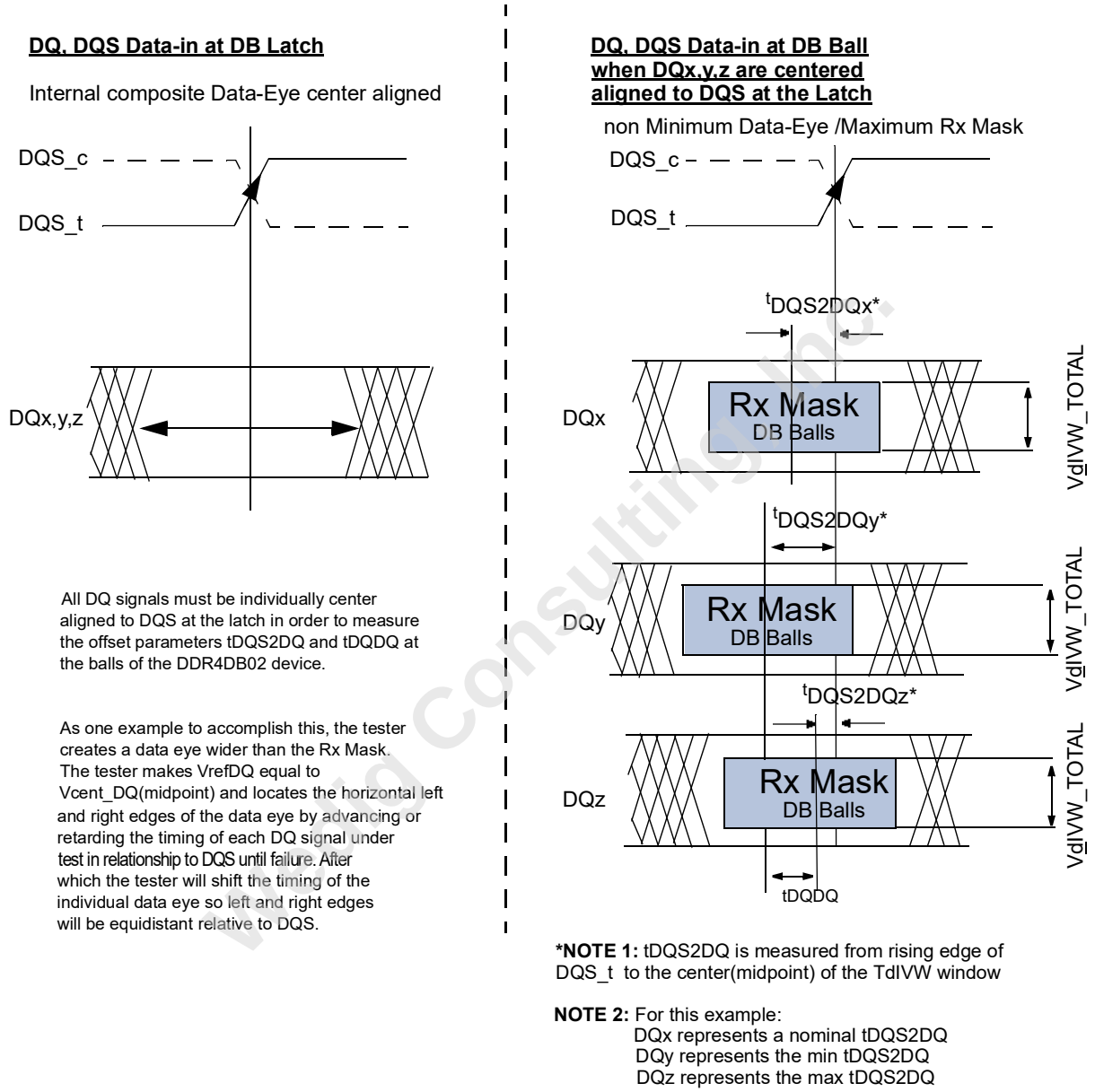

Figure 20 — DQS to DQ Timings at the DDR4DB02 balls referenced from the internal latch

All of the timing terms in Figure 20 are measured from DQS_t/DQS_c to the center(midpoint) of the TdIVW window taken at the VdIVW_TOTAL voltage levels centered around Vcent_DQ(midpoint). In Figure 17 the timings at the balls are referenced with respect to all DQ signals center aligned to the DDR4DB02 internal latch. The data to data offset tDQDQ is defined as the magnitude of the difference between the min and max tDQS2DQ for a given component.

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Table 90 — DQ/DQS Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600/1866/2133/ 2400/2666/2933/3200

Speed		DDR4-1600/1866/2133		DDR4-2400		DRR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Voltage and Timing													
VdIVW_TOTAL	DQ Rx Mask p-p voltage total	-	130	-	100	-	100	-	90	-	80	mV	1,2,3,4, 5
TdIVW_TOTAL	DQ Rx timing window total	-	0.2	-	0.15	-	0.15	-	0.13	-	0.13	UI	1, 4,5
VIHL_AC_d	DQ AC input pulse amplitude pk-pk	160	-	140	-	140	-	130	-	120	-	mV	6
TdIPW	DQ input pulse width	0.5	-	0.4	-	0.4	-	0.35	-	0.35	-	UI	7
tDQS2DQ	DQS to DQ offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	8
tDQDQ	DQ to DQ offset	-	0.04	-	0.04	-	0.043	-	0.043	-	0.043	UI	9
SRIN_dIVW	Input Slew Rate over VdIVW_TOTAL	1	9	1	9	1	9	1	9	1	9	V/ns	10

* UI=tck(avg)min/2

NOTE 1: Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint). The data Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER ≤1e-16.
NOTE 2: Rx mask voltage AC swing peak-peak requirement over TdIVW_TOTAL with at least half of VdIVW_TOTAL(max) above Vcent_DQ(midpoint) and at least half of VdIVW_TOTAL(max) below Vcent_DQ(midpoint).
NOTE 3: The VdIVW voltage levels are centered around Vcent_DQ(midpoint).
NOTE 4: Defined over the DQ internal Vref range 1.
NOTE 5: Overshoot and Undershoot Specifications see Table 101 and Figure 37.
NOTE 6: DQ input pulse signal swing into the receiver must meet or exceed VIHL_AC_d for at least one point over the duration of TdIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC_d is the peak to peak voltage centered around Vcent_DQ(midpoint), which is defined in Figure 17.
NOTE 7: DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
NOTE 8: DQS to DQ offset is within a nibble at DDR4DB02 balls. Includes all DDR4DB02 process, voltage and temperature variation.
NOTE 9: DQ to DQ offset is defined as the magnitude of the difference between the min and max DQS to DQ offset within a nibble at DDR4DB02 balls for a given component. Includes all DDR4DB02 voltage and temperature variation.
NOTE 10: Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). This single-ended slew rate also applies to DQS_t and DQS_c.

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6.1.2 MDQ Input Receiver Specifications

The MDQ input receiver mask for voltage and timing is shown in Figure 21. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR4DB02 input receiver to successfully capture a valid input signal with BER < 1e-16. The mask is a receiver property for each pin and it is not the valid data eye.

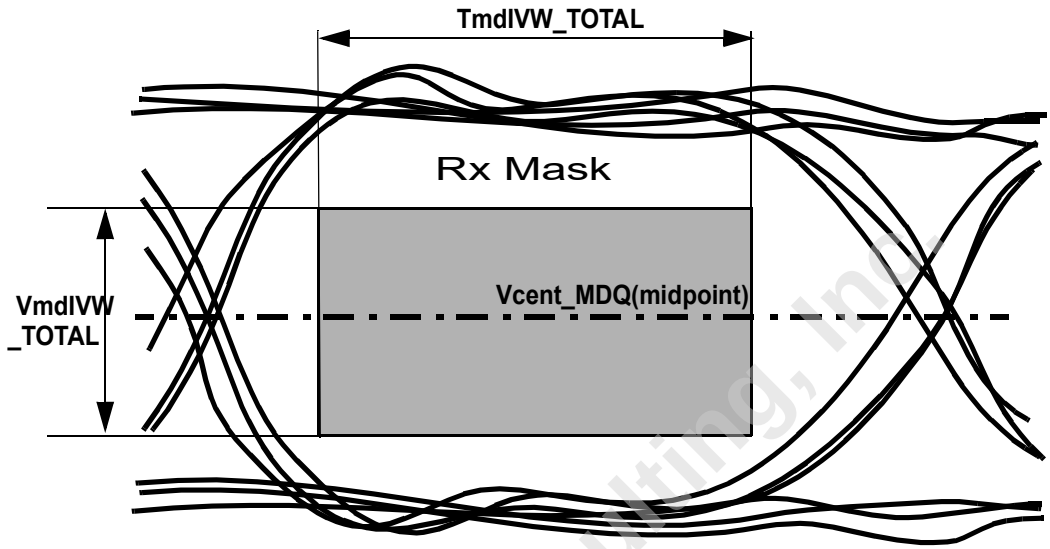

Figure 21 — MDQ Receiver(Rx) mask

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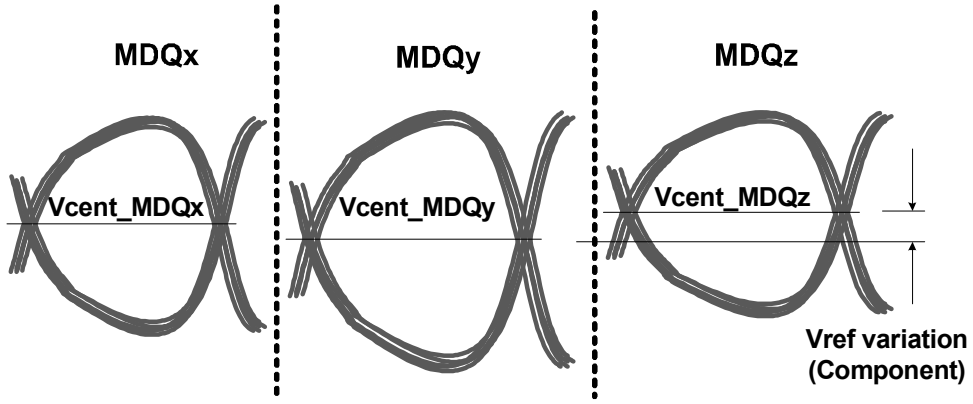

Figure 22 — Across pin Vcent_MDQ voltage variation

Vcent_MDQ(midpoint) is defined as the midpoint between the largest Vcent_MDQ voltage level and the smallest Vcent_MDQ voltage level across all MDQ pins for a given DDR4DB02 component. Each MDQ pin Vcent level is defined by the center, i.e. widest opening of the cumulative data input eye as depicted in Figure 22. This clarifies that any DDR4DB02 component level variation must be accounted for within the DDR4DB02 Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

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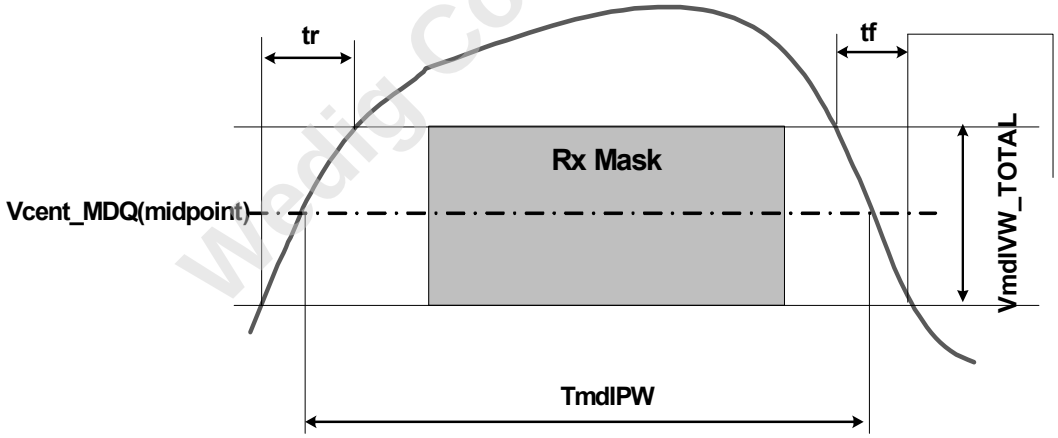

NOTE 1: SRIN_mdIVW = VmdIVW_TOTAL / (tr or tf)

Figure 23 — MDQ TmdIPW and SRIN_mdIVW definition (for each input pulse)

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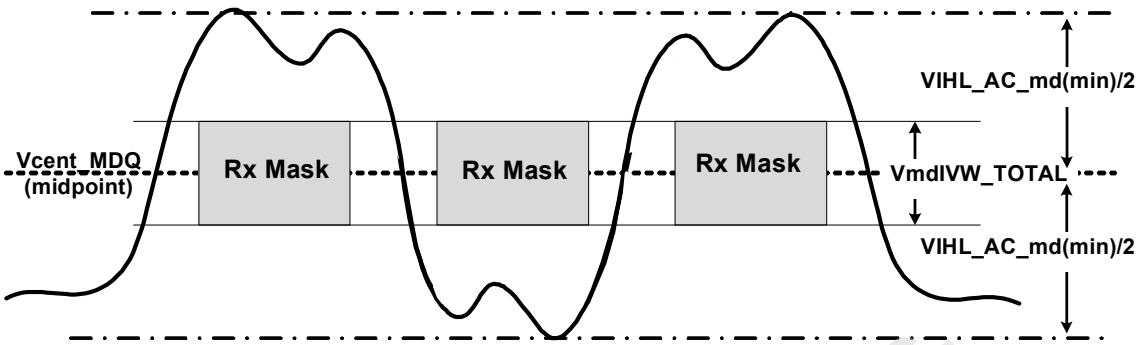

NOTE 1: The VIHL_AC_md requirement has to be met for any UI making a transition. It does not have to be met for a UI when there is no signal transition.

Figure 24 — VIHL_AC_md(min) requirement (for each input pulse)

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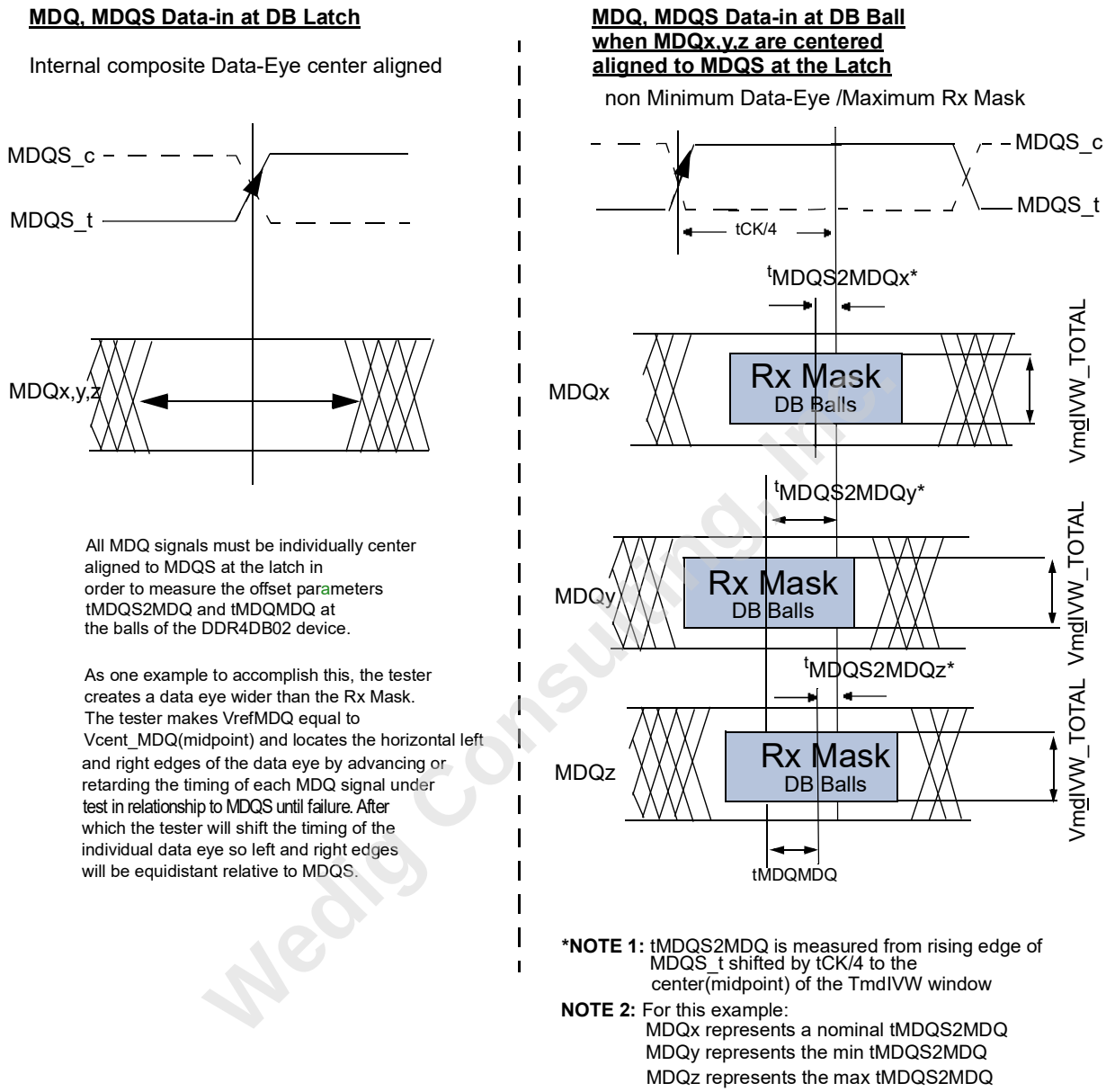

Figure 25 — MDQS to MDQ Timings at DDR4DB02 Balls

All of the timing terms in Figure 25 are measured from MDQS_t/MDQS_c to the center(midpoint) of the TmdIVW window taken at the VmdIVW_TOTAL voltage levels centered around Vcent_MDQ(midpoint). In Figure 25 the timings at the balls are referenced with respect to all MDQ signals center aligned to the DDR4DB02 internal latch. The data to data offset tMDQMDQ is defined as the magnitude of the difference between the min and max tMDQS2MDQ for a given component.

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Table 91 — MDQ/MDQS Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600/1866/ 2133/2400/2666/2933/3200

Speed		DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Voltage and Timing													
VmdIVW_TOTAL	MDQ Rx Mask p-p voltage total	-	130	-	100	-	100	-	90	-	80	mV	1,2,3, 4,5
TmdIVW_TOTAL	MDQ Rx timing window total	-	0.2	-	0.15	-	0.15	-	0.15	-	0.15	UI	1,4,5
VIHL_AC_md	MDQ AC input pulse amplitude pk-pk	160	-	140	-	140	-	130	-	120	-	mV	6
TmdIPW	MDQ input pulse width	0.5	-	0.4	-	0.4	-	0.4	-	0.35	-	UI	7
tMDQS2MDQ	MDQS to MDQ offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	8
tMDQMDQ	MDQ to MDQ offset	-	0.04	-	0.04	-	0.043	-	0.043	-	0.043	UI	9
SRIN_mdIVW	Input Slew Rate over VmdIVW_TOTAL	1	9	1	9	1	9	1	9	1	9	V/ns	10

* UI=tck(avg)min/2

NOTE 1: Data Rx mask voltage and timing total input valid window where VmdIVW is centered around Vcent_MDQ(midpoint). The data Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER ≤1e-16.
NOTE 2: Rx mask voltage AC swing peak-peak requirement over TmdIVW_TOTAL with at least half of VmdIVW_TOTAL(max) above Vcent_MDQ(midpoint) and at least half of VmdIVW_TOTAL(max) below Vcent_MDQ(midpoint).
NOTE 3: The VmdIVW voltage levels are centered around Vcent_DQ(midpoint).
NOTE 4: Defined over the MDQ internal Vref range 1.
NOTE 5: Overshoot and Undershoot Specifications see Table 101 and Figure 37.
NOTE 6: MDQ input pulse signal swing into the receiver must meet or exceed VIHL_AC_md for at least one point over the duration of TmdIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC_md is the peak to peak voltage centered around Vcent_MDQ(midpoint), which is defined in Figure 22.
NOTE 7: MDQ minimum input pulse width defined at the Vcent_MDQ(midpoint).
NOTE 8: MDQS to MDQ offset is within a nibble at DDR4DB02 balls. Includes all DDR4DB02 process, voltage and temperature variation.
NOTE 9: MDQ to MDQ offset is defined as the magnitude of the difference between the min and max MDQS to MDQ offset within a nibble at DDR4DB02 balls for a given component. Includes all DDR4DB02 voltage and temperature variation.
NOTE 10: Input slew rate over VmdIVW Mask centered at Vcent_MDQ(midpoint). This single-ended slew rate also applies to MDQS_t and MDQS_c.

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6.1.3 CTRL Input Receiver Specifications

The CTRL input receiver mask for voltage and timing is shown in Figure 26. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR4DB02 input receiver to successfully capture a valid input signal with BER < 1e-16. The mask is a receiver property for each pin and it is not the valid data eye.

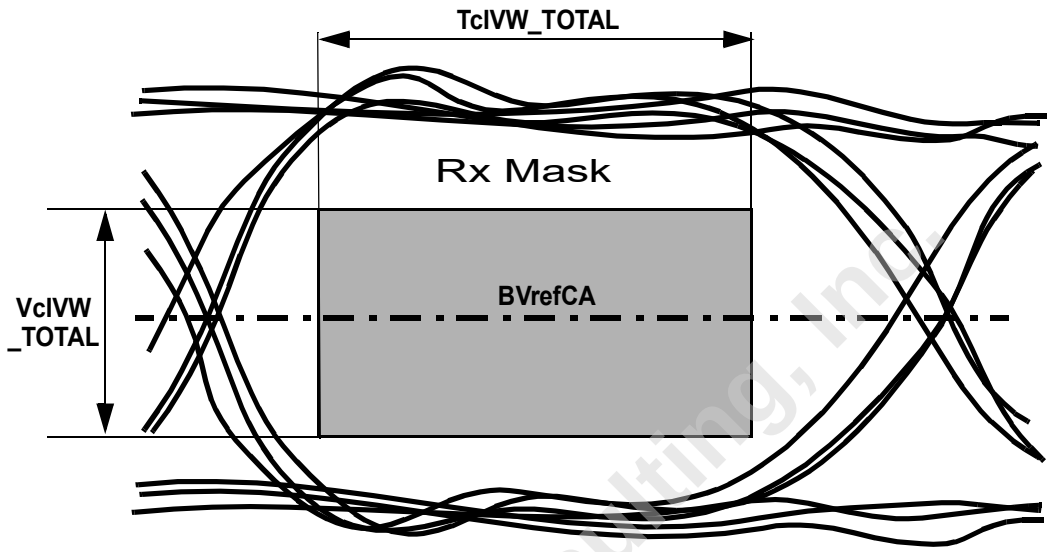

Figure 26 — CTRL Receiver(Rx) mask

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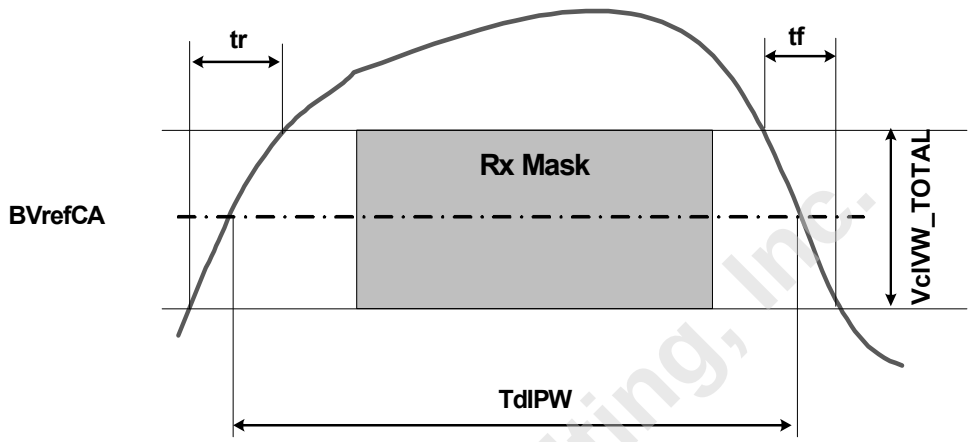
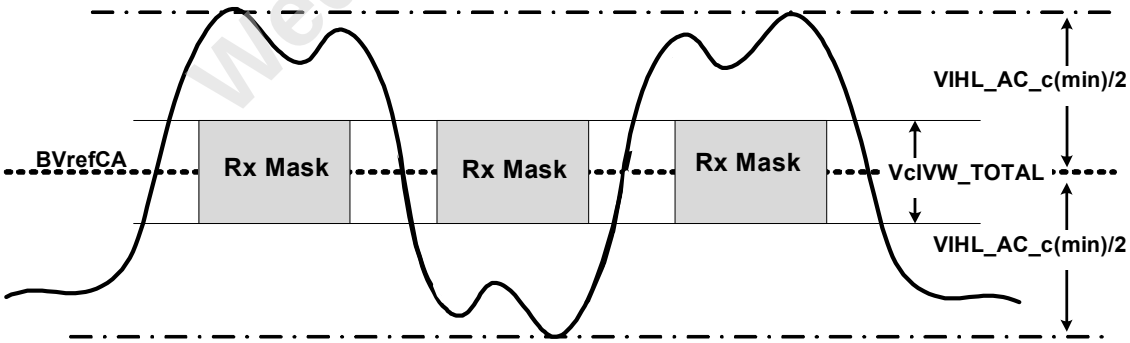
The component level BVrefCA is provided by the DDR4RCD02.



NOTE 1: SRIN_cIVW=VcIVW_TOTAL/(tr or tf)

Figure 27 — CTRL TcIPW and SRIN_cIVW definition (for each input pulse)



NOTE 1: The VIHL_AC_c requirement has to be met for any UI making a transition. It does not have to be met for a UI when there is no signal transition.

Figure 28 — VIHL_AC_c (min) requirement (for each input pulse)

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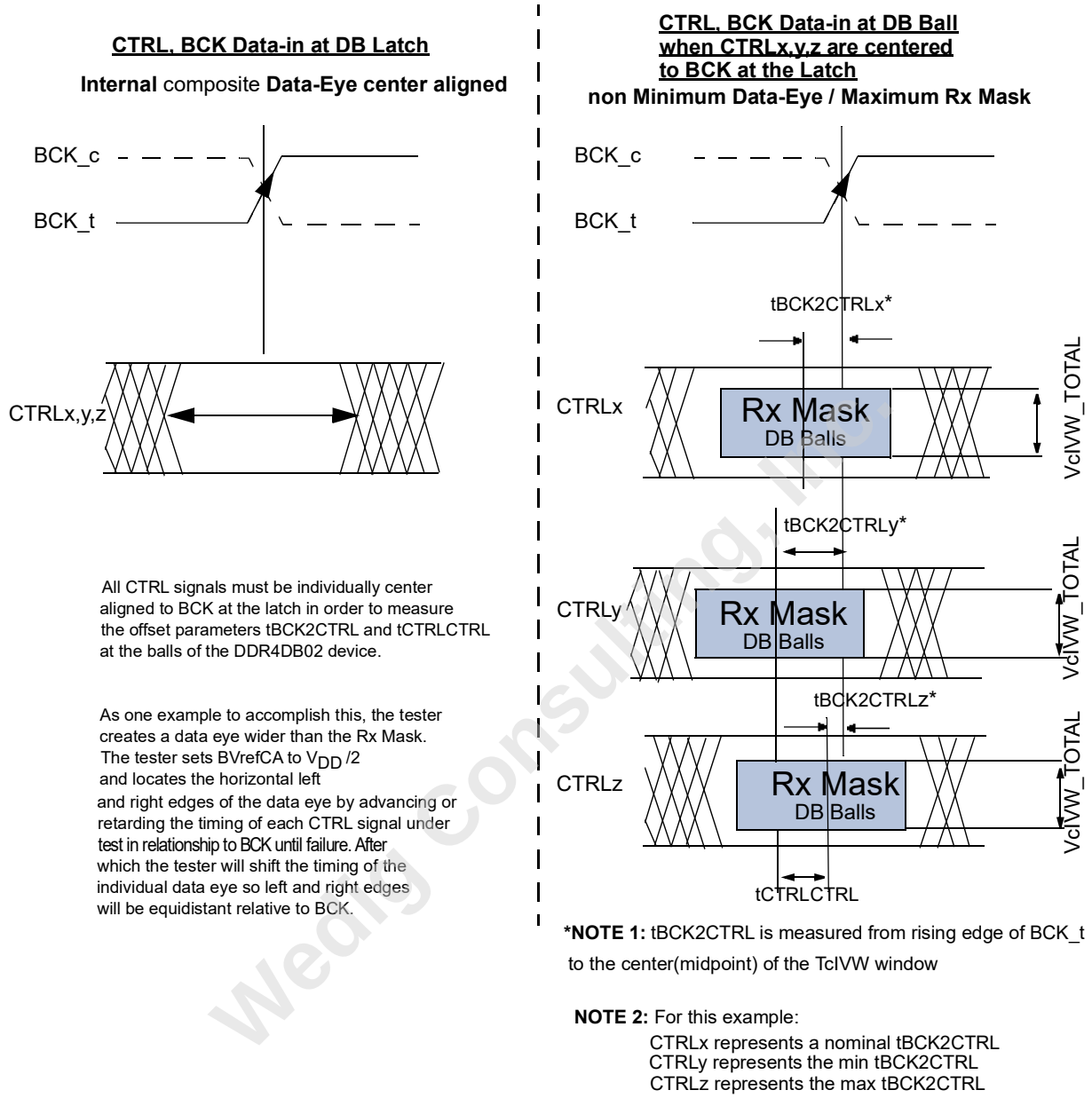

Figure 29 — BCK to CTRL Timings at DDR4DB02 Balls

All of the timing terms in Figure 29 are measured from BCK_t/BCK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_TOTAL voltage levels centered around BVrefCA. In Figure 29 the timings at the balls are referenced with respect to all CTRL signals center aligned to the DDR4DB02 internal latch. The data to data offset tCTRLCTRL is defined as the difference between the min and max tBCK2CTRL for a given component.

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Table 92 — CTRL Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600/1866/2133/ 2400/2666/2933/3200

Speed		DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Voltage and Timing													
VcIVW_TOTAL	Rx Mask p-p voltage total	-	150	-	120	-	100	-	90	-	90	mV	1, 2, 3, 5
TcIVW_TOTAL	Rx timing window total	-	0.2	-	0.15	-	0.15	-	0.15	-	0.15	UI	1, 5
VIHL_AC_c	CTRL AC input pulse amplitude pk-pk	180	-	150	-	140	-	130	-	120	-	mV	6
TcIPW	CTRL input pulse width	0.5	-	0.4	-	0.4	-	0.4	-	0.4	-	UI	7
tBCK2CTRL	BCK to CTRL offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	8
tCTRLCTRL	CTRL to CTRLoffset	-	0.04	-	0.04	-	0.04	-	0.04	-	0.04	UI	9
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	5	1	5	1	5	1	5	1	5	V/ns	10

* UI=tck(avg)min

NOTE 1: CTRL Rx mask voltage and timing total input valid window where VcIVW is centered around BVrefCA. The CTRL Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER <1e-18.
NOTE 2: Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above BVrefCA and at least half of VcIVW_TOTAL(max) below BVrefCA.
NOTE 3: The VcIVW voltage levels are centered around BVrefCA.
NOTE 4: Not defined
NOTE 5: Overshoot and Undershoot Specifications see Table 99 and Figure 35.
NOTE 6: CTRL input pulse signal swing into the receiver must meet or exceed VIHL_AC_c for at least one point over the duration of TcIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC_c is the peak to peak voltage centered around BVrefCA.
NOTE 7: CTRL minimum input pulse width defined at the BVrefCA.
NOTE 8: BCK to CTRL offset is within all CTRL inputs at DDR4DB02 balls. Includes all DDR4DB02 process, voltage and temperature variation.
NOTE 9: CTRL to CTRL offset is defined as the magnitude of difference between the min and max CTRL to CTRL offset at DDR4DB02 balls for a given component. Includes all DDR4DB02 voltage and temperature variation.
NOTE 10: Input slew rate over VcIVW Mask centered at BVrefCA. This single-ended slew rate also applies to BCK_t and BCK_c.

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6.2 AC and DC Logic Input Levels for Differential Signals

6.2.1 Differential signal definition

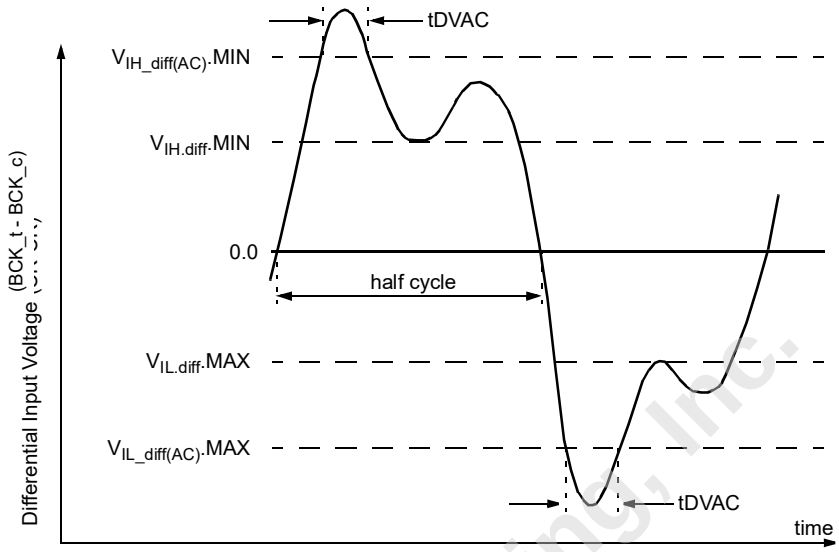

Figure 30 — Definition of differential AC-swing and "time above AC-level" t_{DVAC}

NOTE 1: Differential signal rising edge from $V_{IL.diff}$.MAX to $V_{IH.diff}$.MIN must be monotonic slope.
NOTE 2: Differential signal falling edge from $V_{IH.diff}$.MIN to $V_{IL.diff}$.MAX must be monotonic slope.

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6.3 Differential swing requirements for BCK_t / BCK_c

Table 93 — AC and DC Input Levels for BCK

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input high	BVrefCA+90	Note 3	BVrefCA+75	Note 3	mV	1
$V_{IL(AC)}$	AC input low	Note 3	BVrefCA-90	Note 3	BVrefCA-75	mV	1
V_{IHdiff}	Differential input high	+130	Note 3	+100	Note 3	mV	2
V_{ILdiff}	Differential input low	Note 3	-130	Note 3	-100	mV	2
$V_{IH-diff(AC)}$	Differential input high ac	2 x ($V_{IH(AC)}$. MIN - BVrefCA)	Note 3	2 x ($V_{IH(AC)}$. MIN - BVrefCA)	Note 3	mV	
$V_{ILdiff(AC)}$	Differential input low ac	Note 3	2 x ($V_{IL(AC)}$.MAX - BVrefCA)	Note 3	2 x ($V_{IL(AC)}$.MAX - BVrefCA)	mV	

Symbol	Parameter	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH(AC)}$	AC input high	BVrefCA+70	Note 3	BVrefCA+ 65	Note 3	BvrefCA - 65	Note 3	mV	1
$V_{IL(AC)}$	AC input low	Note 3	BVrefCA-70	Note 3	BVrefCA- 65	Note 3	BVrefCA- 65	mV	1
V_{IHdiff}	Differential input high	+90	Note 3	+ 80	Note 3	+80	Note 3	mV	2
V_{ILdiff}	Differential input low	Note 3	- 90	Note 3	- 80	Note 3	-80	mV	2
$V_{IH-diff(AC)}$	Differential input high ac	2 x ($V_{IH(AC)}$.MIN - BVrefCA)	Note 3	2 x ($V_{IH(AC)}$.MIN - BVrefCA)	Note 3	2 x ($V_{IH(AC)}$.MIN - BVrefCA)	Note 3	mV	
$V_{ILdiff(AC)}$	Differential input low ac	Note 3	2 x ($V_{IL(AC)}$MAX - BVrefCA)	Note 3	2 x ($V_{IL(AC)}$MAX - BVrefCA)	Note 3	2 x ($V_{IL(AC)}$MAX - BVrefCA)	mV	

NOTE 1: This is a single-ended parameter. It is used to define the differential input specs.
NOTE 2: Used to define a differential signal slew-rate.
NOTE 3: These values are not defined, however the differential signals BCK_t / BCK_c need to meet the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”

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Table 94 — Allowed time before ringback (tDVAC) for BCK_t / BCK_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 180 mV		t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 150 mV		t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 140 mV		t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 130 mV	
	min	max	min	max	min	max	min	max
> 4.0	125	-	105	-	100	-	95	-
4.0	120	-	100	-	95	-	90	-
3.0	115	-	95	-	90	-	85	-
2.0	110	-	90	-	85	-	80	-
1.8	105	-	85	-	80	-	75	-
1.6	100	-	80	-	75	-	70	-
1.4	95	-	75	-	70	-	65	-
1.2	90	-	70	-	65	-	60	-
1.0	85	-	65	-	60	-	55	-
< 1.0	80	-	60	-	55	-	50	-

6.4 Single-ended requirements for BCK_t / BCK_c

Each individual component of the differential signal BCK_t / BCK_c has also to comply with certain requirements for single-ended signals.

BCK_t and BCK_c have to approximately reach V_{SEH} min / V_{SEL} max (equal to the AC-levels ($V_{IH(AC)}$ / $V_{IL(AC)}$)) in every half-cycle.

Note that the applicable AC-levels for BCK_t / BCK_c are different per speed bin.

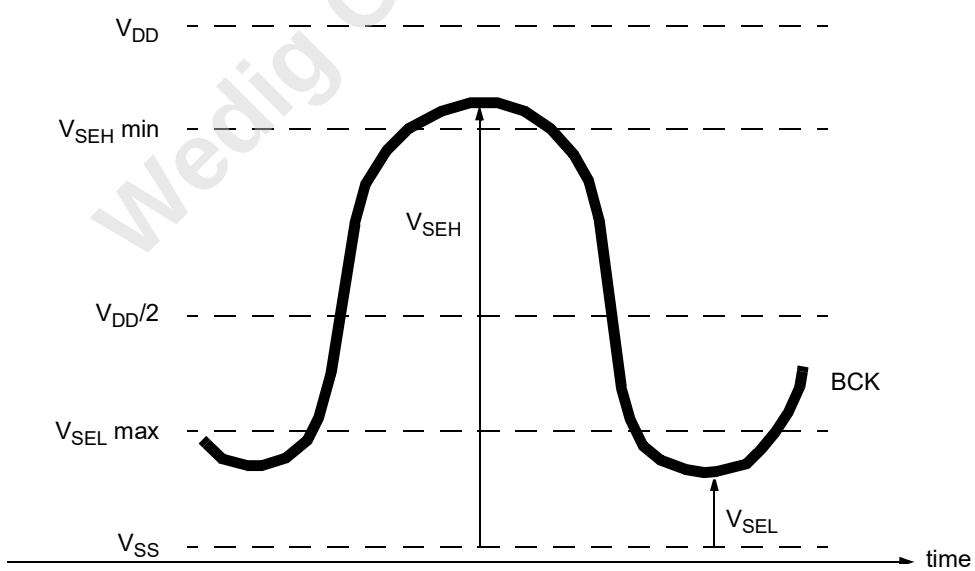

Figure 31 — Single-ended requirement for differential signals.

Note that, while CTRL signal requirements are with respect to BVrefCA, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the

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requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 95 — Single-ended levels for BCK_t / BCK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for BCK_t / BCK_c	$(V_{DD}/2) + 90$	NOTE 3	$(V_{DD}/2) +75$	NOTE 3	mV	1, 2
V_{SEL}	Single-ended low-level for BCK_t / BCK_c	NOTE 3	$(V_{DD}/2) - 90$	NOTE 3	$(V_{DD}/2) - 75$	mV	1, 2

Symbol	Parameter	DDR4 2666		DDR4 2933		DDR4 3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for BCK_t / BCK_c	$(V_{DD}/2) + 70$	NOTE 3	$(V_{DD}/2) + 65$	NOTE 3	$(V_{DD}/2) + 65$	NOTE 3	mV	1, 2
V_{SEL}	Single-ended low-level for BCK_t / BCK_c	NOTE 3	$(V_{DD}/2) - 70$	NOTE 3	$(V_{DD}/2) - 65$	NOTE 3	$V_{DD}/2) - 65$	mV	1, 2

NOTE 1: For BCK_t/ BCK_c use $V_{IH(AC)}$ / $V_{IL(AC)}$
NOTE 2: $V_{IH(AC)}$ / $V_{IL(AC)}$ is based on BVrefCA
NOTE 3: These values are not defined, however the single-ended signals BCK_t /BCK_c need to be within the limitations for overshoot and undershoot.

6.5 Differential Input Cross point voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (BCK_t / BCK_c) must meet the requirements in Table 96. The differential input cross point voltage Vix is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

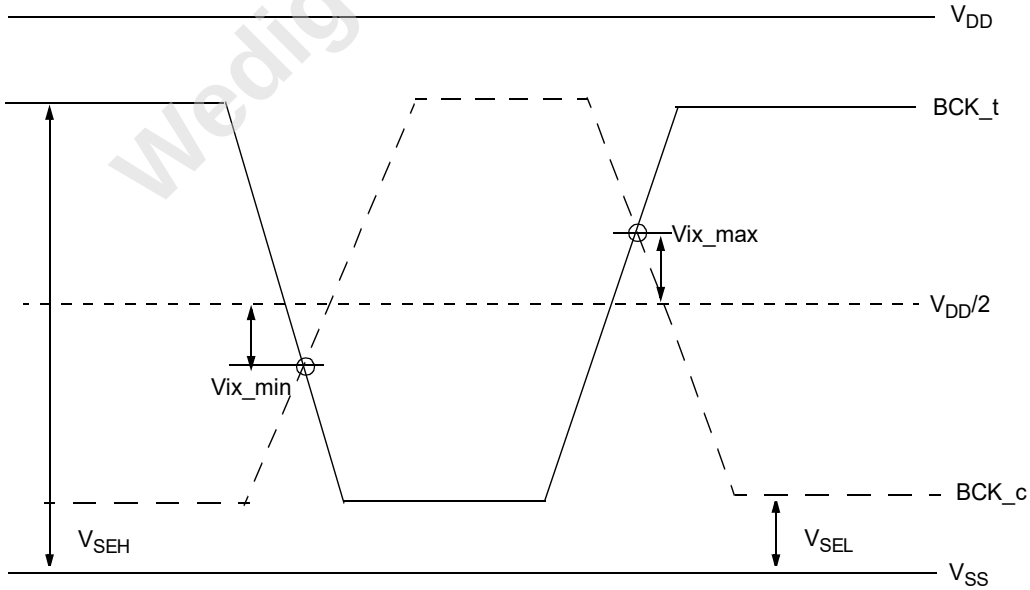

Figure 32 — Vix Definition (BCK)

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Table 96 — Cross point voltage for differential input signals (BCK)

Symbol	Parameter	DDR4-1600/1866/2133				Unit	Note
		min		max			
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2 - 145$	$V_{DD}/2 - 145 \le V_{SEL} \le V_{DD}/2 - 90$	$V_{DD}/2 + 90 \le V_{SEH} \le V_{DD}/2 + 145$	$V_{DD}/2 + 145 \le V_{SEH}$	mV	
V_{IX}(BCK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for BCK_t, BCK_c	-120	$-(V_{DD}/2 - V_{SEL}) + 25$	$(V_{SEH} - V_{DD}/2) - 25$	+120	mV	2
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2 - 175$	$V_{DD}/2 - 175 \le V_{SEL} \le V_{DD}/2 - 90$	$V_{DD}/2 + 90 \le V_{SEH} \le V_{DD}/2 + 175$	$V_{DD}/2 + 175 \le V_{SEH}$	mV	
V_{IX_EX}(BCK)	Extended Differential Input Cross Point Voltage relative to $V_{DD}/2$ for BCK_t, BCK_c	-150	$-(V_{DD}/2 - V_{SEL}) + 25$	$(V_{SEH} - V_{DD}/2) - 25$	+150	mV	1, 3

Symbol	Parameter	DDR4-2400/2666/2933/3200				Unit	Note
		min		max			
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2 - 145$	$V_{DD}/2 - 145 \le V_{SEL} \le V_{DD}/2 - 75$	$V_{DD}/2 + 75 \le V_{SEH} \le V_{DD}/2 + 145$	$V_{DD}/2 + 145 \le V_{SEH}$	mV	
V_{IX}(BCK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for BCK_t, BCK_c	-120	$-(V_{DD}/2 - V_{SEL}) + 25$	$(V_{SEH} - V_{DD}/2) - 25$	+120	mV	2
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2 - 175$	$V_{DD}/2 - 175 \le V_{SEL} \le V_{DD}/2 - 75$	$V_{DD}/2 + 75 \le V_{SEH} \le V_{DD}/2 + 175$	$V_{DD}/2 + 175 \le V_{SEH}$	mV	
V_{IX_EX}(BCK)	Extended Differential Input Cross Point Voltage relative to $V_{DD}/2$ for BCK_t, BCK_c	-150	$-(V_{DD}/2 - V_{SEL}) + 25$	$(V_{SEH} - V_{DD}/2) - 25$	+150	mV	1, 3

NOTE 1: Extended range for Vix is only allowed for clock, if single-ended clock input signals BCK_t and BCK_c are monotonic with a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2$ +/- 50 mV, and when the differential slew rate of BCK_t / BCK_c is larger than 3 V/ns.

Refer to Table 95 for V_{SEL} and V_{SEH} standard values.

NOTE 2: See Figure 60

NOTE 3: See Figure 61

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To guarantee tight setup and hold parameters with respect to strobe, each cross point voltage of differential input signals (DQS_t - DQS_c and MDQS_t - MDQS_c) must meet the requirements in Table 97.

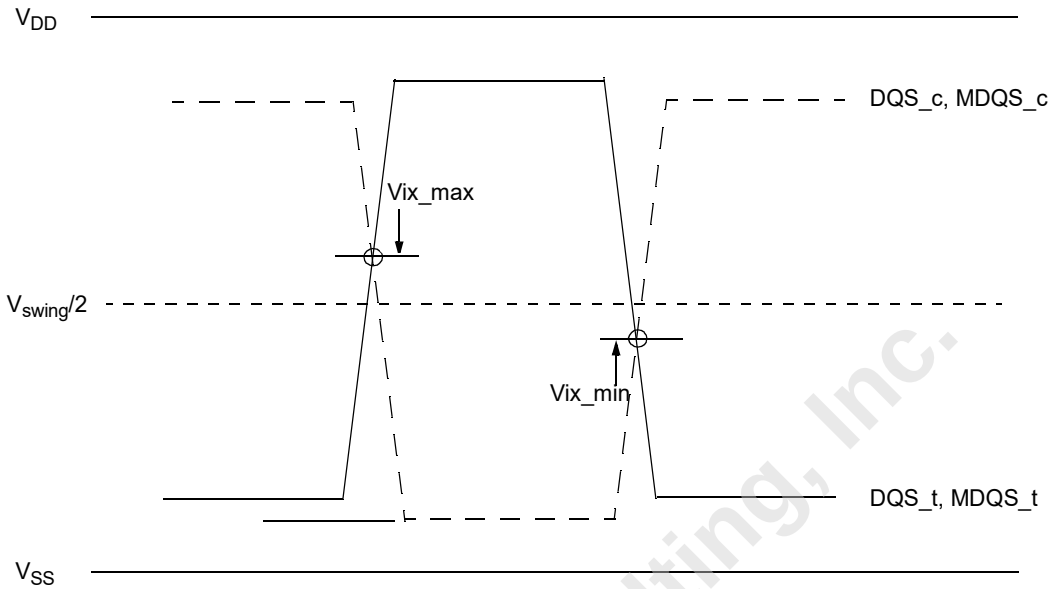

Figure 33 — Vix Definition ([M]DQS)

Table 97 — Cross point voltage for differential input signals ([M]DQS)

Parameter	Symbol	DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max	min	max		
[M]DQS Differential input cross point voltage ratio	Vix_DQS_ratio	-	15	-	15	-	15	-	15	%	1,2

NOTE 1: Referenced to Vswing/2=avg 0.5(VDQS_t + VDQS_c) where the average is over 400 UI.

NOTE 2: Ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (|Vix_DQS|/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|

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6.6 Differential Input Slew Rate Definitions for BCK

Input slew rate for differential signals BCK_t / BCK_c are defined and measured as shown in Table 98 and Figure 34.

Table 98 — Differential Input Slew Rate Definition for BCK_t / BCK_c

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (BCK_t / BCK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (BCK_t / BCK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff
NOTE: The differential signal (i.e. BCK_t / BCK_c) must be linear between these thresholds.			

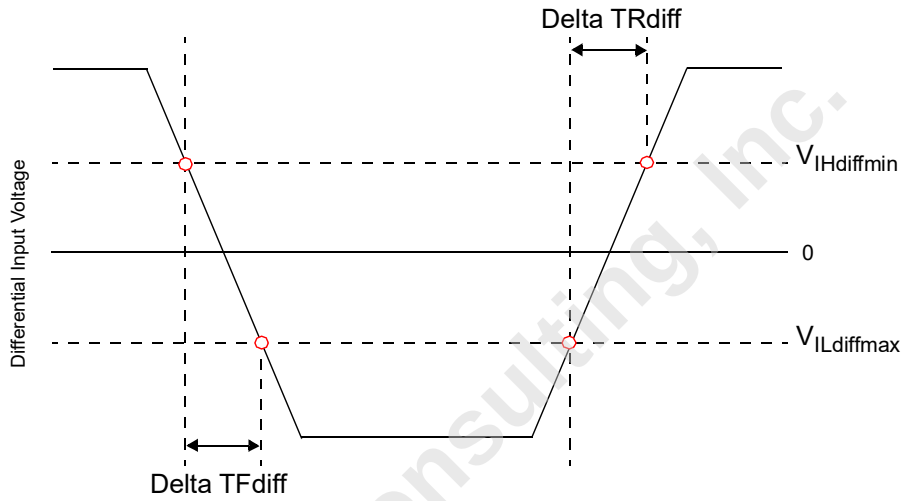

Figure 34 — Differential Input Slew Rate Definition for BCK_t / BCK_c

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6.7 Overshoot and Undershoot Specifications

Table 99 — AC overshoot/undershoot specification for Control pins

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Maximum peak amplitude above V_{DD} Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Delta value between V_{DD} Absolute Max and V_{DD} Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area per 1 t_{CK} above V_{DD} Absolute Max	0.0083	0.0071	0.0062	0.0055	0.0047	0.0040	0.0034	V-ns
Maximum overshoot area per 1 t_{CK} between V_{DD} Absolute Max and V_{DD} Max	0.2550	0.2185	0.1914	0.1699	0.1505	0.1330	0.1180	V-ns
Maximum undershoot area per 1 t_{CK} below V_{SS}	0.2644	0.2265	0.1984	0.1762	0.1568	0.1375	0.1250	V-ns

NOTE 1: The AC overshoot/undershoot specification in Table 84 applies to BCOM[3:0], BODT, BCKE

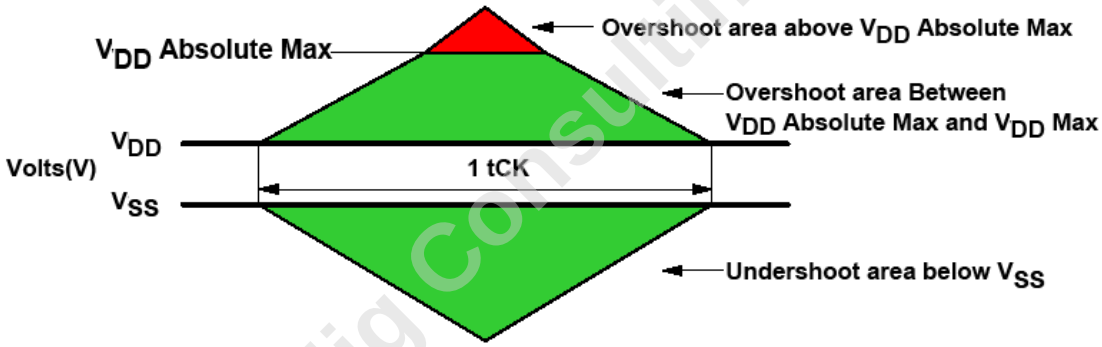

Figure 35 — Control Overshoot and Undershoot definition

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Table 100 — AC overshoot/undershoot specification for Clock

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Maximum peak amplitude above V_{DD} Absolute Max allowed for overshoot area	0.16	0.16	0.16	0.16	0.16	0.16	0.16	V
Delta value between V_{DD} Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitued allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area per 1 UI above V_{DD} Absolute Max	0.0150	0.0129	0.0113	0.0100	0.0090	0.0082	0.0075	V-ns
Maximum overshoot area per 1 UI between Absolute Max and V_{DD} Max	0.1050	0.090	0.0788	0.0700	0.0632	0.0573	0.0525	V-ns
Maximum undershoot below per 1 UI V_{SS}	0.1031	0.0884	0.0774	0.0688	0.0619	0.0563	0.0516	V-ns

NOTE 1: The AC overshoot/undershoot specification in Table 85 applies to BCK_t/BCK_c

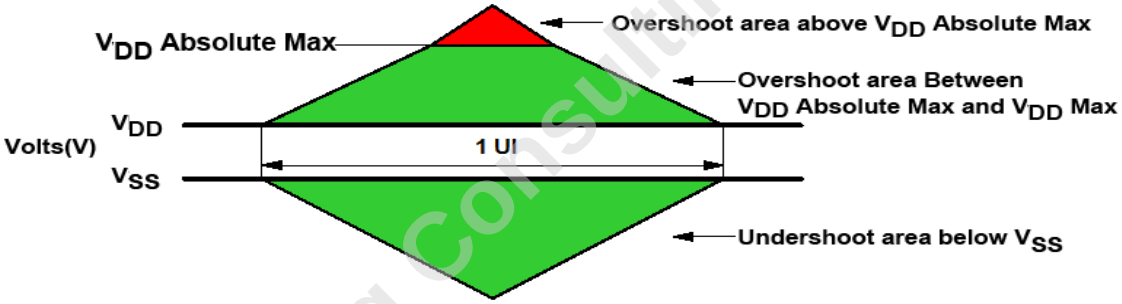

Figure 36 — Clock Overshoot and Undershoot definition

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Table 101 — AC overshoot/undershoot specification for Data and Strobe Pins

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Maximum peak amplitude above Max absolute level of Vin, Vout	0.16	0.16	0.16	0.16	0.16	0.16	0.16	V
Overshoot area between Max absolute level of Vin, Vout and V_{DD} Max	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Undershoot area between Min absolute level of Vin, Vout and V_{SS}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Maximum peak amplitude below Min absolute level of Vin, Vout	0.10	0.10	0.10	0.10	0.10	0.10	0.10	V
Maximum peak amplitude per 1 UI above Max absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	0.0090	0.0080	0.0070	V-ns
Maximum overshoot area per 1 UI between Max absolute level of Vin, Vout and VDD Max	0.1050	0.090	0.0788	0.0700	0.0632	0.0575	0.0494	V-ns
Maximum undershoot area per 1 UI between Min absolute level of Vin, Vout and V_{SS}	0.1050	0.090	0.0788	0.0700	0.0632	0.0575	0.0494	V-ns
Maximum undershoot area per 1 UI below Min absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	0.0090	0.0080	0.0070	V-ns

NOTE 1: The AC overshoot/undershoot specification in Table 86 applies to DQ[7:0], DQS_t[1:0], DQS_c[1:0], MDQ[7:0], MDQS_t[1:0], MDQS_c[1:0]

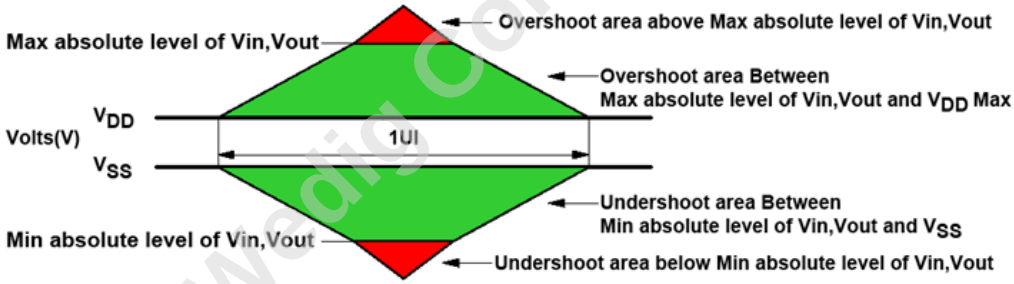

Figure 37 — Data and Strobe Overshoot and Undershoot definition

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6.8 DQ Vref Specifications

The internal DQ Vref specifications parameters are Vref operating range, Vref step size, Vref set tolerance, Vref step time and Vref valid tolerance.

The DQ Vref operating range specifies the minimum required Vref setting range for DDR4DB02 devices and is specific by a Vref min operating point and a Vref max operating point, as depicted in Figure 38 below.

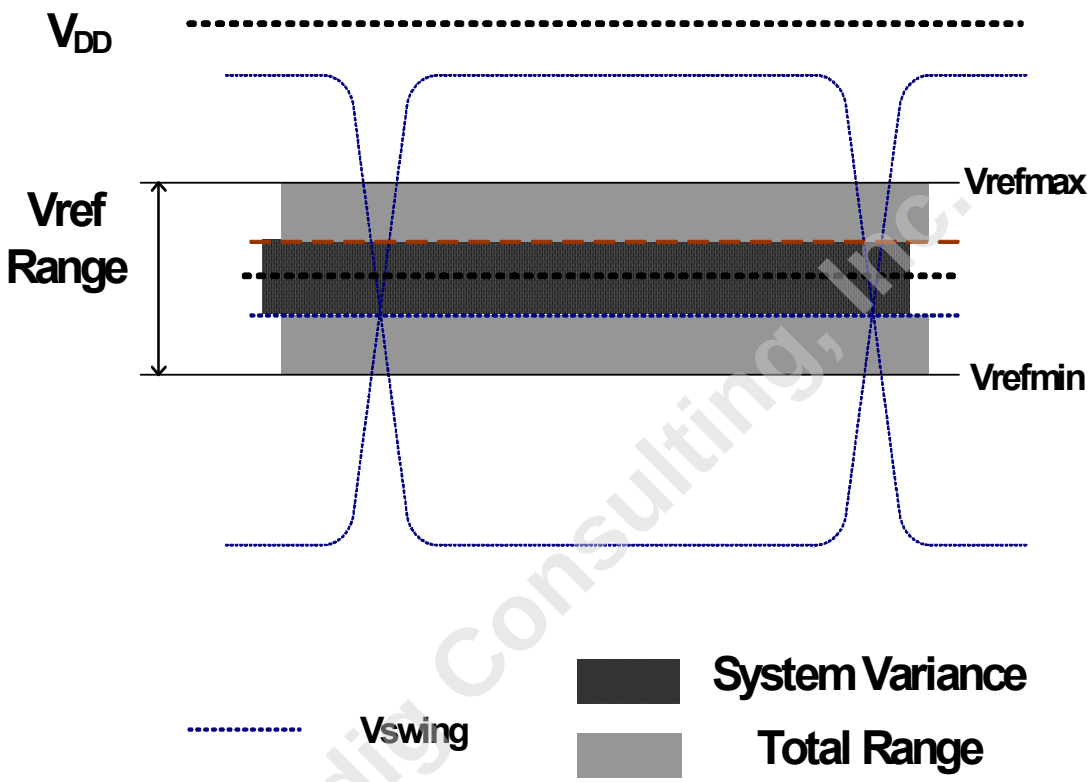

Figure 38 — Vref operating range(Vrefmin, Vrefmax)

The Vref step size is defined as the step size between adjacent steps. Vref step size ranges from 0.5% V_{DD} to 0.8% V_{DD}. However, for a given design, DDR4DB02 has one value for Vref step size that falls within this range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n, hence there are two parameters for Vref set tolerance uncertainty for different numbers of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on two endpoints, where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the step size and Vref set tolerance is below.

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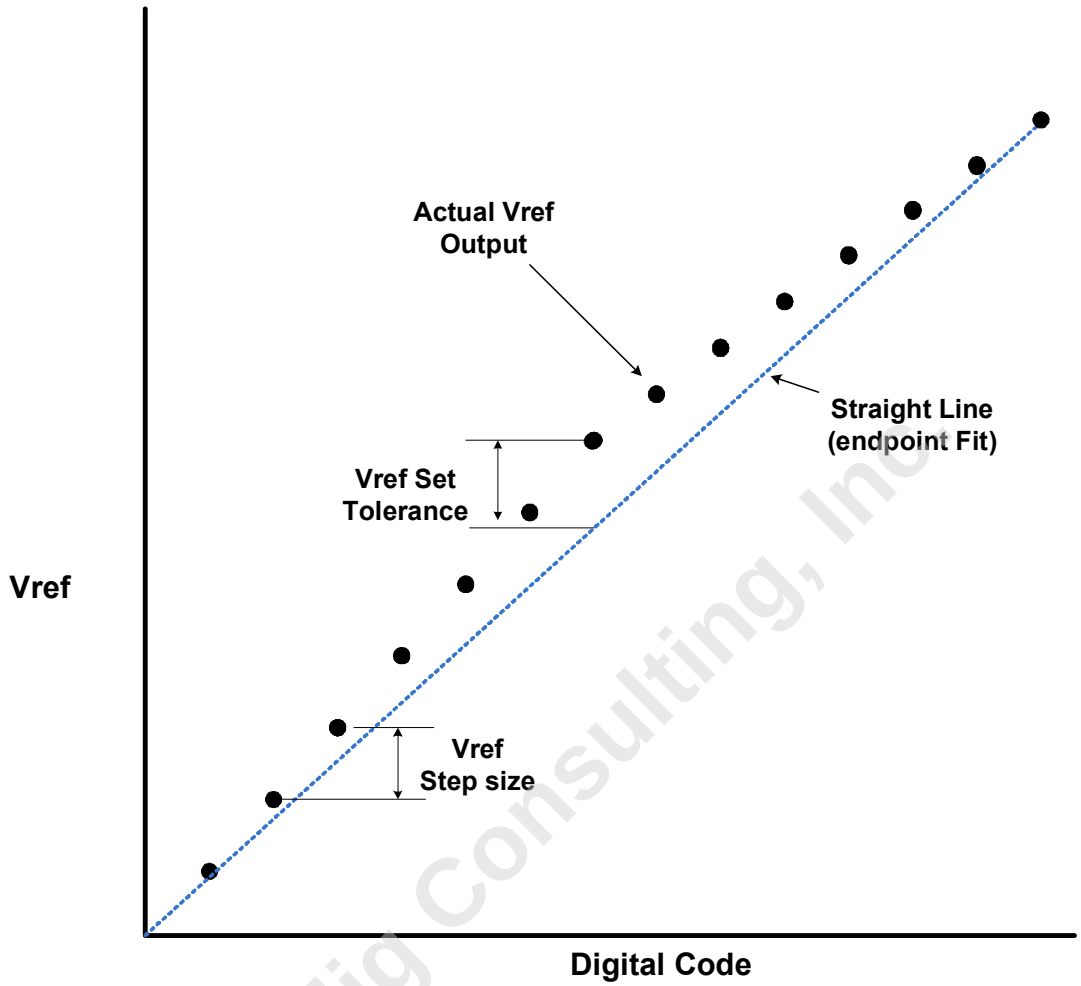

Figure 39 — Example of Vref set tolerance(max case only shown) and step size

The Vref increment/decrement step times are defined by Vref_time_short and Vref_time_long. Vref_time_short and Vref_time_long are defined from t0 to t1 as shown in the Figure 40 below where t0 is referenced to when the BCW write occurs and t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance(Vref_val_tol).

The Vref valid level is defined by Vref_val_tol to qualify the step time t1 as shown in Figure 41. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

Vref_time_short is for a single step size increment/decrement change in Vref voltage.

Vref_time_long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to RCW write command clock

t1 - is referenced to the Vref_val_tol

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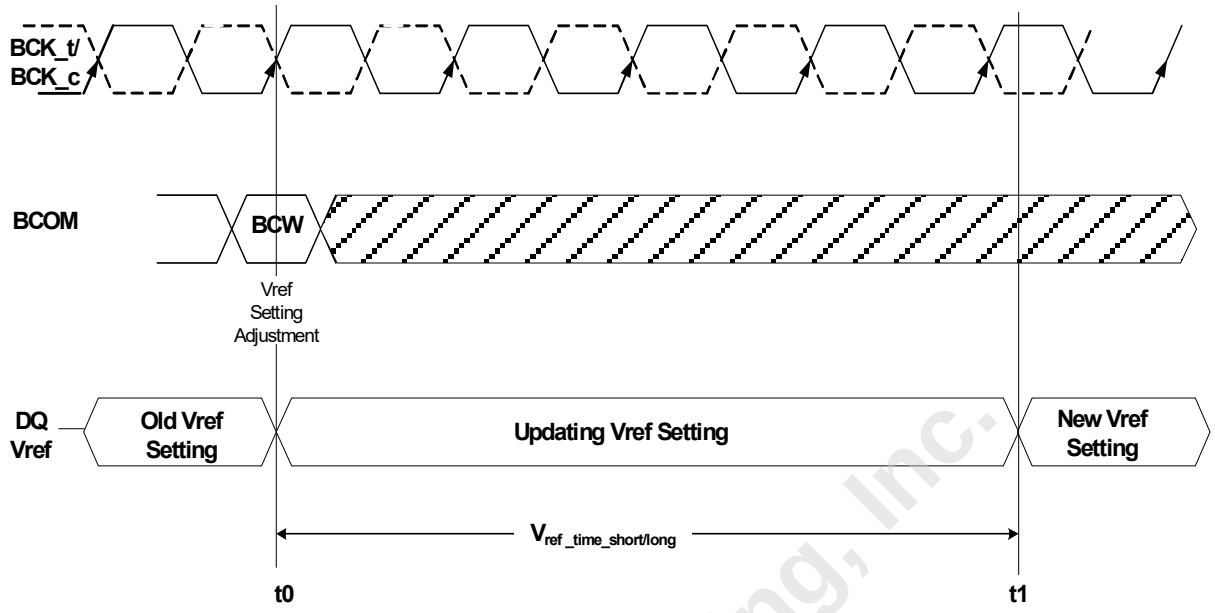

Figure 40 — Vref_time for short and long timing diagram

A BCW write to the F5BC5x or F5BC6x (Connector Interface Vref Control Word or DRAM Interface Vref Control Word) is used to program the Vref value.

The minimum time required between two Vref BCW commands is Vref_time_short for single step and Vref_time_long for a full voltage range step.

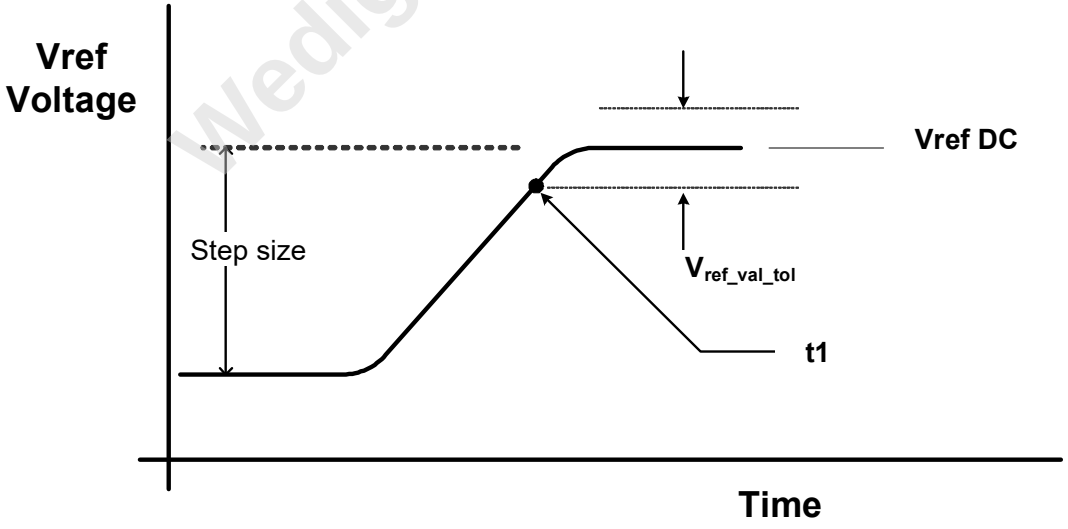

Figure 41 — Vref step single step size increment case

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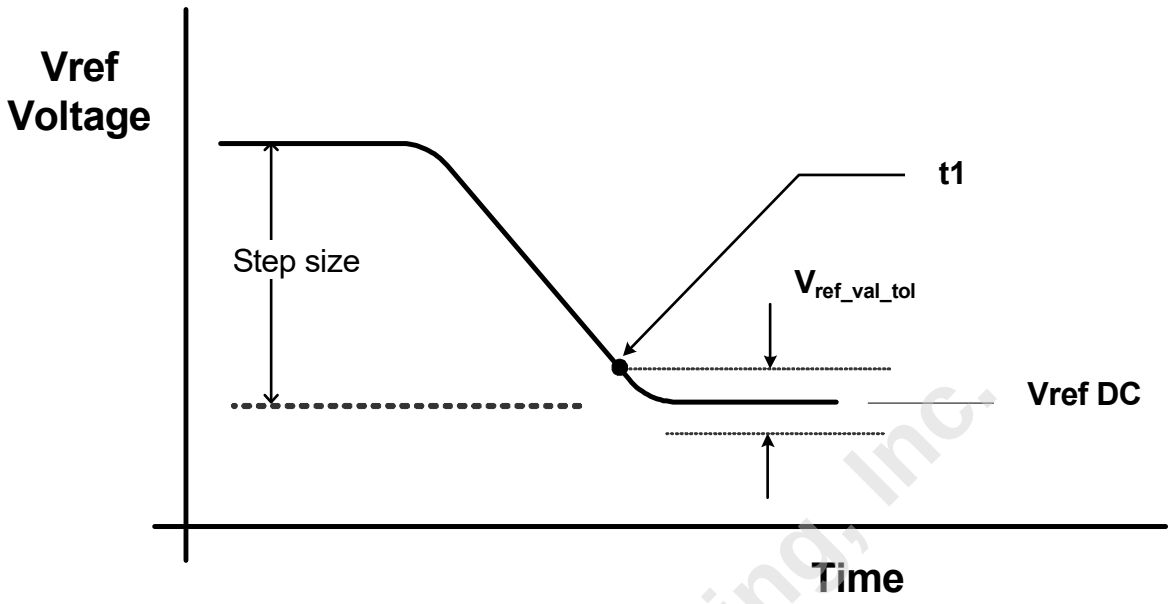

Figure 42 — Vref step single step size decrement case

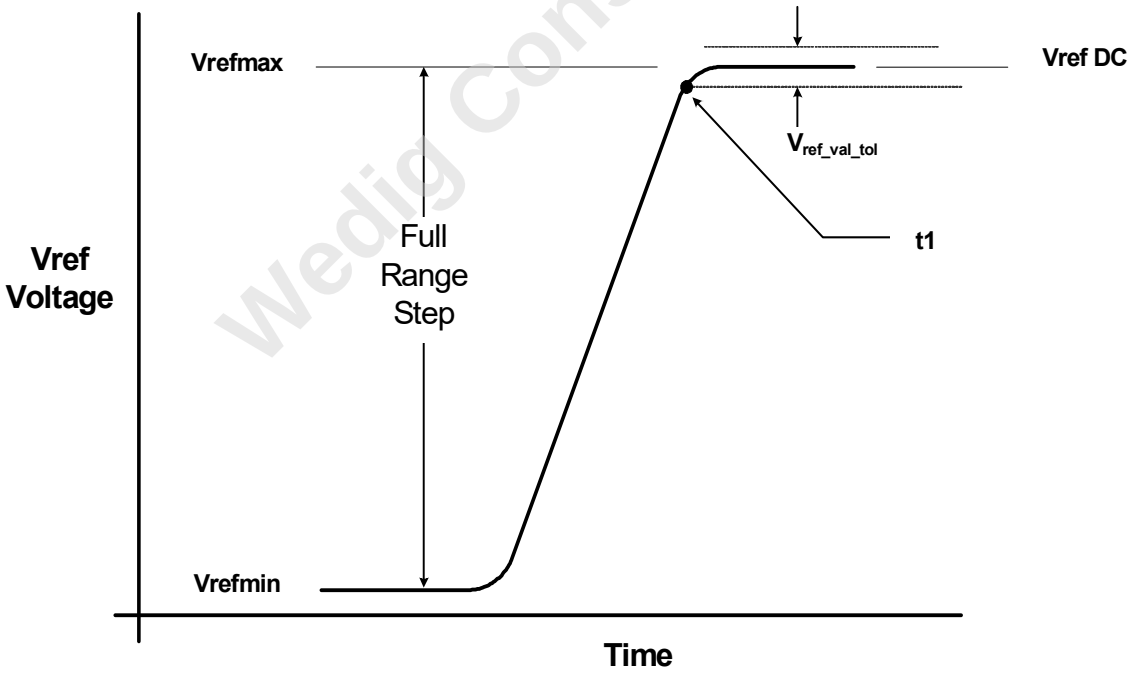

Figure 43 — Vref full step from Vrefmin to Vrefmax case

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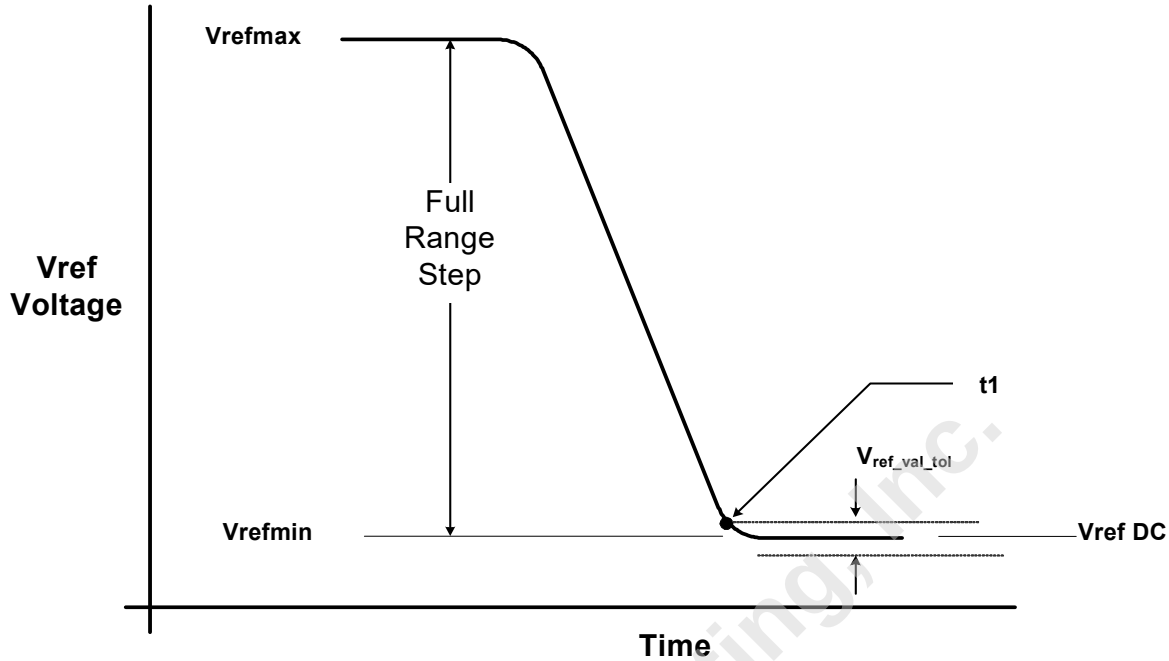

Figure 44 — Vref full step from Vrefmax to Vrefmin case

The table below contains the DQ Vref specifications that will be characterized at the component level for compliance.

Table 102 — Internal DQ Vref Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Vref Max Operating Point Range 1	Vref_max	92.5%	-		V_{DD}	
Vref Min Operating Point Range 1	Vref_min		-	60%	V_{DD}	
Vref Max Operating Point Range 2	Vref_max	77.5%	-		V_{DD}	
Vref Min Operating Point Range 2	Vref_min		-	45%	V_{DD}	
Vref Step size	Vref_step	0.5%		0.8%	V_{DD}	9
	Vref_step(avg)	0.65%	-	Vref_step.max	V_{DD}	
Vref Set Tolerance	Vref_set_tol_big	-1.625%	0.0%	1.625%	V_{DD}	1, 2, 4, 8
	Vref_set_tol_small	-0.15%	0.0%	0.15%	V_{DD}	1 , 3, 5
Vref Step Time	Vref_time_short	-	-	200	ns	6
	Vref_time_long	-	-	500	ns	7
Vref Valid Tolerance	Vref_val_tol	-0.15%	0.0%	0.15%	V_{DD}	8

NOTE 1: Vref_new = Vref_old +/- n*Vref_step; n=number of steps

NOTE 2: The minimum value of Vref setting tolerance = Vref_new - 1.625%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 1.625%*V_{DD}. For n > 4.

NOTE 3: The minimum value of Vref setting tolerance = Vref_new - 0.15%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 0.15%*V_{DD}. For n $\leq$ 4.

NOTE 4: Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 5: Measured by recording the min and max values of the Vref output across four consecutive steps (n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 6: Time from BCW write to increment or decrement one step size for Vref.

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NOTE 7: Time from BCW write to increment or decrement more than one step size up to full operating range for Vref.
NOTE 8: Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 9: Vref_step(avg) = (Vref Max - Vref Min)/50.

6.9 DFE Tap Coefficient and Gain Adjustment tolerances (DNL and INL)

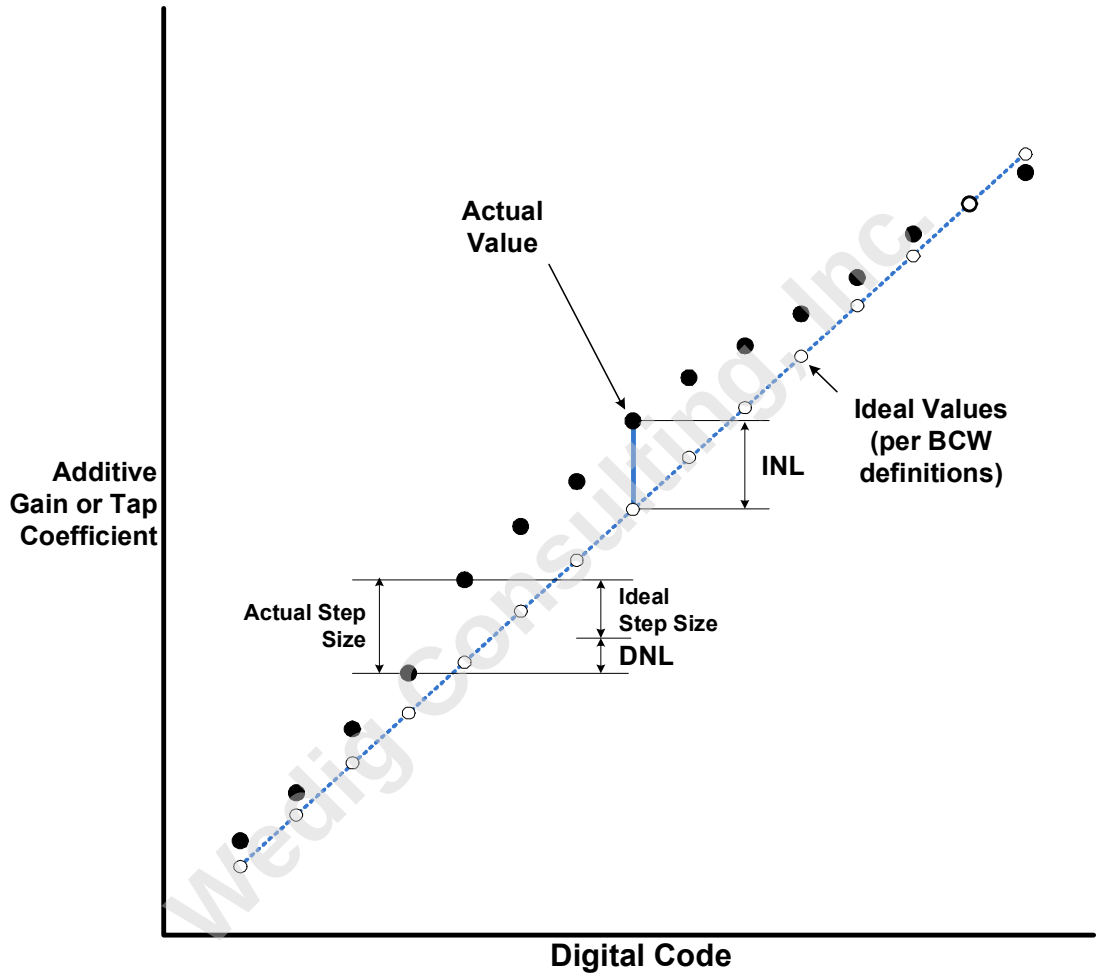

Figure 45 — Example of Tap Coefficient and Gain Adjustment tolerances (DNL and INL)

Differential nonlinearity (DNL) is the deviation between effective and ideal control step sizes for any pair of analog values resulting from adjacent settings in Receiver DFE Tap Coefficient and Gain Adjustment control words as defined in F2BCFx, F3BCCx, F3BCDx, F3BCEx, and F3BCFx.

Integral nonlinearity (INL) is the deviation between effective analog values and expected ideal values for the corresponding settings in Receiver DFE Tap Coefficient and Gain Adjustment control words as defined in F2BCFx, F3BCCx, F3BCDx, F3BCEx, and F3BCFx.

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6.10 DFE Timing Parameters.

Table 103 — DFE Timing Parameters

Parameter	Symbol	Conditions	Min	Max	Unit
DFE Global Enable/Disable Settling Time	t_{DFE_GLEN}	Delay between any BCW Write command that modifies the value of Bit DA7 in F2BCEx and any other command affected by Host Receiver DFE circuits (assuming power on default settings in all DFE-related control words)	250	-	nS
DFE Training Mode Enable	$t_{DFE\ TRNEN}$	Delay between any BCW Write command that modifies the settings in the eight control registers mapped to Bit DA7 in F2BCFx and any other command affected by Host Receiver DFE circuits	1	-	uS
DFE Tap Enable/Disable Settling Time	$t_{DFE\ TAPEN}$	Number of clock cycles between any BCW Write command that modifies the settings in the Tap Enable control bits (i.e., Bit DA6 in F3BCCx/Dx/Ex/Fx) and any other command affected by Host Receiver DFE circuits.	64	-	tCK
DFE Gain Offest Settling Time	$t_{DFE\ GAOF}$	Delay between any BCW Write command that modifies any of the Gain Offset control settings mapped to Bits DA[2:0] of F2BCFx and any other command affected by Host Receiver DFE circuits	120	-	nS
Vref_DFE Short Settling Times	$t_{DFEVREFS}$	The Short settling time for DFE_VREF single step without sign change in F6BC4x DA2	200	-	nS
Vref_DFE Long Settling Times	$t_{DFEVREFL}$	The Long settling time for DFE_VREF with more than one step or sign change in F6BC4x DA2	500	-	nS

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7 Output AC and DC Specifications

7.1 [M]DQ/[M]DQS Output Driver DC Electrical Characteristics

The values in Table 104 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 Ω +/- 1%.

Table 104 — [M]DQ/[M]DQS and ALERT_n Output Driver DC Electrical Characteristics

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Note
30 Ω	RON_{30Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/8$	1,2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/8$	1,2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/8$	1,2
	RON_{30Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/8$	1,2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/8$	1,2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/8$	1,2
34 Ω	RON_{34Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
	RON_{34Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
40 Ω	RON_{40Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/6$	1, 2
	RON_{40Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/6$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
48 Ω	RON_{48Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2
	RON_{48Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
60 Ω (for MDQ/MDQS only)	RON_{60Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/4$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/4$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/4$	1, 2
	RON_{60Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/4$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/4$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/4$	1, 2
16 Ω (for ALERT_n only	RON_{16Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.2	16 Ω	1, 5
		$V_{OMdc} = 0.5 \times V_{DD}$	0.8	1.0	1.2	16 Ω	1, 5
		$V_{OHdc} = 0.8 \times V_{DD}$	0.8	1.0	1.4	16 Ω	1, 5

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Table 104 — [M]DQ/[M]DQS and ALERT_n Output Driver DC Electrical Characteristics

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Note
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OMdc} = 0.8 \times V_{DD}$	-10		10	%	1, 2, 4
Mismatch [M]DQ-[M]DQ within byte variation pull-up, MM_{Pudd}		$V_{OMdc} = 0.8 \times V_{DD}$	0		10	%	1, 2, 3
Mismatch [M]DQ-[M]DQ within byte variation pull-dn, MM_{Pddd}		$V_{OMdc} = 0.8 \times V_{DD}$	0		10	%	1, 2, 3

NOTE: A functional representation of the output buffer is shown in Figure 46 Output impedance RON is defined by the value of the external reference resistor R_{ZQ} as defined in Table 88.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off.

Chip Drive Mode

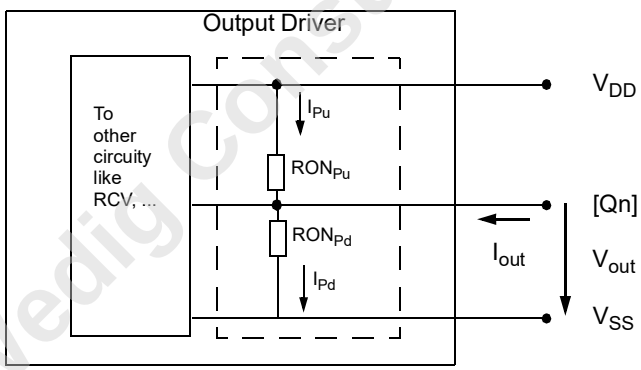

Figure 46 — Output Driver: Definition of Voltages and Currents

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DD} and 1.1 * V_{DD}.
3. [M]DQ to [M]DQ mismatch within byte variation for a given component including [M]DQS_t and [M]DQS_c (characterized).

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4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
   Measure RON_{Pu} and RON_{Pd}, both at 0.8 * V_{DD} separately;Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

5. RON variance range ratio to RON nominal value in a given component, including [M]DQS_t and [M]DQS_c.

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

6. ALERT_n pull-down output driver impedance is recommended to be calibrated at 0.5 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 * V_{DD} and 0.8 * V_{DD}.

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7.2 Output Driver and Termination Resistor Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.
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Table 105 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
R_{ONPD}	0.8 x VDD	90 - ($dR_{ONPD}dT$ x |ΔT|) - ($dR_{ONPD}dV$ x |ΔV|)	110 + ($dR_{ONPD}dT$ x |ΔT|) + ($dR_{ONPD}dV$ x |ΔV|)	%	1,2,3
R_{ONPU}	0.8 x VDD	90 - ($dR_{ONPU}dT$ x |ΔT|) - ($dR_{ONPU}dV$ x |ΔV|)	110 + ($dR_{ONPD}dT$ x |ΔT|) + ($dR_{ONPD}dV$ x |ΔV|)	%	1,2,3
R_{TT}	0.8 x VDD	90 - ($dR_{TT}dT$ x |ΔT|) - ($dR_{TT}dV$ x |ΔV|)	110 + ($dR_{TT}dT$ x |ΔT|) + ($dR_{TT}dV$ x |ΔV|)	%	1,2,3

Note.
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
2. $dR_{ONPD}dT$, $dR_{ONPD}dV$, $dR_{ONPU}dT$, $dR_{ONPU}dV$, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.

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3. This parameter applies to Input/Output pins DQS,MDQS, LDQS, DQ, MDQ and LDQ.

.

Table 106 — Output Driver and Termination Resistor Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	R_{ONPD} Temperature Sensitivity	0.00	0.2.	%/°C
$dR_{ONPD}dV$	R_{ONPD} Voltage Sensitivity	0.00	0.15	%/mV
$dR_{ONPU}dT$	R_{ONPU} Temperature Sensitivity	0.00	0.2	%/°C
$dR_{ONPU}dV$	R_{ONPU} Voltage Sensitivity	0.00	0.15	%/mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.2	%/°C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.15	%/mV

7.3 ALERT_n Output Driver DC Electrical Characteristic

Table 107 — ALERT_n Output Driver DC Electrical Characteristics

Symbol	Parameter	Applicable Signals	Condition	Min	Nom	Max	Unit
I_{OL}	LOW-level output current ALERT_n	Measured at V_{OL} of 0.4 V		20.8	-	-	mA
V_{OL}	Output LOW voltage ALERT_n	Measured at I_{OL} = 20.8 mA		-	-	0.4	V

Table 108 — ALERT_n Ron Specification

Symbol	Parameter	DDR4-1600 to 3200			Unit
		Min	Nom	Max	
$R_{on(ALERT)}$	ALERT_n pull-down impedance	see Table 104	16	see Table 104	Ω

7.4 Single-ended AC & DC Output Levels

Table 109 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/ 2933/3200	Unit	Note
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DD}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DD}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DD}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DD}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DD}	V	1

NOTE 1: The swing of ± 0.15 × V_{DD} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 Ω and an effective test load of 50 Ω to V_{TT} = V_{DD}.

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7.5 Differential AC Output Levels

Table 110 — Differential AC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/ 2666/2933/3200	Unit	Note
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DD}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DD}	V	1

NOTE 1: The swing of ± 0.3 × V_{DD} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7 Ω and an effective test load of 50 Ω to V_{TT} = V_{DD} at each of the differential outputs.

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7.6 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals as shown in Table 111 and Figure 47.

Table 111 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

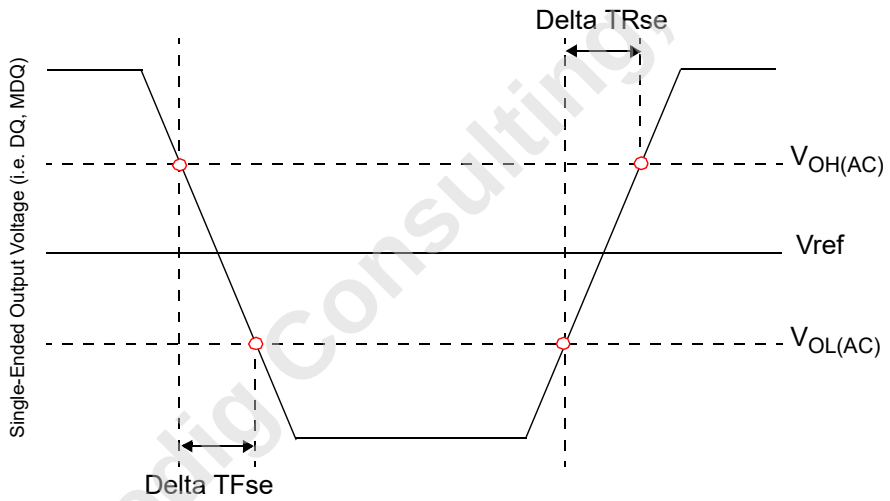

Figure 47 — Single-Ended Output Slew Rate Definition

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Table 112 — Output Slew Rate (single-ended)

		DDR4-1600/ 1866/2400/2666		DDR4-2933		DDR4-3200		Unit
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Single-ended Output Slew Rate[1]	SRQse	4	9[2]	4	9[2]	4	9[2]	V/ns
Single-ended Output falling Slew rate for ALERT_n	$dV/dt_f_{ALERT_n}$[3]	1	5	1	5	1	5	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note 1: This parameter only applies to DQ[7:0] and MDQ[7:0]
Note 2: In two cases, a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane.
Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
Case_2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9V/ns applies.
Note 3: This parameter only applies to ALERT_n falling edge slew rates. Measured at 0.75 V_{DD} +/- 0.15 V_{DD} into reference load in Figure 62

7.7 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 113 and Figure 48.

Table 113 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	**to**	
Differential output slew rate for rising edge[1,2]	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge[1,2]	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff

NOTE 1: Output slew rate is verified by design and characterization, and may not be subject to production test.
NOTE 2: These parameters only apply to DQS[1:0] and MDQS[1:0]

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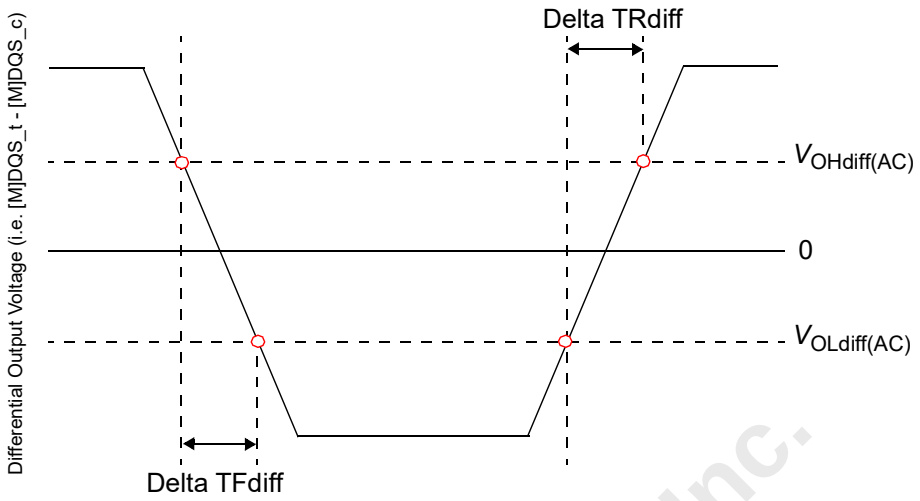

Figure 48 — Differential Output Slew Rate Definition

Table 114 — Differential Output Slew Rate

		DDR4-1600/ 1866/2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Differential Output Slew Rate	SRQdiff	8	18	8	18	8	18	8	18	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals For Ron = RZQ/7 setting										

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7.8 Differential Output Cross Point Voltage

The differential cross point output voltage is defined as the max to min cross point measured on the differential signals DQS_t - DQS_c and MDQS_t - MDQS_c.

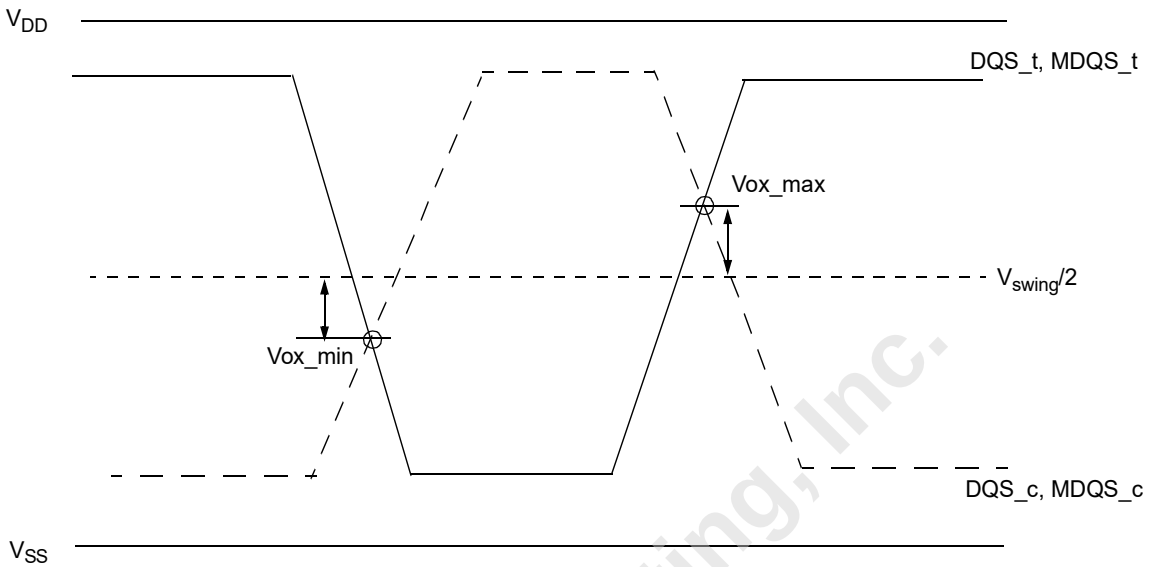

Figure 49 — Vox Definition

Table 115 — Cross point voltage for differential output signals ([M]DQS)

Parameter	Symbol	DDR4-1600/ 1866/2133/ 2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max	min	max		
[M]DQS Differential output cross point voltage ratio	Vox_DQS_ratio	-	10	-	10	-	10	-	10	%	1,2

NOTE 1: Referenced to Vswing/2=avg 0.5(VDQS_t + VDQS_c) where the average is over 400 UI.
NOTE 2: Ratio of the Vox pk voltage divided by Vdiff_DQS : Vox_DQS_Ratio = 100* (|Vox_DQS|/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|

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7.9 On-Die Termination (ODT) Levels and I-V Characteristics

The host interface ODT mode of the DDR4DB02 has 4 states, Data Termination Disable, RTT_NOM, RTT_WR and RTT_PARK. The value of these terminations is determined by the settings of bits DA[2:0] in BC00, BC01 and BC02, respectively.

After entering clock stopped power down mode, the DDR4DB02 automatically disables host interface ODT termination and sets Hi-Z as termination state regardless of these setting.

- RTT_WR: The DIMM that is being written to provide termination regardless of BODT pin status (either HIGH or LOW)

- RTT_NOM: DDR4DB02 turns ON RTT_NOM if it sees BODT asserted HIGH (except RTT_NOM is disabled in BC00).

- RTT_PARK: Default parked value set via BC02 to be enabled and BODT pin is driven LOW.

- Data Termination Disable: DDR4DB02 driving data upon receiving READ command disables the termination after CL + AL + PL+ MRE(R) + tPDM_RD -X and stays off for a duration of BL/2 + X +Y clock cycles.

X is 2 for 1tCK and 3 for 2tCK read preamble mode.

Y is 0 when CRC is disabled and 1 when it's enabled.

The Host Interface Termination State Table is shown in Table 116.

Those RTT values have priority as following:

1. Data Termination Disable

2. RTT_WR

3. RTT_NOM

4. RTT_PARK

which means if there is WRITE command along with BODT pin HIGH, then DDR4DB02 turns on RTT_WR not RTT_NOM, and also if there is READ command, then DDR4DB02 disables data termination regardless of BODT pin and goes into Driving mode.

Table 116 — Host Interface Termination State Table

RTT_PARK BC02 (DA[2:0])	RTT_NOM BC00 (DA[2:0])	BODT pin	Host interface termination	Note
Enabled (≠ 000)	Enabled (≠ 000)	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled (= 000)	Don't care[3]	RTT_PARK	1,2
Disabled (= 000)	Enabled (≠ 000)	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled (= 000)	Don't care[3]	Hi-Z	1,2

NOTE 1: When READ command is executed, DDR4DB02 host interface termination state will be Hi-Z for defined period independent of BODT pin and BCW setting of RTT_PARK/RTT_NOM.

NOTE 2: If RTT_WR is enabled, RTT_WR will be activated by WRITE command for defined period time independent of BODT pin and BCW setting of RTT_PARK /RTT_NOM.

NOTE 3: If RTT_NOM is disabled in BC00, BODT input receiver will be disabled to save power.

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Host interface ODT is applied to the DQ[7:0], DQS0_t/DQS0_c and DQS1_c/DQS1_t pins. The DDR4RCD02 controls the DDR4DB02 host interface ODT condition with BCOM WR/RD command and BODT pin.

The DRAM interface ODT mode of the DDR4DB02 has 2 states, Data Termination Disable and RTT_MDQ. The value of RTT_MDQ is determined by the settings of bits DA[2:0] in BC04.

After entering clock stopped power down mode or CKE power down mode, the DDR4DB02 automatically disables the DRAM interface MDQS/MDQ termination regardless of these setting. If RTT_PARK is enabled in BC02 DA[2:0], the data buffer must continue to provide RTT_PARK termination while in CKE power down state regardless of the setting in BC09 DA2. This is needed to match the behavior described for the DDR4 SDRAM in section 4.28.1 of JESD79-4,

DRAM interface ODT is applied to the MDQ[7:0], MDQS0_t/MDQS0_c and MDQS1_c/MDQS1_t pins. The DDR4RCD02 controls the DDR4DB02 DRAM interface ODT condition with BCOM RD command.

The DDR4DB02 supports On Die Termination effective RTT values of 240 Ω, 120 Ω, 80 Ω, 60 Ω, 48 Ω, 40 Ω, and 34 Ω and infinite. However, each specific host interface or DRAM interface state may only support a subset of these values - see BC00, BC01, BC02 and BC04 definitions.

A functional representation of the On-Die Termination is shown in the figure below.

$$RTT = \frac{V_{DD} - V_{out}}{|\ I_{out}\ |}$$

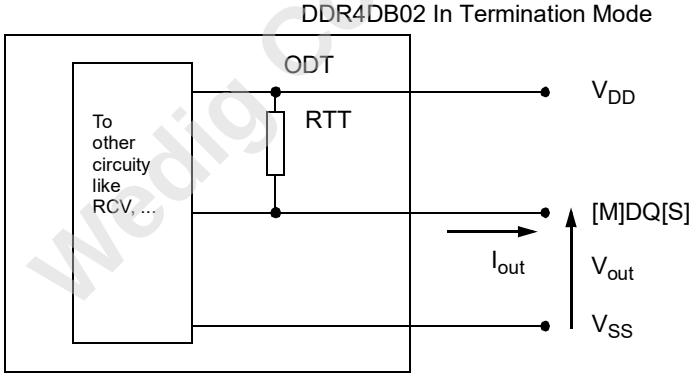

Figure 50 — On Die Termination

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The values in Table 117 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 Ω +/- 1%.

Table 117 — ODT DC Electrical Characteristics

RTT	Vout	min	nom	max	Unit	Note
240 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	R_{ZQ}	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	R_{ZQ}	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	R_{ZQ}	1, 2
120 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/2$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/2$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/2$	1, 2
80 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/3$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/3$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/3$	1, 2
60 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/4$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/4$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/4$	1, 2
48 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/5$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/5$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/5$	1, 2
40 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/6$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/6$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/6$	1, 2
34 Ω	VOLdc = 0.5 * V_{DD}	0.9	1.00	1.25	$R_{ZQ}/7$	1, 2
	VOMdc = 0.8 * V_{DD}	0.9	1.00	1.1	$R_{ZQ}/7$	1, 2
	VOHdc = 1.1 * V_{DD}	0.8	1.00	1.1	$R_{ZQ}/7$	1, 2
[M]DQ-[M]DQ mismatch within byte	VOMdc = 0.8 * V_{DD}	0		10	%	1, 2, 3, 4

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DD} and 1.1 * V_{DD}.
3. [M]DQ to [M]DQ mismatch within byte variation for a given component including [M]DQS_t and [M]DQS_c (characterized).
4. RTT variance range ratio to RTT nominal value in a given component, including [M]DQS_t and [M]DQS_c.

$$MM_{DQ-DQ} = \frac{R_{TT}Max - R_{TT}Min}{R_{TT}Nom} x100$$

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8 DC specifications, IDD Measurement Conditions

8.1 DC Electrical Characteristics

Table 118 — DC Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input current	$V_I = V_{DD}$ or GND	-	-	±5	µA
I_{ID}	Input current	Data inputs[1], $V_I = V_{DD}$ or GND	-	-	±25	µA

1. DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c

8.2 IDD Specification Parameters and Test Conditions

In this chapter, IDD measurement conditions such as test load and patterns are defined. Figure 51 shows the setup and test load for IDD measurements.

- IDD currents are measured as time-averaged currents with all V_{DD} balls of the DDR4DB02 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin as specified in Table 117 .
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR4DB02. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 52.

For IDD measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{IL(AC)}$.max.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IH(AC)}$.min.
- "MID-LEVEL" is defined as inputs are Vref = V_{DD} / 2.
- Basic IDD Measurement Conditions are described in Table 119.
- Detailed IDD Measurement-Loop Patterns are described in Table 120 through Table 131.
- IDD Measurements are done after properly initializing the DDR4DB02. This includes but is not limited to setting
  Host interface RTT_WR = R_{ZQ}/4 (60 Ω in BC01);
  Host interface RTT_PARK = R_{ZQ}/7 (34 Ω in BC02);
  Host interface RON = R_{ZQ}/7 (34 Ω in BC03);
  DRAM interface RTT = R_{ZQ}/5 (48 Ω in BC04);
  DRAM interface RON = R_{ZQ}/7 (34 Ω in BC05);
  Host interface DQ/DQS and DRAM interface DQ/DQS drivers enabled in BC03 and BC05 respectively;
  Fixed burst length = 8 (Fixed) in F4BC0x;
  Write CRC disabled in F4BC2x;
  Read preamble = 1 nCK and Write Preamble = 1 nCK in F4BC4x
- **ATTENTION:** The IDD Measurement-Loop Patterns need to be executed at least one time before actual IDD measurement is started.

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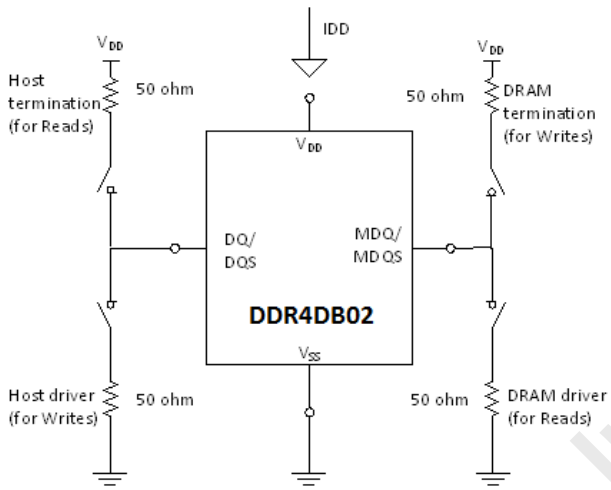

Figure 51 — Measurement Setup and Test Load for IDD Measurements

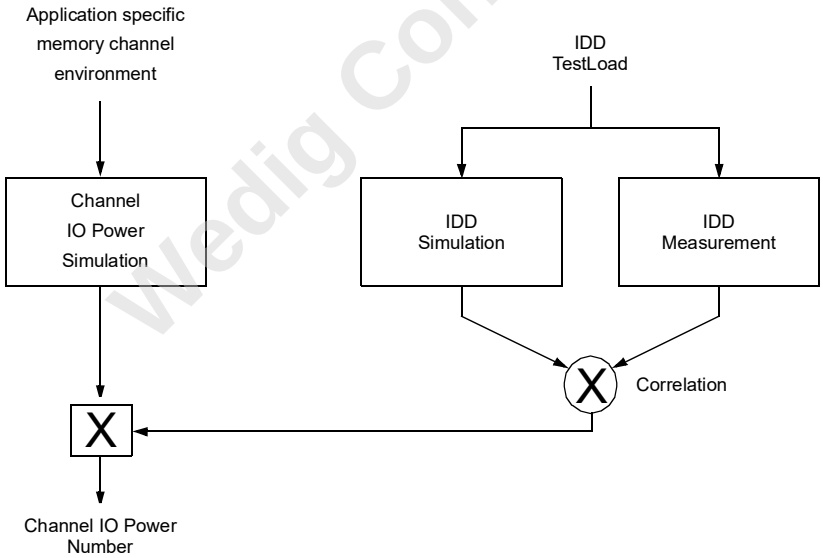

Figure 52 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDD Measurement

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Table 119 — Basic IDD Measurement Conditions

Symbol	Description
IDD3N1	**Active Idle Current with 50% LOW / 50% HIGH Data** **BCKE**: HIGH; **External clock:** On; **Data IO:** see Table 120 on page 144; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, RTT_PARK = 34 Ω ; **BODT Signal:** stable at 0; **Pattern Details:** see Table 120 on page 144
IDD3P1	**CKE Power Down Current with ODT On (BC09 DA[3:2] = 10) with 50% LOW / 50% HIGH Data** **BCKE:** LOW; **External clock:** On; **Data IO:** see Table 120 on page 144; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, RTT_PARK = 34 Ω; **BODT Signal:** stable at 0; **Pattern Details:** see Table 121 on page 144
IDD3P2	**CKE Power Down Current with ODT Off (BC09 DA[3:2] = 11) with 50% LOW / 50% HIGH Data** **BCKE:** LOW; **External clock:** On; **Data IO:** see Table 120 on page 144; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, RTT_PARK = disabled;**BODT Signal:** MID-LEVEL; **Pattern Details:** see Table 121 on page 144
IDD3N2	**Active Idle Current with 100% LOW Data** **Pattern Details:** see Table 122 on page 145; **Other conditions:** see IDD3N1
IDD3P3	**CKE Power Down Current with ODT On (BC09 DA[3:2] = 10) with 100% LOW Data** **Pattern Details:** see Table 123 on page 145; **Other conditions:** see IDD3P1
IDD3P4	**CKE Power Down Current with ODT Off (BC09 DA[3:2] = 11) with 100% LOW Data** **Pattern Details:** see Table 123 on page 145; **Other conditions:** see IDD3P2
IDD4R1	**Operating Burst Read Current with 100% utilization and 50% LOW / 50% HIGH Data** **BCKE:** HIGH; **External clock:** On; **BL**: 8[1]; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 124 on page 146; **Host interface Output Buffer:** RON = 34 Ω ; **DRAM drive strength:** Ron = 50 Ω; **DRAM interface ODT:** RTT = 48 Ω; **BODT Signal:** stable at 0; **Pattern Details:** see Table 124 on page 146
IDD4R2	**Operating Burst Read Current with 25% utilization and 50% LOW / 50% HIGH Data** **Pattern Conditions**: see Table 125 on page 147; **Other conditions:** see IDD4R1
IDD4R3	**Operating Burst Read Current with 100% utilization and 100% LOW Data** **Pattern Details:** see Table 126 on page 148; **Other conditions:** see IDD4R1
IDD4R4	**Operating Burst Read Current with 25% utilization and 100% LOW Data** **Pattern Details**: see Table 127 on page 149; **Other conditions:** see IDD4R1
IDD4W1	**Operating Burst Write Current with 100% utilization and 50% LOW / 50% HIGH Data** **BCKE:** HIGH; **External clock:** On; **BL**: 8[1]; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 128 on page 150; **Host drive strength:** Ron = 50 Ω; **Host interface ODT:** RTT_WR = 60 Ω; **DRAM interface Output Buffer:** RON = 34 Ω; **DRAM ODT:** RTT_WR = 50 Ω; **BODT Signal:** stable at 0; **Pattern Details:** see Table 128 on page 150
IDD4W2	**Operating Burst Write Current with 25% utilization and 50% LOW / 50% HIGH Data** **Data IO**: see Table 129 on page 151; **Other conditions:** see IDD4W1
IDD4W3	**Operating Burst Write Current with 100% utilization and 100% LOW Data** **Pattern Details:** see Table 130 on page 152; **Other conditions:** see IDD4W1
IDD4W4	**Operating Burst Write Current with 25% utilization and 100% LOW Data** **Pattern Details**: see Table 131 on page 153; **Other conditions:** see IDD4W1
IDD6R	**Static Reset Current** **BCKE:** HIGH; **External clock:** Off; BCK_t and BCK_c: LOW; **Data IO:** V_{DD}; **BODT Signal:** MID-LEVEL
IDD6S	**Clock Stopped Power Down Current** **BCKE:** LOW; **External clock:** Off; BCK_t and BCK_c: LOW; **Data IO:** V_{DD}; **BODT Signal:** MID-LEVEL

NOTE 1: Burst Length BL8 fixed: set F4BC0x DA[1:0] = 00

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Table 120 — IDD3N1 Measurement-Loop Pattern

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[1]
toggling	Static HIGH	0	0	1010 (NOP)	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	1010 (NOP)	0	-
			2	1010 (NOP)	0	-
			3	1010 (NOP)	0	-
		1	4	1010 (NOP)	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-

NOTE 1: DQ and DQS signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 121 — IDD3P1 and IDD3P2 Measurement-Loop Pattern

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT[1]	Data[2]
toggling	Static LOW	0	0	1010 (NOP)	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	1010 (NOP)	0	-
			2	1010 (NOP)	0	-
			3	1010 (NOP)	0	-
		1	4	1010 (NOP)	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-

NOTE 1: BODT is terminated at MID-LEVEL for IDD3P2 measurements.
NOTE 2: DQ and DQS signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

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Table 122 — IDD3N2 Measurement-Loop Pattern

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[1]
toggling	Static HIGH	0	0	1010 (NOP)	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	1010 (NOP)	0	-
			2	1010 (NOP)	0	-
			3	1010 (NOP)	0	-
		1	4	1010 (NOP)	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-

NOTE 1: DQ and DQS signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 123 — IDD3P3 and IDD3P4 Measurement-Loop Pattern

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT[1]	Data[2]
toggling	Static LOW	0	0	1010 (NOP)	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	1010 (NOP)	0	-
			2	1010 (NOP)	0	-
			3	1010 (NOP)	0	-
		1	4	1010 (NOP)	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-

NOTE 1: BODT is terminated at MID-LEVEL for IDD3P4 measurements.
NOTE 2: DQ and DQS signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

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Table 124 — IDD4R1 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1001 (RD)**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	0100 (BC8, Rank 0)	0	-
			2	1101 (Even Parity)	0	-
			3	1010 (NOP)	0	-
		1	4	**1001 (RD)**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	0100 (BC8, Rank 0)	0	-
			6	1101 (Even Parity)	0	-
			7	1010 (NOP)	0	-
		2[3]	8	1010(NOP)	0	-
			9	1010(NOP)	0	-
			10	1010(NOP)	0	-
		3	11,12,13,14	repeat Sub-Loop 0, use Rank 1 instead		
		4	15,16,17,18	repeat Sub-Loop 1, use Rank 1 instead		
		5[3]	19,20,21	repeat Sub-Loop 2		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD8 Commands.
NOTE 2: Burst Sequence received on each MDQ pin and driven on each DQ pin by RD8 Command.
NOTE 3: Since timings for 2666 MT/s and higher are still undefined, therefore additional NOPs may be required.

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Table 125 — IDD4R2 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub -Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1001 (RD)**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	0100 (BC8, Rank 0)	0	-
			2	1101 (Even Parity)	0	-
			3	1010 (NOP)	0	-
			4	1010 (NOP)	0	-
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-
			8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
			11	1010 (NOP)	0	-
			12	1010 (NOP)	0	-
			13	1010 (NOP)	0	-
			14	1010 (NOP)	0	-
			15	1010 (NOP)	0	-
		1	16	**1001 (RD)**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			17	0100 (BC8, Rank 0)	0	-
			18	1101 (Even Parity)	0	-
			19	1010 (NOP)	0	-
			20	1010 (NOP)	0	-
			21	1010 (NOP)	0	-
			22	1010 (NOP)	0	-
			23	1010 (NOP)	0	-
			24	1010 (NOP)	0	-
			25	1010 (NOP)	0	-
			26	1010 (NOP)	0	-
			27	1010 (NOP)	0	-
			28	1010 (NOP)	0	-
			29	1010 (NOP)	0	-
			30	1010 (NOP)	0	-
			31	1010 (NOP)	0	-
		2	32-47	repeat Sub-Loop 0, use Rank 1 instead		
		3	48-63	repeat Sub-Loop 1, use Rank 1 instead		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD8 Commands, otherwise V_{DD}.
NOTE 2: Burst Sequence received on each MDQ pin and driven on each DQ pin by RD8 Command, otherwise V_{DD}.

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Table 126 — IDD4R3 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1001 (RD)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	0100 (BC8, Rank 0)	0	-
			2	1101 (Even Parity)	0	-
			3	1010 (NOP)	0	-
		1	4	**1001 (RD)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			5	0100 (BC8, Rank 0)	0	-
			6	1101 (Even Parity)	0	-
			7	1010 (NOP)	0	-
		2[3]	8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
		3	11,12,13,14	repeat Sub-Loop 0, use Rank 1 instead		
		4	15,16,17,18	repeat Sub-Loop 1, use Rank 1 instead		
		5[3]	19,20,21	repeat Sub-Loop 2		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD8 Commands.
NOTE 2: Burst Sequence received on each MDQ pin and driven on each DQ pin by RD8 Command.
NOTE 3: Since timings for 2666 MT/s and higher are still undefined, therefore additional NOPs may be required.

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Table 127 — IDD4R4 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub -Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1001 (RD)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	0100 (BC8, Rank 0)	0	-
			2	1101 (Even Parity)	0	-
			3	1010 (NOP)	0	-
			4	1010 (NOP)	0	-
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-
			8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
			11	1010 (NOP)	0	-
			12	1010 (NOP)	0	-
			13	1010 (NOP)	0	-
			14	1010 (NOP)	0	-
			15	1010 (NOP)	0	-
		1	16	**1001 (RD)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			17	0100 (BC8, Rank 0)	0	-
			18	1101 (Even Parity)	0	-
			19	1010 (NOP)	0	-
			20	1010 (NOP)	0	-
			21	1010 (NOP)	0	-
			22	1010 (NOP)	0	-
			23	1010 (NOP)	0	-
			24	1010 (NOP)	0	-
			25	1010 (NOP)	0	-
			26	1010 (NOP)	0	-
			27	1010 (NOP)	0	-
			28	1010 (NOP)	0	-
			29	1010 (NOP)	0	-
			30	1010 (NOP)	0	-
			31	1010 (NOP)	0	-
		2	32-47	repeat Sub-Loop 0, use Rank 1 instead		
		3	48-63	repeat Sub-Loop 1, use Rank 1 instead		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD8 Commands, otherwise V_{DD}.
NOTE 2: Burst Sequence received on each MDQ pin and driven on each DQ pin by RD8 Command, otherwise V_{DD}.

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Table 128 — IDD4W1 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1000 (WR)**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	0100 (BC8, Rank 0)	0	-
			2	1100 (Even Parity)	0	-
			3	1010 (NOP)	0	-
		1	4	**1000 (WR)**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	0100 (BC8, Rank 0)	0	-
			6	1100 (Even Parity)	0	-
			7	1010 (NOP)	0	-
		2[3]	8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
		3	11,12,13,14	repeat Sub-Loop 0, use Rank 1 instead		
		4	15,16,17,18	repeat Sub-Loop 1, use Rank 1 instead		
		5[3]	19,20,21	repeat Sub-Loop 2		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR8 Commands.
NOTE 2: Burst Sequence received on each DQ pin and driven on each MDQ pin by WR8 Command.
NOTE 3: Since timings for 2666 MT/s and higher are still undefined, therefore additional NOPs may be required.

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Table 129 — IDD4W2 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1000 (WR)**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	0100 (BC8, Rank 0)	0	-
			2	1100 (Even Parity)	0	-
			3	1010 (NOP)	0	-
			4	1010 (NOP)	0	-
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-
			8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
			11	1010 (NOP)	0	-
			12	1010 (NOP)	0	-
			13	1010 (NOP)	0	-
			14	1010 (NOP)	0	-
			15	1010 (NOP)	0	-
			16	**1000 (WR)**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			17	0100 (BC8, Rank 0)	0	-
			18	1100 (Even Parity)	0	-
			19	1010 (NOP)	0	-
			20	1010 (NOP)	0	-
			21	1010 (NOP)	0	-
			22	1010 (NOP)	0	-
			23	1010 (NOP)	0	-
			24	1010 (NOP)	0	-
			25	1010 (NOP)	0	-
			26	1010 (NOP)	0	-
			27	1010 (NOP)	0	-
			28	1010 (NOP)	0	-
			29	1010 (NOP)	0	-
			30	1010 (NOP)	0	-
			31	1010 (NOP)	0	-
		2	32-47	repeat Sub-Loop 0, use Rank 1 instead		
		3	48-63	repeat Sub-Loop 1, use Rank 1 instead		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR8 Commands, otherwise V_{DD}.
NOTE 2: Burst Sequence received on each DQ pin and driven on each MDQ pin by WR8 Command, otherwise V_{DD}.

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Table 130 — IDD4W3 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1000 (WR)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	0100 (BC8, Rank 0)	0	-
			2	1100 (Even Parity)	0	-
			3	1010 (NOP)	0	-
		1	4	**1000 (WR)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			5	0100 (BC8, Rank 0)	0	-
			6	1100 (Even Parity)	0	-
			7	1010 (NOP)	0	-
		2[3]	8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
		3	11,12,13,14	repeat Sub-Loop 0, use Rank 1 instead		
		4	15,16,17,18	repeat Sub-Loop 1, use Rank 1 instead		
		5[3]	19,20,21	repeat Sub-Loop 2		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR8 Commands.
NOTE 2: Burst Sequence received on each DQ pin and driven on each MDQ pin by WR8 Command.
NOTE 3: Since timings for 2666 MT/s and higher are still undefined, therefore additional NOPs may be required

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Table 131 — IDD4W4 Measurement-Loop Pattern[1]

BCK_t, BCK_c	BCKE	Sub-Loop	Cycle Number	BCOM	BODT	Data[2]
toggling	Static HIGH	0	0	**1000 (WR)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			1	0100 (BC8, Rank 0)	0	-
			2	1100 (Even Parity)	0	-
			3	1010 (NOP)	0	-
			4	1010 (NOP)	0	-
			5	1010 (NOP)	0	-
			6	1010 (NOP)	0	-
			7	1010 (NOP)	0	-
			8	1010 (NOP)	0	-
			9	1010 (NOP)	0	-
			10	1010 (NOP)	0	-
			11	1010 (NOP)	0	-
			12	1010 (NOP)	0	-
			13	1010 (NOP)	0	-
			14	1010 (NOP)	0	-
			15	1010 (NOP)	0	-
			16	**1000 (WR)**	0	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00**
			17	0100 (BC8, Rank 0)	0	-
			18	1100 (Even Parity)	0	-
			19	1010 (NOP)	0	-
			20	1010 (NOP)	0	-
			21	1010 (NOP)	0	-
			22	1010 (NOP)	0	-
			23	1010 (NOP)	0	-
			24	1010 (NOP)	0	-
			25	1010 (NOP)	0	-
			26	1010 (NOP)	0	-
			27	1010 (NOP)	0	-
			28	1010 (NOP)	0	-
			29	1010 (NOP)	0	-
			30	1010 (NOP)	0	-
			31	1010 (NOP)	0	-
		2	32-47	repeat Sub-Loop 0, use Rank 1 instead		
		3	48-63	repeat Sub-Loop 1, use Rank 1 instead		

NOTE 1: [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR8 Commands, otherwise V_{DD}.
NOTE 2: Burst Sequence received on each DQ pin and driven on each MDQ pin by WR8 Command, otherwise V_{DD}.

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9 Input/Output Capacitance

Table 132 — Silicon pad I/O Capacitance values

Symbol	Parameter	Conditions	DDR4-1600 to 2400		DDR4-2666		DDR4- 2933		DDR4- 3200		Unit
			min	max	min	max	min	max	min	max	
C_{IO}	Input/Output capacitance, DQ IOs	see footnote[1,2]	0.7	1.5	0.7	1.15	0.7	1.1	0.7	1.1	pF
C_{IOD}	Delta capacitance over all DQ IOs	see footnote [2]	-	0.2	-	0.15	-	0.10	-	0.10	pF
C_{DQSD}	Delta capacitance between DQS_t and DQS_c		-	0.1	-	0.05	-	0.04	-	0.04	pF
C_I	Input capacitance, Control inputs	see footnote[1,3]	0.2	0.8	0.2	0.8	0.2	0.8	0.2	0.8	pF
C_{ID}	Delta capacitance over all control inputs	see footnote [3]	-	0.2	-	0.2	-	0.2	-	0.2	pF
C_{CK}	Input capacitance, BCK_t, BCK_c	see footnote[1]	0.2	0.9	0.2	0.9	0.2	0.9	0.2	0.9	pF
C_{DCK}	Input capacitance delta BCK_t and BCK_c	see footnote[1,4]	-	0.1	-	0.1	-	0.1	-	0.1	pF
C_{ALERT}	Input/output capacitance of ALERT_n		0.5	2	0.5	2	0.5	2	0.5	2	pF

1. This parameter does not include package capacitance
2. DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c
3. BCOM[3:0], BCKE, BODT
4. Absolute value BCK_t - BCK_c

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Table 133 — Package electrical specifications

Symbol	Parameter	DDR4-1600 to 3200		Unit	Notes
		Min	Max		
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	40	70	Ω	1, 2, 4
$Td_{I\ CTRL}$	Input CTRL pins Pkg Delay	15	30	ps	1, 3, 4
$DTd_{I\ CTRL}$	Delta CTRL pins Pkg Delay	-	6	ps	1,3, 4
$Z_{I\ DQ}$	Input/Output DQ pins Zpkg	40	55	Ω	1, 2, 5
Td_{DQ}	Input/Output DQ pins Pkg Delay	12	30	ps	1, 3, 5
DTd_{DQ}	Delta DQ pins Pkg Delay	-	6	ps	1, 3, 5
Z_{CK}	Input BCK pins ZPkg	40	65	Ω	1, 2, 8
Td_{CK}	Input BCK pins Pkg Delay	15	30	ps	1, 3
DZ_{DCK}	Delta Zpkg BCK_t and BCK_c	-	10	Ω	1, 2, 6
DTd_{DCK}	Delta Delay BCK_t and BCK_c	-	5	ps	1, 3, 7
$Z_{O\ ZQ}$	Output ZQCAL Zpkg	30	100	Ω	1, 2
$Z_{O\ ALERT}$	Output ALERT_n Zpkg	30	100	Ω	1, 2
$Td_{O\ ALERT}$	Output ALERT_n Pkg Delay	10	35	ps	1, 3

NOTE 1: This parameter is not subject to production test. It is verified by design and characterization. The package parasitics (L &C) are determined using package only samples. Package capacitance and inductance are computed from S-parameter models. The capacitance is derived with V_{DD}, V_{SS} shorted and all other signals floating. The inductance is derived with V_{DD}, V_{SS} shorted and all other signals shorted at the die side (not pin). .
NOTE 2: Package only impedance (Zpkg) is calculated based on the computed Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT(Lpkg/Cpkg)
NOTE 3: Package only delay (Tdpkg) is calculated based on computed Lpkg and Zpkg total for a given pin where: Tdpkg (total per pin) = SQRT(Lpkg*Cpkg)
NOTE 4: This value applies to BCOM[3:0], BCKE, BODT
NOTE 5: This value applies to DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c
NOTE 6: Absolute value of ZCK_t - ZCK_c
NOTE 7: Absolute value of TdCK_t - TdCK_c
NOTE 8: Single-ended impedance

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10 Timing Requirements

10.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4DB02 device.

10.1.1 Definition for $t_{CK(avg)}$, nCK and $t_{CH(avg)}$ and $t_{CL(avg)}$

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$
$$where \qquad N = 200$$

Unit '$t_{CK(avg)}$' represents the actual clock average $t_{CK(avg)}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. $t_{CK(avg)}$ may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

$\mathbf{t}_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

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10.1.2 Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $t_{CK(abs)}$ is not subject to production test.

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 134 — Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg),min} + t_{JIT(per),min}$	ps
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	$t_{CH(avg),min} + t_{JIT(duty),min} / t_{CK(avg)min}$	$t_{CK(avg)}$
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	$t_{CL(avg),min} + t_{JIT(duty),min} / t_{CK(avg)min}$	$t_{CK(avg)}$

NOTE 1 $t_{CK(avg),min}$ is expressed is ps for this table.
NOTE 2 $t_{JIT(duty),min}$ is a negative value.

10.1.3 Definition for t_{JIT}(per)

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.

$t_{JIT(per)}$ = Min/max of $\{t_{CKi} - t_{CK}(avg)$ where $i = 1$ to $200\}$.

$t_{JIT(per),act}$ is the actual clock jitter for a given system.

$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.

$t_{JIT(per)}$ is not subject to production test.

10.1.4 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT(cc)}$ = Max of $|\{t_{CKi+1} - t_{CKi}\}|$.

$t_{JIT(cc)}$ defines the cycle to cycle jitter.

$t_{JIT(cc)}$ is not subject to production test.

10.1.5 Definition for duty cycle jitter $t_{JIT(duty)}$

$t_{JIT(duty)}$ is defined with absolute and average specification of t_{CH} / t_{CL}.

tJIT(duty), min

$$T(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

tJIT(duty), max

$$T(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

10.1.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.

$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.

$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.

$t_{ERR(nper)}$ is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

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$t_{ERR(nper),min}$ can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$t_{ERR(nper),max}$ can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

10.2 Clock Requirements

Table 135 — Clock Timing Requirements DDR4-1600 to DDR4-2133

Symbol	Parameter	Conditions	DDR4-1600		DDR4-1866		DDR4-2133		Unit
			Min	Max	Min	Max	Min	Max	
tCK(avg, Clock)	Average Clock Period	Application Frequency	1.25	1.6	1.071	1.6	0.938	1.6	ns
tCK(avg, Test)	Average Clock Period	Test Frequency	1.6	7.143	1.6	7.143	1.6	7.143	ns
tJIT(per)_dj	Clock Period Jitter - deterministic[4]		-31	31	-27	27	-23	23	ps

Table 136 — Clock Timing Requirements DDR4-2400 to DDR4-3200

Symbol	Parameter	Conditions	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tCK(avg, Clock)	Average Clock Period	Application Frequency	0.833	1.6	0.750	1.6	0.681	1.6	0.625	1.6	ns
tCK(avg, Test)	Average Clock Period	Test Frequency	1.6	7.143	1.6	7.143	1.6	7.143	1.6	7.143	ns
tJIT(per)_dj	Clock Period Jitter - deterministic[4]		-21	21	-19	19	-17	17	-16	-16	ps

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Table 137 — Clock Timing Requirement 1600 - 3200

Symbol	Parameter	Conditions	DDR4-1600 -3200		Unit
			Min	Max	
tCH(avg)	Average HIGH pulse width		0.48	0.52	$t_{CK(avg)}$
tCL(avg)	Average LOW pulse width		0.48	0.52	$t_{CK(avg)}$
tCH(abs)	Absolute Clock HIGH pulse width[1]		0.45	-	$t_{CK(avg)}$
tCL(abs)	Absolute Clock LOW pulse width[2]		0.45	-	$t_{CK(avg)}$
tCK(abs)	Absolute Clock Period		tCK(avg),min + tJIT(per)_tot, min	tCK(avg),max + tJIT(per)_tot, max	ns
tJIT(per)_tot	Clock Period Jitter - total[1]		-0.1	0.1	UI
tJIT(per, lck)	Clock Period Jitter during tDLLK		-0.08	0.08	UI
tJIT(cc)_tot	Cycle to Cycle Period Jitter - total[3]		0.2		UI
tJIT(cc, lck)	Cycle to Cycle Period Jitter during tDLLK		0.16		UI
tJIT(duty)	Duty cycle jitter		-tbd	-tbd	UI
tERR(2per)	Cumulative error across 2 cycles		-0.1471	0.1471	UI
tERR(3per)	Cumulative error across 3 cycles		-0.1747	0.1747	UI
tERR(4per)	Cumulative error across 4 cycles		-0.1943	0.1943	UI
tERR(5per)	Cumulative error across 5 cycles		-0.2094	0.2094	UI
tERR(6per)	Cumulative error across 6 cycles		-0.2218	0.2218	UI
tERR(7per)	Cumulative error across 7 cycles		-0.2323	0.2323	UI
tERR(8per)	Cumulative error across 8 cycles		-0.2414	0.2414	UI
tERR(9per)	Cumulative error across 9 cycles		-0.2494	0.2494	UI
tERR(10per)	Cumulative error across 10 cycles		-0.2566	0.2566	UI
tERR(11per)	Cumulative error across 11 cycles		-0.2631	0.2631	UI
tERR(12per)	Cumulative error across 12 cycles		-0.2690	0.2690	UI
tERR(nper)	Cumulative error across n = 13, 14 ... 49,50 cycles		tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		UI

1. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.

Table 138 — SSC Characteristics

Symbol	Parameter	Conditions	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit
			Min	Max	
f_{SSC}	SSC modulation frequency[1]		30	33	kHz
a_{SSC}	SSC amplitude[1]		0	-0.5	%

1. The DDR4DB02 must meet all parameters defined in this specification while supporting input clock SSC requirements described in this table

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10.3 Input Timing Requirements

Table 139 — Input Timing requirements

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4-2933/ 3200		Unit
			Min	Max	Min	Max	Min	Max	
t_{ACT}	Inputs active time[1] before BCKE is taken LOW		16	-	16	-	16	-	t_{CK}
t_{CCD_CMP}	Command to command delay with data comparison	Number of clock cycles between DRAM commands during training modes with data comparison	8		8		8		t_{CK}
t_{MRD_PBA}	Control word to control word delay in PBA mode	Number of clock cycles between two buffer control word accesses or any DRAM commands in PBA mode	AL+CWL + PL +3.5 + t_{MOD_PBA}	-	AL+CWL + PL +3.5 + t_{MOD_PBA}	-	AL+CWL + PL +3.5 + t_{MOD_PBA}	-	t_{CK}
t_{MOD_PBA}	Per buffer command update delay	Number of clock cycles from end of PBA mode BCW write to next buffer control word access or any DRAM command	16	-	16	-	16	-	t_{CK}
t_{MRD_L2}	Control word to control word delay	Number of clock cycles between an access to timing related BCWs[2] and the next control word access or DRAM command. Number of clock cycles between any DFE related control words access in DFE training mode.	32	-	32	-	32	-	t_{CK}
t_{MRC}	Buffer command word to BCW or DRAM command delay	Number of clock cycles between buffer command word (BC06) and CW or any DRAM command	16	-	16	-	16	-	t_{CK}
t_{BCW}	Delay between BCW Write or MRS Write and other commands	Number of cycles between BCW Write or MRS Write and CW or any DRAM commands	16	-	16	-	16	-	t_{CK}
t_{BCR}	Delay between BCW Read and the following 1st DRAM Read command and delay from this 1st DRAM Read command to the next DRAM Read command	Number of cycles between BCW Read and 1st DRAM Read command and between 1st DRAM Read command and next Read command[3]	16	-	16	-	16	-	t_{CK}
t_{PBA_S}	DQ0 driven to 0 set-up time to time corresponding to first DQS rising edge[4,5]		0.5	-	0.5	-	0.5	-	UI
t_{PBA_H}	DQ0 driven to 0 hold time to time corresponding to first DQS rising edge[5,6]		0.5	-	0.5	-	0.5	-	UI

1. This parameter is not necessarily production tested.
2. This parameter applies to BCWs F0BC06, F0BC07, F0BC0A, F0BC0C, F0BC1x, F0BC6x, F[1:0]BCCx/Dx/Ex/Fx, F[3:0]BC2x/3x, F[3:0]BC4x/5x, F[3:0]BC8x/9x, F[3:0]BCAx/Bx, F[7:4]BC8x/9x, F[7:4]BCAx/Bx, F[7:4]BCCx/Dx/Ex/Fx and F5BC4x.The DDR4DB02 device is not required to process DRAM Read/Write data transactions correctly for commands received within the $t_{MRD_L2\ Min}$ window.
3.When sending a BCW Read command to the DDR4DB02 device, the host controller must ensure correct BCW Read command spacing so no data bits from a previous BCW Read are in the MPR0 multipurpose registers which have not yet been sent back to the host on the DQ bus.
4.DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
5.Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
6.BVrefCA value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

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10.4 Host and DRAM Interface Preamble and Postamble Timing Requirements

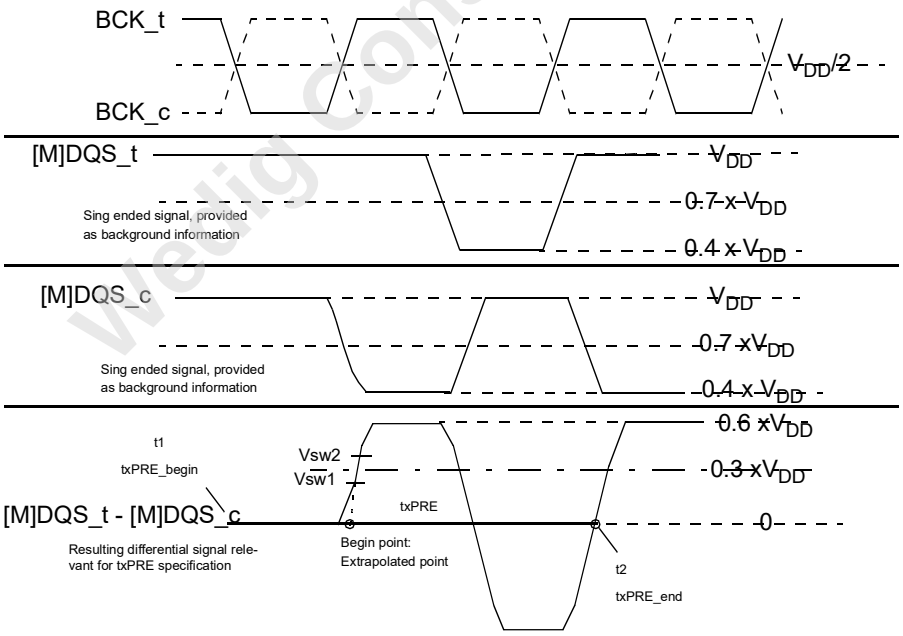
Table 140 — [M]DQS Preamble and Postamble timing requirements

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4-2933/ 3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Data Strobe [M]DQS Input Timing										
tIPRE	Input preamble of strobe signal received by the DDR4DB02		0.85	-	0.85	-	0.85	-	t_{CK}	1
tIPST	Input postamble of strobe signal received by the DDR4DB02		0.30	-	0.30	-	0.30	-	t_{CK}	1
Data Strobe [M]DQS Output Timing										
tOPRE	Output preamble of strobe signal driven by the DDR4DB02		0.95	-	0.95	-	0.95	-	t_{CK}	2, 3
tOPST	Output postamble of strobe signal driven by the DDR4DB02		0.36	-	0.36	-	0.36	-	t_{CK}	2, 3

NOTE 1: These values assume that the DDR4 DRAM's tRPRE and tRPST numbers remain at 0.9 * t_{CK} and 0.33 * t_{CK} respectively.
NOTE 2: These values assume that the DDR4 DRAM's tWPRE and tWPST numbers are 0.9 * t_{CK} and 0.33 * t_{CK} respectively.
NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

10.4.1 txPRE Calculation

The method for calculating differential pulse widths for tIPRE and tOPRE is shown in Figure 53.



NOTE 1: A driver impedance: RZQ/7 (34 Ω)
An effective test load: 50 Ω to V_{DD}
Low Level of [M]DQS_t and [M]DQS_c = V_{DD}/(50 + 34) x 34
= V_{DD} x 0.40

Figure 53 — Method for calculating txPRE transitions and endpoints

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Table 141 — Reference Voltage for txPRE Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t - DQS_c differential WRITE preamble	tIPRE	(0.30 - 0.04) x V_{DD}	(0.30 + 0.04) x V_{DD}	
MDQS_t - MDQS_c differential READ preamble				
DQS_t - DQS_c differential READ preamble	tOPRE	(0.30 - 0.04) x V_{DD}	(0.30 + 0.04) x V_{DD}	
MDQS_t - MDQS_c differential WRITE preamble				

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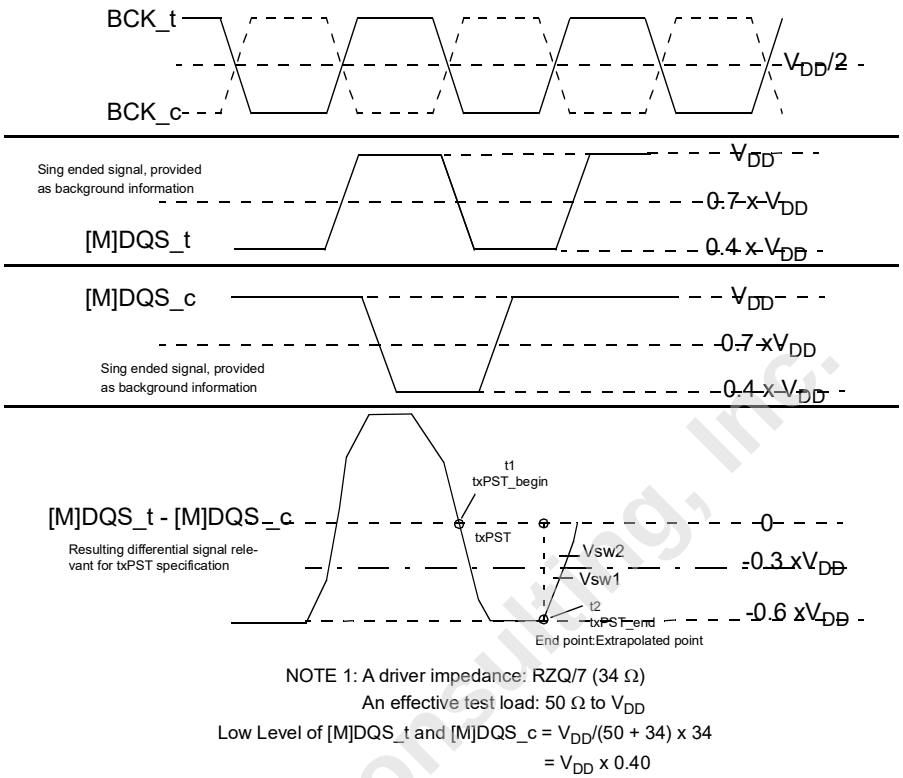
10.4.2 txPST Calculation

The method for calculating differential pulse widths for tIPST and tOPST is shown in Figure 54.



NOTE 1: A driver impedance: RZQ/7 (34 Ω)
An effective test load: 50 Ω to V_{DD}
Low Level of [M]DQS_t and [M]DQS_c = V_{DD}/(50 + 34) x 34
= V_{DD} x 0.40

Figure 54 — Method for calculating txPST transitions and endpoints

Table 142 — Reference Voltage for txPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t - DQS_c differential WRITE postamble	tIPST	-(0.30 - 0.04) x V_{DD}	-(0.30 + 0.04) x V_{DD}	
MDQS_t - MDQS_c differential READ postamble				
DQS_t - DQS_c differential READ postamble	tOPST	-(0.30 - 0.04) x V_{DD}	-(0.30 + 0.04) x V_{DD}	
MDQS_t - MDQS_c differential WRITE postamble				

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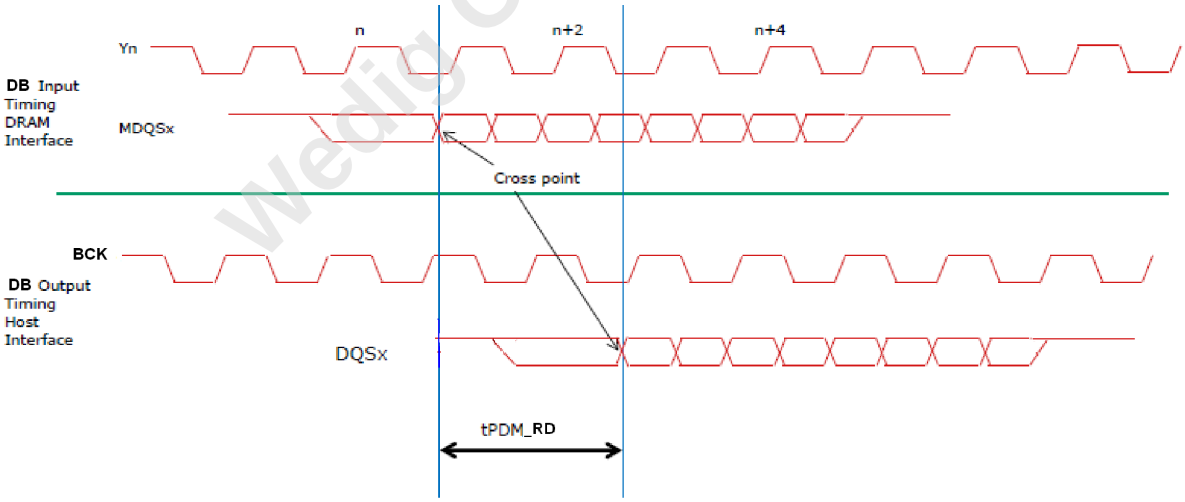
10.5 Output Timing Requirements

Table 143 — Output timing requirements

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PDM_RD}	MDQS to DQS Propagation Delay	1.2 V Operation[1,2,3,]	1.37 + tCK/4	1.62 + tCK/4	ns
t_{PDM_WR}	DQS to MDQS Propagation Delay	1.2 V Operation[1,2,3]	1.37 + tCK/4	1.62 + tCK/4	ns
t_{PDA_DQD}	MDQ to DQ and DQ to MDQ Propagation Delay in Transparent Mode	1.2 V Operation [1,2]	0.3	1.25	ns
D_{PDA_DQ}	Delta between earliest and latest DQx and MDQx bits in transparent mode	1.2 V Operation [1,2]	-	0.4	ns
t_{MRD_TM}	Delay between data direction changes in transparent mode	Number of clock cycles between Read to Write or Write to Read transactions in transparent mode	16[4]	-	tCK
t_{ALERT_HL}	ALERT_n assertion delay from BCK_t / BCK_c	BCK_t / BCK_c to ALERT_n LOW[5]	-	1.5	ns

1. These parameters are only guaranteed after the correct speed range has been programmed in BC0A
2. These timings are only valid with the DA[5:0] bits of the lower and upper nibble read delay and write delay control words (F[3:0]BC4x, F[3:0]BC5x, F[3:0]BC8x and F[3:0]BC9x) at their power on default of '00_0000' and default slew rate control setting of BC0B DA[3:2] = 00.
3. The DRAM tDQSCK parameter directly impacts the tPDM_RD/WR budget. These values assume that the DDR4 DRAM tDQSCK parameter is ~0.19 UI.
4.This value is defined as the minimum dead time between data transfers on the DQ/DQS data bus and the MDQ/ MDQS data bus when changing data path direction.
5. See Figure 62, "Load circuit, ALERT_n Outputs" on page 173 and Figure 63, "Voltage waveforms, tALERT_HL Measurement" on page 173.



tPDM_RD = MDQSx in (DRAM Interface) to DQSx (Host interface) Out

Figure 55 — tPDM_RD Latency Measurement

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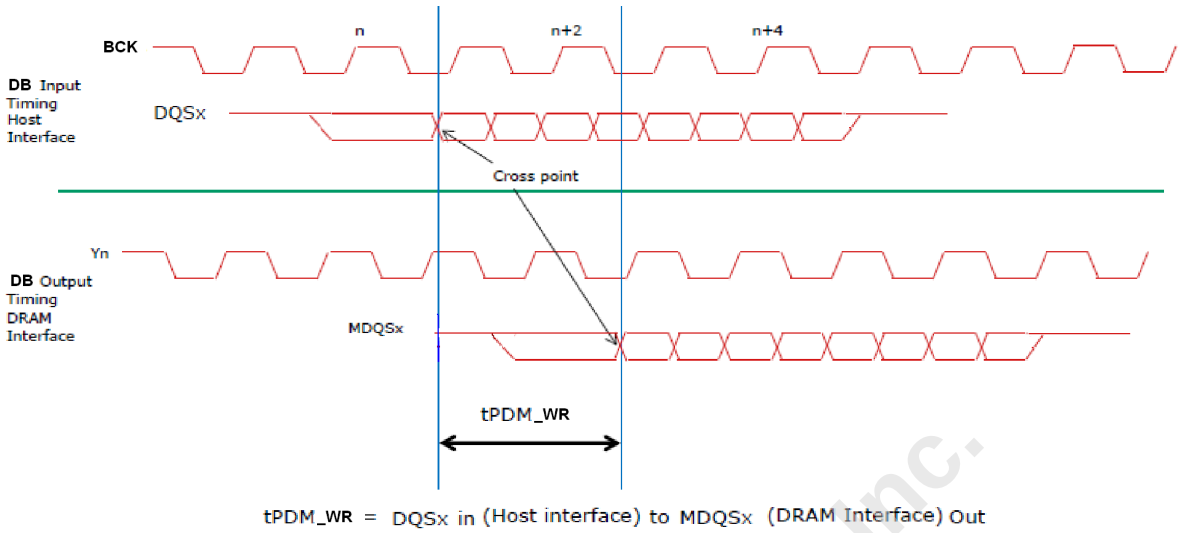

Figure 56 — tPDM_WR Latency Measurement

Table 144 — Output timing requirements in Package Rank Alignment Mode

Symbol	Parameter	Conditions		Min	Max	Unit
$t_{PDM_RD_RA}$[1]	MDQS to DQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + X(R)[5]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + Y(R)[6]	ns
$t_{PDM_WR_RA}$[1]	DQS to MDQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + Z(R)[7]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + W(R)[8]	ns

1. Applies when Package Rank Alignment mode is enabled (F0BC1x DA7 = 1). Package Rank Alignment granularity is 1/64*tCK. Upper Nibble and Lower Nibble are not required to be aligned by DDR4DB02.
2. These parameters are only guaranteed after the correct speed range has been programmed in BC0A
3. These timings are only valid with the DA[5:0] bits of the lower and upper nibble read delay and write delay control words (F[3:0]BC4x, F[3:0]BC5x, F[3:0]BC8x and F[3:0]BC9x) at their power on default of 6b'000000 and default slew rate control setting of BC0B DA[3:2] = 00.
4. Maximum temperature and voltage drift must be 170 ps or less for respective nibble.
5. The value of X is rank dependent and it is equal to the difference between MAX(F[3:0]BC2x) and the value of the Fn-BC2x corresponding to each rank. For example, for the earliest rank X = [MAX(F[3:0]BC2x) - MIN(F[3:0]BC2x)], and for the latest rank X = 0. DDR4DB02 supports the largest value of X of 500 ps.
6. The value of Y is rank dependent and it is equal to the difference between MAX(F[3:0]BC3x) and the value of the Fn-BC3x corresponding to each rank. For example, for the earliest rank Y = [MAX(F[3:0]BC3x) - MIN(F[3:0]BC3x)], and for the latest rank Y = 0. DDR4DB02 supports the largest value of Y of 500 ps.
7. The value of Z is rank dependent and it is equal to the difference between MIN(F[3:0]BCAx) and the value of the Fn-BCAx corresponding to each rank. For example, for the latest rank Z = [MAX(F[3:0]BCAx) - MIN(F[3:0]BCAx)], and for the earliest rank Z = 0. DDR4DB02 supports the largest value of Z of 500 ps.
8. The value of W is rank dependent and it is equal to the difference between MIN(F[3:0]BCBx) and the value of the Fn-BCBx corresponding to each rank. For example, for the latest rank W = [MAX(F[3:0]BCBx) - MIN(F[3:0]BCBx)], and for the earliest rank W = 0. DDR4DB02 supports the largest value of W of 500 ps.

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Ex. 1058, p. 165
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10.5.1 READ Output Timing Definitions

Read timing on the DQ outputs shown in this section is applied when the DLL is locked.

Rising data strobe edge parameters:

- tQSH describes the DQS_t, DQS_c differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS_t, DQS_c differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins

tDVWp both rising/falling edges, describes the minimum valid data window width independently for each DQ bit
tDQSQ; both rising/falling edges of DQS, no tAC defined.

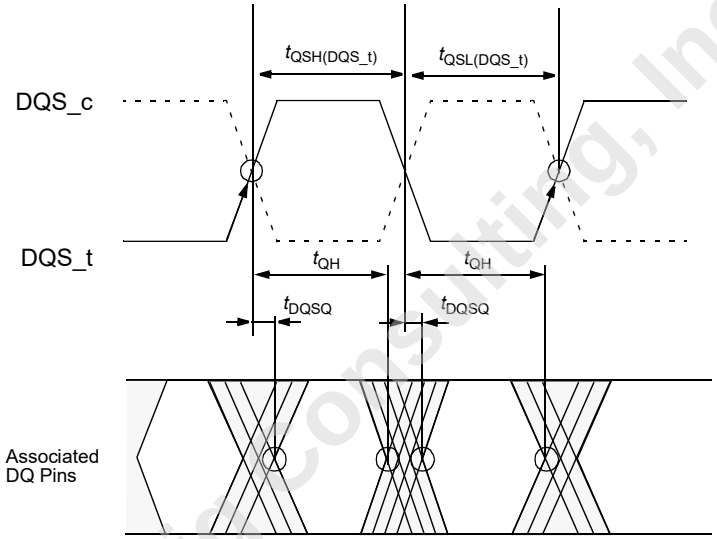

Figure 57 — READ Output Timing Definition

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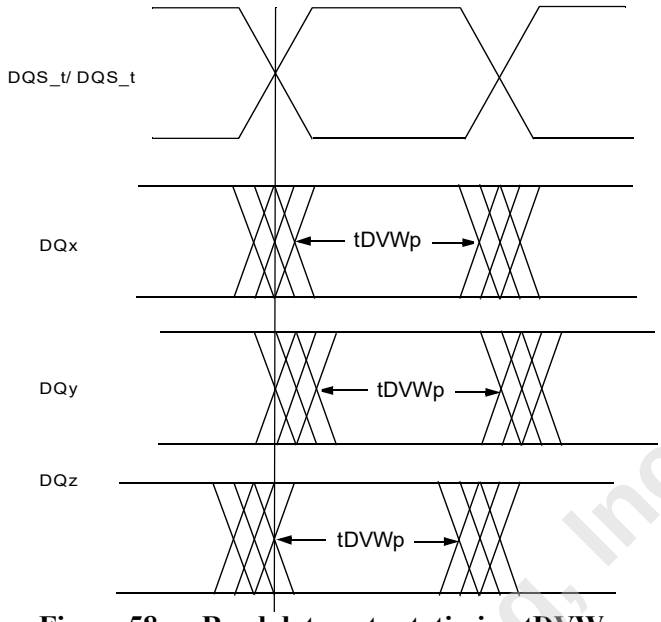

Figure 58 — Read data output timing tDVWp

Table 145 — READ Output Timings

Parameter	Symbol	DDR4-1600 to 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing													
DQS_t, DQS_c to DQ Skew total, per group, per access	tDQSQ	-	0.12	-	0.14	-	0.16	-	0.18	-	0.18	UI	1
DQ output hold time total from DQS_t, DQS_c	tQH	0.85	-	0.82	-	0.80	-	0.77	-	0.76	-	UI	1, 3
Data Valid Window per device: per pin: tQH-tDQSQ each device's output	tDVWp	0.89	-	0.84	-	0.80	-	0.75	-	0.75	-	UI	1,2,3
Data Strobe Timing													
DQS_t - DQS_c differential output low time	tQSL	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	tCK	4, 6
DQS_t - DQS_c differential output high time	tQSH	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	tCK	5, 6

Unit UI = tCK(avg).min/2

NOTE 1: DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.

NOTE 2: Per bit valid data window. Measurement method tbd.

NOTE 3: When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the DDR4DB02 input clock). Example tbd.

NOTE 4: When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the DDR4DB02 input clock). Example tbd.

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NOTE 4: tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 5: tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 6: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

10.5.2 WRITE Output Timing Definitions

Write timing on the MDQ outputs shown in this section is applied when the DLL is locked.

Rising data strobe edge parameters:

- tMQSH describes the MDQS_t, MDQS_c differential output high time.

Falling data strobe edge parameters:

- tMQSL describes the MDQS_t, MDQS_c differential output low time.

tDVA and tDVB; both rising/falling edges of MDQS, no tAC defined.

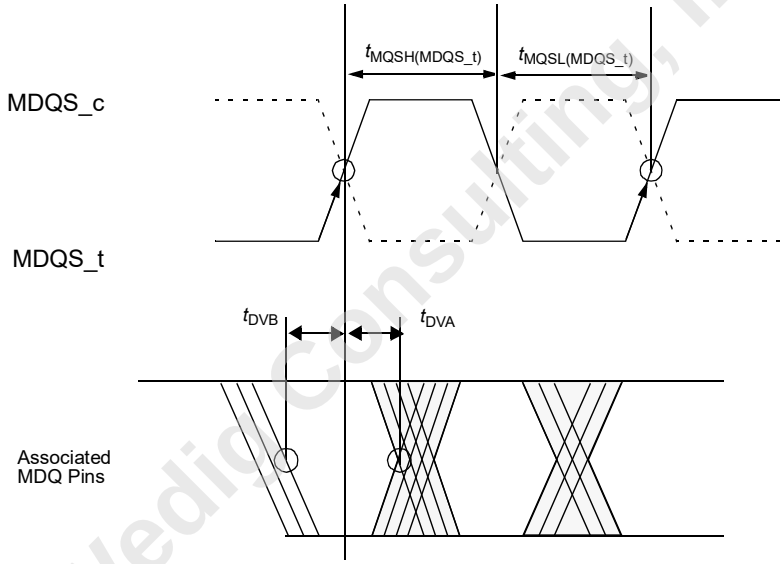

Figure 59 — WRITE Output Timing Definition

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Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

10.6 Package Rank to Package Rank Timing Requirements

Table 147 — DDR4DB02 Operating Spec for Different Package Ranks

Symbol	Parameter	DDR4-1600 to 2400		DDR4-2666/2933		DDR4 -3200		Units	Notes
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
TRDRD	Read to Read Command Spacing	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 4, 8
TWRWR	Write to Write Command Spacing	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 5, 8
TRDWR	Read to Write Command Spacing	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7+ (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tCK(avg)	1, 2, 3, 6, 8
TWRRD	Write to Read Command Spacing	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7- (CL - CWL)	-	tCK(avg)	1, 2, 7, 8

Notes:
1. DDR4DB02 will guarantee the functionality with this minimum command spacing.
2. For operation to same package rank, this restriction does not apply. Host controller follows DRAM JESD79-4 Specification. DDR4DB02 will guarantee the functionality in accordance with DRAM JESD79-4 Specification.
3. This is meant for DDR4DB02 testing on ATE environment purpose to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.

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4. This parameter value includes timing skew between package ranks. The package rank skew between package ranks x and y is ***MRE(Rx) - MRE(Ry)***. For the equations of MRE(R) see section "Command Sequence Descriptions"
5. This parameter value includes timing skew between package ranks. The package rank skew between package ranks x and y is ***DWL(Rx) - DWL(Ry)***. For the equations of DWL(R) see section "Command Sequence Descriptions"
6. This parameter value includes timing skew between package ranks. The package rank skew between package ranks x and y is ***MRE(Rx) - DWL(Ry)***. For the equations of MRE(R) and DWL(R) see section "Command Sequence Descriptions"
7. This parameter value includes timing skew between package ranks. The package rank skew between package ranks x and y is ***DWL(Rx) - MRE(Ry)***. For the equations of MRE(R) and DWL(R) see section "Command Sequence Descriptions"
8. A package rank on a module consists of all DRAM packages that together span the whole data width of the module. A set of 9 (for x8 modules) or 18 (for x4 modules) 3D stacked packages comprises a single package rank while a set of 9 (for x8 modules) or 18 (for x4 modules) dual-die packages constitutes two package ranks.

10.7 Package Rank to Package Rank Timing Requirements in One Rank Timing Mode

Table 148 — DDR4DB02 Operating Spec for Different Package Ranks in One Rank Timing Mode

Symbol	Parameter	DDR4-1600 to 2667		DDR4-2933		DDR4-3200		Units	Notes
		Min	Max	Min	Max	Min	Max		
TRDRD	Read to Read Command Spacing	tRPRE + BL/2 + 0.8	-	tRPRE + BL/2 + 0.8	-	tRPRE + BL/2 + 0.8	-	tCK(avg)	1, 2, 5
TWRWR	Write to Write Command Spacing	tWPRE + BL/2 + 0.8	-	tWPRE + BL/2 + 0.8	-	tWPRE + BL/2 + tbd0.8	-	tCK(avg)	1, 2, 5
TRDWR	Read to Write Command Spacing	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 1.3 + (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 1.3 + (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 1.3 + (CL - CWL)	-	tCK(avg)	1, 2, 3, 4, 5
TWRRD	Write to Read Command Spacing	tRPRE/2 + BL/2 + 1.3 - (CL - CWL)	-	tRPRE/2 + BL/2 + 1.3 - (CL - CWL)	-	tRPRE/2 + BL/2 + 1.3 - (CL - CWL)	-	tCK(avg)	1, 2, 4,5

Notes:
1. DDR4DB02 will guarantee the functionality with this minimum command spacing.
2. For operation to same package rank, this restriction does not apply. Host controller follows DRAM JESD79-4 Specification. DDR4DB02 will guarantee the functionality in accordance with DRAM JESD79-4 Specification.
3. This is meant for DDR4DB02 testing on ATE environment purpose to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.
4. This parameter value includes timing skew between MRE and DWL .
5. A package rank on a module consists of all DRAM packages that together span the whole data width of the module. A set of 9 (for x8 modules) or 18 (for x4 modules) 3D stacked packages comprises a single package rank while a set of 9 (for x8 modules) or 18 (for x4 modules) dual-die packages constitutes two package ranks.

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10.8 MREP and HWL Strobe Sampling Output Delay Parameters

Table 149 — MREP/HWL Strobe Sampling Output Timing

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133/ 2400/2666		DDR4-2666		DDR4-3200		
			Min	Max	Min	Max	Min	Max	Unit
t_{WLO}	[M]DQS (strobe) signal sampling output delay in MREP and HWL training modes.		0	9.5	0	9.5	0	9.5	ns

10.9 MRD Data Comparator Output Delay Parameters

Table 150 — MRD Data Comparator Output Timing

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400		DDR4- 2666		DDR4-2933/ 3200		
			Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{CMP_MRD}	DRAM Read data comparator output delay in MRD training mode.[1]		0	4	0	4	0	8	0	8	t_{CK}
t_{CMP_HIW}	Host Write data comparator status delay in HIW training mode.[2]		0	4	0	4	0	8	0	8	t_{CK}

1. Measured from when the last bits of the 64-bit Read data transfer reach the DDR4DB02 MDQ pins to the last DQ output toggling for a valid comparison result value.
2. Measured from when the last bits of the 64-bit Write data transfer reach the DDR4DB02 DQ pins to the comparison status bits being valid and available for Read commands following a BCW Read command.

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11 Test circuits and switching waveforms

11.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 625 MHz ≤ PRR (Pulse Repetition Rate) ≤ 1620 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

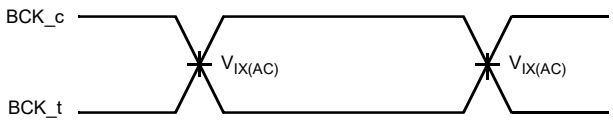
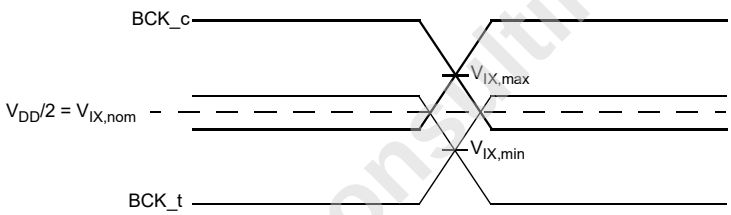


Figure 60 — Voltage waveforms; input clock



For V_{IX} Range testing common mode voltage of BCK_t and BCK_c is shifted around $V_{DD}/2$.
Functional Tests are performed with this V_{IX} shift.

Figure 61 — Input Waveforms V_{IX} range measurement

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11.2 ALERT_n output load circuit and voltage measurement information

All input pulses are supplied by generators having the following characteristics: 625 MHz ≤ PRR ≤ 1620 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

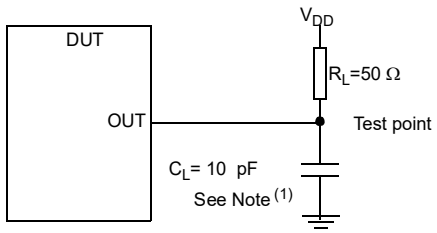

Figure 62 — Load circuit, ALERT_n Outputs

(1) C_L includes probe and jig capacitance.

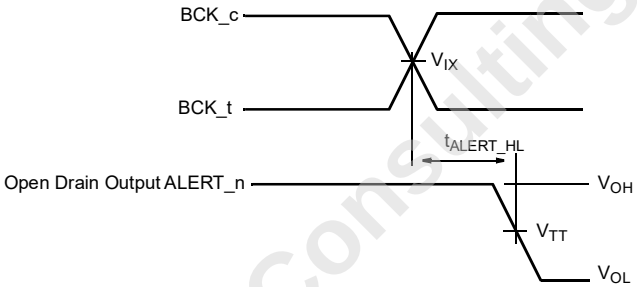

Figure 63 — Voltage waveforms, t_{ALERT_HL} Measurement

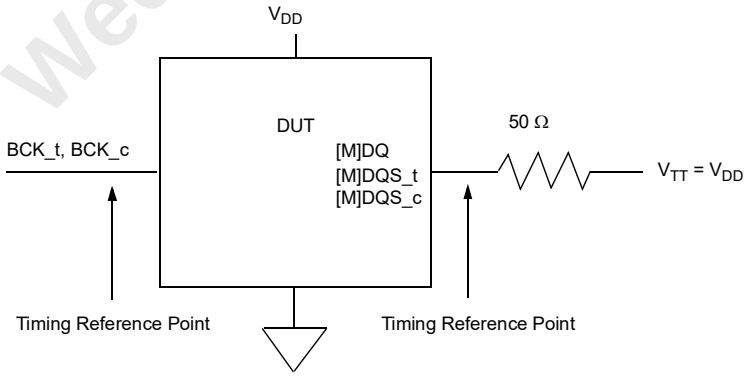

Figure 64 — Reference Load for Output Timing and Output Slew Rate

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12 LDQ/LDQS Input Receiver Specifications

Table 151 — LDQ/LDQS Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600/1866/2133/2400/2666/2933/3200[1]

Speed		DDR4-1600-3200		Unit	Note
Symbol	Parameter	Min	Max		
Data Voltage and Timing					
VldIVW_TOTAL	LDQ Rx Mask p-p voltage total	-	130	mV	2,3,4,5,6
TldIVW_TOTAL	LDQ Rx timing window total	-	0.2	UI	2,5,6
VIHL_AC_ld	LDQ AC input pulse amplitude pk-pk	160	-	mV	7
TldIPW	LDQ input pulse width	0.5	-	UI	8
tLDQS2LDQ	LDQS to LDQ offset	-0.1	0.1	UI	9
tLDQLDQ	LDQ to LDQ offset	-	0.04	UI	10
SRIN_ldIVW	Input Slew Rate over VldIVW_TOTAL	1	9	V/ns	11

* UI=tck(avg)min/(2*N) where N is divider ratio set in F1BC1x[4:3].

NOTE 1: Applies to all operating frequencies and any divider ratio set in F1BC1x[4:3].
NOTE 2: Data Rx mask voltage and timing total input valid window where VldIVW is centered around Vcent_LDQ(midpoint). The data Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER ≤1e-16.
NOTE 3: Rx mask voltage AC swing peak-peak requirement over TldIVW_TOTAL with at least half of VldIVW_TOTAL(max) above Vcent_LDQ(midpoint) and at least half of VldIVW_TOTAL(max) below Vcent_LDQ(midpoint).
NOTE 4: The VldIVW voltage levels are centered around Vcent_LDQ(midpoint).
NOTE 5: Defined over the LDQ internal Vref range 1.
NOTE 6: Overshoot and Undershoot Specifications see Table 101 and Figure 37.
NOTE 7: LDQ input pulse signal swing into the receiver must meet or exceed VIHL_AC_ld for at least one point over the total UI for any UI during which there is a signal transition. No timing requirement above level. VIHL AC_ld is the peak to peak voltage centered around Vcent_LDQ(midpoint), which is defined in Figure 17.
NOTE 8:: LDQ minimum input pulse width defined at the Vcent_LDQ(midpoint).
NOTE 9: LDQS to LDQ[1:0] offset is within LDQ[1:0] at DDR4DB02 balls. Includes all DDR4DB02 process, voltage and temperature variations.
NOTE 10: LDQ to LDQ offset is defined as the magnitude of the difference between the min and max LDQS to LDQ1 and LDQ0 offset at DDR4DB02 balls. Includes all DDR4DB02 voltage and temperature variations.
NOTE 11: Input slew rate over VldIVW Mask centered at Vcent_DQ(midpoint). This single-ended slew rate also applies to LDQS.

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12.1 LDQ/LDQS Output Driver DC Electrical Characteristics

The values in Table 104 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 W +/- 1%.

Table 152 — LDQ/LDQS Output Driver DC Electrical Characteristics

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Note
34 Ω	RON_{34Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
	RON_{34Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
40 Ω	RON_{40Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/6$	1, 2
	RON_{40Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/6$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
48 Ω	RON_{48Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2
	RON_{48Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 1.1 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OMdc} = 0.8 \times V_{DD}$	-10		10	%	1, 2, 4
Mismatch LDQ1-LDQ0 variation pull-up, MM_{Pudd}		$V_{OMdc} = 0.8 \times V_{DD}$	0		10	%	1, 2, 3
Mismatch LDQ1-LDQ0 variation pull-dn, MM_{Pddd}		$V_{OMdc} = 0.8 \times V_{DD}$	0		10	%	1, 2, 3

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DD} and 1.1 * V_{DD}.
3. LDQ1 to LDQ0 mismatch variation for a given component including LDQS (characterized).
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
Measure RON_{Pu} and RON_{Pd}, both at 0.8 * V_{DD} separately; Ron-nom is the nominal Ron value:
RON variance range ratio to RON nominal value in a given component, including LDQS.

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x 100$$

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$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

12.2 LDQ/LDQS Input and Output Timing Requirements

Table 153 — LDQ/LDQS Input and Output timing requirements

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{PDM_RD_LDQ}$	MDQS to LDQS Propagation Delay during Save operation[1,2,3,5]	1.2 V Operation	TBD	TBD	t_{CK}
$t_{PDM_WR_LDQ}$	LDQS to MDQS Propagation Delay during Restore operation[1,2,3,5]	1.2 V Operation[1,2,3]	TBD	-	t_{CK}
t_{LDQSHP}	Post-amble LDQS high to pre-amble LDQ low, Save and Restore operations[4,5]	1.2 V Operation	3 x N	-	t_{CK}

1.Guaranteed after the correct speed range has been programmed in BC0A
2.These timings are only valid with the DA[5:0] bits of the lower and upper nibble read delay and write delay control words F[3:0]BC4x, F[3:0]BC5x, F[3:0]BC8x, and F[3:0]BC9x at their power on default of '00_0000'
3.Over all possible divider ratios allowed in F1BC1x[4:3]
4.Only valid for LDQS mode with pre-amble/post-amble enabled, F1BC1x[1] = 0.
5.N is divider ratio set in F1BC1x[4:3].

12.3 Save and Restore Timing

Save timing when LDQ port is configured in Save mode, BC0D[1:0] = 10, with pre-amble enabled, F1BC1x[1] = 0, is shown in Figure 65

Restore timing when LDQ port is configured in Restore mode, BC0D[1:0] = 01, with pre-amble enabled, F1xBC1x[1] = 0, is shown in Figure 66

Save timing when LDQ port is configured in Save mode, BC0D[1:0] = 10, with pre-amble disabled, F1BC1x[1] = 1, is shown in Figure 67

Restore timing when LDQ port is configured in Restore mode, BC0D[1:0] = 01, with pre-amble disabled, F1xBC1x[1] = 1, is shown in Figure 68.

Requirements for DDR4DB02 and NVC enabling, disabling and termination of LDQS/LDQ[1:0] are shown in Figure 69 for Save mode entry and exit.

Requirements for DDR4DB02 and NVC enabling, disabling and termination of LDQS/LDQ[1:0] are shown in Figure 70 for Restore mode entry and exit.

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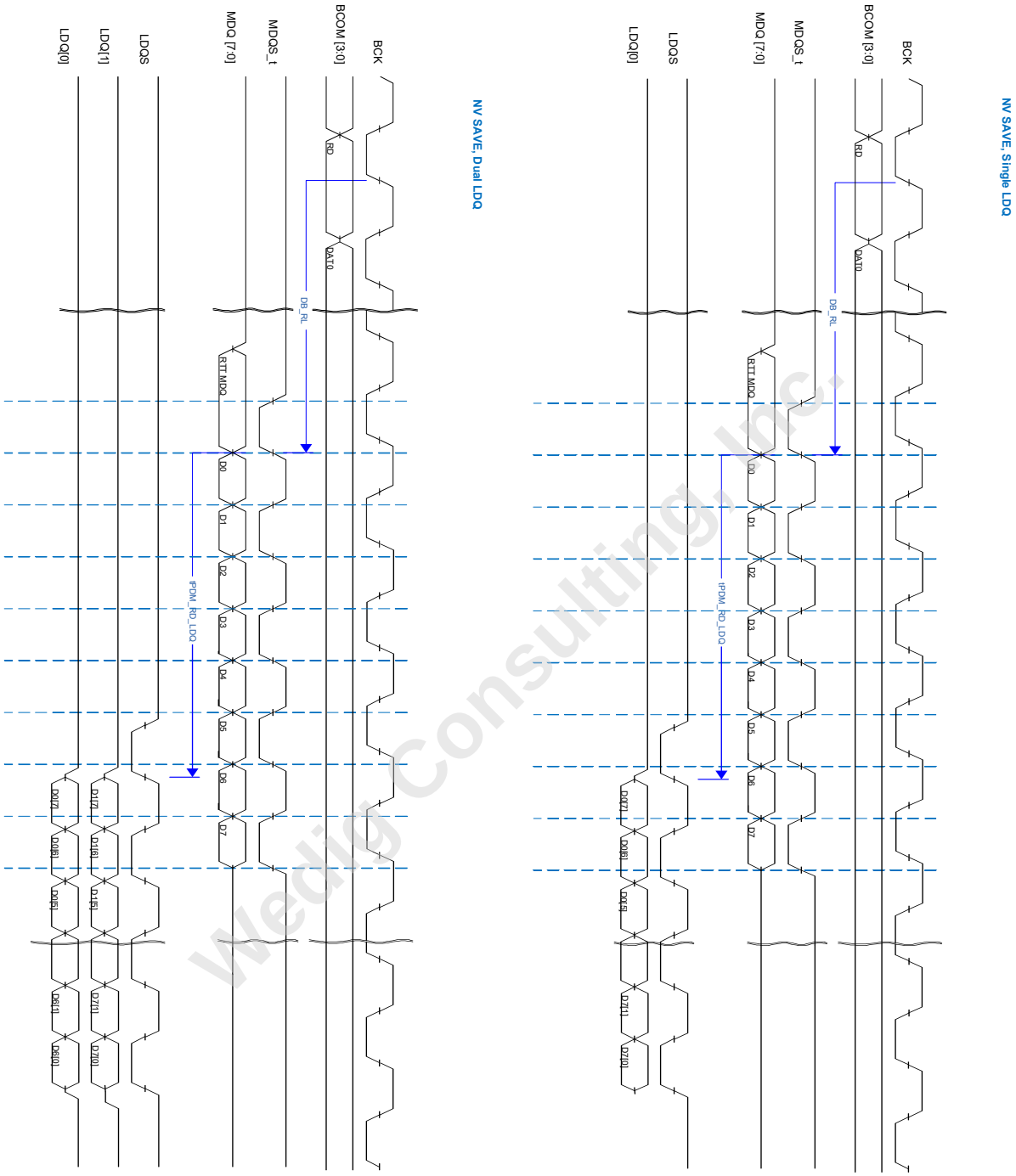

Figure 65 — Save Timing for Single and Dual LDQ pins with pre-amble/post-amble[1,2]

1. LDQS frequency is shown at 1x of BCK for clarity. Actual LDQS frequency will be divided from BCK as specified in F1BC1x[4:3].
2. Bit order for LDQ[1:0] is vendor specific.

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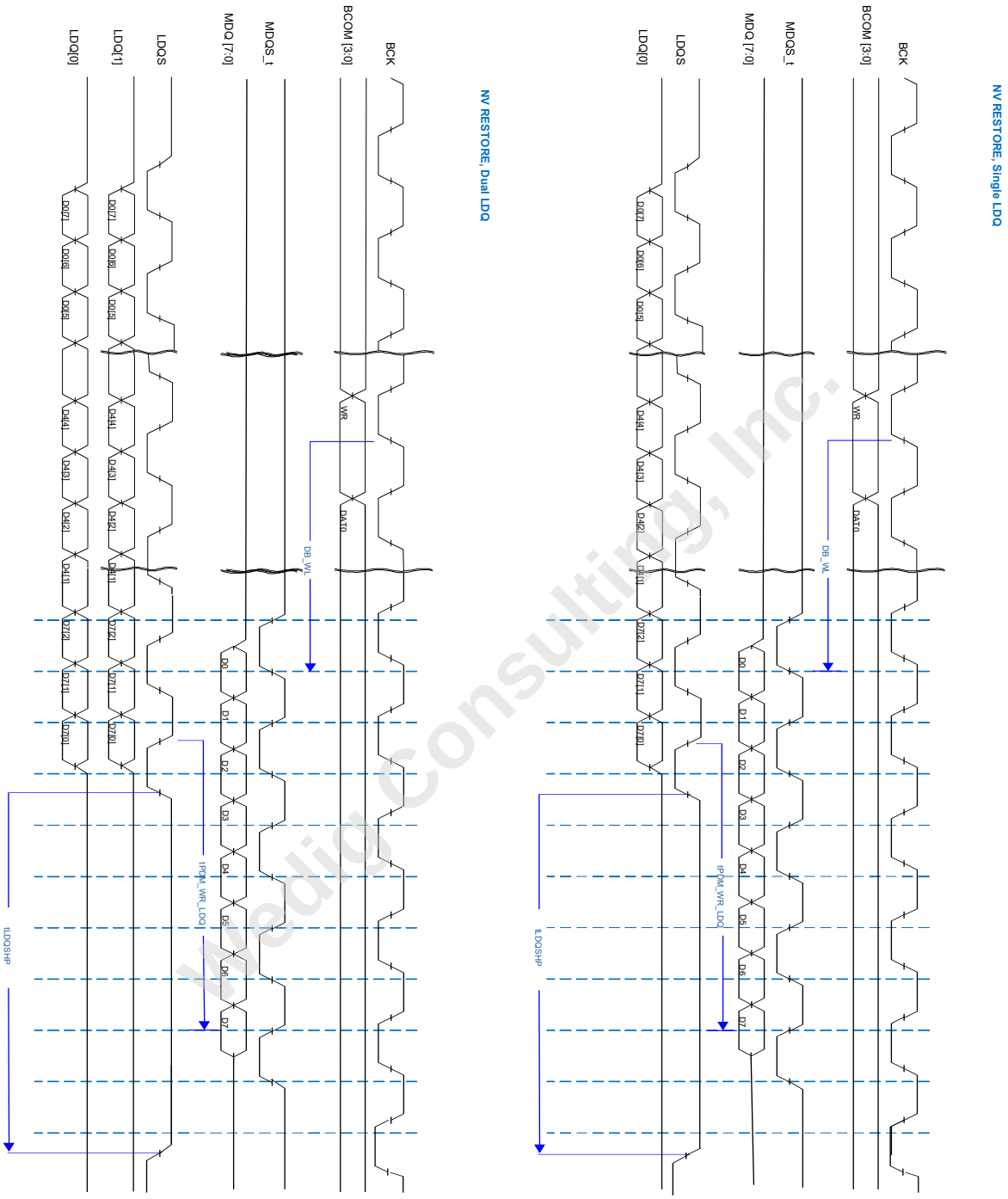

Figure 66 — Restore Timing for Single and Dual LDQ pins with pre-amble/post-amble[1,2]

1. LDQS frequency is shown at 1x of BCK for clarity. Actual LDQS frequency will be divided from BCK as specified in F1BC1x[4:3].
2. Bit order for LDQ[1:0] is vendor specific.

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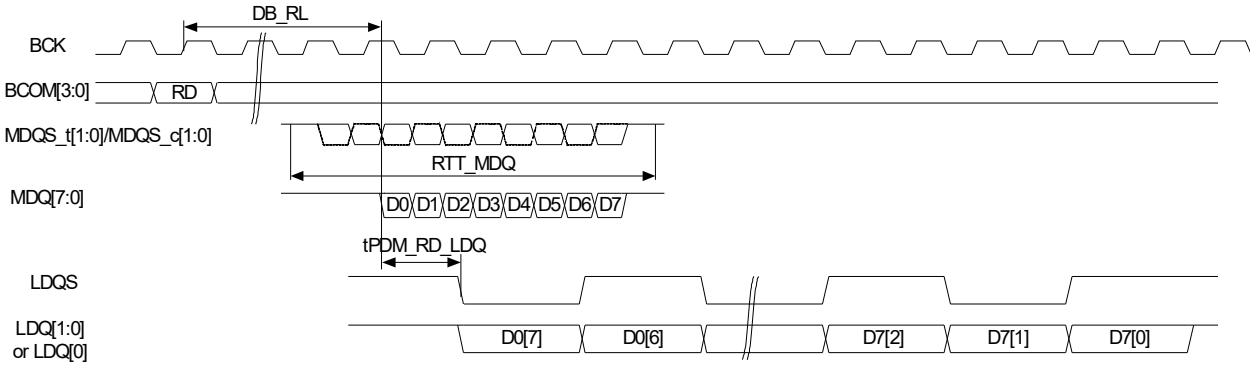

Figure 67 — Save Timing for Single and Dual LDQ pins without pre-amble/post-amble[1,2]

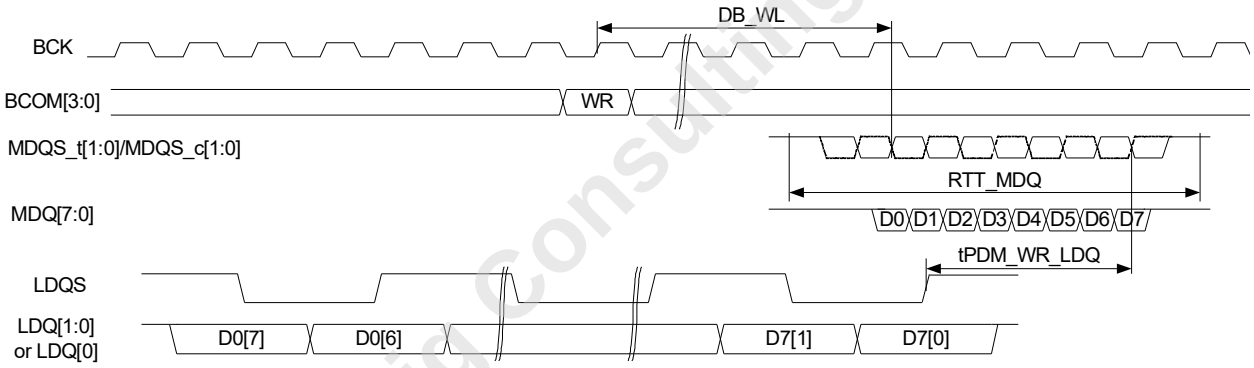

Figure 68 — Restore Timing for Single and Dual LDQ pins without pre-amble/post-amble[1,2]

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1. LDQS frequency is shown at 1/4x of BCK for clarity. Actual LDQS frequency will be divided from BCK as specified in F1BC1x[4:3].
2. Bit order for LDQ[1:0] is vendor specific.

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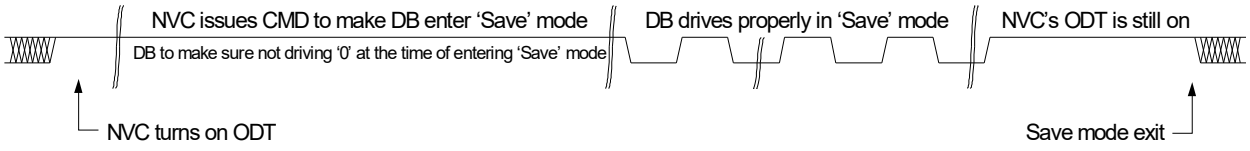

Figure 69 — LDQS/LDQ[1:0] signal assertion and termination during Save mode entry and exit

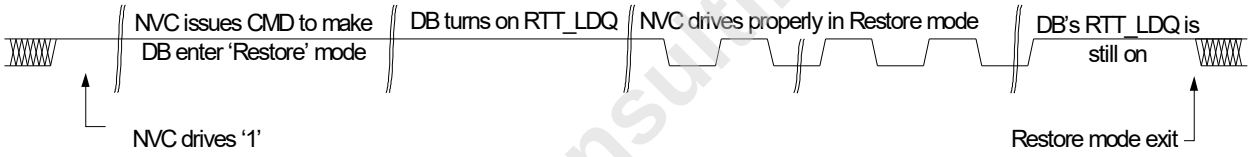

Figure 70 — LDQS/LDQ[1:0] signal assertion and termination during Restore mode entry and exit

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13 References to other applicable documents

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD21-C, *Configuration for Solid State Memories.*

JESD8-11A, *Definition of wide range non-terminated logic*

JESD79-4, *DDR4 SDRAM Specification*

DDR4RCD02 Specification

MO-276F, *Package Mechanical Outline*

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☐ Test method number _____ Clause number _____

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