UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2023-00847
Patent 10,268,608

DECLARATION OF DR. ROBERT WEDIG REGARDING U.S. PATENT NO. 10,268,608

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 10,268,608 ("the '608 Patent") (EX1001) and on the patentability of claims 1-12 of this patent.

B. Background and Qualifications

2. I received a Bachelor of Electrical Engineering degree from the University of Dayton in 1977. I received a Master of Science degree in Electrical Engineering from the University of Southern California in 1979, and received a Ph.D. in Electrical Engineering from Stanford University in 1982.

3. From 1977 through 1979, I worked as a processor design engineer at Hughes Aircraft Company in Fullerton, California. In this capacity, I designed computer systems which interface with memory integrated circuits. As one example, I was responsible for the design of an Input/Output processor which directly interfaced to a memory controller for a military mainframe computer system. From 1979 through June 1982, I was a Research Assistant, Instructor, and Teaching Assistant in the Computer Systems Laboratory at Stanford University. From 1982 through December 1985, I was an Assistant Professor of Electrical and Computer Engineering at Carnegie-Mellon University. My research, both as a PhD

student and as an assistant professor, involved the research and design of concurrent computer systems which interface with memory integrated circuits. As a professor, I taught courses in computer design which included memory design issues involving DRAM and SDRAM. Since January 1986, I have worked as an independent consultant, doing business as Wedig Consulting, Inc. As a consultant, I have designed digital circuits, analyzed computer systems and designed software for computer based electronic systems. I have also analyzed high-speed backplane design issues including crosstalk, signal reflection and signal trace timing and impedance.

C. Compensation and Prior Testimony

4. I am being compensated at a rate of $700.00 per hour for work on this matter. I am also being reimbursed for reasonable and customary expenses associated with my work on this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

5. Previously, I have testified either by deposition or at trial in a number of litigation matters. My curriculum vitae, including a list of all of my publications, and cases in which I have previously testified as an expert is attached as Exhibit 1004.

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D. Information Considered

6. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in Attachment B.

7. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

8. My analysis of the materials produced in this matter is ongoing and I will continue to review any new material as it is provided.

II. LEGAL STANDARDS FOR PATENTABILITY

9. In expressing my opinions and considering the subject matter of the claims of the ’608 Patent, I am relying upon certain basic legal principles that have been explained to me.

10. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

11. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and

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generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, etc.).

12. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the '608 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

13. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims, after being construed in this manner, are then to be compared to the information in the prior art.

14. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

15. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. My understanding of the two legal standards is set forth below.

A. Anticipation

16. I understand that the following standards govern the determination of whether a patent claim is "anticipated" by the prior art.

17. I understand that the "prior art" includes patents and printed publications that existed before the earliest filing date (the "effective filing date") of the claim in the patent. I also understand that a patent will be considered prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be considered prior art if it was publicly available before that date.

18. I understand that, for a patent claim to be "anticipated" by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are "inherent" to the thing or process being described in the prior art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

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19. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

20. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

21. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

22. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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23. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the '608 Patent would have been considered obvious as of the priority date of the patent.

24. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

25. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

26. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; satisfying a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected

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results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed inventions are not obvious, and reserve my right to address any such evidence if it is identified in the future.

27. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

28. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one

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device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

29. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

30. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

31. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements

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of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

32. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

33. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or

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more prior art references discourage or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

34. I understand that a person of ordinary skill is also a person of ordinary creativity.

35. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance, the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

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leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE '608 PATENT

A. Effective Filing Date

36. The application that resulted in the '608 Patent (EX1001) is U.S. Patent Application Serial No. 15/820,076 (EX1002), filed November 21, 2017. The '608 Patent claims priority to U.S. Provisional Application No. 61/676,883 (EX1025), filed July 27, 2012. All of the prior art that I rely upon below predates July 27, 2012, and thus, for now, I assume that the claims of the '608 Patent have an effective filing date of **July 27, 2012**, regardless of whether there is actually support in the provisional application for all of the claim limitations.

B. Person of Ordinary Skill in the Art

37. Based upon my experience in the field and the information discussed below, I believe a person of ordinary skill in the art ("Skilled Artisan" or "POSITA") in the field of the '608 Patent in July 2012 would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field. Such a person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with

various standards, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers.

C. Overview of the '608 Patent

38. The '608 Patent discloses a memory module with a module control circuit, memory devices, and data buffers. EX1001 at Abstract. As illustrated in annotated Figure 2C below, the memory module (110) includes memory devices (112, green) organized in groups, each group with an associated data buffer (isolation device 118, blue) and one module control device (116, red) located in the center of the module. *Id.*, 3:25-27, Fig. 2C (reproduced below with annotations). The groups of memory devices (green) and associated data buffers (blue) are distributed length-wise across the memory module. *Id.*, 3:51-54, Fig. 2C (reproduced below with annotations).

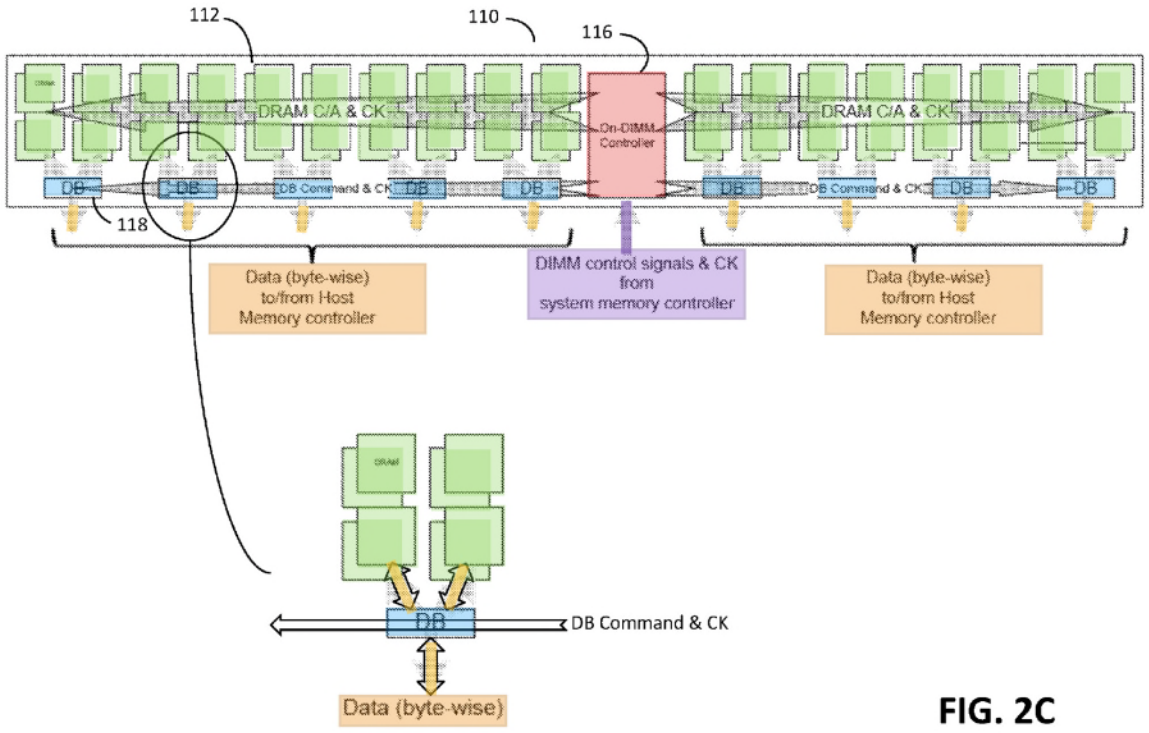

FIG. 2C

39. As shown in annotated Figure 1 below, the memory module (110) is connected to a memory controller (MCH) (101). *Id.*, 3:29-34, 4:20-23, FIG. 1 (reproduced below with annotations).

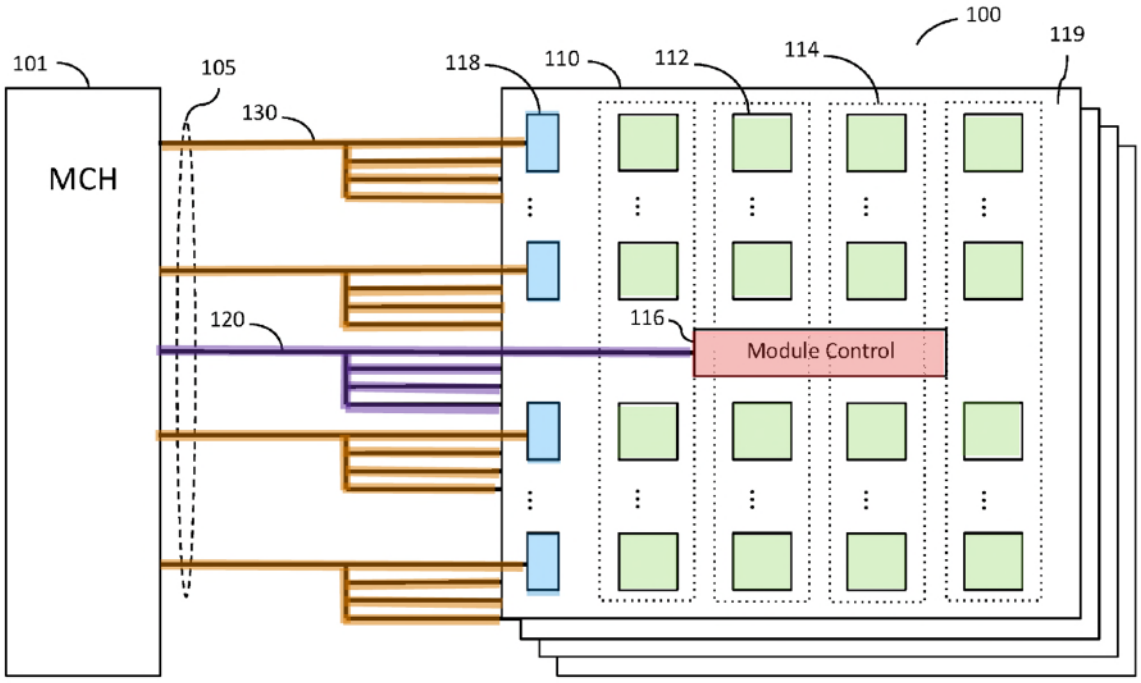

FIG. 1

40. As shown in annotated Figures 1 and 2C above, a memory bus (105) connects the memory controller (MCH) (101) and the memory module (110) with control/address (C/A) signal lines (120, purple) between the memory controller (101) and the module control device (116, red), and data/strobe signal lines (130, orange) between the memory controller and each memory device (112, green) via each data buffer (118, blue). *Id.*, 4:20-32. The memory controller (MCH) (101) issues C/A signals (on lines 120, purple) to the memory module (110) via the module control device (116, red), and sends and receives data/strobe signals (on lines 130, orange) to/from the memory devices (112, green) via the data buffers (118, blue). *Id.*

41. In an exemplary embodiment, the module control device (red) receives the system memory commands represented by a set of system C/A signals from the memory controller (MCH) and generates module command signals and module control signals based on memory commands from the system. *Id.*, 4:65-5:7. The module control device (red) transmits the module command signals to the memory devices (green) via signal lines and the module control signals to the data buffers (blue) via other signal lines. *Id.*, 5:57-66; *see also* FIGS. 2A and 2B (showing connections between the module controller 116, the memory devices 112, and data buffers 118). I note that the '608 patent also refers to the "module controller" as "module control device" or "module control circuit." EX1001, 4:27-30.

42. As shown in annotated Figure 1 above, each group of memory devices can include, for example, four memory devices (green), *id.*, 6:12-16, each consisting of a dynamic random access memory (DRAM), *id.*, 4:60-64. All four of the memory devices (green) can connect in parallel to the memory controller data/strobe signal lines (orange) through their associated data buffer (blue), which isolate the memory devices (green) from the memory controller (MCH). *Id.*, 3:27-29, 6:17-29.

43. The '608 Patent notes that, because the data buffers (blue) and their associated memory devices (green) are distributed across the memory module in

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various positions, "a same set of module control signals may reach different [data buffers (blue)] at different times across more than one clock cycle of the system clock." *Id.*, 9:52-10:6. Each data buffer (blue) thus may include signal alignment circuits that determine time intervals to use to adjust for the signals received at different times. *Id.*, 10:7-21.

44. As shown in Figures 12A below, the data buffer determines a time interval based upon the reception of signals to the data buffer during a write operation. *Id.*, 15:27-50. In particular, the module control circuit receives ***a write command*** (W/C) at time t1, and outputs a corresponding module control signal (MCS) at time t2. *Id*., 15:27-32. The module control signal (MCS) is received by one data buffer at time t3 and by another data buffer, farther away from the module control circuit, at time t3' which "can be in a different cycle of the system clock MCK from the cycle which t3 is in." *Id*., 15:33-38. Both of those data buffers receive the corresponding data strobe signal (DQS1) of the write data at time t4, in accordance with a known write latency (W.L.) after the write command at t1 (W/C). *Id*., 15:38-42. Thus, each data buffer can measure the difference (EWD) between time t3, the reception of the module control signal (MCS), and time t4, the reception of the corresponding data strobe (DQS1). *Id*., 15:42-45. The time interval EWD and the known write latency (W.L.) can then be used to adjust signal

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timing during memory read operations so that the signals are released or processed at the proper times. *Id.*, 15:45-50.

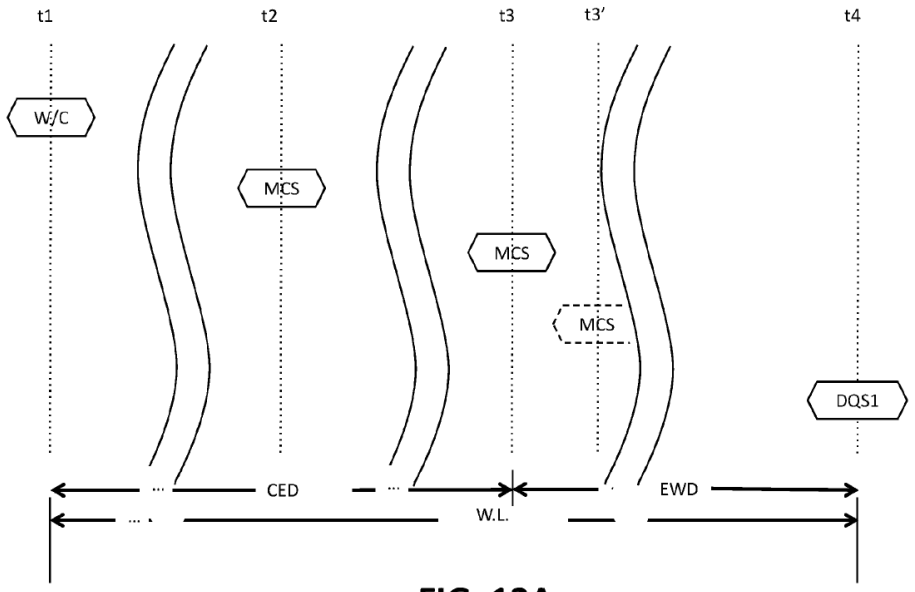

FIG. 12A

In particular, "[w]ith knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can ***add a proper amount of delay to the read data*** signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101…." *Id.*, 15:66-16:6, FIG. 12B (red annotations added).

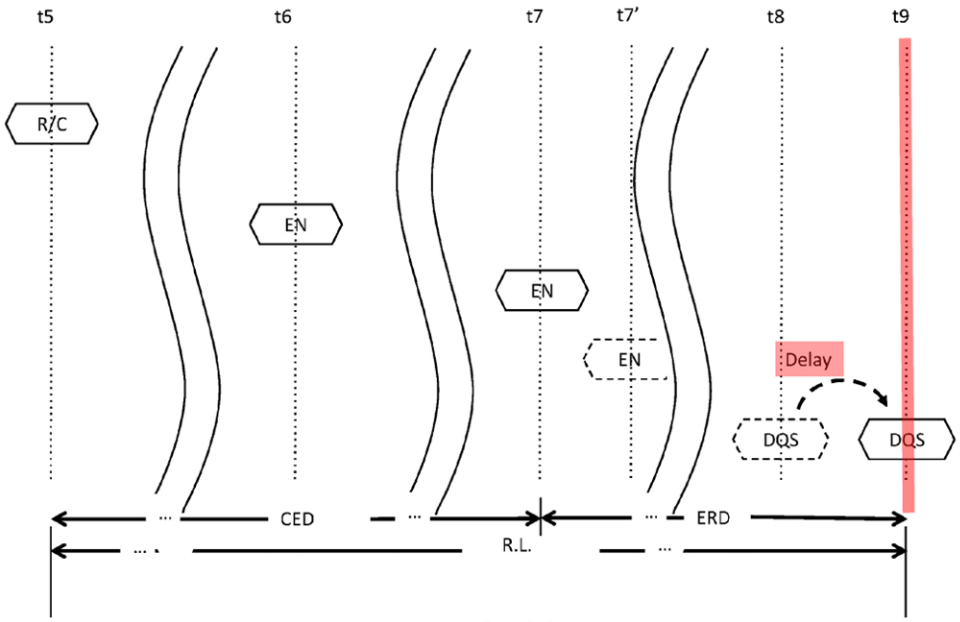

FIG. 12B

D. The Prosecution History

1. The 599 Application (The '632 Patent)

45. U.S. Patent No. 9,128,632 ("the '632 Patent") is related to the '608 Patent. Both the '632 Patent and the '608 Patent claim priority to the filing date of the same provisional application, EX1025, which was filed on July 27, 2012. The '632 Patent issued from Application No. 13/952,599 ("the 599 Application"). EX1010 ('632 File History). The 599 Application presented 20 claims, claims 1-20. *Id.*, 36-39.

46. The Examiner rejected all the claims of the 599 Application as anticipated by the Manohararajah '033 patent, EX1026. *Id.*, 99-108. In response,

the applicant substantially amended the claims, including the final clause of claim 1 to read:

> wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

EX1010 ('632 File History), 134-135. Among other things, the applicant argued that "[n]owhere in Manohararajah it is described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals received by the each respective buffer. Thus, Manohararajah does not anticipate claim 1 as amended." *Id.*, 140-141.

47. In response, the Examiner accepted the applicant's amendments and arguments and issued a Notice of Allowance, stating:

> the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the

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> memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims.

Id., 1078.

2. The 993 Application (The '587 Patent)

48. U.S. Patent No. 9,563,587 ("the '587 Patent") is related to the '608 Patent. Both the '587 Patent and the '608 Patent claim priority to the filing date of the same provisional application, which was filed on July 27, 2012. The '587 Patent issued from Application No. 14/846,993 ("the '993 Application"). EX1011 ('587 File History). The '993 Application presented 20 claims, claims 1-20. *Id.*, 37-41.

49. The Examiner issued a Notice of Allowance, stating:

> the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an

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> operation to configure the timing of transmission of signals to the memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims.

Id., 113.

3. IPR2017-00730 by SK hynix against the ’632 Patent (institution denied)

50. On January 20, 2017, SK hynix filed a petition for *inter partes review* of the ’632 Patent. *See generally* EX1012 (IPR2017-00730, i.e., 632 IPR Petition); EX1013 (Netlist’s Patent Owner Preliminary Response).

51. Claim 1 of the ’632 Patent contains the following limitation, which is not expressly found in the claims of the ’608 Patent:

> wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation

EX1014 at 10.

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52. Based on the claim limitation above, the Board denied institution in IPR2017-00730 on July 21, 2017, stating that "Petitioner argues that [the re-timing in the cited prior art] is related to the time interval determined during the read leveling operation by read leveling circuit 323, but that operation determines a 'time A' that is used to adjust timing of 'the input buffer circuit INB and the like.' [The cited prior art] does not teach time A being used to adjust timing of data output by data buffer circuit 300 to the system controller (i.e., to 'time transmission of a respective set of read data signals,') as recited in the claim [of the '632 Patent]." EX1014 ('632 Decision) at 12-13 (citation omitted).

53. Neither the Board's decision in IPR2017-00730, nor the prior art raised in that IPR, was provided to the examiner of the '608 Patent, despite the fact that IPR2017-00730 concluded in 2017 before the application for the '608 Patent was filed in 2019. *See generally* EX1002 ('608 prosecution history).

4. The 064 Application (The '035 Patent)

54. U.S. Patent No. 9,824,035 ("the '035 Patent"), EX1031, is related to the '608 Patent. Both the '035 Patent and the '608 Patent claim priority to the filing date of the same provisional application, which was filed on July 27, 2012. The '035 Patent issued from Application No. 15/426,064 ("the 064 Application"). EX1032 ('035 File History). The 064 Application originally presented 20 claims, claims 1-20. *Id.* at 46-49. The Examiner rejected the claims for obvious-type

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double patenting over U.S. Patent No. 9,128,632 ("the '632 Patent"). *Id.* at 89-95. In response, the applicant submitted a terminal disclaimer and substantially amended the claims:

> A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> a module board having edge connections for coupling to respective ~~data/strobe~~ signal lines in the memory bus;
>
> a module control device mounted on the module board and configured to receive memory command signals <u>for a first memory operation</u> from the memory controller via the set of control/address signal lines and to ~~produce~~ <u>output</u> module command signals and module control signals in response to the memory command signals; and
>
> memory devices mounted on the module board <u>and configured</u> to perform <u>the</u>~~a~~ first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices <u>corresponding to respective sets of the plurality of sets of data/strobe signal lines</u> ~~each respective set of memory devices corresponding to a respective set of the data/strobe signal lines~~; and

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> a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit ~~providing data paths~~ of the plurality of buffer circuits is coupled between a respective set of ~~the~~ data/strobe signal lines and a respective set ~~of the plurality of sets~~ of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic ~~that responds~~ configured to respond to the module control signals by enabling ~~a subset of~~ the data paths ~~for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices~~, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on ~~the subset of~~ the data paths in accordance with the timing information.

Id. at 105-11. The applicant also presented two new claims, claims 21-22. *Id*., 110.

55. The Examiner subsequently issued a Notice of Allowance. *Id*., 123-130. The applicant filed an Amendment after Notice of Allowance to amend (i) dependent claims 6 and 8 to "correct antecedent basis issues and a minor error," (ii) dependent claims 10 and 12 to change dependency from dependent claim 9 to

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independent claim 1, and (iii) dependent claims 13 and 20 to "correct minor errors." *Id*., 142-47.

5. The 076 Application (The '608 Patent)

56. U.S. Patent No. 10,268,608 ("the '608 Patent"), EX1001, also claims priority to the filing date of the same provisional application, which was filed on July 27, 2012. The '608 Patent issued from Application No, 15/820,076 ("the 076 Application"). EX1002 (608 File History). The 076 Application originally presented 1 claim. *Id.* at 72. The Examiner rejected the claim for obvious-type double patenting over U.S. Patent No. 9,824,035 and U.S. Patent No. 9,128,632. *Id*., 83-91. In response, the applicant submitted terminal disclaimers and amended claim 1 to include "memory operations ~~a first operation~~" and "at least one ~~a~~ tristate buffer." *Id.* at 102, 116-18. The applicant also presented new dependent claims 2-12. *Id*., 119-20.

57. The Examiner subsequently issued a Notice of Allowance. *Id*., 122-29; *see also id.*, 92, 204-06. The Examiner provided the following reasons for allowance:

> The following is an examiner's statement of reasons for allowance:
>
> Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module

> system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Id., 127-28 (citing *id.*, 46-71 ("Description of the Embodiments")).

58. The applicant filed an Amendment after Notice of Allowance to amend claims 1 and 10 to "correct antecedent basis issues." *Id.*, 266-269, 277.

6. The 151 Application (The '506 Patent)

59. The '506 Patent issued from Application No. 16/391,151 ("the 151 Application"). EX1052 (506 File History). The 151 Application originally presented 1 claim. *Id.* at 45. The Examiner rejected the claim for obvious-type double patenting over the '608 Patent, the '035 Patent, the '587 Patent, and the '632 Patent. *Id.*, 140-151. The Examiner also rejected the original claim 1 as anticipated by U.S. Patent No. 8,565,033 to Manohararaja (EX1026). *Id.*, 151-153.

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In response, the applicant submitted terminal disclaimers, canceled the original claim 1, and introduced twenty new claims. *Id.*, 173-184.

60. The Examiner subsequently issued a Notice of Allowance. *Id.*, 195. In that Notice, the Examiner provided the following reasons for allowance:

> Prior art teaches memory controller systems with memory arranged into memory ranks and memory modules including a buffer provided for buffering signals / data to and from memory chips on the memory modules; and memory systems that implement delays for transmitting signals to and from memory devices of a memory module including delaying strobe signals, however, the prior art does not fairly teach or suggest, individually or in combination, a memory controller system with memory modules having control and address signal lines implemented to be used corresponding to memory read operations to and from memory devices of the memory module that are arranged in multiple ranks with data buffers coupled to the memory devices, where memory read operations output read data and read strobes associated with the memory read operations, and where the data buffer implemented delaying of a first read strobe by e predetermined amount, i.e. generating a delayed read strobe, sampling the first section of read data using the delayed read strobe, and transmitting the section of read data to a data bus, where the predetermined amount of delay is determined based at least on signals received by the data buffer before the memory read operation as claimed. Applicant argues these limitations on Pages 11-13 of Applicant's Remarks filed 4/10/2020. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Id., 201-202 (citing *id.*, 19-44).

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61. During prosecution of the ’506 Patent, the applicant did not disclose to the Examiner U.S. Patent Publication No. 2010/0312956 to Hiraishi (EX1005), U.S. 8,020,022 to Tokuhiro (EX1006), or U.S. Patent Publication No. 2007/0008791 to Butt (EX1029), and I am not aware of any evidence that the Examiner considered these references during prosecution. *See* EX1052.

7. IPR2022-00236 by Micron against the ‘035 Patent (instituted)

62. On December 23, 2021, Micron filed a petition for *inter partes review* of the ’035 Patent, which was instituted on July 19, 2022. EX1040. The instituted grounds assert, among others, obviousness of the ‘035 Patent’s claims over U.S. Pat. Pub. No. 2020/0312925 to Osani (“Osanai”) and Tokuhiro (EX1006). EX1040 at 6-7. Osanai is related to and has a specification similar to Hiraishi (EX1005).

63. The Board found, in instituting Micron’s ‘035 IPR, that petitioner’s arguments were persuasive concerning the existence of a motivation to combine Osani and Tokuhiro, and that the combination rendered obvious the limitation of “wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.” EX1040 at 22-26.

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64. The claims of the '608 Patent are not patentably distinct from those of the '035 Patent. For example, as noted above, during prosecution of the '608 Patent the Examiner rejected the claim for obvious-type double patenting over U.S. Patent No. 9,824,035:

> Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-

EX1002, pp. 83-91. In response, the applicant submitted a terminal disclaimer for the '035 Patent. *Id.* at 102-103.

8. IPR2022-00237 by Micron against the '608 Patent (institution denied)

65. On December 23, 2021, Micron filed a petition for *inter partes review* of the '608 Patent, which was not instituted on July 19, 2022. EX1041. The proposed grounds, unlike the Micron '035 IPR (*supra*, 54-55), included an anticipation ground based on Osanai, where Micron argued Osanai alone disclosed the disputed claim language: "*delay circuit configured to delay a signal through the data path.*" EX1041 at 6-7, 17-19.

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66. The Board found, in denying Micron's '608 IPR, that "we agree with Patent Owner that Petitioner has not identified a data path that includes Osanai's write leveling circuit 322" and that "Petitioner does not … state, or otherwise make a showing, that the write and read leveling circuitry are included in any one of the data paths that are relied upon by Petitioner. Nor does Petitioner show how these circuits would be included in the recited data path." EX1041 at 18-19. Although Micron also raised an obviousness ground based on Osanai and Tokuhiro, that combination did not address the disputed limitation. *Id.* at 20 ("Petitioner's contentions regarding Tokuhiro … do not address or remedy the deficiencies discussed above with respect to Ground 1. … Petitioner does not rely on Tokuhiro … as disclosing that the delay circuit is included in the recited data path, as required by claim 1."). As explained below, Hiraishi in view of Butt renders obvious the limitations of the '608 Patent claims, including the limitation of a "*delay circuit configured to delay a signal through the data path.*"

9. IPR2022-00711 by Samsung against the '506 Patent (instituted)

67. On Mar. 22, 2022, Samsung filed a petition for *inter partes review* of the '506 Patent, which was instituted on October 21, 2022. EX1047. I provided an expert declaration in support of this petition. *Id.* at 7 ("Petitioner also relies on the Declaration of Robert G. Wedig, Ph.D. (Ex. 1003) in support of its arguments."). The instituted grounds assert obviousness of the '035 Patent's claims over Hiraishi

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(EX1005), Butt (EX1029), Tokuhiro (EX1006), Ellsberry (EX1007), and Kim (EX1008), the same references I rely on below:

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–20 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)[2]	Hiraishi, Butt
3, 5, 12, 16	103(a)	Hiraishi, Butt, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Kim
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt, Tokuhiro
3, 5, 12, 16	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Tokuhiro, Kim

EX1047 at 6-7.

68. The Board found, in instituting Samsung's '506 IPR, that petitioner's arguments were persuasive concerning the existence of a motivation to combine Hiraishi and Butt, as well as Hiraishi, Butt, and Tokuhiro, and that the combination rendered obvious the limitations of "delay the first read strobe by a first predetermined amount to generate a first delayed read strobe" and "wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations." EX1047 at 18-23. In so doing, the Board credited my testimony in that proceeding, noting that "[a]lthough Patent Owner argues that the combination would not successfully delay the read strobe signal based on previous operations due to Hiraishi's read

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leveling circuit not being connected to its delay circuit and due to the combination not providing DQ read data to delay circuit 372, at this stage of the proceeding we credit Dr. Wedig's testimony that a person of ordinary skill would have had a reasonable expectation of success in making the combination." *Id.* at 22-23.

69. The claims of the '506 Patent are not patentably distinct from those of the '608 Patent. For example, during prosecution of the '506 Patent the Examiner rejected the claim for obvious-type double patenting over the '608 Patent (in addition to the '035 Patent and '632 Patent):

> Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608, as listed below, and as such anticipate the claims of the copending application:

EX1052, pp. 140-151. In response, the applicant submitted a terminal disclaimer for the '035 Patent. *Id.* at 185-186.

E. Challenged Claims

70. This declaration relates to claims 1-12 of the '608 Patent. Those claims are listed below starting on page 249.

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F. Construction of Terms Used in the Patent Claims

71. I understand that claim terms should be given their ordinary and customary meaning as understood by one of ordinary skill in the art in view of the patent and its file history. As detailed in my analysis and set forth below, I have used what I believe to be the ordinary and customary meaning of the claim terms as understood by one of ordinary skill in the art in view of the '608 Patent and its file history.

72. I also understand that where a patent applicant provides an explicit definition of a claim term in the specification, that definition may control the interpretation of that term in the claim.

73. I also understand that if no explicit definition is given to a term in the patent specification, the claim terms must be evaluated using the ordinary meaning of the words being used in those claims, evaluated from the perspective of a person of ordinary skill in the art.

74. I understand that in litigation between Micron and Netlist involving the parent and grandparent to the '608 Patent, there is a claim construction dispute where Micron asserts that certain terms are subject to § 112, ¶ 6 and indefinite for failure to disclose an adequate structure or algorithm, EX1041 at 9-11, while Netlist asserts that those terms are not subject to § 112,¶ 6 and should be given their plain and ordinary meaning, EX1042 at 4-5. I am not aware of any claim

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construction ruling resolving this claim construction dispute, so for now I am assuming that those claim terms (and the corresponding claim terms in the '608 Patent) are not invalid, and as discussed below, the prior art discloses the examples provided in the '608 Patent, and thus it is not necessary for purposes of my analysis to determine whether any terms of the '608 Patent are governed by § 112,¶ 6.

75. I understand that, in IPR2017-00730, Petitioner proposed constructions for certain terms under the broadest reasonable interpretation; Patent Owner asserted that those terms have the ordinary meaning as understood by a Skilled Artisan; and the Board found that no express construction was necessary for any of those terms. EX1014 (632 Decision) at 8. Below, I address some claim terms in the '608 Patent, including some terms that were also discussed in IPR2017-00730, and I show how the specification uses those terms. As I further discuss below, the prior art discloses these terms in the same sense as used in the '608 Patent. Accordingly, I do not expect that an express construction is necessary for these terms to resolve the validity issues discussed in this declaration.

1. "*memory operation*"

76. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*memory operation*" includes, but is not limited to, "memory operations in response to memory commands (e.g., read, write, refresh,

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precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module." EX1001, 3:29-34. During such operations, the module controller will transmit the command and address signals received from the memory controller to the memory devices. EX1001, 5:58-63. I understand that in related litigation Netlist has interpreted this claim term broadly, even though a narrower interpretation may be more reasonable. *See infra* ¶¶ 113, 246. My analysis below shows that the claims are invalid under both interpretations.

2. "*memory module*"

77. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*memory module*" includes a printed circuit board or other removable carrier that contains one or more RAM memory chips.

78. For instance, the '608 Patent discloses that a "memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB)." EX1001 at 1:50-55; *see also* Microsoft Computer Dictionary 334 (5th ed. 2002) (EX1023) (defining a "memory module" as a "removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips.").

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3. "*memory controller*"

79. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*memory controller*" includes "any device capable of sending instructions or commands, or otherwise controlling memory devices." EX1001 at 4:46-49.

4. "*memory bus*"

80. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*memory bus*" includes "any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller." EX1001 at 4:50-53. "For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission." *Id*. at 4:53-58.

5. "*system command signals*"

81. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*system command signals*" includes signals, such as control and address signals, that the module control device received from the memory controller and correspond to commands to control memory operations.

82. For example, the '608 Patent states that "[t]he memory module is operable to perform memory operations in response to memory commands (*e.g.*,

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read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals." EX1001 at 3:29-38; *see also* 4:65-5:4 ("the module control device 116 receives system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal lines 120").

6. "*module command signals*"

83. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*module command signals*" includes signals, such as control and address signals, that the module control device derived from the "*system command signals*" and provided to the memory devices to control the operation of the memory devices.

84. The '608 Patent states that "the module control device ... generates a set of module command signals ... in response to each memory command from the memory controller," and that the "module command signals are transmitted by the module control device to the memory devices via module C/A signal lines." EX1001 at 3:41-46. The '608 Patent also explains that the "[m]odule control

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device 116 transmits the module command signals to the memory devices 112 via module C/A signal lines 220. The memory devices 112 operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller." EX1001 at 5:58-63; *see also id.* at 5:27-42 ("Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.").

7. "*module control signals*"

85. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*module control signals*" includes signals that the module controller (also referred to as "module control device" or "module

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controller") derived from the "*memory command signals*" and provided to buffer circuits to control their operations. EX1001, 4:27-30.

86. For example, the '608 Patent states that "the module control device ... generates ... a set of module control signals in response to each memory command from the memory controller," EX1001 at 3:41-44, and that in each buffer circuit the "module control signals from the module control circuit . . . control the data path," *id.* at Abstract; *see also id.* at 3:47-50 ("[T]he module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines."); *id.* at 5:43-51 ("Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (*e.g.*, test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals.").

8. "*metastability*"

87. In light of the '608 Patent specification, a Skilled Artisan would have understood that the claim term "*metastability*" includes a condition when a signal

has a misalignment with the relevant clock signal resulting in an output signal with a temporary indeterminate binary value.

88. For example, the '608 Patent states that, "[a]s the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals." EX1001 at 9:42-45 (emphasis added).[1]; *see also* EX1022 (Stone textbook) at 107 (explaining "metastable" state is when "the output lies about midway between a logic 0 and logic 1. The output stays in this condition for a variable and unpredictable amount of time, then relaxes unpredictably to either a logic 0 or logic 1.")

IV. OVERVIEW OF THE PRIOR ART

A. U.S. Publication No. 2010/0312956 to Hiraishi (EX1005)

89. United States Published Patent Application No. US 2010/031256 to Hiraishi ("Hiraishi") was filed in the United States on June 3, 2010 and published on December 9, 2010. EX1005. I therefore understand that Hiraishi is prior art to the '608 Patent pursuant to 35 U.S.C. §§ 102(a) & (b) & (e). Hiraishi was not cited or discussed during prosecution of the '608 Patent. *See* EX1002. Indeed, although institution of the IPR to the related 632 Patent was denied over a related reference,

[1] All emphasis in this declaration has been added unless otherwise indicated.

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US Pat. Pub. No. 2010/0309706 (Saito), the '608 claims are broader than the '632 claims according to Netlist, and I have seen no evidence that the '608 claims were considered in light of either Saito or Hiraishi. *See* EX1014 ('632 Decision); *supra* § III.D.5, ¶¶ 56-61.

90. Hiraishi discloses an information processing system 10 including a memory system (20) with a memory module (100) and a memory controller ("memory control hub," MCH 12) for controlling the memory module. EX1005 (Hiraishi), FIG. 2, [0063-65].

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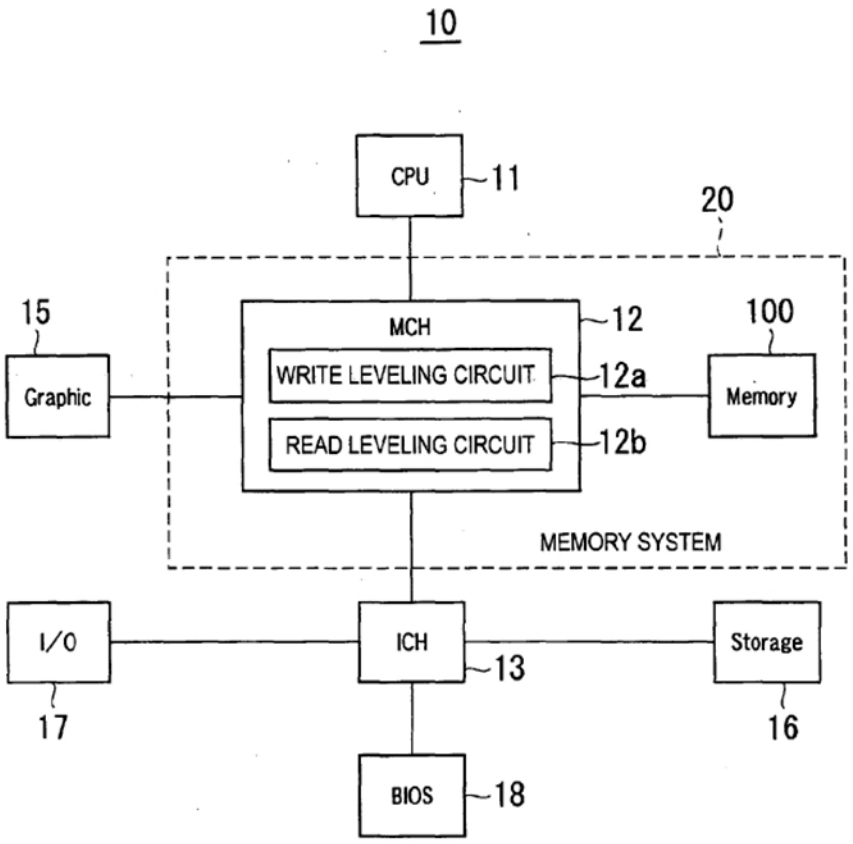


FIG.2

Hiraishi also discloses a perspective view that includes the memory system 20. *Id*. [0067-68], FIG. 3 (reproduced below).

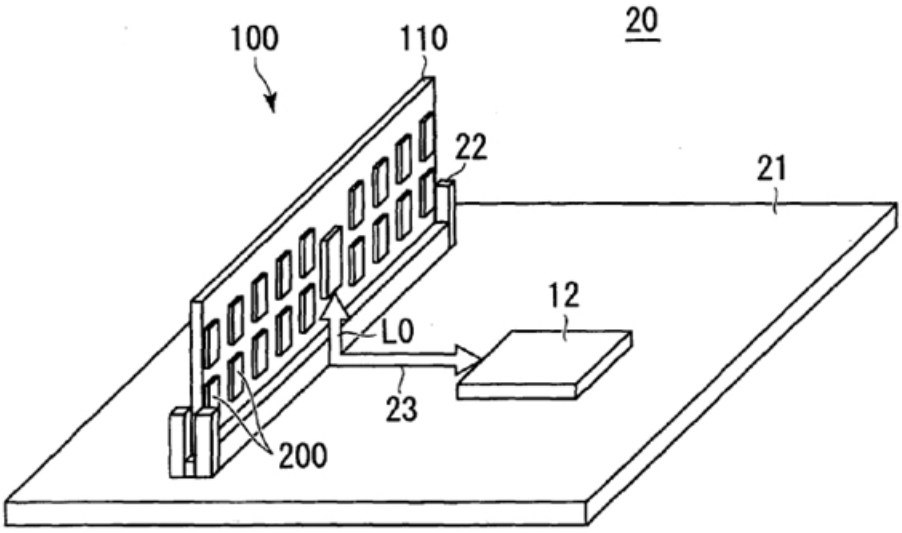
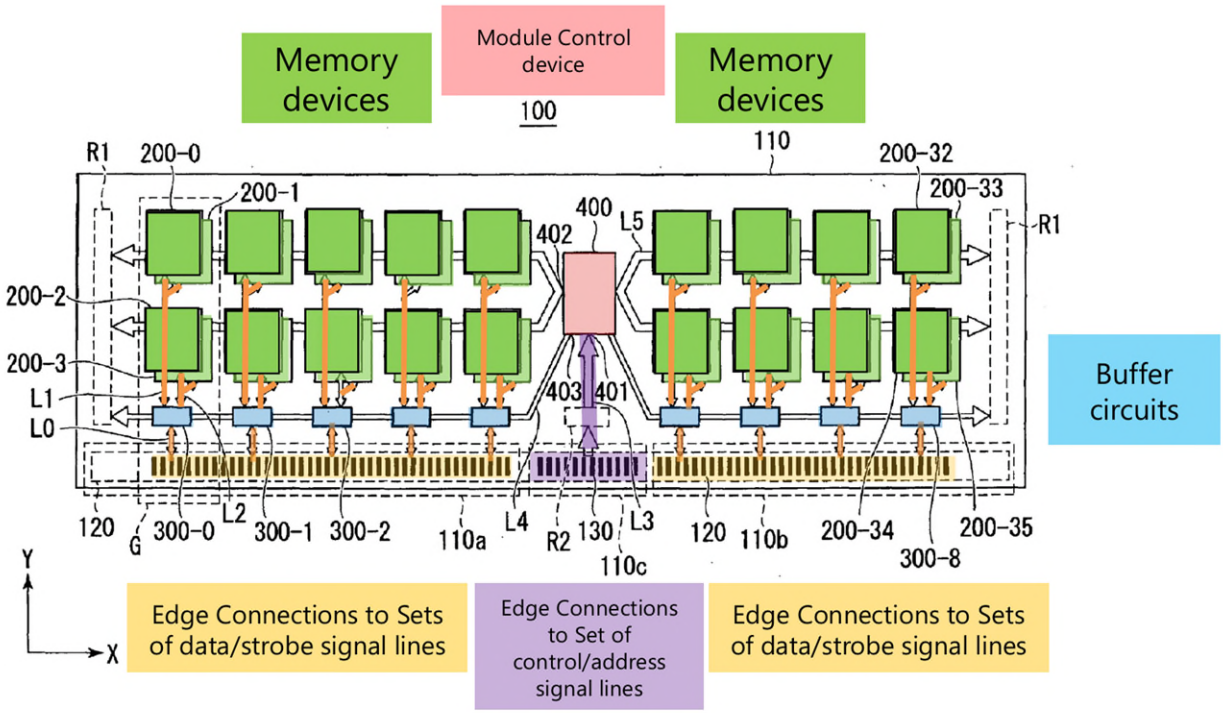


FIG.3

"As shown in FIG. 3, a memory slot 22 is provided on the motherboard 21, so that the memory module 100 is inserted in the memory slot 22. On the other hand, a memory controller 12 is directly mounted on the motherboard 21." *Id*.

91. Annotated Figure 1 of Hiraishi, reproduced below, illustrates an implementation of the memory module 100. The memory module 100 includes a "command/address/control register buffer" (400, red), EX1005 at ¶¶[0045], [0059], [0060], "memory chips" (200, green), *id*., and "data register buffers" (300, blue), *id*. at ¶¶[0046], [0055]. The memory module also includes "data connectors" (120, yellow), *id.*, ¶[0048], and "command/address/control connectors" (130, purple), *id*., at ¶[0049], to couple the corresponding data/strobe lines and control/address signal lines of a system memory bus.



A connection diagram of the memory module 100 is illustrated in FIG. 7 of Hiraishi, showing the connections in the middle and one (left) side of the module 100, including the bus L0 between the data connectors 120 and the data register buffer, the busses L1 and L2 between the data register buffer (300) and the memory devices (200), the bus L3 between the command/address/control connectors 130 and the command/address/control register buffer 400, the bus L4 between the command/address/control register buffer 400 and the data register buffer (300), and the bus L5 between the command/address/control register buffer 400 and the memory devices (200). *Id.* [0103], [0107] and FIG. 7 (reproduced below with annotations).

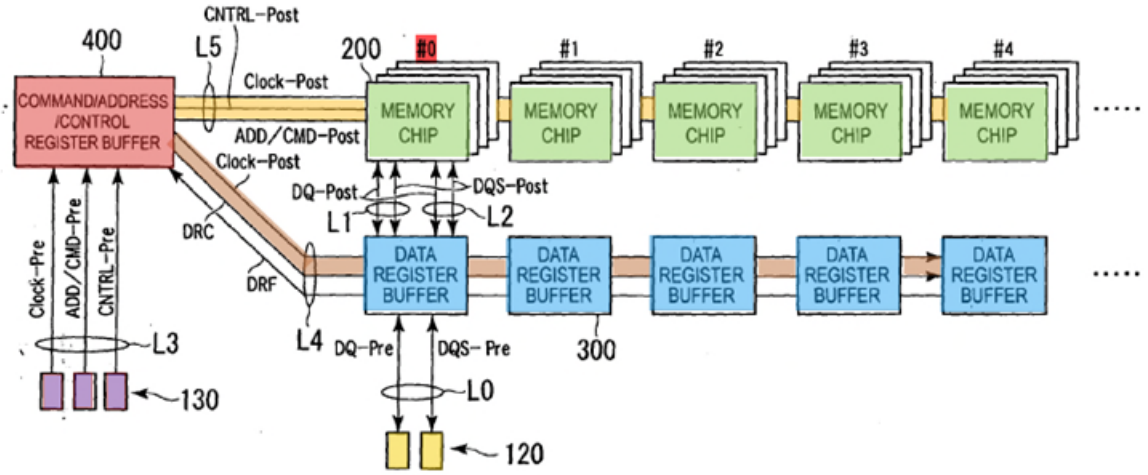


FIG.7

92. The memory module can include "thirty-six memory chips," (200, green), EX1005, ¶[0046], which are mounted on "a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle." *Id.*, ¶[0047]. A plurality of data connectors (120, yellow) and a plurality of command/address/control connectors (130, purple) are located along one of the long sides, and are provided "for making an electrical connection with a memory controller via a memory slot." *Id.*

93. The 36 memory chips are in a "4-rank configuration." *Id.*, ¶[0051]. "[F]our memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other." *Id.*, ¶[0052]. The memory module includes "nine data register buffers"

(300, blue), each of which is associated with one of the nine groups of four memory chips. *Id.*, ¶[0046], [0055]. The data connectors (120, yellow) "exchang[e] write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller." *Id.*, ¶[0048]. The data connectors are located "substantially right below the memory chips," with the corresponding data register buffers in between the memory chips and the connectors. *Id.*, ¶[0048], [0056] & Fig.1.

94. The "command/address/control register buffer" (400, red) is centrally located on the memory module. *Id.*, ¶[0059]. The "command/address/control connectors" (130, purple) are centrally located below the "command/address/control register buffer" (400, red), and are "connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400." *Id.*, ¶[0049] & Fig.1.

95. The "command/address/control register buffer" (400, red) "receives the command signal, the address signal, the control signal, and the clock signal" from the memory controller at an input terminal 401 (purple), "buffers the signals, and supplies the signals" at an output terminal 402 (orange) to the memory chips (200, green). *Id.*, ¶¶[0060], [0061]. Simultaneously, the "command/address/control register buffer" (400, red) "generates a control signal" and supplies it at the output

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terminal 403 (brown) to the data register buffers (300, blue). *Id.*, ¶¶[0060], [0096-97], FIG. 6 (reproduced below with annotations).

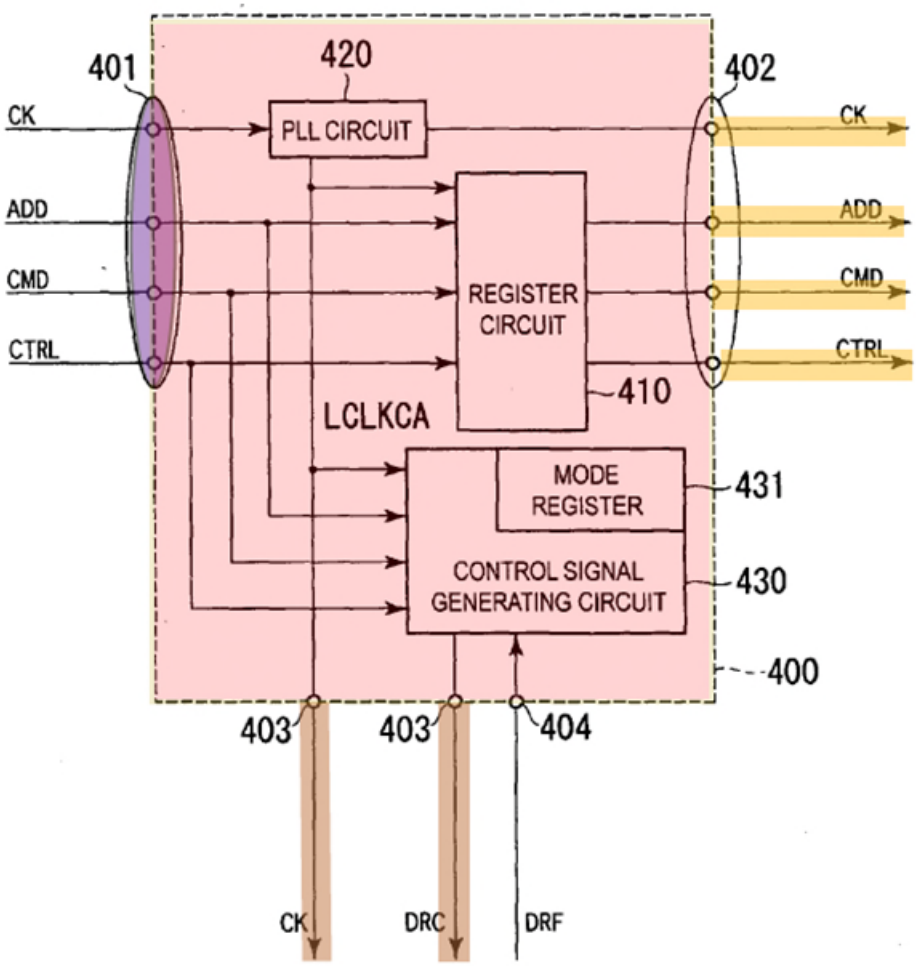

FIG.6

96. Because of high speed operation and differing locations of "memory chips" (200, green) and "data register buffers" (300, blue) relative to the "command/address/control register buffer" (400, red), Hiraishi recognizes that there may be signal timing discrepancies. *Id.*, ¶¶[0090], [0104]. Accordingly, the memory module makes "timing adjustments" to account for the signal timing

discrepancies during initialization by performing write leveling and read leveling operations. *Id.*, ¶¶ [0140]-[0141]. Each group of memory chips/data register buffers performs two sets of write and read leveling operations, one "between the data register buffer 300 and the memory chip 200" referred to as "Step S4," *id.*, ¶[0140], and one "between the memory controller and the data register buffer 300" referred to as "Step S5," *id.*, ¶[0141].

97. An implementation of Hiraishi's data register buffer 300 is illustrated in FIG. 5 (reproduced below with annotations). As shown here, the data register buffer 300 (blue) includes a data register control circuit 320 (upper right) with a write leveling circuit 322 and a read leveling circuit 323 to perform the "S4" leveling operations between the data buffer and the memory chips. EX1005, [0142], [0147], and FIG. 5 (reproduced below with annotations).

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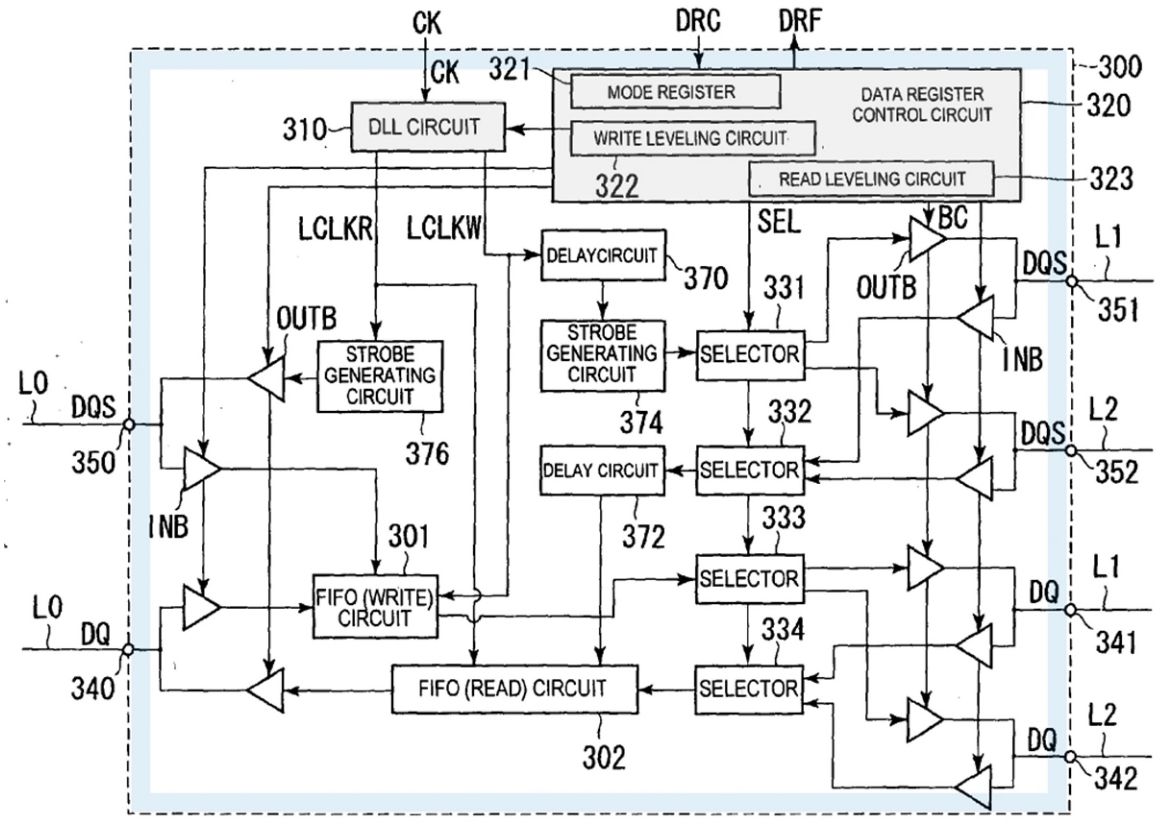

FIG.5

The "data register buffer" (300, blue) also includes a "DLL circuit" (310). *Id.*, ¶[0084]. "The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400." *Id.*, ¶[0087]. For example, "[a]n output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310[, and a]n output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310." *Id.*

B. U.S. Patent No. 8,020,022 to Tokuhiro (EX1006)

98. U.S. Patent No. 8,020,022 to Tokuhiro (EX1006) was filed on September 12, 2008 and issued on September 13, 2011. I understand that Tokuhiro is prior art to the '608 Patent pursuant to at least 35 U.S.C. §§ 102(a) & (e). Tokuhiro was not cited or discussed during the prosecution of the '608 Patent. *See* EX1002.

99. Tokuhiro discloses a memory module that includes a plurality of SDRAMs connected to a memory controller by signal lines. EX1006 at 1:38-47. Tokuhiro recognizes the problems of fly-by delays, for example, in DDR3 memory systems. Tokuhiro explains:

> [I]n the DDR3 memory interface, because the clock signal line for the clock signal CK is wired to the plurality of SDRAMs 92-1 to 92-n through the daisy chain connection and a propagation delay is generated, ***the clock signal CK output from the memory controller 90 cannot reach all the SDRAMs 92-1 to 92-n at the same time***. According to the JEDEC standards, for example, a length L1 of outer dimension of the DIMM module 91 is determined to be 133 mm. Assuming a data transmission speed to be 7 ps/mm, therefore, a difference of about 1 ns is generated in arrival time of the clock signal CK between the SDRAM 92-1 disposed at one end and the SDRAM 92-n disposed at the other end of the DIMM module 91 in the lengthwise direction thereof (namely, 7 ps/mm×133 mm=931 ps).

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EX1006 at 1:63-29. Tokuhiro further notes that, for this reason, the JEDEC standards specify employing write leveling in the DDR3 memory interface. *Id.* at 2:10-12.

100. However, Tokuhiro notes that although "the DDR3 memory interface compensates the arrival time when the data strobe signals DQS-1 to DQS-n arrive at the SDRAMs 92-1 to 92-n in the write operations according to the JEDEC standards as described above, ***compensations of the signal arrival time in read operations are not provided with the JEDEC standards***." *Id.* at 2:54-59. A Skilled Artisan would have understood that such a compensation of arrival times for read operations was known as read leveling, similar to compensating arrival times for write operations was known as write leveling. Tokuhiro explains that in connection with conventional DDR3 memory interfaces, "the data signal DQ-n and the data strobe signal DQS-n output from the SDRAM 92-n to which the clock signal CK is input lastly arrives at the memory controller 90 approximately 1 ns after the data signal DQ-1 and the data strobe signal DQS-1 output from the SDRAM 92-1 to which the clock signal CK is input firstly where the data transmission speed is 7 ps/mm as the case described above. 7 ps/mm×133 mm=931 ps." *Id.* at 3:1-8.

101. Tokuhiro further identifies a specific problem that happens when this fly-by delay becomes greater than one clock cycle:

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> The delay on the order of 1 ns will become ***greater than a typical data period*** of the DDR3 memory interface, at minimum 0.625 ns, so that ***the delay may affect in reading data*** from the SDRAM 92.

Id. at 3:9-12.

102. As a solution to this problem, Tokuhiro proposes determining a first delay time utilizing the ***write*** leveling function, *i.e.*, a mechanism for determining timing for write operations, and using this delay time not just for write operations but also to delay the transmission of data during ***read*** operations. *See, e.g., id.*, 3:16-26 ("a first variable delay unit for delaying, in the write operation, a data strobe signal output to the memory by ***a first delay time that is set by utilizing the write leveling function*** and ***a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time***"); Fig. 11 (annotated, showing compensations to fly-by delays of memory devices SDRAM-1 to SDRAM-n (green) by respective read delay elements DR-1 to DR-n in a data-handling part (blue) interfacing with the memory devices during a memory read operation):

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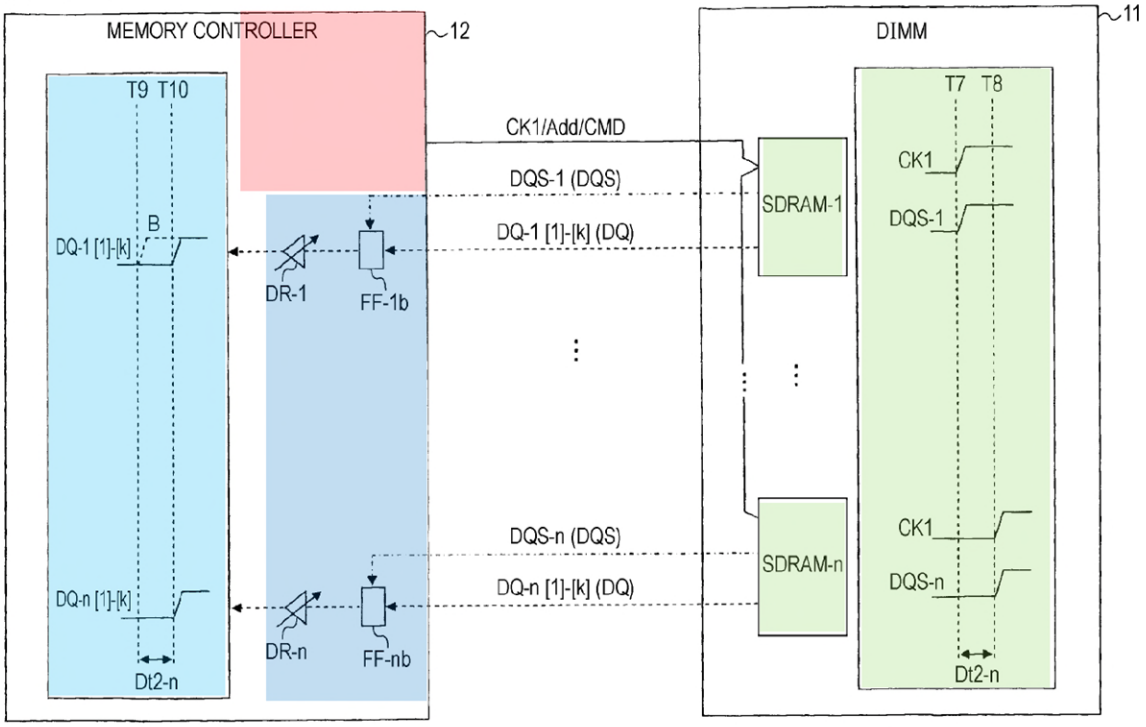
FIG. 11



C. U.S. Patent Publication No. 2006/0277355 to Ellsberry (EX1007)

103. U.S. Patent Application Publication No. 2006/0277355 to Ellsberry ("Ellsberry") (EX1007) was filed on June 1, 2005 and published on December 7, 2006. I understand that Ellsberry is prior art to the '608 Patent pursuant to 35 U.S.C. §§ 102(a) & (b). Although Ellsberry was cited in the '608 Patent (among hundreds of other references, *see* EX1002 at 151, 252), it was not discussed during prosecution. *See* EX1002.

104. Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi and additionally expressly describes modules with 8-bit wide data buffers and with either 8-bit wide chips or

pairs of 4-bit wide chips. For example, Ellsberry's FIGS. 2, 5, and 13 correspond to an embodiment of Ellsberry utilizing 8-bit memory devices, EX1007 at ¶[0056], FIGS. 2, 5, 13 (FIG. 13 reproduced below), while FIGS. 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit memory devices, EX1007 at FIGS. 2, 6, 11 (FIG. 11 reproduced below); *see also* EX1015 ('907 Decision) at 57, 60, 66, 68, 77, 81 (Board concluding that Ellsberry discloses 8-bit memory devices, and also pairs of 4-bit memory devices).

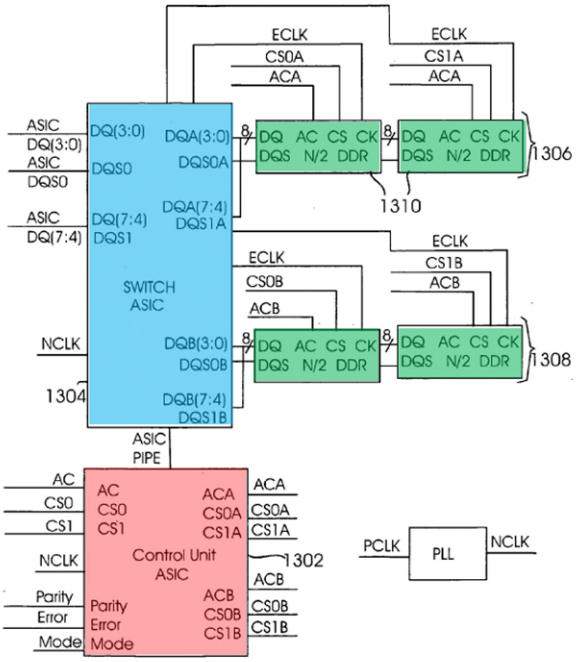


Fig. 13

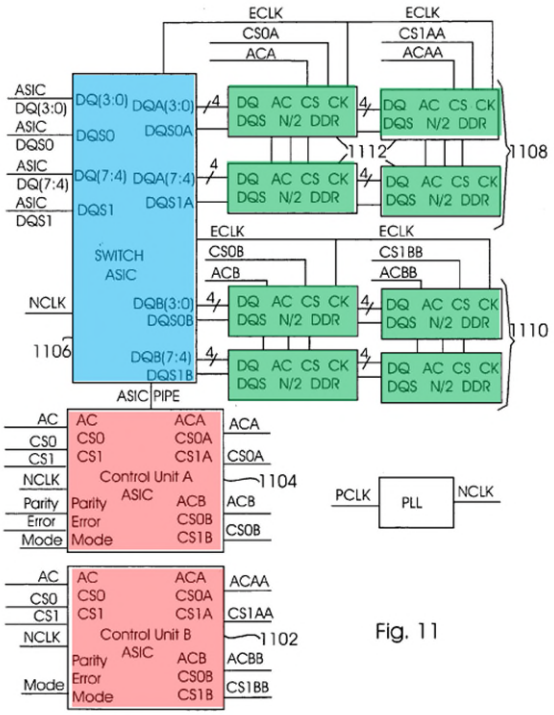


Fig. 11

D. U.S. Patent Publication No. 2007/0008791 to Butt (EX1029)

105. U.S. Patent Publication No. 2007/0008791 to Butt ("Butt") (EX1029) was filed on July 7, 2005, and published on January 11, 2007. I understand that

Butt is prior art to the '608 Patent pursuant to 35 U.S.C. §§ 102(a), (b) & (e). Butt was not cited or discussed during the prosecution of the '608 Patent. *See* EX1002.

106. Butt discloses a method for calibrating a data valid window for memory devices. EX1029 at [0005]. According to Butt, previous approaches "relie[d] heavily on the pre-silicon, system-level, SPICE timing analysis," and there was thus a need for calibrations that could calibrate the actual data valid window in the silicon. *Id.,* [0003]-[0004]. Butt describes the method as follows:

> (A) setting a base delay of one or more datapaths to a predetermined value, (B) determining an optimum offset delay value for each of the one or more datapaths based upon actual memory accesses and (C) delaying a read data strobe signal based upon the base delay and the optimum offset delay value for each of the one or more datapaths.

Id., [0005].

107. Butt further describes an exemplary circuit for implementing this method, with a block diagram of illustration in FIG. 2 (reproduced below). As shown here, physical read datapaths 114 (red) can be configured to receive both the read data signals (DQ) (orange) and the read data strobe (DQS) (orange, dashed) from the DDR memory (green), and to communicate with asynchronous first-in, first-out buffers 112 (olive). *Id.,* [0017].

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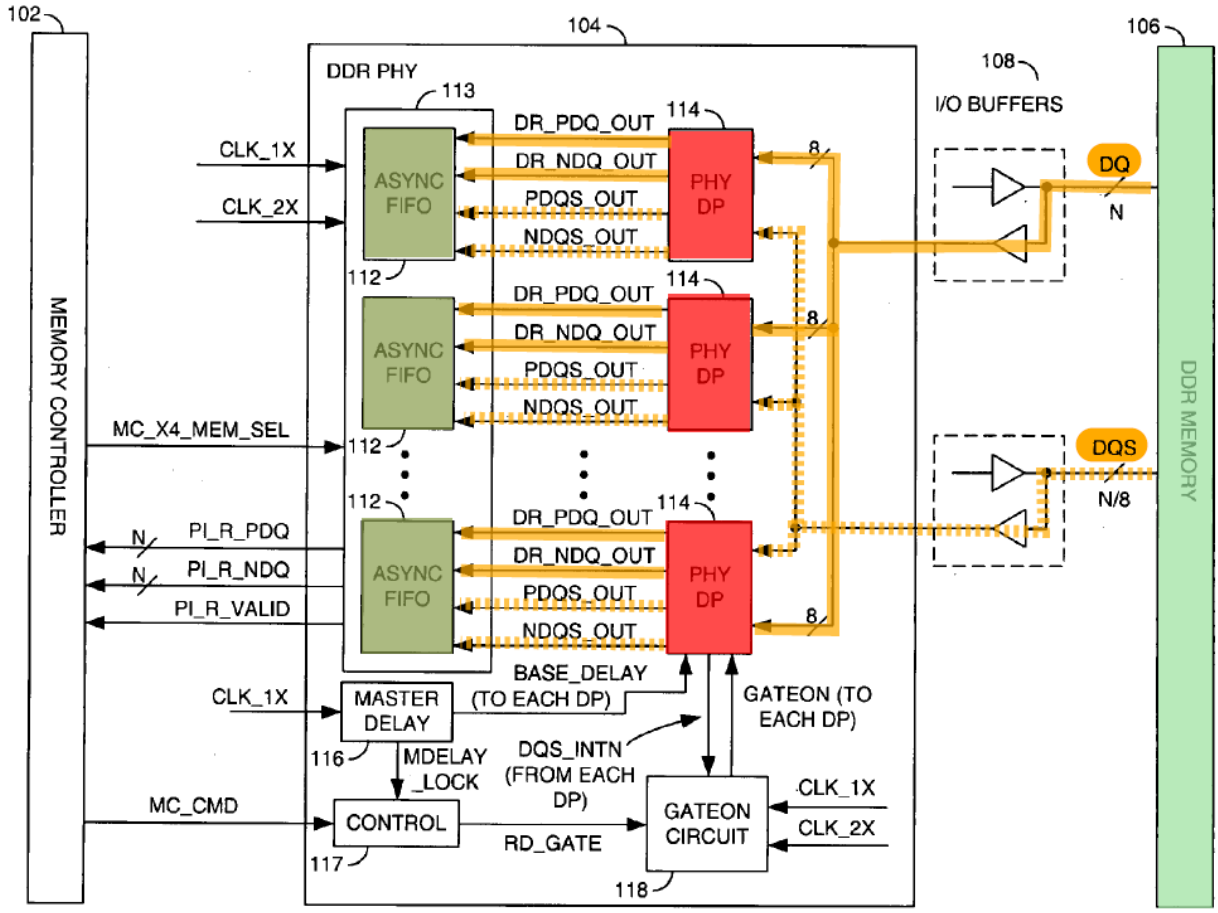

FIG. 2

Id., Fig. 2.

108. Butt further teaches that the datapaths 114 (red) sample the data signal DQ (orange) based on a delayed read strobe signal DQS (orange dashed):

> The DPs may be configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116. Each of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO 112 via the signals DR_PDQ_OUT and DR_NDQ_OUT,

> after the data is sampled using the delayed read data strobe signals DQS.

Id., [0018]. The master delay ("MDELAY") circuit 116 in Butt can set a base delay for the datapaths 114. *Id*., [0014], [0022].

109. Butt further describes additional training by which the datapath 114 can achieve an optimum offset for centering the read strobe DQS data eye in the valid data window:

> The present invention generally provides for adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window. For example, when the delay is too short, the read data strobe signal DQS is generally earlier than a minimum boundary of the valid data eye window (e.g., trace 140). When the delay is too great, the read data strobe signal DQS is generally later than a maximum boundary of the valid data eye window (e.g., trace 142). In general, a correctly set delay places the read data strobe signal DQS within the valid data eye window (e.g., trace 144).

Id., [0035]. As illustrated below in Fig. 5, the optimum offset for each datapath 114 is determined by iteratively checking the validity of test data at different offsets until a maximum and minimum offset are identified. *Id*., [0045], Figs. 6 and 7. These minimum and maximum values can then be used to determine the optimal offset for the data eye. *Id*., [0046].

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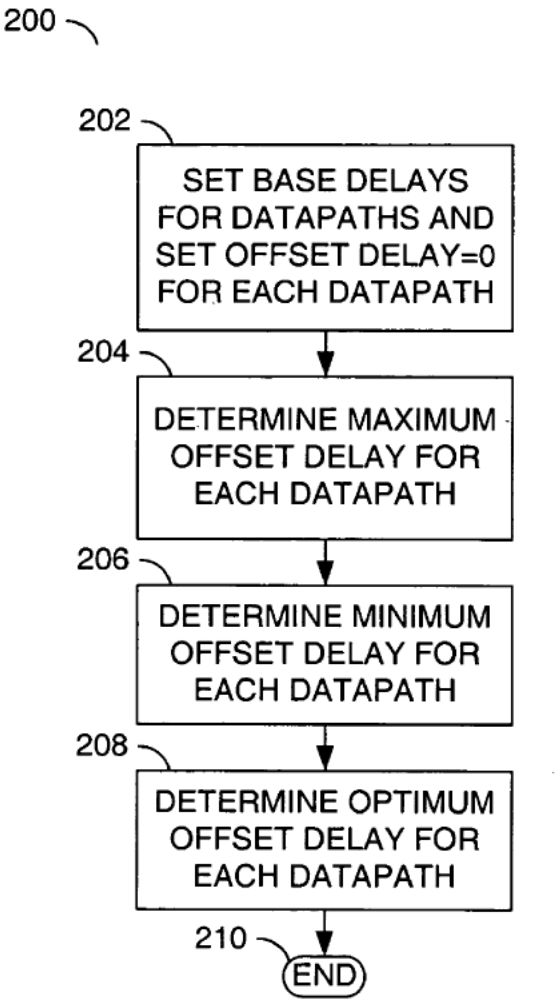

FIG. 5

Id., Fig. 5. The optimum offset values can then be programmed into each datapath 114, which is the end of the training. *Id*., [0046].

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E. U.S. Patent No. 6,184,701 to Kim (EX1008)

110. United States Patent No. 6,184,701 to Kim ("Kim") (EX1008) was filed on May 27, 1999 and issued on February 6, 2001. I therefore understand that Kim is prior art to the '608 Patent pursuant to 35 U.S.C. §§ 102(a) & (b).

111. Kim teaches that, when a circuit "receives input signals at similar analog levels [it] may be prone to generating an output signal in a metastable state (*i.e.*, where the potential of the output signal is greater than a maximum logic 0 level (VJL) and less than a minimum logic 1 level (VJH)). Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output generation." EX1008 at 1:21-31. To solve that problem, Kim discloses "a metastability detection/prevention circuit 20" to be incorporated with any "main active circuit 10" in need thereof. EX1008 at 2:21-22. For example, Kim teaches that the "the circuit 10 may comprise a data input buffer." *Id.* at 2:30-31. "[T]he metastability detection/prevention circuit 20 preferably performs the function of detecting whether the output POUT of the main active circuit 10 has been disposed in a metastable state for a duration in excess of a transition duration." *Id.* at 2:3-37.

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V. COMPARISON OF THE PRIOR ART TO THE CLAIMS

112. My analysis below is based on my understanding of the law and the other information discussed above, including the four Grounds discussed above.

A. Claims 1-12 are Obvious Over Haraishi in Combination with Butt or in further view of Kim and/or Ellsberry

113. I understand that in related litigation involving the '608 Patent and the related '035 Patent, Netlist has asserted that "*memory operations*" can include a read leveling operation between the memory chips and the data buffers, followed by a read operation, and that a "*delay…determined by the command processing circuit [in the buffer circuit]*" can include programming by the system memory controller. *See, e.g.*, EX1035 (Netlist Complaint against Micron) at ¶¶90-91, 121 (accusing DRAM-to-DB Read Delay (MRD) Training Mode where the system memory controller programs the delays); EX1048 at 54 (construing "memory operations" to be not limited to "ones involving writing to or reading from a DRAM"); EX1057 at 62 (pointing to delays from read and write leveling programmed by the system memory controller, EX1058 at 26-27). Netlist's apparent construction for this limitation differs from the teaching of the '608 Patent, which teaches the use of two different memory operations, where the first "*memory operation*" is a memory operation (*e.g.*, write) that transfers data in a different direction than the second "*memory operation*" (*e.g.*, read). During read leveling — the operation that Netlist contends satisfies this limitation — the

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memory provides predetermined read data from a register in response to a read command. After read leveling, the memory can also perform a read operation addressed to the memory array in response to a read command. The '608 Patent, however, focuses on signal timing between circuits, and there is no difference in timing between how the memory provides read data during read leveling vs. a read operation. Although read leveling and a read operation differ in terms of the place which the information is read from (a register during read leveling vs. a memory array location according to an address during a read operation), a Skilled Artisan would have understood at the time that the memory would operate the same way in terms of timing during read leveling and subsequent read operations, since the optimal timing the buffer found during read leveling is for the very purpose of using that optimal timing during the subsequent read operations. Netlist's apparent construction for this limitation also conflicts with the specification of the '608 Patent, which states that the conventional "leveling mechanisms for write and/or read operations for unbalanced wire length … [are] insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules." EX1001 at 2:28-36. As discussed below in detail, the Skilled Artisan would have understood that, during a conventional read leveling operation, the memory provides predetermined read data in response to a read command with its regular timing, and the memory controller detects timing information for

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subsequent read operations assuming that the memory performs those read operations with the same timing. Thus, the '608 Patent teaches to a Skilled Artisan that a traditional leveling operation (e.g., read leveling) followed by a memory operation in the same direction (e.g., read operation) is not directed to two different memory operations, since read leveling finds timing for a read operation and this read timing is subsequently used for the same type of read operations. Instead, the '608 Patent is directed to different operations of the memory, namely to a "signal alignment mechanism to time the transmission of ***read*** data signals based on timing information derived from a prior ***write*** operation." *Id*. 15:23-26 (emphasis added). Similarly, the '608 Patent teaches that it is the buffer circuit which determines the read delays based on the timing of the write command and the corresponding write data. *Id*. at Figs. 12A and 12B, 15:27-16:9 ("The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system 100, and is controllable by the MCH 101 and knowable to the isolation device 118. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device 118 since both these signals are received by the isolation device. Based on such determination, the isolation device 118 can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device 118 to properly time transmission of read data to the MCH, as explained

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further below."). In my analysis below, I show that the claims of the '608 Patent are invalid under both the broader construction for this limitation asserted by Netlist, *infra* § V.A, and under an interpretation that is more consistent with the specification and the file history, *infra* § V.B.

114. I also understand that, in the related litigation, Netlist has further asserted that a single bi-directional "data path" between the buffer circuit and the memory devices in multiple ranks is sufficient to satisfy the claims of the '608 Patent (e.g., one bi-directional data path going to memory devices in four different ranks). *See* EX1035 (Netlist Complaint against Micron) at ¶¶118-19. The '608 Patent, in contrast, discloses two different "data paths" creating a "fork in the road" layout (e.g., two bi-directional data paths, each going to memory devices in two different ranks, for a total of four ranks). *See infra* ¶ 222. Hiraishi discloses the same "fork in the road" layout as the '608 Patent, and thus regardless of whether the claims require a "fork in the road" layout (as disclosed in the '608 Patent), or whether a single "data path" with chip-select signals (as accused of infringement by Netlist) is sufficient, in my opinion Hiraishi invalidates the claims of the '608 Patent either way, as shown below. *See, e.g.*, *infra* ¶¶ 191, 222.

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1. Claim 1

a) 1[pre]: "A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising"

115. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 of Hiraishi below, Hiraishi discloses "*a memory module* [such as memory module 100] *operable to communicate with a memory controller* [MCH 12] *via a memory bus* [line 23], *the memory bus including signal lines, the signal lines including a set of control/address signal lines* [to couple to command/address/control line L3 on the module, purple] *and a plurality of sets of data/strobe signal lines* [to couple to data line L0 on the module, orange]."

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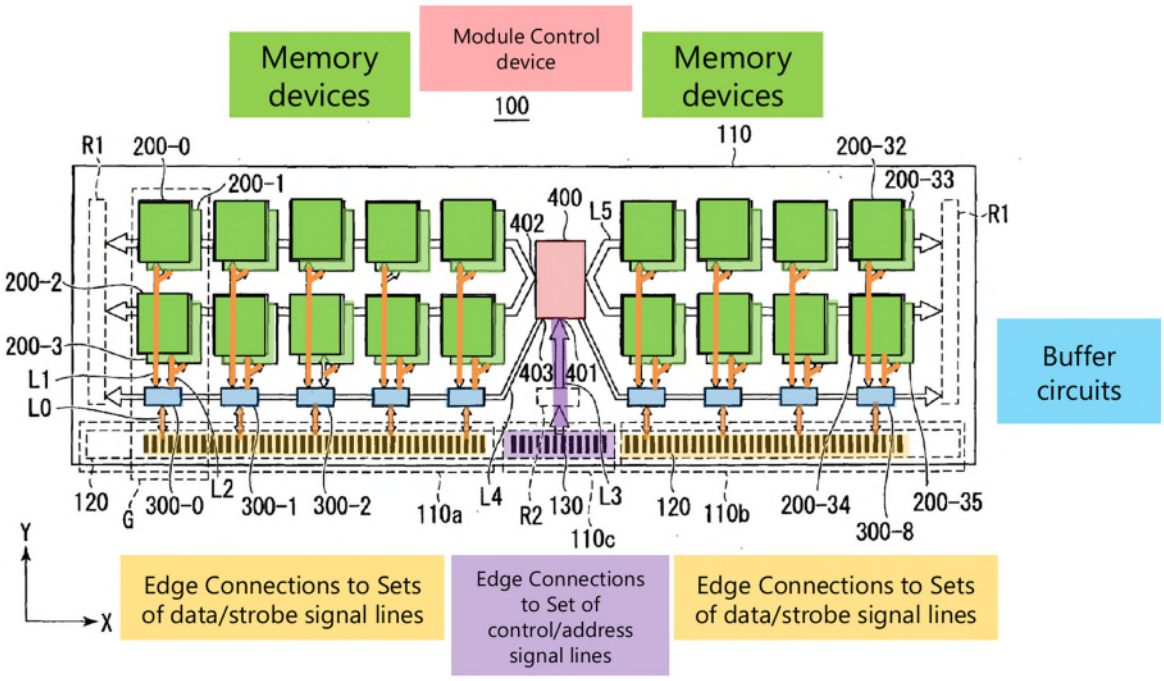

EX1005 (Hiraishi), Fig. 1 (annotated and color added; "command/address/control register buffer" in red, "memory chips" in green, "data register buffers" in blue, "data connectors" in orange, "command/address/control connectors" in purple).

116. Hiraishi discloses that the memory module 100 is connected to memory control hub (MCH) 12 such that the MCH 12 functions as a memory controller for memory module 100:

> The memory module 100 shown in FIG. 1 and a graphic controller 15 are ***connected to the MCH 12***. As shown in FIG. 2, the memory module 100 and the MCH 12 constitute a memory system 20, where the MCH 12 has a controller function for the memory module 100. That is, ***the MCH 12 functions as a memory controller for the memory module 100***.

Id, ¶[0065]. Hiraishi discloses that memory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) that is coupled to data line L0 and the command/address/control line L3 on the memory module 100. EX1005, [0069] and FIGS. 2 and 3 (reproduced below).

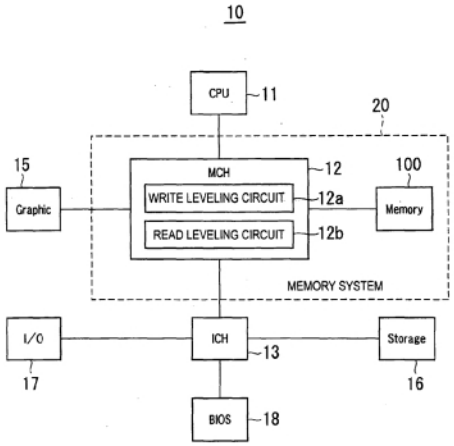

FIG.2

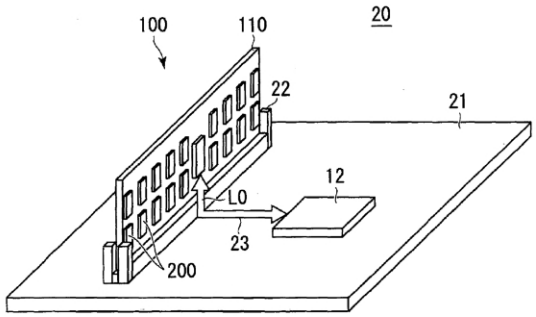

FIG.3

Id., FIGS. 2 and 3. Thus, a Skilled Artisan would have understood that memory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) as recited in the preamble.

117. Hiraishi further discloses that the memory bus (line 23) includes signal lines, the signal lines including a set of control/address signal lines coupling, through command/address/control connectors 130 (purple), to command/address/control line L3, and a plurality of sets of data/strobe signal lines, each set coupling, through data connectors 120 (orange), to data line L0. *See id.*, [0102-103], FIG. 1 (annotated above in ¶ 115) and FIG. 7 (annotated below).

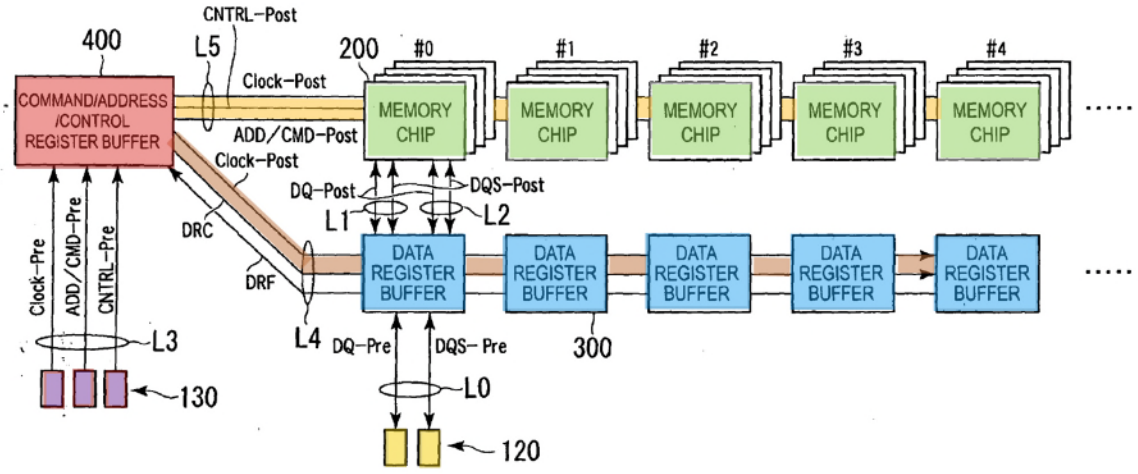

FIG.7

Hiraishi explains that the memory bus includes a set of data/strobe signal lines:

> As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the ***data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, ***a plurality of data transferred through the data line L0*** is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, ***a data strobe signal transferred through the data line L0*** is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

Id., [0103]. Hiraishi also explains that the memory bus includes a set of control/address signal lines:

> The data connectors 120 and the ***command/address/control connectors 130*** are terminals ***for making an electrical connection with a memory controller*** via a memory slot … The ***command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal***, and a clock signal to be supplied to the command/address/control register buffer 400.

Id., [0047], [0049]; *see also* [0069] (explaining that the signal path between the memory controller 12 and memory chips 200 includes line 23 on the motherboard and the data line L0 and the command/address/control line L3 on the module 100). The buffered command/address/control signal is supplied to the memory chips, and the control signal is supplied to the data register buffers."). Thus, a Skilled Artisan would have understood that the memory bus includes signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines as recited in the preamble.

b) 1[a]: "a module board having edge connections for coupling to respective signal lines in the memory bus"

118. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 of Hiraishi below, Hiraishi discloses "*a module board* [module substrate 110] *having edge connections* [including command/address/control

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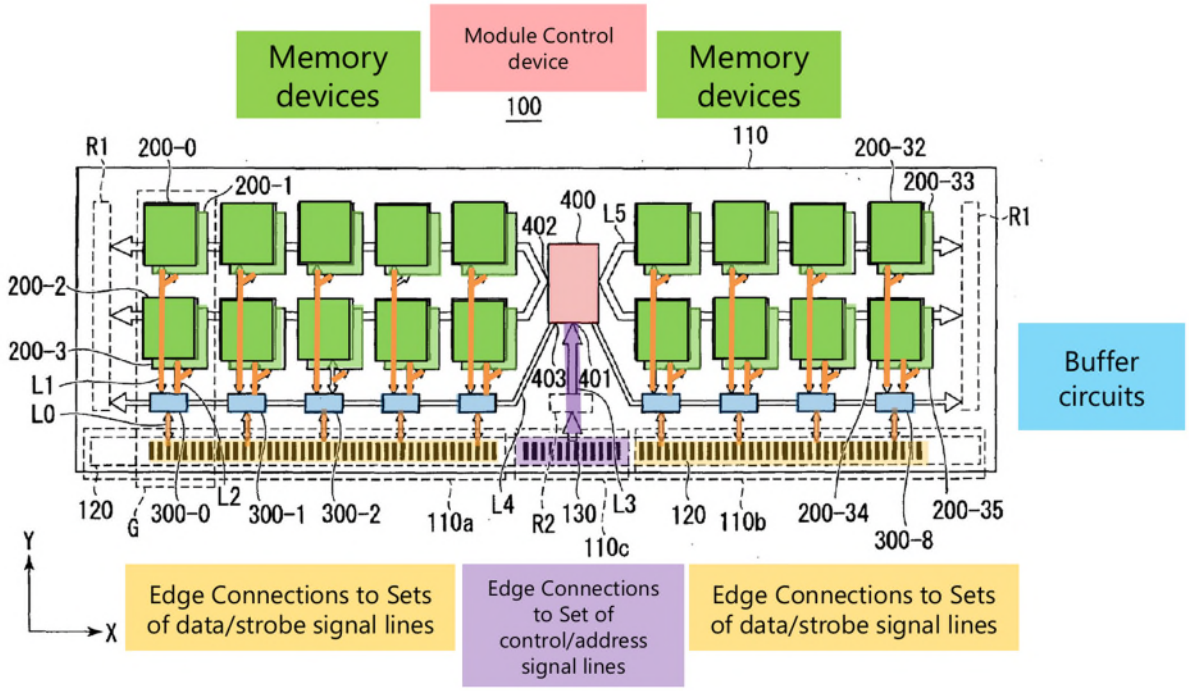
connectors 130 (purple) and data connectors 120 (orange)] *for coupling to respective signal lines in the memory bus* [line 23, shown above in Fig. 3]."



Id., Fig. 1 (annotations and color added showing command/address/control connectors 130 (purple) and data connectors 120 (orange)).

119. Hiraishi discloses that the memory module 100 shown in Figure 1 includes a module printed circuit board (PCB):

> As shown in FIG. 1, the memory module 100 according to the present embodiment includes ***a module substrate 110***, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400. … The ***module***

> ***substrate 110 is a printed circuit board*** that includes a multilayer wiring.

Id, [0045-47].

120. Hiraishi discloses that the module's PCB has connectors 120 and connectors 130 that are arranged at the edge of the PCB:

> The ***module substrate 110 is a printed circuit board*** that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle, as shown in FIG. 1, with a long side in the X direction and a short side in the Y direction. ***On one side of the module substrate 110 along the X direction, which is the long side, a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided***.

Id, [0047]. Thus, a Skilled Artisan would have understood that data connectors 120 and command/address/control connectors 130 are "*edge connections*" as recited in the claim. Indeed, the '608 Patent does not even mention the term "*edge connection*," and its figures provide less detail about connections at the edge of the module than Hiraishi does. *Compare, e.g.*, EX1005, Hiraishi's Fig. 1 (above), to EX1001, Fig. 2C of the '608 Patent (reproduced below with similar coloring annotations).

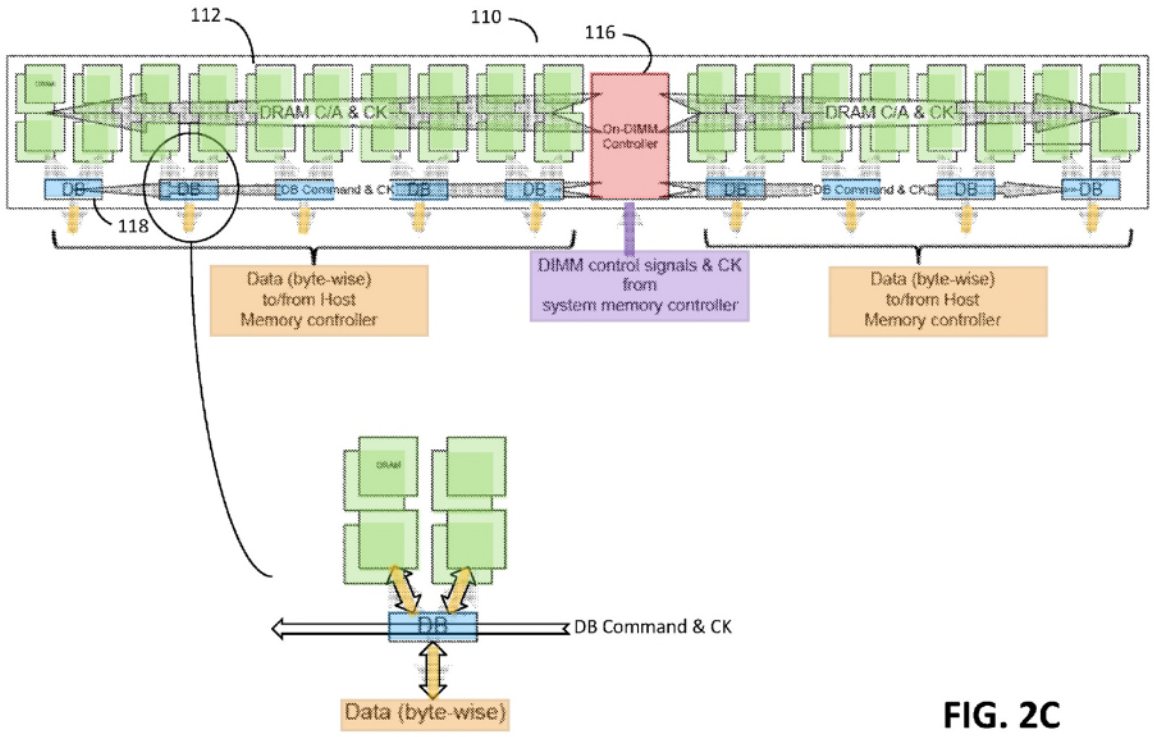


FIG. 2C

121. Hiraishi also discloses that the connectors 120 and 130 are "terminals for making an electrical connection with a memory controller" and that they are used, respectively, for exchanging write and read data with the memory controller, and for supplying command, address, control, and clock signals to the register buffer:

> The data connectors 120 and the command/address/control connectors 130 are ***terminals for making an electrical connection with a memory controller*** via a memory slot, which will be described later.

EX1005 (Hiraishi), [0047];

> The ***data connectors 120*** are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller.

Id., [0048];

> The ***command/address/control connectors 130*** are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400.

Id., [0049]. Thus, a Skilled Artisan would have understood that the "terminals for making an electrical connection" are edge connections for coupling to respective signal lines in the memory bus.

c) 1[b]: "a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal"

122. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 below, Hiraishi discloses "*a module control device* [command/address/control register buffer 400, red] *mounted on the module board* [module substrate 110]."

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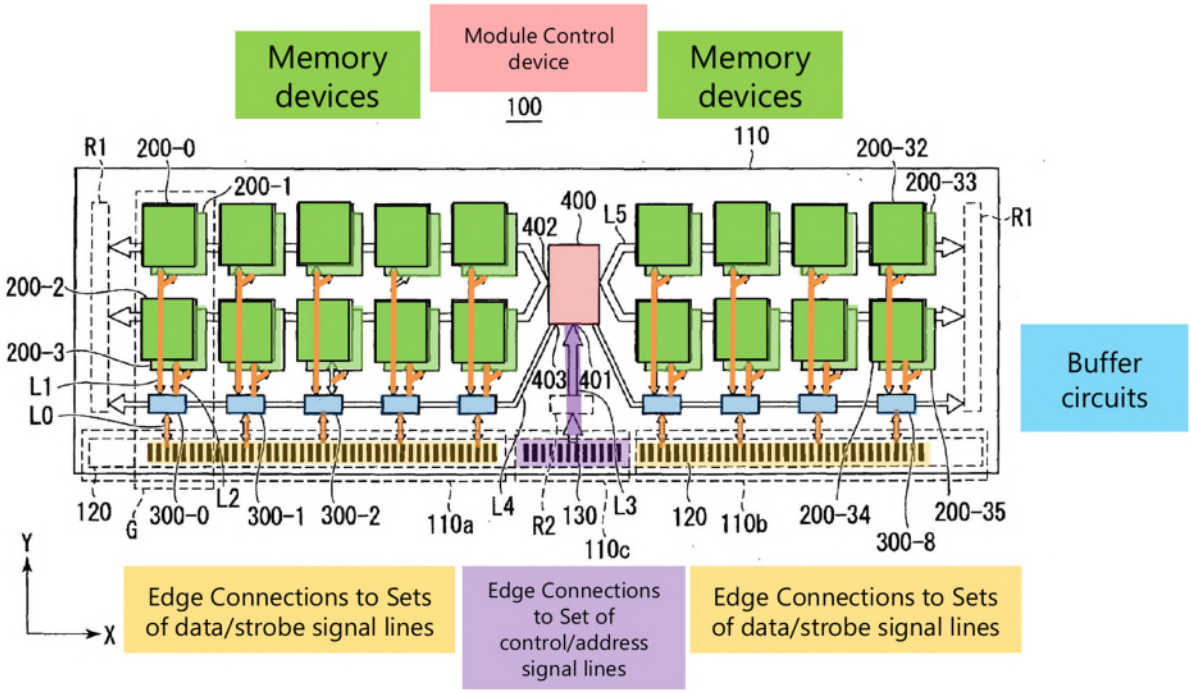

EX1005 (Hiraishi), Fig. 1 (annotations and color added, showing command/address/control register buffer 400 in red).

123. Hiraishi discloses that the command/address/control register buffer 400 is mounted on module substrate 110:

> Only a single ***command/address/control register buffer 400 is mounted on the module substrate 110***. As shown in FIG. 1, the command/address/control register buffer 400 is arranged at an approximate center portion of the module substrate 110 in the X direction, which is the long side.

Id., [0059].

124. Hiraishi also discloses, as illustrated by annotated Figures 6 and 7 below, that the "*module control device*" (command/address/control register buffer

400, red) is "*configured to receive system command signals for memory operations* [such as read or write operations] *via the set of control/address signal lines* [through command/address/control connectors 130 and command/address/control line L3 (Fig. 7) at input terminal 401 (Fig. 6, purple)] *and to output module command signals* [ADD/CMD-Post in module command/address/control line L5 (Fig. 7) at output terminal 402 (Fig. 6, orange)] *and module control signals* [including DRC, brown, on control line L4 (Fig. 7) at output terminal 403 (Fig. 6)] *in response to the system command signals* [received on command/address/control connectors 130 (Fig. 7, purple)], *the module control device being further configured to receive a system clock signal* [Clock-Pre in L3] *and output a module clock signal* [Clock-Post in L4 and L5]."

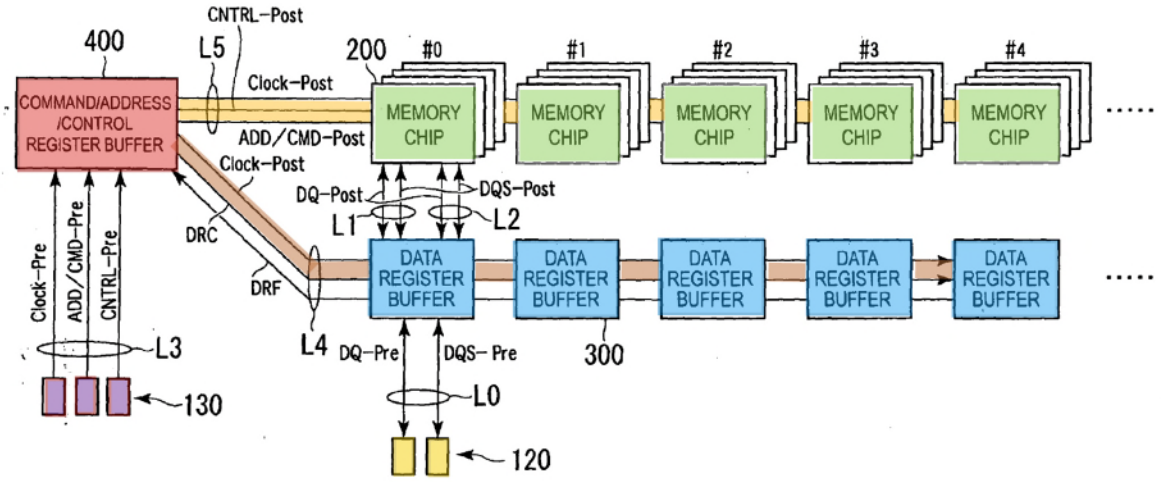

FIG.7

Id., Fig. 7 (color added); *see also* [0019] ("Fig. 7 is a connection diagram of memory module 100");

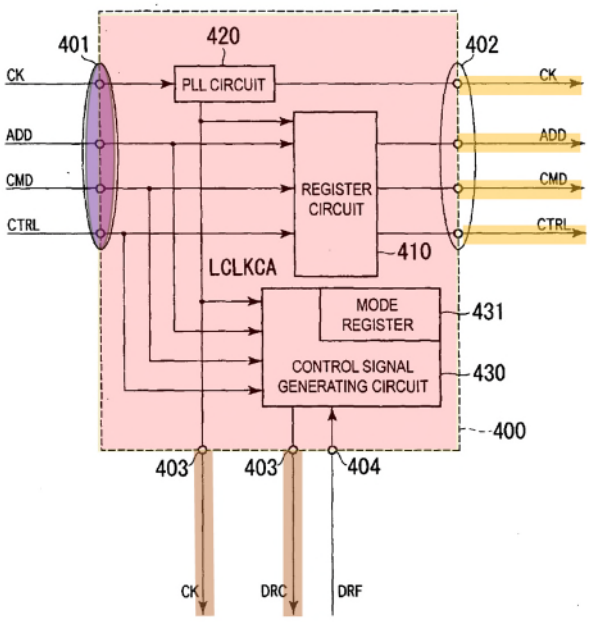

FIG.6

Id., Fig. 6 (color added); *see also id.*, [0018] ("FIG. 6 is a block diagram of the configuration of the command/address/control register buffer 400").

125. For example, Hiraishi discloses that "the command/address/control ***connectors 130*** are terminals for making an electrical ***connection with a memory controller*** via a memory slot" (*Id.*, [0047]) and that "[t]he ***command/address/control register buffer 400 receives the command signal***, ***the address signal, the control signal, and the clock signal*** … that are supplied ***from the command/address/control connectors 130*** through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200." *Id.*, [0060];

see also id. [0097] ("[t]he command/address/control signal that is supplied from the memory controller 12 is input from the input terminal 401."). Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (*i.e.*, command/address/control register buffer 400) is configured to receive system command signals for memory operations via the set of control/address signal lines and a system clock signal via a clock signal line from the memory controller.

126. Hiraishi further discloses that the command/address/control register buffer 400 "receives the ***command signal***, … ***supplied from the command/address/control connectors 130*** through an input terminal 401, ***buffers the signals***, and ***supplies the signals to the memory chips 200***." *Id.*, [0060]; *see also id.* [0097] ("[t]he register circuit 410 is a circuit that buffers the command signal CMD, …, and the ***buffered command signal CMD***, … [is] ***supplied to the memory chip 200*** via the output terminal 402."). Therefore, a Skilled Artisan would have understood that Hiaishi's module control circuit (command/address/control register buffer 400) is configured to output module command signals to the memory devices (200) in response to the system command signals.

127. Hiraishi also discloses that "[a]t the same time, the command/address/control register buffer 400 generates a ***control signal*** … and the

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control signal to be supplied to the data register buffers 300 are output through an output terminal 403." Hiraishi, [0060]. Hiraishi further explains that command/address/control register buffer 400 includes a control signal generating circuit 430 which generates control signals (including DRC) for the data register buffers 300 based on the command/address/control signal supplied by input terminal 401:

> The control signal generating circuit 430 is a circuit that ***generates the control signal DRC*** to be supplied to the data register buffer 300 ***based on the command/address/control signal supplied via the input terminal 401***, of which an operation is performed in synchronization with the internal clock LCLKCA. ***The control signal DRC*** for the data register buffer 300 ***is supplied to the data register buffer 300 via the output terminal 403***. The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404.

Id., [0099]. Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (command/address/control register buffer 400) is configured to output module control signals in response to the system command signals.

128. Hiraishi also discloses that the "clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400. In FIG. 7, a clock signal transferred

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through the command/address/control line L3 is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L5 is represented by a clock signal Clock-Post." *Id.*, [0108]. Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (command/address/control register buffer 400) is configured to receive a system clock signal (Clock-Pre) and output a module clock signal (Clock-Post).

129. Hiraishi also discloses that a memory operation can include a read or a write operation. *See, e.g.*, *id.*, [0122]-[0136]. Figure 11 (annotated below) shows the timing of a read operation, including receiving a read command (red box at "T0") on line CMD(IN) (orange) by the Command/Address/Control Register Buffer (red), and outputting corresponding signals on line CMD(OUT) (orange) to the memory chips (green) and on line CONTROL SIGNAL(OUT) (brown) to the Data Register Buffer (blue). As also shown in these figures, the command and control signals are accompanied by corresponding clock signals (yellow).

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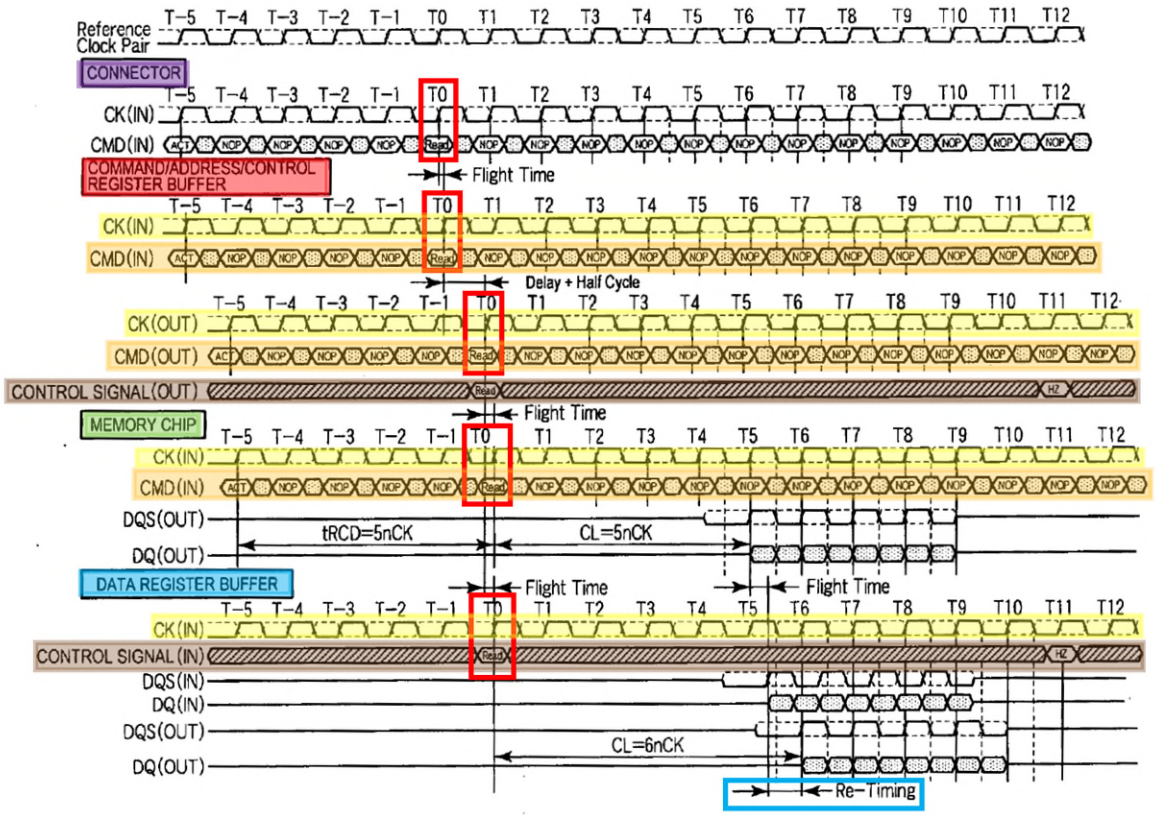


FIG.11

Id., Fig. 11 (annotated). Similarly Figure 12 (annotated below) shows the timing of a write operation, including receiving a write command (red box at "T0") on line CMD(IN) (orange) at the connector (purple) by the Command/Address/Control Register Buffer (red), and outputting corresponding signals on line CMD(OUT) (orange) to the memory chips (green) and on line CONTROL SIGNAL(OUT) (brown) to the Data Register Buffer (blue), the command and control signals being accompanied by corresponding clock signals (yellow):

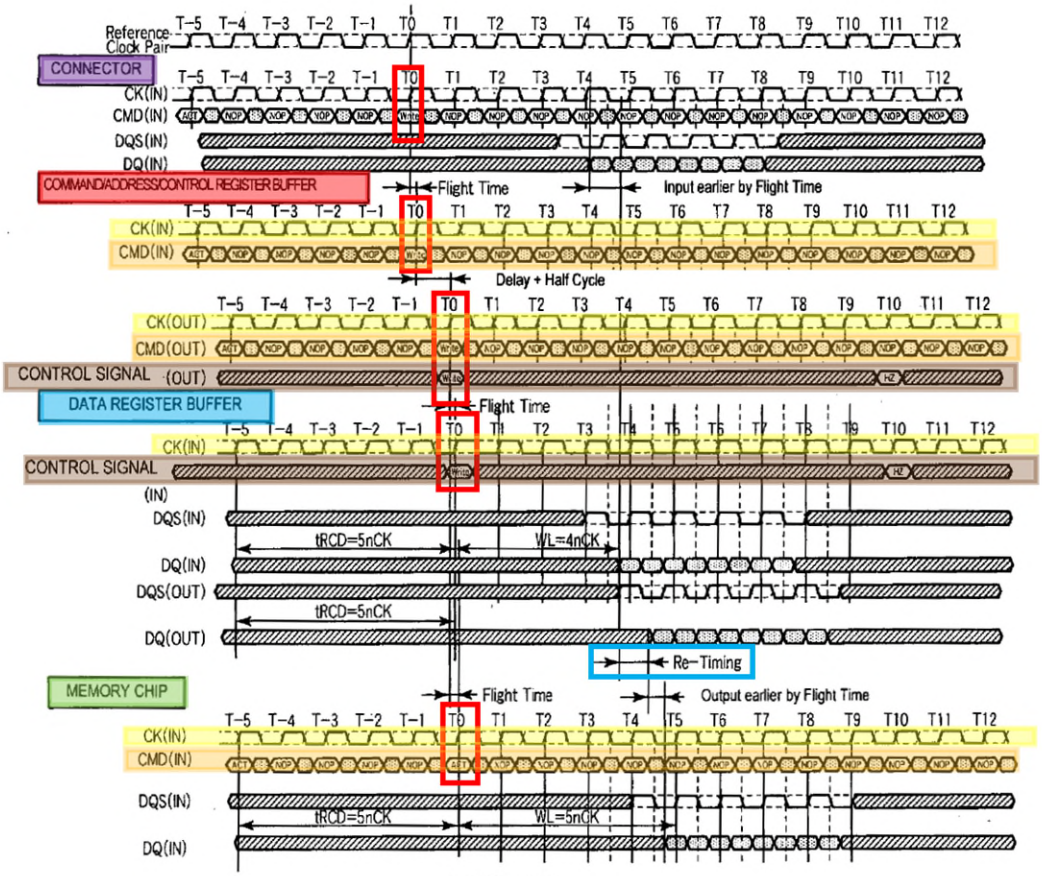


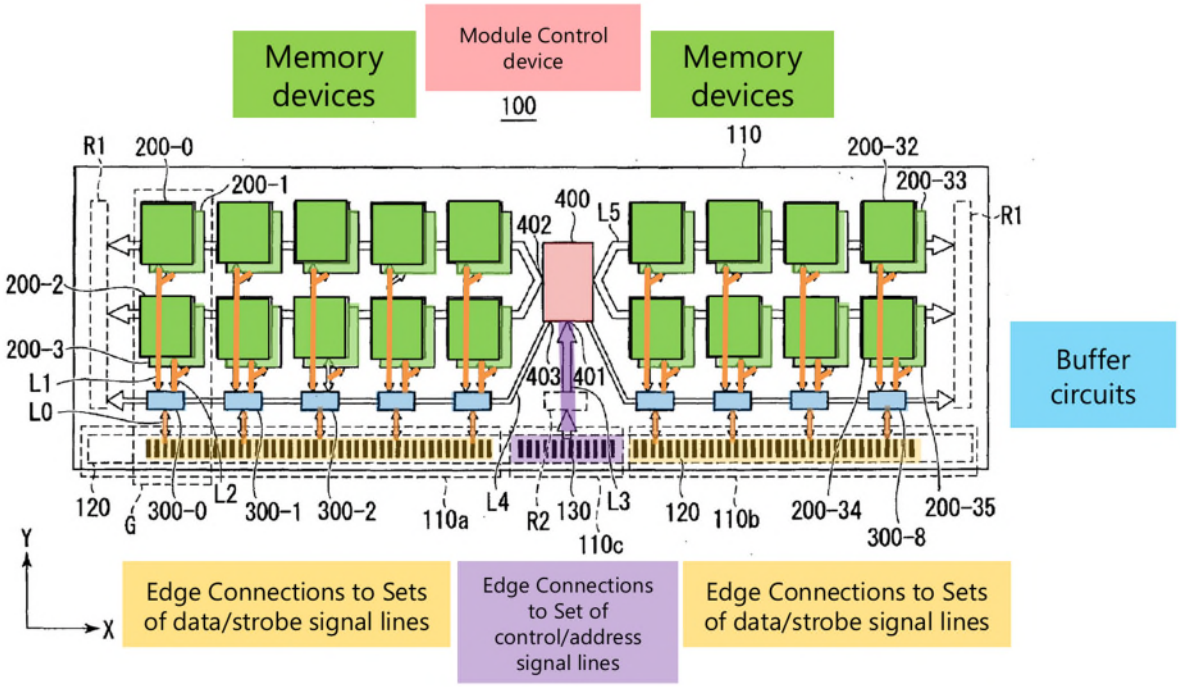
FIG.12

Id., Fig. 12 (annotated). Thus, a Skilled Artisan would have understood that Hiraishi discloses this limitation.

d) 1[c]: "memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines"

130. Hiraishi discloses this limitation. For example, as illustrated by annotated figures 1 and 7 below, Hiraishi discloses "*memory devices* [200-0 to 200-35 (green)] *mounted on the module board and configured to receive the*

module command signals [module command/address/control line L5 (Fig. 7)] *and the module clock signal* [Clock-Post, L5]*, and to perform the memory operations* [such as a write or read operation] *in response to the module command signals* [on line L5], *the memory devices including a plurality of sets of memory devices* [such as a set including memory devices 200-0 to 200-3] *corresponding to respective sets of the plurality of sets of data/strobe signal lines* [the data/strobe lines in the memory bus coupled to L0]."



EX1005 (Hiraishi), Fig. 1 (annotated, "memory chips" in green);

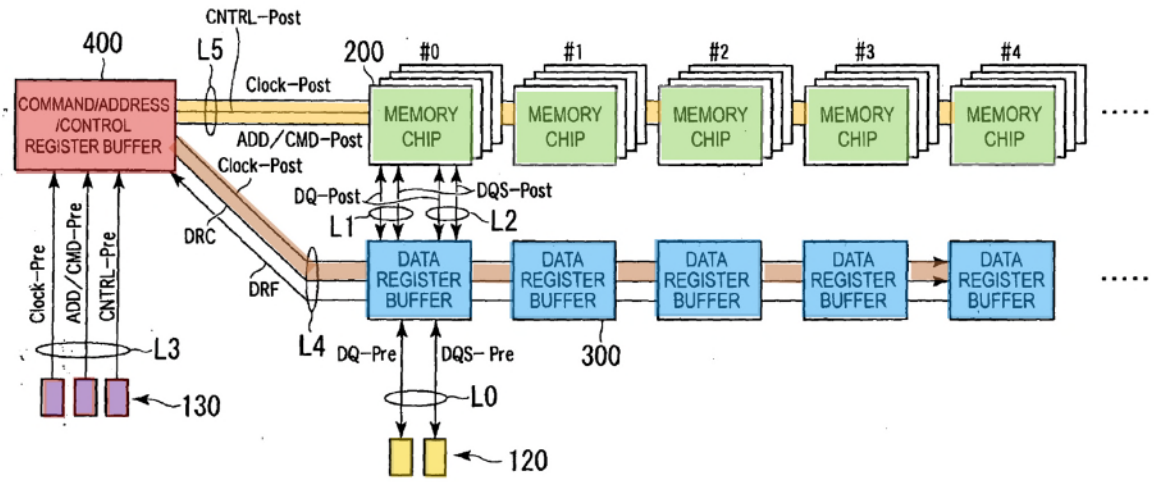


FIG.7

Id., Fig. 7 (annotated, "memory chips" in green).[2]

131. Hiraishi discloses that memory module 100 includes a plurality of memory chips 200 mounted on the module substrate 110:

> As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, ***a plurality***

[2] I note that, in Fig. 1 and Fig. 7, the groups of memory devices and the corresponding data buffers are numbered differently in relation to the module controller. In Fig. 1, the group numbers start at the left side (as group "0") of the module, the farthest away from the module controller in the center. In Fig. 7, the group numbers start to the right of the module controller with group #0 closest to the module controller.

> ***of memory chips 200 mounted on the module substrate 110***, a plurality of data register buffers 300, and a command/address/control register buffer 400.

Id., [0045].

132. Hiraishi discloses that the memory chips 200 are configured to receive the module command signals and the module clock signal, and to perform memory operations in response to the module command signals. For example, Hiraishi discloses that

> An operation of ***the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal*** supplied ***from the command/address/control register buffer 400***.

Id., [0054], see also [0108] ("The clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400."). The memory operation can be, for example, a read operation or a write operation. *See, e.g.*, *id.*, [0122]-[0136], Figs. 11 and 12. For example, Hiraishi discloses:

> The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and ***then outputs them to the memory chip 200***. … The memory chip 200 ***receives the commands ACT and Read, and starts an actual read operation***.

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Id., [0126]-[0127], Fig. 11; *see also* [0133] ("In the write operation, the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data.") and [0136] ("The memory chip 200 receives the write data DQ that is burst output from the data register buffer 300, and writes it in the memory cell array."). Thus, a Skilled Artisan would have understood that the memory chips 200 are configured to perform read and write operations in response to the module command signals. *See also* EX1005 at [0163] and [0170] (disclosing that the memory chips can be DDR3 memory chips), and EX1020 (JESD79-3C, JEDEC standard for DDR3 SDRAM) at 33 (command table including read and write commands), 56-76 (describing read and write operations).

133. Hiraishi discloses that the memory devices include a plurality of sets of memory devices (*e.g.*, a set including memory devices 200-0 to 200-3) corresponding to respective sets of the plurality of sets of data/strobe signal lines (*e.g.*, L0). For example, Hiraishi discloses:

> As shown in FIG. 1, the ***four memory chips 200 constituting a single group*** are connected to one of the data register buffers 300. For example, the ***group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0***. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are ***mounted on the upper side of the module substrate 110*** are connected to the data register buffer 300-0 ***via a data line L1***, and

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> the memory chips 200-2 and 200-3 that are ***mounted on the lower side of the module substrate 110*** are connected to the data register buffer 300-0 ***via a data line L2***. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110.

Id., [0053]; *see also id.* [0056] (describing group G in FIG. 1). That is, Hiraishi discloses that one set of memory devices (200-0 to 200-3) are connected to data register buffer 300-0. In particular, memory devices 200-0 and 200-1 are connected to the buffer 300-0 by data line L1, and memory devices 200-2 and 200-3 are connected to the buffer 300-0 by data line L2. Hiraishi further explains that data buffer 300-0 is, in turn, associated with data line L0 from the edge connectors 120, which comprises a set of data/strobe signal lines:

> As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The ***data connectors 120 and the data register buffer 300 are connected to each other with the data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of ***data transferred through the data line L0 is represented by data DQ-Pre***, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, ***a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre***, and a data

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> strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

Id., [0103]. Thus, a Skilled Artisan would have understood that one set of memory devices (200-0 to 200-3) correspond to one of the sets of data/strobe signal lines (L0, which comprises DQ-pre and DQS-pre). Such a Skilled Artisan would likewise have understood that Hiraishi discloses that each other set of memory devices correspond to other respective sets of data/strobe lines (*e.g.*, as illustrated in Fig. 1, a set for each buffer 300-0 through 300-8). For example, memory devices 200-32 to 200-35 correspond to buffer 300-8 and thus correspond to the DQ and DQS lines from the edge connectors to that buffer (not labeled in Fig. 1).

e) 1[d]: "a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines"

134. Hiraishi discloses this limitation. For example, as illustrated by annotated figures 1 and 7 below, Hiraishi discloses "*a plurality of buffer circuits* [data register buffer circuits 300-0 to 300-8 (blue)] *corresponding to respective sets of the plurality of sets of data/strobe signal lines* [*e.g.*, respective data/strobe signal DQ-Pre and DQS-Pre in L0].

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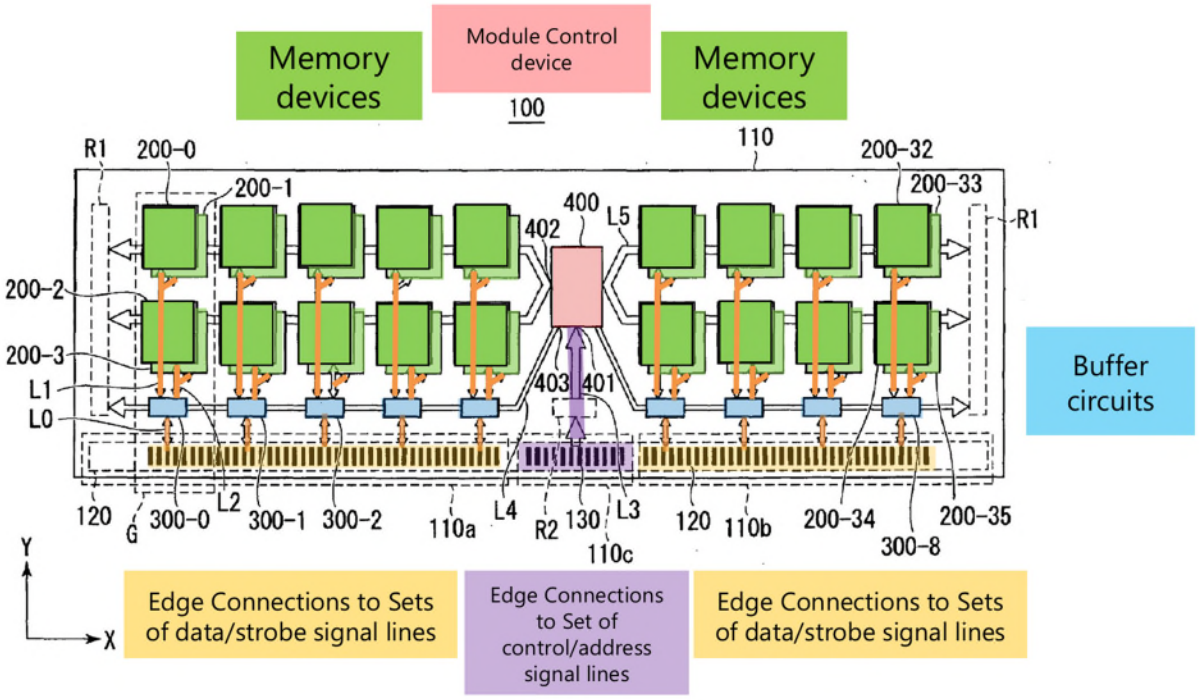

EX1005 (Hiraishi), Fig. 1 (annotated and color added, showing buffer circuits in blue);

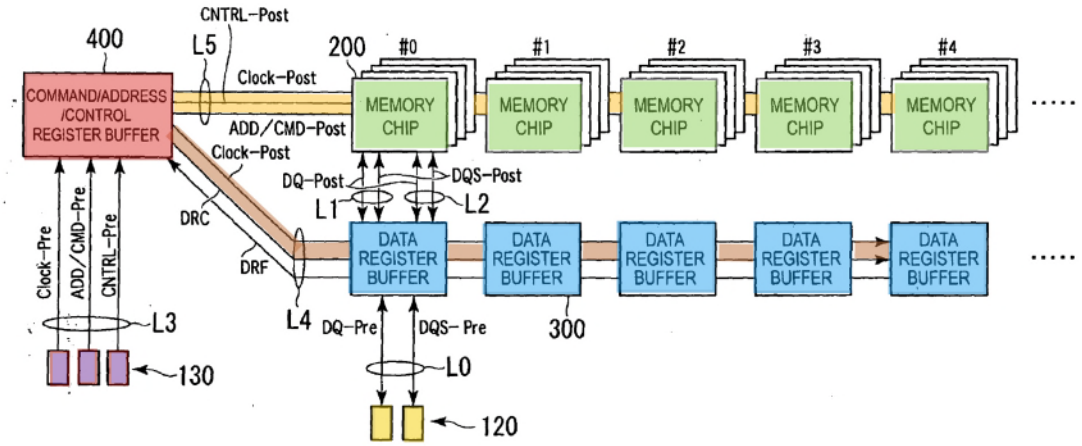

FIG.7

Id., Fig. 7 (annotated and color added, showing buffer circuits in blue and data line L0 comprising DQ and DQS signals).

135. Hiraishi discloses that the memory module includes a plurality of data register buffers (shown in blue in the annotated figures above):

> As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, ***a plurality of data register buffers 300***, and a command/address/control register buffer 400.

Id., [0045]. Hiraishi explains that each of nine buffers is allocated to four memory chips, such that each data register buffer buffers read and write data that is transferred via line L0 to data lines L1 and L2 and *vice versa*:

> A ***single data register buffer 300 is allocated for every four memory chips 200***, as described above, so that ***nine data register buffers 300 are arranged along the X direction***, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred ***via a data line L0*** and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to ***the data line L0***. The data line L0 is also formed inside the module substrate 110.

Id., [0055]. Hiraishi further explains that a single data register buffer, data connectors 120, and the four memory chips corresponding thereto constitute a

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group (G, shown in Figure 1), such that a relative position relationship between each of the buffers and corresponding four memory chips is constant in all groups:

> [T]he ***single data register buffer 300, the data connectors 120 and the four memory chips 200 corresponding to the data register buffer 300 constitute a group G***. The memory chips 200, the data register buffer 300, and the data connectors 120 included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, ***a relative positional relationship between each of the data register buffers 300 and corresponding four memory chips 200 becomes constant in all the groups G.***

Id., [0056].

136. Figure 5 of Hiraishi is a schematic block diagram of a data register buffer 300. *Id.*, [0017].

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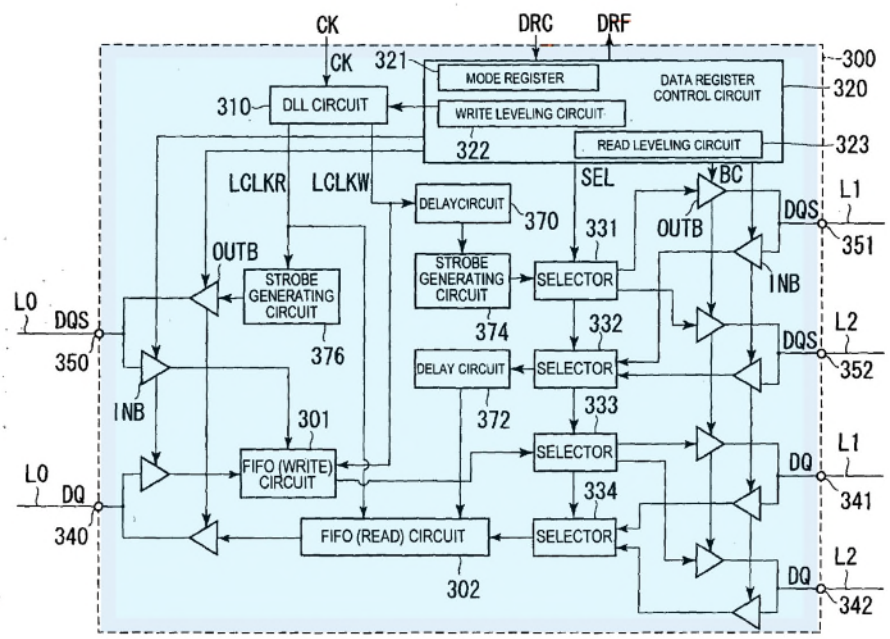

FIG.5

Id., Fig. 5. Hiraishi explains, with reference to Fig. 5, that the data register buffer 300 is coupled between respective sets of data/strobe signal lines:

> As shown in FIG. 5, the data register buffer 300 includes a FIFO (Write) circuit 301 and a FIFO (Read) circuit 302. The FIFO (Write) circuit 301 ***buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350***. The FIFO (Read) circuit 302 buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352. A strobe generating circuit 376 ***generates a data strobe signal DQS to be supplied to the data connectors 120***, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310. A strobe generating circuit 374 generates a data strobe signal DQS to be

> supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.

Id., [0084].

137. Hiraishi further discloses, with reference to Fig. 7, that the buffer circuits intervene between the data connectors 120 and the memory chips 200, such that the data connectors 120 are connected to the buffer via data line L0 (which comprises data and strobe signals DQ-pre and DQS-pre), and the buffer is connected to the memory chips via data lines L1 or L2 (which each comprise data and strobe signals DQ-post and DQS-post):

> As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. ***The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, ***a plurality of data transferred through the data line L0 is represented by data DQ-Pre***, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, ***a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre***, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

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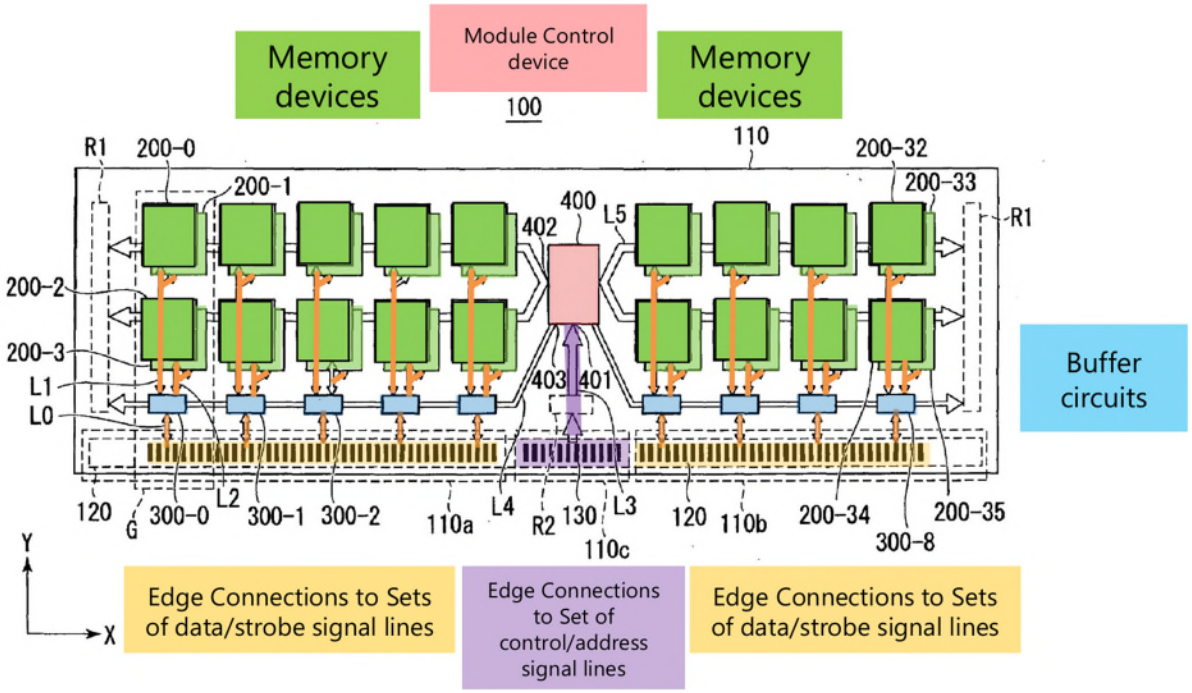
Id., [0103]. Accordingly, a Skilled Artisan would have understood that Hiraishi's buffer circuits correspond to respective sets of the plurality of sets of data/strobe signal lines.

f) 1[e]: "wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal"

138. Hiraishi discloses this limitation to a Skilled Artisan in light of Butt. For example, as illustrated by annotated Figures 1 and 7 below, Hiraishi discloses that "*each respective buffer circuit of the plurality of buffer circuits is mounted on the module board* [data register buffer circuits 300-0 to 300-8, blue]*, coupled between a respective set of data/strobe signal lines* [L0, including lines DQ-Pre and DQS-Pre] *and a respective set of memory devices* [such as memory chips 200-0 to 200-3, connected by data lines L1 and L2, including lines DQ-Post and DQS-Post, to the respective buffer circuit 300]."



EX1005 (Hiraishi), Fig. 1 (annotated and color added, showing buffer circuits in blue and memory devices in green);

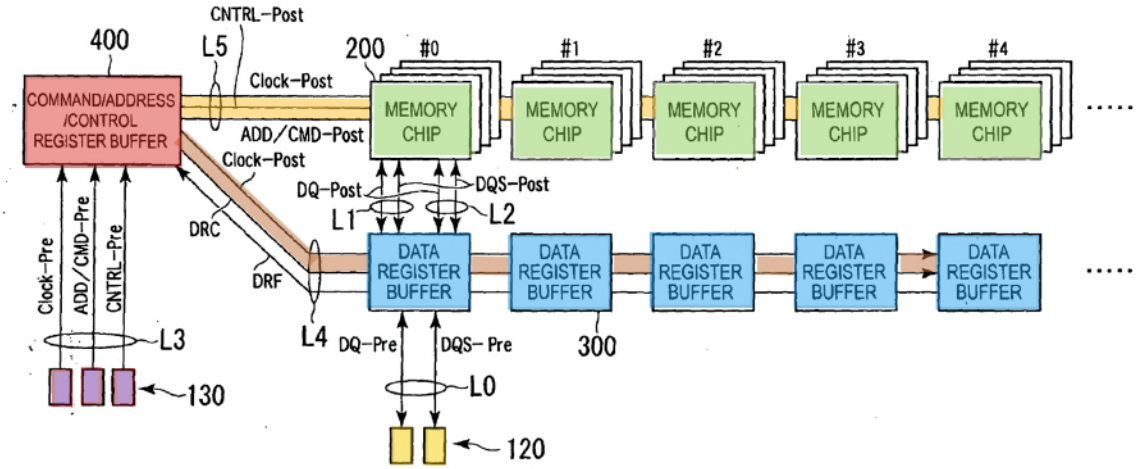


FIG.7

Id., Fig. 7 (annotated and color added, showing buffer circuits in blue, memory devices in green, and data lines L0, L1, and L2 comprising DQ and DQS signals).

139. For example, as explained above in connection with limitation 1[d], Hiraishi discloses that each buffer circuit is mounted on the module board and coupled between a respective set of data/strobe signal lines and a respective set of memory devices. *See supra* ¶¶ 134-137 (limitation 1[d]); EX1005 (Hiraishi), [0045], [0055]-[0056], [0084-85], [0103]. For example, Hiraishi discloses that each of the nine buffers is allocated to four memory chips, such that each data register buffer buffers read and write data that is transferred via line L0 to data lines L1 or L2 and *vice versa*. *See* EX1005 (Hiraishi), [0055]. Hiraishi discloses that data line L0 comprises data and strobe signals DQ-pre and DQS-pre, and data lines L1 or L2 each comprise data and strobe signals DQ-post and DQS-post. *See id.*, [0103].

140. Hiraishi also discloses, as illustrated by annotated Figs. 6 and 7 above, and annotated Fig. 5 below, that each respective buffer circuit is "*configured to receive the module control signals* [including DRC] *and the module clock signal* [CK (Clock-Post in Fig. 7)]."

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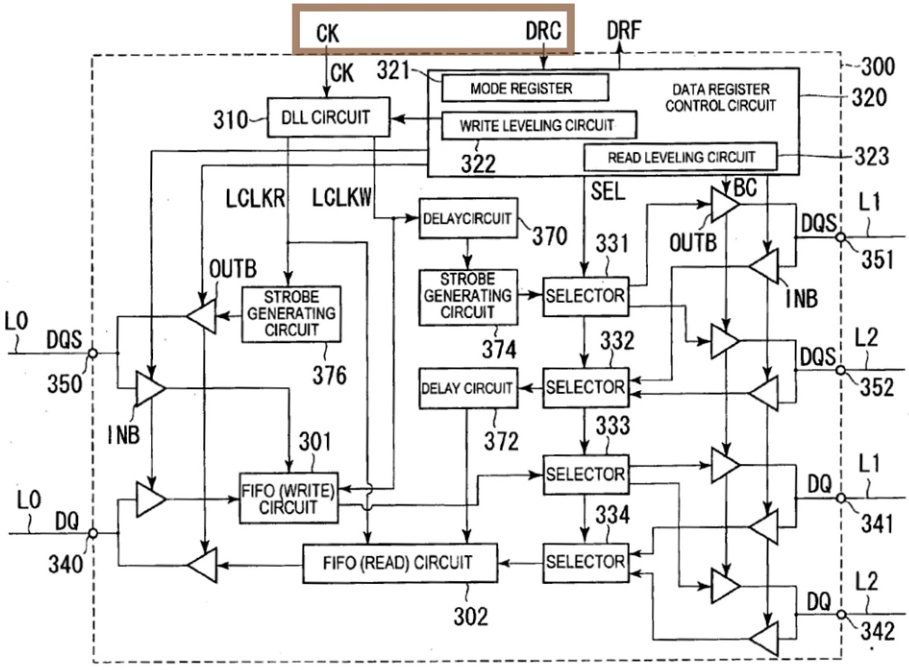

FIG.5

EX1005 (Hiraishi), FIG. 5 (annotated).

141. For example, Hiraishi discloses that the operation of the data register buffer 300 is controlled based on control signals supplied by the command/address/control register buffer 400:

> An operation of the data register buffer 300 is controlled ***based on the control signal supplied from the command/address/control register buffer 400***.

Id., [0058]. Hiraishi further discloses that the data register buffer 300 receives the module clock signal from the command/address/control register buffer 400:

> The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR ***based on the clock signal CK that is supplied from the command/address/control register buffer 400***,

> having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310. … The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 based on a ***control signal DRC that is supplied from the command/address/control register buffer 400***. Specifically, the data register control circuit 320 ***controls operations of an input buffer INB and an output buffer OUTB*** by generating a buffer control signal BC, and at the same time, ***controls operations of selectors 331 to 334 by generating a select signal SEL***. Contents of controlling the output buffer OUTB include, for example, an adjustment of output impedance and an on/off control of an ODT operation. It is selected based on a set content in a mode register 321 that is included in the data register control circuit 320 whether to use the ODT function.

Id., [0087]-[0088].

142. Hiraishi, in view of Butt, also discloses to a Skilled Artisan "*the each respective buffer circuit* [300] *including a data path* [orange in annotated Fig. 5 below for read and write operations] *corresponding to each data signal line in the respective set of data/strobe signal lines* [L0, including lines DQ and DQS (DQ-Pre and DQS-Pre in Fig. 7)]."

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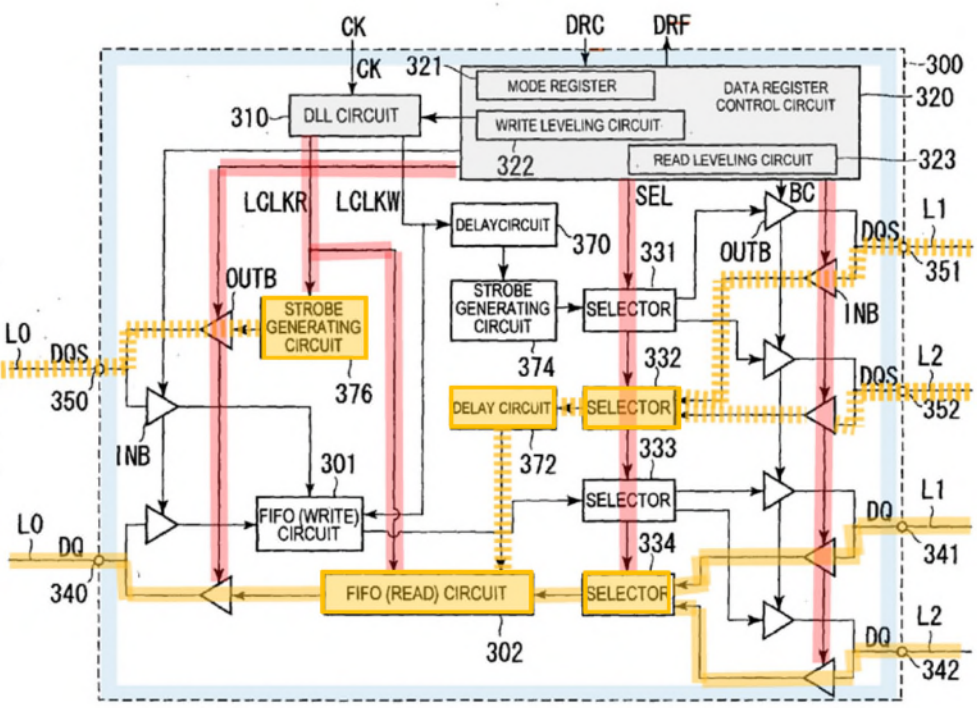
CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
INB
STROBE GENERATING CIRCUIT
376
STROBE GENERATING CIRCUIT
SELECTOR
374
332
L0
DQS
350
DELAY CIRCUIT
SELECTOR
L2
DQS
352
INB
301
372
333
SELECTOR
L1
L0
DQ
FIFO (WRITE) CIRCUIT
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOF
L2
DQ
302
342

FIG.5

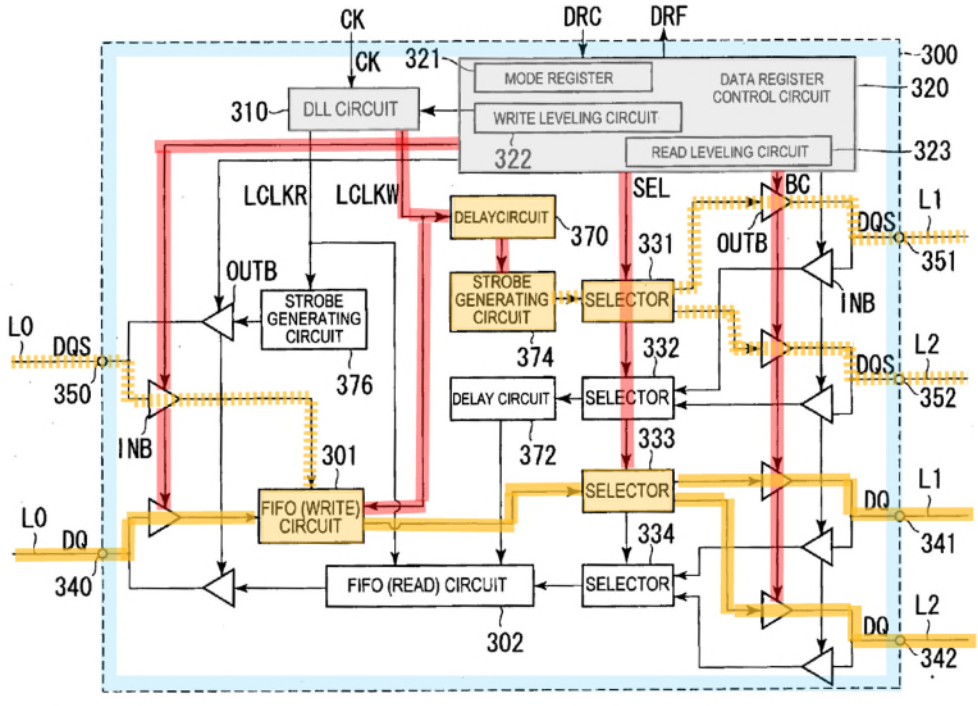
CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
INB
STROBE GENERATING CIRCUIT
376
STROBE GENERATING CIRCUIT
SELECTOR
374
332
L0
DQS
350
DELAY CIRCUIT
SELECTOR
L2
DQS
352
INB
301
372
333
SELECTOR
L1
L0
DQ
FIFO (WRITE) CIRCUIT
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
302
342

FIG.5

143. For example, Hiraishi explains that, during memory read and write operations, the data is buffered in respective FIFO circuits between, on one hand, the data/strobe terminals 340 and 350 coupled to the memory controller (to the left in Fig. 5 above) and, on the other hand, the data/strobe terminals 341/342 and 351/352 coupled to the memory devices (to the right in Fig. 5 above):

> As shown in FIG. 5, the data register buffer 300 includes a FIFO (Write) circuit 301 and a FIFO (Read) circuit 302. ***The FIFO (Write) circuit 301 buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350. The FIFO (Read) circuit 302 buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352.*** A strobe generating circuit 376 ***generates a data strobe signal DQS to be supplied to the data connectors 120***, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310. A strobe generating circuit 374 ***generates a data strobe signal DQS to be supplied to the memory chip 200***, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.

EX1005 (Hiraishi), [0084]. Thus, Hiraishi discloses that each respective buffer circuit receives the data and strobe signals and buffers into a respective FIFO the data signal corresponding to each data signal line in the respective set of data/strobe signal lines.

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144. Similarly, Butt discloses that, in a circuit coupled between a memory controller and the memory devices, data signals are sampled using corresponding strobe signals and the sampled data is buffered in a FIFO. EX1029 (Butt), Fig. 2 and Fig. 3A (reproduced below, annotated).

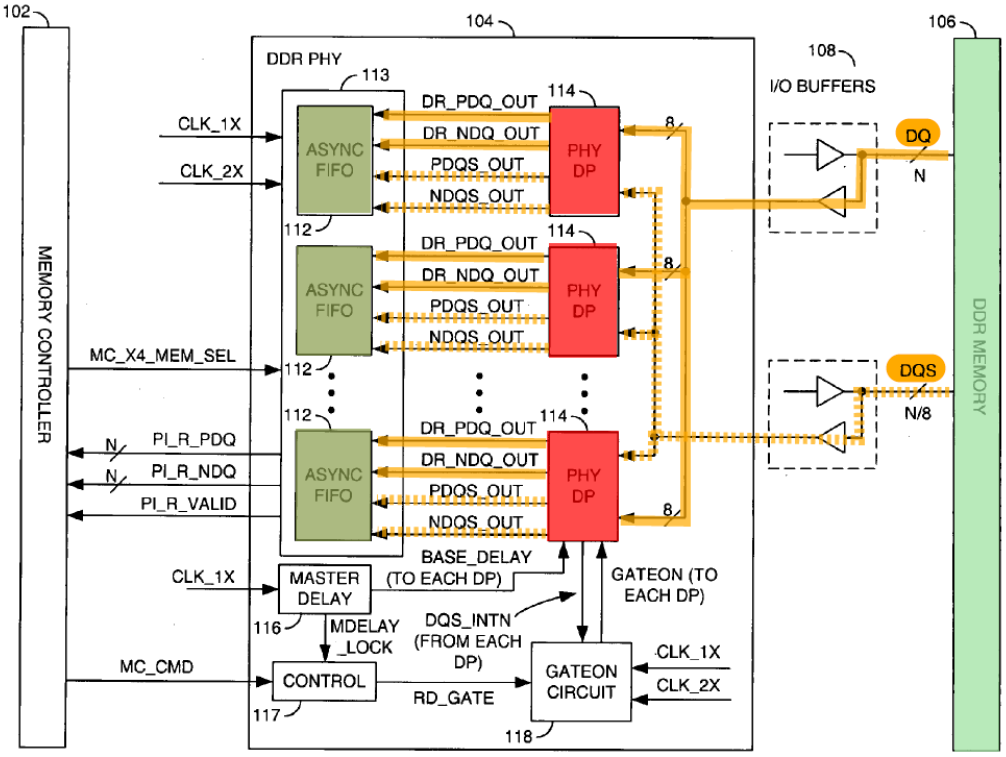

FIG. 2

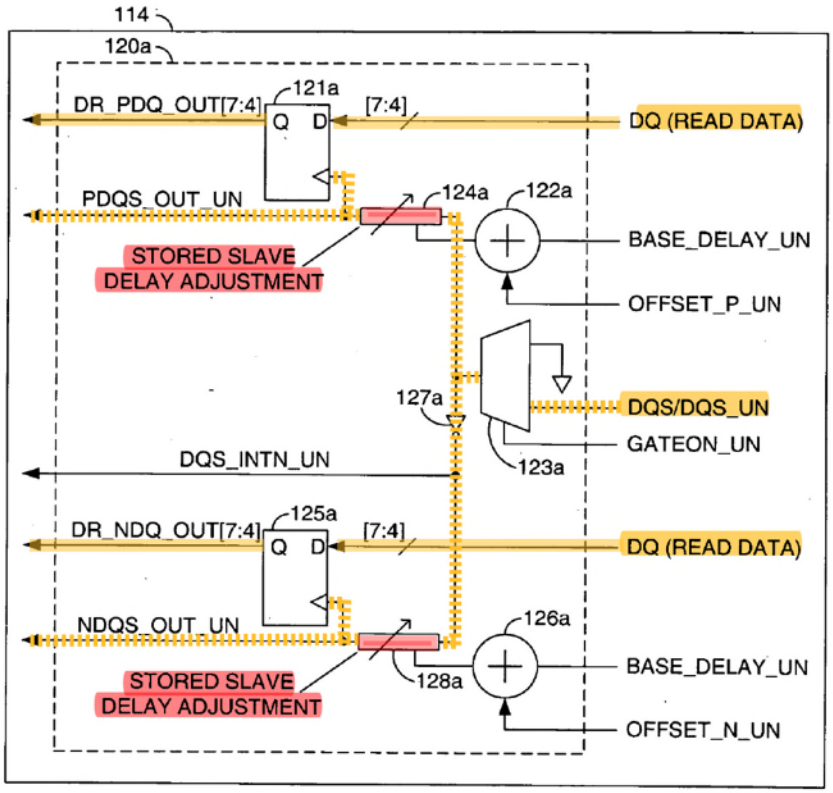

FIG. 3A

Butt also discloses that such a circuit is an implementation of a "data path." EX1029 (Butt), [0017] ("Each of the physical read ***datapaths 114*** may be configured to ***receive*** (i) a respective portion of the read ***data signals DQ*** from the DDR memory 106, (ii) a respective read ***data strobe signal or signals DQS*** associated with the respective portion of the received read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118. Each of the physical read ***datapaths 114 may communicate with a corresponding one of the asynchronous FIFOs*** 112 via a number of signals (e.g., DR_PDQ_OUT, DR_NDQ_OUT, PDQS_OUT, and NDQS_OUT)."). Therefore,

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a Skilled Artisan would have understood from the disclosure of Butt that Hiraishi's data register buffer 300 includes "data paths" (orange) using data strobe signals to sample the data and buffer the sampled data in respective FIFO circuits.

145. Indeed, Hiraishi and Butt are analogous art to the 608 Patent, as each is directed to solving the problem of accurate timing of data transmissions for memory transactions. EX1001 at Title (Memory module with timing-controlled data paths in distributed data buffers); EX1005 (Hiraishi) [0140] ("Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation."); EX1029 (Butt) [005] ("The present invention concerns a method for calibrating a data valid window comprising the steps of: (A) setting a base delay of one or more datapaths to a predetermined value, (B) determining an optimum offset delay value for each of the one or more datapaths based upon actual memory accesses and (C) delaying a read data strobe signal based upon the base delay and the optimum offset delay value for each of the one or more datapaths."). Therefore, a Skilled Artisan would have understood and would have

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been motivated to implement the techniques used in the data paths of Butt in Hiraishi's data register buffer.

146. For example, a Skilled Artisan would have understood that both Hiraishi's data register buffer and Butt's interface circuit communicates data and corresponding strobe signals to and from the memory devices and samples the data signals using the strobe signal and buffers the data samples in a FIFO. Therefore, a Skilled Artisan would have been motivated to determine an optimum offset delay for the data paths as taught by Butt in order to optimize the data capture in Hiraishi's data register buffer as well. EX1029 (Butt), Abstract ("A method for calibrating a data valid window including the steps of: (A) setting a base delay of one or more datapaths to a predetermined value, (B) determining an optimum offset delay value for each of the one or more datapaths based upon actual memory accesses and (C) delaying a read data strobe signal based upon the base delay and the optimum offset delay value for each of the one or more datapaths.") and [0034] ("A receiving device implementing the present invention may realize an optimal timing for the read data strobe signal DQS.").

147. Thus, Hiraishi in view of Butt discloses to a Skilled Artisan that each respective buffer circuit includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines.

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148. Hiraishi in view of Butt also discloses, as illustrated by annotated Fig. 5 above, that each respective buffer circuit includes "*a command processing circuit* [including Data Register Control Circuit 320 and logic in DLL Circuit 310] *configured to decode the module control signals* [including DRC] *and to control the data path in accordance with the module control signals* [such as DRC, received by Data Register Control Circuit 320] *and the module clock signal* [CK, received by DLL circuit 310]," for example by setting the selectors 331-334, activating the correct input and output buffer circuits INB and OUTB, and controlling the FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, delay circuits 370 and 372, and Strobe Generating Circuits 374 and 376, and generating local clock signals such as LCLKR and LCLKW by the DLL circuit in accordance with the module clock signal CK.

149. For example, Hiraishi discloses that the operation of the data register buffer 300 is controlled based on signals supplied by the command/address/control register buffer 400, including module control signals (e.g., DRC), and module clock signal (CK). For example, Hiraishi discloses that:

> An operation of the data register buffer 300 is controlled ***based on the control signal supplied from the command/address/control register buffer 400***.

Id., [0058]. More specifically, Hiraishi discloses that the Data Register Control Circuit 320 receives and decodes the module control signal (DRC) and controls the

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data path accordingly, including the operation of input and output buffers and selectors between different terminals:

> The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 ***based on a control signal DRC*** that is supplied from the command/address/control register buffer 400. Specifically, the data register control circuit 320 ***controls operations of an input buffer INB and an output buffer OUTB*** by generating a buffer control signal BC, and at the same time, ***controls operations of selectors 331 to 334*** by generating a select signal SEL.

EX1005 (Hiraishi), [0088]. "The selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals 341 and 342. The selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302. The selectors 331 and 332 perform the similar functions as those of the selectors 333 and 334, respectively. Specifically, the selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. … The selector 331 supplies the data strobe signal DQS that is supplied from the strobe generating circuit 374 to either one of the input/output terminals 351 and 352." *Id*., [0091]. Hiraishi also discloses that the DLL Circuit 310 receives the module clock signal (CK), and controls the data

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path accordingly, e.g., by controlling the operation timing of the FIFO (Write) circuit and/or FIFO (Read) circuit:

> An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310. An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310. The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR ***based on the clock signal CK that is supplied from the command/address/control register buffer 400***, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310.

Id., [0087]. Furthermore, a Skilled Artisan would have been motivated to implement the data path control techniques of Butt in Hiraishi's data buffer as discussed above. For example, the delay circuit 372 for the input read strobe can be controlled to apply a delay that ensures that data from different memory devices are properly captured as taught by Butt. EX1029 (Butt), Abstract, [0034].

150. A Skilled Artisan would have understood from the above disclosure that, for example in connection with a read operation from memory devices on data line L1, the input buffers on terminals 351 and 341 are activated, the selectors 332 and 334 respectively select the lines from terminals 351 and 341, and the output

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buffers to terminals 350 and 340 are also activated. Thus, the data register buffer includes a command processing circuit (including Data Register Control Circuit 320 and logic in DLL Circuit 310) that decodes the module control signals and controls the data path (for example, for transmitting data and strobe signals associated with a read operation from a memory on data line L1) in accordance with the module control signals (DRC) and the module clock signal (CK). Similarly, for a read operation from memory devices on data line L2, the input buffers on terminals 352 and 342 are activated, and the selectors 332 and 334 respectively select the lines from terminals 352 and 342. I also note that a Skilled Artisan would have understood that each of the read selectors 332 and 334 can select only one of the two connected input buffers. EX1022 (Stone) at 89-90 (explaining driving two signals on the same line leads to bus conflicts which result in failure and may damage the circuitry).

151. Similarly for a write operation to memory devices on data line L1, the input buffers on terminals 350 and 340 are activated, the write selectors 331 and 333 respectively select the lines to terminals 351 and 341, and the output buffers to terminals 351 and 341 are also activated. Thus, the data register buffer includes a command processing circuit (including Data Register Control Circuit 320 and logic in DLL Circuit 310) that decodes the module control signals and controls the data path (for example, for transmitting data and strobe signals associated with a write

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operation to a memory on data line L1) in accordance with the module control signals (DRC) and the module clock signal (CK). Similarly, for a write operation from memory devices on data line L2, the output buffers on terminals 352 and 342 are activated, and the write selectors 331 and 333 respectively select the lines from terminals 352 and 342.

g) 1[f]: "wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals"

152. Hiraishi in view of Butt discloses this limitation to a Skilled Artisan. For example, as illustrated by annotated Figures 5 and 13 of Hiraishi below, Hiraishi discloses to a Skilled Artisan that "*the data path* [orange] *corresponding to the each data signal line includes at least one tristate buffer* [*e.g.*, output buffers OUTB and input buffers INB] *controlled by the command processing circuit* [including Data Register Control Circuit 320 and logic in DLL Circuit 310] *and a delay circuit* [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] *configured to delay a signal through the data path* [e.g., during a read or write operation] *by an amount determined by the command processing circuit* [e.g., determined during the Read/Write Leveling step S4 between the memory devices

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and the data buffer] *in response to at least one of the module control signals* [*e.g.*, DRC]." As discussed above, a Skilled Artisan would have understood from the disclosure of Butt that Hiraishi's data register buffer includes data paths and been motivated to implement Butt's data path techniques in Hiraishi's data register buffer. *Supra* at ¶¶144-147.

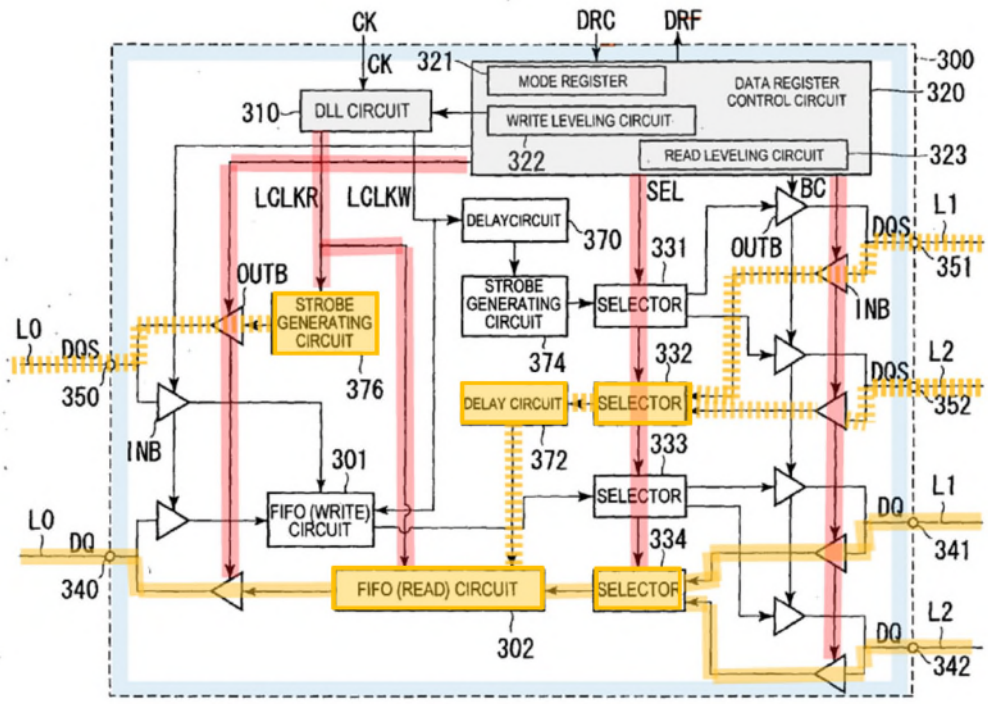

FIG.5

EX1005 (Hiraishi), Fig. 5 (annotated to show signal paths for a read operation).

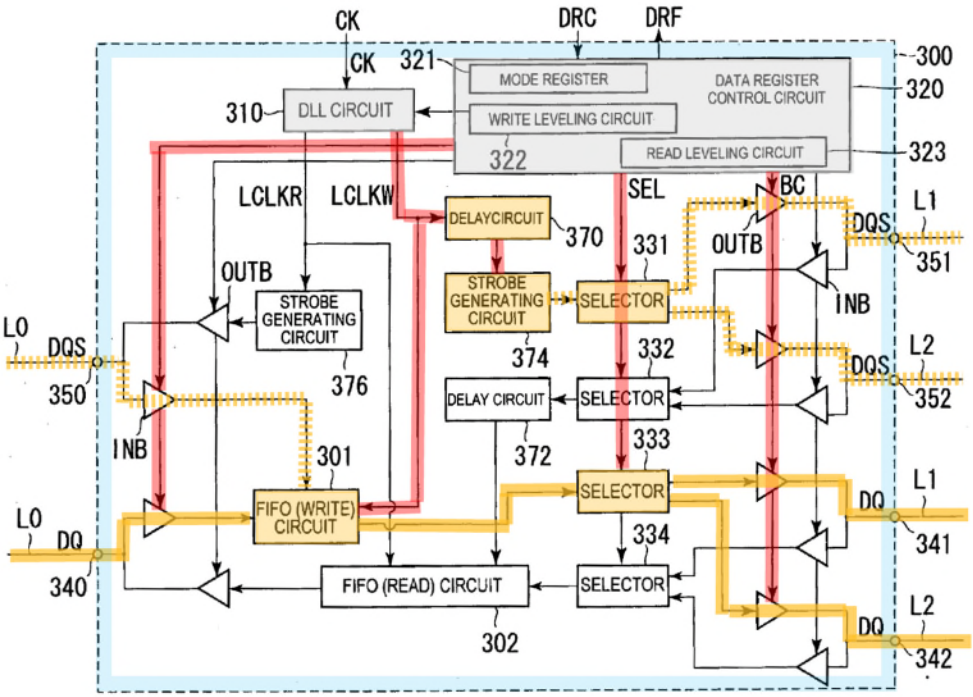

FIG.5

EX1005 (Hiraishi), Fig. 5 (annotated to show signal paths for a write operation).

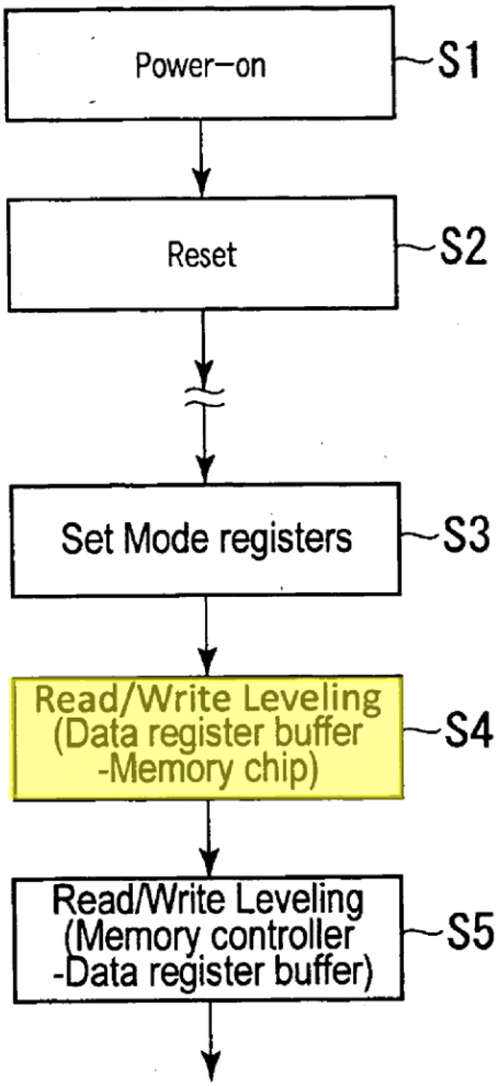

FIG.13

EX1005 (Hiraishi), Fig. 13 (annotated to highlight the S4 step for Read/Write Leveling between Data register buffer and Memory chip).

153. With respect to the requirement that "*the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the*

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command processing circuit," Hiraishi discloses that the "data register control circuit 320" controls several tri-state buffers in the data path, including, for example, buffers OUTB and INB shown in Fig. 5. Hiraishi discloses that:

> The ***data register control circuit 320 is a circuit that controls the operation of the data register buffer*** 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400. Specifically, the ***data register control circuit 320 controls operations of an input buffer INB and an output buffer OUTB*** by generating a buffer control signal BC, and at the same time, controls operations of selectors 331 to 334 by generating a select signal SEL.

EX1005 (Hiraishi), [0088]. Thus, a Skilled Artisan would have understood that these buffers are "controlled by the command processing circuit" (e.g., including data register control circuit 320).

154. A Skilled Artisan would have understood that these OUTB and INB buffers are tri-state buffers for several reasons. First, Fig. 5 depicts these buffers using the commonly accepted symbol for tri-state buffers (a triangle with three connections). *See, e.g.*, EX1022 (Stone) at 68 ("The drivers commonly used for bus systems are tri-state drivers that have a low, high, and off (or high-impedance) mode of operation."), fig. 2.23; *id.* at 74 ("The7424X family … have tri-state drivers…"), fig. 2.28 (showing variations on using two tri-state buffers to implement a bidirectional buffer, reproduced below in part).

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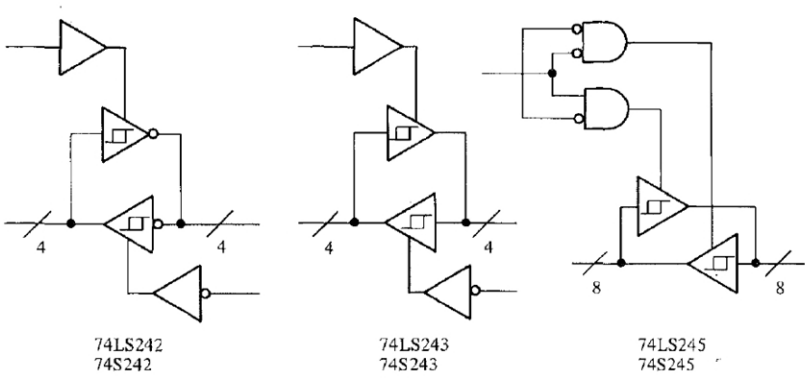

FIGURE 2.28 Drivers and receivers (continued on next page).

A Skilled Artisan would have also understood that bidirectional lines for interfacing memory chips, such as the DQ and DQS lines in Hiraishi, are controlled by such tristate buffers. *Id*. at 133, fig. 4.7 (showing separate tristate buffers for interfacing memory chips to bidirectional data lines, reproduced below).

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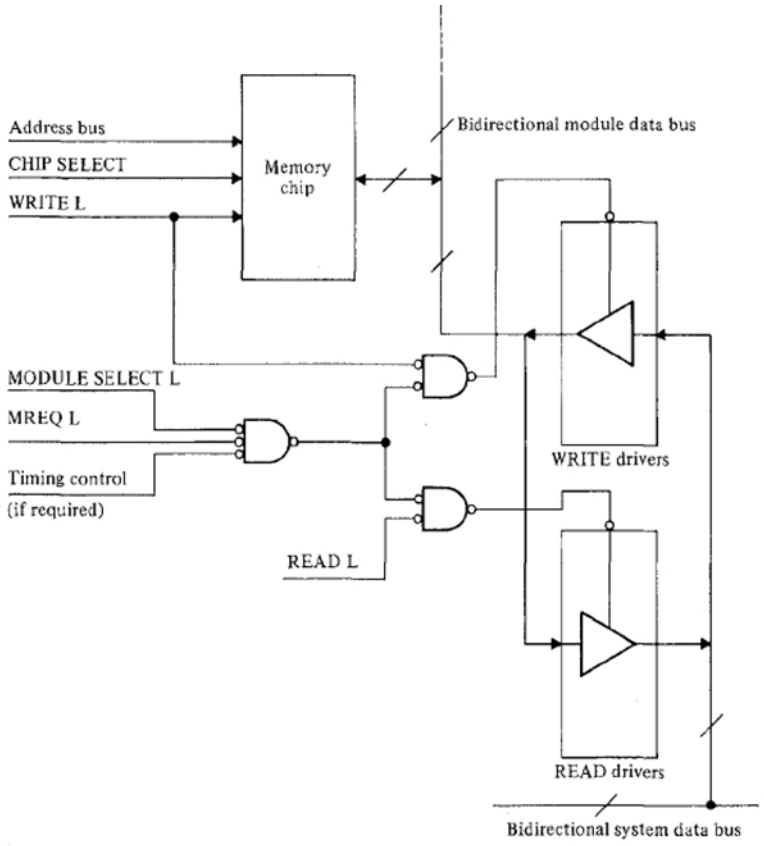

FIGURE 4.7 Tri-state driver control for interfacing memory chips to bidirectional data lines.

Additionally, Hiraishi discloses that the INB and OUTB tristate buffers are activated for an "activation timing" which can be adjusted. *Id*., [0151] ("The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an ***adjustment of an activation timing of the input buffer circuit INB*** and the like."). A Skilled Artisan would have understood that this is the hallmark of a tri-state buffer. In other words, Hiraishi describes OUTB and INB as buffers with an enable input that controls whether the primary input is passed to its output or not, such that when the enable input is low, the output is a high impedance state. A Skilled Artisan would

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have recognized that this is describing a tri-state buffer. *See, e.g.*, EX1022 (Stone) at 68 ("tri-state drivers . . . have a low, high, and off (or high-impedance) mode of operation"); *id.* at 117 ("microprocessors are designed with tri-state drivers on the address and data lines").

155. With respect to the limitation of "*delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals*," I note that the claim language is ambiguous as to whether "*in response to at least one of the module control signals*" modifies the term "*to delay*" or "*determined*." This ambiguity, however, is not relevant here, because Hiraishi discloses both interpretations for the reasons discussed below. For example, Hiraishi's data register buffer 300 determines delays through the data path for read and write operations by respective read and write leveling operations during initialization in response to control signals from the command/address/control register 400, and applies those delays on the data/strobe signals for read and write operations during normal operation in response to read and write commands received from the command/address/control register 400. These operations are discussed below in detail.

156. Hiraishi discloses that the data and strobe signals are buffered by the data register buffer 300, thus the timing is off between the DQ-pre/DQS-pre and

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DQ-post/DQS-post (where DQ-pre and DQS-pre are the data/strobe signals between memory controller and buffer, and DQ-post and DQS-post are the data/strobe signals between the buffer and the memory device):

> Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post.

EX1005 (Hiraishi), [0104]. Accordingly, Hiraishi discloses that it is necessary to separately perform a timing adjustment between the memory chips 200 and the data register buffer 300 (step S-4 in Fig. 13) and between the data register buffer 300 and the memory controller (step S-5 in Fig. 13):

> Therefore, in the present embodiment, it is ***required to perform a timing adjustment*** between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner. Details on the timing adjustments will be described later.

Id. As discussed above, Hiraishi in combination with Butt discloses data paths and their control in the data buffers. *Supra* at ¶¶144-147. Thus, a Skilled Artisan would have understood from the combined disclosure of Hiraishi and Butt that the timing of both the data (DQ) and strobe (DQS) signals are adjusted in the data paths of the data buffers. A Skilled Artisan would have also understood that such a

timing adjustment have to maintain synchronization, including phase relations, between the data and strobe signals in order to interface properly in a DDR SDRAM environment. For example, Butt explains that a "double data rate (DDR) synchronous dynamic random access memory (SDRAM) interface receives aligned data (DQ) and read data strobe (DQS) signals from a DDR SDRAM device. The DDR SDRAM interface is responsible for providing the appropriate DQ-DQS relationship." EX1029 at [0003]. Thus, a Skilled Artisan would have understood from, and been motivated by the disclosure of, Butt to implement Hiraishi's data buffers such that the timing of both the data (DQ) and strobe (DQS) signals through the data paths is adjusted in a way that "the appropriate DQ-DQS relationship" is maintained.

157. Hiraishi's S-4 step includes both read and write leveling between the data register buffer and the memory chips 200. *See* EX1005 (Hiraishi), [0090] ("Furthermore, the data register control circuit 320 includes a write leveling circuit 322 and a read leveling circuit 323. The write leveling circuit 322 is a circuit for ***performing a write leveling operation***, and the read leveling circuit 323 is a circuit for ***performing a read leveling operation***."); [0140] ("Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The ***leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a***

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signal. The ***adjustment of the write timing is performed by a write leveling operation***, and the ***adjustment of the read timing is performed by a read leveling operation***").

158. As explained below, Hiraishi's of S-4 leveling is performed such that a "*delay circuit [is] configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.*"

159. For example, Hiraishi discloses that the S-4 write leveling operation is performed during initialization "to adjust a write timing … in consideration of a propagation time of a signal." EX1005 (Hiraishi), [0140]. The data register circuit 300 includes a write leveling circuit 322 for performing the write leveling operation to determine delays for write data and strobe signals such that the write data and strobe signals arrive at corresponding memories in synchronization with their local clocks. *Id*. at [0090], [0142], Fig. 5. A Skilled Artisan would have understood that, because such a write leveling operation is performed during initialization, the data register circuit 300 is instructed to perform this write leveling to determine the write delays in response to module control signals, including DRC signals. *Id*. at [0088] ("The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer

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400."). For example, Hiraishi discloses that the "control signal DRC includes signals such as … a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like." *Id*. at [0100]. A Skilled Artisan would have understood that such mode switching and mode register setting commands can be used during initialization to perform write leveling operations by the data register buffers to determine the write delays. Indeed, a Skilled Artisan would have understood that the memory chips also have to be put in a write-leveling mode by mode register set commands to perform write leveling operations. EX1020 (JESD79-3C), 43 ("DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low'"). In response to the write leveling mode register set command, the memory device performs specific operations, including providing feedback, on the DQ data lines, of its local clock signal sampled at the rising edge of the received data strobe DQS signal. *Id*., 42. A Skilled Artisan would have understood that Hiraishi's write leveling circuit 322 is also activated by a corresponding module control signal to process this feedback from the memories during the S-4 write leveling in order to determine the write delays. Therefore, a Skilled Artisan would have been motivated to use Hirashi's mode switching and mode register setting control signals to have the data register buffer also perform the write leveling operation.

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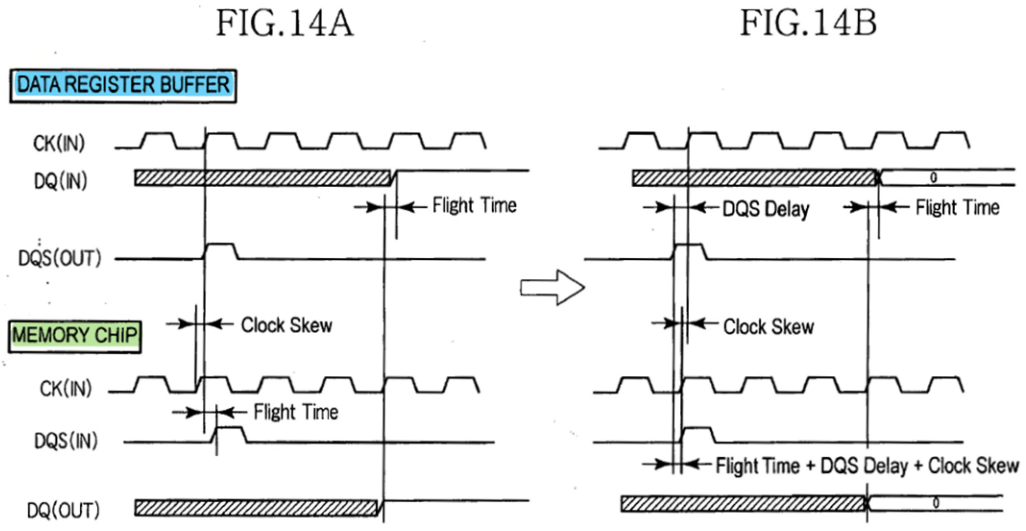
160. Figures 14A and 14B of Hiraishi explain the S-4 write leveling operation between the data register buffer 300 and the memory chips 200. *Id*. at [0142-46], Figs. 14A and 14B (reproduced below, annotated).



"FIG. 14A is a timing chart at the time of starting the leveling and FIG. 14B is a timing chart at the time of ending the leveling." *Id*. at [0142]. As shown in Fig. 14A before write leveling, the data register buffer (blue) outputs the strobe DQS(OUT) in synchronization with its own clock signal CK(IN), but the memory chip (green) receives that strobe DQS(IN) out of sync, due to Clock Skew and Flight Time differences. *Id*. at [0143]. "The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW" such that "the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other" as shown in FIG. 14B. *Id*. at [0145-46]. The resulting

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delays are stored in the data register buffer 300 and applied to delay both the data and data strobe signals during subsequent write operations such that both write data and strobe signals arrive at the memory with a predetermined latency WL=5. *Id*., *see also* Fig. 12 (reproduced below in part annotated with blue box showing the resulting "Re-timing")).

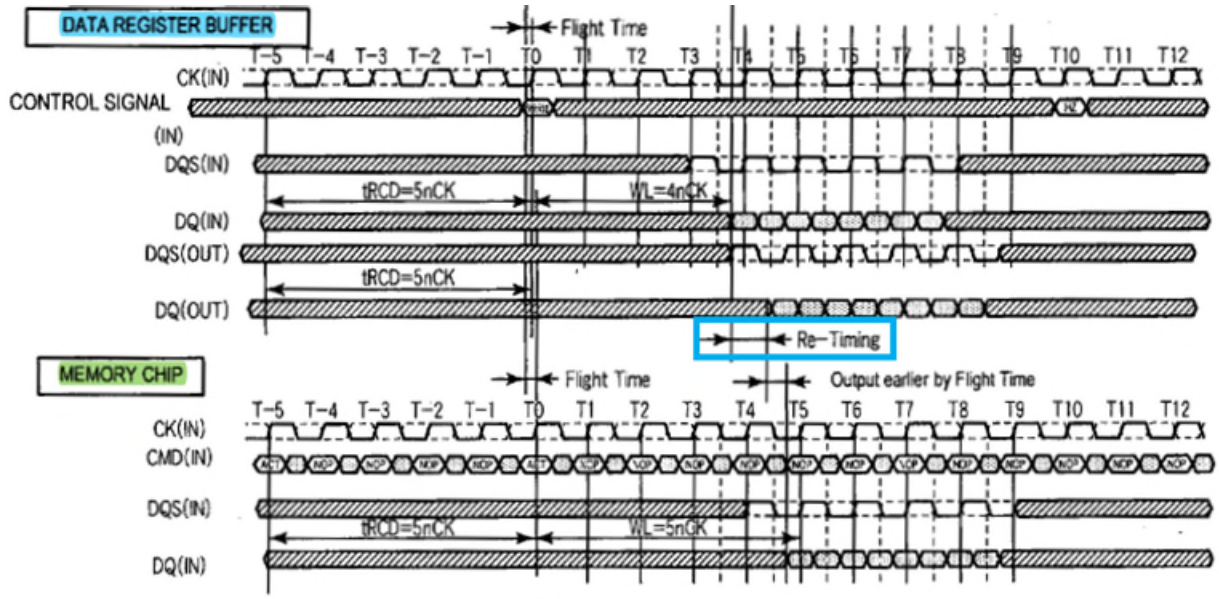

FIG.12

A Skilled Artisan would have understood that delaying both the data and strobe signals ensures that the standard data to strobe timing requirements are met at the memory devices. EX1020 (JESD79-3C) at 68 ("Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command.").

161. In particular, Hiraishi discloses that the "data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 …[and] performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS." EX1005 at [0135], Fig. 5 (reproduced below annotated to show data paths, orange, for write operations). "An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310." *Id*. at [0087]. "A strobe generating circuit 374 generates a data strobe signal DQS to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310." *Id*. at [0084]. "A phase of the data strobe signal DQS generated by the strobe generating circuit 374 is delayed by about 90 degrees with respect to the internal clock LCLKW by a delay circuit 370." *Id*. at [0091].

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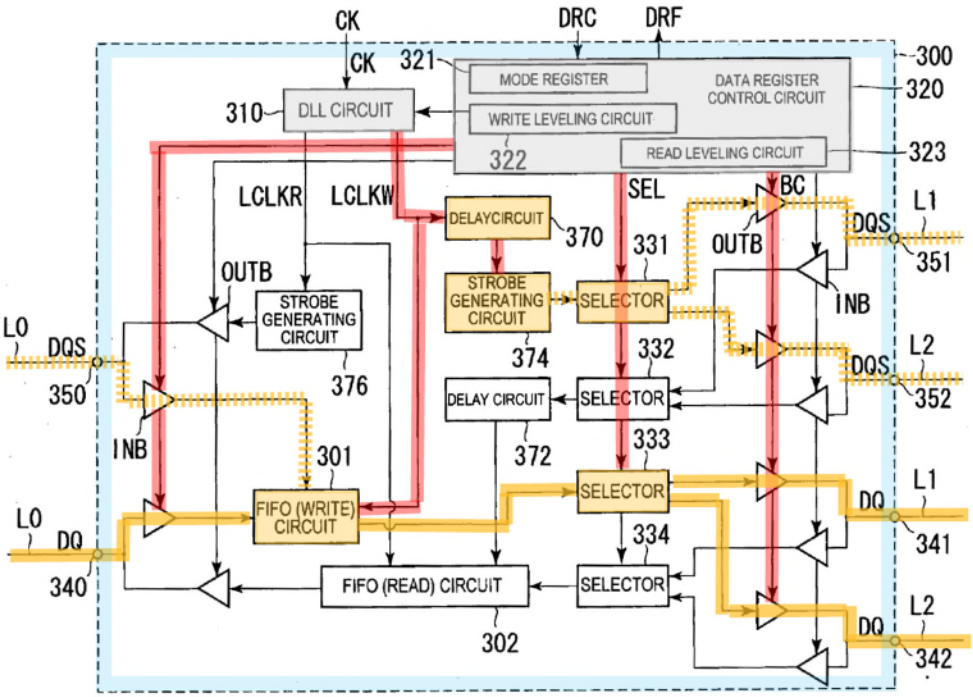

FIG.5

A Skilled Artisan would have understood from this disclosure that Hiraishi's delay circuit for write operations includes the FIFO (write) circuit 301 and performs a re-timing of the DQ/DQS signals in synchronization with the delayed internal clock LCLKW. The LCLKW signal is generated by DLL circuit 310 and used to time the FIFO circuit 301 to output the write data DQ as well as to generate the corresponding strobe DQS with Delay and Strobe Generating Circuits 370 and 374. Because the same LCLKW is used for timing the output of both the delayed data and strobe signals, a Skilled Artisan would have understood that those signals achieve the required synchronization. These write delays are applied to the write data and strobe signals in response to a write command received through the DRC

signals. *Id*. at Fig. 12 (reproduced above in part), [0133-35]. The result of Hiraishi's delay circuit is a variable delay which is set by the write leveling operation in response to write leveling mode setting commands and is applied during the normal write operations in response to write commands.

162. Similarly, Hiraishi discloses that the S-4 read leveling operation is "to adjust … a read timing in consideration of a propagation time of a signal." EX1005 (Hiraishi), [0140]. For example, Hiraishi discloses that read data arrives at the data buffer from different memories at different times A. EX1005, Fig. 15, ¶[150-151].

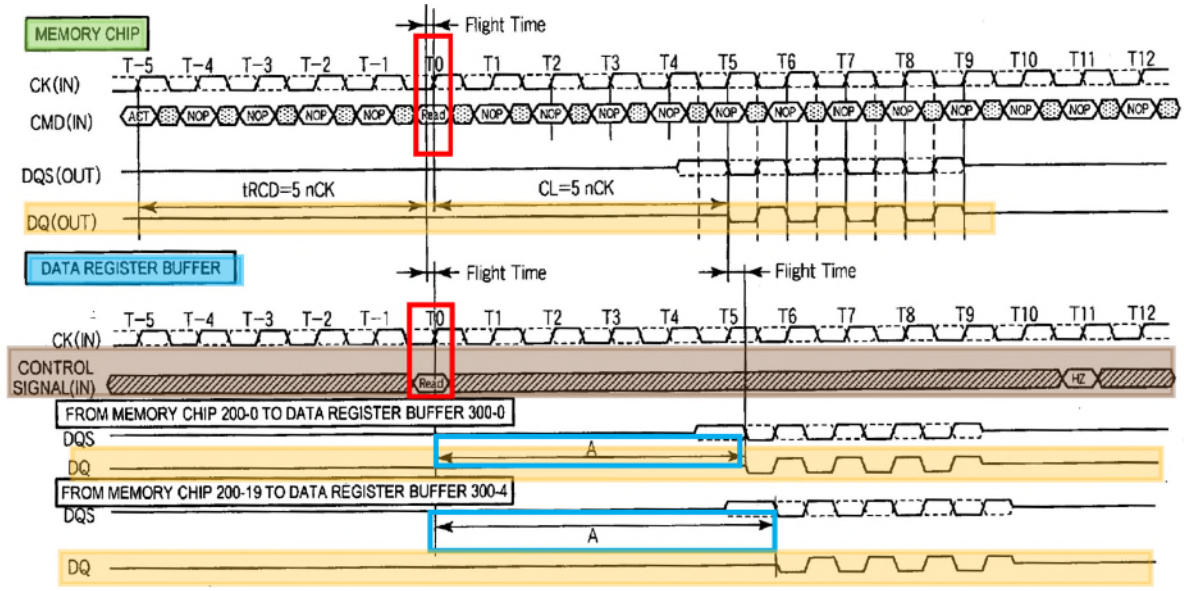

FIG.15

Read leveling determines delays ("Re-Timing") for the read data (DQ) and strobe (DQS) signals received at different times A such that the delayed data and strobe

signals are output CL=6 clock cycles after the read command is received in the data buffer. EX1005, ¶¶[0163], [0147]-[0151], Fig. 11 (reproduced below in part, annotated).

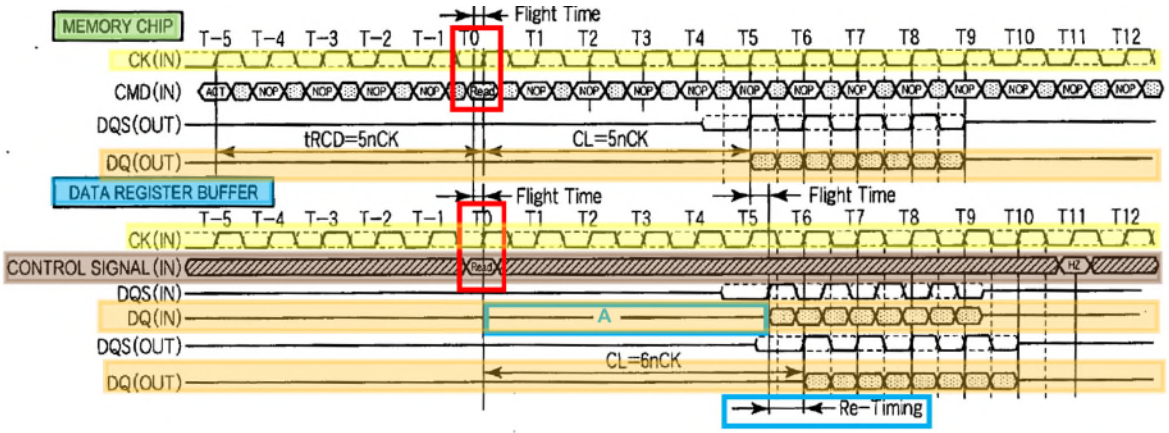

FIG.11

Hiraishi further explains that "the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK." *Id.*, [0163]; *see also* [0147]-[0151].

163. A Skilled Artisan would have understood from this disclosure of Hiraishi that the DQ/DQS read delays are determined as the difference between the time of data output at CL=6 and time A of data arrival. Therefore, the read delays vary based on the timing of the control and clock signals (DRC, CK) carrying the read command (T0), the measured read data arrival time A from the memory, and a latency parameter (CL=6). In a normal read operation, the data (DQ) and strobe

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(DQS) signals received from different memory devices are delayed through the data path by a respective amount determined by the previous read leveling operation such that the DQ/DQS signals will be output with a controlled phase relative to the clock signal CK (e.g., at CL=6) from the command/address/control register buffer ("a phase is controlled with respect to an external clock signal"). EX1005, ¶[0163]. Those read delays are based on the timing of the control signal (DRC) carrying the read command received from the command/address/control register buffer and the measured time A which, together, specify the time when the read data arrives. From the moment the data arrives at time A, it is delayed by an amount that is the difference between CL=6 and time A of the specific memory device (both measured from T0, the time of the Read command). *Id*., Fig. 15, [0151] ("In FIG. 15, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4)."). Accordingly, Hiraishi's delay circuitry controls the timing of the data (DQ) and strobe signals (DQS) on the read data paths in accordance with such timing information for subsequent read operations. This read leveling operation to determine delays for the read data and strobe signals is performed by the read leveling circuit 323 shown in FIG. 5, and a Skilled Artisan

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would have understood that the read leveling circuit 323 is activated by a module control signal DRC. EX1005 (Hiraishi), ¶¶[0147]-[0151]. Indeed, a Skilled Artisan would have understood that the read leveling circuit 323 has to be activated to perform the read leveling operation, and Hirashi's module control signal DRC can be used for such an activation, because other commands, such as Read commands, are also provided to the data register buffer during read leveling "as part of the control signal." *Id*.

164. A Skilled Artisan would have also understood at the time that, during read leveling, the memory devices are also put into a read leveling mode by corresponding mode register set commands to provide a predetermined data pattern (also called "dummy data" in Hiraishi), so that the Read Leveling circuit can compare the received (latched) data with that predetermined data pattern to identify any mismatches and adjust the phases and timing to achieve a better match. *See* EX1005 (Hiraishi), [0150] ("The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner."); *see also id*. [0160] (describing the role of "dummy data" for the read leveling operation between the data register buffer and the system memory controller), and FIGS. 5, 13. Indeed, Hiraishi expressly teaches the importance of the function of DLL circuits (phase matching) for DDR3 DRAM devices. *Id.* at [0163] ("In a recent high speed memory such as a DDR3 DRAM, a use of the DLL

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circuit is substantially essential."). A Skilled Artisan would have also understood at the time that DDR3 memories follow the JESD79-3 standard which describes that, during the read leveling operation, the DDR3 memories output a pre-defined data pattern from a Multi Purpose Register in response to read commands, and this data pattern can be used to verify whether the read data has been properly captured. *Id.*, [0150]; EX1020 (JESD79-3C) at Section 3.4.5.1 (p. 31, "The predefined pattern will be used for read synchronization"), and Section 4.10 (p. 48, "The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence."), Fig. 21 (p. 51, "Memory controller repeats these calibration reads until read data capture at memory controller is optimized."). Thus, a Skilled Artisan would have understood that Hiraishi's read leveling can also use the standard read leveling techniques of the time.

165. A Skilled Artisan would have also understood that the "time A" measured by the data register buffer 300 is also used by the data register control circuit 320 to activate the data and strobe paths (including the input buffers INB) in time so that the data is properly clocked into the FIFO (read) circuit 302. EX1005 (Hiraishi) at [0084-85, 151], Fig. 5 (reproduced below annotated to show data paths for read operations).

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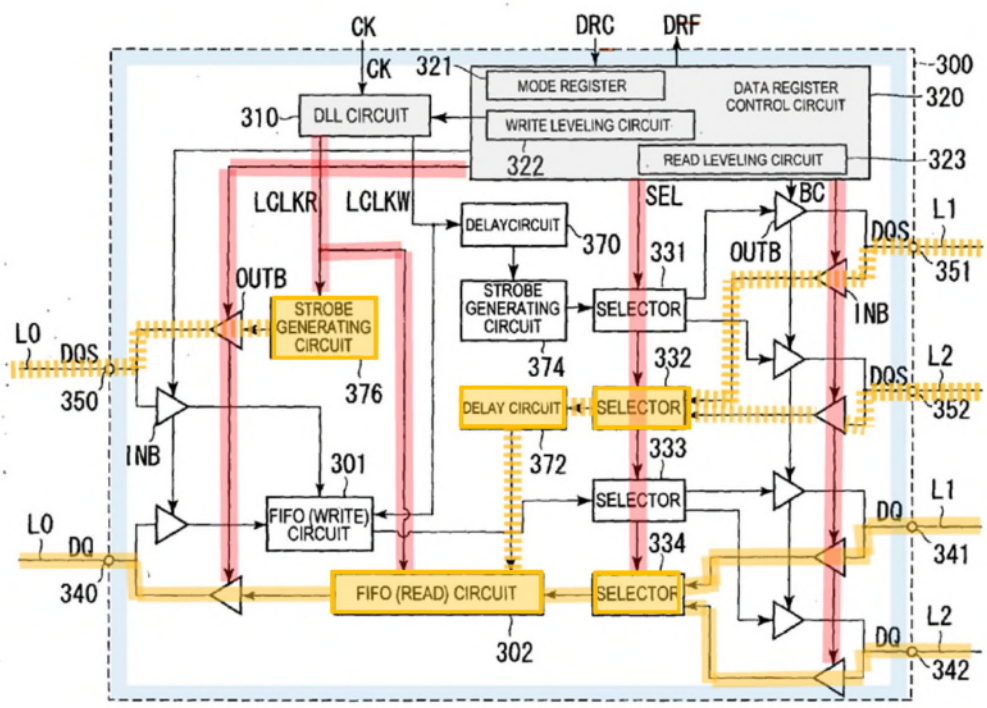

FIG.5

Hiraishi also discloses that "[a]n output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310." *Id*. at [0087]. In addition, a "strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310." *Id*. at [0084]. A Skilled Artisan would have understood from this disclosure of Hiraishi that these operations effectively adjust the timing of the read data and strobe signals by delaying those signals through the data path in response to a read command during normal operation with an amount that was determined during the read leveling operation in response to mode setting commands during initialization. *Id*. at Fig. 11 (reproduced above in part), [0123-130]. For example, the read data

and strobe signals received at "time A" from the memory devices are delayed by a variable amount such that they are output on the data bus in synchronization with the local clock of the data register buffer at CL=6 after receiving the Read command.

166. Therefore, Hiraishi discloses the claimed "*delay circuit*" for read operations, including the FIFO (read) circuit 302 delaying the data signal, delay circuit 372 delaying the input strobe signal, the strobe generating circuit 376 generating the strobe signal for the delayed data, and DLL circuit 310 generating the LCLKR signal for timing the output of the delayed data and strobe signals. In particular, the input of the FIFO (read) circuit 302 (like input buffers INB) is activated in accordance with time A, and the data is read into the FIFO (read) circuit 302 according to a strobe signal delayed by delay circuit 372. EX1005 at [0091] ("The selector 334 … supplies the selected data DQ to the FIFO (Read) circuit 302…, the selector 332 selects a data strobe signal DQS … A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal."). The output of the FIFO (read) circuit 302 is timed by the internal clock LCLKR generated by the DLL circuit 310, therefore delaying the read data signal by a variable amount that is determined such that it is output in synchronization with the clock signal CK at CL=6 after the Read command. *Id*. at

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[0087] ("An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310."). The clock LCLKR is also used to generate the delayed strobe in synchronization with the data output. *Id*. at [0084] ("A strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310."). The result of Hiraishi's delay circuit is a variable read delay which is set by the read leveling operation in response to mode setting commands during initialization. Hiraishi also discloses that the read delay is applied during normal operation in response to module control signals indicating a read operation. EX1005 (Hiraishi), FIG. 11 (reproduced below in part with annotations, showing a Read command, in red box, received by the data register buffer during a read operation, and the "Re-timing" of the read data by an amount of delay which is the difference between CL=6 and time A, as shown in the blue boxes).

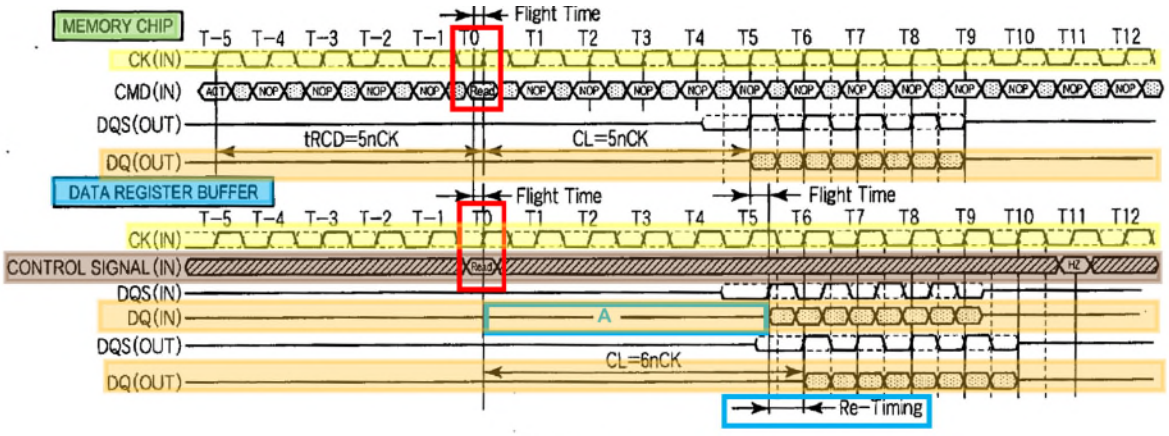

FIG.11

See also id. ¶[0130] ("Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.").

167. A Skilled Artisan would have also understood that the DRF feedback signal in Hiraishi can be used to provide feedback about the status of the read leveling. For example, as shown in FIG. 15 Hiraishi, the command/address/control register buffer issues a read command to the memories and to the data register buffers during read leveling, and the memory chips provide a predefined data pattern in response in accordance with their mode register settings for read leveling. Thus, the command/address/control register needs to know whether it has to send another read command and continue the read leveling operation or it can end the read leveling and change the mode register settings of the memory device for the subsequent regular read operations. A Skilled Artisan would have understood that the data register buffer can use the DRF signal in Hiraishi to indicate that the data pattern has been correctly read, e.g., that the right phase was found. Indeed, Hiraishi discloses that the DRF signal can be used to provide status information from the data register buffer to the command/address/control register buffer. EX1005 (Hiraishi), [0089] ("In addition, the data register control circuit 320 generates a feedback signal DRF and supplies it to the

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command/address/control register buffer 400. The feedback signal DRF is a signal indicating a current status of the data register buffer 300."). A Skilled Artisan would have understood from this disclosure that such a status information can include a status, such as completion, success or failure, of the read leveling operation, so the command/address/control register buffer 400 can continue or stop the read leveling operation and send module control signals to the data register buffer accordingly. Thus, the module controller in Hiraishi, in combination with the data buffer, can perform a read leveling operation between the data buffer and the memory devices.

168. Moreover, I understand that Netlist made several admissions in its Patent Owner Preliminary Response in IPR2017-00730 regarding the disclosure of the prior art reference Saito (which has a disclosure similar to that of Hiraishi). These admissions demonstrate Saito discloses limitation 1[f] under Netlist's apparent claim construction. For example, Netlist characterized Saito as follows, with reference to an annotated version of Saito's Figure 15 (which is similar to Fig. 15 of Hiraishi):

> As illustrated in Fig. 15 (reproduced and annotated below), ***S4-Read Leveling begins with*** the command/address/control register buffer 400 outputting the clock signal CK, the active command (ACT) and the read command (Read). (Id., ¶ [0146].) The ***clock signal CK is supplied to*** the memory chip 200 and ***the data register buffer 300***,

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and the ***Read command is supplied to*** the memory chip 200 and ***the data register buffer 300 (e.g., as a part of the control signal DRC)***. (Id.) The memory chip 200 can perform a read operation in response to the Read command and output a data pattern. (Id., ¶ [0148].) The data output by the memory chip 200 can be received by ***the data register buffer 300***, and used ***to determine time A***. (Id., ¶ [0149].)

EX1013 (Netlist POPR from '632 IPR) at p. 38.

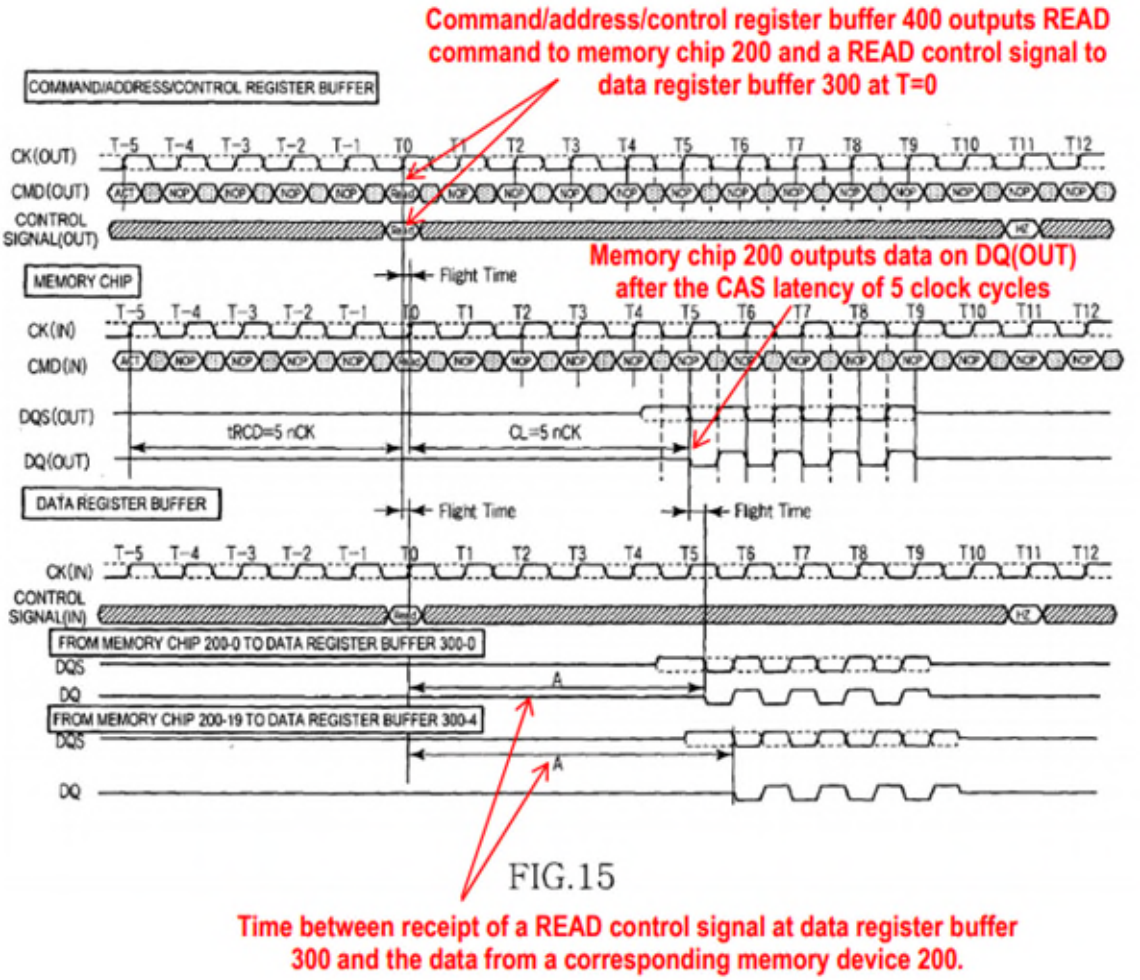

FIG.15

Time between receipt of a READ control signal at data register buffer 300 and the data from a corresponding memory device 200.

EX1013 (Netlist POPR from '632 IPR) at p. 39 (Red annotations from Netlist).

169. Netlist then characterizes Saito's S-4 read leveling as follows:

> Saito's S4-Read Leveling ***measures, for each memory chip, a time A between receipt of a Read Command from a command/address/control register buffer 400 and receipt of read data from a memory chip 200 at the corresponding data register buffer 300.***

Id. at p. 42; *see also id*. at 39-40 ("The S4 Read Leveling operation ***accounts for potential mismatch involving other signals***: ***Read commands signals and clock signals*** being sent to both the memory chip 200 and the data register buffer 300 in parallel."). Thus, Netlist has admitted that Saito discloses the S4 read leveling which it also now points to for infringement purposes.

170. I further note that the claim language in the '632 Patent, which was at issue in that IPR, was not reciting a "*delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.*" As I discussed above, Saito discloses a delay circuit, including the read and write FIFO, strobe delay and strobe generation circuits and the DLL circuit, for re-timing the read and write data by delaying it by an amount that was determined during read and write leveling. For example, the read data which enters Saito's delay circuit at time A after the read command is delayed until CL=6 clock cycles of the module clock signal (CK). EX1005, ¶[0128] ("Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read)

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circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS."). Similarly, the write data and strobe signals are delayed through the data buffer data path to arrive at the memory in sync with the memory's clock signal at WL=5. *Id*. at [0135] ("The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS.") and [0146] ("Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.").

171. Accordingly, at least under Netlist's apparent claim interpretation, claim 1 is rendered obvious by Hiraishi and Butt in light of the knowledge of a Skilled Artisan at the time.

2. Claim 2

a) 2[a]: "The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,"

172. Hiraishi discloses this limitation at least under Netlist's interpretation, *see supra* ¶ 113. As explained above in connection with claim 1, Hiraishi discloses

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S-4 read and write leveling operations. *See supra* ¶¶ 159-164. The S-4 read leveling operation comprises a "*first memory operation*" (as interpreted by Netlist for infringement purposes) and a subsequent normal read operation is a "*second memory operation subsequent to the first memory operation*." For similar reasons, S-4 write leveling operation comprises a "*first memory operation*" (as interpreted by Netlist for infringement purposes) and a subsequent write operation is a "*second memory operation subsequent to the first memory operation*." For example, the memory devices receive write leveling mode register set commands to perform write leveling operations. EX1020 (JESD79-3C) at 43 ("DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 8). … The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1."), 33 (Table 6, reproduced below, in part) and 29 (Fig. 10, reproduced below).

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				

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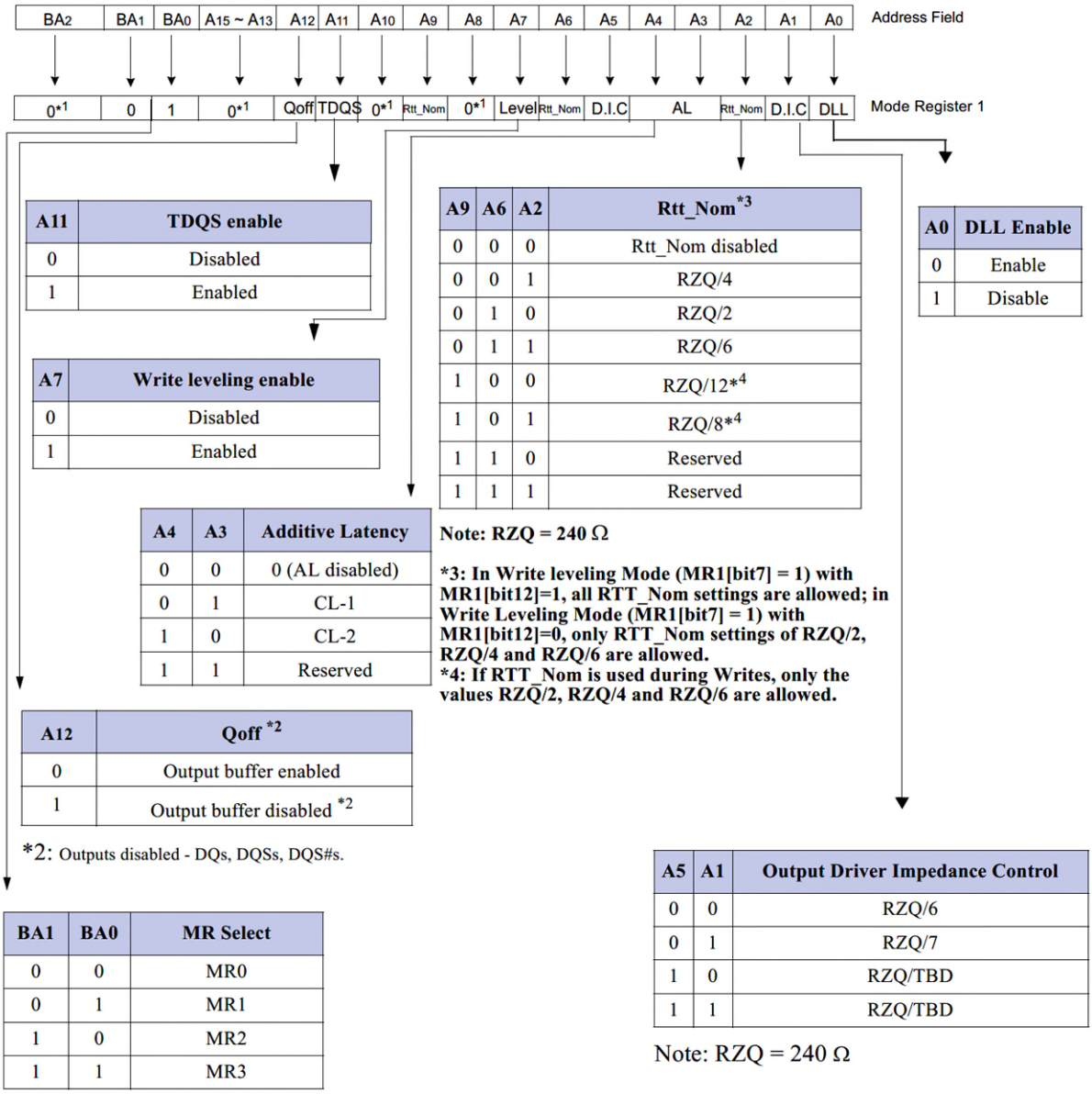

Figure 10 — MR1 Definition

173. In response to such mode register set commands for write leveling, the memory devices sample their local clock signal in accordance with the received data strobe signal and provide feedback of the sampled value on one more data lines. *Id.* ("… the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. ... DRAM samples CK -

CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after …. Either one or all data bits ('prime DQ bit(s)') provide the leveling feedback."). As discussed above, write leveling was a well-known operation for DDR3 memory devices at the time. *Supra* ¶¶ 159-161. The memory stops performing the write leveling operation upon receiving a mode register set command to exit the write leveling. EX1020 (JESD79-3C) at 43 ("During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode."). After exiting the write leveling operation, the memory devices can perform normal write operations in response to activate and write commands and receive the DQ/DQS signals with the timing established during write leveling. *Supra* ¶¶ 159-161. Similarly, the memory devices receive mode register set commands to activate their read leveling operation when they provide predetermined data from a Multi Purpose Register in response to read commands, instead of data stored at a received address. *Supra* at ¶¶ 162-164; EX1020 (JESD79-3C) at 31 (Fig. 12, reproduced below), 33 (Table 6, reproduced above in part), 48-54 (describing multi-purpose register for read calibration, including Fig. 20, reproduced below).

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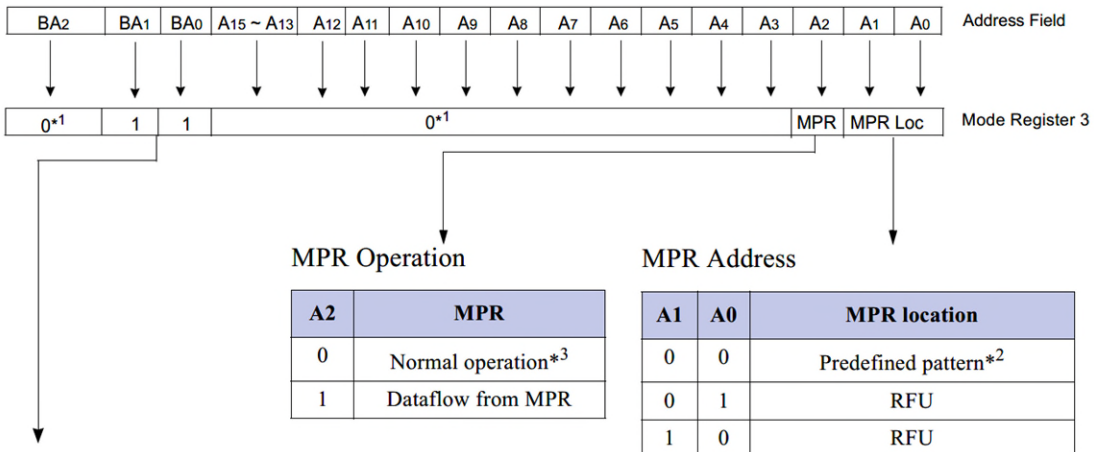
3.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming



MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*** 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.**
*** 2 : The predefined pattern will be used for read synchronization.**
*** 3 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.**

Figure 12 — MR3 Definition

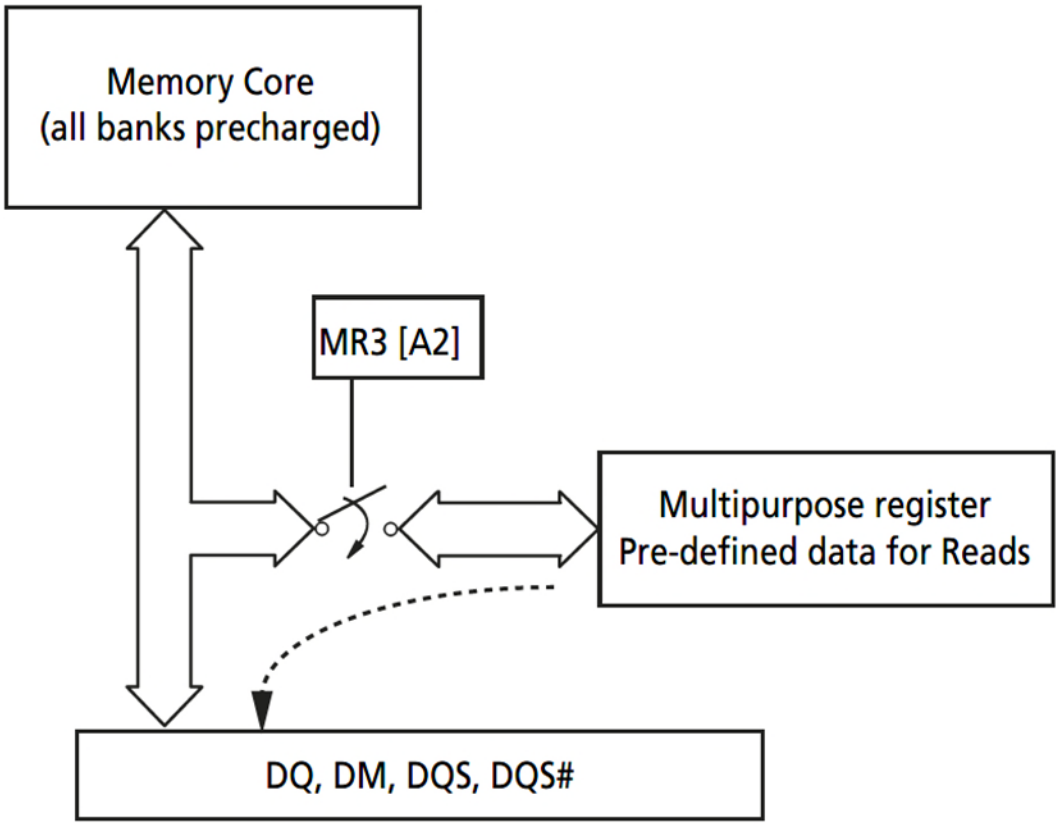


Figure 20 — MPR Block Diagram

After exiting the read leveling operation, the memory devices perform read operations in response to activate and read commands by providing data stored at a received address.

b) 2[b]: "wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,"

174. Hiraishi discloses this limitation to a Skilled Artisan in connection with Hiraishi's disclosure of S-4 read/write leveling (at least as interpreted by Netlist). As an initial matter, I note that the term "*the command signal*" lacks

proper antecedent basis because claim 1 recites both "*system command signals*" and "*module command signals*." To resolve this ambiguity for the purposes of this proceedings, I assume that "*the command signal*" refers to the "*system command signal.*"

175. For example, Hiraishi discloses that read and write command signals ("*second set of command signals*") from the system memory controller are received by command/address/control register 400. Hiraishi at Figs. 11 and 12, [0124-125] ("In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12. … The commands ACT and Read reaching the command/address/control connectors 130 are input to the command/address/control register buffer 400."), [0133-34] ("In the write operation, the memory controller issues an active command ACT and a write command Write … Because a flow of the command is similar to that in the read operation shown in FIG. 11, redundant explanations will be omitted.").

176. A Skilled Artisan would have understood that a "*first set of command signals*" from the memory controller is also necessary for the S4 read/write leveling operation ("*first memory operation*" under Netlist's interpretation). For example, Hiraishi discloses that the "initializing operation includes a mode register setting operation by which predetermined mode information is set in the mode registers 215, 321, and 431 that are included in the memory chip 200, the data

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register buffer 300, and the command/address/control register buffer 400, respectively (Step S3). Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4)." Hiraishi at [0139-40]. A Skilled Artisan would have understood from this disclosure that the system memory controller instructs the command/address/control register buffer on Hiraishi's module to perform the S4 read/write leveling using "*a first set of command signals,*" similar to the mode switching commands and mode register set commands for read and write leveling in the memory devices. *See, e.g.,* EX1020 (JESD79-3C) at 31, 33, 48-54 (multi-purpose register for read calibration), 43 (mode register setting for write leveling); *see also supra* at ¶¶159-160. Accordingly, a Skilled Artisan would have understood that the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation.

c) 2[c]: "wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,"

177. Hiraishi discloses this limitation at least in connection with Hiraishi's disclosure of S-4 read/write leveling.

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178. As explained above in connection with limitation 1[b], *supra* ¶¶ 122-128, Hiraishi discloses that the command/address/control register buffer 400 generates control signals in response to command signals. *See, e.g.*, *id.* [0060] (command/address/control register buffer 400 "receives the ***command signal***, … buffers the signals, and supplies the signals to the memory chips 200. … At the same time, the command/address/control register buffer 400 generates a ***control signal***."). For example, Hiraishi explains that the control signal generating circuit 430 (which is part of the command/address/control register buffer 400), generates control signals based on the command/address/control signal supplied by input terminal 401:

> The control signal generating circuit 430 is a circuit that ***generates the control signal DRC*** to be supplied to the data register buffer 300 ***based on the command/address/control signal supplied via the input terminal 401***, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404.

Id., [0099].

179. Hiraishi discloses that in connection with a read leveling operation, the command/address/control register buffer 400 generates module control signals

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in response to command signals and supplies the module control signals to the data register buffers 300:

> In the read leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 15, the command/address/control register buffer 400 outputs the clock signal CK, and at the same time, issues the active command ACT and the read command Read. The clock signal CK is supplied to the memory chip 200 and the data register buffer 300, and the commands ACT and Read are supplied to the memory chip 200. ***The read command Read is also supplied to the data register buffer 300 as a part of the control signal DRC***.

Id. [0148]. Similarly for write leveling operations, a Skilled Artisan would have understood that, during initialization, the command/address/control register buffer 400 outputs corresponding mode switching and mode register setting commands to the data register buffers 300. *Supra* at ¶¶159-160.

180. In connection with a subsequent a read operation, Hiraishi discloses that "The command/address/control register buffer 400 registers the ***received commands*** ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then outputs them to the memory chip 200. … In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 ***as a part of the control signal DRC***." *Id.* [0126]. For

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a write operation, "a flow of the command is similar to that in the read operation." *Id*. at [0134].

181. Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (e.g., command/address/control register buffer 400) outputs module control signals in response to the system command signals, such that the module control signals include a first set of module control signals in response to the first set of command signals (e.g., the set of command signals corresponding to initiating a read/write leveling operation; the "first memory operation") and a second set of module control signals in response to the second set of command signals (e.g., the set of command signals corresponding to a subsequent read or write operation; the "second memory operation").

d) 2[d]: "wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation."

182. Hiraishi discloses this limitation. The terms "*the at least one of the module control signals*" and "*the signal through the data path*" find antecedent basis in limitation 1[f], which recites "a delay circuit configured to delay ***a signal through the data path*** by an amount determined by the command processing circuit in response to ***at least one of the module control signals***."

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183. As explained above in connection with limitation 2[c], where the "first memory operation" is a read/write leveling operation, "the at least one of the module control signals" includes at least one of the first set of module control signals (i.e., the first set of module control signals corresponding to the set of command signals corresponding to initiating a read/write leveling operation, including, e.g., control signal DRC). Hiraishi discloses that the delay amount is determined by the command processing circuit, as recited in limitation 1[f], in response to this control signal. *See supra* ¶¶ 155-164. For example, Hiraishi discloses that in "the read leveling operation between the data register buffer 300 and the memory chip 200 … The clock signal CK is supplied to the memory chip 200 and the data register buffer 300 … [and] [t]he read command Read is also supplied to the data register buffer as part of the control signal DRC." EX1005 (Hiraishi) [0148].

184. As explained above in connection with limitation 1[f], Hiraishi discloses in view of Butt that subsequent to read/write leveling, the signal through the data path for read and write operations is delayed by an amount determined by read/write leveling. *See supra*, ¶¶ 159-164. Thus, where the "second memory operation" is a read or write operation, Hiraishi discloses that "*the signal through the data path is a signal associated with the second memory operation*," and this signal is delayed by an amount that is determined by the command processing

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circuit in response to at least one of the module control signals during the read/write leveling procedure which is "*at least one of the module control signals*" … "*of the first set of module control signals*."

3. Claim 3

a) 3[a]: "The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks,"

185. Hiraishi discloses that the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks. For example, Hiraishi expressly discloses a "four-Rank configuration" where there are four memory chips in a group ("*the respective set of memory devices*"), and each is in a different rank:

> The memory module 100 according to the present embodiment has a so-called ***4-Rank configuration***. The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner. Although the same address is assigned to each of the Ranks, one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal. In the present embodiment, four memory chips 200 constitute a single group (a single set), and ***the four memory chips 200 constituting the single group belong t*o ***different Ranks from each other***. For example, the memory chips 200-0 to 200-3 constitute a single group, and ***the memory chips 200-0 to 200-3 belong to different Ranks from each other***.

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EX1005 (Hiraishi), [0051]-[0052]. Accordingly, Hiraishi discloses this limitation.

b) 3[b]: "wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and"

186. Hiraishi discloses this limitation at least in connection with Hiraishi's disclosure of S-4 read/write leveling.

187. As explained above in connection with limitation 1[b], *supra* ¶¶ 122-128, Hiraishi discloses that the command/address/control register buffer 400 generates module command signals in response to system command signals. For example, Hiraishi discloses that the "command/address/control register buffer 400 "receives the ***command signal***, … supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and ***supplies the signals to the memory chips 200***." *Id.*, [0060]; *see also id.* [0097] ("[t]he register circuit 410 is a circuit that buffers the command signal CMD, …, and the ***buffered command signal CMD***, … [is] supplied to the memory chip 200 via the output terminal 402.").

188. Hiraishi discloses that, in connection with a read leveling operation, the command/address/control register buffer 400 outputs module command signals to memory devices 200 in response to command signals and supplies the corresponding module control signals to the data register buffers 300:

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> In the read leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 15, the command/address/control register buffer 400 outputs the clock signal CK, and at the same time, ***issues the active command ACT and the read command Read***. The clock signal CK is supplied to the memory chip 200 and the data register buffer 300, and the commands ACT and Read are supplied to the memory chip 200. The read command Read is also supplied to the data register buffer 300 as a part of the control signal DRC.

Id. [0148]. Similarly for write leveling operations, a Skilled Artisan would have understood that, during initialization, the command/address/control register buffer 400 outputs corresponding mode switching and mode register setting commands to the memory devices 200. *Supra* at ¶¶159-160; EX1020 (JESD79-3C), 42-43 ("Write Leveling" and "DRAM setting for write leveling").

189. In connection with a subsequent normal read operation, Hiraishi discloses that "The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then ***outputs them to the memory chip 200***." *Id.* [0126]. For a subsequent write operation, "a flow of the command is similar to that in the read operation." *Id*. at [0134].

190. Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (e.g., command/address/control register buffer 400)

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outputs module command signals to the memory devices in response to the system command signals, such that the module command signals include a first set of module command signals in response to the first set of command signals (e.g., the set of command signals corresponding to a read/write leveling operation) and a second set of module command signals in response to the second set of command signals (e.g., the set of command signals corresponding to a subsequent read or write operation).

c) 3[c]: "wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation."

191. Hiraishi also discloses that the second set of module command signals include chip select signals that select at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation. For example, Hiraishi discloses that each rank is selected by a respective chip select signal:

> Although the same address is assigned to each of the Ranks, ***one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal***.

EX1005 (Hiraishi), [0051]; EX1021 (Jacobs) at 319, 413; EX1018 (JEDEC 21-C) at 6 ("chip select lines"), 10-16 (showing one chip select line for each rank of memory devices). A Skilled Artisan would have understood that, because the

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"*respective set of memory devices*" includes one memory chip from each rank, the chip select signals also select one memory device in that "*respective set*." Hiraishi also discloses that the chip select signals are part of the command signals:

> By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed.

Id., [0076]. This is consistent with the understanding of a Skilled Artisan. *See, e.g.*, EX1020 (JESD79-3C) at 33 (Command Table identifying chip select signals as being part of command signals); *id.*at 13, 34 n.1 (same). Hiraishi further discloses that the selected memory device performs the "*second memory operation*" as it inputs or outputs respective data (DQ) and strobe (DQS) signals on terminals 204 and 205:

> With this arrangement, in the read operation, ***the read data*** read out from the memory cell array 230 ***is output from the data input/output terminal 204***, and in the write operation, ***the write data*** received ***from the data input/output terminal 204 is supplied to the memory cell array 230***. The ***data strobe terminal 205*** is a terminal for performing ***input and output of the data strobe signal DQS***, which is connected to the data strobe signal input/output circuit 214. The data strobe signal input/output circuit 214 generates the internal data strobe signal PDQS described above, and supplies it to the data input/output circuit 213.

EX1005 (Hiraishi), [0078]-[0081], FIG. 4.

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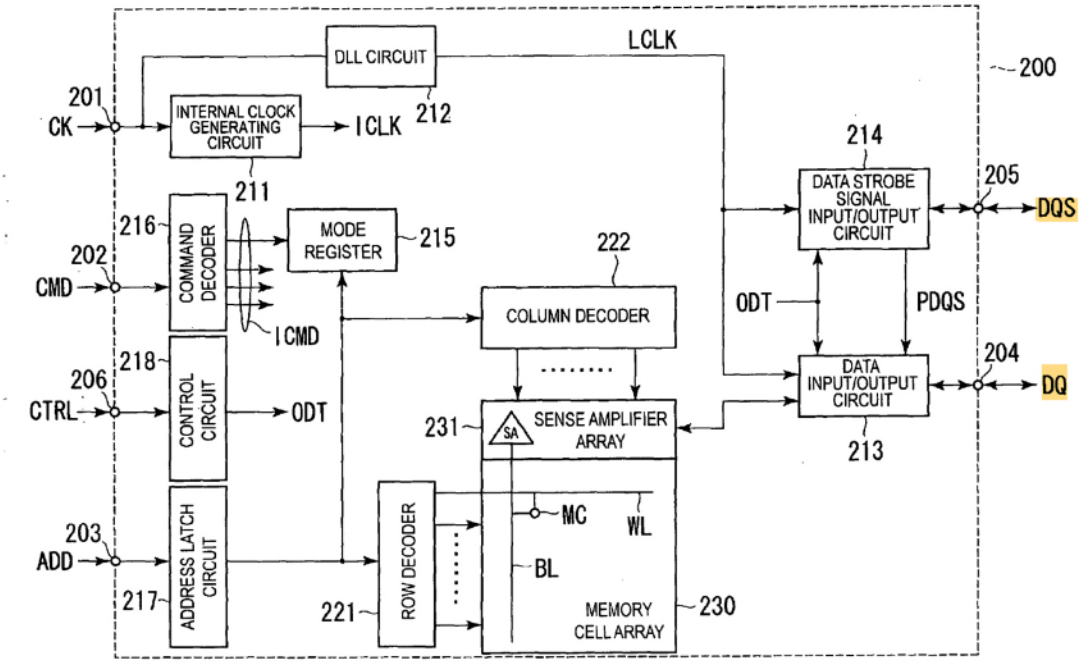

FIG.4

Accordingly, Hiraishi discloses this limitation.

4. Claim 4

192. Claim 4 recites "***The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.***"

193. Hiraishi discloses claim 4. For example, Hiraishi discloses:

> "As shown in FIG. 1, the four memory chips 200 constituting a single group are connected to one of the data register buffers 300. For example, the group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are mounted on the upper side of the module substrate 110 are

> connected to the data register buffer 300-0 via a data line L1, and the memory chips 200-2 and 200-3 that are mounted on the lower side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L2. ***An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte*** (8 bits)."

EX1005 (Hiraishi), [0053];

> In the present embodiment, because a single data register buffer 300 inputs and outputs 1-byte data, 8 sets of the FIFO circuits 301 and 302 are required.

EX1005 (Hiraishi), [0085]. Accordingly, Hiraishi discloses that each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

5. Claim 5 is obvious over Hiraishi and Butt in further view of Ellsberry

194. Claim 5 recites "***The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.***" The Hiraishi-Butt combination alone and in view of Ellsberry renders obvious these limitations.

195. As explained above in connection with claim 4, *see supra* ¶¶ 192-193, Hiraishi discloses that each of the plurality of buffer circuits has a data width of 1 byte. Further, although Hiraishi discloses that each of the memory devices has a data width of 1 byte, Hiraishi does not limit his invention to that particular data

width, *see, e.g.*, EX1005 (Hiraishi) [0073] (stating "memory chip 200 is a DRAM" without limiting the data width of the DRAM) and thus a Skilled Artisan would have understood that a data width of 1 byte is just one implementation, and other implementations can use memory devices with different bit widths. *See, e.g.,* EX1020 (JESD79-3C) at 3-12 (describing standard DDR3 SDRAM devices with x4, x8, and x16 data widths), and EX1018 (JESD21-C) at 4.20.4-25 to -27 (describing DDR SDRAM Module Configurations for Registered DIMM, including x8 and x4 DDR SDRAM devices); *see also* EX1021 (Jacobs) at 370-71 and Table 8.1 (showing x4, x8, and x16 memory devices as known alternatives). Thus, using a pair of 4-bit wide memory devices instead of one 8-bit wide memory device would have been obvious in view of the knowledge of a person of ordinary skill in the art since using either 4-bit or 8-bit wide memory devices on a module was well known at the time. Therefore, Hiraishi renders obvious this limitation.

196. To the extent one might argue that Hiraishi alone does not render obvious using 4-bit memory devices, this claim is also rendered obvious by Hiraishi (as combined with Butt) in view of Ellsberry. Hiraishi and Ellsberry are analogous art to the 608 patent as each is directed to solving the problem of reducing the load of memory modules. EX1001 at 3:25-29 ("A memory module according to one embodiment includes … load reduction devices"); EX1005 (Hiraishi) at Title (Load Reduced Memory Module); EX1007 (Ellsberry) at [0012]

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("Moreover, the load on the bus is not increased because the memory bank switches present a single load to the bus, not the load of the individual memory devices coupled thereto."). For example, Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi (and the 608 patent) and expressly describes modules with 8-bit wide data buffers (SWITCH ASIC with DQ[3:0] and DQ [7:4]) coupled to either 8-bit wide memory chips or 4-bit wide memory chips. *See, e.g.*, EX1007 (Ellsberry) at Fig. 11 (pairs of 4-bit wide memories) and Fig. 13 (8-bit wide memories):

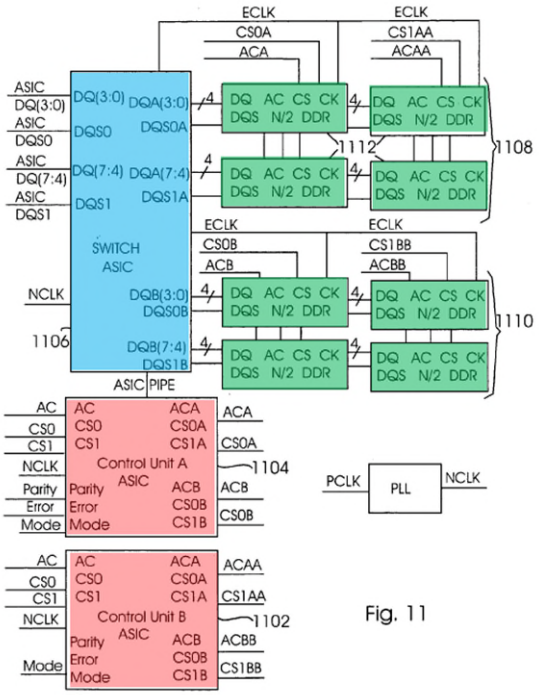

Fig. 11

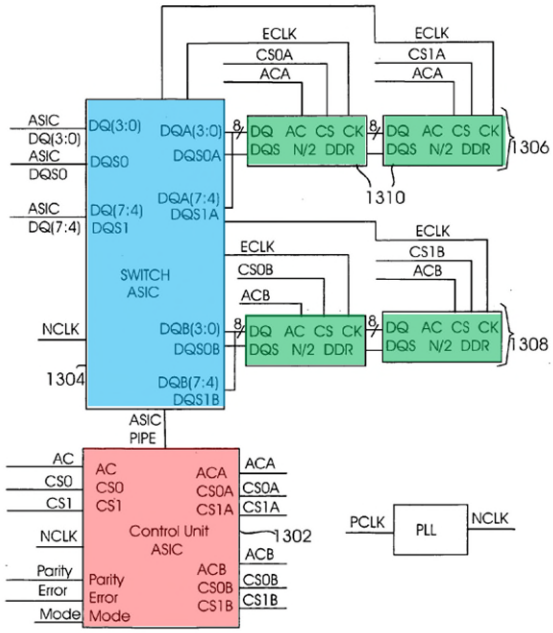

Fig. 13

197. A Skilled Artisan would understand that FIGS. 2, 5, and 13 correspond to an embodiment of Ellsberry utilizing 8-bit memory devices, and FIGS. 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit

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memory devices. EX1015 (FWD of IPR2018-00362) at 77-78 (PTAB agreeing that Ellsberry discloses embodiments with both 4-bit-wide and 8-bit-wide memory devices). With respect to the 4-bit embodiment, Ellsberry explains that the memory module of FIG. 6 "uses a dual stack configuration (similar to that illustrated in FIG. 11) in which two control units 604 are employed, one control unit 604 on each side of the module." EX1007 (Ellsberry), [0051]. A Skilled Artisan would understand from this disclosure that, in this case, two 4-bit wide memory devices are stacked in each "CSP" package shown in FIG. 6. Thus, in FIG. 11, four pairs of 4-bit memory devices are used rather than four 8-bit wide memory devices as shown in FIG. 13. In FIG. 11, two 4-bit wide memory devices are coupled to Port A, bits [3:0] and [7:4], respectively, and receive the same chip select signal. For example, a pair of 4-bit memory devices coupled to bits [7:0] of Port A for this arrangement receive the CS0A chip select signal generated by Control Unit A ASIC as shown in Fig. 11, above. *See also id*., [0051,54]. Also, another control unit ASIC (B) is mounted to the other side of the module in FIG. 6, but otherwise the module operates as before. *Id*.

198. A Skilled Artisan trying to select the available bit width of the memory devices and the corresponding buffers for Hiraishi's memory module would have been motivated to look at Ellsberry's disclosure because Ellsberry discloses a memory module with the same distributed buffer architecture and four

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ranks of memories as Hiraishi and expressly describes modules with 8-bit wide data buffers and with 8-bit and 4-bit wide chips. The combination provided nothing more than expected at the time, a memory module of Hiraishi with two 4-bit wide chips being used instead of a single 8-bit wide chip as taught by Ellsberry. Therefore, Hiraishi and Butt in view of Ellsberry also renders obvious this limitation.

6. Claim 6 is obvious over Hiraishi and Butt in further view of Kim

199. The Hiraishi-Butt combination alone renders obvious claim 6 and, even if someone may argue it does not, claim 6 is also rendered obvious by the combination of Hiraishi (as combined with Butt) and Kim.

200. Claim 6 recites "***The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal***."

201. As illustrated by annotated Figure 5 of Hiraishi below, Hiraishi discloses that the "*each respective buffer further includes a receiver circuit* [in DLL circuit 310 and Data Register Control circuit 320] *for each of the module control signals* [*e.g.*, DRC]," and at least renders obvious that "*the receiver circuit includes a metastability detection circuit configured to determine a metastability*

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condition [such as a metastability condition in capturing signal values] *in the each of the module control signals* [*e.g.*, DRC] *with respect to the module clock signal* [CK]."

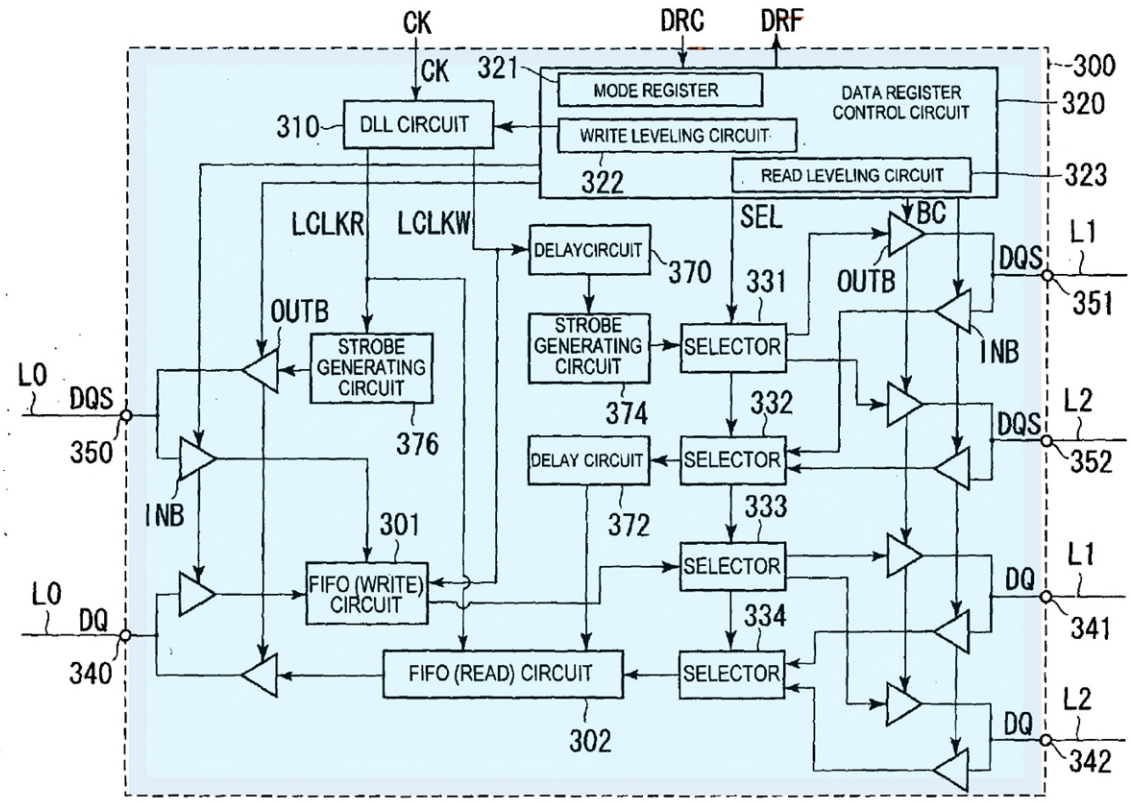

FIG.5

EX1005 (Hiraishi), Fig. 5 (annotated).

202. For example, Hiraishi discloses that the control signal DRC and the corresponding clock CK are transmitted on control line L4 to multiple Data Register Buffers. *Id*. at Fig. 7.

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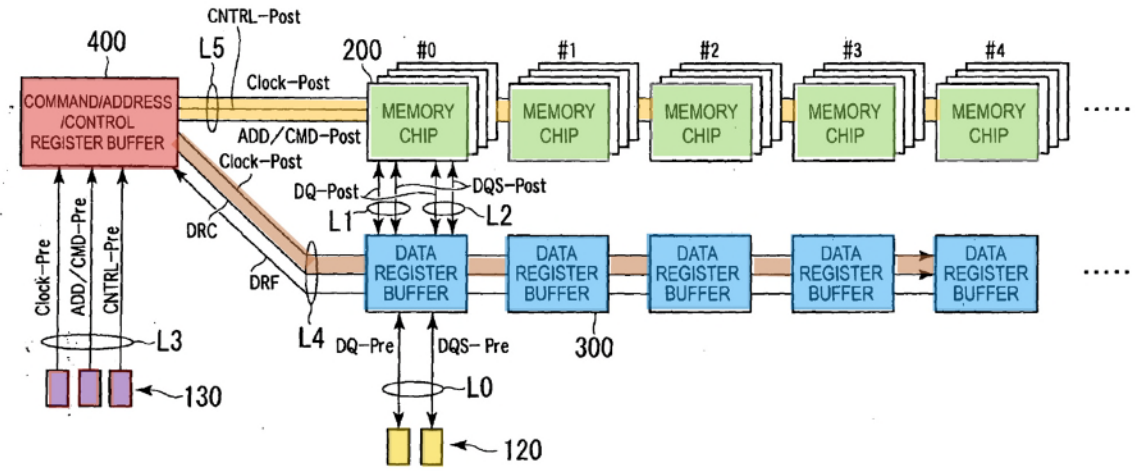

FIG.7

Hiraishi also discloses that the DLL circuit 310 in the data register buffer receives the module clock signal CK and generates from the received CK signal a number of internal clocks, including LCLKR and LCLKW, with fine phase adjustments that are used for the internal operation of the data buffer. *See, e.g.*, EX1005 (Hiraishi), FIG. 5. Hiraishi further discloses that the DRC signal is captured by the Data Register Control unit 320. *Id*.

203. A Skilled Artisan would have understood from this disclosure that DLL circuit 310 generates, based on the received clock signal CK, the internal clock that is used to capture the DRC signal. A Skilled Artisan would have also understood that the DLL circuit generates that internal clock with a specific phase that is selected to avoid metastability because the control information conveyed by the DRC signal may not be correctly captured if there is a metastability condition

at the input of the DRC signal. EX1008 (Kim) at 1:21-31 ("Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output generation."). Indeed, due to the high speed at which the memory devices operated at the time, a Skilled Artisan would have understood that the "use of the DLL circuit is substantially essential." EX1005 (Hiraishi), [0163].

204. In light of the possibility of erroneous DRC signal reading, it would have been obvious to a Skilled Artisan to have the Data Register Control Circuit 320 include a known metastability condition detector (such as taught by Kim, EX1008) and implement the DLL circuit 310 to avoid such potential metastability by adjusting the phase of the internal clock signal that is used to capture the DRC signal (similar to how Hiraishi's DLL circuit adjusts the LCLKW signal's phase). A Skilled Artisan would have understood that such a metastability condition detector can be used, e.g., during initialization to indicate the presence of a metastability condition so that the phase of the internal clock is adjusted to avoid the metastability condition.

205. To the extent one might argue that Hiraishi's disclosure (with Butt) does not disclose or render obvious a metastability detection circuit and/or signal adjustment circuit as claimed, U.S. Patent No. 6,184,701 to Kim ("Kim") (Ex.

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1008) discloses such circuitry. Kim is analogous art to Hiraishi, since each is directed to solving the problem of reliable communication between integrated circuits. *See, e.g.,* EX1005 (Hiraishi) at Figs. 13-15 (describing read and write leveling operations between the data register buffers and the memory chips to ensure that the data communicated between the data buffer and the memory chips are properly captured); EX1008 at 1:12-14 ("The present invention relates to integrated circuit devices, and more particularly to integrated circuit devices which may be prone to generating metastable output signals."). A Skilled Artisan would have understood that such a reliable communication is also needed between Hiraishi's command/address/control register buffer 400 and data buffers 300. For example, Kim teaches that, when a circuit "receives input signals at similar analog levels [it] may be prone to generating an output signal in a metastable state (*i.e.*, where the potential of the output signal is greater than a maximum logic 0 level (VJL) and less than a minimum logic 1 level (VJH)). Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output generation." Ex. 1008 at 1:21-31. To solve that metastability problem, Kim discloses "a metastability detection/prevention circuit 20" to be incorporated with

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any "main active circuit 10" in need thereof, including "a data input buffer." Ex. 1008 at 2:23-37.

206. It would have been obvious to a Skilled Artisan to combine the functionality of Kim's metastability detection circuitry with the DRC inputs in Hiraishi's data register buffers. A Skilled Artisan would have been motivated to make the combination in order to obtain more reliable communication by avoiding metastability at the input of the DRC signals. Indeed, a Skilled Artisan would have understood that the DRC signals carry important control information. EX1005 (Hiraishi), [0100] ("The control signal DRC includes signals such as a signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L0 side of the data register buffer 300, a signal for controlling an ODT timing at the data lines L1 and L2 side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer 300, and a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like.").

207. In particular, as discussed above, a Skilled Artisan would have understood that the metastability can be avoided by the DLL adjusting the phase of the internal clock used by the input buffer. Furthermore, Hiraishi already teaches that its DLL circuit 310 can perform fine phase adjustments, such as those used for the LCLKW internal clock signal. Accordingly, making the combination would

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have been well within the level of skill at the time and provided nothing more than expected from the prior art: detecting metastability at the DRC input and removing the metastability by adjusting the phase of the corresponding internal clock. Therefore, the combination of Hiraishi and Butt further in view of Kim renders obvious that Hiraishi's "*receiver circuit include[es] a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal*."

7. Claim 7 is obvious over Hiraishi and Butt in further view of Kim

208. Claim 7 recites "***The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte***."

209. Claim 7 depends on claim 6. As explained above, claim 6 is rendered obvious by Hiraishi (as combined with Butt) or further in view of Kim. *See supra* ¶¶ 199-207. Additionally, as explained above in connection with claim 4, Hiraishi discloses that "*each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte*." *See supra* ¶¶ 192-193. Accordingly, claim 7 is rendered obvious over Hiraishi (with Butt) alone or further in view of Kim for the same reasons.

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8. Claim 8 is obvious over Hiraishi and Butt in further view of Kim and Ellsberry

210. Claim 8 recites "***The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits***."

211. Claim 8 depends on claim 6. As explained above, claim 6 is rendered obvious by Hiraishi (as combined with Butt) or further in view of Kim. *See supra* ¶¶ 199-207. Additionally, as explained above in connection with claim 5, Hiraishi (with Butt) alone and in view of Ellsberry renders obvious that "*each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.*" *See supra* ¶¶ 194-198. Accordingly, claim 8 is rendered obvious over Hiraishi (as combined with Butt) and in view of Kim and Ellsberry for the same reasons discussed above with reference to claims 5 and 6. In particular, the metastability circuit of claim 6 was obvious for the reasons discussed above with reference to claim 6, and the memory device width of 4 bits was obvious for the reasons discussed above with reference to claim 5, and the same reasoning applies when both the metastability circuit and four-bit wide memories are used in Hiraishi's module.

9. Claim 9

212. Hiraishi (with Butt) discloses claim 9[a] and at least renders obvious claim 9[b], and therefore renders claim 9 invalid.

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a) 9[a]: "The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,"

213. Hiraishi discloses that "*the each respective buffer circuit further includes a clock regeneration circuit* [including DLL circuit 310] *configured to generate a local clock signal* [for internal operations] *having a programmable phase relationship with the module clock signal* [CK]," [the local clocks LCLKW and LCLKR have a programmable phase relationship with the module clock signal CK]. EX1005 (Hiraishi), Fig. 5:

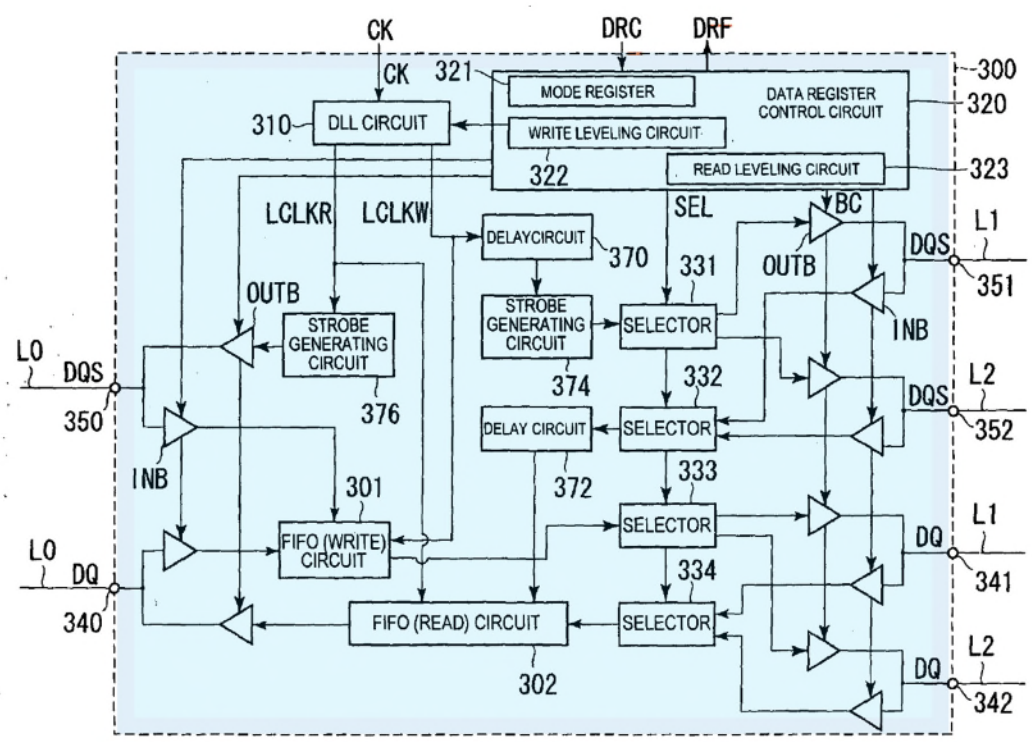

FIG.5

214. For example, Hiraishi expressly explains that the DLL circuit 310 generates local clock signals LCLKR and LCLKW based on the module clock signal CK:

> An output operation timing of the FIFO (Write) circuit 301 is defined by the ***internal clock LCLKW that is generated by the DLL circuit 310***. An output operation timing of the FIFO (Read) circuit 302 is defined by the ***internal clock LCLKR that is generated by the DLL circuit 310***. The DLL circuit 310 is a circuit that ***generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400***, having the ***same circuit configuration and function as that of the DLL circuit 212*** provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310.

Id., [0087]. With respect to DLL circuit 212 in the memory chip, which has the same function as the DLL circuit 310 in the data register buffer, *id*., Hiraishi further explains:

> The ***DLL circuit 212 takes a role of generating an internal clock LCLK*** and supplying the internal clock LCLK to a data input/output circuit 213 and a data strobe signal input/output circuit 214. The internal clock LCLK is a signal ***that is phase-controlled with respect to the clock signal CK, of which a phase is slightly advanced with respect to the clock signal CK such that***

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> ***phases of read data DQ and a data strobe signal DQS match with a phase of the clock signal CK***.

Id., [0074]. Hiraishi also discloses that:

> As described above, the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK.

Id., [0163]; *see also id.*, [0145] ("The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift."). A Skilled Artisan would have understood from this disclosure that Hiraishi's DLL circuit 310 is a clock regeneration circuit configured to generate local clock signals with a programmable phase relationship relative to the module clock signal CK, including a local clock used for the internal operation of the Data Register Buffer.

b) 9[b]: "wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices."

215. Hiraishi (with Butt) in view of the knowledge of a Skilled Artisan at least renders obvious that "the each respective buffer circuit is configured to output the local clock signal to the respective set of memory devices."

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216. Although Hiraishi discloses embodiments in which the buffer circuits 300 and memory devices 200 each have their own DLL circuits (and thus generate their own local clock signal, such that the local clock of the buffer circuits is not output to the memory devices), Hiraishi also discloses that:

> [W]hile the above embodiment has described a memory chip that includes a DLL circuit therein as the memory chip 200, ***a memory chip that does not include a DLL circuit therein can be alternatively used***. In this case, ***the DLL circuit included in the data register buffer 300 is used to adjust the input/output timing***."

Id. at [0200]. A Skilled Artisan would thus have understood from this disclosure that, when the memory chips do not include a DLL circuit, it is the DLL circuit in the buffer circuit 300 which is used to adjust the input/output timing in the memory chips as well, and a local clock signal of the buffer circuits would be output to the respective set of memory devices in order to synchronize the operations of those memory devices with the buffer circuit. EX1007 (Ellsberry) at Figs. 10-11 (showing a data buffer called Switch ASIC outputting a clock signal ECLK to the coupled memory chips) and Fig. 4 (showing a PLL in the data buffer generating a local clock).

217. Indeed, a Skilled Artisan would have known that sharing circuitry between buffer circuits and memory devices, including circuits that generate a

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local clock, was a well-known design choice at the time of the invention, and that one common technique is to output the local clock of the buffer circuit to the memory devices. For example, U.S. Pat. No. 8,566,516 to Schakel ("Schakel," filed October 30, 2007 and claiming priority to July 31, 2006) discloses several configurations of memory modules, one of which involves a plurality of memory devices (DRAM modules) electrically interconnected to each other and a single buffer circuit ("intelligent buffer 133"), which includes the functionality of an interface circuit ("interface circuit 102"). *See, e.g.*, EX1009 Schakel at 4:5-14 ("In some embodiments, the any of the memory devices 104A-N may itself be a group of memory devices, or may be a group in the physical orientation of a stack. For example, FIG. 1B shows a memory device 130 which is comprised of a group of DRAM memory devices 132A-132N all electrically interconnected to each other and an intelligent buffer 133. In alternative embodiments, the intelligent buffer 133 may include the functionality of interface circuit 102. Further, the memory device 130 may be included in a DIMM (dual in-line memory module) or other type of memory module."); FIG. 1B:

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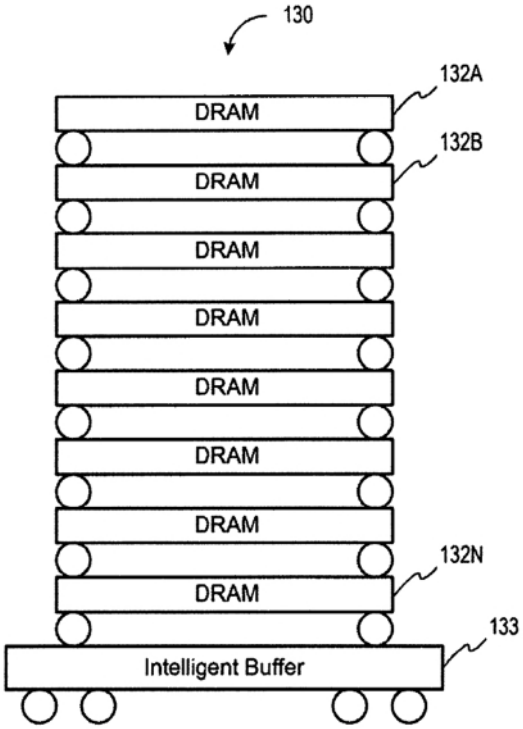

FIG. 1B

218. Schakel teaches that, in such an arrangement, "[t]he interface circuit 102 interfaces a plurality of signals 108 between the system device 106 and the memory devices 104A-N. The signals 108 may include, for example, data signals, address signals, control signals, ***clock signals***, and the like. In some embodiments, all of the signals 108 communicated between the system device 106 and the memory devices 104A-N are communicated via the interface circuit 102."). *Id.*, 4:31-41. In other words, Schakel discloses that as an alternative to each DRAM module having its own clock generating circuitry, they can be associated with a single buffer circuit which outputs a clock signal thereto. This disclosure is consistent with the knowledge of a Skilled Artisan at the time—that it would have

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been obvious to output the local clock signal of the buffer circuit to the memory devices.

10. Claim 10

219. Hiraishi in view of Butt discloses the limitations of claim 10 to a Skilled Artisan and thus renders claim 10 obvious.

220. Claim 10 recites "***The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.***"

221. I note that "*the second memory operation*" as recited in claim 10 does not have antecedent basis. I assume for purposes of my analysis that claim 10 intended to depend from claim 2, which recites "*a second memory operation*."

222. As illustrated by the annotated version of Fig. 5 of Hiraishi, below, a Skilled Artisan would have understood in view of Butt that the data paths for read operations ("*second memory operation*") include a first data path for transmitting a strobe signal, such as the data path coupled to the line L1 at the input/output terminal 351 for transmitting data strobe signals (DQS, dashed orange line). *See*

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also supra at ¶¶144-147. As further illustrated by annotated Fig. 5, the data paths for read operations include a second data path for transmitting a data signal, such as the data path coupled to the data line L1 at the input/output terminal 341 for transmitting a data signal (DQ, solid orange line):

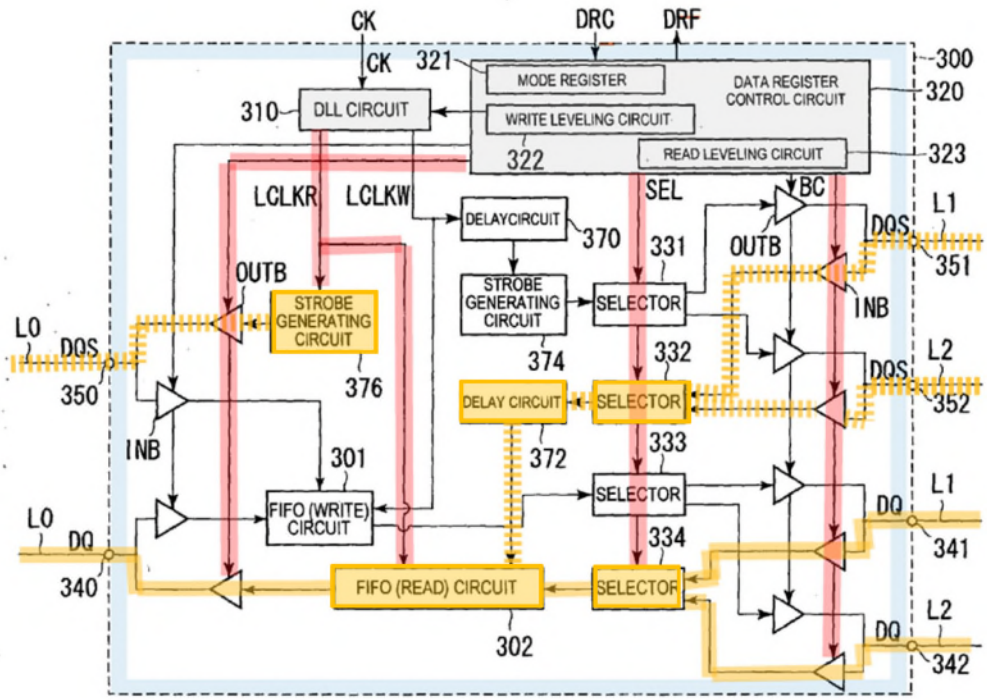

FIG.5

EX1005 (Hiraishi), FIG. 5 (annotated). As also shown in FIG. 5 of Hiraishi, data paths for read operations include another data path for transmitting a strobe signal, such as the data path coupled to the line L2 at the input/output terminal 352 for transmitting data strobe signals (DQS, dashed orange line), as well as for transmitting a data signal, such as the data path coupled to the line L2 at the input/output terminal 342 for transmitting data signals (DQ, solid orange line). Either L1 or L2 could be considered a "*first data path*," but only one of them

would be used at a given time. That is, the data paths have a "fork in the road" arrangement in Hiraishi for routing data and strobe signals from either one (L1) or the other (L2) branch to the same output (terminal 350, coupled to line L0 for strobe signals; terminal 340, coupled to line L0 for data signals) during read operations. This is substantially the same "fork in the road" arrangement as in the '608 Patent (strobe routing circuit 620 routing data strobe signals from either YA_{DQS} or YB_{DQS} to the same DQS terminal 1501 during read operations). *Compare* FIG. 5 of EX1005 (Hiraishi), *with* FIGS. 15-16 of EX1001 (the '608 Patent) (both reproduced below with annotations: solid orange lines added to indicate paths for data signals during read operations, and dashed orange lines added to indicate the sampled strobe signal—the gap in the dashed orange lines includes circuitry that provides the required delays of strobe signals through the data buffer).

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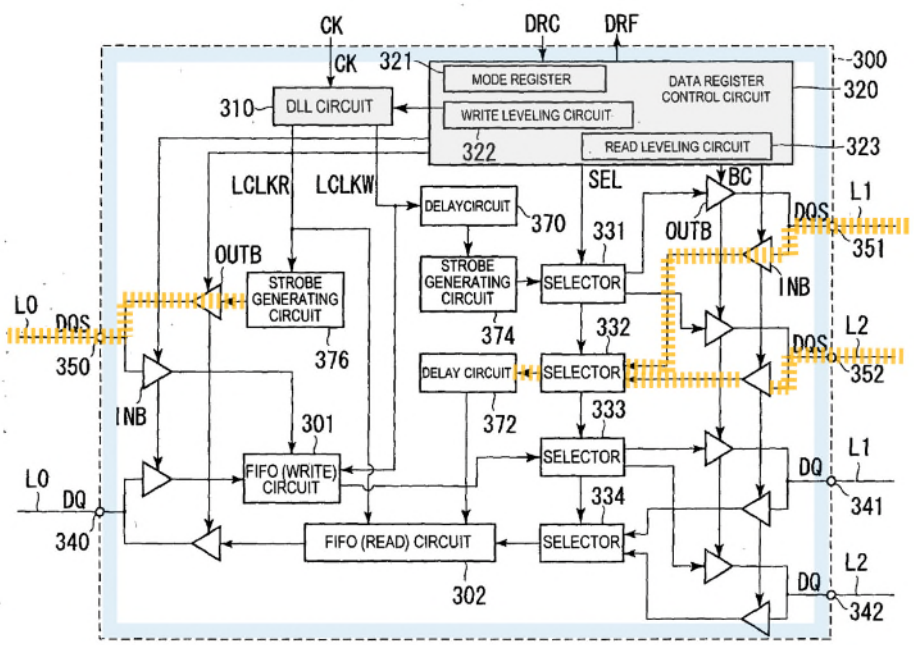
CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
LO
DQS
350
374
332
L2
DQS
352
376
DELAY CIRCUIT
SELECTOR
INB
372
333
301
SELECTOR
L1
LO
DQ
FIFO (WRITE) CIRCUIT
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
342
302

FIG.5

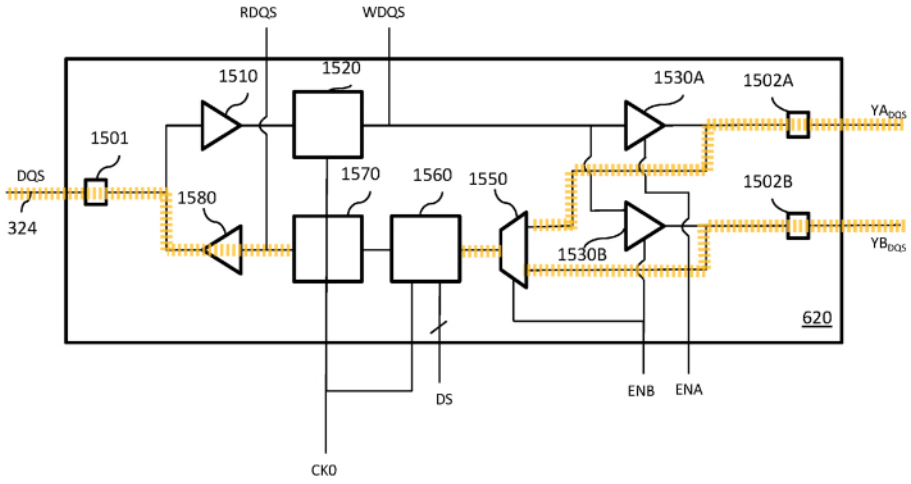
RDQS
WDQS
1510
1520
1530A
1502A
YA_DQS
1501
DQS
324
1580
1570
1560
1550
1502B
1530B
YB_DQS
620
DS
ENB
ENA
CKO

FIG. 15

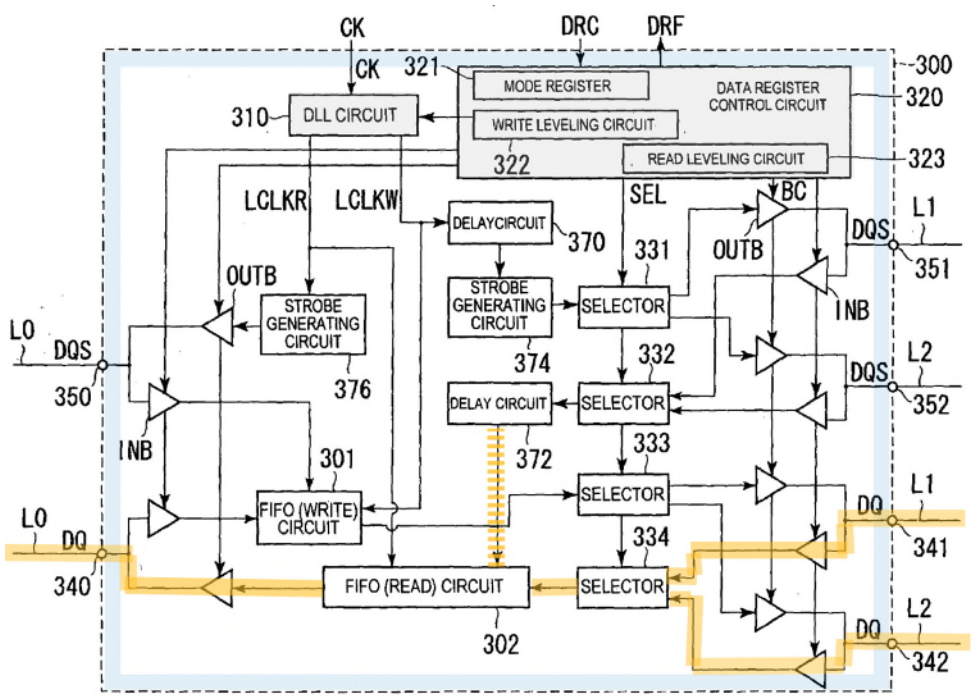

FIG.5

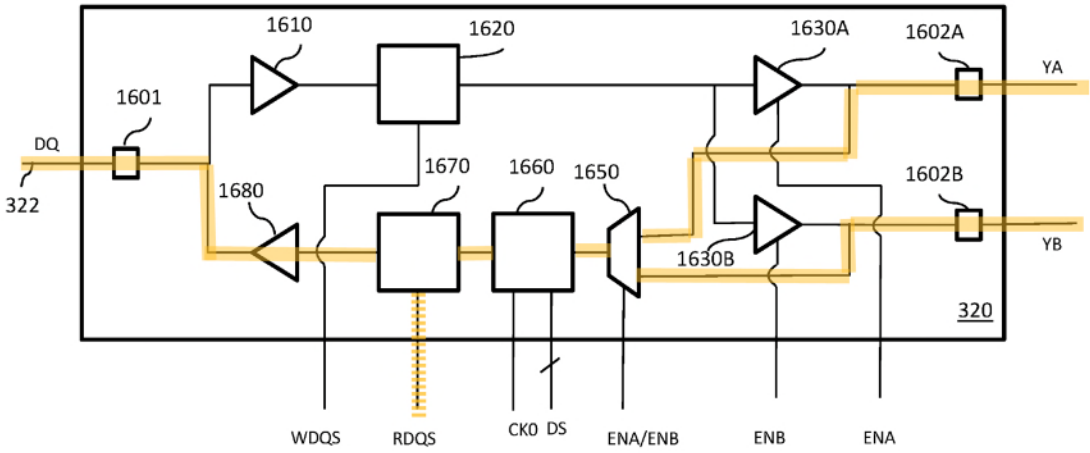

FIG. 16

223. A Skilled Artisan would have understood that the data path in Hiraishi includes a sampler, such as a register circuit, that samples the strobe signal in accordance with the local clock signal, and samples the data signal in accordance

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with the sampled strobe signal, similar to the data path disclosed in the '608 Patent. *See, e.g.*, EX1001 at 13:23-27 (disclosing that "a sampler or register circuit … samples the … signal … according to the …. clock signal"); *id.* at 17:10-13 ("The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0."). Hiraishi discloses in connection with a read operation that "***[a] phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372***, and ***then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal***." EX1005 (Hiraishi), [0091]. A Skilled Artisan would have understood that sampling happens at delay circuit 372 to delay the DQS signal by about 90 degrees, and that sampling happens in accordance with the local clock of the Data Register Buffer (for example, in order to detect the phase of the DQS signal). *See, e.g.,* EX1028 (US 9,536,579) at FIG. 2 (showing a phase comparator 35 formed by a D flip-flop (F/F) sampling the strobe signal DQS in accordance with a local clock CLKb to delay the strobe signal by 90 degrees); *see also id.* FIGS. 3–4. Thus, a Skilled Artisan would have understood that Hiraishi's delay circuit "*samples the strobe signal* [DQS] *in accordance with the local clock signal.*"

224. A Skilled Artisan would have understood from the disclosure of Hiraishi (alone or with Butt) that the data signal is sampled in accordance with the

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delayed, thus sampled, strobe signal when the data is clocked into the FIFO (Read) circuit (302). For example, a Skilled Artisan would have understood that Hiraishi's capture of the read data is similar to that in Butt disclosing that read data is sampled in accordance with a corresponding strobe signal in a register and the sampled data is buffered in a FIFO. EX1029 (Butt) at [0020] ("As briefly described above, the read datapaths 114 are generally programmable from when the data/strobe pairs DQ/DQS are received at the input to the circuit 104, to sampling the read data with the read data strobe signal DQS, and passing the data to the memory controller 102."). In particular, she would understand that this process requires a latch: the delay circuit 372 provides the sampled strobe signal that determines the timing for how the FIFO clocks in the data. A Skilled Artisan would have understood that, when the data signal is latched in the FIFO, it necessarily is sampled (registered) and because the delayed DQS signal acts "as an input trigger signal" to latch the data in the FIFO (Read) circuit 302, it is necessarily sampled in accordance with the sampled strobe signal. *See generally* Ex. 1021 (Jacobs textbook) at pp. 331, 332-35 (discussing using DQS strobe to sample data signal).

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11. Claim 11

225. Claim 11 recites "***The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte***."

226. As explained above in connection with claim 4, Hiraishi discloses that "each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte." *See supra* ¶¶ 192-193. Accordingly, claim 11 is obvious in light of Hiraishi for the same reasons.

12. Claim 12 is obvious over Hiraishi and Butt in further view of Ellsberry

227. Claim 12 recites "***The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.***" The Hiraishi-Butt combination alone and in view of Ellsberry renders obvious these limitations.

228. As explained above in connection with claim 5, Hiraishi (with Butt) alone and in view of Ellsberry renders obvious that "*each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.*" *See supra* ¶¶ 194-198. Accordingly, claim 12 is rendered obvious over Hiraishi (with Butt) alone and in view of Ellsberry for the same reasons discussed above with reference to claim 5. In particular, using 4-bit wide

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memory device in Hiraishi's module was obvious for the reasons discussed above with reference to claim 5.

B. Claims 1-12 are Obvious Over Hiraishi and Butt in View of Tokuhiro

229. As explained above, the '608 Patent discloses a first "*memory operation*" (e.g., write) that is in a different direction than a second "*memory operation*" (e.g., read). *See supra* ¶ 113. Under this claim interpretation, which is narrower than Netlist's interpretation addressed above in § V.A, claims 1-12 are obvious in light of Hiraishi and Butt in view of Tokuhiro (or in further view of Ellsberry and/or Kim) as explained below.

1. Tokuhiro's teaching

230. Tokuhiro teaches that a DDR3 memory interface employs fly-by topology for connection between a memory controller and a DIMM (Dual Inline Memory Module). EX1006 (Tokuhiro), 1:22-33. The JEDEC standards specify how to adjust timing in the fly-by configuration for write data, but do not specify a mechanism to adjust the fly-by delays of the read data. *See* EX1006 (Tokuhiro), 2:54-59 ("Although, the DDR3 memory interface compensates the arrival time when the data strobe signals DQS-1 to DQS-n arrive at the SDRAMs 92-1 to 92-n in the write operations according to the JEDEC standards as described above, compensations of the signal arrival time in read operations are not provided with the JEDEC standards."). Tokuhiro further explains that, with increasing speed of

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memories, such fly-by delays of the read data "will become greater than a typical data period of the DDR3 memory interface … so that the delay may affect in reading data." *Id*., 3:9-12. Thus, Tokuhiro teaches to a Skilled Artisan that fly-by delays need to be compensated for read data and not just for write data, and problems arise if the fly-by delay in read operations exceeds the clock period. Tokuhiro teaches techniques to solve this problem of inputting read data with large fly-by delays in a simple way using read delay units "without providing a special mechanism, such as an FIFO," where the read delays are obtained from the timing for write operations. *See, e.g., id*., 3:16-26, 18:66-19:7 ("Also, with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.").

231. In particular, Tokuhiro proposes delaying the transmission of the read data to compensate for those fly-by delays before the read data enters the common clock domain of the receiver. To implement these delays, Tokuhiro discloses "a ***second variable delay unit*** for delaying, in the ***read operation***, a data signal input

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from the memory ***by a second delay time***." *Id.*, 3:16-26. Tokuhiro also teaches that, for the read operation, the "***second delay time ... is set based on the first delay time***" which is determined using "a ***first variable delay unit for delaying***, in the ***write operation***, ***a data strobe signal output to the memory by a first delay time*** that is set by utilizing the write leveling function." *Id*.

232. Tokuhiro's embodiments are described in connection with unbuffered DIMMS where the memory controller (12) directly interfaces with the memory devices. *See, e.g.*, EX1006 (Tokuhiro), Fig. 7. For example, as illustrated in Tokuhiro's Fig. 7, the memory controller 12 directly controls the write leveling operation between the memory controller and the memory chips:

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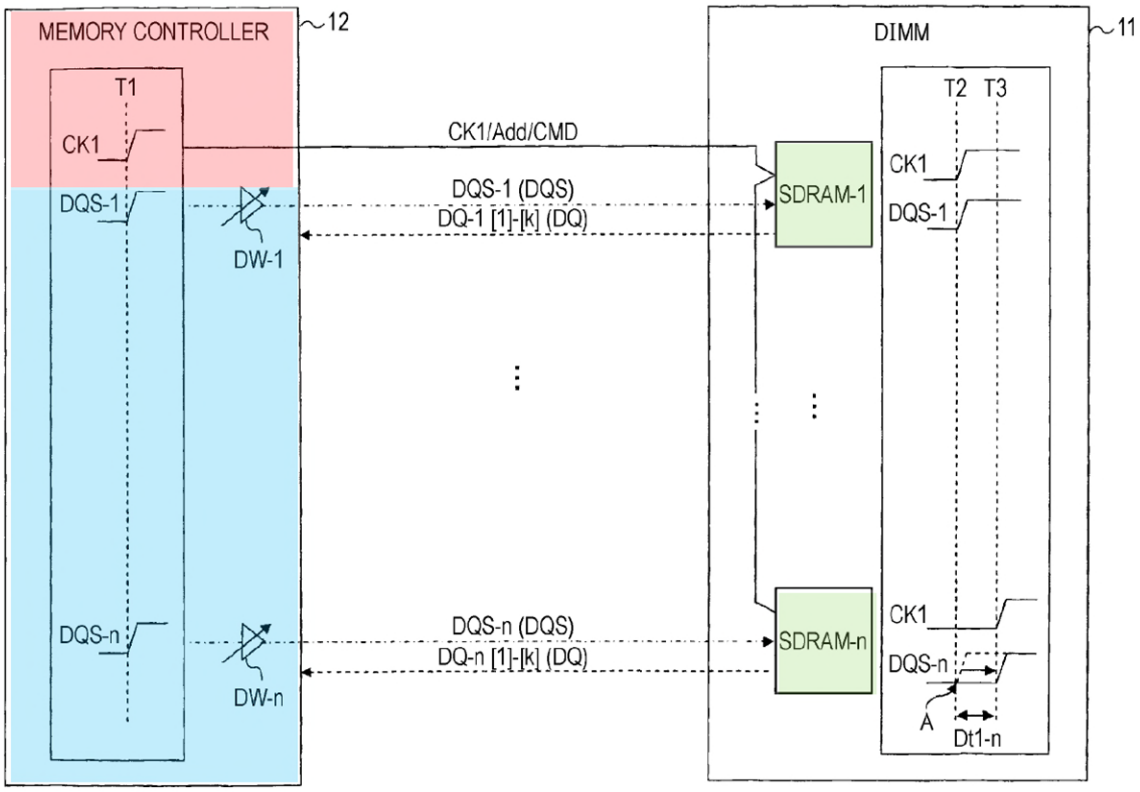
FIG. 7



233. Tokuhiro's FIG. 7 shows that, inside the memory controller (on the left side of the figure), the clock (CK1) and strobe (DQS-1, …, DQS-n) signals are all in sync, i.e., transitioning at the same time (T1). Accordingly, before write leveling (no delay applied by DW-1, … DW-n), the strobe signals arrive substantially at the same time (T2) to the DIMM (on the right side of the figure). The clock signal CK1 (and the corresponding address and command signals) arrives with different delays to the different memory devices (SDRAM-1, …, SDRAM-n; green) due to the "fly-by" arrangement of those memories. As an example, Tokuhiro illustrates that the clock CK1 arrives in sync with the DQS-1

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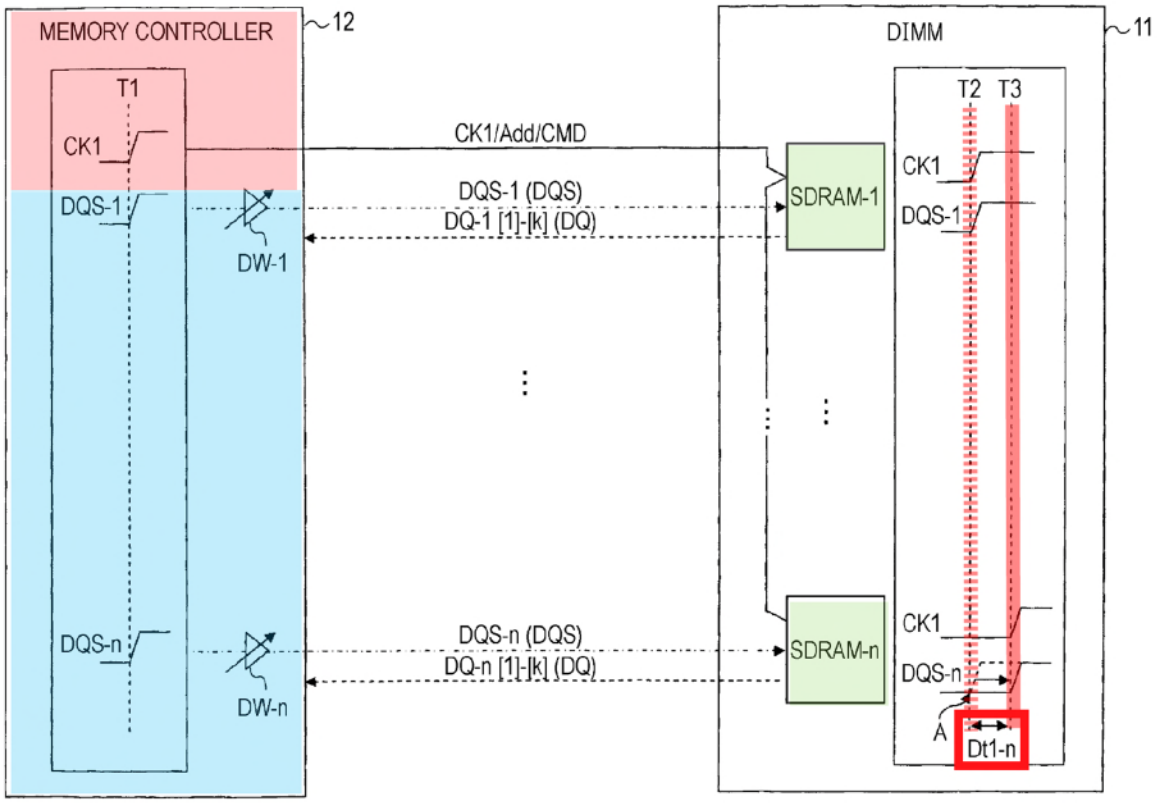
signal at time T2 (dashed red line) in SDRAM-1, but there is a delay Dt1-n (red box) when the clock signal arrives at the last device SDRAM-n in the fly-by arrangement at time T3 (solid red line). EX1006 (Tokuhiro) at FIG. 7 (reproduced below with annotations).

FIG. 7



During write leveling, the memory controller adjusts the delay unit DW-n to delay DQS-n by Dt1-n, allowing DQS-n to arrive at the same time (T3, solid red line) as the delayed clock signal CK1 at the n-th device SDRAM-n.

234. Tokuhiro teaches that the write delay Dt1 can also be used to determine delays for ***read*** data transmissions in order to compensate for large fly-by delays before the read data enters the clock domain of the memory controller.

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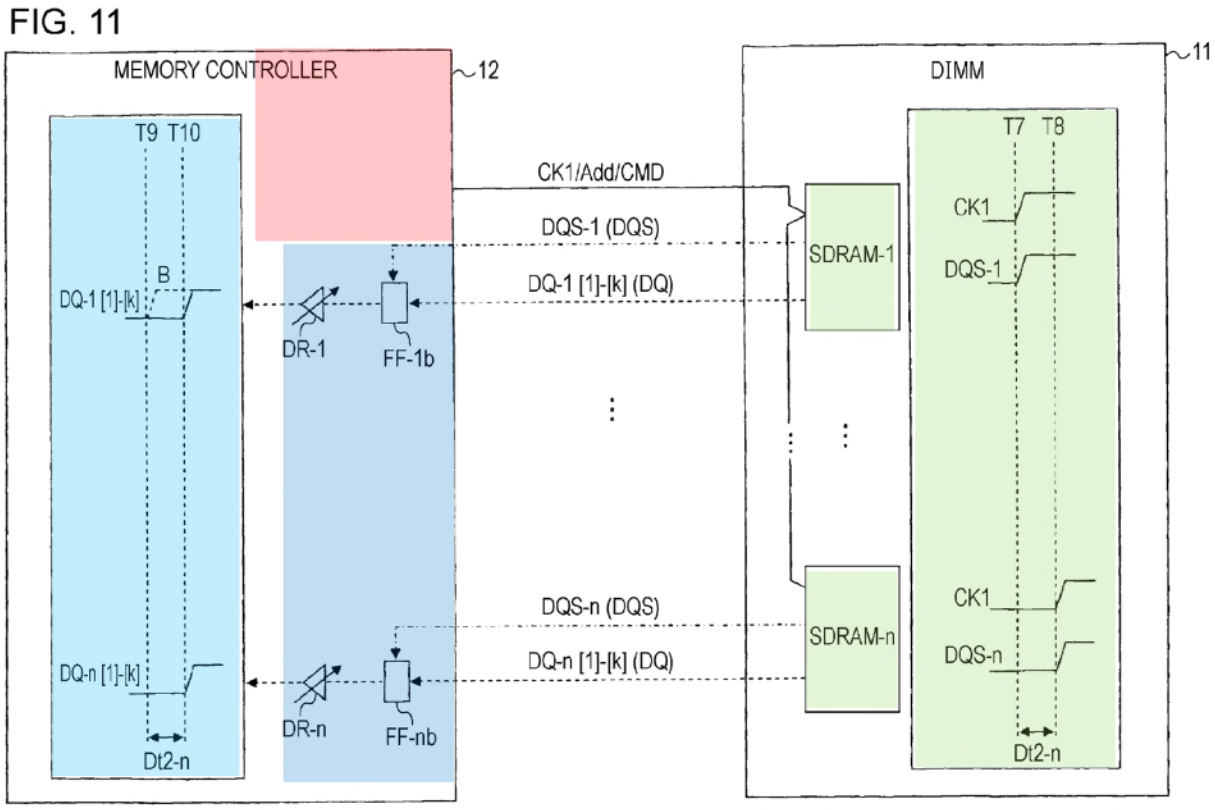
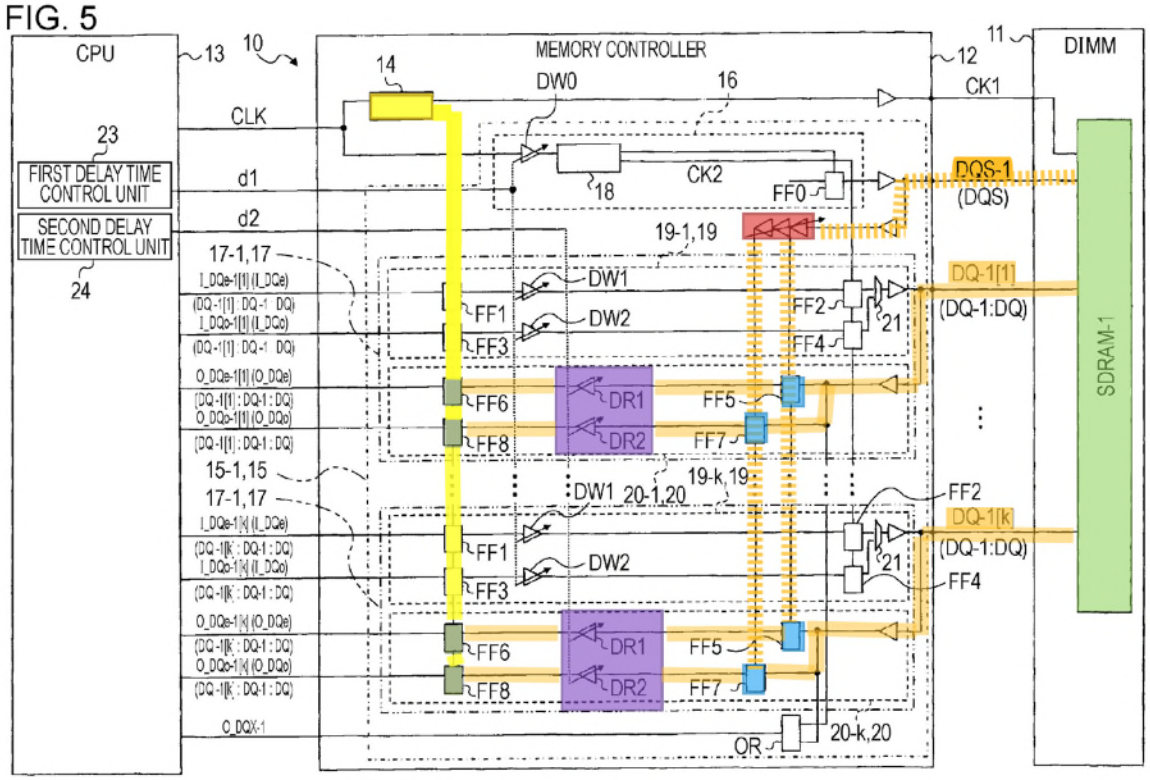
For example, Tokuhiro at FIG. 11 shows a read operation where data DQ-1 is transmitted from SDRAM-1 at T7 and data DQ-n is transmitted from SDRAM-n at T8 with a delay of Dt2-n. EX1006 (Tokuhiro) at FIG. 11 (reproduced below with annotations). Tokuhiro teaches that, after the read data is clocked into respective flip-flops FF-1b to FF-nb using the corresponding strobe signals, delay elements DR-1 and DR-n delay their respective read data such that, at T10, all corresponding data bits can be captured with the memory controller local clock. *Id*.

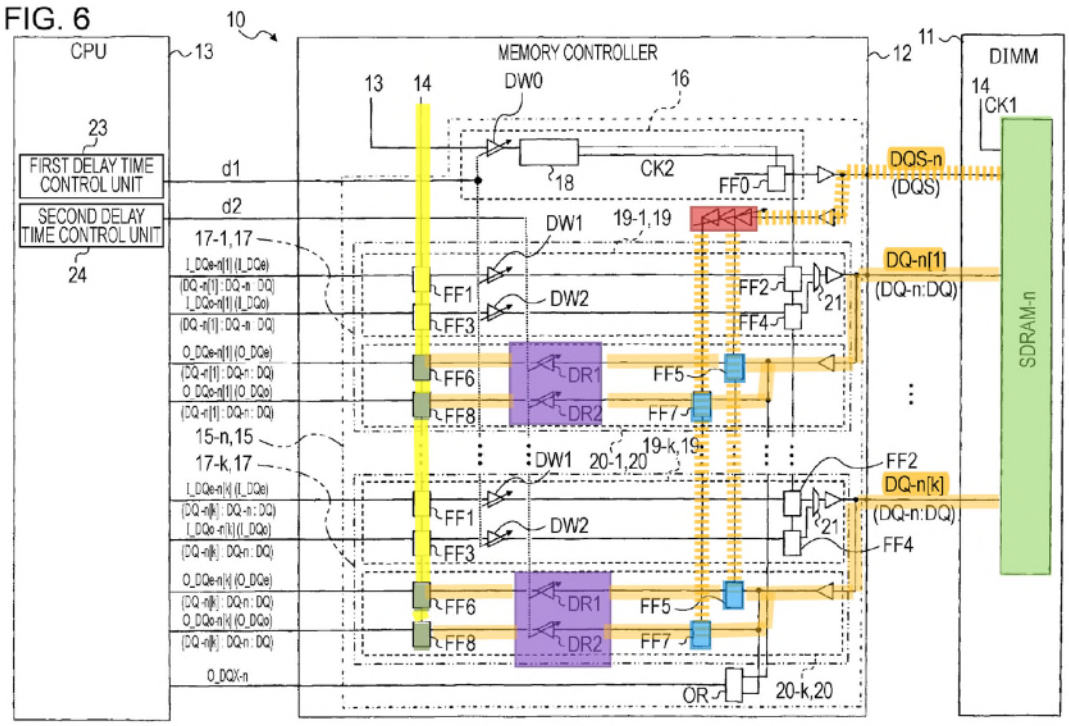


EX1006 (Tokuhiro), Fig. 11 (annotated).

235. As shown below, the details of delaying the data signals (solid orange) by the delay elements DR1 and DR2 (purple) before the values of those signals are captured by the flip-flops FF6 and FF8 (olive green) that use the clock domain (yellow) of the memory controller are illustrated by Tokuhiro's FIG. 5 (for SDRAM-1) and FIG. 6 (for SDRAM-n) (both reproduced below with annotations).

FIG. 5





236. Tokuhiro explains that, "with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO." EX1006 (Tokuhiro), 18:66-19:7. A Skilled Artisan would have understood from Tokuhiro's teaching that the delay elements DR1 and DR2 (purple) can compensate for fly-by delays of read data in a simple way using the delays for

write operations without special circuitry (such as FIFOs), even if the fly-by delay between two memory devices, such as between SDRAM-1 in FIG. 5 and SDRAM-n in FIG. 6, is larger than a clock cycle. EX1006 (Tokuhiro), FIGS. 5 and 6.

2. Motivations to Combine Tokuhiro and Hiraishi (in view of Butt)

237. Tokuhiro and Hiraishi are analogous art to the 608 patent since each is directed to improving memory systems using memory modules arranged in a configuration where synchronization issues arise due to signal delays, such as a fly-by configuration of modules using DDR3 memory chips. EX1001, e.g., at 8:22-34 ("in a fly-by configuration … issues can arise with respect to signal alignment…"); EX1005 (Hiraishi), e.g., at Figs. 14A-17 (explaining read and write leveling operations to compensate for signal delays), [0163] ("In a recent high speed memory such as a DDR3 DRAM, a use of the DLL circuit is substantially essential."); EX1006 (Tokuhiro) at 1:15-20 ("The memory control circuit, delay time control device, and delay time control method relate to a technique for controlling read/write operations for a plurality of memories to which a clock signal line is wired through the daisy chain connection, as in, e.g., a DDR3 memory interface, by supplying a clock signal through the clock signal line."). Therefore, a Skilled Artisan would have been motivated to look at Tokuhiro's teaching to implement Hiraishi's module with improved read and write leveling

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operations. In particular, a person of ordinary skill would have been motivated to combine Tokuhiro and Hiraishi for at least three reasons, discussed below.

a) First motivation: Tokuhiro teaches calculating read delays based on the delays for write operations, which is more efficient than Hiraishi's technique of performing read leveling independent of the write delays

238. As shown below, Hiraishi discloses that the data register buffers on the module (blue) buffer the data (DQ) and strobe (DQS) signals and, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner." EX1005 (Hiraishi) at [0104], FIG. 7.

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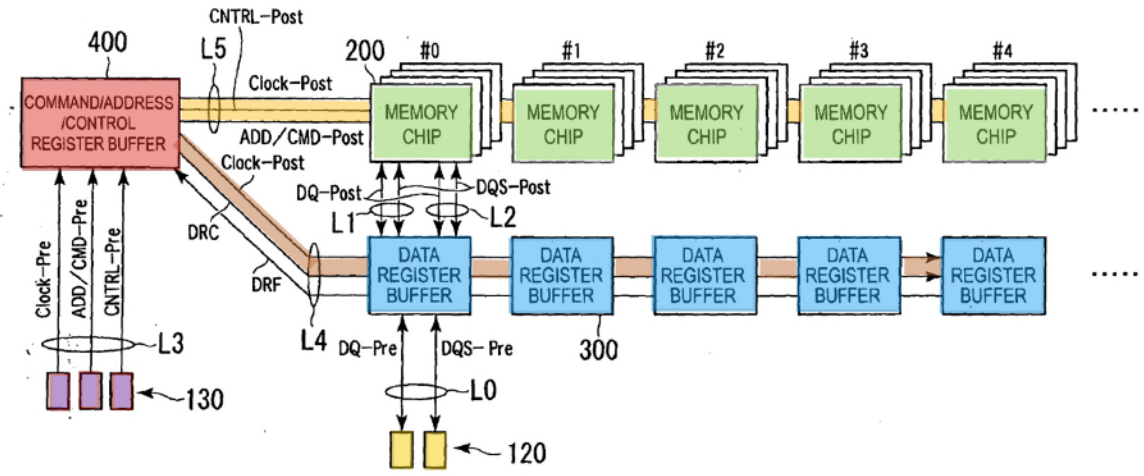

FIG.7

239. In Hiraishi, these timing adjustments include write and read leveling operations that are performed independent from each other. EX1005 (Hiraishi) at [0140] ("The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation."); *see also id.* at FIGS. 14A and 14B (explaining the write leveling operation between the data register buffer 300 and the memory chip 200), FIG. 15 (explaining the read leveling operation between the data register buffer 300 and the memory chip 200), FIGS. 16A and 16B (explaining the write leveling operation between the memory controller 12 and the data register buffer 300), FIG. 17 (explaining the read leveling operation between the memory controller 12 and the data register buffer 300).

240. For example, during Hiraishi's "S4" read leveling between the data register buffer and the memory devices, "the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like." EX1005 (Hiraishi) at [0151], FIG. 15.

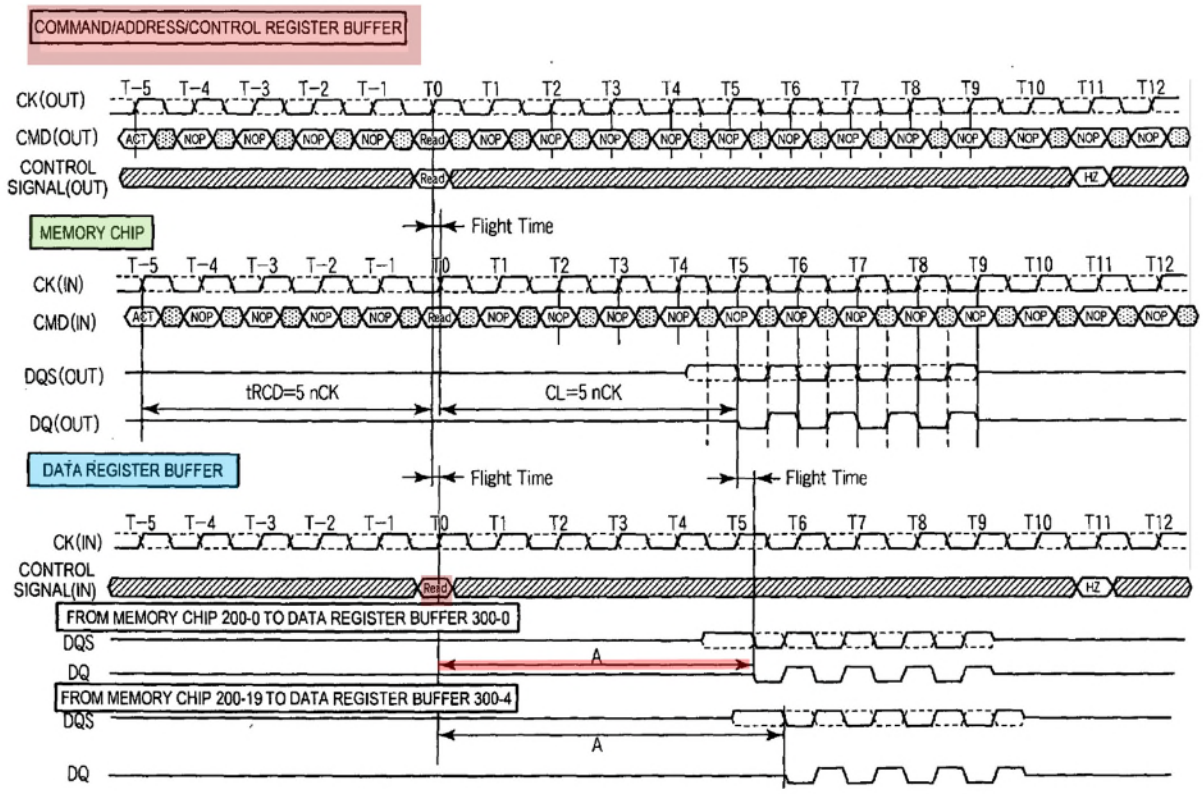

FIG.15

As a result of the read leveling, even though the data arrives from different memory devices at different times (as shown in Fig. 15 by the different times A for different memory devices), Hiraishi's S4 read leveling delays the data and strobe signals such that they are output at the same time in sync with the local clock signal. EX1005 (Hiraishi) at Fig. 11 and [0130] ("Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.").

241. Similarly, during Hiraishi's "S5" read leveling between the data register buffer and the memory controller, "the memory controller 12 can find a time B from an issuance timing of the read command Read until the read data DQ is input. The time is measured for each of the data register buffers 300, stored in the internal circuit of the memory controller 12, and used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like." EX1005 (Hiraishi) at [0161] and FIG. 17 (reproduced below).

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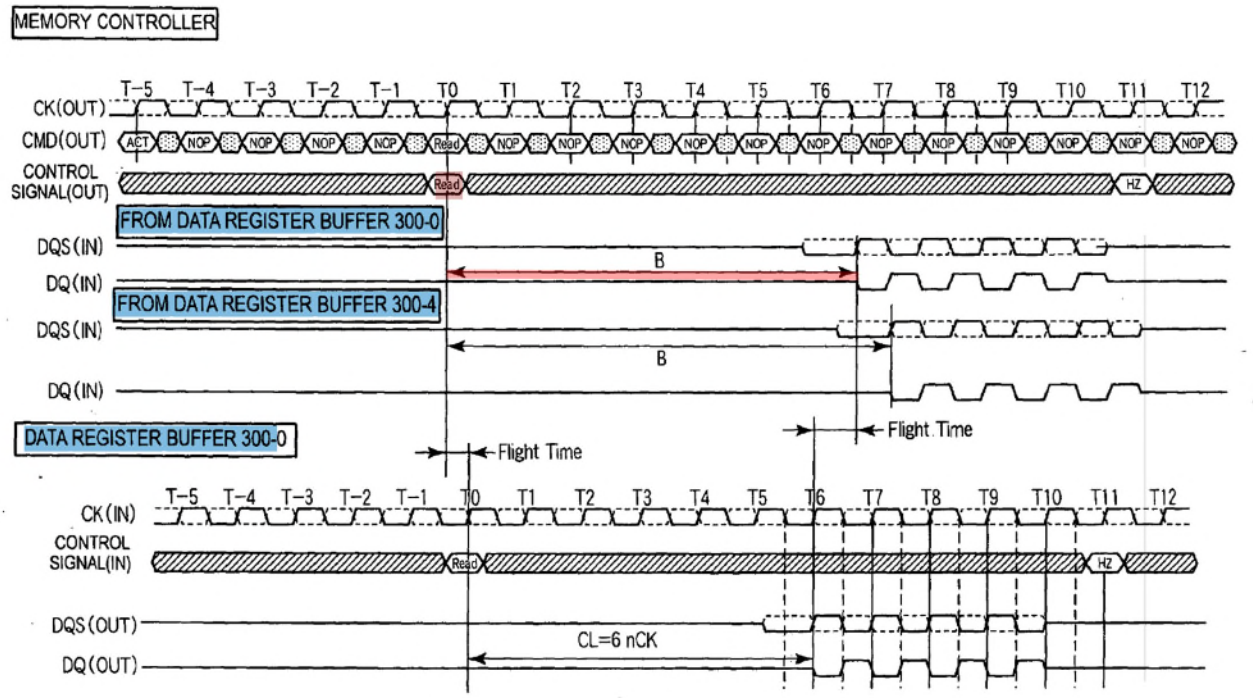

As shown in this figure, even though each of the data register buffers outputs the read data with a latency of CL=6 from receiving the Read command, the data arrives from different data register buffers at different times due to the fly-by delays (as illustrated by the different times B in Fig. 17). *Id*. at [0161] ("In FIG. 17, two cases are shown including a first case that the time B from the issuance of the read command Read until the input of the read data DQ is short (between the memory controller 12 and the data register buffer 300-0) and a second case that the time B is long (between the memory controller 12 and the data register buffer 300-4)."). Thus, the memory controller needs to deal with this time difference as part of the read leveling operation.

242. A Skilled Artisan would have understood that performing these write and read leveling operations independently as disclosed by Hiraishi would require time and corresponding circuitry in both the data register buffers and in the memory controller. Thus, a Skilled Artisan would have been motivated to simplify these write and read leveling operations and the corresponding circuitry.

243. For example, a Skilled Artisan would have understood that Tokuhiro discloses using the time delays found for write operations to determine the delays for read operations. EX1006 (Tokuhiro) at Abstract ("For each of the plurality of memories, a first variable delay unit delays, in a write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit delays, in a read operation, a data signal input from the memory by a second delay time that is set based on the first delay time."). Tokuhiro further explains that "with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO." EX1006 (Tokuhiro) at 18:66-19:7.

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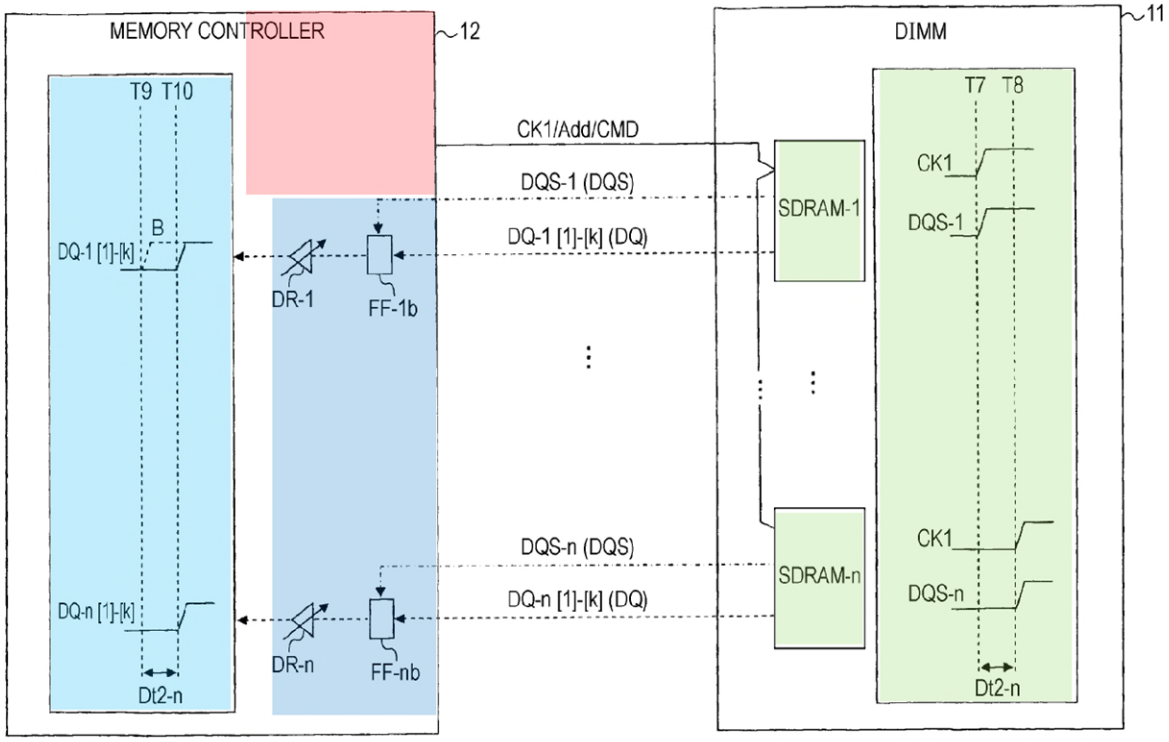
244. In particular, as shown below, Tokuhiro's FIG. 11 illustrates its technique of handling large fly-by delays of the memory devices (green) during a memory read operation where the memory controller's data handling part (blue), which interfaces with the memory devices, includes the read delay elements DR-1 to DR-n (reproduced below with annotations).

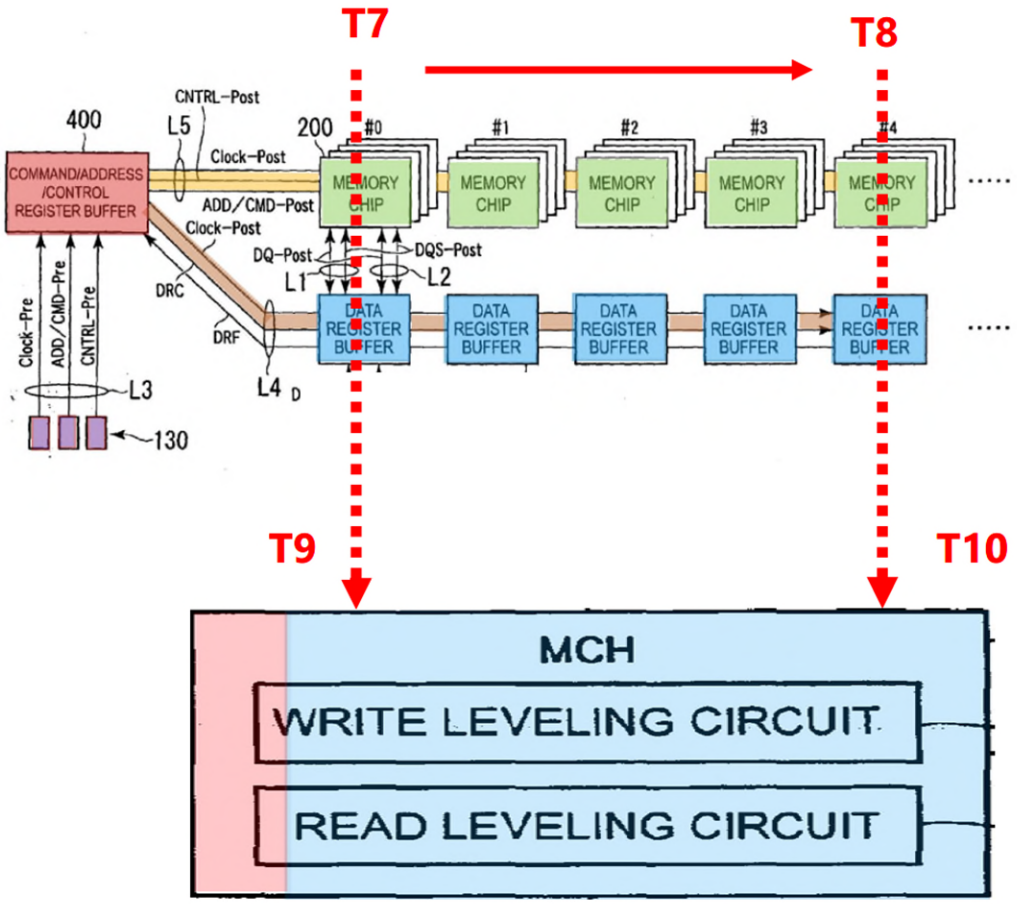
FIG. 11



During the read operation, the first memory in the chain (SDRAM-1) (upper right) sends the data strobe DQS (and the corresponding data signal) at T7, but the last SDRAM-n (bottom right) sends its data and strobe signals at T8, after a delay Dt2-n. Accordingly, the data arrives at the memory controller from SDRAM-1 at T9

(upper left), but from SDRAM-n only at T10, after the delay Dt2-n (bottom left). Tokuhiro's solution is that those delays are compensated by the read delay elements DR-1 to DR-n such that the data arrives from all the memories substantially at the same time T10 (light blue timing diagram), thus the properly delayed data can be captured in a single clock cycle of the memory controller.

245. The corresponding timing delays in Hiraishi's system are illustrated below in an annotated version of Hiraishi's FIG. 7 (with the MCH and timing added).



As shown by the added timing annotations, the memory devices in Hiraishi have similar fly-by arrangements, and thus similar fly-by delays, as in Tokuhiro. That is, if the first memory device (in group #0) starts sending the read data at time T7, the last memory in the chain (in group #4) will start sending its read data at a later time T8 due to the fly-by delay (solid red arrow). The data register buffers (dark blue) of Hiraishi have a fly-by arrangement similar to that of the memory devices, and thus they transmit the read data to the memory controller (MCH) with similar fly-by delays. In particular, the data register buffers transmit the read data with a pre-set latency from the time of receiving the read command which also arrives with those fly-by delays (on bus L4, horizontal in FIG. 7). EX1005, [0130]. A Skilled Artisan would have also understood that the transmission delays from the data register buffers to the memory controller are substantially the same for each of the data-buffer-to-controller data paths. Accordingly, the read data from the first memory (in group #0) will arrive at time T9 at the memory controller, and the read data from the last memory (in group #4) would arrive at time T10 at the memory controller with a large fly-by delay which is substantially the same as the fly-by delay considered by Tokuhiro (EX1006) in its FIG. 11. *Supra* at ¶244. Thus, the same problem of large fly-by delays happens in Hiraishi when the clock speeds of the memory devices increases.

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246. Furthermore, techniques for read and write leveling were known at the time, *see, e.g.*, EX1020 (JESD79-3C) at 26-27, 33, 42-45 (write leveling); *id.* at 31, 33, 48-54 (multi-purpose register for read calibration), and Netlist has asserted that read and write leveling are "memory operations" in the sense of the '608 Patent (which has the same disclosure as the '035 Patent). *See* EX1035 at 38-52; *see also* EX1048 at 54 (construing "memory operations" to be not limited to "ones involving writing to or reading from a DRAM"); EX1057 at 62 (pointing to delay from write leveling, EX1058 at 27). For example, Netlist points to mode register set and buffer control commands that are used during read and write leveling as corresponding to a "memory operation." EX1035 at 39, 42-43 (command tables including MRS, BCW Write, and BCW Read commands, i.e., mode register set, write buffer control word and read buffer control word commands, respectively, that are used during read and write leveling); *id.* at 49 (buffer control words for training, including read and write delay and host interface write training); *id.* at 50-52 (initialization including read delay training and write leveling operations).

247. Therefore, a Skilled Artisan would have been motivated to implement Tokuhiro's technique of setting the read delays based on the write delays in the memory system of Hiraishi in order to simplify the read leveling operations and the corresponding circuitry. Such a combination would have been well within the level of skill at the time, since Tokuhiro teaches in detail how to calculate the read

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delays based on the delays for write operations, and the combination would have provided what is expected from the combination: a memory system where the read leveling operation is simplified by using the write delays.

b) *Second motivation: Tokuhiro provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays*

248. As discussed above, Hiraishi discloses that, during the "S4" read leveling operation, its data buffer determines, for each memory device, a "time A" between the Read command and the arrival of the corresponding read data, and uses that time A for the "adjustment of an activation timing of the input buffer circuit INB and the like." EX1005 (Hiraishi) at [0151], FIG. 15. Hiraishi further discloses using a Read FIFO 302 for re-timing the read data and outputting the read data in sync with the local clock signal. *Id*. at [0130] ("Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.").

249. As also discussed above, Hiraishi discloses that, during the "S5" read leveling operation, its memory controller determines, for each data buffer, a "time B" between the Read command and the arrival of the read data, and uses that time B for "an adjustment of an activation timing of an input buffer circuit (not shown) and the like." EX1005 (Hiraishi) at [0161], FIG. 17. Hiraishi, however, does not

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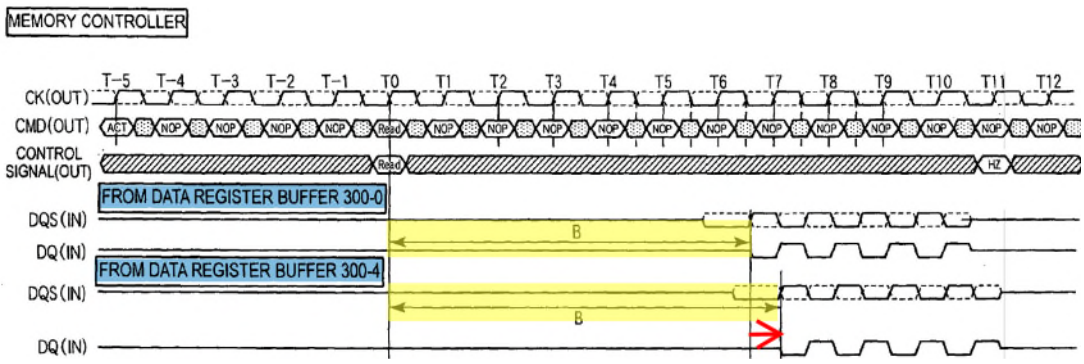
disclose the specific technique its memory controller uses for re-timing the read data from different data buffers to a common clock. Indeed, Hiraishi's Figure 17 shows that the read data arrives at the memory controller from different data buffers with different "time B." *Id*. at FIG. 17 (reproduced below in part with annotations).[3] That is, the memory controller in Hiraishi still has to remove the fly-by delay (red arrow) between the different data buffers. *Id*.



250. Tokuhiro, however, teaches that, "with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling

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[3] I note that, in Fig. 17 of Hiraishi, the numbering of the data register buffers starts from the module controller, just like in Fig. 7, with data register buffer 300-0 being in group #0, i.e., closest to the module controller, and data register buffer 300-4 being in group #4, i.e., farthest from the module controller. This is similar to the issue discussed above in footnote 2 on page 83.

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function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO." EX1006 (Tokuhiro) at 18:66-19:7. A Skilled Artisan would have understood from this disclosure of Tokuhiro that the delay circuits of Tokuhiro can be used in the memory module of Hiraishi to compensate for the fly-by delays between the different data buffers during a read operation so that the read data arrives at the memory controller from the different data buffers at substantially the same time. A Skilled Artisan would have also understood that, as a result of such a fly-by delay compensation in the memory module, the memory controller of Hiraishi would not have to manage large fly-by delays of read data, and could be implemented without "a special mechanism, such as an FIFO." EX1006 (Tokuhiro) at 18:66-19:7. A Skilled Artisan would have also understood that implementing such a fly-by delay compensation in the memory module would simplify the read leveling in the memory controller of Hiraishi and make the system's operation more reliable since the large fly-by delays of read data would be removed at an early stage so that the rest of the system does not have to manage such large fly-by delays.

251. Therefore, a Skilled Artisan would have been motivated to use Tokuhiro's technique of using delay circuits DR in the system of Hiraishi in order

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to match the input times of the respective read data signals in a simple way without using a special mechanism, such as FIFO based techniques.

c) Third motivation: Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not

252. Tokuhiro teaches that compensating for the fly-by delays of the read data is not specified by the JEDEC standards even though such delays can be larger than a clock cycle, which can cause problems at the receiver. *See* EX1006 (Tokuhiro), 2:54-59 ("compensations of the signal arrival time in read operations are not provided with the JEDEC standards"), 3:9-12 ("The delay on the order of 1 ns will become ***greater than a typical data period*** of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92."). Thus, Tokuhiro teaches to a Skilled Artisan that problems arise if the fly-by delay on read operations are not compensated, in particular if such delay exceeds the clock period, and teaches simple techniques to solve this problem of large fly-by delays at the arrival of read data based on timing for the write operations. *Id*., *e.g.*, 3:16-26.

253. Moreover, fly-by delays greater than a clock cycle was a known problem for persons of ordinary skill in the art. For example, U.S. Patent No. 9,263,103 to Giovannini ("Giovannini"), which was filed March 17, 2008, around the same time as Tokuhiro, also explains that a "'fly-by delay separation' which

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results from a difference in delay between the clock signal on the fly-by path and the data-strobe signal on a direct path ***can exceed one clock period***." EX1024 (Giovannini) at 2:17-20. "[I]f the fly-by delay separation between the clock signal and the data-strobe signal exceeds one clock period, the above-described timing adjustment process will adjust the phase relationship properly, but ***the timing adjustment may be off by a multiple of a clock period***." *Id*. at 5:25-31. To solve this known problem of fly-by delays that are larger than a clock cycle, Giovannini discloses a special, FIFO-based circuitry in the memory controller. *Id.* at 6:56-7:2.

254. The following annotated version of Hiraishi's Fig. 1 shows that Hiraishi suffers from the same potential problem identified by Tokuhiro of fly-by delays that can be greater than a clock cycle:

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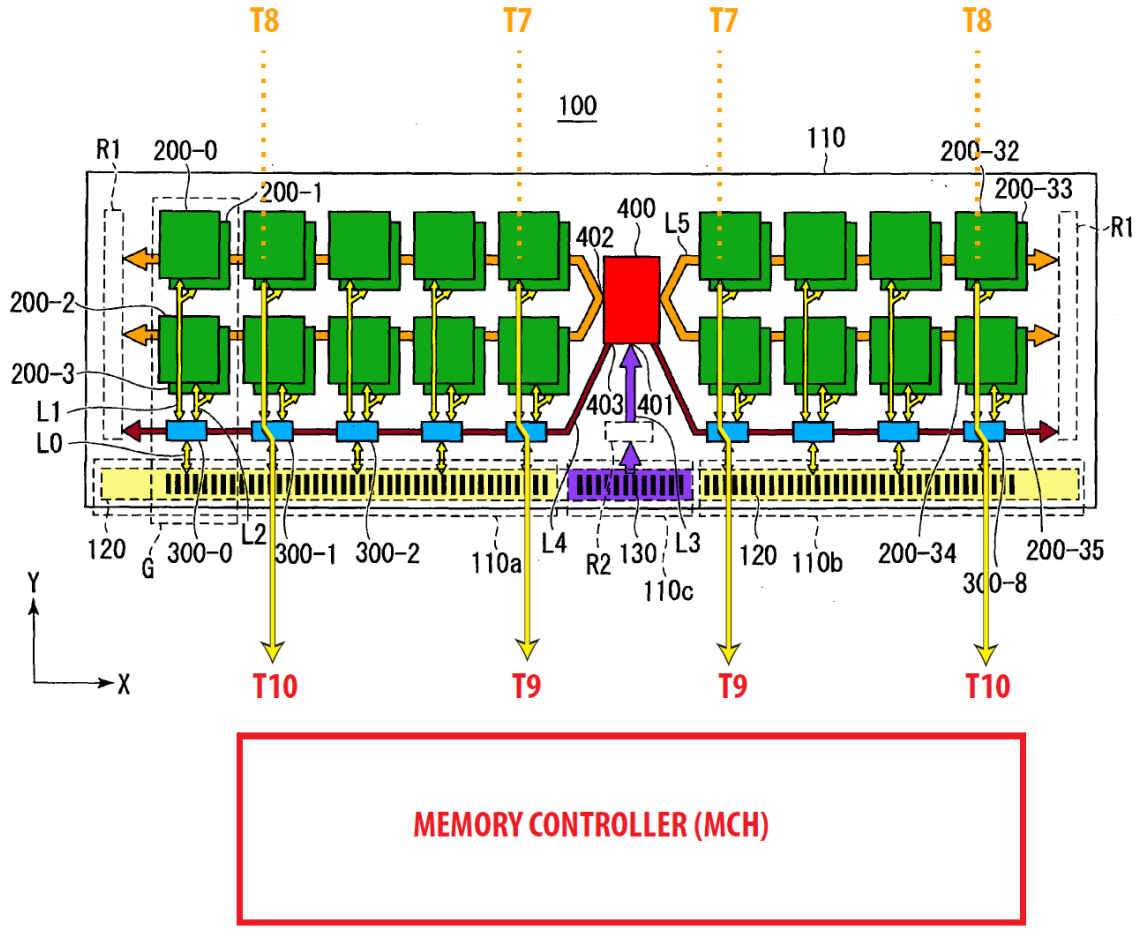

EX1005 (Hiraishi), Fig. 1 (annotated); *see also supra* ¶ 245 (similar annotation of Hiraishi Fig. 7). Here, times T7 to T10 correspond to the times shown in Fig. 11 of Tokuhiro. *See* EX1006 (Tokuhiro), 18:15-48. Tokuhiro teaches that due to fly-by delays, the memory devices nearer to the center of the module will execute the read command at T7 (and the memory controller will receive the data at T9), while the memory devices further from the center will execute the read command at T8 (and the memory controller will receive the data at T10). *Id*. Tokuhiro says there will be a problem when the difference between T9 and T10 is greater than one clock

cycle. *Id.*, 3:9-12. Tokuhiro says the solution is to add read delay elements DR to the inputs of the memory controller so that all the read data is processed by the memory controller at T10. *Id.*, 18:43-53 ("[a]s a result, the respective data signals DQ corresponding to the SDRAM-1 to the SDRAM-n are input to the CPU 13 substantially at the same time, whereby the read operation is executed.").

255. Thus, Hiraishi suffers from the same problem identified by Tokuhiro: Hiraishi transmits the read data from the buffers to the memory controller with fly-by delays. *See also* EX1014 ('632 Decision) at 13 (discussing Saito which has a similar disclosure than Hiraishi: "Saito describes using the determined time interval only to adjust the timing of an *input* buffer of memory controller 12, not to adjust the timing of *output* by data register buffer 300.") (emphasis in original). As the speed of the memories increases (and the clock period decreases), such large fly-by delays would be a concern in Hiraishi's system as well. EX1005 (Hiraishi) at [0005]. This is illustrated by a modified version of Hiraishi's Fig. 17, reproduced below.

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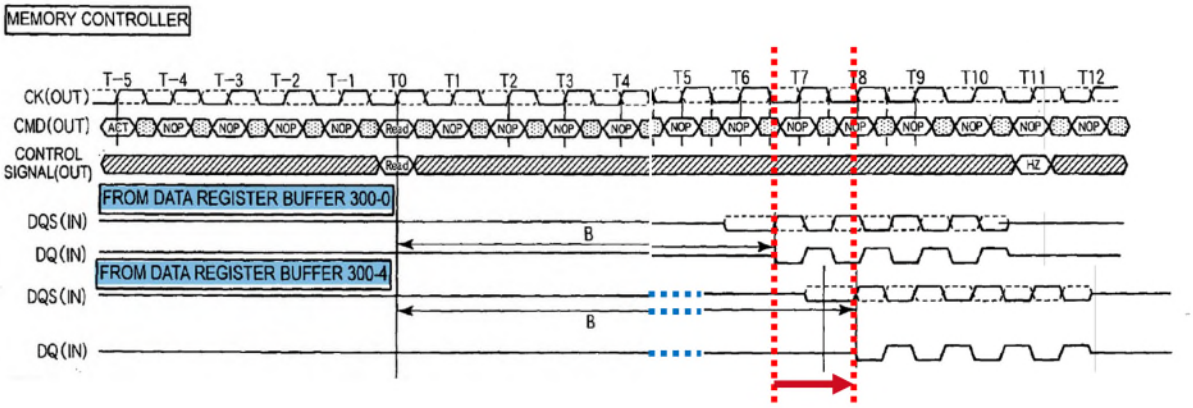

Here, for example, Fig. 17 has been modified such that the fly-by delay (red arrow) is increased to be longer than a clock cycle. This can happen, even if the physical dimensions of the module stay the same, if the clock cycle is shortened to allow for faster memory operations. In Hiraishi's system, the data buffers have separate local clocks having similar fly-by delays as the memory devices. In contrast, the system memory controller is a single device with its own local clock. As a result of the large fly-by delays in the modified version of Figure 17 above, Hiraishi's memory controller cannot simply capture, in the same clock cycle, both the first byte of read data from data register buffer 300-0 (left dashed red line) and the first byte of read data from the data register buffer 300-4 (right dashed red line), and instead would require circuitry and logic to re-align the read data that arrives with more than a clock cycle of fly-by delay. *See, e.g.*, EX1024 (Giovannini) at 6:56-7:2 ("'Read-alignment' (also referred to as 'read-data-alignment') involves synchronizing the read data to the same clock signal as the read data comes out of,

for example a first in, first out buffer ('FIFO') in the memory controller and is provided to the core of the memory controller."). Thus, a Skilled Artisan would have understood that large fly-by delays cause problems, in particular with reception of the read data in the memory controller.

256. Further, a Skilled Artisan would have understood that the fact that Hiraishi teaches read leveling in the memory controller (*see, e.g.,* EX1005 (Hiraishi), Fig. 2) does ***not*** necessarily solve the problem of larger-than-clock-cycle fly-by delays. Indeed, Hiraishi describes the read leveling operation between the memory controller and the data register buffer with reference to FIG. 17, including the memory controller measuring a time B, which is "used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like." EX1005, ¶[0161] and FIG. 17. Adjusting the activation timing of the input buffer circuit, however, does not align the read data with the local clock of the memory controller. Thus, without any further processing, read data with larger than clock cycle delays at the end of the fly-by chain would be latched at different cycles. Hiraishi, however, is silent about any solution in the memory controller for fly-by delays *greater* than one clock cycle, and instead only shows fly-by delays *less* than one clock cycle. *See, e.g.,* EX1005 (Hiraishi) at FIG. 17 (annotated above at ¶249 showing a fly-by delay (red arrow) which is less than a clock cycle). Therefore, Hiraishi is silent about the details of its read leveling operation in the

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memory controller, in particular, about larger-than-clock-cycle delays or how to handle the problems caused by those delays. A Skilled Artisan would have known about these problems, motivating her to look for solutions.

257. Tokuhiro, for example, discloses that, "with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO." EX1006 (Tokuhiro) at 18:66-19:7.

258. Thus, a Skilled Artisan would have been motivated to use Tokuhiro's technique of using delay circuits DR to get rid of the fly-by delays of the read data before that data is input to the local clock domain of the memory controller, so that the memory controller does not need special FIFO-based circuitry for re-timing the read data.

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3. The combination of Hiraishi in view of Butt and in further view of Tokuhiro relied upon here

a) It would have been obvious to implement Tokuhiro's delay elements in Hiraishi's data register buffers

259. As discussed above, a Skilled Artisan would have been motivated to implement Tokuhiro's technique of delaying read data based on delays for write operations so that the read data from all the memory devices arrive at substantially the same time in the clock domain of the memory controller. A Skilled Artisan would have also understood from Tokuhiro's disclosure that it was advantageous to implement Tokuhiro's delays in the data buffers of Hiraishi.

260. For example, a Skilled Artisan would have understood that, if Tokuhiro's delays of the read data are implemented in the data buffers of Hiraishi and those delays are determined from the delays for write operations, the memory controller does not have to manage large fly-by delays of read data and the memory controller does not require any extra circuitry (e.g., FIFOs) to handle those large delays. Accordingly, a Skilled Artisan would have been motivated to implement Tokuhiro's read data delaying technique in the data register buffers of Hiraishi, including determining delays for write operations and using those write delays to determine read delays for read operations.

261. In particular, it would have been obvious to a person of ordinary skill to implement Tokuhiro's delay elements in Hiraishi's data register buffers (rather

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than in the memory controller), and such a person would have had a reasonable expectation of success in making such a combination. For example, Tokuhiro teaches to apply the read delay (e.g., DR-1, purple) immediately after the corresponding read data from the memory (SDRAM-1, green) has been latched (e.g., by flip-flop FF5, blue, in red box), as illustrated in an annotated version of Tokuhiro's Figure 5 below (upper left). Hiraishi teaches that the read data from the memory (DRAM, green added) is latched into FIFO (Read) Circuit 302 (blue, in red box). EX1005 (Hiraishi), FIG. 5 (reproduced below, lower right, with annotations). Accordingly, a Skilled Artisan would have been motivated to add Tokuhiro's read delay elements (e.g., DR-1) to Hiraishi's data register buffer immediately after the read data from the memory is latched.

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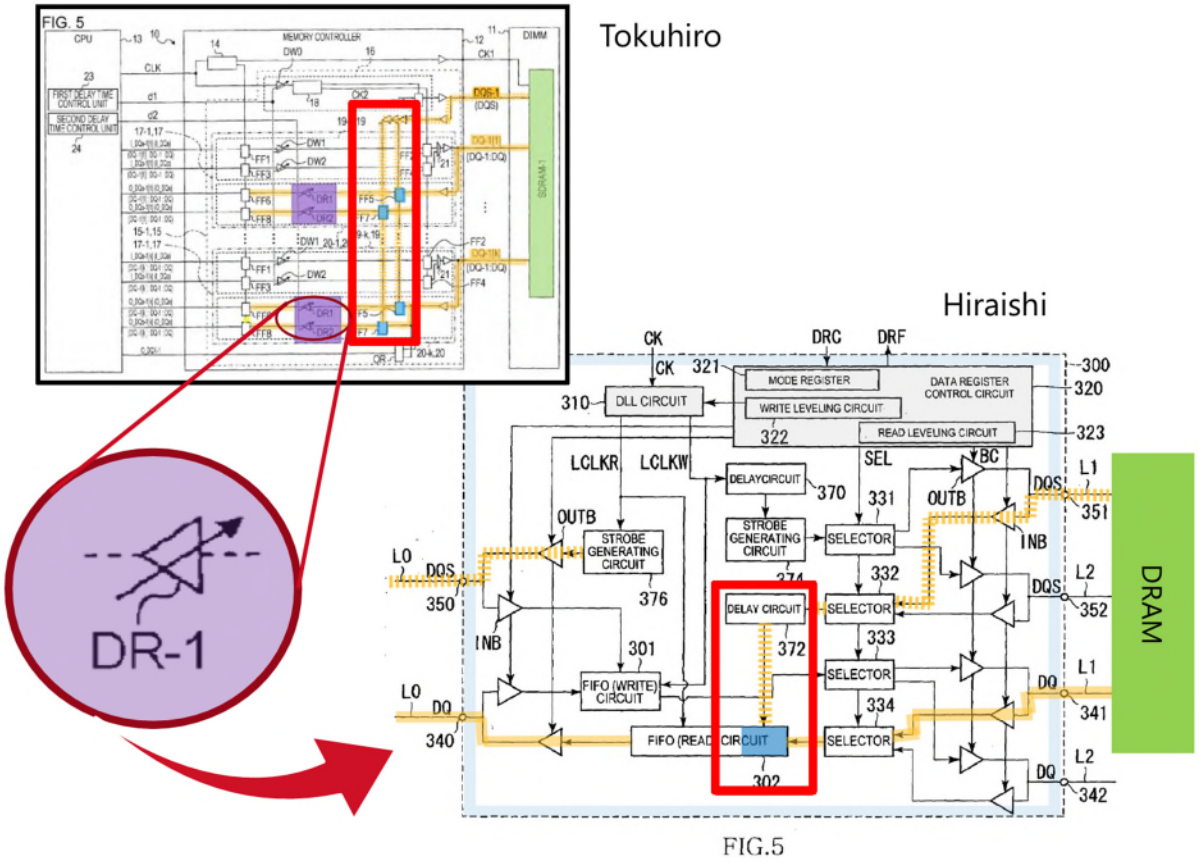

FIG.5

Annotated version of Tokuhiro Fig. 5 and Hiraishi Fig. 5

262. A Skilled Artisan would have understood that, in a read operation, the data signal (DQ, 340) is transmitted from the data buffer to the memory controller with a corresponding strobe signal (DQS, 350) which is in sync with the data signal. EX1005 (Hiraishi), FIG. 5. Thus, a Skilled Artisan would have understood that the strobe (DQS) and data signals (DQ) have to be in sync after Tokuhiro's read delay has been added to Hiraishi's data buffer. Delaying both data and strobe signals were well known in the art, and one such implementation is disclosed even

by Tokuhiro for the write operations. *See, e.g.*, EX1006 (Tokuhiro) at FIGS. 5-6 (showing delay element DW0 for a strobe signal and delay elements DW1 and DW2 for data signals) and 9:33-40 ("More specifically, a first delay time Dt1-1 is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-1 shown in FIG. 5. Likewise, a first delay time Dt1-n is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-n shown in FIG. 6.") A Skilled Artisan would have understood that the same functionality can be implemented in the data buffer of Hiraishi to delay the transmission of read data along with its strobe signal to the memory controller. An example of such an implementation is illustrated in a modified FIG. 5 of Hiraishi below.

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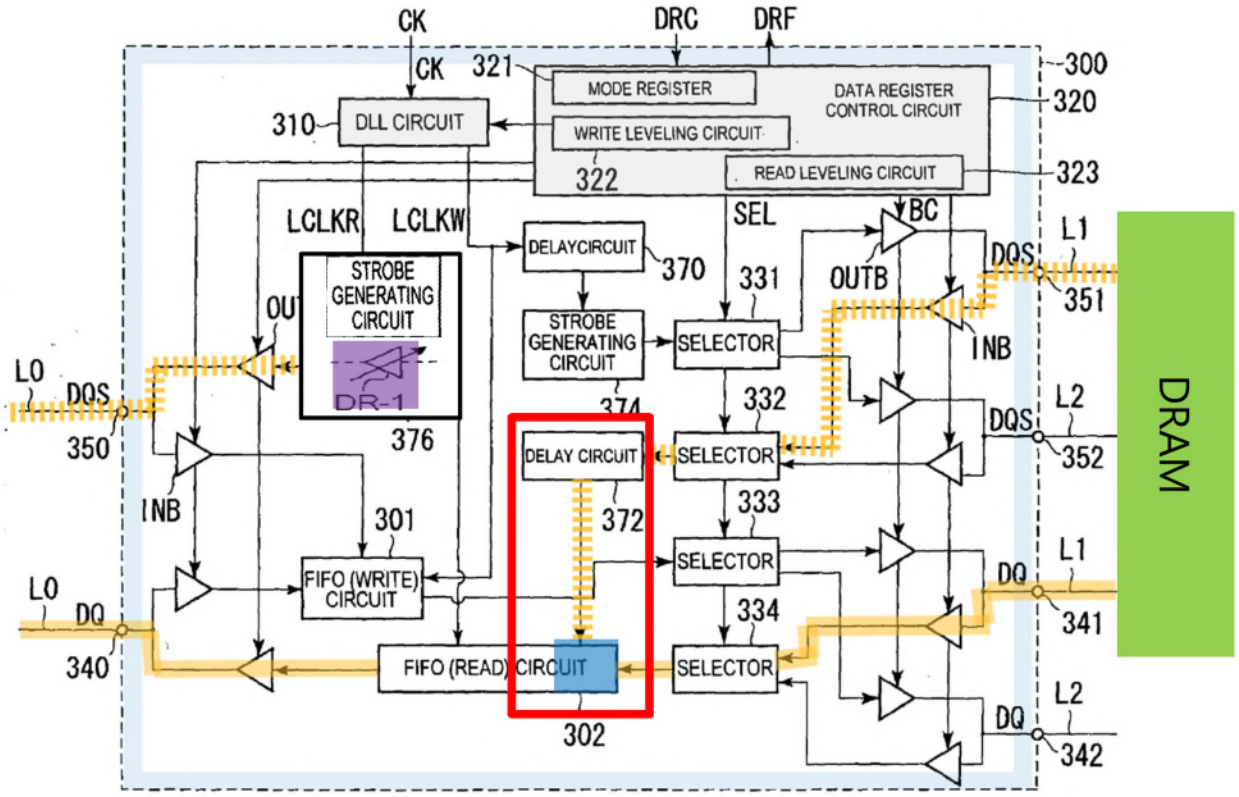

FIG.5

In this exemplary implementation, Tokuhiro's read delay circuit (DR-1, purple) is added to Hiraishi's strobe generating circuit 376 to implement the functionality of delaying both the read data strobe signal 350 (dashed orange) and the signal used to clock out the data from the FIFO (Read) circuit 302 in order to synchronize the read data 340 with its strobe 350. *See, e.g.,* EX1020 (JESD79-3C), p. 56 (Fig. 25 showing read data output in synchronization with the corresponding strobe). I note that, in this implementation, Hiraishi's existing read FIFO circuit is adapted to delay the read data, so there is no need to add delay circuits to the data line (DQ). A Skilled Artisan would have also understood that, in alternative implementations,

delay elements similar to Tokuhiro's DR elements can be used instead of or in addition to Hiraishi's FIFO circuit for delaying the read data.

263. In Hiraishi, the memory devices interface with the data register buffers, not directly with the memory controller (MCH), as illustrated in the annotated FIG. 5 of Hiraishi above. Hiraishi also expressly teaches a Skilled Artisan to implement read and write leveling circuitry in each data buffer as part of the functionality of interfacing with the memory devices, in addition to write and read leveling circuitry in the memory controller. *See, e.g.,* EX1005 (Hiraishi) at FIG. 5 (illustrating write and read leveling circuits 322 and 323 in the data buffer) and FIG. 2 (illustrating write and read leveling circuits in the MCH); Fig. 13 (identifying S4 read and write leveling, which takes place between buffers and memory devices, as a separate step from S5 read and write leveling, which takes place between buffers and memory controller). Since Hiraishi already teaches read (and write) leveling circuitry in the data register buffers, a Skilled Artisan would have been motivated to implement the functionality of the delay elements (DR) of Tokuhiro in the data buffers of Hiraishi to delay transmission of read data in order to compensate for the fly-by delays of the data register buffers of Hiraishi.

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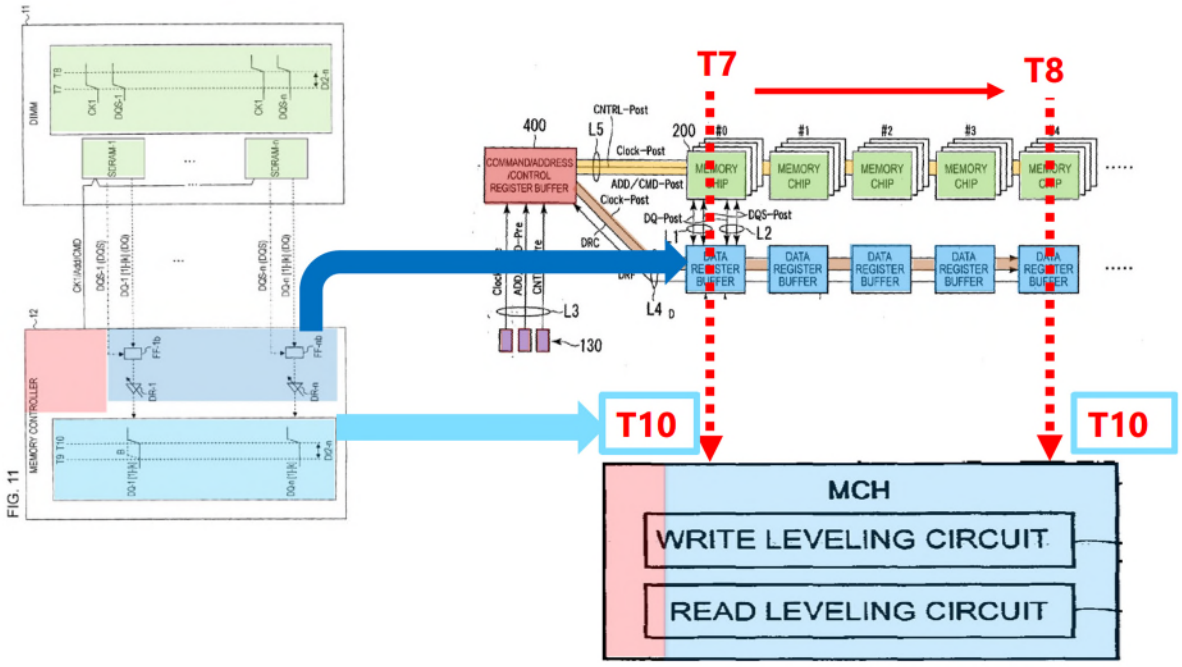

264. As illustrated above in the annotated FIG. 11 of Tokuhiro (on the left above) and FIG. 7 of Hiraishi (on the right above), the combination implements the functionality of the additional read delay of Tokuhiro in the data register buffers of Hiraishi (as illustrated by the dark blue arrow). As a result of these additional read delays, the read data arrives to the memory controller (MCH) at substantially the same time (T10) despite the fly-by delay (from T7 to T8) on the memory module. In the annotated figures above, the light blue arrow illustrates that the additional read delays compensate for the fly-by delays in accordance with Tokuhiro's teaching by delaying the read data so that it all arrives from each data buffer at substantially the same time. As a result, the memory controller can capture the

corresponding read data from all the memories in a single clock cycle even if the fly-by delays on the module are larger than a clock cycle. In particular, as a result of the additional delays implemented in the data register buffers of Hiraishi, the data from all of the data registers would arrive to the MCH without fly-by delays, at substantially the same time (T10).

265. A Skilled Artisan would have understood that an important advantage of this combination is that the memory controller (MCH) receives all read data at substantially the same time, so it does not have to manage large fly-by delays of read data either during the training or during normal operation as it tries to capture the correct value of the read data. Accordingly, the memory controller can be implemented with less circuitry and functionality. For example, the memory controller does not need extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles due to the larger than clock cycle fly-by delays on the module.

266. Furthermore, a Skilled Artisan would have also understood that the advantages of implementing Tokuhiro's read delays in the data buffers of Hiraishi include that it would remove the large fly-by delays on the module at the first practically available location, so that the rest of the system does not have to manage those large fly-by delays. Indeed, as Tokuhiro explains, the JEDEC standards did not provide a solution for the read leveling in the memory devices,

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thus JEDEC-compliant memory devices do not have Tokuhiro's read delay elements. EX1006 (Tokuhiro) at 2:54-59. A Skilled Artisan, however, would have understood that Hiraishi's data buffer can include delay elements like those of Tokuhiro, since it already includes both read and write leveling functionality. Accordingly, a Skilled Artisan would have been motivated to implement Tokuhiro's read delays in the data buffers of Hiraishi.

267. In addition, I understand that, when there is a design need to solve a problem, and there are a finite number of identified predictable solutions to the problem, all of those solutions likely are obvious. Here, a Skilled Artisan would have understood that, in the combination of Hiraishi and Tokuhiro, the delay elements of Tokuhiro can be implemented either in the data buffers or in the memory controller of Hiraishi, rendering both of those solutions obvious.

b) It would have been obvious for either of Hiraishi's memory controller and module controller to program Tokuhiro's delay elements in Hiraishi's data buffers

268. A Skilled Artisan would have understood that there are two potential ways to implement Tokuhiro's technique of adding read delay elements to Hiraishi's data register buffer to solve the problem of large fly-by delays: (1) the system ***memory controller*** can determine the read delays based on the timing for a write operation and, in turn, program the read delay elements in the data register buffers on the module accordingly, or (2) the ***module controller*** and/or data

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register buffers on the module can determine the read delays based on the delays measured by the data register buffers during a write operation and, in turn, program the read delay elements in the data register buffers accordingly. *See, e.g.,* EX1006 (Tokuhiro), 16:18 (Formula 3-6 for calculating the read delays from the write delays, including the maximum of those write delays). Either way can satisfy the claims, at least under Netlist's broader interpretation as discussed above in ¶ 113.

269. The first implementation (where the ***memory controller determines the fly-by delays***) would read on limitation 1[f] under Netlist's apparent claim construction, *see supra* ¶ 113, since Netlist has asserted that infringement happens when the memory controller programs the data buffers with certain timing parameters. *See, e.g.*, EX1035 (Netlist Complaint against Micron) at ¶121 (pointing to the memory controller programming the timing in the data buffers); *see also* EX1057 at 62 (pointing to parameters programmed during read and write leveling by the system memory controller, EX1058 at 26-27).

270. The second implementation (where the ***controller and/or data buffers on the module determine the fly-by delays***) would read on the limitations of claim element 1[f] under an interpretation more consistent with the specification and the claim language of the 608 patent. The interpretation most consistent with the specification requires that it is the "command processing circuit" in the data buffer,

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as opposed to the memory controller, that determines the amount by which to delay a signal through the data path.

271. As discussed above, a Skilled Artisan would have been motivated to implement the teaching of Tokuhiro to determine the specific delays for the read delay elements in the data buffers of Hiraishi based on the delays for the write operations. *Supra at* ¶¶ 238-247. A Skilled Artisan would have also understood that using delays for the write operations to determine the fly-by delays for read operations would have worked for its intended purpose as taught by Tokuhiro because, as discussed below, either the ***memory controller*** can determine the fly-by delays *during* write leveling or, alternatively, the ***data buffers*** can detect the fly-by delays Dt1 *before* write leveling, when the memory controller issues a write command to the memory module. In either case, the result is that the memory controller does not have to manage large fly-by delays when trying to capture the read data.

272. **As to the first method** of utilizing the teachings of Tokuhiro in the memory system of Hiraishi, the memory controller in Hiraishi can determine the fly-by delays on the module during write leveling as taught by Tokuhiro. *See supra* ¶¶ 232-233; EX1006 (Tokuhiro), Fig. 7 (annotated). Tokuhiro further explains that these Dt1 delay times obtained from write leveling are used to set the delays Dt2 for the read data. *Supra* ¶¶ 234-236. For example, "the second delay

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times Dt2-1 to Dt2-n corresponding respectively to the SDRAM-1 to the SDRAM-n are set so as to become shorter gradually in the order from the 1-channel SDRAM-1 toward the n-channel SDRAM-n." EX1006 (Tokuhiro) at 16:43-46.

273. Thus, in this first implementation of the combination of Hiraishi and Tokuhiro (under Netlist's apparent interpretation), a Skilled Artisan would implement Tokuhiro's calculation of the fly-by delays based on write leveling in Hiraishi's memory controller and, based on these fly-by delays, the memory controller would program the additional read delay elements in the data buffers. In particular, a Skilled Artisan would have implemented Hiraishi's leveling operations between the memory controller and the data buffers (Step S5 of Fig. 13) by the memory controller performing write leveling first, programming the read delay elements in the data buffers based on the write delays next, and performing the simplified read leveling last. EX1005, Fig. 13 (reproduced below with annotations in accordance with the first implementation of the Hiraishi-Tokuhiro combination). As taught by Tokuhiro, the result of this combination is that the read data arrives to the memory controller without substantial fly-by delays, thus simplifying the memory controller's job and circuitry for properly capturing the read data. For example, the memory controller does not have to compensate for fly-by delays in the read data, although it may still require read training to activate the input buffers in time and, if necessary, to adjust the phase of a local clock "for

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matching the phases of the read data DQ and the data strobe signal DQS."

EX1005, [0161], [0163].

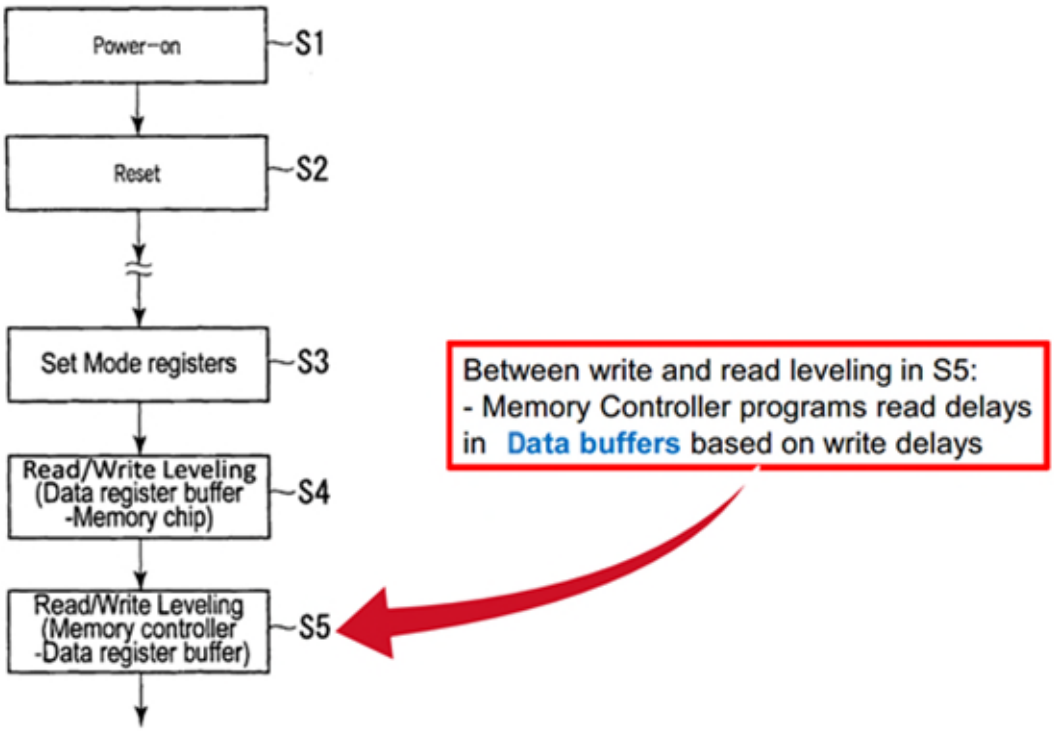

FIG.13

EX1005 (Hiraishi) Fig. 13 (annotated).

274. This implementation was well within the level of ordinary skill and provided nothing more than what was expected from the combination. For example, implementing Tokuhiro's read delay functionality in Hiraishi's data register buffers required adding a known function (delaying the read data as taught by Tokuhiro) to a known data register buffer of Hiraishi, where the data register buffer already had similar functionalities, including read and write leveling

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functions. Similarly, since Tokuhiro already taught how to calculate and set those read delays, a Skilled Artisan would have understood how to modify Hiraishi's memory controller to add the same functionalities. The result of the combination is as expected: a memory system in which the memory controller does not have to manage large delays, in particular larger than a clock cycle, when trying to capture the correct values of read data.

275. **As to the second method** of utilizing the teachings of Tokuhiro in the memory system of Hiraishi, a Skilled Artisan would have understood that Tokuhiro's technique can also be implemented in Hiraishi's memory module such that the ***buffer circuits*** measure timing information to determine the fly-by delays during a write operation, and Hiraishi's module controller can be implemented to program the corresponding read delays in the data buffers with more than a reasonable expectation of success.

276. A Skilled Artisan would have been motivated to implement Tokuhiro's technique in Hiraishi's module, as opposed to the memory controller, because Hiraishi already teaches that functionalities of the memory controller, including interfacing with the memory chips and performing read and write leveling, can be performed by the controller and data register buffers of the memory module. *See, e.g.*, EX1005 (Hiraishi) at FIG. 5 (showing write and read leveling circuits 322 and 323). For example, Hiraishi expressly teaches that "the

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data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input." EX1005 (Hiraishi) at [0151]. In addition, Tokuhiro explains that, before the write leveling, the write strobe signals arrive to the module at substantially the same time (T2), but the corresponding clock/address/command signals have respective fly-by delays in the chain (such as a delay Dt1-n for the n-th device). EX1006 (Tokuhiro), FIG. 7 (reproduced below with annotations); *see also* FIG. 10, 13:30-37 ("For example, ***before the first delay time Dt1 is adjusted based on the write leveling function***, as shown in FIG. 7, the clock signal CK1 and the data strobe signal DQS-1 are input to the 1-channel SDRAM-1 substantially at the same time (see a time 'T2' in FIG. 7), while the clock signal CK1 is input (see a time 'T3' in FIG. 7) to ***the n-channel SDRAM-n with a delay of the time Dt1-n after the input of the data strobe signal DQS-n*** (see the time 'T2' and a point 'A' in FIG. 7).").

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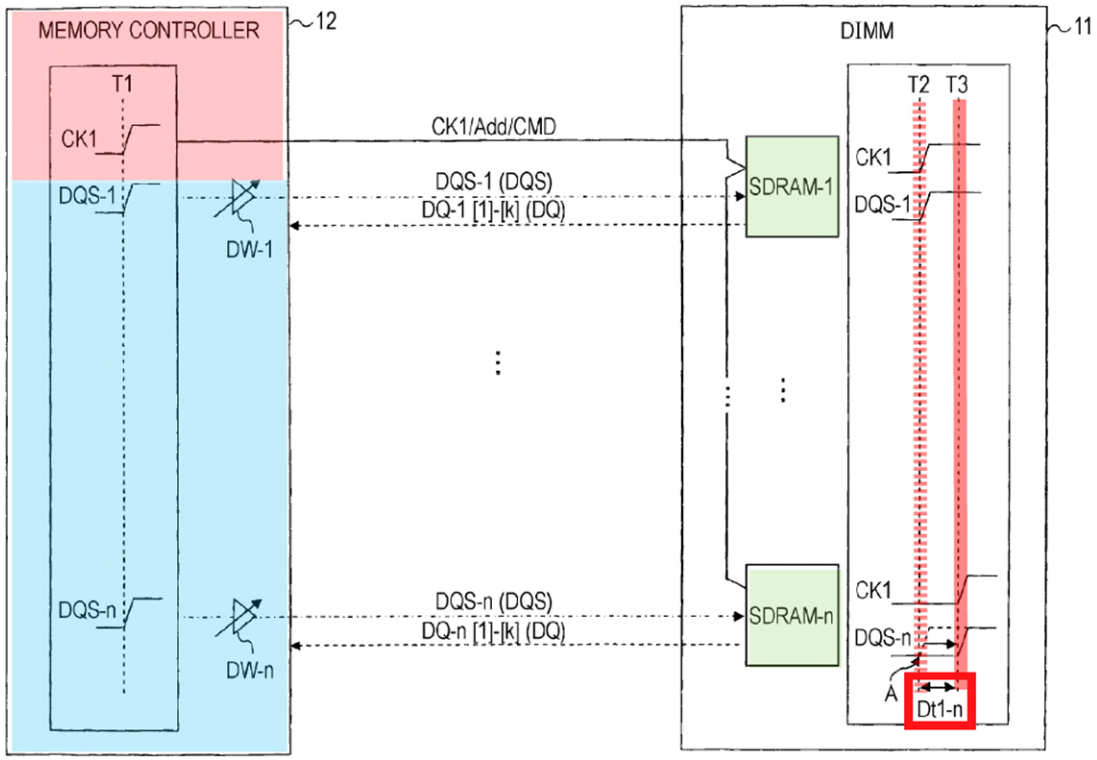
FIG. 7



Accordingly, a Skilled Artisan would have been motivated to use Hiraishi's time measuring technique in the data buffer to determine the fly-by delays during a *write* operation and set the *read* delays accordingly as taught by Tokuhiro.

277. For example, when Hiraishi's memory controller issues a ***write command***, say at time T1, the module controller forwards the write command on the DRC lines to the data buffers, and each of the data buffers will receive that write command with a corresponding fly-by delay: the data buffer closest to the module controller receives the write command at T2, and the n-th buffer receives the same write command at T3 with a fly-by delay Dt1-n. *See* annotated and modified FIG. 7 of Hiraishi below. After a pre-determined write latency, the

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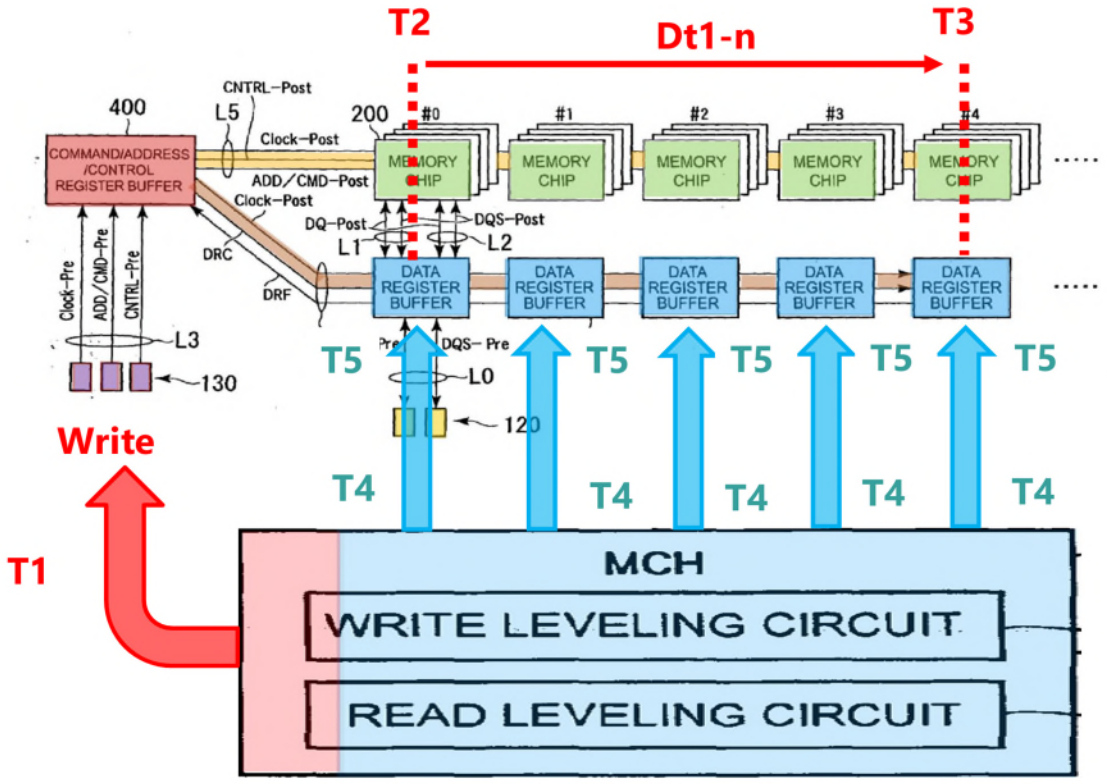
memory controller sends the data corresponding to that write command. *Before* write leveling, the data (DQ) and strobe (DQS) signals are sent at the same time (T4) and those signals also arrive to the data buffers at substantially the same time (T5) as taught by Tokuhiro. EX1006 (Tokuhiro) at FIGS. 7 and 10.



278. Thus, in this implementation, the write command arrives at each data buffer with respective fly-by delays (Dt1) that depend on the distance from the module controller. The write data (blue arrows), however, would arrive at each data buffer substantially at the same time T5, since the write leveling delays are not yet applied by the memory controller. As such, each data buffer can measure the time difference between the time of receiving the write command (between T2 and

T3, depending on the buffer) and the time of the arrival of the data (T5). For the data buffer closest to the module controller, that time difference is the difference between T5 and T2, and for the data buffer furthest from the module controller, that time difference is the difference between T5 and T3.

279. A Skilled Artisan would have understood that those time differences for a write operation can be measured using the same technique that Hiraishi's data buffer is already using to determine a time delay between receiving a read command and the arrival of the corresponding read data. EX1005 (Hiraishi) [0151] ("The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200…"); *see also id.*, Fig. 15. Thus, a Skilled Artisan would have understood that the functionality of measuring the difference between the time of receiving a read command and the time of the arrival of the corresponding read data can also be implemented to measure the difference between the time of receiving a write command and the time of the arrival of the corresponding write data. Accordingly, a Skilled Artisan would have been motivated to use Hiraishi's time measuring technique to measure a time interval between the arrival of a write command (e.g., T3) and the respective strobe signal (DQS) travelling with the corresponding write

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data (DQ) (e.g., T5) in order to determine the corresponding fly-by delays (e.g., Dt1-n).

280. A Skilled Artisan would have then understood that Hiraishi's memory buffers can use the feed-back channel DRF to communicate the measured time intervals to the module controller which, in turn, can use those time intervals to determine the corresponding fly-by delays for a read operation as taught by Tokuhiro, and program the read delay elements in the data buffers for transmitting the read data accordingly. *See* EX1005 (Hiraishi), [0089] ("the data register control circuit 320 generates a feedback signal DRF and supplies it to the command/address/control register buffer 400. The feedback signal DRF is a signal indicating a current status of the data register buffer 300."); [0099] ("The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404."). A Skilled Artisan would have also understood that, instead of the module controller determining the read delays based on the measured write delays, it can send sufficient information to the memory buffers such that the memory buffers can determine and program the read delays. For example, Tokuhiro teaches that a read delay for a specific memory can be determined from the maximum of the write delays and the write delay measured for that memory. EX1006, 16:15-42 (see, e.g., Equation (3-6), reproduced below).

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$$\text{Delay}(R)n=\max(\text{Delay}(W))-\text{Delay}(W)n \quad (3\text{-}6)$$

Thus, a Skilled Artisan would have understood that Hiraishi's module controller can send such a maximum write delay to the memory buffers so that each memory buffer could use that maximum delay and the locally measured write delay to determine the read delay and apply it to subsequent read operations. A Skilled Artisan would have been motivated to have the data buffers determine and set the read delays because it requires less communication between the data buffers and the module controller.

281. In this implementation of the Hiraishi-Tokuhiro combination, Tokuhiro's read delay functionality is added to the data register buffers of Hiraishi's module such that, advantageously, no changes to the circuitry of the memory controller are necessary. Furthermore, Tokuhiro's functionality of determining the fly-by delays from delays for the write operations and setting the additional read delays accordingly is also implemented in Hiraishi's memory module. Thus, as illustrated by modified Fig. 13 of Hiraishi below, the system memory controller's operation in this combination changes in that it issues one (or more, if necessary) write commands and subsequently sends corresponding (dummy) write data *without* applying the write leveling delays, *e.g.*, *before* write leveling in step S5, so that the memory module then can set the read delay

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elements as taught by Tokuhiro. That is, the data buffers receive the write command from the module controller with fly-by delays and the subsequent write data without those fly-by delays from the memory controller; the data buffers measure the time difference between the write command and the write data, and report it to the module controller; the module controller calculates the additional read delays for each data buffer and programs them accordingly. After the additional read delays have been set in the data register buffers, Hiraishi's memory controller can perform its write leveling function. Since the read data now arrives to the memory controller without substantial fly-by delays, the memory controller's training to capture the proper values of read data has been advantageously simplified.

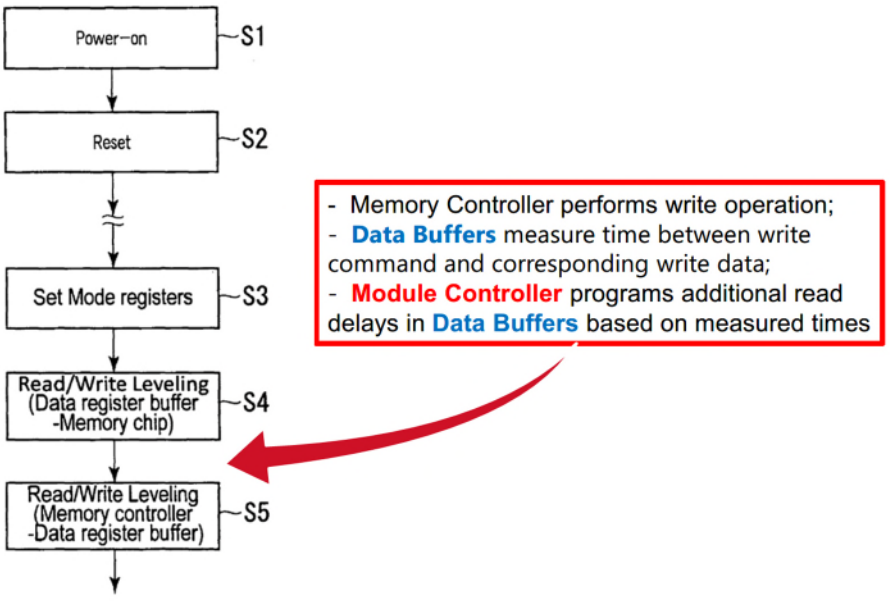

FIG.13

EX1005 (Hiraishi), Fig. 13 (annotated according to the second implementation of the Hiraishi and Tokuhiro combination). A Skilled Artisan would have understood that adding such write commands to the boot-up sequence of the system memory controller is a simple software change that can be easily implemented even in systems that use traditional system memory controllers. Thus, the memory module of the Hiraishi-Tokuhiro combination can also be advantageously used in traditional memory systems.

4. Claim 1

282. Claim limitations 1[pre] through 1[e] are rendered obvious by Hiraishi in view of Butt as explained above in Section V.A.1.a-f, *supra* ¶¶ 115-150.

283. Claim limitation 1[f] is also met by the combination of Hiraishi and Butt in further view of Tokuhiro as explained above in Section V.C.1-3, *supra* ¶¶ 230-281.

284. Claim limitation 1[f] recites "*wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals*."

285. As explained above, the first combination of Hiraishi (in view of Butt) and Tokuhiro has the delay element added to Hiraishi's buffer circuits, and the

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system memory controller measures the fly-by delays during write leveling. *See supra* ¶¶ 259-267, 272-274. In this combination, "*the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path* [e.g., using delay elements, as taught by Tokuhiro to delay DQ and DQS signals on data path L0 (see demonstrative figure showing Tokuhiro Fig. 5 and Hiraishi Fig. 5 annotated below)] *by an amount determined by the command processing circuit in response to at least one of the module control signals* [e.g., the memory controller performs write leveling and programs the read delay elements in Hiraishi's data buffers (similar to Netlist's infringement allegations)]." *See, e.g.,* Hiraishi's annotated FIG. 13 (reproduced below).

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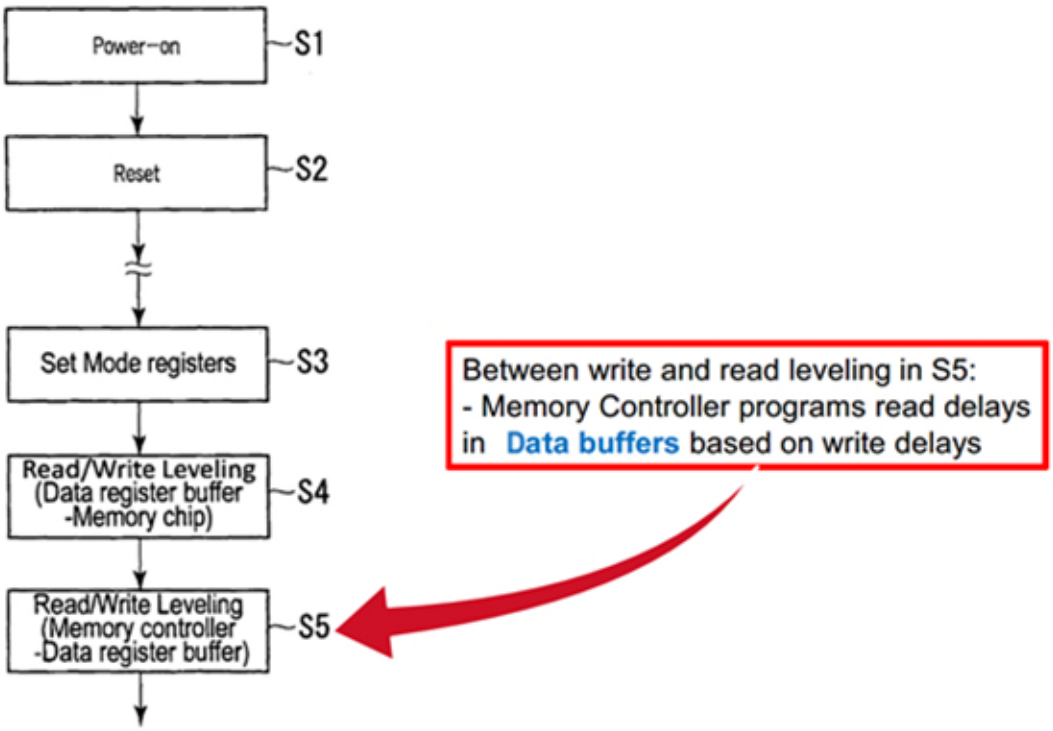

FIG.13

286. As explained above, in the second combination of Hiraishi (in view of Butt) and Tokuhiro, where the delay element is added to Hiraishi's buffer circuits and a time interval is measured by the data buffers during a write operation, *see supra* ¶¶ 259-267, 275-281, "*the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path* [*e.g.*, using delay elements, as taught by Tokuhiro to delay DQ and DQS signals on data path L0 (see demonstrative figure showing Tokuhiro Fig. 5 and Hiraishi Fig. 5 annotated below)] *by an amount determined by the command processing circuit in*

response to at least one of the module control signals [*e.g.*, by comparing the timing of DQ/DQS signals (from the memory controller) and a corresponding Write command (supplied by the memory controller and transmitted to the buffer circuits via the module controller)].”

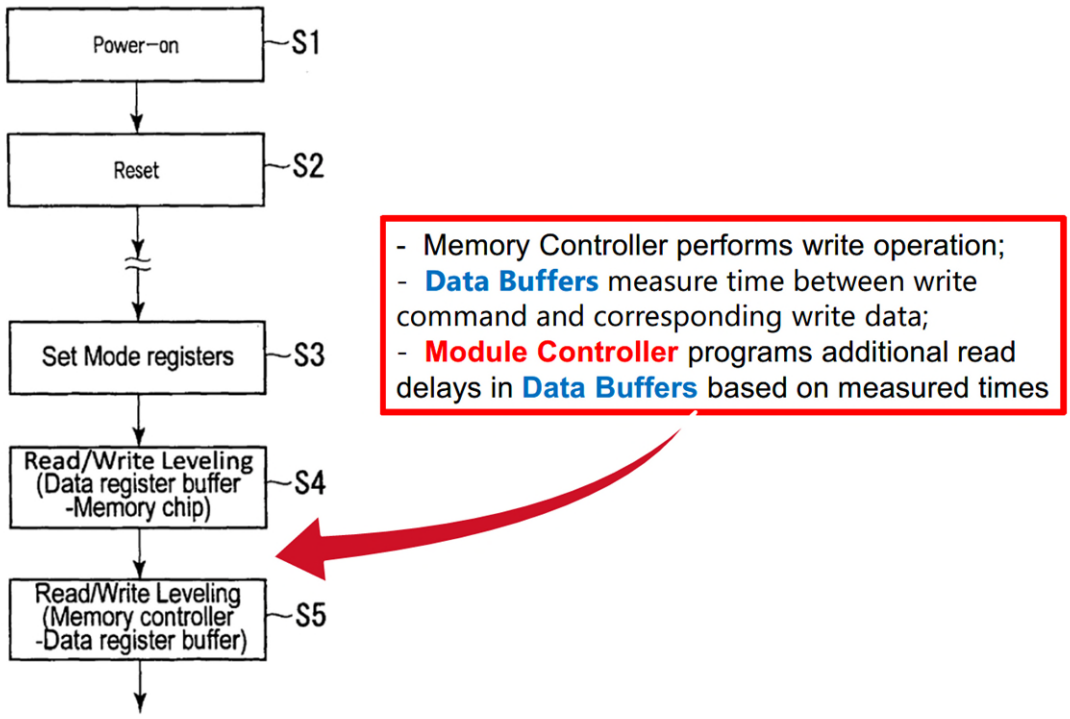

FIG.13

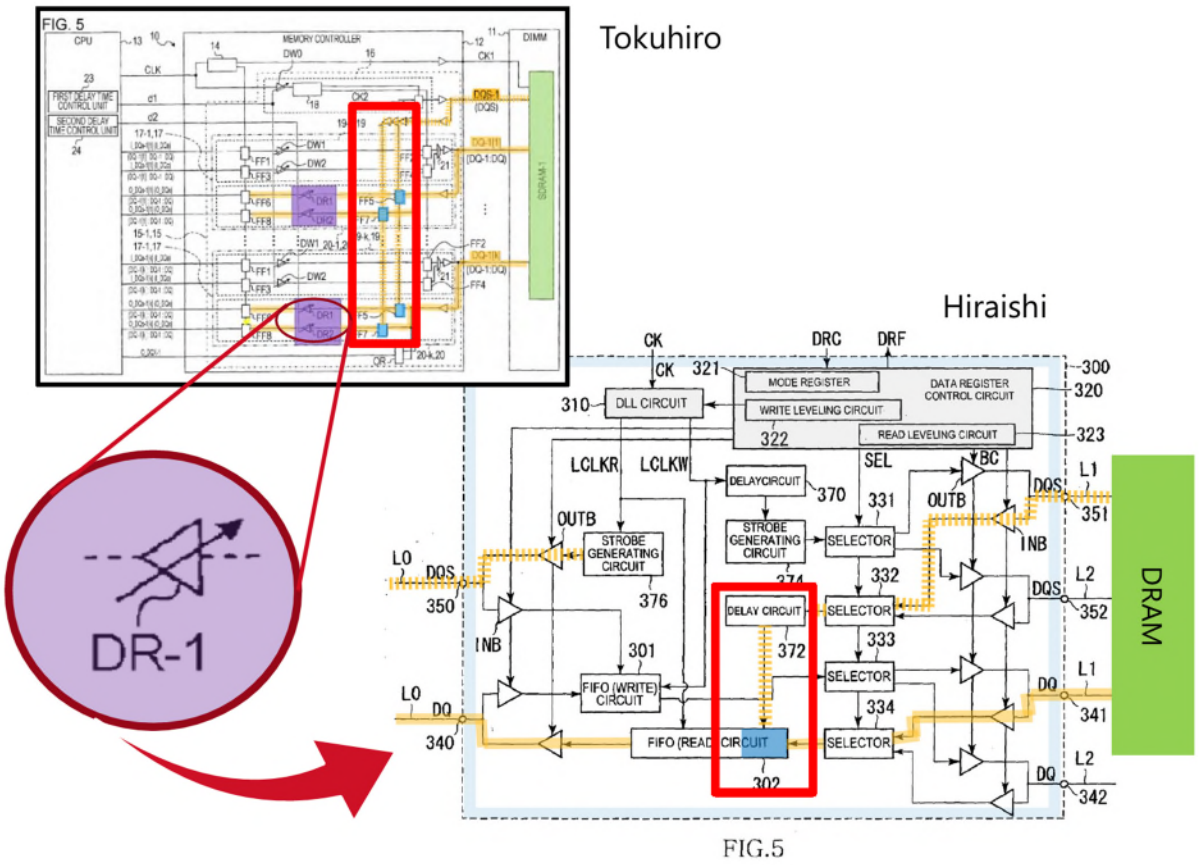

FIG.5

5. Claim 2

a) 2[a]: "The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,"

287. Claim limitation 2[a] is met by the combination of Hiraishi (in view of Butt) and Tokuhiro as explained above in Section V.C.1-3, *supra* ¶¶ 230-281.

288. In particular, in connection with the first combination of Hiraishi (in view of Butt) and Tokuhiro above, *see supra* ¶¶ 259-267, 272-274, the "*first memory operation*" is an S5 write leveling operation, which is a "*memory operation*" according to Netlist, *see, e.g.*, *supra* ¶ 246, and is used in order to

obtain delay timing information for the read delay elements added into Hiraishi's data buffer for subsequent read operations. As explained above, in the second combination of Hiraishi and Tokuhiro, the delay element is added to Hiraishi's buffer circuits and a time interval is measured by the data buffers during a write operation. *See supra* ¶¶ 259-267, 275-281. In this combination, "*the memory operations include a first memory operation* [*e.g.*, a write operation initiated after S4 leveling but prior to S5 leveling (*see* modified Hiraishi Fig. 13 below)] *and a second memory operation subsequent to the first memory operation* [*e.g.,* a subsequent read operation]."

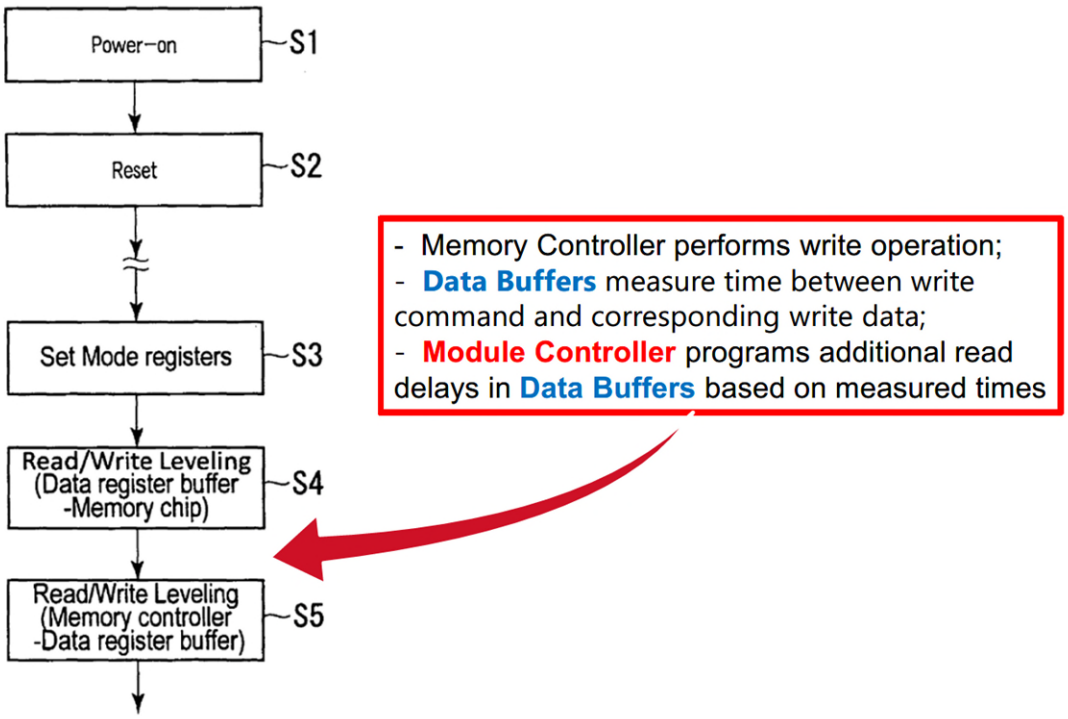

FIG.13

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b) 2[b]: "wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,"

289. Claim limitation 2[b] is met by the combination of Hiraishi, Butt, and Tokuhiro as explained above in Section V.C.1-3, *supra* ¶¶ 230-281.

290. As explained above, the term "*the command signals*" lacks proper antecedent basis, but the combination renders this limitation obvious in either case. *See supra* ¶ 174. In the first combination, *see supra* ¶¶ 259-267, 272-274, the "*the first memory operation*" is an S5 write leveling operation, and the memory controller issues commands ("*system command signals*") to the module to initiate the write leveling. *See, e.g.*, EX1020 (JESD79-3C), p.43 (describing MRS command to initiate write leveling). Since the S5 write leveling is between the memory controller and the data buffers, a Skilled Artisan would have understood that the module controller sends no-operation (NOP) commands ("*module command signals*") to the memory devices. *See, e.g.*, EX1020 (JESD79-3C), p. 33.

291. In the second combination of Hiraishi (with Butt) and Tokuhiro, *see supra* ¶¶ 259-267, 275-281, the "*first memory operation*" is a write operation that is initiated after S4 leveling but before S5 leveling:

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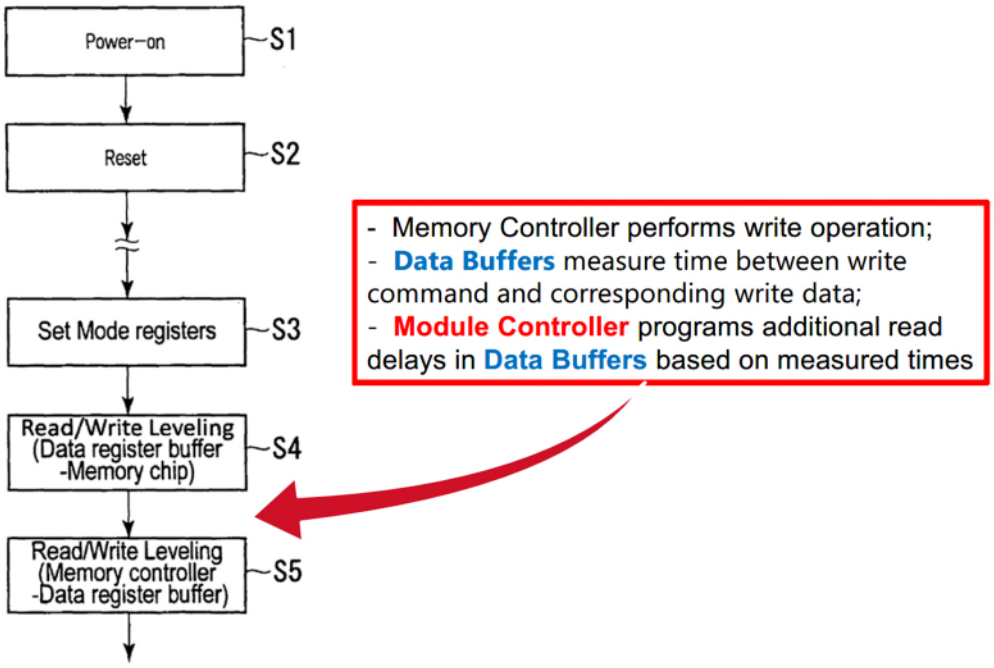

FIG.13

EX1005 (Hiraishi), Fig. 13 (annotated). During this operation, a Write command is transmitted from the memory controller to the module controller (command/address/control register buffer 400 receiving "*system command signals*") which either forwards the write command or sends no-operation commands to the memory devices ("*module command signals*"). After a write latency, the write DQ and DQS signals are sent from the memory controller (MCH 12) to each buffer circuit (300). The command/address/control register buffer 400 also transmits the Write command to each buffer circuit. Each buffer circuit calculates the respective time interval based on the arrival timing of the DQ and DQS signals as compared to the arrival timing of the Write command signal. In

this combination, the "*second memory operation*" is a subsequent read operation, for which the memory controller transmits at least a read command ("*system command signals*") and the module controller forwards the read command to the memory devices ("*module command signals*"). *See, e.g.*, EX1005 (Hiraishi), [0124] ("In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12."), FIG. 11 (showing the read command forwarded to the memory devices). Thus, "*the command signals include a first set of command signals* [e.g., write command] *for the first memory operation* [write operation after S4 but before S5 leveling] *and a second set of command signals* [e.g., read command] *for the second memory operation* [subsequent read operation]."

c) 2[c]: "wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,"

292. Claim limitation 2[c] is met by the combination of Hiraishi, Butt and Tokuhiro as explained above in Section V.C.1-3, *supra* ¶¶ 230-281.

293. As explained above, in the first combination, *see supra* ¶¶ 259-267, 275-281, the S5 write leveling is a "first" operation which is performed when the module control device sends module control signals to Hiraishi's data buffers to initiate the write leveling operation, and the "second" operation is a read operation

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when the module control device uses the module control signals to send the read command to the data buffers. In the second combination of Hiraishi (in view of Butt) and Tokuhiro, *see supra* ¶¶ 259-267, 275-281, the "first memory operation" is a write operation that is initiated after S4 leveling but before S5 leveling and the first set of command signals includes a write command:

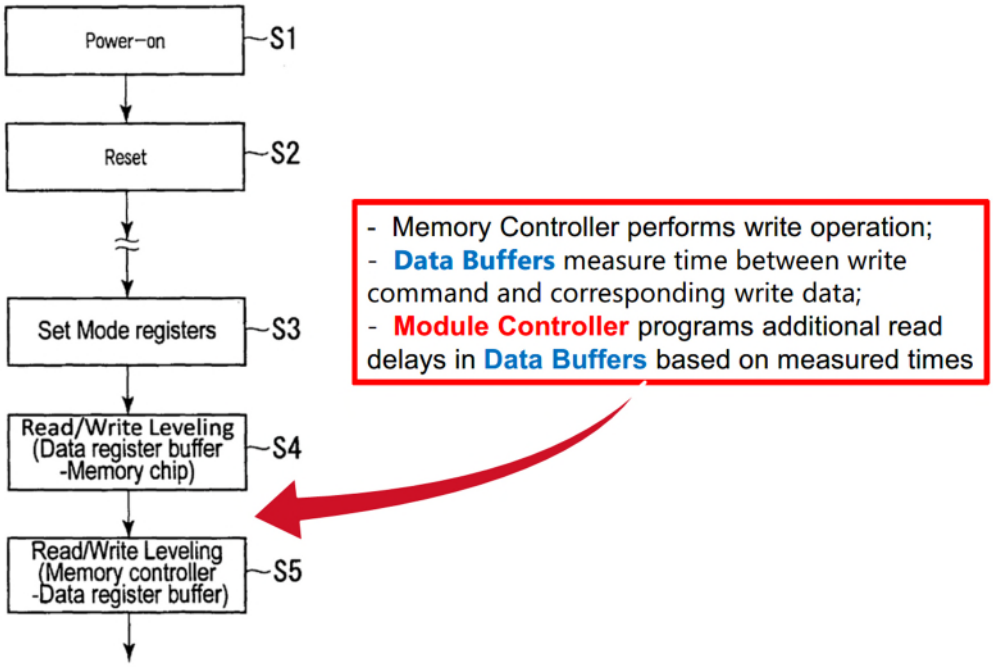

FIG.13

EX1005 (Hiraishi), Fig. 13 (annotated). The command/address/control register buffer 400 transmits the Write command to each buffer circuit as part of the control signal DRC. *See supra*, ¶ 277 ("the module controller forwards the write command on the DRC lines to the data buffers"). In this combination, the "second memory operation" is a subsequent read operation, for which the memory

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controller transmits at least a read command. This read command is also transmitted to each buffer circuit as part of the control signal DRC. *See*, *e.g.,* EX1005 (Hiraishi), [0126] ("the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 ***as a part of the control signal DRC***."). Thus, "*the module control signals include a first set of module control signals* [control signal DRC transmitting Write command] *output by the module control device* [command/address/control register buffer 400] *in response to the first set of command signals* [Write command issued after S4 but before S5 leveling] *and a second set of module control signals* [control signal DRC transmitting Read command] *output by the module control device in response to the second set of command signals* [subsequent read command]."

d) 2[d]: "wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation."

294. Claim limitation 2[d] is met by the combination of Hiraishi, Butt, and Tokuhiro as explained above in Section V.C.1-3, *supra* ¶¶ 230-281.

295. As explained above, in the first combination, *see supra* ¶¶ 259-267, 275-281, the S5 write leveling is a "first" operation which is performed when the module control device sends module control signals to Hiraishi's data buffers to

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initiate the write leveling operation, and the "second" operation is a read operation when the read data signals pass through the data buffers.

296. In the second combination of Hiraishi (in view of Butt) and Tokuhiro, *see supra* ¶¶ 259-267, 275-281, the "first set of module control signals" comprises the control signal DRC used to transmit the Write command to data register buffers 300. In response to this write command, each buffer circuit calculates the respective time interval based on the arrival timing of the DQ and DQS signals compared to the arrival timing of the Write command signal. *See supra*, ¶¶ 277-281. As explained above, the delay amount is determined by the command processing circuit, as recited in limitation 1[f], in response to this control signal. *Id.* The signal through the data path for subsequent read operations is delayed by the determined delay amount. *Id.* Thus, in the combination, "*the at least one of the module control signals include at least one of the first set of module control signals* [the control signal DRC used to transmit the Write command to data register buffers 300]*, and wherein the signal through the data path is a signal* [DQ or DQS] *associated with the second memory operation* [subsequent read operation]."

6. Claims 3-12

297. As explained above, *supra* ¶¶ 185-228, claims 3-12 are rendered obvious by Hiraishi and Butt alone. Thus, the combination of Hiraishi and Butt in

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view of Tokuhiro described directly above also renders obvious those claims for at least the same reasons.

C. Claims 1-12 are Obvious Over Haraishi and Butt in View Tokuhiro in Further View of Ellsberry and/or Kim

298. As explained above, *supra* ¶¶ 185-228, claims 3-12 are rendered obvious by Hiraishi and Butt alone and in view of Ellsberry (e.g., for claims 5, 8, and 12 requiring "*each of the memory devices has a data width of 4 bits*") and/or Kim (e.g., for claims 6-8 requiring "*a metastability detection circuit*"). Thus, the combination of Hiraishi and Butt in view of Tokuhiro described directly above also renders obvious those claims in further view of Ellsberry and/or Kim for at least the same reasons.

* * *

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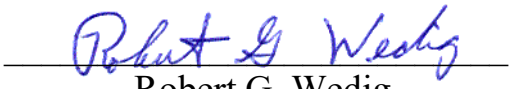
I, Robert Wedig, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: April 27, 2023



Robert G. Wedig

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 10,268,608
1002	File History of U.S. Patent No. 10,268,608
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. US2010/0312956 to Hiraishi
1006	U.S. Patent No. 8,020,022 to Tokuhiro
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry
1008	U.S. Patent No. 6,184,701 to Kim
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	U.S. Patent Pub. No. 2011/0062999 to Nimaiyar
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

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Exhibit #	Description
1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts)
1022	Harold S. Stone, Microcomputer Interfacing (1982)
1023	Microsoft Computer Dictionary (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to ’632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 7,808,849 to Swain
1028	U.S. Patent No. 6,906,555 to Ma
1029	U.S. Patent Pub. No. 2007/0008791 to Butt
1030	U.S. Patent No. 7,036,053 to Zumkehr
1031	U.S. Patent No. 9,824,035
1032	File History of U.S. Patent No. 9,824,035
1033	U.S. Patent No. 5,036,221 to Brucculeri
1034	U.S. Patent No. 9,536,579 to Iijima
1035	*Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021)

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Exhibit #	Description
1036	Order Transferring Cases to the Austin Division, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Feb. 14, 2022)
1037	Joint Claim Construction Statement, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Apr. 14, 2022)
1038	Order on Motion to Stay, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. May 11, 2022)
1039	[intentionally omitted]
1040	Decision Granting Institution of *Inter Partes* Review, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 16 (PTAB July 19, 2022) (U.S. Patent No. 9,824,035)
1041	Decision Denying Institution of *Inter Partes* Review, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00237, Paper 15 (PTAB July 19, 2022) (U.S. Patent No. 10,268,608)
1042	[intentionally omitted]
1043	[intentionally omitted]
1044	Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021) (asserting U.S. Patent No. 10,860,506)
1045	First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. May 3, 2022)
1046	U.S. Patent No. 10,860,506
1047	Decision Granting Institution of *Inter Partes* Review, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00711, Paper 14 (PTAB Oct. 21, 2022) (U.S. Patent No. 10,860,506)

Exhibit #	Description
1048	Joint 4-3 Claim Construction and Prehearing Statement, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Aug. 19, 2022 and Aug. 23, 2022)
1049	Joint Claim Construction Chart Pursuant to P.R. 4-5(d), *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Sept. 30, 2022)
1050	Claim Construction Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 14, 2022)
1051	Defendants' Objections to Claim Construction Memorandum Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 29, 2022)
1052	File History of U.S. Patent No. 10,860,506
1053	Complaint, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (asserting U.S. Patent No. 10,860,506)
1054	Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 1, 2022)
1055	First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Aug. 15, 2022)
1056	Netlist's motion to amend its complaint to assert U.S. Patent No. 10,268,608, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1057	Netlist's proposed Second Amended Complaint asserting U.S. Patent No. 10,268,608 in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1058	JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019)
1059	[intentionally omitted]

Exhibit #	Description
1060	[intentionally omitted]
1061	[intentionally omitted]
1062	[intentionally omitted]
1063	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1064	Federal Court Management Statistics (June 30, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2>

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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1[pre]	1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
1[a]	a module board having edge connections for coupling to respective signal lines in the memory bus;
1[b]	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
1[c]	memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
1[d]	a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,
1[e]	wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,
1[f]	wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

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Ref. #	Listing of Challenged Claims
2[a]	2. The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,
2[b]	wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,
2[c]	wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,
2[d]	wherein the at least one of the module control signals include at least one of the first set of module control signals, and
2[e]	wherein the signal through the data path is a signal associated with the second memory operation.
3[a]	3. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks,
3[b]	wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and
3[c]	wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.
4	4. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
5	5. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

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Ref. #	Listing of Challenged Claims
6	6. The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.
7	7. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
8	8. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.
9[a]	9. The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,
9[b]	wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.
10[a]	10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation,
10[b]	the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.
11	11. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
12	12. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.