

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00847
Patent No. 10,268,608

PATENT OWNER PRELIMINARY RESPONSE

Mail Stop “PATENT BOARD”
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

	<u>Page</u>
I. INTRODUCTION	1
II. STATUTORY DISCLAIMER.....	2
III. THE PETITION SHOULD BE DENIED UNDER 35 U.S.C. §325(d).....	3
A. Petitioner’s Art and Arguments Are the Same or Substantially the Same as Those Raised and Rejected in the Micron -0237 IPR.....	3
1. The Primary Reference (Hiraishi) Is the Same as the Primary Reference (Osanai) the Board Considered in Micron -0237.....	5
2. Butt Does Not Weigh Against Denying Institution Under § 325(d) Because Butt Is Not Used to Satisfy any Claim Limitation and the Arguments Are Substantially the Same as in Micron -237	5
(a) Element 1[e].....	6
(b) Element 1[f]	9
3. Tokuhira	12
4. Ellsberry	12
5. Kim.....	14
6. The Challenged Claims Are The Same As In Micron - 0237.....	14
7. Samsung’s Arguments Are Substantially the Same Arguments as in Micron -0237	15
8. Conclusion	23
B. Petitioner Has Not Demonstrated Office Error.....	23

C.	Both Parts of <i>Advanced Bionics</i> are Satisfied.....	24
IV.	CONCLUSION.....	25

TABLE OF AUTHORITIES

Page(s)

Cases

<i>Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH,</i> IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020).....	<i>passim</i>
<i>General Electric Company v. United Technologies Corp.,</i> IPR2017-00491, Paper 9, 2-3 (PTAB July 6, 2017).....	2, 3
<i>Samsung Electronics Co., Ltd. et al. v. Power2B, Inc.,</i> Case No. IPR2021-01190, Paper 11 (P.T.A.B. January 6, 2022)	14
<i>Vectra Fitness, Inc. v. TNWK Corp.,</i> 162 F.3d 1379 (Fed. Cir. 1998)	3

Statutes

35 U.S.C. §325(d)	<i>passim</i>
-------------------------	---------------

Regulations

37 C.F.R. § 1.321(a).....	2, 3
37 C.F.R. §42.107(e).....	2

EXHIBIT LIST

Exhibit No.	Document
EX2001	Statutory Disclaimer for 15/820,076
EX2002	Power of Attorney and Filing Receipt for 15/820,076
EX2003	IPR2022-00237 IPR Petition
EX2004	U.S. Publication No. 2010/0312925 (Osanai)
EX2005	IPR2022-00711 Record of Oral Hearing
EX2006	IPR2022-00237 DECISION Denying Institution of IPR
EX2007	IPR2022-0711 IPR Petition
EX2008	U.S. Patent No. 8,713,379 (Takeman)
EX2009	IPR2022-00237 Petitioner's Request for Rehearing
EX2010	IPR2022-00237 DECISION Denying Petitioner's Request for Rehearing
EX2011	IPR2022-00237 Declaration of Donald Alpert, Ph.D.

STATEMENT OF MATERIAL FACTS IN DISPUTE

Petitioner did not submit a statement of material facts in this Petition. Accordingly, no response is due pursuant to 37 C.F.R. § 42.23(a), and no facts are admitted.

I. INTRODUCTION

The Petition presents nothing the Board hasn't already considered and rejected. The prior art and arguments are the same or in substance the same as what the Board was asked to consider in IPR2022-00237 by Micron ("Micron -0237"). The main reference in Micron -0237 was Osanai, which shares the same specification as the Hiraishi reference relied on here. Despite that, the Petitioner attempts to evade §325(d) by contending that Hiraishi is presented only in combination with Butt as an obviousness challenge, and not as an anticipation challenge as was the case in Micron -0237. But, as explained below in Section III, Butt is not used to modify Hiraishi's data buffer structure in any way, nor is Butt's data sampling optimization process (or any other functionality) relied on to satisfy an actual claim limitation. The inclusion of Butt in Ground 1 is window dressing, and should not detract from the fact that Samsung is seeking to waste Board resources by presenting for a second time Micron's same prior art and arguments, albeit using the final written decision from Micron -0237 as a road map.¹ The Board should decline to institute under Section 325(d).

¹ The rest of the references are the same or substantially the same as what the Office has already considered as well. *See infra*, Section III.

II. STATUTORY DISCLAIMER

Patent Owner has recorded in the Office a statutory disclaimer disclaiming claims 6-12 pursuant to 37 C.F.R. § 1.321(a) and 37 C.F.R. §42.107(e). As the Board previously articulated in *General Electric Company v. United Technologies Corp.*, IPR2017-00491, Paper 9, 2-3 (PTAB July 6, 2017) (precedential):

Under 37 C.F.R. § 42.107(e), ‘patent owner may file a statutory disclaimer under 35 U.S.C. 253(a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent’ and ‘[n]o inter partes review will be instituted based on disclaimed claims.’ A disclaimer under 35 U.S.C. § 253(a) is ‘considered as part of the original patent’ as of the date on which it is ‘recorded’ in the Office. 35 U.S.C. § 253(a).

Under 37 C.F.R. § 1.321(a), for a disclaimer to be “recorded” in the Office, the document filed by the patent owner must:

- (1) Be signed by the patentee, or an attorney or agent of record;
- (2) Identify the patent and complete claim or claims, or term being disclaimed. A disclaimer which is not a disclaimer of a complete claim or claims, or term will be refused recordation;
- (3) State the present extent of patentee's ownership interest in the patent; and
- (4) Be accompanied by the fee set forth in 37 C.F.R. § 1.20(d).

See id. at 3; *see also Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1382 (Fed. Cir. 1998) (holding that § 253 disclaimer is immediately “recorded” on the date that the Office receives the disclaimer meeting the requirements of 37 C.F.R. § 1.321(a) and that no further action is required in the Office).

The disclaimer of claims 6-12 of the ’608 patent (EX2001), which was signed by the attorney of record (EX2002), satisfies each of the above requirements and therefore has been recorded with the Office as of September, 13, 2023.

III. THE PETITION SHOULD BE DENIED UNDER 35 U.S.C. §325(d)

“[U]nder §325(d), the Board uses the following two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential).

A. Petitioner’s Art and Arguments Are the Same or Substantially the Same as Those Raised and Rejected in the Micron -0237 IPR

The Petition challenges the claims of the ’608 patent based on the following grounds:

	Ground	Claims
1	<u>Hiraishi</u> + <u>Butt</u>	1-12
2	Ground 1 + <u>Tokuhiro</u>	1-12
3	(Ground 1 or 2) + <u>Ellsberry</u>	5, 12
4	(Ground 1 or 2) + <u>Kim</u>	6-8
5	(Ground 1 or 2) + <u>Kim</u> and <u>Ellsberry</u>	8

However, the '608 patent was previously challenged by Micron in IPR2022-00237 (“Micron -0237”). In Micron -0237, the following grounds were presented to the Board:

Ground	Claims	Basis for Unpatentability
1	1 and 4	Anticipated by Osanai (Ex. 1005)
2	1–5	Obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006)
3	1–5	Obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006), in further view of Takefman

EX2003 (Micron -0237 Petition), 4.

Institution was denied in Micron -0237 because the Board determined that claim 1 “requires the *data path* include the delay circuit,” but that Micron had failed to demonstrate that Osanai satisfies that limitation. EX2006 (Micron -0237 Institution Decision), 19-20.

Using Netlist’s POPR in Micron -0237 and the Board’s non-institution

decision as a roadmap, Samsung presents the same or substantially the same prior art and arguments as Micron, but substituting Osanai with Hiraishi that is materially the same. *Compare* EX1005 (Hiraishi) with EX2004 (Osanai). As such, the Board should exercise its discretion and deny institution under Section 325(d).

1. The Primary Reference (Hiraishi) Is the Same as the Primary Reference (Osanai) the Board Considered in Micron -0237

Osanai from Micron -0237 not only “is related to Hiraishi,” (Pet., 113), it is the same as Hiraishi in all material respects, as Samsung’s counsel admitted during oral argument in IPR2022-00711 against the related ’506 patent (“the ’506 IPR”). EX2005 (Record of Oral Argument), Paper 41, 6:7-10 (“And as shown on the right side, both Grounds 1 and 4 rely on Hiraishi, which is equivalent to the Osanai reference”), 10:18-21. Thus, Hiraishi is undisputably the same prior art as that already considered by the Board for the ’608 patent in Micron -0237.

Given that there are no substantive differences between Hiraishi and Osanai, and certain none alleged, the Petition’s decision to use Hiraishi instead of Osanai serves only to create the appearance of a new challenge when in fact the challenge here is simply a re-packaged version of Micron -0237, as further explained below.

2. Butt Does Not Weigh Against Denying Institution Under § 325(d) Because Butt Is Not Used to Satisfy any Claim Limitation and the Arguments Are Substantially the Same as in Micron -237

Petitioner attempts to distinguish the Board’s prior consideration of

Osanai/Hiraishi in Mircon -0237 based on the argument that “Micron relied on *anticipation*” but “[t]his petition asserts *obviousness* over Hiraishi in combination with Butt.” Pet., 113 (original emphasis included). That is a distinction without a difference, however, because the Petition here relies on only Hiraishi substantively for all claim limitations under Ground 1. Pet., 15-71. Elements 1[e] and 1[f] are the only elements of any claim which mention Butt. But even for these two elements, it is the teachings of Hiraishi which are actually relied on to allege that the limitations are satisfied by the prior art. *See* Pet., 31-52.

(a) Element 1[e]

For Element 1[e], the Petition first explains why Hiraishi is alleged to satisfy the element on its own (Pet., 31-34). Only after the discussion of Hiraishi alone allegedly meeting Element 1[e] does the Petition then cursorily argue that “[s]imilarly, Butt discloses that a circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffers the data samples in FIFOs.” Pet., 35. Here, Petitioner does not assert that Butt teaches a data path that includes a delay circuit, the element that the Board found to be missing from Osanai/Hiraishi. EX2006 (Micron -0237 Institution Decision), 19-20.

The Petition also does not suggest modifying the structure of Hiraishi’s data buffer in any way to meet Element 1[e] or any other limitation, nor does the Petition suggest modifying the functionality of Hiraishi’s data buffer in order to meet any

specific aspect of Element 1[e]. Instead, the Petition merely argues that Butt's disclosure would inform what a POSITA would understand about Hiraishi's data register buffer 300 including the recited "data paths." Pet. 36 ("Therefore, a POSITA would have understood from the disclosure of Butt that Hiraishi's data register buffer 300 includes 'data paths' (orange) where data strobe signals sample the data and the data samples are buffered in respective FIFO circuits." That is, Samsung relies on Butt for Element 1[e] as evidence of purported knowledge in the field and how Hiraishi allegedly should be interpreted. That Butt is being used to explain, rather than modify Hiraishi is also clear from the fact that the Petition seemingly draws no distinction between Butt's and Hiraishi's treatment of data and strobe signals. Pet. 37 ("[B]oth Hiraishi's data register buffer and Butt's interface circuit communicate data and strobe signals to and from the memory devices, sample the data signals using the strobe signal, and buffer the data in a FIFO."). Providing evidence of the state of the art or what a POSITA would know, generally, does not create a new prior art combination.

Samsung may argue that it did propose modification to Hiraishi based on Butt by pointing to the Petition's reference to Butt's data sampling optimization process and its argument that it would have been obvious to use that process to "optimize Hiraishi's data register buffer." Pet., 37. But the Petition does not explain how Hiraishi's data register buffer is to be optimized in light of Butt. And, even if a

POSITA would have looked to Butt's sampling process to optimize Hiraishi's data register buffer as asserted (they would not), **Butt's sampling optimization process is not relied on to satisfy any claim limitation.** For example, the Petition describes in detail how Hiraishi, and Hiraishi alone, discloses a "data register buffer 300 [that] is controlled by the command/address/control register buffer 400 using module control signals (e.g., DRC) and a module clock signal (CK)." Pet., 37. The Petition further alleges that Hiraishi's "Data Register Control Circuit 320 receives and decodes the module control signal (DRC) and controls the data path accordingly, e.g., by setting selectors 331-334, activating selected buffer circuits INB and OUTB, and selectively controlling FIFO Write and Read Circuits 301/302, delay circuits 370/372, and Strobe Generating Circuits 374/376." Pet., 37-38. None of that involves "determining an optimum offset delay for data sampling," as Butt is alleged to disclose. The claims do not recite a sampling operation at all, nor is Butt's "optimum offset delay" calculations used in any way to allegedly satisfy any claim limitation.

Moreover, nothing in the references or the Petition suggests that the optimized offset involved delaying the data (DQ) signals: after all, in the '506 IPR relying on the same combination, Petitioner argued that the combination allegedly taught delaying data strobe (DQS) signals for that optimum offset delay for data sampling. EX2007 (IPR2022-0071 ('506) Petition), 43-48. Instead, like using Hiraishi instead

of Osanai, the Petition's discussion of Butt's sampling optimization serves only to create the appearance of a new challenge when, in substance, the art and arguments are substantially the same as what the Board already considered in Micron -0237.

(b) Element 1[f]

The Petition's discussion of Element 1[f] includes a single sentence suggesting that Butt's data sampling optimization process—the same process discussed above, is being used in Hiraishi, citing to Dr. Wedig's declaration which suggests that “the delay circuit 372 for the input read strobe can be controlled to apply a delay that ensures that data from different memory devices are properly captured as taught by Butt.” Pet., 38 (citing EX1003, ¶149). But again, Samsung's attempt to mask what is essentially a Hiraishi anticipation ground as a Hiraishi+Butt obviousness ground is exposed by the Petitioner's own theories for how the actual “delay circuit” limitation of Element [1f] is alleged to be satisfied. In particular, the Petitioner relies exclusively on Hiraishi's original and unmodified S4 write and read leveling operations to satisfy the Element [1f] limitation of a “delay circuit configured to delay a through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.” Pet., 39-51. Specifically, the Petition argues that a combination of components in Hiraishi apparently is the “delay circuit” of the claims. Pet., 47, 51. The Petition then goes on to allege how that combined “delay circuit” applies the

determined amount of delay to a signal based on Hiraishi's existing S-4 leveling. Pet., 47 (“The result of Ground 1’s delay circuit is a variable delay for the DQ/DQS signals (*‘a delay circuit configured to delay a signal through the data path’*),² whose amount is determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 based on the result of the write leveling operation (*‘by an amount determined by the command processing circuit.’*); 51 (“The result is a delay of the DQ/DQS signals (*‘a delay circuit configured to delay a signal through the data path’*) by an amount determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 based on the result of the read leveling operation (*‘by an amount determined by the command processing circuit’*) (original emphasis included). But none of these operations are alleged to involve the manner in which Hiraishi samples data. In fact, in the entire 12-page section of the Petition dedicated to Element 1[f] and the “delay circuit,” sampling is mentioned only once, and even then the sampling is respect to a “local clock,” not a “signal through the data path” “corresponding to the each data

² Element 1(f) recites “the data path corresponding to the each data [DQ] signal line ...” and “a delay circuit configured to delay a signal through the data path” Pet., xiii. Hence, the signal that is claimed to be delayed is the DQ signal, not the DQS signal. Petitioner’s analysis conflates DQ and DQS and does not show DQ, instead of DQS, is being delayed.

signal line.” *Compare* Pet., 45 (alleging that “memory devices provide feedback of a local clock sampled by the strobe signal ...”) with Element 1[f].

To be clear, this is not a situation where a second petition combines a new secondary reference with a previously-used primary reference to cure some deficiency in the primary reference. Here, as noted above, the deficiency of Hiraishi/Osanai in Micron -0237 was a failure to establish a delay circuit in the recited data path. EX2006 (Micron -0237 Institution Decision), 19-20. Samsung does not propose, however, to use Butt to modify Hiraishi’s circuitry so that there is a delay circuit located in a data path. Instead, Samsung relies on Butt only to help explain what a POSITA would have understood about Hiraishi’s data register buffer 300, much like a background reference would be used. *See* Pet., 36. And, although the Petition ostensible suggests that it would have been obvious to use Butt’s data sampling optimization process in Hiraishi, it doesn’t ever use that process to satisfy any actual claim limitation. Instead, the Petition is clear that Butt “**is similarly** ... discloses that a circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffers the data samples in FIFOs,” (Pet., 35), and that “a POSITA would have understood from the disclosure of Butt that Hiraishi’s data register buffer 300 includes ‘data paths’ (orange) where data strobe signals sample the data and the data samples are buffered in respective FIFO circuits.” Pet., 36.

Accordingly, the inclusion of Butt in Ground 1 is mere window dressing, apparently intended to misdirect the Board from recognizing that Samsung is asking the Board to re-consider the same art and arguments the Board already considered (and rejected) in Micron -0237. The Board should decline to do so.

3. Tokuhito

Tokuhito is the same Tokuhito reference already considered by the Board in Micron -0237, and was similarly proposed to be combined with Osanai/Hiraishi. This is not in dispute.

4. Ellsberry

Ellsberry is not relied on to teach or suggest a data path that includes a delay circuit configured to delay a DQ signal through the data path corresponding to each data signal line. Instead, Ellsberry is only relied on **in the alternative** for the limitation of “a data width of 4 bits” found in dependent claim 5 and now-disclaimed claim 12. However, the inclusion of Ellsberry as an alternative basis for certain dependent claims also supports exercising discretionary denial under § 325(d).

First, Petitioner acknowledges that Ellsberry was submitted during prosecution of the '608 patent, and therefore there is no dispute that Ellsberry was before the Office. Pet., 114 (citing EX1002, 151).

Second, Ellsberry is also cumulative of what the Board has already considered in Micron -0237. For example, the Petition here argues Hiraishi's memory device

data width of 1 byte “could be replaced with a pair of 4-bit wide memory devices, as was a standard option at the time.” Pet., 59 (citing DDR3 SDRAM standard as “describing standard DDR3 memory devices with x4, x8, and x16 data widths”). That is substantially the same argument advanced in Micron -0237 for claim 5. EX2003 (Micron -0237 Petition), 61 (“[A] POSITA would have been motivated to modify Osanai’s memory devices to use four bits instead of eight bits ... to comply with the commercial standardization of the DDR3 standard, which specified four bits.”).

Moreover, Samsung takes the position that Ellsberry has “the same distributed buffer architecture as Hiraishi to reduce load” Pet., 108. Thus, Ellsberry is not relied on for presenting any different buffer architecture. That only leaves Ellsberry’s alleged disclosure of “4-bit wide memory chips” (Pet., 108), which is substantially the same as what was argued in Micron -0237 about what the DDR3 standard discloses. EX2003 (Micron -0237 Petition), 61.

Third, in a separate ground, Micron -0237 also relied on the additional disclosure in secondary reference Takefman. EX2003 (Micron -0237 Petition), 64-65. In particular, Micron cited to disclosure in Takefman (EX2008 at 7:30-40) of a “DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8),” where “x4” was argued to mean “DRAMs AMs with “x4” width, which means the DRAM has a “*data width of 4 bits.*” EX2003

(Micron -0237 Petition), 65. However, Samsung does not explain how Ellsberry's disclosure differs from that disclosure in Takefman, or how its arguments about Ellsberry's alleged disclosure of 4-bit memory devices isn't substantially the same as Micron's arguments about Takefman's alleged 4-bit memory devices.

Even if Ellsberry had not been considered by the examiner or was not cumulative of art and arguments presented in Micron -0237 (it is), reliance on a secondary reference in the alternative does not weigh against exercising discretionary denial under § 325(d). See *Samsung Electronics Co., Ltd. et al. v. Power2B, Inc.*, Case No. IPR2021-01190, Paper 11 at 16-17 (P.T.A.B. January 6, 2022) (finding first prong of *Advanced Bionics* met where primary reference was before the Office, despite the fact that secondary references relied on only in the alternative or for dependent claims were not previously considered).

5. Kim

Kim is relied on solely for its alleged disclosure of the “metastability detection circuit” of claim 6, which has been disclaimed as described below in Section II. Therefore, the inclusion of Kim in the Petition does not impact any of the reasons supporting discretionary denial under § 325(d).

6. The Challenged Claims Are The Same As In Micron -0237

While only claims 1-5 were challenged in Micron -0237, and claims 1-12 are challenged in this Petition, Patent Owner has statutorily disclaimed claims 6-12, as

described in Section II above. Therefore, there is complete overlap between the challenged claims here and the claims challenged in Micron -0237. This further weighs in favor of denial under § 325(d) because there are no claim terms or dependent claim arguments that the Board can consider here which were not already before the Office in Micron -0237.

7. Samsung's Arguments Are Substantially the Same Arguments as in Micron -0237

It is indisputable that the Petition relies on the same prior art as what the Office has already considered or, in the case of Butt, is not used to actually satisfy any claim limitation. For that reason alone, Part I of *Advanced Bionics* is satisfied.

In addition, the Petition here presents substantially the same arguments as what the Board considered in Micron -0237. The table below provides examples of the substantially similar arguments in Micron -0237 and Samsung's Petition.

<u>Micron's Petition (Micron -0237)</u>	<u>Samsung's Petition</u>
"To compensate for this propagation delay, Osanai discloses both read and write leveling circuitry 322 and 323 located in the data register control circuit 320 inside data buffer 300. Id., Fig. 5, [0096]; see also id., [0146]–	Hiraishi's S-4 write leveling operation is performed during initialization in response to module control signals (e.g., DRC conveying "mode switching" or "mode register set" commands) by a write leveling circuit 322 "to adjust a

[0164], Figs. 14A–17. These read and write leveling operations ‘adjust a write timing or a read timing in consideration of a propagation time of a signal.’ Id. [0146].” EX2003 (Micron -0237 Petition) at 16.	write timing...in consideration of a propagation time of a signal.” Pet., 44-45.
As shown in annotated Figure 7, Osanai’s command/address/control register buffer 400 (‘module control device’) outputs a Clock-Post signal (‘a module clock signal’) (shown as pink arrow) and DRC (‘module control signals’) (shown as blue arrow) to buffers 300” EX2003 (Micron -0237 Petition) at 35.	“This read leveling operation is performed by the read leveling circuit 323 (in Fig.5), which a POSITA would have understood to be activated by a module control signal DRC.” Pet., 49.
“Figure 7 shows that each data register buffer 300 has ‘data paths’ that correspond to each data signal line, L1 and L2 data lines, connected to each memory chip group (#0 through #4...),	“Hiraishi discloses that ‘each respective buffer circuit of the plurality of buffer circuits is ... coupled between a respective set of data/strobe signal lines [L0, including lines DQ-Pre and DQS-

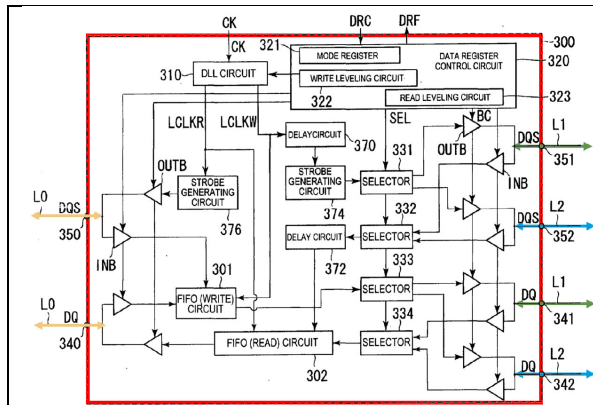
[illegible]

Pre] and a respective set of memory devices [e.g., memory chips 200-0 to 200-3, connected by data lines L1 and L2, including lines DQ-Post and DQS-Post, to the respective buffer circuit 300].” Pet., 31.

“To make these adjustments, the read/write leveling circuitry and DLL Circuit 310 (part of the claimed ‘command processing circuit’) use the module clock (CK) signal sent from the command/address/control register buffer 400. Ex. 1003, ¶ 122; see Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. Based on this clock signal, a ‘timing

“The result of Ground 1’s delay circuit is a variable delay for the DQ/DQS signals (‘a delay circuit configured to delay a signal through the data path’), whose amount is determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 based on the result of the write leveling operation (‘by an amount determined by the command

adjustment’—that is, an added time delay—is then used to compensate for propagation delays.” EX2003 (Micron -0237 Petition) at 43.	processing circuit.’).” Pet., 47.
“To correct this timing error, the write leveling circuitry 322 delays the output timing of the DQS sent from data register buffer 300, thus creating DQS-Post (‘delay[ing] a signal through the data path by an amount determined by the command processing circuit’). EX2003 (Micron -0237 Petition) at 43.	“Furthermore, Ground 1 discloses to a POSITA that the data buffers adjust the timing of both the data (DQ) and strobe (DQS) signals through the data path such that “the appropriate DQ-DQS relationship” is maintained.” Pet., 44.
In addition, a POSITA would have understood these data paths include circuitry components in the data register buffer 300 that connect each L0 data lines (“respective set of data/strobe signal lines”) at terminals 340 and 350, shown in Figure 5 below:	“[A] POSITA would have understood from the disclosure of Butt that Hiraishi’s data register buffer 300 includes “data paths” (orange) where data strobe signals sample the data and the data samples are buffered in respective FIFO circuits.” Pet., 36.



EX2003 (Micron -0237 petition) at 36-37.

“Fig.5 (below, showing data paths, orange, for read and write operations).

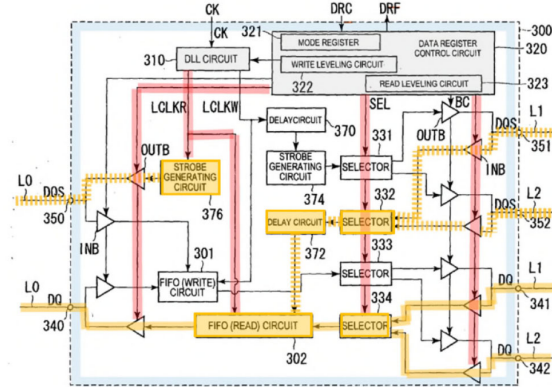
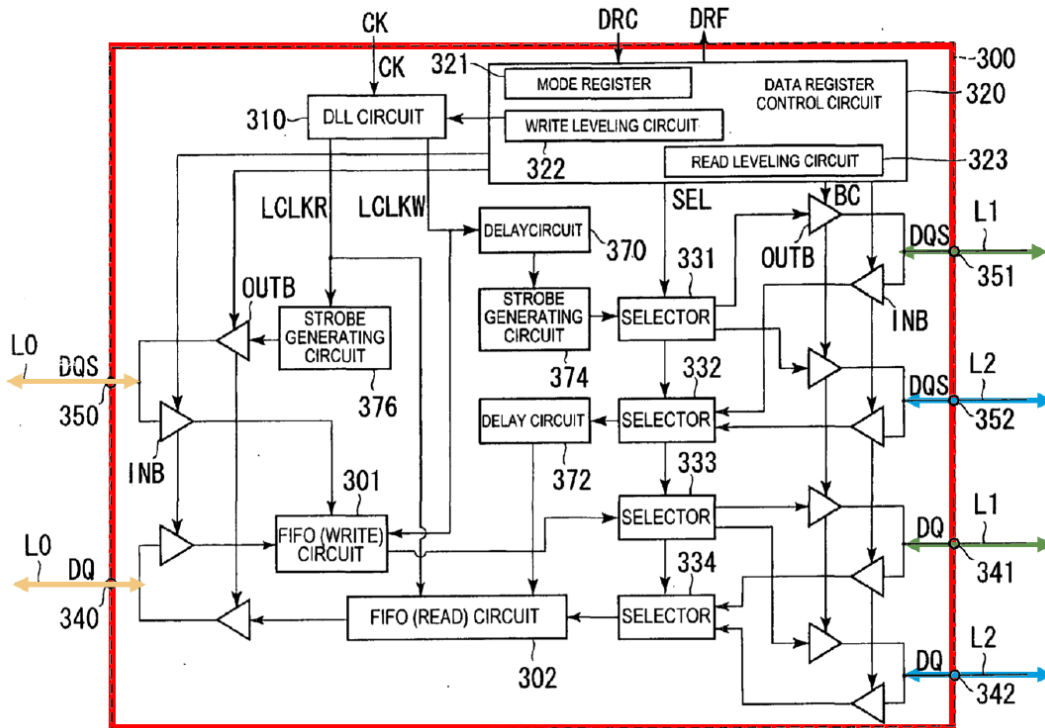


FIG.5

Pet., 39-40.

Samsung may argue that it has identified specific components in Hiraishi that allegedly comprise the recited “data path” which were not relied on by Micron. However, as identified in the table above, Micron argued that the “**data paths include circuitry components in the data register buffer 300 that connect each L0 data lines** (“respective set of data/strobe signal lines”) at terminals 340 and 350, shown in Figure 5 below:



EX2003 (Micron -0237 petition). Each of the components that Samsung now alleges comprise the “data path” are included in the Hiraishi figure above which Micron provided in its petition to show the “circuitry components in the data register buffer 300 that connect each L0 data lines” that allegedly comprised the “data paths.” Thus, at best all Samsung has done is to identify a subset of the components that Micron previously identified as allegedly comprising the “data path.” That is not a substantially different argument.

Moreover, when addressing claim 4, which recites that each of the “buffer circuits has a data width of 1 byte,” Micron specifically relied on Osanai’s FIFO circuits 301 and 302, thus showing that Micron was including the FIFO circuits 301 and 302 in the “circuitry components” that it alleged comprised the “data paths.”

EX2003, 44-45 (citing to EX2004 (Osanai) at [0091] (“The FIFO circuits 301 and 302 shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits 301 and 302 as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer 300 inputs and outputs I-byte data, 8 sets of the FIFO circuits 301 and 302 are required.”)).

Samsung may also argue that it has identified specific components in Hiraishi to allegedly comprise the recited “delay circuit” which were not relied on by Micron. However, both Micron and Samsung relied on the same Hiraishi’s S4 write leveling and read leveling processes for the function allegedly performed by the “delay circuit” of “delay[ing] a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.” EX1001, Cl. 1. For example, the petition in Micron -0237 argued that a “‘timing adjustment’—that is, an added time delay—is then used to compensate for propagation delays,” citing to paragraphs [0149]–[0157] in Osanai which describe the S4 “write leveling operation” of FIGs. 14A-14B. EX2003 (Micron -0237 petition), 43; EX2004 (Osanai), [0149]–[0157]. Samsung similarly relies on Hiraishi’s same S4 write leveling process, prominently featuring FIGs. 14A-14B in the Petition here. *See generally*, Pet., 43-47; *see id.*, at 45-46 (“The delays determined during write leveling are stored in the data register buffer 300 and

applied by the control circuit 320 to delay both the data and data strobe signals during subsequent write operations to ensure that the standard data to strobe timing requirements are met at the memory devices.”).

The petition in Micron -0237 further argued that “[a] similar read leveling process **results in signals being delayed**,” citing to paragraphs [0153]–[0157] in Osanai which describe the S4 “read leveling operation” of FIG. 15. EX2003 (Micron -0237 petition), 43; EX2004 (Osanai), [0153]–[0157]; *see also* EX2003 at 44 (“Using these leveling techniques, the leveling circuitry ‘adjust[s] a write timing or a read timing in consideration of a propagation time of a signal,’” and “the specific delay chosen depends on whether the DRC mode that represents a read operation or write operations, which use different ‘module control signals.’”). Here again, Samsung follows the Micron script by arguing that “[s]imilarly, Hiraishi discloses that S-4 read leveling is “to adjust...a read timing in consideration of a propagation time of a signal,” providing a description of FIG. 15, and concluding that “[t]he result of these operations is a variable delay adjusting the timing of the read data and strobe signals on the data path.” Pet., 48-50.

Thus, to the extent that Samsung argues it identified specific components in Hiraishi as allegedly comprising the recited “delay circuit” which were not identified by Micron, that is immaterial because Samsung relies on the same Osanai/Hiraishi leveling operations as Micron did (*i.e.*, S4 write and read leveling) and those

operations would necessarily be performed by the same components. Therefore, the substance of Samsung's arguments are substantially the same as in Micron -0237.

8. Conclusion

As described above, each of the prior art references and arguments actually relied on in the challenge are the same or substantially the same as what has already considered by the Office. Therefore, the first part of *Advanced Bionics*' two-part test is satisfied.

B. Petitioner Has Not Demonstrated Office Error

Petitioner makes no argument that the examiner or the Board in Micron -0237 erred in any manner. Indeed, Petitioner's own rehearing arguments and the Board's decision on rehearing in Micron -0237 show no Office error occurred.

Specifically, Micron argued on rehearing that the Board overlooked the fact that the -0237 petition explained how Osanai allegedly disclosed a data path that includes the delay circuit, which was the limitation the Board found had not been satisfied. EX2006 (Micron -0237 Institution Decision), 19-20; EX2009 (-0237 Request for Rehearing). For example, Micron argued on rehearing that the -0237 petition "stated that selectors 331-334 and input/output terminals, 341 and 342, of data register buffer 300 are included in data paths for read and write operations." EX2009, 5 (citing -0237 petition at 39-40). Micron further argued that the -0237 petition "further explains that the read and write data paths include different

components—that is, a FIFO (Write) circuit and FIFO (read) circuit. Ex. 1005, [0097] (describing, for a write operation, that “[t]he selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals.”); *id.* (describing, for a read operation, that “[t]he selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302.”).” EX2009, 6. Micron further argued that the “petition also explained that components in each of the read or write paths use their respective local clock, LCLKR and LCLKW.” *Id.*, 7 (citing -0237 petition at 40, EX1003, ¶¶ 115, 122, and Osanai at [0093]).

However, the Board’s Rehearing Decision (EX2010) shows that no error occurred. Instead, in denying Micron’s Rehearing Request, the Board stated that “it was incumbent upon the Petitioner to set forth the evidence and explain how it demonstrates that the data path includes the delay circuitry.... Because Petitioner did not do so, we are not persuaded to modify our Decision.” EX2010, 6. Thus, Samsung cannot now contend that the Board erred by overlooking those aspects of Hiraishi/Osanai on which Micron sought rehearing and lost.

C. Both Parts of *Advanced Bionics* are Satisfied

Because the same or substantially the same prior art and arguments were previously presented to the Office and Petitioners have not demonstrated any error

on the part of the Office, let alone a material one, both parts of *Advanced Bionics* are satisfied. Therefore, the Board should decline Samsung's attempt at a second bite at the apple based on issues already considered by the Office by exercising its discretion to deny institution under § 325(d).

IV. CONCLUSION

Based on the foregoing, the Board should deny the Petition in its entirety and decline to institute a *inter partes* review of the '608 patent.

Dated: September 14, 2023

Respectfully submitted,

By: /Jonathan M. Lindsay/

H. Annita Zhong (Reg. No. 65,530)

Jonathan M. Lindsay (Reg. No. 45,810)

Jason Sheasby (*pro hac vice* to be requested)

Irell & Manella LLP

1800 Avenue of the Stars, Suite #900

Los Angeles, CA 90067-4276

Telephone: (310) 203-7183

Fax: (310) 203-7199

CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Preliminary Response contains 5,765 words, excluding the words in the table of contents, table of authorities, exhibit list, this certificate of word count, and certificate of service. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/s/ Jonathan Lindsay
Jonathan M. Lindsay

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on September 14, 2023, a complete copy of the foregoing document **PATENT OWNER PRELIMINARY RESPONSE** and **Exhibits 2001 – 2011** were served by electronic mail, as agreed to by the parties, upon the following:

BAKER BOTTS L.L.P.

Eliot D. Williams, Reg. No. 50,822

Theodore W. Chandler, Reg. No. 50,319

Ferenc Pazmandi, Reg. No. 66,216

Michael E. Knierim, Reg. No. 78,268

Brianna L. Potter, Reg. No. 76,748

DLSamsungNetlistIPRs@BakerBotts.com

/Pia S. Kamath/

Pia S. Kamath