

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00711
Patent 10,860,506 B2

Record of Oral Hearing
Held: July 20, 2023

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

IPR2022-00711
Patent 10,860,506 B2

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P-R-O-C-E-E-D-I-N-G-S

2:07 p.m.

JUDGE GALLIGAN: Good afternoon. This is an oral argument for IPR2022-000711. The patent is 10,860,506 B2. I'm Administrative Patent Judge Galligan, and with me are APJs Boucher and Jurgovan.

In this case, we have the following Petitioner entities: Samsung Electronics Company, Limited; Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC. And the Patent Owner is Netlist, Inc.

First, I'd like to start with appearances of counsel for Petitioner and starting with the Samsung Petitioner, please.

MR. CHANDLER: Good morning, Your Honor. This is Theodore Chandler from Baker Botts on behalf of the Petitioner, Samsung Electronics Co., Limited. With me is lead counsel, Eliot Williams, and our colleague, Ference Pazmandi. And then counsel for Micron is here, as well, who will introduce themselves.

JUDGE GALLIGAN: Micron.

MR. HOPKINS: May it please the Board. Matthew Hopkins from Winston & Strawn for Petitioner Micron.

JUDGE GALLIGAN: Great. And the Micron entities were joined later through a joinder motion and petition. And, Mr. Chandler, you'll be presenting for all the Petitioner entities?

1 MR. CHANDLER: Yes, Your Honor.

2 JUDGE GALLIGAN: Okay. Thank you. Patent Owner.

3 MR. LINDSAY: Yes, Your Honor. This is Jonathan Lindsay for
4 Patent Owner, Netlist, Inc. And I'm joined by my colleague, Annita Zhong,
5 lead counsel.

6 JUDGE GALLIGAN: Thank you, Mr. Lindsay. So some
7 housekeeping items. First, each party, each side, has one hour of argument
8 time. And our first priority is your right to be heard, so, if at any time
9 during the hearing you encounter difficulties that you feel undermine your
10 ability to adequately represent your client, please let us know immediately
11 and you can do this by contacting the team that provided you with the
12 connection information. And if you stop hearing and drop off, please just
13 note what you last heard and we'll try to pick up when we reconnect.

14 Please mute your microphone and only unmute when speaking.
15 Please identify yourself when speaking so that the transcript accurately
16 reflects the speaker. When referring to an item in the record, please do so
17 with specificity so the panel can follow along and just so the record reflects
18 that. We have all the papers and we have the slides. So you can just point
19 us to slide number and paper if you don't want to present.

20 And there is a public line for this hearing, and I don't think there's
21 anything confidential in this case. So that shouldn't be an issue.

22 Petitioner, you have the burden of persuasion to show the challenged

1 claims are unpatentable. You go first. You may reserve some time for
2 rebuttal. Would you like to reserve any time?

3 MR. CHANDLER: Yes, Your Honor. Fifteen minutes, please.

4 JUDGE GALLIGAN: Okay. Great. I'll give you a heads up when
5 you're into your rebuttal time. You may continue, and, when you finish, I'll
6 note the time remaining. Let me get my stopwatch here. And you may
7 begin.

8 MR. CHANDLER: Thank you. I have some slides that I would like
9 to share on my screen. Judge Galligan, are you able to see these slides?

10 JUDGE GALLIGAN: Yes. We can see them. Thank you.

11 MR. CHANDLER: Thank you. So starting with slide five, this
12 provides an overview of the 506 patent. As highlighted in the upper left,
13 the title is Memory Module with Timing-Controlled Data Buffering. And
14 it's really that timing control that is the focus of the parties' dispute.

15 The right side shows Claim 1 of the 506 patent. Most of the
16 limitations are not disputed because they merely concern conventional
17 features found in any memory module, and it's only a couple of limitations at
18 the end which I've highlighted that are in dispute.

19 On the left side, I've highlighted an earlier patent in the family,
20 9,824,035, because it was the subject of a recent final written decision that
21 we contend precludes the arguments raised by Netlist in this IPR, as I will
22 discuss in a few moments. I have also highlighted July 27th, 2012, which is

1 the date the parties have assumed for purposes of this IPR is the invention
2 date for the claims of the 506 patent.

3 Slide seven reprints Claim 1 of the 506, and, again, it's the last four
4 limitations highlighted as 1F to 1I that are the subject of the parties' dispute.

5 Slide nine summarizes the instituted grounds. There are six grounds,
6 but Netlist is only focused on Grounds 1 and 4, which I have highlighted in
7 pink. And as shown on the right side, both Grounds 1 and 4 rely on
8 Hiraishi, which is equivalent to the Osanai reference that recently
9 invalidated Claim 1 and other claims of the related 035 patent in
10 combination with Tokuhiko. And, again, this is the issue that relates to
11 collateral estoppel that I'll talk about in just a moment.

12 Slide 11 and the next few slides give a little background on the prior
13 art and the state of the art. As shown on slide 11, by the time of the
14 invention in 2012, DDR3 memory devices had clock speeds in billionths of a
15 second, making it important to align the clock signal, abbreviated CK; the
16 strobe signal, abbreviated DQS; and the data signal, abbreviated DQ.

17 Slide 12 is Figure 15 from Hiraishi, which also shows a clock signal,
18 CK; a strobe signal, DQS; and an DQ data signal on the bottom. The clock
19 signal is similar to the strobe signal, but, as you can see on this figure, a
20 clock signal is always running, whereas a strobe signal can start and stop.
21 In a typical memory module, the clock signal is used to determine when to
22 sample the command signal, such as the read command signal in the red box,

1 to see what the command is, why the DQS strobe signal is typically used to
2 determine when to sample the DQ data signal to see what the value of the
3 data signal is. Thus, to make everything work properly, it's important for
4 the clock, the strobe, and the data signals to be aligned properly.

5 Slide 13 provides an overview of the Hiraishi reference that's used in
6 all the grounds. Hiraishi shows a memory module with memory devices in
7 green, data register buffers in blue distributed along the bottom of the
8 memory module, and then at the center in red is the command address
9 control register buffer. So Figure 1 on the left provides the overview of the
10 entire module, Figure 7 on the right provides a little more detail and
11 essentially shows half or one side of the module.

12 Slide 14 shows on the right side that Hiraishi teaches that, when the
13 memory module is powered on, it should perform a series of steps, including
14 a step S4 performing read and write leveling between the data buffer in the
15 middle and the memory devices on the right shown in green and then, at step
16 S5, performing read and write leveling between the system memory
17 controller on the far left and the data buffer in the middle. So I want to
18 pause on this point just to emphasize Hiraishi teaches that you should
19 perform read and write leveling twice, not just once but twice, both at step
20 S4 between the data buffer and the memory chip and also at step S5 between
21 the system memory controller and the data buffer.

22 Slide 15 shows Figure 6 of Hiraishi on the left, which is the command

1 address control register buffer, and on the right is Figure 5 which is the data
2 buffer. Figure 6 supplies the control signal DRC and the clock signal CK
3 over to the data buffer in Figure 5. And in Figure 5 in the upper right, there
4 is the data register control circuit 320, which includes a write leveling circuit
5 322 and a read leveling circuit 323 that are used to perform the S4 read and
6 write leveling operations.

7 Slide 16 provides an overview of the Butt reference used in all the
8 grounds. Butt discloses the details for sampling a data signal at the
9 optimum time based on a delayed read strobe signal DQS. And then slide
10 17 provides an overview of the Tokuhiro reference using Grounds 4 to 6.
11 Tokuhiro solves the problem of large fly-by delays by determining a first
12 delay time using the write leveling function and then using that delay to
13 delay the transmission of data during read operations. So in this particular
14 example, all of the read data would arrive at time T10 instead of being
15 staggered at different times between T9 and T10.

16 Slide 19 summarizes the obviousness combination of Hiraishi and
17 Butt for Ground 1. The benefit of the Ground 1 combination is that it
18 centers the DQS strobe signal with the DQ data signal so that the DQ data
19 signal is sampled at the optimum time.

20 Slide 20 provides a little bit more detail about the Ground 1
21 combination. In this combination, Hiraishi's data register buffer in the
22 middle uses delay circuit 372 circled in red to delay the read strobe signal

1 DQS to sample the data signal DQ from the memory device at the optimum
2 time. That optimum time was determined during read leveling, and this was
3 all taught by Butt.

4 Slide 21 summarizes the obviousness combination of Hiraishi, Butt,
5 and Tokuhiro for Ground 4. The benefit of the Ground 4 combination is
6 that it removes fly-by delays. On the left is Hiraishi alone, which has fly-by
7 delays such that read data arrives at the system memory controller at
8 different times between T9 and T10. On the right is the Ground 4
9 combination which removes the fly-by delays, let all the read data, arrives at
10 the system memory controller at the same time, which in this example is
11 T10.

12 Slide 22 provides a little more detail about the Ground 4 combination.
13 The upper left shows that Tokuhiro teaches applying a read delay element
14 DR-1 highlighted in purple immediately after the read data from the memory
15 device in green has been latched by a flip-flop highlighted in blue. The
16 bottom shows that Hiraishi has a similar configuration where read data from
17 the memory device in green is latched into a FIFO shown in blue. So the
18 proposed combination takes Tokuhiro's delay element DR-1 in purple and
19 puts it in the same place in Hiraishi as shown in the next slide.

20 So slide 23 shows that in the Ground 4 combination, the DR-1 delay
21 element in purple is added to Hiraishi's data buffer to remove fly-by delays.
22 This combination is consistent with the earlier Ground 1 combination where

1 delay circuit 372 continues to make the fine timing adjustments to the
2 incoming DQS strobe signal so that it is centered with the incoming BQ data
3 signal, but the DR-1 delay circuit has the effects of delaying the output of
4 both DQS and DQ on the left-side of the data buffer to remove fly-by delays.

5 So now I want to turn to collateral estoppel. Slide 26 shows that
6 Micron's final written decision on the left in IPR2022-00236, which has
7 been marked in this IPR as Exhibit 1058, and on the right we have included
8 some legal authority for why that decision is binding against Netlist in this
9 IPR.

10 On the upper right is 37 CFR 42.73(d)(3), which states that Netlist is,
11 quote, precluded from taking action inconsistent with the adverse judgment,
12 end quote. And then on the lower right is a quote from the Federal Circuit's
13 recent decision in Google v. Hammond which makes clear that patent claims
14 need not be identical for collateral estoppel to apply, quote, so long as the
15 differences between the unadjudicated patent claims and adjudicated patent
16 claims do not materially alter the question of invalidity, end quote.

17 Slide 27 shows that Micron's final written decision relied on
18 equivalent prior art. Netlist has admitted on the upper right that Micron's
19 Osanai reference, which has been marked in this IPR as Exhibit 2004, is
20 materially identical to Hiraishi, a reference used for all grounds in this IPR
21 marked as Exhibit 1005. And then as shown at the bottom, Micron's
22 Tokuhito reference is the same reference used in this IPR for Grounds 4 to 6,

1 and it's been marked as Exhibit 1006.

2 Slide 28 shows that, during prosecution of the 506 patent, the claims
3 were rejected on the left as not patentably distinct from the 035 claims.
4 And in response, a terminal disclaimer was filed as shown in the bottom and
5 on the right.

6 Slide 29 shows that Micron's final written decision resolved an issue
7 that's highly relevant to Ground 1 in this IPR, which is that read and write
8 leveling operations of Osanai render obvious the claim limitations to
9 memory operations. In the 506 patent, the claim language is operation
10 rather than memory operation as in the 035 patent, which means that, if
11 anything, the 506 claims would have a broader scope rather than a narrower
12 scope, as compared to the 035 patent. Thus, as shown on the left, our
13 contention is that Netlist should be precluded from disputing that Hiraishi's
14 read and write leveling renders obvious the claims of one or more previous
15 operations that are used to determine delay for the DQ and DQS signals,
16 given Micron's final written decision on this issue.

17 Slide 30 shows that the disputed issues in the Micron final written
18 decision shown on the left and also the claim language in the Micron final
19 written decision shown in the middle are not materially different from the
20 disputed issues in this IPR shown on the right. The yellow highlighting
21 refers to the step of read leveling performed by Osanai and Hiraishi, which
22 the Board found renders obvious the top half of Claim 1J in the 035 patent

1 and which we contend renders obvious Claim Limitation 1I in the 506
2 patent. And then the blue highlighting refers to the step of taking the delay
3 value that was previously determined during read leveling and using that
4 value to delay the strobe signal during a normal read command, which the
5 Board found renders obvious the bottom half of Claim 1J in the 035 patent
6 and which we contend renders obvious Claim Limitations 1F through 1H in
7 the 506 patent.

8 Slide 31 is similar to the last slide. It shows additional reasoning by
9 the Board on the left side, and, again, the color coding of yellow and blue
10 matches up with the disputed claim language in the 035 patent in the middle
11 and the 506 patent on the right.

12 Slide 32 shows that Micron's final written decision also resolved
13 issues highly relevant to Ground 4 in this IPR, including that a person of
14 ordinary skill in the art would have been motivated to combine Tokuhiro's
15 delay elements with Osanai/Hiraishi's data buffer with a reasonable
16 expectation of success. The left column shows that the petition in this IPR
17 proposed the same combination. The middle column shows that Netlist has
18 argued that such a combination will not be operable and would not have
19 been made. And then the right column shows that the Board concluded in
20 Micron's final written decision that one of ordinary skill would have been
21 able to make the combination and would have been able to overcome any
22 differences between the two references.

1 Slide 33 is similar to the last slide, but it shows additional arguments
2 from this IPR on the left, additional arguments from Netlist in the middle,
3 and additional conclusions on the right by the Board that are relevant here,
4 specifically that it would be obvious to take Tokuhiro's leveling technique
5 and apply them to a data buffer on the memory module.

6 Slide 34 is similar to the last slide, but it focuses on the motivation to
7 combine Osanai/Hiraishi with Tokuhiro. As shown on the left, the petition
8 in this IPR argued that Tokuhiro's technique was more efficient, thus
9 providing motivation to combine. As shown in the middle, Netlist has
10 argued that the combination would not be more efficient and, instead,
11 supposedly would be less efficient because it supposedly would increase the
12 number of steps. And then, as shown on the right, the Board concluded in
13 Micron's final written decision that Tokuhiro's technique reduces the number
14 of steps, thus providing a motivation to combine consistent with our position
15 in this IPR.

16 Slide 35 is an important slide because it applies to many, many of
17 Netlist's arguments. Here, the Micron final written decision rejected
18 arguments raised by Netlist about bodily incorporation. This is significant
19 because many of the arguments that Netlist raises in this IPR are also about
20 bodily incorporation where Netlist alleges, for example, that a wire is
21 missing from a figure or that a clock signal is shown instead of a strobe
22 signal. As the Board explained in Micron's final written decision, quote,

1 Petitioner is not required to physically incorporate Tokuhiro's variable delay
2 circuits DR-1 and DR-2 in the Osanai, end quote. And that finding by the
3 Board is very important because many of the arguments Netlist makes here
4 about Ground 4 at bottom are bodily incorporation arguments about reasons
5 why DR-2 wouldn't work in the Figure 5 of Hiraishi.

6 Slide 36 addresses a legal question, which is whether collateral
7 estoppel should apply now, even before Netlist has appealed Micron's final
8 written decision. Now, of course, by the time there's a final written
9 decision in this IPR in three months or so, the time for appeal will have run,
10 and so we'll know whether or not Netlist has appealed. But regardless of
11 whether Netlist appeals or not, our position is that collateral estoppel should
12 apply right now.

13 However, to be candid on this issue, we want to point out on the left
14 that there's at least one panel of the Board that has stated that collateral
15 estoppel does not apply before an appeal to the Federal Circuit. That's the
16 Samsung v. M&K Holdings decision in IPR2018-00696, Paper 10.

17 However, there's ample precedent to the contrary from both the Federal
18 Circuit and the Supreme Court. In SSIH, the Federal Circuit held that the
19 law is well settled, that the pendency of an appeal has no effect on the
20 finality or binding effect of a trial court's holding. That's 718 F.2d 370.
21 The Federal Circuit relied, in part, on the treatise Wright and Miller, which
22 states, quote, the preclusive effect of a lower court judgment cannot be

1 suspended simply by taking an appeal that remains undecided. That's 18A
2 Federal Practice and Procedure, Section 4433.

3 The Federal Circuit also has relied on the Restatement (Second) of
4 Judgments, Section 13, which states that a judgment, otherwise final,
5 remains so despite the taking of an appeal. And the Restatement (Second)
6 of Judgments is significant because the Supreme Court recently stated in
7 B&B Hardware, 575 U.S. at 148, quote, we regularly turn to the Restatement
8 (Second) of Judgments for a statement of the ordinary elements of issue
9 preclusion, end quote.

10 And then there's also the SK Hynix v. Netlist case where Netlist was
11 the one arguing for the immediate application of collateral estoppel. In that
12 case, it was under 35 USC, Section 315(e), and the Board agreed in that case
13 to apply collateral estoppel immediately. So we would submit collateral
14 estoppel should apply now.

15 Before I move on to the next topic, which gets to the narrative of the
16 technical arguments in this IPR, does the Board have any questions for us on
17 our position with respect to collateral estoppel?

18 JUDGE GALLIGAN: I don't think so. Thank you.

19 MR. CHANDLER: All right. There's one other case I would point
20 out on collateral estoppel is the Mobile Tech v. Invue Security Products
21 case, IPR 2018-00481, Paper 29, July 16th, 2019. That case also dealt with
22 whether collateral estoppel should apply pending an appeal, and the Board

1 held on page 33, quote, the fact that an appeal is pending does not prevent
2 the application of collateral estoppel, end quote. However, the Board went
3 on to say, out of an abundance of caution, however, we decline to apply
4 collateral estoppel in this claim and will address petitioner's arguments on
5 the merits. And, Judge, Galligan, you were one of the judges on that Board
6 decision, so I want you to know we're aware of the decision, we're aware of
7 the different statements of the law by the Board, but our position as shown
8 on the right of Slide 36 is that the precedent supports applying collateral
9 estoppel immediately.

10 JUDGE BOUCHER: Actually, Mr. Chandler, this is Patrick
11 Boucher. I do actually have a question about the collateral estoppel. In the
12 Micron case, that was addressed in an institution decision. Do you happen
13 to know whether or not the collateral estoppel issue was raised again at trial
14 in the Micron proceeding. I could look, but, if you know, it would be
15 helpful.

16 MR. CHANDLER: Are you referring to the Samsung v. M&K?

17 JUDGE BOUCHER: Yes, sorry, sorry. That's what I meant, yes.

18 MR. CHANDLER: My understanding is it did not come up again,
19 and part of the reason is that the earlier decision in Samsung v. M&K was a
20 case called Infobridge. In Infobridge, the Board took a narrow view of
21 what printed publication is. Infobridge was up on appeal when Samsung
22 M&K was instituted, and so the patent owner was arguing that printed

1 publication should be construed narrowly and they argued collateral estoppel
2 based on Infobridge required at institution that printed publication should be
3 defined narrowly to exclude standard setting documents. The Federal
4 Circuit and Infobridge ended up disagreeing with the Board and vacating
5 and remanding. And so by the time M&K was a final decision, Infobridge
6 had, the Federal Circuit had changed the outcome, and so there was no
7 longer collateral estoppel that the patent owner could point to. To the
8 contrary, the petitioner, Samsung, was able to point to the Infobridge appeal
9 to support its view that printed publication should be understood broadly.
10 And then Samsung v. M&K went up on appeal, and the Federal Circuit
11 again held that printed publication should be understood broadly.

12 So to answer your question, I don't know of the exact time line, but,
13 certainly by the final written decision, the earlier judgment that the patent
14 owner liked was no longer valid.

15 JUDGE BOUCHER: Okay. So there is a potential distinction there
16 in what --

17 MR. CHANDLER: Yes. So Samsung v. M&K was an institution
18 decision. It was not a final written decision. Furthermore, the cases that
19 Samsung and M&K points to were cases where it just so happened that the
20 first decision had already gone up on appeal and been decided. And when
21 that's happened, I mean, clearly, there's going to be collateral estoppel when
22 the first decision has already been up on appeal and it's been decided.

1 There was no dispute in the cases cited by Samsung v. M&K about whether
2 or not that qualified as collateral estoppel. There wasn't the fact pattern we
3 have here where you've got a final written decision and the appeal is not yet
4 included.

5 The Mobile Tech case in 2019, IPR 2018-00481, which was a final
6 written decision, is perhaps a closer analogy where there were a number of
7 earlier final written decisions, as shown on page eight of that decision, some
8 of which the appeal had been concluded but some others of which, such as
9 this 1900 decision on page nine, the appeal was still pending. And that is
10 where, on page 33, the Board held that collateral estoppel did apply, but
11 then, as a legal matter, should apply but then said, out of an abundance of
12 caution, we're going to reach the merits. And on the merits, they went
13 ahead and found all the claims unpatentable.

14 JUDGE BOUCHER: Okay. Thank you.

15 MR. CHANDLER: All right. So going to slide 38, this shows
16 Claim 1, again, the disputed limitations are 1F through 1I. Slide 40 shows,
17 at the institution decision, the Board agreed that Ground 1, which is the
18 combination of Hiraishi and Butt, renders obvious the disputed Limitations
19 1F and 1I. The other two limitations are not disputed for Ground 1. Only
20 1F and 1I are disputed.

21 Slide 41 shows that Butt provides a motivation for Hiraishi's delay
22 circuit 372 circled in read on the bottom left to be adjusted by the read

1 leveling circuit 323 also circled in red to reliably capture the read data in the
2 center of the data eye. And an example of a data eye is shown on the right
3 side of this slide.

4 Slide 42 shows that Hiraishi's delay circuit 372 does not merely apply
5 a fixed 90-degree delay as advocated by Netlist. As shown on the upper
6 right, Hiraishi states that the delay will be about 90 degrees, not exactly 90
7 degrees. And then as shown on the bottom right, Hiraishi states that the
8 leveling operation is to adjust a write timing or a read timing in
9 consideration of a propagation time of a signal. Thus, Hiraishi teaches
10 performing read leveling to make timing adjustments and Butt makes it
11 obvious that one of the adjustments that should be made is to center the DQS
12 strobe signal with the DQ data signal.

13 Slide 43 shows that --

14 JUDGE GALLIGAN: Mr. Chandler, this is Judge Galligan. I
15 wanted to turn back to slide 42. I had some questions about this. I just
16 wanted to talk through some stuff. So my understanding, and I'm going to
17 talk to Patent Owner about this, too, is that read leveling, there is some
18 adjustment of the data strobe as a result of leveling operations. I don't think
19 that's disputed; is that your understanding?

20 MR. CHANDLER: I think that's, yes, that's my understanding is that
21 they don't dispute that read leveling will adjust the strobe relative to the
22 clock. I think they're disputing whether read leveling would adjust the

1 strobe relative to the DQ signal, and our position is you need to align all
2 three of those signals, clock, strobe, and DQ, and Butt focuses on techniques
3 for aligning strobe and the DQ data signal.

4 JUDGE GALLIGAN: Okay. And so that's helpful. I'll have to
5 ponder on that because I'm looking at the claim and the requirement, I think,
6 is to delay the first read strobe by a predetermined amount, and then, of
7 course, the predetermined amount is determined based on a previous
8 operation.

9 My question is, as I was reading the briefing and the evidence, the
10 testimony of the declarants, it appears that there's this dispute about where
11 any delay happens. And Petitioner's point or Petitioner's arguments seems
12 to be that it's in delay circuit 372. There's no dispute that there is a delay
13 that happens there of a quarter clock cycle, 90 degrees, you know. It's in
14 there. The question is whether the additional delay or any additional delay
15 is done there. And I was just wondering is it necessary for your argument
16 that the delay is inserted by a particular box in that diagram?

17 MR. CHANDLER: No, no.

18 JUDGE GALLIGAN: Okay. Can you please explain that?
19 Because I've read through your briefing, and it seems to say a lot the delay
20 circuit does this, the delay circuit, and I'm wondering, if I'm persuaded by
21 Patent Owner's argument that there's no wire there, then do you lose?

22 MR. CHANDLER: No, we don't because, again, that's a bodily

1 incorporation argument about, you know, whether it's box 372 or whether
2 there's a wire between 323 and 372, and the Micron final written decision, as
3 I pointed out, I think is helpful on this point because it explicitly found, with
4 respect to Tokuhiro but the same logic would apply here, is that a petitioner
5 is not required to show exactly where delay element DR-1 from Tokuhiro
6 would be plopped into Figure 5. And for this Ground 1, we're not required
7 to show exactly where Butt, where his circuitry would be plopped into
8 Figure 5 of Hiraishi. So we don't lose if, you know, box 372 is
9 unsatisfactory because Butt provides the motivation and there's a reasonable
10 expectation of success that Hiraishi would be able to implement Butt's
11 technique of aligning the strobe and the data signal in addition to aligning
12 the strobe with the clock signal.

13 JUDGE GALLIGAN: And to follow-up on that, this is Judge
14 Galligan, so the releveling happens and Patent Owner's argument is that --
15 okay. I don't think there's a dispute that the read leveling is a previous
16 operation. If Patent Owner disputes that, I didn't see it in the papers. But
17 the Patent Owner's argument, I believe, is that the read leveling operation
18 results in turning on the input buffers, which are -- it's hard for me to read
19 the numbers there. It's INB, yes, INB, on those buffers there.

20 So, you know, there's a read leveling happens and it somehow adjusts
21 the timing of those. So does that result in a delay of the read strobe?

22 MR. CHANDLER: So if I understand your question, it's does the

1 INB perform the delay or does the delay circuit 372 perform the delay, and
2 that's actually on the next slide, 43.

3 JUDGE GALLIGAN: Okay.

4 MR. CHANDLER: So on the right-hand side of the slide is the
5 Micron final written decision, which is quoting from Osanai, paragraph 157.
6 I believe in Hiraishi it's paragraph 151, but it's the same quote, which is that,
7 during the read leveling, quote, used in an adjustment of an activation timing
8 of the input buffer circuit INB and the like. So there's been a lot of focus
9 on, so when you're doing read leveling, how much of that is performed by
10 the INB circuit versus how much is performed by whatever circuitry is
11 encompassed by the phrase and the like.

12 Our expert interpreted and the like to indicate that it's the delay circuit
13 372 that would do the fine-tuning adjustment. In the Micron final written
14 decision, I don't think the Board narrowed it down to only the INB that
15 performs the delay as part of read leveling because, again, the Board quoted
16 the entire sentence, which is the INB and the like.

17 So regardless of whether it's INB or 372 in Hiraishi, it doesn't really
18 matter because we've got Butt and Butt tells us that you want to align DQ
19 and DQS because they can get misaligned. And there's going to be a
20 reasonable expectation of success of combining those references, given that
21 it's analogous art, given the motivation to do it, given the similarity in the
22 structures between Hiraishi and Butt, et cetera.

1 JUDGE GALLIGAN: Okay. And this is Judge Galligan. So just
2 to follow up, so I'm really trying to understand Figure 5, and I've read the
3 declarant's testimony on it and I have some questions for Patent Owner, but
4 it appears to me that, as far as I can tell, the INB buffers, the Patent Owner's
5 declarant talked about how they're activated and that's where the read
6 leveling occurs, but does the activation of those INB buffers at a certain time
7 then operate to delay the strobe that arrives at L-1, the DQS, or L-2?

8 MR. CHANDLER: I don't know that there's enough detail in Figure
9 5 of the text of Hiraishi to answer that question specifically because, again,
10 the phrase of the patent of Hiraishi is INB and the like. So it's certainly the
11 case that, during read leveling, you need to time the INB to open up at the
12 correct time. I mean, it can't be closed because that would block the signal
13 from coming in. And so you need, during the read leveling, you're going to
14 be adjusting when INB opens up and closes.

15 With respect to, okay, then what circuit or what structure is it that
16 delays everything as part of read leveling, the Board said INB and the like.
17 Our expert has read INB and the like and has believed that 372 would be
18 where you'd do it. It would also be possible that INB, you know, there
19 could be more going on in INB than just this little triangle, that there could
20 be a delay as part of INB. I mean, that could be possible.

21 JUDGE GALLIGAN: And this is Judge Galligan. So my
22 understanding is the signal or Patent Owner's description of it is the signal

1 comes down from the one you've highlighted there, you have your cursor,
2 it's the one that goes into the control signal in INB. And it comes from the
3 320 circuit, the read leveling circuit. I'm just trying to figure out, the strobe
4 comes in from the memory on the read. The memory says we've read the
5 data and it passes the data and a strobe. The strobe, I mean, unless that INB
6 is turned on, then the strobe will not pass through to the selector, right?

7 MR. CHANDLER: Correct.

8 JUDGE GALLIGAN: I mean, I was just trying to figure out is that
9 where the delay happens as then the strobe comes in but the read leveling
10 circuit has figured out there has to be a slight delay, so then it just opens the
11 buffer up slightly after the strobe comes in?

12 MR. CHANDLER: That's not the way Butt teaches doing it. I
13 mean, Butt teaches you take the strobe and the data and you would compare
14 them. And Hiraishi does not go into the level of detail that you're asking
15 about as to how you line it up. It says INB and the like. It shows the
16 timing diagrams to show what you're trying to accomplish with essentially
17 lining up the clock and the strobe and the data signal, and it has the box 323.
18 But as we talk about a little bit later, this is just a block diagram, so on slide
19 56, Hiraishi, paragraph 17, says Figure 5 is just a block diagram. As our
20 expert explained, there's going to be a lot more going on than what's just
21 shown there. And if we get, for example, the next slide, this is about write
22 leveling. Whether you're doing read leveling or write leveling, so slide 57

1 is write leveling, there has to be communication between, as you point out,
2 the incoming strobe and how it compares, there's got to be some feedback
3 into the read leveling circuit or the write leveling circuit. So there has to be
4 wire, if you will, going to 322 for write leveling and 323 for read leveling.
5 That level of detail is not shown in Figure 5. It doesn't mean it's not there.
6 Again, we see that as sort of this bodily incorporation point that the precise
7 wiring is not what's important. It's the teaching, the teaching of read
8 leveling in Hiraishi and then Butt gives a lot more detail about how to do the
9 DQS, the DQ alignment that we're pointing to for Ground 1.

10 JUDGE GALLIGAN: Okay. Thanks. I was just tracing through
11 this, and I was trying to figure out what's going on. I appreciate the
12 explanation. I'll have questions for Patent Owner. It appears to me,
13 though, that at least, I mean, looking at Figure 5 of Hiraishi, the strobe that
14 comes in at points L-1 and L-2 for instance is delayed by a fixed amount of
15 quarter cycle, 90 degrees. I think that's agreed and that's expressly in there.
16 And then the operation of the read leveling would introduce some delay.
17 The dispute is where that delay occurs?

18 MR. CHANDLER: Well, I mean, yes. I think there would be a
19 dispute as to where the delay is measured during read leveling, and then
20 there would also be a dispute during normal operation where do you apply
21 that delay. We would say that you would apply the delay at 372. That
22 would be the normal way to read this figure is that --

1 JUDGE GALLIGAN: This is Judge Galligan. So I guess I'm trying
2 to focus on the language of the claim here is the data buffer does this, does
3 this delay. So my understanding is that the delay is, for instance, not at the
4 memory device. I mean, the memory device just gives a strobe, and then
5 any delay after that is done at the buffer.

6 MR. CHANDLER: Correct.

7 JUDGE GALLIGAN: Okay. Because it seemed like you were
8 focusing or the Petitioner is focusing a lot on a particular box doing is that
9 accurate and whether there's a line there, and I'm just trying to get a bigger
10 picture of whether a delay occurs, and it can't be at the memory device
11 obviously. The memory device gives the strobe, and then, in the claim, the
12 buffer is what then would delay it, obviously, because the memory device
13 just, you know, sends something out; is that correct?

14 MR. CHANDLER: Yes, we agree.

15 JUDGE GALLIGAN: All right. Thanks. And I'll ask Patent
16 Owner about this. I want to clarify the record a little bit.

17 MR. CHANDLER: Thank you. So slide 43 talks about that phrase
18 and the like, which is in both Hiraishi and Osanai. The Micron final written
19 decision relied upon that phrase to conclude that sufficient to teach
20 controlling the timing of the data and strobe signals on the data path, and
21 that conclusion is consistent with Dr. Wedig's testimony on the left.

22 Slide 44 is Dr. Wedig testifying that, if the world were perfect, you

1 could simply apply fixed 90 degrees. But then he explains on the right that
2 the reality is that the world is not perfect, which is why you need to do the
3 fine-tuning of the DQS strobe signal in order to make sure that you reliably
4 receive the data and sample it at the right time.

5 Slide 45 is an important admission by Netlist's expert where he
6 admitted on the left that, under the JEDEC standard, the DQ and DQS
7 signals coming from the memory device from the get-go can be misaligned
8 by up to 28.8 degrees and then, after the signals, leave the memory device,
9 and they're traveling along the wire to the data buffer. That misalignment
10 could get even worse. So that is another motivation, in addition to Butt, as
11 to why you would want the data buffer to do this alignment of the DQS
12 strobe and the DQ data signal because, in the real world, they will not be
13 perfectly aligned. You want them to be aligned, you hope they're aligned.
14 If you're lucky, maybe they will be aligned sometimes. But in the real
15 world, there will often be misalignments that need to be fixed.

16 Slide 46 shows in the upper left that there's a reference that confirms
17 that read leveling is not simply the strobe and the clock but also these
18 strobes being positioned in the middle of the DQ window and another
19 admission on the right by Netlist's expert who agreed that read leveling
20 includes the step of centering the DQS strobe signal with the DQ data signal,
21 and his answer was I expect so.

22 And then slide 47 shows that Tokuhiro, which is not part of Ground 1

1 but it corroborates that it would be normal and expected to have a variable
2 delay element on the incoming DQS strobe signal, and that's shown in red on
3 the left. And on the right is the testimony by Netlist's expert where he
4 agreed that, yes, that red is a variable delay of the incoming strobe signal.

5 So jumping ahead to expectation of success, slide 50 shows that the
6 institution decision agreed that there would be a reasonable expectation of
7 success for the Ground 1 combination. Slide 54 shows that Netlist does not
8 dispute that a person of ordinary skill in the art would be familiar with
9 ASICs, and this is relevant because an ASIC is the type of circuit that
10 Hiraishi's data buffer would use and an ASIC could easily include one
11 additional delay element to implement Butt. And then --

12 JUDGE GALLIGAN: You're into your rebuttal, which is fine.
13 Keep going. I'll let you know.

14 MR. CHANDLER: I'll just finish on this slide.

15 JUDGE JURGOVAN: Counsel, can I ask a question?

16 MR. CHANDLER: Yes.

17 JUDGE JURGOVAN: Concerning Claim 2 and I think Claim 4, it
18 talks about, it seems to say that the delay elements can be individually
19 programmed. I'm sorry. The data buffers can be individually programmed
20 with first and second predetermined amounts of delay. Is that your
21 understanding, and do any of the references actually teach that feature? In
22 looking at the petition, I see, primarily, you're relying on your expert's

1 declaration, but I don't see where there's any cite to the references teaching
2 that each one of the data buffers, you know, in that distributed architecture is
3 being individually programmed with the delay?

4 MR. CHANDLER: That's what Hiraishi teaches. Hiraishi teaches
5 that the read leveling and write leveling is done for every single data buffer,
6 and it's going to be a different amount of delay for each one of those. And
7 so, for example, if we look at Exhibit 1050, 1050 just summarizes on one
8 piece of paper several of the figures and paragraphs from Hiraishi. So
9 Figure 15 at the upper right here shows that there's going to be a different
10 flight time, a different potential delay highlighted in blue here, from memory
11 chip 200-0 to data register buffer 300-0. So that's going to be a different
12 read and write leveling operation than for the next one, which is from
13 memory chip 219 to data register buffer 300-4.

14 So Hiraishi teaches that you're doing the read and write leveling for
15 each individual data buffer.

16 JUDGE JURGOVAN: Thank you.

17 MR. CHANDLER: So this is the last point I was going to make is
18 slide 55. A lot of arguments by Netlist on the left about bodily
19 incorporation, about how a wire is missing or you couldn't plop in Butt into
20 Figure 5 of Hiraishi, but on the right side there's a lot of precedent from the
21 Federal Circuit that bodily incorporation is not the standard.

22 So I'll save the remainder of my time for rebuttal.

1 JUDGE GALLIGAN: Okay. Thank you, Mr. Chandler. You used
2 48 minutes. You have 12 remaining. Let me make a note of that.

3 And, Mr. Lindsay, how much time would you like to reserve for
4 surrebuttal if Petitioner chooses to have a rebuttal?

5 MR. LINDSAY: I'll reserve ten minutes, Your Honor.

6 JUDGE GALLIGAN: Great. I'll give you a heads-up at 15 minutes
7 then, and you can continue. And please keep time, as well. And you may
8 begin.

9 MR. LINDSAY: Okay. May it please the Board. Let me share my
10 screen here. I'd just like to start, Your Honors, I'll say a quick word about
11 Netlist as a company. It was founded in 2000. It's been a leading
12 innovator in high-performance memory module technology. They were
13 shipping samples to IBM and Dell and others in 2009. They secured
14 qualifications for their HyperCloud products on IBM and HP servers.
15 HyperCloud was actually the industry's first LRDIMM and later used that
16 buffer architecture in the DDR4 LRDIMM standard.

17 So on slide two, this is just a quick overview of some of our key
18 points. It's our position that Hiraishi alone or even with Butt is missing a
19 limitation: the strobe delay feature. It's also our position that Hiraishi does
20 not have these DQ, DQS skew problems that Samsung had suggested it
21 does. There's no reason to look to Butt's variable strobe centering on
22 Grounds 4 and 5.

1 The Hiraishi/Tokuhiro combination here is also missing a limitation.
2 In this case, it's the sampling limitation. Samsung attempts to rectify that
3 issue and presents a new sampling theory. It's improper, but it's also
4 incorrect. And this is important to several of their arguments, Your Honors,
5 is that they've presented a combination of Hiraishi/Tokuhiro combination.
6 It's very specific. It's very a bespoke combination, if you will. And their
7 own motivations to modify Hiraishi the way they've proposed here, they're
8 not supported by the actual combination. We'll take a closer look at those,
9 as well.

10 So we've been discussing -- I'll go to slide eight, and this is Claim 1 of
11 the 506 patent. And one of the novel features of the 506 patent is this
12 improved strobe signaling alignment mechanism, and it's about delaying the
13 read strobe signal a predetermined amount of time and generating a delayed
14 read strobe. And that predetermined amount of time of delay is determined
15 in a specific way. It's based on signals received during previous memory
16 operations. In the litigation, the parties had agreed that the term previous
17 operations here were referring to memory operations, and that's the strobe
18 delay feature.

19 Separate from that is the sampling limitation. This is where that read
20 data is actually being sampled by the buffer using that delayed read strobe.
21 We'll talk about that, as well.

22 So I would like to go to slide 13 just to make an architectural point

1 here about Hiraishi's teachings. We've talked about Hiraishi S-4 and S-5
2 leveling. These are procedures that are actually performed by different
3 circuitry. S-4 leveling is performed by the circuitry on the right; that's the
4 data buffer. Hiraishi describes that as determining when input buffers are
5 activated to receive read data and strobe signaling coming from the memory
6 devices. I know Your Honors have questions about that, and we would love
7 to talk to you about that, as well, as we get into the argument. And then S-5
8 leveling. This is done by different circuitry. This is circuitry in the
9 memory controller 12, so it's off module. And according to Dr. Wedig, this
10 S-5 leveling process is used to correct for fly-by delays between the memory
11 controller and the data buffer. So different wires.

12 So on slide 14, Samsung argues that Hiraishi's S-4 read leveling
13 satisfies this delayed read strobe feature, and that's not what it does, Your
14 Honors. Hiraishi says nothing about delaying the DQ read strobe based on
15 these previous memory operations. What it does is what it's showing here
16 in Figure 15. So this is a figure that's in paragraph 147 saying it's
17 explaining read leveling operation. So it shows that there's a time interval,
18 time A, between the memory chips that are outputting that read DQ and
19 DQS signal and a time when it's received. These are called fly-by delays,
20 horizontal delays, if you want to refer to those, as well.

21 So Figure 15 shows us that these fly-by delays can be different
22 between different memory devices, and that's what the time A, that's why the

1 time As are different.

2 So on slide 15, this is the Figure 5 from Hiraishi. And on the right
3 side, we see those input buffers, those INBs, for the incoming DQ and DQS
4 strobe signals and the data signals. And this is what Hiraishi described as
5 its read leveling and its adjusting of the timing of the activation of those
6 buffers by the read leveling circuit. That's the right side red line coming
7 down, and it's activating those.

8 And Dr. Wedig, on slide 16, he confirmed this is what Hiraishi's read
9 leveling is about. So he said it's about activating timing from the input
10 buffers. Okay. Well, what does it mean, he was asked, adjusting an
11 activation timing of an input buffer. He said, well, it allows the data to pass
12 when it's activated. And Dr. Mangione-Smith, in his declaration, he also
13 explained this is what read leveling in the context of Hiraishi is about. It's
14 Exhibit 2006, paragraph 74.

15 So with that in mind, looking at slide 17, Hiraishi describes this
16 adding a fixed 90-degree delay. And, importantly, this is not part of
17 Hiraishi's read leveling. The way that Hiraishi describes read leveling, it
18 does not mention any shifting of the strobe signal. It mentions the 90-
19 degree delay when it's describing this delay circuit 372 here in paragraph 91
20 and then, later, when it's talking about regular read and write operations. So
21 we'll come back to this idea, but the idea here is that Hiraishi treats read
22 leveling on the one hand very differently than delaying a strobe signal by 90

1 degrees on the other hand. They are different concepts based on the
2 specification of Hiraishi.

3 So slide 19 is a diagram. It's an annotated version of that. So you'll
4 find our position, as Your Honor was referring to, is that Hiraishi does not
5 satisfy that strobe delay feature. It's a plain fixed degree. The circuit is not
6 connected in any way. I think that is very clear from this diagram which
7 shows the various signals that are provided by the control circuit 320, and
8 that includes the leveling circuitry for S-4 leveling. And none of them are
9 going to the delay circuit. The delay circuit is a fixed delay.

10 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted to
11 talk about this along the lines of what we discussed with Mr. Chandler. So
12 I'm trying to figure out, so my understanding of a read leveling circuit is that
13 it, based on the 506 patent, I think it even talks about it, that it uses, it
14 compensates for unbalanced wire lengths. In column two, it talks about
15 this. So it introduces some delay, correct? Isn't that the point of a read
16 leveling circuit?

17 MR. LINDSAY: So in the context of Hiraishi, and I guess, as a basic
18 question, read leveling, there's no universal meaning of that term read
19 leveling. Hiraishi uses it one way, the DDR3 standard doesn't use the term
20 at all. What we have, though, is Hiraishi's definition of it, and that is
21 activating the input buffers so that the data can be received. What Hiraishi
22 does in terms of the delays, it has a completely different mechanism that it

1 uses, and Samsung won't talk about this, of course. It's not helpful to their
2 case. But it's a re-timing mechanism, and I'm just finding the best figure for
3 Your Honors. One second.

4 JUDGE GALLIGAN: It's Figure 11, I think, you're referring to.

5 MR. LINDSAY: Right. Okay, yes. So I was looking for the slide,
6 slide, maybe 31. This is not the exact slide that I was going to use. Oh, I
7 found it. Sorry, Your Honors. Slide 21 will be helpful here.

8 So Hiraishi does this re-timing operation, and it's based on an internal
9 clock and it re-times when that read data is being output by the FIFO,
10 generates, and this is why it's very different, it's not delaying read strobe at
11 all. It's generating a new read strobe, and that new read strobe is right here
12 at 376. I'm now looking at slide 19, Your Honors. And that's this local
13 clock signal is syncing that newly-generated DQS signal with the FIFO.
14 The same clock signal is going to clock out that data from that FIFO so they
15 can be output in a proper manner.

16 And Samsung doesn't rely on this re-timing mechanism at all because
17 it's based on a clock signal. It's not helpful to their case. But this is the
18 only re-timing or adjustment of a read data that Hiraishi talks about. It
19 never delays, other than in the delay circuit so that it can sample the data
20 using that fixed 90 degrees we talked about. It doesn't need to delay the
21 read strobe at all because it's creating a new one that's perfectly timed with
22 the data that it's about to output.

1 JUDGE GALLIGAN: Okay. And let me follow -- this is Judge
2 Galligan. Let me follow-up on that. So I was reading paragraph 87 of Dr.
3 Mangione-Smith's declaration, and his testimony is in the context of what
4 these outputs from the module 320, which includes the read leveling circuit,
5 what those outputs do. And paragraph 87 talks about what he calls the
6 output 2 highlighted in blue, and it's the select, so it's in the Figure 5 you
7 have here, and it's the select that goes down to the selector. And it says that
8 a person of skill in the art would understand that this select is not passed to
9 the delay circuit, and fair enough. I think this is getting to the argument that
10 the Patent Owner has that the delay circuit isn't necessarily connected to the
11 read leveling circuit.

12 But it says the selector, he talks about how the selector, you know,
13 forwards the DQS to the delay circuit. The delay circuit then applies the
14 fixed amount. A POSA would readily recognize that the select only affects
15 which DQS is passed but not the amount of delay, and this is all coming
16 from the read leveling circuit. I'm trying to figure out what is the read
17 leveling circuit doing there? It's activating a buffer. My understanding is
18 that there is some, it's introducing some delay or else it's doing nothing.
19 That's what I was trying to kind of go over with Mr. Chandler. What is the
20 read leveling circuit doing if not introducing delay?

21 MR. LINDSAY: So what the record evidence shows is that it is
22 activating the input buffers so that it can properly receive the DQ and the

1 DQS data when it's presented to them. Those different time As reflect the
2 fact that there are fly-by delays, and so they're basing the timing of the
3 activation based on which memory device you happen to be receiving data
4 from.

5 Now, depending on which memory device you happen to be receiving
6 data from, the selector would then pick the L-1, in this example, L-1 or L-2
7 DQS line and then a corresponding L-1 or L-2 DQ line so that it can be
8 passed and so that you were passing the right DQS with the right data.

9 And then, of course, the control circuit is also controlling the output
10 buffers. There's no evidence, Your Honor, in the record that these input or
11 output buffers are delaying signals, DQS or otherwise, in any way. They
12 are passing the data. That's what Dr. Wedig said during his deposition.
13 The delays are being introduced only and exclusively within the delay circuit
14 322. There's no other disclosure express, inherent, or implicit of Hiraishi of
15 any delay inside the data buffer. It doesn't need to. This gets back to my
16 point about re-generating the new data strobe signal. Hiraishi has a
17 different mechanism; he doesn't need to get caught up with this business of
18 delaying a DQS so that you can account for fly-by delays or otherwise. He
19 generates a new DQS signal. It's perfectly aligned with the data because of
20 that local clock sync, that DLL circuit that's providing that local clock.

21 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I'm looking
22 at paragraph 151 of Hiraishi, and this is the quote that was in paragraph 156

1 or 157, the reference in the other case. And it says that the time is
2 measured. This is the read leveling. It's used in an adjustment of an
3 activation timing of the input buffer and the like, and there's some dispute
4 about what "and the like" is. I'm trying to figure out, if it's used in an
5 adjustment of an activation timing, I'm assuming any adjustment is a delay,
6 and so that's what I'm trying to figure out is what is this read leveling circuit
7 doing if not -- it would just pass it through and it gets it, but it's doing
8 something, and that's where I'm -- and Dr. Mangione-Smith's testimony
9 seems to imply that the delay is not in the 372, but there is a delay as a result
10 of read leveling or could be, depending on which memory module you're
11 talking about or which memory device to buffer path you're talking about, I
12 suppose.

13 MR. LINDSAY: So, I mean, to be clear, Dr. Mangione-Smith, I do
14 not believe he testified that there was any delay going on in the input
15 buffers. There's nothing in the record, to my knowledge, Your Honors, that
16 would suggest there's any delay being imposed by the input buffers. The
17 activation of an input buffer allows data to pass.

18 What happens when it's not activated is not evidence in this record
19 either. One could think the data is lost, that it's not passing. It can't hold
20 an infinite amount of data, obviously, so data is lost. That's not delaying
21 data.

22 Again, just based on what the record shows, Samsung has not put in

1 any evidence to explain what Hiraishi means. This is their reference and,
2 with respect, their obligation to explain their challenge. And they also have
3 not relied on, there's nothing in their papers, no arguments that have relied
4 on the input buffers for the delay. They are specific and exclusive in terms
5 of their reliance on the 372 circuit. They've got to obviously explain the
6 basis for their challenge with particularity, and they did that, and they said
7 the delay is imposed by delay circuit 372.

8 JUDGE GALLIGAN: And going back to, I'm trying to understand,
9 you know, read leveling. So in a previous parent or grandparent
10 application, I think it was the subject of the other case we discussed, it had
11 maybe more specificity. It talks about a memory operation and then even a
12 memory write operation, as opposed to previous operations. And I'm
13 reading Claim 1, and it appears Claim 1 says that the buffer needs to get a
14 strobe and delay it and then sample the data, you know, using the delayed
15 strobe. So you're sampling, you're registering it, when the delayed strobe
16 comes in, you know, based on some other timing let's say. And it appears
17 that if you ever do a read leveling that delays a strobe for any amount of
18 time, it would satisfy that. And that's where I'm wondering what Hiraishi,
19 there seems to be a delay somewhere introduced, putting aside the fixed 90-
20 degree delay. And if not, I don't know what the point of, I guess, another
21 adjustment. Of course, we have the Butt combination, as well.
22 But isn't that what read leveling does?

1 MR. LINDSAY: So, Your Honors, we'll go to, to address the
2 question, maybe slide 36. I'm sorry. Not slide 36, slide 38. And it's our
3 view that there's no universal meaning of read leveling. You were talking
4 about this earlier. And the Petitioner likes to blur the line between read
5 leveling in Hiraishi and strobe centering in Butt, but what Hiraishi calls read
6 leveling doesn't mention strobe centering at all. It has a separate discussion
7 when it's talking about this fixed strobe center. And Butt comes along and
8 talks about strobe centering but never uses the term read leveling. Now, on
9 reply, they introduce this Bhakta reference that talks about read leveling
10 being exactly strobe centering, it would appear from this citation.

11 The point being there's no universal meaning of read leveling, and
12 Hiraishi's read leveling is very specific to the fact that it's doing this DQS
13 regeneration process. So it doesn't need to delay any of those strobe signals
14 other than to sample it with the fixed 90 degrees.

15 So, again, its read leveling is specific to Hiraishi. We have to take
16 Hiraishi at his word that that's what he means by read leveling, and I don't
17 believe there's any evidence in the record, Your Honor, that read leveling
18 necessarily includes or inherently requires a delay.

19 JUDGE GALLIGAN: Okay. Thanks.

20 MR. LINDSAY: Okay. So maybe jumping ahead a bit to slide 24,
21 our position is that, even in the combination, the combination doesn't satisfy
22 this strobe delay signal, and the reason is let's consider what the actual

1 combination is. And Dr. Wedig has laid out with specificity, as he's
2 required to do, and he's explained that in the combination with Butt that Butt
3 is using the read leveling circuit 322 and the delay circuit 323 and the delay
4 circuit 372 to iteratively test his memory accesses, figure out different
5 offsets, optimize that ultimate offset, and then program using that read
6 leveling circuit program at delay circuit 372. That's their proposed
7 combination.

8 Now, importantly, as we've said, Petitioner is not proposing any
9 changes to Hiraishi's circuitry. Dr. Wedig here was very clear on this point.
10 He's only proposing to implement Butt's calibration process using the
11 existing data buffer circuitry of Hiraishi. Well, the problem with that is it
12 doesn't work. The read leveling circuit, as we've talked about, cannot
13 control the delay circuit 372. It's not connected.

14 And to be clear, this is not an argument about bodily incorporation.
15 I'll say a word on this. First, we are taking Samsung's proposed
16 combination as they have presented it to the Board, as we're required to do.
17 Notions of bodily incorporation, when we're talking about Hiraishi alone,
18 just don't apply. That's not the standard for a single reference analysis.
19 And in this case, where there is a combination, again, we're not proposing
20 additional circuitry that they haven't said is required. We're taking their
21 challenge at its face.

22 So on slide 27, they kind of concede the fact that this doesn't work and

1 it's no wire shown that they say would be there, especially in the
2 combination with Butt. At the end of this quote, he says especially in the
3 combination with Butt, and this is the Petitioner's reply. But why would a
4 person of skill in the art understand the delay circuit being connected to the
5 read circuit, read leveling circuit even more so in a combination with Butt
6 than without Butt when they aren't changing any of the circuitry. It just
7 doesn't track. It doesn't really make sense, unless they really are changing
8 something.

9 And then on slide 28, we see that Dr. Wedig confirmed here that they
10 do need to change things quite a bit. This isn't just about a wire. He
11 testified that if Hiraishi is not doing variable strobe centering, not the fixed
12 version but variable strobe centering, which we don't believe it's doing, then
13 you need a whole lot more than just a wire. He talked about having a
14 mechanism to program the delay. He talked about generating various
15 offsets. He said you'd need a mechanism for feedback back from the value.
16 You would need all the different aspects that cause Butt to operate. Again,
17 this isn't a bodily incorporation argument. This is what Dr. Wedig is telling
18 the Board is required for their combination to work.

19 And in terms of some of those missing aspects of Butt, well, there's
20 quite a few of them in here and there's a lot in this diagram. Butt is not a
21 simple patent or reference. It has a very particular way that it's able to
22 achieve its variable strobe delay feature. It has a number of signals that are

1 required, including this gate-on circuit here which is generating this gate-on
2 signal that's in Figure 3A. This is used to carry out its process. It requires
3 control from two different clock signals, a data strobe signal. You need all
4 these signals that Dr. Wedig didn't address at all, didn't explain how this
5 would work.

6 So our position is that, even with Hiraishi, this combination with Butt
7 does not satisfy, does not satisfy the strobe delay feature, at least not without
8 substantial additional modifications which aren't explained here at all.

9 In the background, Your Honors, I just want to quickly cover.
10 They've talked about needing to adjust, Hiraishi needing to adjust the DQS
11 signal so that it's properly positioned in order to read data. And Hiraishi
12 says otherwise. It tells us very clearly from its specifications. They ignore
13 the express disclosure here that the DQS and DQ signals are edge-aligned
14 when they leave the memory device or the memory chip, and they're edge-
15 aligned when they arrive at the data buffer. There's no indication that
16 Hiraishi is suffering from any of these problems.

17 And there's good reason for that. If we look at slide 34 for example,
18 there are very short trace lines that are at issue here. And Hiraishi touts the
19 fact that its architecture creates these shortened lines between the data
20 buffers and the memory devices and that these lines are subsequently equal
21 among the different groups. So he is telling us that he does not have
22 DQS/DQ skew problems in his diagrams, and he's telling us why. He's got

1 very short runs.

2 And on slide 35, there's good reason for this. There's the standard.
3 He imposes this skew that the buffer or whatever happens to be receiving the
4 data can rest assured that it's receiving it within a narrow band. Now,
5 Petitioner argues about this, saying this is 28 percent and it's a large number,
6 but what their argument basically comes down to saying there is you can't
7 rely on the JEDEC standard. They've actually mandated a specific
8 DQ/DQS skew that will cause problems. It's not good enough. You still
9 need to correct something, and that's just not the way standard-setting
10 process works. I mean, these are prescribed tolerances, they're purposeful,
11 they're meaningful, and the idea that JEDEC would pick a tolerance that
12 tended to lead to errors is not just tenable.

13 And the idea that Butt is this solution to this well-known problem is
14 also not true. What Butt is actually doing is providing an alternative to a
15 conventional approach of dealing with timing issues at design time. He
16 calls it SPICE timing analysis. Butt specifically talks about this in the
17 background.

18 So to the extent there's some memory devices that may have timing
19 issues caused by skew, maybe by traversing along paths, which is an issue in
20 Hiraishi, but says, hey, there's a conventional way of addressing that. So
21 this notion, again, that every system needs Butt and Butt would optimize any
22 module sampling process, that's just not supported by the evidence. The

1 notion is contradicted by Butt itself.

2 And Tokuhiro, on slide 37, it's in accord. Dr. Mangione-Smith
3 explains in his declaration why Tokuhiro also assumes DQ and DQS are
4 arriving at the same time. So this isn't something -- now, there's a new
5 argument here they raise, Your Honor, on slide 43. I want to jump to it
6 quickly --

7 JUDGE GALLIGAN: This is Judge Galligan. Before we get to
8 that, we were talking briefly about Butt or you were talking briefly about
9 Butt, and I wanted to talk a little bit about it because I think, when we're
10 talking about obviousness, we're looking at teachings of the references, and
11 if the patent says, look, the 506 patent says there's been read leveling
12 operations but they may not be good enough for high-speed applications,
13 something along those lines, in the background, and so there's a strobe, you
14 know, the patent discusses in the claims delaying the strobe in a buffer.
15 And so whether or not it would be optimal or whether or not someone would
16 always want to do what Butt does, I mean, Butt appears to teach a very
17 fundamental aspect, which is that you adjust the data strobe to provide, you
18 know, maybe an optimum point at which to register the data.

19 So why isn't that something that a person of skill in the art would look
20 at and say, oh, that's an improvement or that's just something that's suitable
21 to be used in any memory?

22 MR. LINDSAY: So thank you, Your Honor. A few reasons.

1 Number one is the DDR 3 standard provides for this very specific skew
2 between DQ and DQS. Butt is a much older reference. It references only
3 DDR standard, DDR technology. So what may have been a problem at the
4 time of Butt has not been shown to be a continuing problem at the time of
5 Hiraishi, which was five years later I think it was filed. And, again, not a
6 problem in the context of DDR's very specific mandated tolerance.

7 And then, as my point was a moment ago, Your Honor, Butt isn't
8 saying that this is a problem for everyone, you should do what we're doing.
9 Butt says in the background section, hey, look, we know conventionally this
10 is dealt with at design time. We know that this is a manufacturing issue that
11 takes care of any issues, maybe having longer running times, but we're
12 proposing a different way to do it.

13 So does Hiraishi use the conventional way of solving this, assuming it
14 needs to. We don't think it needs to. His diagrams don't show he needs it,
15 short run lengths certainly don't suggest that he needs it. But even if he did,
16 one wouldn't assume that Hiraishi is deficient. The expert, Dr. Mangione-
17 Smith, testified nobody would look at Hiraishi and think it's deficient in this
18 perspective. Again, Butt is very specific. It's only an alternative to a
19 conventional way of doing this at manufacturing time. Maybe Hiraishi does
20 this at manufacturing time, and that would be a logical conclusion.

21 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I'm not sure
22 that's the right framework. I don't know if a reference has to be deficient in

1 itself. There's always, there are things that can be swapped in and out, there
2 are improvements that can be made. I mean, is that the right framework to
3 say there's no deficiency; therefore, you wouldn't do anything to it?

4 MR. LINDSAY: No, but there would be a need to balance the
5 benefit and the cost of doing that. What we're arguing is that there's no
6 demonstrative benefit, and there is certainly additional cost. We saw the
7 testimony from Dr. Wedig, all the different things that would be required if
8 Hiraishi doesn't have this. If it's not doing variable strobe delay, you would
9 need all these different mechanisms to carry it out. That's a substantial
10 amount of additional complexity. Without a showing of any benefit to do
11 so, our position is that a person of ordinary skill in the art wouldn't
12 undertake the additional expenses and complexity for no reason.

13 JUDGE GALLIGAN: This is Judge Galligan. So the benefit,
14 though, I think, would, I guess, Petitioner can speak to this, would be that
15 you'd optimize the point at which you registered the data. You align it
16 better, you provide the optimum strobe timing, right? So why isn't that a
17 benefit that would motivate a person or at least provide a reason for a person
18 to look at the teachings and apply them?

19 MR. LINDSAY: Because it would be ignoring Hiraishi's express
20 disclosure that it's receiving those signals edge aligned, that they're leaving
21 the memory devices edge aligned, that it's being received edge aligned, that
22 he can apply a fixed 90-degree delay, that he can generate his new DQS

1 strobe on the output to account for this re-timing to six clock cycles. It
2 would be ignoring that express disclosure, Your Honor.

3 JUDGE GALLIGAN: Thank you.

4 MR. LINDSAY: And then Tokuhiro, in slide 43, also this is related
5 to the same point, it's an accord here, as well. Now, they've identified this
6 component in red as being a variable strobe delay. That's a new argument
7 that's never been made before except on reply, but the important point to
8 focus on here is that there's no control signal to that red component like there
9 are to all of other Tokuhiro's other variable delay elements, like DR-1, DR-
10 2. Tokuhiro describes control and clock signals going to every single one
11 of his other delay elements, but there isn't even a mention of this component
12 at all. It's never mentioned, let alone shown, and this is not a lazy diagram.
13 These are detailed diagrams in Tokuhiro.

14 So if this symbol corresponds to an element that's delaying a DQS
15 signal, it's not delaying it during operation, like all of Tokuhiro's other
16 variable delay elements are showing. There's no way it could. It's
17 certainly not described that way. Again, if anything, this delay element is
18 what we're talking about, that it's understood that, whatever variability needs
19 to be injected, that's done at manufacturing time. That's based on the design
20 of the circuit.

21 So, Your Honors, before I was going to go on to the next ground, but I
22 want to address the collateral estoppel arguments that Samsung has raised.

1 I want to switch to their figures and, in particular, slide 26. Hopefully, you
2 can see slide 26 of Samsung's slides. Quickly here, looking at the Google
3 Hammond case, it says that there can be slight differences in claim language,
4 slight differences, so long as those differences don't materially alter the
5 question of invalidity. Well, here there are more than slight differences
6 between the claims first, and those differences certainly have altered the
7 question of validity.

8 Slide 30, we're looking at now, the 035 patent recites a timing
9 information, 506 patent recites determining a predetermined amount of
10 delay. The 035 patent then goes on to use that timing information to control
11 timing of data and strobe signals. The 506 patent uses the predetermined
12 delay differently, uses it to generate a first delay read strobe. And also,
13 critically, the 035 patent doesn't have a sampling limitation at all. It doesn't
14 say it's doing any sampling, let alone with anything in particular, whereas
15 the 506 patent specifically uses that delayed read strobe to sample the read
16 data.

17 Now, I said a moment ago that the issues here are materially different
18 because of these differences in claim language, but you don't need to take
19 our word for it. It's plainly evident from the fact that the theory of
20 invalidity that's applied to the claims in this case, in the 506 IPR, is
21 completely different than the theory of invalidity applied in the 035 IPR.
22 They're the same references, so why change your theory of invalidity

1 completely if the question of validity is the same? Well, you wouldn't do
2 that. Particularly, the 035 IPR, the theory there is that Osanai is S-4
3 leveling, that's the leveling operations between the data buffering of the
4 memory devices, that's what was relied on. The proposed combination
5 basically incorporated Tokuhiro's processing into Osanai's existing S-4
6 leveling circuitry.

7 In direct contrast here, the theory of invalidity in this case is that the
8 leveling at issue is between the buffer and the memory controller, so that's
9 like Hiraishi's S-5 leveling. And also unlike the 035 IPR, the theory here
10 requires adding a new component to Hiraishi to Tokuhiro's delay element,
11 along with, I guess, control lines and programming and such. None of that
12 is part of Hiraishi, and they've got to do that here, right, because the claims
13 of the 506 recite delaying the read strobe by that predetermined amount.
14 Then it's going to use that to sample the data. The 035 patent doesn't need
15 to sample the data. It's not using the delayed read strobe.

16 JUDGE GALLIGAN: Counsel, this is Judge Galligan. So I wanted
17 to back up. Did you say that in this case Petitioner is not relying on S-4
18 read leveling?

19 MR. LINDSAY: Right. So for the Tokuhiro, for the combination
20 between Hiraishi and Tokuhiro.

21 JUDGE GALLIGAN: Oh, okay.

22 MR. LINDSAY: I was switching gears to the next --

1 JUDGE GALLIGAN: Oh, I'm sorry. Yes, I was talking about
2 Hiraishi in general. Okay. You're talking about -- okay.

3 MR. LINDSAY: I apologize. I was trying to get to things too
4 quickly.

5 JUDGE GALLIGAN: No, no, that's fine. On this point, I mean, the
6 panel in that case did find that the read leveling, yes, we're read leveling in
7 Osanai, which is the same disclosure as Hiraishi. I think you acknowledged
8 that in the preliminary response, and it is very similar. You know, that does
9 delay the strobe or that, you know, changes the strobe timing, so why isn't
10 that something that we should take into account?

11 MR. LINDSAY: So for Ground 4, we're focusing on Ground 4 or
12 was that a question about Ground 1?

13 JUDGE GALLIGAN: Ground 1 actually. Thank you.

14 MR. LINDSAY: Oh, okay. So based on their theory, the theory as
15 they presented, and they have been very clear, Your Honors, about what's
16 doing the delaying. The delaying is done by delay circuit 372. In that 035
17 IPR, I believe that Hiraishi alone wasn't going to satisfy the limitations that
18 Tokuhiro was doing. I believe that the previous operation actually ended up
19 being Tokuhiro's leveling that they were looking at. So it's the combination
20 there, again, which is not at issue here for Ground 1.

21 And, again, I believe what was -- I may have a note on this. Right.
22 So I believe what was going on in the 035 is that those module clock signals

1 that were being used to generate local clock signals in Hiraishi, that's what
2 was being relied on for the timing signals. But then later, in reply, I think
3 the Petitioner started arguing that the signals that were actually used to
4 adjust the input buffers were the timing signals. That may be what Your
5 Honor is referring to, and those were signals that were found to control
6 timing. I don't know that they were signals that created a delay, certainly
7 not a predetermined amount of delay, which was then used to sample the
8 read data.

9 So, again, the claims aren't as similar as Samsung may have suggested
10 they are. They're varying scopes and then, again, a limitation is not even at
11 issue on the 035.

12 JUDGE GALLIGAN: Counsel, I had a quick question on something
13 you said a while back, and I wanted to turn to it. So I wanted to understand
14 your position on Butt. I think you said that the adjustment is done at, is it
15 design time, so it's not done every time you run it; did I understand that
16 right?

17 MR. LINDSAY: Right. So Butt has a disclosure in the background
18 section where he talks about -- he or she, I'm not sure. And this is on slide
19 36 of our slides, so we'll go there. And, yes, so he talks about a
20 conventional approach relied heavily on pre-silicon, system-level SPICE
21 timing analysis. So this would be done at design time or manufacturing
22 time, not during operation of the device certainly.

1 JUDGE GALLIGAN: Sorry. I'm just looking at the slide. So that
2 was the conventional art that Butt was addressing, but it looks like Butt says
3 that you would, he wants to avoid that; is that right? You want to eliminate
4 reliance on that?

5 MR. LINDSAY: No, it's not reliance on it. This isn't a general, it's
6 not every memory module that's put into service has a DQ/DQS skew
7 problem. There are other ways of dealing with it without having to have a
8 variable strobe signal. There's nothing in this record that suggests variable
9 strobe signal is better or preferable to, you know, a preset delay like
10 Tokuhiko may use, like Butt is talking about.

11 Again, there's no evidence in this case, that would be a very different
12 IPR. What we're faced with here in this IPR is that the notion of the
13 suggestion that Hiraishi suffers from a DQ/DQS problem and Butt comes
14 along with a solution to that problem, and this was a known problem. And
15 our position is that's not true. Express disclosure in Hiraishi shows that is
16 not the case. We cannot ignore that express disclosure. And even in the
17 context of Butt, out point is is there are other ways, design level,
18 manufacturing level ways, that this could be done, that Hiraishi could do it,
19 for example, that wouldn't need this complex variable strobe system.

20 JUDGE GALLIGAN: Okay. Thank you very much.

21 MR. LINDSAY: And then just back to the one slide I wanted to talk
22 about, also because Mr. Chandler emphasized this one, slide 35. This is, in

1 our opinion, disingenuous because, in the 035 IPR, Tokuhiro's delay on it
2 was not being relied on at all in the combination; yet, it most certainly is the
3 case here, as we talked about. They explicitly have to add it and rely on it
4 in Hiraishi in order to try and cover sampling limitation, which, again, is not
5 part of the 035.

6 So what may have been argument about bodily incorporation there is
7 the basis for the challenge here, and that's put forth not by us but by
8 Samsung.

9 I did want to say, I did want to move on to Ground 4 now, slide 45, if
10 we could. So the ground is missing, in our opinion, a sampling limitation.
11 They've relied on, this is for Ground 4 of the petition for these two sampling
12 steps for independent Claim 1 and 14, they simply refer back to the same
13 reasons as Ground 1. So what is that in Ground 1? Well, slide 46 tells us
14 that the sampling limitation is alleged to be satisfied by a read strobe coming
15 out of the delay circuit 372 going into that FIFO.

16 Now, Hiraishi doesn't say it's sampling. It says it's used as an input
17 trigger signal. But that's what Samsung said. It said sampling the data.
18 That's their theory for satisfying the sampling limitation in Ground 1.

19 Okay. So here is a new read strobe signal, and the red read strobe --
20 they've switched gears. They're now relying on a different strobe signal.
21 The alleged delayed strobe signal is in purple. The red should say not
22 alleged delayed read strobe at Ground 4. They switched this, and it even

1 confused me. So, again, the important point is that they're not alleging that
2 the delayed read strobe in Ground 4 is coming out of the delay circuit 372.
3 They've created a new delayed read strobe that's coming out of this new DR-
4 1 element.

5 And why does that matter? Well, because the delayed strobe signal
6 from DR-1 is not being relied on and not being used to sample that read data
7 for Ground 4. And that's not our opinion, that's what Samsung said. It's
8 being used to clock out the data so that it's in sync with the strobe signal.
9 This is in their petition. This is a cite from their petition. It says the
10 delayed read strobe signal is clocking out the DQ data so that it can sync it
11 with that strobe, and that's it. Instead, for the sampling limitation, we saw
12 the petition just refers back up to Ground 1, and, in that case, the strobe
13 signal coming out of the preexisting delay circuit 372 is what's being relied
14 on.

15 And this paragraph here, 304, that's a citation to Dr. Wedig's
16 declaration. So what did he say about it? He was very clear here with
17 what his theory was, even though they've now kind of changed it on reply
18 with a new argument about how the sampling step is met. But we see here
19 in the same paragraph that the petition cited to, Dr. Wedig explains that the
20 first existing delay circuit is still making those adjustments, still properly
21 latching in the data. That's the term they use, latching in the data, that they
22 say necessarily means sampling the data, right? So according to the

1 petition, latching equals sampling.

2 Then what they say on page 37, this is on page 37 of the petition, they
3 now double-down in the reply on this, and that's reply page 20. But
4 continuing the same paragraph, we see Dr. Wedig goes on to explain that
5 this new delayed strobe is not just clocking out the data, the FIFO data. It's
6 doing this so that the data coming out is in sync, so it has a purpose. It's
7 like Hiraishi's local clock was before, turning to maybe duplicate what
8 Hiraishi was doing. The point is their position and their evidence does not
9 support that this new strobe signal is sampling the data that's coming into or
10 out of the FIFO. It's being used, according to them, to synchronize the data
11 and the DQS signal.

12 So at the end of the day, Ground 4 introduces new delayed strobe
13 signal. It didn't exist in Hiraishi. Instead, they're using a delayed strobe
14 signal to sample the data. It's being used to sync that data, I should say, and
15 that's why Ground 4 does not satisfy the sampling step.

16 Now, in slide 51, they change their theory. They realize that their
17 argument doesn't work, and this is not an elaboration or an explanation of
18 their original theory. It's specifically changing what it said, the sampling
19 limitation where it was previously just referring to Ground 1, which is
20 latching data into the FIFO using that delayed strobe from the delay circuit
21 372. And now it's relying on a brand new strobe signal that they had to add
22 to Hiraishi because it wasn't there, couldn't get it, and that's being used to

1 sync the data to the output. Nothing about sampling it.

2 So this is a new theory that they came up with. We don't think the
3 Board should consider under PTAB rules, but, if it were to consider it,
4 there's no evidence in support. Why is that the case? Well, they still have
5 to show two things they haven't shown. That this proposed DQ signal
6 coming down from the DR-1 is actually capable of clocking out data. This
7 is a DQS signal, not a clock signal now like it was in Hiraishi. And then,
8 secondly, that clocking-out data, which is how they're describing this, from a
9 FIFO is actually sampling within the meaning of the 506 patent. So that's
10 the burden even for this new theory, and we don't believe they've met it.
11 And the reason is is that none of Dr. Wedig's testimony supports this
12 assertion that strobe signals can properly clock out data from a FIFO. This
13 was Petitioner's own characterization of Dr. Wedig's testimony and his
14 testimony about Hiraishi's clock signal, not a DQS signal, is being used to
15 sample the outgoing DQ data from the FIFO. This is their own
16 characterizations.

17 Now, in paragraph 304 of their declaration, Dr. Wedig does describe
18 his proposed modification. He says he's proposing to use the delayed strobe
19 signal to clock out data from FIFO so that it's in sync. We talked about
20 that. But when he's asked during his deposition about what is actually
21 possible and, you know, the part about clocking out being a sampling, in
22 those cases, he was referring exclusively to clock signals. So the evidence

1 does not support their contention.

2 Dr. Wedig, on page 54, admitted that clock signals are not strobe
3 signals, they each have their purpose. And on slide 55, this was on redirect,
4 even after he took some time to think about it, you know, he again was
5 referring to clock signals. And, again, this is their reading of his testimony,
6 not our characterization. There's no other evidence in the record that
7 supports this idea of a DQS signal being used to clock out data.

8 JUDGE GALLIGAN: Counsel, this is Judge Galligan. You're at
9 your ten-minute warning. You may continue.

10 MR. LINDSAY: I'm at ten minutes now, Your Honor?

11 JUDGE GALLIGAN: Yes, of your total amount. You've got
12 whatever -- you can eat into your rebuttal if you want.

13 MR. LINDSAY: Okay. I just wanted to maybe finalize this last
14 point. So there's nothing in the record that suggests you can use this DQS
15 signal to clock out data from a FIFO. We'll look quickly at slide 56. It's
16 Hiraishi. Hiraishi exclusively uses clock signals to clock out data from
17 FIFO, both the write and the read. In slide 57, this is Tokuhiro again.
18 Their own references also support the fact that it's usually this clock signal
19 in yellow that's being used to clock out data from the flip-flops, FF-6, FF-8,
20 and so forth. And, again, even this is consistent with the 506 patent itself
21 on slide 59 where it describes using this delayed strobe signal to read data.
22 That's the citation up there. It's using this delayed signal that is then

1 sampled in a receiving circuit, 1670.

2 Separate from that, there's a delay circuit, 1660, shown in green. And
3 in that case, the DQ data, which would be, you know, temporarily stored, it's
4 a delay circuit, in that case it's being clocked using a clock signal CK-0.

5 Dr. Mangione-Smith explained this in his deposition, as well.

6 So the 506 patent is also clear on this point. The data is sampled, not
7 clocked, using the DQS signal at the front, and it's clocked, not sampled,
8 using the clock signal.

9 And I'll reserve the rest of my time, Your Honor.

10 JUDGE GALLIGAN: Okay. Thank you, Mr. Lindsay. You have a
11 little over eight minutes remaining. Let me make a note of that. Okay.
12 Petitioner, you have 12 minutes remaining. You may begin.

13 MR. CHANDLER: Thank you, Your Honors. Is there a particular
14 area that you would like me to respond to first, any particular questions that
15 you have now?

16 JUDGE GALLIGAN: Yes, I wanted you to respond briefly about the
17 argument the Patent Owner made that Butt is talking about a different sort of
18 thing, a design time. And I think I got some clarification after my question,
19 but whether Butt's read training is done every time you fire up the memory
20 or if it's just a design time. Could you address that?

21 MR. CHANDLER: Yes. So that's Netlist's slide 36, which I have
22 on the screen. So when Butt was talking about the conventional approach

1 where you would use SPICE timing analysis, that was at manufacturing time
2 you would try to essentially even out the wires to make the timing aligned.
3 And Butt says that is not sufficient. Butt teaches, as you correctly
4 recognized, a technique that is performed whenever you initialize the
5 memory device. But when it's actually up and running, you need to do fine-
6 level adjustments between the strobe and the data signal.

7 And if you look at Samsung's slide 63, Netlist's expert, Dr. Mangione-
8 Smith, admitted for DDR3 memory as the DQ and DQS signals can become
9 out of alignment, and he admitted that Butt's technique can solve that
10 problem. Answer: I think that accurately paraphrases some of what Butt
11 claims to teach, sure. So Butt is a one-time solution given that the clock
12 speeds were getting so fast.

13 Slide 61 shows Butt on a time line. Netlist incorrectly argues that
14 Butt is only relevant to the older DDR1 standard. That's not true. Butt
15 came out after DDR1 and DDR2 had already been finalized. Butt invented
16 while DDR3 was in the process of being standardized. So by that time,
17 everyone knew clock speeds were getting faster. Everyone knew that
18 leveling was going to be important. And as shown on slide 62, Butt's
19 invention is not limited to DDR1. Butt improves the current DDR2
20 techniques by disclosing a new technique of data eye training to enable high-
21 speed applications. Butt is directly relevant to DDR3.

22 On the collateral estoppel point, the Board's previous findings in the

1 Micron final written decision are directly relevant. I want to draw the
2 attention again to the Mobile Tech case, page 18, where the Board stated that
3 the law for collateral estoppel is, quote, under traditional principles of issue
4 preclusion; however, a party may be bound not simply by the ultimate
5 conclusion, e.g. unpatentability of a claim, but by any subsidiary factual
6 determinations that were actually litigated and essential to the judgment, end
7 quote.

8 And in the Micron final written decision, as shown on Samsung's slide
9 30, the Board found that when Osanai performs read leveling, the result, as
10 shown at the bottom left in blue, is that Osanai's, the disclosures of Osanai
11 are sufficient to teach controlling the timing of the data and strobe signals on
12 the data paths. That's all that both the 035 patent required and the 506
13 patent. That finding by the Micron final written decision is sufficient to
14 render obvious delaying the first read strobe. The same issue that's been
15 decided but provides additional motivation and teaching to do that, the
16 Board already found that Osanai and Hiraishi alone was sufficient to provide
17 that teaching.

18 On Ground 4, there was some argument that somehow Petitioner had
19 changed its theory on Ground 4 that I would like to respond to with
20 Samsung's slide 86. So the Ground 1 figure from the petition, page 36 and
21 37, is shown at the top. The Ground 4 figure from the petition, page 109 to
22 110, is shown at the bottom. The claim language, as shown on the left,

1 from Claim 1, for both Ground 1 and Ground 4, the sampling is you just
2 sample with the strobe. There's no dispute that a strobe can be used to
3 sample data. That's been done forever. That's what the JEDEC standard
4 shows. That's what Hiraishi shows. So sampling with a strobe is well
5 known. The dispute and the difference between Ground 1 and Ground 4 is
6 what is the first delayed read strobe that is being pointed to. Ground 1
7 points to the delayed read strobe that's coming into the FIFO from 372,
8 whereas Ground 4 is pointing to the delayed read strobe that's coming from
9 Tokuhiko's delay element, which would be used on the output of FIFO 302.

10 And if you look at slide 85, the Ground 4 combination of using a
11 delayed strobe for the output of the FIFO is very similar to what the 506
12 patent expressly says is sampling. So this blue dash line in Figure 15 and
13 16 of the 506 patent is a delayed strobe, and at box 60 and 70, when that
14 delayed strobe is used, that is sampling the output of 1670. And so for
15 Netlist to argue that Ground 4, as shown on slide 86, doesn't satisfy the
16 sampling limitation is entirely inconsistent with their own patent, which
17 teaches that that is sampling.

18 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I think the
19 issue that Petitioner points out is a couple of things. One is the Petitioner
20 says that 1G remains the same, and the sampling is done by the signal
21 coming from delayed circuit 372. I think in the Hiraishi/Butt combination
22 says that that's when the register, the 302 registers the data, samples the data.

1 And then in your petition at page 110, the Petitioner's petition at page 110, it
2 says that this additional delay element is used to clock out the data from the
3 FIFO so that, you know, Patent Owner is saying, look, you've already
4 registered the data, clocking out the data isn't the sampling that you
5 previously talked about, even though you pointed to in the next slide,
6 whatever that slide was, with Figures 15 and 16. I mean, maybe there's
7 another buffer because there's a sampling there.

8 It did seem like you switched a little bit when on redirect, I think, Dr.
9 Wedig said, well, yes, clocking is a type of sampling. I certainly read your
10 petition to say that the sampling occurs when it's registered into the FIFO
11 buffer.

12 MR. CHANDLER: There's two samplings, Your Honor, and they
13 both happen in Ground 4. So there's the sampling into the FIFO, which is
14 all that Ground 1 relies on. And then there's a sampling out of the FIFO,
15 which is what Ground 4 relies on. And in Ground 4, you still have the
16 sampling into the FIFO. I mean, so, in other words, Ground 4 doesn't rely
17 on Ground 1, but Ground 4 is consistent with Ground 1. You could still
18 have Butt and all of its teachings in Ground 4, but Ground 4 has the
19 sampling out of the FIFO which is exactly what the 506 patent does, as
20 shown on slide 85, is the delayed strobe is used to sample the delayed data
21 out of the FIFO and then it goes off to the left, which is the same thing that
22 Ground 4 does.

1 And the petition on slide 87, Samsung slide 87, you cited to page 110
2 of the petition, which we've shown on the left here. The petition is clear.
3 It's the delayed strobe that clocks out the data, and we didn't have to show a
4 figure but we annotated a figure to be crystal clear about what we were
5 pointing to, which is on the right, is the purple delayed strobe that's to the
6 output of the FIFO in Ground 4, that's what's being identified as the delayed
7 strobe.

8 And on slide 88, Netlist argued in its surreply that Dr. Wedig never
9 testified that a person of ordinary skill in the art would have used a DQS
10 signal instead of a clock signal to clock out data from a FIFO. It's directly
11 contradicted by what Dr. Wedig actually said in paragraph 304 shown on the
12 right where Dr. Wedig expressly said use the delayed strobe to clock out the
13 data from the FIFO.

14 With respect to this issue about LCLKR, this is Samsung slide 81, the
15 way the questioning went is Dr. Wedig was being asked about the input to
16 the FIFO, and he said, no, the LCLKR isn't being used to sample the input to
17 the FIFO. And then there was a question asked about the output of the
18 FIFO, and there was an objection to the form of the question because, the
19 way the question was asked, it was unclear whether the question was asked
20 about the input or the output. But Dr. Wedig's answer to the question
21 makes clear that he was saying that LCLKR couldn't be used to sample the
22 input because that's what the DQS strobe is doing. Instead, LCLKR is

1 sampling the output, and he made that clear on redirect and as well as on
2 recross, that he was just saying that you wouldn't use LCLKR to sample the
3 input, you would use it to sample the output.

4 JUDGE BOUCHER: Mr. Chandler, could I just take a moment to
5 talk about this collateral estoppel issue?

6 MR. CHANDLER: Yes.

7 JUDGE BOUCHER: You would agree, wouldn't you, that this panel
8 is not bound by the findings of the Micron panel, or would you not agree
9 with that?

10 MR. CHANDLER: I disagree. I mean, the Micron panel is a final
11 written decision on the Board. Well, you're saying is this panel bound? I
12 think, as a matter of precedent, that, for collateral estoppel, it should be
13 applied. I mean, that is the precedent, that is the law, that when there's a
14 final decision that it should be binding.

15 JUDGE BOUCHER: Even if it's not designated precedential and
16 even if this panel thinks the previous panel was just simply wrong on an
17 issue?

18 MR. CHANDLER: Yes. I mean --

19 JUDGE BOUCHER: Your position is we would be precluded from
20 any contrary finding?

21 MR. CHANDLER: Yes. Collateral estoppel is not stare decisis. I
22 mean, collateral estoppel is separate. It's an issue that it binds Netlist, and

1 so Netlist's remedy, if Netlist disagrees with the Micron decision, Netlist can
2 appeal the Micron decision. But in this IPR, Netlist should be bound by the
3 prior decision and, I mean, like we said, I think the precedent, as shown on
4 slide 36, is clear that collateral estoppel --

5 JUDGE BOUCHER: I understand that, and I don't want to belabor it,
6 but I don't see why the panel would be bound by a non-precedential
7 decision, and I'm having difficulty understanding the application of the
8 collateral estoppel when the arguments were made by the Patent Owner in
9 briefing before that previous decision was made. It seems like you're
10 suggesting we would be precluded from even considering those arguments.

11 MR. CHANDLER: They had an opportunity to be heard on the
12 arguments that we've shown, for example, on slides 30 and 31. So, I mean,
13 they had their day in court on whether or not Osanai and Hiraishi actually
14 delays the strobe signal. They had an entire IPR proceeding on that. There
15 was a final written decision, and there should be consequences from that
16 final written decision for Netlist since they've had their day in court on that
17 issue.

18 On the issue of whether this panel is bound by the prior panel, I mean,
19 I am aware, as I said, of the Mobile Tech case where the outcome on page
20 33 was that panel said, yes, the fact that an appeal is pending does not
21 prevent the application of collateral estoppel, but then the panel went on to
22 say, out of an abundance of caution, however, we decline to apply collateral

1 estoppel to this claim and we'll address the Petitioner's arguments on the
2 merits. And then on the merits, you know, the second panel invalidated the
3 claims.

4 So that's sort of a middle-of-the-road approach to agree that collateral
5 estoppel should apply but then to still reach the merits, but, as to your legal
6 question, I would say, yes, collateral estoppel is binding. I mean, to your
7 point of, you know, what if the new panel thinks the earlier panel was
8 wrong, that's the whole effect of collateral estoppel is that Netlist doesn't get
9 a second bite at the apple to come up with a whole new set of arguments. If
10 you didn't like my arguments the first time, let's start back at square one and
11 I'll give you a whole new set of arguments in the second case. That's the
12 whole point of collateral estoppel is that Netlist does not get two bites at the
13 apple, even if their second bite was better than their first bite.

14 JUDGE BOUCHER: Okay. I understand your position I think.
15 Thanks.

16 JUDGE GALLIGAN: And, Mr. Chandler, you're out of time.

17 MR. CHANDLER: Okay. I'll stop there.

18 JUDGE GALLIGAN: Thank you very much. Mr. Lindsay, we gave
19 Mr. Chandler a few extra minutes, three extra minutes, three and a half extra
20 minutes. You have about 11, yes, you've got about 12 minutes remaining
21 with the extra time, 11 and a half minutes. And you may begin.

22 MR. LINDSAY: Thank you. Thank you, Your Honors. So a

1 couple of quick points I would like to make. I would like to go back and
2 revisit one of our earlier conversations about Hiraishi's buffers or input
3 buffers and whether they were somehow delaying the DQS signal. I would
4 just point out a couple of things. One is that's not an argument that's ever
5 been made in this IPR. Dr. Wedig never raised this in his declaration part
6 of the petition. Dr. Mangione-Smith did not talk about this being an issue
7 and that the delay that was being predetermined was actually imposed by the
8 input buffers. It was always being imposed by the delay circuit. We can't
9 address arguments that are not made in this IPR, and I think we took the
10 combination as it was presented to us.

11 I'd like to share my screen actually and go to slide 90. I mentioned
12 that DQS signal cannot be used to clock out the data, and there's a reason for
13 that. A DQS signal is very different than a clock signal. It has a preamble
14 and it has a postamble, and we talked about this on surreprely, we pointed this
15 out since, you know, this is kind of a new theory for them on how this
16 delayed read strobe signal can be satisfied now on Ground 4. And you're
17 going to clock out additional bits. You're not going to have the data line up
18 with the way you need it to you if you're using a DQS signal which, again
19 have these requirements. That's the standard down in the lower left corner
20 that we're looking at, and the effect of that is shown in Hiraishi itself in
21 Figure 15. So, again, we don't think that's a feasible combination of
22 suggestion this is their new argument.

1 As to another point, we talked about Butt's reference to a conventional
2 design time system. So Samsung's arguments don't depend at all, haven't
3 ever raised what Butt said was conventional. That's not part of the record
4 either. Dr. Wedig did not indicate that there's any preference for one way
5 or the other. Instead, what we're told is that Hiraishi just inherently needs
6 this, even though Hiraishi's express disclosure says otherwise. So, again,
7 we'll just point that out that we've heard this just for the first time, I think,
8 today, and there's no evidence in the record that would suggest, you know,
9 that Butt is improving, can improve Hiraishi. Again, we're taking their
10 arguments at their face.

11 And I'll just pause and see if Your Honors have specific questions for
12 me with our remaining time because I want to make sure I address those.

13 JUDGE GALLIGAN: I don't think I did. Proceed.

14 JUDGE JURGOVAN: I'll ask another question, and that is are you
15 saying that, in Petitioner's mapping, they are using the DQS signal both to
16 clock or to sample the data into the FIFO buffer and also to clock it out of
17 the FIFO buffer? Is that what you're saying?

18 MR. LINDSAY: So for Ground 4, so the position that they've taken
19 is that the delayed strobe signal that's being relied on, I'll jump down to slide
20 95 to orient us a bit, the purple line here is the delayed read strobe signal for
21 purposes of Ground 4. Now, that's for the sampling limitation, they just
22 said, oh, sampling is done the same way as it's done in Ground 1. Well, in

1 Ground 1, the sampling was done using this little line that comes down from
2 372 to the FIFO 302. The problem is that the sampling for the claims has to
3 be done using what you've now determined to be, through these previous
4 memory operations, you've determined there to be a predetermined amount
5 of delay, which is again what they're saying this purpose line is that's going
6 into the FIFO. But that's not sampling the data. That's clocking it out, just
7 like Hiraishi's old internal clock signal was doing. They're trying to
8 duplicate this effect so that they get the data synchronized on the way out.

9 The combination just doesn't work for a number of reasons, Your
10 Honor, that we've pointed out, including why you would take, you know,
11 here's memory controller, extract the delay element out of that, put it into the
12 data buffer for Hiraishi to do basically the same thing that Hiraishi was
13 already doing with S-5 leveling using the memory controller. Tokuhiko
14 does S-5 leveling using the memory controller. But they've created this,
15 you know, Frankenstein combination because they're trying to get to that
16 delayed read strobe signal. They just couldn't do it even with all the
17 additional machinations of this combination.

18 Had they done it the way Tokuhiko did, adjusting for those fly-by
19 delays into the memory controller using the memory controller, that would
20 be something to talk about. Had they done it the way Hiraishi does it, S-5
21 leveling, that would be something to talk about. But that's not the challenge
22 here. That's not at all what they've challenged the claims based on.

1 So there's a little bit of mix and matching, back to your question, as to
2 delayed strobe signals. They say this delayed strobe signal is doing the
3 sampling for Ground 1. I don't believe that's challenged. And then in
4 Ground 4, they're saying it's done the same way but, hey, you know what,
5 this time we're going to rely on the purple line to be our delayed strobe
6 signal. And so it just didn't work.

7 JUDGE JURGOVAN: Okay. So one more time, if you could just
8 explain to me why Hiraishi does not need to adjust DQS relative to DQ.

9 MR. LINDSAY: Okay. Let me find a diagram of our Figure 5.
10 Okay, good. So I'm going to go up to Figure 19. So the question was why
11 does Hiraishi not need to adjust DQ versus DQS?

12 JUDGE JURGOVAN: Yes, I think that's what you were arguing.

13 MR. LINDSAY: Yes. So Hiraishi does two things. So it has this
14 delay circuit that we've already -- so for purposes of sampling, it uses a fixed
15 90-degree delay, so it does need to do that shift for sampling purposes into
16 the circuit.

17 JUDGE JURGOVAN: Okay.

18 MR. LINDSAY: The reason it doesn't need to, you know, it has
19 those fly-by delays. We looked at the time A. I'll go up one slide here.
20 These time As right there are different for different memory chips and
21 different buffers. The fly-by delay, horizontal delays, I think, sometimes
22 the papers call it. So what does it do about that? Well, it doesn't do what

1 maybe other systems may think of doing, certainly not what Samsung has
2 argued in this case. What it does is it says, you know what, we're not going
3 to try to figure out delays, we're just going to generate, we're going to go the
4 next clock cycle, clock cycle 6, and we're going to generate our new -- this is
5 that retiming operation I mentioned. You haven't heard any of it from
6 Samsung because I think it kind of shows you what's going on in Hiraishi
7 and why it's not concerned with delays. It's regenerating a new strobe
8 signal. This strobe signal that came in through the selector, it's terminated,
9 it's done. It's not being used in the rest of the circuit. It's not passed
10 through. In fact, that's why they had to add that DR-1 element in Ground 4.
11 It was trying to find some DQS to pass through because, normally, it doesn't.
12 It gets regenerated right here in 376, and the reason that's important is
13 because it uses this clock signaling syncing mechanism where it can
14 confidently say and it can confidently report to the memory controller, at
15 least the memory controller will know, hey, I'm going to get this data in six
16 clock cycles, this device is going to meet the latency that I'm expecting it to
17 have, six clock cycles. It's not going to do that by delaying it. It's going to
18 do that by generating for me a new DQS signal. It's going to be synced
19 with the FIFO, and it's exactly six clock cycles later.

20 JUDGE JURGOVAN: So what you're saying is that it's only
21 necessary to adjust DQS relative to DQ if you're not generating those signals
22 internally to the data buffer?

1 MR. LINDSAY: Right. Well, it's definitely not necessary to delay a
2 signal that you're not even using. You're terminating it to the FIFO and
3 you're regenerating it before output. Whether it's necessary in other
4 systems, you know, I can't say, of course, but that's why Hiraishi doesn't
5 need any internal delay.

6 JUDGE JURGOVAN: Thank you.

7 MR. LINDSAY: So I think, as a final point, we didn't talk too much
8 about the Tokuhiro and Hiraishi combination. We have a number of
9 arguments about their three motivations to combine. They provide these
10 three motivations to combine about fly-by delays greater than one clock
11 cycle. The papers address those, we think. But before the Board even
12 needs to get to any of those things, we'd just point out that what they're
13 actually proposing to do in the combination has nothing to do with those
14 three motivations. What they're proposing to do by taking this delay circuit
15 out of Tokuhiro's memory controller and sticking it into Hiraishi's data
16 buffer are completely unrelated. They could have easily implemented
17 Tokuhiro as it's described using the memory controller controlled by the
18 CPU, dedicated signals into the memory controller to operate those delay
19 elements. That's what Tokuhiro describes.

20 Hiraishi, they say it takes care of fly-by delays on its own using test
21 five, but they ignore all those express teachings and instead created
22 something from scratch, and they did it in ways unrelated to achieving the

1 three motivations that they suggest are the motivating factors for the
2 combinations.

3 JUDGE GALLIGAN: You have about 30 seconds left.

4 MR. LINDSAY: Okay, Your Honors. I will end there and let us all
5 save 30 seconds then.

6 JUDGE GALLIGAN: Thank you very much. Excellent
7 presentations. We appreciate the counsel's preparedness. We are
8 adjourned, and a final decision will issue in due course.

9 (Whereupon, the above-entitled matter went off the record at 4:19
10 p.m.)

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