

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,860,506

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Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH TIMING-CONTROLLED DATA
BUFFERING

Inter Partes Review No. IPR2022-00711

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
10,860,506**

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EXHIBIT LIST

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1001	U.S. Patent No. 10,860,506
1002	File History of U.S. Patent No. 10,860,506
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. 2010/0309706 to Hiraishi
1006	U.S. Patent No. 8,020,022 to Tokuhiro
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry
1008	U.S. Patent No. 6,184,701 to Kim
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	U.S. Patent Pub. No. 2011/0062999 to Nimaiyar
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

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1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts)
1022	Harold S. Stone, Microcomputer Interfacing (1982)
1023	Microsoft Computer Dictionary 334 (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to '632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 5,036,221 to Brucculeri
1028	U.S. Patent No. 6,906,555 to Ma
1029	U.S. Patent Pub. No. 2007/0008791 to Butt
1030	U.S. Patent No. 7,036,053 to Zumkehr
1031	U.S. Patent No. 9,824,035
1032	File History of U.S. Patent No. 9,824,035
1033	U.S. Patent No. 10,268,608
1034	File History of U.S. Patent No. 10,268,608
1035	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)

Exhibit #	Reference Name
1036	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1037	Netlist’s motion to dismiss the First Amended Complaint, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1038	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1039	JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019)
1040	Order extending response to complaint to April 12, 2022, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 29, 2021)
1041	Micron’s proposed claim constructions, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 6:21-cv-00431 (W.D. Tex. Dec. 23, 2021)
1042	Netlist’s proposed claim constructions, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 6:21-cv-00431 (W.D. Tex. Dec. 23, 2021)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1[pre]	1. A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
1[a]	a module board having edge connections to be coupled to respective signal lines in the memory bus;
1[b]	a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
1[c1]	memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals
1[c2]	wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
1[d]	data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and
1[e]	wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
1[f]	delay the first read strobe by a first predetermined amount to generate a first delayed read strobe.

Ref. #	Listing of Challenged Claims
1[g]	sample the first section of the read data using the first delayed read strobe; and
1[h]	transmit the first section of the read data to a first section of the data bus;
1[i]	wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.
2[a]	2. The memory module of claim 1, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and
2[b]	wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:
2[c]	delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;
2[d]	sample the second section of the read data using the second delayed read strobe; and
2[e]	transmit the second section of the read data to a second section of the data bus;
2[f]	wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.
3[a]	3. The memory module of claim 2, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe,
3[b]	wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and

Ref. #	Listing of Challenged Claims
3[c]	wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:
3[d]	delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;
3[e]	sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and
3[f]	transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;
3[g]	wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.
4[a]	4. The memory module of claim 2, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and
4[b]	wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation
5	5. The memory module claim 2, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.
6	6. The memory module of claim 1, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation.

Ref. #	Listing of Challenged Claims
7[a]	7. The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and
7[b1]	wherein the first data buffer is further configurable to: receive the module clock signal;
7[b2]	generate a local clock signal having a programmable phase relationship with the module clock signal; and
7[b3]	output the local clock signal;
7[c]	wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.
8[a]	8. The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and
8[b]	output a module clock signal together with the module control signals to the data buffers, and
8[c]	wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.
9[a]	9. The memory module of claim 8, where-in the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and
9[b]	wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and

Ref. #	Listing of Challenged Claims
9[c]	to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.
10[a]	10. The memory module of claim 9, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to
10[b]	select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and
10[c]	wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.
11	11. The memory module of claim 1, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.
12	12. The memory module of claim 1, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.
13	13. The memory module of claim 1, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.
14[pre]	14. A method, comprising:

Ref. #	Listing of Challenged Claims
14[a]	at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including
14[b]	a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board,
14[c1]	memory devices arranged in multiple ranks on the module board and coupled to the module control device, and
14[c2]	data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer,
14[d]	wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;
14[e]	receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;
14[f1]	outputting, at the module control device, registered C/A signals in response to the input C/A signals,
14[f2]	wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;
14[g]	outputting, at the module control device, module control signals;
14[h]	receiving, at each of the data buffers, the module control signals from the module control device;

Ref. #	Listing of Challenged Claims
14[i]	the method further comprising, at the first data buffer, in response to one of more of the module control signals:
14[j]	delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;
14[k]	sampling the first section of the read data using the first delayed read strobe; and
14[l]	transmitting the first section of the read data to a first section of the data bus; and
14[m]	the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.
15[a]	15. The method of claim 14, wherein the data buffers further include a second data buffer, and
15[b]	wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe,
15[c]	the method further comprising, at the second data buffer, in response to the one or more of the module control signals:
15[d]	delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;
15[e]	sampling the second section of the read data using the second delayed read strobe; and
15[f]	transmitting the second section of the read data to a second section of the data bus;
15[g]	wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations.

Ref. #	Listing of Challenged Claims
16[a]	16. The method of claim 15, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe,
16[b]	the method further comprising, at the first data buffer, in response to the one or more of the module control signals:
16[c]	delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;
16[d]	sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and
16[e]	transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;
16[f]	wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations.
17[a]	17. The method of claim 15, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and
17[b]	the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.
18[a]	18. The method of claim 14, further comprising:
18[b]	receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;
18[c]	outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
18[d]	receiving, at the first data buffer, the module clock signal;

Ref. #	Listing of Challenged Claims
18[e]	generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and
18[f]	outputting, at the first data buffer, the local clock signal;
18[g]	receiving, at the first memory device, the local clock signal; and
18[h]	outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.
19[a]	19. The method of claim 14, further comprising: receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;
19[b]	outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
19[c]	generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.
20[a]	20. The method of claim 19, further comprising, at the first data buffer: generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;
20[b]	selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;
20[c]	selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and
20[d]	sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

I. PETITIONER’S MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 10,860,506.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-CV-00136 (W.D. Tex. filed Apr. 28, 2021)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237
- U.S. Patent Application No. 17/114,478

The following proceeding is no longer pending:

- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to

DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-20 of U.S. Patent No. 10,860,506 (“’506 Patent”)(EX1001) based on Hiraishi (EX1005) alone or in combination with various secondary references, which were not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Grounds for Standing (§42.104(a))

Petitioner certifies that the ’506 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’506 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-20 of the ’506 Patent as follows:

	Ground	Claims
1	Obvious over <u>Hiraishi</u> and <u>Butt</u>	1-2,4,6-7,11,13-15,17-18
2	Obvious over <u>Hiraishi</u> and <u>Butt</u> and further in view of <u>Ellsberry</u>	3,5,12,16
3	Obvious over <u>Hiraishi</u> and <u>Butt</u> and further in view of <u>Kim</u>	8-10,19-20
4	Obvious over <u>Hiraishi</u> and <u>Butt</u> and further in view of <u>Tokuhiro</u>	1-2,4,6-7,11,13-15,17-18
5	Obvious over <u>Hiraishi</u> and <u>Butt</u> and further in view of <u>Tokuhiro</u> and <u>Ellsberry</u>	3,5,12,16

	Ground	Claims
6	Obvious over <u>Hiraishi</u> and <u>Butt</u> and further in view of <u>Tokuhiro</u> and <u>Kim</u>	8-10,19-20

Petitioner’s proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon in this petition is listed above on page xi.

IV. THE CONTESTED PATENT

A. Effective Filing Date

The ’506 Patent claims priority to a provisional application filed 7/27/12 (EX1025), which is after the prior art relied on by Petitioner, so for purposes of this IPR, Petitioner assumes that the claims of the ’506 Patent have an effective filing date of **July 27, 2012**. EX1003,¶36.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the ’506 Patent in July 2012 (“POSITA”) would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor’s degree in such engineering disciplines and at least three years of work experience in the field. EX1003,¶37. She would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how

they interact with other components of a computer system, such as memory controllers. *Id.* She would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers. *Id.*

C. The '506 Patent

1. Overview

The '506 Patent discloses a memory module (110) including memory devices (112, green) organized in groups, each group with an associated data buffer (isolation device 118, blue) and one module control device (116, red) located in the center of the module. EX1003,¶38;EX1001,Abstract,3:25-27,3:51-54,Fig.2C (annotated below)¹:

¹ Throughout the Petition, all emphases in quotations and color annotations to figures have been added unless indicated otherwise.

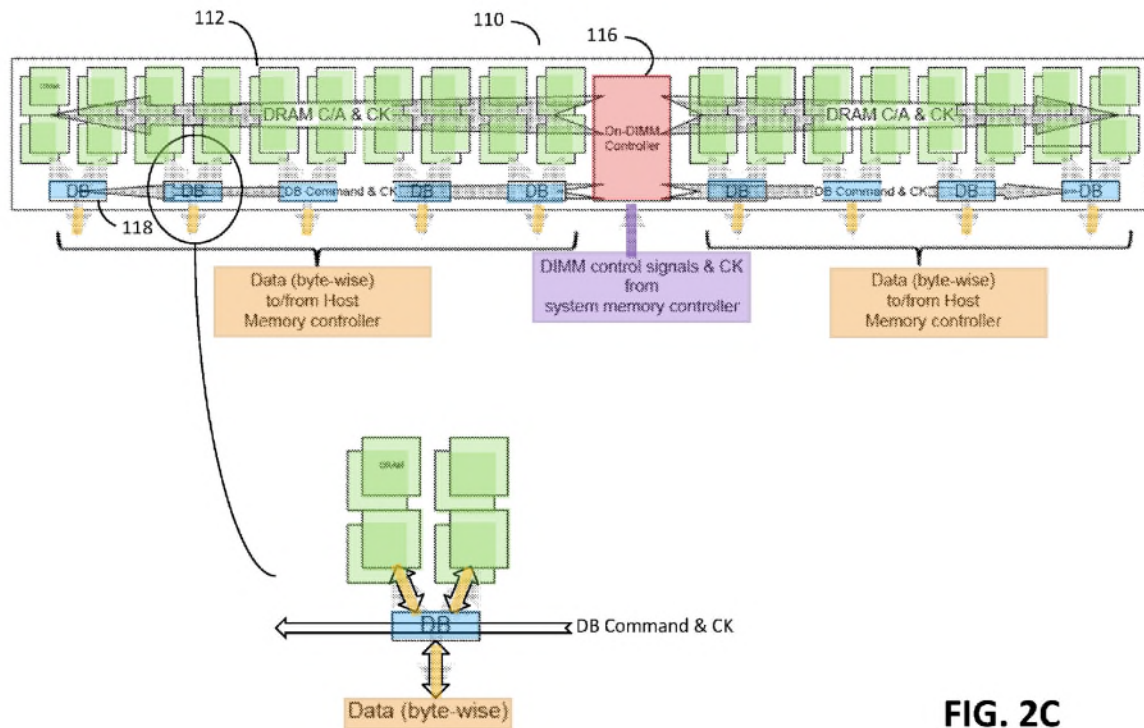


FIG. 2C

The memory module (110) is connected to a memory controller (MCH)

(101). EX1003, ¶39; EX1001, 3:29-34, 4:20-23, FIG. 1 (annotated below):

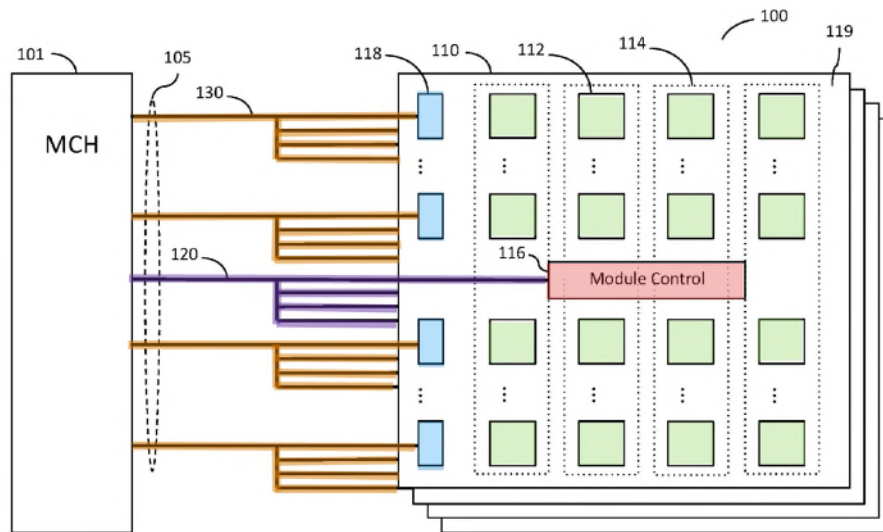


FIG. 1

As shown in the two figures above, a memory bus (105) connects the memory controller (MCH) (101) and the memory module (110) with control/address (C/A) signal lines (120, purple) between the memory controller (101) and the module control device (116, red), and data/strobe signal lines (130, orange) between the memory controller (101) and each memory device (112, green) via each data buffer (118, blue). EX1003,¶40;EX1001,4:20-32. The memory controller (101) issues C/A signals (on lines 120) to the memory module via the module control device (116), and sends and receives data/strobe signals (on lines 130) to/from the memory devices (112) via the data buffers (118). *Id.* The module control device (116) receives commands represented by a set of system C/A signals from the memory controller (101), and generates from them module command signals sent to the memory devices (112) and module control signals sent to the data buffers (118). EX1003,¶41-42;EX1001,4:65-5:7,5:57-65, *see also, id.*, FIGS. 2A-2B, 3:27-29, 4:60-64, 6:12-29.

The '506 Patent notes that, because the data buffers (blue) and their associated memory devices (green) are distributed across the memory module, “a same set of module control signals may reach different [data buffers (blue)] at different times across more than one clock cycle of the system clock.” EX1001,9:52-10:6,10:7-21;EX1003,¶43. As shown below, the data buffer can determine a time interval based upon the reception of signals to the data buffer

during a write operation—in particular, the difference (EWD) between reception of module control signal (MCS) corresponding to a **write command** (W/C) and reception of the corresponding data strobe (DQS1) (Fig.12A, below)—which can then be used to adjust signal timing during memory **read operations** (Fig.12B, below). EX1003,¶44;EX1001,15:27-50,15:66-16:6,FIGS.12A-12B:

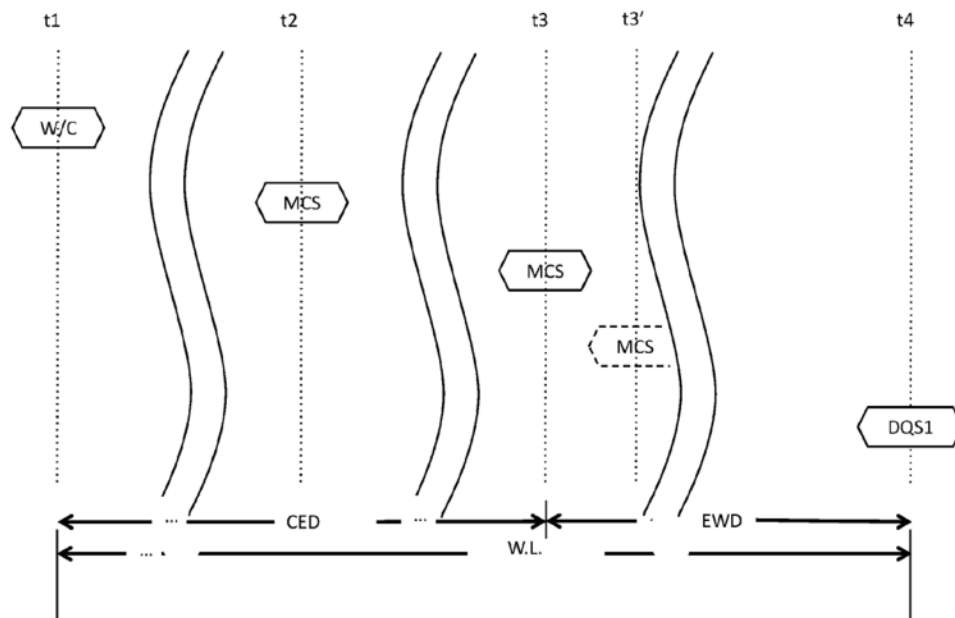


FIG. 12A

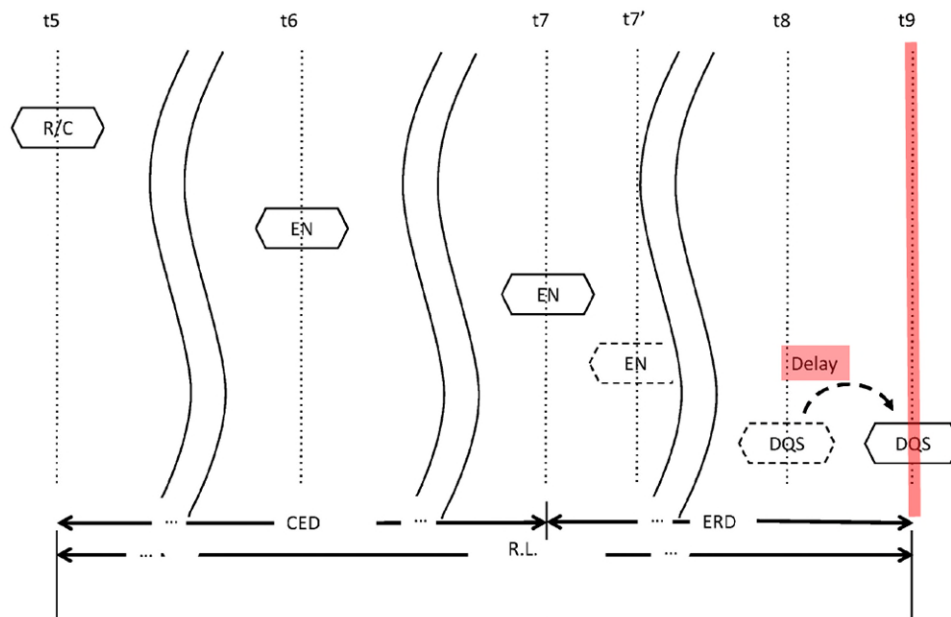


FIG. 12B

2. Prosecution History

The '506 Patent has the same written description as U.S. Patent No. 9,128,632 ("the '632 Patent"), which was previously the subject of an IPR petition by SK hynix (IPR2017-00730), challenging certain claims as obvious over US2010/0309706 combined with US7,808,849 and further in view of Kim (EX1008). EX1003, ¶¶50-52; EX1012. The Board denied institution on the basis of specific claim language in the '632 Patent not found in the '506 Patent. EX1003, ¶¶50-52; EX1014, pp.10-14. During prosecution of the '506 Patent, Patent Owner did not disclose anything about the '632 IPR, including the cited art, to the Examiner. EX1003, ¶53; EX1002. In the reasons for allowance, the Examiner

noted that many limitations of the claims were taught in the prior art.

EX1002,201-02;EX1003,¶60.

D. 35 U.S.C. §325(d)

The Board should not deny institution under *Advanced Bionics* and §325(d) given that neither the primary reference (Hiraishi) nor the combinations cited by Petitioner were presented to the Office, and no similar references were evaluated, during prosecution of the '506 Patent. EX1003,¶¶59-61. Only one of the secondary references relied on by Petitioner here (Ellsberry) was even submitted during prosecution of the '506 Patent, in an IDS among hundreds of other references. EX1002,116; *see also Thorne Research, Inc. v. Trustees of Dartmouth Coll.*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021) (“The fact that one piece of art from the combination was previously presented...to the Office alone is insufficient to satisfy the first prong of *Advanced Bionics* two-part test...”).

With respect to the prior IPR petition for the '632 Patent (great-grandparent to the '506 Patent), a different obviousness combination was presented (Saito and Swain), and the claims included language not found in the '506 Patent:

wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory **write** operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory **read** operation

EX1014 at 10. The Board's decision not to institute that IPR depended on this different claim language. *Id.*,10-14. Furthermore, the Board did not consider a reference like Butt (presented here) which describes the details of determining a time interval that is used to re-time the transmission of data signals. Thus, neither the Board nor the Examiner has considered whether the references presented here render obvious claims like those in the '506 Patent.

To the extent the '506 Patent is interpreted to require using signals received during a write operation to calculate a delay for a read operation (similar to the '632 Patent above), Petitioner is not relying on the obviousness combination presented in the '632 IPR to show that element. Instead, as explained below, Petitioner submits that such operation is obvious in view of Tokuhiro (EX1006), which was not considered by the Board or the Examiner. *Infra*,§VI.D-E,pp.93-126.

E. Construction of Terms Used in the Claims

Petitioner submits that the Board need not expressly construe any claim term because the prior art invalidates the claims under any plausible construction. EX1003,¶¶63-75. Indeed, Patent Owner took the position that similar terms in the related '632 Patent should be given their ordinary meaning, and the Board found no construction was necessary for those terms. *Id.*;EX1014,8.

In separate litigation between Patent Owner and Micron involving the parent and grandparent to the '506 Patent, there is currently a claim construction dispute

where Micron asserts that certain terms are subject to §112, ¶6 and indefinite for failure to disclose an adequate structure or algorithm, EX1041 at 9-11, while Patent Owner asserts that those terms are not subject to §112, ¶6 and should be given their plain and ordinary meaning, EX1042 at 4-5. Petitioner is not involved in the Micron litigation, and Petitioner and Patent Owner only recently began litigating in district court over the '506 Patent, so neither party has proposed any claim constructions yet, but depending on the resolution of the claim construction dispute involving Micron, that may cause Petitioner in the future to assert in district court that certain terms in the '506 Patent are subject to §112, ¶6 and indefinite for failure to disclose an adequate structure or algorithm. For purposes of this Petition, however, Petitioner adopts Patent Owner's current position on claim construction that §112, ¶6 does not apply. This is consistent with approaches previously approved by the Board and Federal Circuit. *See, e.g., Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (PTAB Nov. 10, 2020) ("Petitioner's alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review."); *Samsung Elecs. Am., Inc. v. Prisia Eng'g Corp.*, 948 F.3d 1342, 1355 (Fed. Cir. 2020) (holding that indefiniteness arguments in another forum "do[] not necessarily preclude the Board from addressing the patentability of the claims on section 102 and 103 grounds.").

V. OVERVIEW OF THE PRIOR ART

A. Hiraishi (EX1005)

US2010/0312956 (“Hiraishi”)(EX1005), published in 2010, is prior art under §102(b). Hiraishi was not cited or discussed during prosecution. EX1002;EX1003,¶76.

Hiraishi discloses an information processing system 10 including a memory system (20) with a memory module (100) and a memory controller (“memory control hub,” MCH 12) for controlling the memory module. EX1005,¶¶[0063-65],[0067-68],FIGS.2-3;EX1003,¶77.

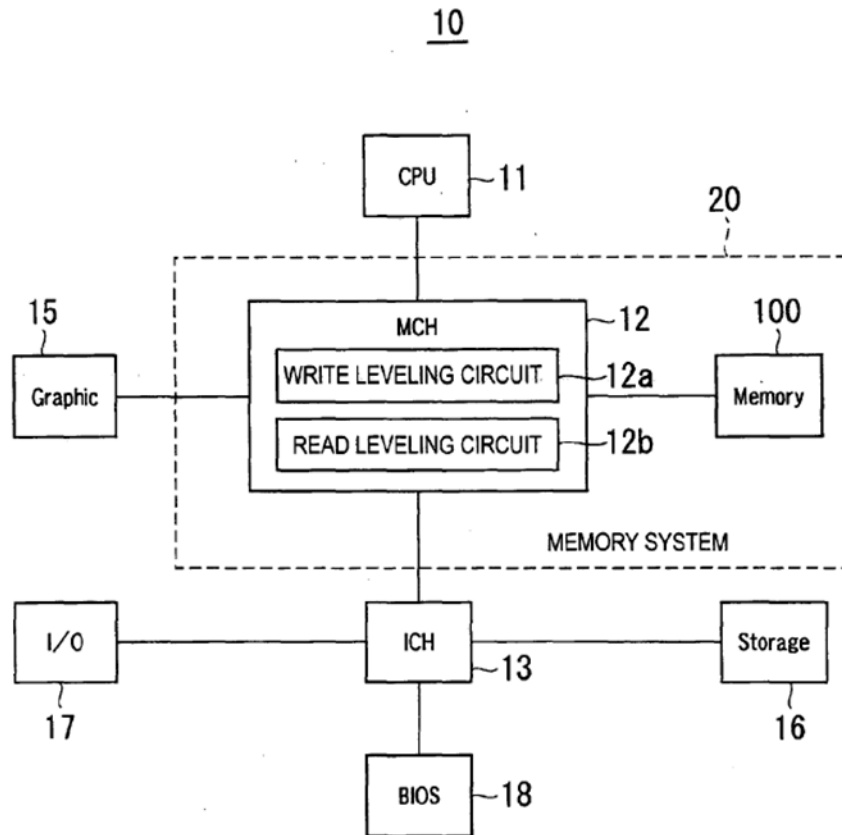


FIG.2

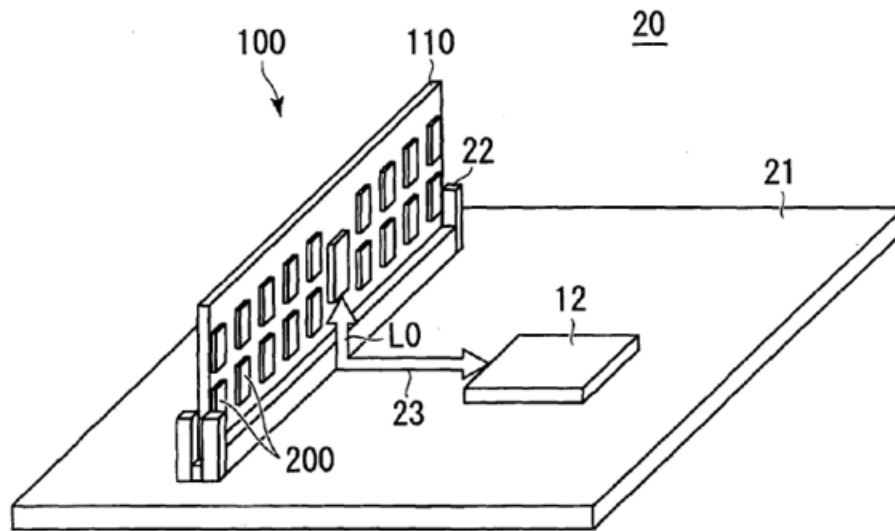


FIG.3

Annotated Figure 1 below illustrates an implementation of the memory module 100, including 36 memory devices (green) in a 4-rank configuration with 9 data register buffers (blue). EX1003,¶¶78-82;EX1005,¶¶[0045-49],[0051-52],[0055-56],[0059-61],[0103],[0107],FIGS.1,7.

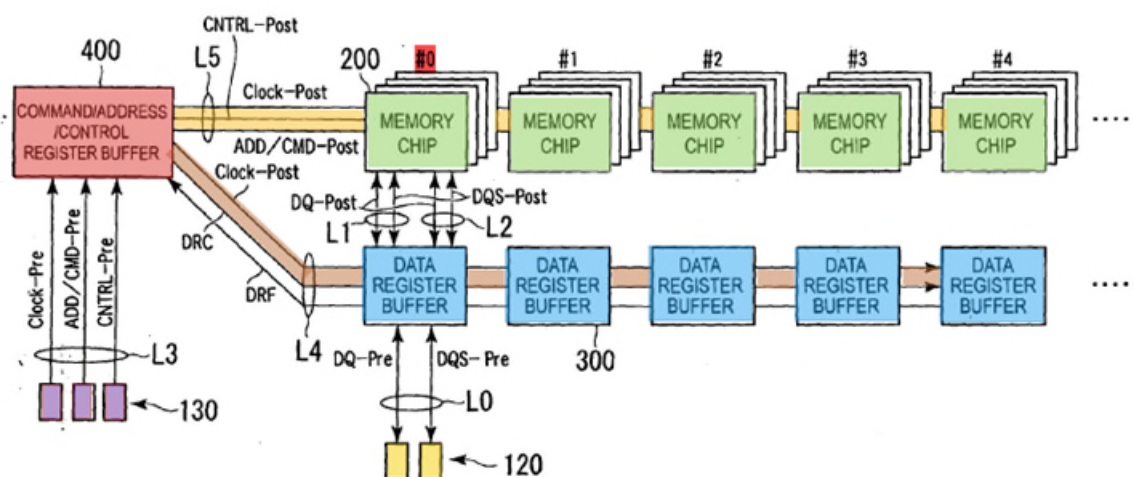
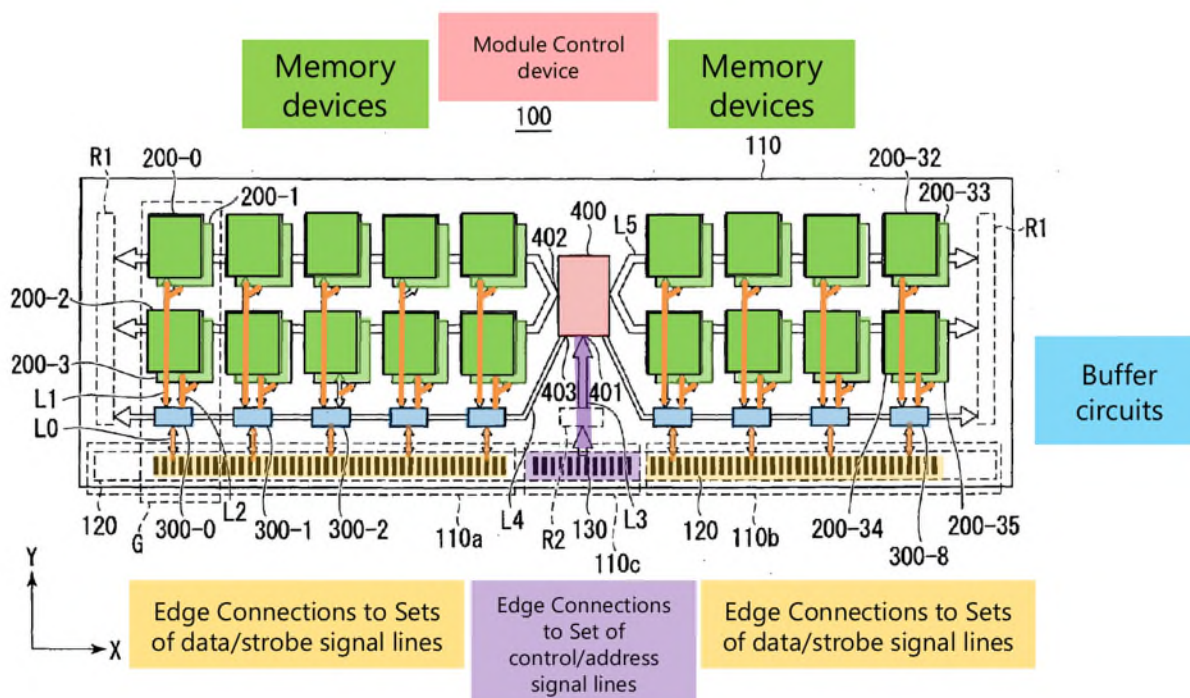


FIG.7

As annotated above (FIGS.1&7) and below (FIG.6), the “command/address/control register buffer” (400, red) “receives the command signal, the address signal, the control signal, and the clock signal” from the memory controller at an input terminal 401 (purple, below), buffers the signals, and supplies them at an output terminal 402 (orange, below) to the memory chips (200, green, above). EX1005, ¶¶[0060-61],[0103],[0107],FIG.7;EX1003, ¶¶78,82. Simultaneously, the “command/address/control register buffer” “generates a control signal” and supplies it at the output terminal 403 (brown, below) to the data register buffers (300, blue). EX1005, ¶¶[0060],[0096-97],FIG.6:

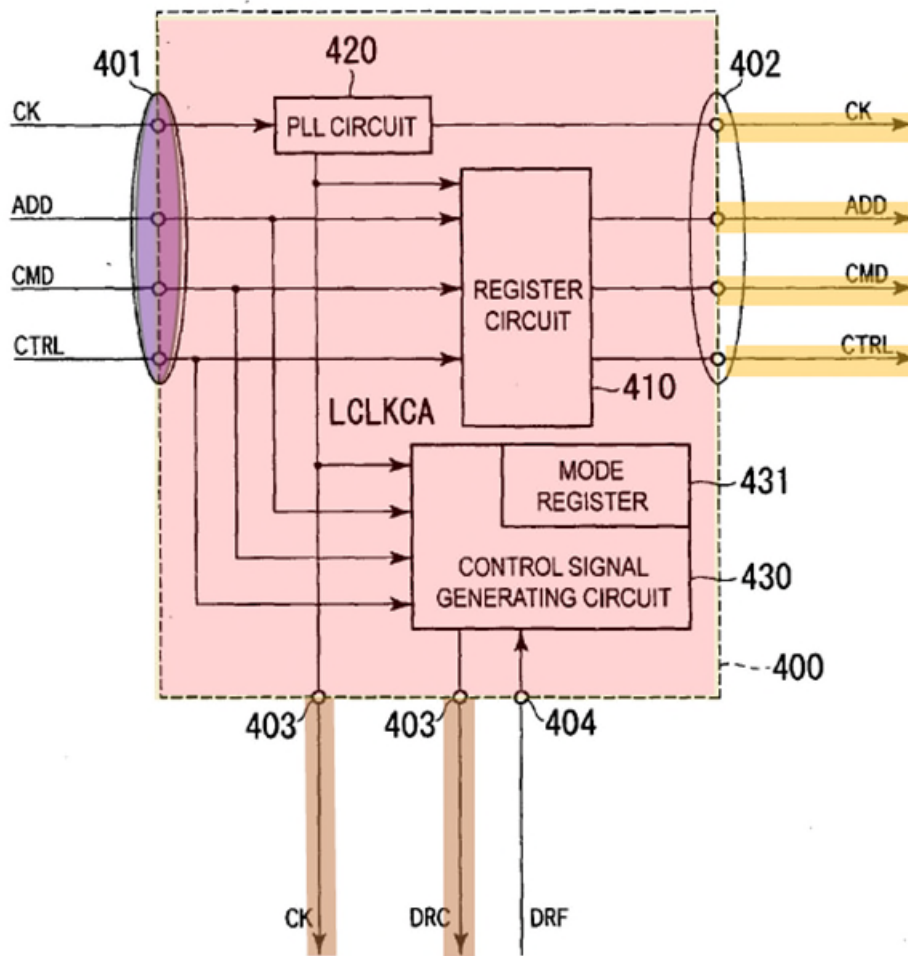


FIG.6

EX1003, ¶82.

Hiraishi's memory module makes "timing adjustments" to account for possible signal timing discrepancies due to high-speed operation and differing distances of the "memory chips" (green) and "data register buffers" (blue) from the "command/address/control register buffer" (red), EX1005, ¶¶[0090],[0104], during initialization by performing write leveling and read leveling operations.

Id., ¶¶[0140-41]. Each group of memory chips/data register buffer performs two

sets of write and read leveling operations, one “between the data register buffer 300 and the memory chip 200” (“Step S4”), *id.*, ¶[0140], and one “between the memory controller and the data register buffer 300” (“Step S5”), *id.*, ¶[0141]; EX1003, ¶83. An implementation below shows the data register buffer 300 (blue), including a data register control circuit 320 (upper right) with a write leveling circuit 322 and a read leveling circuit 323 to perform the “S4” leveling operations. *Id.*, ¶¶[0084],[0087],[0142],[0147], FIG.5.

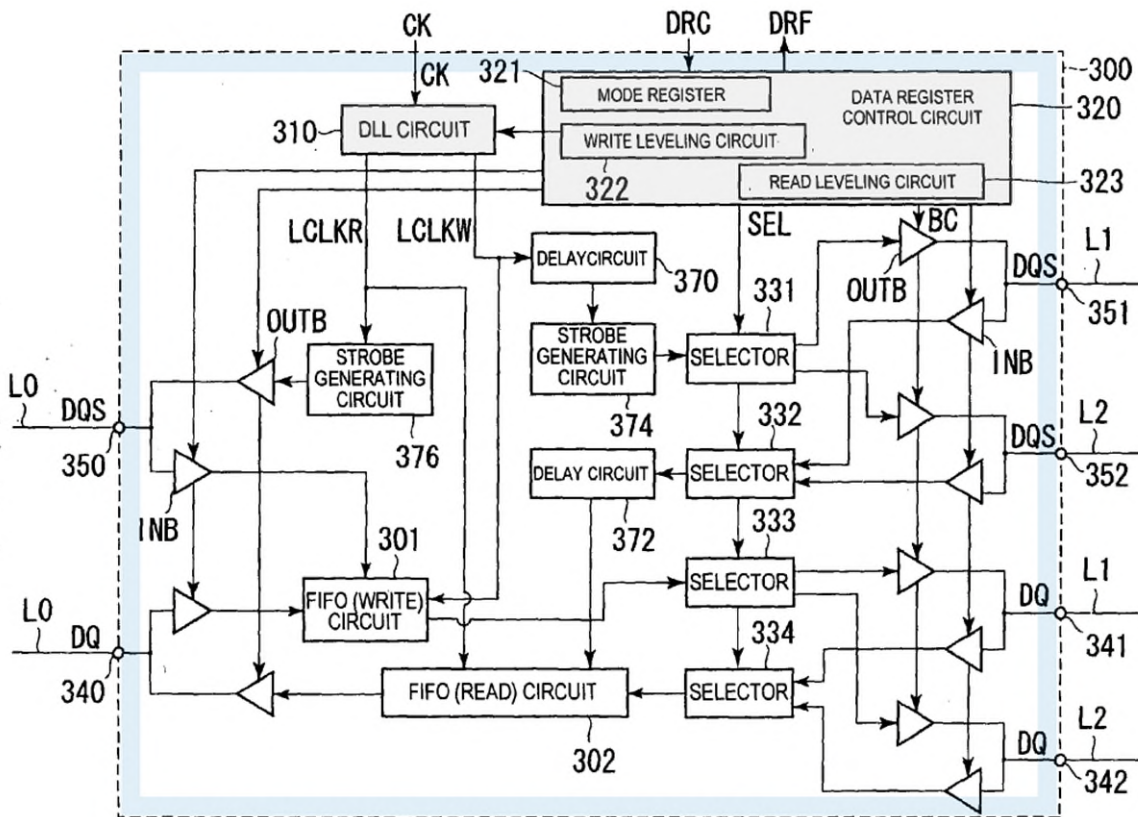


FIG.5

EX1003, ¶84.

B. Butt (EX1029)

US2007/0008791 (“Butt”)(EX1029), published in 2007, is prior art under §102(b). Butt was not cited or discussed during prosecution.

EX1002;EX1003,¶85. Butt discloses the details for sampling a data signal DQ at the optimum time based on a delayed read strobe signal DQS. EX1029, FIGS.2&5;EX1003,¶¶86-89.

C. Tokuhiro (EX1006)

US8,020,022 to Tokuhiro (“Tokuhiro”)(EX1006), issued 9/13/11, is prior art under §102(a)&(e). Tokuhiro was not cited or discussed during prosecution of the ’506 Patent. EX1002;EX1003,¶90.

Tokuhiro recognizes the problems of fly-by delays, e.g., in DDR3 memory systems, particularly where the delay is larger than one clock cycle, EX1003,¶¶91-93;EX1006,1:63-2:9,2:10-12,2:54-59,3:1-12, and, as a solution, proposes determining a first delay time utilizing the *write* leveling function, and using this delay time not just for write operations but also to delay the transmission of data during *read* operations. EX1003,¶94;EX1006,3:16-26,FIG.11.

D. Ellsberry (EX1007)

US2006/0277355 to Ellsberry (“Ellsberry”)(EX1007), published in 2006, is prior art under §102(b). Ellsberry was cited among hundreds of references but not discussed during prosecution of the ’506 Patent. EX1002,116;EX1003,¶95.

Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi and additionally expressly describes modules with 8-bit wide data buffers (blue) and with either 8-bit wide memory devices (EX1007,Figs.2,5,13(below left, green)) or pairs of 4-bit wide memory devices (EX1007,Figs.2,6,11(below right, green)) as confirmed by the Board in a final decision binding against Patent Owner.

EX1003,¶96;EX1007,¶[0056],Figs.2,5-6,11,13;EX1015,pp.57,60,66,68,77,81.

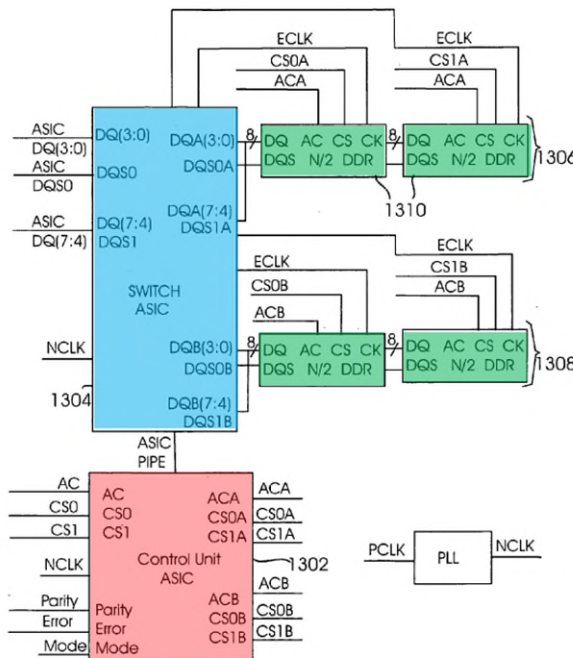


Fig. 13

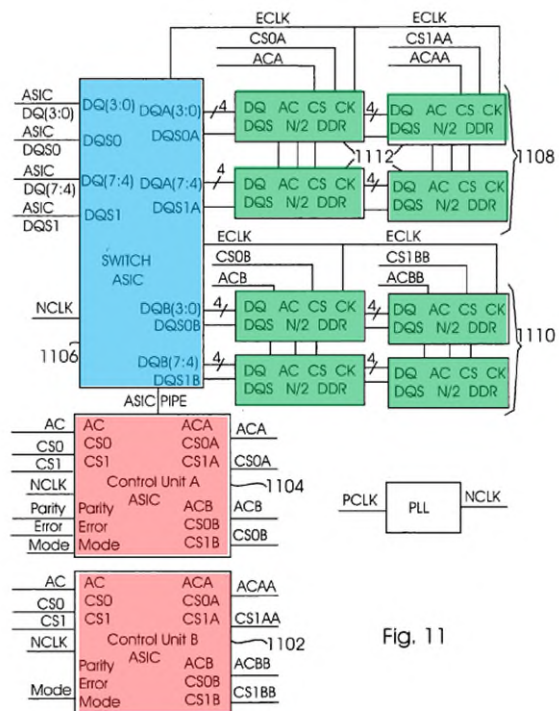


Fig. 11

E. Kim (EX1008)

US6,184,701 to Kim ("Kim") (EX1008), issued in 2001, is prior art under §102(b). Kim was not cited or discussed during prosecution of the '506 Patent. EX1002;EX1003,¶97.

Kim recognizes the problem of signals in a metastable state, which “may result in device failure,” EX1008,1:21-31, and discloses “a metastability detection/prevention circuit 20” to be incorporated with any “main active circuit 10” in need thereof to solve that problem, *id.*,2:23-24,2:30-31,2:33-37; EX1003,¶¶98.

VI. PRECISE REASONS FOR RELIEF REQUESTED

The claims of the ’506 Patent are invalid under both Patent Owner’s apparent interpretation for the claims, *infra*, §§VI.A-C, pp.20-93, and under a narrower interpretation consistent with the specification, *infra*, §VI.D-E, pp.93-127; EX1003, ¶¶99-100.

A. Ground 1: Claims 1-2,4,6-7,11,13-15,17-18 are Obvious Over Hiraishi and Butt

In related litigation, Patent Owner has suggested that claim 1 of the of the ’506 Patent is satisfied by read training between the memory chips and the data buffers, followed by a read command. *See*, EX1038, ¶¶46,48; EX1039, pp.26,28-29,32-33. That interpretation is broader than the teachings of the ’506 Patent, which discloses the use of two different operations, where the “*previous operation*” is a memory operation (*e.g.*, write) that transfers data in a different direction than the later read operation. *See supra*, §IV.C.1, pp.3-7; EX1003, ¶¶43-44, 99-100. In any event, under this interpretation, the claims of the ’506 Patent are

a) *1[pre]*

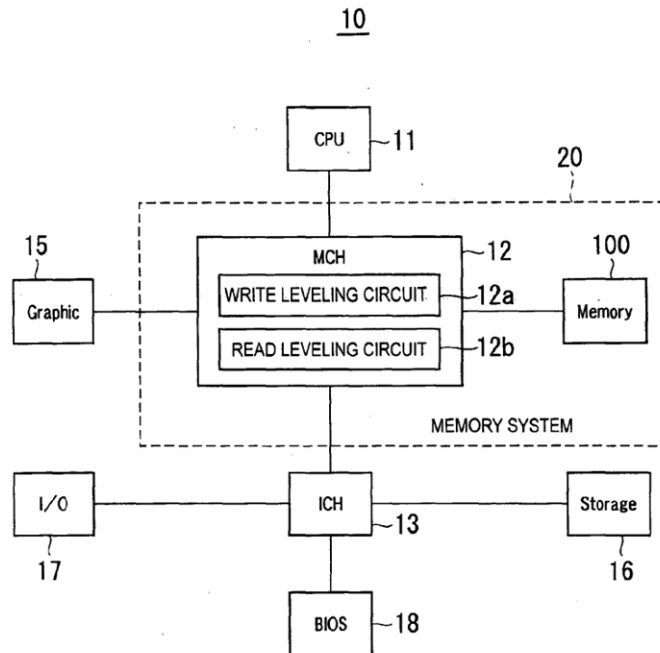


FIG.2

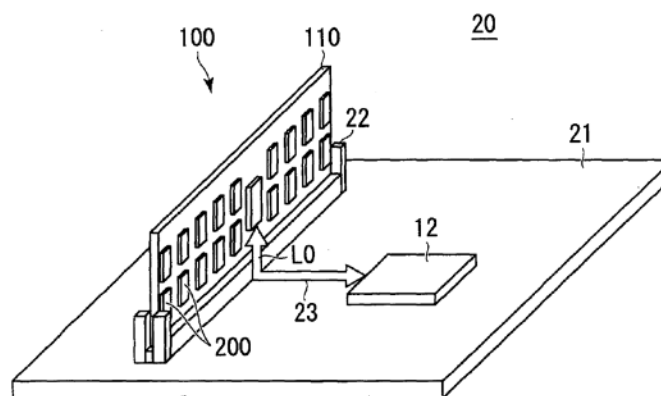


FIG.3

As shown above, Hiraishi's memory module 100 connects to a memory control hub 12 by a memory bus 23. Bus 23 includes a set of control/address signal lines coupling, through connectors 130 (purple, above and below), to

command/address/control line L3, and a plurality of sets of data/strobe signal lines, each set coupling, through connectors 120 (orange, above and below), to data line L0. EX1003,¶¶102-103;EX1005,¶¶[0047],[0049],[0060],[0069][0102-03],[0107],FIGS.1&7.

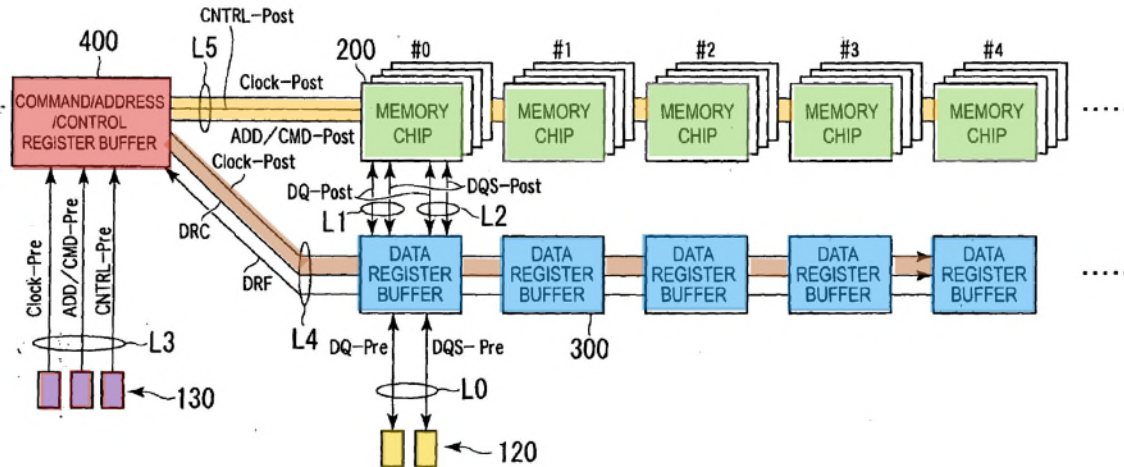
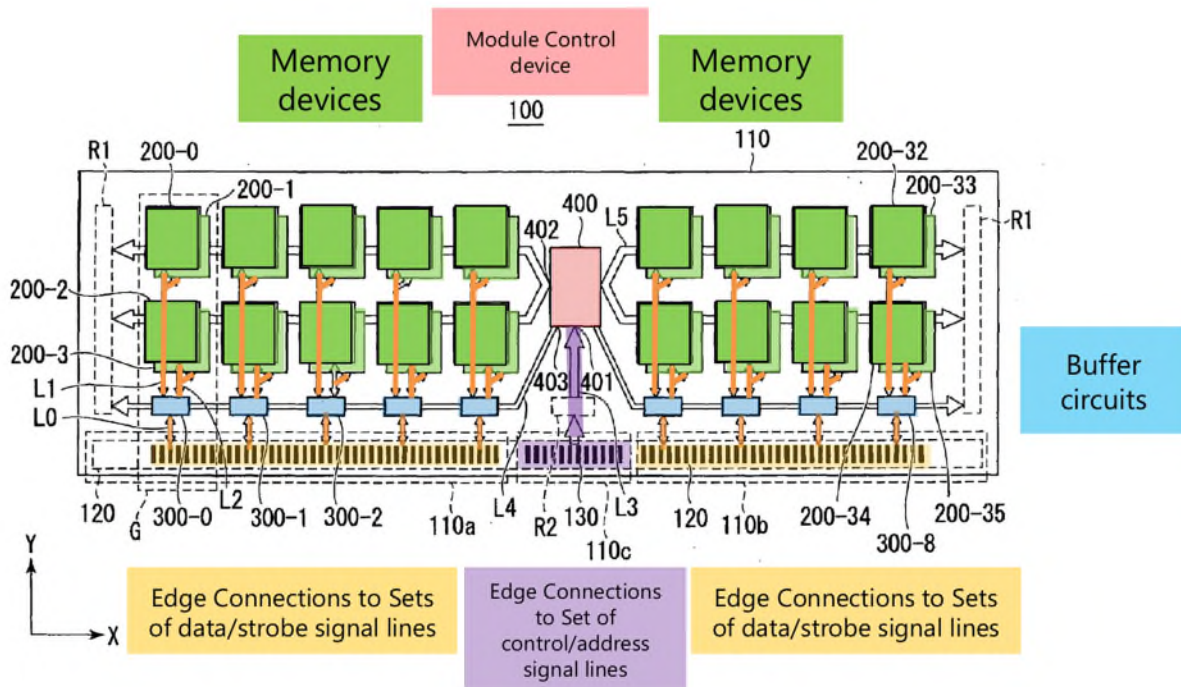


FIG.7

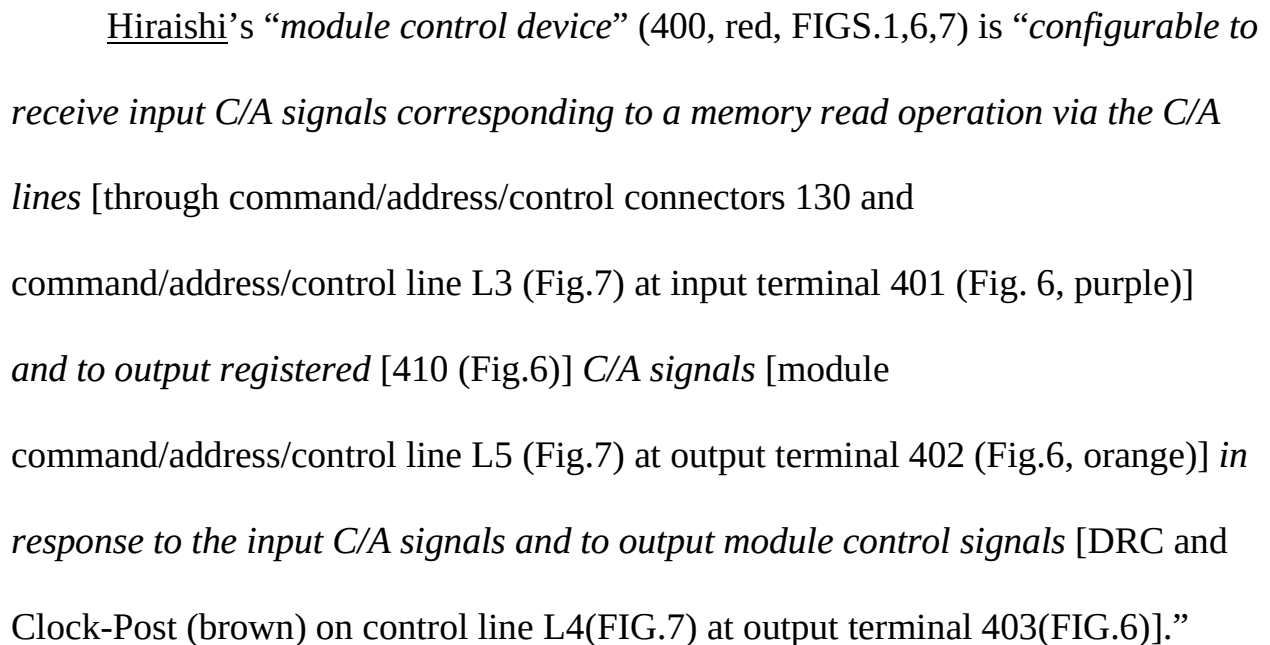
b) 1[a]: Module Board

Hiraishi discloses “a module board [module substrate 110] having edge connections [including command/address/control connectors 130(purple) and data connectors 120(orange) “for making an electrical connection with a memory controller via a memory slot”] to be coupled to respective signal lines in the memory bus [line 23, above, Fig.3].” EX1003,¶¶104-107;EX1005,¶¶[0045],[0047-49],Fig.1.



c) 1[b]: Module Control Device

Hiraishi discloses “a module control device [command/address/control register buffer 400, red] on the module board [110]”:



EX1003, [[110-112]; EX1005, [[0018-19],[0047],[0060],[0097],[0099],Figs.1,6,7.

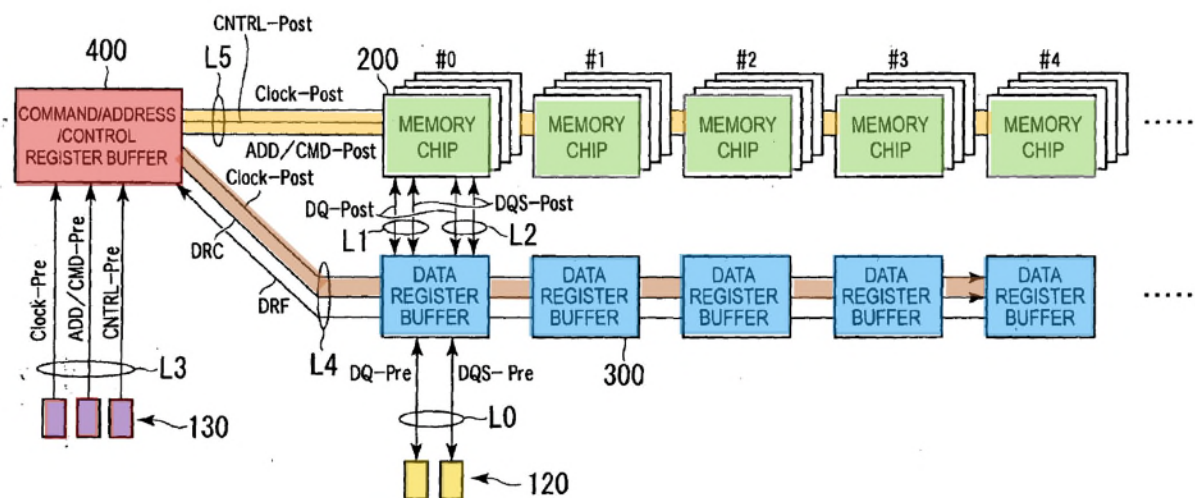


FIG.7

EX1003, $\parallel 110$; EX1005, $\parallel [0019]$, FIG. 7.

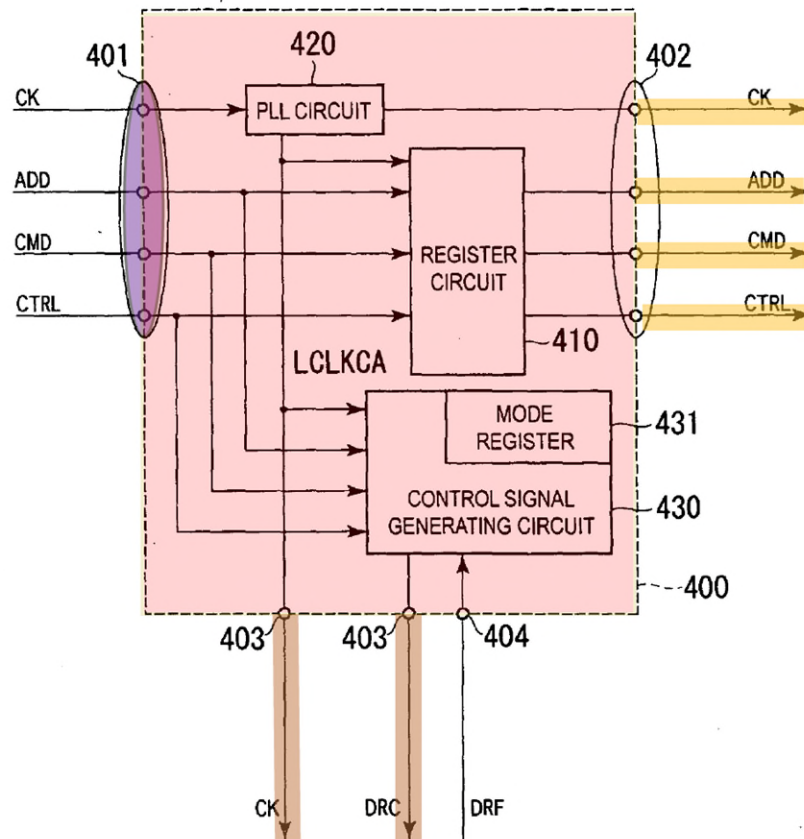


FIG.6

EX1003,¶110;EX1005,¶[0018],FIG.6.

Hiraishi discloses that one memory operation can be a read operation (red box below). EX1005,¶¶[0122-31];EX1003,¶113.

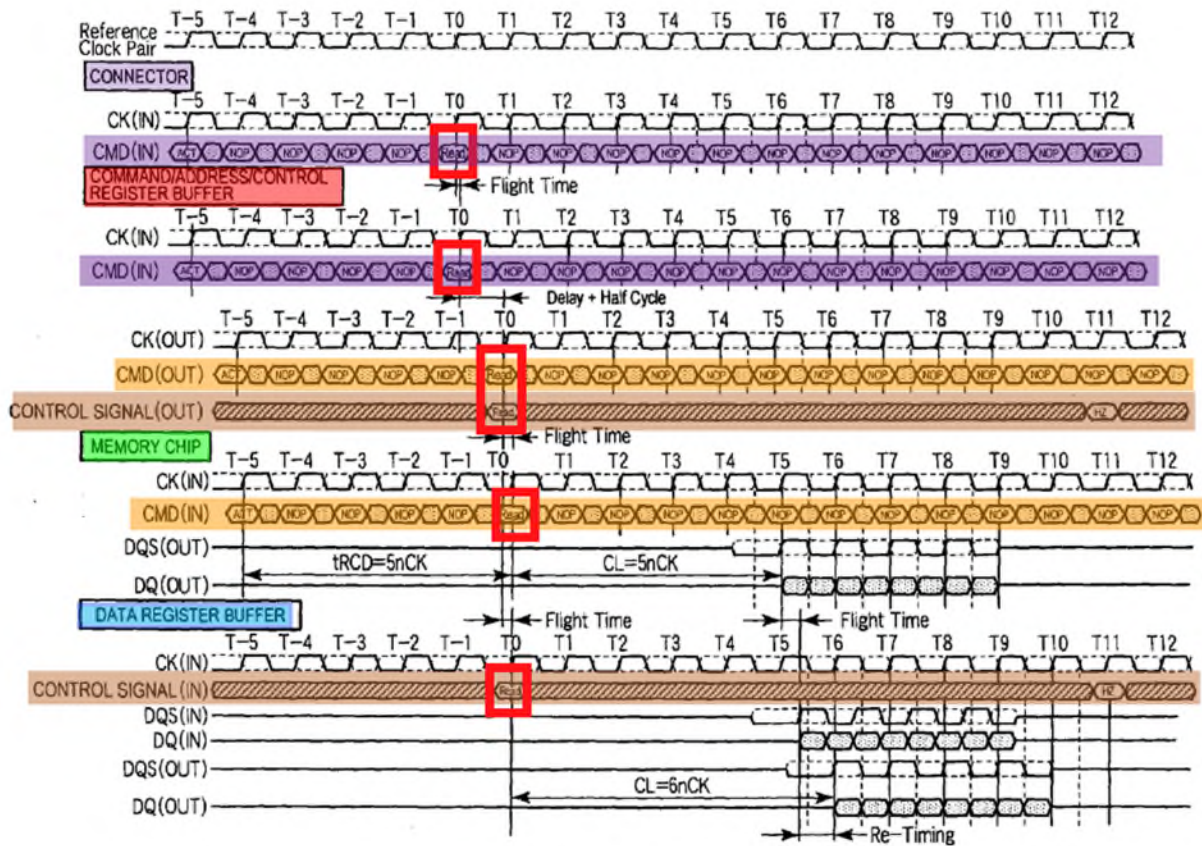
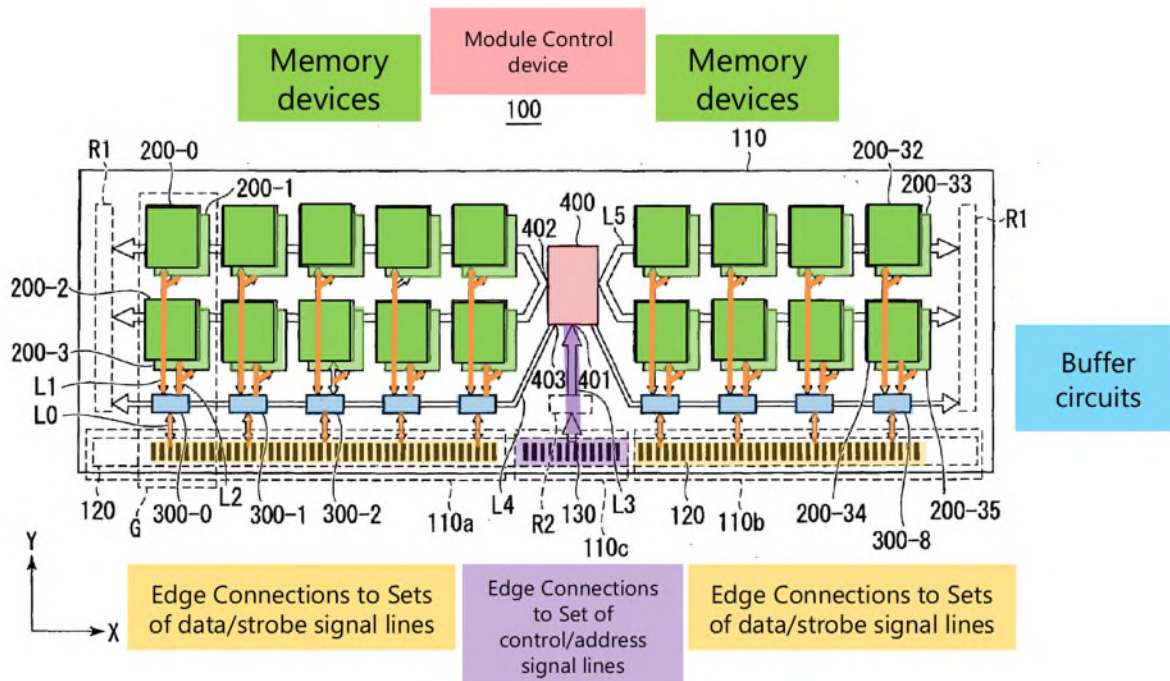


FIG.11

EX1003,¶113;EX1005,FIG.11.

d) 1[c1]: Memory Devices

Hiraishi discloses “memory devices [200-0 to 200-35 (green)] arranged in multiple ranks [e.g., 200-0, 200-1, 200-2, and 200-3 in four different ranks] on the module board [110] and coupled to the module control device via module C/A signal line [line L5] that conduct the registered C/A signals [such as ADD/CMD-Post on L5 (Fig.7).” EX1003,¶¶114-116;EX1005,¶¶[0045],[0050-52],[0107],Figs.1,7.



EX1003,¶114;EX1005,FIG.1(annotated).

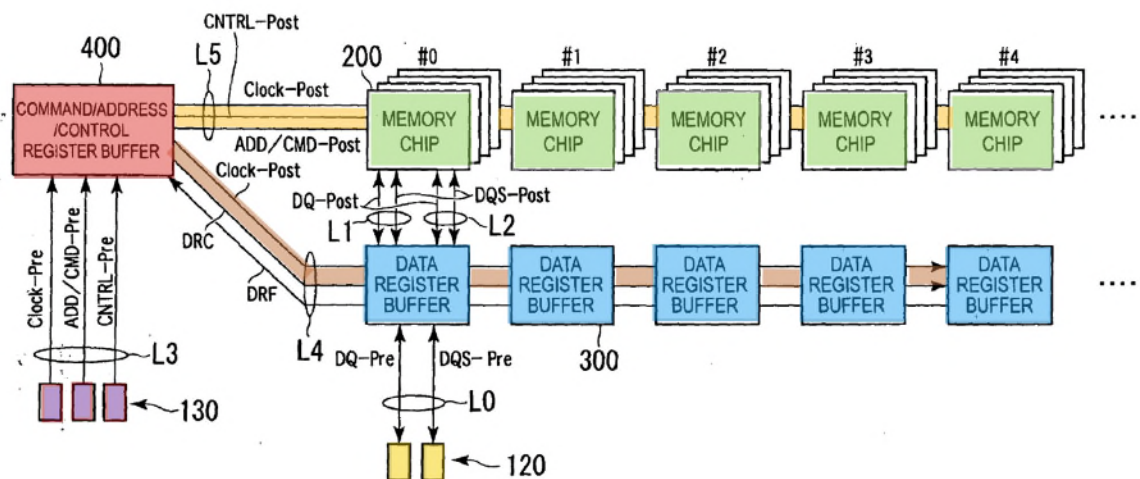


FIG.7

EX1003,¶114;EX1005,FIG.7(annotated).

e) 1[c2]: Memory Read Operation

Hiraishi discloses “*wherein the registered C/A signals [on line L5 (Fig.7)] cause a selected rank of the multiple ranks [e.g., one of the 4 ranks (EX1005,¶[0051]), say rank 0] to perform the memory read operation by outputting read data and read strobes associated with the memory read operation [e.g., using input/output circuits 213 and 214 (Id.,¶¶[0079-80],Fig.4)], and wherein a first memory device [e.g., memory device 200-0 (Fig.1)] in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe [on DQ/DQS-Post lines L1 (Figs.1,7)].*” EX1003,¶¶117-121; EX1005,¶¶[0051-53],[0056],[0076],[0079-80],[0054],[0103],[0120-29],Figs.1,4,7; *see,also,id.*,[0163],[0170];EX1018,pp.4.20.4-6,-10 to -16;EX1020,pp.13,33,34n.1, 56-67;EX1021,pp.319,413.

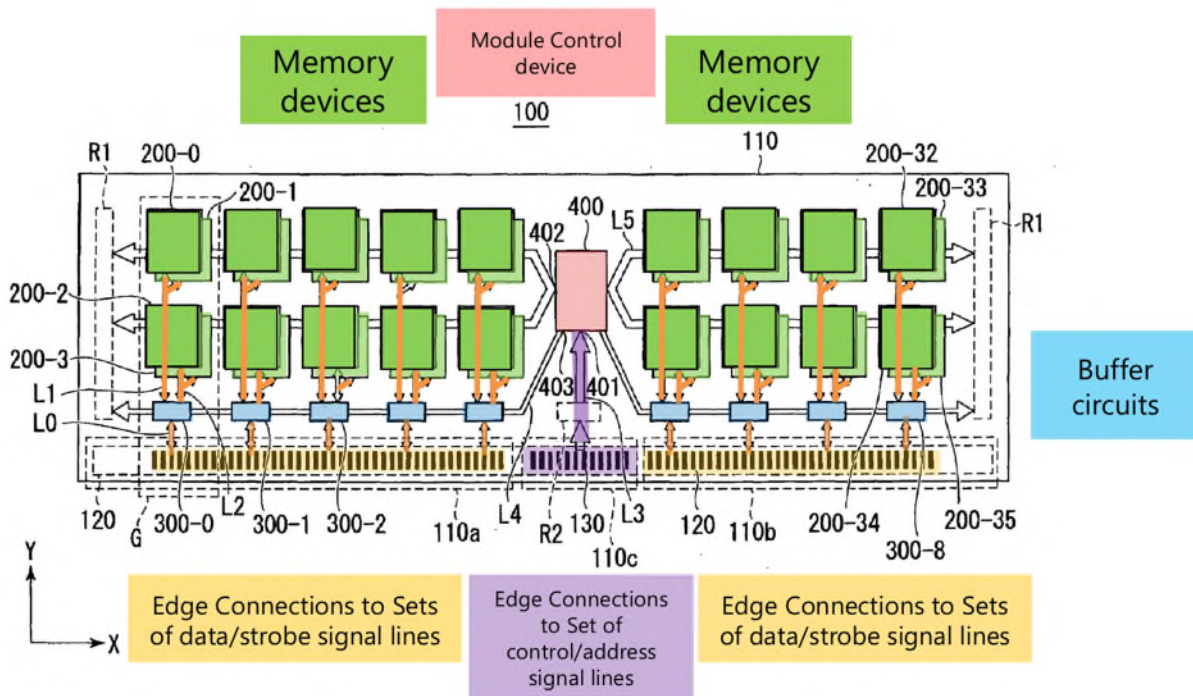
Hiraishi discloses a plurality of sets of memory devices (e.g., a set including memory devices 200-0 to 200-3, called a group, each memory device in a different rank) corresponding to respective sets of the plurality of sets of data/strobe signal lines (e.g., L0), one set of memory devices (200-0 to 200-3) being connected to a data register buffer (300-0). EX1003,¶119;EX1005,¶¶[0051-53],[0056],[0103]. Consistent with the JEDEC standard, commands (such as read) include a chip-select signal, such that all memory devices in a selected rank perform the command together (e.g., each memory device in the rank outputs read data along

with a strobe). EX1003,¶¶120-121;EX1005,¶¶[0051-52],[0076];

EX1021,pp.319,413;EX1020,pp.13,33,34n.1;EX1018,pp.4.20.4-6,-10 to -16.

f) 1[d]: Data Buffers

Hiraishi discloses “*data buffers [300-0 to 300-8 (blue)] on the module board between the edge connections and the memory devices [e.g., 300-0 is positioned between the set of memory devices 200-0 to 200-3 (green) and the connectors 120 (yellow) connecting to the data line L0(Fig.1)] wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks [e.g., data buffer 300-0 is coupled to at least memory devices 200-0 to 200-3 in four different ranks] and is configurable to receive the module control signals from the module control device [e.g., data buffer 300-0 receives module command/address/control line L4 (Figs.1,7) from command/address/control register buffer 400 (including DRC, brown (Figs.1,7))]*. EX1003,¶¶122-126.



EX1003,¶122;EX1005,FIG.1.

Figure 1 above shows nine data buffers (blue), each corresponding to four memory devices (green), such that each data buffer buffers 8 bits of read or write data that is transferred via line L0 to either data line L1 or L2 and *vice versa*.

EX1003,¶123;EX1005,¶¶[0045],[0052],[0055-56],[0085].

Figure 5 below also confirms that the data buffer 300 (blue) is positioned between respective sets of data(DQ)/strobe(DQS) signal lines (L0 on one side and L1/L2 on the other). EX1003,¶¶124-125;EX1005,¶¶[0017],[0084],[0103],FIG.5; *id.*,FIG.7(same).

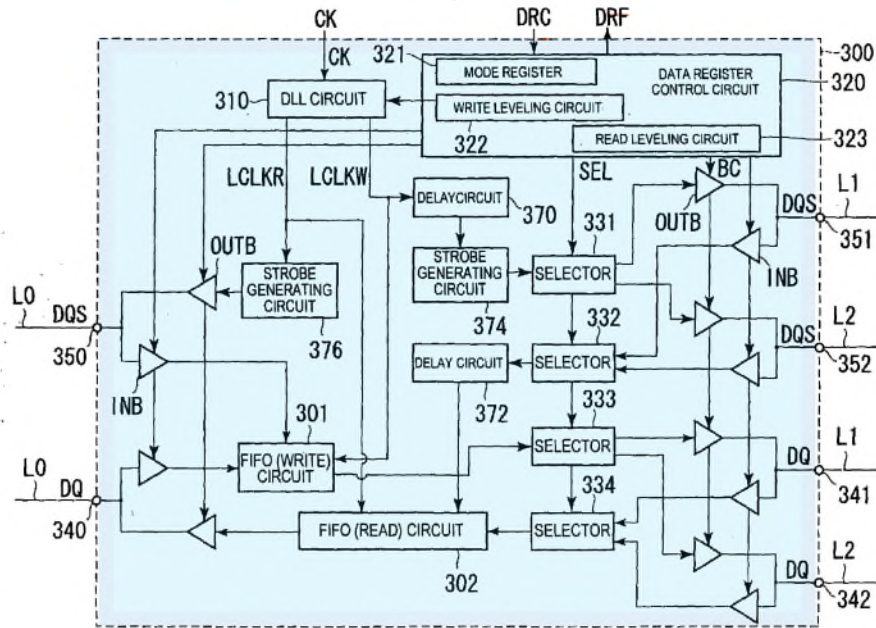


FIG. 5

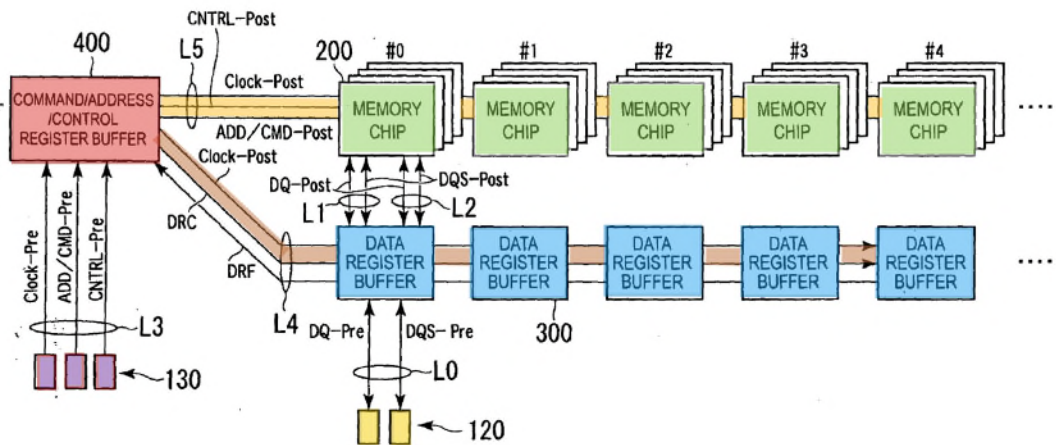


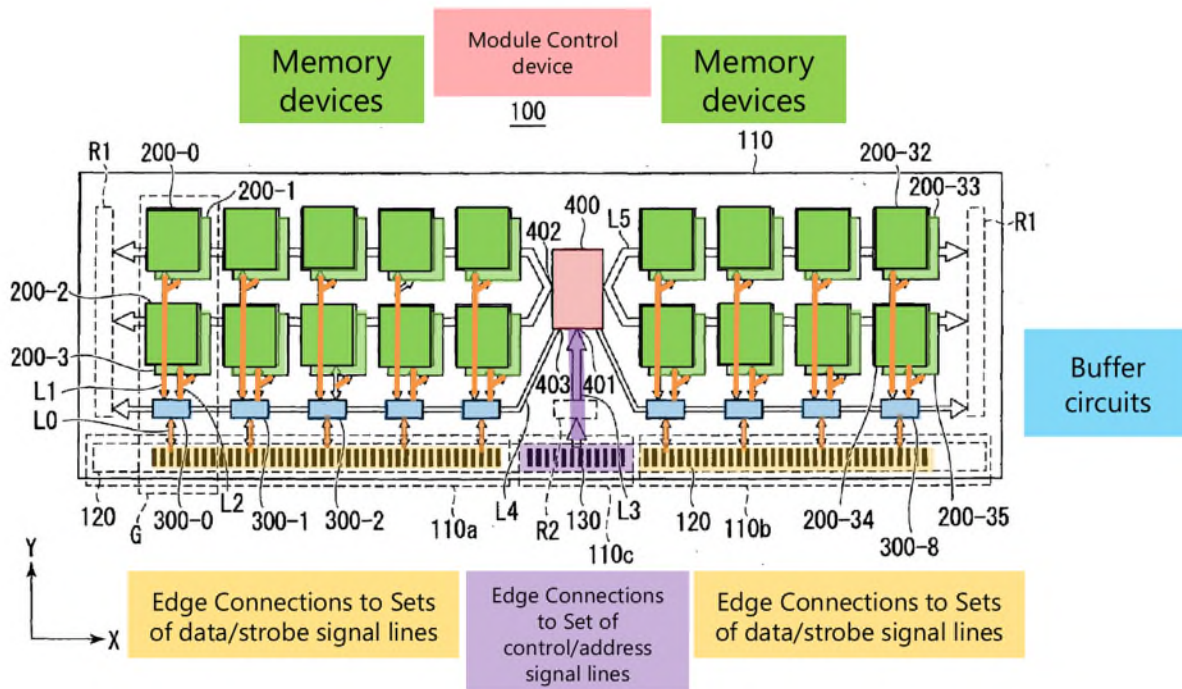
FIG. 7

Figure 7 above shows that the data buffers (blue) receive module control signals on L4 (brown, including DRC) from the module control device (400, red).

EX1003,¶¶122,126;EX1005,¶[0099]&FIG.7.

g) 1[e]: Module Control Signals

As shown below, and discussed in 1[d] above, Hiraishi discloses that “*a first data buffer of the data buffers [e.g., 300-0] is coupled to the first memory device [e.g., 200-0], and is configurable to, in response to one or more of the module control signals [signals on line L4 from buffer 400 (including DRC, brown, Figs.1,7)]....*” *Supra*,§VI.A.1.f),pp.31-33;EX1003,¶¶127-128;EX1005,¶¶[0045],[0055-56],[0084],[0099],[0103],Figs.1,7.



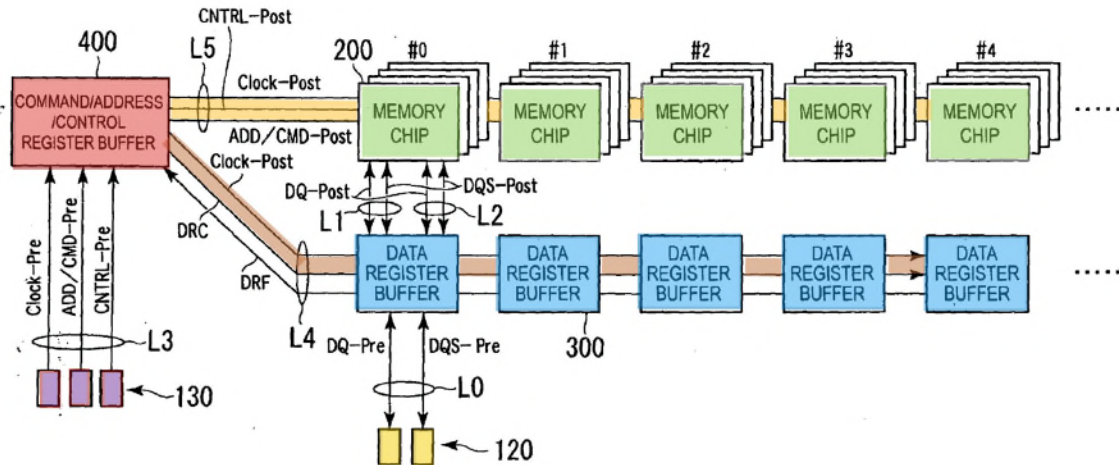


FIG. 7

h) 1[f]: Delay First Read Strobe

Hiraishi discloses that data register buffers (300), including delay circuit 372, can “*delay the first read strobe [orange dashed line, e.g., on 351] by a first predetermined amount [e.g., “about 90 degrees” (EX1005, ¶[0091])] to generate a first delayed read strobe [e.g., the DQS signal supplied to FIFO (Read) circuit 302].*” EX1003, ¶¶99-100, 129-130; EX1005, ¶[0091], FIG. 5(below).

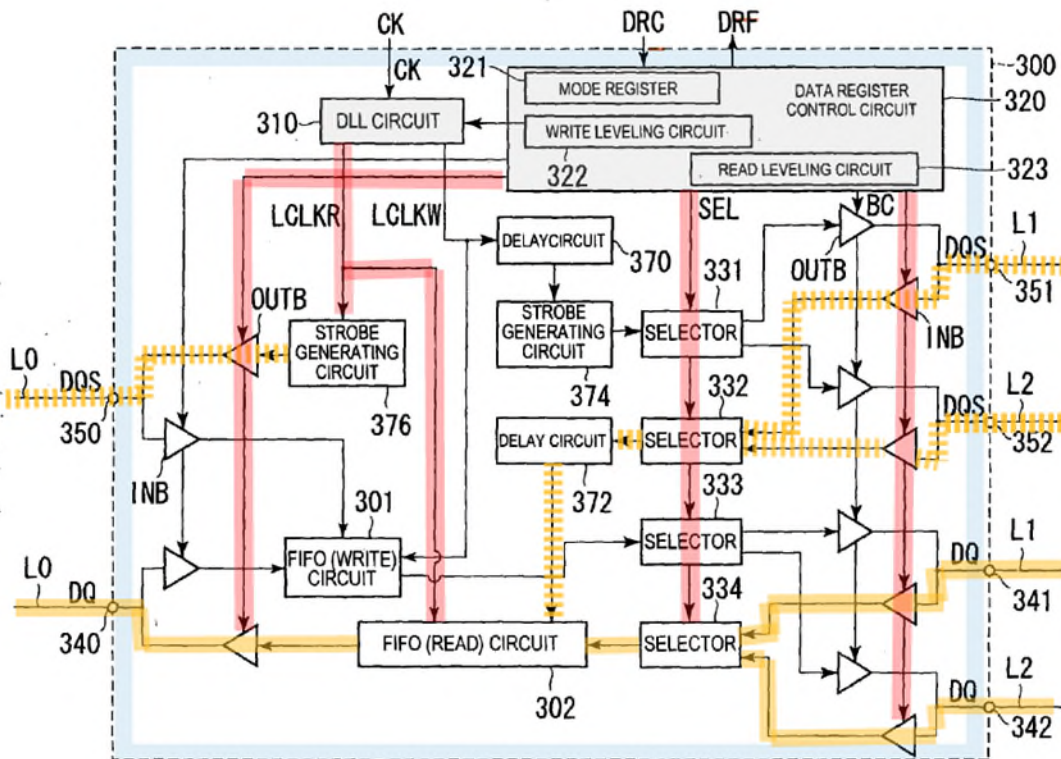


FIG. 5

i) 1[g]: Sample First Section of Read Data

Hiraishi alone or with Butt teaches that FIFO (Read) circuit 302 in data buffer 300 would “sample the first section of the read data [DQ, orange line, e.g., on 341] using the first delayed read strobe [DQS, orange dashed line, from delay circuit 372].” EX1003, ¶¶131-133; EX1005, ¶[0091], Fig. 5; EX1029, ¶¶[0018-19], [0035].

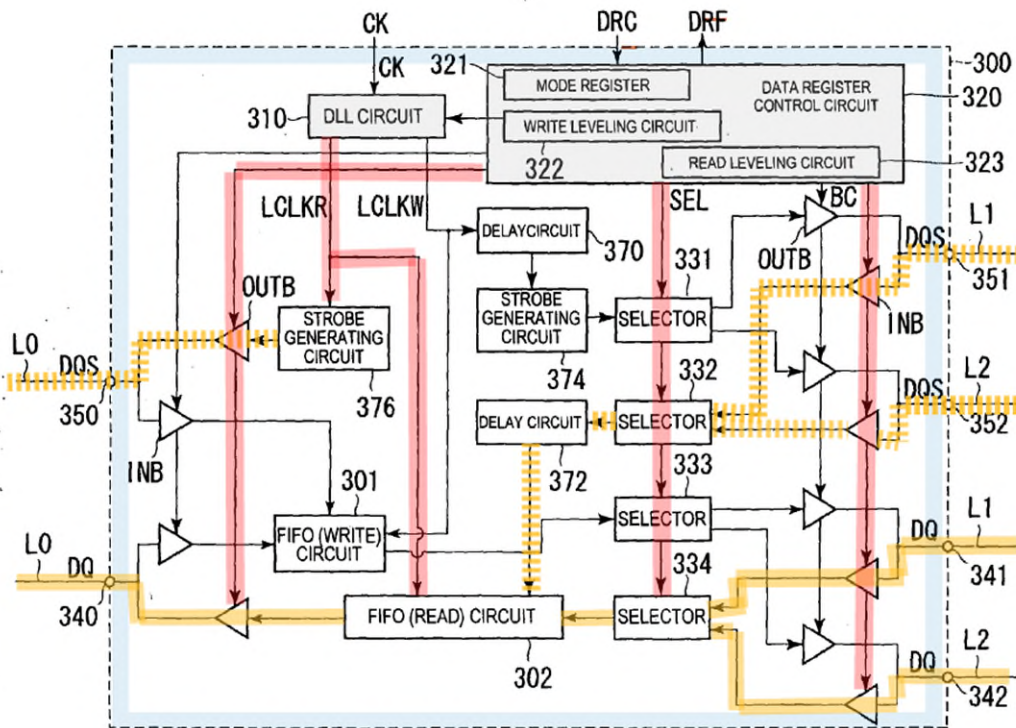


FIG.5

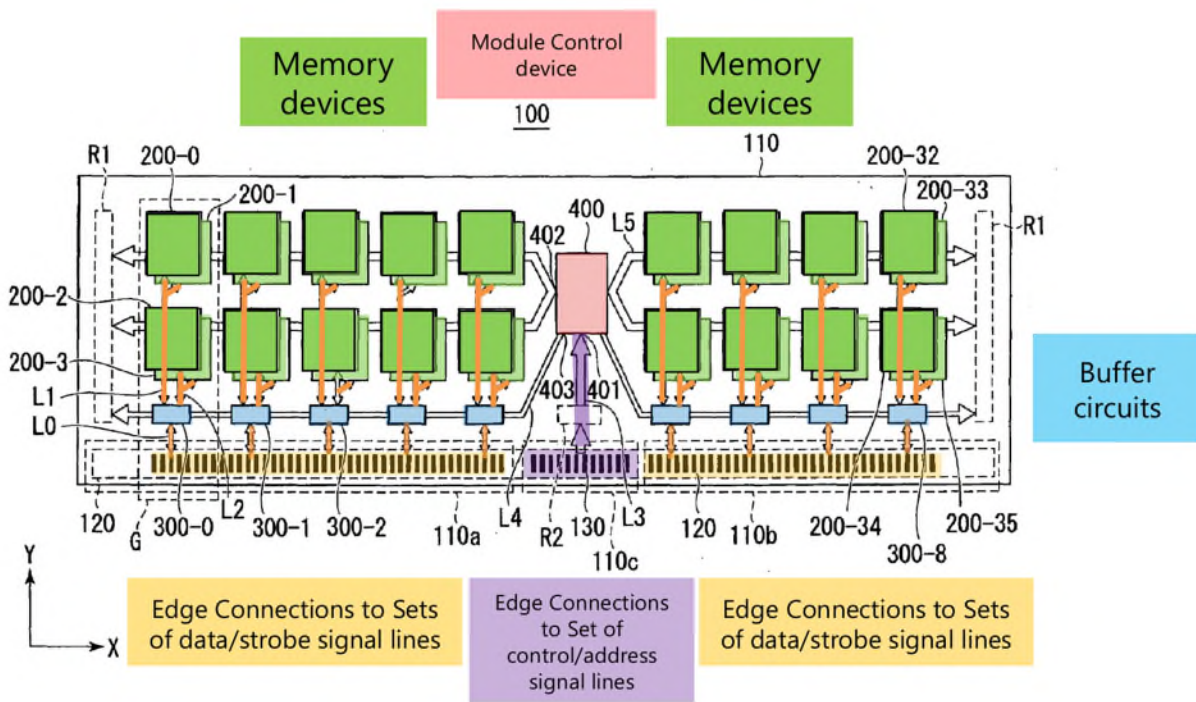
A POSITA would have understood that, when the data signal is latched in the FIFO, it necessarily is sampled (registered) and, because the delayed DQS signal acts “as an input trigger signal” to latch the data in the FIFO (Read) circuit 302, this is necessarily done in accordance with the delayed strobe signal received from delay circuit 372. EX1003,¶132;EX1005,[0091]; see also EX1001,13:27-29,17:15-18 (discussing sampling).

To the extent one might argue Hiraishi alone does not disclose this limitation, it is obvious in view of Butt, which discloses a method for calibrating a delayed read strobe DQS, EX1029,¶[0035], such that “data is sampled using the delayed read data strobe signals DQS,” *id.*,[0018]. The operation Butt describes as

“sampling” is equivalent to Hiraishi’s use of the DQS signal to trigger the FIFO (Read) circuit 302. EX1029,¶[0019]. Thus, it would have been obvious to configure Hiraishi to “sample” the read data using the delayed read strobe signal as disclosed in Butt. EX1003,¶¶133,144-151. This combination, and the motivation to combine, is discussed more in 1[i], *infra*,pp.39-48.

j) 1[h] Transmit First Section of Read Data

Hiraishi discloses that the first data buffer (300-0) can “transmit the first section of the read data [e.g., DQ on L0 via 340 (Figs.1,5)] to a first section of the data bus [e.g., from buffer circuit 300-0 (blue) to the connectors 120 (yellow) connecting to the data line L0 (Fig.1) connecting to a section of line 23 (Fig.3)].” EX1003,¶¶134-135;*supra*,§VI.A.1.e),pp.30-31.



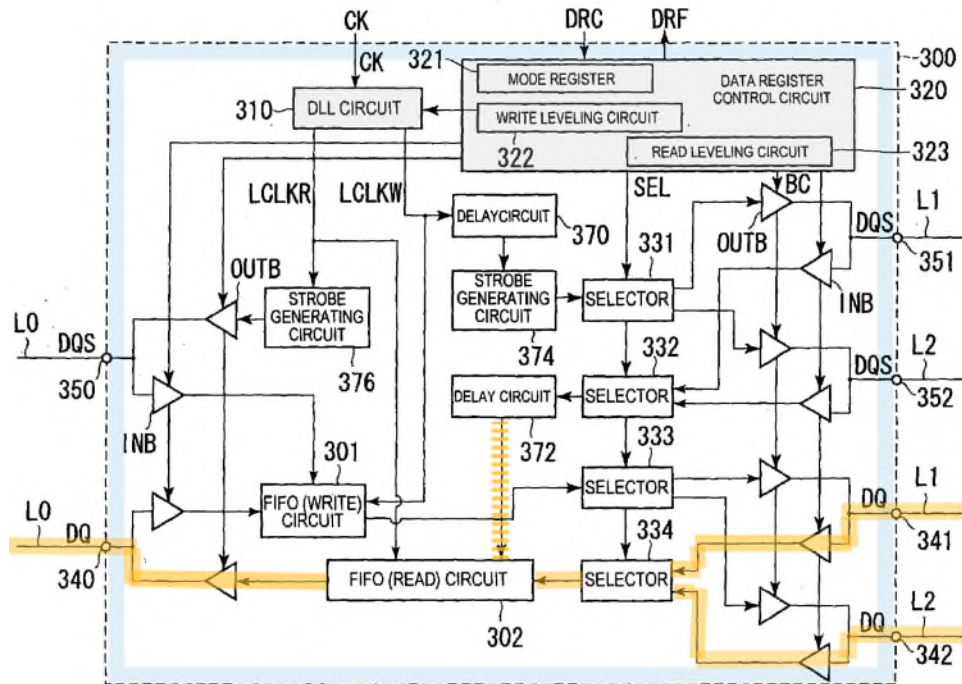
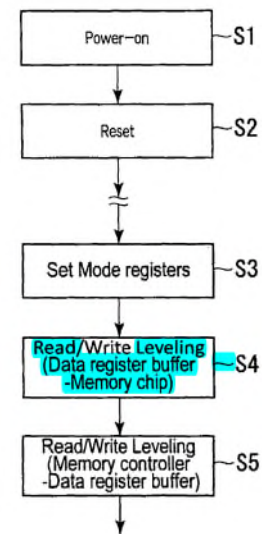
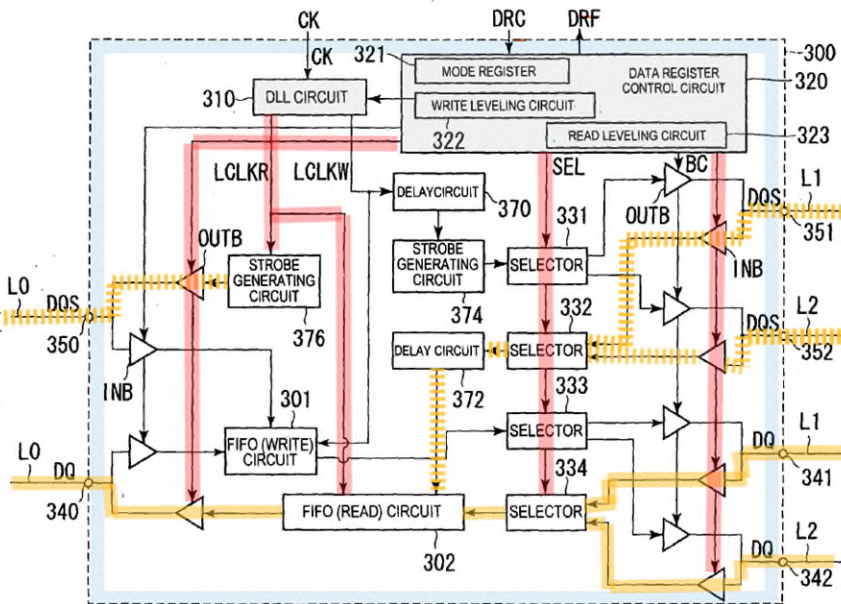


FIG. 5

k) 1[i]: First Predetermined Amount

Hiraishi alone or with Butt discloses “the first predetermined amount [e.g., applied by delay circuit 372 (Fig. 5)] is determined based at least on signals [e.g., dummy data or strobe signals] received by the first data buffer during one or more previous operations [e.g., the S4 read leveling operation (Fig. 13)].”

EX1003, ¶¶ 136-151.



EX1020,pp.31&n.2,48-54;EX1005,¶¶[0150],

[0160];EX1029,¶[0044];EX1003,¶¶138,141.

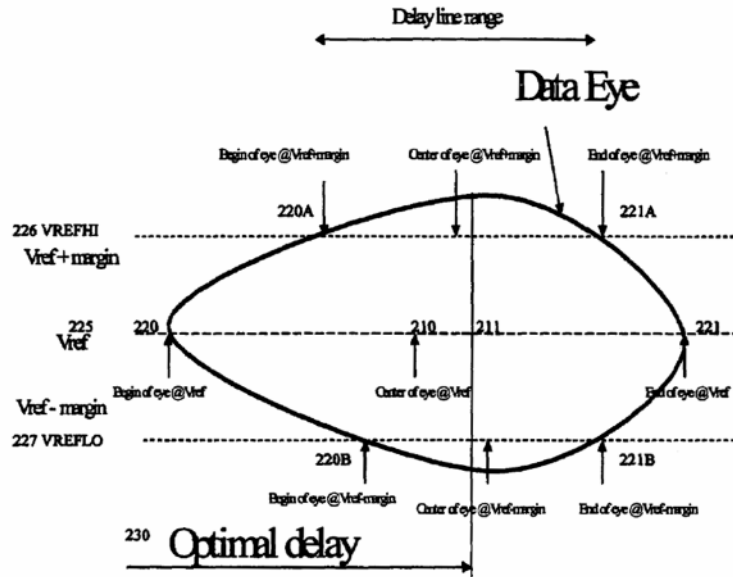


FIG. 2B: Data Eye for DDR

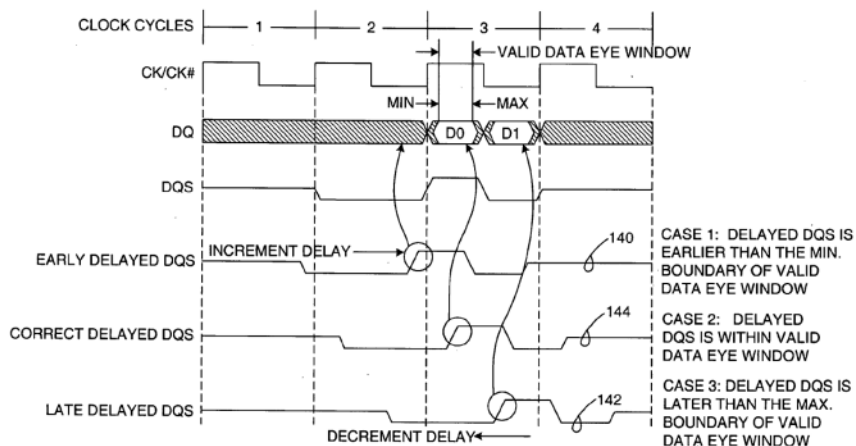


FIG. 4

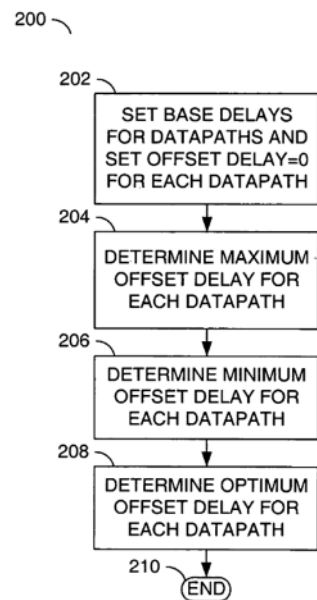


FIG. 5

Hiraishi discloses that this fine tuning of DQ/DQS is necessary both between the memory devices 200 and the data buffer 300 (step S-4), and between the data buffer 300 and the memory controller (step S-5).

EX1005, ¶¶[0090],[0104],[0140],Fig.13;EX1003, ¶¶137-140.

A POSITA would have understood Hiraishi's read leveling circuit 323 is capable of using the standard read leveling techniques of the time, e.g, in the JEDEC standard, particularly since Hiraishi expressly teaches the importance of DLL circuits (phase matching) for standard DDR3 memory devices.

EX1005, ¶¶[0090],[0140],[0148-50],[0160],[0163];EX1020,pp.31&n.2,48,51;

EX1003, ¶141.

Read leveling in Hiraishi includes performing a read operation, meaning data buffer 300 (blue) receives a DQS (strobe) signal, e.g., “FROM MEMORY CHIP 200-0 TO DATA REGISTER BUFFER 300-0,” as shown at the bottom of the timing diagram below. EX1005, ¶¶[0028],[0150],FIG.15; EX1003, ¶142.

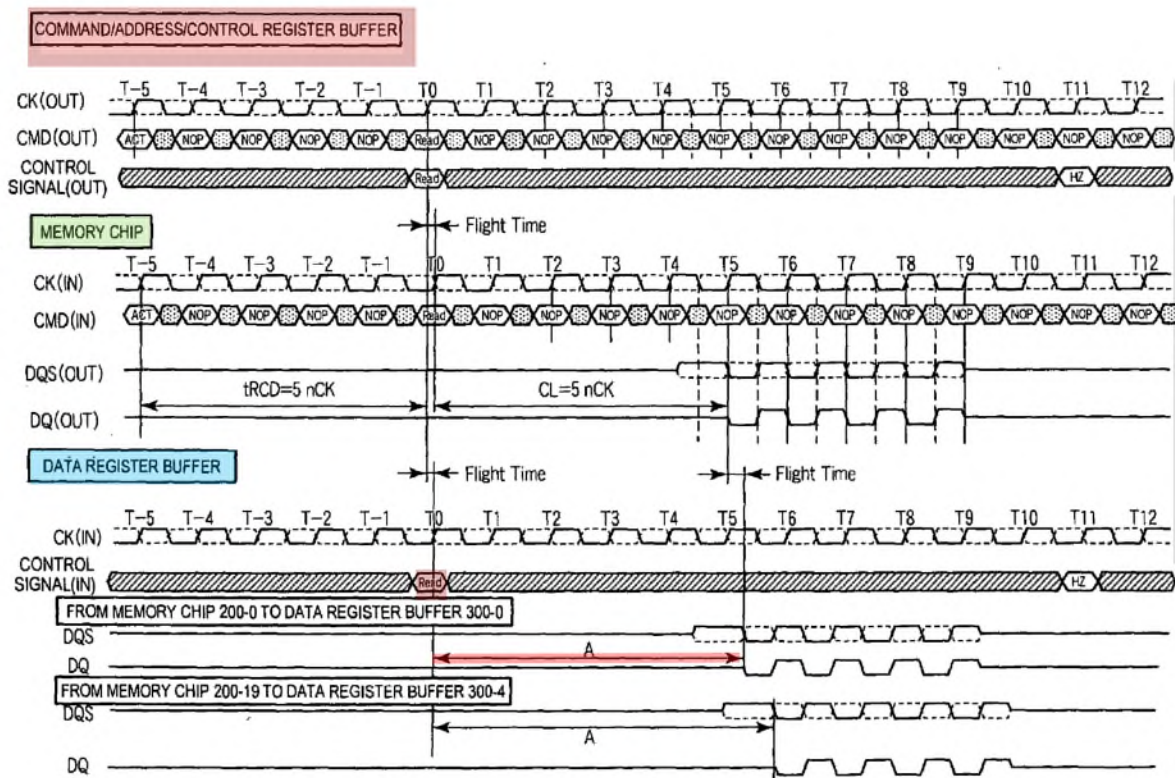


FIG. 15

Thus, the amount of delay applied to the strobe signal DQS by delay circuit 372 would be based at least on signals received by the data buffer 300 during S4 read leveling (e.g., the DQS from memory device 200, and the “dummy data” used in S4 read leveling). EX1003, ¶143.

To the extent one might argue Hiraishi alone does not disclose this limitation, it would also be obvious in view of Butt’s disclosure that “*wherein the first predetermined amount [e.g., the delay applied by datapaths 114 to the data strobe signal DQS] is determined based at least on signals [e.g., data strobes*

during read training] received by the first data buffer during one or more previous operations [e.g., read training process 200].” EX1003,¶144.

Butt (below) discloses a circuit 104 between a memory controller (left) and a DDR memory (right, green):

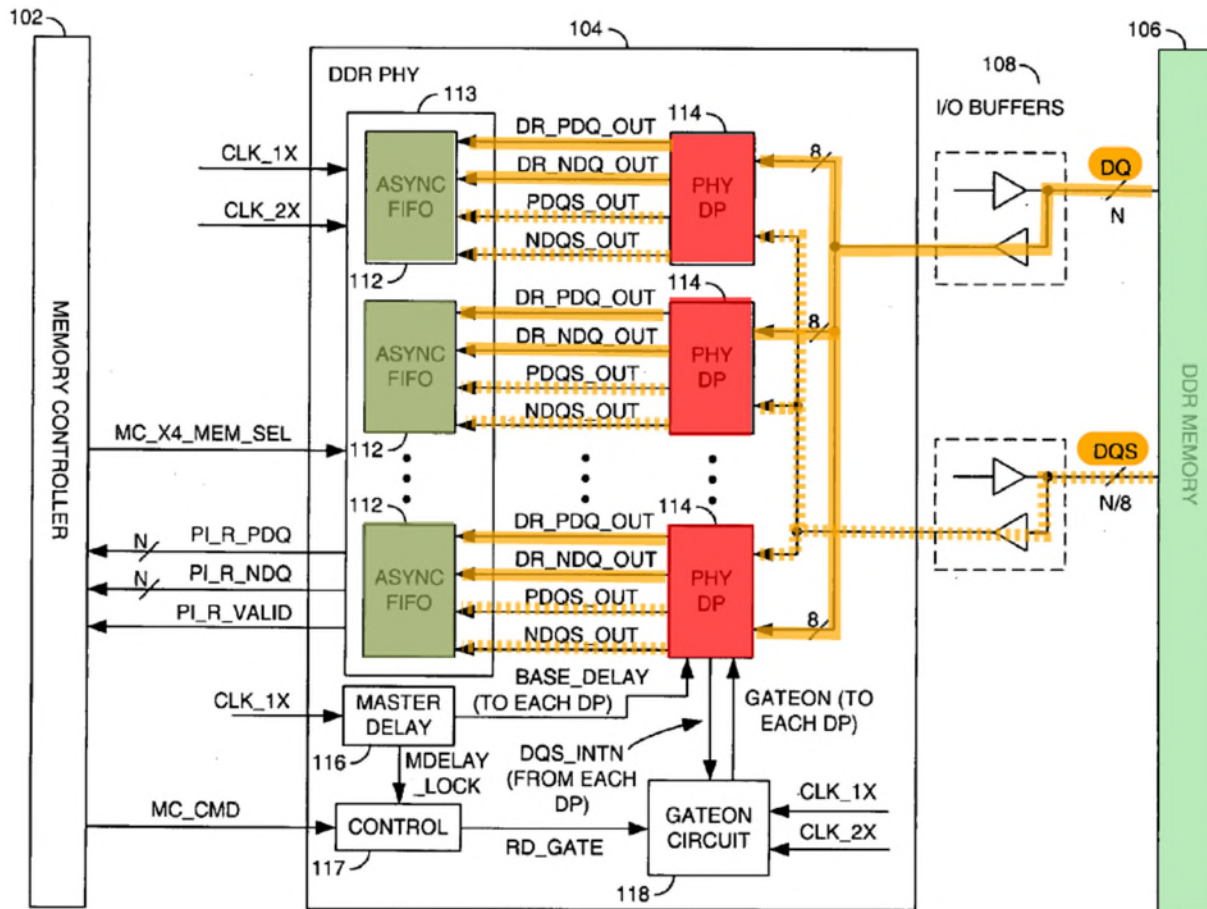


FIG. 2

EX1029,FIG.2. Circuit 104 includes physical datapaths 114 (red, also below in FIG.3A) that can delay the read strobe signal DQS (orange dashed) that is used to read data signal DQ (orange). EX1029,¶¶[0017-18],FIG.3A;EX1003,¶145. Butt

describes a method of “read training” that can “establish optimum DQS settings” by “adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal...” EX1029, ¶¶[0033],[0035], FIG. 3A(annotated below). Figure 5 (below) illustrates the overall process, with more details for specific steps shown in Figures 6-7. EX1003, ¶¶145-147.

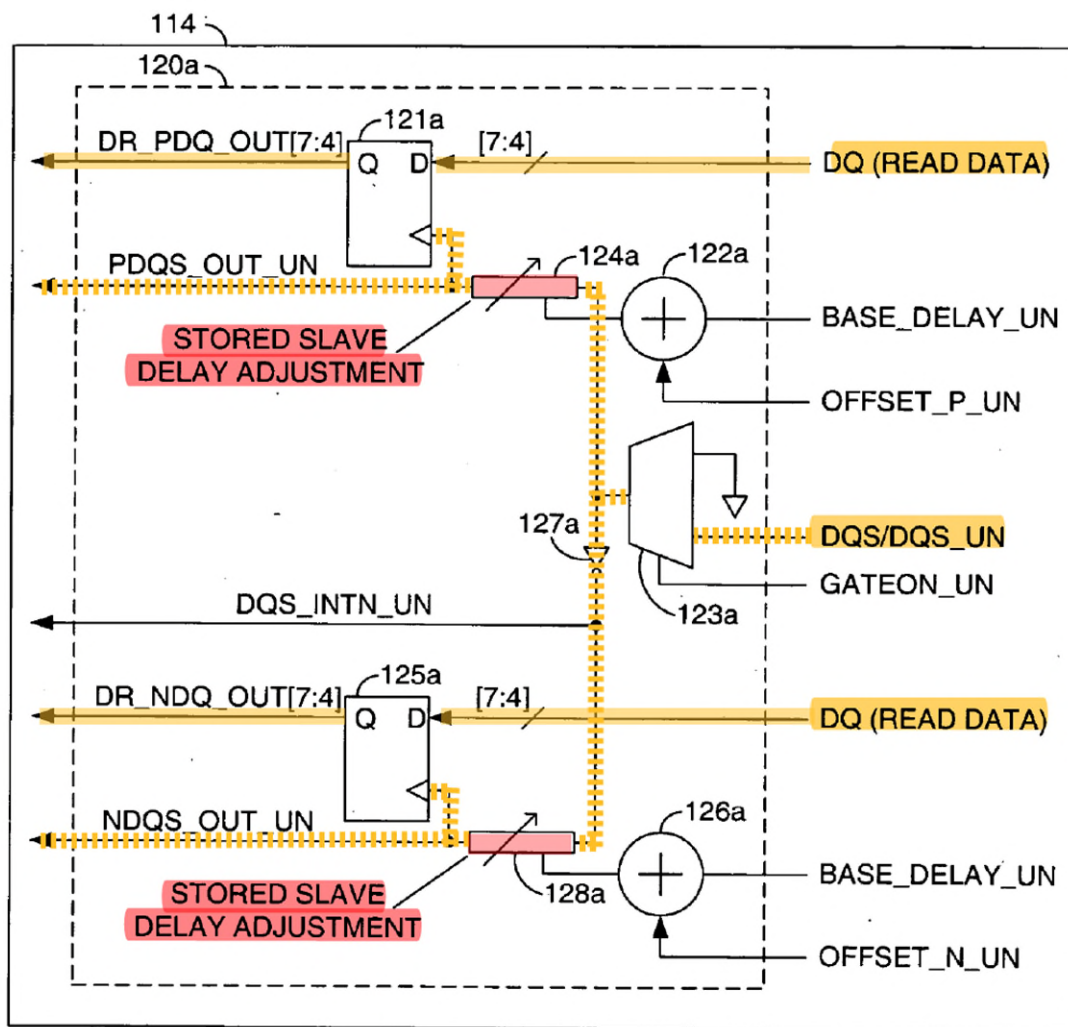


FIG. 3A

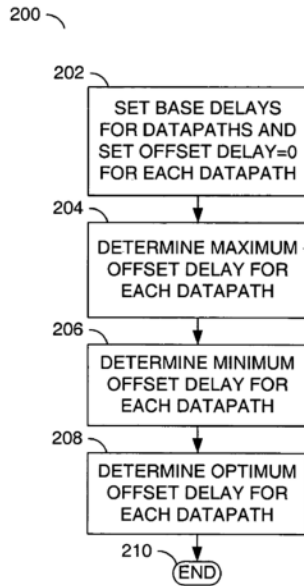


FIG. 5

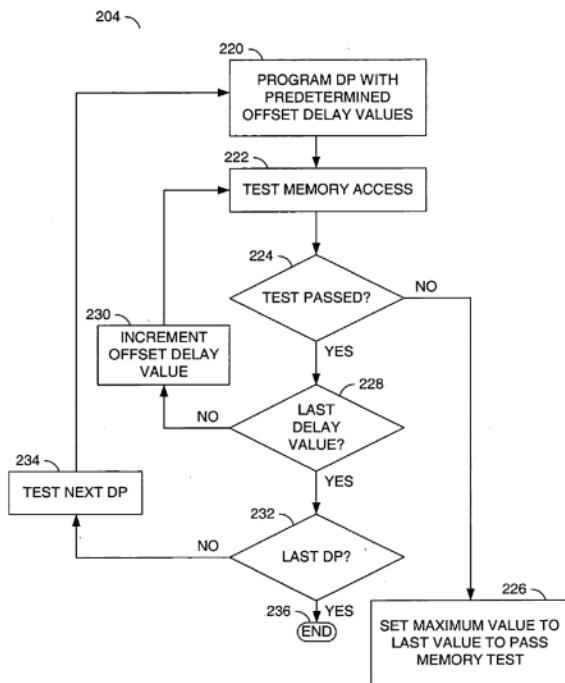


FIG. 6

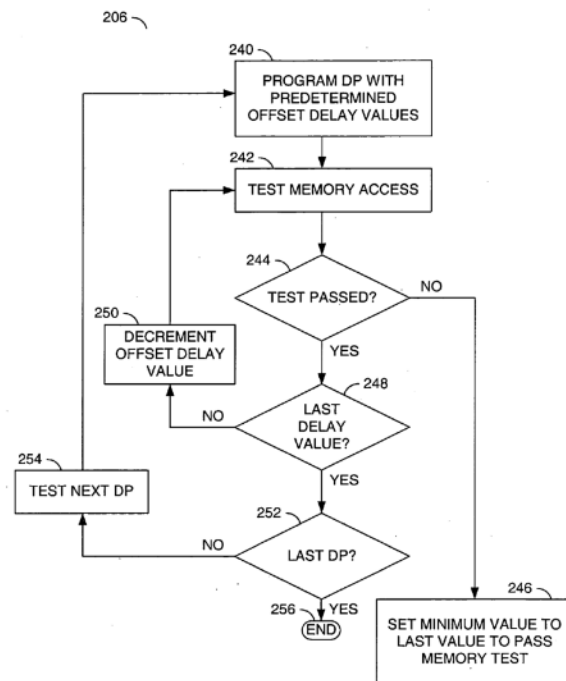


FIG. 7

EX1029, FIGS. 5-7. Each datapath in Butt iteratively tests different offsets from a base delay for valid memory access to determine a minimum and maximum acceptable offset. *Id.*, [0033], [0037], [0045], [0048-61]; EX1003, ¶147.

A POSITA would understand from Butt that these minimum and maximum offsets are used to determine an optimum offset, which is programmed into the datapath for use during later read operations. EX1029, ¶¶ [0046], [0022], [0054], [0061], Figs. 5-7; EX1003, ¶¶ 148, 150. A POSITA would therefore understand that datapaths 114 in Butt delay the data strobe signal DQS in an amount based on signals received during a previous operation—e.g., the dummy data and strobe signals received during read training in process 200 (Figs. 5-7 above). EX1003, ¶¶ 148, 150.

It would have been obvious to apply the teachings of Butt to Hiraishi to set the delay for delay circuit 372 in Hiraishi's Figure 5, e.g., by read leveling circuit 323, based on signals received during a prior read leveling process.

EX1003, ¶¶ 149-150. Hiraishi explicitly calls for “read leveling,” e.g., EX1005, ¶¶ [0090], [0140], [0147], Fig. 5(323), Fig. 13(step S4), Fig. 15, and as explained above Butt teaches the details for performing read leveling. Butt provides the motivation: to “enable[] a reliable data read operation for high speed applications.” EX1029, ¶ [0036]. A POSITA would have had a reasonable expectation of success because the combination would be a simple application of

known techniques to improve similar technology in a similar way, and Butt's calibration process 200 would offer the same benefit for Hiraishi's delay circuit 372 as for Butt. EX1003,¶¶149-150.

2. Claim 2

a) 2[a]: Second Memory Device

Hiraishi discloses “a second memory device in the selected rank [e.g., memory device 200-32(Fig.1) in rank 0] is configurable to output at least a second section of the read data and at least a second read strobe [signals (orange) sent from memory device 200-32 to data buffer 300-8].” EX1003,¶¶152-154. As explained for 1[c1] and 1[c2] and shown below, Hiraishi discloses ranks comprising multiple memory devices 200 each with data and strobe lines connecting to a data buffer 300. *See supra*,§VI.A.1.d)-e),pp.28-31;EX1003,¶¶152-154.

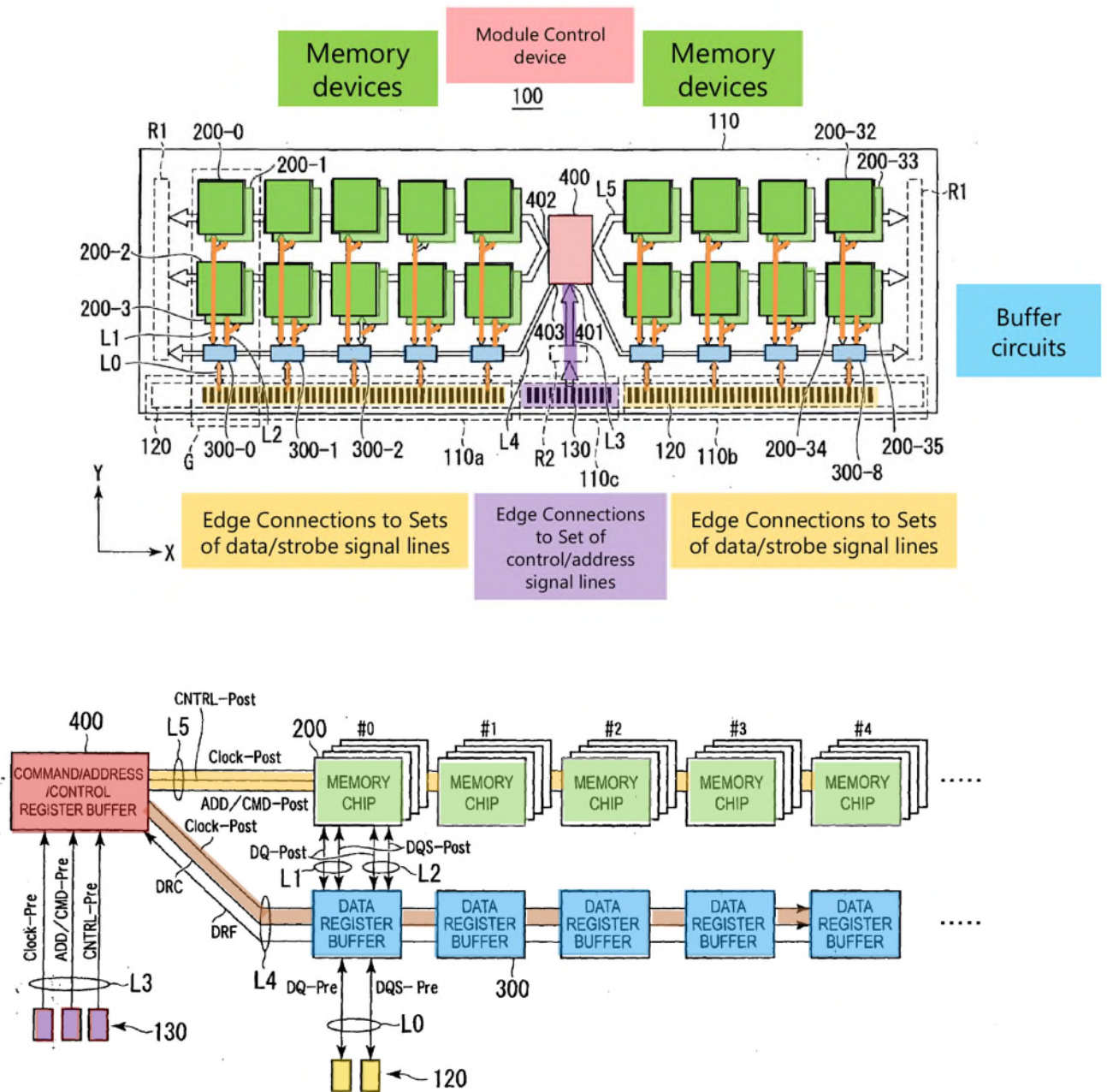


FIG. 7

A POSITA would understand that just as memory 200-0 in rank 0 outputs a “first” section of the read data (DQ) and a “first” strobe signal (DQS), memory device

Similar to 1[e], Hiraishi discloses “*the data buffers [data register buffer circuits 300] further include a second data buffer [e.g., 300-8 (blue, Fig. 1)] configurable to, in response to the one or more of the module control signals [e.g., module command/address/control line L4 (Figs. 1, 7) from command/address/control register buffer 400 (including DRC, brown, Figs. 1, 7)]...*” EX1003, ¶155; *supra*, §VI.A.1.g), pp. 34-35.



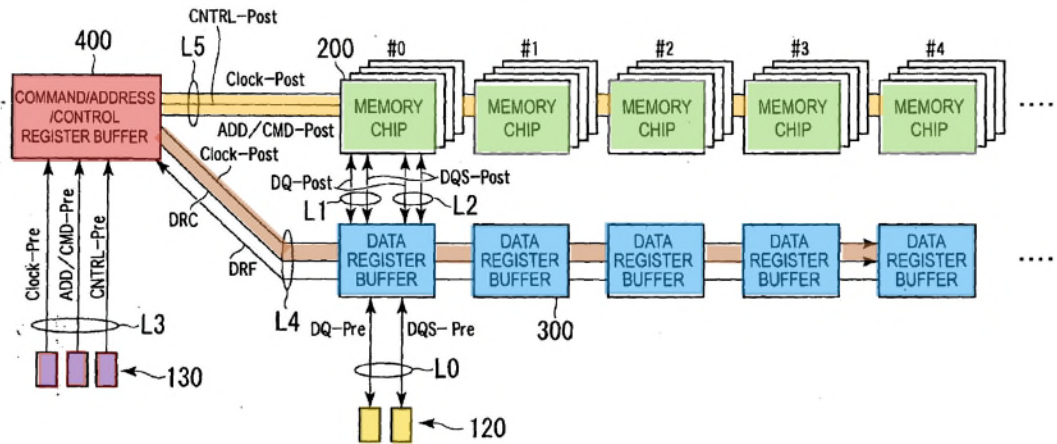


FIG.7

c) **2[c]: Delay Second Read Strobe**

A POSITA would understand that Hiraishi's "*second data buffer*" [e.g., 300-8] behaves analogous to the "*first data buffer*" [e.g., 300-0]. EX1003, ¶156. Thus, this element is met for the same reasons as for 1[f]. *Id.;supra*, §VI.A.1.h), pp.35-36.

d) 2[d]: Sample Second Section of Read Data

Because a POSITA would understand that Hiraishi's "*second data buffer*" [e.g., 300-8] behaves analogous to the "*first data buffer*" [e.g., 300-0], Hiraishi alone or with Butt discloses this element for the same reasons as for 1[g].

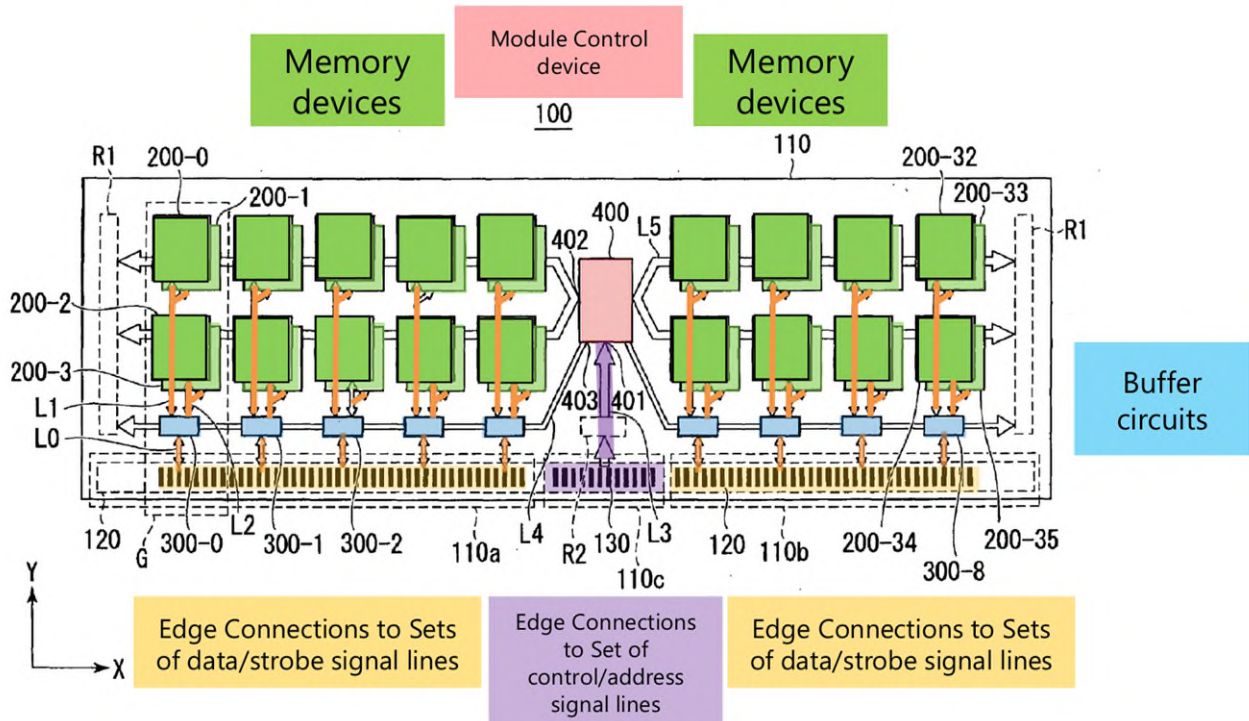
EX1003, ¶¶157-158; *supra*, §VI.A.1.i), pp.36-38.

e) 2[e]: Transmit Second Section of Read Data

Hiraishi discloses that *the second data buffer* [300-8] can “transmit the second section of the read data [e.g., data from 200-32] to a second section of the data bus [from data buffer 300-8 to the connectors 120 connecting to a section of

line 23 (Fig.3)]” similar to 1[h]. EX1003,¶¶159-160;EX1005,¶[0048];

supra,§VI.A.1.j),pp.38-39.



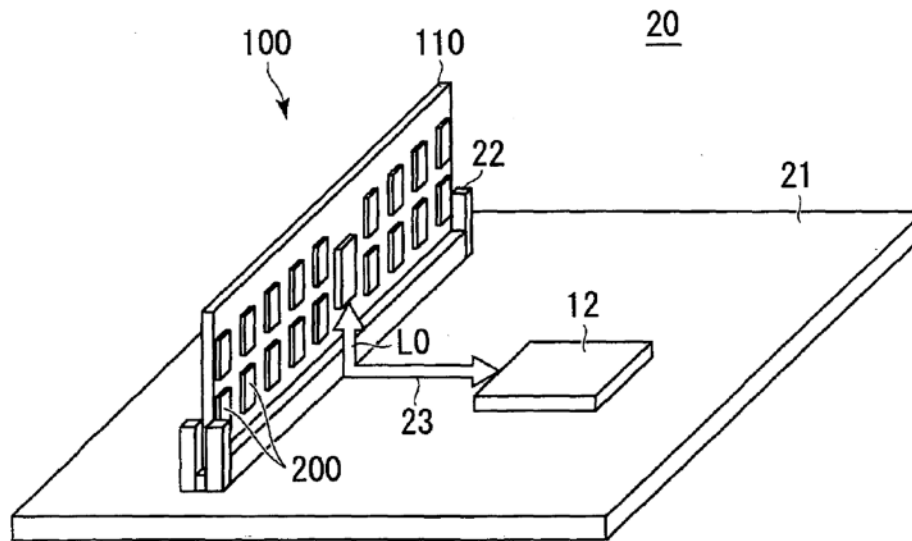


FIG.3

f) 2[f]: Second Predetermined Amount

Because a POSITA would understand that Hiraishi's "second data buffer" [e.g., 300-8] behaves analogous to the "first data buffer" [e.g., 300-0], Hiraishi alone or with Butt discloses the "second predetermined amount" [e.g., the amount of delay imposed by data register buffer circuit 300-8] for the same reasons described for the "first predetermined amount" addressed above in claim 1[i].
EX1003, ¶¶161-162; *supra*, §VI.A.1.k), pp.39-48.

3. Claim 4

a) 4[a]: Signals Received by First Data Buffer

As explained for 1[i], Hiraishi alone or with Butt discloses "the signals received by the first data buffer [e.g., 300-0] during one or more previous

operations [e.g., signals received during Hiraishi's S4 leveling, or by Butt's datapaths 114 during process 200] include at least a strobe signal associated with a previous operation [e.g., a DQS signal from Hiraishi's memory device 200-0 to data buffer 300-0, or DQS signal on which each offset in Butt is tested]."

EX1003, ¶¶163-164; *supra*, §VI.A.1.k), pp.39-48.

b) 4[b]: Signals Received by Second Data Buffer

Because a POSITA would understand that Hiraishi's "second data buffer" behaves analogous to the "first data buffer," Hiraishi alone or with Butt discloses the "second data buffer [e.g., 300-8]" would receive a strobe signal from 200-32 during read leveling in the same manner described above for 4[a] and 1[i] that the "first data buffer [e.g., 300-0]" would receive a strobe signal from 200-0 during read leveling. EX1003, ¶¶165-166; *supra*, §VI.A.3.a), p.53; §VI.A.1.k), pp.39-48.

4. Claim 6: Signals Received by First Data Buffer

Hiraishi alone or with Butt discloses claim 6 for the same reasons as 4[a]. EX1003, ¶167; *supra*, §VI.A.3.a), p.53.

5. Claim 7:

a) 7[a]: Receive System Clock Signal and Output Module Clock Signal

Hiraishi discloses that the "the module control device [e.g., 400 (red, Figs.6-7)] is further configurable to receive a system clock signal [CK/Clock-Pre, purple]

and output a module clock signal [CK/Clock-Post, brown].”

EX1003,¶168;EX1005,¶¶[0060],[0108],Figs.6-7.

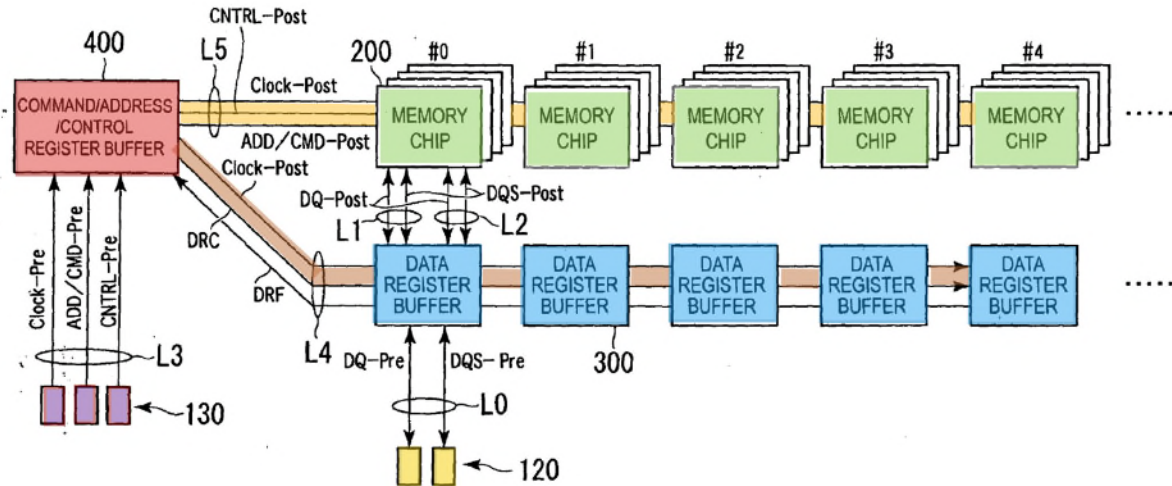


FIG.7

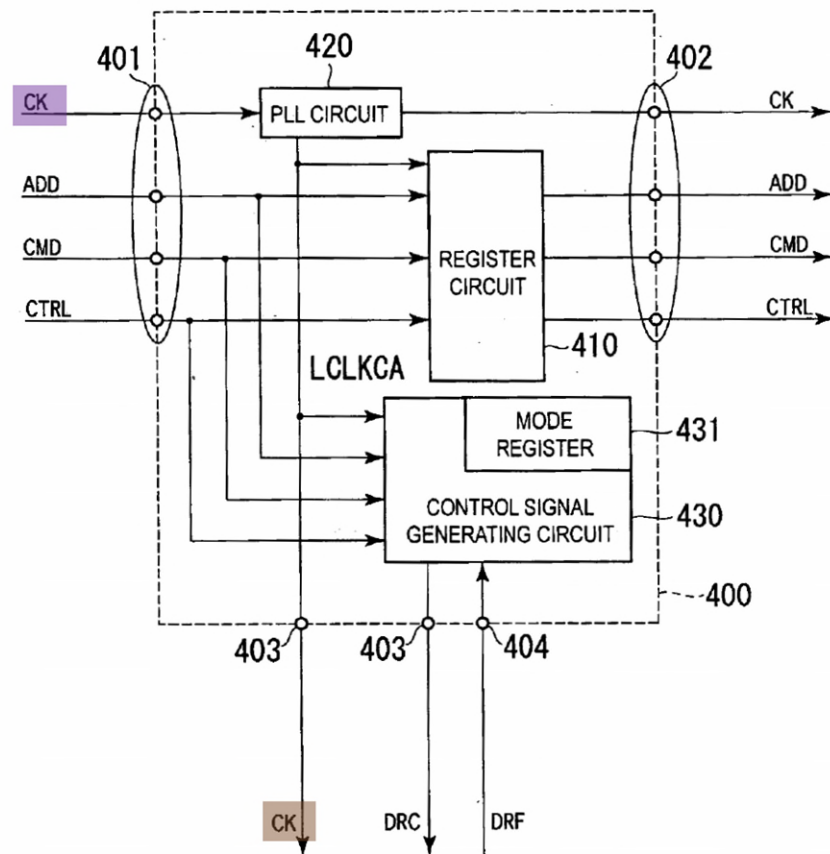


FIG. 6

b) 7[b1]: Receive Module Clock Signal

Hiraishi discloses “the first data buffer [e.g., 300-0] is further configurable to receive the module clock signal [CK (Figs.5-6), also shown as Clock-Post (Fig. 7)].” EX1003,¶169;EX1005,¶[0087],Figs.5-7.

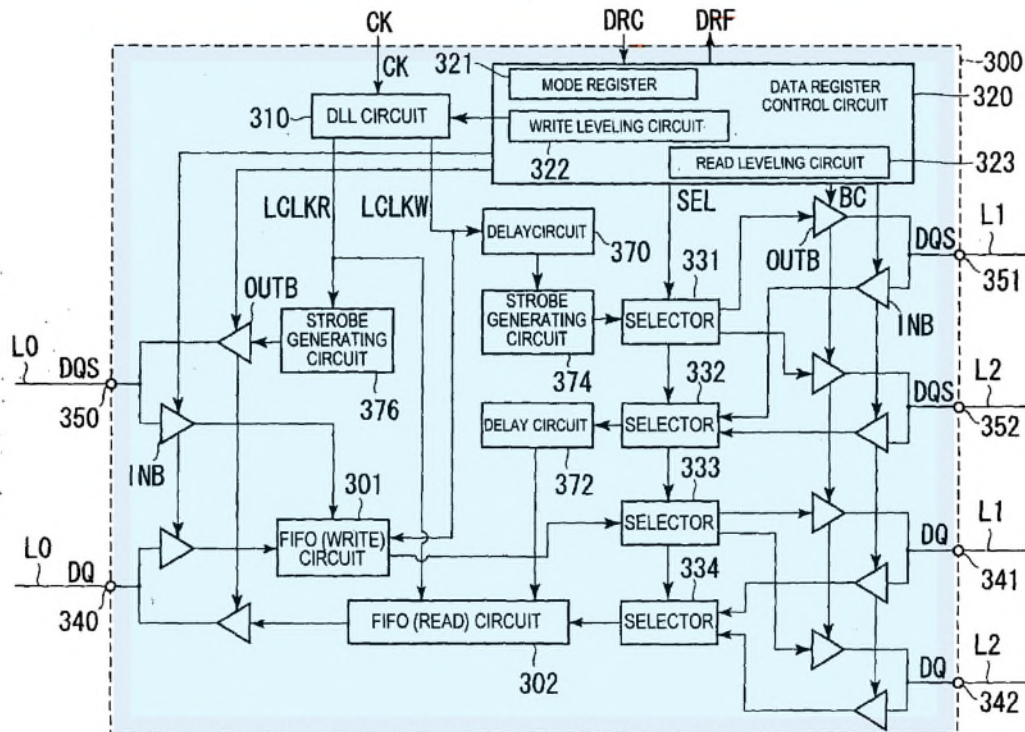


FIG. 5

c) 7[b2]: Generate Local Clock Signal

Hiraishi discloses “the first data buffer [e.g., 300-0 including DLL circuit 310(Fig.5)] is further configurable to...generate a local clock signal [e.g., LCLKW and LCLKR (Fig.5)] having a programmable phase relationship with the module clock signal [from 7[a] and 7[b1]].”

EX1003,¶170;EX1005,¶¶[0074],[0087],[0140],[0145],[0163]. A POSITA would understand from Hiraishi’s disclosure that the read and write leveling operations include “program[ing] [the] phase relationship” of the local clock used for read and write operations. *Id.* Furthermore, the DLL 310 in the data buffer has the same function as DLL 212 in the memory device, which includes generating local

clock signals with a programmable phase relationship relative to the clock signal CK. *Id.*; EX1005, ¶¶[0074],[0163].

d) 7[b3]: Output Local Clock Signal

Hiraishi discloses an embodiment where “*the first data buffer [e.g., 300-0] is further configurable to output the local clock signal [e.g., to the memory device 200-0].*” EX1003, ¶¶171-174. Hiraishi states that when the memory chip 200 does not include a DLL circuit, “the DLL circuit included in the data register buffer 300 is used to adjust the input/output timing” of the memory devices, too.

EX1005, ¶[200]; EX1003, ¶172. In such an embodiment, a POSITA would understand that a local clock signal would be output from the data buffer [e.g., 300-0] to the respective set of memory devices to synchronize the operations of those memory devices with the buffer circuit. *Id.* Sharing circuitry between buffer circuits and memory devices, including circuits that generate a local clock, was a well-known design choice, and one common technique was to output the local clock of the buffer circuit (e.g., 108 below) to the memory devices.

See, e.g., EX1009, 4:5-14; FIG. 1B, 4:31-41, FIG. 1A; EX1003, ¶173-174; *see also* EX1007, Figs. 10-13 (showing data buffer transmitting ECLK to memory devices).

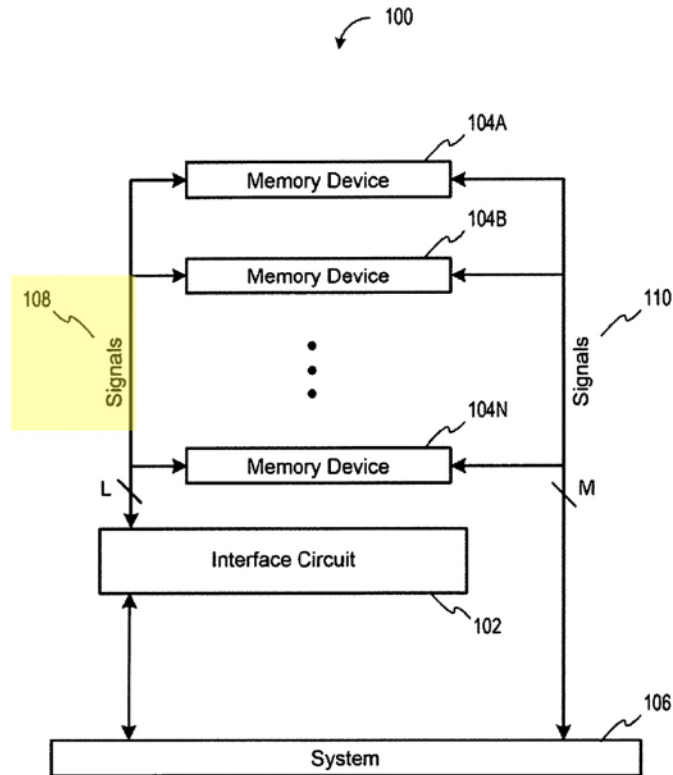


FIG. 1A

e) 7[c]: Receive Local Clock Signal

As explained for 7[b2] and 7[b3], a POSITA would understand that when the output of Hiraishi's DLL circuit 310 [e.g., LCLKR and/or LCLKW] is “used to adjust the input/output timing” of the memory device 200, EX1005,¶[0200]), “*the first memory device [e.g., 200-0] is configurable to receive the local clock signal [e.g., LCLKR and/or LCLKW from DLL circuit 310] and to output the first section of the read data and first read strobe in accordance with the local clock signal.*” EX1003,¶175;*supra*,§VI.A.5.c),p.57;§VI.A.5.d),p.58.

6. Claim 11: Circuitry

Hiraishi alone or with Butt discloses that “*the first data buffer* [e.g., 300-0] *includes circuitry* [including read leveling circuit 323 and delay circuit 372] *that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations* [e.g., S4 read leveling]” for the reasons explained for 1[i]. EX1003,¶¶176-177;*supra*,§VI.A.1.k),pp.39-48.

7. Claim 13: Memory Devices

Hiraishi discloses “[t]he memory chips 200 are, for example, DRAMs,” EX1005,¶[0050], and can be, in particular, “DDR3 DRAM,” *id.*,¶¶[0163],[0170], which a POSITA would understand is a type of “*double-data-rate dynamic random-access memory*” standardized by JEDEC, EX1021,pp.465,471-72,476-77;EX1020,pp.56,59,69, satisfying claim 13. EX1003,¶178.

8. Claim 14

a) 14[pre]: A Method

Claim 14 is a method corresponding to the memory module of claim 1. Thus, Hiraishi discloses 14[pre] (“A *method*...”). EX1003,¶179; EX1005,Figs.11,13,15.

b) 14[a]: Memory Module

Hiraishi discloses [14a] for the same reasons as 1[pre]. EX1003,¶180;*supra*,§VI.A.1.a),pp.21-23.

c) 14[b]: Module Board

Hiraishi discloses 14[b] for the same reasons as 1[a] and 1[b].

EX1003,¶181;*supra*,§§VI.A.1.b)-c),pp.23-28.

d) 14[c1]: Memory Devices

Hiraishi discloses 14[c1] for the same reasons as 1[c1].

EX1003,¶182;*supra*,§VI.A.1.d),pp.28-29.

e) 14[c2]: Data Buffers

Hiraishi discloses 14[c2] for the same reasons as 1[d].

EX1003,¶183;*supra*,§VI.A.1.f),pp.31-33.

f) 14[d]: Each Buffer Coupled to One Respective Memory Device

Hiraishi discloses that “*each respective data buffer [e.g., data register buffer 300] is coupled to one respective memory device [e.g., memory device 200] having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks,*” as explained for 1[d].

EX1003,¶184;*supra*,§VI.A.1.f),pp.31-33. Hiraishi discloses that the data buffer 300 “inputs and outputs 1-byte data,” EX1005,¶[0085];*id.*,¶[0053], and a POSITA would understand that 8-bit-wide (“x8), and pairs of 4-bit-wide (“x4”), memory devices were standard at the time, *e.g.*,EX1020,p.1;EX1018,pp.4.20.4-12,-16.

EX1003,¶184.

g) 14[e]: Receiving Input C/A Signals

Hiraishi discloses 14[e] for the same reasons as 1[b].

EX1003,¶185;*supra*,§VI.A.1.c),pp.24-28.

h) 14[f1]: Outputting Registered C/A Signals

Hiraishi discloses 14[f1] for the same reasons as 1[b].

EX1003,¶186;*supra*,§VI.A.1.c),pp.24-28.

i) 14[f2]: Perform Read Operation

Hiraishi discloses 14[f2] for the same reasons as 1[c2].

EX1003,¶187;*supra*,§VI.A.1.e),pp.30-31.

j) 14[g]: Outputting Module Control Signals

Hiraishi discloses 14[g] for the same reasons as 1[b].

EX1003,¶188;*supra*,§VI.A.1.c),pp.24-28.

k) 14[h]: Receiving Module Control Signals

Hiraishi discloses 14[h] for the same reasons as 1[d].

EX1003,¶189;*supra*,§VI.A.1.f),pp.31-33.

l) 14[i]: At First Data Buffer

Hiraishi discloses 14[i] for the same reasons as 1[e].

EX1003,¶190;*supra*,§VI.A.1.g),pp.34-35.

m) 14[j]: Delaying First Read Strobe

Hiraishi discloses 14[j] for the same reasons as 1[f].

EX1003,¶191;*supra*,§VI.A.1.h),pp.35-36.

n) 14[k]: Sampling First Section of Read Data

Hiraishi alone or with Butt discloses 14[k] for the same reasons as 1[g].

EX1003,¶192;*supra*,§VI.A.1.i),pp.36-38.

o) 14[l]: Transmitting First Section of Read Data

Hiraishi discloses 14[l] for the same reasons as 1[h].

EX1003,¶193;*supra*,§VI.A.1.j),pp.38-39.

p) 14[m]: Determining Frist Predetermined Amount

Hiraishi alone or with Butt discloses 14[m] for the same reasons as 1[i].

EX1003,¶194;*supra*,§VI.A.1.k),pp.39-48.

9. Claim 15

a) 15[a]: Second Data Buffer

Claim 15 is a method corresponding to claim 2. Thus, Hiraishi discloses 15[a] for the same reasons as 2[b]. EX1003,¶195;*supra*,§VI.A.2.b),pp.50-51.

b) 15[b]: Second Memory Device

Hiraishi discloses 15[b] for the same reasons as 2[a].

EX1003,¶196;*supra*,§VI.A.2.a),pp.48-50.

c) 15[c]: At Second Data Buffer

Hiraishi discloses 15[c] for the same reasons as 2[b].

EX1003,¶197;*supra*,§VI.A.2.b),pp.50-51.

d) 15[d]: Delaying Second Read Strobe

Hiraishi discloses 15[d] for the same reasons as 2[c].

EX1003,¶198;*supra*,§VI.A.2.c),p.51.

e) 15[e]: Sampling Second Section of Read Data

Hiraishi alone or with Butt discloses 15[e] for the same reasons as 2[d].

EX1003,¶199;*supra*,§VI.A.2.d),p.51.

f) 15[f]: Transmitting Second Section of Read Data

Hiraishi discloses 15[f] for the same reasons as 2[e].

EX1003,¶200;*supra*,§VI.A.2.e),pp.51-53.

g) 15[g]: Second Predetermined Amount

Hiraishi alone or with Butt discloses 15[g] for the same reasons as 2[f].

EX1003,¶201;*supra*,§VI.A.2.f),p.53.

10. Claim 17

a) 17[a]: Signals Received by First Data Buffer

Hiraishi alone or with Butt discloses 17[a] for the same reasons as 4[a].

EX1003,¶202;*supra*,§VI.A.3.a),p.53.

b) 17[b]: Signals Received by Second Data Buffer

Hiraishi alone or with Butt discloses 17[b] for the same reasons as 4[b].

EX1003,¶203;*supra*,§VI.A.3.b),p.54.

11. Claim 18

a) 18[a]: Further Comprising

Hiraishi alone or with Butt discloses claim 14.

EX1003,¶204;*supra*,§VI.A.8,pp.61-64.

b) 18[b]: Receiving System Clock Signal

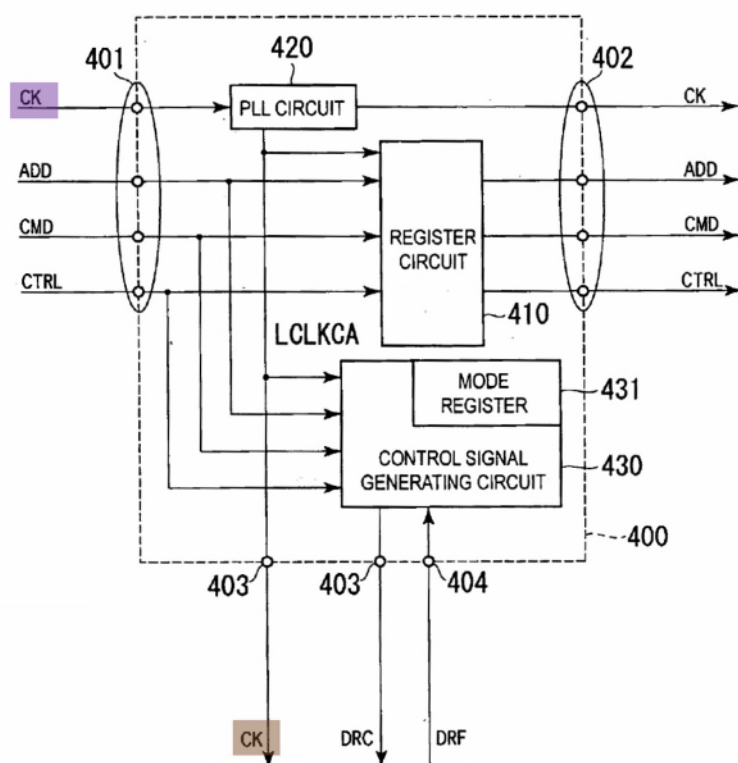
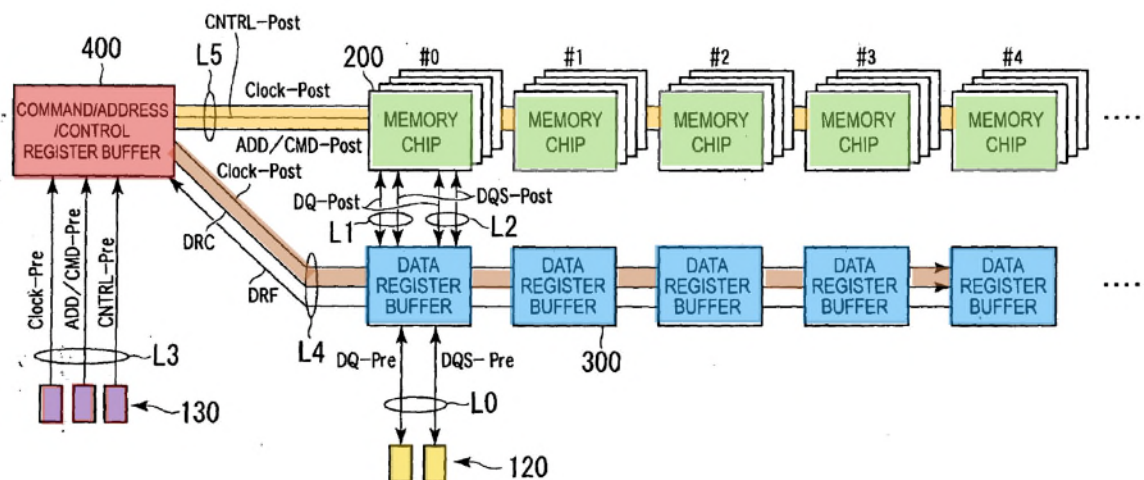
Hiraishi discloses 18[b] for the same reasons as 7[a].

EX1003,¶205;*supra*,§VI.A.5.a),p.54. As shown in Figures 6-7 (below), Hirashi discloses that the “system clock signal” [CK/Clock-Pre, purple] is received at the “module control device” [400] “concurrently with receiving the input C/A signals” [CNTRL-Pre,ADD/CMD-Pre] at terminal 401. EX1005,¶[0060],Figs.6-7.

c) 18[c]: Outputting Module Clock Signal

Hiraishi discloses 18[c] for the same reasons as for 7[a].

EX1003,¶206;*supra*,§VI.A.5.a),p.54. Hiraishi discloses “outputting, at the module control device [400, red], a module clock signal [e.g., CK/Clock-Post, brown] concurrently with outputting the module control signal [e.g., DRC]” on line L4 (Fig.7) at the same output terminal 403 (Fig.6) synchronized by the same clock signal (LCLKCA). EX1003,¶206;EX1005,¶¶[0019],[0060],[0098-99],[0108],Figs.6-7.



d) 18[d]: Receiving Module Clock Signal

Hiraishi discloses 18[d] this for the same reasons as 7[b1].

EX1003,¶207;*supra*,§VI.A.5.b),p.56.

e) 18[e]: Generating Local Clock Signal

Hiraishi discloses 18[e] for the same reasons as 7[b2].

EX1003,¶208;*supra*,§VI.A.5.c),p.57.

f) 18[f]: Outputting Local Clock Signal

Hiraishi discloses 18[f] for the same reasons as 7[b3].

EX1003,¶209;*supra*,§VI.A.5.d),pp.58-60.

g) 18[g]: Receiving Local Clock Signal

Hiraishi discloses 18[g] for the same reasons as 7[c].

EX1003,¶210;*supra*,§VI.A.5.e),p.60.

h) 18[h]: Outputting First Section of Read Data

Hiraishi discloses 18[h] for the same reasons as 7[c].

EX1003,¶211;*supra*,§VI.A.5.e),p.60.

B. Ground 2: Claims 3,5,12,16 are Obvious Over Hiraishi and Butt and Further In View of Ellsberry

Claims 3, 5, 12, and 16 recite variations where pairs of 4-bit wide (“x4”) memory devices replaces individual 8-bit wide (“x8”) memory devices. Using a pair of 4-bit wide memory devices instead of an 8-bit wide memory device (200) in Hiraishi would have been obvious to a POSITA because using either 4-bit or 8-bit

wide memory devices on a module was well-known at the time and standardized by JEDEC. EX1003,¶¶212-213;EX1005,¶[0073];EX1020,1,3-12;EX1018,4.20.4-12, -15, -25 to -27;EX1021,370-71,Table8.1.

Ellsberry incorporates the JEDEC standards by reference and teaches that his invention is compatible with modules that comply with the JEDEC standards, *see* EX1007,[0051] & claim 10, and thus the JEDEC standards can be used to explain how a POSITA would understand Ellsberry, as previously determined by the Board. EX1015,62-63 (citing *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019)).

For example, Ellsberry teaches using either x8 or pairs of x4 memory devices on a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi. Thus, it would have been obvious to combine the teachings to implement Hiraishi with pairs of x4 memory devices, and there would have been a reasonable expectation of success. EX1003,¶¶214-216. As shown below, Ellsberry discloses 8-bit wide data buffers (SWITCH ASIC, blue, with DQ[3:0](lower nibble) and DQ[7:4](upper nibble)), coupled to **either** 8-bit wide memory devices (below right, green), EX1007,Figs.2,5,13, **or** pairs of 4-bit wide memory devices (below left, green, e.g., the pair connected to chip-select signal CS0A), EX1007,Figs.2,6,11. EX1015,77-

78;EX1007,¶¶[0051],[0054];EX1020,p.6(“Stacked” x4 memory devices);EX1003,¶¶214-215.

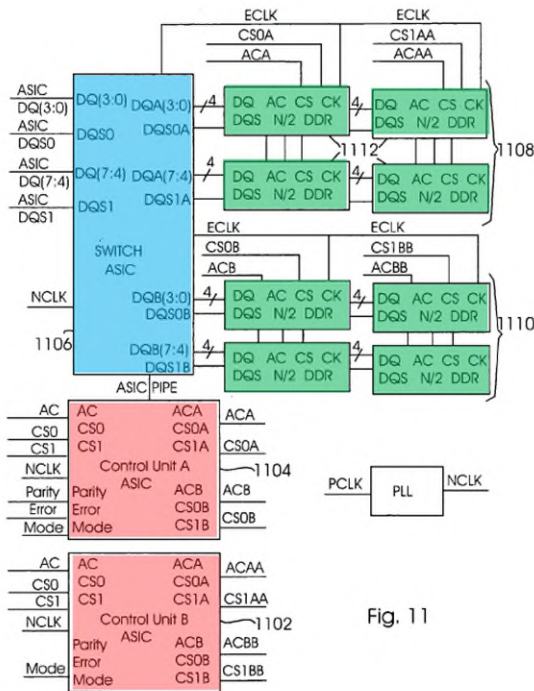


Fig. 11

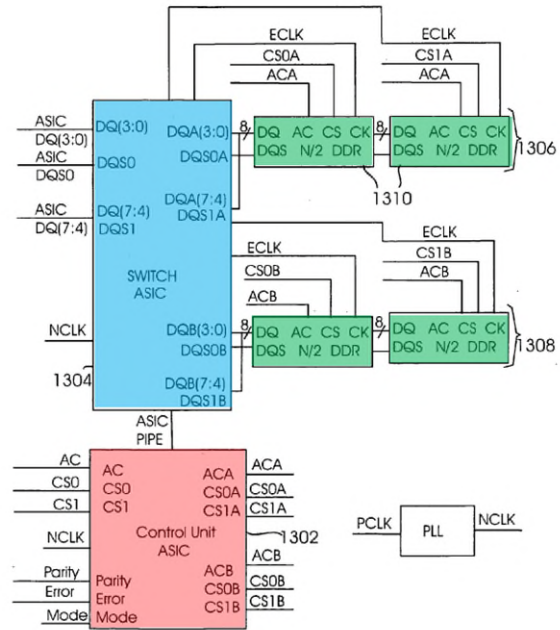


Fig. 13

1. Claim 3

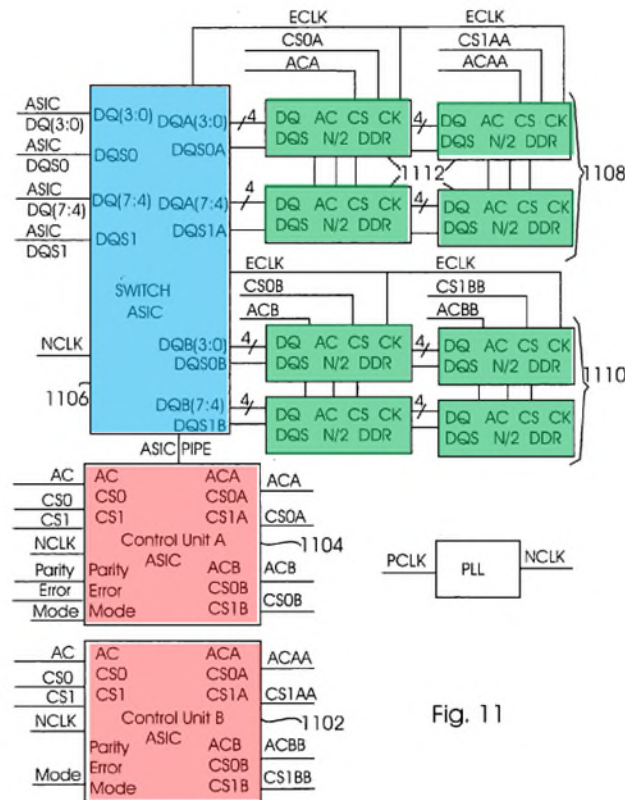
a) 3[a]: Third Memory Device

Hiraishi alone or with Ellsberry (discussed above) renders obvious using a pair of 4-bit memory devices instead of an 8-bit memory device. EX1003,¶217. Thus, the “*first memory device*” from 1[c2] (e.g., 200-0 in rank 0) could be a 4-bit memory device handling a lower nibble of a data byte (like DQA(3:0) in Ellsberry), and there could be a second 4-bit memory device for handling the upper nibble of that data byte (like DQA(7:4) in Ellsberry) in the same rank (e.g., “*a third memory device in the selected rank*,” here rank 0), together making a pair of

4-bit memory devices connected to the same data buffer (e.g., 300-0).

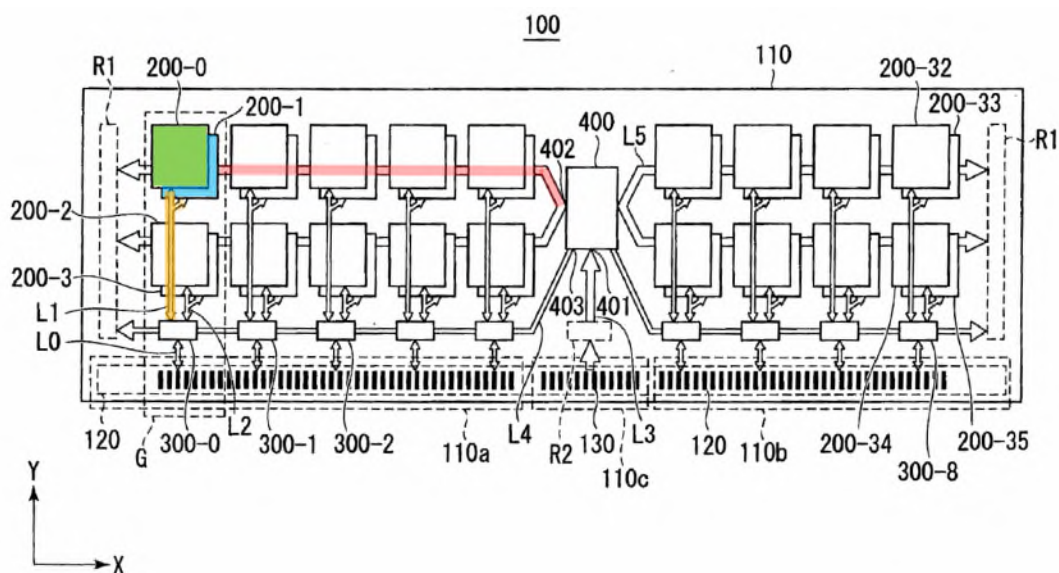
EX1003,¶¶213-217;EX1007,Fig.11. This “*third memory device*” for the upper nibble would be “*configurable to output a third section of the read data and a third read strobe*” to the “*first data buffer*” (300-0).

EX1003,¶217;EX1007,¶[0051],Fig.11.



A POSITA would know that different arrangements of 4-bit wide (i.e., “x4”) memory devices were possible. EX1003,¶217. For example, as taught by JEDEC, the lower nibble of a given rank (e.g., DQ0-DQ3) could be placed on one side of the module, while the upper nibble of that rank (e.g., DQ4-DQ7) could be placed at the same location on the other side of the module. EX1018,pp.4.20.4-8,-14,-31. A

POSITA would also know that x4 memory devices can be stacked to conserve space, and that different stacking arrangements would be possible. *E.g.*, EX1020,p.6. For example, instead of one x8 memory device, it would be possible to stack two x4 memory devices that provide the lower and upper nibble of a given byte in a given rank. EX1003,¶217. Alternatively, it would be possible to stack the lower nibbles of two ranks (e.g., ranks 0 and 1) on one side of the printed circuit board (e.g., at the location of the green box below) and to stack the upper nibbles of those two ranks (e.g., ranks 0 and 1) on the other side of the printed circuit board at the same horizontal and vertical location (e.g., at the location of the blue box below), with the lower and upper nibble in a given rank (e.g., rank 0) receiving one chip-select signal, and the lower and upper nibble in the other rank (e.g., rank 1) receiving a different chip-select signal, as taught by JEDEC. EX1020,p.6;EX1018,pp.4.20.4-8,-9,-15,-21,-35; EX1007,¶[0051],Figs. 6,11.



Each of these physical arrangements was well known and obvious. *See, e.g., KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.”). And each would result in a pair of x4 memory devices, instead a single x8 memory device, in a given rank (e.g., rank 0) connected to the same data buffer (e.g., 300-0). EX1003,¶217.

b) 3[b]: Each Section of Read Data 4-bit Wide

When pairs of 4-bit memory devices are used in Hiraishi as explained above, each 4-bit memory device would read 4-bit wide sections of data, and thus “*each of the first section* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-0], *the second section* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-8], *and the third section of the read data* [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] *is 4-bit wide.*” EX1003,¶218.

c) 3[c]: Module Control Signals

When pairs of 4-bit memory devices are used in Hiraishi as explained above, the “*first data buffer*” [300-0] would be “*coupled to the third memory device*” [upper nibble of the byte in rank 0 connected to data buffer 300-0]. EX1003,¶219.

As explained for 1[e], the “*first data buffer* [300-0]...respon[ds] to the one or more of the module control signals.” *Id.*;supra,§VI.A.1.g),pp.34-35.

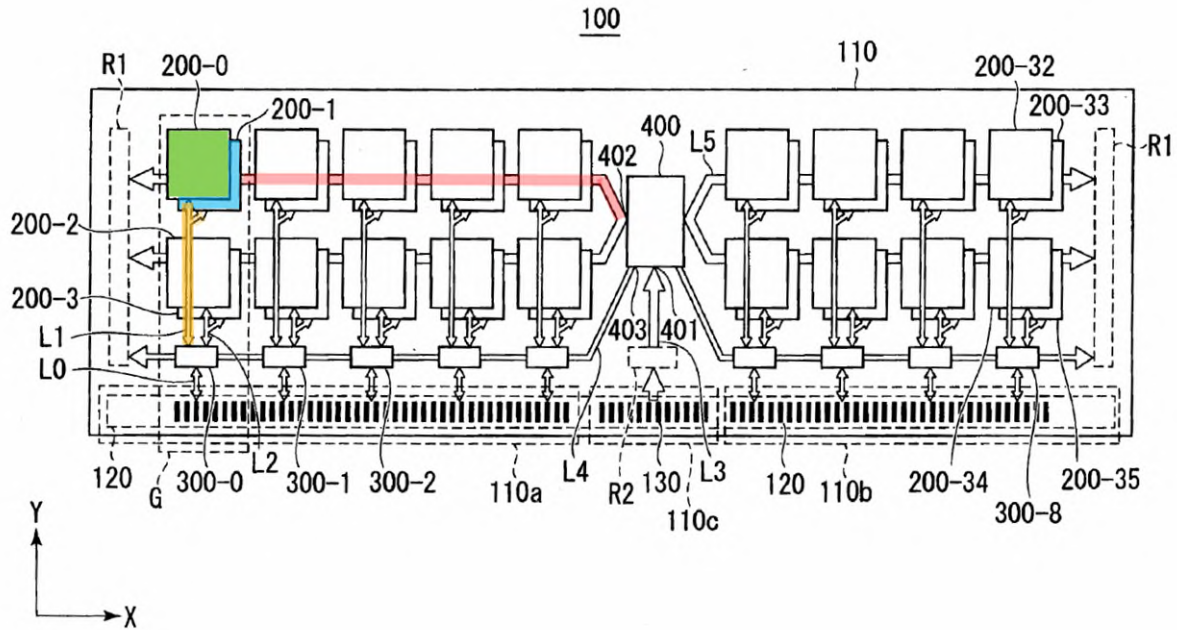
d) 3[d]: Delay Third Read Strobe

When pairs of 4-bit memory devices are used in Hiraishi as explained above, the “*first data buffer*” [300-0] would “*delay the third read strobe by a third predetermined amount to generate a third delayed read strobe*” in the same manner as described for the “*first read strobe*” in claim 1[f], supra,§VI.A.1.h),pp.35-36. EX1003,¶220.

e) 3[e]: Sample Third Section of Read Data

Hiraishi, alone or with Ellsberry and/or Butt, discloses that the “*first data buffer*” [300-0] would “*sample the third section of the read data* [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] *using the third delayed read strobe*” in the same manner described in 1[g] for the “*first section of the read data*,” supra,§VI.A.1.i),pp.36-38. EX1003,¶¶221-223. Furthermore, this would be done “*concurrently with sampling the first section of the read data* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-0] *using the first delayed read strobe*,” because both 4-bit memories in the pair would receive the same read command (with the same chip-select signal, e.g., CS0A) at the same time, supra pp.68-73, and in response, would output their respective read data and strobe signals concurrently, such that the “*first data buffer*” [300-0] would process the

read data and strobe signals from the pair of memory devices concurrently,
including “sampling” the respective section of the read data using the respective
delayed strobe. EX1003,¶¶221-223;EX1005,FIG.1;EX1007,FIG.11;
EX1021,pp.319,413.



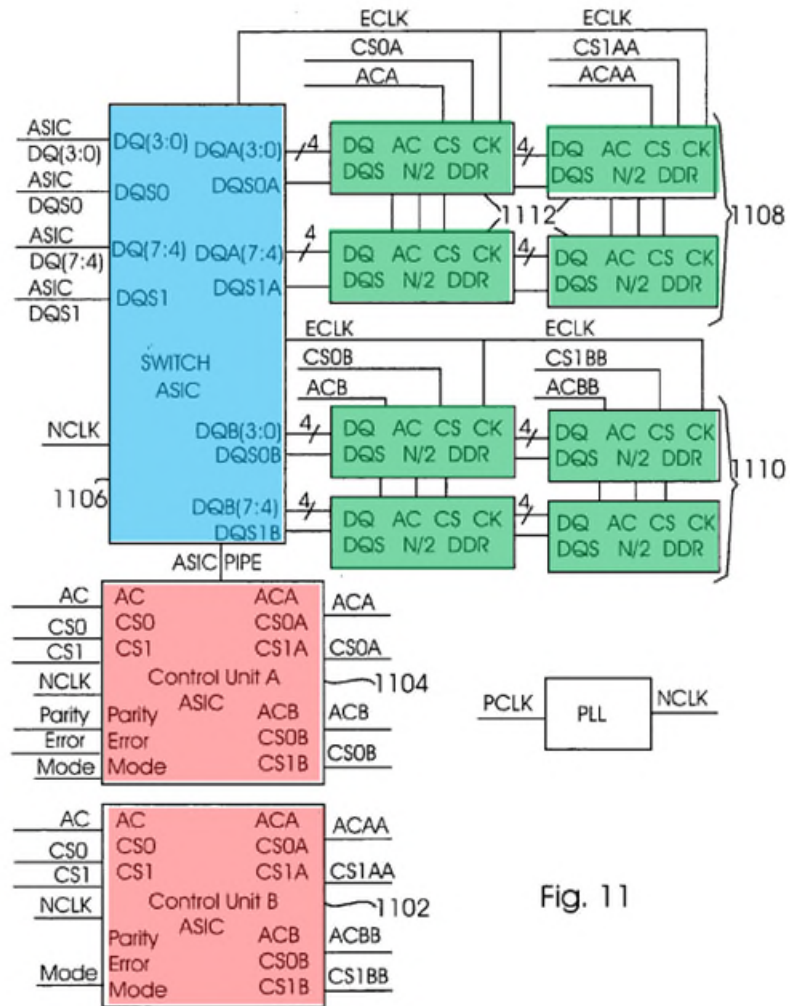


Fig. 11

f) 3[f]: Transmit Third Section of Read Data

When pairs of 4-bit memory devices are used in Hiraishi, the “*first data buffer*” [300-0] would “*transmit the third section of the read data* [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] *to a third section of the data bus* [e.g., the upper nibble from buffer circuit 300-0 (blue) to the connectors 120 (yellow) connecting to the data line L0 (Fig.1) connecting to a section of line 23 (Fig.3)] *concurrently with transmitting the first section of the read data* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-0] *to the first*

section of the data bus” as explained for 1[h]. *Supra*,§VI.A.1.j),pp.38-39;EX1003,¶224. A POSITA would understand that data read in a single read operation from two 4-bit memory devices would be transmitted concurrently. *Id.*

g) 3[g]: Third Predetermined Amount

When pairs of 4-bit memory devices are used in Hiraishi, the “*third predetermined amount* [e.g., the amount of delay for the upper nibble of the byte in rank 0 connected to data buffer 300-0] can be determined similar to the “*first predetermined amount*” [e.g., the amount of delay for the lower nibble of the byte in rank 0 connected to data buffer 300-0] as explained for 1[i]. *Supra*,§VI.A.1.k),pp.39-48;EX1003,¶¶225-226.

2. Claim 5: First and Second Section of Read Data 4-bit Wide

Hiraishi alone or with Ellsberry discloses claim 5 for the same reasons discussed above for claim 3. *Supra*,pp.68-77;EX1003,¶227.

3. Claim 12: First Section of Read Data 4-bit Wide

Hiraishi alone or with Ellsberry discloses claim 12 for the same reasons discussed immediately above for claim 5. EX1003,¶228.

4. Claim 16

a) 16[a]: Third Memory Device

Claim 16 is a method corresponding to claim 3. Thus, Hiraishi alone or with Ellsberry discloses 16[a] for the same reasons as 3[a].

EX1003, ¶229; *supra*, §VI.B.1.a), pp.70-73.

b) 16[b]: At First Data Buffer

Hiraishi alone or in view of Ellsberry discloses 16[b] for the same reasons as 3[c]. EX1003, ¶230; *supra*, §VI.B.1.c), p.73.

c) 16[c]: Delaying Third Read Strobe

Hiraishi alone or in view of Ellsberry discloses 16[c] for the same reasons as 3[d]. EX1003, ¶231; *supra*, §VI.B.1.d), p.74.

d) 16[d]: Sampling Third Section of Read Data

Hiraishi alone or with Butt or in further view of Ellsberry discloses 16[d] for the same reasons as 3[e]. EX1003, ¶232; *supra*, §VI.B.1.e), pp.74-76.

e) 16[e]: Transmitting Third Section of Read Data

Hiraishi alone or with Ellsberry discloses 16[e] for the same reasons as 3[f]. EX1003, ¶233; *supra*, §VI.B.1.f), p.76.

f) 16[f]: Third Predetermined Amount

Hiraishi alone or with Butt or in further view of Ellsberry discloses 16[f] for the same reasons as 3[g]. EX1003, ¶234; *supra*, §VI.B.1.g), p.77.

C. Ground 3: Claims 8-10 and 19-20 are Obvious Over Hiraishi and Butt and Further View of Kim

Claims 8-10 and 19-20 recite additional limitations related to the detection and handling of “metastability” states. As explained below, these metastability limitations were all known in the art at the time of the ’506 Patent, and would have been obvious further in view of Kim (EX1008). EX1003, ¶¶239-246.

1. Claim 8

a) 8[a]: Receive System Clock Signal

Hiraishi discloses that “the module control device [command/address/control register 400] is further configurable to receive a system clock signal [e.g., CK/Clock-Pre in L3, purple].” EX1005, ¶¶[0098],[0108], Figs.6-7; EX1003, ¶¶235-236.

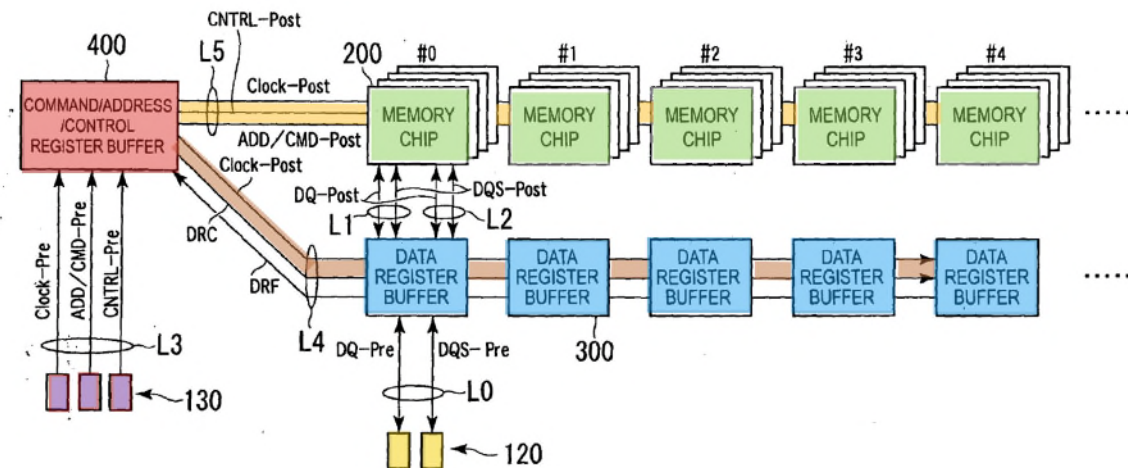


FIG. 7

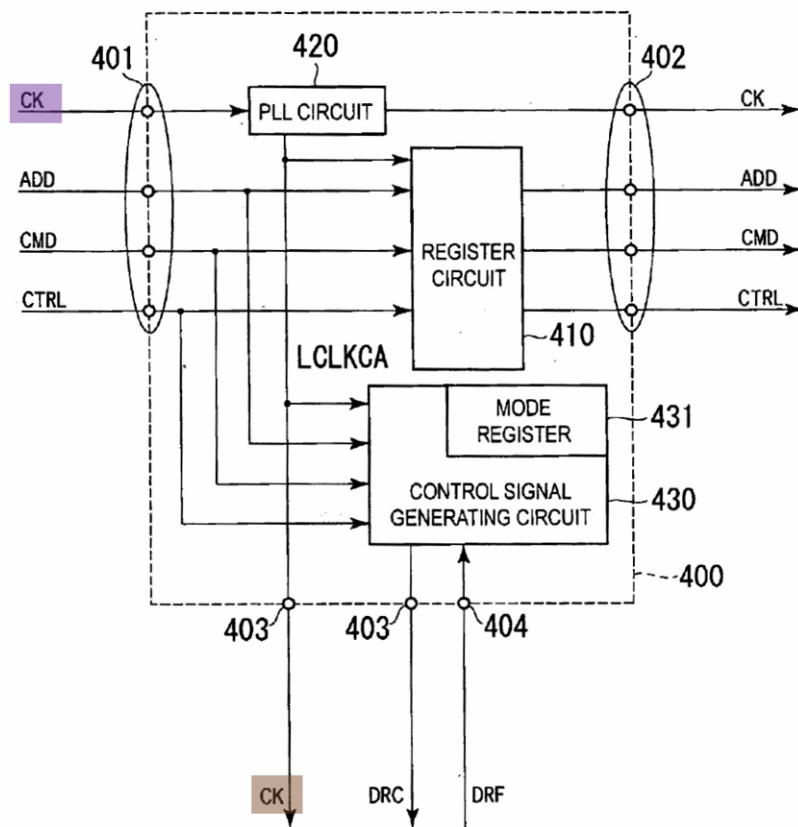


FIG.6

b) 8[b]: Output Module Clock Signal

Hiraishi discloses that “the module control device [400] is further configurable to ... output a module clock signal [e.g., CK/Clock-Post in L4, brown] together with the module control signals [e.g., DRC in L4, brown] to the data buffers [300, blue]” because both signals are output at the output terminal 403 (Fig.6) and the generation of the module control signals (DRC) is synchronized by the same clock signal (LCLKCA). EX1005, ¶¶[0098],[0099],[0108], Figs.6-7; EX1003, ¶¶237-238.

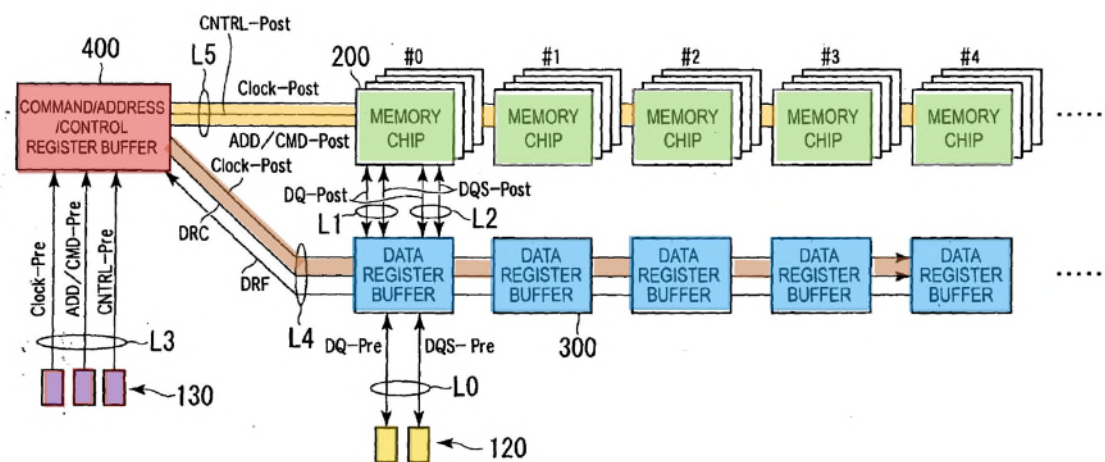


FIG.7

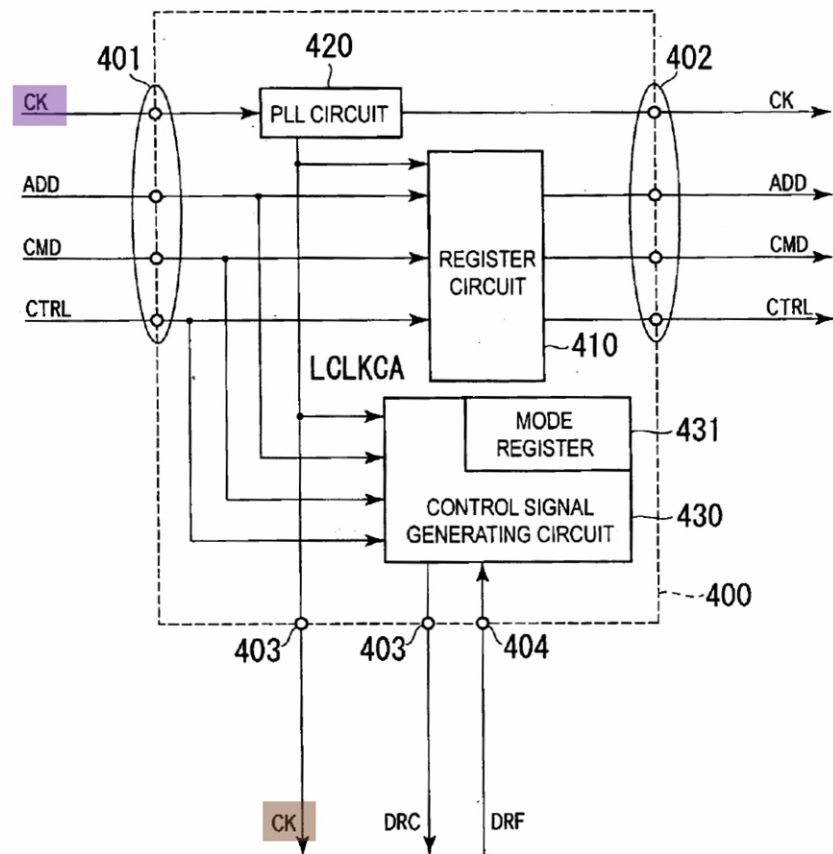


FIG. 6

c) 8[c]: Metastability Detection Circuit

Hiraishi alone or with Kim, as illustrated by Hiraishi's Figure 5 (below), discloses that "the first data buffer further includes receiver circuits [in DLL circuit 310 and Data Register Control circuit 320] corresponding to respective ones of the module control signals [e.g., the signals in control signal DRC]," and renders obvious "a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition [such as a

metastability condition in capturing signal values] *in the respective module control signals* [e.g., the signals in control signal DRC] *with respect to the module clock signal* [CK].” EX1003, ¶239.

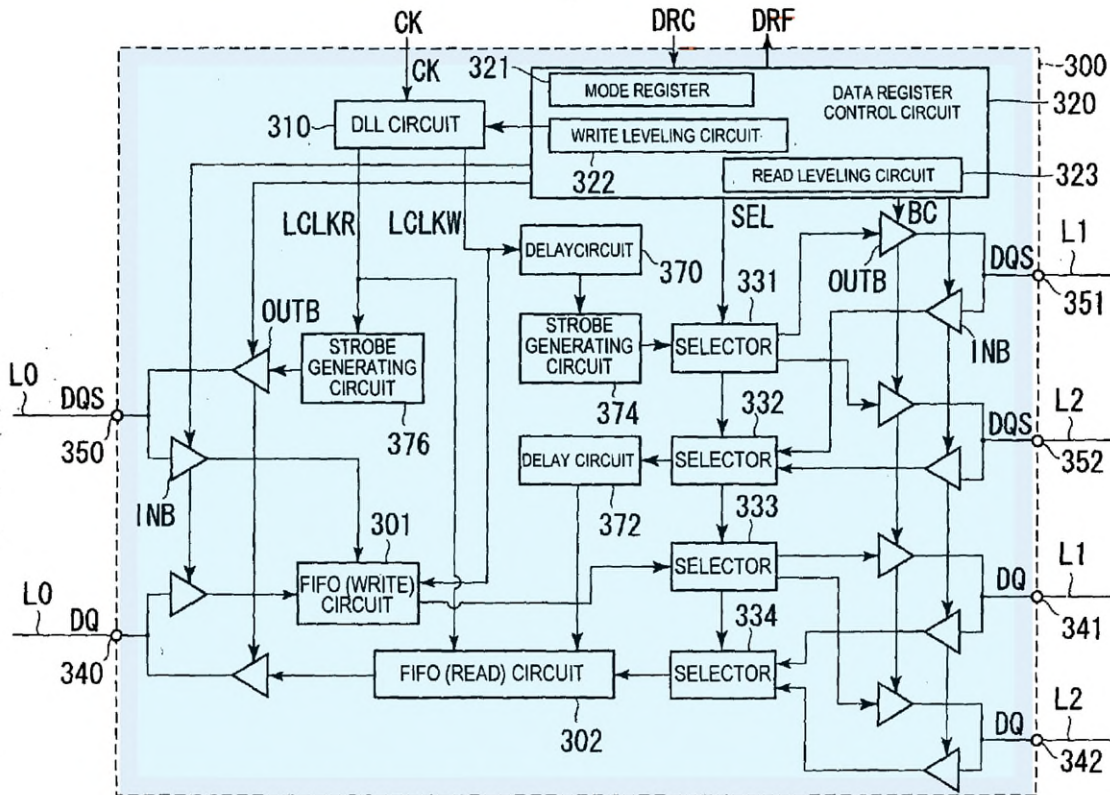


FIG. 5

As discussed for 8[a] and 8[b], Hiraishi discloses that the control signal DRC and the corresponding module clock CK are transmitted on line L4 to multiple data buffers 300. *Id.*, FIG. 7; *supra*, §§ VI.C.1.a)-b), pp. 79-82; EX1003, ¶240. Hiraishi further discloses that the DLL circuit 310 in the data buffer 300 receives the module clock signal CK and generates from the received CK signal a number of internal clocks, including LCLKR and LCLKW, with fine phase adjustments

that are used for the internal operation of the data buffer. EX1005,¶¶[0074], [0087],FIG.5;EX1003,¶240. Hiraishi also discloses that the DRC signal is captured by the Data Register Control Circuit 320. EX1005,¶[0088]; EX1003,¶240. A POSITA would understand from this that DLL circuit 310 generates the internal clock that is used to capture the DRC signal based on the received clock signal CK. EX1003,¶¶240-241.

Because the control information conveyed by the DRC signal may not be correctly captured if there is a metastability condition at the reception of the DRC, a POSITA would have understood, and been motivated, to use the DLL circuit of Hiraishi to generate the internal clock from the received module clock signal CK with a specific phase relative to the DRC signals to avoid metastability.

Id.;EX1008,1:21-31. A POSITA would have understood that such metastability may happen in Hiraishi when the received clock and DRC signals are captured by the DLL and register control circuit with an incorrect time alignment.

EX1003,¶241;EX1027,2:53-56;EX1028,1:36-46;EX1030,FIG.2A,1:33-35.

Indeed, due to the high speed at which the memory devices operated at the time, a POSITA would have understood that the “use of the DLL circuit is substantially essential.” EX1005,¶[0163];EX1003,¶241.

In light of the possibility of erroneous DRC signal reading, it would have been obvious to a POSITA to have the DLL circuit 310 and Data Register Control

Circuit 320 include the functionality of a known metastability condition detector (such as taught by Kim, EX1008) and implement the DLL circuit 310 and Data Register Control Circuit to avoid such potential metastability, including adjusting the phase of the internal clock signal and/or the phase of the DRC signal (similar to how Hiraishi's DLL circuit adjusts the LCLKW signal's phase). EX1003,¶242. A POSITA would have understood that such a detector can be used, e.g., during initialization, to indicate the presence of a metastability condition so that the phases of the internal clock and the DRC signals can be adjusted to avoid the metastability condition. *Id.*

To the extent one might argue Hiraishi alone does not render obvious the claimed metastability detection circuit, Kim discloses such circuitry. EX1008,1:12-14,1:21-31,2:23-27;EX1003,¶243. Further, a POSITA would have understood from at least Kim's disclosure that, to detect and adjust for a metastability condition, the metastability detection circuit “*generate[s] one or more metastability indicators,*” and that the output described in Kim indicates the presence of metastable states, thus including “*one or more metastability indicators.*” EX1008,Abstract;*see also*,EX1028,FIG.8,8:25-27;EX1003,¶246.

Kim is analogous art to Hiraishi since each aim to make communication between integrated circuits more reliable. EX1003,¶243;EX1008,1:12-14. Kim discloses “a metastability detection/prevention circuit 20” to be incorporated with

any “main circuit 10” in need thereof, including “a data input buffer.”

EX1008,1:21-31,2:23-37. It would have been obvious to combine the functionality of Kim’s metastability detection circuitry with the DRC inputs in Hiraishi’s data register buffers (300). EX1003,¶244. The motivations for this combination would include obtaining more reliable communications by avoiding metastability at the input of the clock and DRC signals, which signals carry important control information. *Id.*;EX1005,¶[0100].

Combining Kim’s metastability detection functionality into Hiraishi’s data register buffer would have been well within the level of skill at the time and provided nothing more than expected from the prior art: detecting metastability at the clock and DRC inputs and removing it. EX1003,¶245;EX1030,FIG.2A,1:33-35;EX1005,¶[0087];EX1016,¶¶[0021-22]. Hiraishi already teaches that its DLL circuit 310 can perform fine phase adjustments, and a POSITA would have understood that metastability can be avoided by adjusting the phases of the internal clock and the DRC signal to properly latch the control signal value in the input buffer. *Id.*;EX1005,¶[0087]; *see also* EX1030,FIG.2A,1:33-35. A POSITA also would have understood that either or both of the clock and DRC signals can be delayed as required for the proper capture of the data values. EX1003,¶245; *see also* EX1016,¶¶[0021-22].

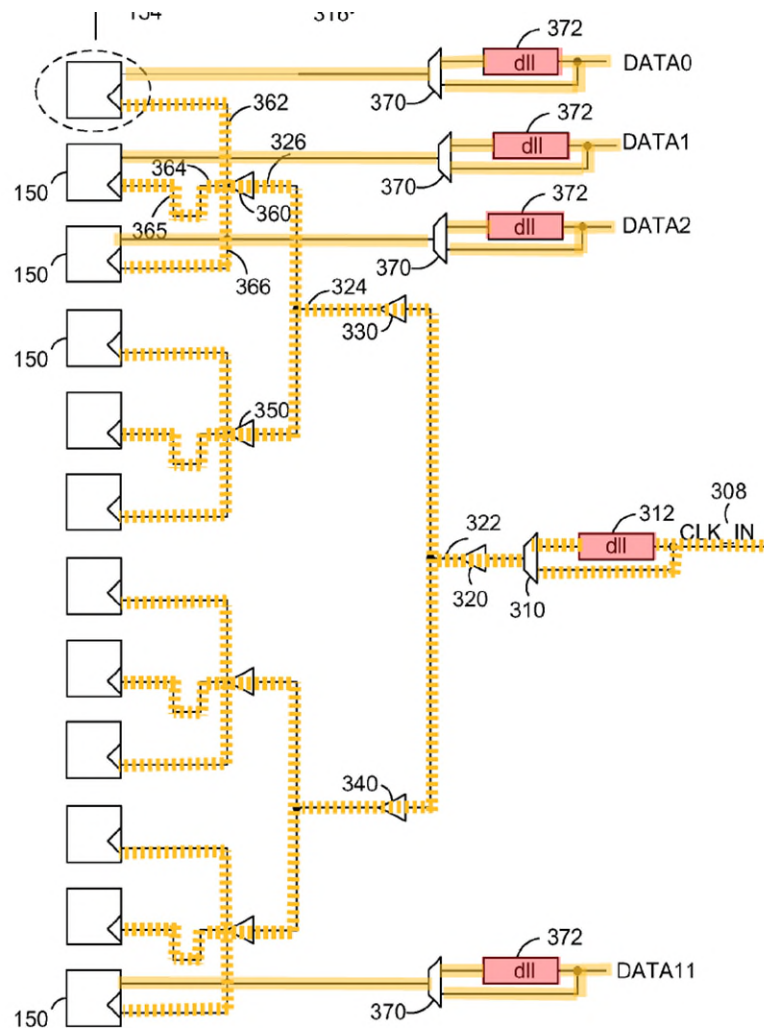
2. Claim 9

a) 9[a]: Generate Delayed Version of Module Clock Signal

Hiraishi alone or with Kim discloses “*the metastability detection circuit [including DLL circuit 310 and Data Register Control Circuit 320] is further configurable to generate at least one delayed version of the module clock signal [an internal clock phase delayed to lag relative to the received clock], and at least one delayed version of the respective module control signal [a delayed DRC, so that the phase of clock signal CK moves forward relative to the delayed DRC].*” EX1003,¶248.

As previously discussed, a POSITA would have understood that Hiraishi’s DLL circuit 310 and data register control circuit 320 adjust the relative phase of the internal clock signal and the DRC signal to correctly capture the DRC signal values. *Supra*,§VI.C.1.c),pp.82-86;EX1003,¶¶241-247. A POSITA would have also understood that the phase of the received clock signal CK could be early or late relative to the phase of the received DRC signal, so she would have been motivated to generate both a delayed clock signal (in case the clock is early) and a delayed control signal DRC (in case the clock is late) and select the one which removes the metastability condition. *See,e.g.*,EX1016,¶¶[0021-22],Fig.3(below). Delaying both these signals was well within a POSITA’s level of skill (similar to delaying the strobe signal to capture the eye of the read data, EX1030,Figs.2A,2B).

EX1003, ¶¶245,249-252; EX1016, FIG. 3 (reproduced below in part, annotated, showing optional delay lines 372 and 312 for data and clock signals, respectively), [0018], [0021-22]; EX1028, FIG. 4 (reproduced below, showing specific metastability detection circuitry including delay elements to delay both the clock and data signals).



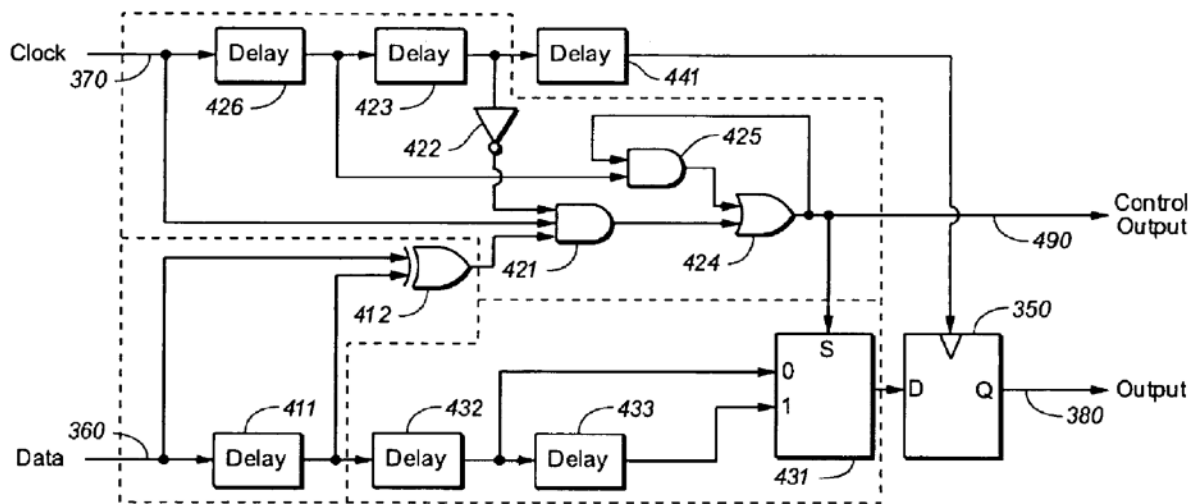


FIG. 4

Thus, it would have been obvious to a POSITA, and a POSITA would have been motivated to implement the functionality of Kim's metastability detection together with delaying elements for both the clock and DRC, as evidenced, e.g., by Nimaiyar (EX1016) and Ma (EX1028) shown above. EX1003, ¶¶249-251.

b) 9[b]: Signal Selection Circuit

As explained for 9[a], it would be obvious in view of Hiraishi alone or with Kim to prepare for both an early and a late received clock CK by generating a delayed clock to use as an alternative to the received clock signal.

Supra, §VI.C.2.a), pp.87-89; EX1003, ¶¶248-253. To implement these two signals, a POSITA would understand that a signal selection circuit would be needed to select either the received clock signal CK (if the clock is late or on time) or the delayed clock (if the clock is early). EX1016, ¶¶[0018],[0020-22], Fig.3; EX1003, ¶253.

c) 9[c]: First Metastability Indicator

A POSITA would understand that whether to use the delayed clock signal, or the received clock signal, depends on which signal avoids metastability.

EX1003, ¶¶255-256; *see also* EX1016, ¶[0018], FIG.3. Thus, it would be obvious to a POSITA in view of Hiraishi alone or with Kim to use “*at least a first metastability indicator*” in selecting between “*the module clock signal and the at least one delayed version of the module clock signal.*” EX1003, ¶¶255-256.

3. Claim 10

a) 10[a]: Receive Module Control Signal

As discussed for claims 8 and 9, a POSITA would have been motivated to implement Kim’s metastability detection functionality in Hiraihsi’s DLL and data register control circuits 310 and 320, including generating delayed versions of **both** the DRC signal and the clock signal. *See*, §VI.C.1-2, pp.79-90; EX1003, ¶¶235-257. A POSITA would have been motivated to have “*the signal selection circuit*” be “*configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal*” because a delayed DRC signal may be needed to properly capture the DRC signal value in the case where the clock signal is late. *See, e.g.*, EX1016, ¶¶[0021-22], FIG.3; EX1028, FIG.4, 7:35-39; EX1003, ¶¶257-258.

b) 10[b]: Second Metastability Indicator

As discussed for 10[a], a POSITA would have been motivated to select either the DRC signal or the delayed DRC signal to properly capture the DRC signal values, depending on whether or not the clock signal was late.

See, supra, §VI.C.3.a), p.90; EX1003, ¶257. A POSITA would have been motivated to implement the functionality of Kim's metastability detection circuit in Hiraishi's data register controller 320 to use a metastability detection circuitry which provides both a "*first metastability indicator*" to detect whether the clock needs to be delayed and "*a second metastability indicator*" to detect whether the DRC needs to be delayed, and select delaying the clock or the DRC based on these metastability indicators for reasons discussed above. *Supra*, §VI.C.2.a), pp.87-90; EX1003, ¶¶249-250, 259-260; *see also* EX1028, FIG.4(above); EX1008, Abstract; EX1016, FIG.3(above). For example, as also discussed above with respect to Hirashi and Butt, a POSITA would have understood that latching predefined data with different relative phases can be used to identify which combination of delayed clocks and/or data captures the data properly. *Supra*, §VI.A.1.k), pp.39-48. Thus, a "*first metastability indicator*" would indicate whether the DRC signal is correctly captured with delayed clock, and "*a second metastability indicator*" would indicate whether the DRC signal is correctly captured with delayed DRC signal. EX1003, ¶¶259-260.

c) 10[c]: Sampler

As discussed for 10[a] and 10[b], a POSITA would have been motivated to implement Kim's metastability detection functionality in Hiraishi such that the DRC signal and the CK clock signal can be delayed to avoid metastability and properly capture the DRC signal values. *Supra*, §§VI.C.3.a)-b), pp.90-91; EX1003, ¶¶257-262; *see also* EX1016, ¶¶[0021-22], Fig.3; EX1030, FIGS.2A,2B. A POSITA would have further understood that, after the proper selection, the DRC signal values can be captured by circuitry, such as a register, that samples the selected version of the DRC signal according to the selected version of the clock signal. *Id.*

4. Claim 19

a) 19[a]: Receiving System Clock Signal

Hiraishi discloses 19[a] for the same reasons as 18[b].
EX1003, ¶263; *supra*, §VI.A.11.b), p.66.

b) 19[b]: Outputting Module Clock Signal

Hiraishi discloses 19[b] for the same reasons as 18[c].
EX1003, ¶264; *supra*, §VI.A.11.c), pp.66-67.

c) 19[c]: Metastability Indicators

Hiraishi alone or with Kim discloses 19[c] for the same reasons as 8[c].
EX1003, ¶265; *supra*, §VI.C.1.c), pp.82-86.

5. Claim 20

a) 20[a]: Generating Delayed Version of Module Clock Signal

Hiraishi alone with Kim discloses 20[a] for the same reasons as 9[a].

EX1003, ¶266; *supra*, §VI.C.2.a), p.87-89.

b) 20[b]: Selecting Clock Signal

Hiraishi alone or with Kim discloses 20[b] for the same reasons as 9[c].

EX1003, ¶267; *supra*, §VI.C.2.c), p.90.

c) 20[c]: Selecting Module Control Signal

Hiraishi alone or with Kim discloses 20[c] for the same reasons as 10[b].

EX1003, ¶268; *supra*, §VI.C.3.b), p.91.

d) 20[d]: Sampling Module Control Signal

Hiraishi alone or with Kim discloses 20[d] for the same reasons as 10[c].

EX1003, ¶269; *supra*, §VI.C.3.c), p.92.

D. Ground 4: Claims 1-2,4,6-7,11,13-15,17-18 are Obvious Over Hiraishi and Butt in view of Tokuhiro

The '506 Patent discloses a “previous operation” (e.g., write) in a different direction than the later “operation” (e.g., read). EX1003, ¶¶43-44,99-100. Under this claim interpretation, which is narrower than Patent Owner’s interpretation addressed above, the claims of the '506 Patent are obvious in further view of Tokuhiro (EX1006).

1. Tokuhiro's teachings

Tokuhiro teaches that a DDR3 memory interface employs fly-by topology for connections between a memory controller and a DIMM (Dual Inline Memory Module). EX1006,1:22-33,2:54-59;EX1003,¶271. Tokuhiro teaches that fly-by delays need to be compensated for both write *and* read data, and problems arise if the fly-by delay in read operations exceeds one clock period. EX1006,3:9-12;EX1003,¶271.

Tokuhiro solves this problem by delaying the transmission of the read data to compensate for the large fly-by delays before the read data enters the common clock domain of the receiver, without the need for special mechanisms like a FIFO. EX1003,¶¶271-272;EX1006,3:16-26,18:66-19:7. To do this, Tokuhiro discloses “a ***second variable delay unit*** for delaying, in the ***read operation***, a data signal input from the memory ***by a second delay time***.” EX1003,¶272;EX1006,3:16-26.

Tokuhiro also teaches that, for the ***read*** operation, the “***second delay time ... is set based on the first delay time***” which is determined during a ***write*** operation. *Id.*

Thus, Tokuhiro discloses the technique corresponding to the narrower construction of the claims requiring different memory operations. *Id.*; see also EX1006,10:63-12:5,13:23-37,13:47-14:2,18:26-52,18:66-19:7,Figs.5-7,11;EX1003,¶¶273-277.

2. Motivations to Combine Tokuhiro and Hiraishi

Tokuhiro and Hiraishi are analogous art since each is directed to improving memory systems using memory modules where memory chips are arranged in a fly-by configuration, such as modules using DDR3 memory chips. EX1003,¶278. A POSITA would have been motivated to combine Tokuhiro and Hiraishi for at least three reasons, below. *Id.*

- a) ***First motivation: Tokuhiro teaches calculating read delays based on the delays for write operations, which is more efficient than Hiraishi's technique of performing read leveling independent of the write delays***

Hiraishi recognizes that “because the data DQ is buffered by the data register buffer 300,” the timing is off between DQ/DQS-Pre and DQ/DQS-Post, thus recognizing the necessity of timing adjustments. EX1003,¶279; EX1005,¶[0104],FIG.7(below).

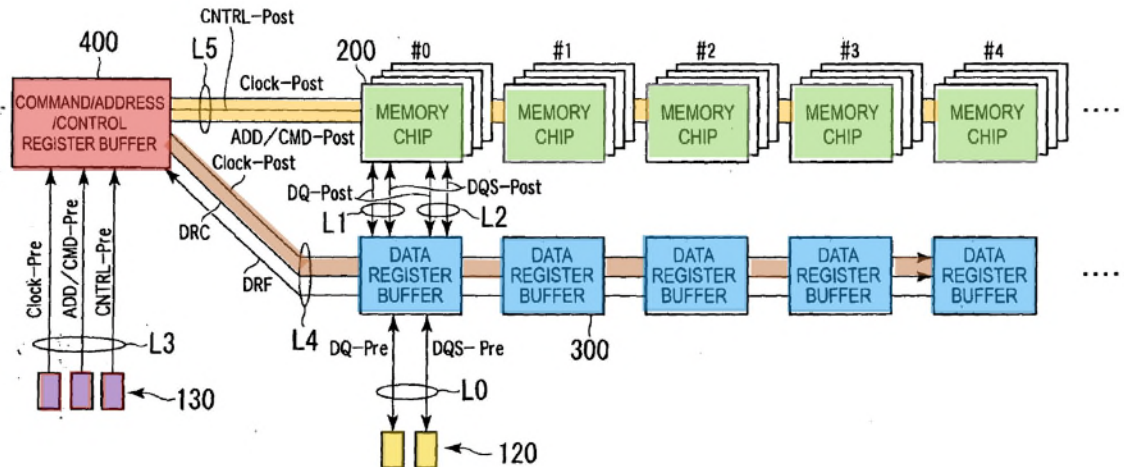


FIG. 7

In Hiraishi, these timing adjustments include write and read leveling operations, which are performed independently from each other. EX1003, ¶¶280-282; EX1005, ¶¶[0140],[0151],[0161], FIGS. 14-17 (annotated FIGS. 15 (“S4” read leveling”) & 17 (“S5” read leveling) below):

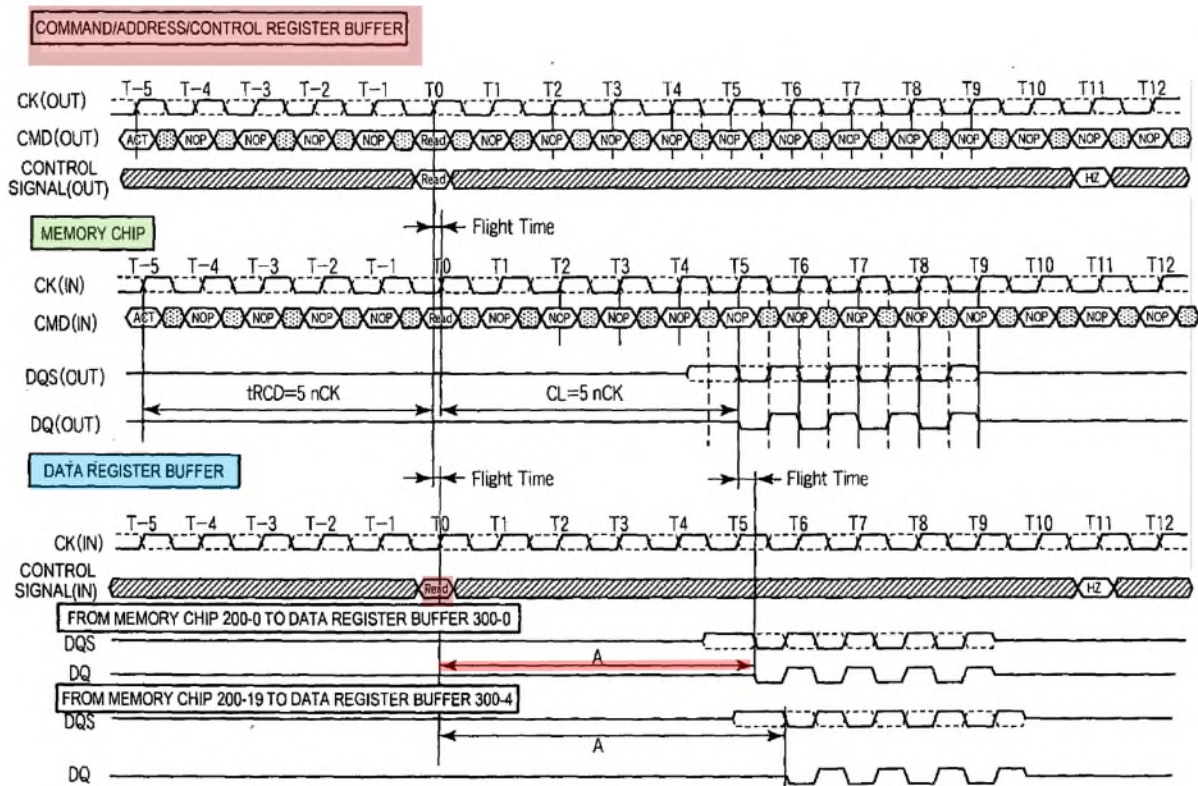
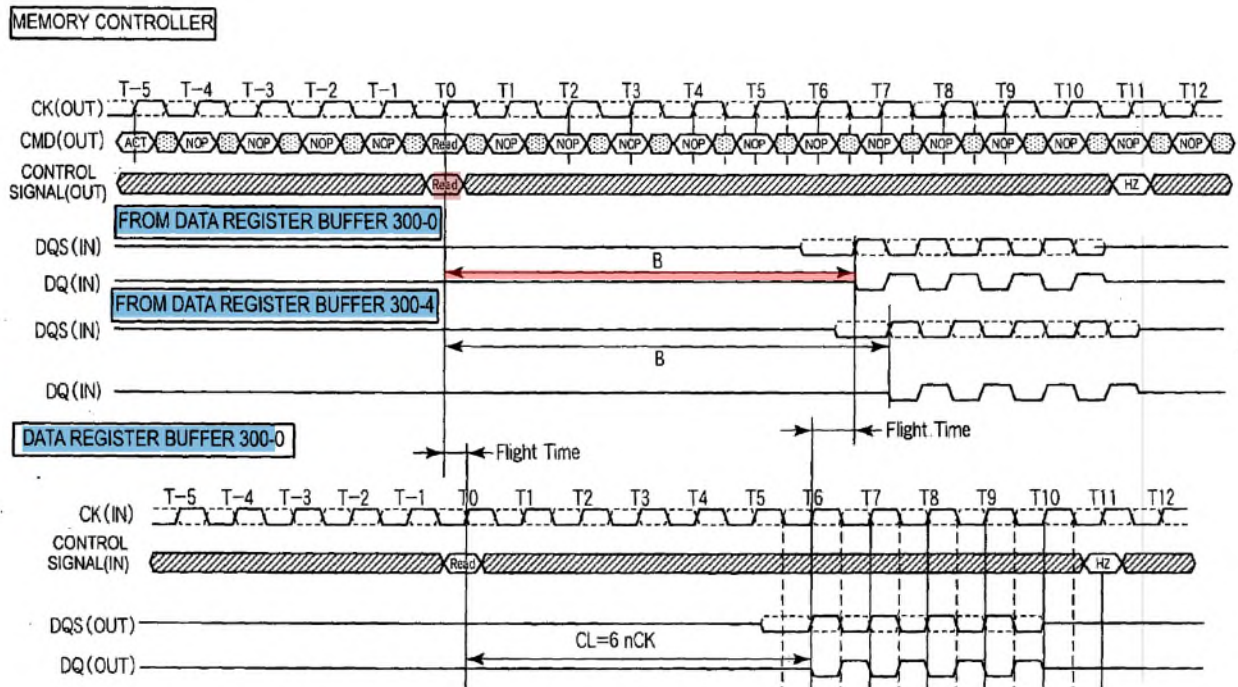
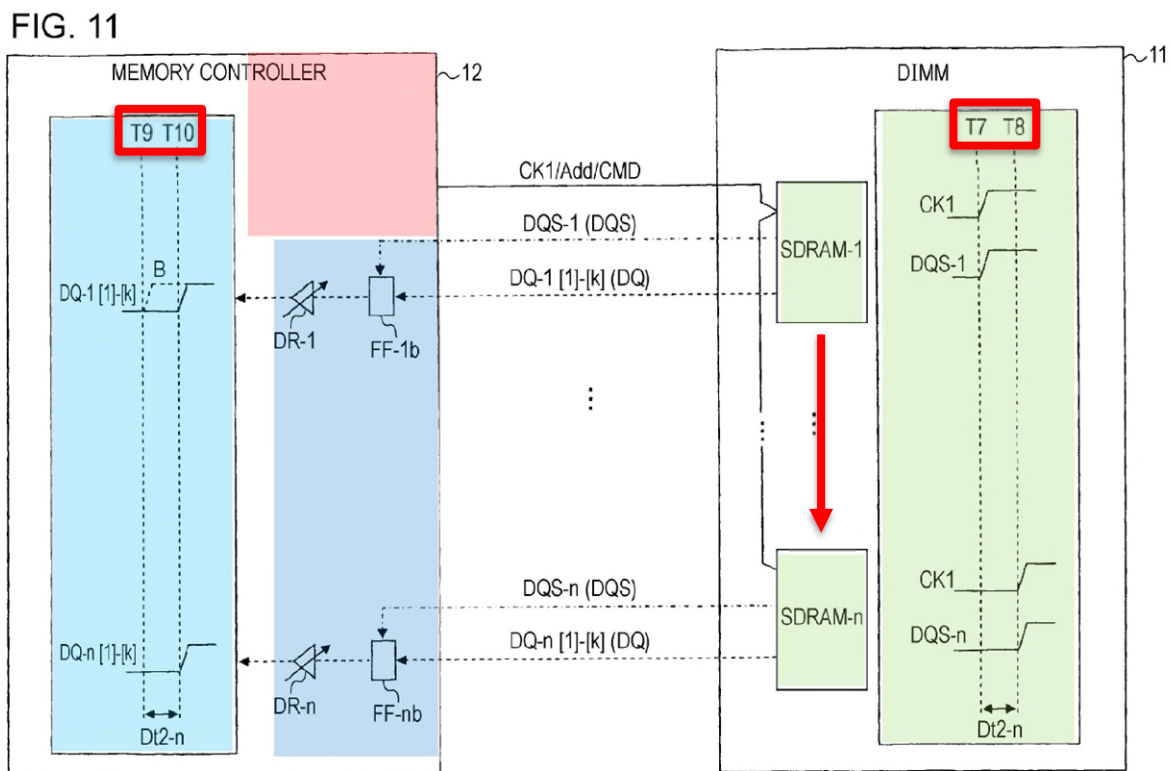
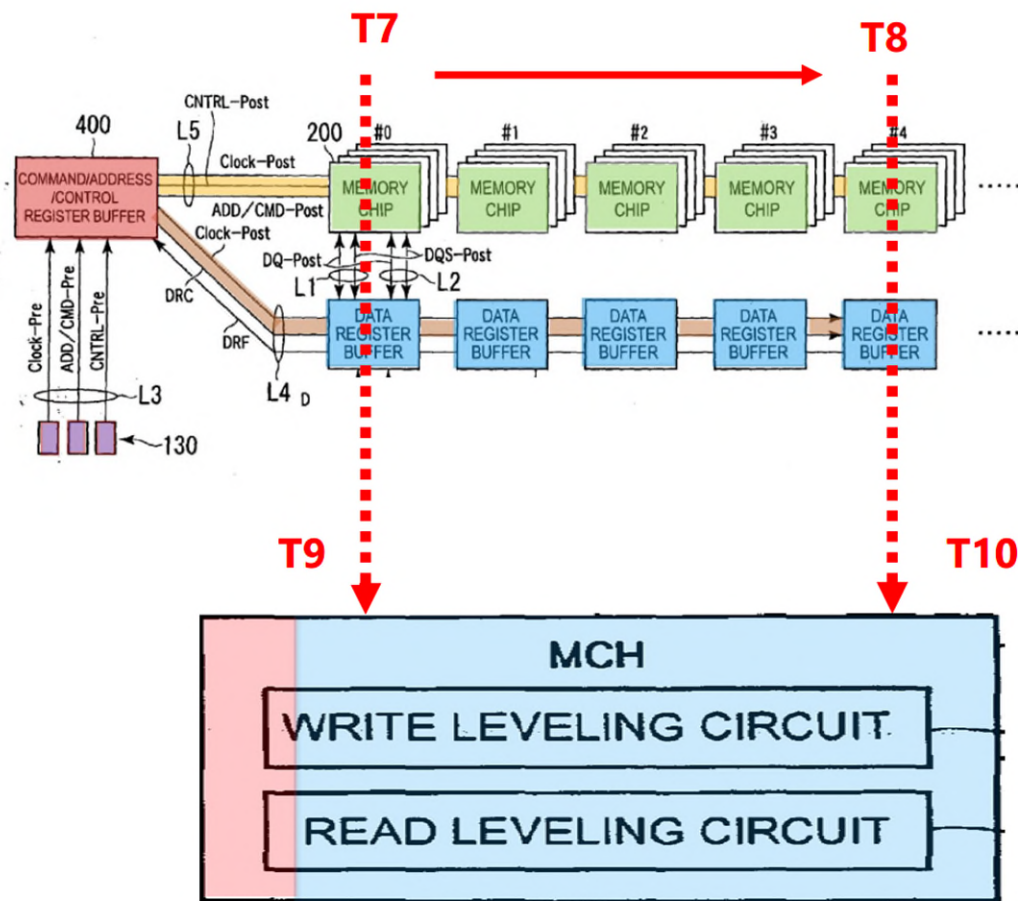


FIG. 15



A POSITA would have understood that performing write and read leveling operations independently, as in Hiraishi, requires time and corresponding circuitry, thus motivating her to simplify these operations, e.g., by using Tokuhiro's technique of setting the read delays based on the write delays. EX1003,¶¶283-286,288;EX1006,Abstract,18:66-19:7,FIG.11(annotated below showing read delay elements DR-1 to DR-n in Tokuhiro so all read data arrives at T10, rather than between T9 and T10 due to fly-by delays);EX1005,¶¶[0129-30],FIGS.11,7(annotated, MCH and timing T7 to T10 added to show similar fly-by delays in Hiraishi).



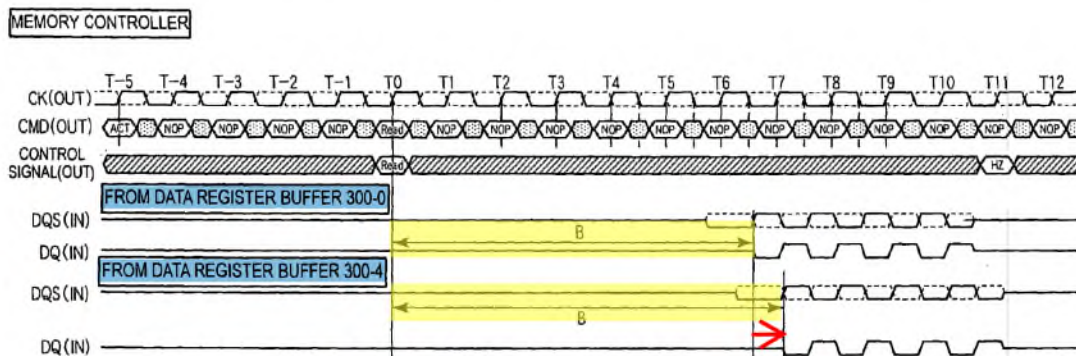


This combination would have been well within the level of skill at the time, since Tokuhiro details how to calculate the read delays based on the write operations' delays, and this would have provided what is expected from the combination: a memory system with a simplified read leveling operation.

EX1003, ¶288. Techniques for write and read leveling were well known at the time, EX1020, 26-27, 33, 42-45; *id.*, 31, 33, 48-54, and can be the claimed “operations” according to Patent Owner, EX1038, ¶48; EX1003, ¶287.

b) Second motivation: Tokuhiro provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays

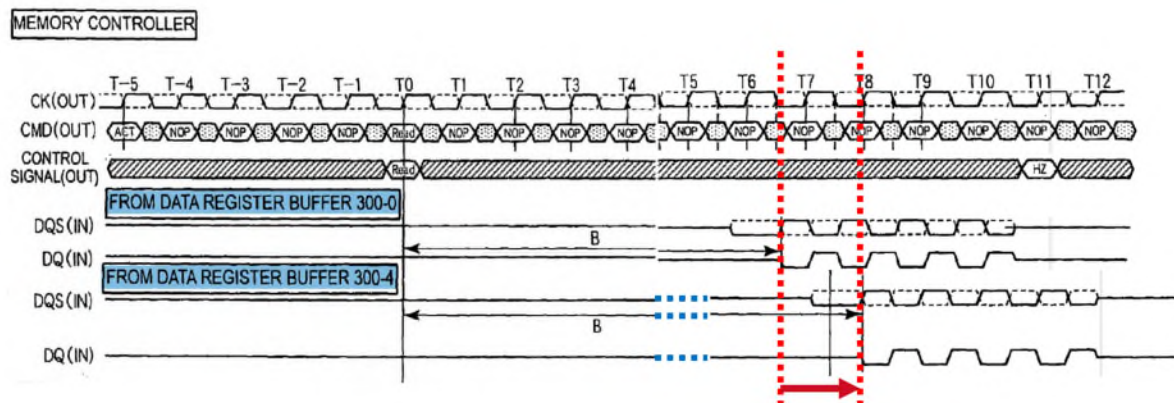
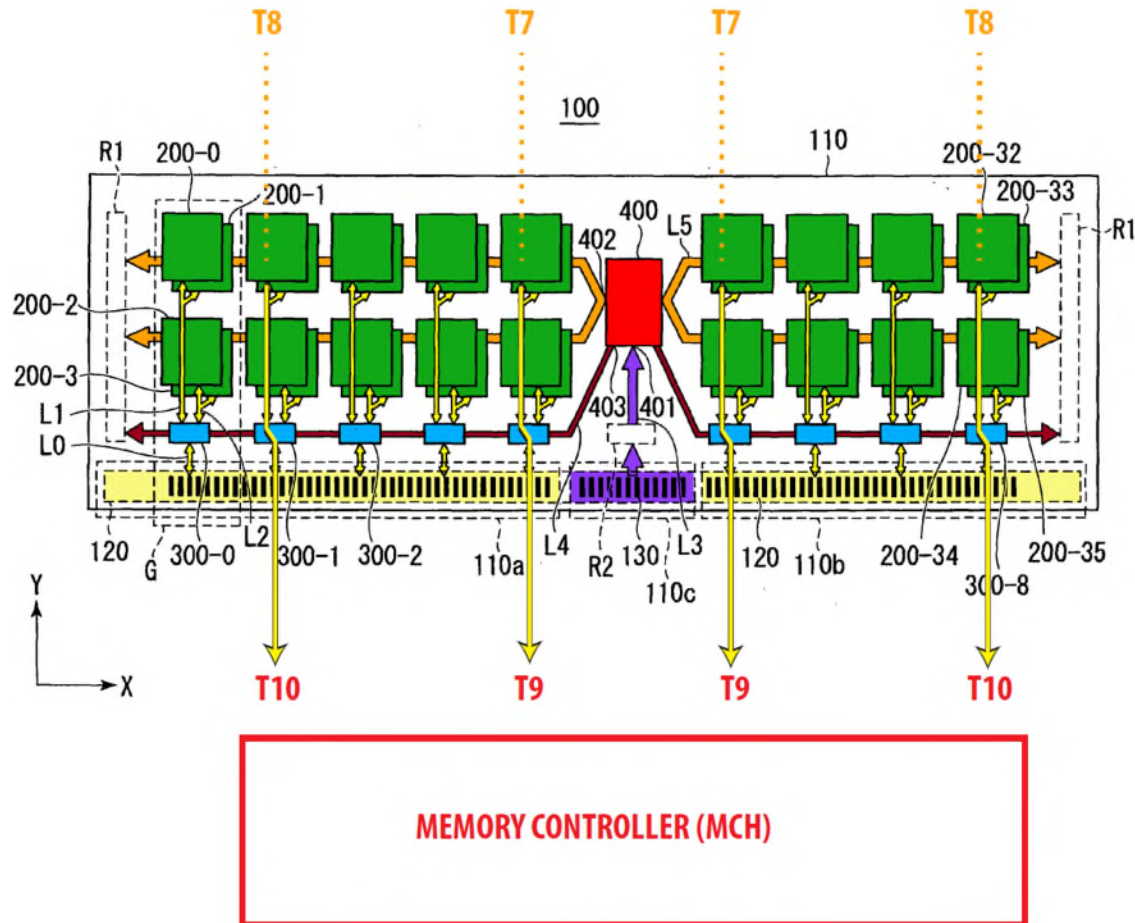
Hiraishi discloses both “S4” and “S5” read leveling. EX1003,¶289; EX1005,¶¶[0130],[0151],[0161],FIGS.15,17. Even after “S5” read leveling, however, the read data arrives at the memory controller from different data buffers with different “time B” delays, so Hiraishi’s memory controller must remove the fly-by delay (red arrow) between the different data buffers. EX1003,¶¶289-290; EX1005,FIG.17:



A POSITA would have understood that Tokuhiro’s “DR” delay circuits, which remove fly-by delays without the need for a special FIFO, could be used in connection with Hiraishi to compensate for the remaining fly-by delays, making the read data arrive at the memory controller from the different data buffers at substantially the same time. EX1006,18:66-19:7;EX1003,¶291. A POSITA would have thus been motivated to use Tokuhiro’s simple technique of using delay circuits DR with Hiraishi’s memory module. EX1003,¶¶291-292.

c) *Third motivation: Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not*

A POSITA would have understood that Hiraishi suffers from the same potential problem identified by Tokuhiro: fly-by delays that are greater than one clock cycle. EX1003,¶¶293-296;EX1005,FIG.1(Hiraishi's module annotated below to show times T7 to T10 from Tokuhiro Fig.11 where the delays T7 to T8, and T9 to T10, can be greater than one clock cycle),FIG.17(Hiraishi's timing modified below to show a fly-by delay greater than one clock-cycle); EX1006,FIG.11,2:54-59,3:9-12,3:16-26,18:15-48,18:43-53. Delays greater than one clock cycle were a known problem that had been solved with special FIFO circuitry. EX1024,5:26-31,6:56-7:2.



Hiraishi only shows fly-by delays less than one clock cycle, and it is silent about how to handle delays greater than one clock cycle (see modified Hiraishi's Fig.17 above). EX1003,¶297;EX1005,¶[0161],FIG.17. A POSITA would have

known about the problem of fly-by delays greater than one clock cycle, motivating her to look for solutions to get rid of such large fly-by delays of the read data, such as Tokuhiro's technique of using simple "DR" delay circuits. EX1003,¶¶297-299;EX1006,18:66-19:7.

3. The combination of Hiraishi in view of Tokuhiro relied upon here

a) It would have been obvious to implement Tokuhiro's delay elements in Hiraishi's data register buffers

It would have been obvious to a POSITA to implement Tokuhiro's delay elements in Hiraishi's data register buffers, and a POSITA would have had a reasonable expectation of success in doing so. EX1003,¶¶300-302. A POSITA would have understood from Tokuhiro's teaching that the delay elements DR1 and DR2 (purple, FIGS.5,6, below) can compensate for fly-by delays of read data (e.g., Dt2 in Fig.11 below) using the delays for write operations (e.g., Dt1 in Fig.7, below), even if the fly-by delay between two memory devices (e.g., SDRAM-1 and SDRAM-n), is larger than one clock cycle. EX1003,¶¶271-272,274,305-307;EX1006,18:66-19:7,3:9-26,FIGS.5-6,FIG.7(annotated),13:23-37,13:47-14:2,3:16-26,18:26-52,FIG.11(annotated). The memory devices in Hiraishi interface with the data register buffers, not directly with the memory controller (MCH). EX1003,¶305;EX1005,FIG.5. A POSITA would have understood that the delay elements of Tokuhiro can be implemented in either the data buffers or the

memory controller of Hiraishi—a finite number of predictable solutions to the same problem—rendering both of those solutions obvious. EX1003,¶309. And since Hiraishi already teaches read (and write) leveling circuitry in the data register buffers, a POSITA would have been motivated to implement the functionality of the delay elements (DR) of Tokuhiro in the data buffers of Hiraishi (as shown below). EX1003,¶305;EX1005,FIGS.5,2,13.

FIG. 7

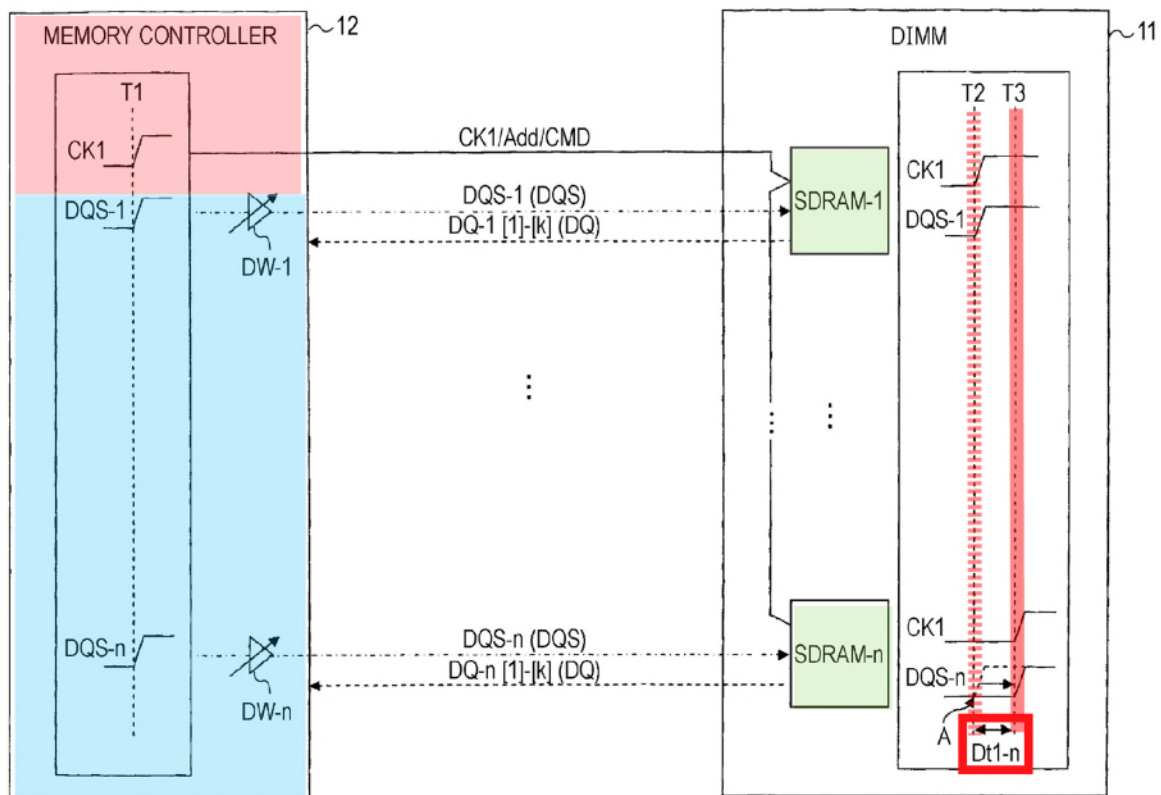
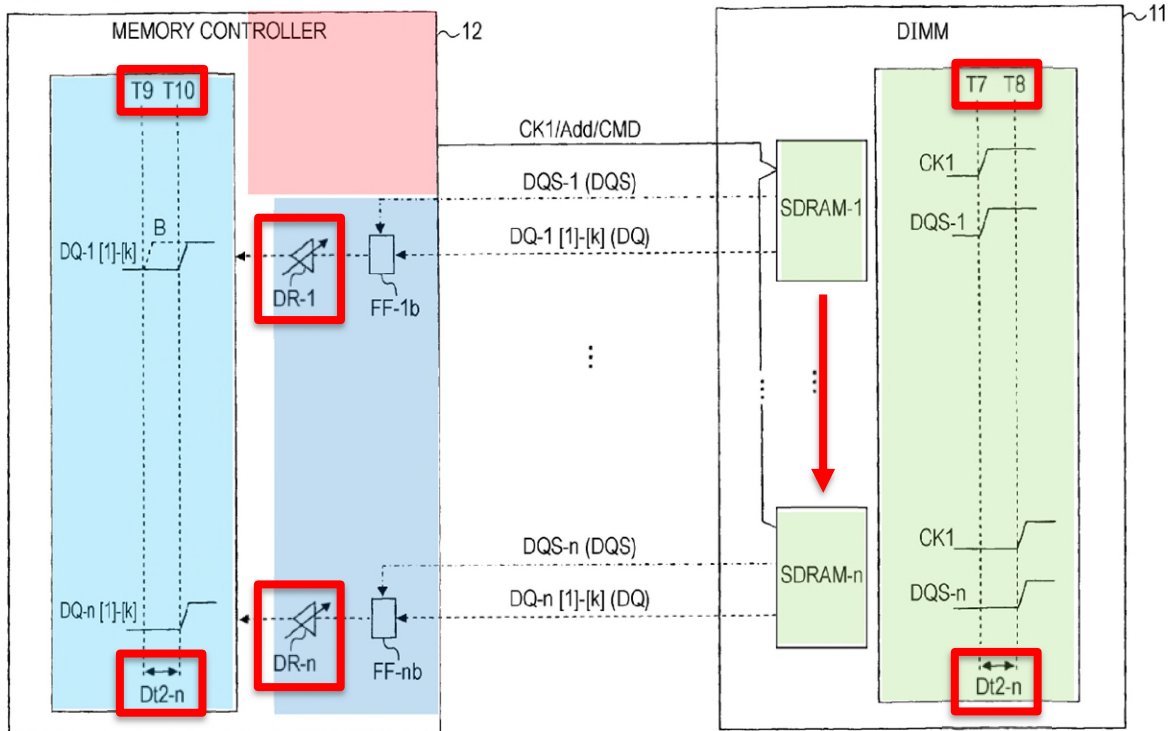


FIG. 11



Id.;EX1006,FIG. 11.

FIG. 5

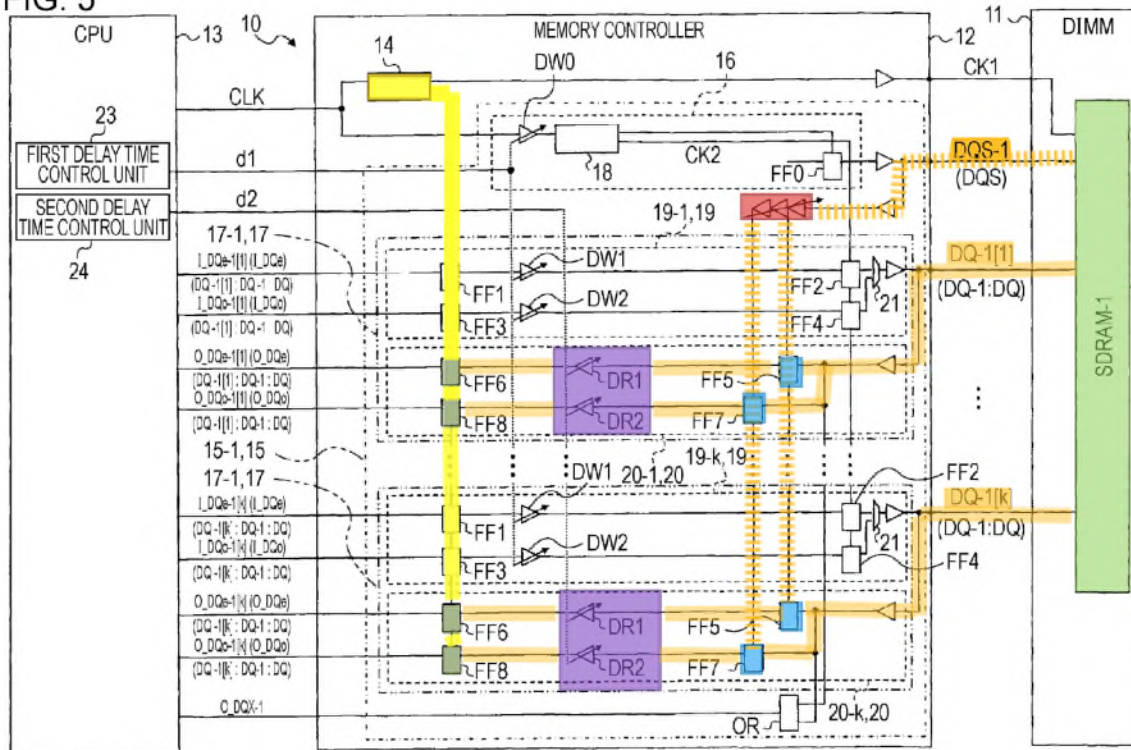
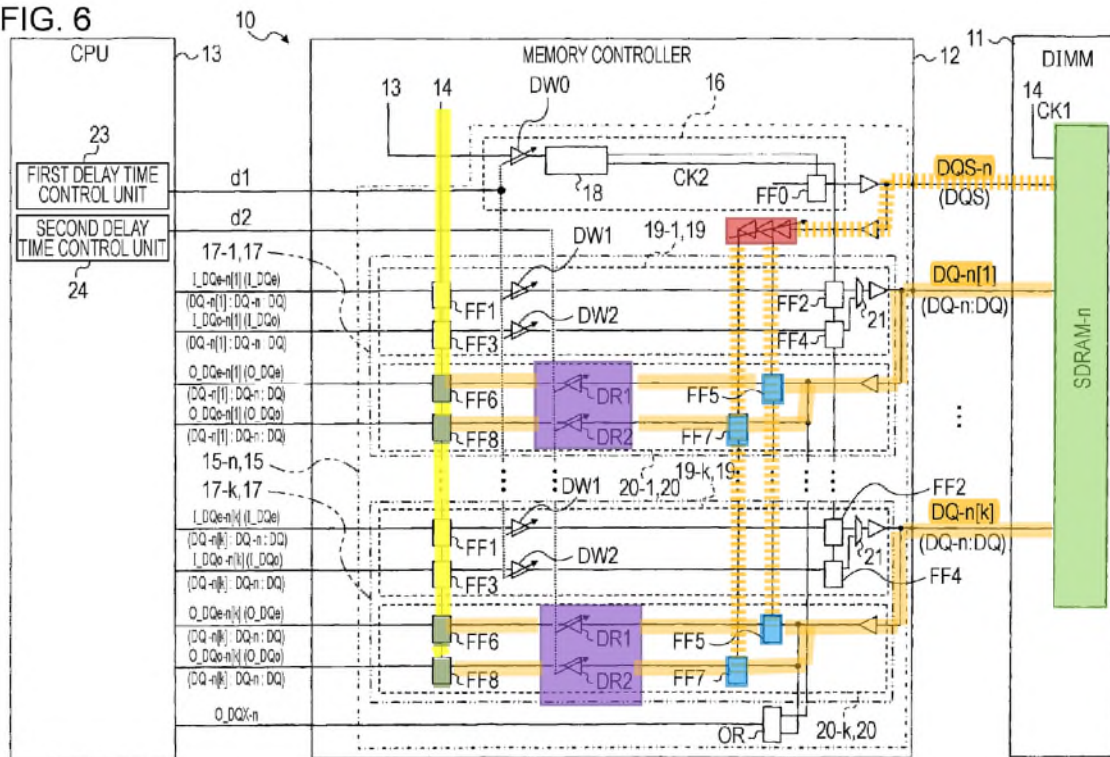


FIG. 6

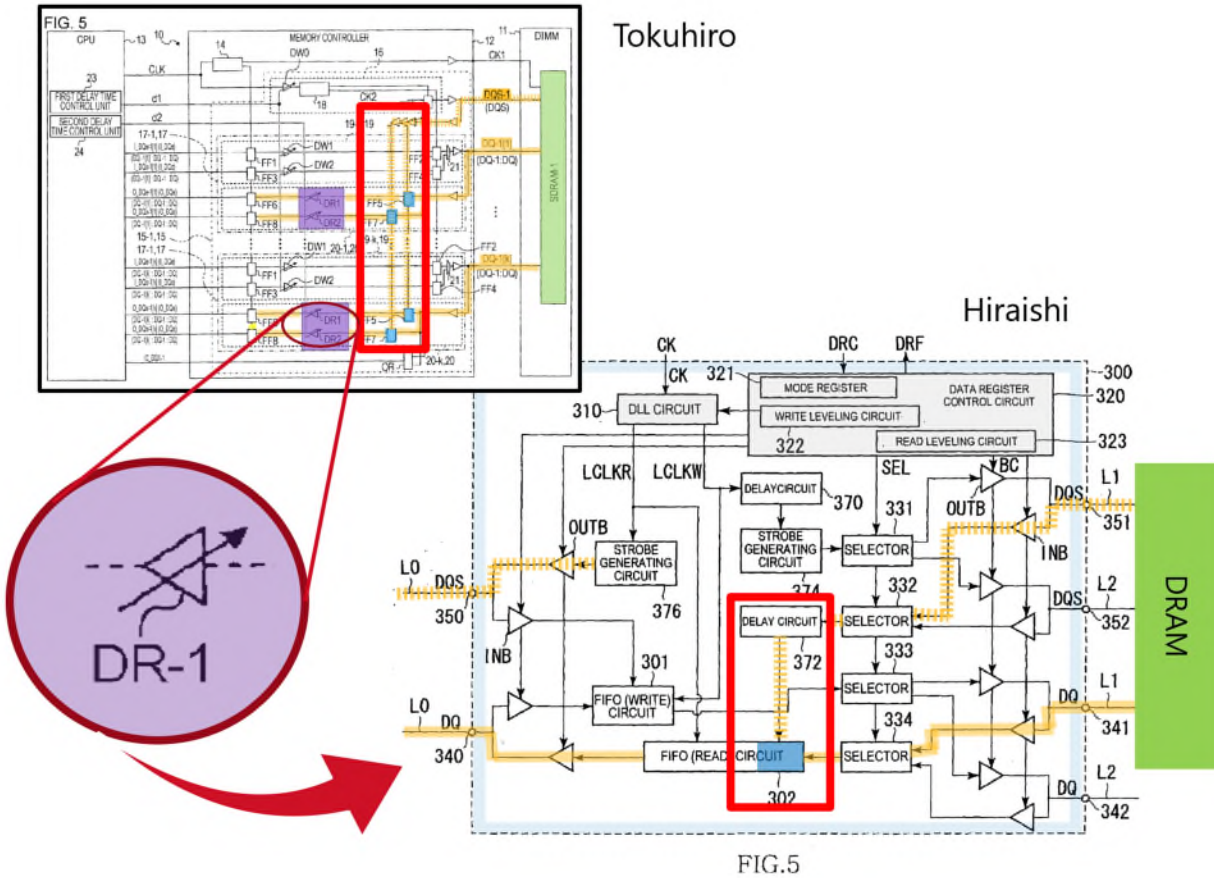


EX1003,¶276;EX1006,10:63-12:5,FIGS.5-6(annotated).

Tokuhiro teaches to apply the read delay (e.g., DR-1, purple) immediately after the corresponding read data from the memory (e.g., SDRAM-1, green) has been latched (e.g., by flip-flop FF5, blue, in red box, below), as illustrated in an annotated version of Tokuhiro's Figure 5 below (upper left). EX1003,¶302.

Hiraishi teaches that the read data from the memory (DRAM, green added) is latched into FIFO (Read) Circuit 302 (blue, in red box, below).

Id.;EX1005,FIG.5(reproduced below, lower right, with annotations). Accordingly, a POSITA would have been motivated to add Tokuhiro's read delay elements (e.g., DR-1) to Hiraishi's data register buffer immediately after the read data from the memory is latched (red box), as shown below. EX1003,¶302.



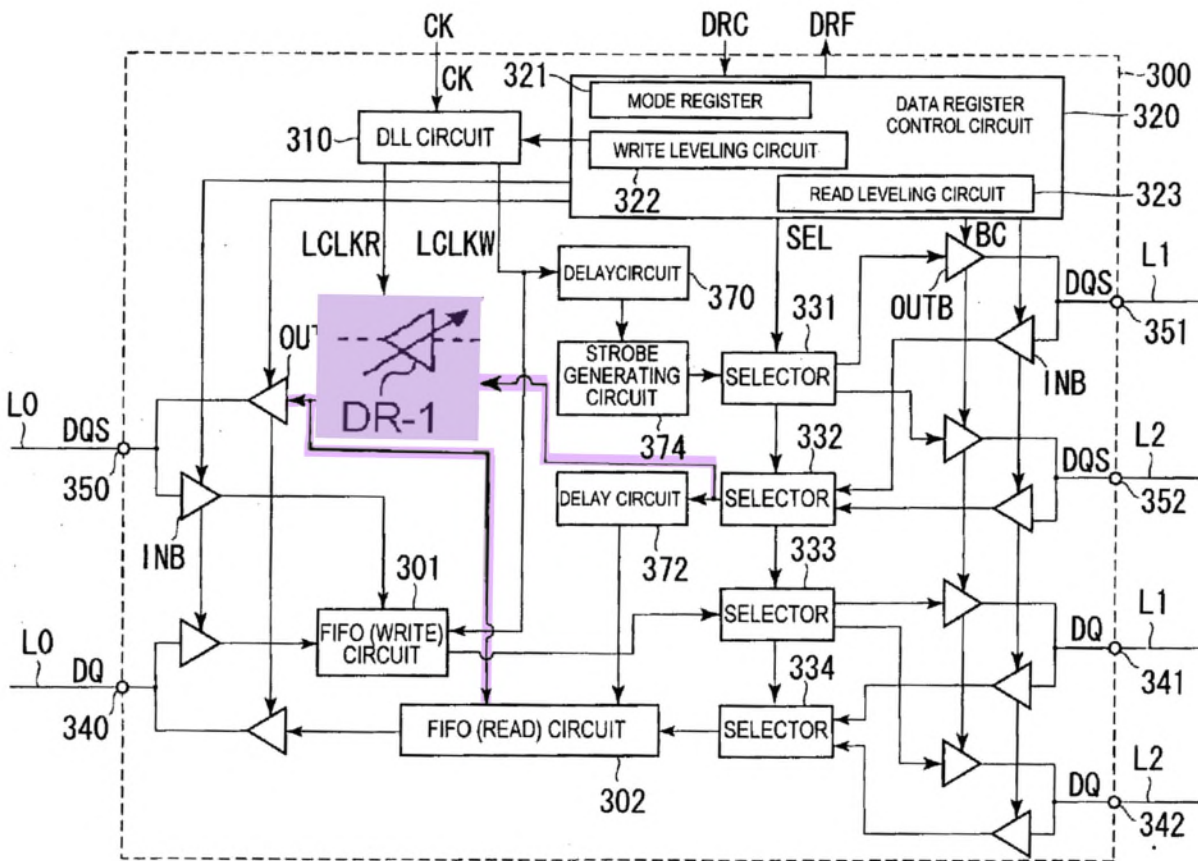
EX1003, ¶302.

In this combination, a POSITA would have understood that in a read operation the data signal (DQ, 340) is transmitted from the data buffer to the memory controller with a corresponding strobe signal (DQS, 350) which is in sync with the data signal, and thus the strobe and data signals have to be in sync after Tokuhiro's read delay has been added to Hiraishi's data buffer.

EX1003, ¶303; EX1005, FIG. 5. Delaying both data and strobe signals were well known in the art, and disclosed by Tokuhiro for write operations.

Id.; EX1006, FIGS. 5-6, 9:33-40. A POSITA would have understood that the same

functionality could be implemented in the data buffer of Hiraishi to delay the transmission of read data along with its strobe signal to the memory controller, such as illustrated in Hiraishi's Figure 5 (modified to show the combination with Tokuhiro) below:

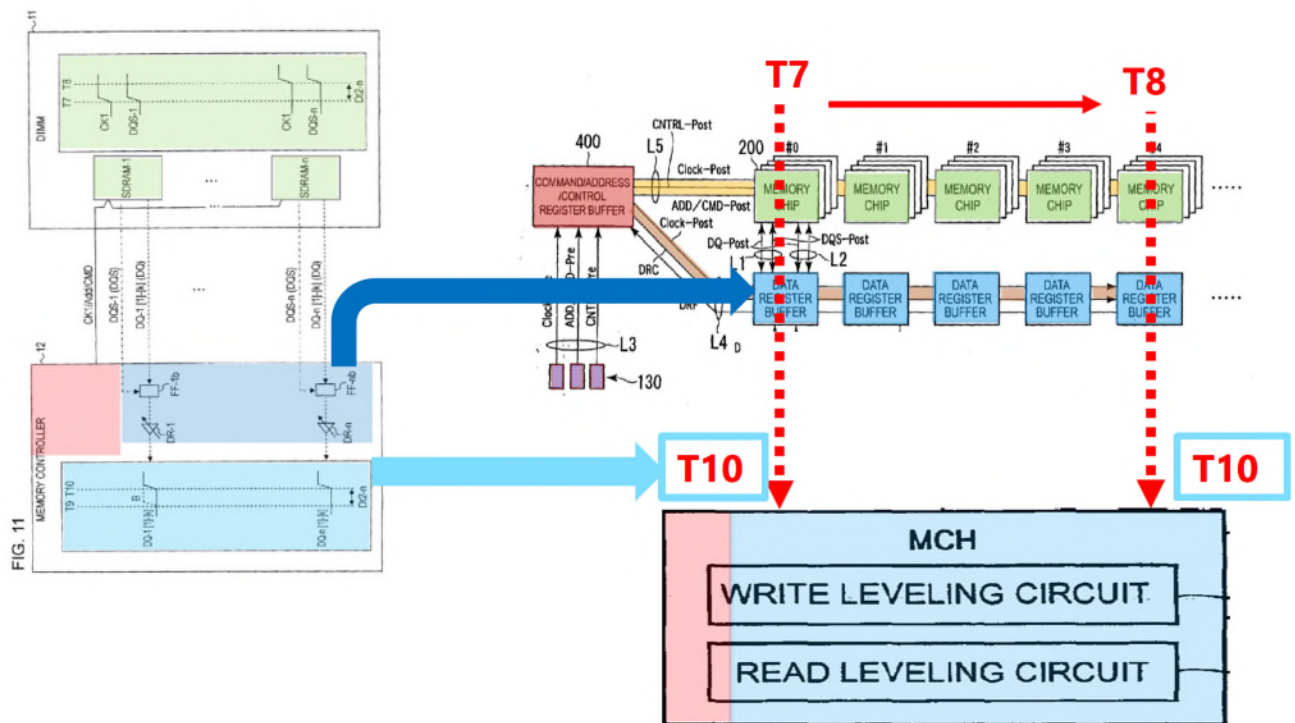


EX1003, ¶303.

In this combination, Tokuhiro's read delay circuit (DR-1, purple) is added to Hiraishi's data buffer to remove the large fly-by delays, while the existing delay circuit 372 continues to make fine timing adjustments to the phase of the incoming

strobe DQS as before to properly latch the incoming data DQ. Based on Tokuhiro's teachings, the added read delay circuit DR-1 is configured to delay the read data strobe signal DQS (purple, received from selector 332, purple) and to use the delayed strobe to clock out data from FIFO (Read) Circuit 302 so that the delayed data DQ from the Read FIFO is in sync with the delayed strobe.

EX1003,¶304;EX1020,p.56;EX1006,18:53-64. Alternatively, delay elements similar to Tokuhiro's DR elements could be used instead of (or in addition to) Hiraishi's FIFO circuit for delaying the read data. EX1003,¶304.



As illustrated above in Tokuhiro's Figure 11 (left above) and Hiraishi's Figure 7 (right above), the combination advantageously implements the functionality of the additional read delay of Tokuhiro in the data register buffers of

Hiraishi (as illustrated by the dark blue arrow). EX1003,¶306. As a result of these additional read delays, the read data arrives to the memory controller (MCH) at substantially the same time (T10) despite the fly-by delay (from T7 to T8) on the memory module, so the read data from all memories can be captured in a single clock cycle, even if the fly-by delays on the module are larger than one clock cycle. *Id.* A POSITA would have understood that this combination avoids the memory controller having to manage large fly-by delays of read data during either the training or normal operation, thus requiring less circuitry and functionality for implementation, such as extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles. EX1003,¶307. Another advantage is that large fly-by delays are removed on the module at the first practically available location (the data buffers, since JEDEC-compliant memory devices would not have such delay elements), preventing the rest of the system from having to manage those large fly-by delays. EX1003,¶308; EX1006,2:45-59.

b) It would have been obvious for either Hiraishi's memory controller or module controller to program Tokuhiro's delay elements in Hiraishi's data buffers

A POSITA would have understood that there are two potential ways to implement Tokuhiro's technique of adding read delay elements to Hiraishi's data buffer to solve the problem of large fly-by delays: (1) the **system memory controller** could determine the read delays based on the timing for a write

operation *during* write leveling and program the read delay elements in the data buffers accordingly, or (2) the **module controller** could determine the read delays based on the delays measured by the data buffers during a write operation *before* write leveling (when the memory controller issues a write command to the memory module) and program the read delay elements in the data buffers accordingly. EX1003, ¶¶310-311; EX1006, 16:18 (Formula 3-6 for calculating the read delays from the write delays, including the maximum of those write delays). Either way, the result is that the memory controller does not have to manage large fly-by delays when trying to capture the read data. EX1003, ¶311. These two alternatives are discussed below.

(1) *First implementation of the combination (system memory controller determines the read delay)*

A POSITA would have understood that the system memory controller in Hiraishi can determine the fly-by delays on the module during write leveling as taught by Tokuhiro. EX1003, ¶¶273-274, 312; EX1006, FIG. 7. Tokuhiro explains that these Dt1 delay times obtained from write leveling are used to set the delays Dt2 for the read data. EX1003, ¶¶275-277, 312; EX1006, 16:43-46, Figs. 7, 11. Thus, in this implementation of the combination, a POSITA would implement Tokuhiro's calculation of the fly-by delays based on write leveling in Hiraishi's system memory controller and, based on these fly-by delays, the system memory controller would program the additional read delay elements in the data buffers.

EX1003,¶313. A POSITA would implement Hiraishi's "S5" leveling operations (between the system memory controller and the data buffers) so that the system memory controller performs write leveling, then programs the read delay elements in the data buffers (based on the write delays) to remove fly-by delays, and then performs any necessary read leveling (without fly-by delays) for any fine tuning of DQ/DQS alignment. *Id.*; EX1005,¶¶[0091],[0141],[0161],[0163], FIG.13(below with annotations in accordance with the first implementation of the Hiraishi-Tokuhiro combination).

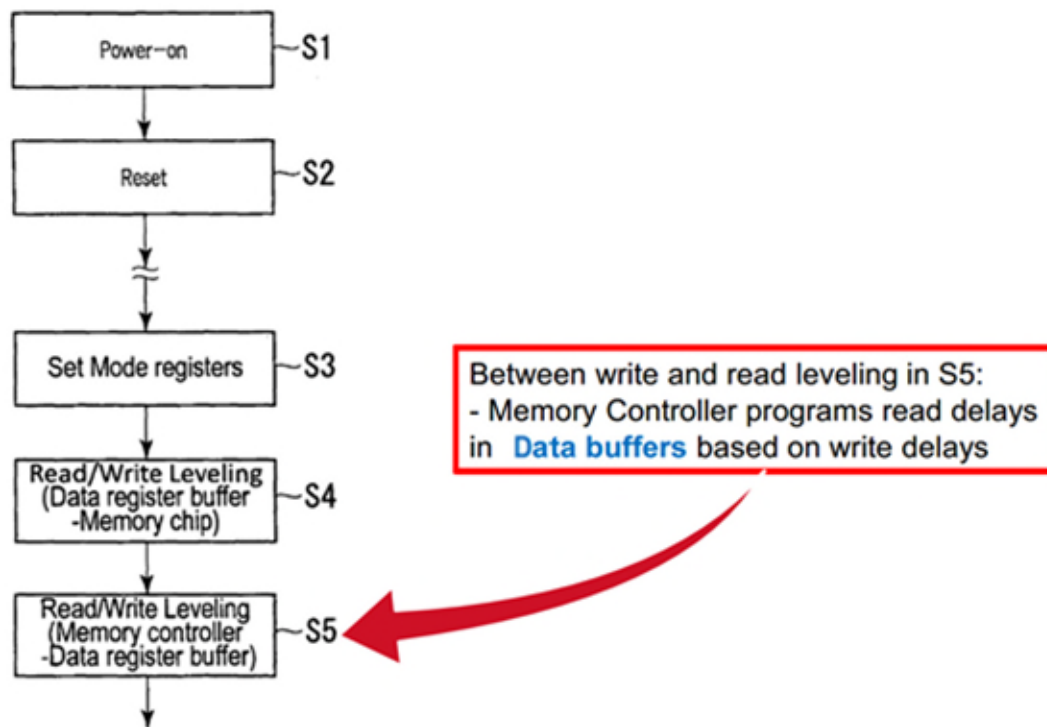


FIG.13

As taught by Tokuhiro, the result of this is the read data arriving at the memory controller without substantial fly-by delays, thus simplifying the memory controller's job and circuitry for properly capturing the read data.

Id.; EX1003, ¶313.

This implementation was well within the level of ordinary skill and provided nothing more than what was expected from the combination. EX1003, ¶314. For example, implementing Tokuhiro's read delay functionality in Hiraishi's data buffers comprises adding a known function (delaying the read data as taught by Tokuhiro) to a known data buffer of Hiraishi, where the data buffer already had similar functionalities, including read and write leveling functions. *Id.* Similarly, since Tokuhiro taught how to calculate and set those read delays, a POSITA would have understood how to modify Hiraishi's system memory controller to add the same functionalities. *Id.* The result of the combination is as expected: a memory system in which the system memory controller does not have to manage large delays, in particular larger than one clock cycle, when trying to capture the correct values of read data. *Id.*

**(2) *Second implementation of the combination
(module controller determines the read delay)***

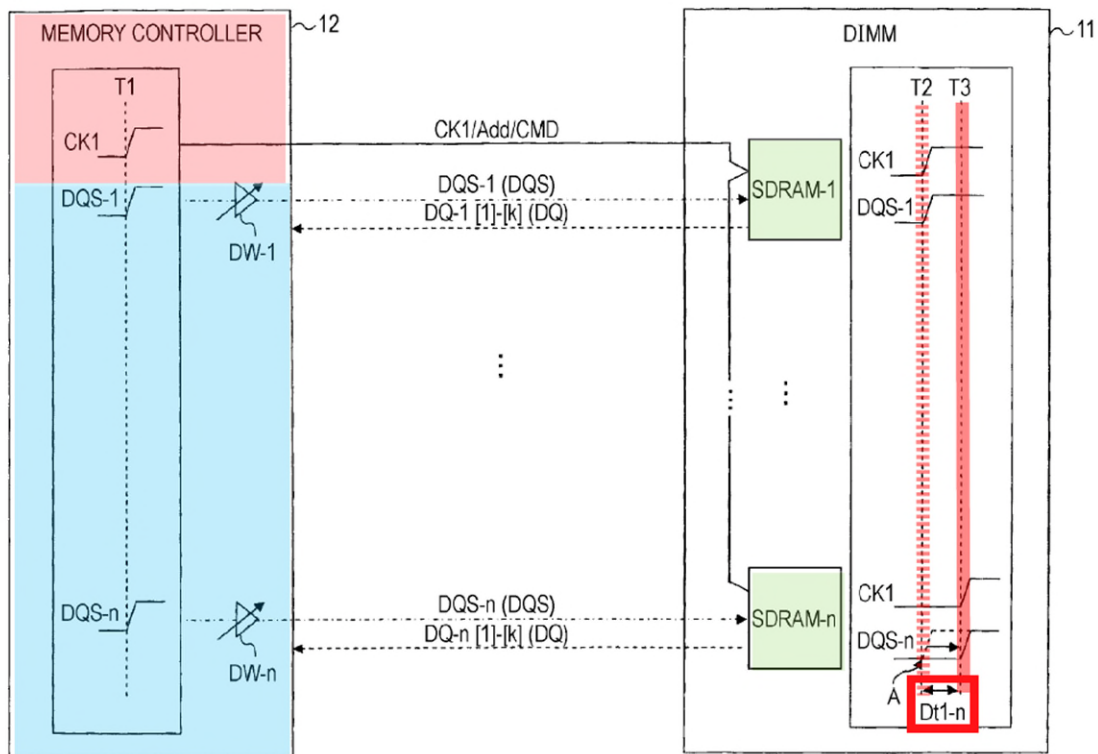
Additionally, a POSITA would have understood (and had a reasonable expectation of success) that Tokuhiro's technique can also be implemented in Hiraishi's memory module such that the ***data buffer circuits*** measure timing

information to determine the fly-by delays during a write operation, and Hiraishi's **module controller** programs the corresponding read delays in the data buffers.

EX1003,¶315.

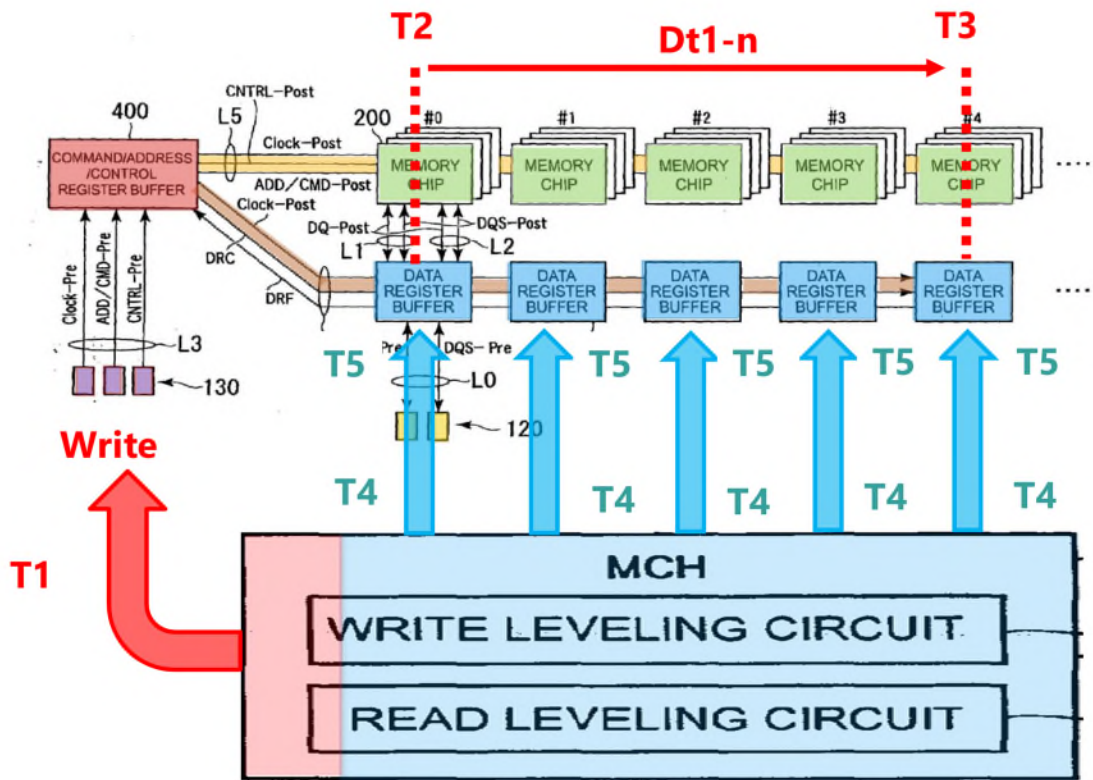
A POSITA would have been motivated to implement Tokuhiro's technique in Hiraishi's module, as opposed to the memory controller, because Hiraishi teaches that functionalities of the memory controller—including interfacing with the memory chips and performing read and write leveling—can be performed by the module controller and data buffers. EX1003,¶316;EX1005,FIG.5,¶[0151]. Tokuhiro explains that, before the write leveling, the write strobe signals arrive to the module at substantially the same time (T2), but the corresponding clock/address/command signals have respective fly-by delays in the chain (such as a delay Dt_{1-n} for the n-th device). EX1006,FIG.7(reproduced below with annotations),FIG.10,13:30-37.

FIG. 7



Accordingly, a POSITA would have been motivated to use Hiraishi's time measuring technique in the data buffer to determine the fly-by delays during a *write* operation and set the *read* delays as taught by Tokuhiro and shown below.

EX1003, ¶¶316-317; EX1006, FIGS. 7, 10; EX1005, FIG. 7 (annotated version reproduced below).



In this implementation, the write command arrives at each data buffer with respective fly-by delays ($Dt1$) dependent on the distance from the module controller. EX1003, ¶318. The write data (blue arrows), however, would arrive at each data buffer substantially at the same time $T5$, since the write leveling delays have not yet been applied by the memory controller. Thus, each data buffer can measure the time difference between when the write command is received (between $T2$ and $T3$, depending on the buffer) and when the data arrives ($T5$). *Id.*

A POSITA would have understood that those time differences for a write operation can be measured using the same technique that Hiraishi's data buffer already uses to determine a time delay between receiving a read command and the

arrival of the corresponding read data. EX1003,¶319;EX1005,¶[0151],FIG.15.

Thus, a POSITA would have understood that the functionality of measuring the time difference between receipt of a read command and arrival of corresponding read data can also be implemented to measure the time difference between receipt of a write command and arrival of corresponding write data. EX1003,¶319.

Accordingly, a POSITA would have been motivated to use Hiraishi's time measuring technique to measure a time interval between the arrival of a write command (e.g., T3) and the respective strobe signal (DQS) travelling with the corresponding write data (DQ) (e.g., T5) to determine the corresponding fly-by delays (e.g., Dt1-n). *Id.*

A POSITA would have understood that Hiraishi's memory buffers can use the feed-back channel DRF to communicate the measured time intervals to the module controller which can then use those time intervals to determine the corresponding fly-by delays for a read operation as taught by Tokuhiro, and program the read delay elements in the data buffers for transmitting the read data accordingly. EX1003,¶320;EX1005,¶¶[0089],[0099].

In this implementation, Tokuhiro's read delay functionality is added to the data buffers of Hiraishi's module such that, advantageously, no changes to the circuitry of the system memory controller are necessary. EX1003,¶321.

Furthermore, Tokuhiro's functionality of determining the fly-by delays from

delays for the write operations and setting the additional read delays accordingly is implemented in Hiraishi's memory module, as shown in modified Figure 13 below.

Id.

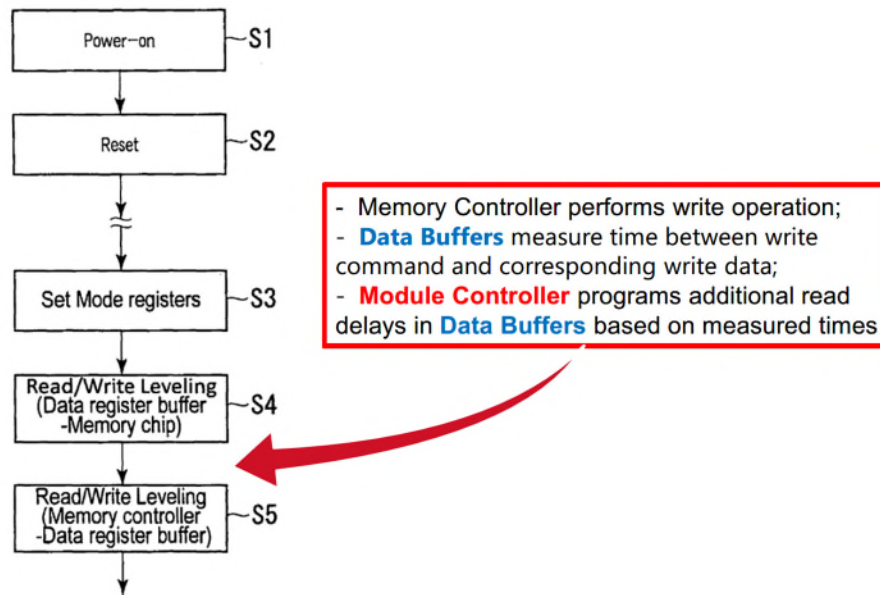


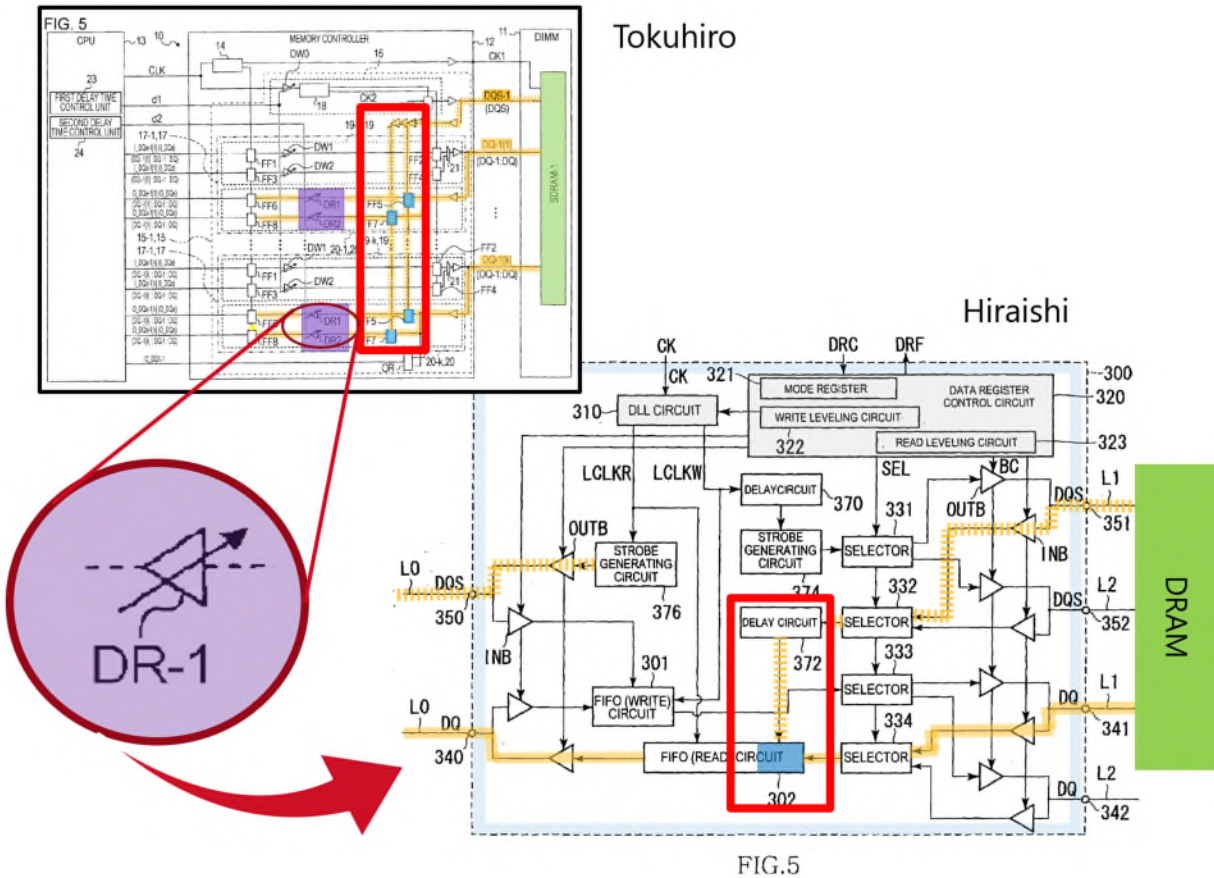
FIG.13

EX1003, ¶321; EX1005, FIG.13 (annotated according to the Hiraishi and Tokuhiro combination's second implementation).

4. Claim 1

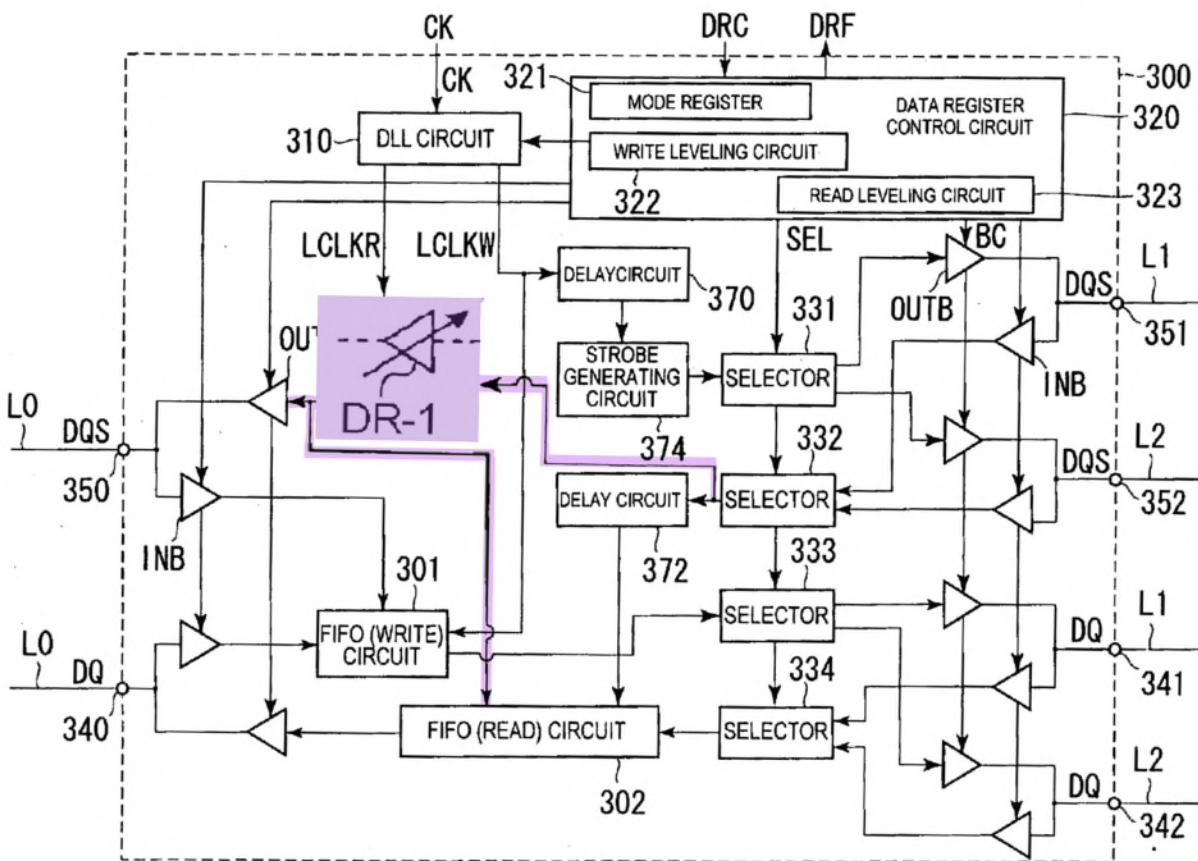
Claim limitations 1[pre] through 1[e], 1[g], and 1[h] are disclosed by Hiraishi alone or with Butt as explained in Ground 1. *Supra*, §§VI.A.1.a)-g), i)-j), pp.21-35, 36-39. Claim limitations 1[f] and 1[i] are met by the combination of

Hiraishi and Tokuhiro as explained below.



a) $1/f$ Delay First Read Strobe

Hiraishi combined with Tokuhiro includes a delay element DR-1 added to Hiraishi's data buffer circuits, which would delay the strobe signal from selector 332 and provide that delayed strobe signal to FIFO (Read) Circuit 302 (and to the output 350). *Supra*, §VI.D.3, pp.103-119; EX1003, ¶323.



Therefore, the modified data buffer 300-0 would be configured to “*delay the first read strobe* [e.g., DQS from selector 332 to purple delay element DR-1, as taught by Tokuhiro] *a first predetermined amount* [e.g., the amount calculated as taught by Tokuhiro to remove fly-by delays] *to generate a first delayed read strobe* [e.g., sent to FIFO (Read) Circuit 302].” EX1003, ¶323.

b) 1[i] First Predetermined Amount

In Hiraishi, as modified by Tokuhiro, the delay introduced by DR-1 for the read operation would be based on a write operation. EX1003, ¶324; EX1006, 18:53-63. The write operation used to set the delay time as taught by Tokuhiro would

include the data buffer receiving signals, such as data strobe signals. *Id.*,2:13-18. Thus, in either implementation of the Hiraishi/Tokuhiro combination discussed above, pp.111-119, the modified data buffer 300-0 would thus disclose “*wherein the first predetermined amount* [e.g., applied by added delay elements DR-1] *is determined based at least on signals* [e.g., data strobe signal DQS from the earlier write operation] *received by the first data buffer during one or more previous operations* [e.g., the earlier write operation as discussed above, *supra*,§VI.D.3,pp.103-119].” EX1003,¶325.

5. Claim 2

Claim limitations 2[a], 2[b], 2[d], and 2[e] are disclosed by Hiraishi alone or with Butt, as explained above. *Supra*, §§VI.A.2.a)-b),d)-e),pp.48-51,51-53. Claim limitations 2[c] and 2[f] are satisfied by the combination of Hiraishi and Tokuhiro, as explained below.

a) 2[c]: Delay Second Read Strobe

Hiraishi, as modified by Tokuhiro, discloses this limitation involving the “*second data buffer*” in the same manner as for the analogous operation for the “*first data buffer*” described in 1[f]. *Supra*,§VI.D.4.a),pp.120-121;EX1003,¶327.

b) 2[f]: Second Predetermined Amount

Hiraishi, as modified by Tokuhiro, discloses the “*second predetermined amount*” [e.g., the amount of delay imposed by data buffer 300-8] can be

determined in a manner similar to the analogous “*first predetermined amount*” in 1[i]. *Supra*, §VI.D.4.b), pp.121-122; EX1003, ¶328.

6. Claim 4

a) 4[a]: Signals Received by First Data Buffer

Hiraishi in combination with Tokuhiro disclose “*the signals received by the first data buffer [300-0] during one or more previous operations [e.g., the earlier write operation] include at least a strobe signal associated with a previous operation [e.g., data strobe signal DQS corresponding to memory device 200-0],*” as explained for 1[i]. *Supra*, §VI.D.4.b), p.121; EX1003, ¶333.

b) 4[b] Signals Received by Second Data Buffer

Hiraishi, in combination with Tokuhiro, discloses the “*second data buffer [data buffer 300-8]*” would receive a strobe signal corresponding to memory device 200-32 in the same manner as described for the analogous determination for the “*first data buffer,*” as described for 4[a]. *Supra*, §VI.D.6.a), p.123; EX1003, ¶334.

7. Claim 6

For the same reasons stated for claim 4[a], Hiraishi in combination with Tokuhiro discloses or renders obvious claim 6. *Supra*, §VI.D.6.a), p.123; EX1003, ¶335.

8. Claim 7

For the same reasons described in Ground 1, Hiraishi and Butt with Tokuhiro discloses or renders obvious claim 7. *Supra*,§VI.A.5,pp.54-60;EX1003,¶342.

9. Claim 11

As explained for the “second” implementation of the combination, it would have been obvious to calculate the amount of delay (as taught by Tokuhiro) in the data buffer 300 of Hiraishi. *Supra*,§VI.D.3.b)(2),pp.114-119. Thus, in this implementation, “*the first data buffer [e.g., 300-0] includes circuitry [e.g., in data register control circuit 320] that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.*” EX1003,¶336.

10. Claim 13

For the same reasons described in Ground 1, Hiraishi and Butt with Tokuhiro discloses or renders obvious claim 13. *Supra*,§VI.A.7,p.61;EX1003,¶342.

11. Claim 14

Claim limitations 14[pre] through 14[i], 14[k], and 14[l] are disclosed by Hiraishi and Butt with Tokuhiro for the same reasons described in Ground 1. *Supra*,§VI.A.8.a)-l),n)-o),pp.61-63,64-64. Claim limitations 14[j] and 14[m] are

disclosed by the combination of Hiraishi and Tokuhiro for the same reasons as for 1[f] and 1[i]. *Supra*, §§VI.D.4.a)-b), pp.120-122; EX1003, ¶337.

12. Claim 15

Claim limitations 15[a] through 15[c], 15[e], and 15[f] are disclosed by Hiraishi and Butt with Tokuhiro for the same reasons described in Ground 1. *Supra*, §§VI.A.9.a)-c), e)-f), pp.64-64, 65-65. Claim limitations 15[d] and 15[g] are disclosed by the combination of Hiraishi and Tokuhiro for the same reasons as for 2[c] and 2[f]. *Supra*, §§VI.D.5.a)-b), pp.122-123; EX1003, ¶338.

13. Claim 17

a) 17[a]: Signals Received by First Data Buffer

Hiraishi alone or with Tokuhiro discloses 17[a] for the same reasons as 4[a]. *Supra*, §VI.D.6.a), p.123; EX1003, ¶340.

b) 17[b]: Signals Received by Second Data Buffer

Hiraishi alone or with Tokuhiro disclose 17[b] for the same reasons as 4[b]. *Supra*, §VI.D.6.b), p.123; EX1003, ¶341.

14. Claim 18

For the same reasons described in Ground 1, Hiraishi and Butt with Tokuhiro discloses or renders obvious claim 18. *Supra*, §VI.A.11, pp.66-68; EX1003, ¶342.

E. Ground 5: Claims 3,5,12,16 are Obvious Over Hiraishi and Butt in view of Tokuhiro and Ellsberry

1. Claim 3

As described in Ground 2, claim limitations 3[a], 3[b], 3[c], 3[e], and 3[f] are disclosed by Hiraishi and Butt alone or in view of Ellsberry.

Supra, §§VI.B.1.a)-c),e)-f),pp.70-74,74-77. Claim limitations 3[d] and 3[g] are disclosed by Hiraishi with Tokuhiro for the reasons below.

a) 3[d]: Delay Third Read Strobe

Hiraishi with Tokuhiro and in further view of Ellsberry discloses the “*first data buffer*” [e.g., 300-0] can “*delay the third read strobe by a third predetermined amount to generate a third delayed read strobe*” in the same manner as for the analogous operation for the “*first read strobe*” in 1[f]. *See*,§VI.D.4.a),pp.120-121;EX1003,¶330.

b) 3[g]: Third Predetermined Amount

Hiraishi with Tokuhiro and in further view of Ellsberry discloses the “*third predetermined amount*” [e.g., the amount of delay for the upper nibble of the byte in rank 0 connected to data buffer 300-0] can be determined in a manner similar to the analogous “*first predetermined amount*” in 1[i]. *Supra*,§VI.D.4.b),pp.121-122;EX1003,¶331.

2. Claims 5,12

Hiraishi and Butt with Tokuhiro and in further view of Ellsberry discloses claims 5 and 12 for the same reasons discussed in Ground 2. *Supra*, §§VI.B.2-3, p.77; EX1003, ¶342.

3. Claim 16

Claim limitations 16[a], 16[b], 16[d] and 16[e] are disclosed by Hiraishi and Butt in further view of Ellsberry as explained in Ground 2. *Supra*, §§VI.B.4.a)-b), d)-e), pp.78-78. Claim elements 16[c] and 16[f] are also met by the combination of Hiraishi and Tokuhiro, in further view of Ellsberry, for the same reasons as for 3[d] and 3[g]. *Supra*, §§VI.E.1.a)-b), pp.126-126; EX1003, ¶339.

F. Ground 6: Claims 8-10 and 19-20 are Obvious Over Hiraishi and Butt in view of Tokuhiro and Kim

Hiraishi with Butt in view of Tokuhiro and/or Kim renders obvious claims 8-10 and 19-20 for the same reasons discussed in Ground 3. *Supra*, §VI.C, pp.79-93; EX1003, ¶342.

VII. 35 U.S.C. §314(a)

The *Fintiv* factors do not support denying institution. There are two cases currently pending between the parties that involve the '506 Patent: a declaratory judgment action filed by Petitioner in the District of Delaware (EX1035, EX1036), and an action filed by Patent Owner in the Eastern District of Texas (EX1038). Both of these cases are in their infancy; neither party has answered the other

party's complaint yet. EX1037;EX1040. Thus, there currently is no trial date in either case (factor 2), nor has any discovery taken place (factor 3). Invalidity is currently not even at issue in either case, and at present it is unclear if or when invalidity will become an issue (factor 6). In any event, given that both cases are still in the pleading stages, the Final Written Decision here likely would occur before any invalidity decision in either district court (factor 2), regardless of any potential stay in district court (factor 1).

VIII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-20 be canceled as unpatentable.

Dated: March 22, 2022

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,964 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 22nd day of March, 2022, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by FedEx Express on the following counsel of record for patent owner:

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