

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS,  
INC.; and MICRON TECHNOLOGY TEXAS LLC,  
Petitioner,

v.

NETLIST, INC.,  
Patent Owner.

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Case No. IPR2022-00237  
U.S. Patent No. 10,268,608

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**PETITIONER'S REQUEST FOR REHEARING  
OF DECISION DENYING INSTITUTION**

## TABLE OF CONTENTS

|                                                                                                                                     | Page |
|-------------------------------------------------------------------------------------------------------------------------------------|------|
| I. Introduction .....                                                                                                               | 1    |
| II. Argument.....                                                                                                                   | 2    |
| A. The Board Correctly Understood How Petitioner Explained That Osanai Discloses Claim Elements Associated With the Data Path. .... | 2    |
| B. The Decision Overlooked the Petition’s Explanation of How a Data Path Is Controlled and Its Evidence.....                        | 4    |
| C. Conclusion .....                                                                                                                 | 12   |

## **TABLE OF AUTHORITIES**

**Page(s)**

### **Cases**

|                                                                                     |   |
|-------------------------------------------------------------------------------------|---|
| <i>Ultratec, Inc. v. CaptionCall, LLC</i> ,<br>872 F.3d 1267 (Fed. Cir. 2017) ..... | 2 |
|-------------------------------------------------------------------------------------|---|

### **Other Authorities**

|                                |   |
|--------------------------------|---|
| 37 C.F.R § 42.71 (c)–(d) ..... | 2 |
|--------------------------------|---|

## I. Introduction

In its Decision Denying Institution (Paper No. 15), the Board concluded that Petitioner did not demonstrate how Osanai (Ex. 1005) discloses the following limitation: a “*data path*” that “*includes . . . the delay circuit.*” See Decision (“Dec.”) at 18–19. The Board recognized that Petitioner relied on Osanai’s write leveling circuitry 322 and read leveling circuitry 323 as disclosing the recited “*delay circuit.*” See Dec. at 19, n.2. But the Board determined that Petitioner did not show how “the write and read leveling circuitry are included in any one of the paths that are relied upon by petitioner.” Dec. at 19. In doing so, the Decision overlooked the Petition’s explanation of how the “*data paths*” are controlled and its supporting evidence, which show that the data paths include the delay circuit.

Without mentioning that explanation, the Board’s Decision focused primarily on the Petition’s explanation of how Osanai discloses disputed limitation 1[j]: “*a delay circuit configured to delay a signal through the data path . . .*” The preceding limitation, limitation 1[i], focuses on the claimed “*data path*” by reciting “*a command processing circuit configured to . . . control the data path.*” In addressing this limitation, the Petition explained how Osanai’s register buffer circuit 300 selects a read or write data path, identifies the components each of these data paths, and, most importantly, how these two data paths use one of two local clocks (i.e., LCLKR and LCLKW) that originate from write leveling circuitry 322 and read leveling

circuitry 323 as a delay circuit included in the data path. *See* Pet. 38–40. The Board, however, overlooked this explanation in its discussion about the disputed limitation. Consequently, the Board overlooked the Petition’s explanation describing how Osanai discloses “*data paths*” and concluded erroneously that the Petition did not describe how Osanai’s data paths include the write and read leveling circuitry, each satisfying the recited delay circuit.

## **II. Argument**

A request for rehearing must specifically identify the matters that the Board “misapprehended or overlooked,” and the panel reviews its decision for abuse of discretion. 37 C.F.R. § 42.71 (c)–(d). The Board abuses its discretion where its decision “(1) is clearly unreasonable, arbitrary, or fanciful; (2) is based on an erroneous conclusion of law; (3) rests on clearly erroneous fact findings; or (4) involves a record that contains no evidence on which the Board could rationally base its decision.” *Ultratec, Inc. v. CaptionCall, LLC*, 872 F.3d 1267, 1272 (Fed. Cir. 2017).

### **A. The Board Correctly Understood How Petitioner Explained That Osanai Discloses Claim Elements Associated With the Data Path.**

The Board’s Decision noted that claim 1 requires that the “data path include two elements: (1) at least one tristate buffer and (2) a delay circuit.” Dec. at 18. First, the Board determined “that Petitioner relies on Osanai’s write leveling circuitry 322 and read leveling circuitry 323 as disclosing the recited ‘*delay circuit*.’”

Dec. at 19, n.2, *citing* Pet. 43. Annotated Figure 5 of Osanai shows these read and write leveling circuitries in data register buffer 300, highlighted below:

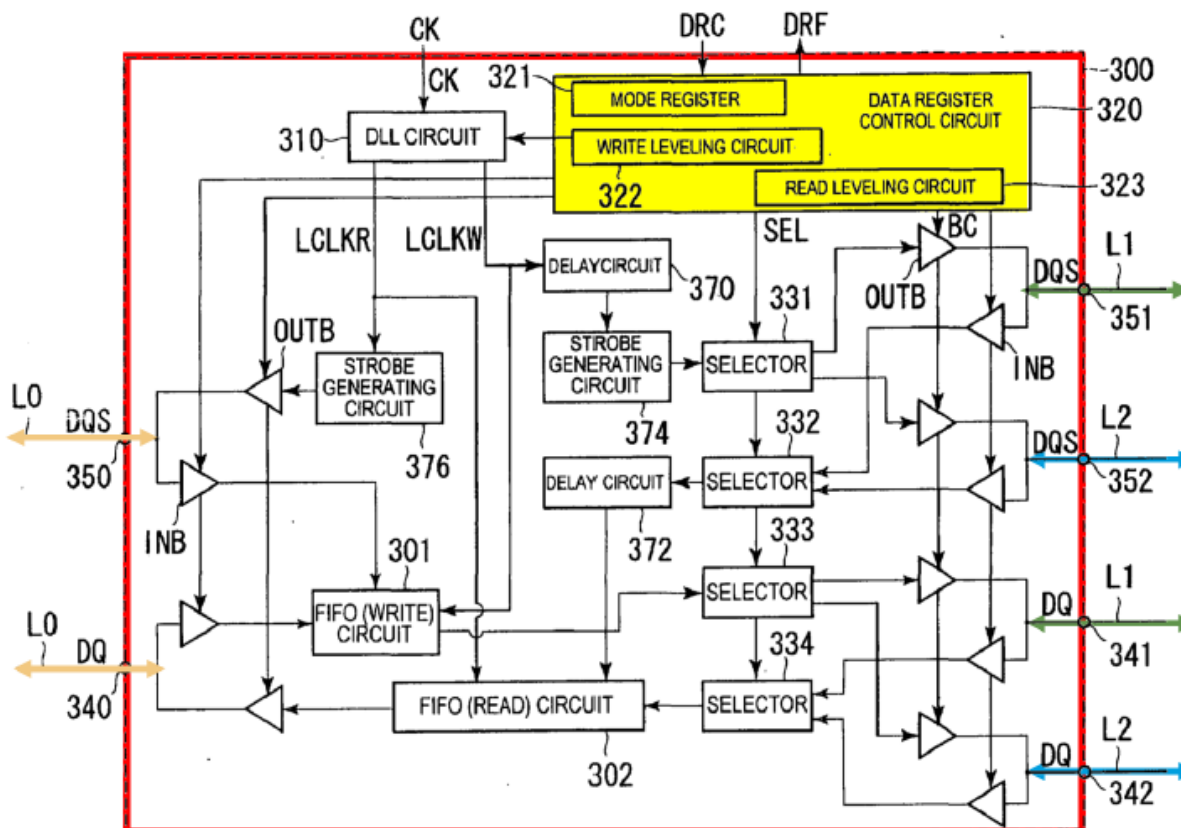


Figure 5 (annotated), Pet. 42. The Decision also correctly noted that the Petition identified buffers, such as the OUTB buffers, as disclosing the claimed “*tristate buffer*.” Dec. at 19; Pet. at 40. The Decision also noted that the Petition explained that “[a]ny data path selected by Osanai’s data register control circuit includes a ‘tristate buffer’” *Id.* The Board thus correctly understood Petitioner’s mapping for the two “*data path*” elements: (1) at least one tristate buffer (e.g., OUTB) and (2) a delay circuit (i.e., either Osanai’s read or write leveling circuitries).

The Board's Decision takes issue whether the Petition shows that Osanai discloses the recited delay circuit included in the claimed "*data path*." This Decision, however, overlooks the Petition's explanation of how Osanai discloses "*a command processing circuit configured to . . . control the data path*" in limitation 1[i], as explained below, which contained the information the Board suggested was missing.

**B. The Decision Overlooked the Petition's Explanation of How a Data Path Is Controlled and Its Evidence**

The Board overlooked the Petition's description of Osanai's "*data path*" in addressing limitation 1[i]. *See* Pet. at 38-40. For this limitation, the Board correctly noted that that Petitioner "identifie[d] the data register control circuit 320 and DLL circuit 310 in the data register buffer 300 as the recited 'command processing circuit' and argues that this circuitry uses the received DRC signals and clock signals *to select the appropriate data path*.'" Dec. at 16 (emphasis added). The Board, however, overlooked this explanation and its cited evidence showing how Osanai discloses how the appropriate "*data path*" is selected. This overlooked explanation, as explained further below, described how buffer circuit 300 in Figure 5 has two data paths—that is, one for read operations and another for write operations—each having their own components. The Petition also explained how components in each of these paths use local clocks generated from Osanai's read and write leveling

circuitries. The petition thus showed how these two data paths in Osanai both satisfy that the “*data path*” “*includes . . . the delay circuit.*”

The Petition initially explained that each buffer circuit 300 has two “different data paths for reading and writing operations.” Pet. at 39, *citing* Ex. 1005, [0094], [0105], and [0106]. The Petition relies on paragraph 106 of Osanai for support, which explains that the control signal DRC supplied to the data register control circuit 320 includes a “signal indicating a direction of transmitting or receiving data.” *Id.*, [0106]; *see also id.*, [0132]. Accordingly, the DRC signal determines the data path direction through Figure 5 based on whether it is a read operation (i.e., right to left) or write operation (i.e., left to right). Figure 5 thus shows two data paths—one for read operations and another for write operations—each of which has a data signal that travels an individual direction through buffer circuit 300.

The Petition further explained what components belong to each of these read or write paths. *See* Pet. at 39–40. Specifically, the Petition stated that selectors 331–334 and input/output terminals, 341 and 342, of data register buffer 300 are included in data paths for read and write operations:

[A] POSITA would have understood these disclosures to teach that the data register control circuit 320 selects (or “controls”) certain paths using SEL, INB, and OUTB signals as well as selectors 331–334, which supplies data

DQ to input or output terminals, 341 and 342, to certain memory chips 200.

Pet. at 39–40, *citing* Ex. 1003, ¶ 115; Ex. 1005, [0094], [0097]. The Petition also cites paragraph 97 of Osanai, which further explains that the read and write data paths include different components—that is, a FIFO (Write) circuit and FIFO (read) circuit. Ex. 1005, [0097] (describing, for a write operation, that “[t]he selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals.”); *id.* (describing, for a read operation, that “[t]he selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302.”). To summarize, the Petition explains (or cites evidence that specifies) that the read and write data paths include at least<sup>1</sup> the following components in Figure 5:

- Write data path includes FIFO (Write) circuit 301, selector 333, Terminals 341 and 342; and
- Read data path includes Terminals 341 and 342, selector 334, FIFO (Read) Circuit.

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<sup>1</sup> The remaining components include tristate buffers, which the Board’s Decision acknowledged that the Petition showed were in Osanai’s data path. Dec. at 19–20.

The Petition therefore identified which components in Figure 5 make up the data paths for read and write operation, respectively.

The petition also explained that components in each of the read or write paths use their respective local clock, LCLKR and LCLKW. Specifically, the Petition explained a “POSITA would have recognized that that the data path would have used [the LCLKR and LCLKW for read and write operations, respectively,] for their respective read/write operation data paths.” Pet. at 40 (citing Ex. 1003, ¶ 115). As shown in Figure 5 above, the FIFO (read) circuit and FIFO (write) circuit—each of which is included in the read or write data path, respectively—use their respective local clocks. See Ex. 1005, [0093] (explaining how both FIFO circuits have their “output operation timing” “defined” by their respective local clock). Petitioner’s expert likewise confirms that read and write operations use these respective local clocks:

A POSITA would have understood that Osanai’s DLL circuit 310 receives this module (CK) signal, which uses that signal to generate two local clocks: one for read operations (LCLKR) and another for write operations (LCLKW). Ex. 1005, [0090], [0093].

Ex. 1003, ¶ 122. Patent Owner’s Preliminary Response (Paper No. 12) (“POPR”) confirms that the LCLKR and LCLKW are used in read and write operations. POPR at 18 (“The strobe generating circuit 376 uses internal clock signal LCLKR to

generate the DQS used in read operations.”); *id.* (“The strobe generating circuit 374 uses internal clock signal LCLKW phase adjusted a fixed 90 degrees by delay circuit 370 to generate the DQS for write operations.”). Accordingly, it is undisputed that the LCLKR and LCLKW are used for timing read and write operations, which necessarily means that these clocks are used in the respective read or write data paths.

Local clocks LCLKR and LCLKW originate from their respective read and write leveling circuitries<sup>2</sup>—each being the claimed “*delay circuit*” for its respective read/write data path. Petitioner’s expert explains, in detail, that Osanai’s read and write leveling circuitry 323 and 322 use these local clocks to make timing adjustments so data signals are sent at the appropriate time:

121. Osanai discloses both read and write leveling techniques, which are performed by circuitry 323 and 322 located in the data register control circuit 320. . . Osanai’s techniques make timing adjustments so that signals between “the memory chips 200 and the data register buffer 300” are sent at the appropriate time. Ex. 1005, [0110]; see also *id.*, [0096], [0146].

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<sup>2</sup> As the Board noted, the Petition identified these leveling circuitries as being the claimed “*delay circuit*.” see Dec. at 19, n.2.

122. To make these adjustments, the read and write leveling circuitry and DLL Circuit 310 . . . use the module clock (CK) signal sent from the command/address/control register buffer 400 . . . A POSITA would have understood that Osanai’s DLL circuit 310 receives this module (CK) signal, which uses that signal to generate two local clocks: one for read operations (LCLKR) and another for write operations (LCLKW). Ex. 1005, [0090], [0093].

Ex. 1003, ¶¶ 121–122. Osanai’s specification further explains how write leveling circuitry 322 uses LCLKW to change the output timing for write operations. *See* Ex. 1005 at [00151] (“The write leveling circuit 322 . . . changes an output timing of the data strobe signal by displacing the internal clock LCLKW based on the direction of the phase shift.”). Petitioner’s expert testimony confirms how the leveling circuitries use their local clocks to change output timing for their respective operations:

123. Using [(LCLKR) and (LCLKW)], a “timing adjustment”—that is, an added time delay—is then used [to] compensate for propagation delays. For example, and during the write leveling operation, Osanai’s “data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK,” which is supplied by command/address/control register buffer 400. *Id.* [0149]. Because of differing propagation delays, however, “input timings of the clock signal CK and the data strobe

signal DQS are not always the same on the memory chip 200 side.” *Id.* To correct this timing error, the write leveling circuitry 322 delays the output timing of the DQS sent from data register buffer 300, thus creating DQS-Post (“*delay[ing] a signal through the data path by an amount determined by the command processing circuit*”). *Id.* [0151]–[0152]. A similar read leveling process results in signals being delayed. Ex. 1005, [0153]–[0157].

Ex. 1003, ¶ 123. Moreover, Patent Owner’s annotated Figure 5 shows that the LCLKW originates<sup>3</sup> from the Osanai’s write leveling circuitry 322:

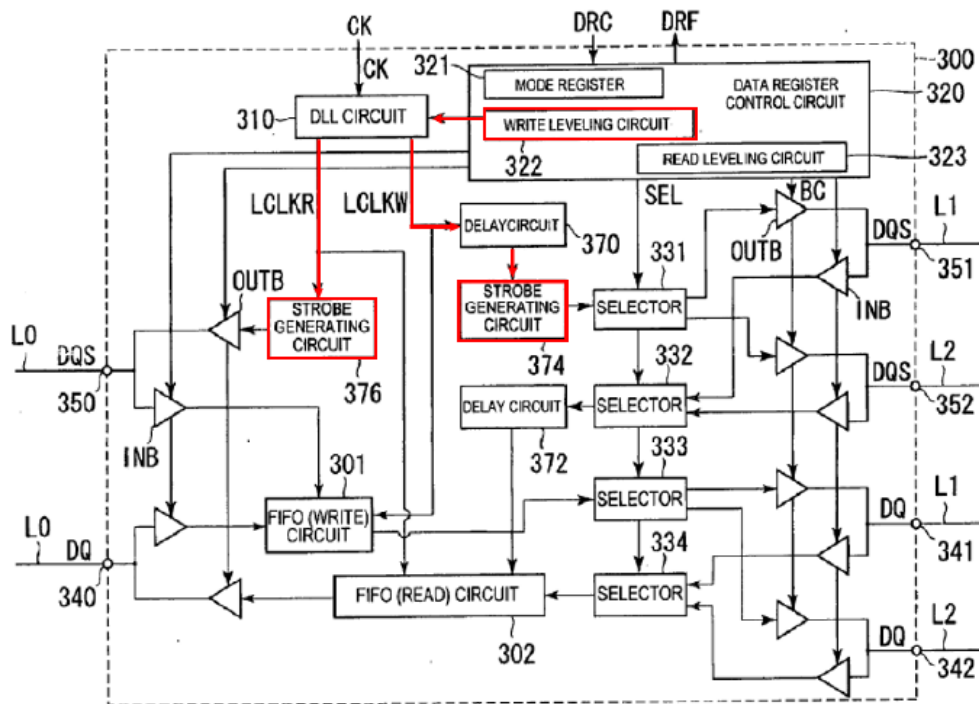


FIG. 5

<sup>3</sup> Petitioner disputes that LCLKR (local read clock) originates from the write leveling circuit, which Patent Owner’s annotated Figure 5 appears to show.

Prelim. Resp. (Paper 12) at 18. Accordingly, both sides interpret Osanai to disclose that at least the LCLKW originates from Osanai's Write Leveling Circuitry 322.

As shown above, each of Osanai's "*data paths*" include a component (i.e., the FIFO (READ) and (WRITE) Circuits) that uses these local clock signals thereby showing every "*data path*" "*includes . . . a delay circuit.*" To the extent that the Board disagrees that this claim feature is satisfied by having a component in the delay path use a clock signal supplied from the claimed delay circuit, Petitioner submits that such a determination would raise a claim construction issue that neither party has briefed. In addition, Patent Owner's infringement contentions show a delay circuit supplying a clock signal to a component in the data path satisfies the claimed "*data path*" that "*includes. . . a delay circuit*" even though the delay circuit is located outside the data path. Moreover, Petitioner's proposed modification of Osanai with Tokuhiro's technique, *see* Pet. at 45–51, would necessarily include a "*data path*" that "*includes . . . a delay circuit*" under any reasonable interpretation of the claims. Thus, Petitioner respectfully requests institution of an *inter partes* review so that both Patent Owner and Petitioner can fully address any claim construction issue arising for how to interpret a "*data path*" that "*includes . . . a delay circuit,*" if needed.

At bottom, the Petition explained that Figure 5 includes both a read and write data path—each including its own respective FIFO buffer that uses its own local

clock, LCLKR or LCLKW. These local clocks are determined by the read or write leveling circuitries, which the Petition identified as each being the claimed “*delay circuit*.” Because each of Osanai’s “*data paths*” include a component that uses these local clock signals, each of the claimed “*data paths*” for read and write operations includes “*a delay circuit*.” Accordingly, the Petition’s explanation of how a data path is controlled shows how the Petition “identified a data path that includes Osanai’s write leveling circuitry” contrary to the Board’s determination. *See* Dec. at 18.

### **C. Conclusion**

For the reasons set forth above, Petitioner respectfully requests that the Board reconsider and grant *inter partes* review of the challenged claims of the ’608 patent.

Dated: August 18, 2022

Respectfully submitted,

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## **CERTIFICATE OF SERVICE**

The undersigned hereby certifies that the foregoing **PETITIONER'S REQUEST FOR REHEARING OF DECISION DENYING INSTITUTION** were served electronically via e-mail on August 18, 2022, in its entirety on the following counsel of record for Patent Owner:

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