

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inter Partes Review

U.S. Patent No. 10,268,608

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS,
INC.; and MICRON TECHNOLOGY TEXAS LLC,

Petitioner

v.

NETLIST, INC.

Patent Owner

IPR2022-00237

DECLARATION OF DONALD ALPERT, PH.D.

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I, Donald Alpert, of Sacramento, California, declare that:

I. INTRODUCTION

1. In view of my scientific and technical knowledge relating to systems and methods for computer architecture and memory, I have been retained by Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (“Micron”) in this *Inter Partes* Review as an independent expert to provide my opinions on the subject matter recited in the claims of U.S. Patent No. 10,268,608 in view of the state of the field at the time of the filing of that patent and various publications (“references”) that predate the priority date of this patent. I will refer to U.S. Patent No. 10,268,608 as the ’608 patent or the Challenged Patent.

II. BACKGROUND AND QUALIFICATIONS

2. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 2020 21st Street, Sacramento, CA 95818. I am over the age of eighteen, and I am a citizen of the United States.

3. I have 45 years of academic and industrial experience in applying, designing, studying, teaching, and writing about microprocessors and computer

systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford University. I earlier received an Electrical Engineering B.S. degree from MIT in 1973 and an Electrical Engineering M.S. degree from Stanford University in 1978. I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

4. From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data communications based on Intel 8080 microprocessor components. From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time. The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (e.g., network, hard drive, USB) for system peripheral

devices. Additionally, I served as co-manager for the Itanium processor design from 1993 to 1997.

5. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000. I was the keynote speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference proceedings. My paper entitled “Architecture of the Pentium Processor” was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30 U.S. patents that pertain to microprocessors, computer systems, and related technology.

6. I have reviewed the '608 patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, and peripheral devices for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More

specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for initializing, calibrating, and testing the memory system, which comprised a memory controller and standard SDRAM modules.

7. My curriculum vitae, including my publications and patents, is submitted herewith as Ex. 1004.

III. SCOPE OF WORK

8. I have been asked to consider and provide my opinions on the claims of the Challenged Patent, including the technical subject matter and the application of various references that predate the priority date of the patent. In particular, I have been asked to consider what one of ordinary skill in the art would have understood from the claims and specification of the Challenged Patent, whether certain references disclose or suggest the features recited in the claims of the Challenged Patent, and whether one of ordinary skill in the art would have had reason to combine certain references to arrive at the claimed subject matter.

9. I am compensated at a rate of \$600/hour for my work. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceeding.

10. In forming my opinions, I have reviewed the Challenged Patent (Ex. 1001), its prosecution history (Ex. 1002), and the following references:

Ex. No.	Brief Description
1005	U.S. Patent Application Publication No. 2010/0312925 to Osanai et al. (“Osanai”)
1006	U.S. Patent No. 8,020,022 to Tokuhiro (“Tokuhiro”)
1007	U.S. Patent No. 8,713,379 to Takefman et al. (“Takefman”)
1008	U.S. Patent No. 9,824,035 to Lee et al.
1009	RESERVED
1010	File History of U.S. Patent No. 9,128,632
1011	U.S. Patent No. 8,565,033 to Manohararajah et al. (“Manohararajah”)
1012	Excerpts from DDR4 SDRAM Load Reduced DIMM Design Specification, JEDEC Standard, JESD2C, Revision 1.00 (August 2015)
1013	DDR3 SDRAM, JEDEC Standard, JESD79-3C (November 2008)
1014	RESERVED
1015	Graf, Rudolph F., Modern Dictionary of Electronics, 7 th ed. (1999)
1016	RESERVED
1017	RESERVED
1018	RESERVED

IV. SCOPE OF DECLARATION AND LEGAL STANDARDS

11. I am not an attorney and will not offer opinions on the law, but I have been instructed in and applied the law as described in this section.

A. Legal Standard for Prior Art

12. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

13. I am informed by counsel that the applicable law in this case for prior art is 35 U.S.C. § 102 as written before the America Invents Act.

14. I am informed that the patent owner Netlist, Inc. (“Netlist”) contends that the ’608 patent claims priority to July 27, 2012.

15. I understand that the “priority date” of a patent is the date on which it is filed, or the date on which an earlier-filed patent application is filed if the patentee claims it is entitled to the benefit of priority to that earlier-filed patent application. To be entitled to that benefit, I further understand that the earlier filed application must support the claimed subject matter in the manner required by 35 U.S.C. § 112. I understand that this section requires the patent’s specification to contain a sufficient written description of the claimed invention to demonstrate that the applicant actually possessed the invention as of the filing date as broadly as it is

claimed. In considering whether this written description requirement is met, I understand that I should consider the written description from the viewpoint of a person of ordinary skill in the art. I also understand that I should consider whether this person of ordinary skill would have recognized that the written description describes the full scope of the claimed invention and that the inventor actually possessed that full scope as of the claimed effective filing date. I understand that a person of ordinary skill would be able to immediately discern the limitations of the claims from the priority specification. I understand that a priority specification may provide inherent support if explicit support is missing. I understand that a person of ordinary skill would have understood an element to be inherent if the priority specification requires that element, but inherency cannot be established by probabilities or possibilities. I understand that a subgenus is not necessarily implicitly described by a genus or species unless the specification directs the person of ordinary skill to the claimed subgenus. I also understand that law for priority is not the same as the obviousness analysis under 35 U.S.C. § 103.

16. I further understand that the priority date is significant because patents, systems, or documents that are public prior to the priority date may invalidate the claims.

17. I understand that a U.S. patent may qualify as prior art to an asserted patent if the date of publication or issuance is prior to the invention in the asserted patent. I further understand that a printed publication, such as a book or an article published in a magazine or trade publication, may qualify as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent. A paper or presentation may also qualify as prior art if presented at a publicly available seminar, conference, or trade show prior to the invention in the asserted patent.

18. I understand that a U.S. patent or published patent application may qualify as prior art to the asserted patent if the application for that U.S. patent or published patent application was filed in the United States before the invention of the asserted patent.

19. I understand that to qualify as prior art, a reference must contain an enabling disclosure that allows one of ordinary skill to practice the claims without undue experimentation.

20. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

B. Anticipation

21. I understand that once the claims of a patent have been properly construed, determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

22. I understand that a prior art reference “anticipates” an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either explicitly or inherently (i.e., necessarily present or implied).

23. I understand that a patent is anticipated if, before such person’s invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

24. I have written this report with the understanding that in an *inter partes* review, anticipation must be shown by a preponderance of the evidence.

C. Obviousness

25. I have been instructed by counsel on the law regarding obviousness, and understand that even if a patent is not anticipated, it is still invalid under 35 U.S.C. § 103, as written before the America Invents Act, if the differences between

the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art.

26. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents a person of ordinary skill from using one's insight or hindsight in deciding whether a claim is obvious.

27. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

28. I am informed that secondary considerations of non-obviousness may include (1) a long-felt but unmet need in the prior art that was satisfied by the invention of the patent, (2) commercial success or lack of commercial success of processes covered by the patent, (3) unexpected results achieved by the invention, (4) praise of the invention by others skilled in the art, (5) taking of licenses under the patent by others, and (6) deliberate copying of the invention. I also understand

that there must be a relationship or “nexus” between any such secondary indicia and the invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

29. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link between two or more prior art references is simple common sense. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, can drive innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

30. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

31. I also understand that practical and common-sense considerations should guide a proper obviousness analysis, because familiar items may have

obvious uses beyond their primary purposes. I further understand that a person of ordinary skill in the art looking to overcome a problem will often be able to fit the teachings of multiple publications together like pieces of a puzzle, although the prior art need not be like two puzzle pieces that must fit perfectly together. I understand that obviousness analysis therefore considers the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

32. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

33. I understand that the combination of familiar elements according to known methods may be proven obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same

field or a different one. If a person of ordinary skill can implement a predictable variation, obviousness likely bars its patentability.

34. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. Additionally, a reference outside of the field of endeavor may still be prior art if the reference is reasonably pertinent to the particular problem being solved by the patentee.

35. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense and knowledge of one of skill in the art.

36. I understand that a person of ordinary skill could have combined two pieces of prior art or substituted one prior art element for another if the substitution can be made with predictable results, even if the swapped-in element is different from the swapped-out element. In other words, the prior art need not be like two puzzle pieces that must fit together perfectly. The relevant question is whether

prior art techniques are interoperable with respect to one another, such that a person of skill would view them as a design choice, or whether a person of skill could apply prior art techniques into a new combined system. The person of ordinary skill would use ordinary creativity and is not limited like an automaton.

37. In sum, my understanding is that prior art teachings are properly combined where a person of ordinary skill in the art, having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

38. I have been informed and understand that the obviousness analysis requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

39. I have written this report with the understanding that in an *inter partes* review, obviousness must be shown by a preponderance of the evidence.

V. LEVEL OF ORDINARY SKILL IN THE ART

40. My opinions are provided based on what a person of ordinary skill in the art in the technical field of the purported invention would have understood at the time of the purported invention of the Challenged Patent. I have been asked to assume the date of the purported invention for the '608 patent is July 27, 2012 ("'608 priority date").

41. I have been informed and understand that the content of a patent and prior art should be interpreted the way a person of ordinary skill in the art would have interpreted those references at the time of the invention of the patent. I understand that the person of ordinary skill is a hypothetical concept referring to one who thinks along the lines of conventional wisdom at the time.

42. I was asked to provide an opinion as to the level of one of ordinary skill in the art pertinent to the subject matter set forth in the Challenged Patent at the time of the priority date. Around 2012, it is my opinion that a person of ordinary skill in the art in the field of the Challenged Patent would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have

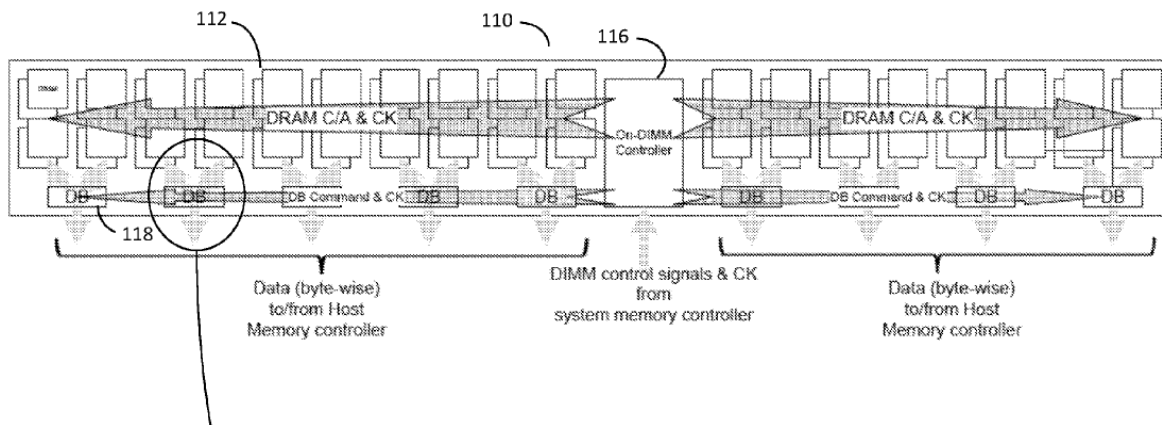
been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers. Standards for DRAM and SDRAM devices would have included, for example, DDR3 standards. *See, e.g.*, Ex. 1013. Throughout this declaration, I use the term “POSITA” to refer to a person with these or similar qualifications. To have similar qualifications, an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

43. The basis for my familiarity with the level of ordinary skill is my interaction with large numbers of workers in the computer industry who were at this level of skill. In reaching this opinion as to the hypothetical person of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field.

VI. OVERVIEW OF THE CHALLENGED PATENT**A. U.S. Patent No. 10,268,608 (Ex. 1001)**

44. U.S. Patent No. 10,268,608, entitled “Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers,” to applicants Lee, et al., was issued on April 23, 2019. Ex. 1001 at Cover. The ’608 patent originated from application U.S. Ser. No. 15/820,076, which was filed on November 21, 2017. *Id.* Through a series of continuations, which include its parent U.S. Patent No, 9,824,035 (the “’035 patent”), the ’608 patent claims priority to a provisional application, U.S. Provisional Application No. 61/676,883, which was filed on July 27, 2012.

45. The ’608 patent relates to computer memory modules. Ex. 1001, 1:37–39. It discloses a memory module that includes multiple memory devices 112, data buffers 118, and a module control device 116. Ex. 1001, Abstract. Each of these components is shown in Figure 2C below:



Ex. 1001, Fig. 2C excerpted.

46. As shown above, module control device 116 is located at the center of memory module 110. *See id.* Several memory devices 112 share a respective data buffer 118. Ex. 1001, 8:36–39. Both memory devices 112 and their respective data buffers 118 are distributed lengthwise across the memory module. *See* Ex. 1001, Fig. 2C.

47. Memory module 110 has a memory bus 105 to receive commands from and to communicate data with a memory controller 101. Ex. 1001, Fig. 1, 4:29–44. This bus includes both control/address (C/A) 120 and data/strobe 130 signal lines that connect the memory controller to the module control device 116 and to each memory device 112 via its shared data buffer 118, respectively. Ex. 1001, 4:29–44. To command the memory module 110, the memory controller

issues command signals across C/A signal lines. As one command signal, C/A signals are sent to the module control device 116 that instruct the memory module to perform operations, such as read or write operations. *Id.*, 3:29–38. For another, the memory controller sends and receives data (DQ) and strobe (DQS) signals to/from the memory devices 112 via the data buffers 118. *Id.*, 7:63–8:3; *see also id.*, 10:31–11:7. The data (DQ) signals convey data for the read and write commands; the strobe (DQS) signals carry timing information for those commands. *Id.*, 7:63–8:3; *see also id.*, 10:31–11:7.

48. Figure 2C of the '608 patent, shown above, illustrates that data buffers 118 and their associated memory devices 112 are distributed across the memory module at varying distances from the module control device 116. These varying distances result in “unbalanced wire lengths” that cause different propagation delays—stated otherwise, module control signals take longer to reach their destination because they are farther away from the module control device 116. Ex. 1001, 2:28–32. Conventional systems used “leveling mechanisms for write and/or read operations” in the memory controllers to compensate for such propagation delays. Ex. 1001, 2:28–32. A similar problem exists for DDR3 memory modules. Ex. 1013, p. 6 (“For better signal integrity, DDR3 memory module adopted fly-by

topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew.”). As memory density and speed increases, however, the ’608 patent explains that these leveling mechanisms can no longer accurately compensate for these propagation delays to ensure “proper timing of the control and/or data signals received and/or transmitted by the memory modules.” Ex. 1001, 2:32–36.

49. To solve this problem, each data buffer includes a signal alignment circuit that determines appropriate time intervals used for transmission timing so that signals arrive at the appropriate time. *See id.*, 10:7–21, 15:17–26. The ’608 patent discloses that the time interval is to be determined by the data buffer based on the timing of a write operation. Ex. 1001, 10:11–21; *see id.*, 10:7–11, 15:17–26. Using the timing interval used in the write operation, the signal alignment circuit determines the time interval for a read operation. Ex. 1001, 10:11–21; *see id.*, 10:7–11, 15:17–26.

50. Claim 1 is illustrative of the challenged claims, shown below:

[Claim] 1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe

signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ex. 1001, Claim 1.

B. Assumed Effective Filing and Invention Dates

51. I have been informed by counsel for this Petition that I should assume the earliest possible effective filing date for the '608 patent is July 27, 2012. I have also been informed by counsel for this Petition that I should assume the invention date for this patent is the same as its earliest effective filing date.

C. Relevant Prosecution History

52. The examiner never rejected the '608 patent over prior art. Instead, the examiner rejected the claims under obvious-type double patenting over U.S. Patent No. 9,128,632 (the "'632 patent") and the '035 patent (Ex. 1008). Ex. 1002, pp. 81–93. The applicant, in response, obviated that rejection by filing a terminal disclaimer. Ex. 1002, pp. 102–103, 106. The examiner then allowed the patent. Ex. 1002, pp. 126–128.

53. The prosecution history of its parent—U.S. Patent No. 9,128,632 (the "'632 patent")—explains why the examiner allowed the '608 patent. For that patent, the prosecution history explains what amendments persuaded the examiner that the claims overcame the prior art. The examiner initially rejected the claims as being anticipated by U.S. Patent No. 8,565,033 to Manohararajah et al. Ex. 1010 at 100–108; Ex. 1011. In response, the applicant first argued that Manohararajah

disclosed buffer circuits as part of the memory controller instead of the memory module as claimed. *Id.*, 139–140. The applicant then argued that Manohararajah did not teach the claims as amended. *Id.* at 140. Those amendments required each claimed data buffer to both:

- “determine a respective time interval based on signals received by the each respective buffer circuit during a memory *write operation*,” and
- “time transmission of a respective set of *read data signals* received from a respective group of memory devices in accordance with the time interval and a read latency parameter”

Ex. 1010 at 134–35 (emphasis added). The applicant similarly argued that the prior art did not teach these requirements. Ex. 1010, pp. 140–141 (“[n]owhere in Manohararajah it is [sic] described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals [sic] received by the each respective buffer.”); *see id.*, pp. 139, 142–143. Instead, the applicant characterized Manohararajah’s disclosure as describing how to delay “DQ/DWS” control signals for optimal phase alignment. *Id.*, 140–141.

54. The notice of allowance for the ’632 patent confirms that these amendments and corresponding argument persuaded the examiner. Referencing

this argument, Ex. 1010, p. 1078, the examiner explained why the prior art did not teach or render obvious the claimed amendments. *Id.* That explanation focused on how the claimed buffer circuits each determine their own respective time interval for the transmission timing of signals for read operations using signals received by each buffer circuit during write operations:

[The p]rior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module...

[T]he prior art does not fairly teach or suggest ... a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to ***determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the memory devices***, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the

receiving of a first signal from the controller and
receiving a second signal with for each buffer, i.e. each
buffer determines its own respective time interval used
for transmitting read/write signals to their respective
groups of memory devices as claimed in the independent
claims.

Ex. 1010, 1078 (emphasis added). Stated otherwise, the examiner observed that the prior art used buffered memory modules to delay signal transmissions, but there was no finding of buffers as claimed that determine a time interval for a *write operation* and use that information to determine the time interval for the *read operation*. Ex. 1010, pp. 100–108, 134–143, 1078.

55. The examiner made a similar statement in allowing the claims of the '608 patent. Ex. 1002, pp. 205–206. Initially, the examiner acknowledged that the prior art taught most claimed components: “memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module.” Ex. 1002, p. 206. The examiner, like the '632 patent application, focused the reason for allowance on how each buffer includes logic that obtains timing information based on signals

received by the buffers during a second memory operation prior to a first memory operation:

[T]he prior art does not fairly teach or suggest ... a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data/ strobe signal lines and the memory devices, wherein the logic is configured to ***obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information ...***

Ex. 1002, 206 (emphasis added).

56. These limitations, however, do not appear in the '608 patent and instead appear in its parent '035 patent. See Ex. 1008, Claim 1. Despite filing an after-final response, see Ex. 1002, pp. 265–269, the applicant did not seek any clarification on the examiner's reasons for allowance nor attempt to correct the

record. At most, this supposedly novel feature appears in claim 2 that further requires both (i) a “first memory operation,” a subsequent “second memory operation,” and (ii) the delayed “signal” is “associated with the second memory operation” in response to “control signals” belonging to the “first memory operation.” See Ex. 1001, 19:36–20:4. Based on the above disclosures, a POSITA would have recognized that the ’608, ’035, and ’632 patents were allowed by the examiner for the same reason.

VII. PRIOR ART REFERENCES

A. Osanai (Ex. 1005)

57. U.S Patent Application Publication No. 2010/0312925 to Osanai et al. (“Osanai”) is entitled “Load Reduced Memory Module.” Osanai was published on December 9, 2010. I have been instructed to assume that Osanai is prior art.

58. Osanai discloses a memory module 100 that includes multiple memory chips 200, data buffers 300, and a command/address/control register buffer 400, shown in Figure 1 below:

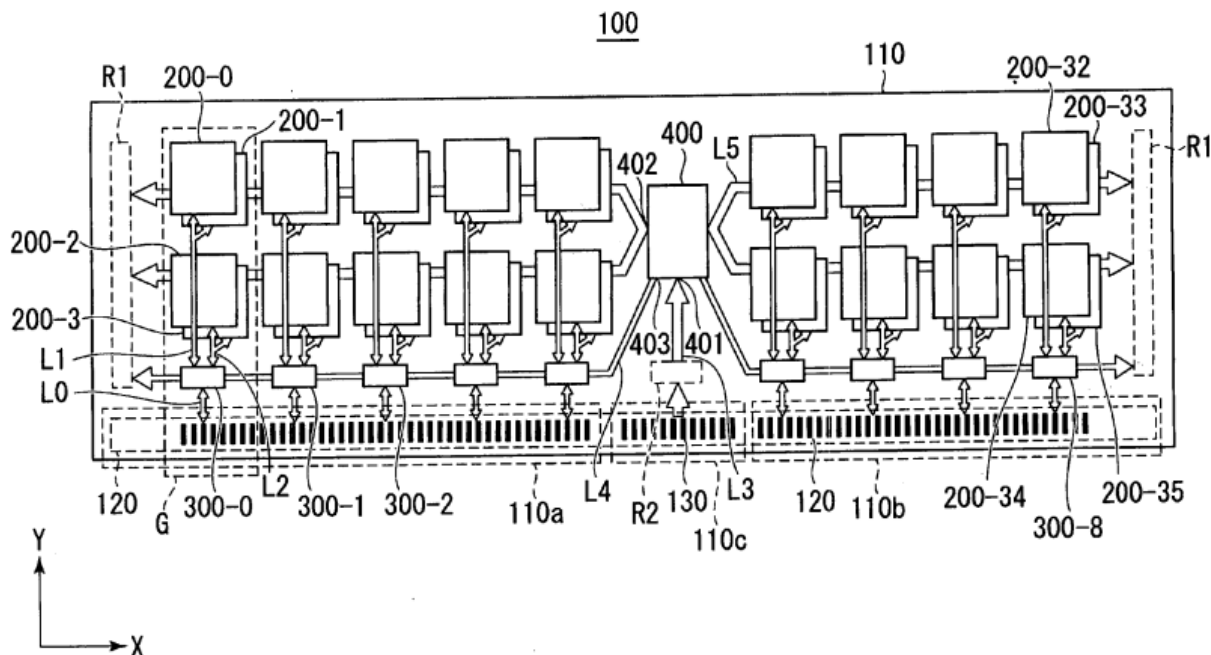


FIG.1

Ex. 1005, Fig. 1, [0051]–[0052]. Command/address/control register buffer 400 is located at the center of the memory module 100. *See* Ex. 1005, Fig. 1. Memory chips 200 are organized into sets with chips in the same set sharing a buffer 300. *See* Ex. 1005, Fig. 1, [0051]–[0052]; *see also* Ex. 1005, [0057]–[0058]. The same chips are also organized into ranks, which include one chip from each set. *Id.*, [0111]. Both memory chips 200 and their respective buffers 300 are distributed lengthwise across the memory module. *See* Ex. 1005, Fig. 1, [0052]–[0054].

59. Osanai's memory module 100 mirrors the topology described in the Joint Electron Device Engineering Council (JEDEC) standards for Double Data

Rate 4¹ (DDR4) SDRAM Load Reduced DIMM Design Specification. *See* Ex.

1012, p. 2. Figure 3 of that standard depicts a LRDIMM topology, shown below:

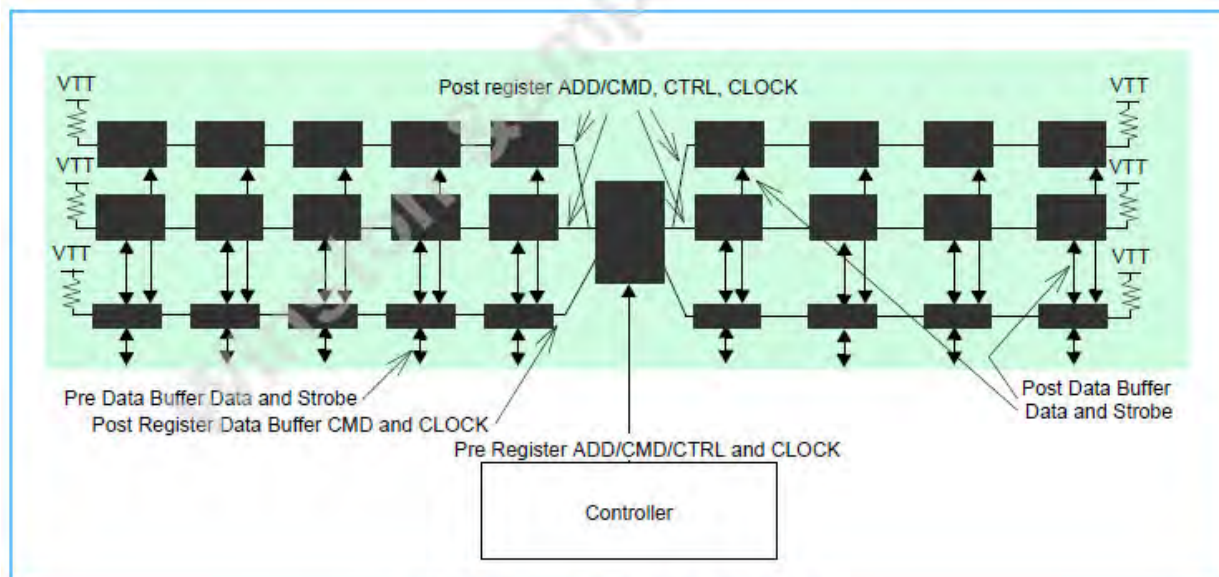


Figure 3 — LRDIMM Topologies

Id. Based on this and Osanai's disclosures, a POSITA would have recognized that both Osanai's Figure 1 and the topology shown above in Figure 3 represent the same LRDIMM topologies. *See id.*; Ex. 1005, Fig. 1, [0051]–[0054]; *see also* Ex. 1005, [0057]–[0058]. In addition, Osanai discloses the same signal groups described in the JEDEC standard. *Compare* Ex. 1012, p. 2 *with* Ex. 1005, Fig. 7,

¹ A POSITA would have known that the DDR4 Specifications for LRDIMM technologies were under development around 2012.

[0108]–[0114]. Based on these disclosures, a POSITA would recognize that Osanai's memory module 100 is consistent with the LRDIMM topology described in the JEDEC standard.

60. Memory module 100 receives commands from memory controller 12, shown in Figure 3 below:

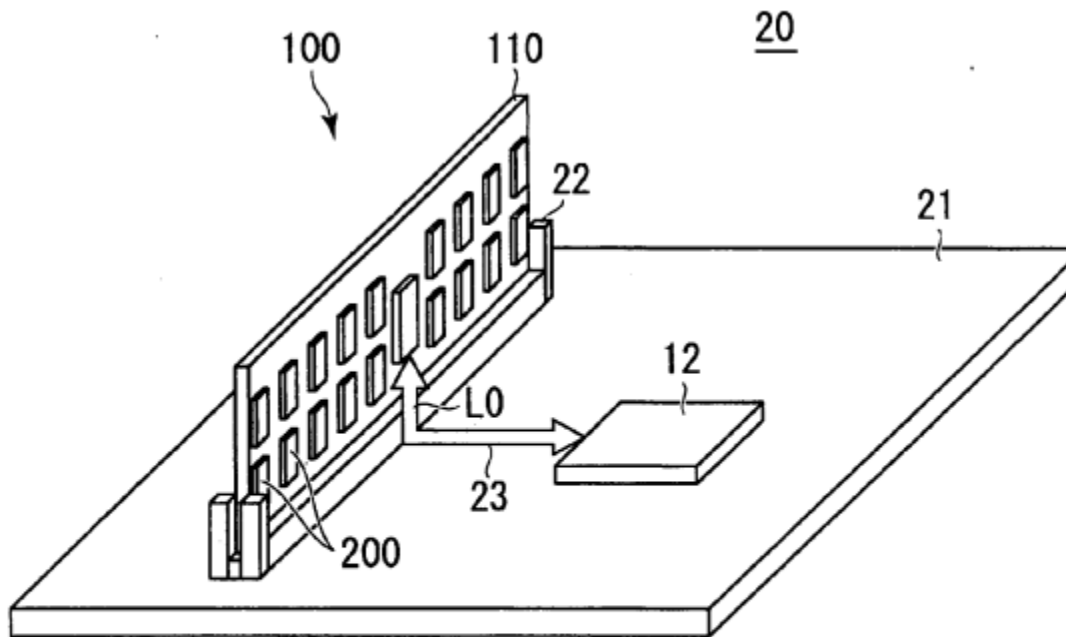


FIG.3

Ex. 1005, Fig. 3, [0074]–[0075]. To do so, memory module 110 receives commands across control/address (C/A) signal lines that connect the memory controller 12 and the command/address/control register buffer 400. Ex. 1005,

Figure 2, line 23, [0075]. A POSITA would have understood that these commands are sent over Osanai's line 23, which connects to data lines L0 and command/address/control line L3. Ex. 1005, [0075]. Memory controller 12 issues command signals across C/A signal lines to the command/address/control register buffer 400, which then sends C/A signals to instruct the memory chips 200 to perform operations, such as read or write operations. Ex. 1005, [0054]–[0055]. Memory controller 12 also sends and receives data/strobe signals to/from the memory chips 200 via the buffers 300 used to convey data for the read and write commands. Ex. 1005, [0054]–[0055].

61. Osanai recognized that, because these memory chips 200 and their respective buffers 300 are located at different distances from command/address/control register buffer 400, signals arrive at memory chips 200 later when those chips are located farther away. *See id.*, [0146]–[0149]. To compensate for this propagation delay, Osanai discloses both read and write leveling circuitry 322 and 323 located in the data register control circuit 320 of data buffer 300. *Id.* at Fig. 5, [0096]; *see also id.*, [0146]–[0164], Figs. 14A–17. These read and write leveling operations “adjust a write timing or a read timing in consideration of a propagation time of a signal.” *Id.* [0146]. Stated otherwise,

these techniques make timing adjustments so that signals between “the memory chips 200 and the data register buffer 300” are sent at the appropriate time. Ex. 1005, [0110]; *see also id.*, [0096], [0146].

B. Tokuhiro (Ex. 1006)

62. U.S. Patent No. 8,020,022 to Tokuhiro (“Tokuhiro”) is entitled “Delay Time Control of Memory Controller.” Tokuhiro was published on March 19, 2009. I have been instructed to assume that Tokuhiro is prior art.

63. Tokuhiro relates to computer memory and discloses a timing “technique for controlling read/write operations for a plurality of memories” Ex. 1006, 1:15–20. Tokuhiro recognized that memory modules designed according to JEDEC standards have SDRAMs placed in a “lengthwise direction” away from the memory controller resulting in differing propagation delays where each memory will not receive the clock signal the same time. *Id.* 1:63–2:1 (“Thus, in the DDR3 memory interface, because the clock signal line for the clock signal CK is wired to the plurality of SDRAMs 92-1 to 92-*n* through the daisy chain connection and a propagation delay is generated, the clock signal CK output from the memory controller 90 cannot reach all the SDRAMs 92-1 to 92-*n* at the same time.”); *see id.*, 2:1–23. A POSITA would have understood that Tokuhiro’s “daisy

chain” technology is also referred to as JEDEC’s “fly-by topology.” See Ex. 1006, 1:63–2:23; Ex. 1013, p. 6.

64. Tokuhiro describes the same problem identified by the ’608 patent. Compare Ex. 1006, 1:63–2:1 with Ex. 1001, 2:25–33. Tokuhiro recognizes that the JEDEC standard specifies a “write leveling function” where variable delay circuits are used to sample the clock signal from the memory controller output during write operations “and adjusting (compensating) a delay time of the data strobe signal.” Ex. 1006, 2:10-23. Tokuhiro also recognizes, however, that the JEDEC standard does not provide for a corresponding delay compensation for read operations. Ex. 1006, 2:54-59 (“compensations of the signal arrival time in read operations are not provided with the JEDEC standards”).

65. A POSITA would have recognized that both Tokuhiro and the ’608 patent propose the same solution, as well. Tokuhiro proposes a solution of calculating a delay time for read operations based on timing information obtained from prior write operations. Ex. 1006, Abstract (“For each of the plurality of memories, a first variable delay unit for delaying, in the write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read

operation, a data signal input from the memory by a second delay time that is set based on the first delay time.”). *see id.*, 15:14–23, 15:54–58. Likewise, the ’608 patent calculates its read operation delay the same way: “[t]his time interval [determined during the write operation] is used during a subsequent read operation to time the transmission of read data to the [memory controller]” Ex. 1001, 4:8–19. Accordingly, a POSITA would have recognized that both Tokuhiro and the ’608 patent describe the same solution—the supposed inventive concept that the examiner focused on in the notice of allowance.

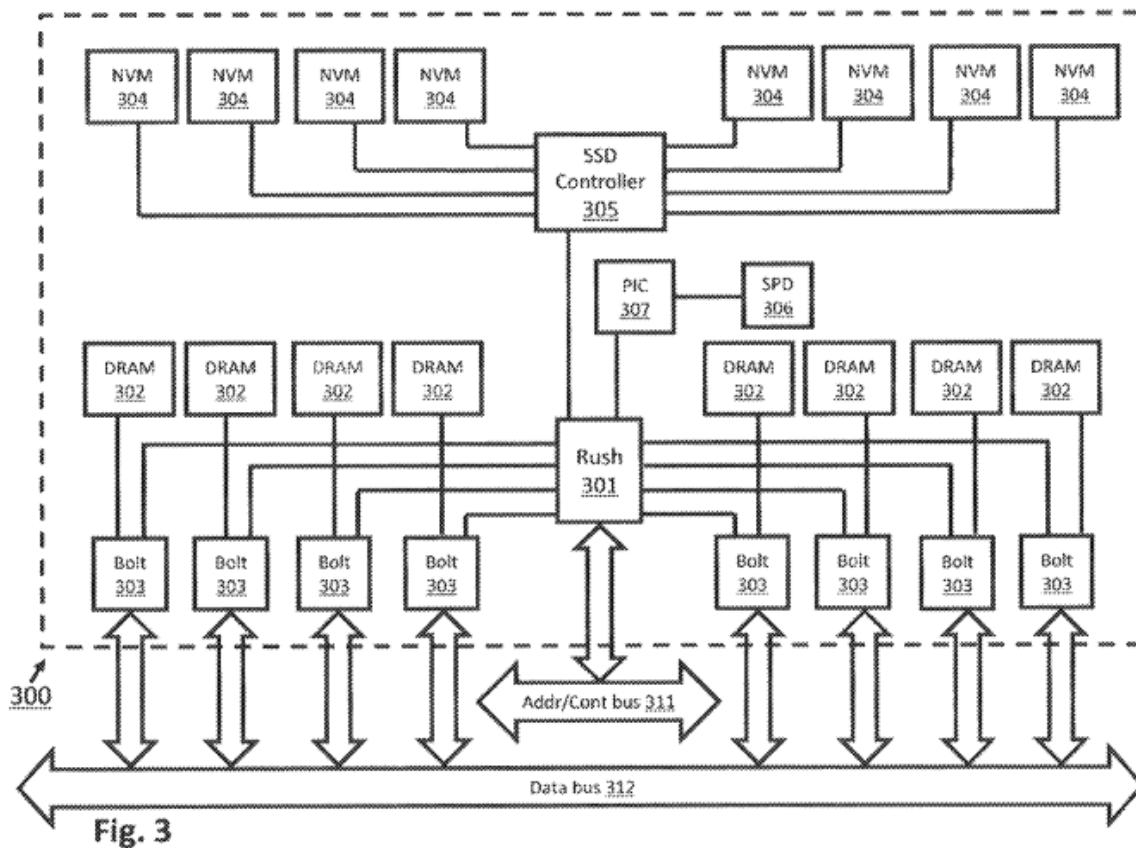
66. Based on the above disclosures, a POSITA would have understood that Tokuhiro and the ’608 patent thus describe the same propagation delay problem caused by memory chips being located at different distances lengthwise across a memory module. Such a person would have recognized that both propose the same solution: for each memory, calculate the delay for the read operation using the delay determined during a write operation.

C. Takefman (Ex. 1007)

67. U.S Patent No. 8,713,379 to Takefman et al. (“Takefman”) is entitled “System and Method of Interfacing Co-Processors and Input/Output Devices Via a

Main Memory System.” Takefman was filed on November 22, 2011. I have been instructed to assume that Takefman is prior art.

68. Takefman also discloses a TeraDIMM architecture that includes DRAM 302, “data buffer devices” (called Bolt devices) 303, and a Rush 301, shown in Figure 3 below:



As shown above, Rush 301 is located centrally to the DRAMs 302 of the memory module 300. *See id.*, Fig. 3. DRAM 302 can be organized into groups called ranks. *See id.*, 5:2–10. Each DRAM 302 also connects to a corresponding Bolt

device 303. Ex. 1007, Fig. 3; 5:53–63. Both DRAM and their respective Bolt devices are distributed lengthwise across TeraDIMM 300. Ex. 1007, Fig. 3; 5:53–63.

69. Takefman further discloses that, “[b]ecause of the difference in the distances between the Bolt devices 303 and the Rush 301 and the Bolt devices 303 and the DRAM devices 302, the TeraDIMM may arrange its launch time.” Ex. 1007, 6:17–20. This allows “data [to] arrive[] at an appropriate time.” *Id.* To do so, Rush 301 includes per-lane delay compensation circuits that provide “programmable launch times and lane de-skew.” Ex. 1007, 6:14–17. Stated otherwise, a POSITA would have understood that these compensation circuits delay signal transmission so that signals arrive at the appropriate time.

VIII. CLAIM CONSTRUCTION

70. I understand that claim terms are given their ordinary and customary meanings that would have been understood by one of ordinary skill in the art reading the specification of the Challenged Patent at the time of the priority date unless there is evidence that the inventor applied a special definition to a term in the claims or there was some statement made during prosecution that would affect the meaning of a term.

71. As of today, I understand Patent Owner has not advanced any claim constructions for the '608 patent. I reserve the right to supplement this declaration based on any future constructions argued by Patent Owner.

IX. THE '608 PATENT IS INVALID

72. In my opinion, claims 1 and 4 are anticipated by Osanai (Ex. 1005). In addition, and in my opinion, claims 1–5 would also have been obvious to a person of ordinary skill over Osanai (Ex. 1005) in view of Tokuhiko (Ex. 1006). Finally, and in my opinion, claims 1–5 would also have been obvious to a person of ordinary skill over Osanai (Ex. 1005) in view of Tokuhiko (Ex. 1006), in further view of Takefman (Ex. 1007).

A. Claims 1 and 4 are anticipated by Osanai (Ex. 1007)

1. Claim 1

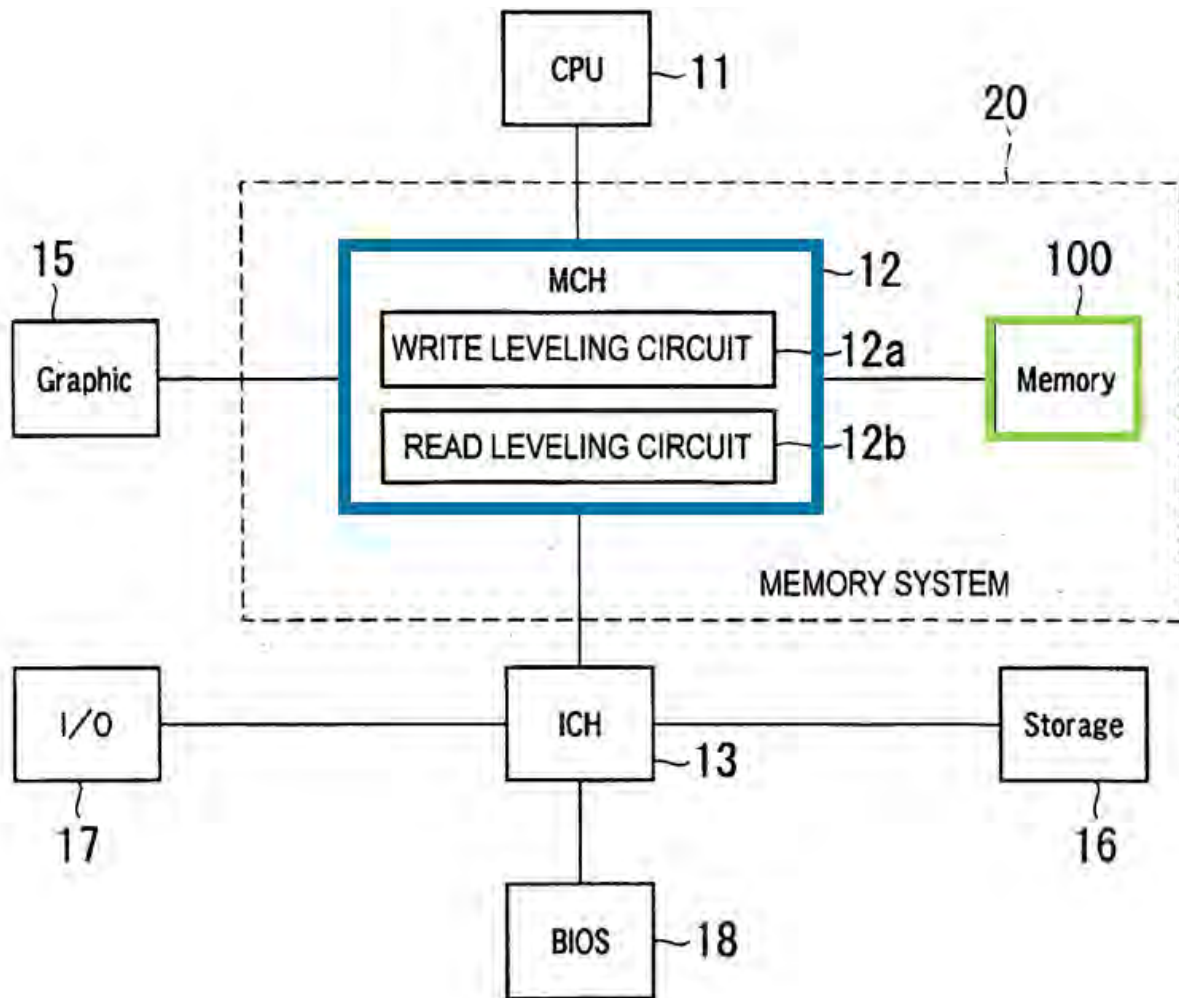
73. In my opinion, claim 1 is anticipated by Osanai.

- a. “[a] memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:”

74. Claim 1’s preamble recites “[a] *memory module operable to communicate with a memory controller via a memory bus ... the memory module.*”

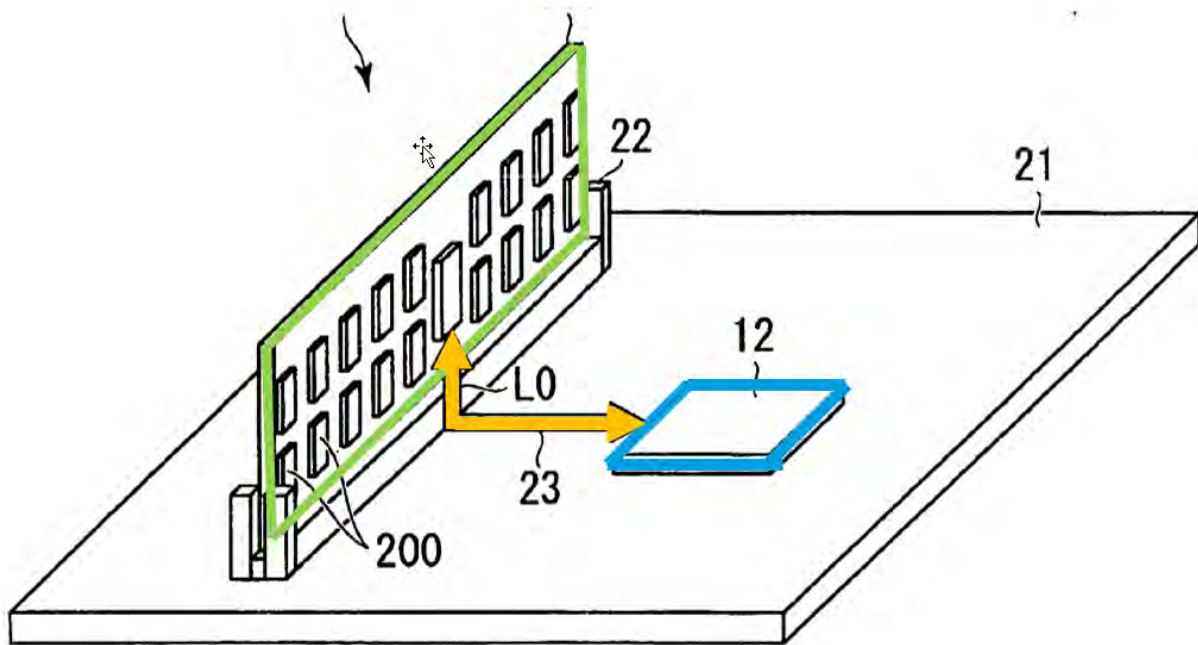
To the extent that one argues the preamble is limiting, Osanai teaches this limitation.

75. Osanai discloses a memory module 100 that operates in a memory system 20 with a memory control hub (or MCH) 12. Ex. 1005, [0069–71], Fig. 2. Figure 2 of Osanai illustrates that this memory module 100 is connected to memory control hub 12 (a “*memory controller*”), shown below:



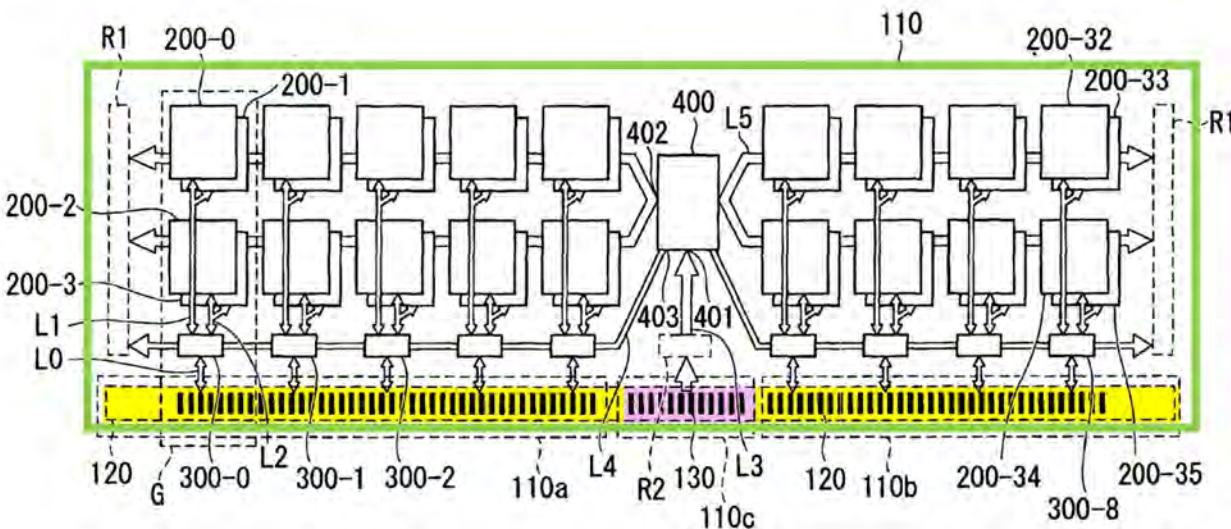
Ex. 1005, Fig. 2 (annotated). Memory control hub 12 “functions as a memory controller for the memory module.” Ex. 1005, [0071]. This functionality is consistent with how the ’608 patent describes a memory controller: “a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices.” Ex. 1001, 4:46-49.

76. Memory module 100 and control hub 12 communicate using connectors and a communication line 23. A POSITA would have understood that Osanai's line 23, which connects to data lines L0 and command/address/control line L3. Ex. 1005, [0075]. As shown in Figure 3 below, those components communicate over line 23:



Ex. 1005, Fig. 3, [0075] (“On a signal path between the memory controller 12 and the memory chips 200 [of memory module 100], there exists a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module substrate PCB 110.”).

77. In addition, the memory module 100 communicates with the memory controller using data connectors 120 (shown in yellow) and command/address/control connectors 130 (shown in pink), shown in annotated Figure 1 below:



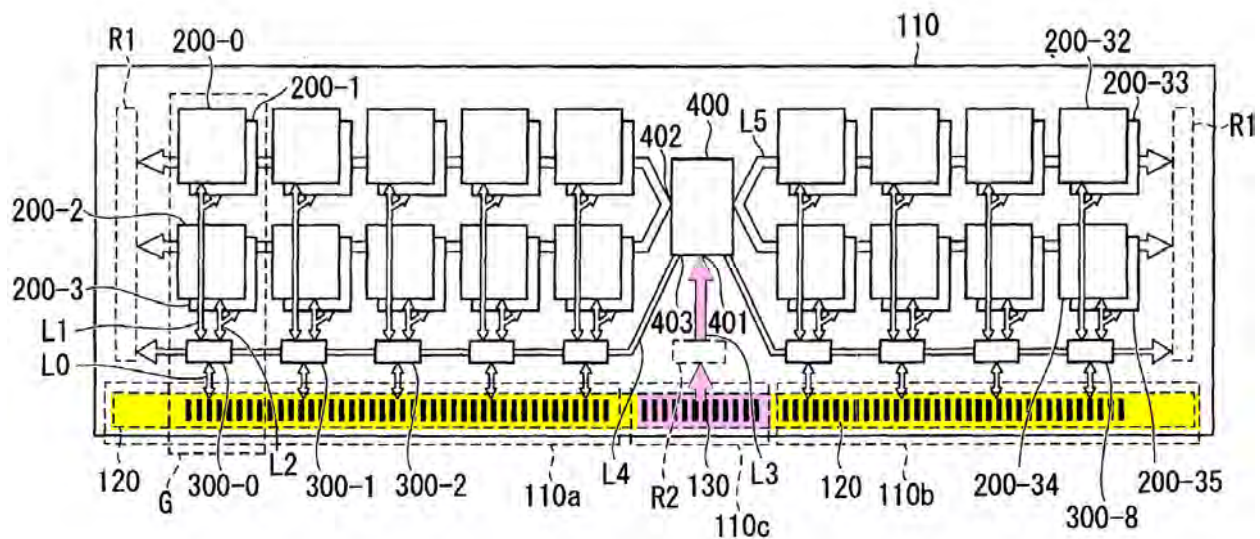
Ex. 1005, Fig. 1 (annotated), [0054]–[0055].

78. To communicate, memory module 100 and control hub 12 use line 23, data connectors 120, and command/address/control connectors 130. Based on the above disclosures, a POSITA would have understood that L0 and L3 signal lines and communication line 23, collectively, are a “bus.” Ex. 1005, [0126] (“As a result, the read data output from the data register buffer 300 can also be supplied to the memory controller without interruption, so that the usage efficiency of a bus

can be enhanced.”); see Figs. 1 and 2C (showing the path from MCH to connector to L0 data lines). This understanding is consistent with how the ’608 patent broadly describes a memory bus. Ex. 1001, 4:49-53 (“in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller”). Osanai therefore discloses a “*memory module [100] operable to communicate with a memory controller [12] via a memory bus.*”

79. Claim 1’s preamble further recites “*memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines.*” Osanai discloses this limitation.

80. As I explained above, Osanai’s Figure 1 illustrates a “*memory bus.*” This “*memory bus*” includes line 23 (see Ex. 1005, Fig. 3), which is connected to data connectors 120 (shown in yellow) and command/address/control connectors 130 (shown in pink):



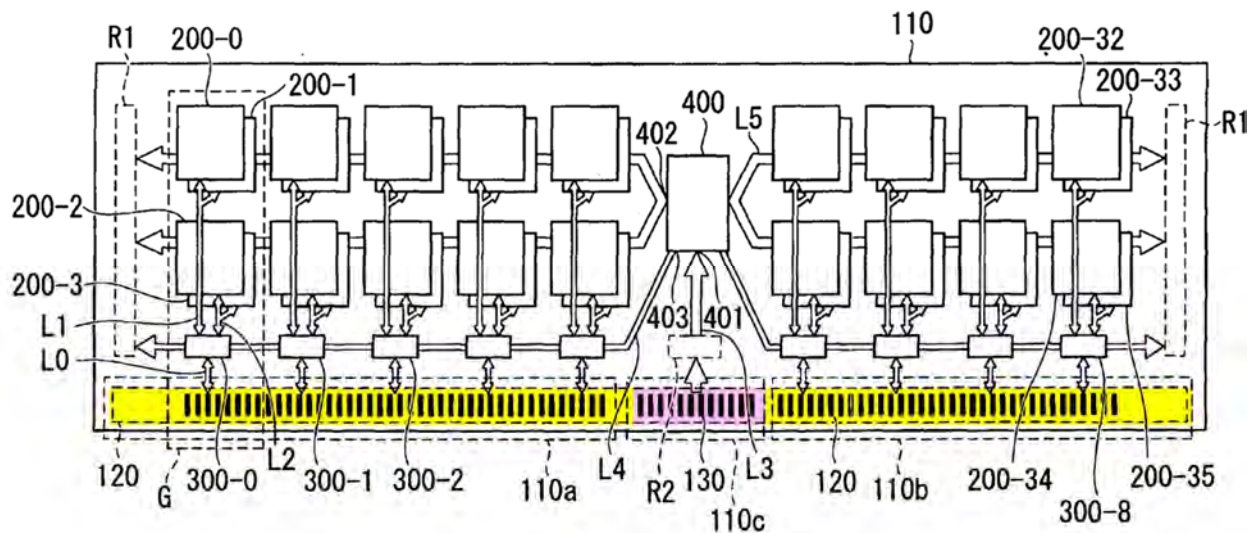
Ex. 1005, Fig. 1 (annotated), [0054]–[0055], [0075]. Connectors 120–130 connect to a set of “*signal lines*” shown above as L0 and L3. Ex. 1005, [0054]–[0055], [0075]. Based on these disclosures, a POSITA would have recognized that the L3 signal line represents the “*control/address signal lines*” and L0 signal lines represent the “*data/strobe signal lines.*” Ex. 1005, [0054]–[0055], [0075].

81. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses the preamble.

b. “a module board having edge connections for coupling to respective signal lines in the memory bus”

82. Osanai discloses “*a module board having edge connections for coupling to respective signal lines in the memory bus.*”

83. Figure 1 of Osanai shows that memory module 100 includes data connectors 120 and 130 (the “*edge connections*”). As shown in Figure 1 below, a POSITA would have recognized that these connectors are located at the edge of module 110 and connect the signal lines L0 and L3 to line 23 of the memory bus so they satisfy the claimed “*edge connections*”:



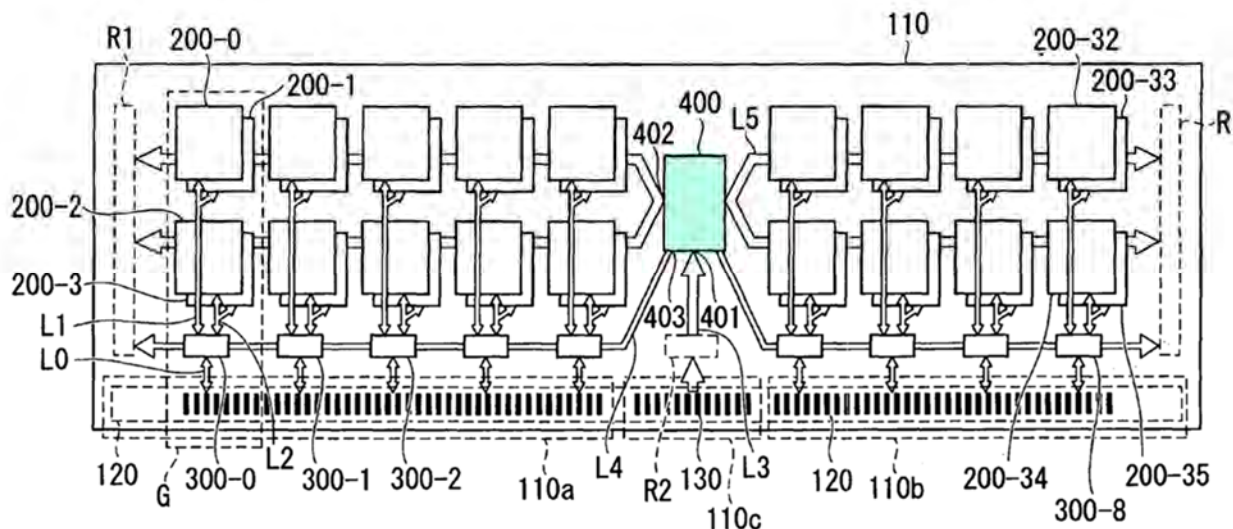
Ex, 1005, [0054] (“The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between memory module 100 and the controller [12].”).

84. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

- c. “a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals, the module control device being further configured to receive a system clock signal and output a module clock signal”

85. Osanai discloses this limitation.

86. Figure 1 of Osanai shows a command/address/control register buffer 400 (“module control device”) mounted on memory module 100, shown below:



Osanai further discloses that the command/address/control register buffer 400 receives various command signals from the memory controller (“receiv[ing] system command signals for memory operations from the memory controller”):

[t]he command/address/control register buffer 400

receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200.

Ex. 1005, [0066]; *see also id.* Fig. 6, path 401 to 402, [0101]–[0103].

87. Osanai's memory controller 12 sends command/address/control signals to buffer 400, which are "*system command signals*." Ex. 1005, [0053], [0102]. In response, Osanai's command/address/control register buffer 400 ("*module control device*") outputs "*module command*" and "*control signals*," such as address (ADD), Command(CMD), Control(CTRL), and Clock (CK) (each being a "*module command signal*") as well as control signal DRC ("*module control signal*"). Ex. 1005, Fig. 6, [0103-0105]. These signals are shown in Figure 6 below:

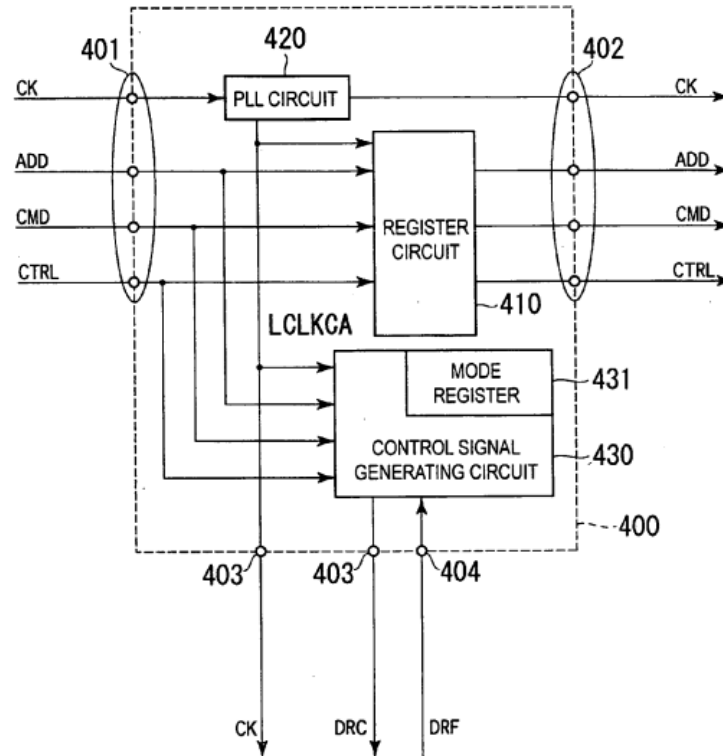


FIG.6

See Ex. 1005, [0103]. In addition, the command/address/control register buffer 400 also outputs DRC (Data Register Control), which are also “*module control*” and “*command signals*,” to the DRC circuit 320 to control operation of the input and output buffers of the data register buffer 300, *e.g.*, adjustment of output impedance and/or control of ODT operations signals. Ex. 1005, [0066], [0105], [0106]. (“In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 as a part of the control signal

DRC.”); [0132]; *see* Ex. 1005, Figs. 4 and 6, [0078]–[0084], [0093], [0103]. These DRC signals are also considered both a “*module control*” and “*command signals*.” *See* Ex. 1005, Figs. 4 and 6, [0078]–[0084], [0093], [0103], [0106]. These examples of Osanai disclosing both a “*module control*” and “*command signals*” are consistent with how the ’608 patent describes “*command signals*” and “*control signals*.” *See* Ex. 1001, 7:59-63 (explaining what constitutes memory command signals); *id.*, 3:25-50, 4:65-5:10. Osanai’s command/address/control register buffer 400 is configured to receive these signals for “*memory operations*,” such as a read operation. *See id.* Figs. 7, 11, 12, 15, and 17, [0112-114], [0129-0136] (read operations), [0137]–[0142] (write operations); *see also id.*, [0080] and [0085]. Accordingly, a POSITA would thus have understood that Osanai discloses the claimed “*module control*” and “*command signals*.”

88. The ’608 patent confirms that these signals described by Osanai are the claimed “*module control*” and “*command signals*” for the first memory operation (a read operation). Ex. 1001, 3:25-50, 5:11–57. The ’608 patent explains that the claimed signals include both signals generated from both clock signals and C/A signals:

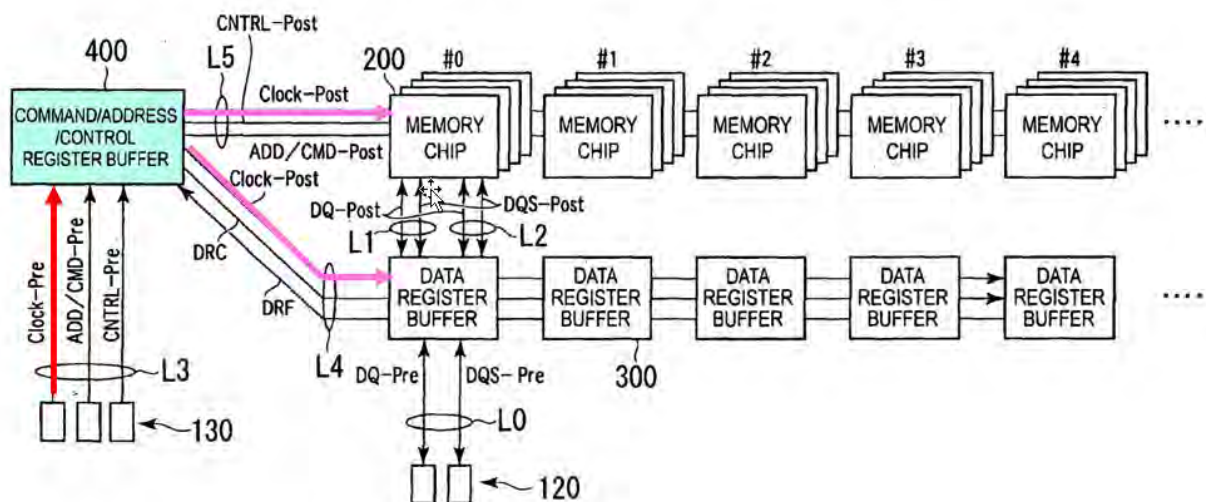
The memory module is operable to perform memory

operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller.

Ex. 1001, 3:29-44. Based on this disclosure, a POSITA would have recognized that the '608 patent confirms that the above signals described in Osanai, *see* Ex. 1005, [0078]–[0084], [0093], [0103], [0106], are the same claimed “*module control signals*” described by the '608 Patent. Ex. 1001, 3:25-50.

89. Osanai further discloses “*the module control device being further configured to receive a system clock signal and output a module clock signal.*”

90. As shown in annotated Figure 7, Osanai's command/address/control register buffer 400 ("module control device") also receives a Clock-Pre Signal ("system clock signal") (shown as red arrow) and outputs a Clock-Post signal ("a module clock signal") (shown as pink arrow):



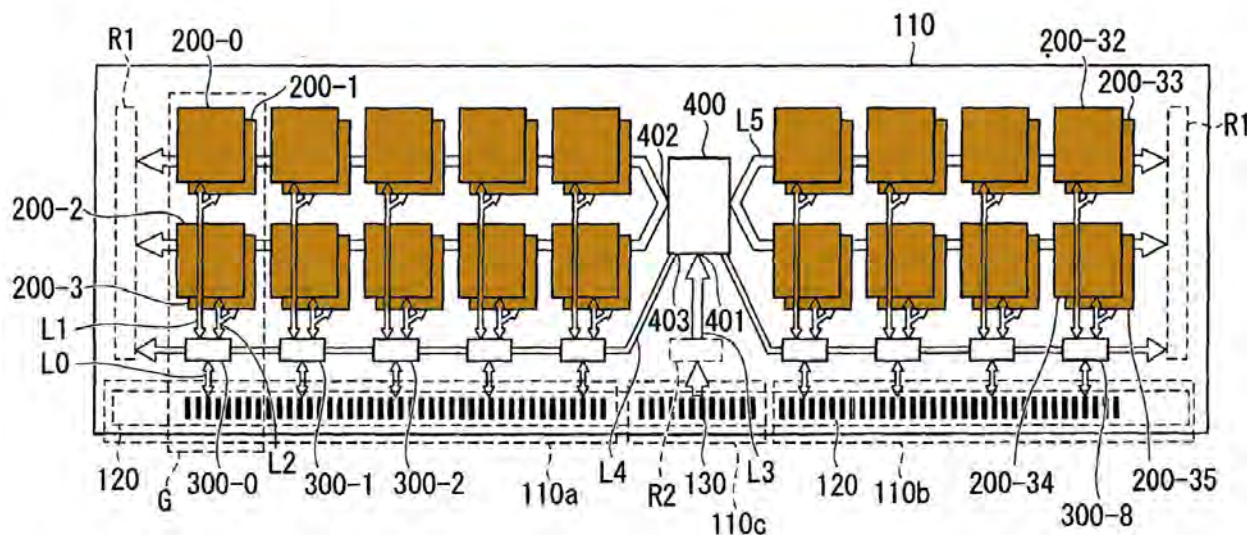
Ex. 1005, Fig. 7 (annotated), [0114]; see Ex. 1005, Figs. 6–7, [0104], [0112]–[0113]. A POSITA would have recognized that Osanai's command/address/control register buffer 400 outputs the same Clock-Post signal to the data buffer and memory chips. See Ex. 1005, Figs. 4–6, 7, 19, [0104], [0112]–[0113], [0154]. Such a person would have recognized that these CLK signals output to the memory chips and the data buffer have the same timing. See Ex. 1005, Figs. 12, 15, 17 and 19, [0154].

91. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

- d. **“memory devices mounted on the module board and configured to receive the module command signals and the module clock signal and to perform the first memory operation in response to the module command signals;”**

92. Claim 1 recites “*memory devices mounted on the module board and configured to receive the module command signals and the module clock signal and to perform the first memory operation in response to the module command signals.*” Osanai discloses this limitation.

93. Figure 1 of Osanai discloses multiple memory chips 200 (“*memory device*”) mounted on the memory module 100, shown below:



Ex. 1005, Fig. 1 (annotated). These memory chips 200 perform memory operations as instructed. Ex. 1005, [0060] (“An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer 400. Details on the memory chip 200 will be described later.”). To do so, a POSITA would have understood that Osanai’s memory chips receive both CNTRL-Post signals (“*module command signals*”) and Clock-post signals (“*clock signals*”) to instruct them to perform operations. Ex. 1005, [0112] (“The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from the command/address/control register buffer 400.”); *see id.* Figs. 6 and 7, [0104], [0101]–[0111], [0113]–[0114]. Such memory operations include both read and write operations. Ex. 1005, [0060], [0085], [0090], [0128]–[0142].

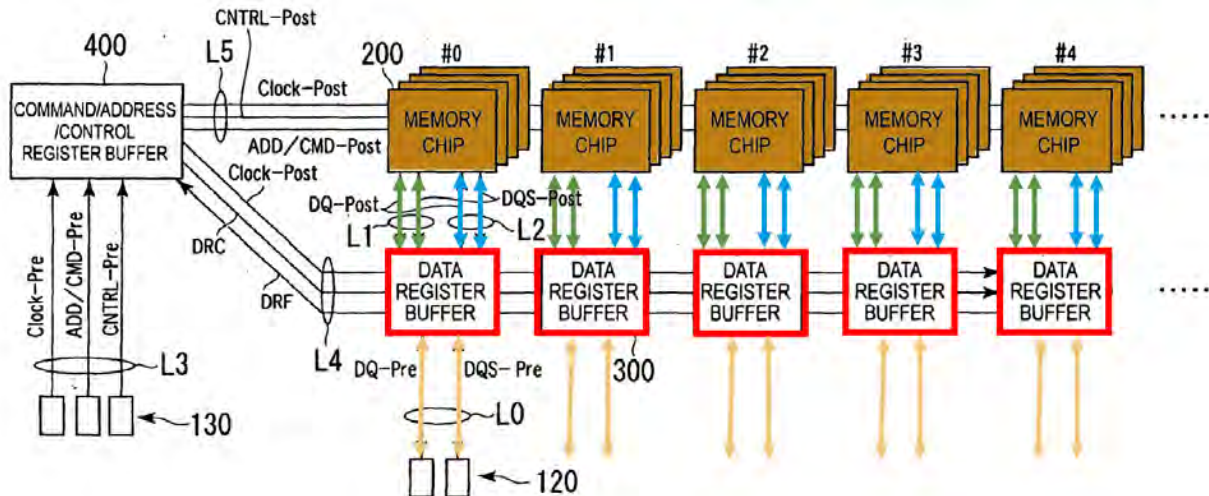
94. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

e. “the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines”

95. Claim 1 recites “*the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines.*” Osanai teaches this limitation.

96. Osanai’s memory chips 200 are grouped into sets making “*a plurality of sets of memory devices.*” Ex. 1005, [0058] (“In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other.”). Each group has its own respective set of data/strobe signal lines, L0 data lines. Lines L1 and L2 are coupled to the memory bus via their data buffer 300 and respective connectors in Line L0. See Ex. 1005, Figs. 5 and 7.

97. Annotated Figure 7 of Osanai illustrates all these lines:



Ex. 1005, Fig. 7, [0109]. Accordingly, memory chip sets communicate with their respective data register buffer and have a corresponding set of L0 data lines (a “*plurality of sets of data/strobe data/strobe signal lines*”).

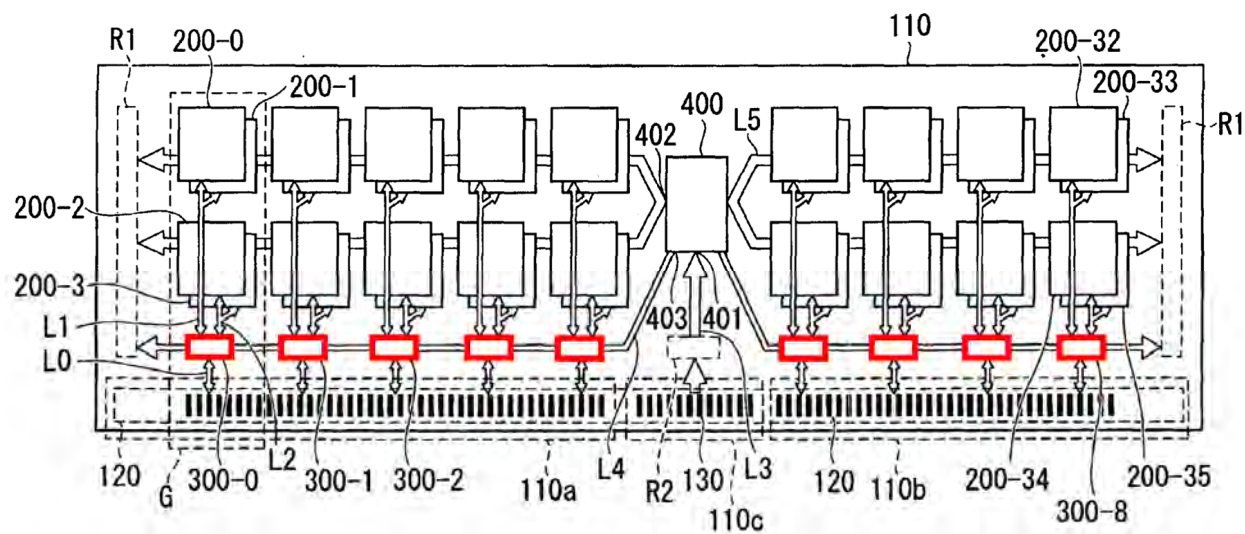
98. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

f. “a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board;”

99. Claim 1 recites “a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each

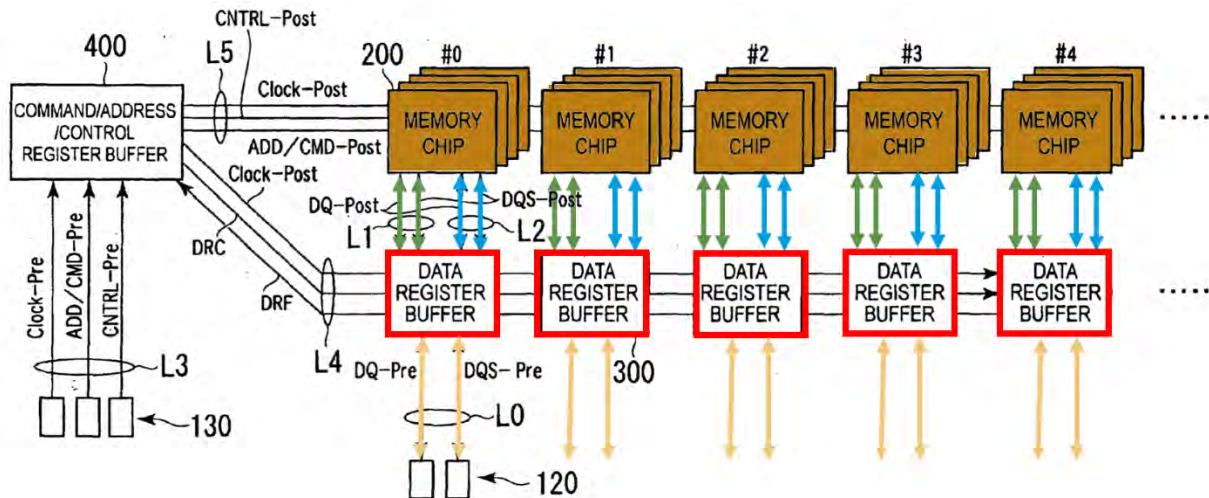
respective buffer circuit of the plurality of buffer circuits is mounted on the module board.”

100. Figure 1 of Osanai discloses data register buffers 300 that are mounted on the memory module 100 (“*wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board*”), shown below:



Ex. 1005, Fig. 1 (annotated), [0052] (“Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8.”).

101. Likewise, Figure 7 shows that each data register buffer 300 is paired with a set of memory chips and L0 data lines (“*respective sets of the plurality of sets of data/strobe signal lines*”):



Ex. 1005, Fig. 7 (annotated), [0061]–[0062], [0109]; *see id.*, Fig. 1.

102. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

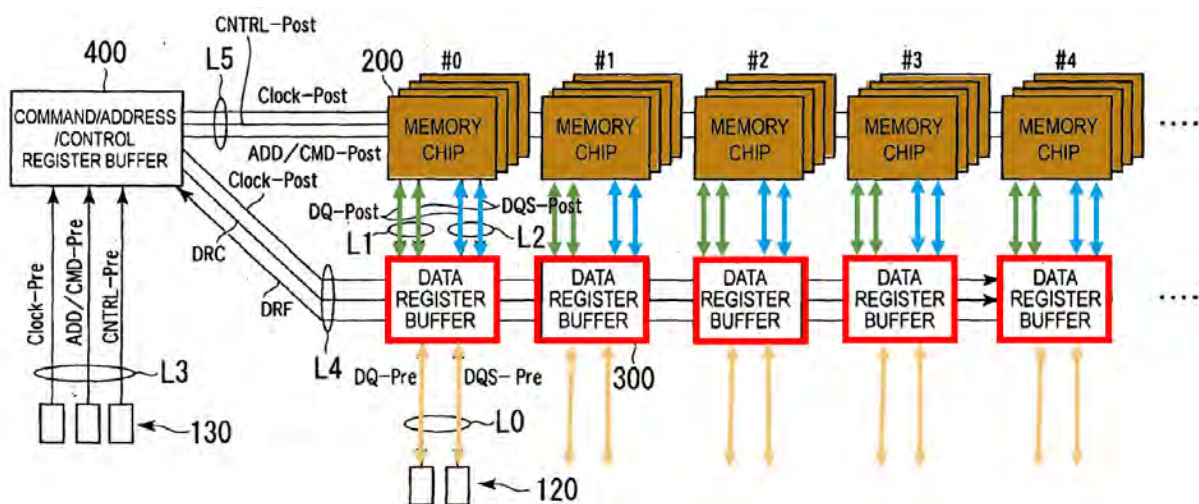
- g. “[wherein each respective buffer circuit of the plurality of buffer circuits is] coupled between a respective set of data/strobe signal lines and a respective set of memory devices and configured to receive the module control signals and the module clock signal;”

103. Claim 1 recites “*wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective*

set of data/strobe signal lines and a respective set of memory devices and configured to receive the module control signals and the module clock signal.”

Osanai discloses this limitation.

104. Figures 1 and 7 show that each data register buffer 300 (a “buffer circuit”) is mounted on the module between L0 data lines (“respective sets of the plurality of set of data/strobe signal lines”) and its respective memory chip group (e.g., shown as #0 through #4 below and additional groups are unshown) (each being a “respective set of memory devices”), shown below:



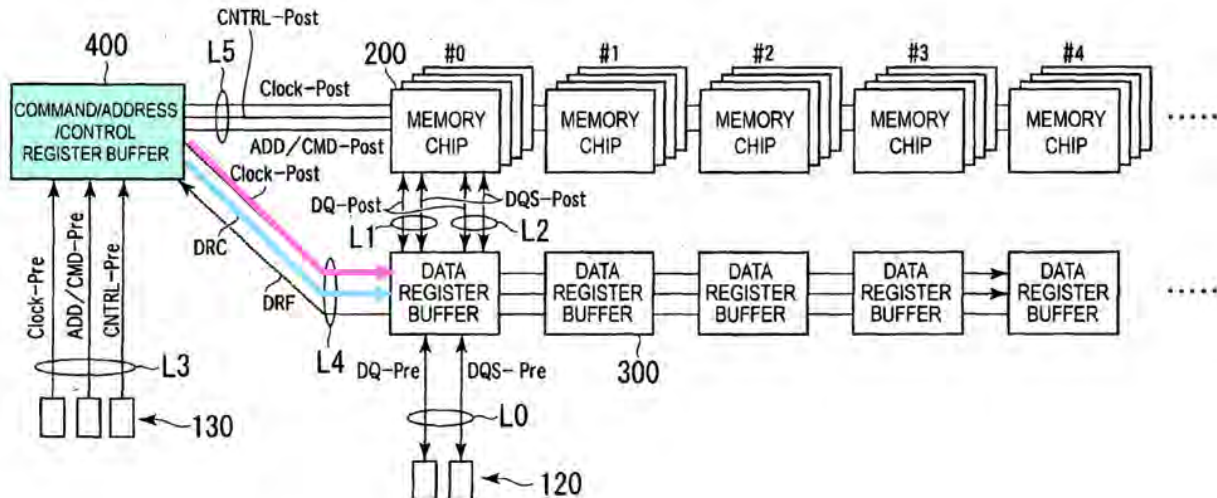
Id. at Fig. 7 (annotated), [0109]; see *id.*, Fig. 1, Claim 8. This functionality of “data/strobe signal lines,” which a part of the claimed “memory bus,” is consistent with how the ’608 patent describes those lines. See Ex. 1001, 4:49-53 (“in the

context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller”).

105. As shown in annotated Figure 7 above, memory chips are organized into groups, thereby making a “*respective set of memory devices.*” Ex. 1005, [0057]–[0058]. In describing Figure 7, Osanai states that “the data register buffer 300 and [each group of] memory chips 200... are connected to each other with the data line L1 or L2.” Ex. 1005, [0109]; *see also* Fig. 1. Lines L1 and L2 are coupled to the memory bus via their respective connector from L0 data lines, which are “*respective sets of the plurality of set of data/strobe signal lines.*” *See* Ex. 1005, Figs. 5 and 7, [0109].

106. Osanai further discloses “*wherein each respective buffer circuit of the plurality of buffer circuits is... configured to receive the module control signals and the module clock signal.*”

107. As shown in annotated Figure 7, Osanai’s command/address/control register buffer 400 (“*module control device*”) outputs a Clock-Post signal (“*a module clock signal*”) (shown as pink arrow) and DRC (“*module control signals*”) (shown as blue arrow):



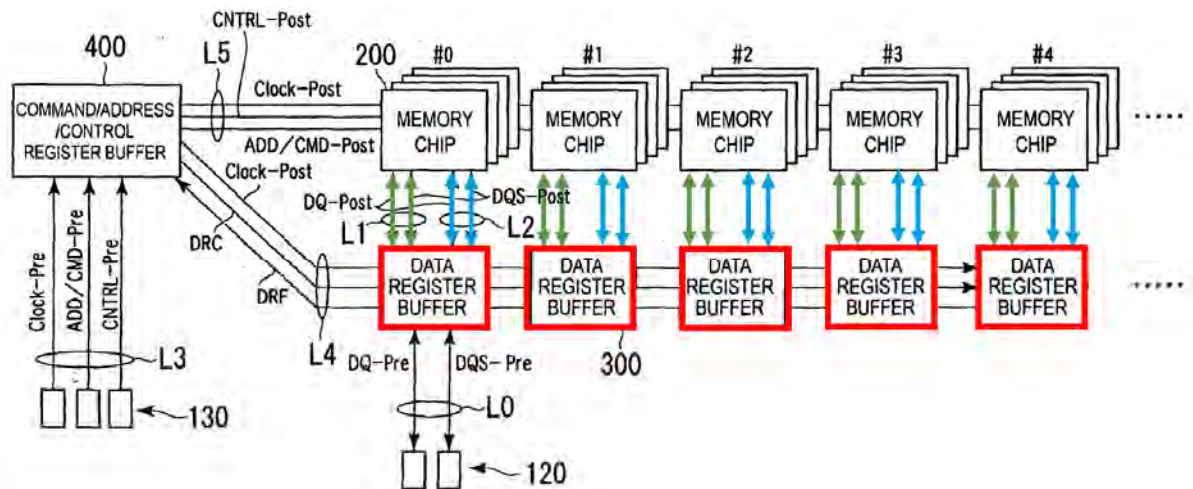
Ex. 1005, Fig. 7 (annotated), [0114]; see Ex. 1005, Figs. 6–7, [0104], [0112]–[0113]. Based on Osanai’s disclosures, a POSITA would have recognized that Osanai’s command/address/control register buffer 400 outputs clock signals outputted to the data buffer. See Ex. 1005, Figs. 6 and 7, [0093], [0104], [0112]–[0113]. Such a person would have recognized that the command/address/control register buffer 400 also outputs “module control signals,” such as Read commands, to the data register 300 as part of the control signal DRC. See Ex. 1005, [0154], [0157], [0164].

108. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

h. “each respective buffer circuit includ[es] a data path corresponding to each data signal line in the respective set of data/strobe signal lines”

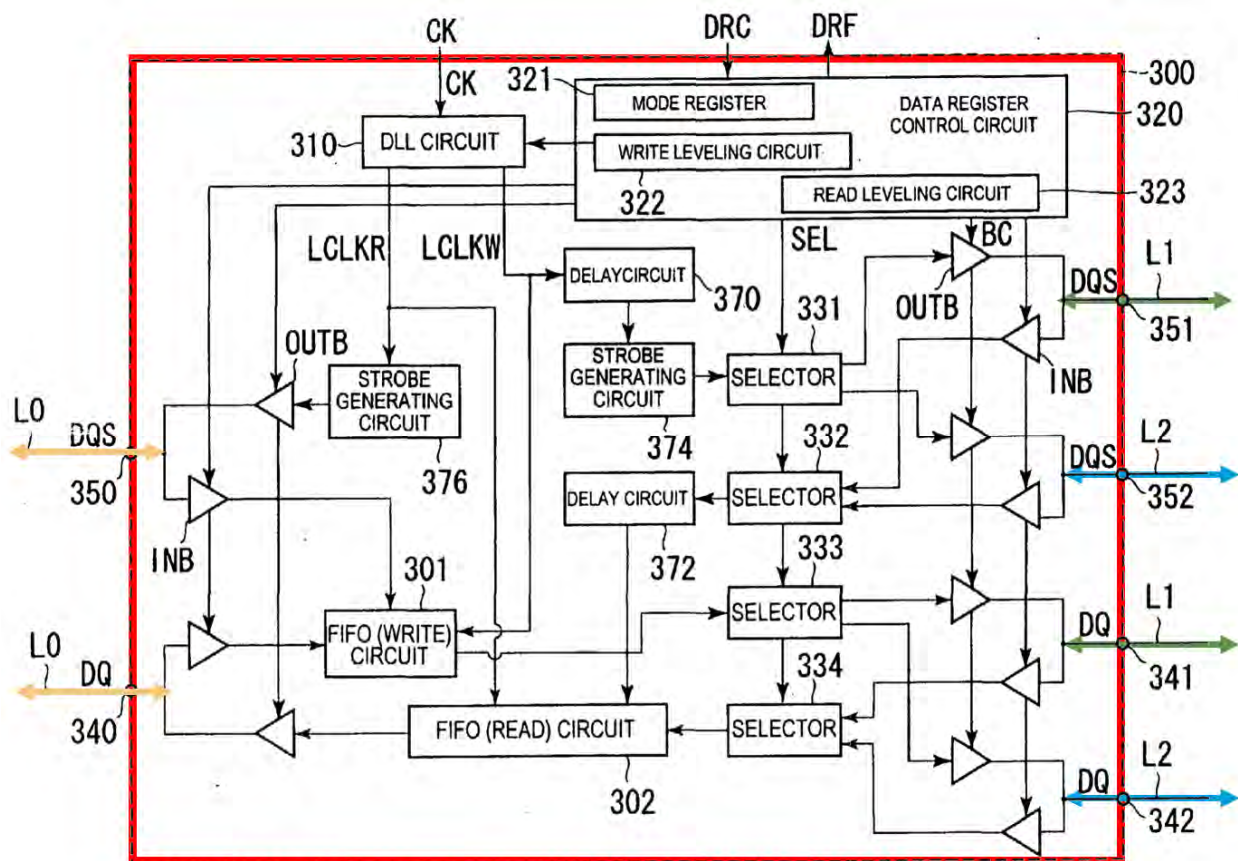
109. Osanai discloses this limitation.

110. Figure 7 shows that each data register buffer 300 has “*data paths*” that correspond to each data signal line, L1 and L2 data lines, connected to each memory chip group (e.g., shown as #0 through #4 below and additional groups are unshown), shown below:



Id. at Fig. 7 (annotated), [0109] (“The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line[s] L1 or L2.”); *see also* Fig. 1 (showing multiple data register buffers). In addition, a POSITA would have understood these data paths include circuitry

components in the data register buffer 300 that connect each L0 data lines (“respective set of data/strobe signal lines”) at terminals 340 and 350, shown in Figure 5 below:



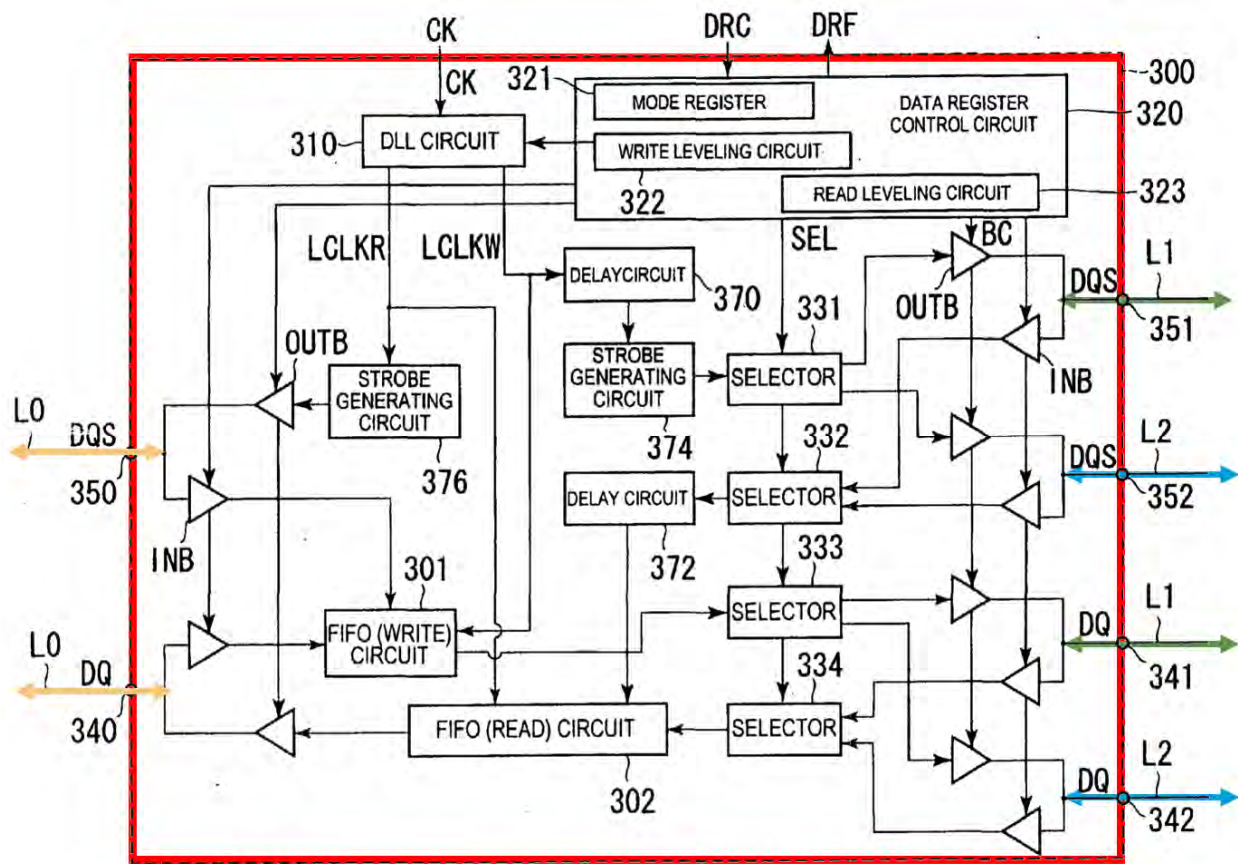
Ex. 1005, Fig. 5 (annotated), [0109].

111. Using L1 or L2, data register buffer 300 transmits “data and strobe signals.” Osanai explains as much:

“In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of

data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and ***a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.***”

Ex. 1005, [0109] (emphasis added). Specifically, data buffer 300 receives DQS-Pre signals from data line L0 and outputs DQS-Post over data lines L1 or L2. See Ex. 1005, [0109]. Using the same data lines, data register buffer 300 also sends DQ-Post after processing DQ-Pre received over data line L0. Ex. 1005, [0109]. Both L1 and L2 data paths are shown in Figure 5, shown below:



Accordingly, DQ-Post and DQS-Post are “data and strobe signals.”

112. Based on these disclosures, a POSITA would have understood that these two signals, DQ-Post and DQS-Post, together are “data and strobe signals.” Osanai states that “[a]n operation of the memory chip 200 is controlled based on” multiple signals, including DQ-Post and DQS-Post signals. Ex. 1005, [0060]. Further, both these signals are associated with memory read and write operations. See Ex. 1005, [0090]; [0097], [0109]–[0110].

113. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

- i. **“and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit;”**

114. Osanai discloses this limitation.

115. Figure 5 of Osanai illustrates a data register buffer 300 that includes a data register control circuit 320 and DLL Circuit (collectively, the “*command processing circuit*”) that uses received DRC signals and clock signals to select the appropriate data path, shown below:

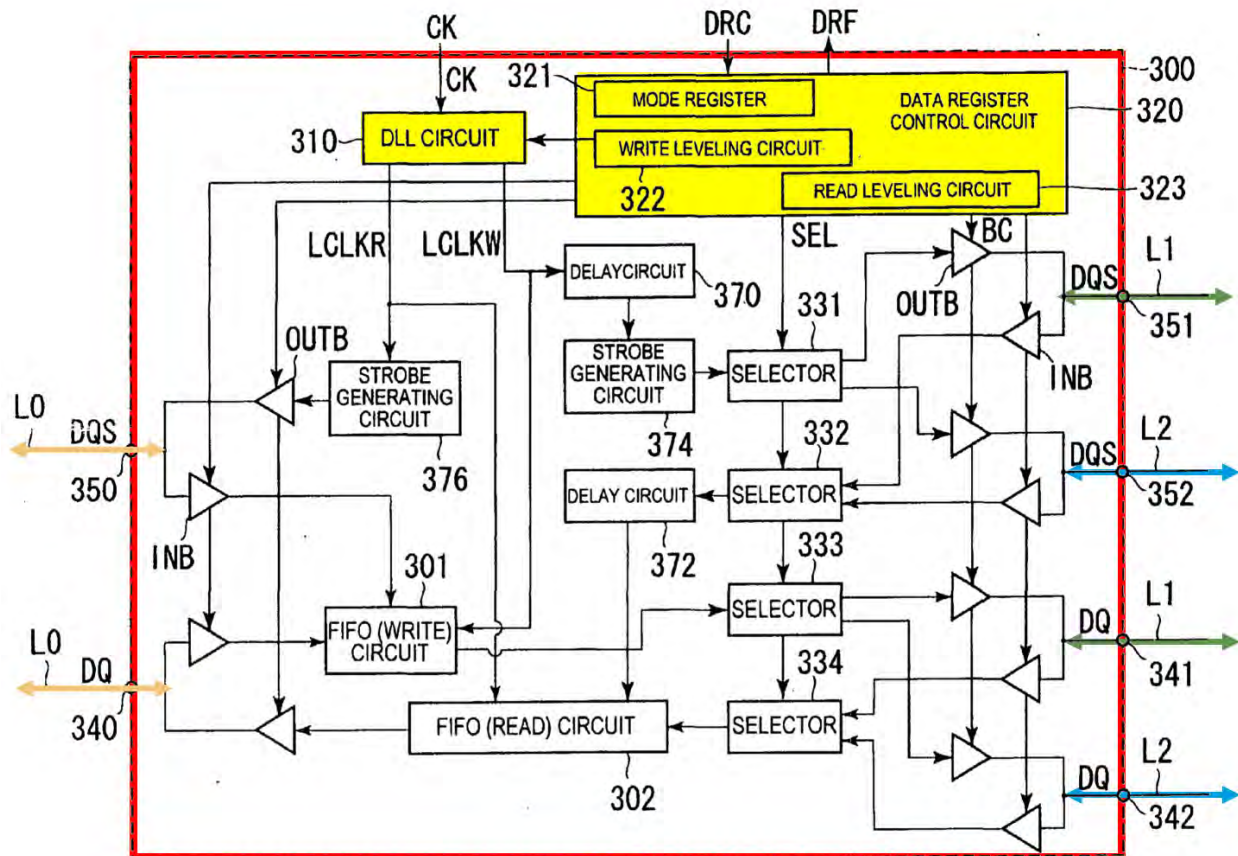


FIG.5

Id., Fig. 5 (annotated), [0094]; *see id.*, Fig. 2, [0094], [0096]; *see also id.*, [0158], [0163]. This control circuit “controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400.” Ex. 1005, [0094] (explaining how data path is selected using SEL and BC signals); [0132] (“In addition, the command/address/control register buffer 400 supplies a read command *Read* to the data register buffer 300 as a part of the control signal DRC”) (emphasis added). Using decoded DRC signals

(“*module control signals*”), the data register buffer 300 enables different data paths (or “*controls the data path*”) for reading and writing operations, respectively. See Ex. 1005, [0106] (“The control signal DRC includes ... a signal indicating a direction of transmitting and receiving data”); see also *id.*, [0094], [0105]. A POSITA would have understood these disclosures to teach that the data register control circuit 320 selects (or “*controls*”) certain paths using SEL, INB, and OUTB signals, as well as selectors 331–334, which supplies data DQ to input or output terminals, 341 and 342, to certain memory chips 200. Ex. 1005, [0094], [0097]. This interpretation is consistent with how the ’608 patent describes “*control[ing] a data path.*” See Ex. 1001, 5:46–49, 12:7–26, 18:15–20. Also, Osanai’s DLL circuit 310 receives this module (CK) signal and uses that signal to generate two local clocks: one for read operations (LCLKR) and another for write operations (LCLKW). Ex. 1005, [0090]. Based on these disclosures, a POSITA would have recognized the data path would have used the appropriate clocks in their respective read/write operation data paths. Accordingly, such a person would have recognized that Osanai’s data register buffer 300 selects data paths “*in accordance with the module control signals and the module clock signal.*”

116. Any data path selected by Osanai's data register control circuit 320 includes a "*tristate buffer*." For example, Osanai discloses tristate buffers, such as the OUTB buffer. Ex. 1005, [0094], Fig. 5. A POSITA would have understood that the buffers from these disclosures are tristate buffers because each has three states—namely, on off, or electrically disconnected. Ex. 1015, p. 6. For example, such a person would have recognized that, in addition to its on/off states, the buffers used for read operations over line 340 would necessarily need to be in a high impedance state during write operations. See Ex. 1005, Figs. 5 and 11, [0129]–[0136] (Figure 11 demonstrates that the buffer for the DQ read output to the memory controller (Fig. 5, node 340) is not driven for a portion of time by the OUTB tristate buffer in Fig. 5); see also Ex. 1005, [0090]–[0094], [0097]–[0098], [0105]–[0106]. A POSITA would have recognized that using this high impedance state ensures that the buffer does not overload or interfere with the other buffer operations. Such person would also have recognized that these buffers are part of data paths controlled by data register control circuit 320, (see Ex. 1005, [0090]–[0094], [0097]–[0098], [0105]–[0106]), and connected to L1 and L2 data lines that connect to memory chips 200, (see Ex. 1005, Fig. 1). Accordingly, a POSITA would have understood that Osanai's data register buffer 300 includes "*data*

path(s) [that] correspond[] to the each data signal line [and] include[] at least one tristate buffer controlled by the command processing circuit.”

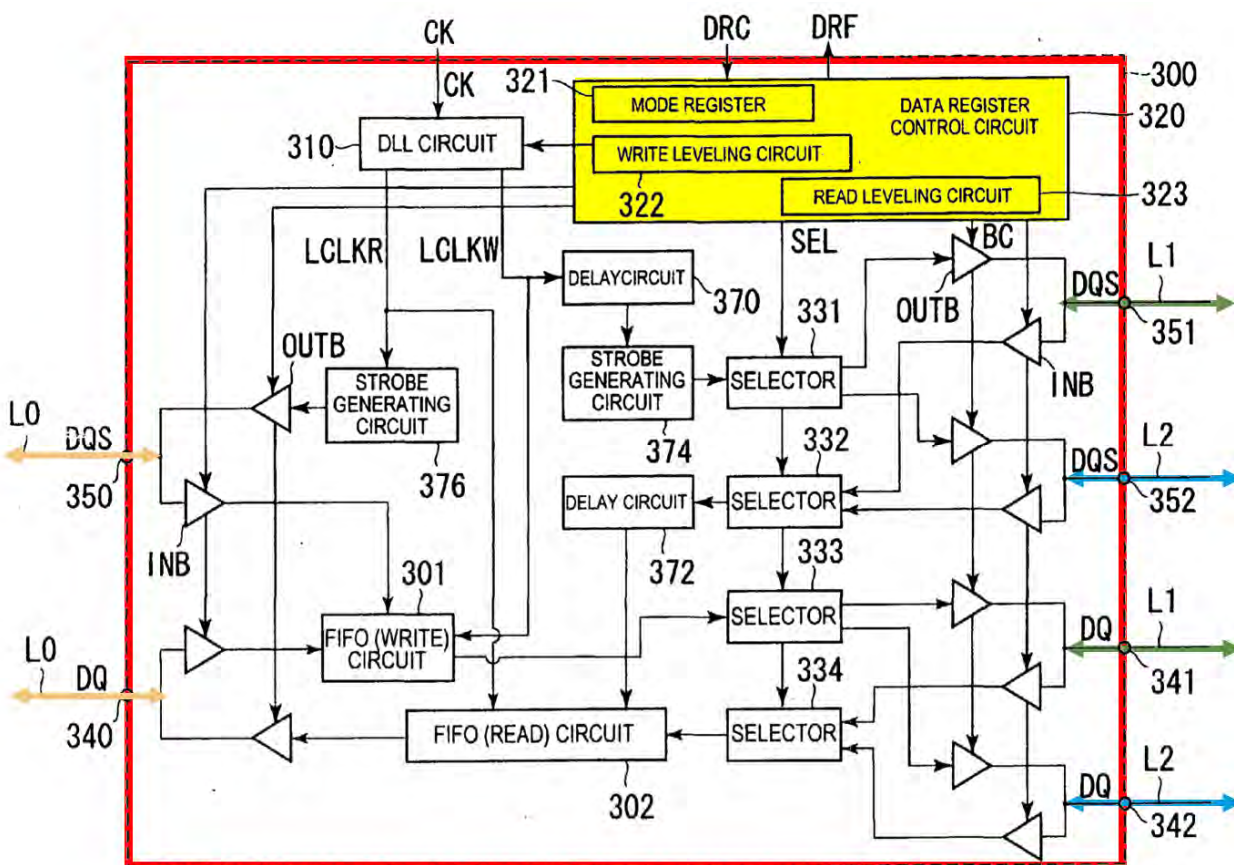
117. Inside control circuit 320, and as shown above in annotated Figure 5, Osanai discloses read leveling and write leveling circuits 323 and 322. *Id.*, Fig. 5, [0096] (“Furthermore, the data register control circuit **320** includes a write leveling circuit **322** and a read leveling circuit **323**. The write leveling circuit **322** is a circuit for *performing a write leveling operation*, and the read leveling circuit **323** is a circuit for *performing a read leveling operation*.”) (emphasis added); *see also id.*, [0158], [0163]. Based on these disclosures, a POSITA would have recognized that this data register control circuit 320 that both read and write leveling circuitries compensate for propagation delays caused by some memory chips being placed farther away from their respective data register buffers. Ex. 1005, [0146] (“The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal.”).

118. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

j. **“a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals”**

119. Osanai discloses this limitation.

120. Osanai's control circuit 320 further includes read leveling and write leveling circuits 322 and 323, shown below:



121. Osanai discloses both read and write leveling techniques, which are performed by circuitry 323 and 322 located in the data register control circuit 320

(part of the claimed “*command processing circuit*”). Osanai recites that “the data register control circuit 320 includes a write leveling circuit 322 and a read leveling circuit 323...[which the] write leveling circuit 322 is a circuit for performing a write leveling operation, and the read leveling circuit 323 is a circuit for performing a read leveling operation.” *Id.*, [0096]; *see also id.*, [0146]–[0164], Figs. 14A–17. Osanai’s techniques make timing adjustments so that signals between “the memory chips 200 and the data register buffer 300” are sent at the appropriate time. Ex. 1005, [0110]; *see also id.*, [0096], [0146].

122. To make these adjustments, the read and write leveling circuitry and DLL Circuit 310 (part of the claimed “*command processing circuit*”) use the module clock (CK) signal sent from the command/address/control register buffer 400. *See* Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. A POSITA would have understood that Osanai’s DLL circuit 310 receives this module (CK) signal, which uses that signal to generate two local clocks: one for read operations (LCLKR) and another for write operations (LCLKW). Ex. 1005, [0090], [0093].

123. Using these clock signals, a “timing adjustment”—that is, an added time delay—is then used compensate for propagation delays. Ex. 1005, [0110]; *see id.*, [0149]–[0157]. For example, and during the write leveling operation,

Osanai's "data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK," which is supplied by command/address/control register buffer 400. *Id.* [0149]. Because of differing propagation delays, however, "input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip **200** side." *Id.* To correct this timing error, the write leveling circuitry 322 delays the output timing of the DQS sent from data register buffer 300, thus creating DQS-Post ("*delay[ing] a signal through the data path by an amount determined by the command processing circuit*"). *Id.* [0151]–[0152]. A similar read leveling process results in, signals being delayed. Ex. 1005, [0153]–[0157]. Using these leveling techniques, the leveling circuitry (or "*delay circuit*") "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal." Ex. 1005, [0146], [0149]–[0157]. This is consistent with the write leveling concept described in the JEDEC standard. Ex. 1013, p. 6 ("The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back

CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected.”). Using these leveling techniques, the leveling circuitry “adjust[s] a write timing or a read timing in consideration of a propagation time of a signal.” Ex. 1005, [0146], [0149]–[0157].

124. Based on these disclosures, a POSITA would have recognized that specific delays were chosen “*in response to at least one of the module control signals.*” For example, the specific delay chosen depends on whether the DRC mode that represents a read operation or write operations (one type of “module control signals”). Ex. 1005, [0132] (“In addition, the command/address/control register buffer 400 *supplies a read command Read to the data register buffer 300 as a part of the control signal DRC.*”) (emphasis added); *see id.*, Fig. 7, [0094], [0154]–[0157], [0164]. Alternatively, such a person would have recognized that read and write leveling circuitry use the module clock (CK) signal (another type of “*module control signal*”) to determine the delay. *See* Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. Consequently, a POSITA would have understood that Osanai’s control circuit 320 determines the delay “*amount... in response to at least one of the module control signals.*”

125. For these reasons, a person of ordinary skill in the art would have understood that Osanai discloses this limitation.

2. Claim 4

126. Claim 4 depends on claim 1 and recites “*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.*” As I explained above, see § IX.A.1, claim 1 is anticipated by Osanai. The additional element recited in claim 4 would have likewise been anticipated by Osanai.

127. Osanai’s data register buffer 300 has a data width of 1 byte. Ex. 1005, [0091]. Osanai expressly discloses that “a single data register buffer 300 inputs and outputs 1-byte data....” *Id.* Each of Osanai’s memory devices also has a data width of eight bits (“*each of the memory devices has a data width of 1 byte*”). Ex. 1005, [0059] (“An arrow of each of the data lines L1 and L2 shown in Fig. 1 indicates a line of 1 byte (8 bits)).”). Osanai thus discloses that “*each of the plurality of buffer circuits has a data width of 1 byte*” and “*each of the memory devices has a data width of 1 byte.*”

B. Claims 1–5 are rendered obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006)

128. As I explained above, Claim 1 is anticipated by Osanai. Claims 1–5 are also obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006). For the reasons below, a POSITA considering the teachings of these references would have found the claimed subject matter obvious.

1. Claim 1: “*delay[ing] a signal through the data path by an amount determined... in response to at least one of the module control signals*”

129. To the extent that one argues that Osanai does not expressly disclose discloses “*delay[ing] a signal through the data path by an amount determined...in response to at least one of the module control signals,*” a POSITA would have determined that this feature was rendered obvious based on the teachings of Tokuhiro.

i. Tokuhiro discloses a technique that “*delay[s] a signal through the data path by an amount determined... in response to at least one of the control signals.*”

130. Tokuhiro discloses read and write leveling techniques. Tokuhiro explains that such leveling techniques are necessary to compensate for different propagation delays. Ex. 1006, 1:63–2:9. Specifically, Tokuhiro states that

propagation delays differ because memory units have different wiring lengths. *Id.* To compensate for these different delays, “the difference in the delay time caused in the write operations between the memory controller 90 and the plurality of SDRAMs 92 is adjusted by employing the write leveling function.” *Id.*, 2:46–49. Tokuhiro recognizes that the “delay [determined from the write leveling function] may affect [] reading data from the SDRAM 92,” as well. *Id.*, 3:9–12.

131. Tokuhiro teaches a delay unit that calculates a first delay time determined during a write operation to use in its calculation of a second delay time used for a read operation (“*delay[ing] a signal through a data path by an amount determined.*”). *Id.* 3:16–26 (“[A] first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time.”). Specifically, Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation:

Because the wirings for connection between the memory controller 12 and the DIMM 11 are formed in the same length, ... ***In other words, the second delay time $Dt2$ for the data signal DQ input from the SDRAM can be***

calculated by using the first delay time Dt1 that has been set in the write leveling. Accordingly, in the second delay time control unit 24, the second delay time Dt2-x corresponding to one SDRAM-x is set by using the above-mentioned formula (3-5) so that the sum of the first delay time Dt1-x and the second delay time Dt2-x both corresponding to the relevant SDRAM-x is equal to a preset value.

id., at 16:1–28 (emphases added). Based on these disclosures, a POSITA would have recognized that, because Tokuhiro uses timing information determined during the write operation for a subsequent read operation, the write operation necessarily occurred before the read operation.

132. A POSITA would have recognized that Tokuhiro’s delay technique determines delay times for read and write operations using “control signals.” See Ex. 1006, 9:1–32, 11:5–46, 12:42–58, 14:59–15:15, 16:47–17:11, 23:23–40, 26:21–46. Tokuhiro explains as much:

Further, the first delay time control unit 23 outputs *the respective first control signals d1* to the first variable delay circuits DW-1 to DW-n so that the set first delay times Dt1-1 to Dt1-n are obtained. In accordance with the first control signals d1, the first variable delay circuits

DW-1 to DW-n delay the data strobe signals DQS-1 to DQS-n by the first delay times Dt1-1 to Dt1-n, respectively....Further, the second delay time control unit **24 outputs the respective second control signals d2** to the second variable delay circuits DR-1 to DR-n so that the set second delay times Dt2-1 to Dt2-n are obtained. In accordance with the second control signals d2, the second variable delay circuits DR-1 to DR-n delay the data signals DQ-1 to DQ-n by the second delay times Dt2-1 to Dt2-n, respectively.

Ex. 1006, 14:59–15:53; *see id.*, 9:1–32, 11:5–46, 12:42–58, 16:47–17:11, 23:23–40, 26:21–46. Based on these disclosures, a POSITA would have recognized that Tokuhiro’s technique “*delay[s] a signal through a data path by an amount determined... in response to at least one of the... control signals.*”

133. Based on the above disclosures, a POSITA would have recognized that the challenged claims encompass Tokuhiro’s technique, which mirrors the ’608 patent’s description of how the timing information is obtained. The ’608 patent describes that timing information is determined during a write operation and used to determine a delay in a subsequent read operation:

Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, *during a write*

operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This *time interval is used during a subsequent read operation* to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

Ex. 1001, 4:9–19; (emphasis added); *see also id.*, Claim 2. As I explained above, Tokuhito likewise discloses that timing information determined during a write operation is used in determining a delay for subsequent read operations. Ex. 1006, 3:16–26, 16:14–23. Accordingly, and as I explained above, *see* § VI.C, a POSITA would have recognized that Tokuhito’s technique teaches the supposed novel claim feature described in the examiner’s reasons for allowance.

134. For these reasons, Tokuhito thus discloses a technique that obtains timing information that is used to “*delay a signal through the data path by an amount determined...in response to at least one of the... control signals.*”

ii. *It would have been obvious to use Tokuhiro's technique in Osanai's buffer leveling circuitries*

135. Osanai and Tokuhiro are analogous art to the '608 patent. Both are analogous art because they are directed toward the same field of endeavor—namely, memory modules. Ex. 1001, 1:37–39 (“The disclosures herein are related generally to memory modules....”); Ex. 1005, [0001] (“The present invention relates to a memory module....”), Ex. 1006, 1:15–20 (“The memory control circuit, delay time control device, and delay time control method relate to a technique for controlling read/write operations for a plurality of memories....”). Moreover, both are analogous art because they are reasonably pertinent to a problem described by the '608 patent: “as memory operating speed and memory density continue to increase[s], however, such [read and write] leveling mechanisms are also insufficient to [ensure] proper timing of the control and/or data signals....” Ex. 1001, 2:32–36; Ex. 1005, [0110] (“Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300....”); Ex. 1006, 1:15–20.

136. A POSITA would have been motivated to incorporate Tokuhiro's leveling technique in Osanai's data register control circuit 320 for three reasons. Each reason is discussed further below.

137. First, it would have been obvious to use Tokuhiro's teaching in Osanai's data register buffer to achieve the same benefit achieved by Tokuhiro's device, i.e., reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling. A POSITA would have recognized that incorporating Tokuhiro's technique would provide the same benefit to Osanai's memory module. Such a modification to Osanai's data register buffer would not be beyond the skill of an ordinary artisan. A POSITA would have recognized that such a modification would have been obvious.

138. Second, a POSITA would have been motivated to modify Osanai's data register buffer to incorporate Tokuhiro's technique based on the express teaching found in Tokuhiro—namely, reduced power consumption and circuit area. Ex. 1006, 24:26–29 (“Accordingly, the delay times Dt1 and Dt2 from the input of the two signals to the output thereof ***can be efficiently set without increasing the power consumption and the area*** occupied by the apparatus.”) (emphasis added); see Ex. 1006, Figs. 16-17, 21:15-24:42. Based on these disclosures, such a person would have recognized that Tokuhiro's technique of using a common structure for implementing write and read delays would improve power consumption for

Osanai. That person would have also recognized that, by reducing the circuit area, it would have necessarily reduced costs by increasing manufacturing yield. By compensating for a delay in this manner, a POSITA would have recognized that the delay calculated using Tokuhiro's technique would be more energy-efficient than a conventional read/write leveling techniques that did not account for a write operation's delay. *See id.*, Figs. 16-17, 21:15-24:42. Based on these disclosures, a POSITA would have been motivated to use Tokuhiro's leveling technique in Osanai's data register control circuit 320.

139. Third, a POSITA would have been motivated to modify Osanai's data register control circuit 320 to incorporate Tokuhiro's teaching to improve signal fidelity, decrease timing skew among components, and/or lower the load perceived by the memory controller. Osanai and Tokuhiro recognize these are problems in the prior art. Ex. 1005, [0004]–[0005], [0075]–[0076], [0117]–[0119], [0176], [0194]; Ex. 1006, 1:63–2:28, 3:1–13. Based on these disclosures, a POSITA would have sought ways to mitigate these problems and Tokuhiro's technique would have provided a way to do so. Ex. 1006, 3:16–26, 19:8–13, 19:25–33. Accordingly, such a person would be motivated to modify Osanai's data register control circuit 320 to incorporate Tokuhiro's teaching.

140. For any of these reasons, a person of ordinary skill in the art would have been motivated to incorporate Tokuhiro's leveling technique in Osanai's data register control circuit 320. By doing so, the combination of Osanai and Tokuhiro render obvious "*delay[ing] a signal through the data path by an amount determined...in response to at least one of the module control signals.*" Accordingly, claim 1 is obvious over the combination of Osanai and Tokuhiro.

2. Claim 2

141. Claim 2 depends on claim 1 and further recites "*wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.*" As I

explained above, see §§ IX.A.1 and IX.B.1, claim 1 would be anticipated by Osanai alone or obvious in combination with Tokuhiro. The additional element recited in claim 4 would have likewise been obvious over Osanai and Tokuhiro.

142. Osanai's data register buffer 300 has logic that calculates the timing information used in both read and write operations. Ex. 1005, Fig. 2, [0096] ("Furthermore, the data register control circuit **320** includes a write leveling circuit **322** and a read leveling circuit **323**. The write leveling circuit **322** is a circuit for *performing a write leveling operation*, and the read leveling circuit **323** is a circuit for *performing a read leveling operation*.") (emphases added). As combined with Tokuhiro, a POSITA would have recognized that Osanai's data register buffer obtains timing information during a write memory operation prior to the read memory operation because Tokuhiro's technique uses the timing information from the writing operation to determine the delay amount for the read operation. Ex. 1006, 3:16–26, 16:1–28. Accordingly, the combination of Osanai and Tokuhiro render obvious "*a first memory operation and a second memory operation subsequent to the first memory operation*."

143. Osanai, as modified to use Tokuhiro's technique, also discloses "*wherein the command signals include a first set of command signals for the first*

memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals.” As I explained above, see § IX.A.1.c, Osanai discloses a command/address/control register buffer 400 that receives “*system command signals*” and outputs “*module command*” and “*control signals*.” Osanai also explains that these “*signals*” are different for each memory operations, such as a write operation (or “*first memory operation*”) and read operation (“*second memory operation*”). Ex. 1005, [0060] (states that “[a]n operation of the memory chip 200 is controlled based on the command signal”); see Ex. 1005, [0090], [0097], [0109]–[0110]. Based on these disclosures, a POSITA would have understood these disclosures to mean that read or write operations have different “*set of command signals*” that results in a different “*set of module control signals output by the module control device in response to the first set of command signals*.” Ex. 1005, Fig. 11, Fig. 12 [0129]–[0132], [0138]–[0140]. Such a person would thus have recognized that Osanai discloses that a write operation (the “*first memory operation*”) “*includes a first set of command*

signals” that is received by command/address/control register buffer 400 (“*module control device*”), which then outputs “*a first set of module control signals*” in response to those “*command signals.*” Likewise, such a person would have recognized that Osanai discloses that a read operation (the “*second memory operation*”) “*includes a second set of command signals*” that is received by command/address/control register buffer 400 (“*module control device*”), which then outputs “*a second set of module control signals*” to those “*command signals.*” Osanai, as modified to use Tokuhiro’s technique, therefore renders this limitation obvious.

144. Claim 2 also requires “*wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.*” A POSITA would have understood this limitation, stated otherwise, to require that data register buffer use the “*first set of module control signals*” for one memory operation to determine the delay and that delay would be applied to “*a signal associated with the second memory operation.*” See Ex. 1001, Claims 1 and 2. According to the prosecution history, see § VI.C above, this limitation most closely resembles the supposed novel feature that the examiner stated overcame the

prior art: having a buffer that “obtains timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information.” Ex. 1002, p. 206; Ex. 1008, Claim 1.

145. Osanai, as modified to incorporate Tokuhiro’s technique, discloses this limitation as well. As I explained above, *see* § IX.B.1.i , Tokuhiro’s delay technique obtains delay times for read and write operations using “*module control signals*” and that it calculates a first delay time from a write operation to use in its calculation of a second delay time used for a read operation. A POSITA would have understood that, by incorporating Tokuhiro’s technique into Osanai’s data register control circuit 320, the modified circuit would use “*module control signals*” to determine delay time for the write (or “*first*”) memory operation (“*wherein the at least one of the module control signals include at least one of the first set of module control signals*”). Such a person would have also recognized that this delay time for the writer operation would be used to determine the delay for the subsequent read (or “*second*”) operation, which is applied to “*a signal associated with the second memory operation.*”

146. For the above reasons, the combination of Osanai and Tokuhito render claim 2 obvious.

3. Claim 3

147. Claim 3 depends on claim 2 and recites “*wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.*” As I explained above, see §§ IX.A.1 and IX.B.1, claim 1 would be anticipated by Osanai alone or obvious in combination with Tokuhito. The additional element recited in claim 4 would have likewise been made obvious by Osanai and Tokuhito.

148. Osanai discloses a memory module with memory chips organized into multiple ranks. For example, Osanai discloses how the memory module organizes

four memory chips 200 into a single group (or set), with one memory chip from each set belonging to a rank. (*“the respective set of memory devices include one memory device from each of the plurality of ranks.”*). *Id.*, [0057]–[0058], [0111].

For example, Osanai explains that memory module 100 is a “4-Rank configuration.” Ex. 1005, [0057]. “The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner.” Ex. 1005, [0057]; *see id.* [0058]. Memory chips in different ranks “are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL.” Ex. 1005, [0111]. Using these signals, memory chips are chosen for read/write operations. *Id.*

149. A POSITA would have recognized that such operations include *“module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals.”* For example, and as explained in claim 2, a POSITA would have understood these disclosures to mean that read or write operations have a different *“set of command signals”* that result in different *“module command signals.”* Ex. 1005, Fig. 11, Fig. 12 [0129]–[0132], [0138]–

[0140]. Such a person would thus have recognized that Osanai discloses that a write operation (the “*first memory operation*”) “*includes a first set of command signals*” that is received by command/address/control register buffer 400 (“*module control device*”), which then outputs “*a first set of module command signals.*”

Likewise, such a person would have recognized that Osanai discloses that a read operation (the “*second memory operation*”) “*includes a second set of command signals*” that is received by command/address/control register buffer 400 (“*module control device*”), which then outputs “*a second set of module command signals.*”

150. Consequently, a POSITA would have also recognized that Osanai discloses “*wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.*” In read operations, for example, a POSITA would have understood that the second set of module command signals would include chip select (CS) or the clock enable (CKE) signals. Ex. 1005, [0057]–[0058], [0111]. A POSITA would have further understood that these signals select “*the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform*” the memory operation. See Ex. 1005, [0057]–[0058], [0111].

151. For these reasons, a POSITA would have understood that Osanai and Tokuhiro render claim 6 obvious.

4. Claim 4

152. Claim 4 depends on claim 1 and recites “*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.*” As I explained above, see §§ IX.A.1 and IX.B.1, claims 1 and 4 would be anticipated by Osanai alone or obvious in combination with Tokuhiro. To the extent one argues that the additional element recited in claim 4 is not anticipated by Osanai, it would have been obvious over Osanai and Tokuhiro.

153. Osanai’s data register buffer 300 has a data width of 1 byte (“*each of the plurality of buffer circuits has a data width of 1 byte*”). Ex. 1005, [0091] (“In the present embodiment, because ***a single data register buffer 300 inputs and outputs 1-byte data***, 8 sets of the FIFO circuits 301 and 302 are required.”) (emphasis added). Osanai explains, however, that the number of “memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number.” Ex. 1005, [0196]. A POSITA would have understood that the inventors of Osanai envisioned different data widths.

154. To the extent that one argues that Osanai does not disclose this limitation, modifying Osanai's memory module to include buffer circuits and memory devices to each have data widths of one byte would be obvious. A POSITA, however, would have been motivated to modify Osanai's memory devices to use eight bits for at least four reasons. First, such a person would have used eight bits to comply with the commercial standardization of the DDR3 standard, which specified four bits. Ex. 1013, p. 4 (showing x8 DRAM with four data lines). Alternatively, such a person would have been motivated to reduce packaging costs, thereby reducing cost savings on the module. Ex. 1013, p. 4. Third, having a data width of four bits would have been a common design tradeoff; for example, implementing a data width of eight bits would simplify routing, allow for increased memory density, and potentially improve speed by having fewer devices connected to each data line and reduce load on each line. Such a person would also realize the design tradeoff benefits of selecting a data width of four bits that is compliant with the JEDEC standard. Ex. 1013, p. 4. Finally, modifying Osanai's memory module to implement a data width of eight bits would simply arrange old elements with each performing the same function it had been known to

perform and yields no more than one would expect from such an arrangement, and would have been obvious.

155. For these reasons, a POSITA would have understood that Osanai and Tokuhiro render claim 4 obvious.

5. Claim 5

156. Claim 5 depends on claim 1 and recites “*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.*” As I explained above, see §§ IX.A.1 and IX.B.1, claim 1 would be anticipated by Osanai alone or obvious in combination with Tokuhiro. The additional element recited in claim 5 would have likewise been obvious over Osanai and Tokuhiro.

157. Osanai’s data register buffer 300 has a data width of 1 byte (“*each of the plurality of buffer circuits has a data width of 1 byte*”). Ex. 1005, [0091] (“In the present embodiment, because ***a single data register buffer 300 inputs and outputs 1-byte data***, 8 sets of the FIFO circuits 301 and 302 are required.”) (emphasis added). Osanai explains, however, that the number of “memory chips 200 allocated to a single data register buffer 300 is not limited to a particular

number.” Ex. 1005, [0196]. A POSITA would have understood that the inventors of Osanai envisioned different data widths.

158. Each of Osanai’s memory devices also have a data width of eight bits. Ex. 1005, [0059] (“An arrow of each of the data lines L1 and L2 shown in Fig. 1 indicates a line of 1 byte (8 bits)).”). A POSITA, however, would have been motivated to modify Osanai’s memory devices to use four bits instead of eight bits for at least four reasons. First, such a person would have used four bits to comply with the commercial standardization of DDR3 standard, which specified four bits. Ex. 1013, p. 3 (showing x4 DRAM with four data lines). Alternatively, such a person would have been motivated to reduce packaging costs thereby reduce cost savings on the module. Ex. 1013, p. 3. Third, having a data width of four bits would have been a common design tradeoff; for example, implementing a data width of four bits instead of eight bits would simplify routing, allow for increased memory density, and potentially improve speed by having fewer devices connected to each data line and reduce load on each line. Such a person would also realize the design tradeoff benefits of selecting a data width of four bits that is compliant with the JEDEC standard. Ex. 1013, p. 3. Finally, modifying Osanai’s memory module to implement a data width of four bits would simply arrange old elements

with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, and would therefore have been obvious.

159. For these reasons, a POSITA would have understood that Osanai and Tokuhito render claim 5 obvious.

C. Claims 1–5 are rendered obvious over Osanai (Ex. 1005) in view of Tokuhito (Ex. 1006), in further view of Takefman (Ex. 1007)

160. Claims 1–5 are obvious over Osanai (Ex. 1005) in view of Tokuhito (Ex. 1006), in further view of Takefman (Ex. 1007). For the reasons below, a POSITA considering the teachings of these references would have found the claimed subject matter obvious.

1. Claim 1: “*Tristate Buffer*”

161. In my opinion, claim 1 would also have been obvious over the combination of Osanai and Tokuhito, in further view of Takefman. To the extent that one argues that Osanai does not disclose a “tristate buffer,” such a feature would have been obvious because a POSITA would have been motivated to incorporate Takefman’s tristate buffer into Osanai’s “*data signal lines*.”

162. Takefman’s buffer circuits—called Bolt devices 303—include DDR-3 ports that “can be tri-stated” and can signal using “DDR-3 DQ/DQS signaling.”

Ex. 1007, 6:4–9. Takefman describes the tri-stated Bolt device 303 as follows:

Each of the Bolt devices include three DDR-3 ports
with... each port of the DDR-3 ports can be ***tri-stated***
and can signal using DDR-3 DQ/DQS signaling.

163. *Id.* (emphasis added). Based on these disclosures, a POSITA would have understood that Takefman discloses a “*tristate buffer[s]*.”

164. Such a person would have been motivated to include Takefman’s “*tristate buffers*” in the Osanai’s “*data signal lines*” for three reasons. First, such a person would have understood that modifying Osanai’s data signal lines to include tristate buffers would mitigate any interference caused by one buffer used in read operations during write operations. Second, a POSITA would have understood that tristate buffers allow the output to be sent at a specific time, which is especially important to leveling techniques. Finally, such a person would have recognized that such a modification would have been a simple substitution for Osanai’s buffers. *See* Ex. 1005, [0094]. A POSITA would have recognized that both Osanai’s buffers and Takefman’s DDR-3 ports operate similarly, both use DDR-3 DQ/DQS signaling for write/read operations. Ex. 1005, [0169], [0176];

Ex. 1007, 6:4–9. Such a modification would not be beyond the skill of an ordinary artisan and the modification would have produced no unexpected results.

2. Claim 4

165. Claim 4 depends on claim 1 and recites “*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.*” As I explained above, see §§ IX.A.1 and IX.B.1, claim 1 would be anticipated by Osanai alone or obvious in combination with Tokuhiro. The additional element recited in claim 4 would have likewise been obvious over Osanai and Tokuhiro, in further view of Takefman.

166. As I explained above, Osanai’s buffer circuits and memory devices also have a data width of eight bits, (Ex. 1005, [0059]). To the extent that one argues that Osanai’s memory devices do not have a data width of eight bits, such a data width would be obvious. Osanai explains that the number of “memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number”—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196].

167. Takefman discloses multiple memory devices, each having “*a data width of 1 byte.*” Ex. 1007, 7:30–40 (“DIMM configuration data including the

number of ranks of DRAM present and the organization of the DRAM (x4/x8).”). Specifically, Takefman discloses that each DIMM can use DRAMs with “x8” width, which means the DRAM has “*data width of the 1 byte*” or 8 bits. Ex. 1007, 7:30–40 (“DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8).”). A POSITA would have been motivated to modify the data width of Osanai’s memory chips 200 to be four bits for the same reasons that I explained for Ground 2 above. See § IX.B.4.

3. Claim 5

168. Claim 5 depends on claim 1 and recites “*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.*” As I explained above, see §§ IX.A.1 and IX.B.1, claim 1 would be anticipated by Osanai alone or obvious in combination with Tokuhiro. The additional element recited in claim 5 would have likewise been obvious over Osanai and Tokuhiro, in further view of Takefman.

169. As I explained above, Osanai’s buffer circuits and memory devices also have a data width of eight bits (Ex. 1005, [0059]), but Osanai’s memory devices also have a data width of eight bits (Ex. 1005, [0059]). Osanai explains, however, that the number of “memory chips 200 allocated to a single data register

buffer 300 is not limited to a particular number”—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196].

170. One such data width—four bits—is disclosed by Takefman. Takefman discloses multiple memory devices, each having “*a data width of 1 byte.*” Ex. 1007, 7:30–40 (“DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8).”). Specifically, Takefman discloses that each DIMM can use DRAMs with “x4” width, which means the DRAM has “*data width of the 4 bits.*” Ex. 1007, 7:30–40 (“DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8).”). A POSITA would have been motivated to modify the data width of Osanai’s memory chips 200 to be eight bits for the same reasons discussed in Ground 2 above. See § IX.B.5.

X. RESERVATION OF RIGHTS

171. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the ’608 patent that would render any of the asserted claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any

arguments raised by the owner of the '608 patent and to consider new information that becomes available to me.

XI. CONCLUSION

172. For the reasons discussed above, it is my opinion that claims 1 and 4 of the '608 patent would have been anticipated to a POSITA by Osanai.

Alternatively, claims 1-5 would have been obvious to a POSITA over Osanai in view of Tokuhiko. Finally, the claims 1-5 would also have been obvious to a POSITA over Osanai in view of Tokuhiko, and in further view of Takefman.

173. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: December 22, 2021

A handwritten signature in black ink, reading "Donald Alpert", written over a horizontal line.

Donald Alpert, Ph.D.