

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Case IPR2023-00847

Patent 10,268,608

**PETITIONER'S AUTHORIZED
REPLY TO PATENT OWNER'S PRELIMINARY RESPONSE**

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 10,268,608
1002	File History of U.S. Patent No. 10,268,608
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. US2010/0312956 to Hiraishi
1006	U.S. Patent No. 8,020,022 to Tokuhiro
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry
1008	U.S. Patent No. 6,184,701 to Kim
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	U.S. Patent Pub. No. 2011/0062999 to Nimaiyar
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

Exhibit #	Description
1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts)
1022	Harold S. Stone, Microcomputer Interfacing (1982)
1023	Microsoft Computer Dictionary (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to '632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 7,808,849 to Swain
1028	U.S. Patent No. 6,906,555 to Ma
1029	U.S. Patent Pub. No. 2007/0008791 to Butt
1030	U.S. Patent No. 7,036,053 to Zumkehr
1031	U.S. Patent No. 9,824,035
1032	File History of U.S. Patent No. 9,824,035
1033	U.S. Patent No. 5,036,221 to Brucculeri
1034	U.S. Patent No. 9,536,579 to Iijima
1035	<i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021)

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1036	Order Transferring Cases to the Austin Division, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 1:22-cv-00136 (W.D. Tex. Feb. 14, 2022)
1037	Joint Claim Construction Statement, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 1:22-cv-00136 (W.D. Tex. Apr. 14, 2022)
1038	Order on Motion to Stay, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 1:22-cv-00136 (W.D. Tex. May 11, 2022)
1039	[intentionally omitted]
1040	Decision Granting Institution of <i>Inter Partes</i> Review, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00236, Paper 16 (PTAB July 19, 2022) (U.S. Patent No. 9,824,035)
1041	Decision Denying Institution of <i>Inter Partes</i> Review, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00237, Paper 15 (PTAB July 19, 2022) (U.S. Patent No. 10,268,608)
1042	[intentionally omitted]
1043	[intentionally omitted]
1044	Complaint, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021) (asserting U.S. Patent No. 10,860,506)
1045	First Amended Complaint, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. May 3, 2022)
1046	U.S. Patent No. 10,860,506
1047	Decision Granting Institution of <i>Inter Partes</i> Review, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00711, Paper 14 (PTAB Oct. 21, 2022) (U.S. Patent No. 10,860,506)

Exhibit #	Description
1048	Joint 4-3 Claim Construction and Prehearing Statement, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Aug. 19, 2022 and Aug. 23, 2022)
1049	Joint Claim Construction Chart Pursuant to P.R. 4-5(d), <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Sept. 30, 2022)
1050	Claim Construction Order, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Dec. 14, 2022)
1051	Defendants' Objections to Claim Construction Memorandum Order, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Dec. 29, 2022)
1052	File History of U.S. Patent No. 10,860,506
1053	Complaint, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (asserting U.S. Patent No. 10,860,506)
1054	Complaint, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. filed Aug. 1, 2022)
1055	First Amended Complaint, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. Aug. 15, 2022)
1056	Netlist's motion to amend its complaint to assert U.S. Patent No. 10,268,608, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1057	Netlist's proposed Second Amended Complaint asserting U.S. Patent No. 10,268,608 in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1058	JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019)
1059	[intentionally omitted]

Exhibit #	Description
1060	[intentionally omitted]
1061	[intentionally omitted]
1062	[intentionally omitted]
1063	<i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (June 21, 2022)
1064	Federal Court Management Statistics (June 30, 2022), available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2
1065 [NEW]	Email from counsel for Samsung to counsel for Patent Owner re: stipulation not to pursue certain invalidity defenses if an IPR proceeding is instituted
1066 [NEW]	Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00236, Paper 34 (PTAB June 20, 2023) (U.S. Patent No. 9,824,035)
1067 [NEW]	Decision Granting Petitioner’s Request on Rehearing of Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00236, Paper 36 (PTAB August 16, 2023) (U.S. Patent No. 9,824,035)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1[pre]	1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
1[a]	a module board having edge connections for coupling to respective signal lines in the memory bus;
1[b]	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
1[c]	memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
1[d]	a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,
1[e]	wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,
1[f]	wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ref. #	Listing of Challenged Claims
2[a]	2. The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,
2[b]	wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,
2[c]	wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,
2[d]	wherein the at least one of the module control signals include at least one of the first set of module control signals, and
2[e]	wherein the signal through the data path is a signal associated with the second memory operation.
3[a]	3. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks,
3[b]	wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and
3[c]	wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.
4	4. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
5	5. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

Ref. #	Listing of Challenged Claims
~~6~~ [†]	6. The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.
~~7~~	7. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
~~8~~	8. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.
~~9~~ ^a	9. The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,
~~9~~ ^b	wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.
~~10~~ ^a	10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation,
~~10~~ ^b	the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.
~~11~~	11. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
~~12~~	12. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

[†] Claims 6–12 were disclaimed on September 13, 2023. *See* EX2001.

REPLY TO PATENT OWNER’S PRELIMINARY RESPONSE

Netlist concedes that “Osanai [used by Micron] . . . is the same as Hiraishi [used by Samsung] in all material respects.” POPR 5. Netlist’s § 325(d) arguments focus on IPR2022-00237, *see* POPR 1, 3–25, where Institution was denied based on *anticipation* by Osanai, *see* EX1041/EX2006 at 17–20; EX2010 at 4–6, but Netlist ignores IPR2022-00236 and -00711, where Institution was granted for similar claims based on *obviousness* grounds similar to those here (i.e., Hiraishi/Osanai in view of Butt and/or Tokuhiro), *see* Pet. 113–14; EX1040 at 6–7, 22–26; EX2007 at 1–2, 35–48, 93–122; EX1047 at 18–26, 31–32. And the Board just issued a Final Written Decision in IPR2022-00236 finding similar claims obvious based on Osanai in view of Tokuhiro — like Ground 2 here:

IPR2022-00236 (’035 Patent) EX1066 at 5–7, 22–43, 46–52; EX1067	’608 Patent Pet. 39–53, 98–101
[1.j] wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation to <i>control timing of the respective data and strobe signals on the data paths</i> in accordance with the timing information	[1.f] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a <i>delay circuit configured to delay a signal through the data path</i> by an amount determined by the command processing circuit in response to at least one of the module control signals.

With respect to Ground 2 here, Netlist incorrectly states that “Tokuhiro [was] already considered by the Board in Micron -0237.” POPR 12. To the contrary, in IPR2022-00237 the Board never considered Tokuhiro because

“[Micron] does not rely on Tokuhiro . . . as disclosing that the delay circuit is included in the recited data path, as required by claim 1 [above right].”

EX1041/EX2006 at 20. Thus, the Board only considered **anticipation** by Osanai in IPR2022-00237. *See id.* at 17–20; EX2010 at 4–6. But in IPR2022-00236, the Board considered **obviousness** based on Osanai and Tokuhiro, and invalidated a claim very similar to claim 1 of the ’608 Patent, as shown above.

Thus, § 325(d) and Part 1 of *Advanced Bionics* favor Petitioner, because Petitioner does not present the same **anticipation** argument rejected in IPR2022-00237, *see Oticon Medical AB v. Cochlear Ltd.*, IPR2019-00975, Paper 15, at 9–19 (PTAB Oct. 16, 2019) (precedential), but instead presents “the same or substantially the same prior art or arguments” that were **accepted** by the Board in IPR2022-00236 and -00711, as explained above. *See* Pet. 113–14.

Netlist’s arguments to the contrary are without merit. First, Netlist asserts “[t]he inclusion of Butt in Ground 1 is window dressing,” POPR 1, and “the Petition here relies on only Hiraishi substantively for all claim limitations under Ground 1,” POPR 6; *see also id.* at 5–12 (similar). To the contrary, Butt (which was not considered in IPR2022-00237) is an integral part of Ground 1: “a POSITA would have understood from the disclosure of Butt that Hiraishi’s data register buffer includes data paths and would have been motivated to implement Butt’s data path controlling technique in Hiraishi’s data register buffer.” Pet. 33–41.

Netlist is thus incorrect that “Butt’s sampling optimization process is not relied on to satisfy any claim limitation.” POPR 8. Netlist is also incorrect that “[t]he claims do not recite a sampling operation at all.” *Id.* Claim 10, which depends from claim 1, requires sampling, *see* Pet. 67–71, confirming that “Butt’s sampling optimization process” is also relevant to claim 1.

Second, Netlist is incorrect that “Hiraishi/Osanai . . . fail[s] to establish a delay circuit in the recited data path.” POPR 11. The Board found precisely the opposite in IPR2022-00236: “We determine that these disclosures of Osanai are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.” EX1066 at 35–36. The reason the Board denied Institution in IPR2022-00237 (while granting Institution the same day in IPR2022-00236, which also involved Osanai, *see* EX1040 at 6–7, 22–26) is because the anticipation argument in IPR2022-00237 made “no mention” of delaying signals (e.g., with “FIFO circuits”), *see* EX2010 at 4, and did not “even assert that the data path includes the delay circuitry,” *id.* at 5–6. Here, the Petition shows how those limitations are obvious, *see, e.g.*, Pet. 39–53, 98–101, similar to the showings that were accepted by the Board in Micron’s IPR2022-00236 and Samsung’s IPR2022-00711 as discussed above.

Third, Netlist is incorrect that “the Petition here presents substantially the same arguments as what the Board considered in Micron -0237,” POPR 15, and

“all Samsung has done is to identify [in orange below, *see* POPR 18–19; Pet. 39–40; EX2007 at 35–40] a subset of

the components that Micron previously identified as allegedly comprising the ‘data path,’” POPR 20. To the contrary, the Board specifically found that Micron made “no mention” of the

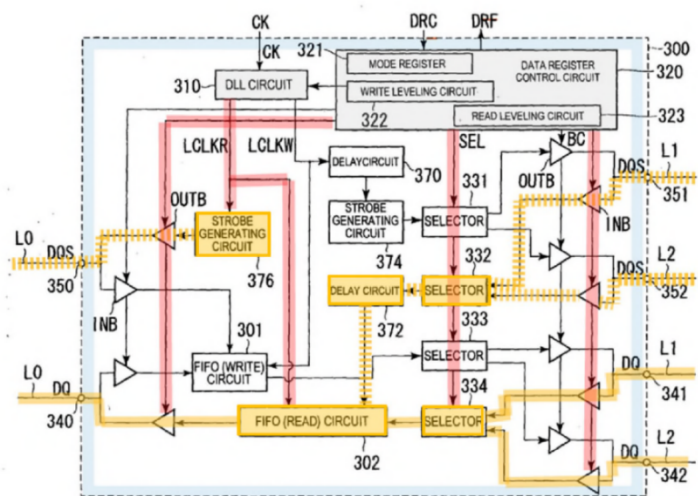


FIG. 5

components identified by Samsung in orange above, *see* EX2010 at 4, and Micron did not “even assert that the data path includes the delay circuitry,” *id.* at 5–6.

Finally, under Part 2 of *Advanced Bionics*, the Examiner clearly erred by allowing the claims (without any substantive rejection, just a double-patenting rejection). *See* Pet. 113. “[I]f the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics*, IPR2019-01469, Paper 6, at 10; *Yita LLC v. MacNeil IP LLC*, IPR2023-00172, Paper 12, at 45–46 (PTAB June 13, 2023). That is the case here. The remaining claims of the ’608 Patent are clearly obvious in light of Grounds 1–3, as confirmed by the Final Written Decision against the ’035 Patent in IPR2022-00236 discussed above.

Dated: September 26, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Authorized Reply to Patent Owner's Preliminary Response**, excluding the parts of the brief exempted by 37 C.F.R. § 42.24, complies with the page limits provided by the Board in Exhibit 3001 (Sept. 25, 2023), which stated: "The reply shall not exceed 4 pages and is limited to addressing Patent Owner's arguments in the Preliminary Response concerning discretionary denial under § 325(d). The sur-reply shall not exceed 4 pages and is limited to responding to Petitioner's arguments in the reply. The reply is due 7 business days from the date of this grant, with the sur-reply due 7 business days after the filing of the reply."

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 26th day of September, 2023, **Petitioner's Authorized Reply to Patent Owner's Preliminary Response** was served by email on the following counsel for Patent Owner:

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