

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00847
Patent No. 10,268,608

DECLARATION OF DR. WILLIAM HENRY MANGIONE-SMITH

I declare that all statements made here on my own knowledge are true and that all statements made contain information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Date: 3/29/24


Dr. William Henry Mangione-Smith

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DECLARATION OF WILLIAM HENRY MANGIONE-SMITH, PH. D

I, William Henry Mangione-Smith, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained on behalf of Netlist, Inc. (“Patent Owner”) as an expert to evaluate certain technical aspects of U.S. Patent No. 10,268,608 (“the ’608 patent”), and to provide certain related opinions. I am personally knowledgeable about the matters stated here and am competent to make this declaration.

2. I understand that Patent Owner will submit this declaration (“Declaration”) in connection with IPR2023-00847 (“Proceeding”), which I have been informed is an *inter partes* review (IPR) proceeding before the Patent Trial and Appeal Board in which claims 1-5 of the ’608 patent are being challenged by Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”).

3. I receive compensation at my normal consulting rate for my time working on this matter, plus expenses. I have no financial interest in Patent Owner or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The opinions I present are due to my own judgment.

4. All “EX10XX” cites here are to exhibits I understand were submitted by the Petitioner in this Proceeding. All “EX20XX” cites here are to exhibits I understand were or will be submitted by the Patent Owner in this Proceeding. All “Appendix _” cites followed by a letter are to appendices to this Declaration. All

citations to “Section XX” are internal citations to the sections of this Declaration. All citations to “Paragraph XX” are internal citations to the paragraphs of this Declaration.

II. BACKGROUND AND QUALIFICATIONS

5. I received my Bachelor of Science in Engineering in 1987 and my Master of Science in Engineering in 1992, both from the University of Michigan. I also received my Doctorate in Engineering from the University of Michigan.

6. I am a Member of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE). I've served as the Program Chair and the General Chair for the 26th and 36th International Symposiums on Microarchitecture, respectively. I have served as the Associate Editor of IEEE Transactions on Computers, the Associate Editor of ACM Transactions on Embedded Computing Systems, and the Associate Editor of IEEE Computer. I have served on various Program Committees, including ISCA, Network Processors Workshop, Complexity-Effective Design, and Workshop on Mediaprocessors and DSP. I have published numerous journal articles on computing, given 49 conference presentations, and authored several book chapters and magazine articles on such issues. I am listed as an inventor on 121 patents nearly all of which are related to microprocessor and memory technology and am listed on more than 200 pending patent applications.

7. I have an extensive background working with electronics and computer patents. I currently work as a consultant on intellectual property matters, including reviewing and valuing patents and patent portfolios for Phase Two LLC, and I have held this position since 2009. Prior to that, from 2005-2008, I was employed at Intellectual Ventures, working on patent valuation, with a focus on computer patents, and outbound licensing in consumer electronics, among other focuses. During my time at Intellectual Ventures the company developed intellectual property that resulted in several successful startups. I was not involved in any of the litigation while I was at Intellectual Ventures, focusing instead on developing new ideas. From 1995-2005, I worked as an Assistant and an Associate Professor in electrical engineering at the University of California, Los Angeles. From 1993-1995, I worked as a Systems Architect for the Motorola Wireless Data Group, where I worked on designing and developing the microprocessor for an early smartphone. From 1991-1992, I worked with Motorola Corporate research, focusing on parallel computer performance monitoring and low-power processor architecture. Finally, from 1986-1987, I worked as a Software Architect at Chrysler Corporation, where I operated supercomputers related to designing, testing, and simulating car designs. I have been accepted by various courts as an expert in the fields of computer engineering, including computer architecture and microarchitecture.

8. A current curriculum vitae is attached as Appendix A and includes the above listed credentials, additional background and information, and my experience as an expert witness from the previous four years.

III. MATERIALS CONSIDERED

9. I have considered information from various sources in forming my opinions. Besides drawing from my decades of experience in the computer industry, I have reviewed the Petition and supporting declaration from Dr. Wedig (EX1003), the '608 patent and its file history, the prior art discussed below, Dr. Wedig's deposition transcript, and the other documents and references cited here.

IV. LEGAL STANDARDS

10. I have relied on instructions from counsel as to the applicable legal standards to use in arriving at my opinions in this Declaration.

11. I understand that a patent claim is unpatentable and invalid if the subject matter of the claim as a whole would have been obvious to a person of ordinary skill in the art of the claimed subject matter, as of the time of the invention at issue.

12. I have been informed and understand that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time of the alleged invention. Even if all the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject

matter in the prior art and the subject matter in the claim, would have been obvious to a person of ordinary skill in the art at the time of the alleged invention.

13. I understand that the following factors must be evaluated to determine whether the claimed subject matter is obvious: (1) the scope and content of the prior art; (2) the difference or differences, if any, between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

14. I have been informed and understand that the teachings of two or more references may be combined if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on multiple references would have been obvious, it is appropriate to consider, among other factors: (1) whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results; (2) whether a person of ordinary skill in the art could implement such a combination, and would see the benefit of doing so; (3) whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art; (4) whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim; (5) whether there is some teaching or suggestion in the prior art to make the modification or combination of elements

claimed in the patent; and (6) whether the claimed invention applies a known technique that had been used to improve a similar device or method in a similar way.

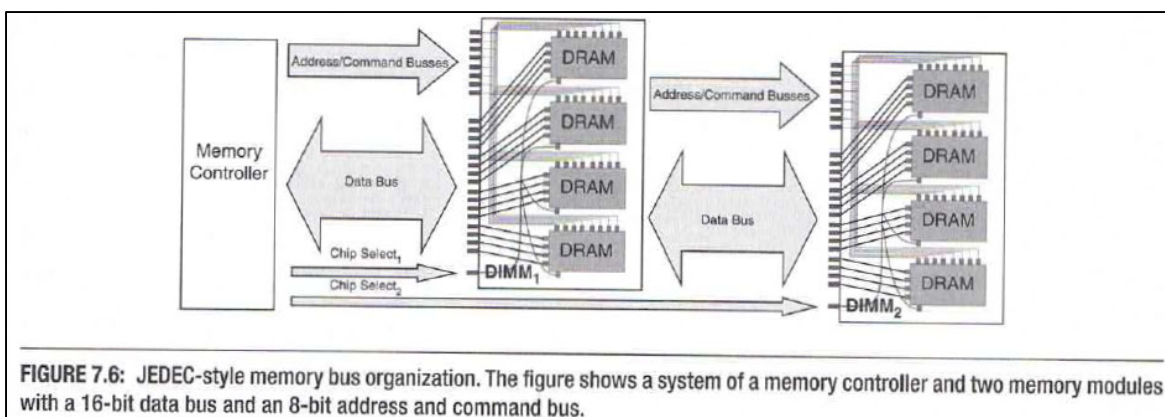
15. I have been informed and understand that one of ordinary skill in the art has ordinary creativity and is not an automaton.

16. I have been informed and understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

V. TECHNICAL BACKGROUND

17. A dynamic random-access memory (DRAM) system is a type of computer memory that allows a computer processor to access a random part of the memory directly rather than having to access a larger portion of the memory which includes the desired memory, by proceeding sequentially from a starting point. DRAM memory system is comprised of a memory controller and a number of DRAM chips organized into DIMMs (dual in-line memory modules, which are printed circuit boards containing a number of DRAMs). EX1021 (Jacob), 11.

18. Memory buses are classified by their function—i.e., data buses, address/command buses, and control buses, as shown in Figure 7.6 below.



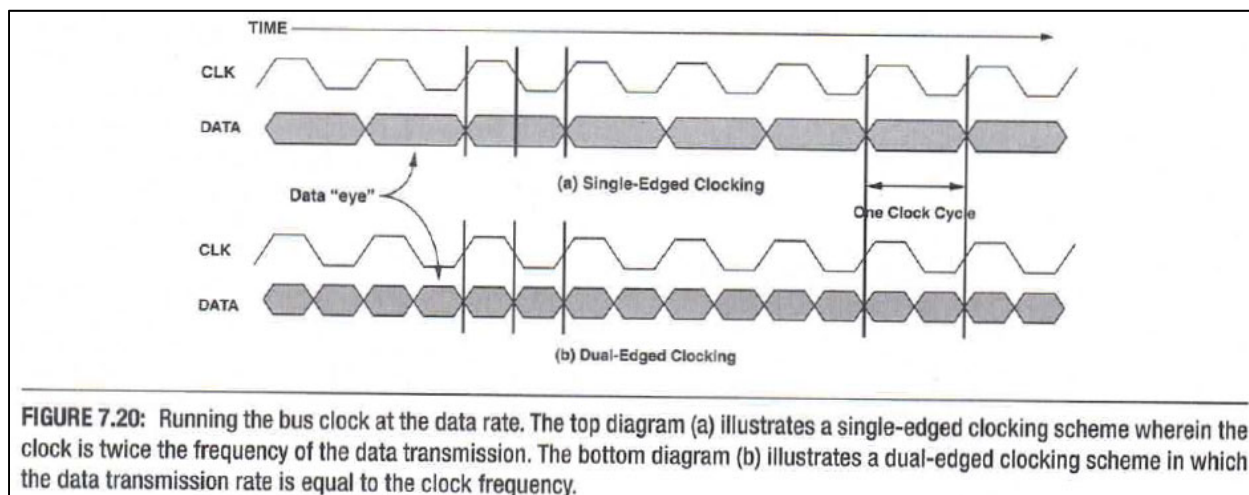
Id.

19. This arrangement is referred to as a JEDEC-style memory organization, where JEDEC is a standard-setting body that covers standardization of discrete semiconductor devices and integrated circuits, including DRAM chips. *See id.*, 332. The data bus, unlike the address bus, is bi-directional, shuttling signals back and forth between the DRAM chips and the controller. When data needs to be written to the DRAM, the controller drives the data bus. Similarly, when data needs to be read from the DRAM, the DRAM drives the data bus to send out the stored data.

20. A common type of DRAM is synchronous DRAM, or SDRAM, which uses a system-level clock to time all actions, i.e., command and data transmissions. *See id.*, 332. Most modern SDRAM is “Double Data Rate” (DDR) memory. JEDEC creates standards for DDR memory, and has done so for each successive version, e.g., DDR, DDR2, DDR3. *See id.*, 333. Unlike single data rate SDRAM which transmits data (i.e., a data period) once per clock cycle, DDR SDRAM uses both the rising edge and the falling edge of the clock cycle to transmit data, effectively

doubling the amount of data transmitted in each clock cycle. EX1021 (Jacob), 333.

The difference between single rate and DDR is shown in Figure 7.20 below.

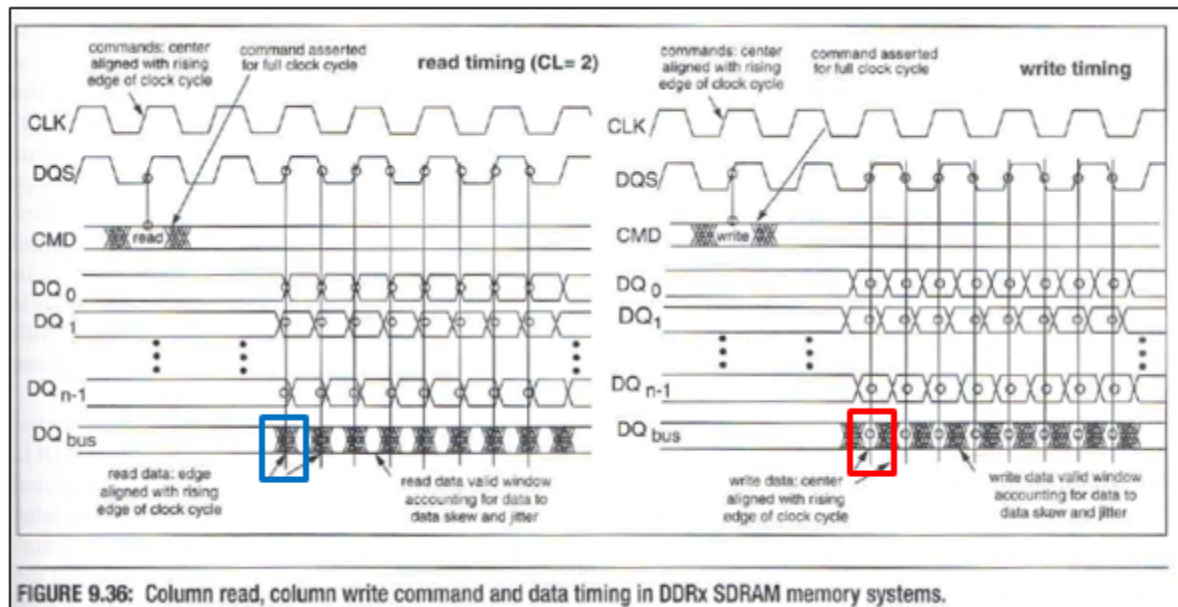


Id., 334.

21. In a system that uses a single-edged clock (single data rate), there are two clock edges for every data “eye,” which is the approximate midpoint of the duration in which a read or write data signal is present. As shown in the bottom diagram above, in DDR, there is only one clock edge for every data eye, and the clock edges are either edge-aligned or center-aligned with the data. *See id.*, 333-334. In other words, data is transmitted twice per clock cycle. DDR SDRAM typically uses a data strobe signal to ensure accurate timing for sampling/capturing data. *See id.* The data strobe signal, or “DQS” signal, is specified by the DDR standard. Generally, a strobe signal indicates that another signal, e.g., data or command, is present and valid. *See id.*, 318, fn 1. This technique allows the system to distinguish each data transmission cycle accurately in a clock cycle, to facilitate the receiver to

receive data accurately. I note that the timing of strobe signals does not affect timing of the data signal themselves, just the accuracy in capturing the data itself.

22. In the context of the DQS signal, the DDR standard requires a center-aligned data strobe signal be provided by the memory controller for all DRAM writes, which the DRAM uses directly to sample the incoming data. *See id.*, 334-335. For DRAM reads, on the other hand, the data strobe is edge-aligned with the data and system clock, therefore requiring memory controller to provide its own mechanism for generating a center-aligned DQS signal for read operations. *See id.*; *see also* EX2014 (JESD79-2F), 13 (stating that the strobe signal is “[e]dge-aligned with read data, centered in write data.”); EX1019 (JESD79-3C), 34; EX2015 (JESD79-3F-2), 13. DRAM can use the strobe signal directly to sample the incoming write data. EX1021, 334. In contrast, because the DQS is edge-aligned with the read data, the memory controller delays the read strobe by a fixed amount to capture the data in the valid window. *Id.*; *see also* Butt, [0021]. The differences between read and write timing are illustrated below in Figure 9.36.



EX1021 (Jacob), 405.

23. This is also reflected directly in the DDR2 standard.

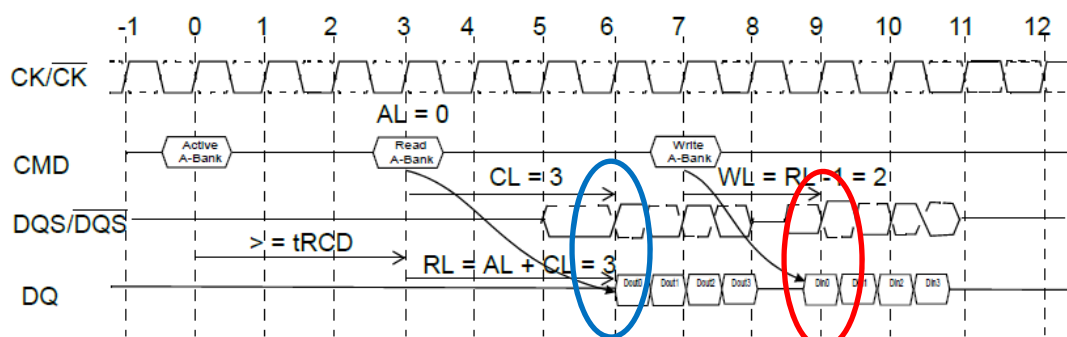


Figure 31 — Example 2: Read followed by a write to the same bank, where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

EX2014 (JEDEC Standard No. 79-2F), 13 (strobe signal is “[e]dge-aligned with read data, centered in write data”); Figure 31, page 33 (showing edge-aligned DQ and DQS for read command and 1/4 clock cycle offset (center-aligned) DQ and DQS for write comment).

24. As shown above, per the JEDEC standard, read and write data is sent and received on different phase offsets the DQS signal in DDR memory systems. DRAM devices place data on the bus for read commands at the edge of the DQS signal (highlighted in blue above). The DRAM memory controller then must determine the center of the valid data windows and latch the data at the appropriate time. This latching is done by having the memory controller delay the DQS signal by 90 degrees (1/4 clock cycle) relative to the DQS. EX2012 (Jacob) at 405. In contrast, the memory controller provides write data center-aligned with the edge of the DQS signal (highlighted in red above) so that the DRAM devices can latch in the data relative to each edge of the DQS signal without having to shift or delay the data. *See id.*

25. The difference in phase relationships between DQS signals for read operations and for write operations provided for under the DDR standard was intentional, and part of the JEDEC specification. DRAMs are intended to be inexpensive, commodity devices. To facilitate that goal, the JEDEC standard effectively shifts some of the burden of timing synchronization from the DRAMs to the memory controller by first forcing the memory controller to provide a correctly centered DQS signal for write operations, and then to further correct the phase of the DQS for read operations so that the data can be latched in the center of the valid data

window (the eye) despite the fact that the DRAM devices are placing read data on the data bus with the same phase as the DQS signal. *See id.*, 406.

VI. THE '608 PATENT

26. With reference to FIG. 1 reproduced below, the '608 patent generally relates to memory systems 100 which comprise a memory controller (MCH) 101 and memory modules 110 coupled to the MCH 101 by a memory bus 105. EX1001, 4:20-22. The disclosed system 100 which comprises a memory controller (MCH) 101 and memory modules 110 coupled to the MCH 101 by a memory bus 105.

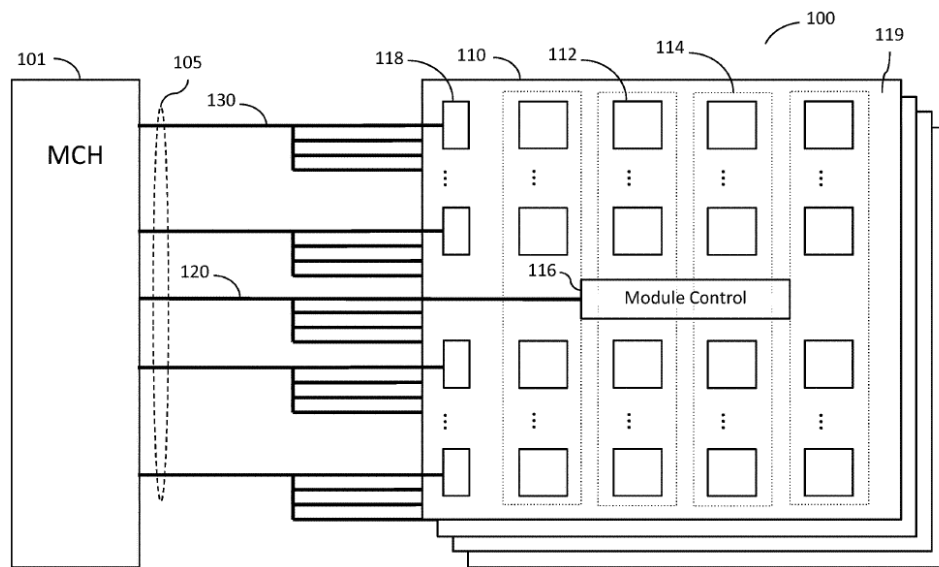


FIG. 1

27. The memory bus 105 includes control/address (C/A) signal lines 120 and data/strobe signal lines 130. *See id.*, 4:23-25. As shown with reference to FIG. 2A below, each memory module 110 includes a plurality of memory devices 112

(highlighted in orange) organized in a plurality of ranks 114 (highlighted in dashed purple line). *See id.*, 4:25-27.

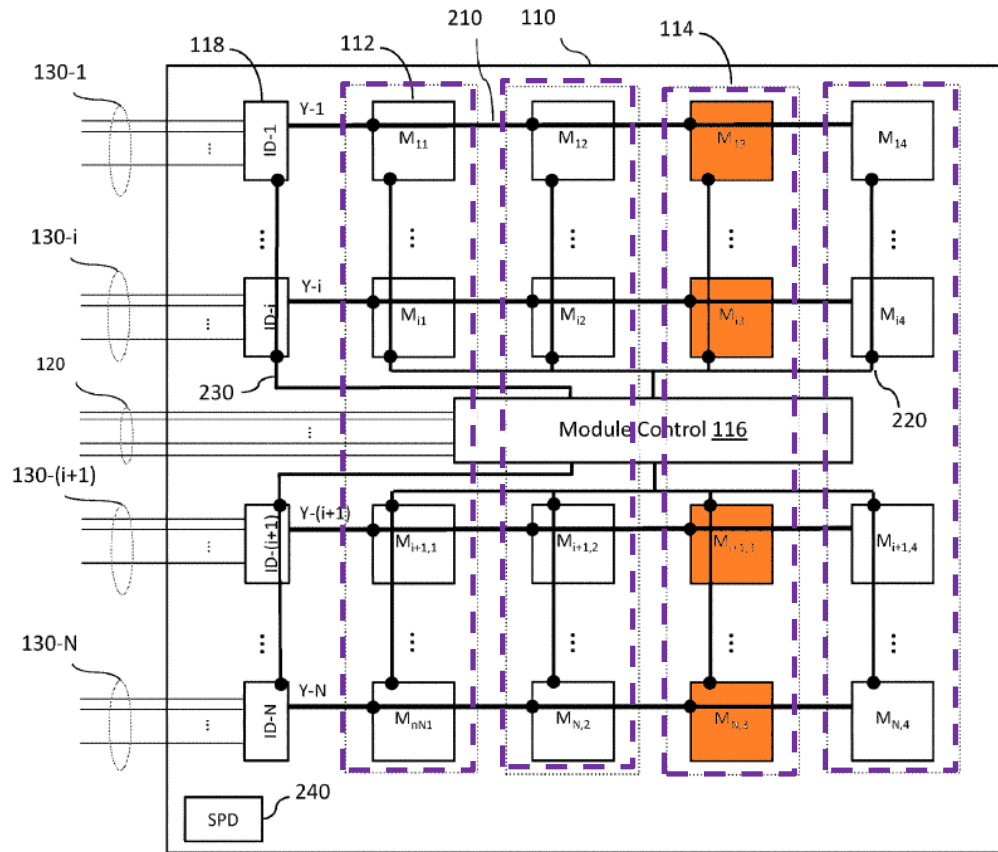


FIG. 2A

28. Each memory module 110 includes a module control device 116 (highlighted in blue below) and a plurality of buffers 118 (also referred to as “isolation devices”) (highlighted in green below). *See id.*, 4:27-32.

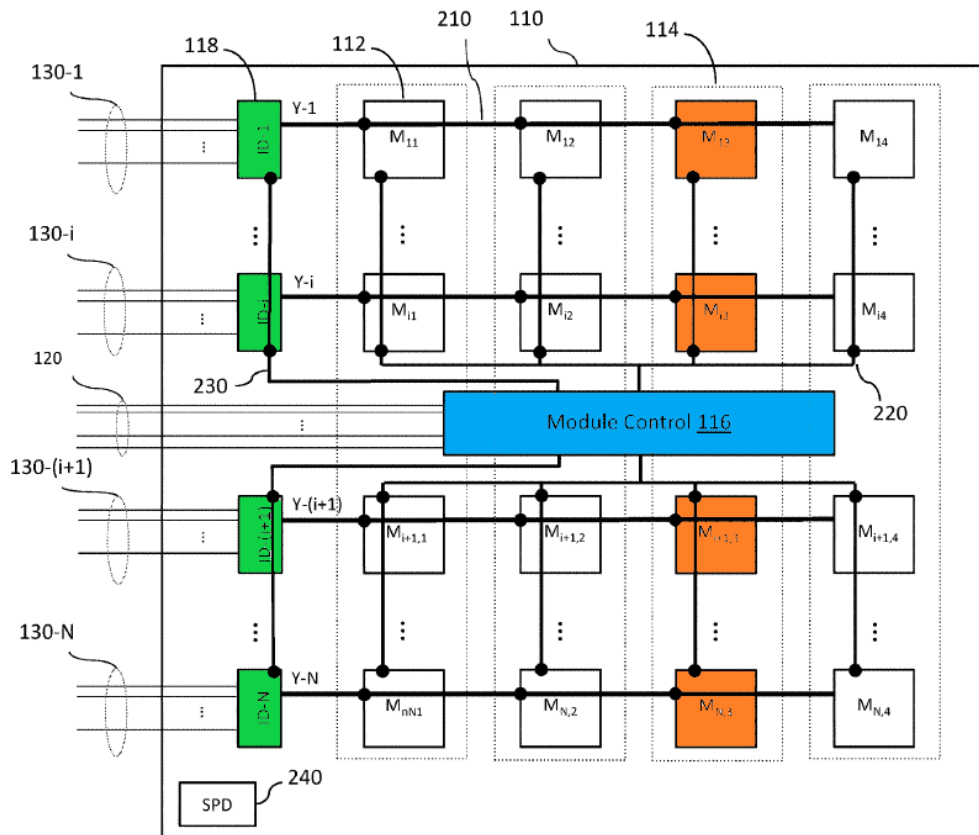


FIG. 2A

29. The module control device 116 receives system command signals corresponding to a memory operation via a set of C/A signal lines and outputs module command signals and module control signals to the memory devices 112 and the buffers 118, respectively. See id., cl. 1 (19:21-26), 4:65-5:4, 5:58-66. The module control device 116 further receives a system clock signal and outputs a module clock signal. See id., cl. 1 (19:26-28). The memory devices 112 perform memory operations, such as read or write operations, in response to receiving the module command signals and the module clock signal from the module control device 116. See id., cl. 1 (19:28-33), 5:11-26.

30. In operation, the module control device 116 receives input C/A signals corresponding to a memory operation via the C/A signal lines. Module control device 116 transmits registered C/A signals and module control signals to the memory devices 112 and the buffers 118, respectively. *See id.*, cl. 1 (19:23-27), 4:65-5:4, 5:58-66. Each buffer (isolation devices 118) includes a command processing circuit that decodes the received module control signals and the module clock signal and controls a data path in the buffer in accordance with the module control signals and the module clock signal. *See id.*, cl. 1 (19:45-49); 12:3-19. The data path for each data signal line includes a tristate buffer controlled by the command processing circuit. *See id.*, cl. 1 (19:49-51); 12:19-26.

31. The memory devices 112, which are arranged in multiple ranks 114, cause a selected rank of the multiple ranks to perform a memory operation, such as a memory read operation, in response to receiving the registered C/A signals from the module control device 116. *See id.*, cl. 1 (19:28-33), 5:11-26. In the case of a memory read operation, the memory devices 112 output read data and read strobes associated with the memory read operation. *See id.*, cl. 1 (19:33-37), 5:60-62, 7:66-8:3.

32. The buffer circuits (isolation devices 118) include a delay control circuit 650 that determines an amount of delay for a signal through the data path in

response to at least one of the module control signals. *See id.*, cl. 1 (19:52-55), 10:11-21, 11:8-13, 12:14-37, 15:23-26, 16:10-12.

33. The '608 patent describes the need to overcome limitations of prior art memory modules and the complications posed by increasing the memory speed and the number of memory devices, and thus the memory density, on the memory module. For example, the specification describes the limitations of conventional read and write leveling mechanisms that were known in the prior art and used to compensate for unbalanced wire lengths and loading:

In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Id., 2:28-35; *see also id.*, 15:21-22 (“[C]onventional read/write leveling techniques are not sufficient for managing read/write data timing.”).

34. Thus, the embodiments of the '608 patent present mechanisms for buffering command, address, and data via a module control device, a plurality of buffer circuits, and memory devices located on the memory module, collectively resulting in modules with higher capacity and higher performance. Specifically, the '608 patent discloses that the buffer circuits 118 include a data path that includes a

delay circuit that is configured to delay a signal through the data path by an amount determined by the command processing circuit in response to module control signals. *See id.*, cl. 1; *see also id.*, 15:23-26 (“[T]he isolation devices 118 include[] signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation”).

VII. SKILL LEVEL OF A POSA

35. The Petition states that a person of ordinary skill in the art (POSA) in the field of the '608 patent in July 2012 would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field. *See* Petition, 2.

36. For purposes of the opinions I set forth here, and to simplify the issues, I have adopted that understanding as to the level of skill in the relevant field at the time of the invention, noting that none of the opinions I express here would change if a somewhat higher or somewhat lower level of skill were adopted. However, I reserve the right to separately analyze the appropriate level of skill at the time of the invention, and to propose a different ordinary level of skill in the art based on that analysis.

VIII. THE PRIOR ART

37. Under the first ground, the Petition challenges claims 1-5 of the '608 patent based on U.S. Publication No. 2010/0312956 ("Hiraishi") (EX1005), and U.S. Publication No. 2007/0008791 ("Butt") (EX1029) only to allegedly provide additional explanation as to how a POSA would understand Hiraishi. I understand the Board agreed that "Hiraishi is the main reference relied upon for the teachings of the claim limitations, and Butt is used to provide further explanations or interpretations of the teachings of Hiraishi and/or to explain the knowledge of one of ordinary skill in the art." Institution Decision at 11-12. The second ground identified in the Petition challenges claims 1-5 of the '608 patent based on Hiraishi in combination with U.S. Patent No. 8,020,022 ("Tokuhiko") (EX1006). Below I provide a brief overview of those references.

A. Hiraishi (EX1005)

38. Hiraishi is directed to a memory module including a plurality of data register buffers, data connectors, and memory chips in a line along a memory module substrate. EX1005 (Hiraishi), [0009]-[0011].

39. As illustrated by Hiraishi's Fig. 3, which is reproduced and annotated below, memory system 20 includes a memory controller 12 and a memory module 100 inserted into memory slot 22. The memory controller 12 and memory module 100 communicate via data and command/address/control lines provided via a signal

path (Line 23) between the memory controller 12 and memory module 100. *See id.*, [0068]-[0069].

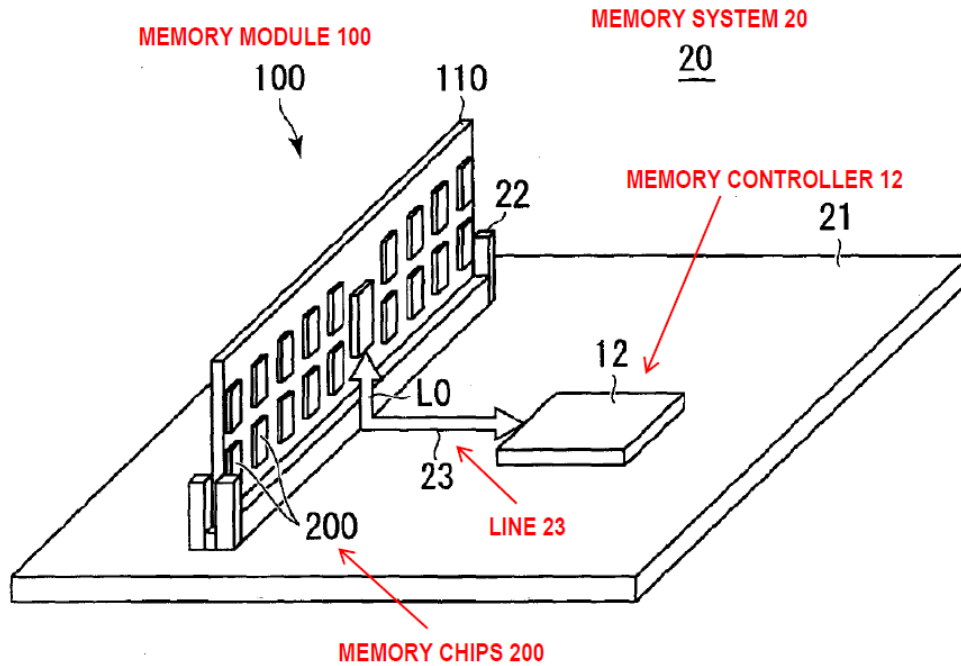


FIG.3

40. The data register buffers 300 intervene between the data connectors 120 and the memory chips 200. EX1005, [0103]. See FIG. 7 below.

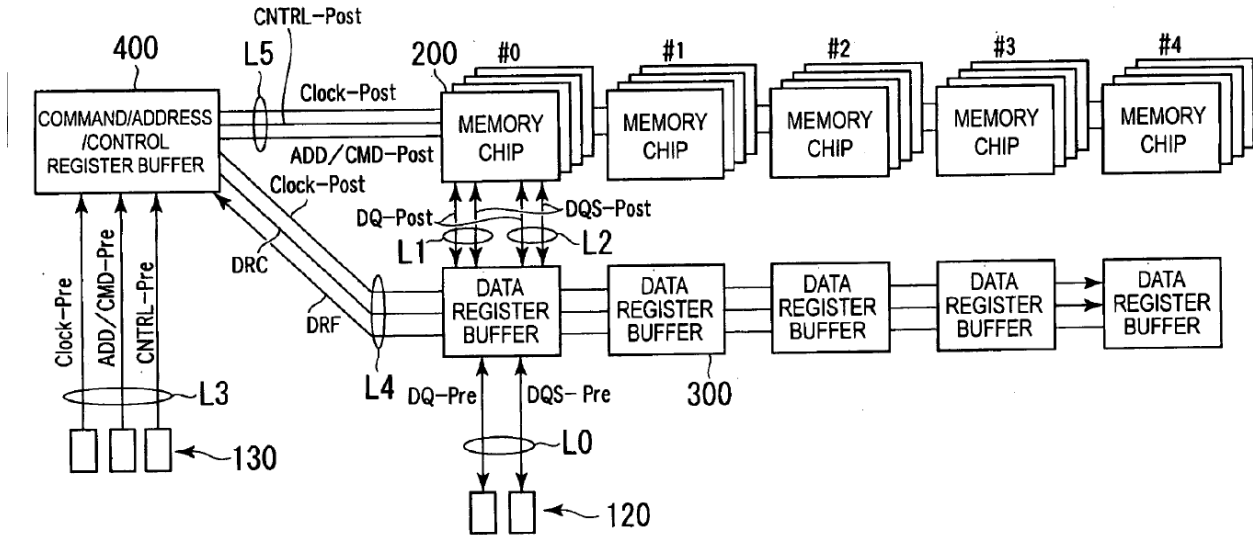


FIG. 7

41. Similarly, because the command/address/control register buffer 400 is connected to the command/address/control line L3, the memory controller cannot experience the load capacitance of the memory chips 200 that exist on the signal path beyond the command/address/control register buffer 400. Therefore, the load capacitance of the signal path that connects the memory controller and the memory module 100 is reduced, making it possible to reliably achieve a high data transfer rate. *See id.*, [0069].

42. The memory module 100 includes a plurality of memory chips 200 arranged in a 4-rank configuration, a plurality of data register buffers 300, and a command/address/control register buffer 400. *See id.*, [0046], [0051]. Data

connectors 120 are connectors for exchanging write data and read data read between the memory module 100 and the off-module memory controller. *See id.*, [0048]. The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal from the off-module memory controller to the command/address/control register buffer 400. *See id.*, [0049].

43. As shown in FIG. 7, the data register buffers 300 intervene between the data connectors 120 and the memory chips 200. *See id.*, [0103]. The data connectors 120 and each of the data register buffers 300 are connected via data/strobe signal lines L0, and each of the data register buffers 300 and the corresponding memory chips 200 are connected to each other via data/strobe signal lines L1 or L2. *See id.* Data/strobe lines L0-L2, each consisting of one DQS and multiple DQ lines, transfer data and data strobe signals between the memory controller, data register buffers 300 and memory chips 200. Data connectors 120 exchange write data and read data between the memory module 100 and the off-module memory controller (controller 12). *See id.*, [0048].

44. The command/address/control connectors 130 and the command/address/control register buffer 400 are connected via the command/address/control line L3. *See id.*, ¶ [0107]. The command/address/control register buffer 400 and each of the data register buffers 300 are connected via control

line L4. See *id.* The command/address/control register buffer 400 and the memory chips 200 are connected via a command/address/control line L5. See *id.*

45. During operation, a command/address/control signal, a control signal and a clock signal can be transferred via command/address/control line L3 from the memory controller and supplied to command/address/control register buffer 400. See *id.*, ¶[0054]. The command/address/control register buffer 400 buffers the signals to the memory chips 200 and generates a control signal and clock to be supplied to data register buffers 300. See *id.*, [0060]-[0061].

46. Hiraishi recognizes that the placement of the data register buffer between the memory chips 200 and the memory controller affects the timing of memory read and write operations. See *id.*, [0104]. In relation to the timing for the data register buffer, Hiraishi requires two distinct read leveling adjustments and two distinct write leveling adjustments be performed during initialization. See *id.* Specifically, the read leveling operations and write leveling operations are performed during an initialization stage before read and write operations can begin. See Fig. 13, Steps S4 and S5 (reproduced below).

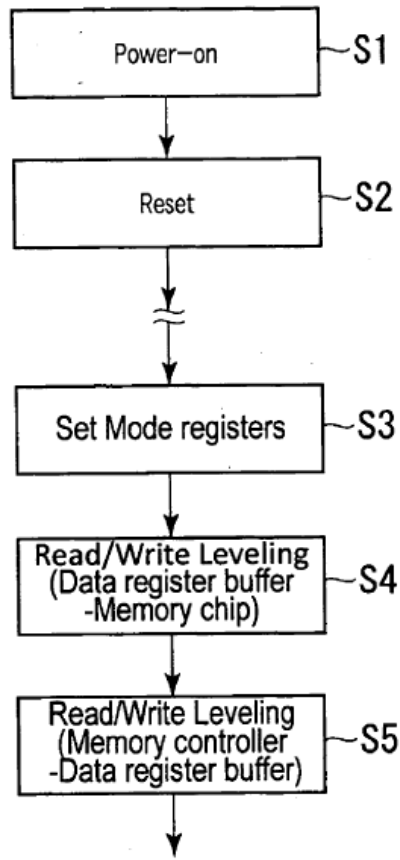


FIG.13

47. Hiraishi's FIG. 13 is a flowchart for explaining initialization of the memory module 100 at the time of activation. *See id.*, [0138]. During initialization Step S4, a read leveling function and a write leveling function for the interface between the memory chips 200 and the data register buffers 300 are performed. *See id.*, [0142]-[0151]. I will generally refer to the write and read leveling functions between a data register buffer 300 and a memory chip 200 as "S4 leveling."

48. Additionally, during initialization Step S5, read leveling and write leveling functions for the interface between the memory controller 12 and the data

register buffers 300 are performed. *See id.*, [0141], [0152]-[0161]. I will generally refer to these write and read leveling functions between a data register buffer 300 and a memory controller 12 as “S5 leveling.”

49. Hiraishi’s S4 leveling and S5 leveling are performed by different circuitry. Specifically, the S4 leveling is performed by write leveling circuit 322 and read leveling circuit 323 in a data register control circuit 320 of the data register buffer 300. *See id.*, Fig. 5 (annotated and reproduced below).

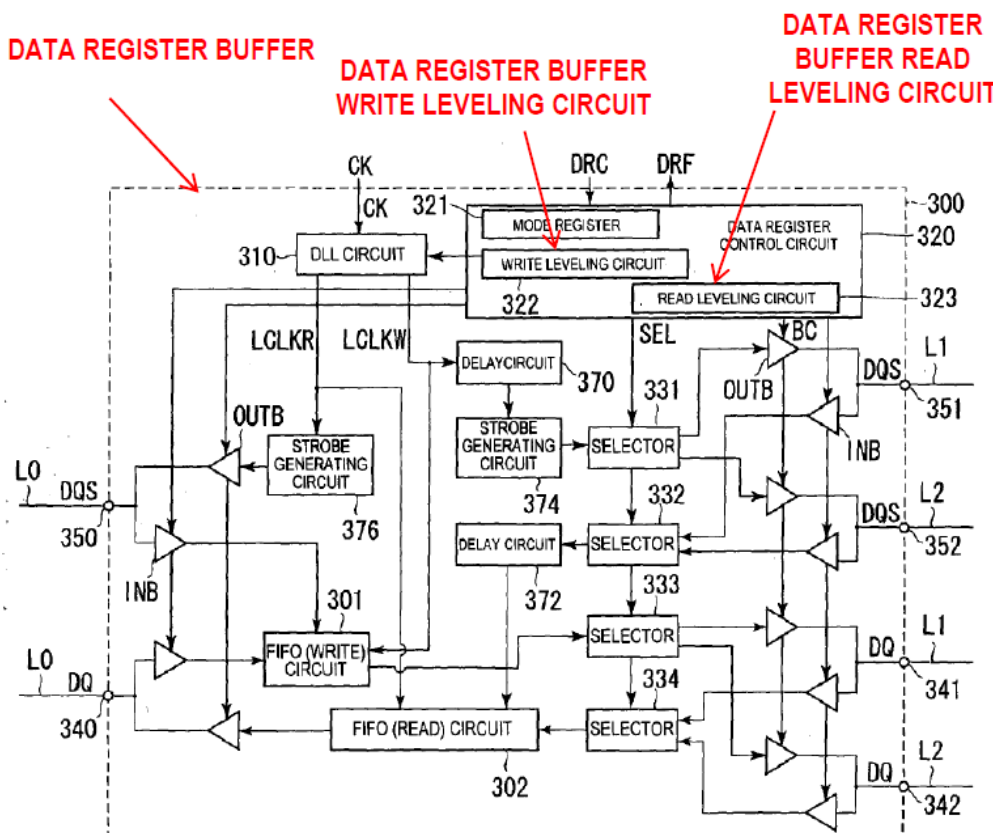


FIG.5

50. The S5 leveling, in contrast, is performed by write leveling circuit 12a and read leveling circuit 12b in the memory controller 12. *See id.*, Fig. 2 (annotated and reproduced below).

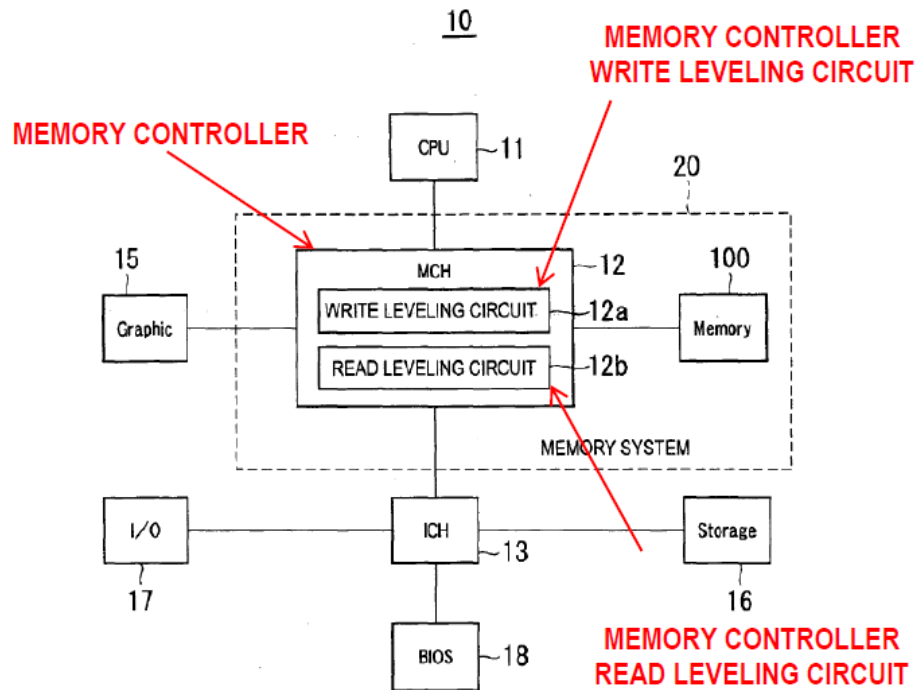
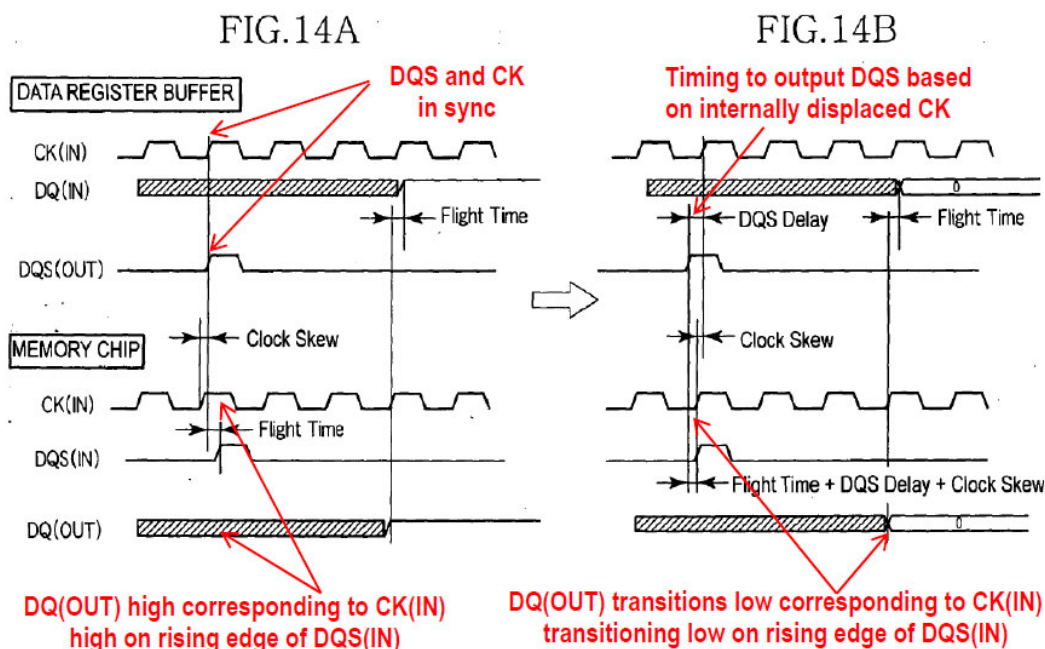


FIG.2

51. Hiraishi's S4 write leveling accounts for mismatch between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. *See id.*, [0142]-[0143]. The mismatch is due to the differential propagation delay of CK versus the DQS generated by the data register buffer 300 (to be sent to terminal 351 or 352). *See id.*, [0143]. The clock signal is provided from the command/address/control register buffer 400 directly to the memory chip 200, as well as provided to data register buffer 300 to synchronize the generation of the DQS

signal. *See id.* A result of the write leveling operation is stored in the data register control circuit 320 in the data register buffer 300. *See id.*, [0146]. Upon completing S4 write leveling, the phase of the clock signal CK and the DQS signal input to the memory chip are aligned. *See id.*, [0144], [0146].

52. Hiraishi achieves the timing alignment of S4 write leveling by adjusting the output timing of the DQS signal by displacing the internal clock LCLKW of data register buffer 300. *See id.*, [0145]. As illustrated in Fig. 14A, to begin, the data register buffer 300 generates a DQS signal, DQS(OUT), in synchronization with the CK signal, CK(IN). *See id.* During the write leveling function, memory chip 200 can output a logic value on a DQ signal, DQ(OUT) corresponding to the state of clock signal received by the memory chip, CK(IN), on the rising edge of the DQS signal received by the memory chip, DQS(IN). *See id.*



53. Data register buffer 300 can displace the internal clock LCLKW in the opposite direction of the phase shift to displace the generation of the DQS signal, DQS(OUT) with respect to the clock signal, CK(IN). *See id.*, [0145]-[0146]. Eventually, as illustrated in Fig. 14B, DQ(OUT) transitions when the state of clock signal transitions on the rising edge of the DQS signal received by the memory chip. *See id.* The displacement of LCLKW can be stored in data register control circuit 320. *See id.*, [0146].

54. Hiraishi's S4 read leveling is performed by read leveling circuit 323 of data register buffer 300. *See id.*, [0147]. Hiraishi does not explain how to perform the read leveling function. Hiraishi's S4 read leveling operation determines when input buffers INB are activated to receive read data signals and strobe signals coming from memory chips 200 over L1 and L2 via terminals 341, 342, 351, and 352. EX1005, [0140], [0147-151], Fig. 15. I understand Dr. Wedig agreed during his deposition that the read leveling in Hiraishi adjusts the timing of the activation of input buffers INB. EX2016, 59:4-18.

55. A control signal from Data Register Control Circuit 320 (which includes read leveling circuit 323) turns on input buffers for signals DQS and DQ before the expected arrival of the data and strobe signals so they can pass through to the selectors and be captured by the FIFO (Read) circuit 302 according to the timing information provided by the corresponding strobe signal. EX1005, FIG. 5, [0088],

[0151]. As such, Hiraishi's read leveling adjusts the timing of when the input buffers INB are turned on so they are active when data arrives; it does not adjust the timing of any data or data strobe signal on the bus or within the buffer. EX1005, [0151] ("The time is ... used in an adjustment of an activation timing of the input buffer circuit INB and the like."). The results of Hiraishi's read leveling adjustment are "stored in the data register control circuit 320 in the data register buffer 300" *Id.*, [0151].

56. I further understand that Dr. Wedig believes that Hiraishi's S4 read leveling involves additional operations beyond activating the input buffers INB based on the fact that Hiraishi discloses that "[t]he time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB *and the like.*" EX1005, [0151] (emphasis added); EX2016, 59:19-60:18. However, a POSA would understand Hiraishi's use of the phrase "and the like" to refer to similar activation circuitry necessary for the data buffer to receive read data as and when it arrives, through possible equivalent but different structures.

57. Therefore, Hiraishi describes an approach for read leveling that does not rely on adjusting the timing of the strobe signals themselves, but instead only adjusts the timing of when the input buffers INB are turned on, so they are active

when data arrives. Hiraishi does describe a separate re-timing operation which I discuss below.

58. Hiraishi's S5 read leveling function is performed by read leveling circuit 12b of the memory controller, and not by the data buffer 300. EX1005, [0157]. Moreover, while S4 leveling pertains to data transmission between the memory chips 200 and the data register buffers 300 (*see id.* at [0140],[0142],[0147]), S5 leveling pertains to transmissions between the memory controller and the data buffer. *See id.*, [0141, [0152 – 0156], [0157 – 0161]. S5 read leveling begins with the memory controller outputting the clock signal CK, the activate command (ACT) and the read command (Read). *See id.*, [0158]. The clock signal CK is supplied to the data register buffer 300, and the read command is supplied to the data register buffer 300 (*e.g.*, as a part of the control signal DRC) via the command/address/control register buffer 400. *See id.* The data register buffer 300 can automatically generate a dummy output data pattern in response to the Read command. *See id.*, [0160]. The dummy data output by the data register buffer 300 can be received by the memory controller, and used to determined time B. *See id.*, [0161].

B. Butt (EX1029)

59. Butt discloses a method for DQS strobe centering for DDR memory using a specialized circuitry, specifically in the form of circuit 104. With reference

to FIG. 2 below, Butt describes the specialized circuit 104 as being coupled to the memory controller 102, and includes a number of physical read datapaths (DPs) 114, each of which receives “(i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118.” EX1029 (Butt), [0017].

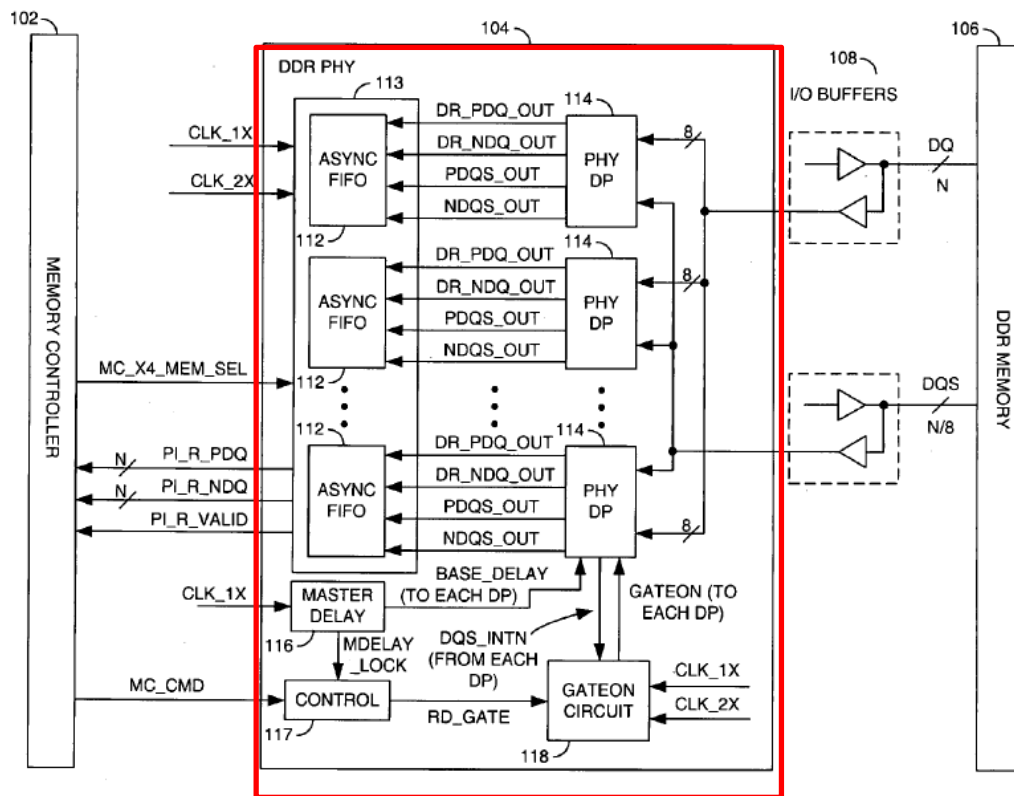


FIG. 2

60. Butt describes that “the circuit 104 generally receives aligned DQ and DQS signals from the DDR SDRAM device(s) 106.” *Id.*, [0033]. Butt applies a base delay (using clock signal CLK_1X) “to center a read data capture clock (e.g., the

signal DQS) in a valid DDR device read data window.” *Id.*, [0021]. Butt refers to this delay as a base delay (e.g., BASE_DELAY_UN). *See id.*, [0022].

61. In addition to the base delay prescribed by the DDR standard, Butt discloses a method for using the specialized circuit 104 to “determine[] optimum offset delay values for each of the DPs 114 and loads (or programs) the optimum offset delay values into the DPs 114 (e.g., the block 208).” *Id.*, [0046]. Butt determines the optimum offset delay value for each DP 114 by calculating the highest delay setting that yields valid data, referred to as the maximum offset for the respective delay, and calculating the lowest delay value that yields valid data, or the minimum offset for the respective delay. *See id.*, [0048]-[0053], [0056]-[0060]. The optimum offset value is then determined based on the average of the maximum and minimum offset values. *See id.*, [0046].

62. As shown in FIGs. 6-7, to determine the maximum and minimum offset values, Butt discloses using a positive adjustment routine, in the case of determining the maximum offset value, and a negative adjustment routine, in the case of determining the minimum offset value. *See id.*, [0048]-[0053], [0056]-[0060]. In both cases, a current offset value is incremented and the corresponding read data is tested. This proceeds until valid data cannot be read. *See id.*, [0052], [0059]. This is illustrated in FIG. 4, reproduced below.

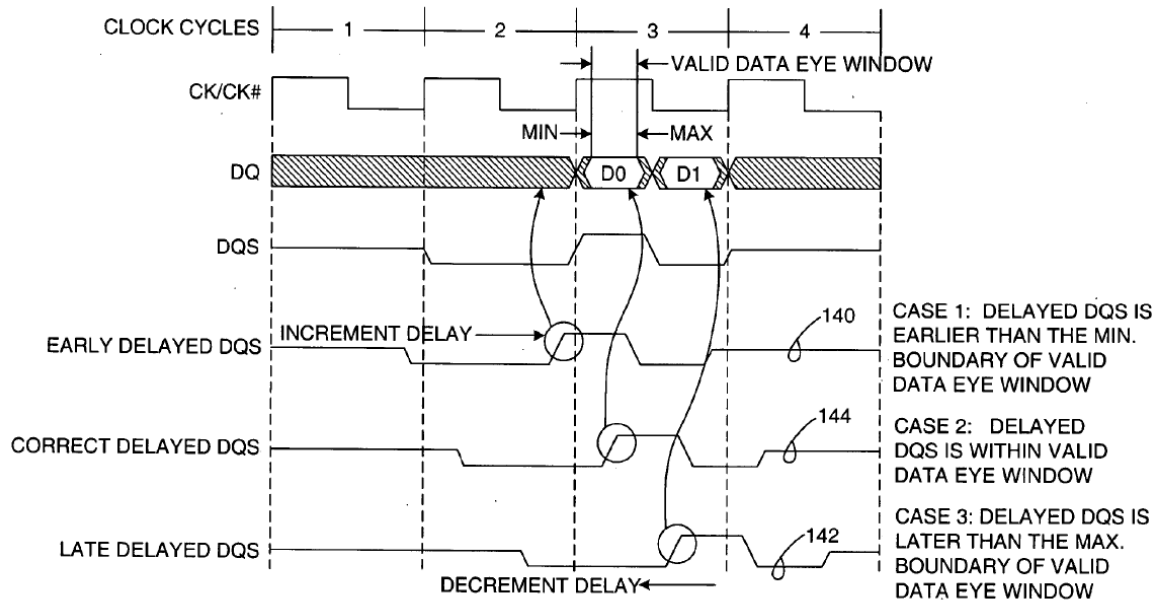
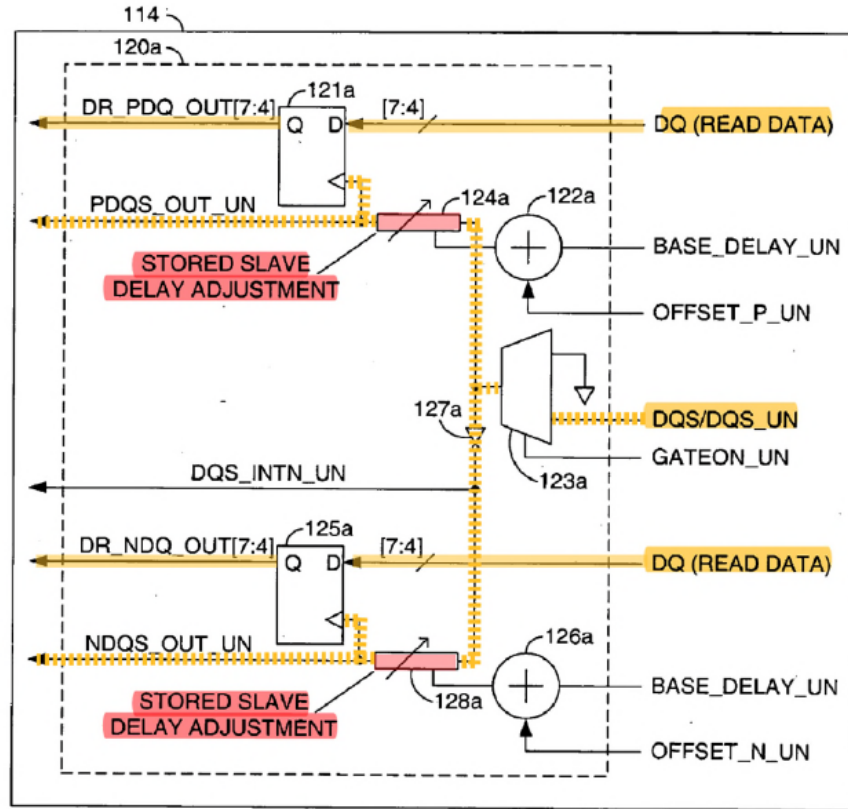


FIG. 4

63. The process of determining the optimum offset value and then applying the offset value is performed by each DP 114, a more detailed diagram of which is provided in FIGs. 3A-3B which “illustrat[e] an example read data latching and gating circuit in accordance with a preferred embodiment of the present invention.” *Id.*, [0025]. That the offset delay is determined by and stored in each DP 114 is confirmed by FIG. 3A. Below I have reproduced the annotated version of FIG. 3A from the Petition. *See* Petition, 36.



C. Tokuhiro (EX1006)

64. Tokuhiko discloses a fly-by topology for command/address/clock wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11. EX1006 (Tokuhiko), 5:24-30. Tokuhiko purports to describe an improved off-module memory controller that incorporates known write leveling mechanisms, as disclosed in the JEDEC DDR3 SDRAM Standard, JESD79-3. *See* EX1006, 1:22-32; 2:10-18; 2:46-49; 2:54-59. The specification describes this as follows:

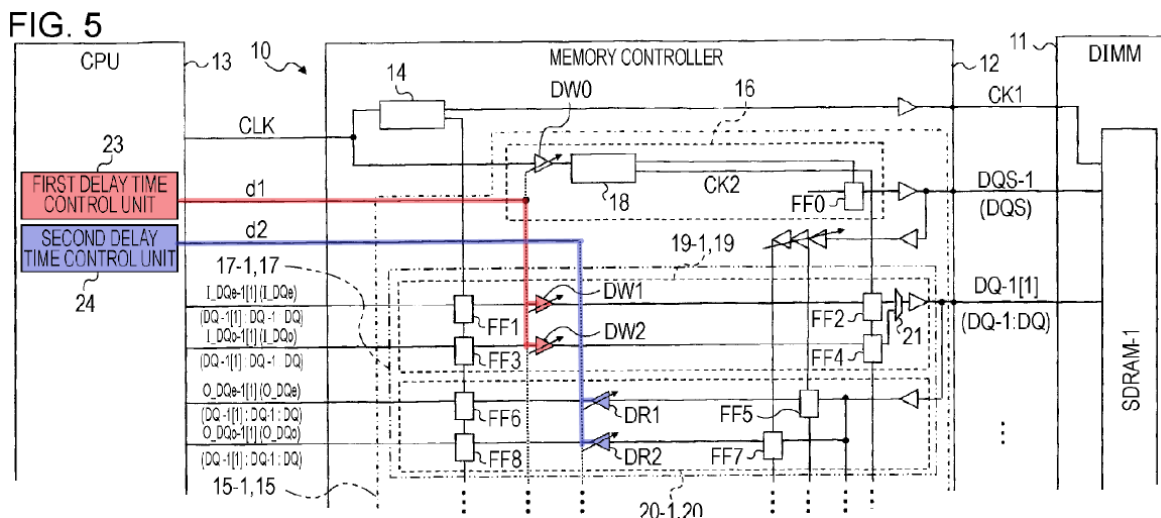
The term “write leveling function” refers to the function of sampling the clock signal CK by using the data strobe signal DQS output from the memory controller 90, detecting the phase relationship between the data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.

EX1006 (Tokuhiro), 2:13-18.

65. In this way, “the difference in the delay time caused in the write operations between the memory controller . . . and the plurality of SDRAMs . . . is adjusted by employing the write leveling function.” *Id.*, 2:46-49. Tokuhiro’s memory controller performs a write leveling operation to account for different flight times to different memory devices and to delay the respective data strobe signals accordingly so that strobe signals and clock signal from the system memory controller will arrive at respective SDRAMs on the memory module at substantially the same time. EX1006, 2:39-45, 12:59-63.

66. Tokuhiro focuses on computing time delays for compensating signals during read operations using detected delays by the known JEDEC write leveling function. These operations are determined by and carried out under the control of a first delay time control unit 23 (highlighted in red below) and second delay time control unit 24 (highlighted in blue below) located in the computer’s CPU 13. *See e.g., id.* at Figs. 4-6, 8, 9, 12-15. In all these figures, the CPU’s first and second delay time control units 23 and 24 output control signals d1 and d2 to control variable

delay circuits DW and DR in the memory controller 12. See annotated partial reproduction of FIG. 5 from Tokuhiro below.



67. Tokuhiro explains that the “first delay time control unit 23 outputs the respective first control signals d1 to the first variable delay circuits DW-1 to DW-n so that the set first delay times Dt1-1 to Dt1-n are obtained” *Id.*, 14:59-62. Moreover, “[t]he second delay time control unit 24 controls the second variable delay circuit DR ... to delay the data signal by the second delay time Dt2 in accordance with corresponding one of the first delay times Dt1-1 to Dt1-n set by the first delay time control unit 23, and it outputs the second control signal d2 for setting the second delay time Dt2.” *Id.*, 15:3-9. Tokuhiro explains that “since the plural data signal lines connecting the memory controller 12 and the DIMM 11 to each other are formed in the same length, the formula for calculating the second delay time Dt2 is simplified and the second delay time Dt2 for the data signal DQ input from the SDRAM during the read operation can be easily obtained. *Id.*, 19:8-13.

IX. GROUND 1 DOES NOT SATISFY ELEMENT 1[F]

A. Recited “Data Path” Does Not Include Strobe Signal Lines

68. Dr. Wedig relies on Hiraishi’s DQS strobe signal lines as being included in the recited “data path.” *See e.g.*, EX1003, ¶142. EX2012, 40:11-16 (“Q. What is the data path through Hiraishi's buffer shown in Figure 5? A. So it’s – it’s at least all of the orange lines, both solid and hashed, shown in the two depictions of Figure 5 on page 98 of my declaration.”) (objection omitted).

69. Below I reproduced the annotated figure to which Dr. Wedig was referring.

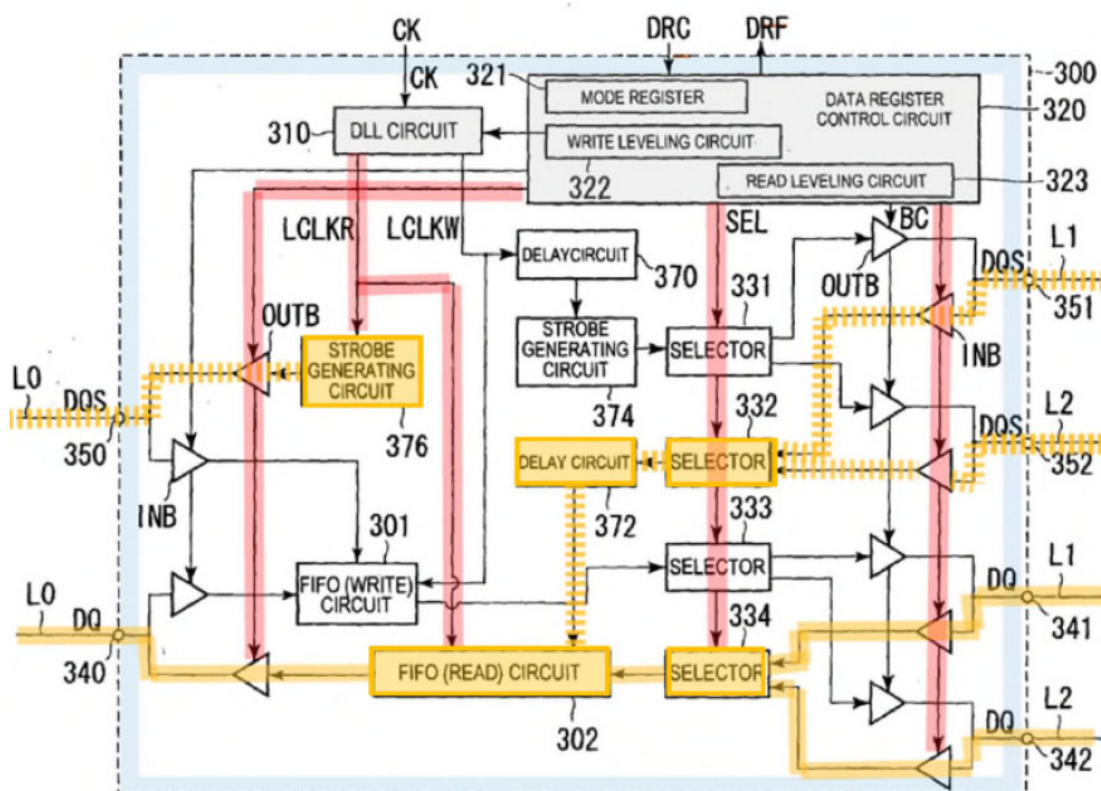


FIG.5

EX1003, p. 98; EX2012, 40:21-41:1 (“Q. So to satisfy the data path that’s recite in Claim 1 you’re identifying the combination of the solid orange DQ paths and the crosshatched DQS paths; is that -- do I understand that correctly? A. Yes. As illustrated in the two representations of Figure 5. Yes, that's correct.”).

70. I do not agree with Dr. Wedig that strobe signal lines are part of the “data path” recited in the claims of the ’608 patent. First, I note that claim 1 requires that “each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines.” Claim 1 makes it clear that a data signal line is different from a strobe signal line. This requirement would be understood by a POSA to mean that the recited “data paths” correspond to the “data signal lines” in the recited “set of data/strobe signal lines,” and not to strobe signal lines. A POSA would know that the term data path is used to describe the path over which data flows among multiple hardware components, not a path over which strobe signals flow. Also, since each strobe signal path in Hiraishi corresponds to a byte or 8 data signal lines (EX1005, [0053]), Hiraishi does not disclose any path that corresponds to *each* data signal line. Second, the claims are consistent with the specification which also distinguishes between data paths carrying data signals and strobe paths carrying strobe signals. For example, in FIG. 3 the ’608 patent illustrates an embodiment of an isolation device 118, which the patent interchangeably also refers to a buffer circuit. EX1001, 3:27-29, 4:30.

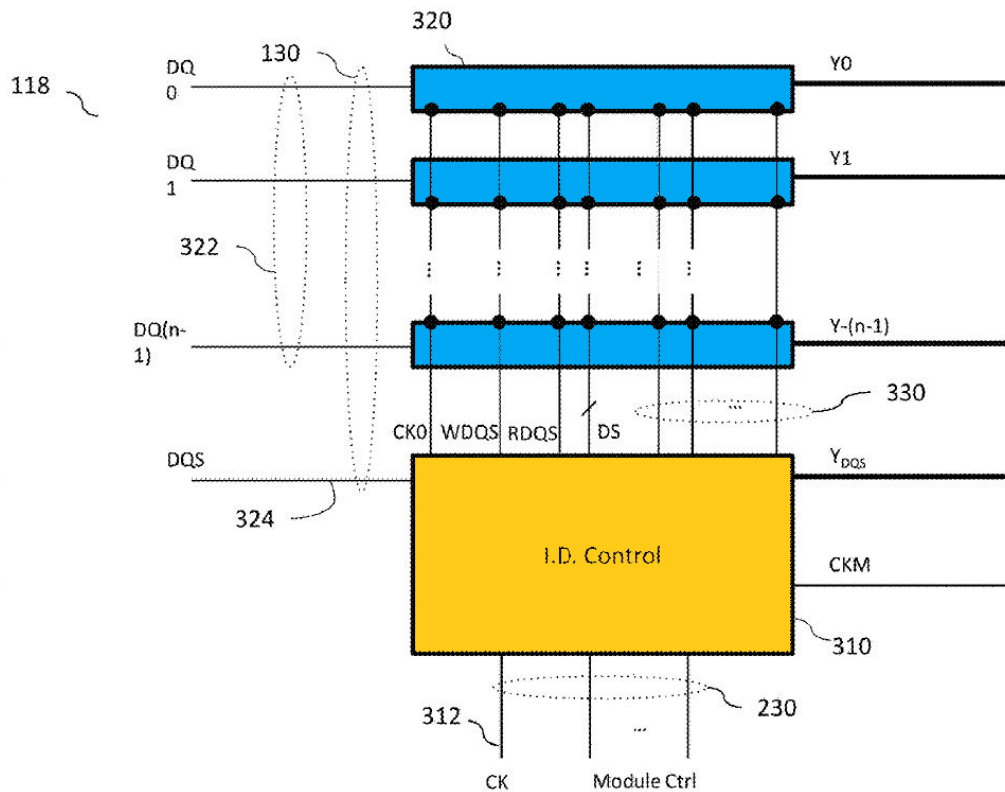


FIG. 3

71. The '608 patent describes FIG. 3 as illustrating that “each group of signal lines 130 include a set of n *data (DQ) signal lines 322* each for transmitting one of a set of data signals $DQ_0, DQ_1, \dots, DQ_{n-1}$, and at least one *strobe (DQS) signal line 324* for transmitting at least one strobe signal DQS .” EX1001, 10:31-35. Also, “[e]ach set of module data/strobe lines Y include a set of n module data signal lines $Y_0, Y_1, \dots, Y_{n-1}$ and at least one module strobe signal line Y_{DQS} .” *Id.*, 10:35-38. In addition, the buffer circuit of FIG. 3 includes a “a set of DQ routing circuits 320 [blue] coupled on one side to respective ones of the set of n DQ signal lines 322, and

on another side to respective ones of the respective set of n module data lines”

EX1001, 10:50-53. An ID control circuit 310 [orange] is couple to the DQS signal line 324.

72. I also note that the '608 patent discloses separate circuitry for routing DQ signals and which is used for routing DQS signals. Specifically, the DQ routing circuit 320 of FIG. 3 receives the DQ signal lines 322, while a separate DQS routing circuit 620, which is part of the ID control circuit 310, receives the DQS signal line 324. See EX1001, FIG. 6 below (DQS routing circuit 620 in purple); see also *id.*, 12:3-37.

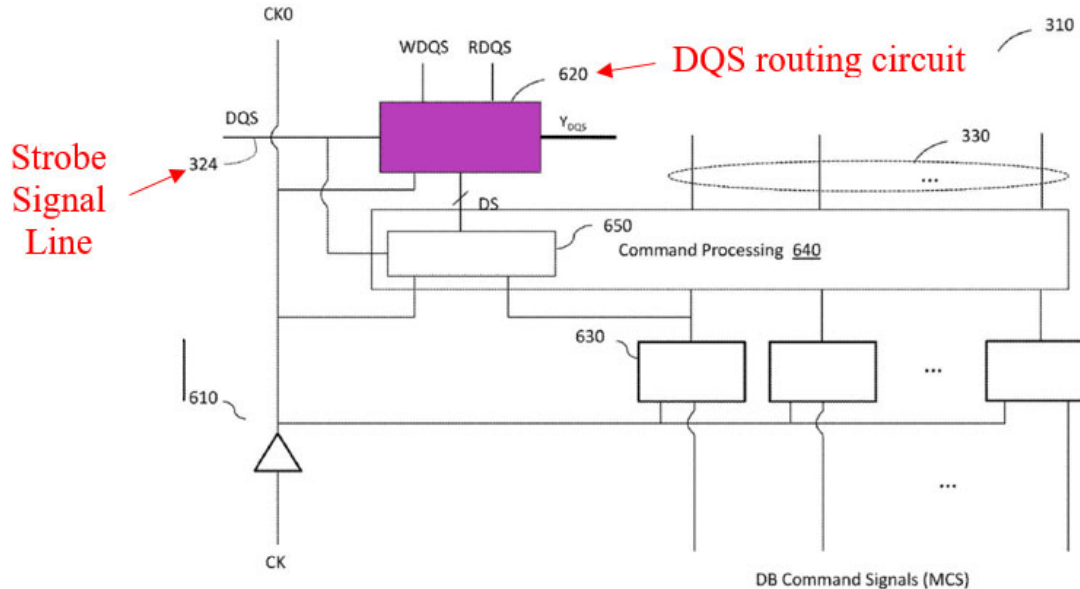


FIG. 6

73. I also note that the '608 patent distinguishes between strobe paths and data paths and discloses using the above-mentioned separate circuitry for routing.

For example, FIG. 15 below is a DQS routing circuit 620 for DQS 324 to be provided from a first DQS pin 1501 to one of a second DQS pin 1502A or third DQS pin 1502B. *See id.*, 16:47-17:22.

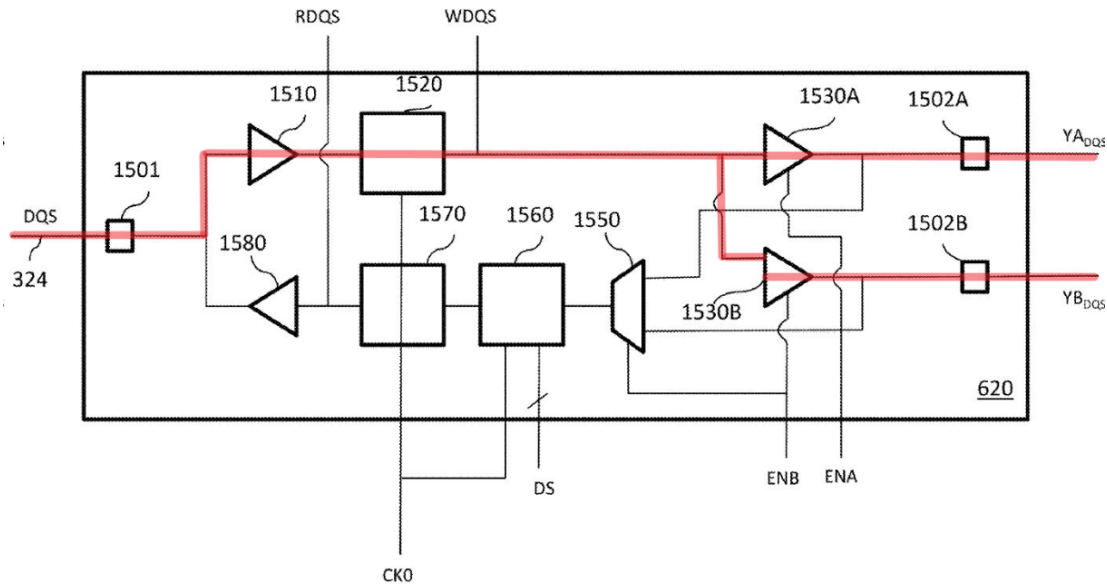


FIG. 15

74. The '608 patent describes, and FIG. 15 above is annotated in red to show, a “***first write strobe path*** coupled between the first DQS pin 1501 and the second DQS pin 1502A and a ***second write strobe path*** coupled between the first DQS pin 1501 and the third DQS pin 1502B.” *Id.*, 16:53-57; *see also id.*, 16:57-17:7 (describing components along first and second write strobe paths for processing DQS signals); *see also id.*, 17:8-22 (describing first and second ***read strobe paths*** and related components).

75. On the other hand, FIG. 16 below is a DQ routing circuit 320 for DQ signal 130 to be provided from a first DQ pin 1601 to one of a second DQ pin 1602A or third DQ pin 1602B. *See id.*, 17:23-29.

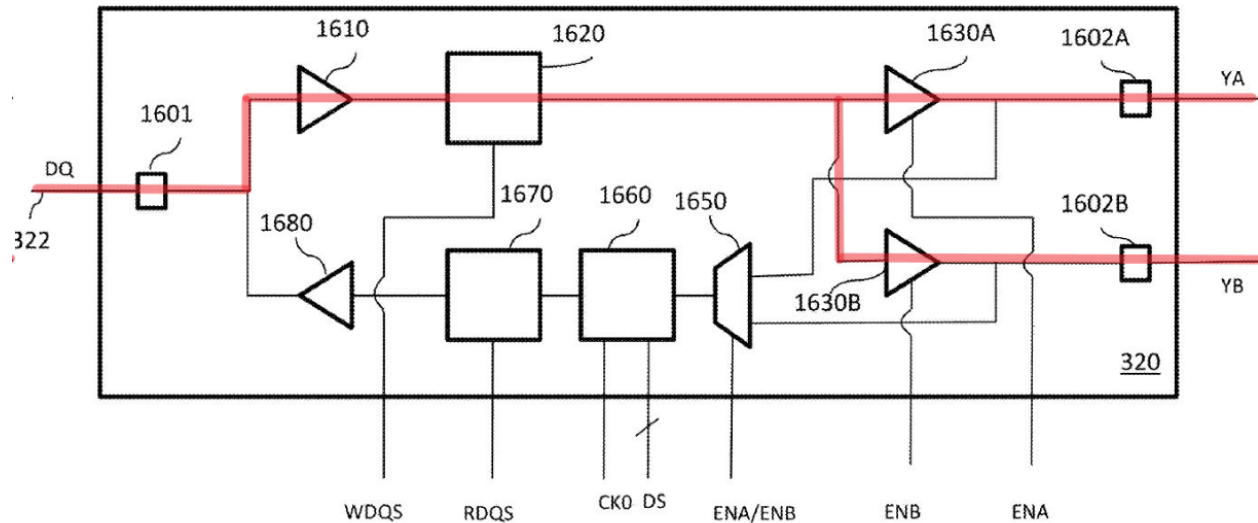


FIG. 16

76. In describing the DQ routing circuit 320 of FIG. 16, the '608 patent discloses, and FIG. 16 above is annotated in red to show, a “**first write data path**” coupled between the first DQ pin 1601 and the second DQ pin 1602A and a **second write data path** coupled between the first DQ pin 1601 and the third DQ pin 1602B.” *Id.*, 17:29-33; *see also id.*, 17:33-47 (describing components along first and second write data paths for processing DQ signals); *see also id.*, 17:48-60 (describing first and second **read data paths** and related components) (see annotated FIG. 16 below in ¶ 82 showing read path). As can be seen, no part of the DQ routing circuit 320 includes any component which allows a strobe signal through it. The read strobe

signal RDQS and write strobe signal WDQS are received by the read sampler 1670 and write sampler 1620, respectively, and are used by the samplers to sample the respective data signals. The strobe signals do not reappear from the samplers and travel through any segment of the data paths.

77. Based upon the ordinary use of the term data path in the industry, and supported by the claim language and at least the portions of the specification described above, a POSA would understand that the recited “data path” corresponds to data signal lines which carry data signals, not to strobe signal lines which carry strobe signals.

78. I note that Dr. Wedig does not identify any support from the '608 patent in his declaration for his position that the recited “data path” includes strobe signal lines. I understand, however, that during his deposition Dr. Wedig identified two locations in the '608 patent that he contends supports his position that the recited “data path” includes strobe signal lines. First, he identified claim 10, and second he identified a passage at col. 3, lines 57-60 of the '608 patent. However, Dr. Wedig's understanding of claim 10 is incorrect. Dr. Wedig indicated that he understands that the recited “first data path” from claim 10 is the same “data path” of claim 1. EX2012, 45:12-46:13. However, as an initial matter I understand that claim 10 has been disclaimed and therefore no longer forms any part of the '608 patent. EX2001. Even then, claim 10 does not support Dr. Wedig's position because the element in

question in claim 10 is introduced as “*a* first data path” which requires it to be *different*, not the same, as the “data path” of claim 1. With respect to the passage Dr. Wedig identified on col. 3, lines 57-60 of the ’608 patent, it only says that “each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller.” This passage does not mention strobe signal lines at all. It only indicates that the buffer circuit is in the data path, which would be satisfied by virtue of the data signal lines extending to and from the buffer circuit. To the extent that Dr. Wedig interprets this passage to mean that the entire buffer circuit must reside inside of the data path, that understanding would be at odds with the rest of the specification which expressly distinguishes data paths from strobe paths.

79. I also note that the Butt reference cited by Dr. Wedig also distinguishes between signal lines that carry DQ data and signal lines that carry DQS strobe signals. See below (showing solid orange lines for DQ data signals and cross-hatched lines for DQS strobe signals).

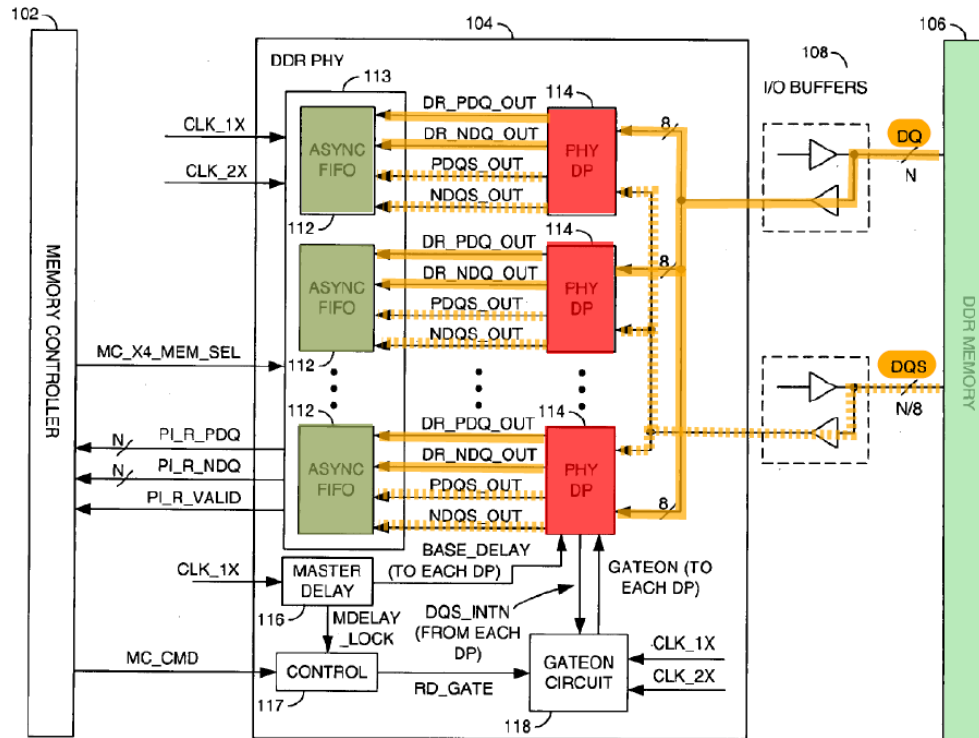


FIG. 2

EX1003, ¶ 144 (citing EX1029, Fig. 2).

80. I note that Butt does not suggest that data signal lines include strobe signal lines. See EX1029, FIG. 3A (showing “datapaths 114” maintain separate data signal lines (yellow) and strobe signal lines (turquoise)).

B. The Delayed Signal Must Be “Through the Data Path” And Delayed by a “Delay Circuit” Residing in the “Data Path”

82. I also note that claim 1 recites that “*the data path* corresponding to the each data signal line *includes ... a delay circuit* configured to *delay a signal through the data path*” This means that the recited delayed signal is through the corresponding buffer circuit’s data path, which corresponds to a data signal line carry data signals, and that the delay circuit resides in the corresponding buffer circuit’s data path, as I described above. For example, FIG. 16 illustrates a DQ routing circuit 320 having “a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line $Y_{A_{DQ}}$, a third DQ pin 1602B that is coupled to a corresponding module DQ line $Y_{B_{DQ}}$.” EX1001, 17:23-29.

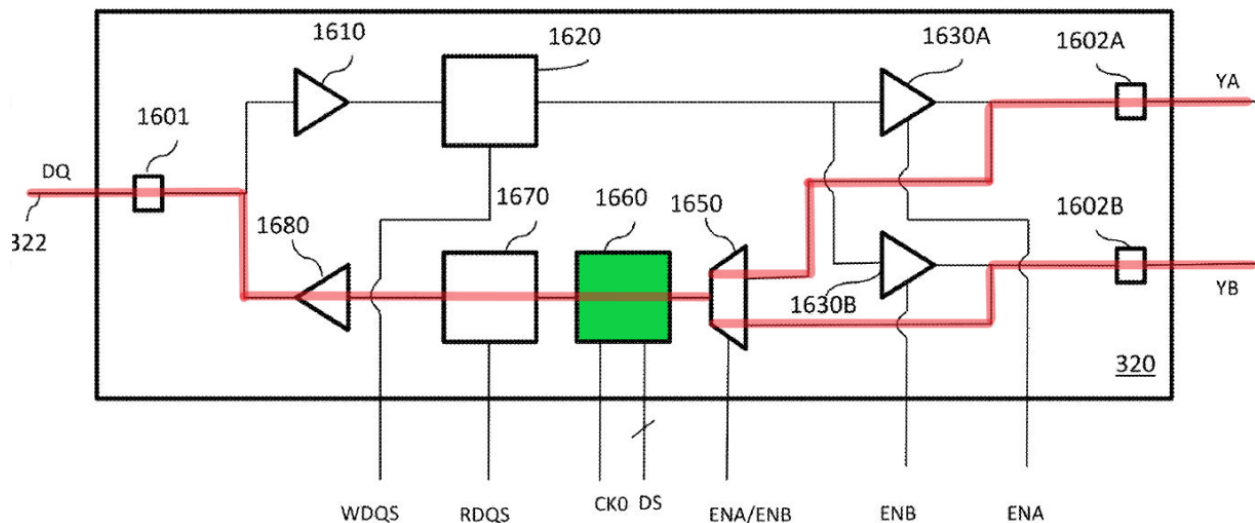


FIG. 16

As shown above, the DQ routing circuit 320 includes write and read data paths coupled between the first DQ pin 1601, on the one side, and either of the second and third DQ pins 1602A/B, on the other side. *See id.*, 17:29-60. A delay circuit 1660 (showing in green) is in a data path (shown in red), which in FIG. 16 above is a read data path between first DQ pin 1601 and second and third DQ pins 1602A and 1602B. The '608 patent describes the delay circuit 1660 as delaying a “selected read data signal ... by an amount controlled by the delay signal DS.” *Id.*, 17:54-55. Thus, just as the claims recite, the disclosed “delay circuit” resides in the corresponding buffer circuit’s data path, as opposed in to residing in a non-data path, such as a strobe path or clock signal path.

83. As I noted above, neither the Petition nor Dr. Wedig rely on the Butt to satisfy any claim limitations art. Instead, Butt is relied on only as alleged evidence of knowledge in the field and how Hiraishi allegedly should be interpreted. See Pet., 36; EX1003, ¶144 (“[A] Skilled Artisan would have understood from the disclosure of Butt that Hiraishi’s data register buffer 300 includes “data paths” (orange) using data strobe signals to sample the data and buffer the sampled data in respective FIFO circuits.”). I note that the Board found “that although Butt is a named secondary reference, Hiraishi is the main reference relied upon for the teachings of the claim limitations, and Butt is used to provide further explanations or interpretations of the

teachings of Hiraishi and/or to explain the knowledge of one of ordinary skill in the art.” Institution Decision at 11-12.

84. Therefore, the Petitioner and Dr. Wedig rely on Hiraishi alone for satisfying the limitations of the ’608 patent, including Element 1[f] which recites “a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.”

C. Dr. Wedig Has Not Established That Hiraishi Discloses the Recited “Delay Circuit” or Delayed “Signal through the Data Path”

85. To satisfy the recited “delay circuit,” Dr. Wedig expressly identifies the combination of Hiraishi’s “DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376.” EX1003, ¶¶152, 161. Dr. Wedig confirmed that his analysis is based on this combination. EX2012, 17:23-18:5 (“I believe that all of those different parts make up the delay circuit, so I guess yes, *it’s a combination of those*. I mean, *they all work together to implement the delay circuit.*”); 20:10-16 (“Q. ... So is it your opinion that the delay circuit that Hiraishi discloses that reads on the claims of the 608 patent includes the FIFO read circuit 302, the delay 16 circuit 372, the strobe generating circuit 376 and then the DLL circuit 310? A. As part of it, yes. And then additionally it has the LCLKR signal.”); 26:25-27:3 (testifying that “the delay circuit for write operations is comprise[d] of the FIFO write circuit 301 and the LCLKW.

Let's see here. The strobe generating circuit 370 and 374. Those are the -- those are the main components.”)

86. However, the recited “delay circuit” resides in the data path and delays “a signal through the data path,” and does so “in response to at least one of the module control signals.” In contrast, the combined circuitry identified by Dr. Wedig as allegedly satisfying the recite “delay circuit” does not satisfy these requirements, as explained below.

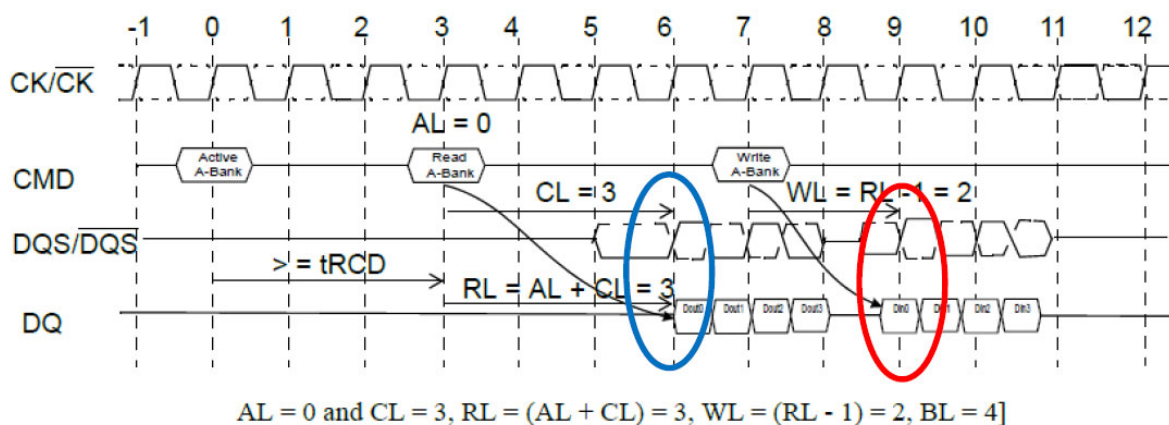
1. The Alleged “Delay Circuit” for Write Operations

a) The Delay Circuit 370

87. Hiraishi’s delay circuit 370 delays the local clock signal (LCLKW) signal. A POSA would understand that this does not satisfy Element 1[f] because (1) any delay imparted the delay circuit 370 is not “in response to at least one of the module control signals,” and (2) the delay circuit 370 is not in a data path and does not delay a data signal at all.

88. With respect to (1), Hiraishi explains that “[a] phase of the data strobe signal DQS generated by the strobe generating circuit 374 is delayed by about 90 degrees with respect to the internal clock LCLKW by a delay circuit 370.” EX1005, [0092]. This quote is the only explanation that Hiraishi provides for the function of delay circuit 370. A POSA would recognize that this fixed delay relates to DDR standard requiring a center-aligned data strobe signal be provided by the memory

controller for all DRAM writes, which the DRAM uses directly to sample the incoming data. EX2014 (JESD79-2F), 13 (stating that the strobe signal is “[e]dge-aligned with read data, centered in write data.”); EX1019 (JESD79-3C), 34; EX2015 (JESD79-3F-2), 13; EX1021 (Jacob), 334-335. The difference in DQ/DQS alignment for read and write operations is illustrated in the DDR standard as well, as shown below.



AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]
Figure 31 — Example 2: Read followed by a write to the same bank,
where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

EX2014 (JEDEC Standard No. 79-2F), Figure 31, page 33 (showing edge-aligned DQ/DQS for read command and 1/4 clock cycle offset (center-aligned) DQ/DQS for write command). Moreover, in describing FIG. 11, which is a timing chart for a read operation of memory module 100, Hiraishi states that “[t]he data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). EX1005, [0129]. This

90-degree delay corresponds to a quarter clock cycle, which is the same fixed base delay added by Butt. EX1029, [0021]. A POSA would understand that, just as in Butt's quarter-clock-cycle delay, Hiraishi's quarter-clock-cycle delay is the product of the fact that, for DRAM reads, the data strobe is edge-aligned with the data, and therefore it is necessary to shift the edges of the DQS signal about a quarter clock cycle (90 degrees) toward the center of the data period for read operations.

89. Therefore, the delay to LCLKW imparted by delay circuit 370 is not in response to the DRC signals received by Hiraishi's data buffer because it is a predetermined fixed delay that results in the strobe generating circuit 374 generated a DQS that is about 1/4 clock cycle offset from the DQ write data output in data lines L1 and L2 so that the write data can be sampled by the memory chips 200. The delay circuit 370 is also not delaying the LCLKW "in response to at least one of the module control signals" because the only input to delay circuit 370 is LCLKW, which is not a module control signal. For example, Hiraishi consistently distinguishes between control signals and clock signals. EX1005, [0049], [0054], [0097]. The '608 patent also made clear that module control signals are distinct from module clock signals. *See e.g.*, EX1001, FIG. 3, (showing separate CK 312 and module ctrl 230; FIG. 6 (CK 610, DB Command Signals (MCS)); FIG. 7 (MCS, CK); FIG. 8, FIG. 9, FIGs. 10A-10D. The delay circuit 370 also does not participate

in Hiraishi's S-4 write leveling operation or operate based on the results from the leveling operation since it only applies a fixed offset.

90. A POSA would understand that the delay circuit 370 generates the fixed delay in response to the system clock signal CK, not a module control signal (alleged to be the DRC signal). I note that the claims of the '608 patent recite "module control signals" and separately recite a "module clock signal." Dr. Wedig does not suggest that the "module control signals" can be a clock signal. EX1003, ¶85 ("[A] Skilled Artisan would have understood that the claim term 'module control signals' includes signals that the module controller (also referred to as 'module control device' or 'module controller') derived from the 'memory command signals' and provided to buffer circuits to control their operations.")(citing EX1001, 4:27-30); *see also* EX1001, 3:47-50 (stating that the module control signals "are transmitted by the module control device to the buffer circuits via module control signal lines."); *see also id.*, 5:43-51. Instead, Dr. Wedig relies on Hiraishi's system clock signal CK as allegedly being the separately recited "module clock signal." EX1003, ¶¶140-141, 144-149.

91. Additionally, Dr. Wedig confirmed that the delay circuit 370 is delaying the local clock signal that it receives. EX2012, 64:24-66:5. Therefore, the delay imparted to LCLKW cannot be "to delay a signal through the data path" because LCLKW is not a data signal and the delay circuit 370 is not on a "data path,"

even under Dr. Wedig's theory of what constitutes a data path. For example, for a write operation in Hiraishi, the Dr., Wedig defines the "data path" in orange below. EX1003, ¶161 ("Fig. 5 (reproduced below annotated to show data paths, orange, for write operations).").

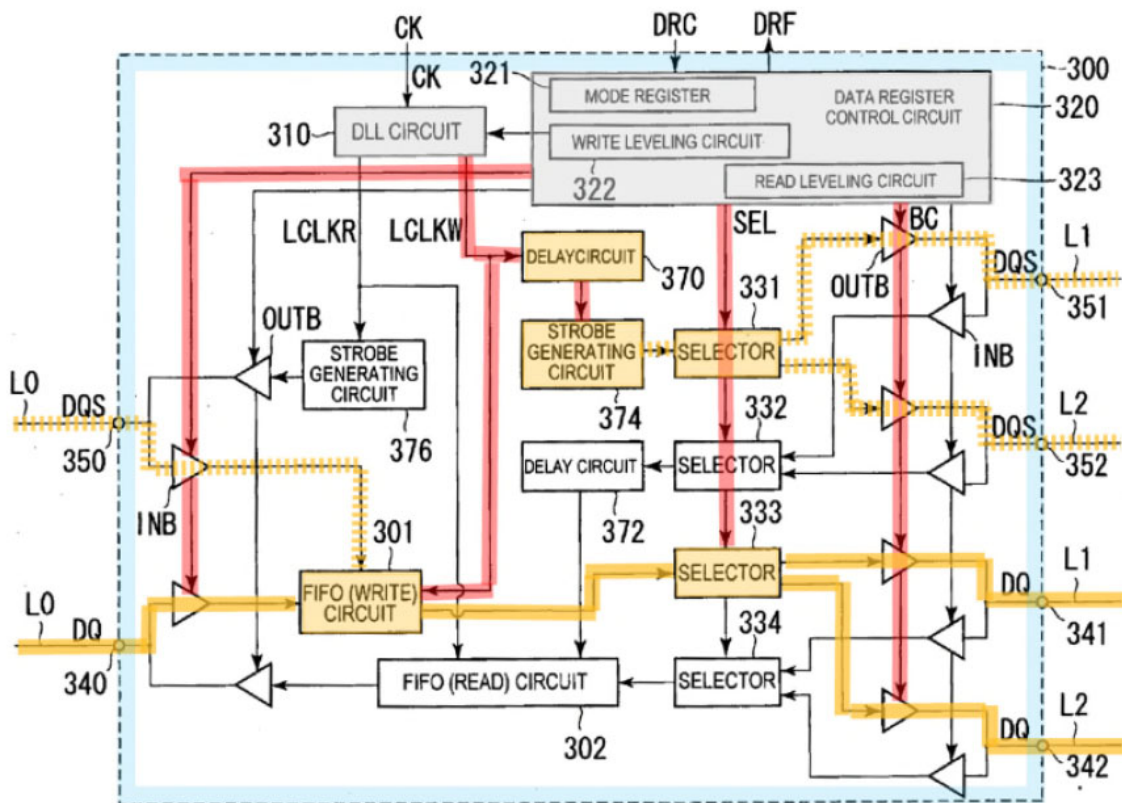


FIG. 5

While Dr. Wedig highlighted the delay circuit 370 itself in orange, neither the LCLKW being input to the delay circuit 370 nor the delayed DQS provided by delay circuit 370 are represented by Dr. Wedig as being part of the data path. EX2012, 41:2-5, 42:1-4 ("Q. How about the red -- I guess red lines? Are those part of the data path? A. No, they're not. They're not part of the data path.... Q. How about the

CLK signals LCLKR and LCLKW are those part of the data path through Hiraishi's data buffer? A. No. They're not.”). The local clock signal (LCLKW) is not part of the claimed “data path” because the local clock signal is not a data signal and does not correspond to a “data signal line in the respective set of data / strobe signal lines,” as recited in claim 1.

b) The Strobe Generating Circuit 374

92. I note that Hiraishi’s strobe generating circuit 374 is another component in the combination of Hiraishi components relied on by Dr. Wedig to satisfy the recited “delay circuit.” EX1003, ¶¶152, 161. However, Hiraishi’s strobe generating circuit 374 (1) is not in a data path and does not delay any signal, least of all a data signal, and (2) does not operate “in response to at least one of the module control signals.”

93. As an initial matter, Hiraishi explains that the “strobe generating circuit 374 **generates a data strobe signal DQS** to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.” EX1005, [0084]. Thus, circuit 374 generates a new signal, as opposed to delaying a signal. Delaying a signal would be understood to mean that a timing of an output signal is delayed with respect to a previous timing of the input. A newly-generated signal does not have any previous timing (since it did not exist), and therefore its timing cannot be delayed. Generating a new signal does not delay a

signal, regardless of when the new signal is generated. Moreover, phase adjustment of the DQS signal is via synchronization with a delayed LCLKW signal, and not by delaying the DQS signal that is generated.

94. In addition, the strobe generating circuit 374 is not in a data path because the strobe generating circuit 374 receives a delayed clock signal from circuit 370, and provides a strobe signal to selector 331, neither of which is a data signal or corresponds to a “data signal line in the respective set of data / strobe signal lines,” as recited in claim 1. In fact, the strobe generating circuit 374 generates a strobe signal that is used to sample a byte of data carried by 8 data signal lines (Hiraishi, [0053]), and cannot be part of a data path corresponding to each of the 8 data signal lines. Also, whatever delay the delay circuit 370 imposes on the generated strobe signal does not affect the timing of the data signal through any of the 8 data signal lines.

95. Hiraishi’s strobe generating circuit 374 generates the new DQS signal in response to an internal clock LCLKW (i.e., “in synchronization with an internal clock LCLKW”). Thus, the strobe generating circuit 374 does not operate in response to the DRC signals, which Dr. Wedig equates with the recited “module control signals,” because the strobe generating circuit 374 operates in response to a clock signal. As noted above, the claims of the ’608 patent claim “module control signals” and separately claim a “module clock signal,” and Dr. Wedig’s theories rely

on Hiraishi's system clock signal CK as allegedly being the recited "module **clock** signal," not a "module control signal." *See* EX1003, ¶¶85, 140-141, 144-149. In particular, Dr. Wedig does not content that a clock signal is a module control signal, nor could he as both Hiraishi and the '608 patent clearly distinguish the two.

c) The DLL Circuit 310

96. Dr. Wedig also relies on Hiraishi’s DLL 310 as allegedly being part of the recited “delay circuit.” However, Dr. Wedig purports to show the alleged “write data path” in orange in the annotated diagram below but omits the DLL circuit 310 from the “orange” path.

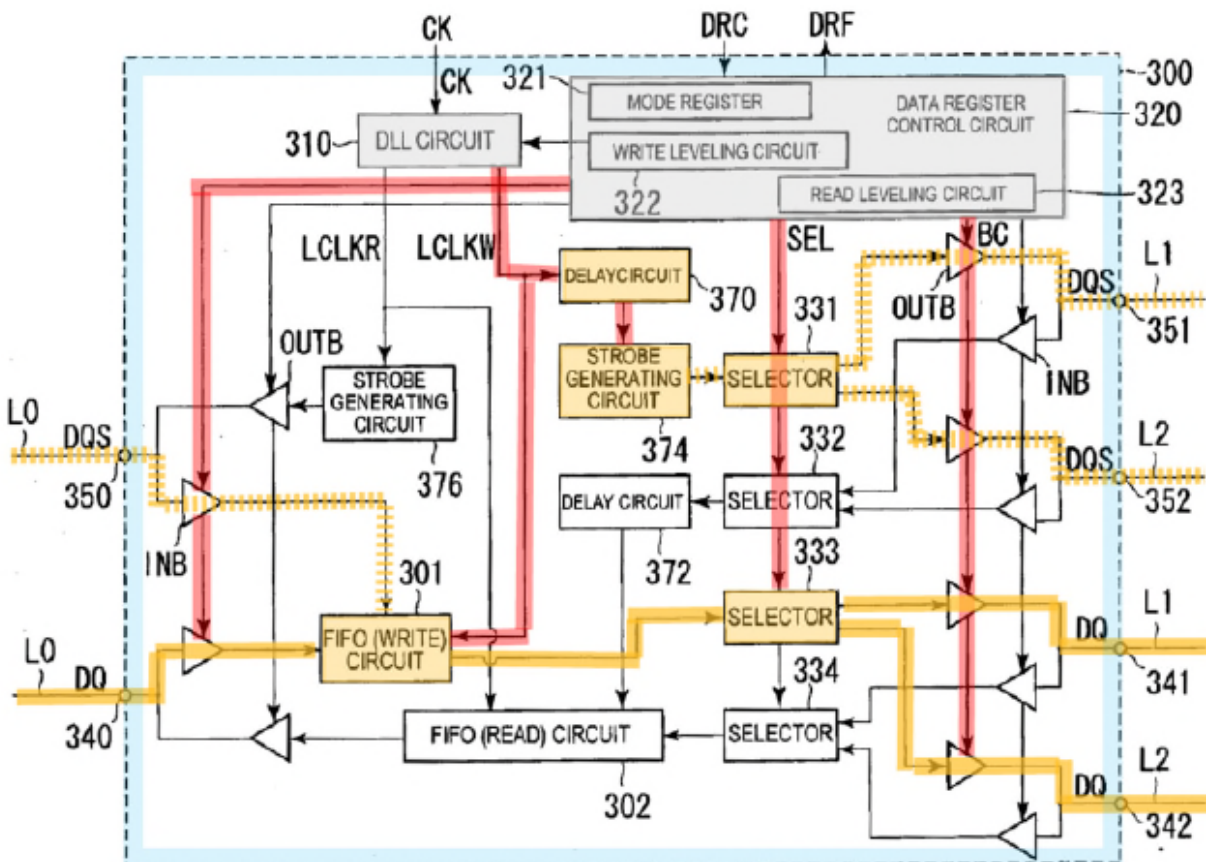


FIG.5

EX1003, ¶161.

97. I understand that Dr. Wedig also explicitly testified that the DLL is *not* in the data path. *See* EX2012, 42:24-43:1 (“Q. Is the DLL circuit 310 part of the data path through Hiraishi's data buffer? A. No, it's not.”).

98. In addition, the DLL 310 does not delay “a signal through the data path.” In Dr. Wedig’s annotated Fig. 5 from Hiraishi above, neither the CK nor LCLKW are identified in orange. I understand Dr. Wedig confirmed this. EX2012, 41:2-5, 42:1-4 (“Q. How about the red -- I guess red lines? Are those part of the data path? A. No, they're not. They're not part of the data path.... Q. How about the CLK signals LCLKR and LCLKW are those part of the data path through Hiraishi's data buffer? A. No. They're not.”).

99. Therefore, a POSA would not understand CK, the DLL 310, or LCLKW as being in a “data path” because none “correspond[] to each data signal line in the respective set of data / strobe signal lines,” as recited in claim 1. Also, the ’608 patent is clear that a clock signal is not part of the data path. *See e.g.*, EX1001, FIG. 3, FIG. 16, 17:23-47.

d) Write FIFO 301

100. Write FIFO 301 does not delay a signal through the data path “in response to at least one of the module control signals.” Specifically, in Hiraishi data is sampled in FIFO 301 using the incoming DQS signal from strobe signal line 350

and is clocked out based on the internal LCLKW clock signal, which is a derivative of the input clock signal CK(IN) received by the data register buffer. EX1005, FIG. 5; EX1005, [0084] (“FIFO (Write) circuit 301 buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350.”); [0087] (“An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310.”); [0135]. Sampling data does not delay the data, nor does Dr. Wedig contend that it does. Dr. Wedig also does not contend that a DQS signal or a clock signal is a module control signal. Both Hiraishi and the ’608 patent distinguishes between DQS signals, clock signals, and control signals. *See supra*, ¶¶89-90; EX1001, FIG. 3 (separate signal lines for DQS 324, CK 312, Module Ctrl 230), FIG. 6-9, 15-16; EX1005, FIG. 7 (separate signal lines for address/command, clocks, and DQS signals).

2. The Alleged “Delay Circuit” for Read Operations

101. Dr. Wedig relies on a similar combination of Hiraishi’s components for read operations. EX1003, ¶166 (“Therefore, Hiraishi discloses the claimed “delay circuit” for read operations, including the FIFO (read) circuit 302 delaying the data signal, delay circuit 372 delaying the input strobe signal, the strobe generating circuit 376 generating the strobe signal for the delayed data, and DLL circuit 310 generating the LCLKR signal for timing the output of the delayed data and strobe signals.”);

EX2012, 16:21-17:5 (“I believe that all of those different parts make up the delay circuit, so I guess yes, *it’s a combination of those*. I mean, *they all work together to implement the delay circuit*.”); 20:10-16(“Q. ... So is it your opinion that the delay circuit that Hiraishi discloses that reads on the claims of the 608 patent includes the FIFO read circuit 302, the delay 16 circuit 372, the strobe generating circuit 376 and then the DLL circuit 310? A. As part of it, yes. And then additionally it has the LCLKR signal.”)

a) The Delay Circuit 372

102. Hiraishi’s delay circuit 372 for read operations, like the delay circuit 370 for write operation, does not impart a delay “in response to at least one of the module control signals,” and (2) is not in a data path and does not delay a data signal.

103. The delay circuit 372 applies a fixed 90-degree delay to a strobe signal. EX1005, [0091] (“A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372.”); EX2012, 22:25-23:2 (“Q. Okay. And for the delay circuit 372, that delays an input strobe signal; right? A. Yes, it does.”). This fixed 90-degree delay relates to center-aligning the data strobe signal so that the buffer circuit can sample the incoming read data in the FIFO circuit. I note that Dr. Wedig seems to agree. EX1003, ¶ 223 (“A Skilled Artisan would have understood that sampling happens at delay circuit 372 to delay the DQS signal by about 90 degrees, and that sampling happens in accordance with the local clock of

the Data Register Buffer (for example, in order to detect the phase of the DQS signal).”). This means that any delay imparted to the incoming DQS by delay circuit 372 is not in response to the DRC signals (which Dr. Wedig alleges are “module control signals”) because the delay is a predetermined fixed delay that results in the DQS being offset by 90 degrees from the DQ read data. A POSA would also understand that the delay circuit 372 is not delaying the DQS “in response to at least one of the module control signals” because the only input to delay circuit 372 is the DQS strobe signal, which is not a control signal. The delay circuit 372 also does not participate in Hiraishi’s S-4 read leveling operation or operate based on the results from the leveling operation since it only applies a fixed offset.

104. I also note that the delay circuit 372 is in the strobe path, not the data path, and it delays a DQS signal, not a “signal through the data path.” As described above in Section IX, both the claim language and specification require the “data path” to correspond to data signal lines which carry data signals, not to strobe signal lines which carry strobe signals.

b) The Strobe Generating Circuit 376

105. Hiraishi’s strobe generating circuit 376 is another component in the combination of Hiraishi components relied on by Dr. Wedig to satisfy the recited “delay circuit.” For similar reasons as I explained above for the strobe generating circuit 374, Hiraishi’s strobe generating circuit 376 (1) is not in a data path and does

not delay any signal, least of all a data signal, and (2) does not operate “in response to at least one of the module control signals. For example, Hiraishi states that the “strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310.” EX1005, [0084].

c) The DLL Circuit 310

106. The DLL 310 generating the local read clock signal (LCLKR) does not satisfy Element 1[f] because neither the CK signal provided to the DLL 310 nor the LCLKR are signals on the “data path,” as I explained above for write operations.

d) Read FIFO 302

107. Read FIFO 302 does not delay a signal through the data path “in response to at least one of the module control signals.” Data is sampled in FIFO 302 using a delayed DQS signal from delay circuit 372 and is clocked out based on the internal LCLKR clock, which is a derivative of the input clock signal CK(IN) received by the data register buffer. EX1005, FIG. 5; EX1005, [0084] (“The FIFO (Read) circuit 302 buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352.”); [0087] (“An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310.”); [0091] (“[T]he data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as

an input trigger signal.”); [0130] (“Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.”). Sampling data does not delay the data, and Dr. Wedig does not contend that a DQS signal or a clock signal is a module control signal. Both Hiraishi and the ’608 patent distinguishes between DQS signals, clock signals, and control signals. *See supra*, ¶¶89-90; EX1001, FIG. 3 (separate signal lines for DQS 324, CK 312, Module Ctrl 230), FIG. 6-9, 15-16; EX1005, FIG. 7 (separate signal lines for address/command, clocks, and DQS signals).

D. Hiraishi’s WL Latency Re-timing Is Not Based on Results from Hiraishi’s Write Leveling and Does Not Satisfy Element 1[f]

108. For Ground 2, Dr. Wedig proposes that “Hiraishi’s data register buffer 300 determines delays through the data path for read and write operations by respective read and write leveling operations during initialization in response to control signals from the command/address/control register 400, and applies those delays on the data/strobe signals for read and write operations during normal operation in response to read and write commands received from the command/address/control register 400.” EX1003, ¶ 155. Dr. Wedig proposes that delays determined during Hiraishi’s S-4 write leveling are used to re-time both data and strobe signals during subsequent write operations. EX1003, ¶¶ 158-161.

109. Hiraishi's S-4 write leveling is unrelated to its re-timing operations, and the results of S-4 write leveling are used to align the output DQS signal to the system clock signal CK, not to re-time the DQ/DQS signals output by the data buffer to the memory devices. As I explain below, Hiraishi avoids having to determine signal delays to account for flight time differences from one memory device to another by generating an entirely new DQS signal based on a predetermined latency value (i.e., WL=5 and CL=6) for write operations and read operations, respectively. See below, Sections IX.D.2, IX.E.2.

1. Hiraishi's S-4 Write Leveling Operations Adjust the Timing of DQS to Align to the System Clock CK

110. Hiraishi's S4 write leveling does not relate to delaying a signal in a data path. Hiraishi's S-4 write leveling accounts for mismatches between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. EX1005, [0142]-[0146]; EX2012, 60:7-12 ("So what happens in S4 write leveling - - we are now looking at the relationship between the CLK and the DQS signal that appears at the input to the memory device. We want that to now be in synch."). Hiraishi describes the S4 write leveling process in connection with FIGs. 14A-14B below.

FIG.14A

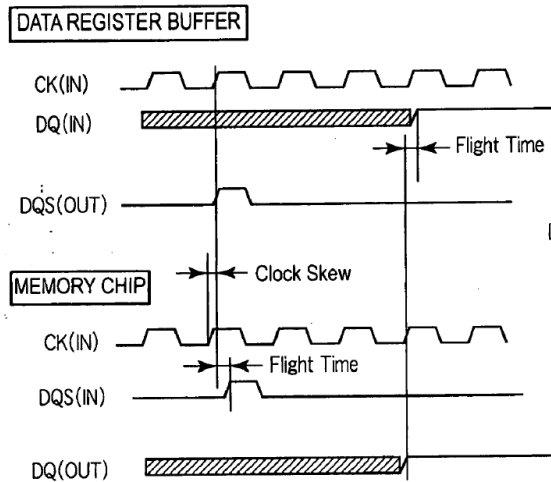
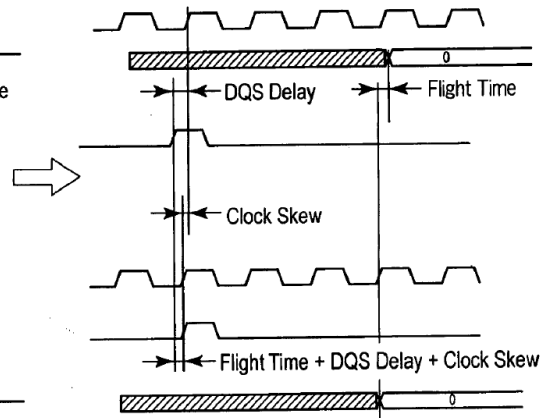


FIG.14B



111. As Hiraishi discloses, “[i]n the write leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 14A, the data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK.” EX1005, [0143]. Hiraishi explains that “[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” *Id.*, [0143]. To compensate, “[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift.” *Id.*, [0145]. Based on Hiraishi’s S4 write leveling, “the data register buffer 300 can find a timing to output the data strobe signal DQS based on the input clock signal CK” and “the phases of the clock

signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.” *Id.*, [0146].

112. Dr. Wedig alleges that the “resulting delays” of S-4 write leveling “are stored in the data register buffer 300 and applied to delay both the data and data strobe signals during subsequent write operations such that both write data and strobe signals arrive at the memory with a predetermined latency WL=5.” EX1003, ¶160. However, Hiraishi states that the “result of the write leveling operation is stored in the data register control circuit 320 in the data register buffer 300,” and that “[u]pon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.” EX1005, [0146]. A POSA would understand this passage to mean that the result of Hiraishi’s write leveling which is stored is not used to delay data and data strobe signals during subsequent write operations, but instead is used to delay or advance DQS signal to match the module-level clock signal CK with DQ(IN) and DQ(OUT) unchanged, as shown in FIGs. 14A-14B below.

FIG.14A

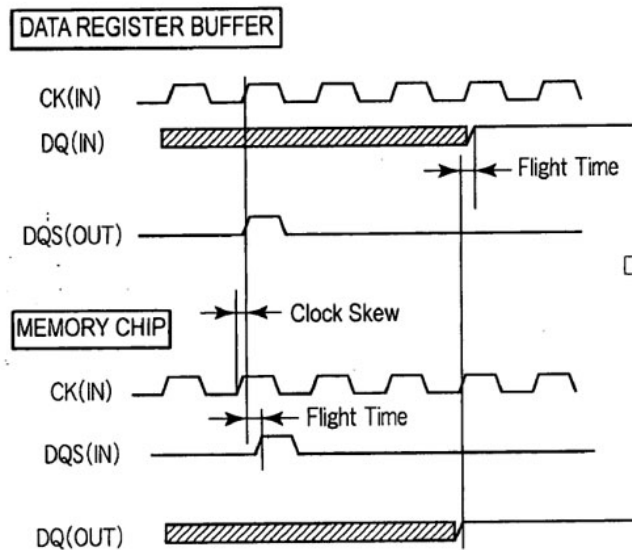
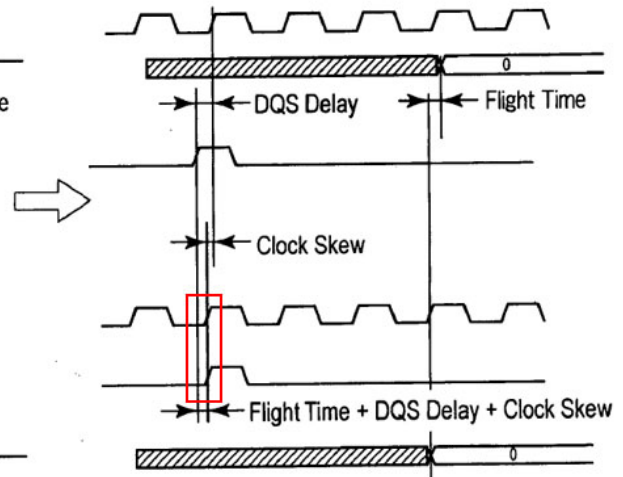


FIG.14B



EX1005, [0027] (“FIGS. 14A and 14B are timing charts for explaining the write **leveling** operation between the data register buffer 300 and the memory chip 200, where FIG. 14A is a timing chart at the time of starting the leveling and FIG. 14B is a timing chart at the time of ending the leveling.”).

113. A POSA would understand that the results of Hiraishi’s S4 write leveling are not used for re-timing DQ/DQS from FIG. 12, which Hiraishi indicates “is a timing chart for explaining the **write operation** of the memory module 100 according to the present embodiment.” In other words, FIG. 12 is describing a normal write operation which would occur only after Hiraishi’s leveling functions because those leveling functions are performed during the initialization stage at the time of activation, i.e., before read and write operations begin. *See* EX1005, [0138] (“FIG. 13 is a flowchart for explaining the initializing operation of the memory

module 100 at the time of activation.”). I understand that Dr. Wedig agreed that Hiraishi’s leveling functions are only performed during the initialization. EX2012, 57:3-10.

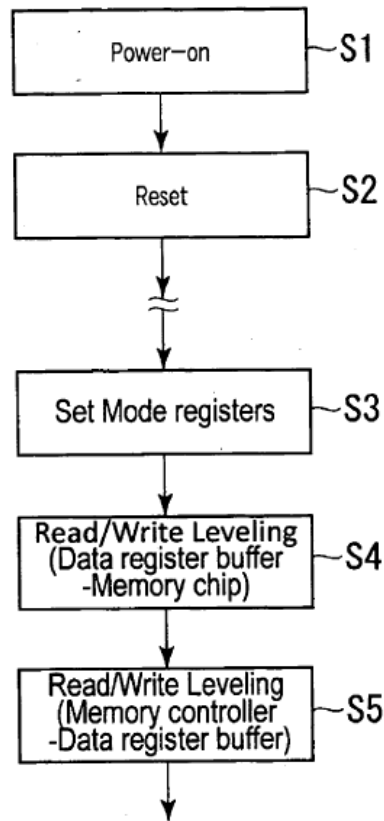


FIG.13

114. Because FIG. 12 describes a normal write operation, it reflects the state of signal timing after Hiraishi’s S-4 write leveling has already been completed. FIG. 12 shows that the results of write leveling are not used to re-time DQ/DQS based on the fact that the CK(IN) and DQS(IN) to the memory chip are aligned (highlighted in red), which is the goal of Hiraishi’s S4 write leveling, while the DQ data re-timing

from a write latency of 4 clock cycles (WL=4) to a write latency of 5 clock cycles (WL=5) is indicated as a distinct occurrence (highlighted in green).

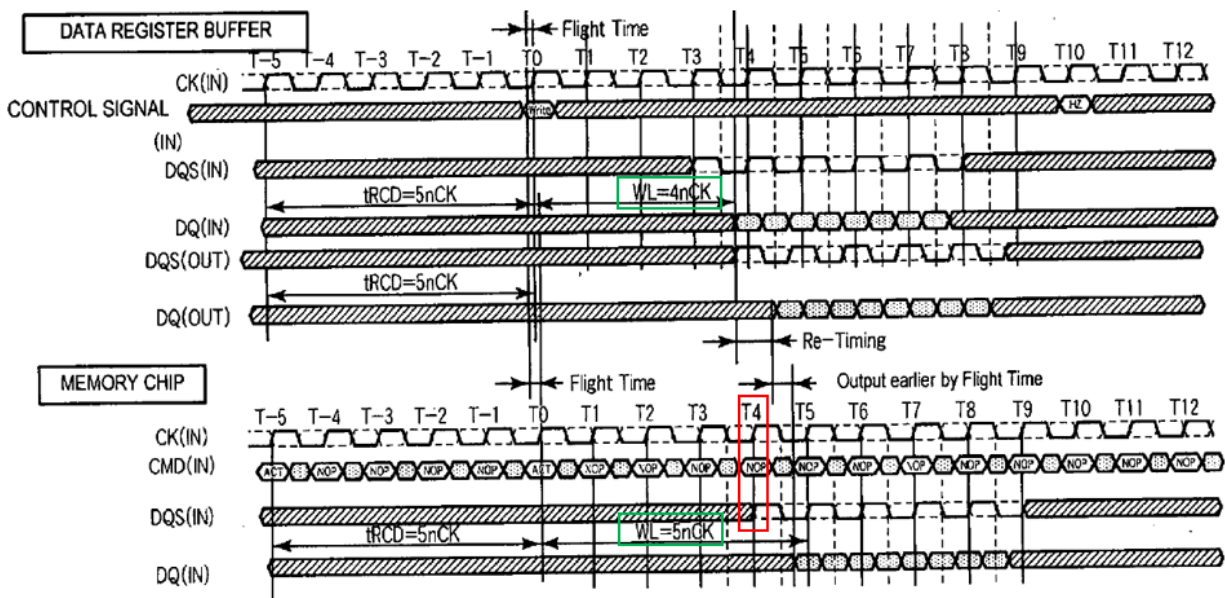


FIG.12

115. Therefore, I do not agree that Hiraishi's S4 write leveling relates to delaying data in a data path, or that the results of S4 write leveling are used to do carry out Hiraishi's WL re-timing.

2. Hiraishi's WL Re-timing Addresses Flight Delays for Write Operations By Adding a Clock Cycle of Latency

116. Hiraishi does not disclose much about its re-timing operation, but does explain that, for the write operation of FIG. 12, "the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data." EX1005, [0133]. See FIG. 12 below.

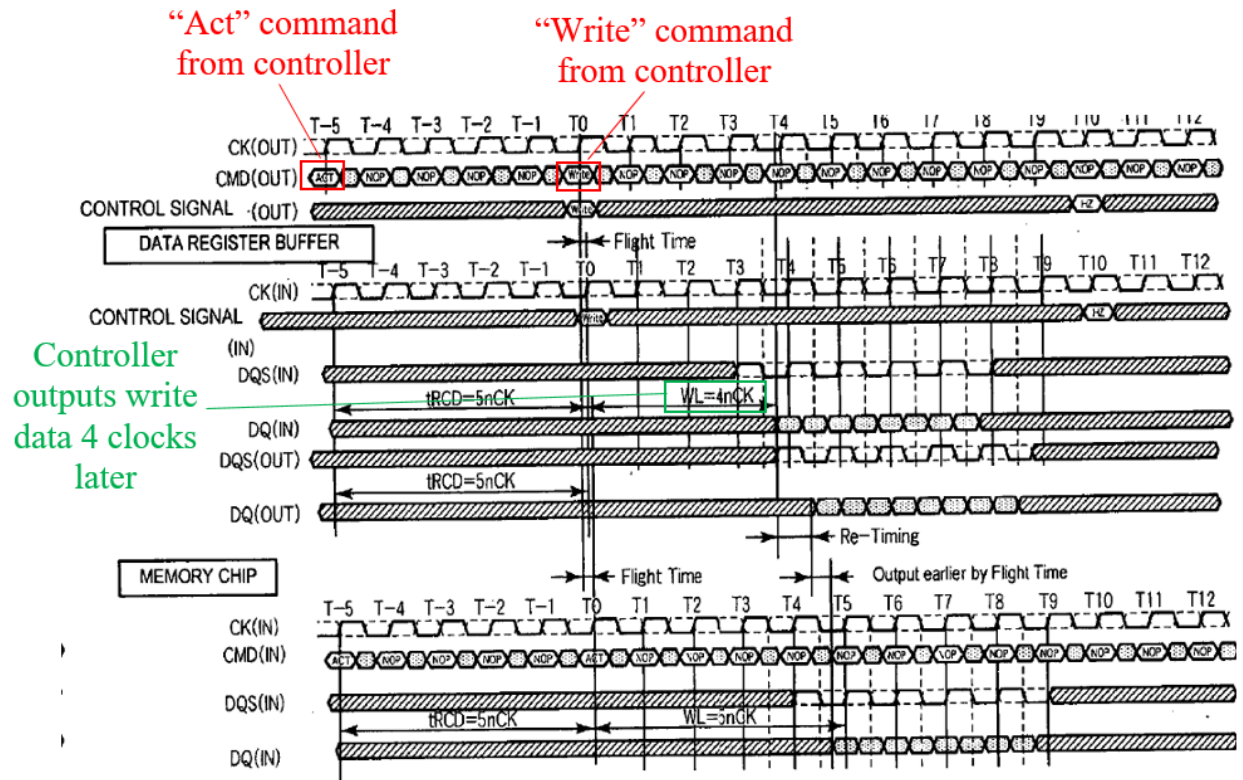


FIG.12

117. Thereafter, the "data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 [and] then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS." EX1005, [0135]. See below. In contrast, write leveling changes the output DQS's timing "*by displacing the internal clock LCLKW based on the direction of the phase shift.*" EX1005, [0145]. That is another indication that re-timing and S-4 leveling are unrelated.

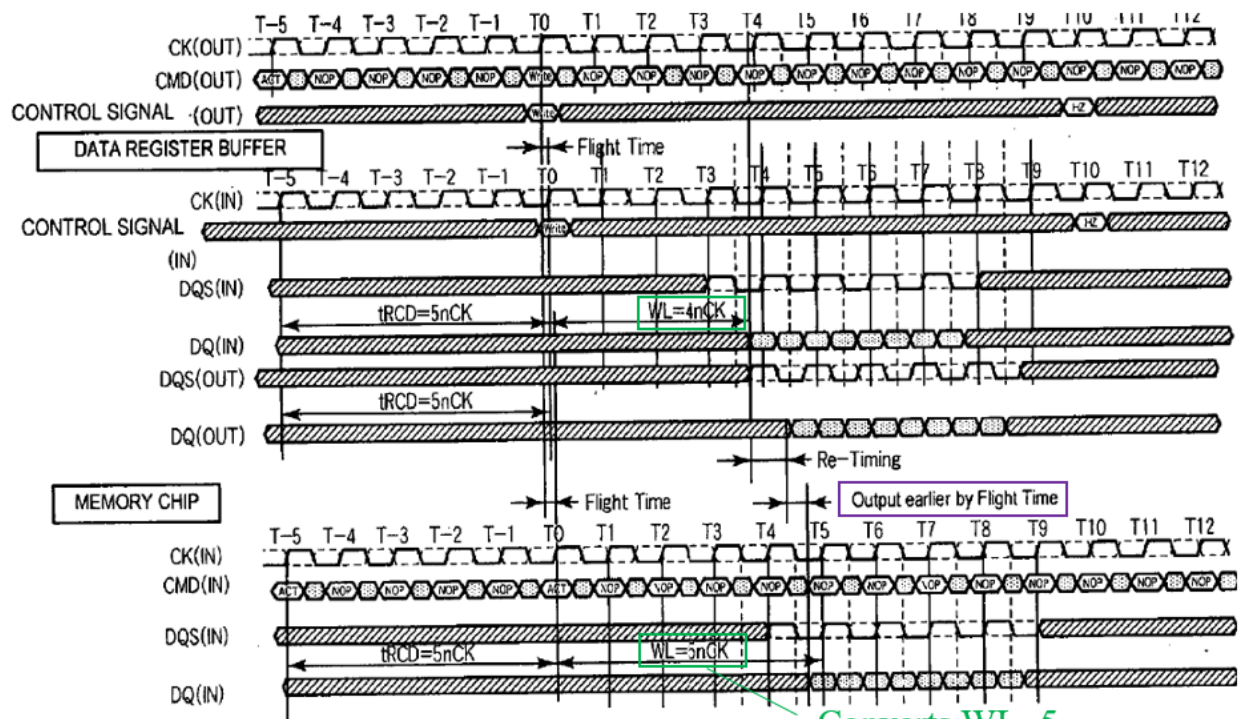


FIG.12

118. I also note that in the same paragraph describing the conversion of WL into WL=5, Hiraishi states that “[t]he data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees).” EX1005, [0135]. This passage refers to the fact that the incoming DQS signal (on strobe signal lines 350 in IFG. 5) is received already phase shifted by 1/4 clock cycle, which is consistent with the JEDEC requirements that data be provided to memory devices center-aligned) so that the incoming DQS signal can be used to sample the incoming write data in the write FIFO 301.

119. Hiraishi explains that “there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200.” EX1005, [0136] (above in purple). It is because of that “predetermined time difference (Flight Time)” that “the data register buffer 300 outputs the write data DQ earlier by an amount equivalent to the Flight Time.” *Id.* The purposes of Hiraishi’s re-timing operation is to account for these time differences by converting the internal latency to the next highest clock cycle, here from WL=4 to WL=5. In other words, Hiraishi resets internal latency to the next highest clock cycle which avoid the tedious process of having the buffer circuit compute individual delays. As a result, Hiraishi’s re-timing operation does not “delay a signal through the data path by an amount determined by the command processing circuit,” as recited in Element [1f].

120. Hiraishi does not envision delays exceeding one clock cycle, as is evident from at least FIG. 15, a partial reproduction is below.

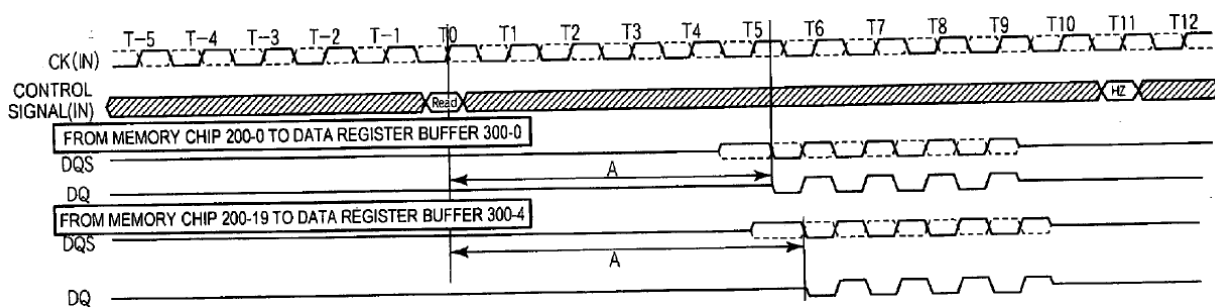


FIG.15

121. Hiraishi indicates that “[t]he time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.” EX1005, [0151]. In describing FIG. 15, Hiraishi then states that “two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4).” *Id.* I’ve annotated Hiraishi’s FIG. 1 to show the relative location of these “two cases” below.

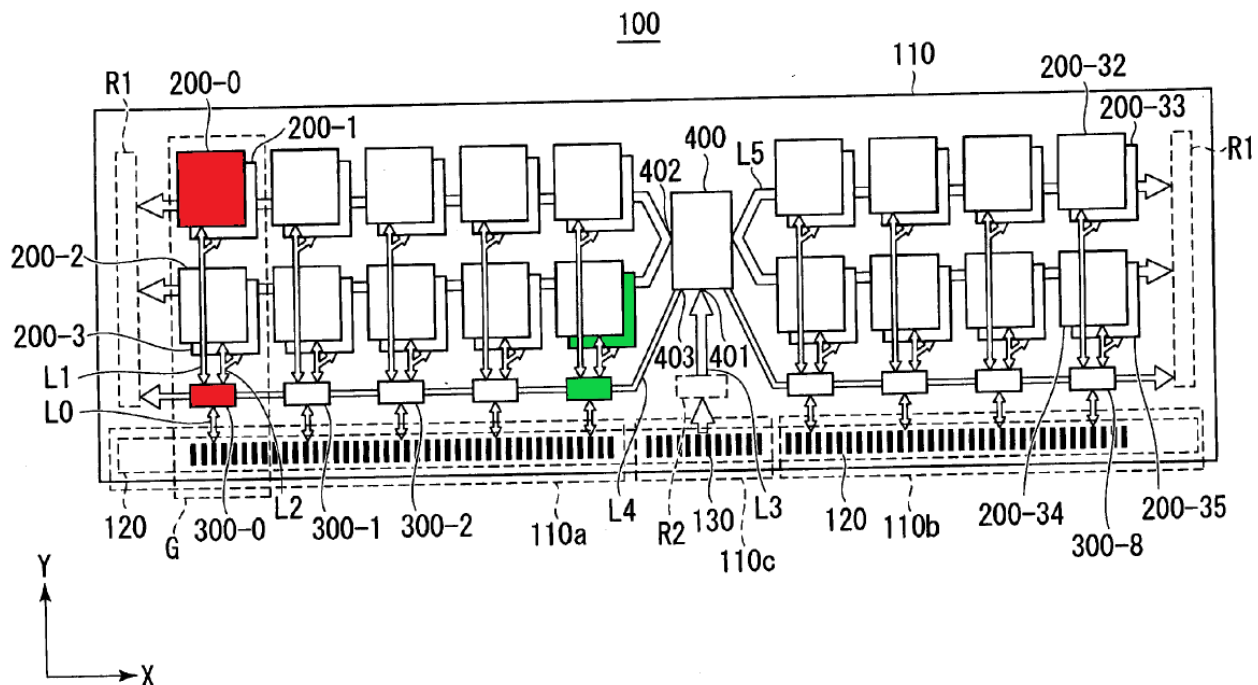


FIG.1

122. As shown above, memory chip 200-0 and data register buffer 300-0, which are labeled in the figure, are highlighted in **red**. Conversely, memory chip 200-19 and the data register buffer 300-4 are highlighted in **green**. While memory chip 200-19 is not labeled, Hiraishi's numbering convention is clear from the fact that it starts at 200-0 and 200-1 on the upper left side, and ends with 200-32, 200-33, 200-34, and 200-35 for the four memory chips on the far-right side. Similarly, while data register buffer 300-4 is not labeled, Hiraishi's numbering convention is clear from the fact that data buffers begin with 300-0 on the far-left side, followed by 300-1, 300-2, ... and ending with 300-8 on the far right side.

123. Even though Hiraishi describes these relative distances as being "short" and "long," the difference in their respective time A in FIG. 15 is only about 1/2 clock cycle.

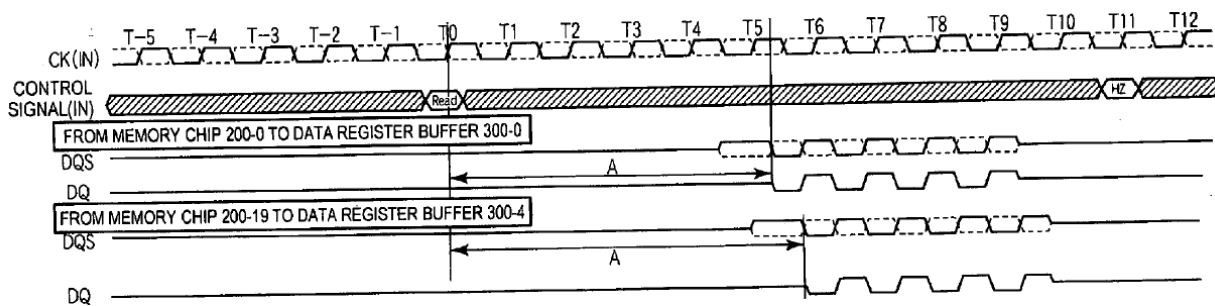
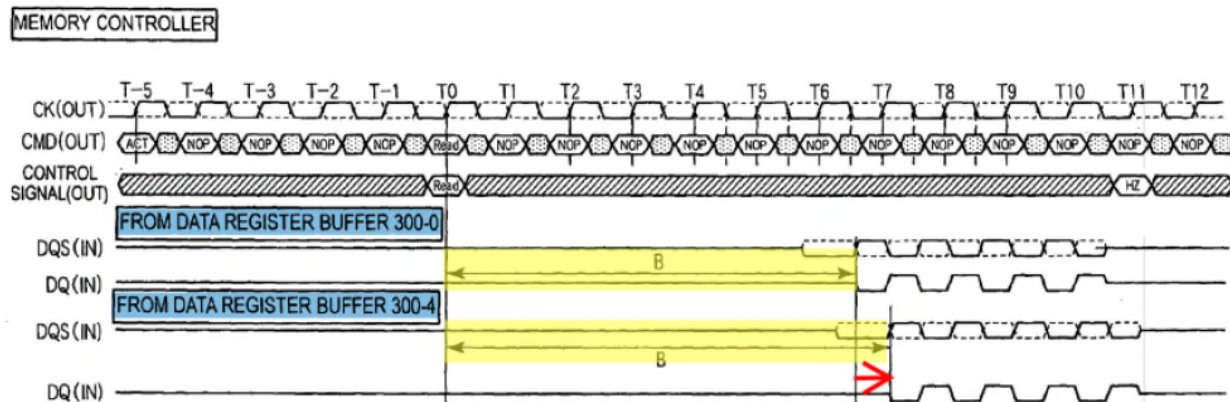


FIG.15

124. Even if the two examples given in Hiraishi do not represent the absolute extreme possible cases, there is no reason to believe that in any circumstance there would be more than double the delay difference between what Hiraishi describes as

“short” and “long” cases. I note that Dr. Wedig agrees that Hiraishi “only shows fly-by delays less than one clock cycle.” EX1003, ¶256 (referring to annotated version of FIG. 17 below):



EX1003, ¶249. In any event, even if delays greater than 1 CK were encountered by Hiraishi, a POSA would understand that Hiraishi would apply the same re-timing technique to increase latency by a fixed 2 clock cycles, or whatever number of clock cycles was required, to account for longer flight delays. This technique would also not require determining an amount of delay for the signal, per the claims of the '608 patent.

125. Because Hiraishi assumes that the differences in fly-by delays is always less than one clock cycle, Hiraishi simply sets the buffer's latency to the next higher clock cycle to adequately address all expected flight delays. Dr. Wedig also confirmed that in each of Hiraishi's re-timing examples, the latency is set to the next highest clock cycle. See EX2012, 72:19-21 (“So you're correct that in these

examples, it changes the write latency and the read latency to add one more CLK cycle.”).

126. Because of this resetting of the latency parameter, Hiraishi’s buffer circuit does not determine the amount of delay to apply to correct for fly-by differences. Moreover, determination of individual delays is unnecessary because, as Dr. Wedig confirmed, all the memory chips, the data buffer and the data register buffer receive the same “system-level CLK” and therefore have a common understanding of timing. EX2012, 74:9-24. As a result, regardless of individual flight time or which memory chip is at issue, the data is all output at the same time by increasing the latency to the next clock cycle. *See id.* 74:25-75:14 .

127. Moreover, because latency delays are set in full clock cycles, it would make no sense to determine individual delays and add corresponding fractional clock cycles to WL or RL.

128. In the context of FIG. 15, I understand that Dr. Wedig explained that for the data buffer to output at the same time T, the buffer is “going to hold the data, if it came in early, and then it's going to output it at T6. And if it comes into the data buffer later, then it's going to hold it until it gets to T6 in this example.” EX2012, 76:13-77:7. I agree. I also note that this involves no computation of delays by the buffer’s command processing circuit (alleged to be the data register control circuit 320 and/or logic in DLL circuit 310). Instead, the operation is based on detecting

when the latency parameter is satisfied, and outputting data at that specific point in time. Dr. Wedig testimony is in accord. EX2012, 78:10-24(“[T]he DLL circuit gives you the timing for the chip. So yeah, so it’s going to generate the CLK. So – so after it’s held it the appropriate amount of time, it will CLK it out at T6. And yeah, the DLL circuit is in charge of making that CLK.”). This occurs at the same time T across all of Hiraishi’s buffers, as Dr. Wedig confirmed. *See id.* 78:25-79:8(“Okay. And then all of the other eight data buffers, if we’re -- if we’re in that type of a module, are also receiving their CLK signals and their respective DLL circuits saying okay for this operation we’re at T6: Okay, for this operation we are at T6. A. Uh-huh. Q. – [And] CLK out whatever we’ve got in the FIFO at that point? A. ... Again for this – for this example, right, it’s going to hold it for whatever length of time it needs so that they all -- you know, to that -- you’re going to hold it until the last one arrives, and then you send it out.”).

129. I understand that Dr. Wedig may have later given certain contradictory testimony based on the notion that each data buffer has its own time T, but it is unclear how that would operate, and in any event is contradicted by Hiraishi’s own disclosure. For example, that the same time T applies for all buffer circuits is reflected in Hiraishi’s FIG. 15. See below showing same system clock CK timing for buffer 300-0 and 300-4.

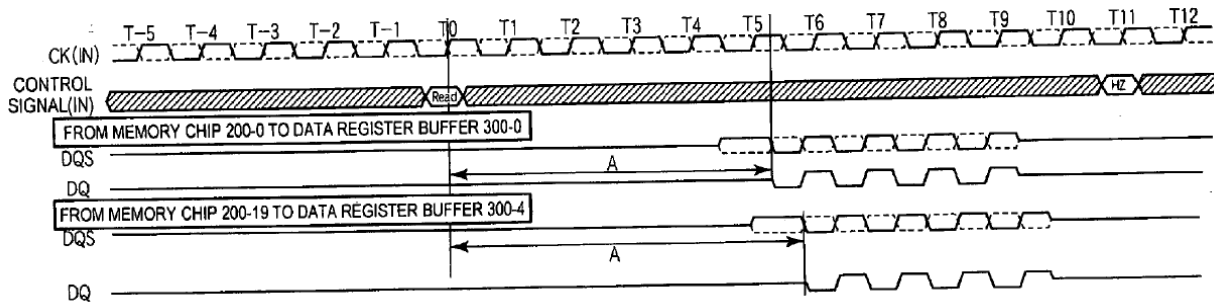


FIG.15

130. For example, buffer 300-0 and 300-4 are shown in FIG. 15 above as operating according to the same system clock CK (IN), which also the case with FIG. 17. Dr. Wedig confirmed that, in reference to FIG. 15 above, the same system clock CK is used for different memory chips and different data buffers. EX2012, 144:5-21.

131. Hiraishi's WL re-timing addresses flight delays during write operations by increasing latency by one clock cycle, and therefore does not "delay a signal through the data path by an amount determined by the command processing circuit," as recited in Element [1f].

E. Hiraishi's CL Re-Timing Is Not Based on the Results of S-4 Read Leveling and Does Not Satisfy Element 1[f]

132. I note that Dr. Wedig separately takes the position that the delays determined during Hiraishi's S-4 read leveling are used to re-time DQ/DQS signals during subsequent read operations. I do not agree for the reasons below.

1. Hiraishi's S4 Read Leveling Operations Adjust the Activation Timing of Hiraishi's Input Buffers

133. Hiraishi's S4 read leveling determines when its input buffers INB are activated to receive read data signals and strobe signals coming from memory chips 200 over L1 and L2 via terminals 341, 342, 351, and 352. EX1005, [0140], [0147-151], Fig. 15; EX2016 (506 IPR Dep. Tr.), 59:4-18 (Dr. Wedig confirming that Hiraishi's read leveling adjusts the activation timing of the input buffers). The data register control circuit 320 (which includes read leveling circuit 323) turns on input buffers for signals DQS and DQ before the expected arrival of the data and strobe signals so they can pass through to the selectors and be captured by the FIFO (Read) circuit 302 according to the timing information provided by the corresponding strobe signal. EX1005, FIG. 5, [0088], [0151]. Adjustment to the timing of when the input buffers INB are turned is carried out to ensure they are active when data. EX1005, [0151] ("The time is ... used in an adjustment of an activation timing of the input buffer circuit INB and the like.").

134. I note that Dr. Wedig also mentions Hiraishi's output buffers (OUTB), but the only disclosure in Hiraishi relating to the output buffers (OUTB) is that they are controlled by the data register control circuit 320 for "an adjustment of output impedance and an on/off control of an ODT operation." EX1005, [0088].

135. Because of flight time delays, the read data might arrive at one data register buffer later than the corresponding data would arrive at a second data register

buffer on the same module, as Hiraishi shows in FIG. 15, which is reproduced and annotated below.

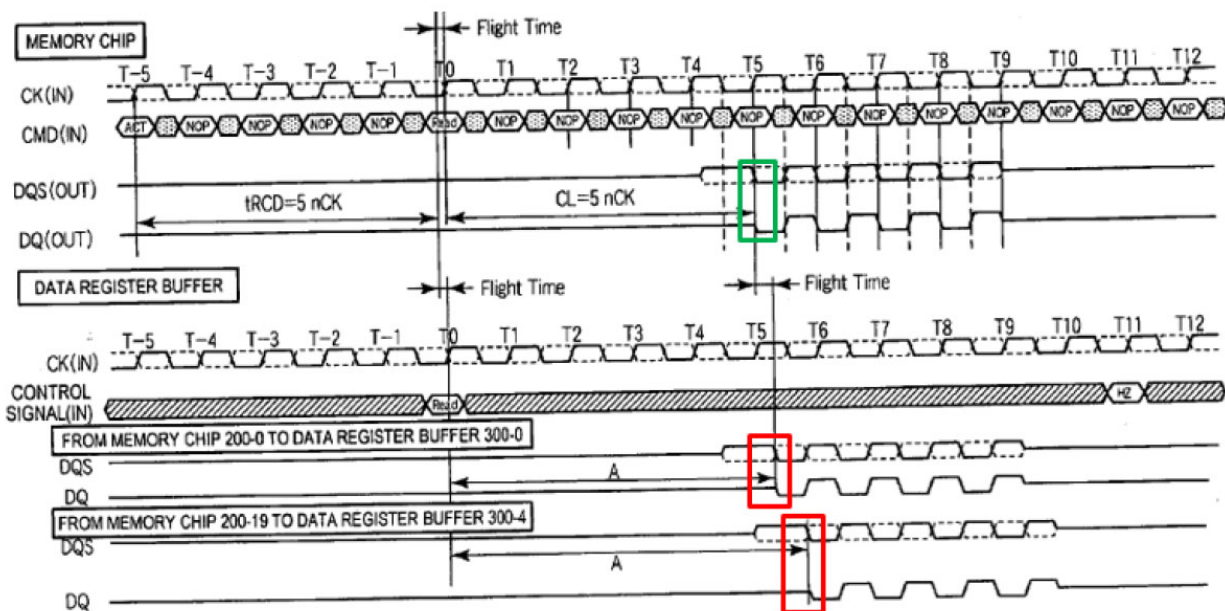


FIG.15

EX1005, FIG. 15.

136. While read DQ/DQS signals are output from the memory chip at T5 (see green box above), the read DQ/DQS signals arrive at the data buffer at T5 plus some “Flight Time” which varies from memory chip to memory chip (see red box above). To account for this variation, Hiraishi performs S-4 read leveling to ensure that the input buffers INB for each given data buffer are active when data arrives. In addition, Hiraishi’s increases the read latency (CL) by one clock cycle for all data buffers in an analogous fashion to the write latency (WL) described above. See Sections IX.D.2, IX.E.2. These operations are distinct. However, and the result of

any adjustment to Hiraishi's INB activation timing is not part of Hiraishi's subsequent CL re-timing. This is because the activation timing of Hiraishi's INB buffers does not impact or result in any delay to the DQ signals. In any event, the DQ data cannot be delayed by any specific or replicable amount by the FIFO because the data has not yet been sample/registered by the FIFO circuit.

137. In addition, I note that Dr. Wedig already relies on Hiraishi's INB buffers to satisfy the separate claim feature of "at least one tristate buffer controlled by the command processing circuit" of claim 1. EX1003, ¶¶152, 154 ("A Skilled Artisan would have understood that these OUTB and INB buffers are tri-state buffers for several reasons."). Also, Dr. Wedig confirmed that Hiraishi's INB/OUTB buffers are not alleged to satisfy the "delay circuit" of Element 1[f]. EX2012, 31:23-25 ("Q. And so those tristate buffers, those OUTB and INB buffers, are those part of the delay circuit as well? A. No, they're not.").

2. Hiraishi's CL Re-timing Addresses Flight Delays for Read Operations By Adding a Clock Cycle of Latency

138. I note that Dr. Wedig cites to Hiraishi's FIG. 11 in support his opinion that "[r]ead leveling determines delays ("Re-Timing") for the read data (DQ) and strobe (DQS) signals received at different times A such that the delayed data and strobe signals are output CL=6 clock cycles after the read command is received in the data buffer." EX1003, ¶162. Dr. Wedig further states that "[a] Skilled Artisan would have understood from this disclosure of Hiraishi that the DQ/DQS read delays

are determined as the difference between the time of data output at CL=6 and time A of data arrival.” EX1003, ¶162. I do not agree that Hiraishi’s read leveling determines delays for the DQ/DQS re-timing operation for the reasons described above in Section IX.E.1.

139. I also do not agree that DQ/DQS read delays are determined as the difference between the time of data output at CL=6 and time A of data arrival because Hiraishi has no need to do so, and expressly describes a different operation. Specifically, like the write latency re-timing described above, Hiraishi sets buffer latency for read operations to the next highest clock cycle, regardless of which memory device is being read from. For example, Hiraishi illustrates how the memory device’s read latency CL=5 is converted by the data buffer into a read latency CL=6 by outputting the data exactly one clock cycle later. See below.

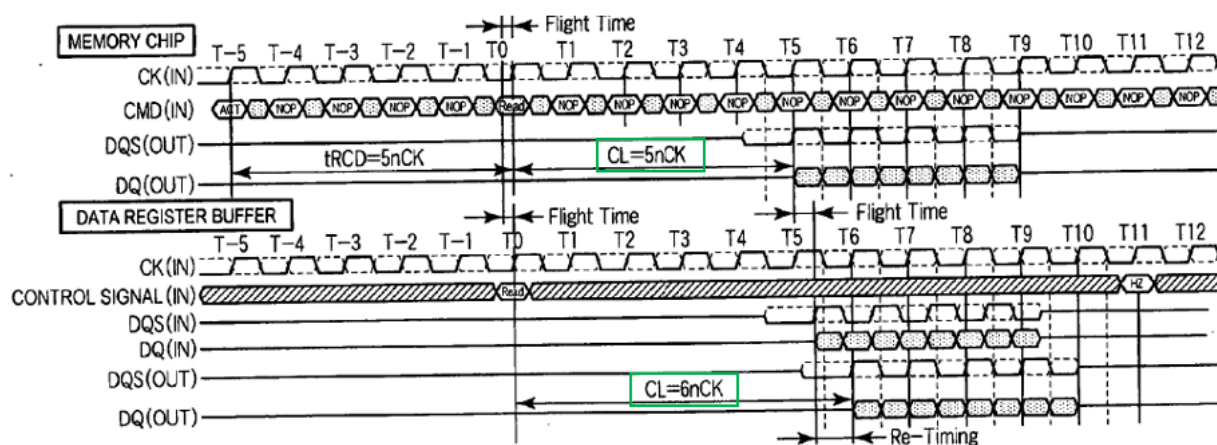


FIG. 11

EX1005, FIG. 11 (partially reproduced and annotated).

140. Hiraishi explains that “there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.” EX1005, [0129]. This predetermined time different (or flight time) varies as between different memory devices as shown by Time A below where the DQ/DQS received by the data buffer from memory chip 200-0 is different than Time A for the DQ/DQS received from memory chip 200-19).

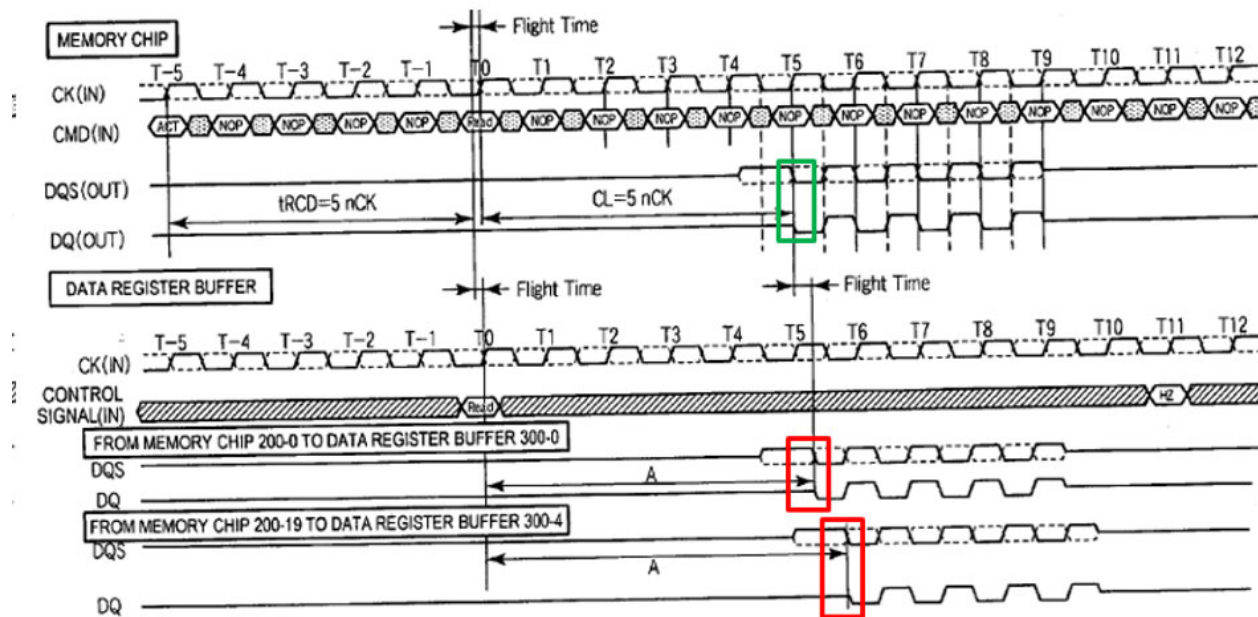


FIG.15

EX1003, FIG. 15. Instead of trying to account for these timing differences by determining specific signal delays for each memory device, Hiraishi describes a simple re-timing operation which sets all buffer latencies to the next highest clock

cycle because CL's are set in whole cycles and it would not make sense to determine individual delays and add fractional clock cycles to CL. Hiraishi explains this:

[T]he data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005, [0130].

141. As shown in FIG. 11, this latency “re-timing” causes both the read data (DQ(OUT)) and the corresponding strobe signal (DQS(OUT)) to begin outputting from the data register buffer 300 exactly 6 clock cycles after T0. A POSA would understand that this synchronizes the transmission of read data, regardless of the flight time for the individual memory devices which are providing the read data.

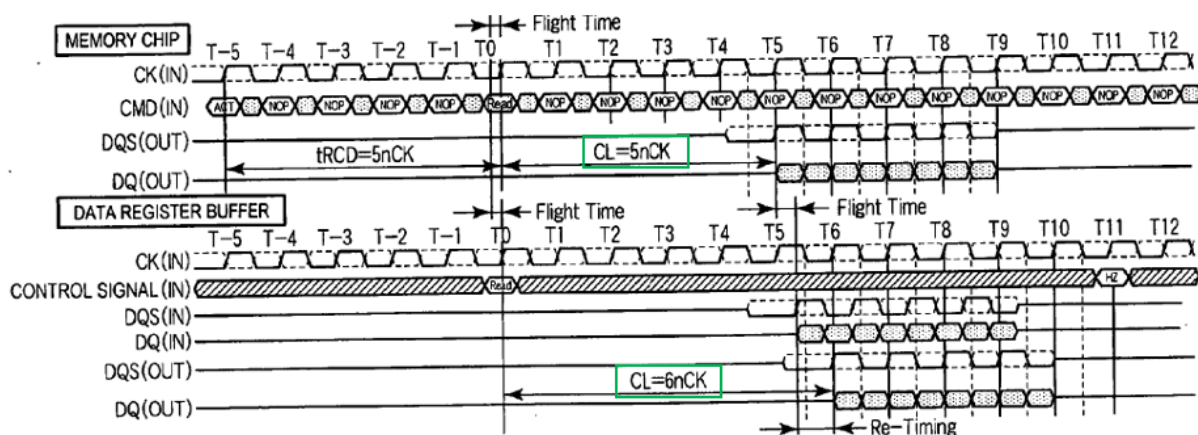


FIG.11

EX1005, FIG. 11 (partially reproduced and annotated to show data buffer converting CL=5 to CL=6).

142. Hiraishi's CL re-timing addresses flight delays during read operations by increasing latency by one clock cycle, and therefore does not "delay a signal through the data path by an amount determined by the command processing circuit," as recited in Element [1f].

X. DR. WEDIG AS NOT ESTABLISHED THAT GROUND 2 INCLUDES A DELAY CIRCUIT IN THE DATA PATH

143. I note that Dr. Wedig proposes a combination of Hiraishi and Tokuhiko in which a delay element DR-1 found in Tokuhiko's memory controller is added into Hiraishi's data buffer, as Dr. Wedig illustrates in the annotated version of Hiraishi's FIG. 5 below.

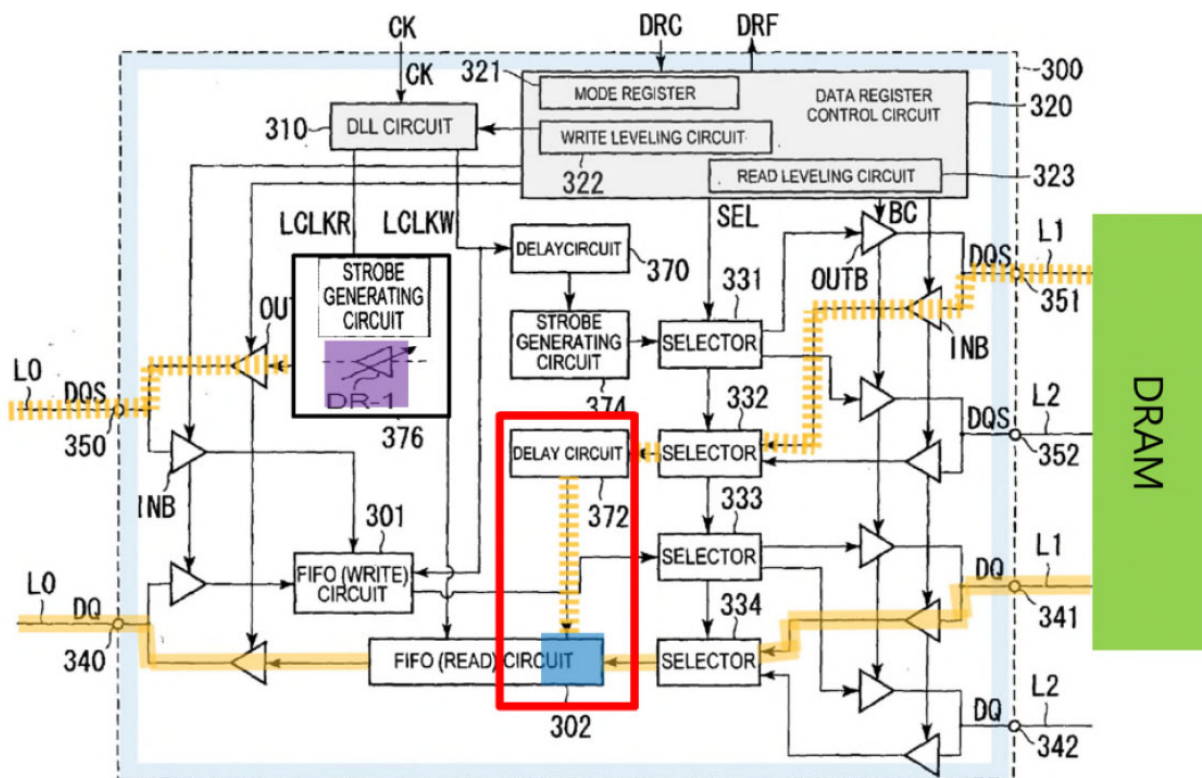


FIG.5

EX1003, ¶ 262.

144. As an initial matter, Tokuhiro's delay circuits do not delay any clock signals. Therefore, a POSITA would not have applied Tokuhiro's teaching to delay a clock signal absent some additional modification to Tokuhiro's teaching and reasoning to do so, which Dr. Wedig does not provide. In addition, Dr. Wedig has not established, however, that the above proposed combination includes a delay circuit in the data path, as required by the claims. In particular, the strobe generating circuit 376 is not in the DQ data path, nor is the DR-1 delay element which has been added to Hiraishi's buffer circuit. See *Supra*, Section IX.A. Instead, as I described above when discussing Hiraishi's strobe generating circuits, and as shown in FIG.

5, the strobe generating circuit 376 receives only the local clock LCLKR, which I understand Dr. Wedig has said is not in the data path EX2012, 41:2-5, 42:1-4. I agree that the local clock LCLKR is not in the data path. Moreover, the only other signal into or out of the strobe generating circuit 376 is the strobe signal DQS on strobe signal line 350. For example, Hiraishi states that the “strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310.” EX1005, [0084]. In the context of the ’608 patent a DQS signal line is not a “data signal line in the respective set of data / strobe signal lines,” as recited in claim 1. *See supra*, Section IX.A.

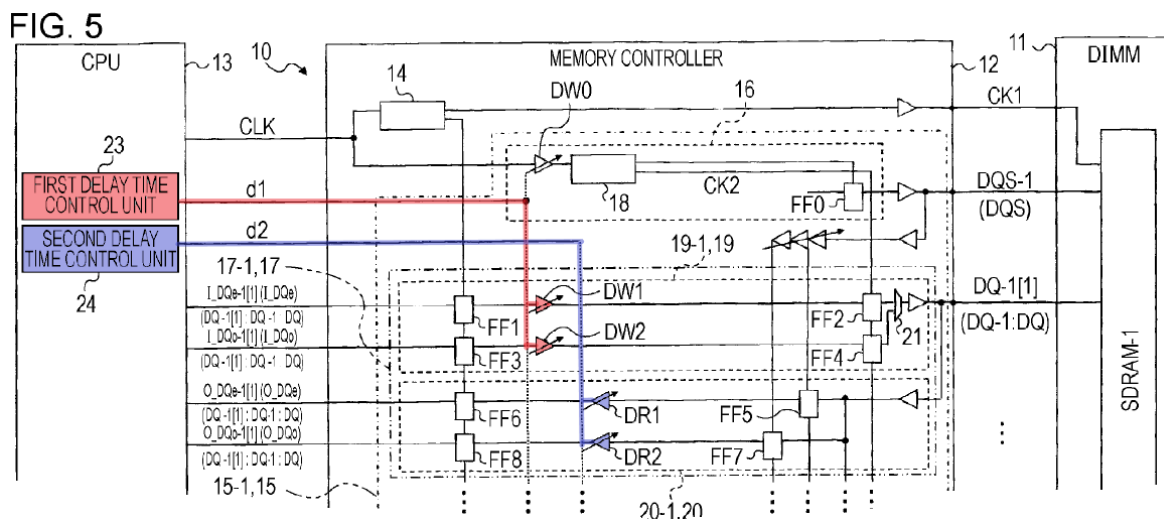
145. I also note that Dr. Wedig states that, in his opinion, “[a] Skilled Artisan would have also understood that, in alternative implementations, delay elements similar to Tokuhiro’s DR elements can be used instead of or in addition to Hiraishi’s FIFO circuit for delaying the read data.” EX1003, ¶262. To the extent that Dr. Wedig is contending that it would have been obvious to add Tokuhiro’s DR1 element to the data path in Hiraishi, there is nothing the prior art to suggest such an arrangement, nor does he provide any support or explanation.

XI. GROUND 2: A POSA WOULD NOT HAVE HAD A REASONABLE EXPECTATION OF SUCCESSFULLY MODIFYING HIRAISHI AS PROPOSED

146. Moving Tokuhiro's DR-1 delay element from the memory controller into Hiraishi's data buffer is not consistent with normal memory module design. In fact, I understand that Dr. Wedig previously testified that he has never seen a reference that does not use the memory controller to adjust for fly-by delays seen by the memory controller. EX2016 (506 IPR Wedig Dep. Tr.), 171:15-21. As to the "second implementation," while Dr. Wedig states in his declaration that it would have been obvious to implement Tokuhiro's teachings in Hiraishi's "module controller" (EX1003, ¶ 268), I understand that he also previously testified that he has never seen a reference describing a "module controller" being used to program a delay element for read leveling. EX2016 (506 IPR Wedig Dep. Tr.), 194:18-21. The lack of disclosures in both cases is to be expected, however, because the transmitter on the memory module for read data would not know the precise delay experienced by the receiving memory controller to remove those delays accordingly. EX1003, ¶264 (arguing to insert Tokuhiro's DR-1 delay element into Hiraishi so that "read data arrives to the memory controller (MCH) at substantially the same time (T10) despite the fly-by delay (from T7 to T8) on the memory module.").

147. A POSA would not expect the combination proposed by Dr. Wedig to be operable for at least two reasons. **First**, the DR-1 delay element is proposed to be

added to Hiraishi's data buffer would be inoperable, as proposed. This limitation occurs because Tokuhiro's read and write leveling are controlled by the computer's main CPU, as Dr. Wedig confirmed. EX2012, 92:2-4, 93:6-9. In Tokuhiro, these operations are performed by the first delay time control unit 23 (highlighted in red below) and second delay time control unit 24 (highlighted in purple below), which are part of the computer's CPU 13, and which also provides the respective control signals d1 and d2 to control the variable delay circuits DW and DR in the memory controller 12 in all of the channels, in order to set the respective delays. EX1006 (Tokuhiro), 12:34-58; 13:55-14:2; 15:3-19. To illustrate, I have annotated a partial reproduction of FIG. 5 from Tokuhiro below. This operation includes not just determining read delays based on respective write delays, but also on the maximum of write delays across all channels. See annotated partial reproduction of FIG. 5 from Tokuhiro below.



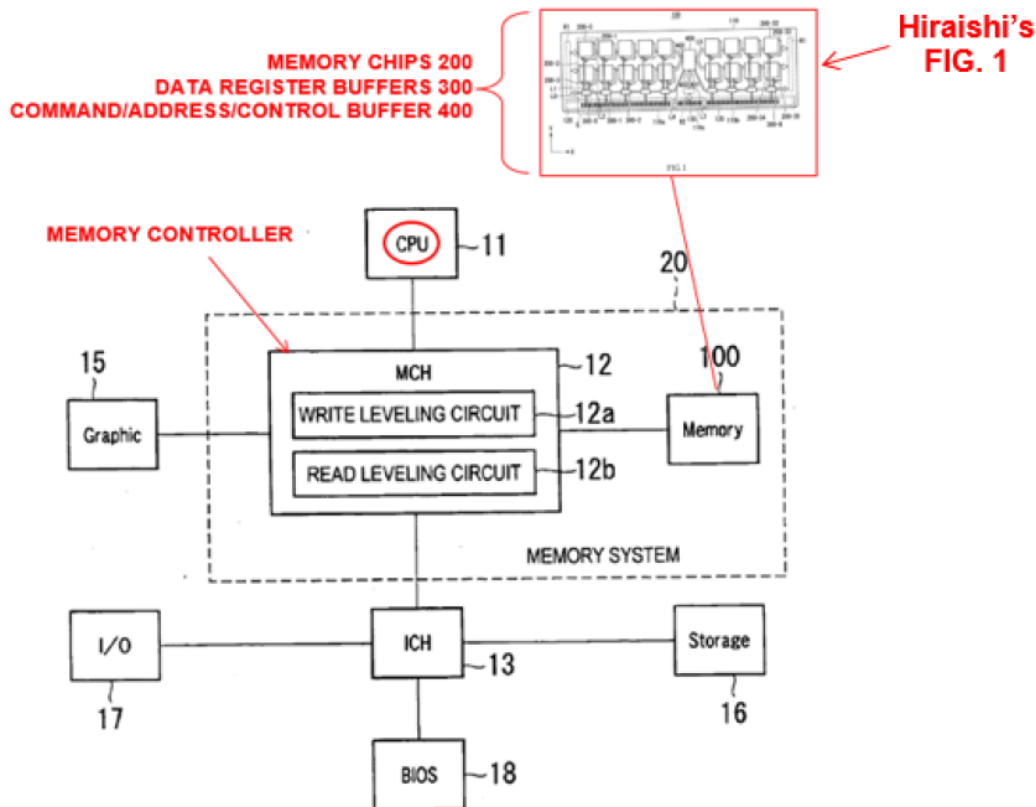
148. For example, Tokuhiro explains that “[t]he first delay time control unit 23 controls the first variable delay circuit DW, which is included in each of the control circuit units 15-1 to 15-in, to delay the data signal by the first delay time Dt1 based on the write leveling function, and it outputs the first control signal d1 for setting the first delay time Dt1.” *Id.*, 12:49-54. Moreover, “[t]he second delay time control unit 24 controls the second variable delay circuit DR ... to delay the data signal by the second delay time Dt2 in accordance with corresponding one of the first delay times Dtl-1 to Dtl-n set by the first delay time control unit 23, and it outputs the second control signal d2 for setting the second delay time Dt2.” *Id.*, 15:3-9. This is for all the channels. The first delay time control unit 23 also controls an additional variable delay circuit DW0 which is used to generate the DQS signal. See *id.*, 6:57-7:18. In Tokuhiro, it is the control signals d1 and d2 transmitted by the first and second time delay control units in CPU that allowed for variable time adjustment.

149. A POSA would understand that this architecture (i.e., Tokuhiro’s delay elements (DW and DR) being connected over dedicated CPU control lines on which control signals d1 and d2 from all channels are provided to the various delay elements) is why Tokuhiro can accommodate variable delay elements and determine the read delays using, not just the respective write delays, but also the maximum of write delays among all of the channels. EX2012, 92:25-93:4 (“Q. ... [S]o the signal

line d1 is dedicated to the DW delay elements and control signal line d2 is *dedicated* to the DR control elements? A. That's the way Tokuhiro implemented it, yes.”).

150. In contrast, in the combination proposed by Dr. Wedig, the only input to the delay element DR-1 is the local clock signal LCLKR, which is not a “control signal” and is not otherwise capable of operating a variable delay element.

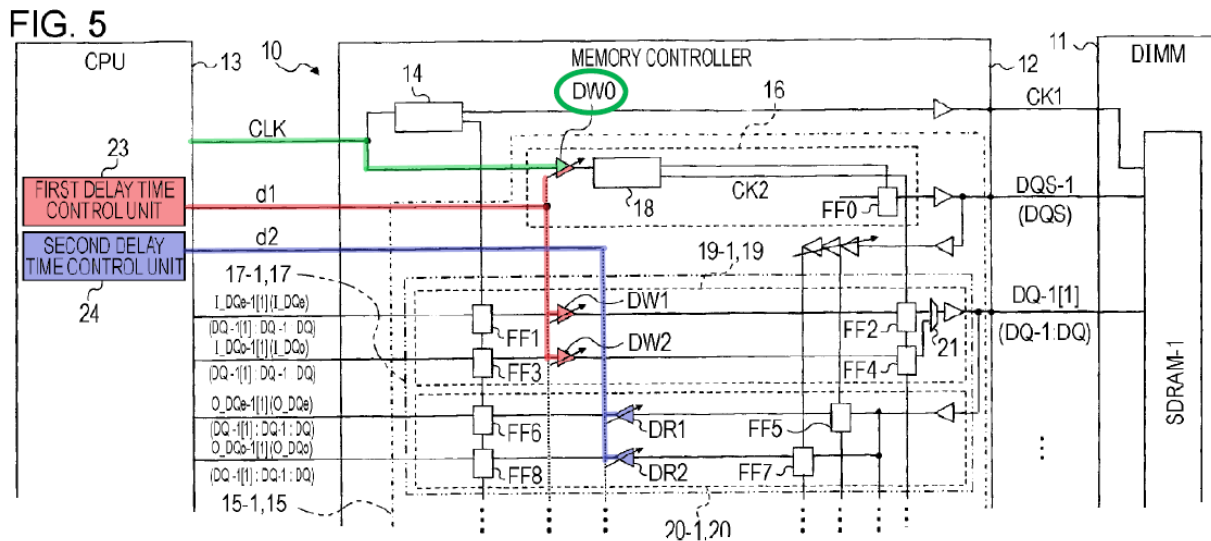
151. Further, I note that Hiraishi’s data register buffers 300 are connected to the memory controller 12 only, which in turn is connected to the CPU 11, as shown in the annotated version of Hiraishi’s FIG. 2 below. CPU 11 is not part of the memory system, and as such, the connection to the d2 signal from the CPU (required by Tokuhiro) would not be possible to make in Hiraishi’s circuit topology shown in FIG. 2 below.



152. As such, a POSA would understand that Dr. Wedig's proposed combination does not represent an operable configuration because, unlike Tokuhiro, in the proposed combination (reproduced below) the only inputs to the delay element DR-1 are the DQS signal (supplied via terminal 351 or 352 via the selector 332) and the local clock signal LCLKR, neither of which are a "control signal" like d2 of Tokuhiro that can operate a variable delay element or are otherwise capable of operating a variable delay element.

153. A POSA would understand that those clock signals and data strobe DQS signals are not control signals, like d2 or d1, that can operate Tokuhiro's delay elements. A delay element is designed to operate on an input, such as a clock signal

or, as here, a data strobe signal. The amount of delay applied to those inputs, however, will depend on control signals, such as d1 and d2 in Tokuhiro. The problem with the proposed combination is that it provides only the parameter that is to be delayed, but not the control that will determine how much delay is to be applied. This is also evident from Tokuhiro as well. Specifically, Tokuhiro's CPU provides control signals d1 and d2 to the memory controller 12 to indicate the desired value of the delay, in addition to providing a clock signal CLK, in each of FIGs. 4-6, 8-9, 12-15. A POSA would understand that the control signal d1 is used to control the amount of delay to be applied to the input parameter CLK. That is, a POSA would recognize immediately from Tokuhiro that CLK is not a control signal, but a signal to be delayed based on the d1 control signal at gate DW0. See below.



154. If a clock signal were capable of operating Tokuhiro's delay elements, Tokuhiro would not go through the additional complexity of adding dedicated

control lines d1 and d2 when the clock signal CLK is already being provided. It is well known in processor design that existing signal lines should be used, if possible, as opposed to adding new pins/signal lines to a CPU. In fact, a POSA would understand that the control lines d1 and d2 are essential since they indicate the value of the delay that the corresponding delay circuits DW and DR respectively need to be programmed with. EX1006, 9:1:6, 9:22-27, 11:5-10, 11:36-41.

155. I also note that Hiraishi's main CPU (CPU 11), as disclosed, cannot provide Tokuhiko's delay element control signal d2, as it does not include Tokuhiko's dedicated control lines. It would also not be obvious to add such control lines because, unlike in Tokuhiko where control is carried out by the CPU, in Hiraishi this would require adding signaling lines between the CPU and each one of Hiraishi's nine data register buffers 300-0 through 300-8. As I explain below, this organization would add substantial complexity which Dr. Wedig does not account for.

156. Adding additional control lines to indicate the delay(s) would be inefficient and needlessly complex on many counts. First, they would make the resulting memory non-compliant with the DIMM pinouts, requiring new signals from the CPU to the memory system that are not part of the DIMM specifications. This would make the resulting DIMM memory incompatible with the JEDEC standard. Secondly, the addition of the control lines would result in increased circuit

complexity because of the use of additional wires, and the extra spacing and power consumption that would be required to route these wires and drive their signals.

157. Therefore, a POSA would not have had a reasonable expectation of implementing the claimed delay features based on the proposed combination because Tokuhiro's delay element is not provided with the control signal it requires for operation.

158. **Second**, a POSA would not be motivated to use the new delayed DQS signal to clock data out from Hiraishi's FIFO because it would not reliably synchronize the DQS/DQ signals, as Hiraishi describes being necessary.

159. Hiraishi uses a local clock LCLKR to clock read data out of the FIFO (Read) 302, as I have highlighted in red below.

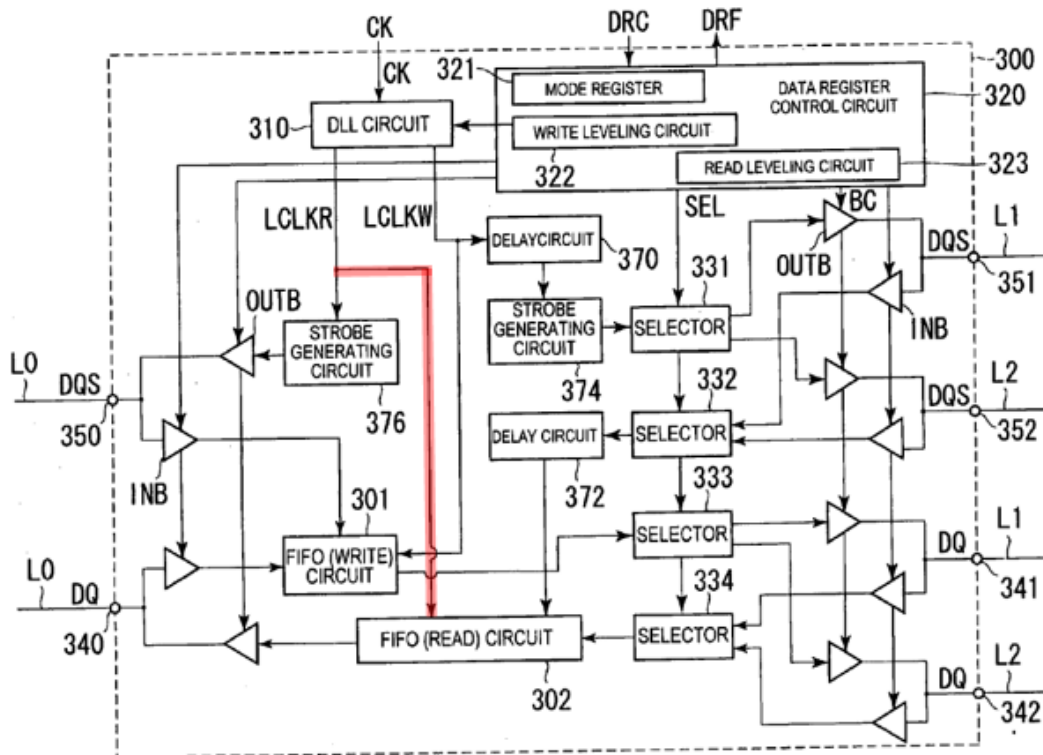
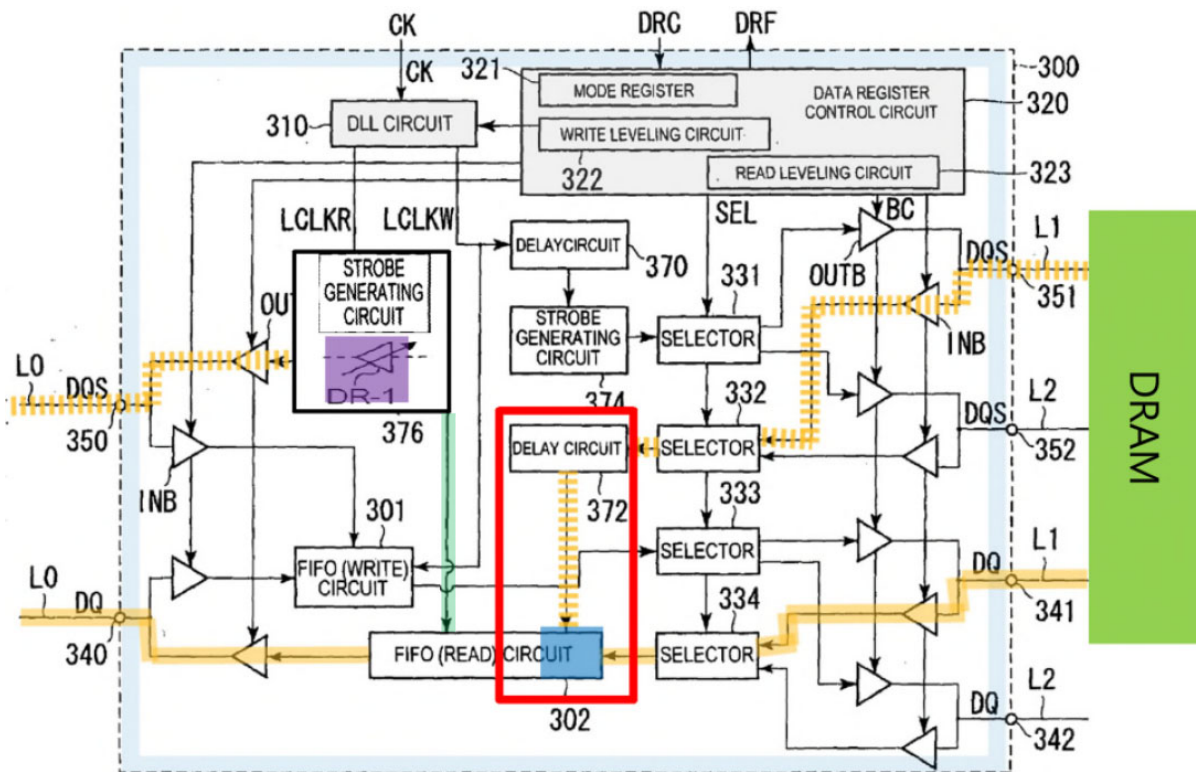


FIG. 5

EX1005, [0087] (“An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310.”). The DQS signal from delay circuit 372 to FIFO 302 is for sampling the data inputted to the read FIFO and does not control when the data is clocked out.

160. However, Dr. Wedig removes the local clock LCLKR signal supplied to the FIFO 302 in his proposed combination and replaces it with a newly-generated signal from Hiraishi’s modified strobe generating circuit 376. I have highlighted this new DQS signal line in **green** below, which is otherwise the same as the annotated version of Hiraishi’s FIG. 5 which Dr. Wedig sets forth in paragraph 262 of his declaration.



161. I understand that Dr. Wedig confirmed that the newly added line above from the modified strobe generating circuit 376 to the FIFO 302 (which I have annotated in green) is a DQS signal delayed by DR-1 that is being provided to clock data out from FIFO 302. EX2012, 90:15-91:18.

162. However, Dr. Wedig does not explain the substitution of the new delayed strobe from delay element DR1 in place of Hiraishi's local clock LCLKR signal going to the FIFO 302. Specifically, it is not clear why Hiraishi's local clock LCLKR does not continue to be used to synchronize the DQS/DQ signals in the same manner Hiraishi describes. In fact, I note that Hiraishi relies exclusively on local clock signals to synchronize output data and corresponding strobe signals for

both write and read operations. EX1005, [0087]. Specifically, for both read and write operations Hiraishi relies on local clocks to drive the corresponding output FIFOs and strobe generators, so that the data output from the FIFOs is properly aligned with the strobe output from the strobe generators, as shown in the annotated version of Hiraishi FIG. 11 below.

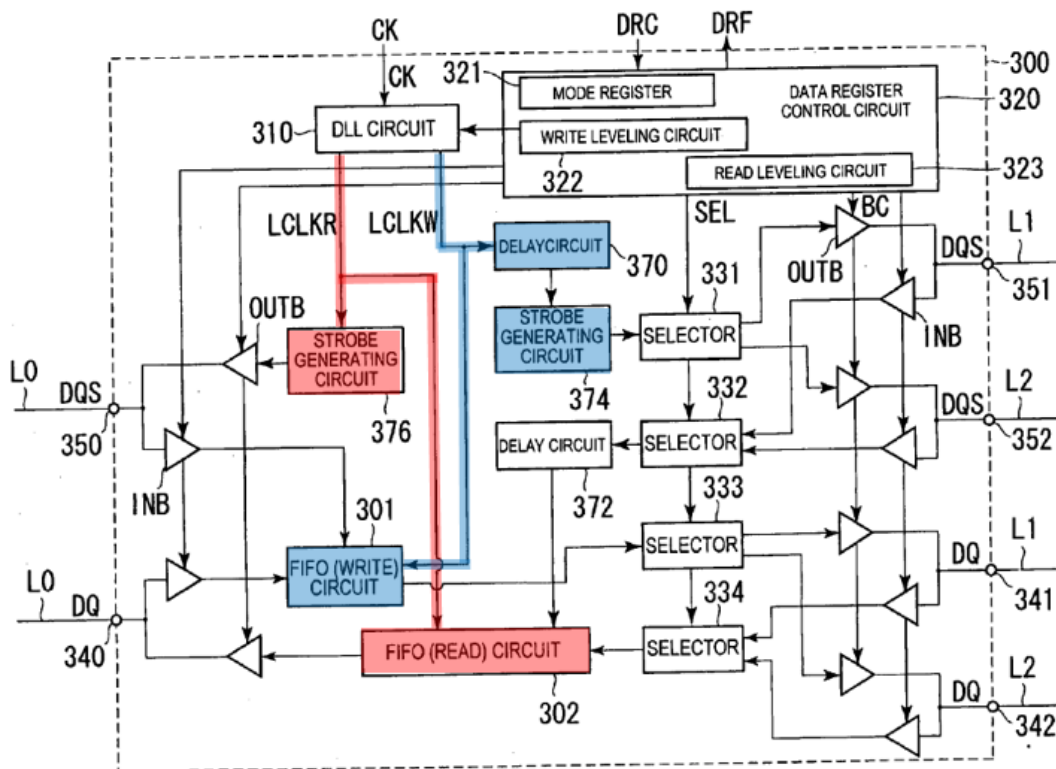
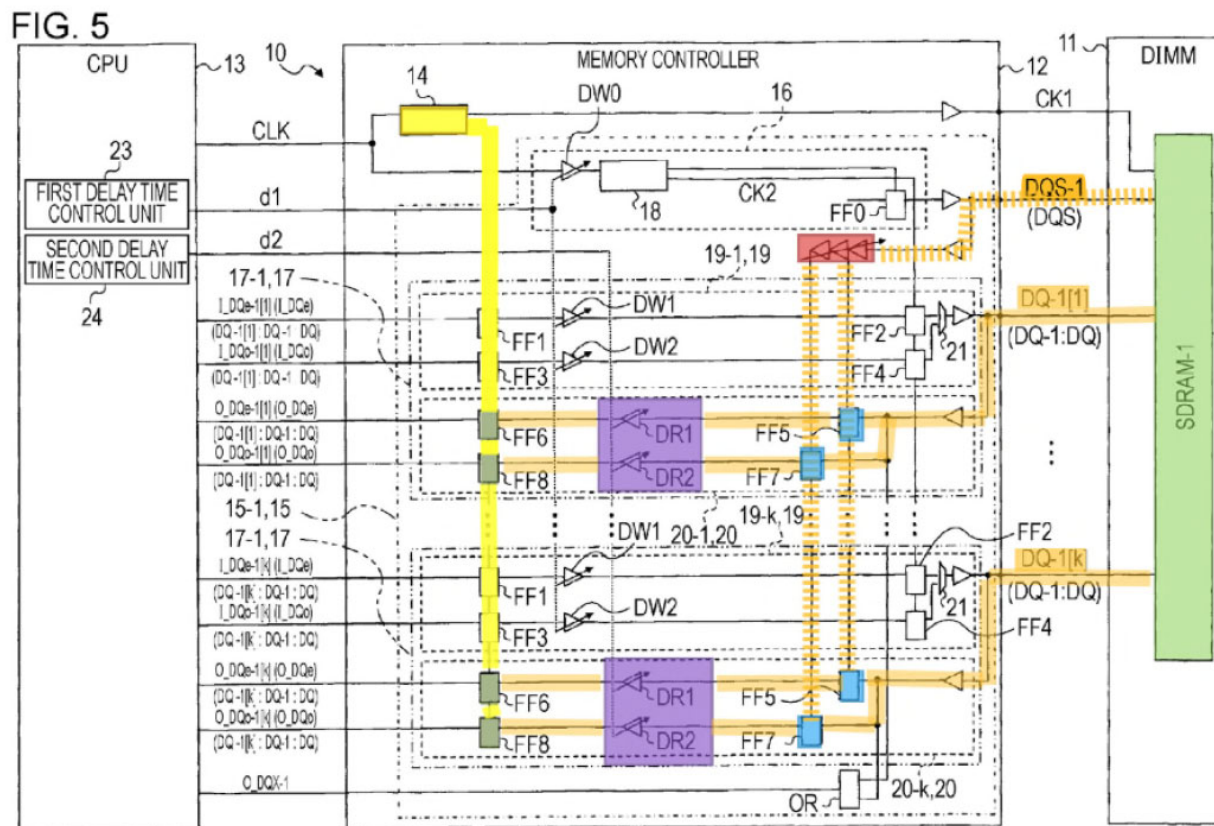


FIG.5

163. Tokuhiro does the same by using a local clock signal from clock signal generator 14 to output data from Tokuhiro's flip-flops. EX1006, 8:64-67, 9:17-21, 11:28-31, 12:1-5. It appears that Dr. Wedig agrees. EX1003, ¶ 235 ("As shown below, the details of delaying the data signals (solid orange) by the delay elements DR1 and DR2 (purple) before the values of those signals are captured by the *flip-*

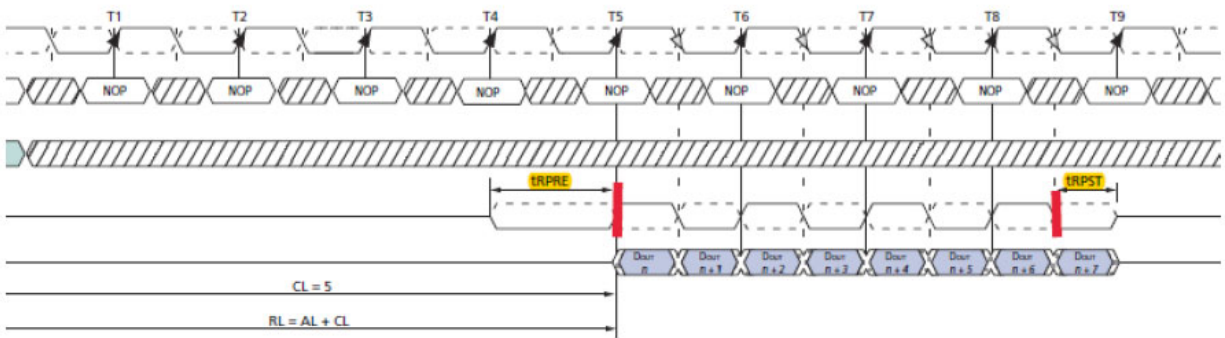
flops FF6 and FF8 (olive green) that use the clock domain (yellow) of the memory controller are illustrated by Tokuhiko's FIG. 5")



164. Like Hiraishi's use of the system clock CK to generate local clocks LCLKR and LCLKW, Tokuhiko's discloses that "[t]he first clock signal generator 14 generates and outputs the clock signal CK1 having a predetermined cycle based on a clock signal CLK input from a CPU 13." EX1006, 6:17-19. Tokuhiko also explains that "[t]he flip-flop FF6 outputs the third data signal O_DQe, which is input from the second variable delay circuit DR1, to the CPU 13 (described later) when the clock signal CK1 generated from the first clock signal generator 14 is input." *Id.*, 11:28-31. In other words, the flip-flops output data signals when the clock signal is

input. A POSA would understand this is describing the well-known mechanism of using a clock signal to clock out data from a data storage element. Thus, both Hiraishi and Tokuhiro expressly rely on clock signals, not DQS signals, to clock data out.

165. That Hiraishi and Tokuhiro rely on clock signals, not DQS signals, to clock data out is consistent with what a POSA would expect because DQS signals cannot reliably be used to clock out data. Unlike a clock signal, DQS signals includes a “Pre-amble” (tRPRE) and “Post-amble” (tRPST) which would cause additional bits to be clocked out due to the additional transitions at the edges of the pre- and post-ambles. See below.



BL8, RL = 5, AL = 0, CL = 5.

Dout n = data-out from column n .

NOP commands are shown for ease of illustration; other commands may be valid at these times.

BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA

Figure 25 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)

EX1020, 56.

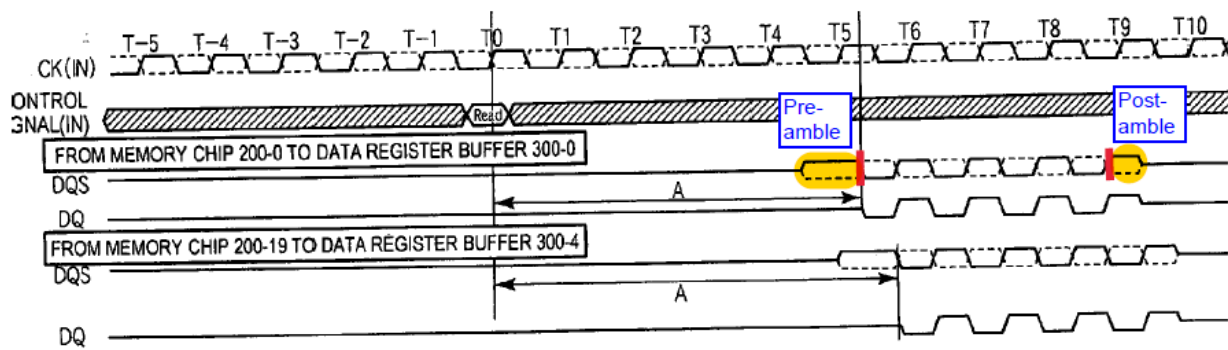


FIG.15

EX1005, FIG. 15 (annotated).

166. Attempting to clock out data from Hiraishi's FIFO with a DQS signal would mean the data is only being clocked out at an edge of the DQS signal, which likely will not be the correct timing at least at least because of the additional pre- and post-amble bits. Such additional bits are not present on clock signals, which is why clock signals are commonly used to clock data out of FIFOs or other data storage elements, like Hiraishi and Tokuhiko. In sum, a POSA would not reasonably expect that using DQS signals to clock data out of Hiraishi's FIFO would provide a reliable mechanism to synchronize the DQS/DQ signals at the data buffer output.

XII. A POSA WOULD NOT HAVE BEEN MOTIVATED TO COMBINE HIRAISHI AND TOKUHIRO, AS PROPOSED

A. Dr. Wedig's Alleged Motivations Do Not Motivate Deviating From Hiraishi's and Tokuhiko's Disclosures of Using Delay Elements in a Memory Controller

167. Dr. Wedig proposes three reasons why a POSA would purported be motivated to undertake the proposed combination of Hiraishi and Tokuhiko. First, to

“implement Tokuhiro’s technique of setting the read delays based on the write delays in the memory system of Hiraishi in order to simplify the read leveling operations and the corresponding circuitry.” EX1003, ¶247. Second, to “compensate for the fly-by delays between the different data buffers during a read operation so that the read data arrives at the memory controller from the different data buffers at substantially the same time.” EX1003, ¶250. Third, to remove fly-by delays that are greater than one clock cycle. EX1003, ¶252-255.

168. Tokuhiro relies on delay elements disposed in a memory controller (memory controller 12), which are programmed by the system’s main CPU (CPU 13). However, Dr. Wedig does not propose to add Tokuhiro’s delay element DR-1 to Hiraishi’s memory controller 12, or to program that delay element DR-1 with Hiraishi’s CPU 11. It is unclear why Dr. Wedig’s proposed combination deviates from Tokuhiro’s expressly disclosure, particularly when Hiraishi already has a memory controller 12 connected directly to the main CPU 13. *See e.g.*, EX1001, FIG. 2. Moreover, this modification appears to be unconnected to Dr. Wedig’s proposed 3 motivations for combining Hiraishi and Tokuhiro because the same alleged benefits would have been achieved if a POSA adhered to Tokuhiro’s express disclosure of using delay elements in the memory controller.

169. For example, regarding the first reason, to the extent that Tokuhiro is relied on as suggesting that read delays can still be based on determined write delays,

this would have to be the case with Tokuhiro's disclosed design of relaying on delay elements in the memory controller. Regarding the second reason, Tokuhiro already makes data available to the system at the same time, as Dr. Wedig confirmed. EX2012, 96:8-13 ("Q. And then is the DQ data being delayed so that it all is available at T10 in the memory controller? A. Yeah **that's exactly what Tokuhiro's teaching** yeah in order to have them so that they're all available at the same time so that **it all appears as though to the system that they arrived at T10.**"). Moreover, Tokuhiro achieves this result without using any "special mechanism, such as FIFO based techniques," which appears to be a related reason. EX1003, ¶251. Regarding the third reason, to the extent that Tokuhiro can manage delays of more than one clock cycle (it cannot as I explain below), that would necessarily have to be the case in Tokuhiro's original design, i.e., based on delay elements in the memory controller.

170. Thus, even if Dr. Wedig's alleged motivations to combine Hiraishi and Tokuhiro were true, a POSA would not have one reason to deviate from Hiraishi's and Tokuhiro's express disclosures of using delay elements in the memory controller, particularly because Hiraishi already has a memory controller 12 that performs leveling, and a CPU 13 connected directly to it.

B. Dr. Wedig's Reasons for Moving Tokuhiro's Delay Elements Are Contrary to General Knowledge

171. Regarding the placement of the delay element in Hiraishi's data buffer, it appears that Dr. Wedig may believe there are separate reasons for doing so.

Specifically, Dr. Wedig states that “[a] Skilled Artisan would have understood that an important advantage of this combination is that the memory controller (MCH) receives all read data at substantially the same time, so it does not have to manage large fly-by delays of read data either during the training or during normal operation as it tries to capture the correct value of the read data. Accordingly, the memory controller can be implemented with less circuitry and function. For example, the memory controller does not need extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles due to the larger than clock cycle fly-by delays on the module.” EX1003, ¶265). I do not agree.

172. First, Tokuhiro does not disclose accounting for delays greater than one clock cycle. Tokuhiro’s memory module is a DDR module which means that there are two data periods for every clock cycle. Specifically, the first DDR standard explained double-data-rate architecture as follows:

The 64 Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ prefetch architecture with an interface **designed to transfer two data words per clock cycle** at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM effectively consists of a single $2n$ -bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n -bit wide, **one-half-clock-cycle data transfers** at the I/O pins.

EX2018, 5 (JEDEC JESD79) (emphasis added).

173. As further evidence that Tokuhiro’s “data period” is referring to half of a clock cycle, I note that Tokuhiro refers to typical DDR3 memory interface, as Dr.

Wedig acknowledges, which at the time of Tokuhiro's DDR3 operated at -800 all the way to -1600 (meaning operating at 400MHz to 800MHz), as shown in Table 50 of the DDR3 standard below.

Table 50 — For IDD testing the following parameters are utilized.

Parameter Bin	DDR3-800		DDR3-1066			DDR3-1333			DDR3-1600			Unit
	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	8-8-8	9-9-9	10-10-10	
$t_{CKmin}(IDD)$	2.5		1.875			1.5			1.25			ns
CL(IDD)	5	6	6	7	8	7	8	9	8	9	10	
$t_{RCDmin}(IDD)$	12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
$t_{RCmin}(IDD)$	50	52.5	48.75	50.63	52.50	46.5	48	49.5	45	46.25	47.5	ns
$t_{RASmin}(IDD)$	37.5	37.5	37.5	37.5	37.5	36	36	36	35	35	35	ns
$t_{RPmin}(IDD)$	12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
$t_{FAW}(IDD)$	x4/ x8	40	40	37.5	37.5	37.5	30	30	30	30	30	ns
	x16	50	50	50	50	50	45	45	45	40	40	ns
$t_{RRD}(IDD)$	x4/ x8	10	10	7.5	7.5	7.5	6.0	6.0	6.0	6.0	6.0	ns
	x16	10	10	10	10	10	7.5	7.5	7.5	7.5	7.5	ns
$t_{RFC}(IDD) - 512Mb$		90	90	90	90	90	90	90	90	90	90	ns
$t_{RFC}(IDD) - 1 Gb$		110	110	110	110	110	110	110	110	110	110	ns
$t_{RFC}(IDD) - 2 Gb$		160	160	160	160	160	160	160	160	160	160	ns
$t_{RFC}(IDD) - 4 Gb$		300	300	300	300	300	300	300	300	300	300	ns
$t_{RFC}(IDD) - 8 Gb$		350	350	350	350	350	350	350	350	350	350	ns

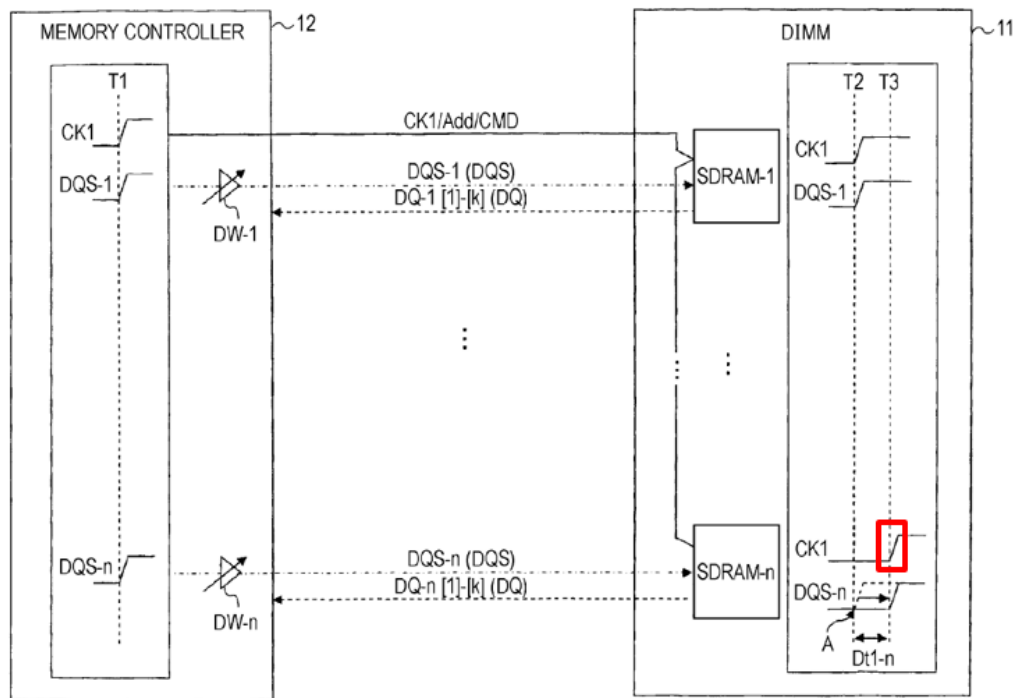
EX2019 (JESD79-3A), p. 128 (Table 50).

174. As shown in the table above, for the fastest DDR3-1600 (i.e. data rate is 1600 million transfer per second 1600MTs) the clock period is exactly 1.25 ns. Tokuhiro expressly states that 1 ns is “greater than a typical data period of the DDR3 memory interface,” which at minimum is 0.625 ns (meaning exactly half the 1.25ns = 0.625ns), see t_{CKmin} in Table 50 above. Thus, the data period in Tokuhiro is referenced to half a clock cycle where one data bit/word is outputted/transmitted.

175. I also note that Tokuhiro cannot deal with delays greater than one clock cycle because Tokuhiro determines delays by “gradually prolong[ing] the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time” EX1006, 13:55-60. This process can only align the DQS-n with the next up or down clock edge, as shown for example in Tokuhiro’s FIG. 7. This limitation is due to the incremental increase in delay time will continue until the process detects a clock transition. But because all clock rising edges look the same and all clock falling edges look the same, the process will not know to skip a clock edge and align the DQS to the next clock edge in order to correct for a greater than one clock cycle delay. Thus, Tokuhiro can only align the DQS with the next up or down clock edge, which would necessarily occur in less than one clock cycle.

176. FIG. 7 of Tokuhiro (reproduced below) shows DQS-n being aligned to the next clock edge that the system detects, which in this case is T3.

FIG. 7



177. Hiraishi's memory controller 12 is on the computer's motherboard 12, not on the memory module 100.

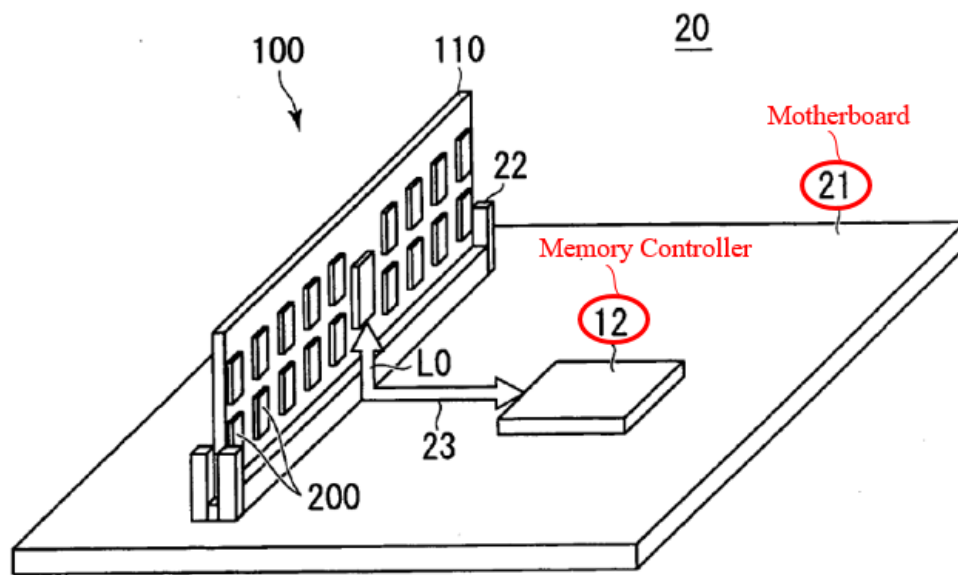
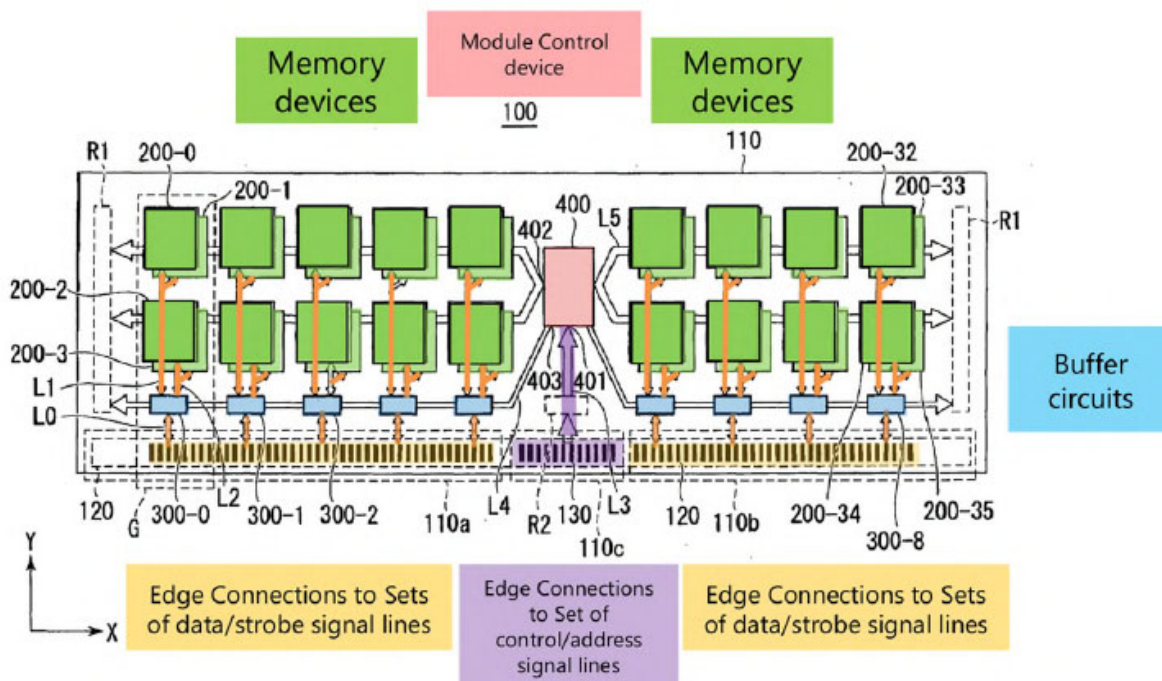


FIG.3

178. In contrast, Hiraishi's data buffers 300 reside directly on the memory module 100, as shown below (light blue).



179. A POSA would understand that the memory controller, located on the motherboard, would be far less space-constrained than the memory module. I understand that Dr. Wedig agrees. EX2016 (506 IPR Dep. Tr.), 143:5-144:2; Moreover, the JEDEC standard limits the size of the memory module, which Dr. Wedig also confirmed. EX2012, 94:11-22; EX2016 (506 IPR Dep. Tr.), 142:15-24. There are persistent market pressures to increase memory capacity and add additional memory devices to the memory module. Moreover, it is known in the context of electronic circuitry generally and memory modules in particular that limited space coupled with intense computing is detrimental to heat dissipation. EX2017 (electronic cooling). Having proper heat dissipation is critical to ensuring reliable and high-performance operation. As such, the last place one would want to add extra

logic and circuitry would be to a component competing with the memory devices for the limited space available on a DIMM.

180. I also note that Dr. Wedig cites to Giovannini in support of his argument that large fly-by delays were a problem. However, like Hiraishi and Tokuhiro, Giovannini also relies on circuitry in the memory controller to address fly-by delays, as Dr. Wedig explains. EX1003, ¶ 253 (“To solve this known problem of fly-by delays that are larger than a clock cycle, Giovannini discloses a special, FIFO-based circuitry in the memory controller.”). Although I disagree that FIFO circuitry is special, it is certainly conventional, Giovannini use of circuitry in the memory controller to address fly-by delays is in accordance with conventional design because the memory controller is the lesser space-constrained component (as compared to the DIMM) in which to add the required logic and circuitry.

181. Moreover, there is also the non-trivial matter of Tokuhiro’s delay elements needing to be programmed. Tokuhiro teaches that its delay circuits are programmed over dedicated control signal lines d1 and d2, as Dr. Wedig acknowledged. I note that Dr. Wedig does not propose a different control mechanism in his declaration. Thus, based on Tokuhiro’s implementation, the combination would also require running an additional control signal line to each of the delay elements added to Hiraishi’s nine data buffers. This modification would

significantly complicate the circuitry and increase costs, as noted above. See *supra*, ¶¶ 155-156.

182. Dr. Wedig also suggests there is a benefit in avoiding the memory controller having to manage fly-by delays and therefore being able to have less logic and circuitry in the memory controller by moving Tokuhiko's delay element into Hiraishi's data buffer is illusory. EX1003, ¶265. However, Dr. Wedig confirmed that, in his proposed implementation, the memory controller is still performing leveling operations and would require the same logic and circuitry as before. See *infra*, ¶185; EX2016, 181:9-15. Thus, it is not clear what logic and circuitry in the memory controller is no longer required in the proposed combination.

183. A related point made by Dr. Wedig is that a "Skilled Artisan would have also understood that the advantages of implementing Tokuhiko's read delays in the data buffers of Hiraishi include that it would remove the large fly-by delays on the module at the first practically available location, so that the rest of the system does not have to manage those large fly-by delays." EX1003, ¶266. It is unclear how or why removing fly-by delays at the first possible location represents an improvement or would otherwise be desirable. What would be desirable is to remove fly-by delays in the most efficient manner, which would be using the module controller, just as Hiraishi, Tokuhiko, and Giovannani all do.

184. There is a significant advantage of having Tokuhiro's delay elements implemented in the memory controller. As taught in Tokuhiro, the delays are determined in a process in which "the first delay time control unit 23 ... gradually prolongs the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signals DQS-n are input to the n-channel SDRAM-n substantially at the same time." EX1006, 13:55-60. This process of "gradually prolong[ing] the delay time for the first variable delay circuit DW-n" would be significantly less complex if performed when the first delay time control unit 23 and the first variable delay circuit DW-n are on the same side of the data bus. If the first delay time control unit 23 and the first variable delay circuit DW-n are on the different sides of the data bus, as Dr. Wedig proposed, the gradual prolonging of the delay time would require the memory controller to instruct the memory module to adjust the delay time repeatedly until the DQS-n is aligned with the edge of the CK. The memory controller can only communicate with the memory module following DDR3 signaling protocols. EX1006, 5:57 ("The memory controller 12 is a DDR3 (Double Data Rate 3) memory interface"). Thus, this process would take a significantly longer amount of time than if where the first delay time control unit 23 and the first variable delay circuit DW-n are on the same side of the data bus, where such operations would not need to comply with DDR3 signaling protocols as they

would all be either internal to the memory controller, or between the CPU and the memory controller.

185. Contrary to Dr. Wedig's assertion, the proposed combination does not significantly reduce the leveling burden on the memory controller, as Dr. Wedig testimony suggests. EX2016 (506 IPR), 181:9-15 ("Q. In the combination of Hiraishi and Tokuhiro, Hiraishi's memory controller is still adjusting the incoming data so that it is being captured in the valid data eye? A. Yeah, just like it was before. I mean, there's no -- you had to do that when you did before you ever added Tokuhiro."). Dr. Wedig further indicated that even in the Hiraishi-Tokuhiro combination the memory controller might have "to do some clean-up, some slight adjustment" for flight time, and in any event would have to include a delay element for adjusting DQS by 90 degrees. EX2012, 105:24-106:1, 106:4-107:10. As such, it is unclear what logic and circuitry in the memory controller would no longer be required in the proposed combination.

186. Moreover, Dr. Wedig's proposed offloading of logic and circuitry from the memory controller is also at odds with the fact that the JEDEC committee intentionally shifted much of the burden of timing synchronization to the memory controller by first forcing the memory controller to provide a correctly centered DQS signal for write operations, and then to further correct the phase of the DQS for read operations so that the data can be latched in the center of the valid data window (the

eye) despite the fact that the DRAM devices are placing read data on the data bus with the same phase as the DQS signal. EX2012, 406.

C. A POSA Would Not Have Been Motivated to Combine Hiraishi and Tokuhiro Based on Dr. Wedig's Alleged Motivations

187. As noted above, Dr. Wedig proposes three reasons why a POSA would purported be motivated to undertake the proposed combination of Hiraishi and Tokuhiro. First, to “implement Tokuhiro’s technique of setting the read delays based on the write delays in the memory system of Hiraishi in order to simplify the read leveling operations and the corresponding circuitry.” EX1003, ¶247. Second, to “compensate for the fly-by delays between the different data buffers during a read operation so that the read data arrives at the memory controller from the different data buffers at substantially the same time.” EX1003, ¶250. Third, to remove fly-by delays that are greater than one clock cycle. EX1003, ¶252-255.

188. With respect to first reason of reducing the number of leveling steps , the combination would not reduce the overall number of leveling steps. It would increase the number of signaling operations. This result is due to the fact that the combination, as it has been proposed, requires the “memory controller” (under the first implementation) or the “module controller” (under the second implementation) to transmit control signals to each of delay elements that have been added to Hiraishi’s nine different data buffers. EX2016 (506 IPR Dep. Tr.), 174:7-11. Moreover, according to Dr. Wedig, each of those nine data buffers would

individually be detecting delays, measuring the delays, providing feedback to the module controller or memory controller, depending on the implementation, and then writing the delay into the nine DR-1 elements. EX2016 (506 IPR Dep. Tr.), 151:2-13 (“[Y]ou would need to be able to provide some feedback to the module controller.”); 152:17-23 (“[Y]ou might need to modify some of it to be able to detect the delay, to be able to measure the delay, and then you need to be able to rewrite the -- you need to be able to write the delay for the read path into DR1.... You would need to be able to do calculations on what the read delay would be, and you would need to be able to write the value into the read delay driver.”).

189. These operations that Dr. Wedig describes are needed are spread out over nine different data buffers, instead of being contained in the memory controller itself, as Hiraishi describes. That would necessarily require the number of signaling steps needed for Hiraishi to perform its S5 leveling to increase, not decrease.

190. With respect to the second reason of “compensate[ing] for the fly-by delays between the different data buffers during a read operation so that the read data arrives at the memory controller from the different data buffers at substantially the same time” (EX1003, ¶250), it is firstly unclear what benefit this proposal provides. Hiraishi’s read data is output from the data buffers at T6 which means that if the data signal lines between the memory controller and DIMM are of “the same length” (EX1006, 5:52-53), as Tokuhiro assumes, the data would have arrived at the memory

controller at same time. Different arrival times would be due to different lengths, but Tokuhiro does not address that solution, let alone provide a solution. The memory controller is the most capable component, as between the data buffer and the controller, for signal processing and managing timing adjustments. The memory controller would have more processing power than the data buffer and could rely on processing circuitry that does not need to be duplicated nine times for each of the data buffers. Moreover, I agree with Dr. Wedig that the delay elements in Tokuhiro effectively makes it appear to the system that all data arrives at the same time. EX2012, 96:8-13 (“Q. And then is the DQ data being delayed so that it all is available at T10 in the memory controller? A. Yeah that's exactly what Tokuhiro's teaching. Yeah, in order to have them so that they're all available at the same time. So that it all appears as though, to the system, that they arrived at T10.”). Thus, whatever perceived benefit there may be from preventing the rest of the system from managing fly-by delays, Tokuhiro’s delay elements already do that in the memory controller. Moreover, the proposed modification is not preventing the memory controller from having to manage delays because there are other signal delays which exist, even in the proposed combination. EX2012, 106:1, 106:4-107:10 (Dr. Wedig indicated that even in the Hiraishi-Tokuhiro combination the memory controller might have “to do some clean-up, some slight adjustment” for flight time, and in any event would have to include a delay element for adjusting DQS by 90 degrees.).

191. With respect to the third reason, as I described above, Tokuhiro does not address fly-by delays greater than one clock cycle. *See supra*, ¶¶172-176.

192. In sum, I do not agree that a POSA would have been motivated to combine Hiraishi and Tokuhiro based on Dr. Wedig's alleged motivations.

XIII. CONSIDERATION OF IPRS OF RELATED PATENTS

A. IPR of U.S. Patent No. 10,860,506

193. I understand that the claims of U.S. Patent No. 10,860,506 (“the ’506 patent”) were challenged in IPR2022-00711 (“the ’506 IPR”). I understand that the Board found that claims 1-20 of the ’506 patent had been shown to be unpatentable. Although the ’506 patent is related to the ’608 patent, the ’506 patent is directed to a different invention and there are several important differences in the claims. For example, the claims of the ’506 patent recite delaying a “first read strobe,” not delaying a data signal through a “data path.” The ’506 patent also does not recite a “delay circuit” at all, particularly not one included in data paths that each correspond to a data signal line in a set of data/strobe signal lines. Also, unlike the ’608 patent, the ’506 patent requires using the delayed strobe signal to sample the read data.

194. Even though similar prior art references were used in the ’506 IPR as are being used in this IPR against the ’608 patent, the actual grounds and theories are substantially different. For example, in the ’506 IPR a strobe centering process described in Butt was used to modify Hiraishi to allege that the Hiraishi's strobe

delay circuit 372 was performing a function of delaying the “first strobe signal.” EX2020 (506 IPR Petition), 43-48. This alleged delayed strobe signal was proposed to then be used to sample the read data in Hiraishi’s FIFO 302, which was alleged to satisfy the “sampling” limitation of the ’506 patent. EX2020 (506 IPR Petition), 36-38. No such allegation was made in the present IPR.

195. I further note that the final written decision in the ’506 IPR was based on findings and reasoning which are not relevant to the claims of the ’608 patent and/or the contentions and theories on which the challenge of the ’608 patent are based. For example, the Board in the ’506 IPR found that “Butt’s read training is such a known technique that would improve Hiraishi’s memory” EX2021 (506 IPR Decision, 15), whereas here Dr. Wedig and the ’608 Petition do not rely on Butt to satisfy any claim limitation, as the Board found at institution. Institution Decision at 11-12. Also, the Board in the ’506 IPR did not have to address the issue of whether Hiraishi’s strobe delay circuit 372 is in a data path that corresponds to a data signal line because the ’506 patent does not include such a limitation. Also, the Board in the ’506 IPR found that claim 1 of the ’506 patent “does not recite any particular location inside the data buffer at which the delay determination is made,” whereas here the claims of the ’608 patent specific that the location of the “delay circuit” as being in the “data path.” EX2022 (506 IPR Rehearing Decision), 4-5.

B. IPR of U.S. Patent No. 9,824,035

196. I understand that the claims of U.S. Patent No. 9,824,035 (“the ’035 patent”) were challenged in IPR2022-00236 (“the ’035 IPR”). I understand that the Board found that claims 1, 10–13, 21 of the ’035 patent were unpatentable, while claims 2, 6, and 22 were not shown to be unpatentable.

197. Although the ’035 patent is related to the ’608 patent, the ’035 patent is directed to a different invention and there are several important differences in the claims. For example, claim 1 of the ’035 patent recites obtaining “timing information,” while ’608 patent recites determining an amount of delay by a command processing circuit. The ’035 patent then uses the “timing information” to “control timing of respective data and strobe signals,” while the ’608 patent delays a signal through a data path corresponding to a data signal line with a delay circuit that is included in the data path. Moreover, the ’608 patent recites tristate buffers in the data path, which are not required by the ’035 patent.

198. In the ’035 IPR, the challenge was based on Osanai’s S4 leveling, which corresponds to the leveling operations between the data buffer and the memory devices. The challenge proposed to incorporate Tokuhiro’s processing into Osanai’s existing S4 leveling circuitry. EX2023 (’035 Final Decision) at 38-39 (“Petitioner’s proposed modification involves using Tokuhiro’s leveling technique in Osanai’s data register control circuit 320,” where the data register control circuit

320 contains the read leveling circuit which implements Hiraishi's S4 leveling operations.). In contrast, the challenge in the '608 IPR theory is based on modifying Hiraishi data buffer to incorporate Tokuihiro's DR-1 delay element, and then using programming that added delay element to account for delays between the memory controller and the buffer circuit (not between the buffer circuit and memory devices which is the province of Hiraishi's S4 leveling).

199. I further note that the final written decision in the '035 IPR was based on findings and reasoning which are not relevant to the claims of the '608 patent and/or the contentions and theories on which the challenge of the '608 patent are based. For example, the Board in the '035 IPR did not have to consider many of issues raised in the '608 IPR, such as any of alleged motivations for moving Tokuihiro's delay element out of the memory controller and into the data buffer. Moreover, regarding the limitation of controlling signal timing, the Board in the '035 IPR expressly relied on Petitioner's argument that Hiraishi's "input buffers (INB) act as a gate allowing data and strobe signals to either pass through or not pass through," and that this was done "in consideration of a propagation time of a signal," to find Osanai's disclosure "sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel." EX2023 ('035 Final Decision) at 36. In contrast, the Petitioner here relies on Hiraishi's input buffers (INB) to satisfy the separate tristate buffer limitation which is not part of the claims

of the '035 patent. Dr. Wedig testified that Hiraishi's INB buffers are not part of the alleged "delay circuit." EX2012, 31:23-25 (Q. And so those tristate buffers, those OUTB and INB buffers, are those part of the delay circuit as well? A. No, they're not.").

APPENDIX A

(Curriculum vitae)

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Highlights

Reviewed and valued thousands of patents.
Priced over \$500M worth in patent portfolios.
Key technical support for licensing that has raised more than \$1B.
Significant experience developing claim charts and evidence of use.
Former tenured professor at the University of California.
Deposition and trial testifying experience.

Education

BSE (1987), MSE (1992), & Ph.D. University of Michigan
Doctoral Thesis 1992: Performance Bounds and Buffer Space Requirements for
Concurrent Processors

Employment

2009-Present	Sole Proprietor of Phase Two LLC – Consulting and intellectual property services All IP related work since 2009 has been conducted under the auspices of Phase Two
2012 May-June	CTO Computers and Consumer Electronics at IP Navigation Group
2005-2008	Intellectual Ventures, Bellevue Washington
2005	Patent valuation, licensing support, focus on computer patents
2006	Head of all IV valuation efforts – managed a team of 12
2007	Director of technology, outbound licensing in consumer electronics
2008	Director of investment strategy, inventor relations
2001-2005	Associate Professor, EE UCLA
1995-2001	Assistant Professor, EE UCLA Focus low power embedded multimedia communications systems
1993-1995	Motorola Wireless Data Group Systems architect for General Magic wireless PDA

1991-1992	Motorola Corporate Research Parallel computer performance monitoring Low power processor architecture
1986-1987	Chrysler Corporation Software Architect

Patents

9,760,588 - Cross-media storage coordination
 9,747,426 - Handling masquerading elements
 9,716,548 - Data center with free-space optical communications
 9,692,887 - Component information and auxiliary information related to information ...
 9,683,884 - Selective audio/sound aspects
 9,680,699 - Evaluation systems and methods for coordinating software agents
 9,659,188 - Obfuscating identity of a source entity affiliated with a communique ...
 9,641,537 - Conditionally releasing a communique determined to be affiliated with a ...
 9,583,141 - Implementing audio substitution options in media works
 9,513,157 - Selective audio/sound aspects
 9,479,535 - Transmitting aggregated information arising from appnet information
 9,455,035 - Management of memory refresh power consumption
 9,426,387 - Image anonymization
 9,374,242 - Using evaluations of tentative message content
 9,372,536 - Touch screen with tactile feedback
 9,367,833 - Data services outsourcing verification
 9,306,975 - Transmitting aggregated information arising from appnet information
 9,274,582 - Power consumption management
 9,230,601 - Media markup system for content alteration in derivative works
 9,219,815 - Identifier technique for communication interchange
 9,215,512 - Implementation of media content alteration
 9,191,341 - Packet routing within an on-chip network
 9,178,911 - Evaluation systems and methods for coordinating software agents
 9,158,771 - Component information and auxiliary information related to information ...
 9,152,928 - Context parameters and identifiers for communication
 9,092,928 - Implementing group content substitution in media works
 9,065,979 - Promotional placement in media works
 9,008,117 - Cross-media storage coordination
 9,008,116 - Cross-media communication coordination
 8,984,579 - Evaluation systems and methods for coordinating software agents
 8,984,133 - Providing treatment-indicative feedback dependent on putative ...
 8,966,630 - Generating and distributing a malware countermeasure
 8,949,337 - Generation and establishment of identifiers for communication

8,943,267 - Management of memory refresh power consumption
8,929,208 - Conditionally releasing a communique determined to be affiliated ...
8,924,975 - Core selection for applications running on multiprocessor systems ...
8,913,753 - Selective audio/sound aspects
8,910,033 - Implementing group content substitution in media works
8,886,577 - Feedback during surgical events
8,850,044 - Obfuscating identity of a source entity affiliated with a communique in ...
8,839,255 - Scheduling of threads by batch scheduling
8,819,686 - Scheduling threads on different processor cores based on ...
8,818,196 - Data center with free-space optical communications
8,799,912 - Application selection of memory request scheduling
8,774,637 - Data center with free-space optical communications
8,732,087 - Authorization for media content alteration
8,730,836 - Conditionally intercepting data indicating one or more aspects ...
8,712,250 - Data center with free-space optical communications
8,682,982 - Preliminary destination-dependent evaluation of message content
8,655,187 - Data center with free-space optical communications
8,640,248 - Handling masquerading elements
8,640,247 - Receiving an indication of a security breach of a protected set of files
8,627,402 - Evaluation systems and methods for coordinating software agents
8,626,848 - Obfuscating identity of a source entity affiliated with a communique ...
8,626,731 - Component information and auxiliary information related to ...
8,613,095 - Smart distribution of a malware countermeasure
8,607,336 - Evaluation systems and methods for coordinating software agents
8,607,234 - Batch scheduling with thread segregation and per thread type marking ...
8,601,530 - Evaluation systems and methods for coordinating software agents
8,601,207 - Management of memory refresh power consumption
8,601,104 - Using network access port linkages for data structure update decisions
8,588,618 - Data center with free-space optical communications
8,583,553 - Conditionally obfuscating one or more secret entities with respect to ...
8,559,307 - Routing packets in on-chip networks
8,555,396 - Authenticatable displayed content
8,549,077 - Usage parameters for communication content
8,539,581 - Efficient distribution of a malware countermeasure
8,516,300 - Multi-voltage synchronous systems
8,483,569 - Data center with free-space optical communications
8,281,036 - Using network access port linkages for data structure update decisions
8,255,745 - Hardware-error tolerant computing
8,243,045 - Touch-sensitive display device and method
8,224,930 - Signaling partial service configuration changes in appnets
8,224,907 - System and method for transmitting illusory identification characteristics
8,214,191 - Cross-architecture execution optimization
8,209,755 - Signaling a security breach of a protected set of files

8,209,524 - Cross-architecture optimization
 8,203,609 - Anonymization pursuant to a broadcasted policy
 8,191,140 - Indicating a security breach of a protected set of files
 8,161,232 - Periodically and empirically determined memory refresh intervals
 8,126,938 - Group content substitution in media works
 8,126,190 - Targeted obstrufication of an image
 8,117,654 - Implementation of malware countermeasures in a network device
 8,082,225 - Using destination-dependent criteria to guide data transmission decisions
 8,065,404 - Layering destination-dependent content handling guidance
 8,055,797 - Transmitting aggregated information arising from appnet information
 8,055,732 - Signaling partial service configuration changes in appnets
 8,055,648 - Managing information related to communication
 7,972,557 - Plasmon filter
 7,930,389 - Adaptive filtering of annotated messages or the like
 7,877,584 - Predictive processor resource management
 7,860,887 - Cross-media storage coordination
 7,752,255 - Configuring software agent security remotely
 7,739,524 - Power consumption management
 7,653,834 - Power sparing synchronous apparatus
 7,607,042 - Adjusting a processor operating parameter based on a performance criterion
 7,519,995 - Programmable hardware for deep packet filtering
 7,512,842 - Multi-voltage synchronous systems
 7,493,516 - Hardware-error tolerant computing
 5,793,991 - Method of equalizing loads on a computer bus

Patent Applications

Dr. Mangione-Smith has no known financial interest in any pending US patent applications other than some applications where he is listed as an inventor. The list of such published patent applications where he is a named inventor can be found by searching the online USPTO database or directly accessed via this link:
<http://goo.gl/Uq2q7Q>.

Expert Consultant in IP Matters – Multi-Year Engagements Noted Once

2022

NETLIST, INC, vs. SAMSUNG ELECTRONICS CO., LTD.

Eastern District of Texas, Marshall Division

Civil Action No. 2:21-CV-463-JRG

Engaged on behalf of Netlist, counsel is with Irell & Manella LLP

WSOU Investments, LLC d/b/a Brazos Licensing and Development v. ZTE

CIVIL ACTION 6:20-CV-00487-ADA
CIVIL ACTION 6:20-CV-00488-ADA
CIVIL ACTION 6:20-CV-00489-ADA
CIVIL ACTION 6:20-CV-00490-ADA
CIVIL ACTION 6:20-CV-00491-ADA
CIVIL ACTION 6:20-CV-00492-ADA
CIVIL ACTION 6:20-CV-00493-ADA
CIVIL ACTION 6:20-CV-00494-ADA
CIVIL ACTION 6:20-CV-00495-ADA
CIVIL ACTION 6:20-CV-00496-ADA
CIVIL ACTION 6:20-CV-00497-ADA

Engaged by Kasowitz Benson Torres LLP on behalf of WSOU Investments

WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Google LLC

CIVIL ACTION 6:20-CV-00571-ADA
CIVIL ACTION 6:20-CV-00572-ADA
CIVIL ACTION 6:20-CV-00573-ADA
CIVIL ACTION 6:20-CV-00575-ADA
CIVIL ACTION 6:20-CV-00576-ADA
CIVIL ACTION 6:20-CV-00579-ADA
CIVIL ACTION 6:20-CV-00580-ADA
CIVIL ACTION 6:20-CV-00583-ADA
CIVIL ACTION 6:20-CV-00584-ADA
CIVIL ACTION 6:20-CV-00585-ADA

Engaged by Folio Law Group on behalf of WSOU

Highlands Advisory
IP evaluation

Interdigital
IP evaluation

KONINKLIJKE KPN N.V., v. XIAOMI CORPORATION et al, and COOLPAD
TECHNOLOGIES INC.,
The District of Delaware
C.A. No. 21-cv-41-LPS-CJB and C.A. No. 21-cv-43-LPS-CJB
Engaged on behalf of KPN
Counsel is Sussman & Godfrey
Provided declaration.

WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Microsoft Corp.,
Case No. 6:12-cv-463 (W.D.T.X.)
Engaged by Susman Godfrey on behalf of WSOU Investments
Provided testimony via declaration

KONINKLIJKE KPN N.V., vs. TELEFONAKTIEBOLAGET LM ERICSSON AND
ERICSSON INC.

Case 2:21-cv-113 in the Eastern District of Texas
Engaged by Susman Godfrey LLP on behalf of Koninklijke KPN
Testified via declaration and deposition.

Barkan Wireless IP Holdings, L.P. v. T-Mobile US, Inc., T-Mobile USA, Inc., and Nokia
of America Corp., No. 2:21-cv-00034-JRG (E.D. Tex.)
Engaged on behalf of Barkan by Heim, Payne & Chorush, LLP
Technology relates to communications equipment.
Provided testimony via declaration and deposition.

Intel Corporation v. FG SRC LLC et al.
Engaged on behalf of FG SRC LLC, by DiMuroGinsberg PC
IPR case number IPR2020-01449
Technology relates to reconfigurable computing
Provided testimony via declaration and deposition.

StratosAudio, Inc. v. multiple automotive manufacturers
Engaged on behalf of StratosAudio, Inc by White & Case LLP
Technology relates to accounting for content distribution

2020

Netlist vs. S. K. Hynix
Nos. 6:20-cv-00194-ADA and 6:20-cv-00525-ADA (W.D. Tex.)
Engaged on behalf of Netlist, provided testimony on behalf of Netlist
Technology relates to memory modules

INTEL CORPORATION, Petitioner v. PACT XPP SCHWEIZ AG
Before the Patent Trial and Appeal Board of the US Patent and Trademark Office
Working with Quinn Emanuel Urquhart & Sullivan on behalf of PACT XPP

Digital Video-Capable Devices and Components Thereof, USITC 337-TA-1224
Working with Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C
On behalf of Koninklijke Philips N.V. and Philips North America LLC
Provided sworn testimony

UNILOC 2017, LLC et al. v. GOOGLE LLC
Northern District of California
4:20-cv-04355-YGR
Prince Lobel Tye LLP
Working on behalf of Uniloc

UNILOC 2017, LLC et al. v. GOOGLE LLC
Working with Ethridge Law Group and Carter Arnett on behalf of Uniloc
Eastern District of Texas, Marshall Division
Case No. 2-18-cv-00492-JRG-RSP, filed 2018-11-17
Case No. 2-18-cv-00496-JRG-RSP, 2018-11-17
Case No. 2-18-cv-00499-JRG-RSP, 2018-11-17
Patent consulting thus far, testimony anticipated
INTEL CORPORATION, v. VLSI TECHNOLOGY LLC
IPR2019-01197, Patent 6,212,633
Working with LOWENSTEIN & WEATHERWAX LLP on behalf of VLSI
Provided expert testimony in the form of a declaration and deposition.

Consulting work for Global Foundries related to computer chips.

GPU++, LLC v. Qualcomm Incorporated, et al.,
Working with Steptoe & Johnson on behalf of GPU++
Texas Western District, case 6:19-cv-00474-ADA, filed 2019-08-16
Testimony provided.
Technology relates to graphics processing systems

VLSI Technology v. Intel
Western District of Texas, case 6:19-CV-256
Working with Irell & Manella LLP on behalf of VLSI Technology LLC
Provided testimony in the form of expert reports and depositions.

2019

VLSI Technology LLC v. Intel
District of Delaware, case 1:18-cv-00966
Working with Irell & Manella LLP on behalf of VLSI Technology LLC
Technology relates to semiconductor manufacturing
Patent consulting thus, testimony anticipated

Consulting work for DivX – related to computer video.

2018

INVT SPE LLC v. Apple Inc., HTC Corp. and HTC America, Inc. ZTE Corp. and ZTE (USA) Inc.

Certain LTE- and 3G-Compliant Cellular Communications Devices, Investigation No. 337-TA-1138

Provided Expert Testimony on behalf of INVT
Technology relates to wireless communications

Mahltig Management- und Beteiligungsgesellschaft mbH in patent proceedings relating to European Patent 1 714 229

Adverse to Intel and Lenovo
Technology relates to microprocessors

Netlist vs. S. K. hynix

US ITC 337-TA-1089

Engaged on behalf of Netlist, provided testimony on behalf of Netlist
Technology relates to memory modules

Voip-Pal.com Inc.

Technology relates to VOIP service providers

Voip-Pal.com, Inc. v. Amazon.com, Inc. et al - 2:18-cv-01076

Voip-Pal.com, Inc. v. Apple, Inc. - 2:16-CV-00260

Voip-Pal.com, Inc. v. Apple, Inc. - 2:18-cv-00953

Voip-Pal.com Inc. v. Verizon and AT&T - 2:16-CV-00271

Voip-Pal.com, Inc. v. Twitter - 2:16-CV-02338

2017

AMD v. LG, Vizio, MediaTek and Sigma Designs

US ITC 337-TA-1044

Provided Expert Testimony on behalf of AMD
Technology relates to graphics processing hardware

Netlist vs. S. K. hynix

US ITC 337-TA-1023

Engaged on behalf of Netlist
Provided Expert Testimony via Report, Deposition and at hearing
Technology relates to memory modules

Advanced Micro Devices Inc.

Engaged on behalf of AMD

USPTO Re-Exam Defense

Provided testimony via expert report and interview
Technology relates to microprocessors

Advanced Micro Devices Inc.
Engaged on behalf of AMD
IPR Defense
Provided testimony via expert report for IPR2015-00321
IPR2015-00328 and IPR2015-00321
Technology relates to microprocessors

2016

INTEL CORPORATION v. FUTURE LINK SYSTEMS, LLC - C.A. No. 14-377-LPS
Retained by Irell and Manella LLP on behalf of Future Link Systems, LLC
Technology relates to computer communications systems
Declarations filed on behalf of Future Link Systems, LLC

Voip-Pal.com Inc.
Technology relates to VOIP service providers
Retained to assist during an IPR action
IPR2016-01198 and IPR2016-01201

TiVo Inc. v. Samsung Electronics Co., Ltd., et al., Case No. 2:15-cv-1503 (E.D. Tex.)
Technology relates to digital video recorders
Retained by Irell and Manella LLP on behalf of TiVo Inc.

Rosetta-Wireless Corporation Inter Partes Reviews Nos. IPR2016-00616 and
IPR2016-00622
Technology relates to personal communications and computing devices. Retained
by Heim, Payne and Chorush on behalf of Rosetta-Wireless Declaration filed.

Innovative Memory Solutions, Inc. (IMS) v. Micron Technology
District of Delaware - 14-cv-01480-RGA
Engaged by IMS via Cohen & Grace, LLC
Technology relates to semiconductor memory manufacturing

Zak v. Facebook
Eastern District of Michigan - 4:15-cv-13437
Engaged by Zak via Harness, Dickey & Pierce PLC
Technology relates to client-server software Declaration
filed.

2015

Advanced Silicon Technologies, LLC Delaware District Court and at the ITC (No matter
number assigned)

Technology relates to programmable processor hardware Accused parties:

Texas Instruments Incorporated 1:15-cv-01175
NVIDIA Corporation 1:15-cv-01177
Renesas Electronics Corporation et al. 1:15-cv-01176
Fujitsu Ten Limited et al. 1:15-cv-01174
Bayerische Motoren Werke AG et al. 1:15-cv-01178
VOLKSWAGEN AG 1:15-cv-01181
Harmon International Industries Incorporated et al. 1:15-cv-01173
Honda Motor Co., Ltd. et al. 1:15-cv-01179
Toyota Motor Corporation 1:15-cv-01180

FlatWorld Interactives LLC v. Samsung and LG
C.A. No. 12-804-LPS and C.A. No. 12-964-LPS
Engaged on behalf of FlatWorld
Technology relates to user interface design

Ericsson Inc. vs. Apple Inc.
EDTX 2:15-cv-290 and 2:15-cv-292
Engaged on behalf of Ericsson
Technology relates to peripheral devices

Synaptics vs. Goodix
US ITC 337-TA-957
Engaged on behalf of Goodix
Provided Expert Testimony via Report, Deposition and at hearing
Technology relates to touch screens

Advanced Micro Devices Inc.
Engaged on behalf of AMD
IPR Defense
Provided testimony via expert report
Technology relates to digital video
IPR2015-00328 and IPR2015-00321

Solocron Media LLC v. Verizon Communications, Inc., Cellco Partnership d/b/a/
Verizon Wireless, AT&T Mobility LLC, T-Mobile USA, Inc., and Sprint Spectrum L.P.
The Eastern District of TX, Case 2:13-cv-1059-JRG
Retained by tensegrity on behalf of Solocron
Technology relates to MMS and multi-media transcoding.
Prepared expert reports on infringement.

Enterprise Systems Technologies S.a.r.l v. Apple Inc., Cirrus Logic Inc., HTC

Corporation, LG Electronics, Inc., Samsung Electronics Co
The International Trade Commission of the United States of America
Inv. No. 337-TA-924
Retained by Mintz, Levin, Cohn, Ferris, Glovsky and Popeo LLP for complainant.
Technology relates to device drivers. Prepared
expert reports and deposed.

Ziilabs Inc., LTD., v. Samsung and Apple
Case 2:14-cv-00203 In the Eastern District of Texas Marshall Division
Retained by Davis of Heim, Payne & Chorush, L.L.P. for Ziilabs Technology
relates to graphics systems.
Provided expert report on infringement as well as deposition testimony.

Packet Intelligence LLC v. Cisco
Case 2:2014cv00252 In the Eastern District of Texas Marshall Division
Retained by Heim, Payne & Chorush, L.L.P. for Packet Intelligence Technology
relates to secure networking.

Advanced Micro Devices, Inc. v. LG Corp., et al.
5:14-cv-01012 U.S. District Court for the Northern District of California Retained
by Robins, Kaplan, Miller & Ciresi LLP on behalf of Advanced Micro Devices,
Inc.
Technology relates to microprocessors and multimedia.

dunnhumby USA, LLC, et al. v. emnos USA Corp.
U.S. District Court for the Northern District of Illinois
Case No.: 1:13-cv-00399
Retained by Baker Hostetler who represents dunnhumby Technology
relates to databases.

Parthenon Unified Memory Architecture LLC, v. HTC CORPORATION and HTC
AMERICA, INC., LG ELECTRONICS, INC. and LG ELECTRONICS USA, INC.
Case No. 2:14-cv-690-JRG-RSP
Case No. 2:14-cv-691-JRG-RSP
Eastern District of Texas, Marshall Division Technology
relates to multimedia systems.
Retained on behalf of Parthenon

Parthenon Unified Memory Architecture LLC, v. SAMSUNG ELECTRONICS CO.,
LTD., ET AL. HUAWEI TECHNOLOGIES CO. LTD, HUAWEI TECHNOLOGIES
USA, INC. and HUAWEI DEVICE USA, INC. and MOTOROLA MOBILITY LLC
Case No. 2:14-cv-902-RSP
Case No. 2:14-cv-687-JRG-RSP

Case No. 2:14-cv-689-JRG-RSP
Eastern District of Texas, Marshall Division Technology
relates to multimedia systems.
Retained on behalf of Parthenon

NEXUS DISPLAY TECHNOLOGIES LLC, Plaintiff, v. DELL INC., LENOVO
(UNITED STATES) INC., PANASONIC CORP. OF NORTH AMERICA, EIZO CORP.
AND
EIZO INC., NEC CORP. AND NEC DISPLAY SOLUTIONS OF AMERICA, INC.
Civil Action No: 2:14-cv-00762
Civil Action No: 2:14-cv-00762
Civil Action No. 2:14-cv-00763
Civil Action No. 2:14-cv-00764
Civil Action No. 2:14-cv-00765
Technology relates to communications circuits.
Retained on behalf of Nexus Display Technologies

INTEL CORPORATION, v. FUTURE LINK SYSTEMS, LLC
C.A. No. 1:14-CV-00377-LPS
District Court for Delaware
Technology relates to communications circuits.
Retained on behalf of Future Link Systems

2014

Content Guard v. Apple Inc., Amazon.com Inc., BlackBerry Corporation, Huawei Device
USA, Inc., Motorola Mobility LLC, BlackBerry Limited, HTC Corporation, HTC
America, Inc., Huawei Technologies Co., Ltd., Samsung Electronics Co., Ltd., Samsung
Electronics America, Inc., and Samsung Telecommunications America, LLC
The Eastern District of TX, case 2:13-cv-01112-JRG
Retained by McKool Smith on behalf of Content Guard
Technology relates to digital right management.

Content Guard v. Google Inc.
The Eastern District of TX, Case 2:14-cv-00061-JRG Retained
by McKool Smith on behalf of Content Guard Technology
relates to digital right management.

Solocron Media LLC v. Verizon Communications, Inc., Cellco Partnership d/b/a/
Verizon Wireless, AT&T Mobility LLC, T-Mobile USA, Inc., and Sprint Spectrum L.P.
The Eastern District of TX, Case 2:13-cv-1059-JRG
Retained by tensegrity on behalf of Solocron
Technology relates to MMS and multi-media transcoding.

Enterprise Systems Technologies S.a.r.l v. Apple Inc., Cirrus Logic Inc., HTC Corporation, LG Electronics, Inc., Samsung Electronics Co
The International Trade Commission of the United States of America
Inv. No. 337-TA-924
Retained by Mintz, Levin, Cohn, Ferris, Glovsky and Popeo LLP for complainant.
Technology relates to device drivers.

Ziilabs Inc., LTD., v. Samsung and Apple
Case 2:14-cv-00203 In the Eastern District of Texas Marshall Division
Retained by Davis of Heim, Payne & Chorush, L.L.P. for Ziilabs Technology
relates to graphics systems.

Packet Intelligence LLC v. Cisco
Case 2:2014cv00252 In the Eastern District of Texas Marshall Division
Retained by Heim, Payne & Chorush, L.L.P. for Packet Intelligence Technology
relates to secure networking.

Rockstar Consortium US v. Asustek, Google, HTC, LGE, Pantech, Samsung and ZTE
2:13-cv-00899 In the Eastern District of Texas Marshall Division
Retained by McKool Smith for Rockstar
Technology relates to user interfaces and messaging.

Advanced Micro Devices, Inc. v. LG Corp., et al.
5:14-cv-01012 U.S. District Court for the Northern District of California Retained
by Robins, Kaplan, Miller & Ciresi LLP on behalf of Advanced Micro Devices,
Inc.
Technology relates to microprocessors and multimedia.

Pragmatus Mobile LLC v. Samsung Electronics Co. Ltd, etc.
U.S. ITC Inv. No. 337-TA-905
Retained by Flagship IP. P.C. on behalf of Complainant Pragmatus Mobile LLC
Technology relates to converged devices.

CallCopy Inc.
Assistance with Reexamination efforts related to Verint Americas Inc.
Retained by Baker Hostetler
Technology related to call systems and call center management. Submitted
declarations with the USPTO.

dunnhumby USA, LLC, et al. v. emnos USA Corp.
U.S. District Court for the Northern District of Illinois
Case No.: 1:13-cv-00399

Retained by Baker Hostetler who represents dunnhumby Technology
relates to database technology.

Graphics Properties Holdings, v. Panasonic et al.

ITC Inv. No. 337-TA-884

Retained by Mintz, Levin, Cohn, Ferris, Glovsky and Popeo LLP for complainant.

Provided testimony through expert reports, deposition and at trial. Technology
relates to graphics hardware.

2013

Graphics Properties Holdings, v. Panasonic et al.

ITC Inv. No. 337-TA-884

Retained by Mintz, Levin, Cohn, Ferris, Glovsky and Popeo LLP for complainant.

Provided testimony through expert reports and deposition. Technology
relates to graphics hardware.

CallCopy Inc.

Assistance with Reexamination efforts related to Verint Americas Inc.

Retained by Hahn Loeser & Parks LLP

Technology related to call systems and call center management. Submitted
declarations with the USPTO.

dunnhumby USA, LLC, et al. v. emnos USA Corp.

U.S. District Court for the Northern District of Illinois

Case No.: 1:13-cv-00399

Retained by Baker Hostetler who represents dunnhumby Technology
relates to database technology.

Microline, LLC v. INTEL CORPORATION, ACER, INC., ACER AMERICA
CORPORATION, ADVANCED MICRO DEVICES, INC., APPLE, INC., DELL, INC.,
GATEWAY, INC., HEWLETT-PACKARD COMPANY, LENOVO GROUP, LTD,
LENOVO (UNITED STATES), INC., NVIDIA CORPORATION, SONY COMPUTER
ENTERTAINMENT AMERICA INC., TOSHIBA CORPORATION, TOSHIBA
AMERICA INC., and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.

Eastern District of Texas

Retained by Eugene M. Cummings, P.C.

Submitted reports regarding infringement, invalidity and claim construction along with
numerous declarations. Appeared at the Markman hearing. Deposed. Technology
relates to microprocessor communications.

FlashPoint Technology, Inc. v. HTC Corporation, HTC America, Inc., Pantech Co., Ltd.,
Pantech Wireless, Inc., Huawei Technologies Co., Ltd., FutureWei Technologies, Inc. d/b/a
Huawei Technologies (USA), ZTE Corporation, ZTE (USA) Inc.,

USA International Trade Commission
Certain Electronic Imaging Devices, Inv. No. 337-TA-850
Expert for FlashPoint, who is represented by Pepper Hamilton, LLP.
Submitted reports numerous declarations. Testified at the ITC. Deposed. Technology relates to converged devices.

2012

FlashPoint Technology, Inc. v. HTC Corporation, HTC America, Inc., Pantech Co., Ltd., Pantech Wireless, Inc., Huawei Technologies Co., Ltd., FutureWei Technologies, Inc. d/b/a Huawei Technologies (USA), ZTE Corporation, ZTE (USA) Inc.,
USA International Trade Commission
Certain Electronic Imaging Devices, Inv. No. 337-TA-850
Expert for FlashPoint, who is represented by Pepper Hamilton, LLP.
Submitted reports numerous declarations. Testified at the ITC. Deposed. Technology relates to converged devices.

Graphics Properties Holdings v. HTC et. al.
Graphics Properties Holdings v. LG Electronics et. al.
Graphics Properties Holdings v. Sony et. al.
Graphics Properties Holdings v. Samsung Electronics et. al.
Graphics Properties Holdings v. Apple
Graphics Properties Holdings v. Research In Motion et. al.
United States District Court for the District of Delaware
Testifying expert witness for GPH on matters related to invalidity.
Pepper Hamilton LLP and Mintz, Levin, Cohn, Ferris, Glovsky and Popeo LLP represent plaintiffs.
Subject matter relates to graphics systems and CPU microarchitecture. Submitted reports numerous declarations. Deposed.

IPValue
Non-litigation related patent evaluation services.

TV Interactive Data Corporation v. Sony Corporation, Sony Computer Entertainment Inc, Sony Computer Entertainment America Inc, Sony Corporation of America, Sony Electronics Inc, Samsung Electronics Co Ltd, Samsung Electronics America Inc, Royal Philips Electronics NV, Philips Electronics North America Corporation, Toshiba Corporation, Toshiba America Inc., Toshiba America Consumer Products LLC, Panasonic Corporation, Panasonic Corporation of North America, Victor Company of Japan, LTD, JVC Americas Corp, LG Electronics Inc, LG Electronics USA Inc., Zenith Electronics LLC, Pioneer Corporation, Pioneer Electronics (USA) Inc., Sharp Corporation, Sharp Electronics Corporation, Funai Electric Co., Ltd., Funai Corporation, Inc., D&M Holdings Inc., D&M Holdings US Inc. and Denon Electronics

(USA), LLC

United States District Court for the Northern District of California Case
5:2010cv00475

Consultant for defendant Funai

Defendants Funai Electric Co. Ltd. and Funai Corporation, Inc. are represented by Kevin
W. Kirsch, David A. Mancino, John F. Bennett, Matthew P. Hayden, and Hayes F.

Michel of Baker Hostetler

Subject matter relates to DVDs and computer Operating Systems.

*Interval Licensing LLC, v. AOL, Inc.,; Apple, Inc.; eBay, Inc.; Facebook, Inc.; Netflix,
Inc.; Office depot, Inc.; Officemax, Inc.; Staples, Inc.; Yahoo! Inc.; and Youtube, LLC.*

United States District Court for the Western District of Washington Case 2:10-cv-01385

Consultant for Interval Licensing LLC

Technology relates to user interfaces and data organization.

Interval Licensing LLC is represented by Michael F. Heim, Eric J. Enger, and Nathan J.
Davis of Heim, Payne & Chorush, L.L.P.

Subject matter relates to online search, advertising and data presentation.

Submitted declarations related to claim construction. Deposed. Technology
relates to user interfaces and data organization.

*St. Clair Intellectual Property Consultants, Inc. v. Acer, Inc., Acer America Corporation,
Dell Inc., Gateway Companies, Inc., Gateway, Inc., Lenovo Group, Limited and Lenovo
(United States) Inc.*

United States District Court for the District of Delaware - 1:2009cv00354

Consultant for St. Clair Intellectual Property Consultants

St. Clair is represented by R. Terrance Rader, Charles W. Bradley, Glenn E. Forbis, and
Justin S. Cohen of Rader Fishman & Grauer PLLC

Subject matter relates to power management and graphics hardware.

Filed reports regarding validity and infringement and provided deposition testimony.

*ST. CLAIR INTELLECTUAL PROPERTY CONSULTANTS, INC., v. APPLE, INC. HIGH
TECH COMPUTER CORP., a/k/a HTC CORP., HTC (B.V.I.), HTC AMERICA, INC.,
EXEDEA, INC., RESEARCH IN MOTION LTD., and RESEARCH IN MOTION
CORPORATION*

United States District Court for the District of Delaware - 1:10-cv-00982-LPS

Consultant for St. Clair Intellectual Property Consultants

St. Clair is represented by R. Terrance Rader, Charles W. Bradley, Glenn E. Forbis, and
Justin S. Cohen of Rader Fishman & Grauer PLLC Filed a declaration.

Subject matter relates to cameras and messaging.

Red Chalk Group

Subject matter relates to patent analysis.

Siemens

Subject matter relates to patent analysis.

Phoenix Technologies

Subject matter relates to patent analysis.

2011

TV Interactive Data Corporation v. Sony Corporation, Sony Computer Entertainment Inc, Sony Computer Entertainment America Inc, Sony Corporation of America, Sony Electronics Inc, Samsung Electronics Co Ltd, Samsung Electronics America Inc, Royal Philips Electronics NV, Philips Electronics North America Corporation, Toshiba Corporation, Toshiba America Inc., Toshiba America Consumer Products LLC, Panasonic Corporation, Panasonic Corporation of North America, Victor Company of Japan, LTD, JVC Americas Corp, LG Electronics Inc, LG Electronics USA Inc., Zenith Electronics LLC, Pioneer Corporation, Pioneer Electronics (USA) Inc., Sharp Corporation, Sharp Electronics Corporation, Funai Electric Co., Ltd., Funai Corporation, Inc., D&M Holdings Inc., D&M Holdings US Inc. and Denon Electronics (USA), LLC

United States District Court for the Northern District of California

Case 5:2010cv00475

Consultant for defendant Funai

Defendants Funai Electric Co. Ltd. and Funai Corporation, Inc. are represented by Kevin W. Kirsch, David A. Mancino, John F. Bennett, Matthew P. Hayden, and Hayes F.

Michel of Baker Hostetler

Subject matter relates to DVDs and computer Operating Systems.

Interval Licensing LLC, v. AOL, Inc.,; Apple, Inc.; eBay, Inc.; Facebook, Inc.; Netflix, Inc.; Office depot, Inc.; Officemax, Inc.; Staples, Inc.; Yahoo! Inc.; and Youtube, LLC.

United States District Court for the Western District of Washington Case 2:10-cv-01385

Consultant for Interval Licensing LLC

Interval Licensing LLC is represented by Michael F. Heim, Eric J. Enger, and Nathan J.

Davis of Heim, Payne & Chorush, L.L.P.

Subject matter relates to online search, advertising and data presentation.

St. Clair Intellectual Property Consultants, Inc. v. Acer, Inc., Acer America Corporation, Dell Inc., Gateway Companies, Inc., Gateway, Inc., Lenovo Group, Limited and Lenovo (United States) Inc.

United States District Court for the District of Delaware - 1:2009cv00354

Consultant for St. Clair Intellectual Property Consultants

St. Clair is represented by R. Terrance Rader, Charles W. Bradley, Glenn E. Forbis, and Justin S. Cohen of Rader Fishman & Grauer PLLC Technology relates to power management.

ST. CLAIR INTELLECTUAL PROPERTY CONSULTANTS, INC., v. APPLE, INC. HIGH TECH COMPUTER CORP., a/k/a HTC CORP., HTC (B.V.I.), HTC AMERICA, INC., EXEDEA, INC., RESEARCH IN MOTION LTD., and RESEARCH IN MOTION CORPORATION

United States District Court for the District of Delaware - 1:10-cv-00982-LPS

Consultant for St. Clair Intellectual Property Consultants

St. Clair is represented by R. Terrance Rader, Charles W. Bradley, Glenn E. Forbis, and Justin S. Cohen of Rader Fishman & Grauer PLLC Filed a declaration.

Subject matter relates to power management and graphics hardware.

Negotiated Data Solutions

Consultant for Negotiated Data Solutions

Negotiated Data Solutions is represented by Susman, Godfrey LLP. Subject matter relates to IO devices.

Acqis LLC

Declarations filed with USPTO in response to a series of reexamination requests.

Deposed in a related case (Texas Eastern District Court 6:2009cv00148) as a consequence of declarations.

Acqis LLC is represented by Cooley, Godward, Kronish LLP Subject matter relates to computer systems.

FlashPoint Technology, Inc. v. Nokia Corp. of Finland, Nokia, Inc. of Irving, Texas, Research In Motion Ltd. of Canada, Research In Motion Corp. of Irving, Texas, HTC Corp. of Taiwan, HTC America, Inc. of Bellevue, Washington, LG Electronics of South Korea, LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey, and LG Electronics MobileComm U.S.A., Inc. of San Diego, California

US ITC Inv. No. 337-TA-726

Consultant for FlashPoint Technology, Inc.

FlashPoint Technology Inc. is represented by William D. Belanger, Gregory D. Len, and Frank Liu of Pepper Hamilton LLP.

Filed reports regarding validity and infringement and provided testimony both via deposition and in court.

Subject matter relates to camera systems.

MicroUnity, Inc. v. Texas Instruments Inc., Qualcomm, Inc., Samsung Electronics Co LTD, Motorola, Inc., Nokia Corporation, Palm, Inc., Samsung TeleCommunications America, LLC, Acer, Inc., HTC Corporation, Google Inc., LG Electronics Inc, Apple, Inc., Cellco Partnership d/b/a Verizon Wireless, Sprint Nextel Corporation and AT&T
2:2010cv00091

Consultant for MicroUnity, Inc.

Eastern District of Texas

MicroUnity, Inc., is represented by Heim, Payne, and Chorush LLP. Subject matter relates to graphics hardware and microarchitecture.

2010

TV Interactive Data Corporation v. Sony Corporation, Sony Computer Entertainment Inc, Sony Computer Entertainment America Inc, Sony Corporation of America, Sony Electronics Inc, Samsung Electronics Co Ltd, Samsung Electronics America Inc, Royal Philips Electronics NV, Philips Electronics North America Corporation, Toshiba Corporation, Toshiba America Inc., Toshiba America Consumer Products LLC, Panasonic Corporation, Panasonic Corporation of North America, Victor Company of Japan, LTD, JVC Americas Corp, LG Electronics Inc, LG Electronics USA Inc., Zenith Electronics LLC, Pioneer Corporation, Pioneer Electronics (USA) Inc., Sharp Corporation, Sharp Electronics Corporation, Funai Electric Co., Ltd., Funai Corporation, Inc., D&M Holdings Inc., D&M Holdings US Inc. and Denon Electronics (USA), LLC

United States District Court for the Northern District of California

Case 5:2010cv00475

Consultant for defendant Funai

Defendants Funai Electric Co. Ltd. and Funai Corporation, Inc. are represented by Kevin W. Kirsch, David A. Mancino, John F. Bennett, Matthew P. Hayden, and Hayes F.

Michel of Baker Hostetler

Subject matter relates to DVDs and computer Operating Systems.

Interval Licensing LLC, v. AOL, Inc.,; Apple, Inc.; eBay, Inc.; Facebook, Inc.; Netflix, Inc.; Office depot, Inc.; Officemax, Inc.; Staples, Inc.; Yahoo! Inc.; and Youtube, LLC.

United States District Court for the Western District of Washington Case 2:10-cv-01385

Consultant for Interval Licensing LLC

Interval Licensing LLC is represented by Michael F. Heim, Eric J. Enger, and Nathan J. Davis of Heim, Payne & Chorush, L.L.P.

Subject matter relates to online search, advertising and data presentation.

St. Clair Intellectual Property Consultants, Inc. v. Acer, Inc., Acer America Corporation, Dell Inc., Gateway Companies, Inc., Gateway, Inc., Lenovo Group, Limited and Lenovo (United States) Inc.

United States District Court for the District of Delaware - 1:2009cv00354

Consultant for St. Clair Intellectual Property Consultants

St. Clair is represented by R. Terrance Rader, Charles W. Bradley, Glenn E. Forbis, and Justin S. Cohen of Rader Fishman & Grauer PLLC

Subject matter relates to power management and graphics hardware.

Negotiated Data Solutions

Consultant for Negotiated Data Solutions

Negotiated Data Solutions is represented by Susman, Godfrey LLP. Subject matter relates to IO devices.

Acqis LLC

Declarations filed with USPTO in response to a series of reexamination requests. Deposed in a related case (Texas Eastern District Court 6:2009cv00148) as a consequence of declarations.

Acqis LLC is represented by Cooley, Godward, Kronish LLP Subject matter relates to computer systems.

FlashPoint Technology, Inc. v. Nokia Corp. of Finland, Nokia, Inc. of Irving, Texas, Research In Motion Ltd. of Canada, Research In Motion Corp. of Irving, Texas, HTC Corp. of Taiwan, HTC America, Inc. of Bellevue, Washington, LG Electronics of South Korea, LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey, and LG Electronics MobileComm U.S.A., Inc. of San Diego, California

US ITC Inv. No. 337-TA-726

Consultant for FlashPoint Technology, Inc.

FlashPoint Technology Inc. is represented by William D. Belanger, Gregory D. Len, and Frank Liu of Pepper Hamilton LLP.

Subject matter relates to camera systems.

Filed reports regarding validity and infringement and provided testimony both via deposition and in court.

MicroUnity, Inc. v. Texas Instruments Inc., Qualcomm, Inc., Samsung Electronics Co LTD, Motorola, Inc., Nokia Corporation, Palm, Inc., Samsung TeleCommunications America, LLC, Acer, Inc., HTC Corporation, Google Inc., LG Electronics Inc, Apple, Inc., Cellco Partnership d/b/a Verizon Wireless, Sprint Nextel Corporation and AT&T 2:2010cv00091

Consultant for MicroUnity, Inc.

Eastern District of Texas

MicroUnity, Inc., is represented by Heim, Payne, and Chorush LLP. Subject matter relates to graphics hardware and microarchitecture.

Saxon Innovations, LLC v. Apple, Inc., Gateway, Inc., Gateway Companies, Inc., Acer America Corp., Acer, Inc., Hewlett-Packard Co. and Dell, Inc

Eastern District of Texas 6:2008cv00265

Consultant for Saxon Innovations, LLC

Representing Saxon Innovations, LLC, who was represented by Heim, Payne, and Chorush LLP.

Subject matter relates to multiprocessors systems and computer systems. Filed reports regarding validity and infringement and provided testimony both via deposition and in court.

Joel M. Geddis and Shaun Legacy v. Microsoft Corporation, Toshiba Corporation, Freescale Semiconductor, Inc., Wolfson Microelectronics, Inc., Wolfson Microelectronics PLC

Superior Court of Washington in and for King County 08-2-40731-4 SEA

Consultant for Toshiba Corporation

Toshiba Corporation is represented by Forsberg & Umlauf, P.S. Subject matter relates to portable audio devices.

2009

Saxon Innovations, LLC v. LG Electronics Inc., LG Electronics USA Inc., LG Electronics Mobilecomm U.S.A., Inc., Samsung Electronics Co. Ltd, Samsung Electronics America Inc., Samsung Telecommunications America LLC, Palm Incorporated, Research in Motion Ltd, Research In Motion Corporation, Nintendo Co. Ltd, and Nintendo of America

Eastern District of Texas 6:07-CV-490

Prepared expert report regarding invalidity on behalf of Saxon Innovations, LLC.

Saxon Innovations, LLC, was represented by Pepper Hamilton LLP.

Subject matter relates to multiprocessors systems and computer systems. Filed reports regarding validity and infringement and provided testimony both via deposition and in court.

Saxon Innovations, LLC, v. Nokia Corp., Research In Motion Ltd., High Tech Computer Corp., Palm, Inc., Panasonic Corporation, US

ITC 337-TA-667

Expert witness for Saxon Innovations, LLC.

Submitted reports, was deposed, and testified at trial regarding claim construction and invalidity.

Saxon Innovations, LLC was represented by William D. Belanger, Aaron J. Levangie, Gregory D. Len, and Charles H. Carpenter of Pepper Hamilton LLP.

Subject matter relates to multiprocessors systems and computer systems.

Advanced Micro Devices, Inc. v. Samsung Electronics Co, Ltd.

U.S. District Court for the Northern District of California 3:08-cv-00986-SI Consultant for Advanced Micro Devices, Inc. Reverse engineering efforts to support infringement contentions.

Advanced Micro Devices, Inc is represented by Robins, Kaplan, Miller and Ciresi LLP. Subject matter relates to memory devices.

Intellectual Ventures

Subject matter relates to patent analysis.

2005

Speedera Networks, Inc., v. Akamai Technologies, Inc.

U.S. District Court for the Northern District of California 5:02-cv-03050-JW Consultant for Speedera Networks, Inc.
Reviewed depositions and provided review of computer security.
Speedera Networks, Inc. was represented by Jim Bowman of O'Melveny & Myers LLP.
Technology related to computer security.

Research in Motion Limited et al. v. Inpro II Licensing SARL
U.S. District Court for the Northern District of Texas 3:03-cv-02669-B Consultant for InPro II Licensing SARL . Provided patent analysis.
InPro II Licensing SARL was represented by Dechert. Technology related to IO devices.

Digi International, Inc. v. Lantronix, Inc., 0:04-cv-01560-DWF-SRN U.S. District Court for the District of Minnesota
Consultant for Lantronix, Inc. Prepared expert reports.
Lantronix, Inc. was represented by Stradling Yocca Carlson & Rauth. Technology related to IO devices.

2004

Intergraph Hardware Technologies Company, Inc v. Hewlett-Packard
U.S. District Court for the Eastern District of Texas *Company*6:04-cv-00214-LED
Expert for Intergraph Hardware Technologies Company, Inc. Prepared expert reports and claim charts.
Intergraph represented by McDermott, Will and Emery LLP. Technology related to computer communications.

Mentor Graphics
Provided licensing support and IP valuation.
Technology related to emulation.

Veterinary Imaging Centers, Inc. v. Sound Technologies, Inc., et al., 1:02-cv-00282-DCN
U.S. District Court for the Northern District of Ohio
Consultant for Sound Technologies, Inc. Prepared expert reports. Technology related to computer communication.

Interealty Corp. v. Superlative, Inc., et al., 8:01-cv-00969-AHS-AN
U.S. District Court for the Central District of California
Consultant for Superlative, Inc. Matter involved software copyright. Prepared expert reports and was deposed.
Superlative, Inc. was represented by Edward F. O'Connor with the law firm of Levin & O'Connor.
Technology related to databases.

All Computers, Inc. v. Intel Corporation, 1:04-cv-00586-GBL-LO
U.S. District Court for the Eastern District of Virginia
Consultant for All Computers, Inc. Filed numerous expert reports. Deposed by Ruffin Cordell of Fish & Richardson.
Plaintiff was represented by Edward F. O'Connor with the law firm of Levin & O'Connor.
Technology related to microprocessors.

2001

Ikos Systems, Inc. v. Axis Systems, Inc., 5:01-cv-21079-JW
U.S. District Court for the Northern District of California
Filed numerous expert reports. Deposed by Ikos Counsel. Presented tutorial to Judge Ware. Deposed.
Axis Systems, Inc. was represented by George Riley of O'Melveny and Myers
Technology related to emulation.

Professional Activities

Member of ACM and IEEE
Program Chair 26'th International Symposium on Microarchitecture
General Chair 36'th International Symposium on Microarchitecture
Associate Editor of IEEE Transactions on Computers
Associate Editor of ACM Transactions on Embedded Computing Systems
Associate Editor of IEEE Computer
Program Committees: ISCA, MICRO, ISLPED, Network Processors Workshop, FPL, Complexity-Effective Design, RAW, Workshop on Mediaprocessors and DSP, FPT, INTERACT

Publications

Journal

1. W. H. Mangione-Smith, T.-P. Shih, S. G. Abraham, and E. S. Davidson, "Approaching a Machine-Application Bound in Delivered Performance on Scientific Codes," *Proceedings of the IEEE*, vol. 81, pp. 1166-1178, 1993.
2. C. Chien, S. Nazareth, P. Lettieri, S. Molloy, B. Schoner, W. A. I. Boring, J. Chen, C. Deng, W. H. Mangione-Smith, and R. Jain, "An Integrated Testbed for Wireless Multimedia Computing," *Journal of VLSI Signal Processing*, vol. 13, pp. 105-24, 1996.
3. K.-G. Chia, H. J. Kim, S. Lansing, W. H. Mangione-Smith, and J. Villasenor, "High Performance Automatic Target Recognition through Data-Specific VLSI," *IEEE Transactions on VLSI*, vol. 6, pp. 364-372, 1998.

4. N. R. Shnidman, W. H. Mangione-Smith, and M. Potkonjak, "On-line Fault Detection for Bus-Based Field Programmable Gate Arrays," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 6, pp. 656-66, 1998.
5. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Low Overhead Fault-Tolerant FPGA Systems," *IEEE Transactions on Very Large Scale Integration*, pp. 212-21, 1998.
6. D. Kirovski, C. Lee, M. Potkonjak, and W. H. Mangione-Smith, "Application-Driven Synthesis of Memory-Intensive Systems-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, pp. 1316-1326, 1999.
7. W. H. Mangione-Smith, "Technical Challenges for Designing Personal Digital Assistants," *Design Automation for Embedded Systems*, vol. 4, pp. 23-39, 1999.
8. D. Kirovski, J. Kin, and W. H. Mangione-Smith, "Procedure Based Program Compression," *International Journal of Parallel Programming*, vol. 27, pp. 457-475, 1999.
9. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Enhanced FPGA Reliability through Efficient Run-Time Fault Reconfiguration," *IEEE Transactions on Reliability*, vol. 49, pp. 296-304, 2000.
10. B. Kahng, J. Lach, W. H. Mangione-Smith, S. Mantik, I. L. Markov, M. Potkonjak, P. Tucker, H. Wang, and G. Wolfe, "Constraint-based Watermarking Techniques for Design IP Protection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, pp. 1236-52, 2001.
11. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Fingerprinting Techniques for Field Programmable Gate Array Intellectual Property Protection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, pp. 1253-61, 2001.
12. C. Lee, J. Kin, M. Potkonjak, and W. H. Mangione-Smith, "Exploring Hypermedia Processor Design Space," *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, vol. 27, pp. 171-186, 2001.
13. J. Kin, C. Lee, W. H. Mangione-Smith, and M. Potkonjak, "Exploring the Diversity of Multimedia Systems," *IEEE Transactions on VLSI Systems*, vol. 9, pp. 474-485, 2001.
14. J. Kin, M. Gupta, and W. H. Mangione-Smith, "Filtering Memory References to Increase Energy Efficiency," *IEEE Transactions on Computers*, vol. 49, pp. 1-15, 2002.
15. G. Memik and W. H. Mangione-Smith, "Precise Instruction Scheduling", *To Appear in the Journal of Instruction-Level Parallelism*, 2005.

Conference

1. T. Conte and W. Mangione-Smith, "Determining Cost-Effective Multiple Issue Processor Designs," presented at International Conference on Computer Design, 1993.
2. W. H. Mangione-Smith, S. G. Abraham, and E. S. Davidson, "The Effects of Memory Latency and Fine-Grain Parallelism on Astronautics ZS-1 Performance," presented at Twenty-Third Hawaii International Conference on System Sciences, 1990.

3. W. H. Mangione-Smith, S. G. Abraham, and E. S. Davidson, "Architectural vs. Delivered Performance of the IBM RS/6000 and the Astronautics ZS-1," presented at Twenty-Fourth Hawaii International Conference on System Sciences, 1991.
4. W. H. Mangione-Smith, S. G. Abraham, and E. S. Davidson, "Vector Register Design for Polycyclic Vector Scheduling," presented at Fourth Conference on Architectural Support for Programming Languages and Operating Systems, 1991.
5. W. Mangione-Smith, S. G. Abraham, and E. S. Davidson, "Register Requirements of Pipelined Processors," presented at International Conference on Supercomputing, 1992.
6. W. H. Mangione-Smith and B. Hutchings, "Configurable Computing: The Road Ahead," presented at Reconfigurable Architectures Workshop, Geneva, 1997.
7. J. Kin, C. Lee, W. H. Mangione-Smith, and M. Potkonjak, "Hypermedia Processors: Design Space Exploration," presented at Multi-Media Signal Processing Conference, 1998.
8. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Fingerprinting Digital Circuits on Programmable Hardware," presented at Second International Workshop on Information Hiding, 1998.
9. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Signature Hiding Techniques for FPGA Intellectual Property Protection," presented at IEEE/ACM International Conference on Computer-Aided Design, 1998.
10. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "FPGA Fingerprinting Techniques for Protecting Intellectual Property," presented at Custom Integrated Circuits Conference, 1998.
11. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Efficiently Supporting FaultTolerance in FPGAs," presented at International Symposium on Field Programmable Gate Arrays, 1998.
12. W. Mangione-Smith, "Configurable Computing: Concepts and Issues," presented at Thirtieth Hawaii International Conference on System Sciences, 1997.
13. J. Villasenor, B. Schoner, C. Kang-Ngee, C. Zapata, K. Hea Joung, C. Jones, S. Lansing, and B. Mangione-Smith, "Configurable Computing Solutions for Automatic Target Recognition," presented at FPGAs for Custom Computing Machines, 1996.
14. B. Mangione-Smith, "Low Power Communications Protocols: Paging and Beyond," presented at IEEE Symposium on Low Power Electronics, 1995.
15. H. J. Kim, W. H. Mangione-Smith, and M. Potkonjak, "Protecting Ownership Rights of a Lossless Image Coder through Hierarchical Watermarking," presented at IEEE Workshop on Signal Processing Systems, 1998.
16. B. Kahng, J. Lach, W. H. Mangione-Smith, S. Mantik, I. L. Markov, M. Potkonjak, P. Tucker, H. Wang, and G. Wolfe, "Watermarking Techniques for Intellectual Property Protection," presented at Design and Automation Conference, 1998.
17. Rashid, J. Leonard, and W. H. Mangione-Smith, "Dynamic Circuit Generation for Solving Specific Problem Instances of Boolean Satisfiability," presented at FPGAs for Custom Computing Machines, 1998.
18. D. Kirovski, C. Lee, M. Potkonjak, and W. Mangione-Smith, "Synthesis of Power Efficient Systems-on-Silicon," presented at Asia and South Pacific Design Automation Conference, 1998.

19. J. Leonard and W. H. Mangione-Smith, "A Case Study of Partially Evaluated Hardware Circuits: Key-Specific DES," presented at Field-Programmable Logic and Applications, 1997.
20. N. R. Shnidman, W. H. Mangione-Smith, and M. Potkonjak, "Fault Scanner for Reconfigurable Logic," presented at Advanced Research in VLSI, 1997.
21. J. Kin, M. Gupta, and W. H. Mangione-Smith, "The Filter Cache: an Energy Efficient Memory Structure," presented at International Symposium on Microarchitecture, 1997.
22. D. Kirovski, J. Kin, and W. H. Mangione-Smith, "Procedure Based Program Compression," presented at International Symposium on Microarchitecture, 1997.
23. D. Kirovski, C. Lee, M. Potkonjak, and W. H. Mangione-Smith, "Application-Driven Synthesis of Core-Based Systems," presented at International Conference on Computer Aided Design, 1997.
24. Mangione-Smith, P. S. Ghang, S. Nazareth, P. Lettieri, W. Boring, and R. Jain, "A Low Power Architecture for Wireless Multimedia Systems: Lessons Learned from Building a Power Hog," presented at International Symposium on Low Power Electronics and Design, 1996.
25. Lee, J. Kin, M. Potkonjak, and W. H. Mangione-Smith, "Media Architecture: General Purpose vs. Multiple Application-Specific Programmable Processor," presented at Design Automation Conference, 1998.
26. Lee, M. Potkonjak, and W. H. Mangione-Smith, "MediaBench: a Tool for Evaluating and Synthesizing Multimedia and Communications Systems," presented at International Symposium on Microarchitecture, 1997.
27. Rashid, J. Asher, W. H. Mangione-Smith, and M. Potkonjak, "Hierarchical Watermarking for Protection of DSP Filter Cores," presented at IEEE 1999 Custom Integrated Circuits Conference, San Diego, CA USA, 1999.
28. H. Zou, H. J. Kim, S. Kim, B. Daneshrad, R. Wesel, and W. H. Mangione-Smith, "Equalized GMSK, Equalized QPSK, and COFDM, a Comparative Study for High Speed Wireless Indoor Data Communications," presented at International Vehicular Technology Conference, Houston, TX USA, 1999.
29. J. Kin, C. Lee, W. H. Mangione-Smith, and M. Potkonjak, "Power Efficient Mediaprocessors: Design Space Exploration," presented at Design Automation Conference, New Orleans, LA USA, 1999.
30. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Robust FPGA Intellectual Property Protection through Multiple Small Watermarks," presented at Design Automation Conference, 1999.
31. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Efficient Error Detection, Localization and Correction for FPGA-based Debugging," presented at Design Automation Conference, 2000.
32. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Algorithms for Efficient Runtime Fault Recovery on Diverse FPGA Architectures," presented at IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 1999.
33. Lee, J. Kin, M. Potkonjak, and W. Mangione-Smith, "Designing Power Efficient Hypermedia Processors," presented at International Symposium on Low Power Electronics and Design, 1999.

34. J. Lach, W. H. Mangione-Smith, and W. Potkonjak, "Enhanced Intellectual Property Protection for Digital Circuits on Programmable Hardware," presented at International Workshop on Information Hiding, 1999.
35. J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Runtime Logic and Interconnect Fault Recovery on Diverse FPGA Architectures," presented at Military and Aerospace Applications of Programmable Devices and Technologies, 1999.
36. Benyamin and W. Mangione-Smith, "Functional Unit Specialization through Code Analysis," presented at International Conference on Computer Aided Design, 1999.
37. J. Kin, C. Lee, W. H. Mangione-Smith, and M. Potkonjak, "A Technique for QoSBased System Partitioning," presented at ASP-DAC, 2000.
38. S. Brown, C. Lee, and W. H. Mangione-Smith, "Offline Program Re-Mapping to Improve Branch Prediction Efficiency in Embedded Systems," presented at ASP-DAC, 2000.
39. H. Kim and W. Mangione-Smith, "Factoring Large Numbers with Programmable Hardware," presented at International Symposium on Field Programmable Gate Arrays, 2000.
40. G. Memik, W. Hu, and W. Mangione-Smith, "NetBench: A Benchmarking Suite for Network Processor," presented at Computer Aided Design, 2001.
41. G. Memik, S. Memik, and W. Mangione-Smith, "Design and Analysis of a Layer Seven Network Processor Accelerator Using Reconfigurable Logic," presented at IEEE Symposium on FPGAs for Custom Computing Machines, 2002.
42. G. Memik and W. Mangione-Smith, "A Flexible Accelerator for Layer 7 Networking Applications," presented at Design Automation Conference, 2002.
43. Y. Cho, S. Navab, and W. Mangione-Smith, "Specialized Hardware for Deep Network Packet Filtering," presented at International Conference on Field Programmable Logic and Application, 2002.
44. G. Memik and W. Mangione-Smith, "Improving Power Efficiency of Multi-Core Network Processors Through Data Filtering," presented at International Conference on Compilers, Architecture and Synthesis for Embedded Systems, 2002.
45. G. Memik, G. Reinman, and W. Mangione-Smith, "Just Say No: Benefits of Early Cache Miss Determination," presented at International Symposium on High Performance Computer Architecture, 2002.
46. G. Memik and W. Mangione-Smith, "NEPAL: A Framework for Efficiently Structuring Applications for Network Processors," presented at NP-2: The Second Workshop on Network Processors, Anaheim, CA, 2003.
47. G. Memik, G. Reinman, and W. H. Mangione-Smith, "Reducing Energy and Delay Using Efficient Victim Caches," presented at International Symposium on Low Power Electronics and Design, Seoul, Korea, 2003.
48. Young Cho and William H. Mangione-Smith, "Programmable Hardware for Deep Packet Filtering on a Large Signature Set." First Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=ac 2), Yorktown, NY, Oct. 6-8, 2004
49. Young Cho and William H. Mangione-Smith, "Deep Packet Filter with Dedicated Logic and Read-Only-Memories." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley / CA, April 2004.

Book Chapters

1. W. H. Mangione-Smith, "Register Requirements for High Performance Code Scheduling," in *The Interaction of Compiler Technology and Computer Architecture*, D. Lilja and P. Bird, Eds.: Kluwer Academic Press, 1994, pp. 51-84.
2. W. H. Mangione-Smith, "Performance Bounds for Rapid Computer System Evaluation," in *Fast Simulation of Computer Architectures*, T. Conte and C. Gimarc, Eds.: Kluwer Academic Press, 1995.
3. G. Memik and W. H. Mangione-Smith, "NEPAL: A Framework for Efficiently Structuring Applications for Network Processors," in *Network Processor Design: Issues and Practices*, vol. 2, P. Crowley, M. A. Franklin, H. Hadimioglu, and P. Z. Onufryk, Eds.: Morgan Kaufman, 2003.

Magazine Articles

1. W. H. Mangione-Smith, S. G. Abraham, and E. S. Davidson, "A Performance Comparison of the IBM RS/6000 and the Astronautics ZS-1," in *IEEE Computer*, vol. 24, 1991.
2. W. H. Mangione-Smith, B. Hutchings, D. Andrews, A. DeHon, C. Ebeling, R. Hartenstein, O. Mencer, J. Morris, K. Palem, V. K. Prasanna, and H. A. E. Spaanenburg, "Seeking Solutions in Configurable Computing," in *IEEE Computer*, vol. 30, 1997, pp. 38-43.
3. W. H. Mangione-Smith, "Application Design for Configurable Computing," in *IEEE Computer*, vol. 30, 1997, pp. 115-17.
4. J. Villasenor and W. H. Mangione-Smith, "Configurable Computing," in *Scientific American*, vol. 276, 1997, pp. 54-9.
5. W. H. Mangione-Smith, "Mobile Computing and Smart Spaces," in *IEEE Concurrency*, vol. 6, 1998, pp. 5-7.
6. W. H. Mangione-Smith, "'Beauty Depends on Size'-Aristotle," in *IEEE Concurrency*, vol. 6, 1998, pp. 8-10.