

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

UNITED STATES PATENT AND TRADEMARK OFFICE COURT
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,
vs.
NETLIST, INC.,
Patent Owner.

-----/

Case No.: IPR2022-00711
U.S. Patent Number 10,860,506

REMOTE VIDEOTAPED DEPOSITION OF
ROBERT WEDIG, Ph.D
Thursday, January 19, 2023
9:00 a.m. - 5:16 p.m. (PST)

Stenographically Reported By:
Kimberly Fontalvo, RPR, CLR
Realtime Systems Administrator
NCRA, CCRA, FCRA

1 APPEARANCES:

2
3
4 On behalf of Petitioner:

5
6 BAKER BOTTS, LLP
101 California Street, Suite 3600
7 San Francisco, CA 94111
BY: TED CHANDLER, ESQ.
8 ted.chandler@bakerbotts.com
9

10 - - and - -
11

12 BAKER BOTTS, LLP
1001 Page Mill Road, Suite 200
13 Palo Alto, CA 94304
BY: FERENC PAZMANDI, ESQ.
14 ferenc.pazmandi@bakerbotts.com
15
16
17
18
19
20
21
22
23
24
25

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

APPEARANCES (Continued:)

On behalf of Patent Owner:

IRELL & MANELLA, LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

BY: JONATHAN LINDSAY, ESQ.

jlindsay@irell.com

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

I N D E X

Examination		Page
Direct	By Mr. Lindsay	5
Cross	By Mr. Chandler	216
Redirect	By Mr. Lindsay	222
Certificate of Oath		227
Certificate of Reporter		228

EXHIBITS

No.		Page
Exhibit 1	Declaration of Dr. Robert Wedig	10
Exhibit 2	Curriculum Vitae of Robert Wedig, Ph.D	11
Exhibit 3	Ex 3 US Publication No. 2006-0277355 (Ellsberry et al)	25
Exhibit 4	JEDEC Standard - DDR3 SDRAM, JESD79-3C	39
Exhibit 5	Ex 5 US Publication No. 2010-0312956 (Hiraishi et al)	42
Exhibit 6	Ex 6 USP 7,036,053 (Zumkehr et al)	66
Exhibit 7	Ex 7 US Publication No. 2007-0008791 (Butt et al)	67
Exhibit 8	USP 8,020,022 (Tokuhiro)	144

1 THE COURT REPORTER: Please raise your
2 right hand.

3 Do you swear that the testimony you are 8:58:47AM
4 about to give will be the truth, the whole
5 truth, and nothing but the truth?

6 THE WITNESS: I do. 9:01:29AM

7 MR. LINDSAY: This is Jonathan Lindsay 9:01:38AM
8 from Irell & Manella for Patent Owner,
9 Netlist, Inc.

10 MR. CHANDLER: Good morning. This is Ted 9:01:47AM
11 Chandler from Baker Botts on behalf of the
12 Petitioner, Samsung Electronics Co. Ltd. And
13 with me is my colleague, Ferenc Pazmandi.

14 DIRECT EXAMINATION 9:02:02AM

15 BY MR. LINDSAY: 9:02:06AM

16 Q. Dr. Wedig, this is a deposition for 9:02:06AM
17 IPR2022-00711 challenging claims of U.S. Patent
18 Number 10,860,506.

19 Is that your understanding? 9:02:20AM

20 A. Yes, it is. 9:02:25AM

21 Q. So, if I refer to IPR2022-0711 as the 9:02:26AM
22 '711 IPR, or "this proceeding," you will know what
23 I'm referring to?

24 A. Yes, I will. 9:02:36AM

25 Q. And is it okay to refer to U.S. Patent 9:02:37AM

1 Number 10,860,506 as the '506 Patent?

2 | A. Yes, it is. 9:02:48AM

3 Q. So I know that you know all of this, but 9:02:52AM
4 just for the record, I would like to go over a few
5 ground rules if that's okay.

6	A. Yes.	9:02:57AM
---	---------	-----------

7 MR. CHANDLER: If I may interject, it 9:02:58AM
8 sounds like the witness's microphone may be on
9 his computer rather than his webcam. It
10 doesn't sound as good as it did before. I
11 don't know if others have the same reaction.
12 So you might try to fix that.

13	(Discussion off the record.)	9:04:07AM
----	------------------------------	-----------

14 MR. LINDSAY: Okay. I think we're ready 9:04:08AM
15 to go back on the record.

16	MR. CHANDLER: Okay. I'm ready.	9:04:12AM
----	--------------------------------	-----------

17	BY MR. LINDSAY:	9:04:19AM
----	-----------------	-----------

18 Q. So Dr. Wedig, I was just going to go over 9:04:24AM
19 some ground rules. Obviously, I know that you know
20 these, but just so it's on this record.

21	You understand that you've taken an oath	9:04:31AM
22	to tell the truth here today?	

23	A. Yes, I know that.	9:04:37AM
----	----------------------	-----------

24 Q. And you understand that this oath has the 9:04:39AM
25 same force and effect as if in a court of law before

1 a judge and a jury?

2 A. Yes. 9:04:46AM

3 Q. And you understand that you could be 9:04:47AM

4 subject to penalty of perjury for providing false or

5 misleading testimony today?

6 A. I understand. 9:04:55AM

7 Q. Is there anything preventing you from 9:04:58AM

8 giving a full and accurate account of your opinions,

9 and answers to my questions today?

10 A. No, there's not. 9:05:05AM

11 Q. If you don't ask me to clarify a question, 9:05:10AM

12 I will assume you understand the question.

13 Is that fair? 9:05:16AM

14 A. I understand. 9:05:17AM

15 Q. And when you are on a break, you 9:05:19AM

16 understand that you are still going to be under

17 oath?

18 A. Yes, I understand. 9:05:25AM

19 Q. Okay. And also when you are on a break, 9:05:26AM

20 you understand that your Counsel is not to coach

21 you, act as an intermediary, interpret questions, or

22 help you to answer questions?

23 A. I understand. 9:05:40AM

24 Q. And you also understand that your Counsel 9:05:45AM

25 cannot instruct you not to answer a question, unless

1 it's necessary to preserve the attorney-client
2 privilege?

3 | A. I understand. 9:05:54AM

4 Q. And if I ask -- if I ask you a question, I 9:05:58AM
5 would just ask that, if there's pending question,
6 that you provide an answer, before asking to take a
7 break, for example.

8 | Is that fair? 9:06:10AM

9 | A. I understand. 9:06:12AM

10 Q. Okay. And, obviously, any time you need 9:06:13AM
11 to take a break, just let us know.

12	A. Okay. I will do that.	9:06:21AM
----	--------------------------	-----------

13 Q. Did you do anything to prepare for your 9:06:24AM
14 deposition here today?

15	A. Yes, I did.	9:06:29AM
----	----------------	-----------

16	Q. And what did you do?	9:06:31AM
----	-------------------------	-----------

17 A. I reviewed all the documents that were 9:06:34AM
18 relevant to this IPR.

19 Q. And by "all the documents relevant to this 9:06:44AM
20 IPR," are you referring to the documents that have
21 been filed with the Patent Trial and Appeal Board?

22 A. Yes, that's what I'm referring to. 9:06:55AM

23 Q. Any other documents, besides the ones that 9:06:58AM
24 were filed?

25	A. Nothing that I can think of, no.	9:07:05AM
----	-------------------------------------	-----------

1 Q. Did you meet with your attorneys in 9:07:10AM
2 preparation for your deposition today?

3 A. Yes, I did. 9:07:14AM

4 Q. About how long did you meet with your 9:07:17AM
5 attorneys?

6 A. There were two sessions. Each was 9:07:23AM
7 approximately 4, 4- to 5 hours. So approximately,
8 I'll say, 10 hours total between the two sessions.

9 Q. Okay. Do you have any documents with you 9:07:43AM
10 right now?

11 A. Yes, I do. 9:07:47AM

12 Q. Which documents do you have? 9:07:50AM

13 A. I have with me a paper copy of my 9:07:52AM
14 declaration. I have a paper copy of Dr. Khatri's
15 declaration. I have a paper copy of a number of
16 exhibits, all individually tabbed. I can read off
17 those exhibit numbers if you would like me to.

18 Q. No. Are those all exhibits that were 9:08:20AM
19 filed in the IPR?

20 A. Yes, that's correct. 9:08:24AM

21 Q. That's fine. You don't have to. 9:08:26AM

22 A. And finally, I've got -- I have the actual 9:08:28AM
23 Petition that was made, along with the Preliminary
24 Response, the Preliminary Reply, Preliminary
25 Sur-reply, and Institution Decision.

1 So everything I have here was -- it's in 9:08:46AM
2 evidence in the case.

3 I also do have -- on a second screen I 9:08:53AM
4 have these same documents, plus maybe a few others,
5 all of which, again, have been made public in this
6 hearing. And I have them on tabs in my browser,
7 just for easy access.

8 Q. Okay. So with respect to the paper 9:09:22AM
9 documents that you have in front of you, did you
10 make any notes or markings on those documents?

11 A. No, I did not. 9:09:29AM

12 MR. LINDSAY: Okay. I'm going to go ahead 9:09:30AM
13 and introduce the first exhibit.

14 (Thereupon, marked as Exhibit 1.) 9:10:12AM

15 MR. LINDSAY: Apologies. It took longer 9:10:30AM
16 than I expected.

17 BY MR. LINDSAY: 9:10:33AM

18 Q. Let me know when you see Exhibit 1. 9:10:33AM

19 (Discussion off the record.) 9:10:49AM

20 A. I did just refresh, and I do see the 9:11:07AM
21 exhibit showing up now under "Marked Exhibits."

22 BY MR. LINDSAY: 9:11:11AM

23 Q. Okay. Would you open that exhibit, 9:11:11AM
24 please?

25 A. Okay. 9:11:16AM

1 Q. Do you recognize this document? 9:11:20AM
2 A. Yes, I do. 9:11:23AM
3 Q. And what is it? 9:11:25AM
4 A. This is the declaration that I submitted 9:11:27AM
5 for this IPR.
6 MR. LINDSAY: Okay. Very good. 9:11:31AM
7 I'm going to go ahead and introduce a 9:11:34AM
8 second exhibit, hopefully quicker this time.
9 (Thereupon, marked as Exhibit 2.) 9:11:42AM
10 BY MR. LINDSAY: 9:12:05AM
11 Q. Okay. That was better. 9:12:05AM
12 Let me know when you see Exhibit 2. 9:12:06AM
13 A. I see Exhibit 2. 9:12:15AM
14 Q. Okay. Would you please open that? 9:12:17AM
15 Do you recognize this document? 9:12:23AM
16 A. Yes, I do. 9:12:25AM
17 Q. And what is this? 9:12:27AM
18 A. This appears to be my CV. 9:12:29AM
19 Q. Take a look and let me know, is this CV 9:12:37AM
20 still accurate?
21 A. Yes, it is. 9:12:55AM
22 Q. So you graduated from Dayton in 1977? 9:13:02AM
23 A. That's correct. 9:13:07AM
24 Q. And during your undergrad years, you list 9:13:09AM
25 professional experience as application programmer?

1	A. Yes, that's correct.	9:13:17AM
2	Q. Was that a part-time position during	9:13:19AM
3	college?	
4	A. Yes, it was.	9:13:22AM
5	Q. You then received your master's from USC	9:13:26AM
6	in 1979?	
7	A. That's correct.	9:13:32AM
8	Q. Under your professional experience, during	9:13:35AM
9	those same years, you indicate that you were working	
10	as a processor design engineer?	
11	A. That's correct. That would have been	9:13:45AM
12	concurrently with getting my master's.	
13	Q. Was that a part-time or a full-time	9:13:50AM
14	position?	
15	A. It was a part-time position when I was	9:13:54AM
16	taking classes. When I was not taking classes, it	
17	was full-time.	
18	Q. What did your work include as a processor	9:14:06AM
19	design engineer for Hughes Aircraft?	
20	A. Well, what the name says, I worked on	9:14:15AM
21	computer processors. I designed a number of	
22	different computer systems or different aspects of	
23	computer systems for Hughes Aircraft.	
24	Q. So when you say you designed computer	9:14:35AM
25	systems, I'm trying to understand, the title says	

1 "processor design." Were you designing
2 microprocessors, or was it more component-level
3 design -- or system-level design, sorry?

4 A. Yeah. It was system-level design at that 9:14:53AM
5 time. I was not designing microprocessors. We were
6 not in the microprocessor design business. This was
7 computer design but done with individual components
8 and not designing a microprocessor.

9 Q. And your work at Hughes Aircraft, did it 9:15:16AM
10 include designing memory modules?

11 A. It included designing memory controllers. 9:15:24AM
12 I had a project where I needed to design a memory
13 controller that interfaced with memory modules.

14 Q. And then you received your Ph.D. in 1982;
15 is that correct?

16 A. That's correct. 9:15:48AM

17 Q. And during that time you worked as a 9:15:48AM
18 research assistant?

19 A. Yes, I did. A research assistant and 9:15:53AM
20 instructor and a teaching assistant.

21 Q. If you can summarize, what were some of 9:16:01AM
22 your work experiences as a research assistant?

23 A. My work focused on detecting parallelism 9:16:12AM
24 in instruction streams in order to be able to try
25 and get maximum computer performance. So it had to

1 do with trying to execute multiple computer
2 instructions at the same time.

3 Q. And then once you graduated with your 9:16:38AM
4 Ph.D. in 1982, you then worked as an assistant
5 professor at Carnegie-Mellon; is that correct?

6 A. That's correct. 9:16:53AM

7 Q. And this CV indicates you were there for 9:16:55AM
8 three years --

9 A. That's correct. 9:16:59AM

10 Q. -- approximately. 9:17:00AM

11 And then at that point, you formed 9:17:02AM
12 Wedig Consulting, Inc.; is that fair?

13 A. That's correct. 9:17:11AM

14 Originally it was not a corporation, but 9:17:12AM
15 eventually I incorporated it.

16 Q. So what is Wedig Consulting, Inc.? 9:17:19AM

17 A. Wedig Consulting, Inc. is a company that 9:17:24AM
18 does computer consulting in any area that I feel
19 competent in performing.

20 Q. What are some of the types of clients that 9:17:42AM
21 might hire Wedig Consulting?

22 A. Clients that would hire me would be 9:17:49AM
23 companies that are interested in various problems in
24 computer design and anything -- like I say, anything
25 that would fit my expertise. I've done a lot of

1 different projects.

2 Q. Have you designed any components, computer 9:18:24AM
3 components, as part of your work at
4 Wedig Consulting?

5 A. You mean actual integrated circuits? 9:18:35AM

6 Q. Yes, correct. 9:18:40AM

7 A. No, that's not part of my work. 9:18:42AM

8 Q. Have you designed any memory modules as 9:18:48AM
9 part of your work at Wedig Consulting?

10 A. I have done work where I have interfaced 9:18:56AM
11 with memory modules and needed to understand their
12 operation. But the actual design of memory modules,
13 no, I was not involved in the actual design of a
14 memory module.

15 Q. Are some of the other types of companies 9:19:22AM
16 that would hire Wedig Consulting law firms?

17 A. Yes. Some of the work I do is with law 9:19:27AM
18 firms.

19 Q. And about what percentage of the work that 9:19:31AM
20 you currently do would you say is for law firms as
21 opposed to non-law firm clients?

22 A. Well, at this time I'm trying to retire, 9:19:43AM
23 and so I really only have one job at this time, and
24 that's working on this IPR. So all the work I'm
25 doing right now is for law firms.

1 Q. Understood. 9:20:04AM
2 So over the last three years, what 9:20:05AM
3 percentage of your work would you say has been for
4 law firms?
5 A. In the last three years, I have been 9:20:15AM
6 retired, and this has been the only case that I've
7 been working on.
8 Q. How about going back five years? 9:20:26AM
9 A. Five years. Let me think. 9:20:31AM
10 Best I recall, it's only been work for law 9:20:35AM
11 firms.
12 Q. So for the last five years, you've only 9:20:41AM
13 been working as a consultant on patent cases?
14 A. Yeah, very sporadically. I mean, it's an 9:20:51AM
15 overstatement to say I've been working on it for the
16 last five years. I haven't done much work at all in
17 the last five years. I mean, it's only been this
18 case, and if you go back five years, I did work on
19 an ITC case related to, again, to memory modules.
20 But that's all I've really done in the last five
21 years. And like I said, it's not been full-time.
22 Q. Understood. 9:21:28AM
23 A. Very intermittent. 9:21:29AM
24 Q. How about from the time period of, say, 9:21:31AM
25 the early 2000s to the mid 2000s, do you recall how

1 much work you were doing at that point for law
2 firms?

3 A. I'm sorry. You said from the early 2000s 9:21:47AM
4 to mid 2000s?

5 Q. Yes. 9:21:53AM

6 A. So approximately the year 2000 to 2005? 9:21:55AM

7 Q. Yes. 9:21:58AM

8 A. Oh, gee, I don't remember. 9:21:59AM

9 I was doing some work for law firms. I 9:22:01AM
10 was also doing work for other companies, for
11 technology companies. It might have been -- it
12 might have been 50/50. I don't recall exactly.
13 That was a long time ago.

14 Q. Sure. Okay. Fair enough. 9:22:21AM

15 And then how about from 2005 to 2010? 9:22:23AM

16 A. Again, I don't recall exactly. Maybe the 9:22:35AM
17 same. Maybe 50/50. Maybe a little more for law
18 firms. I honestly don't remember.

19 Q. Okay. That's fair enough. 9:22:45AM

20 When were you first retained to provide 9:22:47AM
21 testimony in this IPR?

22 A. I think I was first contacted -- it might 9:22:55AM
23 have been -- let's see. We're in 2023 now.

24 It might have been August, approximately 9:23:08AM
25 August of 2021, I think, is when I was first

1	contacted.
---	------------

2 Q. Referring now to your declaration that was 9:23:26AM
3 submitted in the IPR, who wrote that document?

4 | A. I did. 9:23:32AM

5 Q. Did you write the entire document 9:23:34AM
6 yourself?

7 | A. No, I did not. 9:23:37AM

8 Q. What percentage of the declaration would 9:23:41AM
9 you say that you wrote yourself?

10 A. I would say that -- it's hard to quantify. 9:23:47AM
11 I would say I checked over everything. I had a hand
12 in its creation and I approved everything, I
13 verified everything, so I consider it my work.

14	Q. How much time, approximately, did you	9:24:05AM
15	spend preparing the declaration?	

16	A. Oh, gosh. I don't remember. It might	9:24:14AM
17	have been -- I don't know. I don't want to	
18	speculate.	

19	Q. Was it more or less than 50 hours?	9:24:29AM
----	---------------------------------------	-----------

20 A. Oh, I think so, yeah, uh-huh. 9:24:34AM

21	Q. I'm sorry. It was an "or" question.	9:24:39AM
----	--	-----------

22	Did you spend more than 50 hours or less	9:24:41AM
23	than 50 hours?	

24 A. I mean more than 50 hours. 9:24:48AM

25	Q. Would you say more than 100 hours or less	9:24:54AM
----	--	-----------

1 than 100 hours?

2 A. I don't know. I don't recall. I mean, I 9:24:58AM
3 don't recall as I sit here. That was back in 2021.
4 Actually, going into -- it wasn't a day-by-day
5 thing. It was going into 2022, also.

6 Q. All right. The prior art references that 9:25:21AM
7 are discussed in your declaration, did you find
8 those references?

9 A. No, I did not. 9:25:36AM

10 Q. Who provided you with those references? 9:25:41AM

11 A. Counsel for Samsung. 9:25:45AM

12 Q. Did Counsel for Samsung provide you with 9:25:53AM
13 additional prior art references?

14 A. Beyond the ones that I have included in my 9:25:59AM
15 report?

16 Q. Right. 9:26:05AM

17 A. I don't recall. I didn't focus on them if 9:26:15AM
18 they did. I focused on the ones that I used. Did
19 they give me more than that? I just don't remember.

20 Q. Okay. That's fair. 9:26:29AM

21 But sitting here today, you don't recall 9:26:29AM
22 Counsel providing you with any other prior art
23 references, other than the ones that are described
24 and discussed in your declaration?

25 A. That's correct. I don't recall them doing 9:26:41AM

1 it. They may have. I just don't recall because I
2 used the ones that I did.

3 Q. Okay. That's fair. 9:26:53AM

4 Did you -- in reviewing your declaration 9:26:54AM
5 preparing for your deposition today, did you
6 identify any errors in your declaration?

7 A. Nothing substantive. I think I found a 9:27:14AM
8 few spelling mistakes. But, yeah, nothing of any --
9 nothing of any substance that I found.

10 Q. Are your opinions complete as they are set 9:27:30AM
11 forth in your declaration?

12 A. Yes, they are. 9:27:34AM

13 Q. Do you intend to offer any additional 9:27:36AM
14 opinions today that are not in your declaration?

15 A. I don't plan to do that, no. 9:27:43AM

16 Q. You believe you have consulted all of the 9:27:48AM
17 relevant sources of information that may be material
18 to the opinions in your declaration?

19 A. I hope so. I mean, I tried to. 9:27:58AM

20 Q. So let's go to your declaration, 9:28:09AM
21 Paragraph 37 for a moment, okay?

22 A. I'm going to use my paper copy if that's 9:28:23AM
23 okay.

24 Q. Sure. You can use whichever version you 9:28:26AM
25 would like.

1	A. Okay.	9:28:44AM
2	Q. This paragraph discusses your opinion	9:28:45AM
3	about what a person of ordinary skill in the art	
4	would be in the field of the '506 Patent at the time	
5	of the invention, July 2012.	
6	Correct?	9:28:56AM
7	A. That's correct.	9:28:58AM
8	Q. And part of what you've written here is	9:28:58AM
9	that a person of skill would be knowledgeable about	
10	the design and operation of computer memories --	
11	apologies -- and how they interact with other	
12	components of computer systems such as memory	
13	controllers.	
14	Correct?	9:29:24AM
15	A. That's essentially what it says, yes.	9:29:30AM
16	Q. What do you mean by "interact with memory	9:29:32AM
17	controllers"?	
18	A. I'm sorry, are you looking at	9:29:57AM
19	Paragraph 37?	
20	Q. Yes. I'm looking at Paragraph 37, the	9:30:01AM
21	first line of Page 13, where you say "how they	
22	interact with other components."	
23	A. I'm sorry. I was on Page 12.	9:30:15AM
24	I'm sorry. Ask your question again,	9:30:16AM
25	please.	

Page 21

1 Q. The question is, what do you mean by 9:30:32AM
2 "interact with memory controllers"?
3 A. What I mean by that is how they would 9:30:39AM
4 communicate. You know, what signals would be passed
5 back and forth, what protocols would be used, what
6 the timing would be; how they communicate in order
7 to be able to perform their function.
8 Q. Okay. Thank you. 9:31:02AM
9 And for the '506 Patent, would you agree 9:31:02AM
10 that the '506 Patent discloses determining a
11 predetermined amount of delay based on signals
12 received during a write operation?
13 MR. CHANDLER: Object to form. 9:31:21AM
14 A. I don't -- I think we need to go to the 9:31:28AM
15 claim, because I don't think that's exactly the
16 wording of the claim.
17 BY MR. LINDSAY: 9:31:34AM
18 Q. So let me restate the question. I'm not 9:31:34AM
19 asking about the claims.
20 A. Okay. 9:31:41AM
21 Q. I'm asking about the disclosure of the 9:31:42AM
22 '506 Patent.
23 A. Okay. 9:31:46AM
24 Q. Would you agree that the '506 Patent 9:31:46AM
25 discloses determining a predetermined amount of

1 delay based on signals received during a
2 write operation?

3 MR. CHANDLER: Object to form. 9:31:58AM

4 A. I think that that's generally, you know, 9:32:09AM
5 at a very high level, that's what's being taught in
6 the specification.

7 BY MR. LINDSAY: 9:32:18AM

8 Q. And that write operation would be 9:32:18AM
9 initiated by a host controller, right?

10 MR. CHANDLER: Objection, form. 9:32:28AM

11 A. Again, I think maybe we need to get into 9:32:34AM
12 the actual -- if you're going to keep getting more
13 specific as to what's being taught in the patent, I
14 think I would be more comfortable actually looking
15 in the specification.

16 BY MR. LINDSAY: 9:32:45AM

17 Q. Sure. Before we get there, let's -- we 9:32:46AM
18 can take a look at what you said in your
19 declaration. Maybe --

20 A. Okay. 9:32:54AM

21 Q. -- it would be helpful. 9:32:54AM

22 Paragraph 44 of your declaration, you're 9:32:55AM
23 describing Figure 12A?

24 A. Can I read Paragraph 44, please? 9:33:02AM

25 Q. Of course. 9:33:18AM

1	A. Okay. I'm ready.	9:34:04AM
2	Your question again was?	9:34:05AM
3	Q. I was really just going to ask you about	9:34:07AM
4	the first sentence. So you're describing 12A.	
5	You're talking about the data buffer determining a	
6	time interval based on the reception of signals to	
7	the data buffer during a write operation.	
8	A. Yes. That's what happens in the '506	9:34:24AM
9	Patent, that's correct.	
10	Q. And so correct me if I'm wrong, but I	9:34:28AM
11	think you agree that the '506 Patent discloses	
12	determining a predetermined amount of delay based on	
13	signals received during a write operation.	
14	MR. CHANDLER: Objection, form.	9:34:42AM
15	BY MR. LINDSAY:	9:34:43AM
16	Q. Is that fair?	9:34:44AM
17	MR. CHANDLER: Objection, form.	9:34:45AM
18	A. Well, I can state it slightly differently.	9:35:01AM
19	It does perform a write operation. And using the	
20	write operation, through a series of additional	
21	computations, will then determine a predetermined	
22	delay that is -- that's going to then later be used.	
23	BY MR. LINDSAY:	9:35:28AM
24	Q. Okay. So let's focus on the	9:35:28AM
25	write operation.	

1	A. Okay.	9:35:32AM
2	Q. That write operation is initiated by a	9:35:34AM
3	host controller, right?	
4	MR. CHANDLER: Objection, form.	9:35:40AM
5	A. It would be initiated, yes. I mean it	9:35:46AM
6	would be initiated by a host controller, that's	
7	correct.	
8	BY MR. LINDSAY:	9:35:52AM
9	Q. And the host controller would transmit	9:35:52AM
10	control and address signals that are associated with	
11	that write operation to the memory module, right?	
12	A. Yes. They have to communicate with it,	9:36:02AM
13	yes.	
14	MR. LINDSAY: Let me introduce another	9:36:07AM
15	exhibit real quick.	
16	(Thereupon, marked as Exhibit 3.)	9:36:22AM
17	A. Okay.	9:36:23AM
18	BY MR. LINDSAY:	9:36:24AM
19	Q. Please let me know when you see Exhibit 3	9:36:24AM
20	and please open it when you are able to.	
21	A. Okay. I see that.	9:36:55AM
22	Q. Do you recognize this document?	9:36:58AM
23	A. Yes, I do.	9:37:02AM
24	Q. What is it?	9:37:03AM
25	A. This is a patent application publication	9:37:05AM

1 to Ellsberry, et al.

2 Q. Okay. I'll refer to this as Ellsberry if 9:37:22AM
3 that's okay.

4 A. Sure. 9:37:27AM

5 Q. You rely on Ellsberry for teaching certain 9:37:28AM
6 limitations in the dependent claims that require
7 specific bit widths; is that right?

8 A. Yes, I do. 9:37:39AM

9 Q. In your opinion, is Ellsberry describing a 9:37:41AM
10 JEDEC-compliant module?

11 MR. LINDSAY: J-E-D-E-C, for the record. 9:37:52AM

12 A. I would have to review it again. I can't 9:37:58AM
13 tell you off the top of my head without studying it,
14 because my focus on Ellsberry was not whether it was
15 JEDEC compliant or not.

16 So if you could point me to something, I 9:38:12AM
17 would be able to agree or disagree. But I can't
18 tell you without review whether that's correct or
19 not.

20 Q. Okay. That's fair. 9:38:24AM

21 If you could turn to or look at 9:38:25AM
22 Paragraph 50 in Ellsberry, which is described in
23 Figure 5; Figure 5 as well would probably be
24 somewhat helpful.

25 A. So let's see here. I'm going to show 9:38:46AM

1 Paragraph 50, but then if you don't mind, I'm going
2 to bring up in a separate window a copy of Ellsberry
3 that I have on my own computer so I can look at
4 Figure 5.

5 Is that okay?

6 Q. Certainly. These are some of the 9:39:07AM
7 advantages to virtual depositions.

8 A. Yes, it is, isn't it? 9:39:30AM

9 Okay. I have Figure 5, and I'm going to 9:39:31AM
10 read Paragraph 50 now.

11 Okay. I have read Paragraph 50 and I see 9:40:06AM
12 Figure 5.

13 Q. And Paragraph 51 discusses Figure 6. If 9:40:11AM
14 you want to take a look at Figure 6, I think is on
15 the next page as well.

16 A. Okay. I see Figure 6. 9:40:26AM

17 Q. Okay. So the question is, is Ellsberry 9:40:28AM
18 describing a JEDEC-compliant module?

19 A. Again, I see a reference to JEDEC, and it 9:40:40AM
20 says that the JEDEC standards are incorporated by
21 reference. But the exact wording of saying that
22 these -- that this design satisfies the JEDEC
23 standard, I don't see those words.

24 Q. Okay. Well, let me read -- 9:41:04AM

25 A. I'm sorry. Let me say that I'm not saying 9:41:06AM

1 that it isn't. It could possibly be, but I don't
2 see it specifically saying that.

3 Q. Okay. Let me read a sentence then from 9:41:16AM
4 Paragraph 50 and we can talk about it.

5 A. Okay. 9:41:22AM

6 Q. So I'm reading from Paragraph 50, the part 9:41:24AM
7 of it that is on Page 6 of the specification, I
8 guess.

9 It says, "As a result this architecture, 9:41:33AM
10 the memory module presents a single electrical load
11 to the system and is compatible with existing
12 standards (e.g., JEDEC compatible, et cetera)."

13 When you read that sentence, doesn't that 9:41:53AM
14 indicate that Ellsberry's module is JEDEC compliant?

15 A. It would seem to imply it, but it doesn't 9:42:17AM
16 say it exactly. I mean, it says it's compatible
17 with existing standards and then it gives examples
18 of such standards. JEDEC is a standard. But it
19 doesn't say the words "it is compatible with a JEDEC
20 standard."

21 Q. Okay. So in Figure 5, what is 504, 9:42:38AM
22 reference number 504, pointing to?

23 A. 504 is -- it says that -- the words in the 9:43:09AM
24 previous page, bottom of Page 5, says that "In one
25 implementation of the invention illustrated in

1 Figure 5, the memory devices 504 and 512 on memory
2 module 500 may be arranged as nine memory bank
3 switches or sets having two memory banks, 504 and
4 512."

5 So 504 is what Ellsberry is referring to 9:43:44AM
6 as -- the word that it uses is memory bank.

7 Q. Looking at Figure 5, memory bank 504 9:43:56AM
8 includes five rectangles. What do each of those
9 rectangles represent?

10 MR. CHANDLER: Objection, form. 9:44:08AM

11 A. Well, first of all, 504 literally is 9:44:14AM
12 pointing to a single rectangle. Isn't that fair?

13 BY MR. LINDSAY: 9:44:31AM

14 Q. Yeah. So what does Ellsberry mean when it 9:44:31AM
15 refers to a bank?

16 MR. CHANDLER: Objection, form. 9:44:37AM

17 A. Ellsberry's reference to bank is something 9:44:45AM
18 that you have to understand based on the time that
19 Ellsberry came out.

20 So my understanding is that the bank that 9:44:56AM
21 it's referring to is the old terminology that --
22 what we might refer to today as a rank.

23 So it's referring to some amount of 9:45:17AM
24 storage.

25

1	BY MR. LINDSAY:	9:45:32AM
2	Q. Okay. So in Paragraph 50 -- I'm going to	9:45:32AM
3	go back there and just read another sentence.	
4	A. Okay.	9:45:38AM
5	Q. It says, "Each memory device has	9:45:39AM
6	512 megabits of DRAM."	
7	A. I see that.	9:45:51AM
8	Q. What is that talking about in Figure 5?	9:45:53AM
9	A. That's talking about each individual box	9:45:57AM
10	from which, for example, 504 is pointing to one of	
11	them that says DDR2 FBGA 512. That means that one	
12	of those boxes is comprised of 512 megabits of	
13	storage.	
14	Q. And according to Figure 5, is that storage	9:46:29AM
15	DDR2 compliant?	
16	A. It doesn't say that in Paragraph 50.	9:46:45AM
17	Maybe you can help me by -- if you believe that's	
18	the case, you might help me by showing where it	
19	might say that.	
20	Q. I was referring to Figure 5, if you want	9:47:02AM
21	to look at Figure 5.	
22	A. Okay.	9:47:06AM
23	Q. Is that DDR2 memory that we were talking	9:47:06AM
24	about?	
25	A. Yeah.	9:47:12AM

1 It doesn't say that in Figure 5. So, 9:47:12AM
2 again, I can't tell by looking at Figure 5 if that's
3 correct or not.

4 Q. It doesn't say DDR2 FBGA 512? 9:47:20AM

5 A. Oh, I'm sorry. It does say DDR2. I'm 9:47:25AM
6 sorry, I didn't see that.

7 That would imply that it's DDR2 compliant. 9:47:29AM
8 Yeah, I mean -- I think one might see that based on
9 that nomenclature.

10 Q. Okay. So for the original question now, 9:47:43AM
11 considering Paragraph 50 and Figures 5 and 6, is it
12 fair to say that Ellsberry is describing a
13 JEDEC-compliant module?

14 A. It's a module that has DDR2 devices on it. 9:48:02AM
15 But that still does not give you the guarantee that
16 it's JEDEC compliant. You can put DDR2 memory
17 devices on a module and it still may not be JEDEC
18 complaint.

19 Q. Is it fair to say that the memory devices 9:48:36AM
20 themselves are JEDEC compliant?

21 A. Again, just based on the word, DDR2, on a 9:48:45AM
22 picture on Figure 5, no, you can't make that leap.
23 Because you could still come up with something that
24 has a double-data-rate-type device in that time
25 frame. You could put a figure and call it DDR2, but

1 it doesn't necessarily mean that it follows all of
2 the specific requirements for JEDEC compatibility.

3 Q. Isn't it fair to say that Ellsberry is 9:49:22AM
4 trying to communicate that the memory device is DDR2
5 memory by stamping it DDR2?

6 A. Yeah, I will give you the fact that it 9:49:35AM
7 says that it's DDR2. Therefore, you know, it is
8 within the family of possible devices that practice
9 doing a double data rate in that time frame. I
10 would agree with that.

11 Q. Okay. And DDR2 is a JEDEC standard; is 9:50:00AM
12 that correct?

13 A. Well, you can call something DDR2, you 9:50:11AM
14 could call it that, but it's not -- that does not
15 automatically mean that it's JEDEC compliant. I
16 mean, this is -- again, we're looking at a label on
17 an individual figure. So it doesn't necessarily
18 mean that it's JEDEC compliant.

19 Q. Does JEDEC have restrictions against 9:50:42AM
20 labeling components that are not -- with DDR2
21 designations when they are non-compliant?

22 A. No, I don't know. That's not -- that's a 9:50:57AM
23 technical question. I don't know what their
24 restrictions are. I don't know what control they
25 can have over what someone labels their device.

1 Q. So can you take a look at the claims 9:51:15AM
2 section of Ellsberry, Claim 10 in particular?

3 A. Yes. Okay. I see it. 9:51:20AM

4 Q. Is this saying that the memory module that 9:51:38AM
5 Ellsberry is claiming as his invention, his
6 inventive memory module, is JEDEC compliant?

7 A. For Claim 10. In fact, this even supports 9:51:54AM
8 what I've been trying to say, that until Claim 10,
9 you could practice Ellsberry's invention without
10 being JEDEC compliant.

11 So, in fact, Claim 6 and, you know, all of 9:52:10AM
12 the claims before it, could practice Ellsberry
13 without being JEDEC compliant. It's only when you
14 get to Claim 10 that JEDEC compliance is now
15 required in order to satisfy Claim 10.

16 Q. So is it fair to say one embodiment of 9:52:32AM
17 Ellsberry's memory module is JEDEC compliant?

18 A. I think that you need to have -- you need 9:52:43AM
19 have to some teaching of it. So, yeah, I think that
20 Claim 10 -- at least Claim 10, standing by itself,
21 says that in order to practice Ellsberry, for
22 Claim 10, it needs to be JEDEC compliant.

23 MR. LINDSAY: Move to strike as 9:53:08AM
24 non-responsive.

25 Can we read the question back, please? 9:53:27AM

1	(Requested portion read back.)	9:53:31AM
2	A. Understanding that it's necessary for a	9:53:36AM
3	specification to be clear to one of ordinary skill	
4	as to how to practice the patent, I think that	
5	Ellsberry gives an explanation of how to practice	
6	the patent, and it may not necessarily, in the	
7	description of the specification, say that it must	
8	be JEDEC compliant.	
9	But then when you read Claim 10 and it	9:54:06AM
10	says it must be JEDEC compliant, that statement	
11	means that any of the additional details that you	
12	might need in order to be able to make sure that	
13	it's JEDEC compliant would have to be there in order	
14	to satisfy Claim 10.	
15	So I don't think that the specification	9:54:31AM
16	necessarily requires the JEDEC compliance in the	
17	description of the embodiment, but Claim 10 does.	
18	BY MR. LINDSAY:	9:54:46AM
19	Q. So do you understand what I mean when I	9:54:46AM
20	say an embodiment?	
21	A. Yeah, I think so, yes.	9:54:50AM
22	Q. Okay. So I'm not saying -- I'm not asking	9:54:52AM
23	you what Ellsberry's disclosure requires.	
24	A. Okay.	9:55:00AM
25	Q. I'm only asking, is it fair to say that	9:55:00AM

1 one embodiment of Ellsberry is a JEDEC-compliant
2 module?

3 MR. CHANDLER: Objection, outside the 9:55:09AM
4 scope of direct.

5 A. Well, "embodiment" -- let's make sure we 9:55:16AM
6 understand.

7 "Embodiment" means a description in the 9:55:18AM
8 specification as to how the invention works. That's
9 my understanding of an embodiment.

10 Do I have a correct understanding, from 9:55:28AM
11 your perspective?

12 BY MR. LINDSAY: 9:55:33AM

13 Q. I'm not going to comment on your 9:55:33AM
14 understanding of an embodiment.

15 A. Okay. 9:55:43AM

16 Q. What I'm asking is -- well, let's take a 9:55:44AM
17 look at maybe Paragraph 47.

18 A. Okay. 9:55:52AM

19 Q. The first line says, "Figures 5 and 6 9:55:53AM
20 illustrate memory modules according to two different
21 embodiments of the invention."

22 Correct? 9:56:01AM

23 A. Yes, I see that. 9:56:07AM

24 Q. Is it fair to say that Ellsberry discloses 9:56:10AM
25 different embodiments of his invention?

1 A. Yes, that's a fair statement. 9:56:16AM

2 Q. Okay. Is it fair to say that in one of 9:56:17AM

3 | those embodiments, at least, Ellsberry is describing

4 a JEDEC-compliant module?

5 A. No. And I can explain why, if you would 9:56:32AM

6	like.
---	-------

7	Q. Yes, please.	9:56:40AM
---	-----------------	-----------

8	A. Because Ellsberry discloses what it	9:56:43AM
---	--	-----------

discloses and clearly, at least as of Claim 6, JEDEC

10 compliance is not required. And so therefore, if

11 the embodiment required JEDEC compliance, then there

12 would be no additional restrictions, no additional

13 requirements added by Claim 10. And so therefore

14 Claim 6 and Claim 10 would be the same.

15	So therefore, the embodiments that	9:57:27AM
----	------------------------------------	-----------

16 Ellsberry provides must not require JEDEC

17	compliance.
----	-------------

18	Q. I think your definition of "embodiment" is	9:57:44AM
----	---	-----------

19 different than mine.

20	Is Figure 6 describing an embodiment of	9:57:48AM
----	---	-----------

21	Ellsberry?
----	------------

22	A. It's an illustration of the embodiment,	9:58:03AM
----	--	-----------

23	yes.
----	------

24	Q. Is Figure 10 covering the same embodiment	9:58:08AM
----	--	-----------

25 as Figure 6?

1	A. Hang on one second.	9:58:18AM
2	Figure 10. Hang on here.	9:58:27AM
3	Q. I apologize. Strike that.	9:58:43AM
4	A. Okay.	9:58:44AM
5	Q. Is Claim 6 covering one embodiment of	9:58:46AM
6	Ellsberry?	
7	A. Claim 6 is a claim that describes the	9:58:57AM
8	patent. The embodiments help to -- help one of	
9	ordinary skill to understand what the patent is	
10	about, but the claim actually tells you what the	
11	invention is.	
12	So I'm sorry, maybe I -- I don't mean to	9:59:26AM
13	be nonresponsive. Can you ask that question one	
14	more time, please?	
15	Q. Is Claim 6 covering an embodiment of	9:59:34AM
16	Ellsberry?	
17	MR. CHANDLER: Objection, outside the	9:59:41AM
18	scope of direct.	
19	A. Claim 6 would cover -- Claim 6 describes	9:59:49AM
20	an invention which would be described as -- which	
21	would be taught in the specification.	
22	And one of ordinary skill would understand	10:00:12AM
23	what the invention is in Claim 6, given the	
24	description in the specification.	
25	The embodiments help to tell you what the	10:00:28AM

Page 37

1 patent is about; to help teach you as to what the
2 patent is. But does it describe a particular
3 embodiment? I mean, I guess I would have to walk
4 through each claim element to make sure that it's
5 all covered in the embodiment. But the intention is
6 that you know what the invention is based on reading
7 the specification.

8 BY MR. LINDSAY: 10:01:12AM

9 Q. Let's take a look at Paragraph 214 of your 10:01:12AM
10 declaration, please.

11 A. Okay. 10:01:35AM

12 Okay, I see it. 10:01:45AM

13 Q. What do you mean by "Ellsberry discloses a 10:01:49AM
14 memory module with the same distributed buffer
15 architecture and four ranks of memory as Hiraishi"?

16 A. What I mean is that Ellsberry has a very 10:02:08AM
17 similar design as Hiraishi, in that it uses a
18 distributed buffer architecture, just like Hiraishi,
19 and it also has four ranks of memory, just like
20 Hiraishi.

21 Q. Are there any other similarities between 10:02:39AM
22 Ellsberry's memory module architecture and Hiraishi?

23 A. Well, there may be. Those are not the 10:02:47AM
24 ones that I -- I mean, those are the two that I
25 identify. But is there more similarities? I mean,

1 I could go through Ellsberry and look for it. But
2 that's not what I -- that's not in my opinion.

3 Q. Fair enough. But for this paragraph, 10:03:04AM
4 those were the only similarities that you had in
5 mind?

6 A. Those are the two that I identified, yes. 10:03:11AM

7 MR. LINDSAY: I'm going to introduce 10:03:13AM
8 another exhibit.

9 (Thereupon, marked as Exhibit 4.) 10:03:22AM

10 THE COURT REPORTER: We are off the 10:03:23AM
11 record.

12 (Discussion off the record.) 10:04:33AM

13 MR. CHANDLER: Why don't we take a break. 10:04:40AM

14 (Recess was held from 10:04 a.m. until 10:11 a.m.) 10:04:42AM

15 THE COURT REPORTER: Ready to go back on 10:11:07AM
16 the record.

17 BY MR. LINDSAY: 10:11:12AM

18 Q. Dr. Wedig, I'm going to introduce an 10:11:23AM
19 exhibit as Exhibit 4. Please let me know when you
20 see it, and please open it once you do.

21 A. Okay. I have it and I've opened it. 10:11:44AM

22 Q. Okay. What is this document? 10:11:47AM

23 A. This is the JEDEC Standard for the DDR3 10:11:51AM
24 SDRAM.

25 Q. And what does it signify? 10:11:59AM

1 A. It signifies the required -- what is 10:12:06AM
2 required in order to be able to create a DDR3
3 JEDEC-compliant component.

4 Q. And you cite this document in your 10:12:26AM
5 declaration; is that right?

6 A. Yes, I believe I do. 10:12:30AM

7 Q. Is it your understanding that Hiraishi's 10:12:35AM
8 system is compliant with the JEDEC DDR3 standard?

9 A. I guess I would have to look at Hiraishi. 10:12:56AM
10 I don't recall that that's required in order to
11 practice Hiraishi.

12 Is there something you are thinking of in 10:13:04AM
13 Hiraishi that says that it's required to be JEDEC
14 compliant? Because there's nothing that I know that
15 jumps out at me as to -- saying that in order to
16 practice Hiraishi, it must be JEDEC compliant.

17 Q. You cited to the JEDEC DDR3 standard 10:13:33AM
18 several times when describing Hiraishi; is that
19 right?

20 A. That's correct. 10:13:40AM

21 Q. Why did you cite to the standard if it 10:13:45AM
22 wasn't describing or supporting your description of
23 Hiraishi?

24 A. Well, I think there are things in the 10:13:53AM
25 standard that help you to understand the technology

1 of the time and the kind of things that you would
2 need to do in order to be -- in order to make a
3 workable system. And the JEDEC was a well-known
4 standard at that time.

5 I mean, it very well may be that a device 10:14:20AM
6 that practices the Hiraishi patent may be JEDEC
7 compliant, but I'm just saying that I don't see that
8 that is a limitation. I think it's still possible
9 to practice Hiraishi without the JEDEC standard, or
10 JEDEC compliant.

11 Q. So let's take a look, if we could, at 10:14:54AM
12 Paragraph 118 of your declaration.

13 A. Okay. 10:15:01AM

14 Q. At the very end of 118, you cite to this 10:15:09AM
15 JEDEC standard we were just discussing and a
16 parenthetical after describing read operations,
17 correct?

18 A. One moment, please. 10:15:27AM

19 Yes, I see that. 10:15:28AM

20 Q. In this paragraph, you are discussing 10:16:12AM
21 Hiraishi's read operations, among other things. Are
22 those read operations described in the JEDEC
23 standard?

24 A. Can I look at Hiraishi Paragraph-163 and 10:16:56AM
25 170?

1 Q. Sure. I'll go ahead and -- I know you do, 10:17:10AM
2 but let me just introduce it into the record so that
3 we're all on the same page here.

4 A. Okay. 10:17:21AM

5 MR. LINDSAY: I'm introducing Hiraishi as 10:17:36AM
6 Exhibit 5.

7 (Thereupon, marked as Exhibit 5.) 10:17:39AM

8 BY MR. LINDSAY: 10:17:48AM

9 Q. Can you just confirm for me when you see 10:17:48AM
10 that?

11 MR. CHANDLER: Can you wait just a moment 10:17:57AM
12 while I'm pulling that up? I mean I have
13 Hiraishi, but I want to get your copy of it.

14 THE WITNESS: Okay, I have Hiraishi up on 10:18:12AM
15 my screen.

16 MR. CHANDLER: I've got to refresh here. 10:18:21AM
17 One moment.

18 All right. I've got it, thank you. 10:18:25AM

19 BY MR. LINDSAY: 10:18:28AM

20 Q. Is this Exhibit 4 the -- sorry -- 10:18:30AM
21 Exhibit 5 the same Hiraishi reference that you are
22 looking at on your other screen, Dr. Wedig?

23 A. Well, I'm actually looking at it in the 10:18:49AM
24 book. But in my -- I'm actually looking at it in my
25 paper copy. But, yes, it's the same Hiraishi

1 patent. Actually, a patent application.

2 Q. In the lower right corner, there's a label 10:19:01AM
3 there that says "Samsung Electronics Co., Ltd,
4 Exhibit 1005"?

5 A. Yes. Yes, it's the same document. 10:19:12AM

6 I'm sorry, is there a question pending? 10:19:14AM

7 Q. I believe you wanted to look at paragraphs 10:19:32AM
8 in Hiraishi.

9 A. Yes. Yes, thank you. 10:19:36AM

10 All right. I've read 163 and 170 in 10:19:38AM
11 Hiraishi. Now, I'm sorry, what was your question
12 again?

13 THE COURT REPORTER: Would you like me to 10:20:34AM
14 read it back?

15 MR. LINDSAY: Yes, please. 10:20:34AM

16 (Requested portion read back.) 10:21:10AM

17 A. Yeah. I mean, I could go to Page 33 and 10:21:18AM
18 56 through 67 of the JEDEC standard. But, yes, the
19 JEDEC standard does describe read operations of a
20 DDR3 memory device.

21 BY MR. LINDSAY: 10:21:34AM

22 Q. And Hiraishi's read operations that you 10:21:35AM
23 are discussing here, are those compliant with the
24 description of read operations in the JEDEC
25 standard?

1 MR. CHANDLER: Objection, form. 10:21:49AM

2 A. Well, as I sit here right now, I'm not -- 10:21:58AM

3 I don't have anything in mind that makes Hiraishi's

4 read operations not compliant with the JEDEC

5 standard.

6 However, the complete, minuscule detail of 10:22:14AM

7 how Hiraishi does its read operation, I mean, it

8 gives the information to the level that's necessary

9 in order to practice Hiraishi, but it doesn't give

10 as much detail as the JEDEC DDR3 standard.

11 So there's nothing that's incompatible, 10:22:37AM

12 based on what Hiraishi says, to the extent that

13 Hiraishi provides that information.

14 BY MR. LINDSAY: 10:22:54AM

15 Q. So you, in describing Hiraishi, you cite 10:22:54AM

16 to the JEDEC standard I think I counted six times in

17 your declaration. And we can go through each one of

18 those.

19 A. Okay. 10:23:06AM

20 Q. Is it the case that you have cited to the 10:23:08AM

21 JEDEC standard in support of your description of

22 Hiraishi because you believe a person skilled in the

23 art would understand that Hiraishi's system is a

24 DDR3-compliant system?

25 MR. CHANDLER: Objection, form. 10:23:28AM

1 A. When I refer to DDR3 -- when Hiraishi 10:23:44AM
2 refers to DDR3, I think one would naturally go to
3 the JEDEC standard in order to help understand what
4 that means. So I guess -- I mean, I'm sorry, I
5 guess I'm not clear on exactly what the question is.
6 Maybe can you ask it a different way.

7 BY MR. LINDSAY: 10:24:17AM

8 Q. Sure. I'll try again. 10:24:17AM

9 So a person skilled in the art reading 10:24:19AM
10 Hiraishi, would they understand Hiraishi is
11 describing a DDR3-compliant system?

12 A. Well, the reason I'm having trouble with 10:24:32AM
13 that question is because DDR3 is a memory device.
14 The Hiraishi system, the Hiraishi system uses memory
15 devices and it refers to DDR3 memory devices.

16 And so, therefore, it doesn't use what you 10:24:55AM
17 might call the JEDEC -- the JEDEC system, that word
18 "system" does not make sense when comparing it with
19 the teachings of Hiraishi, which is actually a
20 memory module system. So that's where I'm having
21 the difficulty.

22 Q. Okay. I'll rephrase. Is Hiraishi's -- 10:25:21AM
23 strike that.

24 Would a person of ordinary skill in the 10:25:26AM
25 art reading Hiraishi understand that Hiraishi's

1 memory module is DDR3 compliant?

2 A. I think one would understand that that is 10:25:44AM
3 a possibility, and I think that would be, you
4 know -- that would be a common popular device to
5 use.

6 But I don't think Hiraishi is limited that 10:26:04AM
7 the DDR3 device has to follow all of the JEDEC
8 standard. I mean, I think you would be guided by
9 it, but it doesn't say that it must be -- that it
10 must follow the JEDEC standard.

11 So that's the best I can say. That would 10:26:33AM
12 be something that I would look to because it would
13 make sense.

14 Q. Let me unpack that, if I could, and see if 10:26:46AM
15 I understood your answer.

16 So is it your opinion that Hiraishi is not 10:26:49AM
17 limited to DDR3 memory modules?

18 A. Not limited, but it would be, like I said, 10:27:05AM
19 that would be the -- I think you could still
20 practice Hiraishi without being JEDEC compliant.
21 But it would be the most common way, and the way the
22 teachings of Hiraishi provide, it would make sense
23 that you would look to the JEDEC standard in order
24 to help fill in any additional information that you
25 need. That's why I reference it.

1 But I don't -- I just want to make sure 10:27:37AM
2 it's clear that I don't believe that you -- I don't
3 believe that you are limited to having to practice
4 Hiraishi only by following every detailed aspect of
5 the JEDEC standard.

6 Q. Okay. That's fair. 10:28:04AM

7 Is it the case that Hiraishi's memory 10:28:06AM
8 module could be made to be DDR3 compliant?

9 A. Yes, it could be. There's nothing that I 10:28:27AM
10 know of in Hiraishi that is incompatible with the
11 JEDEC standard.

12 Q. Okay. And when Hiraishi is designed to be 10:28:37AM
13 DDR3 compliant, it would be able to process data at
14 speeds that are provided for under the standard,
15 right?

16 A. When it is DDR3 JEDEC compliant, then it 10:28:56AM
17 would need to satisfy all the criteria, all of the
18 requirements of the standard. So, yes, it would
19 operate at the speeds that are required by the
20 standard.

21 Q. Is it your opinion that Hiraishi's 10:29:11AM
22 disclosure is sophisticated enough to describe a
23 memory module which could comply with the DDR3
24 standard?

25 A. Well, I think I already answered that. I 10:29:30AM

1 said there's nothing incompatible in Hiraishi that
2 would not allow it to follow the standard.

3 So the answer -- I think it's kind of the 10:29:48AM
4 same question. Yes, reading Hiraishi, you could
5 make a system taught by Hiraishi that would follow
6 the standard.

7 Q. The DDR3 standard? 10:30:02AM

8 A. The DDR3 memory device standard. 10:30:07AM

9 Q. Okay. In 2005, what was considered high 10:30:14AM
10 speed for memory modules?

11 A. You mean how many megahertz? I don't 10:30:29AM
12 recall as I sit here. I mean, I would have to look
13 that up. I didn't talk about that in my report.

14 Q. Let me ask it maybe a different way. 10:30:41AM

15 In 2005, was DDR2 the prevalent standard 10:30:42AM
16 for memory modules?

17 A. I know that DDR2 existed. I'm not sure 10:30:52AM
18 exactly when DDR3 came out. I can just say that was
19 it prevalent? The best I can say is that DDR2
20 existed in that time frame.

21 Q. If I told you DDR2 came out in 2003, would 10:31:12AM
22 that comport with your recollection?

23 A. Yes. I mean, like I said, I know it 10:31:20AM
24 existed. As I just said, I know it existed and I
25 know it was being used.

1 Was it prevalent in that time frame? I 10:31:28AM
2 mean, I don't know the sales of DDR2. And without
3 further research, I don't remember when DDR3 came
4 out. It was either around that time frame or
5 shortly after.

6 But, again, this is not in my report. I 10:31:44AM
7 can't give you any answer to that without
8 researching it more.

9 Q. That's fair enough. 10:31:58AM

10 DDR3 came out in 2010. It's not relevant 10:31:58AM
11 really when it came out. But the question is, is it
12 your understanding that DDR3 provides specifications
13 for memory modules that are operable at a higher
14 speed than DDR2?

15 A. Yes, that's my understanding, yes. 10:32:26AM

16 By the way, I simply want to maybe correct 10:32:28AM
17 something you just said, which I -- you said that
18 DDR3 came out in 2010. I do see at least the JEDEC
19 standard was released in April of 2008. So I think
20 your timing is off a little bit.

21 Q. You're correct. My apologies. 10:32:50AM

22 So DDR3, when it came out, was supposed to 10:32:54AM
23 be an improvement on DDR2, right?

24 A. We would hope so. 10:33:03AM

25 Q. Were DDR3 memories capable of 10:33:05AM

1 significantly faster speeds than DDR2, if you
2 recall?

3 A. Well, "significant" is kind of a vague 10:33:15AM
4 word. I mean, I would agree that they were capable
5 of faster speeds. Again, I mean, any more -- giving
6 more information beyond just saying, yes, they go
7 faster, I would need to do research on it. None of
8 this is in my report.

9 Q. I understand. 10:33:38AM

10 And so, I mean, it would be fair to say 10:33:38AM
11 that DDR3 memory improved upon DDR2 memory?

12 A. Again, I would say I would hope so. I 10:33:51AM
13 mean, there are lots of differences between DDR2 and
14 DDR3. One change would be faster speed. But how
15 much faster, I mean, I would have to research that.
16 None of this is in my declaration.

17 Q. Right. No, we're talking about memory 10:34:10AM
18 modules that were disclosed in references around
19 this time frame, so I think your understanding of
20 what the prevailing standard was at the time is
21 relevant to your declaration. And in that context,
22 I'm asking these questions.

23 A. Okay. 10:34:33AM

24 Q. That's why we're on this line of 10:34:35AM
25 questions. Okay?

1 A. Okay. Again, I'll answer them to the best 10:34:38AM
2 that I can, based on my professional knowledge of
3 the standards at that time. I can answer questions
4 much better when I've done research and studied.

5 The standards are quite thick. There's a 10:34:51AM
6 lot to them. I don't keep every little aspect of
7 the standard in my mind at all times. So if you
8 start getting more detailed, I'm just going to have
9 to take the time in order to be able study the
10 standard in order to be able to answer your
11 questions.

12 Q. That's perfectly fair. 10:35:09AM

13 To your recollection, was DDR3 inferior to 10:35:11AM
14 DDR2 memory in any way?

15 A. "Inferior" is very qualitative word. I 10:35:25AM
16 mean, I'm sure there are advantages and
17 disadvantages to DDR3 over DDR2.

18 I think this is one of the places where I 10:35:35AM
19 would have to study it more carefully and see what
20 did we give up by going to DDR3?

21 So I can't really answer that question, 10:35:44AM
22 since it's such a qualitative question and it would
23 require study to be able to give you all the
24 differences between DDR2 and DDR3.

25 Q. You wouldn't expect a new standard to 10:35:55AM

1 reduce the reliability of the memory, though, would
2 you?

3 A. I wouldn't expect that, you know. But 10:36:10AM
4 again, in order to answer your questions as
5 carefully as possible, I would want to --

6 You are correct, I wouldn't expect it. 10:36:17AM
7 But I haven't written about that in my declaration.
8 And so beyond saying what my expectations would be,
9 I can't really say more than that.

10 Q. Okay. Generally speaking, though, is it 10:36:32AM
11 fair to say that DD3-compliant memory would be able
12 to process read operations faster than a
13 DDR2-compliant memory?

14 A. As I said earlier, I said I would hope so. 10:36:45AM
15 Why come out with a standard, unless it can do
16 something faster or better.

17 But, you know, I would need to look at it 10:36:54AM
18 in order to be able to see the more detailed -- in
19 more detail than saying it seems as though that
20 should be the case.

21 Q. Okay. That's fair. 10:37:08AM

22 So back to Hiraishi's memory module. 10:37:10AM

23 A. Uh-huh. 10:37:16AM

24 Q. When it's designed to be DDR3 compliant, 10:37:16AM
25 is fair to say that it would be able to process

1 memory operations faster than, you know, a standard
2 DDR2 memory module?

3 A. Again, best I can say is I would hope so. 10:37:33AM
4 But I haven't really researched that, so I don't
5 have that in my opinion.

6 Q. When you say you hope so, is it fair to 10:37:52AM
7 say that you would expect so?

8 A. Well, what I said, and I've said a couple 10:37:58AM
9 times, is that when you come out with a new
10 standard, you would hope that it's an improvement
11 over a previous standard. Why would anybody go to
12 it unless there were some improvements? So in that
13 sense, I would expect that the new standard would
14 have improvements.

15 Speed is a very important issue in memory 10:38:20AM
16 design. So increased speed would be expected, yes.
17 But beyond that, like I said, I would have to look
18 at the documents to be able to tell you exactly what
19 the differences are between DDR2 and DDR3.

20 Q. I understand. I was just trying to get to 10:38:42AM
21 what you meant by "hope" versus "expect".

22 A. Yeah. 10:38:47AM

23 Q. So I don't remember if the question was 10:38:48AM
24 directly answered, but for Hiraishi's memory module,
25 then, you would expect it to process read operations

1 faster than a DDR2 memory module would?

2 A. Well, I think I stated the word "hope" 10:39:12AM

3 because I haven't -- it was not in my report to look

4 at the speed differences between DDR2 and DDR3.

5 So when you say "expect," when we use the 10:39:23AM

6 word "expect," it means that there is the

7 implication that it must be faster. So I think I'm

8 more comfortable saying I would hope so.

9 Q. Okay. What is the difference between 10:40:01AM

10 sampling data and latching in data?

11 A. I know I discussed that. 10:40:13AM

12 At a high level, at a very high level, 10:40:18AM

13 there's no difference. Each of those two words can

14 have very specific meanings, but at a high level,

15 there is no difference.

16 Q. Okay. To latch in read data as it's 10:40:41AM

17 received, a DDR3 module would need to be able to do

18 that at a higher rate than a DDR2 module; is that

19 fair?

20 A. If, in fact, it's going to run faster -- 10:41:08AM

21 if it's going to run faster, then all of its

22 operation would need to be faster. So all of its

23 latching, all of its data transmission, its clock,

24 everything would need to be faster if, in fact, it's

25 going to run faster than DDR2.

1 Q. So between DDR2 and DDR3, do you know what 10:41:44AM
2 changed in terms of how data was being latched into,
3 let's say, a memory controller? Read data, that is.

4 MR. CHANDLER: Object to form. 10:42:03AM

5 A. This is not in my report, so I would have 10:42:07AM
6 to study that. I can't tell you off the top of my
7 head.

8 BY MR. LINDSAY: 10:42:14AM

9 Q. In your declaration, you discuss sampling 10:42:14AM
10 read data, latching in read data, correct?

11 A. Yes, I do. 10:42:23AM

12 Q. The DDR2 standard and the DDR3 standard 10:42:27AM
13 were in effect in the 2000s; is that fair?

14 A. Meaning roughly in that time frame, yes, 10:42:48AM
15 between the period of 2000 and 2010. So in the
16 2000s, yes.

17 Q. So your opinions about how data would be 10:42:57AM
18 sampled or latched would be informed by what DDR2
19 and DDR3 standards might say about that; is that
20 fair?

21 A. I think that would provide -- I think 10:43:14AM
22 those standards would help to provide part of the
23 teaching to me. However, I think the concept of
24 latching or sampling is something that one of
25 ordinary skill knows from fundamental electronics

1 digital design courses.

2 So it would add to it. I would say that 10:43:41AM
3 DDR standards would help add to it, but it would not
4 be my first source for understanding sampling and
5 latching because it's a very basic concept.

6 Q. So sitting here today, you don't know of 10:43:56AM
7 any differences between the DDR2 and DDR3 standard
8 in terms of the way read data is to be latched or
9 sampled?

10 A. Well, again, I would have to -- this is 10:44:09AM
11 not part of my report, so I would have to go back
12 and look. But as I sit here right now, I'm not
13 familiar with any differences. But there may be. I
14 just haven't studied that.

15 Q. Okay. Fair enough. But at the very 10:44:26AM
16 least, it would be your expectation that a DDR3
17 module would be latching in read data at a higher
18 speed than a DDR2 module?

19 A. As I said, would I hope so. 10:44:45AM

20 But, again, I haven't studied that, I 10:44:47AM
21 haven't provided an opinion on that, and so I would
22 have to study it to be able to thoroughly agree with
23 you.

24 Q. You've said this a number of times. 10:45:01AM

25 We've established that DDR3 memory was 10:45:03AM

1 intended to be faster operational memory than DDR2.

2 Is that at least fair?

3 A. I think it's fair to say that DDR3 was 10:45:13AM
4 intended to be better. Speed would be one aspect I
5 would look to. Better, more reliable, easier to
6 use. Speed is a very important part of it. And so
7 as I've said many times, I would hope it would be
8 faster.

9 And I would be happy to look the standard 10:45:32AM
10 side by side and tell you whether it actually was or
11 not, but it is not part of my report.

12 Q. So a DDR3-compliant module would be 10:45:43AM
13 expected to be better, more reliable, and faster
14 than a DDR2 module when latching in read data?

15 MR. CHANDLER: Objection, form. 10:46:03AM

16 A. You keep using the word "expect," and I'm 10:46:04AM
17 saying the words "I would hope so." I would think
18 that that would make sense to me. Whether you
19 expect it or not means that it necessarily is. And
20 I'm just saying without --

21 I'm not willing to give that opinion 10:46:17AM
22 without having studied it, and I have not studied
23 that issue in relation to these -- in relation to my
24 report. So I simply cannot -- I cannot agree with
25 you without having looked at the documents side by

1 side in order to be able to verify.

2 BY MR. LINDSAY: 10:46:59AM

3 Q. Let's take a look at Hiraishi. We had 10:47:07AM
4 introduced that, right, as Exhibit 5.

5 A. Yes, I see it. And I'm going to -- again, 10:47:19AM
6 I'm going to pull out my paper copy just for easier
7 viewing. So I've got the same thing, but I just
8 have it on paper right here.

9 Q. Okay. Great. 10:47:38AM

10 So Hiraishi describes one type of read 10:47:38AM
11 leveling as between the data register buffer 300 and
12 the memory chip 200, right?

13 A. Yes, it does. 10:48:03AM

14 Q. And is that referred to as S4 read 10:48:04AM
15 leveling?

16 A. Yes, that's the way it's described. 10:48:11AM

17 Q. And the read leveling in Hiraishi as 10:48:15AM
18 between the data register buffer 300 and the memory
19 chip 200, does that adjust when Hiraishi's input
20 buffers are turned on so that they're active when
21 the read data arrives?

22 A. I want to make sure that you have 10:48:37AM
23 characterized it correctly. So I don't know what
24 you -- I mean, I'm happy to point you to exactly
25 what I think you are referring to in the patent, or

1 I can state it in my own words. What would you like
2 to do?

3 Q. In your own words would be fine. 10:49:32AM

4 A. Okay. So the read leveling, what it does, 10:49:35AM
5 it's used in an adjustment of the activation timing
6 from the input buffer circuit INB and the like.
7 That's the purpose of S4 leveling.

8 Q. I thought you were going to give me your 10:49:55AM
9 own instead of reading it.

10 A. Well, those are my words. My words come 10:49:59AM
11 from reading the specification. I think the
12 specification is clear.

13 Q. What does it mean to adjust an activation 10:50:09AM
14 timing of an input buffer?

15 A. It means to determine when to activate it, 10:50:15AM
16 when to enable it, when to turn it on, is basically
17 what it means. So it allows the data to pass when
18 it's activated.

19 Q. So I think we're saying the same thing. 10:50:36AM
20 But just to maybe ask the question again, so the
21 read leveling in Hiraishi between the buffer 300 and
22 the memory chip 200, that adjusts when Hiraishi's
23 input buffers are turned on, so that they're on or
24 active when the data arrives?

25 A. Yeah. I mean, that's one of the things 10:51:07AM

1 that S4 does, and then it says "and the like." So,
2 I mean, it does more things than that. But, yes,
3 that's one of the things that it does.

4 I agree with your statement that it is 10:51:19AM
5 partially correct, that is part of what S4 is doing.

6 Q. Okay. And what else does S4 read leveling 10:51:27AM
7 in Hiraishi do?

8 A. Well, it says "and the like." So it does 10:51:34AM
9 a lot of things. It does all the things it needs to
10 do in order to be able to help you have reliable
11 communication between the memory devices and the
12 data buffer.

13 Q. And where are all those other things 10:51:56AM
14 described in Hiraishi?

15 A. One of ordinary skill would understand 10:52:02AM
16 what is necessary. So there is -- it's not given in
17 any more detail than that, but that's within the
18 knowledge of one of ordinary skill.

19 Q. So in Hiraishi, the only disclosure beyond 10:52:21AM
20 activating the input buffers as to what S4 read
21 leveling does are the three words "and the like"; is
22 that right?

23 MR. CHANDLER: Objection, form. 10:52:35AM

24 A. Those words -- those words help one of 10:52:38AM
25 ordinary skill to know. I mean those words remind

1 one of ordinary skill that there's more that needs
2 to be done. Those words are given. But one of
3 ordinary skill knows that you need to do more than
4 that.

5 BY MR. LINDSAY: 10:53:04AM

6 Q. And where would one of ordinary skill in 10:53:04AM
7 the art learn what else needs to be done?

8 A. Well, you can refer to -- I'm going to 10:53:20AM
9 refer to my declaration.

10 Okay. So Hiraishi, as I said, it says 10:53:27AM
11 "and the like." So in studying Hiraishi, as I said
12 earlier, one would utilize the JEDEC standard as a
13 guide for how to make systems of this type.

14 So the JEDEC standard refers to capturing 10:54:47AM
15 data within a data eye. So I think one would have
16 turned -- one would have turned to the JEDEC
17 standard in order to help them understand that more
18 needs to be done.

19 Furthermore, it also -- in Hiraishi it 10:55:20AM
20 talks about -- let me get the word correct. It
21 talks about providing a DQS signal -- oops. Sorry.
22 My -- I'm not sure why my -- hang on a second.
23 There we go.

24 It talks about providing a DQS signal 10:56:01AM
25 about 90 degrees, and that would inform one of

1 ordinary skill that part of the process is to
2 optimize the input so that you can receive it at the
3 proper time.

4 So I would say a combination of using the 10:56:17AM
5 JEDEC standard and, you know, one of ordinary skill
6 understanding that you need to optimize the
7 reception of data into the FIFO, I think that helps
8 to inform someone as to all the things that need to
9 be done as part of read leveling.

10 Q. Does the JEDEC standard -- is it your 10:56:47AM
11 understanding that the JEDEC standard discloses and
12 describes read leveling?

13 A. Not in any real detail, no. It doesn't go 10:56:58AM
14 into it. It provides the mechanisms for it. It
15 provides the mechanisms of what you would do for
16 read leveling, but it doesn't go through a detailed
17 procedure of how to do it in the DDR3 standard.

18 Q. So a person of skill in the art in 10:57:22AM
19 possession of Hiraishi, trying to understand what
20 needs to be done for read leveling, would not look
21 to the JEDEC standard to understand read leveling
22 since it's not described, right?

23 A. One of ordinary skill would know the -- 10:57:38AM
24 one of ordinary skill would know the individual
25 components that are available in the JEDEC standard

1 from doing read leveling, and they would know how to
2 utilize those individual components in order to
3 perform read leveling.

4 THE WITNESS: I'm sorry, I've got to -- I 10:58:00AM
5 got one little problem here. I just noticed
6 that my laptop is not charging. I'm afraid
7 it's going to die. Quickly, can you give me
8 one moment here? I just noticed my battery
9 level is very low.

10 MR. LINDSAY: We can go off the record. 10:58:18AM

11 MR. CHANDLER: Yes. 10:58:20AM

12 THE COURT REPORTER: We're off the record. 10:58:32AM

13 (Recess held from 10:58 a.m. until 11:07 p.m.) 10:58:37AM

14 THE COURT REPORTER: Back on the record. 11:07:13AM

15 BY MR. LINDSAY: 11:07:14AM

16 Q. Dr. Wedig, we were talking about 11:07:37AM

17 Hiraishi's S4 read leveling.

18 A. Uh-huh. 11:07:43AM

19 Q. Does Hiraishi expressly disclose anything 11:07:47AM

20 involved in S4 read leveling, other than turning on
21 the input buffers in order to receive read data?

22 A. It expressly says "and the like." So it 11:08:06AM
23 expressly says that you need to do more than that.

24 So it does say "enabling the input buffer, 11:08:15AM
25 INB," and then it says and more things than that, is

1 what it effectively says.

2 Q. Does it expressly state what those more 11:08:35AM
3 things are?

4 A. No. One of ordinary skill would know 11:08:39AM
5 that.

6 Q. Have you described in your declaration any 11:08:49AM
7 other adjustments made by Hiraishi's S4 read
8 leveling than adjusting the activation timing of the
9 input buffers?

10 A. Yes, I have. 11:09:05AM

11 Q. Where is that discussion? 11:09:07AM

12 A. Let me find it. 11:09:14AM

13 Page 94, Paragraph 137. 11:09:15AM

14 Q. So is it your opinion that read leveling 11:10:13AM
15 as Hiraishi describes it includes the description of
16 what you provided here in 138 regarding sampling
17 data in the middle of the data eye?

18 A. Yes. 11:10:49AM

19 Q. And why is that part of Hiraishi's 11:10:57AM
20 read-leveling operations?

21 A. Well, because Hiraishi talks about 11:11:06AM
22 delaying the DQS signal by about 90 degrees. And
23 one of ordinary skill would know that in order to
24 delay the DQS signal by about 90 degrees, you need
25 to find the exact or the most precise, the most

1 optimal location of how much to delay it by. And
2 that would be done during read leveling.

3 So it would be part of the time when you 11:11:47AM
4 are trying to find the optimal means of
5 communication between the memory device and the data
6 buffer, which is what is being done during read
7 leveling.

8 Q. What support have you pointed to the idea 11:12:10AM
9 that read leveling includes centering data?

10 A. Well, first, I pointed to the "by about 11:12:25AM
11 90 degrees," first of all. The words "and the
12 such," "and the such" meaning we need to do more
13 than that. And I'm also relying on the knowledge of
14 one of ordinary skill.

15 Q. Have you cited to any document that 11:12:57AM
16 describes centering a data eye or capturing data as
17 read leveling?

18 A. Yes, I have. 11:13:11AM

19 Q. What document? 11:13:14AM

20 A. Butt is a patent that discusses that in 11:13:15AM
21 detail. And I believe Zumkehr also discusses it.

22 MR. CHANDLER: You might want to spell 11:13:27AM
23 that.

24 THE WITNESS: Z-U-M-K -- Z-U-M-K-E-H-R is 11:13:28AM
25 my best memory of it. I can look that up. Let

1 me get that right.

2 Z-U-M-K-E-H-R, yes. 11:13:47AM

3 MR. LINDSAY: Okay. Yeah, I just 11:13:55AM

4 introduced Zumkehr as Exhibit 6.

5 (Thereupon, marked as Exhibit 6.) 11:14:11AM

6 A. Okay. Let me get there. 11:14:12AM

7 Okay. I'm there. 11:14:32AM

8 BY MR. LINDSAY: 11:14:33AM

9 Q. Does Zumkehr use the term "read leveling"? 11:14:33AM

10 A. Oh. Gee, I don't know. I don't recall 11:14:40AM

11 off the top of my head.

12 Q. You cited to Zumkehr as describing read 11:14:50AM

13 leveling, but it doesn't use the term "read

14 leveling"?

15 MR. CHANDLER: Objection, form. 11:14:59AM

16 A. What it describes is one of the parts of 11:15:01AM

17 read leveling. I think it describes a computer

18 system that needs to read data at a high speed. It

19 needs to be able to capture data reliably using a

20 DQS and a DQ signal. So it's exactly in the area of

21 the type of things you would do for read leveling.

22 I think one of ordinary skill would 11:15:41AM

23 understand that in order to do read leveling, this

24 is part of it. So this is one piece of it. But

25 I -- you know, I don't know that it specifically

1 says the words "read leveling" in it, but this is
2 clear to one of ordinary skill that this is the kind
3 of thing you would need to do as part of that
4 process.

5 MR. LINDSAY: You mentioned Butt as well. 11:16:16AM
6 I also introduced Butt into the record as
7 Exhibit 7.

8 (Thereupon, marked as Exhibit 7.) 11:16:21AM

9 BY MR. LINDSAY: 11:16:21AM

10 Q. Does Butt use the term "read leveling"? 11:16:21AM

11 MR. CHANDLER: Could I just download the 11:16:22AM
12 exhibit before you two run off? Just one
13 moment, please.

14 THE WITNESS: Are you ready, Mr. Chandler? 11:16:38AM

15 MR. CHANDLER: One moment. 11:16:42AM

16 Yes, I have Exhibit 7/Exhibit 29 Butt. 11:16:42AM

17 A. I don't know if it does or not. To me, 11:16:58AM
18 it's not relevant because it discusses exactly the
19 kind of operations you would need to do in read
20 leveling. It discusses a system that has DDR
21 memories connected to a memory controller with a
22 buffer in between, exactly the same type of thing
23 you have in Hiraishi, and it does the type of
24 operations that it would need to do in read
25 leveling.

1 So it may not say it. I don't know, I 11:17:28AM
2 haven't looked. I don't know whether it says the
3 words "read leveling" or not. But that's not
4 relevant to me because it does exactly the kind of
5 operations that are needed for read leveling.

6 BY MR. LINDSAY: 11:17:40AM

7 Q. Is read leveling a term of art? 11:17:40AM

8 A. I think one of ordinary skill would 11:17:55AM
9 understand what generally is being talked about in
10 read leveling, yes.

11 I mean, a term of art? It's a term that 11:18:03AM
12 one of ordinary skill would know what you mean.

13 Q. And what would that be? 11:18:12AM

14 A. It would be to adjust the signal timings 11:18:16AM
15 in order to allow reliable high speed operation.

16 Q. Why do you suppose that Hiraishi doesn't 11:18:58AM
17 describe what he means by "and the like," yet he
18 goes into such detail about everything else?

19 A. I didn't write the patent. I just can 11:19:11AM
20 only assume that he realizes that one of ordinary
21 skill knows what else you need to do.

22 That was clear to me, that you are going 11:19:24AM
23 to have to make sure that everything is tuned
24 properly in order to be able to work correctly, and
25 part of that is to be able to capture the signal in

1 a reliable manner. So he didn't describe it because
2 I guess he felt it wasn't necessary.

3 Q. Do you think it would have been helpful 11:19:51AM
4 for the Board if he had cited a reference that
5 described read leveling as including data centering?

6 A. Well, I did cite to two different 11:20:02AM
7 references that talk about data centering.

8 Q. Neither used the term "read leveling." 11:20:10AM
9 That's a term of art, and nothing you've cited
10 indicated what it means.

11 MR. CHANDLER: Objection, form. 11:20:15AM

12 A. Is there a question? 11:20:19AM

13 BY MR. LINDSAY: 11:20:20AM

14 Q. Yeah. Do you think it would have been 11:20:20AM
15 helpful if you cited a reference that used the term
16 "read leveling" and described it as included -- as
17 including data centering?

18 A. I don't think it would have made a 11:20:35AM
19 difference in my mind.

20 Q. Do you think the Board understands what 11:20:39AM
21 read leveling is?

22 A. I think the Board understands -- the Board 11:20:43AM
23 understands what one of ordinary skill is presenting
24 to them that, you know -- I think the Board would
25 understand that you need to -- you need to do

1 whatever is necessary in order to have a high
2 performance, reliable operation.

3 And so the fact that I did not -- the fact 11:21:16AM
4 of that being the two references did not
5 specifically say the words "read leveling," when you
6 look at them as a whole, you can see that they're
7 doing a very important aspect of read leveling.

8 They may not say exactly the words, but 11:21:34AM
9 when you compare the patent with Hiraishi, you can
10 see very significant similarities in the patents,
11 and what they're doing is helping to ensure a high
12 performance, reliable operation.

13 So I don't think the words "read leveling" 11:21:56AM
14 are necessary in order to understand the relevance
15 of these references to help enhance the operation of
16 Hiraishi.

17 Q. Have you ever seen a reference use the 11:22:09AM
18 term "read leveling" and describe data centering?

19 A. I haven't looked for that. That's not in 11:22:20AM
20 my report. So have I ever? Yeah, I -- I haven't
21 done that type of search.

22 Q. So sitting here today, you've never seen a 11:22:30AM
23 reference describe read leveling as data centering?

24 MR. CHANDLER: Objection, form. 11:22:38AM

25 A. I'm saying that I have not searched for 11:22:40AM

1 it. So the only reason I haven't seen it is because
2 I haven't searched. I'm sure it's out there. I
3 just haven't actually searched for it.

4 BY MR. LINDSAY: 11:22:51AM

5 Q. So when Hiraishi uses the term "read 11:22:51AM
6 leveling," you didn't think to search for a
7 reference that used the term "read leveling"?

8 A. I looked for references that gave the best 11:23:00AM
9 explanation of what was necessary to do read
10 leveling.

11 Q. And none of those references use the term 11:23:08AM
12 "read leveling," correct?

13 A. These references -- 11:23:10AM

14 MR. CHANDLER: Objection, form. 11:23:13AM

15 A. I'm sorry to speak quickly. 11:23:15AM

16 These references explain it the best.
17 They didn't happen to say the word "read leveling".

18 BY MR. LINDSAY: 11:23:27AM

19 Q. And none of the other references you found 11:23:27AM
20 used the term "read leveling"?

21 A. I didn't look at other references that 11:23:36AM
22 used the word "read leveling."

23 Q. That's because you weren't able to find 11:23:41AM
24 any?

25 A. I didn't search for that. I was searching 11:23:44AM

1 for a reference that best provides the explanation
2 of what would be necessary during read leveling.

3 Q. You found the references that best 11:23:56AM
4 described what you wanted to find rather than what
5 described read leveling; is that right?

6 A. No. I found the references that best 11:24:02AM
7 describe what was happening during read leveling.

8 Q. If you had an opportunity, would you go 11:24:12AM
9 back and search for references that actually used
10 the term "read leveling"?

11 A. I'll do what I'm asked to do. But I don't 11:24:22AM
12 think -- I mean, that's not part of my job at this
13 point. I submitted my report. If they want another
14 report, I'll do more work. But --

15 Q. Do you think you will find a reference 11:24:39AM
16 that uses the term "read leveling" and describes
17 data centering?

18 A. I would suspect, probably, but I can't say 11:24:45AM
19 for sure. I mean I don't know.

20 Q. Does any part of Hiraishi's read leveling 11:25:17AM
21 adjust the timing between the data buffer 300 and
22 the memory chip 200?

23 A. The timing? Let's be specific as to what 11:25:43AM
24 you mean by the timing between them.

25 Are you talking about -- the read leveling 11:25:48AM

1 in Hiraishi optimizes the transfer. So it captures
2 it reliably and it allows the data to enter the data
3 buffer at the correct time.

4 To that extent, I mean, that's exactly 11:26:18AM
5 what it does. If that affects the timing, then,
6 yeah, it does what it does. It allows the data to
7 enter at the correct time and it reliably captures
8 it into the data buffer.

9 Q. Hiraishi also describes read leveling 11:26:40AM
10 between the data buffer and the memory controller,
11 right?

12 A. That's correct. 11:26:46AM

13 Q. And is that referred to as S5 read 11:26:47AM
14 leveling?

15 A. Yes, it is. 11:26:50AM

16 Q. Can you describe S5 read leveling for me? 11:26:55AM

17 A. Essentially, it is the operation for or 11:27:02AM
18 it's the task of presenting the data to the memory
19 controller in a reliable fashion.

20 I mean, we can look at the details of it 11:27:35AM
21 if you would like. But it's similar to S4 leveling
22 in that it needs to reliably transfer the data from
23 the data buffer to the memory controller.

24 Q. And how does Hiraishi perform S5 read 11:27:57AM
25 leveling?

1 A. Well, it's described in detail in the 11:28:03AM
2 patent, if you would like to walk through it.

3 Q. Whatever you need to review to answer the 11:28:19AM
4 question is fine.

5 A. Okay. I mean, I'll walk through the -- I 11:28:25AM
6 can walk through the patent with you and give you a
7 detailed explanation of S5 leveling, if that's what
8 you're looking for.

9 Q. I want your understanding of what S5 read 11:28:39AM
10 leveling is, yes.

11 A. Okay. Well, then let me walk through it 11:28:43AM
12 with you then.

13 Okay. So read leveling between the data 11:29:01AM
14 buffer and the memory controller is illustrated in
15 Figure 17. Okay. I don't know if you want to look
16 at that. And then the explanation starts at
17 Paragraph 157 in Hiraishi. Okay?

18 Q. Okay. 11:31:05AM

19 A. So what happens is, as it's described in 11:31:05AM
20 Hiraishi, that the data buffer outputs a clock
21 signal, and at the same time it issues an ACT and a
22 read command. So that's shown at the top of
23 Figure 7.

24 I don't know if you want me to share my 11:31:33AM
25 screen to show Figure 7. Would that be beneficial

1 to you?

2 Q. No, that's fine. I have it here. 11:31:39AM

3 A. Okay. All right. So it outputs the ACT, 11:31:42AM
4 and then five clocks later it outputs the read
5 command.

6 Then the data buffer receives the read 11:32:08AM
7 command from the module controller, with a slight
8 flight time delay. And then there is -- that then
9 causes the data buffer, after a lapse, after a CAS
10 latency, it outputs dummy data to the memory
11 controller. It comes straight from the memory
12 controller, not from the memory chip.

13 And so what it does is it comes out six 11:33:14AM
14 clocks later if you have a CAS latency of six
15 clocks.

16 So then the memory controller receives 11:33:30AM
17 that data and it determines from the delay, the
18 fly-by delay that is inherent or part of the data
19 buffer communication.

20 And then it uses that in order to help 11:33:54AM
21 determine how much -- or it uses that in order to be
22 able to determine what it needs to do in order to be
23 able to align that data that has come from the data
24 buffer in order to be able to receive and utilize
25 the data all aligned at the same time.

1 I'm not sure that was totally clear, but I 11:34:25AM
2 hope that helps.

3 Q. No, that's helpful. 11:34:30AM

4 So the read leveling between the memory 11:34:31AM
5 controller and the data buffer S5 read leveling,
6 that's carried out by the memory controller?

7 MR. CHANDLER: Objection, form. 11:34:42AM

8 A. The read leveling, S5 read leveling is 11:34:44AM
9 initiated by the memory controller. Yes, that's
10 correct.

11 And then, of course, the data buffer takes 11:34:50AM
12 part by providing the dummy data in order to provide
13 it that data so it can then determine what the
14 proper timing is.

15 So it's correct in that it's initiated by 11:35:04AM
16 the memory controller.

17 BY MR. LINDSAY: 11:35:09AM

18 Q. Okay. Hiraishi's delay circuit 372 -- 11:35:09AM

19 A. Uh-huh. 11:35:20AM

20 Q. -- delays the read strobe by about 11:35:21AM
21 90 degrees is what you said in your declaration,
22 right?

23 A. Yes, that's correct. 11:35:28AM

24 Q. How does 90 degrees translate into clock 11:35:31AM
25 cycles?

1 A. 90 degrees is one -- roughly one 11:35:35AM
2 quarter -- it is one quarter of a clock cycle.

3 Q. Okay. And sticking with Hiraishi for a 11:35:44AM
4 moment, Hiraishi, would you agree, it describes an
5 operable system?

6	MR. CHANDLER: Objection, form.	11:36:02AM
---	--------------------------------	------------

7 MR. LINDSAY: I can rephrase. 11:36:07AM

8	A. Okay.	11:36:08AM
---	----------	------------

9 BY MR. LINDSAY: 11:36:08AM

10	Q. A person skilled in the art reading	11:36:09AM
11	Hiraishi could build Hiraishi's module and it would	
12	be operable?	

13 A. Well, Hiraishi got a patent. I thought it 11:36:23AM
14 was the case that you have to describe an
15 operational system in order to be able to get a
16 patent. So I think just by the fact that Hiraishi
17 has a patent, the patent examiner clearly thought
18 that it was an operational system.

19	Q. That's fair. And I guess I was just	11:36:50AM
20	asking, a person skilled in the art reading Hiraishi	
21	would have enough information to build one of his	
22	modules and that it would work as intended?	

23 A. Yeah. I don't see anything in Hiraishi 11:37:08AM
24 that would not operate correctly. I mean Hiraishi
25 disclosed an invention which described, you know,

1 how to perform the operation or how to perform the
2 functions that were there.

3 And so, of course, it doesn't have every 11:37:28AM
4 transistor, it doesn't have every gate, but from
5 what I read of Hiraishi and my knowledge of one of
6 ordinary skill, I would be able to build a memory
7 module that practiced Hiraishi's teaching.

8 Q. Okay. And comparing Hiraishi's S4 11:37:54AM
9 leveling to S5 leveling --

10 A. Uh-huh. 11:38:01AM

11 Q. -- Hiraishi's S5 leveling is initiated by 11:38:03AM
12 the memory controller, as we talked about, right?

13 A. Correct. 11:38:10AM

14 Q. And then Hiraishi's S4 read leveling is 11:38:11AM
15 performed by the read leveling circuit 323 in the
16 data buffer; is that right?

17 MR. CHANDLER: Objection, form. 11:38:24AM

18 A. Yeah, I think that's the right number. 11:38:29AM
19 Let me just check.

20 Yeah, read leveling circuit 323, yes. 11:38:32AM

21 BY MR. LINDSAY: 11:38:40AM

22 Q. So S4 leveling, S5 read leveling in 11:38:40AM
23 Hiraishi are performed by different circuitry?

24 MR. CHANDLER: Objection, form. 11:38:49AM

25 A. Well, they're initiated by different 11:38:55AM

1 circuitry. I mean, remember, the data register
2 control circuit as a whole needs to provide dummy
3 data back to the memory controller. So the memory
4 controller initiates S5 leveling, but then the data
5 register control circuit has a part in S5 leveling,
6 and then the read leveling circuit inside of the
7 data register control circuit initiates S4 leveling.
8 And then the memory device responds back.

9 So I think it's more accurate to say that 11:39:36AM
10 the memory controller initiates S5 leveling and the
11 read leveling circuit initiates S4 leveling.

12 BY MR. LINDSAY: 11:39:52AM

13 Q. Okay. That's fair. 11:39:52AM

14 So as between the memory controller and 11:39:53AM
15 the data buffer, is the purpose of Hiraishi's S5
16 leveling to account for fly-by delays?

17 A. Yeah, that's my understanding. I mean, it 11:40:14AM
18 helps to even out the fly-by delays into the
19 memory -- into the memory controller.

20 Q. And does Hiraishi provide enough 11:40:32AM
21 information to know how to do that using the
22 knowledge of one of ordinary skill in the art?

23 A. Well, Hiraishi is a little scant on the 11:40:47AM
24 exact details inside the memory controller. But I
25 think one of ordinary skill -- remember, Hiraishi is

1 focusing on the memory module itself. So the
2 information is not fleshed out in detail.

3 But I think one would understand that in 11:41:12AM
4 order to do leveling inside the memory controller,
5 you would have to work out all of that detail. But
6 I think one of ordinary skill would probably be able
7 to do that.

8 Q. Hiraishi describes a command address 11:41:48AM
9 controller register buffer 400 as well, right?

10 A. Yes, that's correct. 11:41:57AM

11 Q. What does the register buffer 400 do? 11:42:02AM

12 A. Well, it's the module controller for the 11:42:08AM
13 memory module. It does the control for -- well, it
14 receives the -- as it says in the patent, it
15 receives the control signals, the address, command,
16 control and clock, and it distributes that to the
17 data buffers. And it also distributes a mode, mode
18 information, in order to instruct the data buffers
19 what to do.

20 Q. So in Hiraishi, the register buffer 400 11:42:53AM
21 doesn't play a role in S4 or S5 leveling, right?

22 MR. CHANDLER: Objection, form. 11:43:03AM

23 A. Well, it does send out the -- what I call 11:43:16AM
24 mode. But it does send the DRC signals. And so,
25 you know, it does send out commands which would be

1 necessary in order to initiate write leveling and
2 read leveling in the data control register -- in the
3 data control circuit, I'm sorry, data control
4 circuit I meant to say.

5 BY MR. LINDSAY: 11:44:05AM

6	Q. So the register buffer 400 is passing	11:44:05AM
7	information between the data buffers and the memory	
8	controller, right?	

9 MR. CHANDLER: Objection, form. 11:44:24AM

10 A. I'm sorry, I'm not sure I caught that. 11:44:26AM

11 One more time, please. Maybe you can read it back.

12	BY MR. LINDSAY:	11:44:31AM
----	-----------------	------------

13	Q. Sure. The register buffer 400 is	11:44:31AM
14	certainly passing information between the memory	
15	controller and the data buffers.	

16 A. That's correct. That's one of its jobs, 11:44:43AM
17 yes.

18	Q. Commands relating to S4 and S5	11:44:47AM
19	read leveling don't initiate from inside the	
20	register buffer 400, though, right?	

21	MR. CHANDLER: Objection, form.	11:44:59AM
----	---------------------------------	------------

22 A. Well, in one sense, you know, the module 11:45:03AM
23 controller 400 would have to be knowledgeable of it,
24 because when you go to the data register control
25 circuit, it's not going to just perform write

1 leveling or read leveling indiscriminately. It's
2 not going to just decide to do it on its own. It's
3 going to need some type of instruction to initiate
4 it.

5 So the only thing that is providing, you 11:45:37AM
6 know, control input to the data register control
7 circuit comes from the module controller.

8 So it's going to have to -- it's going to 11:45:55AM
9 have to do something in order to initiate, in order
10 to cause the data buffer to initiate write leveling
11 and read leveling. They're not going to just decide
12 on their own to do it.

13 BY MR. LINDSAY: 11:46:14AM

14 Q. So a moment ago we talked about S5 11:46:14AM
15 read leveling being initiated by the memory
16 controller.

17 A. Uh-huh. 11:46:21AM

18 Q. Right? 11:46:21AM

19 A. Correct. 11:46:23AM

20 Q. S5 read leveling is not initiated by the 11:46:24AM
21 register buffer 400, right?

22 MR. CHANDLER: Objection, form. 11:46:34AM

23 A. Well, all of the -- other than the 11:46:35AM
24 instruction -- I mean, again, I'm doing a one of
25 ordinary skill. It doesn't talk about this in the

1 specification. But all of the work of doing S4
2 read leveling -- I'm sorry, did you say S4 or S5?
3 Q. S5. 11:46:54AM
4 A. Oh, that's right. Okay. 11:46:55AM
5 S5 is not initiated in the data buffer, 11:46:55AM
6 that's correct.
7 BY MR. LINDSAY: 11:47:00AM
8 Q. Okay. So read leveling between the memory 11:47:00AM
9 controller and the data buffer is initiated in the
10 memory controller, not the register buffer 400?
11 A. That's correct. 11:47:12AM
12 Q. Now, for S4 read leveling, the 11:47:18AM
13 read leveling between the data buffer and the memory
14 chips, where is that initiated?
15 A. As we said, it's initiated in the data 11:47:26AM
16 buffer.
17 Q. Okay. The data buffer 300? 11:47:30AM
18 A. Data buffer 300, correct. 11:47:35AM
19 Q. Okay. So in neither S4 nor S5 leveling is 11:47:38AM
20 the register buffer 400 initiating those operations?
21 MR. CHANDLER: Objection, form. 11:47:52AM
22 A. Well, yeah. 11:47:56AM
23 There is no instruction in Hiraishi on the 11:48:03AM
24 module controller doing any initiation of S4 or S5
25 read leveling. As I said, you know, the module

1 controller -- I'm sorry, the data buffer is going to
2 have to get some notification that it's time to do
3 write leveling or read leveling. So, you know, I
4 don't -- it's simply not taught as to where that
5 comes from.

6 BY MR. LINDSAY: 11:48:41AM

7 Q. For S4 it's not taught? 11:48:41AM

8 A. That's correct. 11:48:52AM

9 Q. Let's take a look at Paragraph 129, if we 11:48:57AM
10 could, of your declaration.

11 A. Okay. Paragraph 129. 11:49:07AM

12 Q. There's a figure here -- 11:49:15AM

13 A. I'm sorry. Give me one minute, please. 11:49:18AM

14 I'm with you. 11:49:19AM

15 Q. Okay. There's a figure here, Figure 5 11:49:28AM
16 from Hiraishi, and this has been annotated with some
17 colors, right?

18 A. Yes, it has. 11:49:37AM

19 Q. Okay. Can you -- so first, what is this 11:49:38AM
20 figure showing?

21 A. This figure is Figure 5, which is a 11:49:49AM
22 diagram of the data buffer.

23 Q. Data buffer 300? 11:49:58AM

24 A. Data buffer 300, correct. 11:50:00AM

25 Q. Can you identify all the data paths 11:50:02AM

1 through Hiraishi's data buffer 300 that's shown here
2 in Figure 5?

3 MR. CHANDLER: Objection, form. 11:50:11AM

4 A. Yes. I mean, I can show you what's 11:50:15AM
5 identified. There is, in the figure, it shows a
6 data path coming into --

7 I'm sorry, you want to know all the data 11:50:34AM
8 paths coming into the data buffer 300? Is that what
9 you asked for?

10 BY MR. LINDSAY: 11:50:41AM

11 Q. Right. 11:50:41AM

12 A. Okay. Well, let's go around the entire 11:50:42AM
13 figure.

14 First of all, there's a clock on the top, 11:50:46AM
15 on the left, the clock that comes in --

16 Q. I'm sorry. Let me -- just to save us some 11:50:53AM
17 time, let me rephrase the question.

18 A. Okay. 11:50:58AM

19 Q. I was asking you about data paths through 11:51:00AM
20 the data buffer --

21 A. I'm sorry. 11:51:06AM

22 Q. -- not signal paths. 11:51:07AM

23 A. Okay. I didn't hear that correctly. 11:51:09AM

24 MR. CHANDLER: Same objection to form. 11:51:11AM

25 A. Okay. So the data paths that I see 11:51:12AM

1 come -- first of all, on the right, on the upper
2 part of the right, there's L1 351 with a DQS signal
3 that comes from a memory device.

4 And then there is an L2, which is a DQS, 11:51:34AM
5 that comes from a different memory device.

6 And then -- I'm sorry, that's 352. 11:51:45AM

7 Then down at the bottom, close to the 11:51:51AM
8 bottom, there's another L1 341, which is marked DQ,
9 and that's the data that goes with the DQS 351 at
10 the top.

11 And then at the very bottom there's an L2 11:52:08AM
12 labeled 342, which goes with the L2 marked 352,
13 which is a DQS.

14 So that's the inputs. You just want the 11:52:18AM
15 inputs or you want the outputs also?

16 BY MR. LINDSAY: 11:52:25AM

17 Q. So what I wanted to focus on were the data 11:52:25AM
18 paths, the DQS data paths through the data buffer.

19 A. Okay. So you're only interested in the 11:52:42AM
20 data path, not the strobe that captures the data.

21 Q. Yeah, not yet. 11:52:50AM

22 A. Okay. All right. All right. I'm sorry. 11:52:51AM
23 I'll say it one more time just to make sure it's
24 clear on the record.

25 At the bottom there is an L1 341, which is 11:52:58AM

1 a DQ that comes in, and then there is a -- at the
2 very bottom is an L2 342, which is also a DQ that
3 comes into this data buffer.

4 Q. So the first component that the data, the 11:53:20AM
5 incoming data encounters is the input buffer; is
6 that right?

7 A. That's correct. 11:53:30AM

8 Q. And then what? 11:53:32AM

9 A. So then both of those inputs, after 11:53:35AM
10 passing through the data buffer, goes into a
11 selector. A selector is basically a MUX or a
12 multiplier. I'm sorry, not a multiplier. It is a
13 MUX or multiplexer, 334, which selects between one
14 of the DQ inputs.

15 Okay? 11:53:58AM

16 Q. Okay. 11:54:03AM

17 A. Continuing on, the next item goes to a 11:54:06AM
18 FIFO read circuit 302. And so after selection
19 through the selector, it goes into the FIFO.

20 Upon exiting the FIFO, it goes through 11:54:19AM
21 another buffer, which is an output buffer, and
22 ultimately it goes out, the DQ signal goes out
23 through the memory controller L0, which is item 340.

24 Q. Okay. So besides the input buffer, the 11:54:36AM
25 selector 334, the FIFO 302, and the output buffer,

1 no other component in Hiraishi's data buffer has
2 access to the DQ read data, right?

3 MR. CHANDLER: Objection, form. 11:54:58AM

4 A. Are you talking about just this diagram or 11:55:03AM
5 you are talking about within the teachings of
6 Hiraishi?

7 BY MR. LINDSAY: 11:55:08AM

8 Q. In this diagram. 11:55:08AM

9 A. This diagram shows what it shows. 11:55:10AM

10 However, there is more teaching that shows 11:55:14AM
11 that there is actually more paths that occur inside
12 Figure 5 than are actually -- there are more paths
13 within Hiraishi that absolute -- that exist that are
14 not shown inside Figure 5.

15 Q. So I just want to focus on Figure 5 if we 11:55:38AM
16 could right now. We can talk about the other
17 disclosures later.

18 A. Okay. 11:55:46AM

19 Q. So in Figure 5, besides the input buffer, 11:55:46AM
20 the selector 334, FIFO 302, and the output buffer,
21 no other component in Hiraishi's data buffer 300
22 shown in Figure 5, has access to the DQE data. Is
23 that correct?

24 MR. CHANDLER: Objection, form. 11:56:07AM

25 A. That's what's shown in Figure 5. 11:56:10AM

1 However, other components do, in fact, 11:56:13AM
2 have access, they're just not shown in Figure 5.
3 BY MR. LINDSAY: 11:56:20AM
4 Q. Okay. In your declaration, do you discuss 11:56:20AM
5 or describe what other components have access to DQ
6 read data, other than the ones we just discussed.?
7 A. Let me -- would you mind if I did a search 11:57:45AM
8 on my declaration?
9 Q. Sure. You mean like a keyword search? 11:59:39AM
10 A. Keyword search, yes. 11:59:43AM
11 Q. Yeah, of course. 11:59:44AM
12 A. All right. I'm going to do that. 11:59:46AM
13 Okay. Well, let me tell you what I got. 12:03:39PM
14 In my report I talk about write leveling and
15 read leveling. In particular, for example,
16 Paragraph 140, talking about how Hiraishi includes
17 both write leveling and read leveling.
18 And when you go to Hiraishi and you look 12:04:06PM
19 at write leveling or read leveling, what you see is
20 that it requires that the DQ signal is needed to --
21 needed in the data buffer in order to allow
22 write leveling and read leveling to occur.
23 So I discuss write leveling and 12:04:32PM
24 read leveling. Hiraishi has all the details on how
25 it does write leveling and read leveling. And

1 putting the two together, it means that you couldn't
2 do Hiraishi -- Hiraishi would not work without the
3 data path going into the data register control
4 circuit.

5 Q. In your declaration, where do you state 12:05:06PM
6 that the DQ data goes into or from the register
7 control circuit?

8 A. Those exact words are not in there. 12:05:24PM

9 However, the words that say that Hiraishi 12:05:26PM
10 does write leveling and read leveling, and by the
11 mere statement of the fact that I say that it
12 performs write leveling and read leveling, it means
13 that it must be doing it -- one of ordinary skill
14 has seen that it successfully is able to do
15 write leveling and read leveling.

16 When you look the details of what it takes 12:05:49PM
17 to do write leveling and read leveling, you see that
18 it has to be done by incorporating the DQ data
19 signal.

20 And so I do not explicitly say that the DQ 12:06:05PM
21 signal goes into the data register control circuit.
22 What I do say is that Hiraishi performs
23 write leveling and read leveling, and in order for
24 that to occur correctly, you have to have the
25 data -- the DQ signal go into the control circuit.

1 Q. Okay. In your declaration you mentioned 12:06:31PM
2 dummy data being used during leveling.

3 A. Yes. 12:07:28PM

4 Q. Is that the data that you are referring to 12:07:32PM
5 must come from the data register control circuit?

6 MR. CHANDLER: Objection, form. 12:07:52PM

7 A. Well, it doesn't say where the dummy 12:08:17PM
8 data -- Hiraishi doesn't say where the dummy data is
9 coming from. So I'm not assuming that the dummy
10 data is being held in the data register control
11 circuit. It's not necessary. It could be, but it's
12 not required.

13 It would need to be -- it needs to be in 12:08:41PM
14 the data buffer somewhere. There's another example
15 where Figure 5 just doesn't show everything. It's
16 got to hold the dummy data somewhere. But it's not
17 required to be in the control circuit. Whereas,
18 when you do read leveling or write leveling, it is
19 required that you have that -- that you have a data
20 signal going to the control circuit.

21 BY MR. LINDSAY: 12:09:13PM

22 Q. Okay. Going back to the annotated version 12:09:13PM
23 of Figure 5 in your declaration under
24 Paragraph 129 --

25 A. Okay. 12:09:29PM

1 Q. -- what are the red lines? 12:09:29PM

2 A. The red lines are all signals that -- 12:09:39PM

3 shown in Figure 5 that -- well, in fact, not all of

4 them. Most of them originate -- all the red lines

5 originate from the data register control circuit,

6 but it's not all the -- it's not all the lines that

7 come from the data register control circuit, it's a

8 subset of them.

9 Q. So are they control signals? I'm trying 12:10:13PM

10 to understand.

11 A. They're not all control signals, no. I 12:10:16PM

12 can tell you which ones are, if you would like.

13 Q. Sure. If you could walk me through that. 12:10:24PM

14 A. Sure. So there is a -- the first signal 12:10:27PM

15 on the far right bottom that goes to the INB buffer,

16 that is a control signal for enabling the INB buffer

17 to allow it to operate.

18 The signal to the left of that marked BC, 12:10:46PM

19 that signal is for controlling the output buffer.

20 That is also a control signal.

21 The next signal to the left of that, SEL, 12:10:57PM

22 is a signal for performing a selection, selecting

23 331, 332, 333 and 334.

24 And now going around to the left side, the 12:11:13PM

25 bottom left side, that next signal is also a control

1 signal, which controls the enabling of the output
2 buffer.

3 So those are the ones that are marked in 12:11:32PM
4 pink. But there is one more signal, if you're
5 interested in that, which comes from the
6 write leveling circuit, and that goes and it drives
7 the DLL circuit.

8 Q. Okay. What does that signal from the 12:11:50PM
9 write leveling circuit 322 to the DLL circuit 310
10 do?

11 A. What it does is it controls the DLL 12:12:02PM
12 circuit in order to be able to adjust the LCLKW --

13 When I say LCLKW, I mean L-C-L-K-W. 12:12:12PM

14 What it does, it controls the DLL circuit 12:12:20PM
15 in order to adjust the LCLKW signal.

16 Q. And how is it -- how is it trying to 12:12:35PM
17 adjust it?

18 A. Well, now we need to go to Hiraishi. But 12:12:39PM
19 it has to do with write leveling.

20 What it's doing is it's adjusting the 12:12:46PM
21 LCLKW signal so that the DQS signal going from the
22 data buffer to the memory device is in sync or in
23 phase with the clock that is at the memory device.

24 Q. Okay. And then what is the LCLKR signal 12:13:24PM
25 that's coming out of the DLL circuit?

1 A. What that signal does is to clock out the 12:13:32PM
2 data from the FIFO read circuit, and it's also
3 involved in the generation of the DQS signal that
4 gets sent back to the memory -- to the memory
5 controller.

6 Q. Can you explain what you mean by "involved 12:14:11PM
7 in the generation of the DQS signal that gets sent
8 back to the memory controller"?

9 A. Well, what it does is it generates -- it 12:14:19PM
10 provides an input to the strobe generating circuit,
11 so that the strobe that gets sent back to the memory
12 controller is in phase, or in other words, in sync,
13 with the data that comes out of the FIFO.

14 Q. And it can be in sync because the same 12:14:46PM
15 LCLKR is clocking out the data from the FIFO 302 and
16 being used to generate the strobe signal that's
17 output from 376? Do I have that right?

18 A. It can generally, yes. I mean, I think 12:15:10PM
19 that the memory controller will probably need to do
20 a tuning of that, but it will generally attempt to
21 come out in sync. It may not be in sync by the time
22 to gets to the memory controller, but yeah, that's
23 the intention, that the two signals come out in sync
24 with each other.

25 Q. Right. Okay. So the data buffer 300 is 12:15:40PM

1 trying to synchronize the DQS and the DQ data at its
2 output, right?

3 A. Yes. It's trying to. But it may not -- 12:16:01PM
4 again, it may not be perfect. Just like every
5 device has a certain amount of tolerance, there's
6 going to be certain tolerance involved there. But
7 that's the intent. That's the intention.

8 Q. Okay. And when you say every device has a 12:16:17PM
9 tolerance, are you referring to just the design
10 tolerances around timing generally?

11 A. Well, what I mean is that, you know, it's 12:16:41PM
12 impossible for every -- it's impossible for every
13 device, when you take into account all of the
14 different variables involved in an operation of an
15 electronic device, for it to be -- for the timing to
16 be perfect.

17 So when I say that, you know, it's 12:17:00PM
18 attempting to, it's doing the best it can, but
19 there's going to be various variables in
20 temperature, process, voltage fluctuations,
21 crosstalk, that could cause it to not be perfect.

22 Q. Understood. Would that apply to, I mean, 12:17:23PM
23 all the components inside of, in our example here,
24 Figure 5?

25 A. It applies to every component in every 12:17:33PM

1 electronic system that I've ever worked with.

2 Q. And then the orange dashed lines in 12:17:44PM
3 Figure 5 that we've been looking at, what are those
4 indicating?

5 A. Those indicate the DQS path that's 12:17:57PM
6 followed from the input from the memory device to
7 the latching in the FIFO.

8 Q. So those are the strobe signals? 12:18:13PM

9 A. Those are the DQS strobes, yes. 12:18:16PM

10 Q. And then there's an input labeled DRC into 12:18:21PM
11 the data register control circuit.

12 What is -- what is DRC? 12:18:32PM

13 A. I don't know exactly what it stands for. 12:18:36PM
14 Data register control -- I could only guess. They
15 never defined the actual, at least I don't remember
16 them defining what it actually is.

17 But the purpose of it is in order to 12:18:50PM
18 communicate to the data buffer from the module
19 controller, in order to tell it whether you are
20 going to do a read or write operation. Basically to
21 instruct the data buffer what type of -- what type
22 of function is going to go on now.

23 Q. So is it a -- so it receives commands? 12:19:15PM

24 A. It receives -- yeah. I mean it receives 12:19:22PM
25 signals. It receives instructions. It receives

1 commands. It receives information of what's going
2 on in the system so that the data buffer can perform
3 correctly. That there's going to be a read, there's
4 going to be a write, that there's going to be a
5 read leveling and a write leveling. It basically
6 instructs the data buffer kind of what to do next.

7 Q. Where do those signals originate? 12:19:51PM

8 A. They come from the module controller, 12:19:54PM
9 which is shown in Figure 6.

10 MR. CHANDLER: I had an objection to form 12:20:01PM
11 if you can give me a moment.

12 THE WITNESS: I'm sorry. A little too 12:20:04PM
13 fast. Thank you.

14 BY MR. LINDSAY: 12:20:18PM

15 Q. Do the signals that are input as DRC 12:20:18PM
16 signals come from the memory controller?

17 MR. CHANDLER: Objection, form. 12:20:29PM

18 A. Not directly, no. I mean, no, the DRC -- 12:20:31PM
19 the origin of the DRC signals are from the module
20 controller of Figure 6. I'm looking at it right
21 here. It's at the bottom center of Figure 6.

22 BY MR. LINDSAY: 12:20:53PM

23 Q. And then what does DRF mean? 12:20:53PM

24 A. DRF is feedback information. It's 12:20:57PM
25 feedback. This is the data buffer instructing or

1 giving information back to the module controller
2 about its operation.

3 Q. So DRF is conveying status or state 12:21:16PM
4 information?

5 A. It's providing whatever information it 12:21:21PM
6 needs to provide. They don't go into detail about
7 that in Hiraishi, but they just say that it provides
8 feedback.

9 Q. In Paragraph 89 of Hiraishi, I'll just 12:21:36PM
10 read it, it says, "The feedback signal DRF is a
11 signal indicating a current status of the data
12 register buffer 300."

13 A. Okay. I'm going to accept that that's 12:21:52PM
14 what it says. That sounds correct.

15 So it gives status. It tells, as I think
16 I said, it tells you what, you know, what the data
17 buffer is doing.

18 Q. So Hiraishi says it provides a current 12:22:14PM
19 status of the data register buffer 300. Are you
20 saying it does something more than that?

21 A. Well, "status" is a very broad word. I 12:22:22PM
22 mean, all information, you know, could be considered
23 status. So it provides whatever information -- it
24 provides whatever information is needed by the
25 module controller.

1 And, you know, that's reported back -- 12:22:49PM
2 that's reported from the data buffer to the module
3 controller. So, I mean, it says the word "status,"
4 but it's basically just information.

5 Q. It's information about the data register 12:23:06PM
6 buffer though, right?

7 A. Yeah. It's status about the operation of 12:23:10PM
8 the data register buffer, yes. I mean, it's coming
9 from -- it's not being passed through, it's not
10 coming from somewhere else. The connection is
11 between the data register buffer and the module
12 controller, and it is passing information between
13 those two devices.

14 MR. LINDSAY: This might be a good time 12:23:43PM
15 for a lunch break, if you would like.

16 THE WITNESS: That's fine. 12:23:50PM

17 MR. CHANDLER: Should we aim for 1 p.m.? 12:23:52PM

18 MR. LINDSAY: It works for me. 12:23:59PM

19 THE WITNESS: Sounds good. 12:24:00PM

20 THE COURT REPORTER: We're going off the 12:24:03PM
21 record.

22 (Recess was held from 12:24 p.m. until 12:59 p.m.) 12:53:11PM

23 THE COURT REPORTER: We're back on the 12:59:43PM
24 record.

25

1	BY MR. LINDSAY:	12:59:45PM
2	Q. Dr. Wedig, still looking at Figure 5, the	12:59:54PM
3	annotated version in your declaration in	
4	Paragraph 129 of Hiraishi's Figure 5.	
5	A. Okay.	1:00:08PM
6	Q. Besides the data register control circuit	1:00:10PM
7	320, is there any other control circuitry in data	
8	buffer 300?	
9	A. There is nothing -- oh, sorry about that.	1:00:21PM
10	Let me fix my video. Hang on one second. Okay.	
11	There we go.	
12	I see no other data register control	1:00:44PM
13	circuit shown in Figure 5, other than the one shown	
14	320.	
15	Q. So there's no other control circuitry	1:00:52PM
16	shown in data buffer 300 than the control circuit	
17	320?	
18	A. Not shown. There's nothing more shown in	1:01:04PM
19	Figure 5, if that's your question, nothing more	
20	shown in Figure 5.	
21	Q. Okay. Yes.	1:01:12PM
22	Does Hiraishi disclose anywhere else	1:01:12PM
23	control circuitry in the data buffer, except for the	
24	data registry control circuit?	
25	A. Yes. Hiraishi discusses a lot that needs	1:01:28PM

1 to be done in the data buffer. And as to whether
2 it's all done inside -- all of the work that the
3 data buffer needs to do, you could annotate it as
4 being done in the data registry control circuit.
5 But the amount of work that needs to be done by the
6 data registry control circuit is not limited to the
7 words found in this figure.

8 So there is no other data registry control 1:02:06PM
9 circuit shown in Figure 5. It doesn't mean that
10 there isn't a lot of control that needs to be done
11 in the data buffer of Hiraishi.

12 Q. So looking at the figure, there's a dashed 1:02:22PM
13 orange line going down from delay circuit 372 to
14 FIFO 302.

15 Do you see that? 1:02:33PM

16 A. Yes, I do. 1:02:33PM

17 Q. What is that signal? 1:02:35PM

18 A. That's a tuned version of the DQS signal. 1:02:38PM

19 Q. In your opinion, is that the first delayed 1:02:50PM
20 read strobe of the claims of the '506 Patent?

21 A. Yes. It says it right above that. "The 1:03:19PM
22 DQS signal supplied to FIFO read circuit 302."
23 Immediately above that figure, that's exactly what
24 it says.

25 Q. So that's what you are equating with the 1:03:34PM

Page 101

1 claimed term "first delayed read strobe"?

2 A. No. I mean it says BC. But, yeah, that's 1:03:46PM
3 what I was thinking about, yes.

4 Q. And in your opinion, that delayed read 1:03:56PM
5 strobe from 372 is sampling the read data in the
6 FIFO 302?

7 A. Yes. It would have to. If it doesn't 1:04:07PM
8 sample it, how is it going to capture it?

9 Q. So what makes you think that the signal is 1:04:17PM
10 sampling -- that signal in particular is sampling
11 the read data in the FIFO 302?

12 A. Well, the data comes into the FIFO from 1:04:33PM
13 the DQ signals, through the selector, 34, and it
14 goes into the FIFO. You see that in Figure 5.

15 Q. Right. 1:04:48PM

16 A. It has to be able to capture it. It has 1:04:50PM
17 to capture it or else it's never going to -- the
18 FIFO will not be able utilize it. I mean you've got
19 to clock it in.

20 And the signal from 372 is exactly what 1:05:06PM
21 it's there for. Because as we understand for the
22 way DDR signals work, it's a source synchronous
23 clocking system. The clock, the mechanism that
24 tells you whether the data is available or not, is
25 the DQS signal.

1 So, therefore, it's obvious that the DQS 1:05:41PM
2 signal is being used to capture, to clock, or to
3 sample the data that is in the first stage of the
4 FIFO.

5 Q. So is it that the first signal into that 1:06:04PM
6 FIFO has to be the signal that's latching the data
7 or sampling the data, because otherwise it wouldn't
8 be available for anything else?

9 MR. CHANDLER: Objection, form. 1:06:22PM

10 A. So you said the first signal. When you 1:06:25PM
11 saying the first signal --

12 BY MR. LINDSAY: 1:06:31PM

13 Q. The first thing that -- let me strike the 1:06:31PM
14 question.

15 A. Okay. 1:06:35PM

16 Q. Is it the case that the first thing that 1:06:38PM
17 has to happen in the FIFO is for the data to be
18 latched or sampled in order for the data to be
19 available for storing or further processing?

20 A. It has to be -- yes, it has to be sampled 1:06:57PM
21 by the DQS signal. So the first thing that has --

22 Well, let's put it this way: The only 1:07:05PM
23 thing that's taught in Hiraishi is that the DQS
24 signal gets delayed and then it's passed to the
25 FIFO.

1 One of ordinary skill knows that the whole 1:07:24PM
2 purpose of the DQS signal is in order to capture or
3 to sample the DQ data inside the data eye in order
4 to be able to utilize it.

5 So, to me, it's completely obvious that 1:07:46PM
6 the DQS signal, after it went through the delayed
7 circuit 372, is capturing the data DQ during the
8 data eye, in the middle of the data eye, and it's
9 being optimized inside 372.

10 Otherwise, you're never going to be able 1:08:09PM
11 to capture -- you're never going to be able to
12 utilize the data, because it won't be in the FIFO if
13 you don't sample it.

14 Q. What about the red line, though, coming 1:08:24PM
15 down into the FIFO, couldn't that be sampling the
16 read data?

17 A. The LCLKR signal is what you are referring 1:08:33PM
18 to?

19 Q. Yes. 1:08:37PM

20 A. Yeah, that's not -- that's not what's 1:08:39PM
21 taught. In fact, you have to -- you've got to
22 accept it in, and then the FIFO delays it, and then
23 you have to read it out.

24 First of all, it would be impossible to 1:08:53PM
25 sample the data with the LCLKR, because the LCLKR

1 doesn't know whether the data is valid. It's only
2 the DQS signal that tells you when the value on the
3 DQ signal is valid. So it's got to be the DQS
4 signal. LQR would not know when the data is valid.

5 Until it gets into the FIFO and now it's 1:09:30PM
6 being passed down the line, and it takes that value
7 after it's been captured already, then LQR passes it
8 out to the memory controller.

9 Q. What do you mean, passes it out? 1:09:46PM

10 A. What I mean is that it goes through the 1:09:51PM
11 FIFO. FIFO does what FIFOs do, and it is first
12 in/first out. It takes the data, passes it down the
13 FIFO, and then the LCLKR signal clocks it. It's a
14 clock. It clocks it in order to send it on to the
15 next point. It goes out of the data buffer to the
16 memory controller.

17 Q. So that signal clocking out the data 1:10:19PM
18 cannot sample the data?

19 MR. CHANDLER: Objection, form. 1:10:27PM

20 A. No, it can't, because it doesn't know when 1:10:30PM
21 the data is there, until it's gotten into the FIFO.
22 LCLKR does not know if the data on the -- it does
23 not know if the value on the DQS signal holds a
24 valid value. That information is provided by DQS.

25 So DQS transitions, it becomes active, 1:10:56PM

1 when the data is valid. So you have to use DQS.
2 One of ordinary skill sees that, and I don't
3 understand why that isn't completely obvious. I
4 mean, it seems completely obvious to me.
5 BY MR. LINDSAY: 1:11:26PM
6 Q. Okay. Fair enough. 1:11:26PM
7 Can we go to a different exhibit. This 1:11:26PM
8 was previously introduced as Exhibit 4. It's the
9 JEDEC DDR3 standard for memory devices.
10 A. Okay. 1:11:44PM
11 (Discussion off the record.) 1:12:03PM
12 THE WITNESS: I'm sorry, which exhibit 1:12:03PM
13 number are you interested in?
14 BY MR. LINDSAY: 1:12:20PM
15 Q. It's Exhibit 4. 1:12:20PM
16 A. Okay. 1:12:23PM
17 Okay. I've got it. 1:12:23PM
18 Q. Apologies. One second here. 1:12:39PM
19 Does the exhibit say Exhibit 1020 in the 1:12:40PM
20 lower right corner?
21 A. Yes, it does. 1:13:37PM
22 Q. Okay. So this is Exhibit 1020 from the 1:13:38PM
23 IPR. I think you cited to this in your declaration,
24 right?
25 A. Yes. Yes, I did. 1:13:46PM

1 Q. Okay. Can you turn to -- it would be 1:13:47PM
2 Page 163 as it's been labeled in the bottom right
3 corner. There's a couple different page numbers
4 around. And it's Table 65. Okay?

5 A. Actually, if you don't mind, I'm looking 1:14:17PM
6 at a paper copy of it. But I have that in front of
7 me.

8 Q. Okay. That's fine. 1:14:25PM
9 What is this table describing? 1:14:26PM

10 A. It says it's a "Timing Parameters by Speed 1:14:31PM
11 Bin" is the way it's titled. And this is showing
12 the timing parameters for various different speed
13 DDR3 memory devices.

14 Q. Okay. So the columns that are labeled 1:14:52PM
15 DDR3-800, DDR3-1066, and so on, is that referring to
16 different DDR3 memory speeds?

17 A. That's my understanding, yes. 1:15:08PM

18 Q. Now, for each of those speeds, there are 1:15:11PM
19 two columns of information below labeled "Min" and
20 "Max"; is that right?

21 A. I see that, yes. 1:15:19PM

22 Q. Why does each memory speed have this 1:15:20PM
23 further Min/Max timing columns?

24 A. Well, as I said earlier, you know, all 1:15:28PM
25 devices are -- there is the ideal, and then there's

Page 107

1 reality that you try to make a device that operates
2 with a particular parameter, but there is a
3 recognition that in the real world, not everything
4 operates in the ideal sense.

5 So what manufacturers do is they make 1:15:56PM
6 devices and they test them extensively to determine
7 what is the reality of the device. So they will --
8 these numbers that we see here are guarantees to
9 their customers that the various parameters that
10 they're measuring will operate within these bounds,
11 that they'll operate between a certain minimum and
12 maximum value.

13 Q. The table continues on the next page and 1:16:42PM
14 there's a section in the left most-column called
15 "Data Timing."

16 Do you see that? 1:16:49PM

17 A. Not exactly. I'm sorry. So I'm on 1:16:58PM
18 Page 165 now.

19 Are you looking at 164? 1:17:03PM

20 Q. Yeah, 164. 1:17:07PM

21 A. Oh, I'm sorry. 1:17:09PM

22 Data timing. I see that, yes. 1:17:09PM

23 Q. What information is this data timing 1:17:16PM
24 section conveying, as you understand it?

25 A. This is giving data timing that's in 1:17:29PM

Page 108

1 relation to the DQ and DQS signals.

2 Q. Okay. And the first row under that 1:17:40PM
3 section is called "DQS, DQS# to DQ skew, per group,
4 per access."

5 Do you see that? 1:17:57PM

6 A. Yes, I do. 1:17:58PM

7 Q. And then its symbol tDQSQ. Right? 1:18:02PM

8 A. Yes, I see that. 1:18:13PM

9 Q. And there's a Min and Max for each memory 1:18:17PM
10 speed for this row as well?

11 A. Yes, I see it. 1:18:25PM

12 Q. What is this value and what information is 1:18:27PM
13 being conveyed in this row?

14 A. Okay. What's being provided here is to 1:18:34PM
15 show the difference in timing between the value that
16 is output by a DQ signal and the value that is
17 provided by a DQS signal.

18 So it's showing what we would call the 1:18:58PM
19 skew, that is, the difference in phase or the
20 difference in the time of change between when a DQS
21 signal activates and a DQ signal activates.

22 Q. And in the column for memory speed 1:19:25PM
23 corresponding to DDR3-800, there's a number 200 in
24 the Max column, right?

25 A. Yes, I see that. 1:19:43PM

1 Q. And that's a picoseconds dimension, right? 1:19:48PM

2 A. Correct. Yes, it's in seconds. The unit 1:19:53PM

3 is seconds and it's in picoseconds, yeah, which is

4 very, very fast.

5 Q. And so at 200 picoseconds, what would be 1:20:03PM

6 the relationship between the DQS and the DQ data?

7 A. So what that means -- 1:20:18PM

8 MR. CHANDLER: Objection, form. 1:20:19PM

9 A. What that means is that this device can be 1:20:24PM

10 sold and would be considered operating within its

11 bounds if the DQS signal were activated, and then up

12 to 200 picoseconds later the DQS signal were

13 activated on the output of the pins of this memory

14 device.

15 So there can be a skew that is a 1:20:58PM

16 difference in time between when the DQS signal

17 activates and the DQ signal activates up to

18 200 picoseconds, and it would still be considered

19 operating within the margins of the manufacturer's

20 specifications.

21 BY MR. LINDSAY: 1:21:21PM

22 Q. I see. And so whatever component is 1:21:21PM

23 receiving that DQ and DQS would receive the DQ and

24 DQS with that skew, whatever it is, up to --

25 assuming it's within operational parameters, between

1 zero and 200 picoseconds skewed?

2 A. Well, in fact, that's a good point, 1:21:50PM
3 because what this says is that it will output these
4 signals with up to a 200-picosecond skew. It may
5 receive it with a possibly even large larger skew.
6 Your statement that you made was that a device would
7 receive it with up to a 200-picosecond skew. It
8 could be more because of line lengths, crosstalk,
9 temperature, all the things that can affect -- all
10 the things that can affect the operational signals
11 within a system.

12 So the best that this can say is that on 1:22:33PM
13 the output pins of the memory device, there can be
14 up to a 200-picosecond skew. It could be received
15 possibly with something even greater.

16 Q. Of course, yes. 1:22:53PM

17 So this is from the perspective of the 1:22:53PM
18 memory device?

19 A. That's correct. This is a specification 1:22:56PM
20 for the memory device, right.

21 Q. So this table isn't talking about skew of 1:23:03PM
22 data that is received, there is no way it could
23 know, right? It can only know what it's sending.
24 So this is a table describing a skew between DQ and
25 DQS that is being sent by the memory device to some

1 other component?

2 A. That's right. 1:23:27PM

3 Q. Okay. Now, I noticed as you go across 1:23:28PM
4 this row from left to right that the Max timing
5 parameter is decreasing. Do you know why that would
6 be?

7 A. Well, as I said earlier, this is what the 1:23:51PM
8 manufacturers test and this is what they guarantee.
9 I think it's going to be -- you're going to have to
10 try and reduce that skew. As you go across to the
11 right, the devices get faster. In fact, the
12 DDR3 1600 is twice as fast as the DDR3 800.

13 So if you don't reduce that -- if you 1:24:19PM
14 don't reduce that skew, then you're going to make it
15 very difficult for the user to be able to utilize
16 these signals, because the clock has become so fast.

17 Q. Okay. I think I want to jump back to the 1:24:46PM
18 exhibit we previously introduced as Exhibit 6, the
19 Zumkehr, I think we called it, Zumkehr reference.

20 A. Exhibit 6. Okay. I'm there. 1:25:05PM

21 Q. So you had discussed this reference in 1:25:14PM
22 your declaration in the context of explaining
23 Hiraishi and Hiraishi's read leveling, I believe; is
24 that correct?

25 A. Yes, I did. 1:25:30PM

Page 112

1 Q. So in your opinion, Zumkehr is performing 1:25:35PM
2 the same type of fine-tuning I think was the term
3 that Hiraishi describes; is that right?

4 A. Yeah. As part of the read leveling, yes, 1:25:48PM
5 uh-huh.

6 Q. And so in Figure 3, if we can look at 1:25:53PM
7 Figure 3 for a moment, of Zumkehr.

8 A. Okay. I see it. 1:26:06PM

9 Q. So Zumkehr discloses that a delay is 1:26:07PM
10 applied by variable delay 320; is that right?

11 A. I see that, yes. 1:26:16PM

12 Q. And variable delay 320 is being controlled 1:26:19PM
13 by memory controller or some logic inside memory
14 controller, correct?

15 A. Yes. It appears to be, the best I can 1:26:35PM
16 see, it appears to be controlled by what's called
17 the MC data eye search state machine 315.

18 Q. Okay. Maybe we should look at a citation 1:26:47PM
19 too.

20 So in column 7, line 55. 1:26:55PM

21 A. Okay. So I'm going to have to leave this 1:27:03PM
22 diagram.

23 Okay. I see that. 1:27:28PM

24 Q. Okay. And then the other side of that on 1:27:30PM
25 column 8, line 7, talks about memory controller

1 instructing variable delay 320 to increase.

2 A. Correct. 1:27:48PM

3 Q. So is it the case that the memory 1:27:48PM
4 controller 300 is controlling the variable delay 320
5 to either increase or decrease the delay that's
6 applied?

7 A. Well, yeah. I mean, the memory controller 1:28:10PM
8 has the ultimate control, but it's instructing this
9 variable delay unit 320. So the variable delay unit
10 320 is doing the increasing or decreasing under the
11 instruction from the memory controller.

12 Q. So in your experience, this type of 1:28:38PM
13 variable delay circuit 320 would require a control
14 signal?

15 A. It has to. I mean, everything uses a 1:28:50PM
16 control signal. You're going to have to be able to
17 tell it what it do. It doesn't just operate on its
18 own.

19 Q. Right. And that would be the case with 1:29:03PM
20 Hiraishi's delay circuit as well, it would require a
21 control signal?

22 A. It would need some type of a control 1:29:16PM
23 signal in order to do that, yes. I mean, again, it
24 doesn't just freely decide when to do things. It
25 has to operate in a way that it knows what to do,

Page 114

1 when to do it.

2 Q. Do fixed delay circuits require a control 1:29:41PM
3 signal?

4 A. What do you mean by a fixed delay circuit? 1:29:47PM

5 Q. Circuitry that applies a fixed amount of 1:29:52PM
6 delay to a signal it receives.

7 A. Something where the delay is predetermined 1:30:04PM
8 that it's an absolute numeric value that's
9 unchanging, is that what you are referring to?

10 Q. Correct. 1:30:13PM

11 A. Yeah, if you're not going to in any way 1:30:14PM
12 modify the delay, if you're not going to try to tune
13 it to get an optimal value, then there would be no
14 need to be able to control it, because it would be
15 built into the design to be able to give a
16 predetermined delay.

17 Q. Okay. I want to move over to the Butt 1:30:49PM
18 reference. I believe we introduced this earlier as
19 Exhibit 7.

20 A. By the way, before we do that, I might 1:30:59PM
21 just point out, I happened to do a search on
22 Zumkehr.

23 Q. Sure. Okay. 1:31:09PM

24 A. No, I take that back. 1:31:29PM

25 I'm sorry. Forget that. Let's go on. 1:31:30PM

Page 115

1 Q. Okay. 1:31:34PM
2 A. I'm sorry, what exhibit are you looking 1:31:39PM
3 at?
4 Q. The Butt reference. We previously 1:31:41PM
5 introduced it as Exhibit 7. In the IPR it was
6 Exhibit 1029.
7 A. Hang on a second. Let me get there. Hang 1:31:54PM
8 on.
9 I'm sorry, one more time. The exhibit 1:32:17PM
10 number was what again?
11 Q. Exhibit 7. 1:32:20PM
12 A. Exhibit 7. 1:32:22PM
13 Q. Well -- 1:32:23PM
14 A. Yep. Okay. I'm there. 1:32:26PM
15 Q. Okay. So if we can look at Paragraph 3 in 1:32:29PM
16 the Butt reference.
17 A. Okay. Paragraph 3. 1:32:41PM
18 Yes. Okay, I'm there. 1:32:42PM
19 Q. So there's a sentence -- I'll just read a 1:32:47PM
20 couple of sentences we can read them together.
21 "Conventional approach" -- maybe I should 1:32:51PM
22 back up.
23 A. Yeah. 1:32:58PM
24 Q. You can just read through that, and then 1:32:59PM
25 I'll pick out a sentence or two.

Page 116

1	A. Okay.	1:33:05PM
2	Q. Let me know when you're done reviewing.	1:33:09PM
3	A. Okay. Sorry. I was going to read along	1:33:12PM
4	with you.	
5	Okay, I read Paragraph 3.	1:33:42PM
6	Q. So one of the sentences in this paragraph	1:33:49PM
7	says that "A conventional approach performs a	
8	system-level timing analysis using a simulation	
9	program or integrated circuit emphasis" -- or SPICE	
10	as the acronym -- "to determine a timing that yields	
11	adequate setup and hold time margins within a data	
12	valid window."	
13	A. I see that.	1:34:16PM
14	Q. Okay. And what is this describing so far?	1:34:17PM
15	A. What this is describing is what would be	1:34:23PM
16	done in most all system designs, that is, to perform	
17	simulations on your design to make sure that it	
18	operates correctly across a variety of parameters.	
19	Q. Sure. I'm sorry. Let me ask a better	1:34:46PM
20	question.	
21	A. Okay.	1:34:50PM
22	Q. Is the operation that they're simulating	1:34:53PM
23	the centering of latching data, incoming data into a	
24	storage device?	
25	MR. CHANDLER: Objection, form.	1:35:17PM

Page 117

1 This says that they do SPICE-level 1:37:19PM
2 analysis to try and determine a timing and a yield
3 that is adequate for the setup and hold time margins
4 within a valid data window.

5 So there is a data window. There is a 1:37:34PM
6 data window where the data is supposed to be valid.
7 There's a setup and a hold time for when that data
8 starts to be valid and for when data is going to end
9 being valid. And they're trying to determine the
10 data margins for that.

11 It's well-known, by one skilled in the 1:37:55PM
12 art, that the DQS does not exit the memory device
13 with the transition in the middle. It exits with
14 the DQS being edge aligned, where the DQS changes
15 when the data first goes valid, and then it changes
16 again when the data goes invalid.

17 And so that's what it's talking about, the 1:38:26PM
18 setup and hold times of the beginning of that window
19 and end of the window, not finding the time in the
20 middle. That's the whole purpose of what Butt is
21 trying to do, is to now take the margins that you
22 are given for the beginning and the end and find
23 what is the best place in the middle.

24 Q. Right. Okay. 1:38:51PM

25 So I guess in Hiraishi, Hiraishi describes 1:38:55PM

1 adding about 90 degrees delay using the delay
2 circuit 372, right?

3 A. It says the words "about 90 degrees," in 1:39:13PM
4 order to take into account that if the world were
5 perfect, it would only have to add 90 degrees.

6 But as we just talked about in relation to 1:39:23PM
7 JEDEC, even the JEDEC standard says you don't have
8 to output it perfectly. It could be off by as much
9 as 200 picoseconds, and it would still satisfy the
10 spec.

11 And so already we know that a 1:39:40PM
12 JEDEC-compliant device is going to be putting out
13 data in the data strobe that are 200 picoseconds --
14 up to 200 picoseconds off from each other.

15 So now if we do a 90-degree delay of the 1:40:00PM
16 DQS, that makes us not in the middle. We're already
17 not in the middle. All the more motivation that you
18 need to do fine-tuning in order to get that in the
19 middle to have a successful, highly reliable part.

20 So, to me, the JEDEC standard, and what 1:40:24PM
21 this is saying here too, is reinforcing that it's
22 necessary to do this fine-tuning in order to make
23 sure that you've got -- that you reliably receive
24 the data and sample it at the right time.

25 Q. Okay. So I'm going to ask about the Butt 1:40:50PM

1 reference here. So Butt tests different offsets
2 from a base delay, right, to determine the Min and
3 Max acceptable offsets to apply to a strobe signal?

4 A. Sure. 1:41:14PM

5 Q. And that base delay is like Hiraishi's 1:41:15PM
6 base delay of 90 degrees?

7 A. Yeah. I never saw -- I don't remember 1:41:23PM
8 reading in Butt that they say it's 90 degrees, but
9 that makes complete sense. They started at what
10 they think is a center point, and the hope is, you
11 know, 90 degrees is about the center point, and then
12 they look to the left and they look to the right.

13 So, yeah, that was my interpretation when 1:41:44PM
14 reading Butt that it probably was 90 degrees, but I
15 don't remember seeing the exact words in Butt saying
16 that it was 90 degree.

17 Q. Okay. Let's see. Let's take a look at 1:41:56PM
18 maybe -- I don't know which figure might be best.
19 Maybe Figure 2 in the Butt reference. Do you have
20 that available?

21 A. Okay. I'll get to it. 1:42:17PM

22 All right. I'm at Figure 2. 1:42:21PM

23 Q. Okay. So towards the bottom of Figure 2, 1:42:23PM
24 there's a component called master delay 116.

25 Do you see that? 1:42:33PM

Page 121

1	A. Yes, I see it.	1:42:34PM
2	Q. And then out from that it says "base delay	1:42:36PM
3	(to each DP)." I'm assuming that means data path.	
4	A. Yes, I see that.	1:42:45PM
5	Q. Is it your understanding that that master	1:42:48PM
6	delay is then applying a base delay based on that	
7	clock signal that it's receiving?	
8	A. That seems to make sense. I mean it says	1:43:01PM
9	"base delay." And then if we look at the detail of	
10	114 in the next figure, Figure 3A, you see the words	
11	"base delay UN." And so it has the same word. So,	
12	yeah, that makes sense to me that that applies to	
13	base delay.	
14	Q. Okay. And all it needs is the clock	1:43:27PM
15	signal to apply that?	
16	MR. CHANDLER: Objection, form.	1:43:36PM
17	BY MR. LINDSAY:	1:44:02PM
18	Q. If you want to look at Paragraph 21.	1:44:02PM
19	A. Okay.	1:44:05PM
20	Q. Save us a little bit of time.	1:44:12PM
21	A. Sure. Let's do that. Paragraph 21.	1:44:14PM
22	Thank you.	
23	Okay, I've read 21, yes. And that didn't	1:45:06PM
24	say 90 degrees, but it does say one-quarter cycle,	
25	which is essentially the same as 90 degrees.	

Page 122

1 So I've read 21. What's your question? 1:45:19PM

2 Q. So I guess in Paragraph 21, it refers to 1:45:22PM

3 it as delay lock loop. My question is, does the

4 master delay 116 generate the base delay based on a

5 clock signal?

6 A. Yes. What it does is it uses the clock 1:45:58PM

7 signal, it delays it by 90 degrees, and then it adds

8 in the offset -- that's a programmable offset -- and

9 then it uses that to control the variable delay

10 mechanism 124 that's shown in Figure 3A.

11 So it's using the offset plus -- the base 1:46:22PM

12 plus the offset, and it's using that as the input

13 for controlling the delay mechanism 124.

14 Q. So delay circuit 116 is not receiving a 1:46:40PM

15 control signal, just a clock signal?

16 A. It's not receiving a control signal yet. 1:46:50PM

17 I mean -- well, 116 is -- that's a free-running

18 clock. I agree. But the control signal for when to

19 actually do the sampling comes from the DQS that's

20 shown in Figure 3A.

21 Q. Right. 1:47:12PM

22 A. And so the 116 is applying an offset, an 1:47:14PM

23 offset clock, that's going to be added to the -- I'm

24 sorry, I don't mean to confuse words here.

25 It's going to send a clock that is shifted 1:47:30PM

1 by one-quarter clock to be added to the offset delay
2 parameter, that's the programmable parameter, and
3 then that all is applied as a control input to the
4 delay mechanism 124.

5 Q. Okay. That makes sense. 1:47:56PM

6 But the part of the delay that's applied 1:47:59PM
7 by master delay circuit 116, that's a set or fixed
8 delay?

9 A. That's a free-running clock. That's a 1:48:10PM
10 free-running clock that has been shifted by one
11 quarter clock. That part is free-running.
12 Free-running meaning there's no additional control
13 on it.

14 Q. Okay. 1:48:24PM

15 A. If that's what you're wondering. 1:48:28PM

16 Q. Yeah, that was it. Thank you. 1:48:30PM

17 A. Yeah. 1:48:32PM

18 Q. And then in -- I guess maybe back to your 1:48:33PM
19 declaration, if we can look at -- you continue your
20 description in Paragraph 148 of how Butt calculates
21 the offset.

22 A. Okay. Hang on. 1:48:54PM

23 Okay. Do you want me to read all of 148? 1:49:41PM

24 I read part of it. Maybe I'll wait for your
25 question and I'll see whether I need to read the

1 whole thing.

2 Sorry about my video again. I'm not sure 1:49:50PM
3 what happened here. There we go. Okay.

4 Q. Okay. So Butt describes this process of 1:49:56PM
5 iteratively testing memory accesses, right?

6 A. Yes, uh-huh. 1:50:16PM

7 Q. Where is the logic that controls that 1:50:17PM
8 iterative testing process?

9 A. In Butt? 1:50:21PM

10 Q. Yes. 1:50:23PM

11 A. Well, Butt doesn't give a complete memory 1:50:48PM
12 device. I mean Butt gives the actual testing
13 circuitry. Butt is not focused on the actual
14 control mechanism for doing the shifting.

15 I mean, it explains it, it's completely 1:51:14PM
16 explained in Figure 6, Figure 7, the actual control
17 that would need to be done, but it doesn't show a
18 box for it. It just explains what would have to be
19 done.

20 Q. Well, if we look at Figure 2, Figure 2 1:51:33PM
21 shows a memory system, I guess we can call it. It's
22 got a controller, it's got DDR memory, and then it's
23 got the circuit 104 that Butt describes in the
24 middle of it, right?

25 A. I'm sorry, say that one more time. I 1:52:02PM

1 | didn't catch everything you said.

2	Q. Sure.	1:52:07PM
---	----------	-----------

3 THE COURT REPORTER: Would you like me to 1:52:07PM
4 read it back?

5 MR. LINDSAY: No, that's okay. 1:52:07PM

6 BY MR. LINDSAY: 1:52:17PM

7 Q. So Figure 2 -- let's do it this way. It 1:52:17PM
8 might be easier. Strike the question, please.

9	So Figure 1, Butt calls, in Paragraph 8,	1:52:27PM
10	"a block diagram illustrating a memory system in	
11	which an embodiment of the present invention may be	
12	implemented."	

13	And then in Paragraph 9, Butt says,	1:52:42PM
14	"Figure 2 is a more detailed block diagram of a read	
15	logic and signal paths of a memory interface of	
16	Figure 1."	

17	A. Okay.	1:52:56PM
----	----------	-----------

18 Q. So you can pick Figure 1 or Figure 2. 1:52:57PM

19 Figure 2 is little more detailed. But my question

20 is --

21	A. Well, now, wait.	1:53:04PM
----	---------------------	-----------

22	I'm sorry. I should let you ask your	1:53:05PM
23	question. Go ahead.	

24	Q. What component is carrying out Butt's	1:53:10PM
25	iterative testing of memory access? Where is the	

Page 126

1 logic that controls that operation?

2 A. Okay. So the last thing you just read, I 1:53:22PM
3 want to get to it myself. You said it was
4 Paragraph 17?

5 "Referring to Figure 2, a more detailed 1:53:26PM
6 block diagram of the circuit 104 is shown
7 illustrating example read data logic and signal
8 paths in which a preferred embodiment of the present
9 invention may be implemented."

10 This is read data logic and signal paths. 1:53:46PM
11 So it's that part of the system which is made up of
12 the read data logic and the signal paths.

13 So you're talking about the actual data 1:53:58PM
14 flow. This is the data flow portion of the system.
15 They're not pretending to say that this encompasses
16 the entire data buffer. The data buffer would be
17 more than that, and that control portion that you
18 are looking for is being described in Figure 6 and
19 7. But not shown in Figure 2. That's not the
20 purpose of Figure 2.

21 Q. Okay. Fair enough. 1:54:33PM

22 So maybe we should look at -- let's look 1:54:35PM
23 at maybe Paragraph 46.

24 A. Okay. Let me get there. 1:54:58PM

25 Q. So here it's saying that "The optimum 1:55:41PM

Page 127

1 values may be written, in one example, to a
2 respective register (a DP slave delay register)."

3 A. Okay. 1:56:00PM

4 Q. Your control register gives that a name. 1:56:00PM

5 Right? And these are optimum values.

6 By "optimum values," is it referring to 1:56:06PM

7 the optimum strobe offset values that it calculates?

8 MR. CHANDLER: Objection, form. 1:56:15PM

9 A. That's the way I interpret it. The value 1:56:16PM

10 which is going to give you the best reliability for

11 capturing the data. That's my understanding.

12 BY MR. LINDSAY: 1:56:26PM

13 Q. So would you agree that the data path 114, 1:56:27PM

14 which is what's applying this optimum offset delay,

15 is being programmed in order to implement the

16 adjustment?

17 A. Being programmed? It doesn't say it's 1:56:55PM

18 doing it in software. Are you referring to like

19 actually running some type of series of

20 instructions?

21 Q. So, yes. So we can talk about this a 1:57:07PM

22 number of different ways, I suppose.

23 A. Okay. 1:57:14PM

24 Q. Let's go to Figure 6. And I think you 1:57:15PM

25 pointed this out earlier, Figure 6 and 7 had this

1 flow diagram for the process of determining the
2 offset values, right?

3 A. Yep, uh-huh. 1:57:27PM

4 Q. It's incrementing each offset value, and 1:57:28PM
5 then it says programming the DP114 with the selected
6 new offset value. Right?

7 A. Right. 1:57:38PM

8 Q. It then tests the read data at each 1:57:38PM
9 increment?

10 A. Yes. 1:57:42PM

11 Q. And it repeats that until it gets a fail, 1:57:43PM
12 a read fail?

13 A. Correct. 1:57:48PM

14 Q. And at that point you know you are at the 1:57:49PM
15 highest?

16 A. Or lowest. 1:57:51PM

17 Q. Or the lowest. 1:57:54PM

18 A. Uh-huh. 1:57:56PM

19 Q. And then it repeats that process going the 1:57:56PM
20 other direction --

21 A. Uh-huh. 1:58:02PM

22 Q. -- and averages those together. 1:58:05PM

23 My question is: The programming of the 1:58:06PM
24 DP114 with the offset values, the testing of the
25 read data, where is that occurring?

1 A. You are looking for a diagram that shows 1:58:26PM
2 the actual comparison being performed? Is that what
3 you are asking about?

4 Q. I'm just asking, as a person skilled in 1:58:34PM
5 the art reading Butt, even if Butt doesn't expressly
6 explain where it is, what would be your
7 understanding? Would that be in the memory
8 controller, would that be in the memory device,
9 would that be inside this circuit 104? Where --

10 A. I think -- Butt doesn't explain it to that 1:59:00PM
11 level and I think it could be in any of those
12 places.

13 Butt explains about how you need to do 1:59:07PM
14 this fine-tuning. The comparison mechanism could be
15 done right here in 104, it could be done in the
16 memory controller. That's not -- that is not the
17 focus of Butt.

18 The focus of Butt is to show you how to 1:59:25PM
19 shift it, the algorithm to use for going to one end
20 and finding the limit and going to the other end and
21 finding the limit and then going to the middle.

22 The actual comparison mechanism and, you 1:59:41PM
23 know, where the comparison mechanism is performed
24 and, you know, who follows through the sequence of
25 steps, whether that be the memory controller,

1 whether that be a state machine within the data
2 buffer, that is up to the user, and I think one of
3 ordinary skill would understand that you can do that
4 in many different places.

5 There is nothing in the disclosure of Butt 2:00:15PM
6 that would limit you from picking a variety of
7 places.

8 Q. Okay. And what would -- in your view, 2:00:23PM
9 what would be the possible places where you could
10 carry out this testing operation?

11 A. I would think -- as I said, you can do it 2:00:35PM
12 anywhere, but I think a reasonable place to do it
13 would be inside the buffer 104 because that's where
14 the data is sampled. 104 is where the physical data
15 path is, and that's where you are doing the
16 delaying. And that's where the signal comes out.
17 And so the most reasonable place to do it would be
18 to check it -- you know, why not check it right
19 after you have sampled it?

20 Q. So the actual circuitry that Butt uses to 2:01:32PM
21 calculate the optimal offset is not disclosed in
22 Butt?

23 A. The actual circuitry is not shown in any 2:01:44PM
24 of the figures. It's described as an algorithm.
25 It's described as an algorithm, it's described in

1 the text. One of ordinary skill would have no
2 problem designing that based on the description, but
3 there is -- the actual comparison circuitry is not
4 shown in the diagram.

5 Q. And it's not described in the 2:02:10PM
6 specification either?

7 MR. CHANDLER: Objection, form. 2:02:12PM

8 A. That's not true. I mean it's described 2:02:13PM
9 saying that you -- it's described quite clearly. We
10 can go back and look at the text again.

11 But it says that you modify the delay 2:02:22PM
12 value and then you test to see whether the memory
13 access passed or not. And in order to pass, it has
14 to be -- the value that you received has to be the
15 value expected.

16 So the diamond-shape figure in Figure 6 2:02:41PM
17 and Figure 7, it says "test passed," that's a
18 comparison right there. One of ordinary skill
19 clearly knows that that's a decision point, a
20 decision point based on a comparison.

21 BY MR. LINDSAY: 2:03:00PM

22 Q. So I'm sorry, Dr. Wedig, I was referring 2:03:00PM
23 to circuitry. You said, just looking back at the
24 realtime, you said: The actual circuitry is not
25 shown in any of the figures.

1 A. That's correct. 2:03:11PM

2 Q. Is the actual circuitry described in the 2:03:12PM
3 specification?

4 A. The circuitry is described as an 2:03:21PM
5 algorithm. The circuitry, the actual -- the actual
6 individual gates that make up the circuitry are not
7 shown, but the circuitry is, in a sense, described
8 by telling you the algorithm, and then one of
9 ordinary skill can easily generate the circuitry
10 based on the explanation given.

11 Q. Would it make sense to implement that 2:03:54PM
12 algorithm in the memory controller?

13 A. I would say that it's not limited to that, 2:04:01PM
14 but that doesn't seem like the ideal place for me,
15 because now you've got data that -- you've got --
16 the information is being passed further away.

17 So like I said, Butt doesn't limit that, 2:04:17PM
18 but I just don't see that as being the ideal place
19 to do it.

20 Q. And where, in your opinion, is the ideal 2:04:29PM
21 place to do it?

22 A. Right after you -- the ideal place to do 2:04:33PM
23 it would be right after you did the sampling. That
24 would be inside 104, and more specifically, inside
25 114, probably.

1 Q. Just so I guess we're clear, in your 2:05:00PM
2 opinion, the most -- strike that.

3 In your opinion, the best place to perform 2:05:07PM
4 Butt's optimization function is inside the data
5 paths 114?

6 A. Well, either -- within 104, I mean, and, 2:05:20PM
7 you know, possibly within 114. But definitely my
8 best place I would think to do it would be within
9 that data buffer, the DDR, physical DDR PHY, within
10 104 somewhere. Possibly within 114.

11 Q. Let's take a look at paragraph 150, if we 2:05:53PM
12 could, in your declaration.

13 A. Okay. 2:06:04PM

14 Q. So in paragraph 150, you're describing 2:06:22PM
15 what calibration process could be implemented in
16 Hiraishi; is that right?

17 A. Yes, I am. 2:06:34PM

18 Q. And so your opinion is it would have been 2:06:38PM
19 obvious to calibrate Hiraishi's delay circuit 372 in
20 the same manner as Butt teaches?

21 A. Yes, that's what I'm saying. 2:06:51PM

22 What happened to my screen again? Hang 2:06:52PM
23 on. I'm not sure what's in video.

24 Okay. I'm back. 2:06:57PM

25 Q. And you are proposing that the read delay 2:07:05PM

Page 134

1 circuit 323 and delay circuit 372 would iteratively
2 test the memory accesses using different offsets tin
3 the same manner that Butt describes?

4 A. That's what I'm saying, yes. 2:07:23PM

5 Q. Is it the read leveling circuit 323 that 2:07:26PM
6 would then figure out the maximum, minimum, and then
7 optimum offsets, if I have that right?

8 A. Yes. I mean within that -- within that 2:07:42PM
9 logic, yes.

10 Q. And then Hiraishi's read leveling circuit 2:07:45PM
11 323, that would adjust the base delay of that
12 optimum offset?

13 MR. CHANDLER: Objection, form. 2:08:06PM

14 A. Yes, the read leveling circuitry would 2:08:16PM
15 include -- would be basically in control of doing
16 all of that. It would implement the algorithms
17 given in Figure 6 and 7.

18 BY MR. LINDSAY: 2:08:45PM

19 Q. So you are not proposing to add any 2:08:45PM
20 additional circuitry from Butt into Hiraishi's data
21 buffer; are you?

22 MR. CHANDLER: Objection, form. 2:08:57PM

23 A. Additional circuitry into -- well, I mean, 2:09:00PM
24 you would need to be able to implement -- you would
25 need to be able to implement Butt.

1 As I said, I thought that Hiraishi already 2:09:13PM
2 was clear to one of ordinary skill in the art that
3 you needed to perform a tuning. But if you are not
4 satisfied that Hiraishi alone would do it, then Butt
5 makes it even more clear.

6 So additional circuitry? I don't think 2:09:36PM
7 there's any additional circuitry because Hiraishi
8 already discusses it. But if you feel that that's
9 not the case, then Butt would use the circuitry and
10 would use the logic, and you'd teaching from Butt in
11 order to be able to implement the mechanisms needed
12 to perform this fine-tuning.

13 So I don't think it's additional circuitry 2:09:59PM
14 because I think Hiraishi already implied that you
15 had it. But if you feel that Hiraishi did not have
16 it, then you would combine Butt with it.

17 Again, I'm just accepting. If you don't 2:10:12PM
18 buy the fact that it already was built into
19 Hiraishi, then it would be an addition to be able to
20 add the teachings of Butt, and it would be the
21 circuitry that is discussed in Butt in order to help
22 make this fine-tuning mechanism obvious.

23 BY MR. LINDSAY: 2:10:54PM

24 Q. I think I understood what you are saying, 2:10:54PM
25 but reading the realtime, I'm not sure. I

1 understand your position that you can implement
2 Butt's algorithm using Hiraishi's read leveling
3 circuit and delay circuit.

4 The question is, you're not proposing to 2:11:15PM
5 add any additional circuitry from Butt that's not
6 already in Hiraishi. Is that fair to say?

7 MR. CHANDLER: Objection, form. 2:11:28PM

8 A. Only because I believe that the 2:11:31PM
9 fine-tuning mechanism already exists in Hiraishi.
10 It already teaches it. It's already there. And so
11 Butt, in that sense, is not even absolutely
12 necessary. So you don't need to add any circuitry,
13 because Hiraishi can stand on its own for teaching
14 the same mechanism.

15 And all I'm saying is that if you don't 2:11:56PM
16 accept that Hiraishi standing on its own teaches
17 this, then you would add Butt. And if Hiraishi
18 doesn't stand on its own, then by that assumption,
19 Hiraishi would not already have that circuitry.

20 As I said, if Hiraishi alone does not 2:12:15PM
21 satisfy it in your mind, in that situation you would
22 need to add the circuitry of Butt in order to be
23 able to provide the mechanism of doing the
24 fine-tuning.

25

1 BY MR. LINDSAY: 2:12:33PM

2 Q. Where in your declaration do you describe 2:12:33PM

3 adding circuitry from Butt into Hiraishi?

4 A. I don't. I'm trying to answer your 2:12:42PM

5 question today. As I said, Hiraishi, standing

6 alone, already does it, so you don't need to add

7 circuitry from Butt. But Butt just makes clear what

8 one of ordinary skill understands is already in

9 Hiraishi.

10 Q. And I understand you're talking about 2:13:04PM

11 adding the functionality of Butt into Hiraishi if

12 one concludes that Hiraishi doesn't already perform

13 that read leveling operation.

14 A. Okay, yes. 2:13:20PM

15 Q. My question, really just yes or no, I 2:13:21PM

16 think we're on the same page, but the answer doesn't

17 really reflect this, you are not now proposing to

18 take circuitry from Butt and add it into Hiraishi,

19 where Hiraishi doesn't already have that circuitry.

20 Is that correct?

21 MR. CHANDLER: Objection, form. 2:13:46PM

22 A. I'm adding the ideas of Butt, which I 2:13:52PM

23 believe are already there.

24 So in order to implement the ideas, to 2:13:59PM

25 implement the invention taught by Butt, if in fact

1 you don't feel as though it already is there, then,
2 of course, you would need to add the circuitry in
3 order to implement the invention of Butt.

4 BY MR. LINDSAY: 2:14:21PM

5 Q. Okay. All right. 2:14:21PM

6 A. I'm sorry. I'm trying to make it clear. 2:14:25PM
7 I don't know how else to say it.

8 Q. So what circuitry -- strike that. 2:14:34PM

9 In a situation where Hiraishi is not 2:14:41PM
10 determined to contain all of the circuitry necessary
11 to perform the read leveling operation that you
12 claim it does, what circuitry from Butt would you
13 specifically add to Hiraishi then?

14 A. Well, this is not in my report, so I would 2:15:04PM
15 have to -- I would be generating new information, I
16 would be generating new opinions. Because like I
17 said, I felt it's already there. But, I mean, you
18 would have to do whatever is necessary in order to
19 implement Butt.

20 And so, again, this is only in the 2:15:22PM
21 assumption that -- only in the assumption that you
22 feel that Hiraishi doesn't already do it. And so
23 you would need a mechanism for -- you would need a
24 mechanism for doing a programmable delay. You would
25 need a mechanism for generating the various offsets.

1 You would need a mechanism for feeding back the
2 value. You would need all the different aspects
3 that cause Butt to operate.

4 But, again, I feel it's already there, so 2:15:59PM
5 you don't need to add it, because Hiraishi -- based
6 on what Hiraishi says and based on one of ordinary
7 skill, all of those mechanisms are necessarily
8 there. I mean it's obvious that they're there.

9 Q. Okay. That's fair enough. 2:16:22PM

10 Is it fair to say that memory modules 2:16:24PM
11 represent a very space-constrained environment?

12 MR. CHANDLER: Objection, form. 2:16:35PM

13 A. Space-constrained environment? I guess I 2:16:37PM
14 don't know what you mean by that.

15 BY MR. LINDSAY: 2:16:42PM

16 Q. Well, when designing a memory module, the 2:16:42PM
17 allocation of area to specific components and
18 circuitry, is that an important design
19 consideration?

20 A. I think it's an important consideration in 2:16:53PM
21 pretty much all electronic design. I'm not sure how
22 it's unique to memory modules. You obviously want
23 to try and design something as small as you can.

24 So I'm not quite seeing how -- if I agree 2:17:12PM
25 to that, I don't see how that answers unique to

1 memory modules. You are always trying to optimize
2 your space.

3 Q. Okay. Well, maybe let's take a look at 2:17:23PM
4 Hiraishi Figure 1 for a moment.

5 A. Okay. 2:17:31PM

6 Q. And then this is labeled 110. What is 2:17:32PM
7 this that we are looking at here labeled 110?

8 A. Okay. Let me get Hiraishi. 2:17:41PM

9 I'm sorry, which figure are you referring 2:17:52PM
10 to?

11 Q. Figure 1. 2:17:55PM

12 A. Figure 1. Okay. 110. 2:17:58PM

13 110 appears to be -- it's a memory module. 2:18:02PM

14 Q. Would it be what might be called a DIMM? 2:18:09PM

15 A. Yes, that's how you would refer to it, a 2:18:12PM
16 DIMM, yes, dual inline memory module.

17 Q. And this memory module, this contains all 2:18:18PM
18 of Hiraishi's data buffers and memory chips mounted
19 onto a substrate; is that right?

20 A. This is a diagram that comes to kind of 2:18:32PM
21 show the overall system at a certain level of
22 detail. I mean, it's got the detail that it's got.
23 It doesn't show everything, but it -- it is trying
24 to show the overall system.

25 Q. Sure. So all I'm saying is that the DIMM 2:18:47PM

1 in Hiraishi includes the data buffers and includes
2 the memory chips.

3 A. Yeah. The memory devices, yes. 2:18:56PM

4 Q. Is it fair to say that space is at a 2:19:02PM
5 premium on a DIMM?

6 MR. CHANDLER: Objection, form. 2:19:08PM

7 A. Well, let's put it this way, the smaller 2:19:09PM
8 you can make it, that means the closer the signals
9 will be, and therefore, the higher speed you can
10 get.

11 So, yeah, I mean, space is at a premium 2:19:17PM
12 only to the extent that you want to try and make it
13 as small as possible to make it go as fast as
14 possible.

15 There is a certain JEDEC specification as 2:19:27PM
16 to what the size of a DIMM must be in order to be
17 able to be compatible and be able to be plugged in.
18 So there's a certain size specification required.
19 And you obviously want to try and pack as much
20 memory as you can onto a DIMM.

21 So, sure, space is at a premium to try and 2:19:46PM
22 get as much functionality and as much storage onto
23 the fixed size that is provided in the JEDEC
24 standard.

25

1	BY MR. LINDSAY:	2:19:59PM
2	Q. Okay. So if you could scroll down to	2:19:59PM
3	maybe Figure 3.	
4	A. Scroll down to Figure 3. Okay.	2:20:05PM
5	Q. Figure 3 of Hiraishi.	2:20:10PM
6	A. Yes.	2:20:11PM
7	Q. Does this show a DIMM 110 mounted, or	2:20:12PM
8	inserted, I should say, into a memory slot?	
9	A. Yes, it does.	2:20:21PM
10	Q. And so memory slot is 22. And this is	2:20:23PM
11	sitting on a motherboard 21; is that right?	
12	A. Yes, that's correct.	2:20:31PM
13	Q. Now, this figure also shows Hiraishi's	2:20:34PM
14	memory controller 12 on that motherboard?	
15	A. Yes, that's correct.	2:20:46PM
16	Q. So the memory controller is on the	2:20:49PM
17	motherboard, not on the DIMM; is that right?	
18	A. That's correct.	2:20:56PM
19	Q. Is there more space on a motherboard for	2:21:03PM
20	Hiraishi's memory controller than you would say is	
21	available on a DIMM?	
22	MR. CHANDLER: Objection, form.	2:21:20PM
23	A. Well, motherboards typically are	2:21:20PM
24	significantly larger than DIMMs. So is there more	
25	space? Yeah. Motherboards are usually, you know,	

1 much larger than the size of a DIMM. So typically
2 that is the case.

3 BY MR. LINDSAY: 2:21:37PM

4 Q. And then if you -- maybe we'll scroll down 2:21:37PM
5 to Figure 5 or a second here.

6 You know what, we actually already 2:21:47PM
7 discussed this earlier. So I can -- I'll skip this
8 line of questions.

9 THE WITNESS: Okay. I wonder, if you want 2:22:04PM
10 to go on something else, we could take a break
11 for five minutes?

12 MR. LINDSAY: Yeah. I was going to 2:22:19PM
13 suggest that.

14 THE WITNESS: 2:27, something like that? 2:22:19PM

15 MR. LINDSAY: Sure. Sounds great. 2:22:22PM

16 (Discussion off the record.) 2:22:25PM

17 THE COURT REPORTER: We're off the record. 2:22:26PM

18 (Recess was held from 2:22 p.m. until 2:28 p.m.) 2:27:30PM

19 THE COURT REPORTER: We're back on the 2:27:30PM
20 record.

21 (Thereupon, marked as Exhibit 8.) 9:18:08AM

22 BY MR. LINDSAY: 2:28:09PM

23 Q. Okay. Dr. Wedig, I'm introducing another 2:28:10PM
24 exhibit. This will be Exhibit 8. It's the Tokuhiko
25 reference.

1	A. Okay. I have it here.	2:28:22PM
2	Q. Tokuhiro is entitled "Delay Time Control	2:28:35PM
3	of Memory Controller." Is that correct?	
4	A. Yes, I see that.	2:28:47PM
5	Q. And do you agree that Tokuhiro disclose a	2:28:48PM
6	fly-by topology?	
7	A. It discloses, yes, a mechanism for	2:28:55PM
8	handling fly-by delays, yeah.	
9	Q. And Tokuhiro is directed to improvements	2:29:04PM
10	in the memory controller, right?	
11	MR. CHANDLER: Objection, form.	2:29:08PM
12	A. It's not limited to the memory controller.	2:29:19PM
13	It's talking about improvements for improving the	
14	problem of fly-by delays from a memory controller as	
15	a possibility, but it's not limited to that.	
16	BY MR. LINDSAY:	2:29:49PM
17	Q. Where else does Tokuhiro disclose	2:29:49PM
18	implementing its invention besides the memory	
19	controller?	
20	A. Well, it discloses it putting it in the	2:29:59PM
21	memory controller, that's correct, but the circuitry	
22	is not limited to being in a memory controller.	
23	There's nothing special about the memory controller	
24	that would require the circuitry only be found	
25	there.	

1 Q. Does Tokuhiro describe implementing his 2:30:19PM
2 invention in any component other than the memory
3 controller?

4 A. The place where Tokuhiro talks about it is 2:30:33PM
5 circuitry that he shows in the memory controller.

6 But as I said, nothing limited to only 2:30:42PM
7 being in the memory controller. So it only shows it
8 in the memory controller, but it's not limited to
9 that.

10 Q. Why do you feel it's not limited to the 2:31:05PM
11 memory controller?

12 A. Well, because there's circuitry here which 2:31:17PM
13 is used for helping to solve fly-by delays. Fly-by
14 delays are problems that occur in many areas. Any
15 time you have very high speed data signals, you're
16 going to have the possibility of fly-by delays.

17 So I think if you are interested in 2:31:35PM
18 seeing -- interested in learning how to try and
19 solve the problem of fly-by delays, you might go to
20 Tokuhiro. Tokuhiro happens to show it in the memory
21 controller, but the teachings for solving the
22 problem could be implemented anywhere.

23 Q. So Tokuhiro discloses write leveling 2:32:05PM
24 procedures, right?

25 A. Write leveling and read leveling, yes. 2:32:12PM

1 Q. And would you agree that Tokuhiro 2:32:15PM
2 discloses write leveling procedures that are
3 consistent with write leveling procedures that are
4 specified in the JEDEC standards?

5 A. It depends on how you use it. It's not 2:32:50PM
6 exactly the same thing, because in Tokuhiro they
7 actually write data. In the JEDEC standard you
8 don't literally write data. So it's not exactly the
9 same thing.

10 Q. Did the DDR standards provide for read 2:34:15PM
11 leveling?

12 MR. CHANDLER: Objection, form. 2:34:21PM

13 A. DDR3 standard, is that what you are 2:34:22PM
14 referring to?

15 BY MR. LINDSAY: 2:34:25PM

16 Q. Yes. 2:34:25PM

17 A. We talked about this earlier. The DDR3 2:34:26PM
18 standard provides for the mechanisms for doing read
19 leveling, but it does not explain the details on how
20 to do it.

21 Q. So the DDR3 standard does provide details 2:34:38PM
22 on how to perform write leveling; is that right?

23 A. Best of my memory, yes, it does. 2:34:45PM

24 Q. Why is it that the DDR standard provides 2:34:49PM
25 details for write leveling but not read leveling?

1 want to dictate what you have to do in order to
2 successfully use the hardware.

3 The hardware that was provided was very 2:36:27PM
4 specific for doing a particular kind of write
5 leveling. So they needed to explain that procedure
6 because -- based on the hardware that was provided.

7 Q. Okay. Let's take a look at -- I'm going 2:36:45PM
8 to say a page number instead of a paragraph
9 number -- Page 216 of your declaration. There's a
10 diagram there.

11 A. Okay. 216. 2:37:03PM

12 Okay. I've got it. 2:37:04PM

13 Q. What is this diagram depicting? 2:37:10PM

14 A. This diagram is depicting Figure 5 from 2:37:15PM
15 Hiraishi and the modification that I would make to
16 this figure in order to incorporate, at least
17 partially, incorporate the teachings of Tokuhiro.

18 Q. Okay. And so the purple signal line from 2:37:39PM
19 selector 332 to DR1 that you've added, is that a
20 read strobe signal?

21 A. That's a DQS read strobe, yes. That's 2:37:56PM
22 what's coming out of 334.

23 I'm sorry. I'm sorry. I'm reading that 2:38:07PM
24 wrong. Thank you.

25 It's what's coming out of selector 332. 2:38:11PM

Page 149

1 Q. So that's a DQS signal that's going into 2:38:15PM
2 the DR1 element that has been added here highlighted
3 in purple?

4 A. That's correct. 2:38:25PM

5 Q. And that delayed element, DR1, from 2:38:28PM
6 Tokuhiko that's been inserted into Hiraishi's
7 Figure 5, that's delaying the DQS signal?

8 A. Right, by a programmable amount, yes. 2:38:45PM

9 Q. And then the delayed DQS signal that's 2:38:51PM
10 coming out of DR1, is that what you are equating
11 with the first delayed read strobe that's recited in
12 the claims of the '506?

13 A. Hang on one second. 2:39:14PM

14 Yes, the first delayed read strobe is the 2:40:00PM
15 output from the programmable DR1.

16 Q. Okay. And then that purple line that's 2:40:11PM
17 coming out of DR1 and is going down to FIFO 302,
18 what is that?

19 A. That is the signal that is the delayed DRQ 2:40:26PM
20 that would pass the -- that would read out the data
21 from the FIFO once the DR -- sorry, once the DQS has
22 been activated, the delayed DQS has been activated.

23 Q. So the purple line that's going down from 2:40:59PM
24 DR1 to FIFO 302, that's clocking out the read data
25 then from 302?

1 A. That's correct. 2:41:10PM

2	Q. Besides the DR1 delay element from	2:41:13PM
---	---------------------------------------	-----------

3 Tokuhiro, does the Hiraishi/Tokuhiro combination
4 require adding, removing, or changing any other
5 circuitry in Hiraishi's data buffer 300?

6 MR. CHANDLER: Objection, form. 2:41:30PM

7 A. Nothing significant. I mean, you need the 2:41:45PM
8 control logic that's taught in Tokuhiro, but you
9 already have -- you already have a section of
10 Figure 5 that has a control circuit.

11 So you would need to make some changes to 2:42:03PM
12 that, and then you would need to be able to provide
13 some feedback to the module controller.

14 But in terms of big blocks, this is the 2:42:15PM
15 only substantive block that would need to change.

16 BY MR. LINDSAY: 2:42:43PM

17 Q. Let me see if I understand that right. 2:42:43PM

18	Besides adding DR1 to Hiraishi's data	2:42:47PM
19	buffer, what else would need to change inside of	
20	Hiraishi's data buffer in order for it to be	
21	operable?	

22 MR. CHANDLER: Objection, form. 2:43:01PM

23 A. Well, you would need to do all the things 2:43:04PM
24 I talked about in my report, none of which requires
25 additional logic blocks. I mean, we can walk

Page 151

1 through the two possible implementations that I was
2 considering, like how to incorporate Tokuhiko to
3 Hiraishi.

4 But just at a very high level, you need to 2:43:28PM
5 be able to have circuitry -- you need to be able to
6 have logic, which is already basically there, a lot
7 of it is already there, but you might need to modify
8 some of it to be able to detect the delay, to be
9 able to measure the delay, and then you need to be
10 able to rewrite the -- you need to be able to write
11 the delay for the read path into DR1.

12 And so the basic control logic is there. 2:44:09PM
13 So you would need to make some changes to that.

14 You would need to be able to do 2:44:16PM
15 calculations on what the read delay would be, and
16 you would need to be able to write the value into
17 the read delay driver.

18 So as I said, the only major block, the 2:44:33PM
19 only thing that is of any real substantive value is
20 you need to add the DR1. Everything else is just
21 some control changes that would just be, you know,
22 modifications of your already-existing data register
23 control circuit.

24 BY MR. LINDSAY: 2:45:10PM

25 Q. Okay. So let's maybe take a look at 2:45:10PM

1 Tokuhiro, maybe Figure 4 is fine -- no, sorry.
2 They're all very similar. Maybe Figure 5.
3 A. Okay. 2:45:59PM
4 Q. So in Figure 5, memory controller 12 is 2:46:05PM
5 connected to CPU 13; is that right?
6 A. Yes, that's correct. 2:46:14PM
7 Q. What is CPU 13? Is that like the main CPU 2:46:17PM
8 of the computer?
9 A. In Tokuhiro, yeah, that's the main central 2:46:21PM
10 processing unit.
11 Q. So it's like a general processor? 2:46:27PM
12 A. A general processor, that's correct. 2:46:30PM
13 Q. Then there's a line labeled "d1" that's 2:46:33PM
14 going from CPU 13 to certain delay elements inside
15 the memory controller.
16 Do you see that? 2:46:43PM
17 A. Yes, that's correct. 2:46:44PM
18 Q. And there is second line labeled "d2" 2:46:45PM
19 that's going from CPU 13 to other delay elements in
20 the memory controller; is that right?
21 A. That's correct. 2:46:53PM
22 Q. Are lines d1 and d2 control signals? 2:46:54PM
23 A. Control signals? I mean very -- at a very 2:47:05PM
24 high level. They're more values. They're values
25 that need to be loaded into these delay elements.

1 So they're control in the sense that they 2:47:19PM
2 control the amount of time of the delay. So, I
3 mean, they hold data. The data that they hold is
4 the amount of delay to be performed. But that data,
5 the purpose of that data is to determine the length
6 of delay of the various delay buffers.

7 Q. All right. Doesn't Tokuhiro refer to them 2:47:51PM
8 as control signals?

9 A. It might. It could well be, because they 2:47:56PM
10 do control. I mean, I would have to go and look in
11 the specification to be sure. I wouldn't be
12 surprised if it did. I'm just trying to help
13 clarify as to what their actual purpose is.

14 Q. Is their purpose to control the variable 2:48:12PM
15 delay elements to apply a specific delay?

16 A. Yeah, that's one way to say it. I mean, I 2:48:22PM
17 was just trying to be more exacting. In order to
18 provide a value -- it's a value of the amount of
19 delay. And so with loading that value, you will, in
20 effect, control the length of the delay.

21 Q. Right. And so each of Tokuhiro's delay 2:48:42PM
22 elements, including the DR1 element, those are
23 variable delay elements?

24 A. Yes, they are. They're programmable delay 2:48:51PM
25 elements.

1 Q. If we disconnected d1 and d2 control 2:48:58PM
2 signal lines, what would those delay elements do?

3 MR. CHANDLER: Objection, form. 2:49:07PM

4 A. I'm sorry, I don't understand that. If 2:49:10PM
5 you disconnected d1 and d2. I don't think I
6 understand your question. Because if you
7 disconnected it, you wouldn't have an operational
8 system. So you need to clarify that question,
9 please.

10 BY MR. LINDSAY: 2:49:24PM

11 Q. Right. I think that -- I mean, you 2:49:24PM
12 answered the question, basically.

13 The delay elements require control signals 2:49:31PM
14 d1 and d2 to be operable, right?

15 A. Well, yeah. You need to load the DW1, the 2:49:42PM
16 actual delay element. DW1 and DW2, they need to be
17 loaded with a particular delay value in order to be
18 able to have a workable system.

19 Q. Now, in Tokuhiro d1 and d2, those are 2:50:06PM
20 dedicated control signal lines coming out of the CPU
21 into the memory controller; is that right?

22 A. That's the way Tokuhiro shows it. That's 2:50:21PM
23 the way he chose to implement it. That's correct.

24 I think one of ordinary skill could do it 2:50:27PM
25 other ways, but okay, that's what he did.

1 (Reporter clarification.) 2:50:27PM

2 A. I'm sorry. I think -- okay. I'm sorry. 2:50:39PM

3 I said, I think one of ordinary skill 2:50:41PM

4 could do it other ways, but that's what he chose to

5 do.

6 BY MR. LINDSAY: 2:50:47PM

7 Q. So let me see if I can ask you a general 2:51:02PM

8 question about circuit design.

9 A. Uh-huh. 2:51:08PM

10 Q. All things being equal, is it preferable 2:51:09PM

11 to use less logic in circuitry to implement a given

12 function?

13 MR. CHANDLER: Objection, form. 2:51:19PM

14 A. I think that all things being equal, given 2:51:23PM

15 that you would have the same functionality, the same

16 speed, the same, you know, fault tolerance, then

17 clearly less is better.

18 But normally that's never the case. 2:51:42PM

19 Normally it's the case that you have to trade off

20 the amount of circuitry for amount of functionality

21 that you get.

22 So your premise is not really a valid 2:51:53PM

23 premise. But, in fact, if it were a valid premise

24 that, all things being equal, yes, of course, less

25 is better.

1 But I -- I have almost never seen that. 2:52:10PM

2 It's almost always the case that you need to add
3 more circuitry to get more functionality to get more
4 reliability to be able to have it operate in a way
5 that you want it to operate.

6 BY MR. LINDSAY: 2:52:26PM

7 Q. So in your declaration I believe you 2:52:26PM
8 provided three reasons to combine Tokuhiko and
9 Hiraishi. It's a lengthy section that starts on
10 Page 195. We can maybe look at the table of
11 contents if that's easier, which it probably is.

12	A. Okay.	2:52:57PM
----	----------	-----------

13 Q. I believe those are on page -- in the 2:52:58PM
14 table of contents, roman numeral 13.

15	A. Okay.	2:53:17PM
----	----------	-----------

16 Q. So the first one you provided is 2:53:18PM
17 calculating read delays based on write delays,
18 right?

19	A. Uh-huh.	2:53:28PM
----	------------	-----------

20 Q. Second one is Tokuhiro provided details of 2:53:29PM
21 how to remove fly-by delays; whereas, Hiraishi
22 doesn't explain how its memory controller handles
23 fly-by delays.

24	A. Uh-huh.	2:53:43PM
----	------------	-----------

25	Q. And then the third is along the lines of	2:53:44PM
----	---	-----------

Page 157

1 Tokuhiko describing how to handle fly-by delays of
2 greater than one clock cycle, which Hiraishi is
3 silent on. Is that fair?

4 A. Yes. That's what it says. 2:53:56PM

5 Q. So if I just summarize that, the reasons 2:53:58PM
6 to modify Hiraishi with Tokuhiko are calculating
7 read delays based on write delays, removing fly-by
8 delays, including fly-by delays greater than one
9 clock cycle?

10 MR. CHANDLER: Objection, form. 2:54:16PM

11 BY MR. LINDSAY: 2:54:17PM

12 Q. Is that accurate? 2:54:17PM

13 MR. CHANDLER: Objection, form. 2:54:19PM

14 A. I think you are leaving out a lot of 2:54:24PM
15 details but, I mean, that's one way to characterize
16 it.

17 I'm sorry. This stupid screen. 2:54:29PM

18 I mean, I'm not going to accept that 2:54:36PM
19 that's the entirety of it, but I think that that is
20 one way to characterize it.

21 BY MR. LINDSAY: 2:54:45PM

22 Q. Well, my question was besides those three 2:54:45PM
23 reasons, do you have any other reasons for modifying
24 Hiraishi with Tokuhiko?

25 A. I gave these reasons, the reasons that I 2:55:00PM

1 have, these are the reasons I came up with. I
2 haven't generated any other reasons beyond this. So
3 these are the reasons that I provided and these are
4 the reasons that I'm willing to stand by.

5 Q. So fair enough. 2:55:19PM

6 So going back, we talked about Tokuhiro 2:55:20PM
7 adjusts for fly-by delays, and it does so using the
8 memory controller. Correct?

9 MR. CHANDLER: Objection, form. 2:55:36PM

10 A. What we said was that Tokuhiro shows it in 2:55:36PM
11 the memory controller, and what I said was that
12 nothing limits you from doing it in the memory
13 controller.

14 BY MR. LINDSAY: 2:55:47PM

15 Q. Right. I understand. 2:55:47PM

16 And so Tokuhiro's disclosed solution for 2:55:49PM
17 handling fly-by delays, including those greater than
18 one cycle, is implemented in the memory controller,
19 right?

20 A. That's the way Tokuhiro shows it in his 2:56:04PM
21 implementation.

22 Q. And then for the feature of using write 2:56:07PM
23 delays to calculate read delays, Tokuhiro also chose
24 to implement that in the memory controller, right?

25 A. Again, that's where he showed the 2:56:19PM

1 implementation in his specification. Nothing stops
2 you from doing it other places.

3 Q. Right. I understand. 2:56:29PM

4 By that same token, would it be possible 2:56:34PM
5 to implement Tokuhiro's memory controller teachings
6 in Hiraishi's memory controller?

7 A. Well, that wouldn't really make sense in 2:57:18PM
8 Hiraishi's system. So that wouldn't accomplish the
9 efficiencies that would be afforded the system, the
10 combined system. So that would not be an obvious
11 thing to do in my book, because it wouldn't give you
12 the efficiencies that I talked about in my
13 motivations to combine. So I wouldn't be motivated
14 to do that.

15 Q. Yeah. That's not the question. 2:57:55PM

16 So the question: Is it going to be 2:57:56PM
17 possible to implement Tokuhiro's memory controller
18 teachings in Hiraishi's memory controller?

19 A. I haven't opined on that. Let me think 2:58:16PM
20 here.

21 I think if you did that, as I said, it 2:58:29PM
22 would not be efficient. It wouldn't satisfy any of
23 the goals of what you want to try and do. So you
24 can do a lot of things that are inefficient, you can
25 do a lot of things that are -- would cause more

1 complication, but there would be no value in it.

2 Q. Well, let me ask you this: Tokuhiro 2:58:53PM
3 achieves efficiencies by using delays for write
4 operations to delay -- to apply the read delays, and
5 it does so in the memory controller, right?

6 A. Correct. Yes, it does. 2:59:12PM

7 Q. If you implemented that feature in 2:59:14PM
8 Hiraishi's memory controller, you would still be
9 able to achieve that same efficiency, right?

10 MR. CHANDLER: Objection, form. 2:59:24PM

11 A. No, you would not. That would not work. 2:59:28PM

12 BY MR. LINDSAY: 2:59:32PM

13 Q. Why not? 2:59:32PM

14 A. Because the whole purpose of Tokuhiro is 2:59:34PM
15 to -- the whole purpose of Tokuhiro is it will solve
16 the problem of fly-by delays, and that is to make it
17 so that the data arrives to the memory controller at
18 the same time.

19 Right now you've got the problem that the 2:59:54PM
20 data does not arrive to the memory controller at the
21 same time because of fly-by delays.

22 If you put all of Tokuhiro's teaching 3:00:02PM
23 inside the memory controller of Hiraishi, then the
24 data would still arrive to the memory controller in
25 a staggered manner. It wouldn't all arrive at the

1 same time. So you wouldn't get any of the benefit
2 of the teaching of Tokuhiro in Hiraishi. So you
3 wouldn't solve any fly-by problem in the data buffer
4 at all.

5 Q. So if you implemented Tokuhiro in 3:00:51PM
6 Hiraishi's memory controller, the memory controller
7 would receive -- would receive data at different
8 times but would correct those before passing it on
9 to the CPU, correct?

10 A. Well, it's a little more complicated. 3:01:26PM

11 Because if you put it in the memory 3:01:30PM
12 controller, then you would not -- you would not --
13 first of all, okay, you have to understand, there's
14 no fly-by delays in the memory controller itself.

15 The memory controller is one big chip 3:01:47PM
16 that, you know, everything is very close. And to
17 get from -- from the time you apply a control signal
18 to one end, it gets to the other side in a very
19 efficient time, no one worries about fly-by delays
20 inside a memory controller.

21 Now, what Tokuhiro is doing is it's 3:02:14PM
22 accounting for the fly-by delays in a system that
23 has fly-by delays. Now, in Tokuhiro, the fly-by
24 delays were out at the DIMMs. Okay? And we were
25 trying to solve that same problem, but we wanted to

1 be able to do it in the data buffer.

2 And so when you do the steps of Tokuhiro, 3:02:42PM
3 the first step you need to do is a write operation
4 and look to see what the fly-by delays are, there
5 would be no fly-by delays in the memory controller.
6 And so you would not have any values -- the values
7 would all be zero delay that you would then load
8 into the read delays. So it just simply wouldn't
9 work.

10 Q. Okay. Let's put aside the first 3:03:15PM
11 motivation for a moment and just focus on fly-by
12 delays.

13 A. Okay. 3:03:23PM

14 Q. We can focus on, I guess, read delays. 3:03:24PM

15 Tokuhiro, if you implemented Tokuhiro's 3:03:35PM
16 solution for removing fly-by delays, including those
17 greater than one clock cycle in Hiraishi's memory
18 controller --

19 A. Okay. 3:03:50PM

20 Q. -- that would remove the fly-by delays 3:03:50PM
21 between Hiraishi's data buffer and the memory
22 controller, right?

23 MR. CHANDLER: Objection, form. 3:03:59PM

24 A. No, because you wouldn't know how much to 3:04:01PM
25 delay the data coming in. The data that's coming in

1 is in a staggered form, into the memory controller,
2 is due to the fly-by delays. You can't correct that
3 unless you know what those fly-by delays are.

4 The only way you know how to do that in 3:04:25PM
5 Tokuhiro, the way Tokuhiro teaches it, is by doing a
6 write operation and measuring the fly-by delay's
7 time difference that occurs. Until you do that
8 write operation, you don't know what the fly-by
9 delay is.

10 So you suggested doing a read and then 3:04:45PM
11 just fixing it in the memory controller. You can't
12 fix it unless you know how much to fix it by. And
13 the only way to find out how much to fix it by is by
14 doing the write operation to see what the fly-by
15 delay is first.

16 BY MR. LINDSAY: 3:05:05PM

17 Q. So in one case Tokuhiro describes using 3:05:09PM
18 the write operation to apply a read delay, but it
19 also describes calculating read delays directly,
20 right?

21 A. Both times it requires doing a write 3:05:32PM
22 operation first. I don't think I've talked anything
23 about calculating read delays without first
24 measuring the fly-by times.

25 So I don't accept your suggestion that 3:05:58PM

Page 164

1 Tokuhiro can just calculate read delays without
2 first measuring what the fly-by delays are.

3 MR. LINDSAY: One second. I've got some 3:06:13PM
4 background noise here.

5 (Discussion off the record.) 3:06:26PM

6 BY MR. LINDSAY: 3:06:26PM

7 Q. Let's come back to this. Let's talk about 3:06:55PM
8 a reference that you discuss in your declaration on
9 page -- or, sorry -- Paragraph 294 of your
10 declaration.

11 A. 294. Okay. 3:07:05PM

12 Which reference are you referring to? 3:07:11PM

13 Q. So it's -- I'll probably butcher 3:07:22PM
14 pronunciation, but it's Giovannini,
15 G-I-O-V-A-N-N-I-N-I.

16 A. Yes, I see that. 3:07:31PM

17 Q. How does the Giovannini reference relate 3:07:34PM
18 to Tokuhiro?

19 A. Well, Giovannini talks about how it's 3:07:54PM
20 possible that the fly-by delays could be so great
21 that they can extend beyond one clock, beyond one
22 clock period.

23 So Giovannini talks about how what could 3:08:08PM
24 happen is that you could have the data be
25 transferred, but that the data that gets sent, part

1 of it could be on one clock, could occur in one
2 clock time, but the remainder of the data might not
3 happen -- may not appear until the next clock cycle.

4 And so, therefore, you've got your data 3:08:37PM
5 one -- what was intended to be a single
6 read operation, actually, the data comes in in two
7 halves or in two parts. The first part of it comes
8 in one clock, the second part comes in via a second
9 clock.

10 Q. So Giovannini has a solution for handling 3:09:05PM
11 those large fly-by delays, right?

12 A. Yes, it does. And I don't know if you 3:09:12PM
13 want to bring it up, if you want to talk about it.

14 Q. Yeah, we can. But we can just look at the 3:09:20PM
15 last sentence of your declaration, Paragraph 294.
16 You mention that Giovannini is a special FIFO-based
17 circuit in the memory controller.

18 A. Yes. That's what Giovannini discloses. 3:09:37PM

19 Q. So is it accurate to say, then, that 3:09:42PM
20 Giovannini and Tokuhiro both rely on memory
21 controller to adjust for large fly-by delays?

22 A. Well, again, I'll say the same thing about 3:09:57PM
23 Giovannini as I said about Tokuhiro, is that that's
24 where they showed implementing circuitry that they
25 disclosed. There's nothing magic about the memory

1 controller that you have to do it there.

2 Q. Okay. 3:10:15PM

3 A. Simply that's where they chose to 3:10:17PM

4 implement it. But in fact, Tokuhiro, for example,
5 you know, it didn't have a data buffer. All it had
6 was the memory controller and the memory module.

7 But there's -- putting a data buffer is not a
8 difficult thing to do and, in fact, it's just
9 supplied buffering.

10 So as I said, I think this is where 3:10:52PM
11 Giovannini and Tokuhiro put it because that's what
12 they had available to them. When I put it in
13 Hiraishi, it makes the most sense, and really only
14 makes the only sense, to put it inside the data
15 buffer.

16 Q. Okay. And then let's talk about Hiraishi 3:11:14PM
17 then as well.

18 A. Okay. 3:11:17PM

19 Q. Hiraishi's S5 leveling, which accounts for 3:11:18PM
20 fly-by delays between the memory controller and the
21 data buffer, that's implemented in the memory
22 controller of Hiraishi, right?

23 MR. CHANDLER: Objection, form. 3:11:31PM

24 A. Again, you know, partially. It requires 3:11:35PM
25 that you get -- you have to get write level, you

Page 167

1 have to get data back from the data buffer.

2 So I think we talked earlier about how 3:11:48PM
3 it's initiated in the memory controller, but it
4 requires interaction between the memory controller
5 and the data buffer.

6 BY MR. LINDSAY: 3:11:57PM

7 Q. And how about -- so for read leveling, S5 3:11:57PM
8 read leveling, it would get data back from the data
9 buffer, right?

10 A. Correct. 3:12:13PM

11 Q. How does Hiraishi implement S5 3:12:14PM
12 write leveling between the memory controller and the
13 data buffer?

14 MR. CHANDLER: I had an objection to form 3:12:24PM
15 to the question before. If you guys could slow
16 down just a little bit, please.

17 THE WITNESS: Okay. I'm sorry. 3:12:33PM

18 A. So the question was how does Hiraishi 3:12:35PM
19 implement S5 read leveling?

20 BY MR. LINDSAY: 3:12:42PM

21 Q. No. I'm sorry. 3:12:42PM

22 So the question is: How does Hiraishi 3:12:44PM
23 implement S5 write leveling?

24 A. Okay. Well, it's discussed in the patent. 3:12:53PM
25 In fact, there's a figure that helps a lot to try

Page 168

1 and show it. I believe it's Figure 16A and 16B in
2 Hiraishi, Page 17. We can walk through that if you
3 would like.

4 Q. Yeah, let's take a look at that. 3:13:33PM

5 A. Okay. Is there a question? 3:13:35PM

6 Q. Yes. So how does Hiraishi perform S5 3:13:42PM
7 write leveling?

8 A. So what it does is to output a -- it 3:13:50PM
9 outputs a DQS signal along with a clock to the data
10 buffer. And what happens is the DQS signal, when
11 it's detected by the data buffer, it samples the
12 value of the clock that also came from the memory
13 controller, went through the module controller, into
14 the data buffer.

15 So it's sampling a value of the clock to 3:14:33PM
16 see whether that clock signal at the time you
17 sampled it is high or low. It then feeds that
18 information back to the memory controller.

19 And if it is -- if that signal is low, it 3:14:51PM
20 know there's misalignment between the DQS signal
21 going out from the memory controller and the clock
22 signal that also went initially from the memory
23 controller through the module controller.

24 So what it does then is it begins to shift 3:15:19PM
25 the DQS signal until it finds that the value that is

1 clocked, or the value that is captured by the DQS
2 signal, which is some value of the clock, the
3 clock -- it captures whether the clock is high or
4 low when the DQS signal transitions.

5 If the clock signal is now high within the 3:15:46PM
6 DQS transition, it means that they are in sync. So
7 at that point, the write leveling is considered
8 completed.

9 Q. So at that point, Hiraishi has removed 3:16:05PM
10 fly-by delays between the memory controller and the
11 data buffer?

12 MR. CHANDLER: Objection, form. 3:16:15PM

13 A. Effectively, yes. 3:16:15PM

14 Oh, sorry. 3:16:17PM

15 MR. CHANDLER: Objection, form. 3:16:19PM

16 A. Right. It's detected those fly-by delays 3:16:22PM
17 and it's accounted for them, yes.

18 So just to be clear, this is what -- this 3:16:27PM
19 is what Hiraishi does. This is not what I'm
20 proposing that you do to combine Tokuhiro when it's
21 controlled by the memory controller.

22 BY MR. LINDSAY: 3:16:58PM

23 Q. Right. I understand. 3:17:04PM

24 A. Okay. 3:17:05PM

25 Q. So we talked about Tokuhiro, Giovannini, 3:17:10PM

1 and now Hiraishi. In each case they have their own
2 way, but in each case they remove fly-by delays that
3 are for signals going to the memory controller using
4 the memory controller; is that right?

5 A. Well, as I said, each of these uses a 3:17:36PM
6 memory controller because other than Hiraishi --
7 Hiraishi is really only trying to time the DQS
8 signal with the clock. That's all it's trying to
9 do.

10 But the other two, they only have a memory 3:17:55PM
11 controller, they don't have a data buffer. So its
12 fly-by delays are the fly-by delays of the
13 individual memory elements.

14 Q. Have you ever -- sorry. 3:18:13PM

15 Have you ever seen a reference that 3:18:15PM
16 doesn't use the memory controller to adjust for
17 fly-by delays that are going to the memory
18 controller?

19 A. I haven't looked for that. I'm not 3:18:37PM
20 familiar with it. I haven't searched. It may be
21 there, I just haven't looked.

22 Q. Well, that's what you've essentially 3:18:49PM
23 created, right, with your combination of Hiraishi
24 and Tokuhiko, you are trying to account for fly-by
25 delays into the memory controller without relying on

1 the memory controller?

2 A. Are you referring to the second 3:19:08PM
3 implementation?

4 Q. Well, I think that it would apply to both 3:19:13PM
5 implementations. Regardless of how you're
6 controlling your delay element, even in the case
7 where you use the memory controller, you still have
8 inserted a delay element that is carrying out part
9 of that fly-by delay adjustment.

10 A. Well, I mean, in the first implementation 3:19:44PM
11 you absolutely need the controller. But I am
12 putting the delay element in the data buffer because
13 that's the most logical place to be able to detect
14 where the delay is. And it's a simple matter of
15 putting it there. It's not a very large circuit to
16 be able to add.

17 Q. But Tokuhiro detects that delay in the 3:20:28PM
18 memory controller. Why isn't that the most logical
19 place to put it?

20 A. Because as I said, in this particular 3:20:35PM
21 system -- see, Tokuhiro did not have a data buffer,
22 so the fly-by delay that it was detecting was out at
23 the memory module.

24 Q. What difference does that make? 3:20:51PM

25 A. The difference is that there is a fly-by 3:20:53PM

Page 172

1 delay in the data buffer. So Hiraishi has a fly-by
2 delay in the data buffer.

3 And I'm trying to solve that problem. I'm 3:21:03PM
4 trying to solve the problem of getting rid of the
5 fly-by delay in the data buffer. So I'm using
6 Tokuhiro's technique, which would apply to any
7 fly-by delay, I'm doing it in a data buffer.

8 Q. Tokuhiro's memory controller, I mean, 3:21:28PM
9 would be agnostic as to whether the data is being
10 received from a data buffer or from a memory device,
11 it's detecting delays and adjusting, right?

12 A. Well, Tokuhiro's memory controller would 3:21:41PM
13 operate much better if it gets its data in a
14 synchronized fashion. Especially as you try to
15 increase speed, any memory controller is going to
16 get significantly more complicated as the delays
17 start to get more than the clock cycle.

18 So this solves that problem without undue 3:22:06PM
19 logic, without a lot of complicated logic. So the
20 most efficient thing to do, as I said in my
21 motivation, is to put it in the data buffer.

22 Q. So how many memory controllers does 3:22:26PM
23 Hiraishi have?

24 MR. CHANDLER: Objection, form. 3:22:33PM

25 A. It has one. 3:22:34PM

Page 173

1 BY MR. LINDSAY: 3:22:34PM

2 Q. And same with Tokuhiro, right? 3:22:34PM

3 MR. CHANDLER: Same objection. 3:22:39PM

4 A. Yes. It only has a memory controller. It 3:22:41PM

5 doesn't have a data buffer.

6 BY MR. LINDSAY: 3:22:46PM

7 Q. How many data buffers does Hiraishi have? 3:22:46PM

8 A. Nine, I think. I don't know if it's eight 3:22:53PM

9 or nine.

10 Q. We can stipulate it's nine. 3:23:04PM

11 A. Okay. I think that's right. 3:23:06PM

12 Q. So if we're modifying Hiraishi's data 3:23:10PM

13 buffers as you proposed, we would need to add nine

14 delay elements, control lines for all that, instead

15 of just implementing all that in one memory module.

16 That's your proposal, right? 3:23:30PM

17 A. Well, first of all, you would not need to 3:23:33PM

18 add any control lines, because they can all be

19 encoded in the lines that already exist. There's

20 nothing that says you have to add more control

21 lines.

22 And the amount of logic I would have that 3:23:46PM

23 would be in the memory controller, would be the same

24 amount of logic as you would have in the memory

25 module. Because you still have to have all the

1 delays. So you are not reducing your amount of
2 hardware at all. It's just a matter of where you
3 put it.

4 As I said, it makes the most sense to put 3:24:10PM
5 it in the place where you want to do the delay,
6 where you are measuring the delay, especially it has
7 to be there because in order to be able to transmit
8 the information both ways, be able to do the read
9 leveling and the write leveling, it all has to be
10 together, and that, as I said, more sufficiently
11 would be in the data buffer.

12 Q. Well, we just talked about Hiraishi. It 3:24:40PM
13 can do write and read leveling using the memory
14 controller for delays between the memory controller
15 and the data buffer. You described in detail how it
16 does that.

17 MR. CHANDLER: Objection, form. 3:24:52PM

18 A. It does the write leveling in order to be 3:24:55PM
19 able to get in sync with the clock. That's its main
20 purpose when doing write leveling. It doesn't do
21 more than that. Its purpose is what it says in
22 Figure 17, in order to line up with the DQS and the
23 clock.

24 BY MR. LINDSAY: 3:25:24PM

25 Q. Isn't that what accounting for fly-by 3:25:28PM

Page 175

1 delays in the combination is doing?

2 MR. CHANDLER: Objection, form. 3:25:32PM

3 A. No, it's doing much more than that. It's 3:25:33PM

4 accounting for the data delay. It's not just

5 aligning up the DQS signals, it's also making sure

6 that the data is lined up.

7 BY MR. LINDSAY: 3:25:49PM

8 Q. Well, you are lining up the DQS signals 3:25:49PM

9 with the data, right?

10 A. In where, which one? 3:25:57PM

11 Q. In Hiraishi's fly-by delay adjustments. 3:25:58PM

12 MR. CHANDLER: Objection, form. 3:26:06PM

13 A. I think that would be necessary, yes. 3:26:10PM

14 BY MR. LINDSAY: 3:26:12PM

15 Q. So a moment ago I asked you if you had 3:26:34PM

16 seen a reference that doesn't use the memory

17 controller to adjust for fly-by delays that are

18 experienced or seen by the memory controller.

19 Do you recall that? 3:26:48PM

20 A. Yes, I do. 3:26:49PM

21 Q. Did you search for such a reference? 3:26:52PM

22 A. No, I did not. 3:26:57PM

23 Q. Wouldn't that reference have been an 3:26:59PM

24 anticipatory reference, in your opinion; it would

25 not require a combination?

1 A. Perhaps. I mean I don't know. It 3:27:10PM
2 depends. In order to anticipate, you have to have
3 all the elements of the claim. So I would have to
4 look at it first to see whether it has all the
5 elements.

6 Q. Wouldn't it make sense to have searched 3:27:22PM
7 for a reference that was much closer than putting
8 two different systems together and then even making
9 some additional changes?

10 A. Obviously, I searched for the best 3:27:38PM
11 references I could. Clearly, an anticipatory
12 reference would only be better. But, you know, I --
13 I'm not aware of one.

14 Q. So is it fair to say you are not aware of 3:27:58PM
15 any reference that adjusts fly-by delays being
16 received by a memory controller that doesn't rely on
17 the memory controller?

18	MR. CHANDLER: Objection, form.	3:28:12PM
----	--------------------------------	-----------

19	A. I have not seen one.	3:28:17PM
----	-------------------------	-----------

20 BY MR. LINDSAY: 3:28:21PM

21 Q. So you propose two ways of controlling 3:28:26PM
22 Tokuhiko's read delay element that's added to
23 Hiraishi, right?

24	A. Right.	3:28:43PM
----	-----------	-----------

25	Q. So in Paragraph 310, you mention a system	3:28:45PM
----	--	-----------

Page 177

1 memory controller. What is that?

2 A. System memory controller is what we've 3:29:07PM
3 been simply calling the memory controller. The main
4 memory controller that talks to the individual
5 memory modules or -- yeah, it's a thing -- it is the
6 block of logic between the CPU and the memory
7 system.

8 Q. So in Hiraishi, would that be memory 3:29:34PM
9 controller 12?

10 A. Let me make sure that's right. 3:29:46PM

11 Yes. That's correct. 3:29:55PM

12 Q. Going down to I think it's Paragraph 313, 3:30:02PM
13 you say the benefit of the first implementation is
14 that data arrives to the memory controller without
15 substantial fly-by delays. So you are simplifying
16 the memory controller's job and circuitry, right?

17 A. Yes, that's correct. 3:30:46PM

18 Q. Is there any other reason why you would 3:30:50PM
19 have done it this way?

20 MR. CHANDLER: Objection, form. 3:30:57PM

21 A. Well, by simplifying its job, it also 3:31:06PM
22 means that, of course, you're reducing the
23 complexity, you are improving the reliability.

24 As I said, it also accounts for -- it 3:31:17PM
25 allows for higher speed in order to be able to

1 account for no -- delays that do not go across the
2 clock cycle. So all the benefits of doing Tokuhiro
3 that we talked about in relation to the motivation.

4 BY MR. LINDSAY: 3:31:46PM

5 Q. So I understand there's a motivation -- 3:31:46PM
6 there are three motivations to combine Tokuhiro and
7 Hiraishi.

8 A. Uh-huh. 3:31:54PM

9 Q. Putting that aside for a second and 3:31:56PM
10 talking about your first implementation, the
11 specific way that you have decided to put these two
12 differences together --

13 A. Uh-huh. 3:32:06PM

14 Q. -- your goal was to simplify the memory 3:32:06PM
15 controller's job and circuitry, right?

16 MR. CHANDLER: Objection, form. 3:32:14PM

17 A. Yeah -- yes, right. With all of the -- 3:32:18PM
18 yes, that's the goal, with all of those
19 ramifications of that simplification, which were
20 discussed in the motivation.

21 BY MR. LINDSAY: 3:32:32PM

22 Q. So then in Paragraph 313, you mention that 3:32:32PM
23 the memory controller will still require retraining
24 to activate the input buffers in time and adjusting
25 the phase of the local clock.

1 Do you see that? 3:32:54PM

2 A. Yes. That's right. 3:32:54PM

3 Q. What are we referring to there? 3:32:57PM

4 A. Well, once you get the data, you've got to 3:33:00PM

5 make sure that you catch it reliably so the -- it's

6 the exact same problem as we had over in the data

7 buffer when we were catching the data from the

8 memory device into the data buffer.

9 Again, for all the reasons that we talked 3:33:28PM

10 about, you have to do the tuning of the DQ-to-DQS

11 signal in capturing the data reliably. You're going

12 to need to do the same thing in the memory

13 controller. You know, you can't ignore that, just

14 like we didn't ignore it with the data buffer.

15 You are still going to need to make sure 3:33:54PM

16 that the data that all comes over now in lock step,

17 or comes over at the same time, you've got to make

18 sure that you capture that data correctly by tuning

19 that delay of the DQS so that it is in the middle of

20 the data window.

21 Q. So the memory controller still has to 3:34:17PM

22 adjust for delays associated with each individual

23 buffer?

24 A. Yeah. I mean, you've got to do that -- 3:34:33PM

25 every time you transfer data -- every time you

1 transfer DQ data with a source-synchronous DQS, you
2 are going to have to make sure that you capture that
3 data in the center of the eye.

4 That is exactly why I said you had to do 3:34:52PM
5 it over in the data buffer and why one of ordinary
6 skill would know that that's required. Well, the
7 same requirement would be necessary in the memory
8 controller.

9 Q. In the combination of Hiraishi and 3:35:09PM
10 Tokuhiko, Hiraishi's memory controller is still
11 adjusting the incoming data so that it is being
12 captured in the valid data eye?

13 A. Yeah, just like it was before. I mean, 3:35:30PM
14 there's no -- you had to do that when you did --
15 before you ever added Tokuhiko.

16 As I said, every time you transfer DQ data 3:35:40PM
17 using DQS as your timing signal, you are going to
18 have to make sure that you catch it optimally. And
19 that happens whether you use Tokuhiko or not.

20 Q. So the combinations -- memory controller 3:36:00PM
21 is still performing what you were calling earlier
22 read leveling steps?

23 MR. CHANDLER: Objection, form. 3:36:13PM

24 A. It's still doing part of the read leveling 3:36:17PM
25 process. We talked about how tuning -- the

1 acceptance of tuning the DQS to sample in the middle
2 of the data eye is part of read leveling. You've
3 still got to do that, because just like you had to
4 do it before, you're always going to do that
5 whenever you transfer DQ and DQS. So you did that
6 before Tokuhiro.

7 When all we had was Hiraishi, when we had 3:36:47PM
8 Hiraishi with Butt, we had to do that in the memory
9 controller. And so that particular step does not
10 change.

11 BY MR. LINDSAY: 3:36:58PM

12 Q. Okay. Now, you also referred to the 3:36:58PM
13 module controller for the second implementation.

14 A. Yes. 3:37:08PM

15 Q. What's the benefit of using the module 3:37:10PM
16 controller?

17 A. Well, it's necessary -- when you have 3:37:14PM
18 Tokuhiro, you go through Tokuhiro in detail, you
19 want to know how big is the skew; you've got to know
20 how far apart is the first data element coming in
21 from the last data element come in.

22 And the way you do that is by feeding that 3:37:40PM
23 information in the module controller. And then the
24 module controller uses that information to send back
25 the delay values.

1 So you need that information across all 3:37:54PM
2 the different data buffers. And the module
3 controller, of course, has the ability to
4 communicate with all the data buffers.

5 MR. CHANDLER: I had an objection to form 3:38:06PM
6 there. So let's, please, try not to talk over
7 each other.

8 THE WITNESS: Okay. 3:38:13PM

9 BY MR. LINDSAY: 3:38:18PM

10 Q. So moving down to Paragraph 316, at the 3:38:18PM
11 very end of that paragraph, you say, "Accordingly, a
12 skilled artisan would have been motivated to use
13 Hiraishi's time-measuring technique in the data
14 buffer."

15 Do you see that? 3:38:38PM

16 A. Not yet, no. 316 on Page 226? 3:38:39PM

17 Q. Yes, it begins on 226, but the part I read 3:38:45PM
18 from is on Page 227.

19 A. Okay. Yes, I see that now, yes. 3:38:50PM

20 Q. What are you referring to there when you 3:39:01PM
21 say "Hiraishi's time-measuring technique"?

22 A. Well, if you remember correctly, Hiraishi 3:39:06PM
23 talks about measuring two different times, he
24 measured the time A and the time B, the time A being
25 the difference in time -- well, actually, time B is

1 actually done in memory controller in Hiraishi.

2 So let's just talk about time A. In time 3:39:24PM

3 A, there is a difference in time between when the
4 read operation occurs and the data is returned from
5 the memory devices. And it says in Hiraishi, and I
6 can go find the wording for it if you would like,
7 that there is -- it measures the time A.

8 So there has to be a measuring mechanism. 3:39:47PM

9 There has to be a measuring mechanism in Hiraishi.
10 So I'm just using that same mechanism in this
11 combination during the write operation in order to
12 set the read delays.

13 Q. Right. So Hiraishi's time-measuring 3:40:12PM
14 technique is for read operations, right?

15 A. It's a measuring circuit. It's a 3:40:20PM
16 measuring circuit. I mean, in Hiraishi it was used
17 during read leveling, but it is a measuring circuit.

18 And so it seems to me that it's a trivial 3:40:33PM
19 circuit modification to add write information into
20 the measuring circuit versus read information. It's
21 just a matter of adding one multiplex.

22 Q. So Hiraishi doesn't expressly disclose a 3:40:51PM
23 time-measuring technique for write operations,
24 right?

25 A. It discloses a time-measuring mechanism, 3:40:59PM

Page 184

1 and yes, he discloses it using it for
2 read operations. But upon reading it, one of
3 ordinary skill would recognize that there is
4 time-measuring operation. He happened to use it for
5 reading, that is correct.

6 Q. Okay. So I'm just making a point. You 3:41:14PM
7 are making a change from what Hiraishi expressly
8 discloses, an obvious change, but a change
9 nonetheless?

10 A. I'm utilizing a mechanism that's already 3:41:24PM
11 in Hiraishi and I'm repurposing it for something
12 else. But yes, it's a change, but it's an obvious
13 change.

14 Q. Okay. And then that result of the 3:41:37PM
15 time-measuring technique, that's sent back through
16 the DRF channel to the module controller, if I have
17 that right.

18 A. That's correct. 3:41:48PM

19 Q. Does Hiraishi send the result of his 3:41:51PM
20 time-measuring technique back through the DRF
21 channel expressly?

22 A. I'm sorry, I didn't catch that question. 3:42:03PM
23 One more time, please.

24 Q. Does Hiraishi expressly disclose sending 3:42:06PM
25 the result of his time-measuring technique back

1 through the DRF channel?

2 A. The reason I'm confused is because you are 3:42:16PM
3 combining two different things.

4 Oh, no. Okay. Sorry. I'm getting tired 3:42:21PM
5 here.

6 Does it disclose -- Hiraishi talks about a 3:42:27PM
7 DRF channel, and it says it's used for sending back
8 status. Right?

9 So you can send anything -- as I said, 3:42:39PM
10 status is any type of information. So Hiraishi does
11 talk about sending information from the data buffer
12 to the module controller. So I'm utilizing the
13 mechanism that's been provided by Hiraishi for
14 sending back the timing information, which is a type
15 of status.

16 Q. Doesn't Hiraishi store the 3:43:10PM
17 timing-measuring information in the read leveling
18 circuit?

19 A. It's returned back -- 3:43:15PM

20 MR. CHANDLER: Objection, form. 3:43:18PM

21 A. Sorry. Got to slow down. 3:43:22PM

22 After it gets computed in the module 3:43:27PM
23 controller, it gets sent back to the data buffer.
24 That's now via the DRC.

25

1	BY MR. LINDSAY:	3:43:41PM
2	Q. I'm sorry, I'm confused.	3:43:44PM
3	A. Okay.	3:43:45PM
4	Q. The time measuring that is disclosed in	3:43:47PM
5	Hiraishi is performed by the leveling circuit in the	
6	data buffer; is that correct?	
7	MR. CHANDLER: Objection, form.	3:44:00PM
8	A. If we're talking about -- we're talking	3:44:00PM
9	about Hiraishi before you add Tokuhiko?	
10	BY MR. LINDSAY:	3:44:08PM
11	Q. Yes, let's start there.	3:44:08PM
12	A. Okay. The time-measuring mechanism is	3:44:12PM
13	done by Hiraishi during read leveling. Okay. Yes.	
14	Q. And the result of that is stored in the	3:44:26PM
15	read leveling circuit?	
16	MR. CHANDLER: Objection, form.	3:44:31PM
17	A. The result of that is -- yes. It says	3:44:34PM
18	it's used in order enable the INB buffer and the	
19	like. So, yeah, that is stored in the control	
20	circuit of the data buffer.	
21	BY MR. LINDSAY:	3:44:50PM
22	Q. And I'll just read from Paragraph 151 so	3:44:50PM
23	we're on the same page.	
24	A. 151, I'm sorry, of Hiraishi?	3:45:00PM
25	Q. Of Hiraishi, yeah.	3:45:03PM

1 A. Okay. Let me get to it, please. 3:45:04PM

2 Q. I was just going to really confirm what 3:45:21PM

3 you just said.

4 It says, "The time is measured for each of 3:45:25PM

5 the memory chips 200 stored in the data register

6 control circuit 320 in data register buffer 300."

7 I just want to confirm that Hiraishi 3:45:40PM

8 stores the result of his read leveling -- I'm sorry.

9 Strike that.

10 Hiraishi stores the result of his 3:45:46PM

11 time-measuring technique in the -- I guess it's the

12 register control circuit 320, which includes the

13 read leveling circuit, right?

14 MR. CHANDLER: Objection, form. 3:46:00PM

15 A. Yeah. I mean it includes the read 3:46:00PM

16 leveling control circuit, yes, it does.

17 BY MR. LINDSAY: 3:46:06PM

18 Q. Okay. 3:46:06PM

19 A. I mean, it just says it stores it in 320, 3:46:07PM

20 so somewhere in there.

21 Q. Sure. So now, in the combination, we are 3:46:13PM

22 modifying Hiraishi so that instead of storing the

23 time-measuring results in the control circuit 320,

24 it is sending that information back through the DRF

25 channel to the module controller.

1 Do I have that right? 3:46:36PM

2 MR. CHANDLER: Objection, form. 3:46:39PM

3 A. Yes, that's part of what it needs to do, 3:46:42PM

4 yeah. It's going to be used in order to compute the

5 read delay, yeah.

6 So you are correct, it is taking that 3:46:49PM

7 information and then sending it on -- sending it

8 back via the DRF to the module controller.

9 BY MR. LINDSAY: 3:46:58PM

10 Q. Okay. So that's another change from 3:46:58PM

11 Hiraishi's expressed original disclosure, right?

12 MR. CHANDLER: Objection, form. 3:47:05PM

13 A. I mentioned that earlier. I said that 3:47:07PM

14 there would be some modifications in the control

15 circuitry, but it's not a substantial change. It's

16 not an additional module, it's just a little

17 reprogramming in the data register control circuit.

18 BY MR. LINDSAY: 3:47:30PM

19 Q. Okay. Fair enough. 3:47:30PM

20 And then on the module controller, that's 3:47:31PM

21 used to program the read delay element that is now

22 added to Hiraishi's buffer, right?

23 A. That's correct. 3:47:45PM

24 Q. And the module controller, does 3:47:46PM

25 Hiraishi -- well, strike that.

1 When you refer to the module controller, 3:47:54PM
2 you are referring Hiraishi's command address control
3 register buffer 400, correct?

4 A. Yes, of course. I mean, that's what we've 3:48:05PM
5 been talking about. That's the words I have been
6 using, that's what I've heard you use. I think
7 that's been clear all along, hasn't it?

8 Q. So my question is: Does Hiraishi's 3:48:17PM
9 register control buffer 400 program any of the delay
10 elements that are in the data buffer 300?

11 MR. CHANDLER: Objection, form. 3:48:33PM

12 A. Yes, it does in -- with the Tokuhiro 3:48:38PM
13 combination.

14 BY MR. LINDSAY: 3:48:41PM

15 Q. I understand that. I'm sorry. 3:48:43PM

16 So in an unmodified Hiraishi, does the 3:48:45PM
17 register buffer 400 program any delay element in the
18 register buffer 300?

19 MR. CHANDLER: Objection, form. 3:48:56PM

20 A. You have a little flaw in your question 3:48:59PM
21 there which you might want to correct.

22 You said "register buffer 400." I think 3:49:03PM
23 you meant module control 400. Do you want to look
24 at your question and state that again?

25

1 BY MR. LINDSAY: 3:49:12PM

2 Q. Okay. So it's not really an error. 3:49:12PM

3 That's what Hiraishi calls it. He calls it a

4 register buffer 400. Command address control

5 register buffer 400, right?

6 A. Okay. We've been calling that the module 3:49:25PM

7 controller. But okay.

8 Q. Well, the reason I'm bringing this up now 3:49:30PM

9 is only because if we want to look at Tokuhiro --

10 I'm sorry. If we want to look at Hiraishi's

11 specification, we're not going to see "module

12 controller" anywhere.

13 So I just want to be clear about what 3:49:45PM

14 Hiraishi expressly discloses, unmodified, about its

15 command address control register buffer 400, which I

16 understand is what you were referring to as a module

17 controller.

18 MR. CHANDLER: Objection, form. 3:50:01PM

19 BY MR. LINDSAY: 3:50:02PM

20 Q. With that out of the way -- 3:50:02PM

21 A. Okay. 3:50:06PM

22 Q. -- the question is: Does Hiraishi, in its 3:50:06PM

23 unmodified form, use the command address control

24 register buffer 400, which we've been referring to

25 as a module controller, to program any delay element

1 in the register buffer 300?

2 MR. CHANDLER: Objection, form. 3:50:26PM

3 A. Unmodified? No, it does not. This is 3:50:32PM

4 part of what I talked about as what is necessary in

5 order to add Tokuhiro. This is part of the --

6 BY MR. LINDSAY: 3:50:48PM

7 Q. Part of the change -- 3:50:48PM

8 A. Part of the teaching that you would need 3:50:49PM

9 in order to implement Hiraishi in light of Tokuhiro.

10 Q. So it's another change to Hiraishi, right? 3:50:57PM

11 MR. CHANDLER: Objection, form. 3:50:59PM

12 A. There's no additional circuitry needed, 3:51:01PM

13 other than programming. There's already control

14 circuitry in module controller 400. It's just a

15 matter of some programming.

16 BY MR. LINDSAY: 3:51:19PM

17 Q. Tokuhiro doesn't have a module controller; 3:51:19PM

18 does it?

19 A. No, Tokuhiro does not. 3:51:30PM

20 Q. So what support did you identify in 3:51:34PM

21 Hiraishi that the command address control register

22 buffer 400 would be capable of programming read

23 delay elements?

24 A. Well, I mean, the module controller is a 3:51:51PM

25 circuit which accepts the DRF signal, DRF signal or

1 signals, which receive status. It generates DRC.

2 And so it has the communication paths for accepting
3 the delay elements and for sending back the delay
4 elements.

5 All we're doing is adding the programming 3:52:23PM
6 for taking the input, doing the computation, and
7 producing the output. That's fundamental logic,
8 fairly basic logic that would be in the module
9 controller. I'm not making any great leap in order
10 to be able to provide that functionality.

11 Q. Did you identify any support in your 3:52:55PM
12 declaration for how a module controller can be used
13 to program a variable delay element?

14 A. Well, yeah. I mean Tokuhiro explains that 3:53:10PM
15 in detail.

16 Q. You just said that Tokuhiro doesn't have a 3:53:17PM
17 module controller, so how could it explain that in
18 detail?

19 A. Because it gives the exact equations, it 3:53:23PM
20 gives the exact algorithm for doing the computation.
21 So it doesn't have a module controller, but it has
22 the logic for doing it. And I put that logic in the
23 most logical place, which is the place where all of
24 the data buffers communicate.

25 So Tokuhiro explains exactly how to 3:53:45PM

1 perform that computation. So I would just take that
2 teaching and I would implement it in the module
3 controller. Because that is the -- it's really the
4 only place you would put it.

5 Q. You could put it in the memory controller. 3:54:13PM
6 That's where Tokuhiro puts it.

7 A. I don't think that would change anything. 3:54:30PM
8 Yeah. I think it would be a lot less efficient
9 because you've already got these immediate
10 communications.

11 I hadn't really thought about it doing 3:54:40PM
12 there, but even if you did it there, it wouldn't
13 change the fact that that combination would still
14 read on the claim.

15 Like I said, I haven't analyzed that 3:54:52PM
16 because that was not the most efficient way to do it
17 in my mind.

18 Q. Have you seen a reference that describes a 3:55:14PM
19 module controller programming a delay element for
20 read leveling?

21 A. No, not a single reference. 3:55:28PM

22 This combination is obvious in my mind, 3:55:32PM
23 but I've not seen a single reference that provides
24 all the necessary elements in the element
25 computation.

1 Q. So to summarize what we've been talking, 3:55:45PM
2 about if I could, and I'll ask questions, so none of
3 the references expressly disclose a time-measuring
4 technique for write operations, right?

5 A. Well, I'm sorry, Tokuhiro does. I mean if 3:56:08PM
6 I understood your question correctly.

7 Q. Well, a moment ago we were talking about, 3:56:15PM
8 as you said in your declaration, using Hiraishi's
9 time-measuring technique for the write operation,
10 and we talked about the fact that it only discloses
11 expressly using it for read operations, right?

12 A. That's correct. I mean the -- Hiraishi 3:56:38PM
13 uses it for read operations. As I said, it's a
14 trivial matter to use the same mechanism for write
15 operations. It's just redirecting the input.

16 Q. So I just want to focus on what's 3:56:53PM
17 expressly disclosed in the references. I understand
18 that there are a lot of things that would have been
19 obvious. I want to find what, you know, what are
20 the points of deviation. Right?

21 A. Sure. Okay. 3:57:04PM

22 Q. So none of the references disclose a 3:57:06PM
23 time-measuring technique in the data buffer for
24 write operations?

25 A. Not that particular narrow -- 3:57:26PM

1 MR. CHANDLER: Objection, form. 3:57:35PM

2 A. Not that very specific teaching. All the 3:57:36PM

3 pieces are there, put together obvious -- it would

4 be obvious, but not exactly as you put it. All of

5 those pieces are not all in one place in one

6 document.

7 BY MR. LINDSAY: 3:57:51PM

8 Q. Also, none of the references disclose 3:57:51PM

9 using a DRF channel to transmit time-measuring read

10 delays?

11 A. Not the DRF channel. I mean Tokuhiko has 3:58:08PM

12 to communicate that information among itself in

13 order to be able to calculate it.

14 But the DRF channel in Hiraishi, by 3:58:16PM

15 itself, does not talk about transmitting the time

16 delays. It's status information, and so it's not

17 really not difficult to do. It would have been

18 obvious. But Hiraishi itself does not teach it.

19 You need to add Tokuhiko.

20 Q. Okay. And, again, I'm just trying to 3:58:45PM

21 identify specific points of obviousness versus

22 express disclosure.

23 A. Okay. 3:58:55PM

24 Q. And then the final one I think we talked 3:58:56PM

25 about was references not expressly using a module

1 controller to program read delay elements.

2 That's also the case, right? 3:59:04PM

3 MR. CHANDLER: Objection, form. 3:59:06PM

4 A. Hiraishi by itself does not teach that. 3:59:22PM

5 It requires combination with Tokuhiro.

6 BY MR. LINDSAY: 3:59:25PM

7 Q. But Tokuhiro doesn't disclose that either. 3:59:26PM

8 Again, I'm talking about using -- the question is

9 using a module controller to program read delay

10 elements.

11 A. Yeah, Tokuhiro, as we said, doesn't have a 3:59:38PM

12 module controller, so of course it doesn't teach it

13 there. But it teaches that it needs to combine all

14 that information together, and the module controller

15 is the one place where all the information is

16 brought together. So that's why I said it was

17 obvious.

18 But to answer your question as directly as 3:59:59PM

19 I can, Tokuhiro doesn't teach it because it doesn't

20 have a module controller. If it did, clearly, that

21 would be the place to do it.

22 Q. So those three modifications, I understand 4:00:15PM

23 your opinion would be obvious, right?

24 A. Correct. 4:00:22PM

25 Q. And those three additional modifications, 4:00:23PM

Page 197

1 at least those three, are required for your second
2 implementation to be operable, right?

3 MR. CHANDLER: Objection, form. 4:00:33PM

4 A. Yes. 4:00:36PM

5 BY MR. LINDSAY: 4:00:36PM

6 Q. Have you, in your declaration, identified 4:00:36PM
7 any support for why any of those three modifications
8 would have been obvious?

9 A. Let me check. 4:01:07PM

10 Well, I think -- I'm sorry. I don't know 4:01:49PM
11 why this keeps doing that. Hang on.

12 It's only what I've already said, that 4:02:01PM
13 when you combine Tokuhiko, it needs to be done. And
14 so I know the functionality is required by Tokuhiko.
15 So I put it in the place that -- I put each of
16 those -- that functionality in Hiraishi in a place
17 that made the most sense.

18 So it's knowledge of one of ordinary 4:02:25PM
19 skill, I think if you give anyone of ordinary skill
20 the two references and you said, you know, I need --
21 Tokuhiko provides this improvement; how can we
22 incorporate it, one of ordinary skill I think would
23 come up with what I did.

24 But the wording is not -- explicitly 4:02:47PM
25 there's no wording in Tokuhiko that says put this

Page 198

into Hiraishi this way, but it seems to me it's obvious, given the thing they're trying to perform, which is to make an improvement on Hiraishi by incorporating the capabilities of Tokuhiko, given the motivations that I stated.

Q. So I think I got that.

4:03:23PM

So just to summarize, your opinion that these three modifications that don't appear in any of the references are obvious is based on just your opinion, you have nothing to point to outside of your opinion in support of that; is that accurate?

MR. CHANDLER: Objection, form.

4:03:47PM

A. It's my opinion based on the improvement I want to make and the mechanisms that are available in Hiraishi.

So, yes, it's my opinion, but not just wildly picking, not just randomly deciding, it's all based on the study of what functionality we want to try and improve in Hiraishi and how one of ordinary skill would do it.

BY MR. LINDSAY:

4:04:29PM

Q. Did you start with the claims and figure out how the two references could be combined to read on the claims?

A. No, I did not. Hiraishi had, as I talked

4:04:38PM

Page 199

1 about in my motivations combined, Hiraishi had
2 certain ways that it could be improved, or it had
3 deficiencies such as the not, you know, not clear
4 they could operate in a higher speed, whereby the
5 fly-by delays might take more than a clock.

6 So I used those deficiencies in Hiraishi 4:05:04PM
7 and I looked out into the art to see what else would
8 help to satisfy those deficiencies, and that's where
9 Tokuhiro came in. The claims had nothing to do with
10 it.

11 Q. Okay. But neither your first 4:05:25PM
12 implementation nor your second implementation
13 implements Tokuhiro's leveling the way Tokuhiro
14 implements it, right? You needed more changes?

15 MR. CHANDLER: Objection, form. 4:05:41PM

16 A. That's -- I don't think that's correct. 4:05:44PM

17 BY MR. LINDSAY: 4:05:48PM

18 Q. We just talked about three additional 4:05:48PM
19 changes that were found in neither reference that
20 you said would have been obvious, but nonetheless,
21 they're changes.

22 A. We just talked about changes to Hiraishi. 4:05:58PM
23 They are taking circuitry or algorithms or
24 discussions in Tokuhiro and they are putting them
25 into Hiraishi. All of which is -- it's all taught

1 in Tokuhiro.

2 So I'm not changing anything from 4:06:18PM
3 Tokuhiro. I'm just taking its teaching and I'm
4 putting it in the places that make sense in
5 Hiraishi.

6 Q. Well, Tokuhiro uses a memory controller to 4:06:32PM
7 carry out its leveling operations in the memory
8 controller, right?

9 A. Exactly. 4:06:40PM

10 Q. That's what Tokuhiro teaches. That's not 4:06:41PM
11 what happens in the combination, correct?

12 A. I'm going to wait and see if Ted is going 4:06:49PM
13 to object to that.

14 MR. CHANDLER: Thank you for waiting. I 4:06:54PM
15 don't have an objection. I understand his
16 question.

17 A. Okay. And I said from the very beginning 4:06:59PM
18 that Tokuhiro only has a memory controller, it
19 doesn't have a data buffer.

20 I think -- well, I can't read Tokuhiro's 4:07:12PM
21 mind. But given the combination, it makes all the
22 more sense to put the capability of Tokuhiro into
23 the data buffer, given that fact.

24 So as I said from the beginning, 4:07:34PM
25 Tokuhiro -- the circuitry in Tokuhiro that's in the

Page 201

1 memory controller could be found anywhere, it just
2 so happens to be in the memory controller. It would
3 work equally well somewhere else, for example, a
4 data buffer.

5 BY MR. LINDSAY: 4:08:00PM

6 Q. So there's no reference you came across, 4:08:00PM
7 like Tokuhiro, that had a data buffer; is that
8 right?

9 A. There was no -- it's correct that I did 4:08:14PM
10 not find a patent that taught the same teachings as
11 Tokuhiro with a data buffer. That's correct.

12 Q. Now, in Tokuhiro, he discloses programming 4:08:26PM
13 the memory controller using the CPU, right?

14 A. That sounds vaguely familiar. If we're 4:08:40PM
15 going to get into more detail, I might want to check
16 that. But I'm not going to disagree with that yet.

17 Q. Well, I don't know that we need to get 4:08:49PM
18 into too much detail, but if you want to look at
19 figures, Figure 5.

20 A. Figure 5 of Tokuhiro? 4:08:58PM

21 Q. Of Tokuhiro. 4:08:59PM

22 A. Okay. Hang on. 4:09:02PM

23 Yeah, I see Figure 5. 4:09:15PM

24 THE COURT REPORTER: Counsel, when you get 4:09:16PM
25 to a good spot, I need a comfort break.

Page 202

1 (Discussion off the record.) 4:09:17PM

2 MR. LINDSAY: Okay. You know, let's go 4:09:19PM

3 ahead and take a break now, because I think I

4 probably only have a bit more after this and

5 then I'll be done. So this might be our last

6 break at least for cross.

7 MR. CHANDLER: How long? Five minutes, 4:09:41PM

8 ten minutes?

9 THE COURT REPORTER: We're off the record. 4:09:49PM

10 (Recess was held from 4:09 p.m. until 4:14 p.m.) 4:09:50PM

11 THE COURT REPORTER: We're back on the 4:14:47PM

12 record.

13 BY MR. LINDSAY: 4:14:51PM

14 Q. Okay, Dr. Wedig, we were just talking 4:14:51PM

15 about Tokuhiro, and I was asking if it was your

16 understanding that he programs a memory controller

17 using the CPU?

18 A. Correct. Yes, you asked that question. 4:15:11PM

19 I'm sorry. Go ahead. 4:15:12PM

20 Q. And I can direct your attention -- there's 4:15:18PM

21 Figure 5, there's number of places -- Figure 5 shows

22 CPU having first delay time control unit 23 --

23 A. Yes. 4:15:37PM

24 Q. -- and second delay time control unit 24. 4:15:37PM

25 Do you see that? 4:15:41PM

1 write leveling of S5. And then, as I say in here,
2 memory controller then programs the read delays in
3 the data buffer based on the write delays.

4 So now that's the memory controller doing 4:18:07PM
5 that, you know, but the memory controller is
6 connected to the CPU.

7 And so I don't quite see the point. I 4:18:21PM
8 don't see the issue. Because memory controller is
9 not going to do anything without at least being
10 initiated by the CPU, right?

11 I mean the CPU is going to at least -- the 4:18:38PM
12 memory controller, like everything, doesn't operate
13 on its own. So it's going to be -- the data
14 buffers -- I'm sorry.

15 The memory controller is going to program 4:18:50PM
16 those read delays in the data buffers, but it would
17 have to at least, you know, get the instruction from
18 the CPU to go and do that.

19 Q. So in Tokuhiro we can take a look at a few 4:19:07PM
20 different places. Column 12.

21 A. Okay. 4:19:17PM

22 Q. Line, I guess, 42. 4:19:21PM

23 A. Column 12, line 42. Okay. 4:19:28PM

24 Q. It says, "The delay time control unit 22 4:19:33PM
25 outputs a control signal for setting the respective

Page 205

1 delay times in the delay circuit DW and the second
2 delay circuit DR." Right?

3 A. Right. I see that. 4:19:48PM

4 Q. And the delay time control unit 22 is in 4:19:53PM
5 the CPU, right?

6 A. Yeah. It's shown in Figure 4. Yes, it's 4:20:10PM
7 shown in the CPU.

8 Q. And not to bounce around too much, but I 4:20:18PM
9 just noticed on the same column, line 34, it says,
10 "The CPU 13 executes various kinds of numerical
11 calculations, information processing, equipment
12 control, et cetera, in the information processing
13 apparatus 10, and it functions as the delay time
14 control unit 22 in this embodiment." Right?

15 A. Yes, I see that. 4:20:47PM

16 Q. So the CPU is programming the delay 4:20:49PM
17 elements in the memory controller in Tokuhiro; is
18 that fair?

19 A. That's what -- yeah, that's what Tokuhiro 4:21:02PM
20 is teaching explicitly, yes.

21 Q. And I'm just asking, in your combination, 4:21:10PM
22 you don't rely on Hiraishi's CPU to program the
23 delay elements. That's carried out by either the
24 memory controller in the first embodiment or the
25 module controller in the second embodiment. Or

1 implementation, I should say. Is that right?

2 MR. CHANDLER: Objection, form. 4:21:35PM

3 A. Yeah, that's explicitly where I say, 4:22:07PM
4 however, knowing that, of course, the memory
5 controller is not going to do anything without
6 getting its direction from the CPU, right? As I
7 said, it's not going to just independently act on
8 its own, it's going to get direction from the CPU to
9 say go and do this.

10 That's the way everything works in a 4:22:29PM
11 computer system. It's all ultimately directed to
12 perform an operation by the CPU.

13 BY MR. LINDSAY: 4:22:41PM

14 Q. But the generation of the control signal 4:22:41PM
15 that programs the read delay in your two
16 implementations does not come from the CPU, right?

17 A. That's not to suggest a combination that 4:22:57PM
18 I'm talking about.

19 Q. And why did you not suggest carrying it 4:23:09PM
20 out as Tokuhiro does, using the CPU to program the
21 delay elements?

22 A. I don't think it matters. I mean, it's 4:23:22PM
23 not relevant. It could have been done by the CPU
24 because, you know -- in fact, as I said, it would
25 have at least been initiated by the CPU, and I think

1 that's an option.

2 Again, I don't think that changes my 4:23:39PM
3 analysis at all, if in fact it were done by the CPU.

4 But no, you are right, I didn't say that, 4:23:51PM
5 but again, I don't believe there's any relevance in
6 terms of, you know, it would work either way. And I
7 don't see how it changes my analysis at all.

8 Q. So is it the case that if you tried to 4:24:10PM
9 implement Tokuhiko's leveling operations in
10 Hiraishi, as Tokuhiko teaches, it wouldn't work?

11 MR. CHANDLER: Objection, form. 4:24:34PM

12 A. I don't see why it wouldn't work. I don't 4:24:38PM
13 agree with that. I believe it would work.

14 BY MR. LINDSAY: 4:24:44PM

15 Q. So you could have implemented Tokuhiko's 4:24:44PM
16 leveling teachings in Hiraishi's memory controller
17 just the way Tokuhiko teaches?

18 MR. CHANDLER: Objection, form. 4:25:04PM

19 A. You can do it the way that I suggested it 4:25:04PM
20 be combined, with all the explanation that I have.

21 So, I mean, I still stand by my 4:25:13PM
22 combination. Are you suggesting that my combination
23 be changed in some way? I stand by the combination
24 that I have. I believe that it will work.

25

1 BY MR. LINDSAY: 4:25:30PM

2 Q. I understand that. I'm not at this point 4:25:30PM

3 questioning whether your combinations would work.

4 I'm asking whether it would have also worked to

5 implement Tokuhiro's teachings in Hiraishi the way

6 Tokuhiro teaches?

7 MR. CHANDLER: Objection, form. 4:25:49PM

8 A. I believe we actually walked through this 4:25:50PM

9 already, and I said that if you put all of Tokuhiro

10 in the memory controller, all of the delay lines,

11 all of the programming, you know, into the memory

12 controller, in a Hiraishi system it will not work.

13 That's where our whole discussion earlier, 4:26:17PM

14 we talked about how it would not calculate the

15 fly-by delays of the data buffer -- I mean, unless

16 your question is different, I think we already had

17 this discussion.

18 BY MR. LINDSAY: 4:26:35PM

19 Q. Right. No, that was the question. 4:26:35PM

20 And so to get the combination to work, you 4:26:38PM

21 needed further modifications, a set of further

22 modifications based on what, in your opinion, would

23 have been obvious to do, right?

24 A. The modification that I talked about was 4:26:50PM

25 exactly what I did in my report, and it's the

1 addition of one delay element in Hiraishi. And then
2 we also talked about the -- you need some
3 programming, as I discussed, in the -- let me see.
4 I want to get the name correct here -- in the data
5 register control circuit, you would need some
6 programming there in order to be able to communicate
7 the delay information over to the module controller,
8 and then you would need computation ability in the
9 module controller in order to calculate the delay
10 and send it back to the data buffer.

11 We talked about all that, and I said that 4:27:44PM
12 all would be obvious, given the teachings of
13 Tokuhiro and given the particular hardware
14 configuration of Hiraishi with data buffers.

15 Q. Let's turn to Page 195 in your 4:28:21PM
16 declaration.

17 A. Okay. Paragraph or Page 195? 4:28:26PM

18 Q. So Page 195. I guess it's Paragraph 279. 4:28:36PM

19 A. Okay. One moment, please. 4:28:41PM

20 Okay. 4:28:51PM

21 Q. So in this section you provide -- and this 4:28:52PM
22 is the same section we were, I think, talking about
23 earlier -- you provide motivations to combine
24 Tokuhiro and Hiraishi, right?

25 A. Yes. 4:29:04PM

Page 210

1 Q. Have you also provided reasons why persons 4:29:04PM
2 skilled in the art would have been motivated to
3 further modify the Hiraishi/Butt combination with
4 Tokuhiro?

5 A. In a sense, yes, because I said, and I can 4:29:30PM
6 find it here, I said that this modification of
7 Tokuhiro would be in addition to the fine-tuning
8 that would need to be done when you first sample the
9 data into the data buffer, which essentially is
10 Butt. Did you want me to find that?

11 Q. Sure. If you have it handy. 4:30:11PM

12 A. Let's see if I can do a search on it here. 4:30:18PM

13 Okay. Found it. Page 216. 4:31:55PM

14 If you look on the first sentence of 4:32:09PM
15 Paragraph 304, it says, "In this exemplary
16 implementation, Tokuhiro's read delay circuit (DR-1,
17 purple) is added to Hiraishi's data buffer to remove
18 the large fly-by delays, while the existing delay
19 circuit 372 continues to make fine timing
20 adjustments to the phase of the incoming strobe DQS
21 as before to properly latch the incoming data DQ."

22 Do you see that? That is a reference 4:32:53PM
23 directly to the adjustments we were referring to
24 earlier that, as I said, I believe is obvious in
25 Hiraishi alone, but is amplified or reinforced with

Page 211

1 Butt.

2 Q. Aren't you just saying there that 4:33:11PM
3 Hiraishi's existing delay circuit 372, not a
4 modified delayed circuit, existing delay circuit 372
5 continues to make the fine timing adjustments. Your
6 position is Hiraishi alone discloses that, right?

7 A. No. No. The wording says, "The existing 4:33:33PM
8 delay circuit 372 continues to make the fine timing
9 adjustments."

10 Unmodified -- when you say unmodified, 4:33:44PM
11 372, in my mind, and we talked about this many
12 times, 372 already has built into it the idea that
13 you need to do fine timing adjustments.

14 As I said, if you are not satisfied that 4:34:01PM
15 Hiraishi alone tells you to do fine timing
16 adjustments, Butt reinforces it. Butt makes it
17 clear.

18 So it's the exact same argument we had 4:34:15PM
19 when we talked about Hiraishi alone or Hiraishi with
20 Butt. And so this uses the -- basically, Tokuhito
21 builds on the Hiraishi and/or the Butt combination.

22 Q. You would agree, though, the reasons to 4:34:42PM
23 modify Hiraishi alone aren't necessarily the same as
24 the reasons to modify a Hiraishi/Butt combination,
25 right?

1 MR. CHANDLER: Objection, form. 4:34:59PM

2 A. When you say "modify Hiraishi alone," 4:35:02PM

3 we're talking about modifying it with Tokuhiro,

4 correct?

5 BY MR. LINDSAY: 4:35:07PM

6 Q. Correct. 4:35:07PM

7 A. Well, it's identical. I mean it's the 4:35:08PM

8 same thing. The optimization or the tuning that

9 goes on over in delay circuit 372 is not affected in

10 any way by the Tokuhiro combination. Tokuhiro

11 combination does nothing to change the operation of

12 delay circuit 372. 372 still has the fine-tuning

13 that it always had.

14 Q. Okay. So I want to ask you a question 4:35:45PM

15 about the claim limitation in Claim 1.

16 A. Okay. 4:36:07PM

17 Q. It's Element 1[i]. And we can look at -- 4:36:07PM

18 Paragraph 136 of your declaration has the quoted

19 term. It's in other places as well, obviously, but

20 we can start there.

21 A. Okay. If you don't mind, I'm just going 4:36:29PM

22 to be looking at it in the back of my declaration on

23 Page 247.

24 Q. Sure. No, that's fine. 4:36:38PM

25 A. Okay. 4:36:40PM

1 Q. So this claim element says, "Wherein the 4:36:42PM
2 first predetermined amount is determined based at
3 least on signals received by the first data buffer
4 during one or more previous operations."

5 A. Uh-huh. 4:36:54PM

6 Q. What is your understanding of what 4:36:57PM
7 "previous operations" means?

8 MR. CHANDLER: Objection, form. 4:37:02PM

9 A. It means operations that happened 4:37:05PM
10 previously. I mean operations that happened before
11 the current operation.

12 BY MR. LINDSAY: 4:37:16PM

13 Q. What is your understanding about the 4:37:16PM
14 meaning of the word "operations"?

15 MR. CHANDLER: Objection, form. 4:37:21PM

16 A. I think "operations" is a broad term, and 4:37:26PM
17 I think it can mean many different things. I think
18 I know what the patent says, but for my analysis, I
19 didn't really have to interpret that. Because I
20 looked at it from multiple different angles, and I
21 believe that my analysis finds that my combinations
22 read on this claim by using multiple different
23 interpretations of the word "operation."

24 So I didn't really come to a conclusion as 4:38:10PM
25 to what "operation" really means.

Page 214

1 BY MR. LINDSAY: 4:38:15PM

2 Q. So sitting here today, you don't have in 4:38:15PM

3 your mind an understanding of what the word

4 "operations" means?

5 MR. CHANDLER: Objection, form. 4:38:28PM

6 A. I can tell you what I said in my 4:38:37PM

7 declaration in Paragraph 99, that I understand that

8 there is some dispute about what it means, but I

9 didn't take a position as to what exactly it means.

10 Because as I said, regardless of which way you

11 interpret it, I believe that my combinations read on

12 any one of the possible interpretations.

13 So I don't take a position. I think 4:39:13PM

14 that's a decision, you know, that a court of law has

15 to make, and it didn't matter to me which way they

16 decide because these combinations satisfy it in any

17 of the possible interpretations.

18 Q. Sure. So the '506 Patent uses the term 4:39:39PM

19 "memory operations," right?

20 A. I believe it does, yes. 4:39:44PM

21 Q. What is your understanding, not in the 4:39:46PM

22 claims, but in the specification, what is your

23 understanding of what the '506 Patent means when it

24 says "memory operations"?

25 A. Well, I didn't opine on that because 4:39:57PM

1 "memory operations" are not used in the claim. So,
2 yeah, I don't think I'm willing to give an opinion
3 off the cuff as to what it means because, again,
4 it's a very broad term. It depends on the context,
5 it depends on how you are using it, and I know that
6 it has, you know, ramifications in claim
7 interpretation.

8 So it wasn't relevant to my opinion and I 4:40:36PM
9 don't feel qualified to give an opinion off the cuff
10 on this.

11 Q. That's fair enough. 4:40:48PM

12 MR. LINDSAY: I don't think I have any 4:41:06PM
13 more questions.

14 MR. CHANDLER: Can we go off the record? 4:41:13PM
15 I'll check my notes and we'll go from there.
16 So maybe 10 minutes?

17 THE COURT REPORTER: We're off the record. 4:41:32PM
18 (Recess was held from 6:41 p.m. until 4:56 p.m.) 4:41:55PM

19 CROSS EXAMINATION 4:56:01PM

20 BY MR. CHANDLER: 4:56:03PM

21 Q. Dr. Wedig, Jonathan, you see -- 4:56:04PM
22 (Technical difficulties.) 4:56:13PM

23 BY MR. CHANDLER: 5:02:38PM

24 Q. Dr. Wedig, I would like to follow up on a 5:02:41PM
25 couple of questions that Counsel for Netlist asked

Page 216

1 you earlier today, if that's all right with you.

2 A. Okay. 5:02:50PM

3 Q. So, there was a colloquy earlier in the 5:02:52PM
4 day, and I will read from the rough transcript some
5 of the questions and answers so that everyone can
6 find the precise questions and answers later on when
7 we have the final transcript.

8 Let me just read a little bit of the rough 5:03:12PM
9 transcript to help refresh your recollection of what
10 the colloquy was, and then I'll ask my questions
11 about it.

12 So there was a question along the lines 5:03:22PM
13 of -- this was all in the context of your annotation
14 of Figure 5 of Hiraishi.

15 There was a question along of lines of, 5:03:33PM
16 what about the red line coming down into the FIFO,
17 couldn't that be sampling the read data?

18 Answer, the LCLKR signal is what you are 5:03:44PM
19 referring to?

20 Question, yes. 5:03:47PM

21 And then there was more questions and 5:03:50PM
22 answers.

23 And then there was a question that I 5:03:54PM
24 objected to based on form because it was ambiguous
25 to me. The question was: So that signal clocking

1 out the data, sample the data, and then I objected
2 to data.

3 Do you have in your mind the question that 5:04:14PM
4 you were asked by Counsel for Netlist along those
5 lines?

6 MR. LINDSAY: Objection, form. 5:04:26PM

7 A. Just to make sure I'm looking at the 5:04:30PM
8 correct question, in the chat you had a kind of
9 prelude, kind of buildup, and then you had some dot
10 dot dot to show that there's some additional
11 colloquy.

12 And then the question you are asking about 5:04:44PM
13 is that, so that signal clocking out the data
14 cannot -- what do we think that should actually be
15 -- 'and fell' data cannot --

16 Q. Sample the data. 5:04:55PM

17 A. The 'and fell' should be sample the data? 5:04:56PM

18 Q. Correct. 5:05:00PM

19 A. And I said, no, it cannot because it 5:05:01PM
20 doesn't when the data is there, or it doesn't know
21 when the data is there until it's gotten into the
22 FIFO.

23 Q. So, that's the question and answer that I 5:05:11PM
24 want to focus on.

25 A. Okay. 5:05:16PM

1 Q. And to be clear, my recollection of the 5:05:17PM
2 question is that Counsel for Netlist asked you, so
3 that signal clocking out the data cannot sample the
4 data.

5 A. Okay. 5:05:33PM

6 Q. And then I objected to form. 5:05:34PM

7 A. Okay. 5:05:36PM

8 Q. So you understand what we're talking 5:05:36PM
9 about?

10 A. I think so, yes. 5:05:38PM

11 And so what is the question, specifically? 5:05:39PM

12 Q. What was your understanding of the 5:05:46PM
13 question you were being asked when you answered, no
14 it cannot?

15 A. So. What I interpreted that as, and maybe 5:05:54PM
16 we were speaking past each other because maybe we
17 misunderstood each other, what I was thinking was
18 you could not use that signal to be the first
19 mechanism for capturing the data eye.

20 Because as I said, in the answer, lower, 5:06:20PM
21 it doesn't know -- it doesn't know when the data is
22 going to be there, until it gets into the FIFO.

23 So, I may have spoken a little too 5:06:36PM
24 quickly. Because the LCLKR is a clock, and it does
25 clock the FIFO. So it does, you know, capture state

1 in a FIFO. It captures whatever is at the end, you
2 know, as it's shown in the diagram, and as shown in
3 Figure 5, it captures data at some point near the
4 end of the FIFO.

5 And so that is a way of catching data, 5:07:19PM
6 recording data, and then it's going to pass that
7 data on to the output.

8 And so by my understanding of the word 5:07:30PM
9 sample, sample meaning the normal English word of
10 sample; that is, to take a sample of or to get a
11 copy of, it does do a type of sampling.

12 What I meant to say was that it cannot be 5:07:46PM
13 the initial sample. It cannot be the thing that
14 catches the -- or determines what data is in the
15 data eye. It cannot substitute for the DQS signal.
16 Because only the DQS signal knows when the data is
17 valid.

18 So it does a type of sampling. It does a 5:08:10PM
19 type of sampling in that this samples the data
20 that's already in the FIFO, but it doesn't -- it
21 does not sample the initial data coming into the
22 FIFO. Only the DQS can do that.

23 That's what I meant to say. 5:08:27PM

24 Q. So for clarity, on Page 87 of your 5:08:30PM
25 declaration in Paragraph 129, where you have the

1 annotated Figure 5 of Hiraishi, can the red line
2 LCLKR be used, in your opinion, to sample the input
3 to the read FIFO?

4 MR. LINDSAY: Objection. 5:09:04PM

5 A. No, it cannot. Oh, sorry. 5:09:05PM

6 No, it cannot, because LCLKR does not know 5:09:06PM
7 when the data coming in from selector 334, it
8 doesn't know when that data eye is valid. It cannot
9 sample -- it cannot sample that input.

10 But it can sample the output, which is the 5:09:27PM
11 data that has already been captured by the DQS
12 signal and passed along to the FIFO. It can then
13 sample that known data in a FIFO and then pass it
14 out to the output buffer.

15 BY MR. CHANDLER: 5:09:49PM

16 Q. So, if I understand correctly, in your 5:09:52PM
17 opinion, can the red line LCLKR in Figure 5 of
18 Hiraishi be used to sample the output of the FIFO
19 read circuit 302?

20 A. Yes. 5:10:16PM

21 MR. LINDSAY: Objection. 5:10:18PM

22 A. I'm sorry. 5:10:19PM

23 Yes, it can sample the output because it 5:10:20PM
24 captures -- it does exactly what sample does, which
25 is to capture a copy of what is in the FIFO and then

1 forward that to the output. So it can sample the
2 output. It can't sample the input. Because it
3 doesn't know whether the incoming data is valid.

4 MR. CHANDLER: Thank you. I have nothing 5:10:43PM
5 further at this time. Pass the witness.

6 REDIRECT EXAMINATION 5:10:47PM

7 BY MR. LINDSAY: 5:10:53PM

8 Q. Yeah, I have a follow-up questions, 5:10:53PM
9 Dr. Wedig.

10 What is the difference between clocking 5:10:57PM
11 out data and sampling data?

12 A. Clocking out data is a little vague. I 5:11:13PM
13 mean, I'll tell you what I think it means. I mean
14 clocking out means to apply a clock to a data
15 register and capturing it, and then taking the
16 results of that and passing it to the output. So
17 clocking out simply is a type of sample, which means
18 that you, as I said, capture a value in the FIFO and
19 pass it to the output.

20 A sample is any time you transition a 5:11:48PM
21 clock signal or transition some type of edge in
22 order to capture a piece of data.

23 And clocking out simply has the 5:12:03PM
24 restriction that it means that it is performing a
25 sample to go to the output.

1 Q. And how does latching in data relate to 5:12:19PM
2 sampling data?

3 A. So latching in data, in my mind, would be 5:12:28PM
4 that you are sampling data at the input.

5 And in this case, in this system, when you 5:12:37PM
6 are latching in, it means that you are using the DQS
7 signal to tell you when the values on the input have
8 a valid, you know, valid value. And so latching in
9 simply means to perform a sample on the input of the
10 FIFO in this case.

11 Q. And going back to the same figure that 5:13:14PM
12 Mr. Chandler was asking you about, what page was
13 that again on?

14 A. Looking on Page 87. 5:13:22PM

15 Q. So the line that's coming down from -- the 5:13:55PM
16 red line that's coming down from the LCLKR, the
17 local clock, is a clock signal; is that right?

18 A. Yes, it is a clock signal, yes. 5:14:12PM

19 Q. And the signal coming down from 372, from 5:14:18PM
20 the delay circuit, that is a strobe signal?

21 A. DQS strobe, yes. 5:14:26PM

22 Q. And a clock signal is not a strobe signal, 5:14:29PM
23 right?

24 MR. CHANDLER: Objection, form. 5:14:34PM

25 A. No. That's correct. I mean they each 5:14:37PM

Page 223

1 have their purpose. But they're not identical, no,
2 that's correct.

3 BY MR. LINDSAY: 5:14:44PM

4 Q. I mean, no one would refer to a clock 5:14:44PM
5 signal as a strobe signal or vice-versa; is that
6 fair?

7 MR. CHANDLER: Objection, form. 5:14:55PM

8 A. I think one of ordinary skill would 5:14:57PM
9 understand the difference, yeah; I don't think they
10 would interchange that terminology.

11 MR. LINDSAY: Okay. No further questions 5:15:03PM
12 then.

13 MR. CHANDLER: That's the end of the 5:15:13PM
14 deposition.

15 To the court reporter, could I get a 5:15:16PM
16 transcript by -- on Monday, the 23rd so we
17 have an opportunity to review and make any
18 corrections, if necessary?

19 (Deposition concluded.) 5:15:28PM

20 THE COURT REPORTER: Sure. I have an 5:15:28PM
21 order for a rough draft tonight, too. Would
22 you like that as well?

23 MR. CHANDLER: Sure. 5:15:30PM

24 MR. LINDSAY: Will we get the final 5:16:02PM
25 transcript then on Monday, is that we were just

Page 224

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

talking about?

THE COURT REPORTER: Yes.

5:16:08PM

MR. LINDSAY: All right.

5:16:08PM

(Proceedings concluded 5:16 p.m. PST)

5:16:08PM

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

I declare under penalty of perjury that the foregoing is true and correct. Subscribed at _____, California, this _____ day of _____, 2023.

ROBERT WEDIG, Ph.D

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

CERTIFICATE OF OATH

I, the undersigned authority, certify
that ROBERT WEDIG, Ph.D appeared remotely before
me and was sworn on the 19th day of January,
2023.

Signed this 22nd day of January, 20223.



KIMBERLY FONTALVO, RPR
Notary Public, State of Colorado
My Commission No. 20214007135
Expires: 2/23/2025

CERTIFICATE OF REPORTER

STATE OF COLORADO

I, KIMBERLY FONTALVO, Registered Professional Reporter, do hereby certify that I was authorized to and did stenographically report the foregoing remote deposition of ROBERT WEDIG, Ph.D; that a review of the transcript was requested; and that the transcript is a true record of my stenographic notes.

I FURTHER CERTIFY that I am not a relative, employee, attorney, or counsel of any of the parties, nor am I a relative or employee of any of the parties' attorneys or counsel connected with the action, nor am I financially interested in the action.

Dated this 22nd day of January, 2023.



KIMBERLY FONTALVO, RPR, CLR

1 Robert Wedig, Ph.D.

2 bob@wedig.com

3 January 22, 2023

4 RE: SAMSUNG ELECTRONICS CO., LTD. vs. NETLIST, INC.

5 January 19, 2023, Robert Wedig, Ph.D. (JOB NO. 5664193)

6 The above-referenced transcript has been
7 completed by Veritext Legal Solutions and
8 review of the transcript is being handled as follows:

9 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Contact Veritext
10 to schedule a time to review the original transcript at
11 a Veritext office.

12 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Locked .PDF
13 Transcript - The witness should review the transcript and
14 make any necessary corrections on the errata pages included
15 below, notating the page and line number of the corrections.
16 The witness should then sign and date the errata and penalty
17 of perjury pages and return the completed pages to all
18 appearing counsel within the period of time determined at
19 the deposition or provided by the Code of Civil Procedure.

20 ___ Waiving the CA Code of Civil Procedure per Stipulation of
21 Counsel - Original transcript to be released for signature
22 as determined at the deposition.

23 ___ Signature Waived - Reading & Signature was waived at the
24 time of the deposition.

25

Page 229

1 _X_ Federal R&S Requested (FRCP 30(e)(1)(B)) - Locked .PDF
2 Transcript - The witness should review the transcript and
3 make any necessary corrections on the errata pages included
4 below, notating the page and line number of the corrections.
5 The witness should then sign and date the errata and penalty
6 of perjury pages and return the completed pages to all
7 appearing counsel within the period of time determined at
8 the deposition or provided by the Federal Rules.
9 ___ Federal R&S Not Requested - Reading & Signature was not
10 requested before the completion of the deposition.

1 SAMSUNG ELECTRONICS CO., LTD. vs. NETLIST, INC.
2 Robert Wedig, Ph.D. (JOB NO. 5664193)
3 E R R A T A S H E E T
4 PAGE_____ LINE_____ CHANGE_____
5 _____
6 REASON_____
7 PAGE_____ LINE_____ CHANGE_____
8 _____
9 REASON_____
10 PAGE_____ LINE_____ CHANGE_____
11 _____
12 REASON_____
13 PAGE_____ LINE_____ CHANGE_____
14 _____
15 REASON_____
16 PAGE_____ LINE_____ CHANGE_____
17 _____
18 REASON_____
19 PAGE_____ LINE_____ CHANGE_____
20 _____
21 REASON_____
22 _____
23 _____
24 WITNESS Date
25

&	110 141:6,7,12	1600 112:12	188:5
& 3:4 5:8	141:13 143:7	163 41:24	2000 17:6
229:23 230:9	114 122:10	43:10 107:2	55:15
1	128:13 133:25	164 108:19,20	2000s 16:25,25
1 4:11 10:14,18	134:5,7,10	165 108:18	17:3,4 55:13
99:17 126:9,16	116 121:24	16a 169:1	55:16
126:18 141:4	123:4,14,17,22	16b 169:1	2003 48:21
141:11,12	124:7	17 74:15 127:4	2005 17:6,15
211:16 213:15	118 41:12,14	169:2 175:22	48:9,15
213:17 230:1	11:07 63:13	170 41:25	2006-0277355
10 4:11 9:8	12 21:23	43:10	4:14
33:2,7,8,14,15	143:14 153:4	1800 3:4	2007-0008791
33:20,20,22	178:9 205:20	19 1:17 229:5	4:21
34:9,14,17	205:23	195 157:10	2008 49:19
36:13,14,24	124 123:10,13	210:15,17,18	2010 17:15
37:2 206:13	124:4	1977 11:22	49:10,18 55:15
216:16	129 84:9,11	1979 12:6	2010-0312956
10,860,506 1:11	91:24 100:4	1982 13:14	4:18
5:18 6:1	220:25	14:4	2012 21:5
100 18:25 19:1	12:24 99:22	19th 227:5	2021 17:25
1001 2:12	12:59 99:22	2	19:3
1005 43:4	12a 23:23 24:4	2 4:12 11:9,12	20214007135
101 2:6	13 21:21 153:5	11:13 121:19	227:15
1020 106:19,22	153:7,14,19	121:22,23	2022 19:5
1029 116:6	157:14 206:10	125:20,20	20223 227:7
104 125:23	136 213:18	126:7,14,18,19	2023 1:17
127:6 130:9,15	137 64:13	127:5,19,20	17:23 226:4
131:13,14	138 64:16	2/23/2025	227:6 228:17
133:24 134:6	140 89:16	227:16	229:3,5
134:10	144 4:22	200 2:12 58:12	2025.520 229:9
10:04 39:14	148 124:20,23	58:19 59:22	229:12
10:11 39:14	150 134:11,14	72:22 109:23	21 122:18,21,23
10:58 63:13	151 187:22,24	110:5,12,18	123:1,2 143:11
11 4:12	157 74:17	111:1,4,7,14	214 38:9
		120:9,13,14	

216 4:4 149:9 149:11 211:13 22 143:10 205:24 206:4 206:14 229:3 222 4:4 226 183:16,17 227 4:5 183:18 228 4:6 22nd 227:7 228:17 23 203:22 23rd 224:16 24 203:24 247 213:23 25 4:14 279 210:18 29 67:16 294 165:9,11 166:15 2:22 144:18 2:27 144:14 2:28 144:18	98:12,19 100:8 100:16 114:4 151:5 188:6 190:10,18 192:1 302 87:18,25 88:20 94:15 101:14,22 102:6,11 150:17,24,25 221:19 304 211:15 310 93:9 177:25 313 178:12 179:22 315 113:17 316 183:10,16 3190 227:12 228:24 320 100:7,14,17 113:10,12 114:1,4,9,10,13 188:6,12,19,23 322 93:9 323 78:15,20 135:1,5,11 33 43:17 331 92:23 332 92:23 149:19,25 333 92:23 334 87:13,25 88:20 92:23 149:22 221:7	34 102:13 206:9 340 87:23 341 86:8,25 342 86:12 87:2 351 86:2,9 352 86:6,12 3600 2:6 37 20:21 21:19 21:20 372 76:18 101:13 102:5 102:20 104:7,9 120:2 134:19 135:1 211:19 212:3,4,8,11,12 213:9,12,12 223:19 376 94:17 39 4:16 3a 122:10 123:10,20	42 4:17 205:22 205:23 44 23:22,24 46 127:23 47 35:17 4:09 203:10 4:14 203:10 4:56 216:18
			5
			5 4:3,17,17 9:7 26:23,23 27:4 27:9,12 28:21 28:24 29:1,7 30:8,14,20,21 31:1,2,11,22 35:19 42:6,7 42:21 58:4 84:15,21 85:2 88:12,14,15,19 88:22,25 89:2 91:15,23 92:3 95:24 96:3 100:2,4,13,19 100:20 101:9 102:14 144:5 149:14 150:7 151:10 153:2,4 202:19,20,23 203:21,21 217:14 220:3 221:1,17 50 18:19,22,23 18:24 26:22 27:1,10,11 28:4,6 30:2,16
3		4	
3 4:14,14 25:16 25:19 113:6,7 116:15,17 117:5 143:3,4 143:5 30 230:1 300 58:11,18 59:21 72:21 83:17,18 84:23 84:24 85:1,8 88:21 94:25		4 4:16 9:7,7 39:9,19 42:20 106:8,15 153:1 206:6 400 80:9,11,20 81:6,13,20,23 82:21 83:10,20 190:3,9,17,22 190:23 191:4,5 191:15,24 192:14,22	

[50 - accounted]

31:11 50/50 17:12,17 500 29:2 504 28:21,22,23 29:1,3,5,7,11 30:10 506 6:1 21:4 22:9,10,22,24 24:8,11 101:20 150:12 215:18 215:23 51 27:13 512 29:1,4 30:6 30:11,12 31:4 55 113:20 56 43:18 5664193 229:5 231:2 5:16 1:18 225:4	67 4:21 43:18 6:41 216:18 7 7 4:21,21 67:7 67:8,16 74:23 74:25 113:20 113:25 115:19 116:5,11,12 125:16 127:19 128:25 132:17 135:17 7,036,053 4:19 711 5:22 8 8 4:22 113:25 126:9 144:21 144:24 8,020,022 4:22 800 112:12 87 220:24 223:14 89 98:9 9 9 126:13 90 61:25 64:22 64:24 65:11 76:21,24 77:1 120:1,3,5,15 121:6,8,11,14 121:16 122:24 122:25 123:7 900 3:4 90067 3:5	94 64:13 94111 2:7 94304 2:13 99 215:7 9:00 1:18 a a.m. 1:18 39:14 39:14 63:13 ability 183:3 210:8 able 13:24 22:7 25:20 26:17 34:12 40:2 47:13 51:9,10 51:23 52:11,18 52:25 53:18 54:17 56:22 58:1 60:10 66:19 68:24,25 71:23 75:22,23 75:24 77:15 78:6 80:6 90:14 93:12 102:16,18 104:4,10,11 112:15 114:16 115:14,15 135:24,25 136:11,19 137:23 142:17 142:17 151:12 152:5,5,8,9,10 152:10,14,16 155:18 157:4 161:9 163:1	172:13,16 175:7,8,19 178:25 193:10 196:13 210:6 above 101:21 101:23 229:6 absolute 88:13 115:8 absolutely 137:11 172:11 accept 98:13 104:22 137:16 158:18 164:25 acceptable 121:3 acceptance 182:1 accepting 136:17 193:2 accepts 192:25 access 10:7 88:2,22 89:2,5 109:4 126:25 132:13 accesses 125:5 135:2 accomplish 160:8 account 7:8 79:16 95:13 120:4 171:24 179:1 accounted 170:17
6			
6 4:19,19 27:13 27:14,16 28:7 31:11 33:11 35:19 36:9,14 36:20,25 37:5 37:7,15,19,19 37:23 66:4,5 97:9,20,21 112:18,20 125:16 127:18 128:24,25 132:16 135:17 65 107:4 66 4:19			

[accounting - ahead]

accounting 162:22 175:25 176:4 accounts 167:19 178:24 accurate 7:8 11:20 79:9 158:12 166:19 199:11 achieve 161:9 achieves 161:3 acronym 117:10 act 7:21 74:21 75:3 207:7 action 228:15 228:16 activate 59:15 179:24 activated 59:18 110:11,13 150:22,22 activates 109:21,21 110:17,17 activating 60:20 activation 59:5 59:13 64:8 active 58:20 59:24 105:25 actual 9:22 15:5,12,13 23:12 96:15 125:12,13,16	127:13 130:2 130:22 131:20 131:23 132:3 132:24 133:2,5 133:5 154:13 155:16 actually 19:4 23:14 37:10 42:23,24 43:1 45:19 57:10 71:3 72:9 88:11,12 96:16 107:5 123:19 128:19 144:6 147:7 148:19 166:6 183:25 184:1 209:8 218:14 add 56:2,3 120:5 135:19 136:20 137:5 137:12,17,22 138:6,18 139:2 139:13 140:5 152:20 157:2 172:16 174:13 174:18,20 184:19 187:9 192:5 196:19 added 36:13 123:23 124:1 149:19 150:2 177:22 181:15 189:22 211:17	adding 120:1 138:3,11,22 151:4,18 184:21 193:5 addition 136:19 210:1 211:7 additional 19:13 20:13 24:20 34:11 36:12,12 46:24 124:12 135:20 135:23 136:6,7 136:13 137:5 151:25 177:9 189:16 192:12 197:25 200:18 218:10 address 25:10 80:8,15 190:2 191:4,15,23 192:21 adds 123:7 adequate 117:11 118:17 119:3 adjust 58:19 59:13 68:14 72:21 93:12,15 93:17 135:11 166:21 171:16 176:17 180:22 adjusting 64:8 93:20 173:11 179:24 181:11	adjustment 59:5 128:16 172:9 adjustments 64:7 176:11 211:20,23 212:5,9,13,16 adjusts 59:22 159:7 177:15 administrator 1:24 advantages 27:7 51:16 affect 111:9,10 118:25 affected 213:9 affects 73:5 afforded 160:9 afraid 63:6 agnostic 173:9 ago 17:13 82:14 176:15 195:7 agree 22:9,24 24:11 26:17 32:10 50:4 56:22 57:24 60:4 77:4 123:18 128:13 140:24 145:5 147:1 208:13 212:22 ahead 10:12 11:7 42:1 126:23 203:3
--	---	--	---

203:19 aim 99:17 aircraft 12:19 12:23 13:9 al 4:15,18,20 4:21 26:1 algorithm 130:19 131:24 131:25 133:5,8 133:12 137:2 193:20 algorithms 135:16 148:7 200:23 align 75:23 aligned 75:25 119:14 aligning 176:5 allocation 140:17 allow 48:2 68:15 89:21 92:17 allows 59:17 73:2,6 178:25 alto 2:13 ambiguous 217:24 amount 22:11 22:25 24:12 29:23 95:5 101:5 115:5 150:8 154:2,4 154:18 156:20 156:20 174:22	174:24 175:1 214:2 amplified 211:25 analysis 117:8 119:2 208:3,7 214:18,21 analyzed 194:15 angeles 3:5 angles 214:20 annotate 101:3 annotated 84:16 91:22 100:3 221:1 annotation 217:13 answer 7:22,25 8:6 46:15 48:3 49:7 51:1,3,10 51:21 52:4 74:3 138:4,16 197:18 217:18 218:23 219:20 answered 47:25 53:24 155:12 219:13 answers 7:9 140:25 217:5,6 217:22 anticipate 177:2 anticipatory 176:24 177:11	anybody 53:11 apart 182:20 apologies 10:15 21:11 49:21 106:18 apologize 37:3 apparatus 206:13 appeal 1:2 8:21 appear 166:3 199:8 appearances 2:1 3:1 appeared 227:4 appearing 229:18 230:7 appears 11:18 113:15,16 141:13 application 11:25 25:25 43:1 applied 113:10 114:6 124:3,6 applies 95:25 115:5 122:12 apply 95:22 121:3 122:15 154:15 161:4 162:17 164:18 172:4 173:6 222:14 applying 122:6 123:22 128:14	approach 116:21 117:7 appropriate 118:3 approved 18:12 approximately 9:7,7 14:10 17:6,24 18:14 april 49:19 architecture 28:9 38:15,18 38:22 area 14:18 66:20 140:17 areas 146:14 argument 212:18 arranged 29:2 arrive 161:20 161:24,25 arrives 58:21 59:24 161:17 178:14 art 19:6,13,22 21:3 44:23 45:9,25 61:7 62:18 68:7,11 69:9 77:10,20 79:22 118:13 119:12 130:5 136:2 200:7 211:2 artisan 183:12
--	---	--	--

[aside - benefit]

aside 163:10 179:9 asked 72:11 85:9 176:15 203:18 216:25 218:4 219:2,13 asking 8:6 22:19,21 34:22 34:25 35:16 50:22 77:20 85:19 130:3,4 203:15 206:21 209:4 218:12 223:12 aspect 47:4 51:6 57:4 70:7 aspects 12:22 140:2 assistant 13:18 13:19,20,22 14:4 associated 25:10 180:22 assume 7:12 68:20 assuming 91:9 110:25 122:3 assumption 137:18 139:21 139:21 attempt 94:20 attempting 95:18 attention 203:20	attorney 8:1 228:12 attorneys 9:1,5 228:14 august 17:24 17:25 authority 227:3 authorized 228:6 automatically 32:15 available 62:25 102:24 103:8 103:19 121:20 143:21 167:12 199:14 avenue 3:4 averages 129:22 aware 177:13 177:14 <tr> <td>b</td><td></td></tr> <tr> <td> b 183:24,25 230:1 back 6:15 16:8 16:18 19:3 22:5 30:3 33:25 34:1 39:15 43:14,16 52:22 56:11 63:14 72:9 79:3,8 81:11 91:22 94:4,8 94:11 98:1 99:1,23 112:17 </td><td></td></tr>	b		b 183:24,25 230:1 back 6:15 16:8 16:18 19:3 22:5 30:3 33:25 34:1 39:15 43:14,16 52:22 56:11 63:14 72:9 79:3,8 81:11 91:22 94:4,8 94:11 98:1 99:1,23 112:17	
b					
b 183:24,25 230:1 back 6:15 16:8 16:18 19:3 22:5 30:3 33:25 34:1 39:15 43:14,16 52:22 56:11 63:14 72:9 79:3,8 81:11 91:22 94:4,8 94:11 98:1 99:1,23 112:17					

 115:24 116:22 124:18 126:4 132:10,23 134:24 140:1 144:19 159:6 165:7 168:1,8 169:18 182:24 185:15,20,25 186:7,14,19,23 188:24 189:8 193:3 203:11 210:10 213:22 223:11 **background** 165:4 **baker** 2:6,12 5:11 **bakerbotts.com** 2:8,14 **bank** 29:2,6,7 29:15,17,20 **banks** 29:3 **base** 121:2,5,6 122:2,6,9,11,13 123:4,11 135:11 **based** 22:11 23:1 24:6,12 29:18 31:8,21 38:6 44:12 51:2 122:6 123:4 132:2,20 133:10 140:5,6 149:6 157:17 158:7 166:16 | 199:9,13,18 205:3 209:22 214:2 217:24 **basic** 56:5 148:3,7,15,16 152:12 193:8 **basically** 59:16 87:11 96:20 97:5 99:4 135:15 152:6 155:12 212:20 **battery** 63:8 **bc** 92:18 102:2 **beginning** 119:18,22 201:17,24 **begins** 169:24 183:17 **behalf** 2:4 3:3 5:11 **believe** 20:16 30:17 40:6 43:7 44:22 47:2,3 65:21 112:23 115:18 137:8 138:23 157:7,13 169:1 208:5,13,24 209:8 211:24 214:21 215:11 215:20 **beneficial** 74:25 **benefit** 162:1 178:13 182:15 |

[benefits - business]

benefits 179:2	69:24	74:14,20 75:6	175:11,15
best 16:10	bob 229:2	75:9,19,24	180:7,8,14,23
46:11 48:19	book 42:24	76:5,11 78:16	181:5 183:14
51:1 53:3	160:11	79:15 80:9,11	186:11,23
65:25 71:8,16	bottom 28:24	80:20 81:6,13	187:6,18,20
72:1,3,6 95:18	86:7,8,11,25	81:20 82:10,21	188:6 189:22
111:12 113:15	87:2 92:15,25	83:5,9,10,13,16	190:3,9,10,17
119:23 121:18	97:21 107:2	83:17,18,20	190:18,22
128:10 134:3,8	121:23	84:1,22,23,24	191:4,5,15,24
147:23 177:10	botts 2:6,12	85:1,8,20	192:1,22
better 11:11	5:11	86:18 87:3,5	195:23 201:19
51:4 52:16	bounce 206:8	87:10,21,21,24	201:23 202:4,7
57:4,5,13	bounds 108:10	87:25 88:1,19	202:11 205:3
117:19 156:17	110:11	88:20,21 89:21	209:15 210:10
156:25 173:13	box 30:9	91:14 92:15,16	211:9,17 214:3
177:12	125:18	92:19 93:2,22	221:14
beyond 19:14	boxes 30:12	94:25 96:18,21	buffering 167:9
50:6 52:8	break 7:15,19	97:2,6,25	buffers 58:20
53:17 60:19	8:7,11 39:13	98:12,17,19	59:23 60:20
159:2 165:21	99:15 144:10	99:2,6,8,11	63:21 64:9
165:21	202:25 203:3,6	100:8,16,23	80:17,18 81:7
big 151:14	bring 27:2	101:1,3,11	81:15 141:18
162:15 182:19	166:13	105:15 127:16	142:1 154:6
bin 107:11	bringing 191:8	127:16 131:2	174:7,13
bit 26:7 49:20	broad 98:21	131:13 134:9	179:24 183:2,4
122:20 168:16	214:16 216:4	135:21 151:5	193:24 205:14
203:4 217:8	brought 197:16	151:19,20	205:16 210:14
block 126:10	browser 10:6	162:3 163:1,21	build 77:11,21
126:14 127:6	buffer 24:5,7	167:5,7,15,21	78:6
151:15 152:18	38:14,18 58:11	168:1,5,9,13	builds 212:21
178:6	58:18 59:6,14	169:10,11,14	buildup 218:9
blocks 151:14	59:21 60:12	170:11 171:11	built 115:15
151:25	63:24 65:6	172:12,21	136:18 212:12
board 1:2 8:21	67:22 72:21	173:1,2,5,7,10	business 13:6
69:4,20,22,22	73:3,8,10,23	173:21 174:5	

[butcher - certainly]

butcher 165:13 butt 4:21 65:20 67:5,6,10,16 115:17 116:4 116:16 119:20 120:25 121:1,8 121:14,15,19 124:20 125:4,9 125:11,12,13 125:23 126:9 126:13 130:5,5 130:10,13,17 130:18 131:5 131:20,22 133:17 134:20 135:3,20,25 136:4,9,10,16 136:20,21 137:5,11,17,22 138:3,7,7,11,18 138:22,25 139:3,12,19 140:3 182:8 211:3,10 212:1 212:16,16,20 212:21,24 butt's 118:14 126:24 134:4 137:2 buy 136:18	calculate 131:21 159:23 165:1 196:13 209:14 210:9 calculates 124:20 128:7 calculating 157:17 158:6 164:19,23 calculations 152:15 206:11 calibrate 134:19 calibration 134:15 california 2:6 226:3 call 31:25 32:13,14 45:17 80:23 109:18 125:21 called 108:14 109:3 112:19 113:16 121:24 141:14 calling 178:3 181:21 191:6 calls 126:9 191:3,3 capabilities 199:4 capability 201:22 capable 49:25 50:4 192:22	capture 66:19 68:25 102:8,16 102:17 103:2 104:2,11 180:18 181:2 219:25 221:25 222:18,22 captured 105:7 170:1 181:12 221:11 captures 73:1,7 86:20 170:3 220:1,3 221:24 capturing 61:14 65:16 104:7 128:11 180:11 219:19 222:15 carefully 51:19 52:5 118:16 carnegie 14:5 carried 76:6 206:23 carry 131:10 201:7 carrying 126:24 172:8 207:19 cas 75:9,14 case 1:10 10:2 16:6,18,19 30:18 44:20 47:7 52:20 77:14 103:16 114:3,19 136:9	144:2 156:18 156:19 157:2 164:17 171:1,2 172:6 197:2 204:7 208:8 223:5,10 cases 16:13 catch 126:1 180:5 181:18 185:22 catches 220:14 catching 180:7 220:5 caught 81:10 cause 82:10 95:21 140:3 160:25 causes 75:9 ccp 229:9,12 ccra 1:25 center 97:21 121:10,11 181:3 centering 65:9 65:16 69:5,7 69:17 70:18,23 72:17 117:23 central 153:9 certain 26:5 95:5,6 108:11 141:21 142:15 142:18 153:14 200:2 certainly 27:6 81:14
c			
c 26:11 93:13 ca 2:7,13 3:5 229:9,12,20			

[certificate - circuit]

certificate 4:5,6 227:1 228:1 certify 227:3 228:5,11 cetera 28:12 206:12 challenging 5:17 chandler 2:7 4:4 5:10,11 6:7 6:16 22:13 23:3,10 24:14 24:17 25:4 29:10,16 35:3 37:17 39:13 42:11,16 44:1 44:25 55:4 57:15 60:23 63:11 65:22 66:15 67:11,14 67:15 69:11 70:24 71:14 76:7 77:6 78:17,24 80:22 81:9,21 82:22 83:21 85:3,24 88:3,24 91:6 97:10,17 99:17 103:9 105:19 110:8 117:25 122:16 128:8 132:7 135:13 135:22 137:7 138:21 140:12 142:6 143:22	145:11 147:12 151:6,22 155:3 156:13 158:10 158:13 159:9 161:10 163:23 167:23 168:14 170:12,15 173:24 174:3 175:17 176:2 176:12 177:18 178:20 179:16 181:23 183:5 186:20 187:7 187:16 188:14 189:2,12 190:11,19 191:18 192:2 192:11 196:1 197:3 198:3 199:12 200:15 201:14 203:7 207:2 208:11 208:18 209:7 213:1 214:8,15 215:5 216:14 216:20,23 221:15 222:4 223:12,24 224:7,13,23 change 50:14 109:20 151:15 151:19 182:10 185:7,8,8,12,13 189:10,15 192:7,10 194:7	194:13 213:11 231:4,7,10,13 231:16,19 changed 55:2 208:23 changes 119:14 119:15 151:11 152:13,21 177:9 200:14 200:19,21,22 208:2,7 changing 151:4 201:2 channel 185:16 185:21 186:1,7 188:25 196:9 196:11,14 characterize 158:15,20 characterized 58:23 charging 63:6 chat 218:8 check 78:19 131:18,18 198:9 202:15 216:15 checked 18:11 chip 58:12,19 59:22 72:22 75:12 162:15 chips 83:14 141:18 142:2 188:5	choose 148:6 chose 148:9 155:23 156:4 159:23 167:3 circuit 59:6 76:18 78:15,20 79:2,5,6,7,11 81:3,4,25 82:7 87:18 90:4,7 90:21,25 91:5 91:11,17,20 92:5,7 93:6,7,9 93:9,12,14,25 94:2,10 96:11 100:6,13,16,24 101:4,6,9,13,22 104:7 114:13 114:20 115:4 117:9 120:2 123:14 124:7 125:23 127:6 130:9 134:19 135:1,1,5,10 137:3,3 151:10 152:23 156:8 166:17 172:15 184:15,16,17 184:19,20 186:18 187:5 187:15,20 188:6,12,13,16 188:23 189:17 192:25 206:1,2 210:5 211:16 211:19 212:3,4
--	---	---	--

[circuit - combination]

212:4,8 213:9 213:12 221:19 223:20 circuitry 78:23 79:1 100:7,15 100:23 115:5 125:13 131:20 131:23 132:3 132:23,24 133:2,4,5,6,7,9 135:14,20,23 136:6,7,9,13,21 137:5,12,19,22 138:3,7,18,19 139:2,8,10,12 140:18 145:21 145:24 146:5 146:12 151:5 152:5 156:11 156:20 157:3 166:24 178:16 179:15 189:15 192:12,14 200:23 201:25 circuits 15:5 115:2 citation 113:18 cite 40:4,21 41:14 44:15 69:6 cited 40:17 44:20 65:15 66:12 69:4,9 69:15 106:23	civil 229:19,20 claim 22:15,16 33:2,7,8,11,14 33:15,20,20,22 34:9,14,17 36:9,13,14,14 37:5,7,7,10,15 37:19,19,23 38:4 139:12 177:3 194:14 213:15,15 214:1,22 216:1 216:6 claimed 102:1 claiming 33:5 claims 5:17 22:19 26:6 33:1,12 101:20 150:12 199:22 199:24 200:9 215:22 clarification 156:1 clarify 7:11 154:13 155:8 clarity 220:24 classes 12:16 12:16 clear 34:3 45:5 47:2 59:12 67:2 68:22 76:1 86:24 134:1 136:2,5 138:7 139:6 170:18 190:7	191:13 200:3 212:17 219:1 clearly 36:9 77:17 132:9,19 156:17 177:11 197:20 client 8:1 clients 14:20,22 15:21 clock 54:23 74:20 76:24 77:2 80:16 85:14,15 93:23 94:1 102:19,23 103:2 105:14 112:16 122:7 122:14 123:5,6 123:15,18,23 123:25 124:1,9 124:10,11 158:2,9 163:17 165:21,22 166:1,2,3,8,9 169:9,12,15,16 169:21 170:2,3 170:3,5 171:8 173:17 175:19 175:23 179:2 179:25 200:5 219:24,25 222:14,21 223:17,17,18 223:22 224:4 clocked 170:1	clocking 94:15 102:23 105:17 150:24 217:25 218:13 219:3 222:10,12,14 222:17,23 clocks 75:4,14 75:15 105:13 105:14 close 86:7 162:16 closer 142:8 177:7 clr 1:23 228:25 coach 7:20 code 229:9,12 229:19,20 colleague 5:13 college 12:3 colloquy 217:3 217:10 218:11 colorado 227:14 228:3 colors 84:17 column 108:14 109:22,24 113:20,25 205:20,23 206:9 columns 107:14,19,23 combination 62:4 118:14 151:3 171:23 176:1,25 181:9
--	---	---	---

[combination - component]

184:11 188:21 190:13 194:13 194:22 197:5 201:11,21 204:11 206:21 207:17 208:22 208:22,23 209:20 211:3 212:21,24 213:10,11 combinations 181:20 209:3 214:21 215:11 215:16 combine 136:16 157:8 160:13 170:20 179:6 197:13 198:13 210:23 combined 160:10 199:23 200:1 208:20 combining 186:3 come 31:23 52:15 53:9 59:10 75:23 86:1 91:5 92:7 94:21,23 97:8 97:16 165:7 182:21 198:23 207:16 214:24 comes 75:11,13 82:7 84:5 85:15 86:3,5	87:1,3 93:5 94:13 102:12 123:19 131:16 141:20 166:6,7 166:8 180:16 180:17 comfort 202:25 comfortable 23:14 54:8 coming 85:6,8 91:9 93:25 99:8,10 104:14 149:22,25 150:10,17 155:20 163:25 163:25 182:20 217:16 220:21 221:7 223:15 223:16,19 command 74:22 75:5,7 80:8,15 190:2 191:4,15,23 192:21 commands 80:25 81:18 96:23 97:1 comment 35:13 commission 227:15 common 46:4 46:21 communicate 22:4,6 25:12 32:4 96:18	183:4 193:24 196:12 210:6 communication 60:11 65:5 75:19 193:2 204:12 communicati... 194:10 companies 14:23 15:15 17:10,11 company 14:17 compare 70:9 comparing 45:18 78:8 comparison 130:2,14,22,23 132:3,18,20 compatibility 32:2 compatible 28:11,12,16,19 142:17 competent 14:19 complaint 31:18 complete 20:10 44:6 121:9 125:11 completed 170:8 229:7,17 230:6 completely 104:5 106:3,4	125:15 completion 230:10 complexity 178:23 compliance 33:14 34:16 36:10,11,17 compliant 26:10,15 27:18 28:14 30:15 31:7,13,16,20 32:15,18,21 33:6,10,13,17 33:22 34:8,10 34:13 35:1 36:4 40:3,8,14 40:16 41:7,10 43:23 44:4,24 45:11 46:1,20 47:8,13,16 52:11,13,24 57:12 120:12 complicated 162:10 173:16 173:19 complication 161:1 comply 47:23 component 13:2 40:3 87:4 88:1,21 95:25 110:22 112:1 121:24 126:24 146:2
---	---	---	---

[components - controller]

components 13:7 15:2,3 21:12,22 32:20 62:25 63:2 89:1,5 95:23 140:17 148:15 comport 48:22 comprised 30:12 computation 193:6,20 194:1 194:25 210:8 computations 24:21 compute 189:4 computed 186:22 computer 6:9 12:21,22,23,24 13:7,25 14:1 14:18,24 15:2 21:10,12 27:3 66:17 153:8 207:11 concept 55:23 56:5 concluded 224:19 225:4 concludes 138:12 conclusion 214:24 concurrently 12:12	configuration 210:14 confirm 42:9 188:2,7 confuse 123:24 confused 186:2 187:2 connected 67:21 153:5 205:6 228:15 connection 99:10 consider 18:13 consideration 140:19,20 considered 48:9 98:22 110:10,18 170:7 considering 31:11 152:2 consistent 147:3 constrained 140:11,13 consultant 16:13 consulted 20:16 consulting 14:12,16,17,18 14:21 15:4,9 15:16 contact 229:9	contacted 17:22 18:1 contain 139:10 contains 141:17 contents 157:11,14 context 50:21 112:22 216:4 217:13 continue 124:19 continued 3:1 continues 108:13 211:19 212:5,8 continuing 87:17 control 25:10 32:24 79:2,5,7 80:13,15,16 81:2,3,3,24 82:6,6 90:3,7 90:21,25 91:5 91:10,17,20 92:5,7,9,11,16 92:20,25 96:11 96:14 100:6,7 100:12,15,16 100:23,24 101:4,6,8,10 114:8,13,16,21 114:22 115:2 115:14 123:9 123:15,16,18	124:3,12 125:14,16 127:17 128:4 135:15 145:2 151:8,10 152:12,21,23 153:22,23 154:1,2,8,10,14 154:20 155:1 155:13,20 162:17 174:14 174:18,20 187:19 188:6 188:12,16,23 189:14,17 190:2,9,23 191:4,15,23 192:13,21 203:22,24 204:2,3 205:24 205:25 206:4 206:12,14 207:14 210:5 controlled 113:12,16 170:21 controller 13:13 23:9 25:3,6,9 55:3 67:21 73:10,19 73:23 74:14 75:7,11,12,16 76:5,6,9,16 78:12 79:3,4 79:10,14,19,24
--	--	--	--

[controller - correct]

80:4,9,12 81:8	169:13,13,18	209:10,12	24:10 25:7
81:15,23 82:7	169:21,23,23	210:7,9	26:18 31:3
82:16 83:9,10	170:10,21	controller's	32:12 35:10,22
83:24 84:1	171:3,4,6,11,16	178:16 179:15	40:20 41:17
87:23 94:5,8	171:18,25	controllers	49:16,21 52:6
94:12,19,22	172:1,7,11,18	13:11 21:13,17	55:10 60:5
96:19 97:8,16	173:8,12,15	22:2 173:22	61:20 71:12
97:20 98:1,25	174:4,23	controlling	73:3,7,12
99:3,12 105:8	175:14,14	92:19 114:4	76:10,15,23
105:16 113:13	176:17,18	123:13 172:6	78:13 80:10
113:14,25	177:16,17	177:21	81:16 82:19
114:4,7,11	178:1,2,3,4,9	controls 93:1	83:6,11,18
125:22 130:8	178:14 179:23	93:11,14 125:7	84:8,24 87:7
130:16,25	180:13,21	127:1	88:23 98:14
133:12 143:14	181:8,10,20	conventional	110:2 111:19
143:16,20	182:9,13,16,23	116:21 117:7	112:24 113:14
145:3,10,12,14	182:24 183:3	conveyed	114:2 115:10
145:19,21,22	184:1 185:16	109:13	129:13 133:1
145:23 146:3,5	186:12,23	conveying 98:3	138:20 143:12
146:7,8,11,21	188:25 189:8	108:24	143:15,18
151:13 153:4	189:20,24	copy 9:13,14,15	145:3,21 150:4
153:15,20	190:1 191:7,12	20:22 27:2	151:1 153:6,12
155:21 157:22	191:17,25	42:13,25 58:6	153:17,21
159:8,11,13,18	192:14,17,24	107:6 220:11	155:23 159:8
159:24 160:5,6	193:9,12,17,21	221:25	161:6 162:8,9
160:17,18	194:3,5,19	corner 43:2	164:2 168:10
161:5,8,17,20	197:1,9,12,14	106:20 107:3	178:11,17
161:23,24	197:20 201:6,8	corporation	185:5,18 187:6
162:6,6,12,14	201:18 202:1,2	14:14	189:6,23 190:3
162:15,20	202:13 203:16	correct 9:20	190:21 195:12
163:5,18,22	204:4,8,12	11:23 12:1,7	197:24 200:16
164:1,11	205:2,4,5,8,12	12:11 13:15,16	201:11 202:9
166:17,21	205:15 206:17	14:5,6,9,13	202:11 203:18
167:1,6,20,22	206:24,25	15:6 19:25	204:4,5 210:4
168:3,4,12	207:5 208:16	21:6,7,14 24:9	213:4,6 218:8

[correct - data]

218:18 223:25 224:2 226:2 corrections 224:18 229:14 229:15 230:3,4 correctly 58:23 68:24 77:24 85:23 90:24 97:3 117:18 180:18 183:22 195:6 221:16 corresponding 109:23 counsel 7:20,24 19:11,12,22 202:24 216:25 218:4 219:2 228:12,14 229:18,21 230:7 counted 44:16 couple 53:8 107:3 116:20 216:25 course 23:25 76:11 78:3 89:11 111:16 139:2 156:24 178:22 183:3 190:4 197:12 207:4 courses 56:1 court 1:1 5:1 6:25 39:10,15 43:13 63:12,14	99:20,23 126:3 144:17,19 202:24 203:9 203:11 215:14 216:17 224:15 224:20 225:2 cover 37:19 covered 38:5 covering 36:24 37:5,15 cpu 153:5,7,7 153:14,19 155:20 162:9 178:6 202:13 203:17,22 204:8,12,15 205:6,10,11,18 206:5,7,10,16 206:22 207:6,8 207:12,16,20 207:23,25 208:3 create 40:2 created 171:23 creation 18:12 criteria 47:17 cross 4:4 203:6 216:19 crosstalk 95:21 111:8 cuff 216:3,9 current 98:11 98:18 214:11 currently 15:20	curriculum 4:12 customers 108:9 cv 11:18,19 14:7 cycle 77:2 122:24 158:2,9 159:18 163:17 166:3 173:17 179:2 cycles 76:25	70:23 72:17,21 73:2,2,6,8,10 73:18,22,23 74:13,20 75:6 75:9,10,17,18 75:23,23,25 76:5,11,12,13 78:16 79:1,3,4 79:7,15 80:17 80:18 81:2,3,3 81:7,15,24 82:6,10 83:5,9 83:13,15,17,18 84:1,22,23,24 84:25 85:1,6,7 85:8,19,20,25 86:9,17,18,18 86:20,20 87:3 87:4,5,10 88:1 88:2,21,22 89:6,21 90:3,3 90:6,18,21,25 91:2,4,5,8,8,10 91:10,14,16,19 92:5,7 93:22 94:2,13,15,25 95:1 96:11,14 96:18,21 97:2 97:6,25 98:11 98:16,19 99:2 99:5,8,11 100:6,7,12,16 100:23,24 101:1,3,4,6,8 101:11 102:5
		d	
		d 4:1 26:11 d1 153:13,22 155:1,5,14,19 204:3 d2 153:18,22 155:1,5,14,19 204:3 dashed 96:2 101:12 data 24:5,7 31:24 32:9 47:13 54:10,10 54:16,23 55:2 55:3,10,10,17 56:8,17 57:14 58:11,18,21 59:17,24 60:12 61:15,15 62:7 63:21 64:17,17 65:5,9,16,16 66:18,19 69:5 69:7,17 70:18	

70:23 72:17,21
73:2,2,6,8,10
73:18,22,23
74:13,20 75:6
75:9,10,17,18
75:23,23,25
76:5,11,12,13
78:16 79:1,3,4
79:7,15 80:17
80:18 81:2,3,3
81:7,15,24
82:6,10 83:5,9
83:13,15,17,18
84:1,22,23,24
84:25 85:1,6,7
85:8,19,20,25
86:9,17,18,18
86:20,20 87:3
87:4,5,10 88:1
88:2,21,22
89:6,21 90:3,3
90:6,18,21,25
91:2,4,5,8,8,10
91:10,14,16,19
92:5,7 93:22
94:2,13,15,25
95:1 96:11,14
96:18,21 97:2
97:6,25 98:11
98:16,19 99:2
99:5,8,11
100:6,7,12,16
100:23,24
101:1,3,4,6,8
101:11 102:5

[data - declaration]

102:11,12,24	168:1,1,5,8,8	220:21 221:7,8	46:1,7,17 47:8
103:3,6,7,17,18	168:13 169:9	221:11,13	47:13,16,23
104:3,3,7,8,8	169:11,14	222:3,11,11,12	48:7,8,18 49:3
104:12,16,25	170:11 171:11	222:14,22	49:10,12,18,22
105:1,4,12,15	172:12,21	223:1,2,3,4	49:25 50:11,14
105:17,18,21	173:1,2,5,7,9	date 229:16	51:13,17,20,24
105:22 106:1	173:10,13,21	230:5 231:24	52:24 53:19
108:15,22,23	174:5,7,12	dated 228:17	54:4,17 55:1
108:25 110:6	175:11,15	day 19:4,4	55:12,19 56:7
111:22 113:17	176:4,6,9	217:4 226:3	56:16,25 57:3
117:11,23,23	178:14 180:4,6	227:5,7 228:17	57:12 62:17
118:10,18	180:7,8,11,14	dayton 11:22	106:9 107:13
119:4,5,6,6,7,8	180:16,18,20	dd3 52:11	107:16 112:12
119:10,15,16	180:25 181:1,3	ddr 56:3 67:20	112:12 147:13
120:13,13,24	181:5,11,12,16	102:22 118:1	147:17,21
122:3 127:7,10	182:2,20,21	125:22 134:9,9	ddr3-1066
127:12,13,14	183:2,4,13	147:10,24	107:15
127:16,16	184:4 186:11	ddr2 30:11,15	ddr3-800
128:11,13	186:23 187:6	30:23 31:4,5,7	107:15 109:23
129:8,25 131:1	187:20 188:5,6	31:14,16,21,25	decide 82:2,11
131:14,14	189:17 190:10	32:4,5,7,11,13	114:24 215:16
133:15 134:4,9	193:24 195:23	32:20 48:15,17	decided 179:11
135:20 141:18	201:19,23	48:19,21 49:2	deciding
142:1 146:15	202:4,7,11	49:14,23 50:1	199:17
147:7,8 150:20	205:3,13,16	50:11,13 51:14	decision 9:25
150:24 151:5	209:15 210:4	51:17,24 52:13	132:19,20
151:18,20	210:10,14	53:2,19 54:1,4	215:14
152:22 154:3,3	211:9,9,17,21	54:18,25 55:1	declaration
154:4,5 161:17	214:3 217:17	55:12,18 56:7	4:11 9:14,15
161:20,24	218:1,1,2,13,15	56:18 57:1,14	11:4 18:2,8,15
162:3,7 163:1	218:16,17,20	ddr3 4:16	19:7,24 20:4,6
163:21,25,25	218:21 219:3,4	39:23 40:2,8	20:11,14,18,20
165:24,25	219:19,21	40:17 43:20	23:19,22 38:10
166:2,4,6	220:3,5,6,7,14	44:10,24 45:1	40:5 41:12
167:5,7,14,21	220:15,16,19	45:2,11,13,15	44:17 50:16,21

[declaration - deposition]

52:7 55:9 61:9 64:6 76:21 84:10 89:4,8 90:5 91:1,23 100:3 106:23 112:22 124:19 134:12 138:2 149:9 157:7 165:8,10 166:15 193:12 195:8 198:6 210:16 213:18 213:22 215:7 220:25 declare 226:1 decrease 114:5 decreasing 112:5 114:10 dedicated 155:20 deficiencies 200:8 deficiencies 200:3,6 defined 96:15 defining 96:16 definitely 134:7 definition 36:18 degree 120:15 121:16 degrees 61:25 64:22,24 65:11 76:21,24 77:1 120:1,3,5	121:6,8,11,14 122:24,25 123:7 delay 22:11 23:1 24:12,22 64:24 65:1 75:8,17,18 76:18 101:13 113:9,10,12 114:1,4,5,9,9 114:13,20 115:2,4,6,7,12 115:16 120:1,1 120:15 121:2,5 121:6,24 122:2 122:6,6,9,11,13 123:3,4,4,9,13 123:14 124:1,4 124:6,7,8 128:2,14 132:11 134:19 134:25 135:1 135:11 137:3 139:24 145:2 151:2 152:8,9 152:11,15,17 153:14,19,25 154:2,4,6,6,15 154:15,19,20 154:21,23,24 155:2,13,16,17 161:4 163:7,25 164:9,15,18 172:6,8,9,12,14 172:17,22	173:1,2,5,7 174:14 175:5,6 176:4,11 177:22 180:19 182:25 189:5 189:21 190:9 190:17 191:25 192:23 193:3,3 193:13 194:19 197:1,9 203:22 203:24 204:3,7 204:16 205:24 206:1,1,2,4,13 206:16,23 207:15,21 209:10 210:1,7 210:9 211:16 211:18 212:3,4 212:8 213:9,12 223:20 delay's 164:6 delayed 101:19 102:1,4 103:24 104:6 150:5,9 150:11,14,19 150:22 212:4 delaying 64:22 131:16 150:7 delays 76:20 79:16,18 104:22 123:7 145:8,14 146:13,14,16 146:19 157:17 157:17,21,23	158:1,7,7,8,8 159:7,17,23,23 161:3,4,16,21 162:14,19,22 162:23,24 163:4,5,8,12,14 163:16,20 164:2,3,19,23 165:1,2,20 166:11,21 167:20 170:10 170:16 171:2 171:12,12,17 171:25 173:11 173:16 175:1 175:14 176:1 176:17 177:15 178:15 179:1 180:22 184:12 196:10,16 200:5 205:2,3 205:16 209:15 211:18 dependent 26:6 depends 147:5 177:2 216:4,5 depicting 149:13,14 deposition 1:15 5:16 8:14 9:2 20:5 224:14,19 228:7 229:19 229:22,24 230:8,10
---	--	--	---

[depositions - diagram]

depositions 27:7 describe 38:2 43:19 47:22 68:17 69:1 70:18,23 72:7 73:16 77:14 89:5 138:2 146:1 described 19:23 26:22 37:20 41:22 58:16 60:14 62:22 64:6 69:5,16 72:4,5 74:1,19 77:25 127:18 131:24 131:25,25 132:5,8,9 133:2,4,7 175:15 describes 37:7 37:19 58:10 62:12 64:15 65:16 66:16,17 72:16 73:9 77:4 80:8 113:3 119:25 125:4,23 135:3 164:17,19 194:18 describing 23:23 24:4 26:9 27:18 31:12 36:3,20	40:18,22 41:16 44:15 45:11 66:12 107:9 111:24 117:14 117:15 134:14 158:1 description 34:7,17 35:7 37:24 40:22 43:24 44:21 64:15 124:20 132:2 design 12:10,19 13:1,3,3,4,6,7 13:12 14:24 15:12,13 21:10 27:22 38:17 53:16 56:1 95:9 115:15 117:17 140:18 140:21,23 156:8 designations 32:21 designed 12:21 12:24 15:2,8 47:12 52:24 designing 13:1 13:5,8,10,11 132:2 140:16 designs 117:16 detail 44:6,10 52:19 60:17 62:13 65:21 68:18 74:1	80:2,5 98:6 122:9 141:22 141:22 148:10 175:15 182:18 193:15,18 202:15,18 detailed 47:4 51:8 52:18 62:16 74:7 126:14,19 127:5 details 34:11 73:20 79:24 89:24 90:16 147:19,21,25 157:20 158:15 detect 152:8 172:13 detected 169:11 170:16 detecting 13:23 172:22 173:11 detects 172:17 determine 24:21 59:15 75:21,22 76:13 108:6 117:10 119:2,9 121:2 154:5 determined 139:10 214:2 229:18,22 230:7 determines 75:17 118:17	220:14 determining 22:10,25 24:5 24:12 129:1 deviation 195:20 device 30:5 31:24 32:4,25 41:5 43:20 45:13 46:4,7 48:8 65:5 79:8 86:3,5 93:22 93:23 95:5,8 95:13,15 96:6 108:1,7 110:9 110:14 111:6 111:13,18,20 111:25 117:24 118:5 119:12 120:12 125:12 130:8 173:10 180:8 devices 29:1 31:14,17,19 32:8 45:15,15 60:11 99:13 106:9 107:13 107:25 108:6 112:11 142:3 184:5 diagram 84:22 88:4,8,9 113:22 126:10 126:14 127:6 129:1 130:1
---	---	--	---

[diagram - doing]

132:4 141:20 149:10,13,14 220:2 diamond 132:16 dictate 149:1 die 63:7 difference 54:9 54:13,15 69:19 109:15,19,20 110:16 164:7 172:24,25 183:25 184:3 222:10 224:9 differences 50:13 51:24 53:19 54:4 56:7,13 179:12 different 12:22 12:22 15:1 35:20,25 36:19 45:6 48:14 69:6 78:23,25 86:5 95:14 106:7 107:3,12 107:16 118:24 121:1 128:22 131:4 135:2 140:2 162:7 177:8 183:2,23 186:3 205:20 209:16 214:17 214:20,22 differently 24:18	difficult 112:15 167:8 196:17 difficulties 216:22 difficulty 45:21 digital 56:1 dimension 110:1 dim 141:14 141:16,25 142:5,16,20 143:7,17,21 144:1 dimms 143:24 162:24 direct 4:3 5:14 35:4 37:18 203:20 directed 145:9 207:11 direction 129:20 207:6,8 directly 53:24 97:18 164:19 197:18 211:23 disadvantages 51:17 disagree 26:17 202:16 disclose 63:19 100:22 145:5 145:17 184:22 185:24 186:6 195:3,22 196:8 197:7	disclosed 50:18 77:25 131:21 159:16 166:25 187:4 195:17 discloses 22:10 22:25 24:11 35:24 36:8,9 38:13 62:11 113:9 145:7,20 146:23 147:2 166:18 184:25 185:1,8 191:14 195:10 202:12 212:6 disclosure 22:21 34:23 47:22 60:19 131:5 189:11 196:22 disclosures 88:17 disconnected 155:1,5,7 discuss 55:9 89:4,23 165:8 discussed 19:7 19:24 54:11 89:6 112:21 136:21 144:7 168:24 179:20 210:3 discusses 21:2 27:13 65:20,21 67:18,20 100:25 136:8	discussing 41:15,20 43:23 discussion 6:13 10:19 39:12 64:11 106:11 144:16 165:5 203:1 209:13 209:17 discussions 200:24 dispute 215:8 distributed 38:14,18 distributes 80:16,17 dll 93:7,9,11,14 93:25 document 11:1 11:15 18:3,5 25:22 39:22 40:4 43:5 65:15,19 196:6 documents 8:17,19,20,23 9:9,12 10:4,9 10:10 53:18 57:25 doing 15:25 17:1,9,10 19:25 32:9 60:5 63:1 70:7 70:11 82:24 83:1,24 90:13 93:20 95:18 98:17 114:10
---	---	--	--

[doing - efficient]

118:13 125:14 128:18 131:15 135:15 137:23 139:24 147:18 148:3 149:4 159:12 160:2 162:21 164:5 164:10,14,21 173:7 175:20 176:1,3 179:2 181:24 193:5,6 193:20,22 194:11 198:11 205:4 dot 218:9,10,10 double 31:24 32:9 download 67:11 dp 122:3 128:2 dp114 129:5,24 dq 66:20 86:8 87:1,2,14,22 88:2 89:5,20 90:6,18,20,25 95:1 102:13 104:3,7 105:3 109:1,3,16,21 110:6,17,23,23 111:24 118:3,7 118:11,21 180:10 181:1 181:16 182:5 211:21	dqe 88:22 dqs 61:21,24 64:22,24 66:20 86:2,4,9,13,18 93:21 94:3,7 95:1 96:5,9 101:18,22 102:25 103:1 103:21,23 104:2,6 105:2 105:3,23,24,25 106:1 109:1,3 109:3,17,20 110:6,11,12,16 110:23,24 111:25 118:3,7 118:11,21 119:12,14,14 120:16 123:19 149:21 150:1,7 150:9,21,22 169:9,10,20,25 170:1,4,6 171:7 175:22 176:5,8 180:10 180:19 181:1 181:17 182:1,5 211:20 220:15 220:16,22 221:11 223:6 223:21 dr 4:11 5:16 6:18 9:14 39:18 42:22 63:16 100:2	132:22 144:23 150:21 203:14 206:2 211:16 216:21,24 222:9 dr1 149:19 150:2,5,10,15 150:17,24 151:2,18 152:11,20 154:22 draft 224:21 dram 30:6 drc 80:24 96:10 96:12 97:15,18 97:19 186:24 193:1 drf 97:23,24 98:3,10 185:16 185:20 186:1,7 188:24 189:8 192:25,25 196:9,11,14 driver 152:17 drives 93:6 drq 150:19 dual 141:16 due 118:22,23 164:2 dummy 75:10 76:12 79:2 91:2,7,8,9,16 dw 206:1 dw1 155:15,16	dw2 155:16 e e 4:1 26:11,11 65:24 66:2 229:9,12 230:1 231:3,3,3 e.g. 28:12 earlier 52:14 61:12 107:24 112:7 115:18 118:5 128:25 144:7 147:17 168:2 181:21 189:13 209:13 210:23 211:24 217:1,3 early 16:25 17:3 easier 57:5 58:6 126:8 157:11 easily 133:9 easy 10:7 edge 119:14 222:21 effect 6:25 55:13 154:20 effectively 64:1 170:13 efficiencies 160:9,12 161:3 efficiency 161:9 efficient 160:22 162:19 173:20 194:8,16
---	--	---	---

eight 174:8 either 49:4 114:5 132:6 134:6 197:7 206:23 208:6 electrical 28:10 electronic 95:15 96:1 140:21 electronics 1:4 5:12 43:3 55:25 229:4 231:1 element 38:4 150:2,5 151:2 154:22 155:16 172:6,8,12 177:22 182:20 182:21 189:21 190:17 191:25 193:13 194:19 194:24 210:1 213:17 214:1 elements 153:14,19,25 154:15,22,23 154:25 155:2 155:13 171:13 174:14 177:3,5 190:10 192:23 193:3,4 194:24 197:1,10 204:4 204:7,16 206:17,23 207:21	ellsberry 4:14 26:1,2,5,9,14 26:22 27:2,17 29:5,14,19 31:12 32:3 33:2,5,12,21 34:5 35:1,24 36:3,8,16,21 37:6,16 38:13 38:16 39:1 ellsberry's 28:14 29:17 33:9,17 34:23 38:22 embodiment 33:16 34:17,20 35:1,5,7,9,14 36:11,18,20,22 36:24 37:5,15 38:3,5 126:11 127:8 206:14 206:24,25 embodiments 35:21,25 36:3 36:15 37:8,25 emphasis 117:9 employee 228:12,13 enable 59:16 187:18 enabling 63:24 92:16 93:1 encoded 174:19 encompasses 127:15	encounters 87:5 engineer 12:10 12:19 english 220:9 enhance 70:15 ensure 70:11 enter 73:2,7 entire 18:5 85:12 127:16 entirety 158:19 entitled 145:2 environment 140:11,13 equal 156:10 156:14,24 equally 202:3 equating 101:25 150:10 equations 193:19 equipment 206:11 errata 229:14 229:16 230:3,5 error 191:2 errors 20:6 especially 173:14 175:6 esq 2:7,13 3:5 essentially 21:15 73:17 122:25 171:22 211:9	established 56:25 et 4:15,18,20,21 26:1 28:12 206:12 eventually 14:15 evidence 10:2 ex 4:14,17,19 4:21 exact 27:21 64:25 79:24 90:8 121:15 180:6 193:19 193:20 212:18 exacting 154:17 exactly 17:12 17:16 22:15 28:16 45:5 48:18 53:18 58:24 66:20 67:18,22 68:4 70:8 73:4 96:13 101:23 102:20 108:17 147:6,8 181:4 193:25 196:4 201:9 209:25 215:9 221:24 examination 4:2 5:14 216:19 222:6 examiner 77:17
---	---	---	---

[example - fair]

example 8:7 30:10 89:15 91:14 95:23 127:7 128:1 167:4 202:3 examples 28:17 except 100:23 execute 14:1 executes 206:10 exemplary 211:15 exhibit 4:11,12 4:14,16,17,19 4:21,22 9:17 10:13,14,18,21 10:23 11:8,9 11:12,13 25:15 25:16,19 39:8 39:9,19,19 42:6,7,20,21 43:4 58:4 66:4 66:5 67:7,8,12 67:16,16 106:7 106:8,12,15,19 106:19,22 112:18,18,20 115:19 116:2,5 116:6,9,11,12 144:21,24,24 exhibits 4:8 9:16,18 10:21 exist 88:13 174:19	existed 48:17 48:20,24,24 existing 28:11 28:17 152:22 211:18 212:3,4 212:7 exists 137:9 exit 119:12 exiting 87:20 exits 119:13 expect 51:25 52:3,6 53:7,13 53:21,25 54:5 54:6 57:16,19 expectation 56:16 expectations 52:8 expected 10:16 53:16 57:13 132:15 experience 11:25 12:8 114:12 experienced 176:18 experiences 13:22 expertise 14:25 expires 227:16 explain 36:5 71:16 94:6 130:6,10 147:19 149:5 157:22 193:17	explained 125:16 explaining 112:22 explains 125:15 125:18 130:13 193:14,25 explanation 34:5 71:9 72:1 74:7,16 133:10 208:20 explicitly 90:20 198:24 206:20 207:3 express 196:22 expressed 189:11 expressly 63:19 63:22,23 64:2 130:5 184:22 185:7,21,24 191:14 195:3 195:11,17 196:25 extend 165:21 extensively 108:6 extent 44:12 73:4 142:12 eye 61:15 64:17 65:16 104:3,8 104:8 113:17 181:3,12 182:2 219:19 220:15 221:8	f fact 32:6 33:7 33:11 54:20,24 70:3,3 77:16 89:1 90:11 92:3 104:21 111:2 112:11 136:18 138:25 156:23 167:4,8 168:25 194:13 195:10 201:23 207:24 208:3 fail 129:11,12 fair 7:13 8:8 14:12 17:14,19 19:20 20:3 24:16 26:20 29:12 31:12,19 32:3 33:16 34:25 35:24 36:1,2 39:3 47:6 49:9 50:10 51:12 52:11,21,25 53:6 54:19 55:13,20 56:15 57:2,3 77:19 79:13 106:6 127:21 137:6 140:9,10 142:4 158:3 159:5 177:14 189:19 206:18 216:11 224:6
---	---	--	---

[fairly - fine]

fairly 193:8 false 7:4 familiar 56:13 171:20 202:14 family 32:8 far 92:15 117:14 182:20 fashion 73:19 173:14 fast 97:13 110:4 112:12 112:16 142:13 faster 50:1,5,7 50:14,15 52:12 52:16 53:1 54:1,7,20,21,22 54:24,25 57:1 57:8,13 112:11 fault 156:16 fbga 30:11 31:4 fcra 1:25 feature 159:22 161:7 federal 230:1,8 230:9 feedback 97:24 97:25 98:8,10 151:13 feeding 140:1 182:22 feeds 169:17 feel 14:18 136:8 136:15 139:1 139:22 140:4 146:10 216:9	fell 218:15,17 felt 69:2 139:17 148:13 ferenc 2:13 5:13 ferenc.pazma... 2:14 field 21:4 fifo 62:7 87:18 87:19,20,25 88:20 94:2,13 94:15 96:7 101:14,22 102:6,11,12,14 102:18 103:4,6 103:17,25 104:12,15,22 105:5,11,11,13 105:21 150:17 150:21,24 166:16 217:16 218:22 219:22 219:25 220:1,4 220:20,22 221:3,12,13,18 221:25 222:18 223:10 fifos 105:11 figure 23:23 26:23,23 27:4 27:9,12,13,14 27:16 28:21 29:1,7 30:8,14 30:20,21 31:1 31:2,22,25	32:17 36:20,24 36:25 37:2 74:15,23,25 84:12,15,15,20 84:21,21 85:2 85:5,13 88:12 88:14,15,19,22 88:25 89:2 91:15,23 92:3 95:24 96:3 97:9,20,21 100:2,4,13,19 100:20 101:7,9 101:12,23 102:14 113:6,7 121:18,19,22 121:23 122:10 122:10 123:10 123:20 125:16 125:16,20,20 126:7,9,14,16 126:18,18,19 127:5,18,19,20 128:24,25 132:16,16,17 135:6,17 141:4 141:9,11,12 143:3,4,5,13 144:5 149:14 149:16 150:7 151:10 153:1,2 153:4 168:25 169:1 175:22 199:22 202:19 202:20,23	203:21,21 206:6 217:14 220:3 221:1,17 223:11 figures 31:11 35:19 131:24 132:25 202:19 figuring 118:10 filed 8:21,24 9:19 fill 46:24 final 196:24 217:7 224:24 finally 9:22 financially 228:15 find 19:7 64:12 64:25 65:4 71:23 72:4,15 119:22 164:13 184:6 195:19 202:10 211:6 211:10 217:6 finding 119:19 130:20,21 finds 169:25 214:21 fine 9:21 59:3 74:4 75:2 99:16 107:8 113:2 120:18 120:22 130:14 136:12,22 137:9,24 153:1 211:7,19 212:5
--	---	--	---

[fine - form]

212:8,13,15 213:12,24 firm 15:21 firms 15:16,18 15:20,25 16:4 16:11 17:2,9 17:18 first 10:13 17:20,22,25 21:21 24:4 29:11 35:19 56:4 65:10,11 84:19 85:14 86:1 87:4 92:14 101:19 102:1 103:3,5 103:10,11,13 103:16,21 104:24 105:11 105:12 109:2 119:15 150:11 150:14 157:16 162:13 163:3 163:10 164:15 164:22,23 165:2 166:7 172:10 174:17 177:4 178:13 179:10 182:20 200:11 203:22 206:24 211:8 211:14 214:2,3 219:18 fit 14:25	five 16:8,9,12 16:16,17,18,20 29:8 75:4 144:11 203:7 fix 6:12 100:10 164:12,12,13 fixed 115:2,4,5 124:7 142:23 fixing 164:11 flaw 190:20 fleshed 80:2 flight 75:8 flow 127:14,14 129:1 fluctuations 95:20 fly 75:18 79:16 79:18 145:6,8 145:14 146:13 146:13,16,19 157:21,23 158:1,7,8 159:7,17 161:16,21 162:3,14,19,22 162:23,23 163:4,5,11,16 163:20 164:2,3 164:6,8,14,24 165:2,20 166:11,21 167:20 170:10 170:16 171:2 171:12,12,17 171:24 172:9	172:22,25 173:1,5,7 175:25 176:11 176:17 177:15 178:15 200:5 209:15 211:18 focus 19:17 24:24 26:14 86:17 88:15 130:17,18 163:11,14 195:16 218:24 focused 13:23 19:18 125:13 focusing 80:1 follow 46:7,10 48:2,5 216:24 222:8 followed 96:6 following 47:4 follows 32:1 130:24 229:8 fontalvo 1:23 227:13 228:4 228:25 force 6:25 foregoing 226:2 228:7 forget 115:25 form 22:13 23:3,10 24:14 24:17 25:4 29:10,16 44:1 44:25 55:4 57:15 60:23	66:15 69:11 70:24 71:14 76:7 77:6 78:17,24 80:22 81:9,21 82:22 83:21 85:3,24 88:3,24 91:6 97:10,17 103:9 105:19 110:8 117:25 122:16 128:8 132:7 135:13,22 137:7 138:21 140:12 142:6 143:22 145:11 147:12 151:6 151:22 155:3 156:13 158:10 158:13 159:9 161:10 163:23 164:1 167:23 168:14 170:12 170:15 173:24 175:17 176:2 176:12 177:18 178:20 179:16 181:23 183:5 186:20 187:7 187:16 188:14 189:2,12 190:11,19 191:18,23 192:2,11 196:1 197:3 198:3 199:12 200:15
--	---	---	--

[form - goes]

207:2 208:11 208:18 209:7 213:1 214:8,15 215:5 217:24 218:6 219:6 223:24 224:7 formed 14:11 forth 20:11 22:5 forward 222:1 found 20:7,9 71:19 72:3,6 101:7 145:24 200:19 202:1 211:13 four 38:15,19 frame 31:25 32:9 48:20 49:1,4 50:19 55:14 francisco 2:7 frcp 230:1 free 123:17 124:9,10,11,12 freely 114:24 front 10:9 107:6 full 7:8 12:13 12:17 16:21 function 22:7 96:22 134:4 156:12 functionality 138:11 142:22 156:15,20	157:3 193:10 198:14,16 199:18 functions 78:2 206:13 fundamental 55:25 193:7 further 49:3 103:19 107:23 133:16 209:21 209:21 211:3 222:5 224:11 228:11 furthermore 61:19	generation 94:3,7 207:14 getting 12:12 23:12 51:8 173:4 186:4 207:6 giovannini 165:14,17,19 165:23 166:10 166:16,18,20 166:23 167:11 170:25 give 5:4 19:19 31:15 32:6 44:9 49:7 51:20,23 57:21 59:8 63:7 74:6 84:13 97:11 115:15 125:11 128:10 148:14 148:15,15 160:11 198:19 216:2,9 given 37:23 60:16 61:2 119:22 133:10 135:17 148:12 156:11,14 199:2,4 201:21 201:23 210:12 210:13 gives 28:17 34:5 44:8 98:15 125:12 128:4 193:19	193:20 giving 7:8 50:5 98:1 108:25 go 6:4,15,18 10:12 11:7 16:18 20:20 22:14 30:3 39:1,15 42:1 43:17 44:17 45:2 50:6 53:11 56:11 61:23 62:13,16 63:10 72:8 81:24 85:12 89:18 90:25 93:18 96:22 98:6 100:11 106:7 112:3,10 115:25 125:3 126:23 128:24 132:10 142:13 144:10 146:19 154:10 179:1 182:18 184:6 203:2,19 204:23 205:18 207:9 216:14 216:15 222:25 goal 179:14,18 goals 160:23 goes 68:18 86:9 86:12 87:10,17 87:19,20,22,22 90:6,21 92:15 93:6 102:14
	g 165:15 gate 78:4 gates 133:6 gee 17:8 66:10 general 153:11 153:12 156:7 generally 23:4 52:10 68:9 94:18,20 95:10 generate 94:16 123:4 133:9 generated 159:2 generates 94:9 193:1 generating 94:10 139:15 139:16,25		

[goes - helpful]

105:10,15 119:15,16 213:9 going 6:18 7:16 10:12 11:7 16:8 19:4,5 20:22 23:12 24:3,22 26:25 27:1,9 30:2 35:13 39:7,18 51:8,20 54:20 54:21,25 58:5 58:6 59:8 61:8 63:7 68:22 81:25 82:2,3,8 82:8,11 84:1 89:12 90:3 91:20,22 92:24 93:21 95:6,19 96:20,22 97:1 97:3,4,4 98:13 99:20 101:13 102:8,17 104:10,11 112:9,9,14 113:21 114:16 115:11,12 117:3 119:8 120:12,25 123:23,25 128:10 129:19 130:19,20,21 144:12 146:16 149:7 150:1,17 150:23 153:14	153:19 158:18 159:6 160:16 169:21 171:3 171:17 173:15 178:12 180:11 180:15 181:2 181:17 182:4 188:2 189:4 191:11 201:12 201:12 202:15 202:16 205:9 205:11,13,15 207:5,7,8 213:21 219:22 220:6 223:11 good 5:10 6:10 11:6 99:14,19 111:2 202:25 gosh 18:16 gotten 105:21 218:21 graduated 11:22 14:3 great 58:9 144:15 165:20 193:9 greater 111:15 158:2,8 159:17 163:17 ground 6:5,19 group 109:3 guarantee 31:15 112:8 guarantees 108:8	guess 28:8 38:3 40:9 45:4,5 69:2 77:19 96:14 119:25 123:2 124:18 125:21 134:1 140:13 163:14 188:11 205:22 210:18 guide 61:13 guided 46:8 guys 168:15 h h 65:24 66:2 231:3 halfs 166:7 hand 5:2 18:11 handle 158:1 handled 229:8 handles 157:22 handling 145:8 159:17 166:10 handy 211:11 hang 37:1,2 61:22 100:10 116:7,7 124:22 134:22 150:13 198:11 202:22 happen 71:17 103:17 165:24 166:3 happened 115:21 125:3 134:22 185:4 214:9,10	happening 72:7 happens 24:8 74:19 146:20 169:10 181:19 201:11 202:2 happy 57:9 58:24 hard 18:10 hardware 148:3,16,24 149:2,3,6 175:2 210:13 head 26:13 55:7 66:11 hear 85:23 heard 190:6 hearing 10:6 held 39:14 63:13 91:10 99:22 144:18 203:10 216:18 help 7:22 30:17 30:18 37:8,8 37:25 38:1 40:25 45:3 46:24 55:22 56:3 60:10,24 61:17 70:15 75:20 136:21 154:12 200:8 217:9 helpful 23:21 26:24 69:3,15 76:3
---	--	---	--

[helping - hope]

helping 70:11 146:13	64:15,21 67:23 68:16 70:9,16	169:2,6 170:9 170:19 171:1,6	52:22 53:24 58:19 59:22
helps 62:7 76:2 79:18 168:25	71:5 73:1,9,24 74:17,20 77:3	171:7,23 173:1 173:23 174:7	63:17 64:7,19 72:20 76:18
high 23:5 48:9 54:12,12,14 66:18 68:15 70:1,11 146:15 152:4 153:24 169:17 170:3,5	77:4,11,13,16 77:20,23,24 78:5,23 79:20 79:23,25 80:8 80:20 83:23 84:16 88:6,13 89:16,18,24 90:2,2,9,22 91:8 93:18 98:7,9,18 100:22,25	175:12 177:23 178:8 179:7 181:9 182:7,8 183:22 184:1,5 184:9,16,22 185:7,11,19,24 186:6,10,13,16 187:5,9,13,24 187:25 188:7 188:10,22 189:25 190:16	77:11 78:7,8 78:11,14 79:15 85:1 88:1,21 100:4 112:23 114:20 121:5 134:19 135:10 135:20 137:2 141:18 143:13 143:20 150:6 151:5,18,20 160:6,8,18 161:8 162:6 163:17,21 167:19 174:12 176:11 181:10 183:13,21 184:13 189:11 189:22 190:2,8 191:10 195:8 206:22 208:16 211:17 212:3
higher 49:13 54:18 56:17 142:9 178:25 200:4	101:11 103:23 112:23 113:3 118:12,13 119:25,25 134:16 136:1,4 136:7,14,15,19 137:6,9,13,16 137:17,19,20 138:3,5,9,11,12 138:18,19 139:9,13,22 140:5,6 141:4 141:8 142:1 143:5 149:15 151:3 152:3 157:9,21 158:2 158:6,24 161:23 162:2 167:13,16,22 168:11,18,22	191:3,14,22 192:9,10,21 195:12 196:14 196:18 197:4 198:16 199:1,3 199:15,19,25 200:1,6,22,25 201:5 204:11 208:10 209:5 209:12 210:1 210:14,24 211:3,25 212:6 212:15,19,19 212:21,23,24 213:2 217:14 221:1,18	161:8 162:6 163:17,21 167:19 174:12 176:11 181:10 183:13,21 184:13 189:11 189:22 190:2,8 191:10 195:8 206:22 208:16 211:17 212:3
highest 129:15			
highlighted 150:2			
highly 120:19			
hiraishi 4:18 38:15,17,18,20 38:22 40:9,11 40:13,16,18,23 41:6,9,24 42:5 42:13,14,21,25 43:8,11 44:7,9 44:12,13,15,22 45:1,10,10,14 45:14,19,25 46:6,16,20,22 47:4,10,12 48:1,4,5 58:3 58:10,17 59:21 60:7,14,19 61:10,11,19 62:19 63:19		hiraishi's 40:7 41:21 43:22 44:3,23 45:22 45:25 47:7,21	hire 14:21,22 15:16 hold 91:16 117:11 118:18 119:3,7,18 154:3,3 holds 105:23 honestly 17:18 hope 20:19 49:24 50:12

[hope - incorporating]

52:14 53:3,6 53:10,21 54:2 54:8 56:19 57:7,17 76:2 121:10 hopefully 11:8 host 23:9 25:3 25:6,9 hours 9:7,8 18:19,22,23,24 18:25 19:1 hughes 12:19 12:23 13:9 huh 18:20 52:23 63:18 76:19 78:10 82:17 113:5 125:6 129:3,18 129:21 156:9 157:19,24 179:8,13 214:5	196:21 ignore 180:13 180:14 illustrate 35:20 illustrated 28:25 74:14 illustrating 126:10 127:7 illustration 36:22 immediate 194:9 immediately 101:23 imperfections 118:22 implement 128:15 133:11 135:16,24,25 136:11 137:1 138:24,25 139:3,19 155:23 156:11 159:24 160:5 160:17 167:4 168:11,19,23 192:9 194:2 208:9 209:5 implementati... 28:25 159:21 160:1 172:3,10 178:13 179:10 182:13 198:2 200:12,12 204:19,20,23	204:24 207:1 211:16 implementati... 152:1 172:5 207:16 implemented 126:12 127:9 134:15 146:22 159:18 161:7 162:5 163:15 167:21 208:15 implementing 145:18 146:1 166:24 174:15 implements 200:13,14 implication 54:7 implied 136:14 imply 28:15 31:7 important 53:15 57:6 70:7 140:18,20 impossible 95:12,12 104:24 improve 199:19 improved 50:11 200:2 improvement 49:23 53:10 198:21 199:3 199:13	improvements 53:12,14 145:9 145:13 improving 145:13 178:23 inb 59:6 63:25 92:15,16 187:18 include 12:18 13:10 135:15 included 13:11 19:14 69:16 229:14 230:3 includes 29:8 64:15 65:9 89:16 142:1,1 188:12,15 including 69:5 69:17 154:22 158:8 159:17 163:16 incoming 87:5 117:23 181:11 211:20,21 222:3 incompatible 44:11 47:10 48:1 incorporate 149:16,17 152:2 198:22 incorporated 14:15 27:20 incorporating 90:18 199:4
i			
idea 65:8 118:10 212:12 ideal 107:25 108:4 133:14 133:18,20,22 ideas 138:22,24 identical 213:7 224:1 identified 39:6 85:5 198:6 identify 20:6 38:25 84:25 192:20 193:11			

[increase - interject]

increase 114:1 114:5 173:15 increased 53:16 increasing 114:10 increment 129:9 incrementing 129:4 independently 207:7 indicate 12:9 28:14 96:5 indicated 69:10 indicates 14:7 indicating 96:4 98:11 indiscriminat... 82:1 individual 13:7 30:9 32:17 62:24 63:2 133:6 171:13 178:4 180:22 individually 9:16 inefficient 160:24 inferior 51:13 51:15 inform 61:25 62:8 information 20:17 44:8,13	46:24 50:6 77:21 79:21 80:2,18 81:7 81:14 97:1,24 98:1,4,5,22,23 98:24 99:4,5 99:12 105:24 107:19 108:23 109:12 133:16 139:15 169:18 175:8 182:23 182:24 183:1 184:19,20 186:10,11,14 186:17 188:24 189:7 196:12 196:16 197:14 197:15 206:11 206:12 210:7 informed 55:18 inherent 75:18 initial 220:13 220:21 initially 169:22 initiate 81:1,19 82:3,9,10 initiated 23:9 25:2,5,6 76:9 76:15 78:11,25 82:15,20 83:5 83:9,14,15 168:3 205:10 207:25 initiates 79:4,7 79:10,11	initiating 83:20 initiation 83:24 inline 141:16 input 58:19 59:6,14,23 60:20 62:2 63:21,24 64:9 82:6 87:5,24 88:19 94:10 96:6,10 97:15 123:12 124:3 179:24 193:6 195:15 221:2,9 222:2 223:4,7 223:9 inputs 86:14,15 87:9,14 inserted 143:8 150:6 172:8 inside 79:6,24 80:4 81:19 88:11,14 95:23 101:2 104:3,9 113:13 130:9 131:13 133:24 133:24 134:4 151:19 153:14 161:23 162:20 167:14 institution 9:25 instruct 7:25 80:18 96:21 instructing 97:25 114:1,8	instruction 13:24 82:3,24 83:23 114:11 205:17 instructions 14:2 96:25 128:20 instructor 13:20 instructs 97:6 integrated 15:5 117:9 intend 20:13 intended 57:1,4 77:22 166:5 intent 95:7 intention 38:5 94:23 95:7 interact 21:11 21:16,22 22:2 interaction 168:4 interchange 224:10 interested 14:23 86:19 93:5 106:13 146:17,18 228:16 interface 118:2 126:15 interfaced 13:13 15:10 interject 6:7
---	---	--	--

[intermediary - know]

intermediary 7:21 intermittent 16:23 interpret 7:21 128:9 214:19 215:11 interpretation 121:13 216:7 interpretations 214:23 215:12 215:17 interpreted 219:15 interval 24:6 introduce 10:13 11:7 25:14 39:7,18 42:2 introduced 58:4 66:4 67:6 106:8 112:18 115:18 116:5 introducing 42:5 144:23 invalid 119:16 invention 21:5 28:25 33:5,9 35:8,21,25 37:11,20,23 38:6 77:25 126:11 127:9 138:25 139:3 145:18 146:2	inventive 33:6 involved 15:13 63:20 94:3,6 95:6,14 ipr 5:22 8:18 8:20 9:19 11:5 15:24 17:21 18:3 106:23 116:5 ipr2022-00711 1:10 5:17 ipr2022-0711 5:21 irell 3:4 5:8 irell.com 3:6 issue 53:15 57:23 205:8 issues 74:21 itc 16:19 item 87:17,23 iterative 125:8 126:25 iteratively 125:5 135:1	32:19 33:6,10 33:13,14,17,22 34:8,10,13,16 35:1 36:4,9,11 36:16 39:23 40:3,8,13,16,17 41:3,6,9,10,15 41:22 43:18,19 43:24 44:4,10 44:16,21 45:3 45:17,17 46:7 46:10,20,23 47:5,11,16 49:18 61:12,14 61:16 62:5,10 62:11,21,25 106:9 118:20 120:7,7,12,20 142:15,23 147:4,7 jesd79-3c 4:16 jlindsay 3:6 job 15:23 72:12 178:16,21 179:15 229:5 231:2 jobs 81:16 jonathan 3:5 5:7 216:21 judge 7:1 july 21:5 jump 112:17 jumps 40:15 jury 7:1	k k 65:24,24 66:2 93:13 keep 23:12 51:6 57:16 keeps 198:11 keyword 89:9 89:10 khatri's 9:14 kimberly 1:23 227:13 228:4 228:25 kind 41:1 48:3 50:3 67:2,19 68:4 97:6 118:7 141:20 149:4 218:8,9 kinds 206:10 know 5:22 6:3 6:3,11,19,19,23 8:11 10:18 11:12,19 18:17 19:2 22:4 23:4 25:19 32:7,22 32:23,24 33:11 38:6 39:19 40:14 42:1 46:4 47:10 48:17,23,24,25 49:2 52:3,17 53:1 54:11 55:1 56:6 58:23 60:25 62:5,23,24 63:1 64:4,23
	j j 26:11 january 1:17 227:5,7 228:17 229:3,5 jedec 4:16 26:10,15 27:18 27:19,20,22 28:12,14,18,19 31:13,16,17,20 32:2,11,15,18		

[know - leveling]

66:10,25,25 67:17 68:1,2 68:12 69:24 72:19 74:15,24 77:25 79:21 80:25 81:22 82:6 83:25 84:3 85:7 95:11,17 96:13 98:16,22 99:1 105:1,4,20,22 105:23 107:24 111:23,23 112:5 117:2 118:22,23 120:11 121:11 121:18 129:14 130:23,24 131:18 134:7 139:7 140:14 143:25 144:6 148:9 152:21 156:16 162:16 163:24 164:3,4 164:8,12 166:12 167:5 167:24 169:20 174:8 177:1,12 180:13 181:6 182:19,19 195:19 198:10 198:14,20 200:3 202:17 203:2 205:5,17 207:24 208:6	209:11 214:18 215:14 216:5,6 218:20 219:21 219:21,25 220:2 221:6,8 222:3 223:8 knowing 207:4 knowledge 51:2 60:18 65:13 78:5 79:22 198:18 knowledgeable 21:9 81:23 known 41:3 119:11 221:13 knows 55:25 61:3 68:21 104:1 114:25 132:19 220:16 I I 93:13,13 I0 87:23 I1 86:2,8,25 I2 86:4,11,12 87:2 label 32:16 43:2 labeled 86:12 96:10 107:2,14 107:19 141:6,7 153:13,18 labeling 32:20 labels 32:25 lapse 75:9	laptop 63:6 large 111:5 166:11,21 172:15 211:18 larger 111:5 143:24 144:1 latch 54:16 211:21 latched 55:2,18 56:8 103:18 latching 54:10 54:23 55:10,24 56:5,17 57:14 96:7 103:6 117:23 223:1,3 223:6,8 latency 75:10 75:14 law 6:25 15:16 15:17,20,21,25 16:4,10 17:1,9 17:17 215:14 lclkr 93:24 94:15 104:17 104:25,25 105:13,22 217:18 219:24 221:2,6,17 223:16 lclkw 93:12,13 93:15,21 leap 31:22 193:9 learn 61:7	learning 146:18 leave 113:21 leaving 158:14 left 85:15 92:18 92:21,24,25 108:14 112:4 121:12 legal 229:7 length 154:5,20 lengths 111:8 lengthy 157:9 level 13:2,3,4 23:5 44:8 54:12,12,14 63:9 117:8 119:1 130:11 141:21 152:4 153:24 167:25 leveling 58:11 58:15,17 59:4 59:7,21 60:6 60:21 62:9,12 62:16,20,21 63:1,3,17,20 64:8,14,20 65:2,7,9,17 66:9,13,14,17 66:21,23 67:1 67:10,20,25 68:3,5,7,10 69:5,8,16,21 70:5,7,13,18,23 71:6,7,10,12,17 71:20,22 72:2
---	---	--	---

[leveling - line]

72:5,7,10,16,20	170:7 175:9,9	35:12 38:8	176:7,14
72:25 73:9,14	175:13,18,20	39:7,17 42:5,8	177:20 179:4
73:16,21,25	181:22,24	42:19 43:15,21	179:21 182:11
74:7,10,13	182:2 184:17	44:14 45:7	183:9 187:1,10
76:4,5,8,8 78:9	186:17 187:5	55:8 58:2 61:5	187:21 188:17
78:9,11,14,15	187:13,15	63:10,15 66:3	189:9,18
78:20,22,22	188:8,13,16	66:8 67:5,9	190:14 191:1
79:4,5,6,7,10	194:20 200:13	68:6 69:13	191:19 192:6
79:11,11,16	201:7 204:25	71:4,18 76:17	192:16 196:7
80:4,21 81:1,2	205:1 208:9,16	77:7,9 78:21	197:6 198:5
81:19 82:1,1	light 192:9	79:12 81:5,12	199:21 200:17
82:10,11,15,20	limit 130:20,21	82:13 83:7	202:5 203:2,13
83:2,8,12,13,19	131:6 133:17	84:6 85:10	207:13 208:14
83:25 84:3,3	148:18,21,25	86:16 88:7	209:1,18 213:5
89:14,15,17,17	limitation 41:8	89:3 91:21	214:12 215:1
89:19,19,22,22	213:15	97:14,22 99:14	216:12 218:6
89:23,24,25,25	limitations	99:18 100:1	221:4,21 222:7
90:10,10,12,12	26:6	103:12 106:5	224:3,11,24
90:15,15,17,17	limited 46:6,17	106:14 110:21	225:3
90:23,23 91:2	46:18 47:3	118:9 122:17	line 21:21
91:18,18 93:6	101:6 133:13	126:5,6 128:12	35:19 50:24
93:9,19 97:5,5	145:12,15,22	132:21 135:18	101:13 104:14
112:23 113:4	146:6,8,10	136:23 138:1	105:6 111:8
135:5,10,14	148:13	139:4 140:15	113:20,25
137:2 138:13	limits 159:12	143:1 144:3,12	144:8 149:18
139:11 146:23	lindsay 3:5 4:3	144:15,22	150:16,23
146:25,25	4:4 5:7,7,15	145:16 147:15	153:13,18
147:2,3,11,19	6:14,17 10:12	151:16 152:24	175:22 205:22
147:22,25,25	10:15,17,22	155:10 156:6	205:23 206:9
148:2,6,10,11	11:6,10 22:17	157:6 158:11	217:16 221:1
148:12,16,20	23:7,16 24:15	158:21 159:14	221:17 223:15
148:22,24	24:23 25:8,14	161:12 164:16	223:16 229:15
149:5 167:19	25:18 26:11	165:3,6 168:6	230:4 231:4,7
168:7,8,12,19	29:13 30:1	168:20 170:22	231:10,13,16
168:23 169:7	33:23 34:18	174:1,6 175:24	231:19

[lined - make]

lined 176:6 lines 92:1,2,4,6 96:2 153:22 155:2,20 157:25 174:14 174:18,19,21 209:10 217:12 217:15 218:5 lining 176:8 list 11:24 literally 29:11 147:8 little 17:17 49:20 51:6 63:5 79:23 97:12 122:20 126:19 162:10 168:16 189:16 190:20 217:8 219:23 222:12 llp 2:6,12 3:4 load 28:10 155:15 163:7 loaded 153:25 155:17 loading 154:19 local 179:25 223:17 location 65:1 lock 123:3 180:16 locked 229:12 230:1 logic 113:13 125:7 126:15	127:1,7,10,12 135:9 136:10 151:8,25 152:6 152:12 156:11 173:19,19 174:22,24 178:6 193:7,8 193:22,22 logical 172:13 172:18 193:23 long 9:4 17:13 148:7 203:7 longer 10:15 look 11:19 23:18 26:21 27:3,14 30:21 33:1 35:17 38:9 39:1 40:9 41:11,24 43:7 46:12,23 48:12 52:17 53:17 54:3 56:12 57:5,9 58:3 62:20 65:25 70:6 71:21 73:20 74:15 84:9 89:18 90:16 113:6,18 116:15 121:12 121:12,17 122:9,18 124:19 125:20 127:22,22 132:10 134:11 141:3 149:7	152:25 154:10 157:10 163:4 166:14 169:4 177:4 190:23 191:9,10 202:18 205:19 211:14 213:17 looked 57:25 68:2 70:19 71:8 118:19 171:19,21 200:7 214:20 looking 21:18 21:20 23:14 29:7 31:2 32:16 42:22,23 42:24 74:8 96:3 97:20 100:2 101:12 107:5 108:19 116:2 127:18 130:1 132:23 141:7 213:22 218:7 223:14 loop 123:3 los 3:5 lot 14:25 51:6 60:9 100:25 101:10 152:6 158:14 160:24 160:25 168:25 173:19 194:8 195:18 lots 50:13	low 63:9 169:17,19 170:4 lower 43:2 106:20 219:20 lowest 129:16 129:17 lqr 105:4,7 lunch 99:15
			m
			m 65:24,24 66:2 machine 113:17 131:1 made 9:23 10:5 47:8 64:7 69:18 111:6 127:11 198:17 magic 166:25 main 153:7,9 175:19 178:3 major 152:18 make 10:10 31:22 34:12 35:5 38:4 41:2 45:18 46:13,22 47:1 48:5 57:18 58:22 61:13 68:23 86:23 108:1,5 112:14 117:17 120:22 122:8 133:6,11 136:22 139:6 142:8,12,13

[make - measuring]

149:15 151:11 152:13 160:7 161:16 172:24 177:6 178:10 180:5,15,17 181:2,18 199:3 199:14 201:4 211:19 212:5,8 215:15 218:7 224:17 229:14 230:3 makes 44:3 102:9 120:16 121:9 122:12 124:5 136:5 138:7 167:13 167:14 175:4 201:21 212:16 making 176:5 177:8 185:6,7 193:9 manella 3:4 5:8 manner 69:1 134:20 135:3 161:25 manufacturer's 110:19 manufacturers 108:5 112:8 manufacturing 118:23 margins 110:19 117:11 118:18 119:3,10,21	marked 10:14 10:21 11:9 25:16 39:9 42:7 66:5 67:8 86:8,12 92:18 93:3 144:21 markings 10:10 master 121:24 122:5 123:4 124:7 master's 12:5 12:12 material 20:17 matter 172:14 175:2 184:21 192:15 195:14 215:15 matters 207:22 max 107:20,23 109:9,24 112:4 121:3 maximum 13:25 108:12 135:6 mc 113:17 mean 15:5 16:14,17 18:24 19:2 20:19 21:16 22:1,3 25:5 28:16 29:14 31:8 32:1,15,16,18 34:19 37:12 38:3,13,16,24 38:25 41:5	42:12 43:17 44:7 45:4 46:8 48:11,12,23 49:2 50:4,5,10 50:13,15 51:16 58:24 59:13,25 60:2,25 68:11 68:12 72:12,19 72:24 73:4,20 74:5 77:24 79:1,17 82:24 85:4 89:9 93:13 94:6,18 95:11,22 96:24 97:18,23 98:22 99:3,8 101:9 102:2,18 105:9 105:10 106:4 114:7,15,23 115:4 122:8 123:17,24 125:12,15 132:8 134:6 135:8,23 139:17 140:8 140:14 141:22 142:11 151:7 151:25 153:23 154:3,10,16 155:11 158:15 158:18 172:10 173:8 177:1 180:24 181:13 184:16 188:15 188:19 190:4	192:24 193:14 195:5,12 196:11 205:11 207:22 208:21 209:15 213:7 214:10,17 222:13,13 223:25 224:4 meaning 55:14 65:12 124:12 214:14 220:9 meanings 54:14 means 30:11 34:11 35:7 45:4 54:6 57:19 59:15,17 65:4 68:17 69:10 90:1,12 110:7,9 122:3 142:8 170:6 178:22 214:7,9 214:25 215:4,8 215:9,23 216:3 222:13,14,17 222:24 223:6,9 meant 53:21 81:4 190:23 220:12,23 measure 152:9 measured 183:24 188:4 measures 184:7 measuring 108:10 164:6
--	---	--	---

[measuring - memory]

164:24 165:2	mellon 14:5	80:13 81:7,14	160:17,18
175:6 183:13	memories	82:15 83:8,10	161:5,8,17,20
183:21,23	21:10 49:25	83:13 86:3,5	161:23,24
184:8,9,13,15	67:21	87:23 93:22,23	162:6,6,11,14
184:16,17,20	memory 13:10	94:4,4,8,11,19	162:15,20
184:23,25	13:11,12,13	94:22 96:6	163:5,17,21
185:4,15,20,25	15:8,11,12,14	97:16 105:8,16	164:1,11
186:17 187:4	16:19 21:12,16	106:9 107:13	166:17,20,25
187:12 188:11	22:2 25:11	107:16,22	167:6,6,20,21
188:23 195:3,9	28:10 29:1,1,2	109:9,22	168:3,4,12
195:23 196:9	29:3,6,7 30:5	110:13 111:13	169:12,18,21
mechanism	30:23 31:16,19	111:18,20,25	169:22 170:10
102:23 123:10	32:4,5 33:4,6	113:13,13,25	170:21 171:3,4
123:13 124:4	33:17 35:20	114:3,7,11	171:6,10,13,16
125:14 130:14	38:14,15,19,22	118:5 119:12	171:17,25
130:22,23	43:20 45:13,14	125:5,11,21,22	172:1,7,18,23
136:22 137:9	45:15,20 46:1	126:10,15,25	173:8,10,12,15
137:14,23	46:17 47:7,23	130:7,8,16,25	173:22 174:4
139:23,24,25	48:8,10,16	132:12 133:12	174:15,23,24
140:1 145:7	49:13 50:11,11	135:2 140:10	175:13,14
184:8,9,10,25	50:17 51:14	140:16,22	176:16,18
185:10 186:13	52:1,11,13,22	141:1,13,16,17	177:16,17
187:12 195:14	53:1,2,15,24	141:18 142:2,3	178:1,2,3,4,5,6
219:19	54:1 55:3	142:20 143:8	178:8,14,16
mechanisms	56:25 57:1	143:10,14,16	179:14,23
62:14,15	58:12,18 59:22	143:20 145:3	180:8,12,21
136:11 140:7	60:11 65:5,25	145:10,12,14	181:7,10,20
147:18 148:2,5	67:21 72:22	145:18,21,22	182:8 184:1,5
148:8,14	73:10,18,23	145:23 146:2,5	188:5 194:5
199:14	74:14 75:10,11	146:7,8,11,20	201:6,7,18
meet 9:1,4	75:12,16 76:4	147:23 153:4	202:1,2,13
megabits 30:6	76:6,9,16 78:6	153:15,20	203:16 204:4,8
30:12	78:12 79:3,3,8	155:21 157:22	204:12 205:2,4
megahertz	79:10,14,19,19	159:8,11,12,18	205:5,8,12,15
48:11	79:24 80:1,4	159:24 160:5,6	206:17,24

[memory - mounted]

207:4 208:16 209:10,11 215:19,24 216:1 mention 166:16 177:25 179:22 mentioned 67:5 91:1 189:13 mere 90:11 microphone 6:8 microprocessor 13:6,8 microprocess... 13:2,5 mid 16:25 17:4 middle 64:17 104:8 119:13 119:20,23 120:16,17,19 125:24 130:21 180:19 182:1 mill 2:12 min 107:19,23 109:9 121:2 mind 27:1 39:5 44:3 51:7 69:19 89:7 107:5 137:21 194:17,22 201:21 212:11 213:21 215:3 218:3 223:3 mine 36:19	minimum 108:11 135:6 minuscule 44:6 minute 84:13 minutes 144:11 203:7,8 216:16 misalignment 169:20 misleading 7:5 mistakes 20:8 misunderstood 219:17 mode 80:17,17 80:24 modification 149:15 184:19 209:24 211:6 modifications 152:22 189:14 197:22,25 198:7 199:8 209:21,22 modified 212:4 modify 115:12 132:11 152:7 158:6 211:3 212:23,24 213:2 modifying 158:23 174:12 188:22 213:3 module 15:14 25:11 26:10 27:18 28:10,14 29:2 31:13,14	31:17 33:4,6 33:17 35:2 36:4 38:14,22 45:20 46:1 47:8,23 52:22 53:2,24 54:1 54:17,18 56:17 56:18 57:12,14 75:7 77:11 78:7 80:1,12 80:13 81:22 82:7 83:24,25 96:18 97:8,19 98:1,25 99:2 99:11 140:16 141:13,16,17 151:13 167:6 169:13,23 172:23 174:15 174:25 182:13 182:15,23,24 183:2 185:16 186:12,22 188:25 189:8 189:16,20,24 190:1,23 191:6 191:11,16,25 192:14,17,24 193:8,12,17,21 194:2,19 196:25 197:9 197:12,14,20 206:25 210:7,9 modules 13:10 13:13 15:8,11	15:12 16:19 35:20 46:17 48:10,16 49:13 50:18 77:22 140:10,22 141:1 178:5 moment 20:21 41:18 42:11,17 63:8 67:13,15 77:4 82:14 97:11 113:7 141:4 163:11 176:15 195:7 210:19 monday 224:16 224:25 morning 5:10 motherboard 143:11,14,17 143:19 motherboards 143:23,25 motivated 160:13 183:12 211:2 motivation 120:17 163:11 173:21 179:3,5 179:20 motivations 160:13 179:6 199:5 200:1 210:23 mounted 141:18 143:7
--	--	--	--

[move - numeric]

move 33:23 115:17 moving 183:10 multiple 14:1 214:20,22 multiplex 184:21 multiplexer 87:13 multiplier 87:12,12 mux 87:11,13	224:18 229:14 230:3 need 8:10 22:14 23:11 33:18,18 34:12 41:2 46:25 47:17 50:7 52:17 54:17,22,24 61:3 62:6,8 63:23 64:24 65:12 67:3,19 67:24 68:21 69:25,25 74:3 82:3 91:13 93:18 94:19 114:22 115:14 120:18 124:25 125:17 130:13 135:24,25 137:12,22 138:6 139:2,23 139:23,25 140:1,2,5 148:16 151:7 151:11,12,15 151:19,23 152:4,5,7,9,10 152:13,14,16 152:20 153:25 155:8,15,16 157:2 163:3 172:11 174:13 174:17 180:12 180:15 183:1 192:8 196:19	198:20 202:17 202:25 210:2,5 210:8 211:8 212:13 needed 13:12 15:11 68:5 89:20,21 98:24 136:3,11 149:5 192:12 200:14 209:21 needs 33:22 60:9 61:1,7,18 62:20 66:18,19 73:22 75:22 79:2 91:13 98:6 100:25 101:3,5,10 122:14 189:3 197:13 198:13 neither 69:8 83:19 200:11 200:19 netlist 1:7 5:9 216:25 218:4 219:2 229:4 231:1 never 70:22 96:15 102:17 104:10,11 121:7 156:18 157:1 new 51:25 53:9 53:13 129:6 139:15,16	nine 29:2 174:8 174:9,10,13 noise 165:4 nomenclature 31:9 non 15:21 32:21 33:24 nonresponsive 37:13 normal 220:9 normally 156:18,19 notary 227:14 notating 229:15 230:4 notes 10:10 216:15 228:10 noticed 63:5,8 112:3 206:9 notification 84:2 number 1:11 5:18 6:1 9:15 12:21 28:22 56:24 78:18 106:13 109:23 116:10 128:22 149:8,9 203:21 229:15 230:4 numbers 9:17 107:3 108:8 numeral 157:14 numeric 115:8
n			
n 4:1 165:15,15 165:15 name 12:20 128:4 210:4 narrow 195:25 naturally 45:2 ncra 1:25 near 220:3 necessarily 32:1,17 34:6 34:16 57:19 140:7 212:23 necessary 8:1 34:2 44:8 60:16 69:2 70:1,14 71:9 72:2 81:1 91:11 120:22 137:12 139:10 139:18 176:13 181:7 182:17 192:4 194:24			

[numerical - okay]

numerical 206:10	156:13 158:10 158:13 159:9	obviously 6:19 8:10 140:22 142:19 177:10 213:19	10:8,12,23,25 11:6,11,14 17:14,19 19:20 20:3,21,23 21:1 22:8,20 22:23 23:20 24:1,24 25:1 25:17,21 26:2 26:3,20 27:5,9 27:11,16,17,24 28:3,5,21 30:2 30:4,22 31:10 32:11 33:3 34:22,24 35:15 35:18 36:2 37:4 38:11,12 39:21,22 41:13 42:4,14 44:19 45:22 47:6,12 48:9 50:23,25 51:1 52:10,21 54:9,16 56:15 58:9 59:4 60:6 61:10 66:3,6,7 74:5,11,13,15 74:17,18 75:3 76:18 77:3,8 78:8 79:13 83:4,8,17,19 84:11,15,19 85:12,18,23,25 86:19,22 87:15 87:16,24 88:18 89:4,13 91:1 91:22,25 93:8
o	161:10 163:23 167:23 168:14 170:12,15 173:24 174:3 175:17 176:2 176:12 177:18 178:20 179:16 181:23 183:5 186:20 187:7 187:16 188:14 189:2,12 190:11,19 191:18 192:2 192:11 196:1 197:3 198:3 199:12 200:15 201:15 207:2 208:11,18 209:7 213:1 214:8,15 215:5 218:6 221:4,21 223:24 224:7	obviousness 196:21 occur 88:11 89:22 90:24 118:21 146:14 166:1 occurring 129:25 occurs 164:7 184:4 offer 20:13 office 1:1 229:11 offset 123:8,8 123:11,12,22 123:23 124:1 124:21 128:7 128:14 129:2,4 129:6,24 131:21 135:12 offsets 121:1,3 135:2,7 139:25 oh 17:8 18:16 18:20 31:5 66:10 83:4 100:9 108:21 170:14 186:4 221:5 okay 5:25 6:5 6:14,16 7:19 8:10,12 9:9	
o 165:15 oath 4:5 6:21 6:24 7:17 227:1 object 22:13 23:3 55:4 201:13 objected 217:24 218:1 219:6 objection 23:10 24:14,17 25:4 29:10,16 35:3 37:17 44:1,25 57:15 60:23 66:15 69:11 70:24 71:14 76:7 77:6 78:17,24 80:22 81:9,21 82:22 83:21 85:3,24 88:3,24 91:6 97:10,17 103:9 105:19 110:8 117:25 122:16 128:8 132:7 135:13,22 137:7 138:21 140:12 142:6 143:22 145:11 147:12 151:6 151:22 155:3	156:13 158:10 158:13 159:9 161:10 163:23 167:23 168:14 170:12,15 173:24 174:3 175:17 176:2 176:12 177:18 178:20 179:16 181:23 183:5 186:20 187:7 187:16 188:14 189:2,12 190:11,19 191:18 192:2 192:11 196:1 197:3 198:3 199:12 200:15 201:15 207:2 208:11,18 209:7 213:1 214:8,15 215:5 218:6 221:4,21 223:24 224:7 obvious 103:1 104:5 106:3,4 134:19 136:22 140:8 160:10 185:8,12 194:22 195:19 196:3,4,18 197:17,23 198:8 199:2,9 200:20 209:23 210:12 211:24		

[okay - opinion]

93:24 94:25	163:13,19	opened 39:21	operational
95:8 98:13	165:11 167:2	operable 49:13	57:1 77:15,18
100:5,10,21	167:16,18	77:5,12 151:21	110:25 111:10
103:15 106:6	168:17,24	155:14 198:2	155:7
106:10,16,17	169:5 170:24	operate 47:19	operations
106:22 107:1,4	174:11 182:12	77:24 92:17	41:16,21,22
107:8,14 109:2	183:8,19 185:6	108:10,11	43:19,22,24
109:14 112:3	185:14 186:4	114:17,25	44:4 52:12
112:17,20	187:3,12,13	140:3 157:4,5	53:1,25 64:20
113:8,18,21,23	188:1,18	173:13 200:4	67:19,24 68:5
113:24 115:17	189:10,19	205:12	83:20 161:4
115:23 116:1	191:2,6,7,21	operates 108:1	184:14,23
116:14,15,17	195:21 196:20	108:4 117:18	185:2 195:4,11
116:18 117:1,3	196:23 200:11	operating	195:13,15,24
117:5,14,21	201:17 202:22	110:10,19	201:7 208:9
119:24 120:25	203:2,14	operation	214:4,7,9,10,14
121:17,21,23	205:21,23	15:12 21:10	214:16 215:4
122:14,19,23	210:17,19,20	22:12 23:2,8	215:19,24
124:5,14,22,23	211:13 213:14	24:7,13,19,20	216:1
125:3,4 126:5	213:16,21,25	24:25 25:2,11	opine 215:25
126:17 127:2	217:2 218:25	44:7 54:22	opined 160:19
127:21,24	219:5,7 224:11	68:15 70:2,12	opinion 21:2
128:3,23 131:8	old 29:21	70:15 73:17	26:9 39:2
134:13,24	once 14:3 39:20	78:1 95:14	46:16 47:21
138:14 139:5	150:21,21	96:20 98:2	53:5 56:21
140:9 141:3,5	180:4	99:7 117:22	57:21 64:14
141:8,12 143:2	ones 8:23 19:14	127:1 131:10	101:19 102:4
143:4 144:9,23	19:18,23 20:2	138:13 139:11	113:1 133:20
145:1 149:7,11	38:24 89:6	163:3 164:6,8	134:2,3,18
149:12,18	92:12 93:3	164:14,18,22	176:24 197:23
150:16 152:25	oops 61:21	166:6 184:4,11	199:7,10,11,13
153:3 155:25	open 10:23	185:4 195:9	199:16 209:22
156:2 157:12	11:14 25:20	207:12 213:11	216:2,8,9
157:15 162:13	39:20	214:11,23,25	221:2,17
162:24 163:10			

opinions 7:8 20:10,14,18 55:17 139:16 opportunity 72:8 224:17 opposed 15:21 optimal 65:1,4 115:13 131:21 optimally 181:18 optimization 134:4 213:8 optimize 62:2,6 141:1 optimized 104:9 optimizes 73:1 optimum 127:25 128:5,6 128:7,14 135:7 135:12 option 208:1 orange 96:2 101:13 order 13:24 22:6 33:15,21 34:12,13 40:2 40:10,15 41:2 41:2 44:9 45:3 46:23 51:9,10 52:4,18 58:1 60:10 61:17 63:2,21 64:23 66:23 68:15,24 70:1,14 75:20	75:21,22,24 76:12 77:15 80:4,18 81:1 82:9,9 89:21 90:23 93:12,15 96:17,19 103:18 104:2,3 105:14 114:23 120:4,18,22 128:15 132:13 136:11,21 137:22 138:24 139:3,18 142:16 149:1 149:16 151:20 154:17 155:17 175:7,18,22 177:2 178:25 184:11 187:18 189:4 192:5,9 193:9 196:13 210:6,9 222:22 224:21 ordinary 21:3 34:3 37:9,22 45:24 55:25 60:15,18,25 61:1,3,6 62:1,5 62:23,24 64:4 64:23 65:14 66:22 67:2 68:8,12,20 69:23 78:6 79:22,25 80:6 82:25 90:13	104:1 106:2 118:12 131:3 132:1,18 133:9 136:2 138:8 140:6 155:24 156:3 181:5 185:3 198:18 198:19,22 199:19 224:8 origin 97:19 original 31:10 189:11 204:6 229:10,21 originally 14:14 originate 92:4 92:5 97:7 output 87:21 87:25 88:20 92:19 93:1 94:17 95:2 109:16 110:13 111:3,13 118:21 120:8 150:15 169:8 193:7 220:7 221:10,14,18 221:23 222:1,2 222:16,19,25 outputs 74:20 75:3,4,10 86:15 169:9 205:25 outside 35:3 37:17 199:10	overall 141:21 141:24 overstatement 16:15 own 27:3 59:1 59:3,9 82:2,12 114:18 137:13 137:16,18 171:1 205:13 207:8 owner 1:8 3:3 5:8 <tr> <td colspan="4">p</td></tr> <tr> <td colspan="4"> p.m. 1:18 63:13 99:17,22,22 144:18,18 203:10,10 216:18,18 225:4 pack 142:19 page 2:12 4:2 4:10 21:21,23 27:15 28:7,24 28:24 42:3 43:17 64:13 107:2,3 108:13 108:18 138:16 149:8,9 157:10 157:13 165:9 169:2 183:16 183:18 187:23 210:15,17,18 211:13 213:23 220:24 223:12 223:14 229:15 </td></tr>	p				p.m. 1:18 63:13 99:17,22,22 144:18,18 203:10,10 216:18,18 225:4 pack 142:19 page 2:12 4:2 4:10 21:21,23 27:15 28:7,24 28:24 42:3 43:17 64:13 107:2,3 108:13 108:18 138:16 149:8,9 157:10 157:13 165:9 169:2 183:16 183:18 187:23 210:15,17,18 211:13 213:23 220:24 223:12 223:14 229:15			
p											
p.m. 1:18 63:13 99:17,22,22 144:18,18 203:10,10 216:18,18 225:4 pack 142:19 page 2:12 4:2 4:10 21:21,23 27:15 28:7,24 28:24 42:3 43:17 64:13 107:2,3 108:13 108:18 138:16 149:8,9 157:10 157:13 165:9 169:2 183:16 183:18 187:23 210:15,17,18 211:13 213:23 220:24 223:12 223:14 229:15											

230:4 231:4,7 231:10,13,16 231:19 pages 229:14 229:17,17 230:3,6,6 palo 2:13 paper 9:13,14 9:15 10:8 20:22 42:25 58:6,8 107:6 paragraph 20:21 21:2,19 21:20 23:22,24 26:22 27:1,10 27:11,13 28:4 28:6 30:2,16 31:11 35:17 38:9 39:3 41:12,20,24 64:13 74:17 84:9,11 89:16 91:24 98:9 100:4 116:15 116:17 117:5,6 122:18,21 123:2 124:20 126:9,13 127:4 127:23 134:11 134:14 149:8 165:9 166:15 177:25 178:12 179:22 183:10 183:11 187:22 210:17,18	211:15 213:18 215:7 220:25 paragraphs 43:7 parallelism 13:23 parameter 108:2 112:5 124:2,2 parameters 107:10,12 108:9 110:25 117:18 parenthetical 41:16 part 12:2,13,15 15:3,7,9 21:8 28:6 55:22 56:11 57:6,11 60:5 62:1,9 64:19 65:3 66:24 67:3 68:25 72:12,20 75:18 76:12 79:5 86:2 113:4 120:19 124:6,11,24 127:11 165:25 166:7,8 172:8 181:24 182:2 183:17 189:3 192:4,5,7,8 partially 60:5 149:17 167:24	particular 33:2 38:2 89:15 102:10 108:2 149:4 155:17 172:20 182:9 195:25 210:13 parties 228:13 228:14 parts 66:16 166:7 pass 59:17 132:13 150:20 220:6 221:13 222:5,19 passed 22:4 99:9 103:24 105:6 132:13 132:17 133:16 221:12 passes 105:7,9 105:12 passing 81:6,14 87:10 99:12 162:8 222:16 past 219:16 patent 1:1,2,8 1:11 3:3 5:8,17 5:25 6:1 8:21 16:13 21:4 22:9,10,22,24 23:13 24:9,11 25:25 34:4,6 37:8,9 38:1,2 41:6 43:1,1 58:25 65:20	68:19 70:9 74:2,6 77:13 77:16,17,17 80:14 101:20 168:24 202:10 214:18 215:18 215:23 patents 70:10 path 85:6 86:20 90:3 96:5 122:3 128:13 131:15 152:11 paths 84:25 85:8,19,22,25 86:18,18 88:11 88:12 126:15 127:8,10,12 134:5 193:2 pazmandi 2:13 5:13 pdf 229:12 230:1 penalty 7:4 226:1 229:16 230:5 pending 8:5 43:6 people 148:5,13 148:19,21 percentage 15:19 16:3 18:8 perfect 95:4,16 95:21 118:25 120:5
---	---	--	---

[perfectly - possibly]

perfectly 51:12 120:8 perform 22:7 24:19 63:3 73:24 78:1,1 81:25 97:2 117:16 134:3 136:3,12 138:12 139:11 147:22 148:19 148:22 169:6 194:1 199:2 207:12 223:9 performance 13:25 70:2,12 performed 78:15,23 130:2 130:23 154:4 187:5 performing 14:19 92:22 113:1 181:21 222:24 performs 90:12 90:22 117:7 period 16:24 55:15 165:22 229:18 230:7 perjury 7:4 226:1 229:17 230:6 person 21:3,9 44:22 45:9,24 62:18 77:10,20 130:4	persons 211:1 perspective 35:11 111:17 petition 9:23 petitioner 1:5 2:4 5:12 ph.d 1:16 4:13 226:10 227:4 228:8 ph.d. 13:14 14:4 229:1,5 231:2 phase 93:23 94:12 109:19 179:25 211:20 phy 134:9 physical 131:14 134:9 pick 116:25 126:18 picking 131:6 199:17 picosecond 111:4,7,14 picoseconds 110:1,3,5,12,18 111:1 120:9,13 120:14 picture 31:22 piece 66:24 222:22 pieces 196:3,5 pink 93:4 pins 110:13 111:13	place 119:23 131:12,17 133:14,18,21 133:22 134:3,8 146:4 172:13 172:19 175:5 193:23,23 194:4 196:5 197:15,21 198:15,16 places 51:18 130:12 131:4,7 131:9 160:2 201:4 203:21 205:20 213:19 plan 20:15 play 80:21 please 5:1 10:24 11:14 21:25 23:24 25:19,20 33:25 36:7 37:14 38:10 39:19,20 41:18 43:15 67:13 81:11 84:13 126:8 155:9 168:16 183:6 185:23 188:1 210:19 plugged 142:17 plus 10:4 123:11,12 point 14:11 17:1 26:16 58:24 72:13	105:15 111:2 115:21 121:10 121:11 129:14 132:19,20 170:7,9 185:6 199:10 205:7 209:2 220:3 pointed 65:8,10 128:25 pointing 28:22 29:12 30:10 points 195:20 196:21 popular 46:4 portion 34:1 43:16 127:14 127:17 position 12:2 12:14,15 137:1 212:6 215:9,13 possession 62:19 possibility 46:3 145:15 146:16 possible 32:8 41:8 52:5 131:9 142:13 142:14 152:1 160:4,17 165:20 215:12 215:17 possibly 28:1 111:5,15 134:7 134:10
--	---	--	---

[practice - proposing]

practice 32:8 33:9,12,21 34:4,5 40:11 40:16 41:9 44:9 46:20 47:3 practiced 78:7 practices 41:6 precise 64:25 217:6 predetermined 22:11,25 24:12 24:21 115:7,16 214:2 preferable 156:10 preferred 127:8 preliminary 9:23,24,24 prelude 218:9 premise 156:22 156:23,23 premium 142:5 142:11,21 preparation 9:2 prepare 8:13 preparing 18:15 20:5 present 126:11 127:8 presenting 69:23 73:18	presents 28:10 preserve 8:1 pretending 127:15 pretty 140:21 prevailing 50:20 prevalent 48:15,19 49:1 preventing 7:7 previous 28:24 53:11 214:4,7 previously 106:8 112:18 116:4 214:10 prior 19:6,13 19:22 privilege 8:2 probably 26:23 72:18 80:6 94:19 121:14 133:25 157:11 165:13 203:4 problem 63:5 132:2 145:14 146:19,22 161:16,19 162:3,25 173:3 173:4,18 180:6 problems 14:23 146:14 procedure 62:17 148:13 148:14,20,22 149:5 229:19	229:20 procedures 146:24 147:2,3 148:10,11 proceeding 5:22 proceedings 225:4 process 47:13 52:12,25 53:25 62:1 67:4 95:20 118:24 125:4,8 129:1 129:19 134:15 181:25 processing 103:19 153:10 206:11,12 processor 12:10,18 13:1 153:11,12 processors 12:21 producing 193:7 professional 11:25 12:8 51:2 228:5 professor 14:5 program 117:9 189:21 190:9 190:17 191:25 193:13 197:1,9 204:16 205:15 206:22 207:20	programmable 123:8 124:2 139:24 150:8 150:15 154:24 programmed 128:15,17 programmer 11:25 programming 129:5,23 192:13,15,22 193:5 194:19 202:12 206:16 209:11 210:3,6 programs 203:16 204:7 205:2 207:15 project 13:12 projects 15:1 pronunciation 165:14 proper 62:3 76:14 properly 68:24 211:21 proposal 174:16 propose 177:21 proposed 174:13 proposing 134:25 135:19 137:4 138:17 170:20 204:15
---	---	--	--

[protocols - ranks]

protocols 22:5 provide 8:6 17:20 19:12 46:22 55:21,22 76:12 79:2,20 98:6 137:23 147:10,21 148:5 151:12 154:18 193:10 210:21,23 provided 19:10 47:14 56:21 64:16 105:24 109:14,17 142:23 148:2,3 149:3,6 157:8 157:16,20 159:3 186:13 211:1 229:19 230:8 provides 36:16 44:13 49:12 62:14,15 72:1 94:10 98:7,18 98:23,24 147:18,24 194:23 198:21 providing 7:4 19:22 61:21,24 76:12 82:5 98:5 118:2,6 204:2 pst 1:18 225:4 public 10:5 227:14	publication 4:14,17,21 25:25 pull 58:6 pulling 42:12 purple 149:18 150:3,16,23 211:17 purpose 59:7 79:15 96:17 104:2 119:20 127:20 154:5 154:13,14 161:14,15 175:20,21 224:1 put 31:16,25 103:22 142:7 161:22 162:11 163:10 167:11 167:12,14 172:19 173:21 175:3,4 179:11 193:22 194:4,5 196:3,4 198:15 198:15,25 201:22 209:9 puts 194:6 putting 90:1 120:12 145:20 167:7 172:12 172:15 177:7 179:9 200:24 201:4	q	209:19 213:14 217:12,15,20 217:23,25 218:3,8,12,23 219:2,11,13 questioning 209:3 questions 7:9 7:21,22 50:22 50:25 51:3,11 52:4 144:8 195:2 216:13 216:25 217:5,6 217:10,21 222:8 224:11 quick 25:15 quicker 11:8 quickly 63:7 71:15 219:24 quite 51:5 132:9 140:24 205:7 quoted 213:18
		qualified 216:9 qualitative 51:15,22 quantify 18:10 quarter 77:2,2 122:24 124:1 124:11 question 7:11 7:12,25 8:4,5 18:21 21:24 22:1,18 24:2 27:17 31:10 32:23 33:25 37:13 43:6,11 45:5,13 48:4 49:11 51:21,22 53:23 59:20 69:12 74:4 85:17 100:19 103:14 117:20 123:1,3 124:25 126:8,19,23 129:23 137:4 138:5,15 155:6 155:8,12 156:8 158:22 160:15 160:16 168:15 168:18,22 169:5 185:22 190:8,20,24 191:22 195:6 197:8,18 201:16 203:18 204:6 209:16	r r 65:24 66:2 231:3,3 r&s 230:1,9 raise 5:1 ramifications 179:19 216:6 randomly 199:17 rank 29:22 ranks 38:15,19

[rate - reasons]

rate 31:24 32:9 54:18 rather 6:9 72:4 reaction 6:11 read 9:16 23:24 27:10,11,24 28:3,13 30:3 33:25 34:1,9 41:16,21,22 43:10,14,16,19 43:22,24 44:4 44:7 52:12 53:25 54:16 55:3,10,10 56:8,17 57:14 58:10,14,17,21 59:4,21 60:6 60:20 62:9,12 62:16,20,21 63:1,3,17,20,21 64:7,14,20 65:2,6,9,17 66:9,12,13,17 66:18,21,23 67:1,10,19,24 68:3,5,7,10 69:5,8,16,21 70:5,7,13,18,23 71:5,7,9,12,17 71:20,22 72:2 72:5,7,10,16,20 72:25 73:9,13 73:16,24 74:9 74:13,22 75:4 75:6 76:4,5,8,8	76:20 78:5,14 78:15,20,22 79:6,11 81:2 81:11,19 82:1 82:11,15,20 83:2,8,12,13,25 84:3 87:18 88:2 89:6,15 89:17,19,22,24 89:25 90:10,12 90:15,17,23 91:18 94:2 96:20 97:3,5 98:10 101:20 101:22 102:1,4 102:5,11 104:16,23 112:23 113:4 116:19,20,24 117:3,5 118:15 118:16 122:23 123:1 124:23 124:24,25 126:4,14 127:2 127:7,10,12 129:8,12,25 134:25 135:5 135:10,14 137:2 138:13 139:11 146:25 147:10,18,25 148:2,6,10,12 148:16,19 149:20,21 150:11,14,20	150:24 152:11 152:15,17 157:17 158:7 159:23 161:4 163:8,14 164:10,18,19 164:23 165:1 166:6 168:7,8 168:19 175:8 175:13 177:22 181:22,24 182:2 183:17 184:4,12,14,17 184:20 185:2 186:17 187:13 187:15,22 188:8,13,15 189:5,21 192:22 194:14 194:20 195:11 195:13 196:9 197:1,9 199:23 201:20 205:2 205:16 207:15 211:16 214:22 215:11 217:4,8 217:17 221:3 221:19 reading 28:6 38:6 45:9,25 48:4 59:9,11 77:10,20 121:8 121:14 130:5 136:25 149:23 185:2,5 229:23	230:9 ready 6:14,16 24:1 39:15 67:14 real 25:15 62:13 108:3 152:19 reality 108:1,7 realizes 68:20 really 15:23 16:20 24:3 49:11 51:21 52:9 53:4 138:15,17 156:22 160:7 167:13 171:7 188:2 191:2 194:3,11 196:17 214:19 214:24,25 realtime 1:24 132:24 136:25 reason 45:12 71:1 178:18 186:2 191:8 231:6,9,12,15 231:18,21 reasonable 131:12,17 reasons 157:8 158:5,23,23,25 158:25 159:1,2 159:3,4 180:9 211:1 212:22 212:24
---	--	--	---

[recall - register]

recall 16:10,25 17:12,16 19:2 19:3,17,21,25 20:1 40:10 48:12 50:2 66:10 176:19 receive 62:2 63:21 75:24 110:23 111:5,7 120:23 162:7,7 193:1 received 12:5 13:14 22:12 23:1 24:13 54:17 111:14 111:22 132:14 173:10 177:16 214:3 receives 75:6 75:16 80:14,15 96:23,24,24,25 96:25 97:1 115:6 receiving 110:23 122:7 123:14,16 reception 24:6 62:7 recess 39:14 63:13 99:22 144:18 203:10 216:18 recited 150:11 recognition 108:3	recognize 11:1 11:15 25:22 185:3 recollection 48:22 51:13 217:9 219:1 record 6:4,13 6:15,20 10:19 26:11 39:11,12 39:16 42:2 63:10,12,14 67:6 86:24 99:21,24 106:11 144:16 144:17,20 165:5 203:1,9 203:12 216:14 216:17 228:10 recording 220:6 rectangle 29:12 rectangles 29:8 29:9 red 92:1,2,4 104:14 217:16 221:1,17 223:16 redirect 4:4 222:6 redirecting 195:15 reduce 52:1 112:10,13,14 reducing 175:1 178:22	refer 5:21,25 26:2 29:22 45:1 61:8,9 141:15 154:7 190:1 224:4 reference 27:19 27:21 28:22 29:17 42:21 46:25 69:4,15 70:17,23 71:7 72:1,15 112:19 112:21 115:18 116:4,16 121:1 121:19 144:25 165:8,12,17 171:15 176:16 176:21,23,24 177:7,12,15 194:18,21,23 200:19 202:6 211:22 referenced 229:6 references 19:6 19:8,10,13,23 50:18 69:7 70:4,15 71:8 71:11,13,16,19 71:21 72:3,6,9 177:11 195:3 195:17,22 196:8,25 198:20 199:9 199:23	referred 58:14 73:13 182:12 referring 5:23 8:20,22 18:2 29:5,21,23 30:20 58:25 91:4 95:9 104:17 107:15 115:9 127:5 128:6,18 132:22 141:9 147:14 165:12 172:2 180:3 183:20 190:2 191:16,24 211:23 217:19 refers 29:15 45:2,15 61:14 123:2 reflect 138:17 refresh 10:20 42:16 217:9 regarding 64:16 regardless 172:5 215:10 register 58:11 58:18 79:1,5,7 80:9,11,20 81:2,6,13,20,24 82:6,21 83:10 83:20 90:3,6 90:21 91:5,10 92:5,7 96:11 96:14 98:12,19
---	---	---	---

[register - researched]

99:5,8,11 100:6,12 128:2 128:2,4 152:22 188:5,6,12 189:17 190:3,9 190:17,18,22 191:4,5,15,24 192:1,21 210:5 222:15 registered 228:4 registry 100:24 101:4,6,8 reinforced 211:25 reinforces 212:16 reinforcing 120:21 relate 165:17 223:1 related 16:19 relating 81:18 relation 57:23 57:23 109:1 120:6 179:3 relationship 110:6 118:3 relative 228:12 228:13 released 49:19 229:21 relevance 70:14 208:5	relevant 8:18 8:19 20:17 49:10 50:21 67:18 68:4 207:23 216:8 reliability 52:1 128:10 157:4 178:23 reliable 57:5,13 60:10 68:15 69:1 70:2,12 73:19 120:19 reliably 66:19 73:2,7,22 120:23 180:5 180:11 rely 26:5 166:20 177:16 206:22 relying 65:13 171:25 remainder 166:2 remember 17:8 17:18 18:16 19:19 49:3 53:23 79:1,25 96:15 121:7,15 183:22 remind 60:25 204:24 remote 1:15 228:7 remotely 227:4	remove 157:21 163:20 171:2 211:17 removed 170:9 removing 151:4 158:7 163:16 repeats 129:11 129:19 rephrase 45:22 77:7 85:17 reply 9:24,25 report 19:15 48:13 49:6 50:8 54:3 55:5 56:11 57:11,24 70:20 72:13,14 89:14 139:14 151:24 209:25 228:6 reported 1:22 99:1,2 reporter 4:6 5:1 39:10,15 43:13 63:12,14 99:20,23 126:3 144:17,19 156:1 202:24 203:9,11 216:17 224:15 224:20 225:2 228:1,5 represent 29:9 140:11	reprogramming 189:17 repurposing 185:11 requested 34:1 43:16 228:9 230:1,9,10 require 26:6 36:16 51:23 114:13,20 115:2 145:24 151:4 155:13 176:25 179:23 required 33:15 36:10,11 40:1 40:2,10,13 47:19 91:12,17 91:19 142:18 148:4,24 181:6 198:1,14 requirement 181:7 requirements 32:2 36:13 47:18 requires 34:16 34:23 89:20 151:24 164:21 167:24 168:4 197:5 research 13:18 13:19,22 49:3 50:7,15 51:4 researched 53:4
--	---	--	--

[researching - rpr]

researching 49:8	224:17 228:8 229:8,10,13 230:2	112:2,4,11 113:3,10 114:19 118:14	184:13,14,24 185:17 186:8 188:13 189:1
respect 10:8		119:24 120:2	189:11,22
respective 128:2 205:25	reviewed 8:17	120:24 121:2	191:5 192:10
responds 79:8	reviewing 20:4 117:2	121:12,22	195:4,11,20
response 9:24	rewrite 152:10	123:21 125:5	197:2,23 198:2
responsibility 118:6	rid 173:4	125:24 128:5	200:14 201:8
responsible 118:2	right 5:2 9:10 15:25 19:6,16	129:2,6,7	202:8,13
responsive 33:24	23:9 25:3,11	130:15 131:18	204:13,17,19
restate 22:18	26:7 40:5,19	132:18 133:22	204:20 205:10
restriction 222:24	42:18 43:2,10	133:23 134:16	206:2,3,5,14
restrictions 32:19,24 36:12	44:2 47:15	135:7 139:5	207:1,6,16
result 28:9 185:14,19,25	49:23 50:17	141:19 143:11	208:4 209:19
187:14,17	56:12 58:4,8	143:17 145:10	209:23 210:24
188:8,10	58:12 60:22	146:24 147:22	212:6,25
results 188:23 222:16	62:22 66:1	148:23 150:8	215:19 217:1
retained 17:20	72:5 73:11	151:17 153:5	223:17,23
retire 15:22	75:3 76:22	153:20 154:7	225:3
retired 16:6	78:12,16,18	154:21 155:11	road 2:12
retraining 179:23	80:9,21 81:8	155:14,21	robert 1:16 4:11,13 226:10
return 229:17 230:6	81:20 82:18,21	157:18 159:15	227:4 228:7
returned 184:4 186:19	83:4 84:17	159:19,24	229:1,5 231:2
review 26:12 26:18 74:3	85:11 86:1,2	160:3 161:5,9	role 80:21
	86:22,22 87:6	161:19 163:22	roman 157:14
	88:2,16 89:12	164:20 166:11	rough 217:4,8 224:21
	92:15 94:17,25	167:22 168:9	roughly 55:14 77:1
	95:2 97:20	170:16,23	row 109:2,10 109:13 112:4
	99:6 101:21	171:4,23	rpr 1:23 227:13 228:25
	102:15 106:20	173:11 174:2	
	106:24 107:2	174:11,16	
	107:20 109:7	176:9 177:23	
	109:24 110:1	177:24 178:10	
	111:20,23	178:16 179:15	
		179:17 180:2	

[rules - second]

rules 6:5,19 230:8 run 54:20,21 54:25 67:12 running 123:17 124:9,10,11,12 128:19	220:13,21 221:2,9,9,10,13 221:18,23,24 222:1,2,17,20 222:25 223:9 sampled 55:18 56:9 103:18,20 131:14,19 169:17 samples 169:11 220:19 sampling 54:10 55:9,24 56:4 64:16 102:5,10 102:10 103:7 104:15 123:19 133:23 169:15 217:17 220:11 220:18,19 222:11 223:2,4 samsung 1:4 5:12 19:11,12 43:3 229:4 231:1 san 2:7 satisfied 136:4 212:14 satisfies 27:22 satisfy 33:15 34:14 47:17 120:9 137:21 160:22 200:8 215:16 save 85:16 122:20	saw 121:7 saying 27:21,25 28:2 33:4 34:22 40:15 41:7 50:6 52:8 52:19 54:8 57:17,20 59:19 70:25 98:20 103:11 118:7 120:21 121:15 127:25 132:9 134:21 135:4 136:24 137:15 141:25 212:2 says 12:20,25 21:15 27:20 28:9,16,23,24 30:5,11 32:7 33:21 34:10 35:19 40:13 43:3 44:12 60:1,8 61:10 63:22,23,25 64:1 67:1 68:2 80:14 98:10,14 98:18 99:3 101:21,24 102:2 107:10 111:3 117:7 118:1,16 119:1 120:3,7 122:2 122:8 126:13 129:5 132:11 132:17 140:6 158:4 174:20	175:21 184:5 186:7 187:17 188:4,19 198:25 205:24 206:9 211:15 212:7 214:1,18 215:24 scant 79:23 schedule 229:10 scope 35:4 37:18 screen 10:3 42:15,22 74:25 134:22 158:17 scroll 143:2,4 144:4 sdram 4:16 39:24 118:1 search 70:21 71:6,25 72:9 89:7,9,10 113:17 115:21 176:21 211:12 searched 70:25 71:2,3 171:20 177:6,10 searching 71:25 second 10:3 11:8 37:1 61:22 100:10 106:18 116:7 144:5 150:13 153:18 157:20
s			
s 231:3 s4 58:14 59:7 60:1,5,6,20 63:17,20 64:7 73:21 78:8,14 78:22 79:7,11 80:21 81:18 83:1,2,12,19,24 84:7 204:25 s5 73:13,16,24 74:7,9 76:5,8 78:9,11,22 79:4,5,10,15 80:21 81:18 82:14,20 83:2 83:3,5,19,24 167:19 168:7 168:11,19,23 169:6 205:1 sales 49:2 sample 102:8 103:3 104:3,13 104:25 105:18 120:24 182:1 211:8 218:1,16 218:17 219:3 220:9,9,10,10			

[second - showing]

165:3 166:8,8 172:2 179:9 182:13 198:1 200:12 203:24 206:1,25 seconds 110:2,3 section 33:2 108:14,24 109:3 151:9 157:9 210:21 210:22 see 10:18,20 11:12,13 17:23 25:19,21 26:25 27:11,16,19,23 28:2 30:7 31:6 31:8 33:3 35:23 38:12 39:20 41:7,19 42:9 46:14 49:18 51:19 52:18 58:5 70:6,10 77:23 85:25 89:19 90:17 100:12 101:15 102:14 107:21 108:8 108:16,22 109:5,8,11,25 110:22 113:8 113:11,16,23 117:13 121:17 121:25 122:1,4 122:10 124:25 132:12 133:18	140:25 145:4 151:17 153:16 156:7 163:4 164:14 165:16 169:16 172:21 177:4 180:1 183:15,19 191:11 200:7 201:12 202:23 203:25 204:1 205:7,8 206:3 206:15 208:7 208:12 210:3 211:12,22 216:21 seeing 121:15 140:24 146:18 seem 28:15 133:14 seems 52:19 106:4 122:8 184:18 199:1 204:9 seen 70:17,22 71:1 90:14 157:1 171:15 176:16,18 177:19 194:18 194:23 sees 106:2 sel 92:21 selected 129:5 selecting 92:22 selection 87:18 92:22	selector 87:11 87:11,19,25 88:20 102:13 149:19,25 221:7 selects 87:13 send 80:23,24 80:25 105:14 123:25 182:24 185:19 186:9 210:10 sending 111:23 185:24 186:7 186:11,14 188:24 189:7,7 193:3 sense 45:18 46:13,22 53:13 57:18 81:22 108:4 121:9 122:8,12 124:5 133:7,11 137:11 154:1 160:7 167:13 167:14 175:4 177:6 198:17 201:4,22 211:5 sent 94:4,7,11 111:25 165:25 185:15 186:23 sentence 24:4 28:3,13 30:3 116:19,25 166:15 211:14	sentences 116:20 117:6 separate 27:2 sequence 130:24 series 24:20 128:19 sessions 9:6,8 set 20:10 124:7 184:12 209:21 sets 29:3 setting 205:25 setup 117:11 118:17 119:3,7 119:18 several 40:18 shape 132:16 share 74:24 shift 130:19 169:24 shifted 123:25 124:10 shifting 125:14 shortly 49:5 show 26:25 74:25 85:4 91:15 109:15 125:17 130:18 141:21,23,24 143:7 146:20 169:1 218:10 showed 159:25 166:24 showing 10:21 30:18 84:20
---	--	---	---

[showing - skew]

107:11 109:18 shown 74:22 85:1 88:14,22 88:25 89:2 92:3 97:9 100:13,13,16 100:18,18,20 101:9 123:10 123:20 127:6 127:19 131:23 132:4,25 133:7 206:6,7 220:2 220:2 shows 85:5 88:9,9,10 125:21 130:1 143:13 146:5,7 155:22 159:10 159:20 203:21 side 57:10,10 57:25 58:1 92:24,25 113:24 162:18 sign 229:16 230:5 signal 61:21,24 64:22,24 66:20 68:14,25 74:21 85:22 86:2 87:22 89:20 90:19,21,25 91:20 92:14,16 92:18,19,20,21 92:22,25 93:1 93:4,8,15,21,21	93:24 94:1,3,7 94:16 98:10,11 101:17,18,22 102:9,10,20,25 103:2,5,6,10,11 103:21,24 104:2,6,17 105:2,3,4,13,17 105:23 109:16 109:17,21,21 110:11,12,16 110:17 114:14 114:16,21,23 115:3,6 121:3 122:7,15 123:5 123:7,15,15,16 123:18 126:15 127:7,10,12 131:16 149:18 149:20 150:1,7 150:9,19 155:2 155:20 162:17 169:9,10,16,19 169:20,22,25 170:2,4,5 171:8 180:11 181:17 192:25 192:25 205:25 207:14 217:18 217:25 218:13 219:3,18 220:15,16 221:12 222:21 223:7,17,18,19 223:20,22,22	224:5,5 signals 22:4,11 23:1 24:6,13 25:10 80:15,24 92:2,9,11 94:23 96:8,25 97:7,15,16,19 102:13,22 109:1 111:4,10 112:16 118:7 142:8 146:15 153:22,23 154:8 155:13 171:3 176:5,8 193:1 204:3 214:3 signature 227:12 228:24 229:21,23,23 230:9 signed 227:7 significant 50:3 70:10 151:7 significantly 50:1 143:24 173:16 signifies 40:1 signify 39:25 silent 158:3 similar 38:17 73:21 118:4 153:2 similarities 38:21,25 39:4 70:10	simple 172:14 simplification 179:19 simplify 179:14 simplifying 178:15,21 simply 49:16 57:24 84:4 163:8 167:3 178:3 222:17 222:23 223:9 simulating 117:22 simulation 117:8 simulations 117:17 single 28:10 29:12 166:5 194:21,23 sit 19:3 44:2 48:12 56:12 sitting 19:21 56:6 70:22 143:11 215:2 situation 137:21 139:9 six 44:16 75:13 75:14 size 142:16,18 142:23 144:1 skew 109:3,19 110:15,24 111:4,5,7,14,21 111:24 112:10
--	---	--	--

[skew - speeds]

112:14 118:6 182:19 skewed 111:1 skill 21:3,9 34:3 37:9,22 45:24 55:25 60:15,18,25 61:1,3,6 62:1,5 62:18,23,24 64:4,23 65:14 66:22 67:2 68:8,12,21 69:23 78:6 79:22,25 80:6 82:25 90:13 104:1 106:2 118:12 131:3 132:1,18 133:9 136:2 138:8 140:7 155:24 156:3 181:6 185:3 198:19 198:19,22 199:20 224:8 skilled 44:22 45:9 77:10,20 119:11 130:4 183:12 211:2 skip 144:7 slave 128:2 slight 75:7 slightly 24:18 slot 143:8,10 slow 168:15 186:21	small 140:23 142:13 smaller 142:7 software 128:18 sold 110:10 solution 159:16 163:16 166:10 solutions 229:7 solve 146:13,19 161:15 162:3 162:25 173:3,4 solves 173:18 solving 146:21 somewhat 26:24 sophisticated 47:22 sorry 13:3 17:3 18:21 21:18,23 21:24 27:25 31:5,6 37:12 42:20 43:6,11 45:4 61:21 63:4 71:15 81:3,10 83:2 84:1,13 85:7 85:16,21 86:6 86:22 87:12 97:12 100:9 106:12 108:17 108:21 115:25 116:2,9 117:3 117:19 123:24 125:2,25	126:22 132:22 139:6 141:9 149:23,23 150:21 153:1 155:4 156:2,2 158:17 165:9 168:17,21 170:14 171:14 185:22 186:4 186:21 187:2 187:24 188:8 190:15 191:10 195:5 198:10 203:19 205:14 221:5,22 sound 6:10 sounds 6:8 98:14 99:19 144:15 202:14 source 56:4 102:22 181:1 sources 20:17 space 140:11 140:13 141:2 142:4,11,21 143:19,25 speak 71:15 speaking 52:10 219:16 spec 120:10 148:1,5 special 145:23 166:16 specific 23:13 26:7 32:2	54:14 72:23 140:17 149:4 154:15 179:11 196:2,21 specifically 28:2 66:25 70:5 133:24 139:13 219:11 specification 23:6,15 28:7 34:3,7,15 35:8 37:21,24 38:7 59:11,12 83:1 111:19 132:6 133:3 142:15 142:18 154:11 160:1 191:11 215:22 specifications 49:12 110:20 specified 147:4 speculate 18:18 speed 48:10 49:14 50:14 53:15,16 54:4 56:18 57:4,6 66:18 68:15 107:10,12,22 109:10,22 142:9 146:15 156:16 173:15 178:25 200:4 speeds 47:14,19 50:1,5 107:16 107:18
--	--	--	---

[spell - substantive]

spell 65:22 spelling 20:8 spend 18:15,22 spice 117:9 119:1 spoke 118:4 spoken 219:23 sporadically 16:14 spot 202:25 stage 103:3 staggered 161:25 164:1 stamping 32:5 stand 137:13 137:18 159:4 208:21,23 standard 4:16 27:23 28:18,20 32:11 39:23 40:8,17,21,25 41:4,9,15,23 43:18,19,25 44:5,10,16,21 45:3 46:8,10 46:23 47:5,11 47:14,18,20,24 48:2,6,7,8,15 49:19 50:20 51:7,10,25 52:15 53:1,10 53:11,13 55:12 55:12 56:7 57:9 61:12,14 61:17 62:5,10	62:11,17,21,25 106:9 118:20 120:7,20 142:24 147:7 147:13,18,21 147:24 standards 27:20 28:12,17 28:18 51:3,5 55:19,22 56:3 147:4,10 standing 33:20 137:16 138:5 stands 96:13 stars 3:4 start 51:8 173:17 187:11 199:22 204:22 213:20 started 121:9 starts 74:16 119:8 157:9 state 24:18 59:1 64:2 90:5 98:3 113:17 131:1 190:24 219:25 227:14 228:3 229:9,12 stated 54:2 199:5 statement 34:10 36:1 60:4 90:11 111:6	states 1:1 status 98:3,11 98:15,19,21,23 99:3,7 186:8 186:10,15 193:1 196:16 stenographic 228:10 stenographic... 1:22 228:6 step 163:3 180:16 182:9 steps 130:25 163:2 181:22 sticking 77:3 stipulate 174:10 stipulation 229:20 stops 160:1 storage 29:24 30:13,14 117:24 142:22 store 186:16 stored 187:14 187:19 188:5 stores 188:8,10 188:19 storing 103:19 188:22 straight 75:11 streams 13:24 street 2:6 strike 33:23 37:3 45:23	103:13 126:8 134:2 139:8 188:9 189:25 strobe 76:20 86:20 94:10,11 94:16 96:8 101:20 102:1,5 120:13 121:3 128:7 149:20 149:21 150:11 150:14 211:20 223:20,21,22 224:5 strobes 96:9 studied 51:4 56:14,20 57:22 57:22 study 51:9,19 51:23 55:6 56:22 199:18 studying 26:13 61:11 stupid 158:17 subject 7:4 submitted 11:4 18:3 72:13 subscribed 226:2 subset 92:8 substance 20:9 substantial 178:15 189:15 substantive 20:7 151:15 152:19
--	--	--	--

[substitute - talk]

substitute 220:15	sur 9:25	symbol 109:7	t
substrate 141:19	sure 17:14	sync 93:22	t 231:3,3
successful 120:19	20:24 23:17	94:12,14,21,21	tabbed 9:16
successfully 90:14 149:2	26:4 34:12	94:23 170:6	table 107:4,9
sufficiently 175:10	35:5 38:4 42:1	175:19	108:13 111:21
suggest 144:13	45:8 47:1	synchronize	111:24 157:10
207:17,19	48:17 51:16	95:1	157:14
suggested 164:10 208:19	58:22 61:22	synchronized	tabs 10:6
suggesting 208:22	68:23 71:2	173:14	take 8:6,11
suggestion 164:25	72:19 76:1	synchronous	11:19 23:18
suite 2:6,12 3:4	81:10,13 86:23	102:22 181:1	27:14 33:1
summarize 13:21 158:5	89:9 92:13,14	system 13:3,4	35:16 38:9
195:1 199:7	115:23 117:17	28:11 40:8	39:13 41:11
supplied 101:22 167:9	117:19 120:23	41:3 44:23,24	51:9 58:3 84:9
support 44:21	121:4 122:21	45:11,14,14,17	95:13 115:24
65:8 192:20	125:2 126:2	45:18,20 48:5	119:21 120:4
193:11 198:7	134:23 136:25	66:18 67:20	121:17 134:11
199:11	140:21 141:25	77:5,15,18	138:18 141:3
supporting 40:22	142:21 144:15	96:1 97:2	144:10 149:7
supports 33:7	154:11 176:5	102:23 111:11	152:25 169:4
suppose 68:16	178:10 180:5	117:8,16	194:1 200:5
128:22	180:15,18	125:21 126:10	203:3 205:19
supposed 49:22	181:2,18	127:11,14	215:9,13
118:21 119:6	188:21 195:21	141:21,24	220:10
	204:22 211:11	155:8,18 160:8	taken 6:21
	213:24 215:18	160:9,10	takes 76:11
	218:7 224:20	162:22 172:21	90:16 105:6,12
	224:23	177:25 178:2,7	talk 28:4 48:13
	surprised	207:11 209:12	69:7 82:25
	154:12	223:5	88:16 89:14
	suspect 72:18	systems 1:24	128:21 165:7
	swear 5:3	12:22,23,25	166:13 167:16
	switches 29:3	21:12 61:13	183:6 184:2
	sworn 227:5	177:8	186:11 196:15
			204:18

[talked - thing]

talked 68:9 78:12 82:14 120:6 147:17 151:24 159:6 160:12 164:22 168:2 170:25 175:12 179:3 180:9 181:25 192:4 195:10 196:24 199:25 200:18,22 209:14,24 210:2,11 212:11,19 talking 24:5 30:8,9,23 50:17 63:16 72:25 88:4,5 89:16 111:21 119:17 127:13 138:10 145:13 179:10 187:8,8 190:5 195:1,7 197:8 203:14 204:19,20 207:18 210:22 213:3 219:8 225:1 talks 61:20,21 61:24 64:21 113:25 146:4 165:19,23 178:4 183:23 186:6	task 73:18 taught 23:5,13 37:21 48:5 84:4,7 103:23 104:21 138:25 151:8 200:25 202:10 204:16 tdqsq 109:7 teach 38:1 196:18 197:4 197:12,19 teaches 134:20 137:10,16 164:5 197:13 201:10 208:10 208:17 209:6 teaching 13:20 26:5 33:19 55:23 78:7 88:10 136:10 137:13 161:22 162:2 192:8 194:2 196:2 201:3 206:20 teachings 45:19 46:22 88:5 118:14 136:20 146:21 149:17 160:5,18 202:10 208:16 209:5 210:12 technical 32:23 216:22 technique 173:6 183:13	183:21 184:14 184:23 185:15 185:20,25 188:11 195:4,9 195:23 technology 17:11 40:25 ted 2:7 5:10 201:12 ted.chandler 2:8 tell 6:22 26:13 26:18 31:2 37:25 53:18 55:6 57:10 89:13 92:12 96:19 114:17 215:6 222:13 223:7 telling 133:8 tells 37:10 98:15,16 102:24 105:2 212:15 temperature 95:20 111:9 118:24 ten 203:8 term 66:9,13 67:10 68:7,11 68:11 69:8,9 69:15 70:18 71:5,7,11,20 72:10,16 102:1 113:2 213:19	214:16 215:18 216:4 terminology 29:21 224:10 terms 55:2 56:8 151:14 208:6 test 108:6 112:8 132:12 132:17 135:2 testimony 5:3 7:5 17:21 testing 125:5,8 125:12 126:25 129:24 131:10 tests 121:1 129:8 text 132:1,10 thank 22:8 42:18 43:9 97:13 122:22 124:16 149:24 201:14 222:4 thick 51:5 thing 19:5 58:7 59:19 67:3,22 82:5 103:13,16 103:21,23 118:8 125:1 127:2 147:6,9 148:4 152:19 160:11 166:22 167:8 173:20 178:5 180:12 199:2 213:8 220:13
---	--	--	---

[things - times]

things 40:24 41:1,21 59:25 60:2,3,9,9,13 62:8 63:25 64:3 66:21 111:9,10 114:24 118:23 118:24 151:23 156:10,14,24 160:24,25 186:3 195:18 214:17 think 6:14 8:25 16:9 17:22,25 18:20 20:7 22:14,15 23:4 23:11,14 24:11 27:14 31:8 33:18,19 34:4 34:15,21 36:18 40:24 41:8 44:16 45:2 46:2,3,6,8,19 47:25 48:3 49:19 50:19 51:18 54:2,7 55:21,21,23 57:3,17 58:25 59:11,19 61:15 62:7 66:17,22 68:8 69:3,14 69:18,20,22,24 70:13 71:6 72:12,15 77:16 78:18 79:9,25	80:3,6 94:18 98:15 102:9 106:23 112:9 112:17,19 113:2 121:10 128:24 130:10 130:11 131:2 131:11,12 134:8 136:6,13 136:14,24 138:16 140:20 146:17 148:18 155:5,11,24 156:2,3,14 158:14,19 160:19,21 164:22 167:10 168:2 172:4 174:8,11 176:13 178:12 190:6,22 194:7 194:8 196:24 198:10,19,22 199:6 200:16 201:20 203:3 207:22,25 208:2 209:16 210:22 214:16 214:17,17 215:13 216:2 216:12 218:14 219:10 222:13 224:8,9 thinking 40:12 102:3 204:21	219:17 third 157:25 thoroughly 56:22 thought 59:8 77:13,17 136:1 194:11 three 14:8 16:2 16:5 60:21 157:8 158:22 179:6 197:22 197:25 198:1,7 199:8 200:18 thursday 1:17 time 8:10 11:8 12:2,13,13,15 12:17 13:5,17 14:2 15:22,23 16:21,24 17:13 18:14 21:4 24:6 29:18 31:24 32:9 37:14 41:1,4 48:20 49:1,4 50:19,20 51:3 51:9 55:14 62:3 65:3 73:3 73:7 74:21 75:8,25 81:11 84:2 85:17 86:23 94:21 99:14 109:20 110:16 116:9 117:11 118:18 118:22 119:3,7	119:19 120:24 122:20 125:25 145:2 146:15 154:2 161:18 161:21 162:1 162:17,19 164:7 166:2 169:16 171:7 179:24 180:17 180:25,25 181:16 183:13 183:21,24,24 183:24,25,25 184:2,2,3,7,13 184:23,25 185:4,15,20,23 185:25 187:4 187:12 188:4 188:11,23 195:3,9,23 196:9,15 203:22,24 205:24 206:4 206:13 222:5 222:20 229:10 229:18,24 230:7 times 40:18 44:16 51:7 53:9 56:24 57:7 119:18 162:8 164:21 164:24 183:23 206:1 212:12
---	--	--	---

[timing - try]

timing 22:6 49:20 59:5,14 64:8 72:21,23 72:24 73:5 76:14 95:10,15 107:10,12,23 108:15,22,23 108:25 109:15 112:4 117:8,10 118:17,25 119:2 181:17 186:14,17 211:19 212:5,8 212:13,15	147:1,6 149:17 150:6 151:3,3 151:8 152:2 153:1,9 154:7 155:19,22 157:8,20 158:1 158:6,24 159:6 159:10,20,23 161:2,14,15 162:2,5,21,23 163:2,15 164:5 164:5,17 165:1 165:18 166:20 166:23 167:4 167:11 170:20 170:25 171:24 172:17,21 174:2 179:2,6 181:10,15,19 182:6,18,18 187:9 190:12 191:9 192:5,9 192:17,19 193:14,16,25 194:6 195:5 196:11,19 197:5,7,11,19 198:13,14,21 198:25 199:4 200:9,13,24 201:1,3,6,10,18 201:22,25,25 202:7,11,12,20 202:21 203:15 204:7,9,17	205:19 206:17 206:19 207:20 208:10,17 209:6,9 210:13 210:24 211:4,7 212:20 213:3 213:10,10 tokuhiro's 154:21 159:16 160:5,17 161:22 163:15 173:6,8,12 177:22 200:13 201:20 208:9 208:15 209:5 211:16 told 48:21 tolerance 95:5 95:6,9 156:16 tolerances 95:10 tonight 224:21 took 10:15 top 26:13 55:6 66:11 74:22 85:14 86:10 topology 145:6 total 9:8 totally 76:1 towards 121:23 trade 156:19 trademark 1:1 transcript 217:4,7,9 224:16,25	228:8,9 229:6 229:8,10,13,13 229:21 230:2,2 transfer 73:1 73:22 180:25 181:1,16 182:5 transferred 165:25 transistor 78:4 transition 119:13 170:6 222:20,21 transitions 105:25 170:4 translate 76:24 transmission 54:23 transmit 25:9 175:7 196:9 transmitting 196:15 trial 1:2 8:21 tried 20:19 208:8 trivial 184:18 195:14 trouble 45:12 true 132:8 226:2 228:9 truth 5:4,5,5 6:22 try 6:12 13:24 45:8 108:1 112:10 115:12 119:2 140:23
--	--	---	--

[try - unique]

142:12,19,21 146:18 160:23 168:25 173:14 183:6 199:19 trying 12:25 14:1 15:22 32:4 33:8 53:20 62:19 65:4 92:9 93:16 95:1,3 119:9,21 138:4 139:6 141:1,23 154:12,17 162:25 171:7,8 171:24 173:3,4 196:20 199:2 tune 115:12 tuned 68:23 101:18 tuning 94:20 113:2 120:18 120:22 130:14 136:3,12,22 137:9,24 180:10,18 181:25 182:1 211:7 213:8,12 turn 26:21 59:16 107:1 210:15 turned 58:20 59:23 61:16,16 turning 63:20 twice 112:12	two 9:6,8 29:3 35:20 38:24 39:6 54:13 67:12 69:6 70:4 90:1 94:23 99:13 107:19 116:25 152:1 166:6,7 171:10 177:8 177:21 179:11 183:23 186:3 198:20 199:23 207:15 type 31:24 58:10 61:13 66:21 67:22,23 70:21 82:3 96:21,21 113:2 114:12,22 128:19 186:10 186:14 220:11 220:18,19 222:17,21 types 14:20 15:15 typically 143:23 144:1	129:3,18,21 156:9 157:19 157:24 179:8 179:13 214:5 ultimate 114:8 ultimately 87:22 207:11 un 122:11 unchanging 115:9 under 7:16 10:21 12:8 47:14 91:23 109:2 114:10 226:1 undergrad 11:24 undersigned 227:3 understand 6:21,24 7:3,6 7:12,14,16,18 7:20,23,24 8:3 8:9 12:25 15:11 29:18 34:19 35:6 37:9,22 40:25 44:23 45:3,10 45:25 46:2 50:9 53:20 60:15 61:17 62:19,21 66:23 68:9 69:25 70:14 80:3 92:10 102:21	106:3 108:24 118:13 131:3 137:1 138:10 151:17 155:4,6 159:15 160:3 162:13 170:23 179:5 190:15 191:16 195:17 197:22 201:15 209:2 215:7 219:8 221:16 224:9 understanding 5:19 29:20 34:2 35:9,10 35:14 40:7 49:12,15 50:19 56:4 62:6,11 74:9 79:17 107:17 122:5 128:11 130:7 203:16 214:6 214:13 215:3 215:21,23 219:12 220:8 understands 69:20,22,23 138:8 understood 16:1,22 46:15 95:22 136:24 195:6 undue 173:18 unique 140:22 140:25
	u		
	u 65:24,24 66:2 u.s. 1:11 5:17 5:25 uh 18:20 52:23 63:18 76:19 78:10 82:17 113:5 125:6		

[unit - videotaped]

unit 110:2 114:9,9 153:10 203:22,24 205:24 206:4 206:14 united 1:1 units 204:2 unmodified 190:16 191:14 191:23 192:3 212:10,10 unpack 46:14 upper 86:1 usc 12:5 use 20:22,24 45:16 46:5 54:5 57:6 66:9 66:13 67:10 70:17 71:11 106:1 130:19 136:9,10 147:5 148:14 149:2 156:11 171:16 172:7 176:16 181:19 183:12 185:4 190:6 191:23 195:14 204:15 219:18 used 19:18 20:2 22:5 24:22 48:25 59:5 69:8,15 71:7 71:20,22 72:9 91:2 94:16 103:2 146:13	184:16 186:7 187:18 189:4 189:21 193:12 200:6 216:1 221:2,18 user 112:15 131:2 uses 29:6 38:17 45:14 71:5 72:16 75:20,21 114:15 123:6,9 131:20 171:5 182:24 195:13 201:6 212:20 215:18 using 24:19 57:16 62:4 66:19 79:21 117:8 120:1 123:11,12 135:2 137:2 148:6 159:7,22 161:3 164:17 171:3 173:5 175:13 181:17 182:15 184:10 185:1 190:6 195:8,11 196:9 196:25 197:8,9 202:13 203:17 204:8 207:20 214:22 216:5 223:6 usp 4:19,22	usually 143:25 utilize 61:12 63:2 75:24 102:18 104:4 104:12 112:15 utilizing 185:10 186:12 v v 165:15 vague 50:3 222:12 vaguely 202:14 valid 105:1,3,4 105:24 106:1 117:12 118:11 118:18 119:4,6 119:8,9,15 156:22,23 181:12 220:17 221:8 222:3 223:8,8 value 105:2,6 105:23,24 108:12 109:12 109:15,16 115:8,13 128:9 129:4,6 132:12 132:14,15 140:2 152:16 152:19 154:18 154:18,19 155:17 161:1 169:12,15,25 170:1,2 222:18 223:8	values 128:1,5 128:6,7 129:2 129:24 153:24 153:24 163:6,6 182:25 223:7 variable 113:10 113:12 114:1,4 114:9,9,13 123:9 154:14 154:23 193:13 variables 95:14 95:19 variety 117:18 131:6 148:6 various 14:23 95:19 107:12 108:9 139:25 154:6 204:3 206:10 verified 18:13 verify 58:1 veritext 229:7,9 229:11 versa 224:5 version 20:24 91:22 100:3 101:18 versus 53:21 184:20 196:21 vice 224:5 video 100:10 125:2 134:23 videotaped 1:15
--	--	--	--

[view - words]

view 131:8 viewing 58:7 virtual 27:7 vitae 4:12 voltage 95:20 vs 1:6 229:4 231:1	157:5 160:23 166:13,13 175:5 182:19 188:7 190:21 190:23 191:9 191:10,13 195:16,19 199:14,18 202:15,18 210:4 211:10 213:14 218:24 wanted 43:7 72:4 86:17 148:18 162:25 way 45:6 46:21 46:21 48:14 49:16 51:14 56:8 58:16 102:22 103:22 107:11 111:22 114:25 115:11 115:20 126:7 128:9 142:7 154:16 155:22 155:23 157:4 158:15,20 159:20 164:4,5 164:13 171:2 178:19 179:11 182:22 191:20 194:16 199:1 200:13 204:9 207:10 208:6 208:17,19,23 209:5 213:10	215:10,15 220:5 ways 128:22 155:25 156:4 175:8 177:21 200:2 we've 56:25 96:3 178:2 190:4 191:6,24 195:1 webcam 6:9 wedig 1:16 4:11,13 5:16 6:18 14:12,16 14:17,21 15:4 15:9,16 39:18 42:22 63:16 100:2 132:22 144:23 203:14 216:21,24 222:9 226:10 227:4 228:7 229:1,5 231:2 wedig.com 229:2 went 104:6 169:13,22 whichever 20:24 widths 26:7 wildly 199:17 willing 57:21 159:4 216:2 window 27:2 117:12 118:11	118:18 119:4,5 119:6,18,19 180:20 witness 5:6 42:14 63:4 65:24 67:14 97:12 99:16,19 106:12 144:9 144:14 168:17 183:8 222:5 229:13,16 230:2,5 231:24 witness's 6:8 wonder 144:9 wondering 124:15 word 29:6 31:21 45:17 50:4 51:15 54:2,6 57:16 61:20 71:17,22 98:21 99:3 122:11 214:14 214:23 215:3 220:8,9 wording 22:16 27:21 184:6 198:24,25 212:7 words 27:23 28:19,23 54:13 57:17 59:1,3 59:10,10 60:21 60:24,24,25 61:2 65:11
w			
w 93:13 wait 42:11 124:24 126:21 201:12 waiting 201:14 waived 229:23 229:23 waiving 229:20 walk 38:3 74:2 74:5,6,11 92:13 151:25 169:2 walked 209:8 want 18:17 27:14 30:20 42:13 47:1 49:16 52:5 58:22 65:22 72:13 74:9,15 74:24 85:7 86:14,15 88:15 112:17 115:17 122:18 124:23 127:3 140:22 142:12,19 144:9 148:8,21 148:25 149:1			

[words - zumkehr]

67:1 68:3 70:5 70:8,13 90:8,9 94:12 101:7 120:3 121:15 122:10 123:24 190:5 work 12:18 13:9,22,23 15:3,7,9,10,17 15:19,24 16:3 16:10,16,18 17:1,9,10 18:13 68:24 72:14 77:22 80:5 83:1 90:2 101:2,5 102:22 161:11 163:9 202:3 208:6,10 208:12,13,24 209:3,12,20 workable 41:3 155:18 worked 12:20 13:17 14:4 96:1 209:4 working 12:9 15:24 16:7,13 16:15 works 35:8 99:18 207:10 world 108:3 120:4 worries 162:19 write 18:5 22:12 23:2,8	24:7,13,19,20 24:25 25:2,11 68:19 81:1,25 82:10 84:3 89:14,17,19,22 89:23,25 90:10 90:12,15,17,23 91:18 93:6,9 93:19 96:20 97:4,5 146:23 146:25 147:2,3 147:7,8,22,25 148:1,10,22,24 149:4 152:10 152:16 157:17 158:7 159:22 161:3 163:3 164:6,8,14,18 164:21 167:25 168:12,23 169:7 170:7 175:9,13,18,20 184:11,19,23 195:4,9,14,24 205:1,3 written 21:8 52:7 128:1 wrong 24:10 149:24 wrote 18:3,9	y	224:9 year 17:6 years 11:24 12:9 14:8 16:2 16:5,8,9,12,16 16:17,18,21 yep 116:14 129:3 yield 119:2 yields 117:10 118:17
		yeah 13:4 16:14 18:20 20:8 29:14 30:25 31:8 32:6 33:19 34:21 43:17 53:22 59:25 66:3 69:14 70:20 73:6 77:23 78:18,20 79:17 83:22 86:21 89:11 94:22 96:24 99:7 102:2 104:20 108:20 110:3 113:4 114:7 115:11 116:23 118:1 121:7,13 122:12 124:16 124:17 142:3 142:11 143:25 144:12 145:8 153:9 154:16 155:15 160:15 166:14 169:4 178:5 179:17 180:24 181:13 187:19,25 188:15 189:4,5 193:14 194:8 197:11 202:23 206:6,19 207:3 216:2 222:8	z z 65:24,24 66:2 zero 111:1 163:7 zumkehr 4:20 65:21 66:4,9 66:12 112:19 112:19 113:1,7 113:9 115:22

Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY.

THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

VERITEXT LEGAL SOLUTIONS
COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

Veritext Legal Solutions is committed to maintaining the confidentiality of client and witness information, in accordance with the regulations promulgated under the Health Insurance Portability and Accountability Act (HIPAA), as amended with respect to protected health information and the Gramm-Leach-Bliley Act, as amended, with respect to Personally Identifiable Information (PII). Physical transcripts and exhibits are managed under strict facility and personnel access controls. Electronic files of documents are stored in encrypted form and are transmitted in an encrypted fashion to authenticated parties who are permitted to access the material. Our data is hosted in a Tier 4 SSAE 16 certified facility.

Veritext Legal Solutions complies with all federal and State regulations with respect to the provision of court reporting services, and maintains its neutrality and independence regardless of relationship or the financial outcome of any litigation. Veritext requires adherence to the foregoing professional and ethical standards from all of its subcontractors in their independent contractor agreements.

Inquiries about Veritext Legal Solutions' confidentiality and security policies and practices should be directed to Veritext's Client Services Associates indicated on the cover of this document or at www.veritext.com.