# JEDEC STANDARD

## DDR3 SDRAM Specification

## JESD79-3A

**(Revision of JESD79-3)**

**September 2007**

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**

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# Contents

1 Scope ..... 1
2 DDR3 SDRAM Package Pinout and Addressing ..... 3
2.1 DDR3 SDRAM x4 Ballout using MO-207 (Top view: see balls through package) ..... 3
2.2 DDR3 SDRAM x8 Ballout using MO-207 (Top view: see balls through package) ..... 4
2.3 DDR3 SDRAM x16 Ballout using MO-207 (Top view: see balls through package) ..... 5
2.4 Stacked / dual-die DDR3 SDRAM x4 Ballout using MO-207 (Top view: see balls through package) ..... 6
2.5 Stacked / dual-die DDR3 SDRAM x8 Ballout using MO-207 (Top view: see balls through package) ..... 7
2.6 Stacked / dual-die DDR3 SDRAM x16 Ballout using MO-207 (Top view: see balls through package) ..... 8
2.7 Pinout Description ..... 9
2.8 DDR3 SDRAM Addressing ..... 11
2.8.1 512Mb ..... 11
2.8.2 1Gb ..... 11
2.8.3 2Gb ..... 11
2.8.4 4Gb ..... 11
2.8.5 8Gb ..... 12
3 Functional Description ..... 13
3.1 Simplified State Diagram ..... 13
3.2 Basic Functionality ..... 14
3.3 RESET and Initialization Procedure ..... 15
3.3.1 Power-up Initialization Sequence ..... 15
3.3.2 Reset Initialization with Stable Power ..... 17
3.4 Register Definition ..... 18
3.4.1 Programming the Mode Registers ..... 18
3.4.2 Mode Register MR0 ..... 18
3.4.3 Mode Register MR1 ..... 22
3.4.4 Mode Register MR2 ..... 25
3.4.5 Mode Register MR3 ..... 27
4 DDR3 SDRAM Command Description and Operation ..... 29
4.1 Command Truth Table ..... 29
4.2 CKE Truth Table ..... 31
4.3 No OPeration (NOP) Command ..... 32
4.4 Deselect Command ..... 32
4.5 DLL-off Mode ..... 33
4.6 DLL on/off switching procedure ..... 34
4.6.1 DLL “on” to DLL “off” Procedure ..... 34
4.6.2 DLL “off” to DLL “on” Procedure ..... 35
4.7 Input clock frequency change ..... 36
4.8 Write Leveling ..... 38
4.8.1 DRAM setting for write leveling & DRAM termination function in that mode ..... 38
4.8.2 Procedure Description ..... 39
4.8.3 Write Leveling Mode Exit ..... 41
4.9 Extended Temperature Usage ..... 42



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Samsung v. Netlist
IPR2023-00847

# Contents

4.9.1 Self-Refresh Temperature Range - SRT ....42
4.10 Multi Purpose Register ....44
4.10.1 MPR Functional Description ....45
4.10.2 MPR Register Address Definition ....46
4.10.3 Relevant Timing Parameters ....46
4.10.4 Protocol Example ....46
4.11 ACTIVE Command ....51
4.12 PRECHARGE Command ....51
4.13 READ Operation ....52
4.13.1 READ Burst Operation ....52
4.13.2 READ Timing Definitions ....53
4.14 WRITE Operation ....62
4.14.1 DDR3 Burst Operation ....62
4.14.2 WRITE Timing Violations ....62
4.14.3 tWPRE Calculation ....64
4.14.4 tWPST Calculation ....64
4.15 Self-Refresh Operation ....70
4.16 Power-Down Modes ....72
4.16.1 Power-Down Entry and Exit ....72
4.16.2 Power-Down clarifications - Case 1 ....77
4.16.3 Power-Down clarifications - Case 2 ....78
4.16.4 Power-Down clarifications - Case 3 ....79
5 On-Die Termination (ODT) ....80
5.1 ODT Mode Register and ODT Truth Table ....80
5.2 Synchronous ODT Mode ....81
5.2.1 ODT Latency and Posted ODT ....81
5.2.2 Timing Parameters ....81
5.2.3 ODT during Reads ....83
5.3 Dynamic ODT ....85
5.3.1 Functional Description: ....85
5.3.2 ODT Timing Diagrams ....86
5.4 Asynchronous ODT Mode ....91
5.4.1 Synchronous to Asynchronous ODT Mode Transitions ....92
5.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry 92
5.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit ..93
5.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods ....94
5.5 ZQ Calibration Commands ....96
5.5.1 ZQ Calibration Description ....96
5.5.2 ZQ Calibration Timing ....97
5.5.3 ZQ External Resistor Value, Tolerance, and Capacitive loading ....97
6 Absolute Maximum Ratings ....98
6.1 Absolute Maximum DC Ratings ....98
6.2 DRAM Component Operating Temperature Range ....99
7 AC & DC Operating Conditions ....100



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IPR2023-00847

# Contents

7.1 Recommended DC Operating Conditions....100
8 AC and DC Input Measurement Levels....101
8.1 AC and DC Logic Input Levels for Single-Ended Signals....101
8.2 AC and DC Logic Input Levels for Differential Signals....103
8.2.1 Differential signal definition....103
8.2.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)104
8.2.3 Single-ended requirements for differential signals....104
8.3 Differential Input Cross Point Voltage....106
8.4 Slew Rate Definitions for Single Ended Input Signals....107
8.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)....107
8.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)....107
8.5 Slew Rate Definitions for Differential Input Signals....108
9 AC and DC Output Measurement Levels....109
9.1 Single Ended AC and DC Output Levels....109
9.2 Differential AC and DC Output Levels....109
9.3 Single Ended Output Slew Rate....110
9.4 Differential Output Slew Rate....111
9.5 Reference Load for AC Timing and Output Slew Rate....112
9.6 Overshoot and Undershoot Specifications....113
9.6.1 Address and Control Overshoot and Undershoot Specifications....113
9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications....114
9.7 34 ohm Output Driver DC Electrical Characteristics....115
9.7.1 Output Driver Temperature and Voltage sensitivity....117
9.8 On-Die Termination (ODT) Levels and I-V Characteristics....118
9.8.1 On-Die Termination (ODT) Levels and I-V Characteristics....118
9.8.2 ODT DC Electrical Characteristics....119
9.8.3 ODT Temperature and Voltage sensitivity....122
9.9 ODT Timing Definitions....123
9.9.1 Test Load for ODT Timings....123
9.9.2 ODT Timing Definitions....123
10 IDD Specification Parameters and Test Conditions....127
10.1 IDD Measurement Conditions....127
10.2 IDD Specifications....139
11 Input/Output Capacitance....141
11.1 Input/Output Capacitance....141
12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600....142
12.1 Clock Specification....142
12.1.1 Definition for tCK(avg)....142
12.1.2 Definition for tCK(abs)....142
12.1.3 Definition for tCH(avg) and tCL(avg)....142
12.1.4 Definition for tJIT(per) and tJIT(per,lck)....142
12.1.5 Definition for tJIT(cc) and tJIT(cc,lck)....143
12.1.6 Definition for tERR(nper)....143
12.2 Refresh parameters by device density....143
12.3 Standard Speed Bins....144



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IPR2023-00847

# Contents

12.3.1 Speed Bin Table Notes ..... 148
13 Electrical Characteristics and AC Timing ..... 149
13.1 Jitter Notes ..... 156
13.2 Timing Parameter Notes ..... 157
13.3 Address / Command Setup, Hold and Derating ..... 159
13.4 Data Setup, Hold and Slew Rate Derating ..... 166



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# List of Figures

Figure 1 —Simplified State Diagram . . . 13
Figure 2 —Reset and Initialization Sequence at Power-on Ramping. . . . 16
Figure 3 —Reset Procedure at Power Stable Condition . . . 17
Figure 4 —tMRD Timing . . . 18
Figure 5 —tMOD Timing . . . 18
Figure 6 —MR0 Definition . . . 19
Figure 7 —MR1 Definition . . . 22
Figure 8 —MR2 Definition . . . 25
Figure 9 —MR3 Definition . . . 27
Figure 10 —DLL-off mode READ Timing Operation . . . 33
Figure 11 — DLL Switch Sequence from DLL-on to DLL-off . . . 34
Figure 12 —DLL Switch Sequence from DLL Off to DLL On . . . 35
Figure 13 —Change Frequency during Precharge Power-down . . . 37
Figure 14 —Write Leveling Concept . . . 38
Figure 15 —Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2 . . . 40
Figure 16 —Timing details of Write leveling exit . . . 41
Figure 17 —MPR Block Diagram . . . 44
Figure 18 —MPR Readout of predefined pattern, BL8 fixed burst order, single readout . . . 47
Figure 19 —MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout 48
Figure 20 —MPR Readout predefined pattern, BC4, lower nibble then upper nibble . . . 49
Figure 21 —MPR Readout of predefined pattern, BC4, upper nibble then lower nibble . . . 50
Figure 22 —READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8) . . . 52
Figure 23 —READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8) . . . 52
Figure 24 —READ Timing Definition . . . 53
Figure 25 —Clock to Data Strobe Relationship . . . 54
Figure 26 —Data Strobe to Data Relationship . . . 55
Figure 27 —tLZ and tHZ method for calculating transitions and endpoints . . . 56
Figure 28 —Method for calculating tRPRE transitions and endpoints . . . 57
Figure 29 —Method for calculating tRPST transitions and endpoints . . . 57
Figure 30 —READ (BL8) to READ (BL8) . . . 58
Figure 31 —READ (BC4) to READ (BC4) . . . 58
Figure 32 —READ (BL8) to WRITE (BL8) . . . 59
Figure 33 —READ (BC4) to WRITE (BC4) OTF . . . 59
Figure 34 —READ (BL8) to READ (BC4) OTF . . . 60
Figure 35 —READ (BC4) to READ (BL8) OTF . . . 60
Figure 36 —READ (BC4) to WRITE (BL8) OTF . . . 61
Figure 37 —READ (BL8) to WRITE (BC4) OTF . . . 61
Figure 38 —Write Timing Definition and Parameters . . . 63
Figure 39 —Method for calculating tWPRE transitions and endpoints . . . 64
Figure 40 —Method for calculating tWPST transitions and endpoints . . . 64
Figure 41 —WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8) . . . 65
Figure 42 —WRITE Burst Operation WL = 9 (AL = CL-1, CWL = 5, BL8) . . . 65
Figure 43 —WRITE (BC4) to READ (BC4) Operation. . . . 66
Figure 44 —WRITE (BC4) to PRECHARGE Operation. . . . 66
Figure 45 —WRITE (BL8) to WRITE (BL8) . . . 67
Figure 46 —WRITE (BC4) to WRITE (BC4) OTF . . . 67



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IPR2023-00847

# List of Figures

Figure 47 —WRITE (BL8) to READ (BC4/BL8) OTF . . . 68
Figure 48 —WRITE (BC4) to READ (BC4/BL8) OTF . . . 68
Figure 49 —WRITE (BL8) to WRITE (BC4) OTF . . . 69
Figure 50 —WRITE (BC4) to WRITE (BL8) OTF . . . 69
Figure 51 —Self-Refresh Entry/Exit Timing . . . 71
Figure 52 —Active Power-Down Entry and Exit Timing Diagram . . . 73
Figure 53 —Power-Down Entry after Read and Read with Auto Precharge . . . 73
Figure 54 —Power-Down Entry after Write with Auto Precharge . . . 74
Figure 55 —Power-Down Entry after Write . . . 74
Figure 56 —Precharge Power-Down (Fast Exit Mode) Entry and Exit . . . 75
Figure 57 — Precharge Power-Down (Slow Exit Mode) Entry and Exit . . . 75
Figure 58 — Refresh Command to Power-Down Entry . . . 76
Figure 59 — Active Command to Power-Down Entry . . . 76
Figure 60 — Precharge / Precharge all Command to Power-Down Entry . . . 77
Figure 61 — MRS Command to Power-Down Entry . . . 77
Figure 62 —Power-Down Entry/Exit Clarifications - Case 1 . . . 78
Figure 63 —Power-Down Entry/Exit Clarifications - Case 2 . . . 78
Figure 64 —Power-Down Entry/Exit Clarifications - Case 3 . . . 79
Figure 65 —Functional Representation of ODT . . . 80
Figure 66 —Synchronous ODT Timing Example for AL = 3; CWL = 5; ODTLon = AL + CWL - 2 = 6.0; ODTLoff = AL + CWL - 2 = 6 . . . 82
Figure 67 —Synchronous ODT example with BL = 4, WL = 7 . . . 83
Figure 68 —ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8) . . . 84
Figure 69 —Dynamic ODT: Behavior with ODT being asserted before and after the write . . . 87
Figure 70 —Dynamic ODT: Behavior without write command, AL = 0, CWL = 5 . . . 87
Figure 71 —Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles . . . 88
Figure 72 —Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.89
Figure 73 —Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles . . . 90
Figure 74 —Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored . . . 91
Figure 75 —Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL = 0; CWL = 5; tANPD = WL - 1 = 4) . . . 93
Figure 76 —Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; tANPD = WL - 1 = 9) . . . 94
Figure 77 —Transition period for short CKE cycles, entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4) . . . 95
Figure 78 —ZQ Calibration Timing . . . 97
Figure 79 —Illustration of VRef(DC) tolerance and VRef ac-noise limits . . . 102
Figure 80 —Definition of differntial ac-swing and “time above ac-level” tDVAC . . . 103
Figure 81 —Single-ended requirement for differential signals . . . 105
Figure 82 —Vix Definition . . . 106



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# List of Figures

Figure 83 —Input Nominal Slew Rate Definition for Single-Ended Signals. . . . . 107
Figure 84 —Differential Input Slew Rate Definition for DQS, DQS# and CK, CK# . . . . . 108
Figure 85 —Single Ended Output Slew Rate Definition . . . . . 110
Figure 86 —Differential Output Slew Rate Definition. . . . . 111
Figure 87 —Reference Load for AC Timing and Output Slew Rate . . . . . 112
Figure 88 —Address and Control Overshoot and Undershoot Definition . . . . . 113
Figure 89 —Clock, Data, Strobe and Mask Overshoot and Undershoot Definition . . . . . 114
Figure 90 —Output Driver: Definition of Voltages and Currents . . . . . 115
Figure 91 —On-Die Termination: Definition of Voltages and Currents . . . . . 118
Figure 92: ODT Timing Reference Load123
Figure 93 —Definition of $t^{AON}$ . . . . . 124
Figure 94 —Definition of $t^{AONPD}$ . . . . . 124
Figure 95 —Definition of $t^{AOF}$ . . . . . 125
Figure 96 —Definition of $t^{AOFPD}$ . . . . . 125
Figure 97 —Definition of $t^{ADC}$ . . . . . 126
Figure 98 —IDD1 Example (DDR3-800-555, 512Mb x8): Data DQ is shown but the output buffer should be switched off (per MR1 bit A12 =”1”) to achieve Iout = 0mA. Address inputs are split into 3 parts. . . . . 130
Figure 99 —IDD2N / IDD3N Example (DDR3-800-555, 512Mb x8). . . . . 132
Figure 100 —IDD4R Example (DDR3-800-555, 512Mb x8): data DQ is shown but the output buffer should be switched off (per MR1 bit A12=”1”) to achieve Iout = 0mA. Address inputs are split into 3 parts. . . . . 135
Figure 101 —Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock). . . . . 162
Figure 102 —Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock). . . . . 163
Figure 103 —Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock) . . . . . 164
Figure 104 —Illustration of tangent line for for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock). . . . . 165
Figure 105 —Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock). . . . . 168
Figure 106 —Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock). . . . . 169
Figure 107 —Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock) . . . . . 170
Figure 108 —Illustration of tangent line for for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock). . . . . 171



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IPR2023-00847

# List of Tables

Table 1 —Input / output functional description . . . . . 9
Table 2 —State Diagram Command Definitions . . . . . 13
Table 3 —Burst Type and Burst Order . . . . . 20
Table 4 —Additive Latency (AL) Settings . . . . . 23
Table 5 —TDQS, TDQS# Function Matrix . . . . . 24
Table 6 —Command Truth Table . . . . . 29
Table 7 —CKE Truth Table . . . . . 31
Table 8 —MR setting involved in the leveling procedure . . . . . 39
Table 9 —DRAM termination function in the leveling mode . . . . . 39
Table 10 —Mode Register Description . . . . . 42
Table 11 —Self-Refresh mode summary . . . . . 43
Table 12 —MPR MR3 Register Definition . . . . . 44
Table 13 —MPR MR3 Register Definition . . . . . 46
Table 14 —Power-Down Entry Definitions . . . . . 72
Table 15 —Termination Truth Table . . . . . 80
Table 16 —ODT Latency . . . . . 81
Table 17 —Latencies and timing parameters relevant for Dynamic ODT . . . . . 85
Table 18 —Timing Diagrams for “Dynamic ODT” . . . . . 86
Table 19 —Asynchronous ODT Timing Parameters for all Speed Bins . . . . . 91
Table 20 —ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period . . . . . 92
Table 21 —Absolute Maximum DC Ratings . . . . . 98
Table 22 —Temperature Range . . . . . 99
Table 23 —Recommended DC Operating Conditions . . . . . 100
Table 24 —Single Ended AC and DC Input Levels . . . . . 101
Table 25 —Differential AC and DC Input Levels . . . . . 104
Table 26 —Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS# . . . . . 104
Table 27 —Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU# . . . . . 105
Table 28 —Cross point voltage for differential input signals (CK, DQS) . . . . . 106
Table 29 —Single-ended Input Slew Rate Definition . . . . . 107
Table 30 —Differential Input Slew Rate Definition . . . . . 108
Table 31 —Single-ended AC and DC Output Levels . . . . . 109
Table 32 —Differential AC and DC Output Levels . . . . . 109
Table 33 —Single-ended Output Slew Rate Definition . . . . . 110
Table 34 —Output Slew Rate (single-ended) . . . . . 110
Table 35 —Differential Output Slew Rate Definition . . . . . 111
Table 36 —Differential Output Slew Rate . . . . . 111
Table 37 —AC Overshoot/Undershoot Specification for Address and Control Pins . . . . . 113
Table 38 —AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask . . . . . 114
Table 39 —Output Driver DC Electrical Characteristics, assuming $R^{ZQ}$ = 240 W ; entire operating temperature range; after proper ZQ calibration . . . . . 115
Table 40 —Output Driver Sensitivity Definition . . . . . 117
Table 41 —Output Driver Voltage and Temperature Sensitivity . . . . . 117



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Netlist EX2019
Samsung v. Netlist
IPR2023-00847

# List of Tables

Table 42 —ODT DC Electrical Characteristics, assuming $R^{ZQ}$ = 240 W +/- 1% entire operating temperature range; after proper ZQ calibration . . . . . 119
Table 43 —ODT Sensitivity Definition . . . . . 122
Table 44 —ODT Voltage and Temperature Sensitivity . . . . . 122
Table 45 —ODT Timing Definitions . . . . . 123
Table 46 —Reference Settings for ODT Timing Measurements . . . . . 123
Table 47 —Overview of Tables providing IDD Measurement Conditions and DRAM Behavior . . . . . 127
Table 48 —Definition of SWITCHING for Address and Command Input Signals . . . . . 127
Table 49 —Definition of SWITCHING for Data (DQ) . . . . . 128
Table 50 —For IDD testing the following parameters are utilized. . . . . 128
Table 51 —IDD Measurement Conditions for IDD0 and IDD1 . . . . . 129
Table 52 —IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q . . . 131
Table 53 —IDD Measurement Conditions for IDD3N and IDD3P(fast exit) . . . . . 133
Table 54 —IDD Measurement Conditions for IDD4R, IDD4W and IDD7 . . . . . 134
Table 55 —IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions . . 136
Table 56 —IDD Measurement Conditions for IDD5B . . . . . 137
Table 57 —IDD Measurement Conditions for IDD6, IDD6ET, and IDD6TC . . . . . 137
Table 58 —$I^{DD}$ Specification Example 512M DDR3 . . . . . 139
Table 59 —$I^{DD6}$ Current Definition . . . . . 139
Table 60 —$I^{DD6}$ Specification . . . . . 140
Table 61 —Input / Output Capacitance . . . . . 141
Table 62 —Refresh parameters by device density . . . . . 143
Table 63 —DDR3-800 Speed Bins. . . . . 144
Table 64 —DDR3-1066 Speed Bins. . . . . 145
Table 65 —DDR3-1333 Speed Bins. . . . . 146
Table 66 —DDR3-1600 Speed Bins. . . . . 147
Table 67 —Timing Parameters by Speed Bin . . . . . 149
Table 68 —ADD/CMD Setup and Hold Base-Values for 1V/ns . . . . . 159
Table 69 —Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based . . . . . 160
Table 70 —Derating values DDR3-1333/1600 tIS/tIH - ac/dc based - Alternate AC150 Threshold . . . . . 160
Table 71 —Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition . . . . . 161
Table 72 —Data Setup and Hold Base-Values . . . . . 166
Table 73 —Derating values DDR3-800/1066 tDS/tDH - ac/dc based . . . . . 167
Table 74 —Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition . . . . . 167



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# 1 Scope

This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

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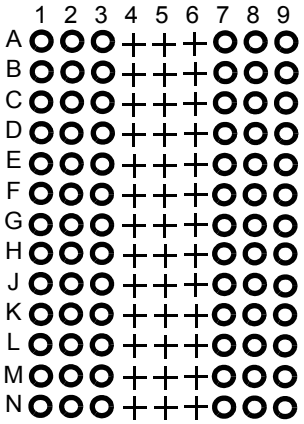
# 2 DDR3 SDRAM Package Pinout and Addressing

## 2.1 DDR3 SDRAM x4 Ballout using MO-207 (Top view: see balls through package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | |
| B | | | | | | | | | | | | |
| C | NC | NC | | NC | | | | NC | | NC | NC | |
| D | | | | | | | | | | | | |
| E | | | | | | | | | | | | |
| F | NC | VSS | VDD | NC | | | | NC | VSS | VDD | NC | A |
| G | | VSS | VSSQ | DQ0 | | | | DM | VSSQ | VDDQ | | B |
| H | | VDDQ | DQ2 | DQS | | | | DQ1 | DQ3 | VSSQ | | C |
| J | | VSSQ | NC | DQS# | | | | VDD | VSS | VSSQ | | D |
| K | | VREFDQ | VDDQ | NC | | | | NC | NC | VDDQ | | E |
| L | | NC | VSS | RAS# | | | | CK | VSS | NC | | F |
| M | | ODT | VDD | CAS# | | | | CK# | VDD | CKE | | G |
| N | | NC | CS# | WE# | | | | A10/AP | ZQ | NC | | H |
| P | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | J |
| R | | VDD | A3 | A0 | | | | A12/BC# | BA1 | VDD | | K |
| T | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | L |
| U | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | M |
| V | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | N |
| W | | | | | | | | | | | | |
| Y | | | | | | | | | | | | |
| AA | NC | NC | | NC | | | | NC | | NC | NC | |
| AB | | | | | | | | | | | | |
| AC | NC | NC | | NC | | | | NC | | NC | NC | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

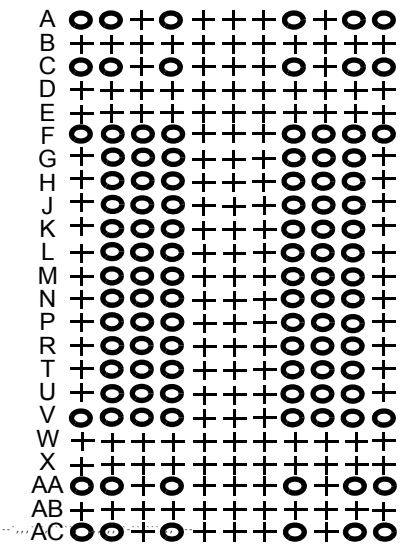
**Note1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

MO-207 Variation DT-z (x4)




**Populated ball**
**Ball not populated**

MO-207 Variation DW-z (x4) with support balls




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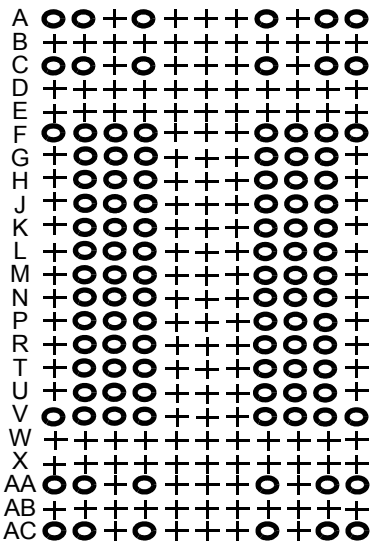
**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

## 2.2 DDR3 SDRAM x8 Ballout using MO-207 (Top view: see balls through package)

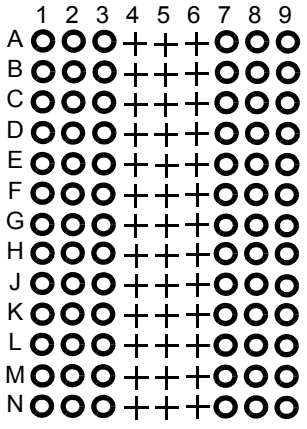
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | A |
| B | | | | | | | | | | | | B |
| C | NC | NC | | NC | | | | NC | | NC | NC | C |
| D | | | | | | | | | | | | D |
| E | | | | | | | | | | | | E |
| F | NC | VSS | VDD | NC | | | | NU/TDQS# | VSS | VDD | NC | F |
| G | | VSS | VSSQ | DQ0 | | | | DM/TDQS | VSSQ | VDDQ | | G |
| H | | VDDQ | DQ2 | DQS | | | | DQ1 | DQ3 | VSSQ | | H |
| J | | VSSQ | DQ6 | DQS# | | | | VDD | VSS | VSSQ | | J |
| K | | VREFDQ | VDDQ | DQ4 | | | | DQ7 | DQ5 | VDDQ | | K |
| L | | NC | VSS | RAS# | | | | CK | VSS | NC | | L |
| M | | ODT | VDD | CAS# | | | | CK# | VDD | CKE | | M |
| N | | NC | CS# | WE# | | | | A10/AP | ZQ | NC | | N |
| P | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | P |
| R | | VDD | A3 | A0 | | | | A12/BC# | BA1 | VDD | | R |
| T | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | T |
| U | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | U |
| V | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | V |
| W | | | | | | | | | | | | W |
| Y | | | | | | | | | | | | Y |
| AA | NC | NC | | NC | | | | NC | | NC | NC | AA |
| AB | | | | | | | | | | | | AB |
| AC | NC | NC | | NC | | | | NC | | NC | NC | AC |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

**Note1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

MO-207 Variation DW-z (x8)
with support balls




MO-207 Variation DT-z (x8)




**O Populated ball**
**+ Ball not populated**

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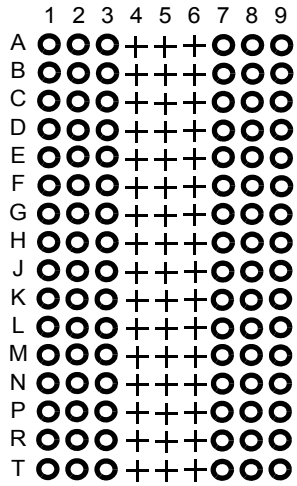
**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

## 2.3 DDR3 SDRAM x16 Ballout using MO-207 (Top view: see balls through package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | A |
| B | | | | | | | | | | | | B |
| C | | | | | | | | | | | | C |
| D | NC | VDDQ | DQU5 | DQU7 | | | | DQU4 | VDDQ | VSS | NC | D |
| E | | VSSQ | VDD | VSS | | | | DQSU# | DQU6 | VSSQ | | E |
| F | | VDDQ | DQU3 | DQU1 | | | | DQSU | DQU2 | VDDQ | | F |
| G | | VSSQ | VDDQ | DMU | | | | DQU0 | VSSQ | VDD | | G |
| H | | VSS | VSSQ | DQL0 | | | | DML | VSSQ | VDDQ | | H |
| J | | VDDQ | DQL2 | DQSL | | | | DQL1 | DQL3 | VSSQ | | J |
| K | | VSSQ | DQL6 | DQSL# | | | | VDD | VSS | VSSQ | | K |
| L | | VREFDQ | VDDQ | DQL4 | | | | DQL7 | DQL5 | VDDQ | | L |
| M | | NC | VSS | RAS# | | | | CK | VSS | NC | | M |
| N | | ODT | VDD | CAS# | | | | CK# | VDD | CKE | | N |
| P | | NC | CS# | WE# | | | | A10/AP | ZQ | NC | | P |
| R | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | R |
| T | | VDD | A3 | A0 | | | | A12 | BA1 | VDD | | T |
| U | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | U |
| V | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | V |
| W | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | W |
| Y | | | | | | | | | | | | Y |
| AA | | | | | | | | | | | | AA |
| AB | NC | NC | | NC | | | | NC | | NC | NC | AB |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

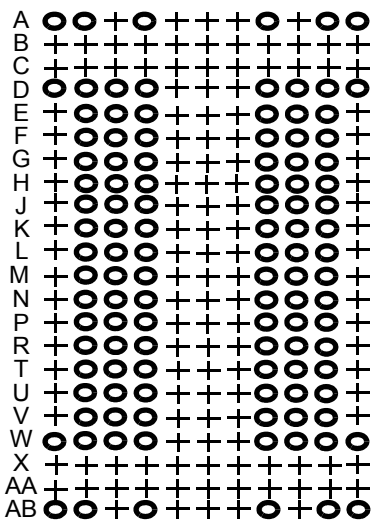
**Note1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

MO - 207 Variation DU-z (x16)




**O Populated ball**
**+ Ball not populated**

MO-207 Variation TBD (x16)
with support balls




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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

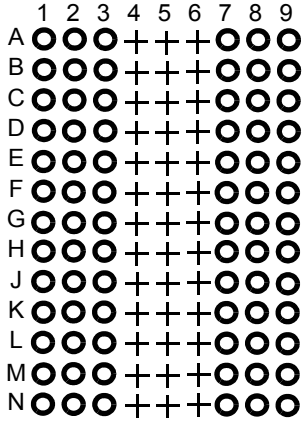
## 2.4 Stacked / dual-die DDR3 SDRAM x4 Ballout using MO-207 (Top view: see balls through package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | A |
| B | | | | | | | | | | | | B |
| C | NC | NC | | NC | | | | NC | | NC | NC | C |
| D | | | | | | | | | | | | D |
| E | | | | | | | | | | | | E |
| F | NC | VSS | VDD | NC | | | | NC | VSS | VDD | NC | F |
| G | | VSS | VSSQ | DQ0 | | | | DM | VSSQ | VDDQ | | G |
| H | | VDDQ | DQ2 | DQS | | | | DQ1 | DQ3 | VSSQ | | H |
| J | | VSSQ | NC | DQS# | | | | VDD | VSS | VSSQ | | J |
| K | | VREFDQ | VDDQ | NC | | | | NC | NC | VDDQ | | K |
| L | | ODT1 | VSS | RAS# | | | | CK | VSS | CKE1 | | L |
| M | | ODT0 | VDD | CAS# | | | | CK# | VDD | CKE0 | | M |
| N | | CS1# | CS0# | WE# | | | | A10/AP | ZQ0 | ZQ1 | | N |
| P | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | P |
| R | | VDD | A3 | A0 | | | | A12/BC# | BA1 | VDD | | R |
| T | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | T |
| U | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | U |
| V | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | V |
| W | | | | | | | | | | | | W |
| X | | | | | | | | | | | | X |
| AA | NC | NC | | NC | | | | NC | | NC | NC | AA |
| AB | | | | | | | | | | | | AB |
| AC | NC | NC | | NC | | | | NC | | NC | NC | AC |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

**Note1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

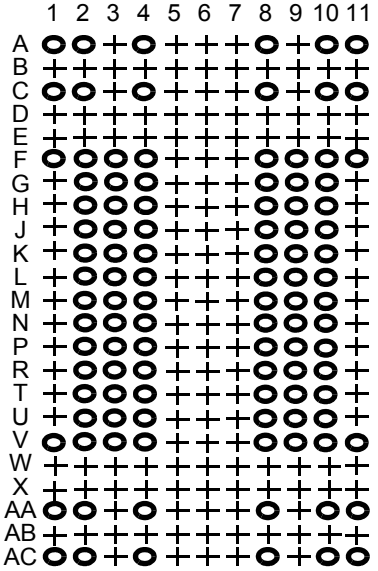
**Note2: This stacked ballout is intended to use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.**

MO-207 Variation DT-z (x4)




**O Populated ball**
**+ Ball not populated**

MO-207 Variation DW-z (x4) with support balls




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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

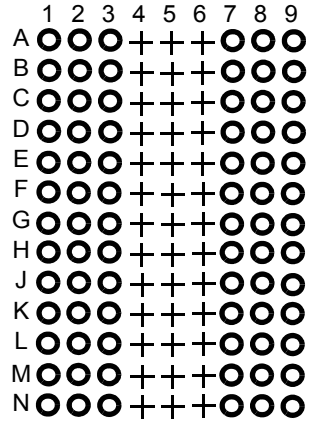
## 2.5 Stacked / dual-die DDR3 SDRAM x8 Ballout using MO-207 (Top view: see balls through package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | A |
| B | | | | | | | | | | | | B |
| C | NC | NC | | NC | | | | NC | | NC | NC | C |
| D | | | | | | | | | | | | D |
| E | | | | | | | | | | | | E |
| F | NC | VSS | VDD | NC | | | | NU/TDQS# | VSS | VDD | NC | F |
| G | | VSS | VSSQ | DQ0 | | | | DM/TDQS | VSSQ | VDDQ | | G |
| H | | VDDQ | DQ2 | DQS | | | | DQ1 | DQ3 | VSSQ | | H |
| J | | VSSQ | DQ6 | DQS# | | | | VDD | VSS | VSSQ | | J |
| K | | VREFDQ | VDDQ | DQ4 | | | | DQ7 | DQ5 | VDDQ | | K |
| L | | ODT1 | VSS | RAS# | | | | CK | VSS | CKE1 | | L |
| M | | ODT0 | VDD | CAS# | | | | CK# | VDD | CKE0 | | M |
| N | | CS1# | CS0# | WE# | | | | A10/AP | ZQ0 | ZQ1 | | N |
| P | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | P |
| R | | VDD | A3 | A0 | | | | A12/BC# | BA1 | VDD | | R |
| T | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | T |
| U | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | U |
| V | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | V |
| W | | | | | | | | | | | | W |
| X | | | | | | | | | | | | X |
| AA | NC | NC | | NC | | | | NC | | NC | NC | AA |
| AB | | | | | | | | | | | | AB |
| AC | NC | NC | | NC | | | | NC | | NC | NC | AC |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

**Note1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

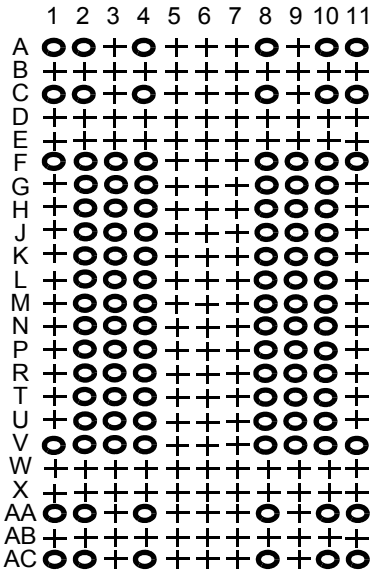
**Note2: This stacked ballout is intended to use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.**

MO-207 Variation DT-z (x8)




**O Populated ball**
**+ Ball not populated**

**MO - 207 Variation DW-z (x8) with support balls**




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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

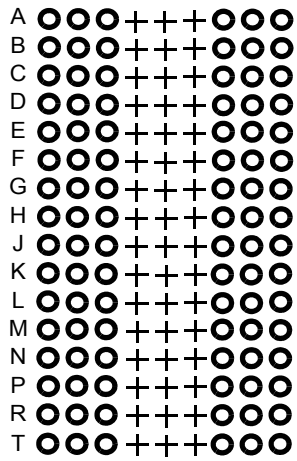
## 2.6 Stacked / dual-die DDR3 SDRAM x16 Ballout using MO-207 (Top view: see balls through package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | NC | | | | NC | | NC | NC | |
| B | | | | | | | | | | | | |
| C | | | | | | | | | | | | |
| D | NC | VDDQ | DQU5 | DQU7 | | | | DQU4 | VDDQ | VSS | NC | A |
| E | | VSSQ | VDD | VSS | | | | DQSU# | DQU6 | VSSQ | | B |
| F | | VDDQ | DQU3 | DQU1 | | | | DQSU | DQU2 | VDDQ | | C |
| G | | VSSQ | VDDQ | DMU | | | | DQU0 | VSSQ | VDD | | D |
| H | | VSS | VSSQ | DQL0 | | | | DML | VSSQ | VDDQ | | E |
| J | | VDDQ | DQL2 | DQSL | | | | DQL1 | DQL3 | VSSQ | | F |
| K | | VSSQ | DQL6 | DQSL# | | | | VDD | VSS | VSSQ | | G |
| L | | VREFDQ | VDDQ | DQL4 | | | | DQL7 | DQL5 | VDDQ | | H |
| M | | ODT1 | VSS | RAS# | | | | CK | VSS | CKE1 | | J |
| N | | ODT0 | VDD | CAS# | | | | CK# | VDD | CKE0 | | K |
| P | | CS1# | CS0# | WE# | | | | A10/AP | ZQ0 | ZQ1 | | L |
| R | | VSS | BA0 | BA2 | | | | A15 | VREFCA | VSS | | M |
| T | | VDD | A3 | A0 | | | | A12 | BA1 | VDD | | N |
| U | | VSS | A5 | A2 | | | | A1 | A4 | VSS | | P |
| V | | VDD | A7 | A9 | | | | A11 | A6 | VDD | | R |
| W | NC | VSS | RESET# | A13 | | | | A14 | A8 | VSS | NC | T |
| Y | | | | | | | | | | | | |
| AA | | | | | | | | | | | | |
| AB | NC | NC | | NC | | | | NC | | NC | NC | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |

**te1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball.**

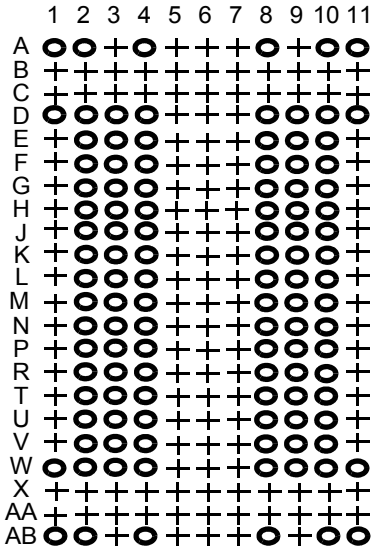
**te2: This stacked ballout is intended to use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.**

MO - 207 Variation DU-z (x16)




**O Populated ball**
**+ Ball not populated**

MO - 207 Variation TBD
(x16) with support balls




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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

## 2.7 Pinout Description

### Table 1 — Input / output functional description

| Symbol | Type | Function |
|---|---|---|
| CK, CK# | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. |
| CKE, (CKE0), (CKE1) | Input | Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CS#, (CS0#), (CS1#) | Input | Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code. |
| ODT, (ODT0), (ODT1) | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT. |
| RAS#. CAS#. WE# | Input | Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered. |
| DM, (DMU), (DML) | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1. |
| BA0 - BA2 | Input | Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A15 | Input | Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions, see below).The address inputs also provide the op-code during Mode Register Set commands. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC# | Input | Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| RESET# | Input | Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of $V_{DD}$, i.e. 1.20V for DC high and 0.30V for DC low. |
| DQ | Input / Output | Data Input/ Output: Bi-directional data bus. |

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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**
**2.7 Pinout Description (Cont'd)**

## Table 1 — Input / output functional description

| Symbol | Type | Function |
|---|---|---|
| DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL# | Input / Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended. |
| TDQS, TDQS# | Output | Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1. |
| NC | | No Connect: No internal electrical connection is present. |
| $V_{DDQ}$ | Supply | DQ Power Supply: 1.5 V +/- 0.075 V |
| $V_{SSQ}$ | Supply | DQ Ground |
| $V_{DD}$ | Supply | Power Supply: 1.5 V +/- 0.075 V |
| $V_{SS}$ | Supply | Ground |
| $V_{REFDQ}$ | Supply | Reference voltage for DQ |
| $V_{REFCA}$ | Supply | Reference voltage |
| ZQ, (ZQ0), (ZQ1) | Supply | Reference Pin for ZQ calibration |
| Note: Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination. | | |

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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**

## 2.8 DDR3 SDRAM Addressing

### 2.8.1 512Mb

| Configuration | 128Mb x 4 | 64Mb x 8 | 32Mb x 16 |
|---|---|---|---|
| # of Banks | 8 | 8 | 8 |
| Bank Address | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| Auto precharge | A10/AP | A10/AP | A10/AP |
| BC switch on the fly | A12/BC# | A12/BC# | A12/BC# |
| Row Address | A0 - A12 | A0 - A12 | A0 - A11 |
| Column Address | A0 - A9,A11 | A0 - A9 | A0 - A9 |
| Page size [1] | 1 KB | 1 KB | 2 KB |

### 2.8.2 1Gb

| Configuration | 256Mb x 4 | 128Mb x 8 | 64Mb x 16 |
|---|---|---|---|
| # of Banks | 8 | 8 | 8 |
| Bank Address | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| Auto precharge | A10/AP | A10/AP | A10/AP |
| BC switch on the fly | A12/BC# | A12/BC# | A12/BC# |
| Row Address | A0 - A13 | A0 - A13 | A0 - A12 |
| Column Address | A0 - A9,A11 | A0 - A9 | A0 - A9 |
| Page size [1] | 1 KB | 1 KB | 2 KB |

### 2.8.3 2Gb

| Configuration | 512Mb x 4 | 256Mb x 8 | 128Mb x 16 |
|---|---|---|---|
| # of Banks | 8 | 8 | 8 |
| Bank Address | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| Auto precharge | A10/AP | A10/AP | A10/AP |
| BC switch on the fly | A12/BC# | A12/BC# | A12/BC# |
| Row Address | A0 - A14 | A0 - A14 | A0 - A13 |
| Column Address | A0 - A9,A11 | A0 - A9 | A0 - A9 |
| Page size [1] | 1 KB | 1 KB | 2 KB |

### 2.8.4 4Gb

| Configuration | 1Gb x 4 | 512Mb x 8 | 256Mb x 16 |
|---|---|---|---|
| # of Banks | 8 | 8 | 8 |
| Bank Address | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| Auto precharge | A10/AP | A10/AP | A10/AP |
| BC switch on the fly | A12/BC# | A12/BC# | A12/BC# |
| Row Address | A0 - A15 | A0 - A15 | A0 - A14 |
| Column Address | A0 - A9,A11 | A0 - A9 | A0 - A9 |
| Page size [1] | 1 KB | 1 KB | 2 KB |

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**2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**
**2.8 DDR3 SDRAM Addressing (Cont'd)**

### 2.8.5 8Gb

| Configuration | 2Gb x 4 | 1Gb x 8 | 512Mb x 16 |
|---|---|---|---|
| # of Banks | 8 | 8 | 8 |
| Bank Address | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| Auto precharge | $A_{10}$/AP | $A_{10}$/AP | $A_{10}$/AP |
| BC switch on the fly | $A_{12}$/BC# | $A_{12}$/BC# | $A_{12}$/BC# |
| Row Address | $A_0$ - $A_{15}$ | $A_0$ - $A_{15}$ | $A_0$ - $A_{15}$ |
| Column Address | $A_0$ - $A_9$, $A_{11}$, $A_{13}$ | $A_0$ - $A_9$, $A_{11}$ | $A_0$ - $A_9$ |
| Page size [1] | 2 KB | 2 KB | 2 KB |

Notes: 1. Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS} * ORG \div 8$

where

COLBITS = the number of column address bits

ORG = the number of I/O (DQ) bits

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# 3 Functional Description

## 3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

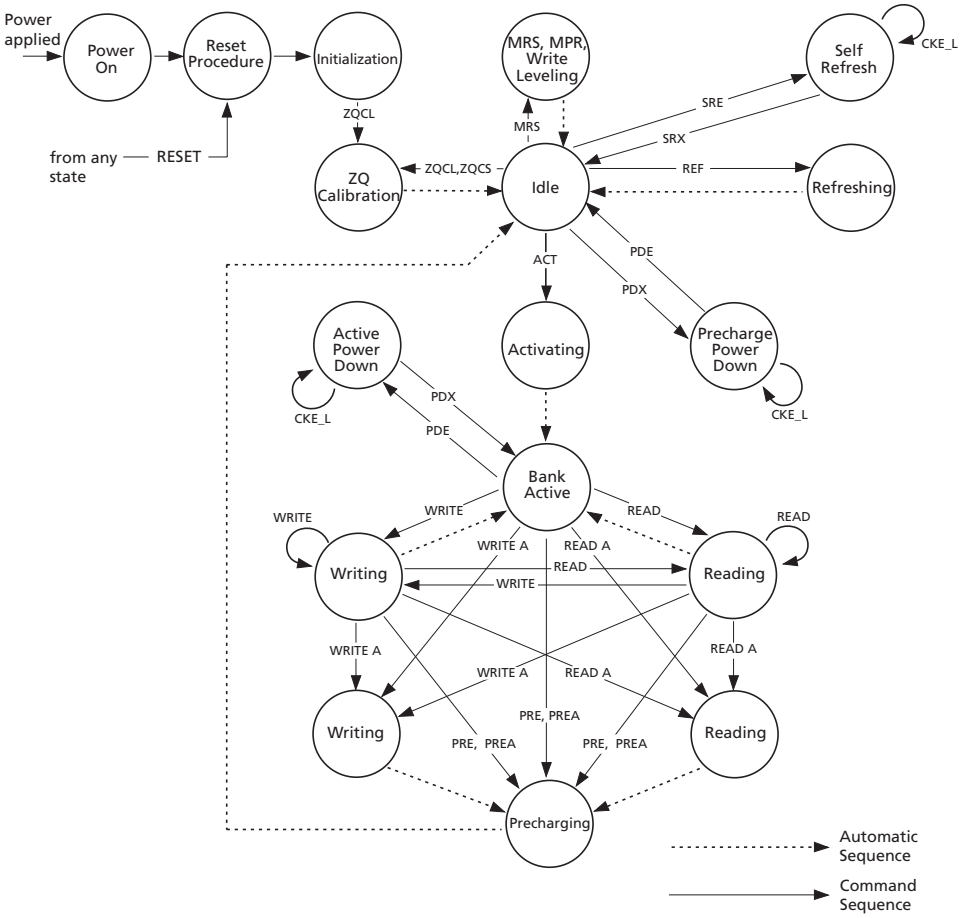



**Figure 1 — Simplified State Diagram**

**Table 2 — State Diagram Command Definitions**

| Abbreviation | Function | Abbreviation | Function | Abbreviation | Function |
|---|---|---|---|---|---|
| ACT | Active | Read | RD, RDS4, RDS8 | PDE | Enter Power-down |
| PRE | Precharge | Read A | RDA, RDAS4, RDAS8 | PDX | Exit Power-down |
| PREA | Precharge All | Write | WR, WRS4, WRS8 | SRE | Self-Refresh entry |
| MRS | Mode Register Set | Write A | WRA, WRAS4, WRAS8 | SRX | Self-Refresh exit |
| REF | Refresh | RESET | Start RESET Procedure | MPR | Multi-Purpose Register |
| ZQCL | ZQ Calibration Long | ZQCS | ZQ Calibration Short | - | - |
| **Note:** See “Command Truth Table” on page 29 for more details. | | | | | |

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## 3.2 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" on page 11 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

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**3 Functional Description (Cont'd)**

## 3.3 RESET and Initialization Procedure

### 3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD, (all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.

    - VDD and VDDQ are driven from a single power converter output, AND
    - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
    - Vref tracks VDDQ/2.

    OR

    - Apply VDD without any slope reversal before or at the same time as VDDQ.
    - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
    - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be meet. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.

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### 3.3 RESET and Initialization Procedure (Cont'd)
### 3.3.1 Power-up Initialization Sequence (Cont'd)

11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

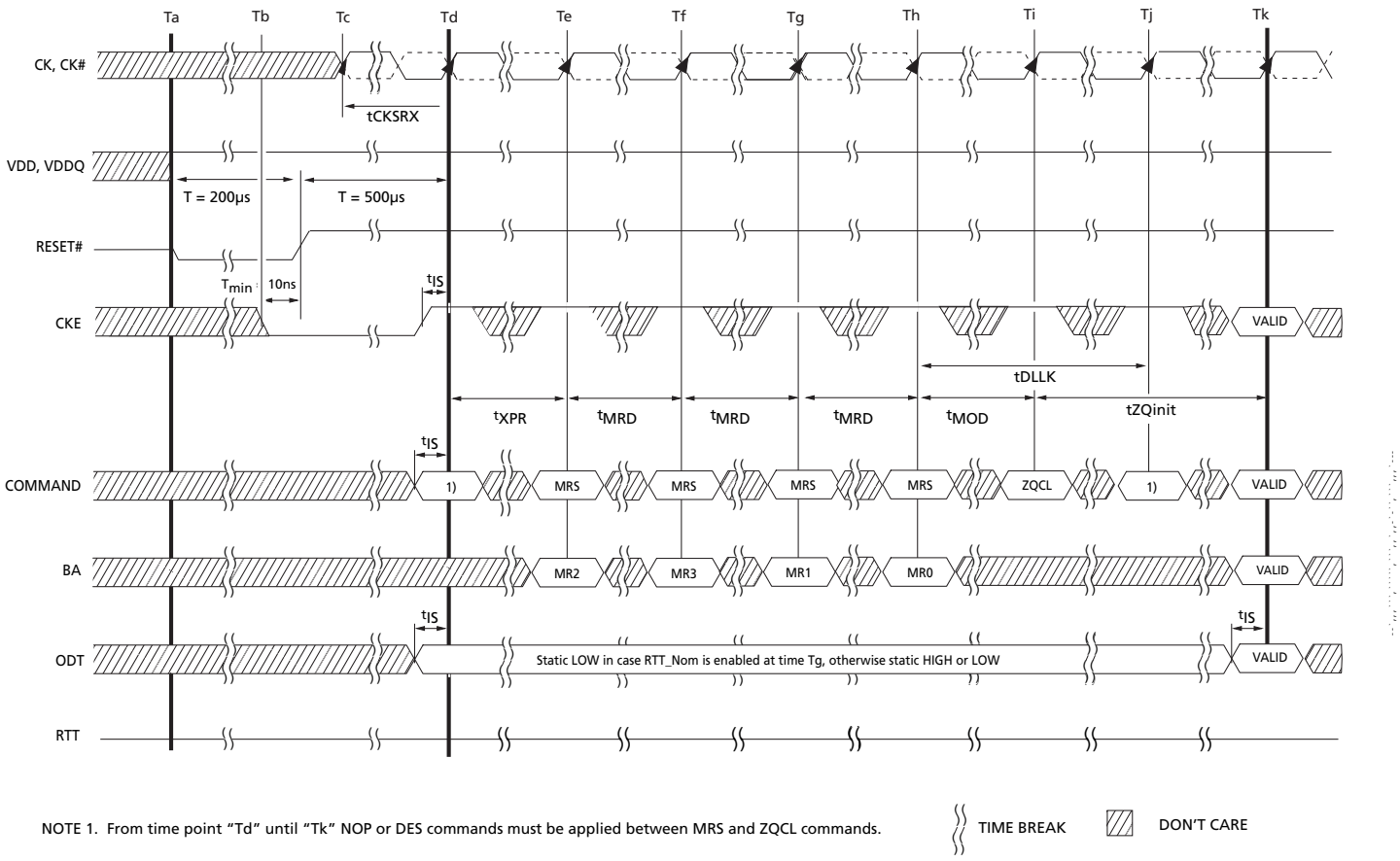



**Figure 2 — Reset and Initialization Sequence at Power-on Ramping**

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**3 Functional Description (Cont'd)**
**3.3 RESET and Initialization Procedure (Cont'd)**

### 3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed, DDR3 SDRAM is ready for normal operation.

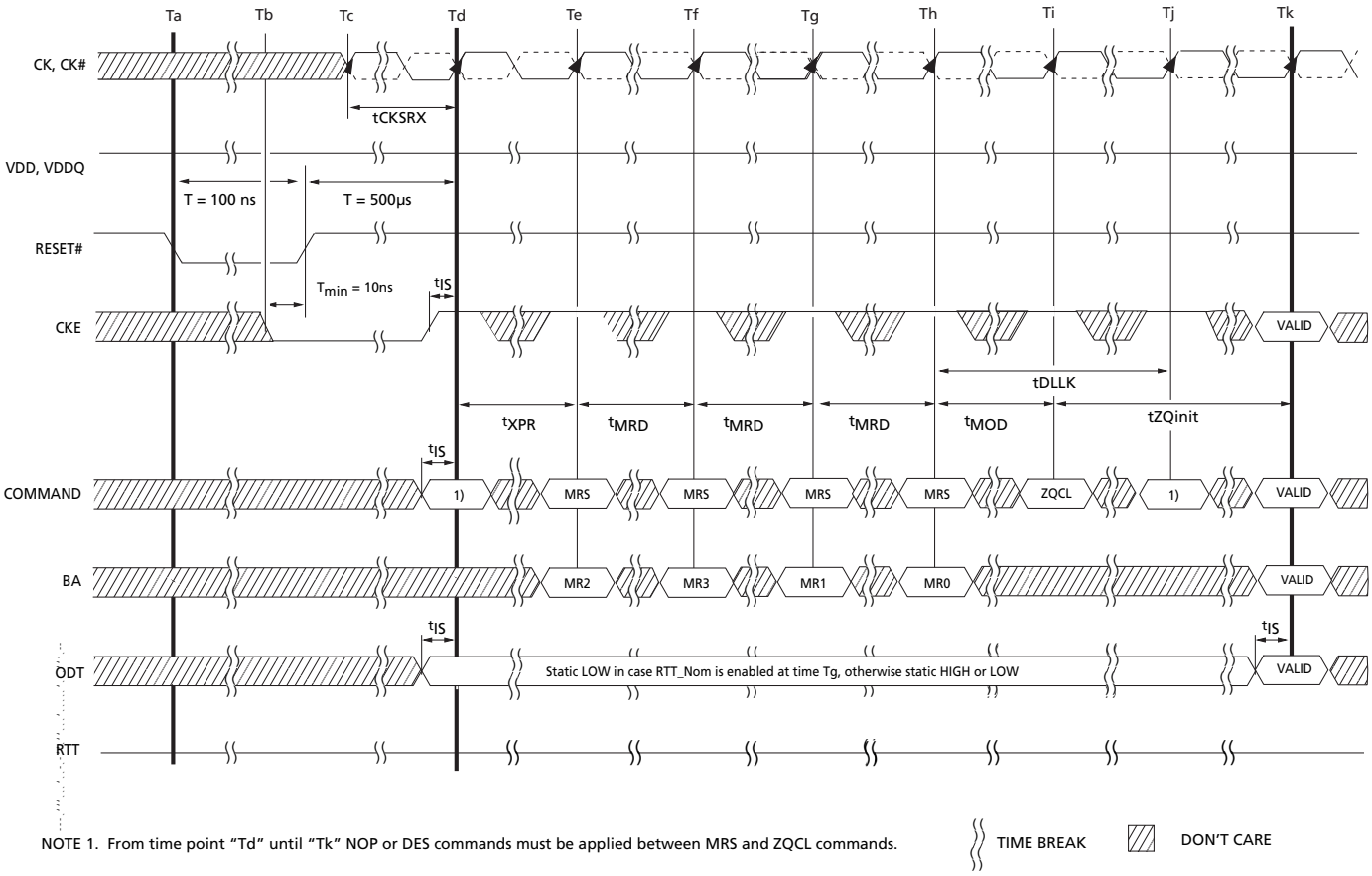



**Figure 3 — Reset Procedure at Power Stable Condition**

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## 3.4 Register Definition

### 3.4.1 Programming the Mode Registers

For application flexibility, various functions, features and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 4.

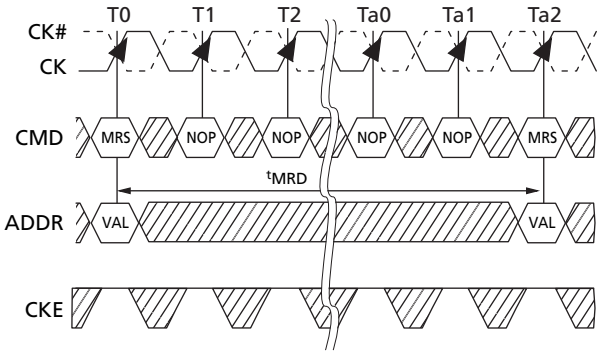



**Figure 4 — tMRD Timing**

The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 5.

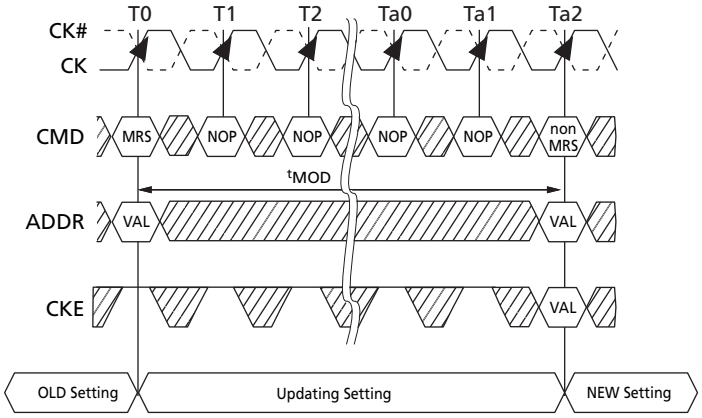



**Figure 5 — tMOD Timing**

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

### 3.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge

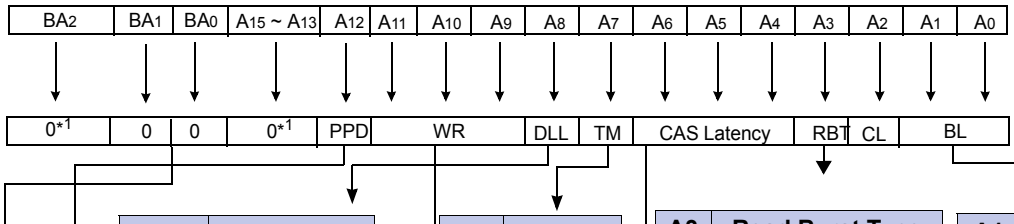
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### 3.4 Register Definition (Cont'd)
### 3.4.2 Mode Register MR0 (Cont'd)

Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to Figure 6.




| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A7 | mode |
|---|---|
| 0 | Normal |
| 1 | Test |

| A3 | Read Burst Type |
|---|---|
| 0 | Nibble Sequential |
| 1 | Interleave |

| A1 | A0 | BL |
|---|---|---|
| 0 | 0 | 8 (Fixed) |
| 0 | 1 | BC4 or 8(on the fly) |
| 1 | 0 | BC4 (Fixed) |
| 1 | 1 | Reserved |

| A12 | DLL Control for Precharge PD |
|---|---|
| 0 | Slow exit (DLL off) |
| 1 | Fast exit (DLL on) |

Write recovery for autoprecharge

| A11 | A10 | A9 | WR(cycles) |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 5*2 |
| 0 | 1 | 0 | 6*2 |
| 0 | 1 | 1 | 7*2 |
| 1 | 0 | 0 | 8*2 |
| 1 | 0 | 1 | 10*2 |
| 1 | 1 | 0 | 12*2 |
| 1 | 1 | 1 | Reserved |

| A6 | A5 | A4 | A2 | CAS Latency |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 1 | 0 | 9 |
| 1 | 1 | 0 | 0 | 10 |
| 1 | 1 | 1 | 0 | 11(Optional for DDR3-1600) |

| BA1 | BA0 | MR Select |
|---|---|---|
| 0 | 0 | MR0 |
| 0 | 1 | MR1 |
| 1 | 0 | MR2 |
| 1 | 1 | MR3 |

*1 : BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.
*2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

**Figure 6 — MR0 Definition**

#### 3.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 6. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 3. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

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**3.4 Register Definition (Cont'd)**
**3.4.2 Mode Register MR0 (Cont'd)**

## Table 3 — Burst Type and Burst Order

| Burst Length | READ/ WRITE | Starting Column ADDRESS (A2,A1,A0) | burst type = Sequential (decimal) A3 = 0 | burst type = Interleaved (decimal) A3 = 1 | Notes |
|---|---|---|---|---|---|
| 4 Chop | READ | 0 0 0 | 0,1,2,3,T,T,T,T | 0,1,2,3,T,T,T,T | 1, 2, 3 |
| | | 0 0 1 | 1,2,3,0,T,T,T,T | 1,0,3,2,T,T,T,T | 1, 2, 3 |
| | | 0 1 0 | 2,3,0,1,T,T,T,T | 2,3,0,1,T,T,T,T | 1, 2, 3 |
| | | 0 1 1 | 3,0,1,2,T,T,T,T | 3,2,1,0,T,T,T,T | 1, 2, 3 |
| | | 1 0 0 | 4,5,6,7,T,T,T,T | 4,5,6,7,T,T,T,T | 1, 2, 3 |
| | | 1 0 1 | 5,6,7,4,T,T,T,T | 5,4,7,6,T,T,T,T | 1, 2, 3 |
| | | 1 1 0 | 6,7,4,5,T,T,T,T | 6,7,4,5,T,T,T,T | 1, 2, 3 |
| | | 1 1 1 | 7,4,5,6,T,T,T,T | 7,6,5,4,T,T,T,T | 1, 2, 3 |
| | WRITE | 0,V,V | 0,1,2,3,X,X,X,X | 0,1,2,3,X,X,X,X | 1, 2, 4, 5 |
| | | 1,V,V | 4,5,6,7,X,X,X,X | 4,5,6,7,X,X,X,X | 1, 2, 4, 5 |
| 8 | READ | 0 0 0 | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 2 |
| | | 0 0 1 | 1,2,3,0,5,6,7,4 | 1,0,3,2,5,4,7,6 | 2 |
| | | 0 1 0 | 2,3,0,1,6,7,4,5 | 2,3,0,1,6,7,4,5 | 2 |
| | | 0 1 1 | 3,0,1,2,7,4,5,6 | 3,2,1,0,7,6,5,4 | 2 |
| | | 1 0 0 | 4,5,6,7,0,1,2,3 | 4,5,6,7,0,1,2,3 | 2 |
| | | 1 0 1 | 5,6,7,4,1,2,3,0 | 5,4,7,6,1,0,3,2 | 2 |
| | | 1 1 0 | 6,7,4,5,2,3,0,1 | 6,7,4,5,2,3,0,1 | 2 |
| | | 1 1 1 | 7,4,5,6,3,0,1,2 | 7,6,5,4,3,2,1,0 | 2 |
| | WRITE | V,V,V | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 2, 4 |

Notes:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

#### 3.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 6. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page 144. For detailed Read operation refer to "READ Operation" on page 52.

#### 3.4.2.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 6. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

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**3.4 Register Definition (Cont'd)**
**3.4.2 Mode Register MR0 (Cont'd)**

#### 3.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations).

#### 3.4.2.5 Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR(write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR(min).

#### 3.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

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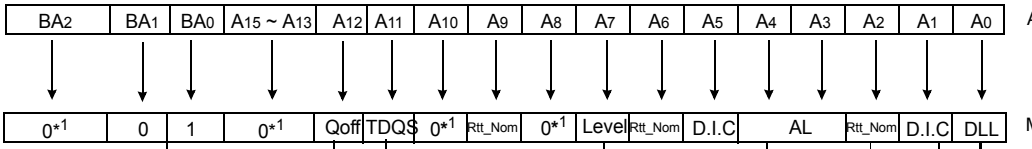
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**3 Functional Description (Cont'd)**
**3.4 Register Definition (Cont'd)**

### 3.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1and BA2, while controlling the states of address pins according to Figure 7.




| A11 | TDQS enable |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| A7 | Write leveling enable |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| A9 | A6 | A2 | Rtt_Nom*3 |
|---|---|---|---|
| 0 | 0 | 0 | Rtt_Nom disabled |
| 0 | 0 | 1 | RZQ/4 |
| 0 | 1 | 0 | RZQ/2 |
| 0 | 1 | 1 | RZQ/6 |
| 1 | 0 | 0 | RZQ/12*4 |
| 1 | 0 | 1 | RZQ/8*4 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Note: RZQ = 240 Ω**

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A4 | A3 | Additive Latency |
|---|---|---|
| 0 | 0 | 0 (AL disabled) |
| 0 | 1 | CL-1 |
| 1 | 0 | CL-2 |
| 1 | 1 | Reserved |

***3: In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.**

***4: If RTT_Nom is used during Writes, only the values RZQ/2,RZQ/4 and RZQ/6 are allowed.**

| A12 | Qoff *2 |
|---|---|
| 0 | Output buffer enabled |
| 1 | Output buffer disabled *2 |

***2: Outputs disabled - DQs, DQSs, DQS#s.**

| A5 | A1 | Output Driver Impedance Control |
|---|---|---|
| 0 | 0 | Reserved for RZQ/6 |
| 0 | 1 | RZQ/7 |
| 1 | 0 | RZQ/TBD |
| 1 | 1 | RZQ/TBD |

**Note: RZQ = 240 Ω**

| BA1 | BA0 | MR Select |
|---|---|---|
| 0 | 0 | MR0 |
| 0 | 1 | MR1 |
| 1 | 0 | MR2 |
| 1 | 1 | MR3 |

*** 1 : BA2 and A8, A10, and A13 ~ A15 are RFU and must be programmed to 0 during MRS.**

**Figure 7 — MR1 Definition**

#### 3.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with

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**3.4 Register Definition (Cont'd)**
**3.4.3 Mode Register MR1 (Cont'd)**

MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to "DLL-off Mode" on page 33.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

#### 3.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure .

#### 3.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A seperate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

#### 3.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table .

**Table 4 — Additive Latency (AL) Settings**

| A4 | A3 | AL |
|---|---|---|
| 0 | 0 | 0 (AL Disabled) |
| 0 | 1 | CL - 1 |
| 1 | 0 | CL - 2 |
| 1 | 1 | Reserved |

**Note:** AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

#### 3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 38 for more details.

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**3.4 Register Definition (Cont'd)**
**3.4.3 Mode Register MR1 (Cont'd)**

#### 3.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 7. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring module power for example. For normal operation, A12 should be set to '0'.

#### 3.4.3.7 TDQS, TDQS#

TDQS (Termination Data Strobe) is a feature of X8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/TDQS# pins that is applied to the DQS/DQS# pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. See Table 5 for details.

The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

**Table 5 — TDQS, TDQS# Function Matrix**

| MR1 (A11) | DM / TDQS | NU / TDQS |
|---|---|---|
| 0 (TDQS Disabled) | DM | Hi-Z |
| 1 (TDQS Enabled) | TDQS | TDQS# |

Notes:
1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.
3. TDQS function is only available for X8 DRAM and must be disabled for X4 and X16.

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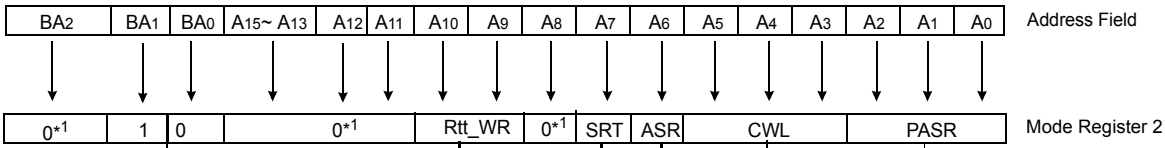
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**3 Functional Description (Cont'd)**
**3.4 Register Definition (Cont'd)**

### 3.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Programming




| A7 | Self-Refresh Temperature (SRT) Range |
|---|---|
| 0 | Normal operating temperature range |
| 1 | Extended (optional) operating temperature range |

| A6 | Auto Self-Refresh (ASR) |
|---|---|
| 0 | Manual SR Reference (SRT) |
| 1 | ASR enable (Optional) |

| A2 | A1 | A0 | Partial Array Self-Refresh (Optional) |
|---|---|---|---|
| 0 | 0 | 0 | Full Array |
| 0 | 0 | 1 | HalfArray (BA[2:0]=000,001,010, &011) |
| 0 | 1 | 0 | Quarter Array (BA[2:0]=000, & 001) |
| 0 | 1 | 1 | 1/8th Array (BA[2:0] = 000) |
| 1 | 0 | 0 | 3/4 Array (BA[2:0] = 010,011,100,101,110, & 111) |
| 1 | 0 | 1 | HalfArray (BA[2:0] = 100, 101, 110, &111) |
| 1 | 1 | 0 | Quarter Array (BA[2:0]=110, &111) |
| 1 | 1 | 1 | 1/8th Array (BA[2:0]=111) |

| A10 | A9 | Rtt_WR *2 |
|---|---|---|
| 0 | 0 | Dynamic ODT off (Write does not affect Rtt value) |
| 0 | 1 | RZQ/4 |
| 1 | 0 | RZQ/2 |
| 1 | 1 | Reserved |

| A5 | A4 | A3 | CAS write Latency (CWL) |
|---|---|---|---|
| 0 | 0 | 0 | 5 (tCK ≥2.5ns) |
| 0 | 0 | 1 | 6 (2.5ns >tCK≥1.875ns) |
| 0 | 1 | 0 | 7 (1.875ns>tCK≥1.5ns) |
| 0 | 1 | 1 | 8 (1.5ns>tCK≥1.25ns) |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| BA1 | BA0 | MR Select |
|---|---|---|
| 0 | 0 | MR0 |
| 0 | 1 | MR1 |
| 1 | 0 | MR2 |
| 1 | 1 | MR3 |

*** 1 : BA2, A5, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.**
*** 2 :** The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

**Figure 8 — MR2 Definition**

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**3.4 Register Definition (Cont'd)**
**3.4.4 Mode Register MR2 (Cont'd)**

#### 3.4.4.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 8 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

#### 3.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure . CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page 144. For detailed Write operation refer to "WRITE Operation" on page 62.

#### 3.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage" on page 42. DDR3 SDRAM's must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

#### 3.4.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT" on page 85.

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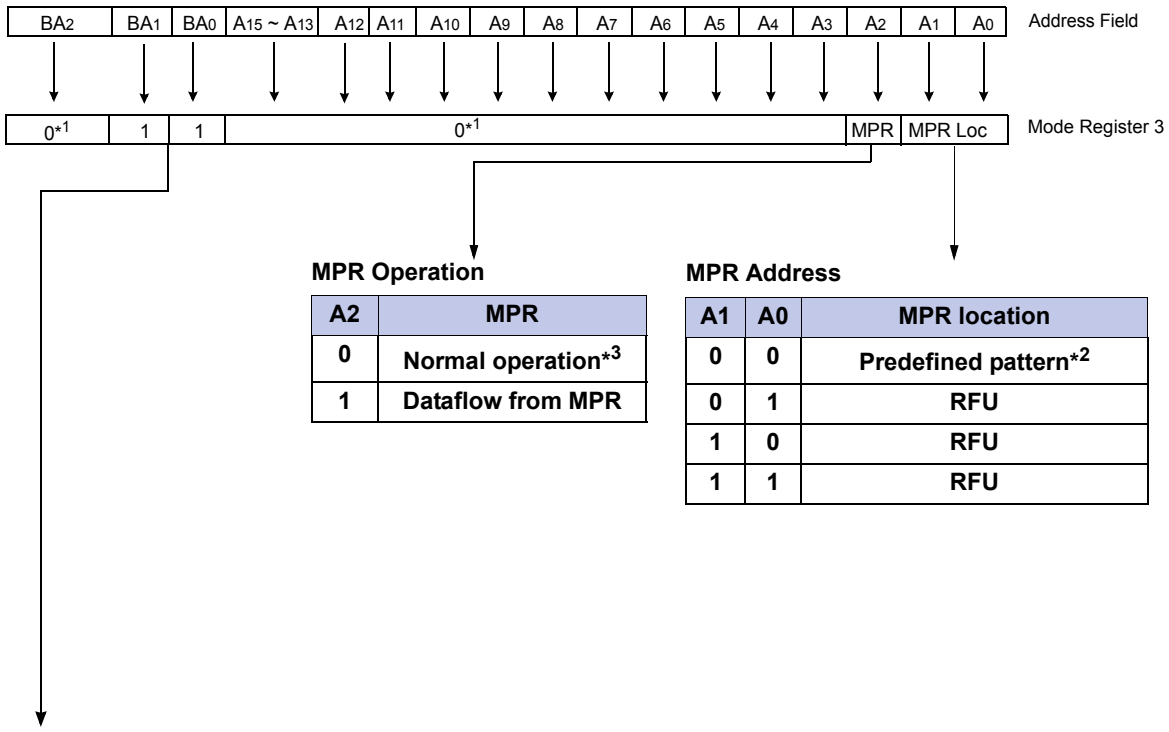
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**3 Functional Description (Cont'd)**
**3.4 Register Definition (Cont'd)**

### 3.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming




**MPR Operation**

| A2 | MPR |
|---|---|
| 0 | Normal operation*3 |
| 1 | Dataflow from MPR |

**MPR Address**

| A1 | A0 | MPR location |
|---|---|---|
| 0 | 0 | Predefined pattern*2 |
| 0 | 1 | RFU |
| 1 | 0 | RFU |
| 1 | 1 | RFU |

| BA1 | BA0 | MR Select |
|---|---|---|
| 0 | 0 | MR0 |
| 0 | 1 | MR1 |
| 1 | 0 | MR2 |
| 1 | 1 | MR3 |

*** 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.**
*** 2 : The predefined pattern will be used for read synchronization.**
*** 3 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.**

## Figure 9 — MR3 Definition

#### 3.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks pre-

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### 3.4 Register Definition (Cont'd)
### 3.4.5 Mode Register MR3 (Cont'd)

charged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to "Multi Purpose Register" on page 44.

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# 4 DDR3 SDRAM Command Description and Operation

## 4.1 Command Truth Table

**(a) note 1,2,3,4 apply to the entire Command Truth Table**

**(b) Note 5 applies to all Read/Write command**

**[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]**

**Table 6 — Command Truth Table**

| Function | Abbreviation | CKE | | CS# | RAS# | CAS# | WE# | BA0-BA3 | A13-A15 | A12-BC# | A10-AP | A0-A9, A11 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Previous Cycle | Current Cycle | | | | | | | | | | |
| Mode Register Set | MRS | H | H | L | L | L | L | BA | OP Code | | | | |
| Refresh | REF | H | H | L | L | L | H | V | V | V | V | V | |
| Self Refresh Entry | SRE | H | L | L | L | L | H | V | V | V | V | V | 7,9,12 |
| Self Refresh Exit | SRX | L | H | H | V | V | V | V | V | V | V | V | 7,8,9,12 |
| | | | | L | H | H | H | | | | | | |
| Single Bank Precharge | PRE | H | H | L | L | H | L | BA | V | V | L | V | |
| Precharge all Banks | PREA | H | H | L | L | H | L | V | V | V | H | V | |
| Bank Activate | ACT | H | H | L | L | H | H | BA | Row Address (RA) | | | | |
| Write (Fixed BL8 or BC4) | WR | H | H | L | H | L | L | BA | RFU | V | L | CA | |
| Write (BC4, on the Fly) | WRS4 | H | H | L | H | L | L | BA | RFU | L | L | CA | |
| Write (BL8, on the Fly) | WRS8 | H | H | L | H | L | L | BA | RFU | H | L | CA | |
| Write with Auto Precharge (Fixed BL8 or BC4) | WRA | H | H | L | H | L | L | BA | RFU | V | H | CA | |
| Write with Auto Precharge (BC4, on the Fly) | WRAS4 | H | H | L | H | L | L | BA | RFU | L | H | CA | |
| Write with Auto Precharge (BL8, on the Fly) | WRAS8 | H | H | L | H | L | L | BA | RFU | H | H | CA | |
| Read (Fixed BL8 or BC4) | RD | H | H | L | H | L | H | BA | RFU | V | L | CA | |
| Read (BC4, on the Fly | RDS4 | H | H | L | H | L | H | BA | RFU | L | L | CA | |
| Read (BL8, on the Fly) | RDS8 | H | H | L | H | L | H | BA | RFU | H | L | CA | |
| Read with Auto Precharge (Fixed BL8 or BC4) | RDA | H | H | L | H | L | H | BA | RFU | V | H | CA | |
| Read with Auto Precharge (BC4, on the Fly) | RDAS4 | H | H | L | H | L | H | BA | RFU | L | H | CA | |
| Read with Auto Precharge (BL8, on the Fly) | RDAS8 | H | H | L | H | L | H | BA | RFU | H | H | CA | |
| No Operation | NOP | H | H | L | H | H | H | V | V | V | V | V | 10 |
| Device Deselected | DES | H | H | H | X | X | X | X | X | X | X | X | 11 |
| Power Down Entry | PDE | H | L | L | H | H | H | V | V | V | V | V | 6,12 |
| | | | | H | V | V | V | | | | | | |
| Power Down Exit | PDX | L | H | L | H | H | H | V | V | V | V | V | 6,12 |
| | | | | H | V | V | V | | | | | | |
| ZQ Calibration Long | ZQCL | H | H | L | H | H | L | X | X | X | H | X | |

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## 4 DDR3 SDRAM Command Description and Operation (Cont'd)

### 4.1 Command Truth Table (Cont'd)

| Function | Abbreviation | CKE | | CS# | RAS# | CAS# | WE# | BA0-BA3 | A13-A15 | A12-BC# | A10-AP | A0-A9, A11 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Previous Cycle | Current Cycle | | | | | | | | | | |
| ZQ Calibration Short | ZQCS | H | H | L | H | H | L | X | X | X | L | X | |

Notes:
1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**

## 4.2 CKE Truth Table

### Table 7 — CKE Truth Table

a) Notes 1-7 apply to the entire CKE Truth Table.

b) For Power-down entry and exit parameters See 4.16 "Power-Down Modes" on page 72.

c) CKE low is allowed only if tMRD and tMOD are satisfied.

| Current State[2] | CKE | | Command (N)[3] RAS#, CAS#, WE#, CS# | Action (N)[3] | Notes |
|---|---|---|---|---|---|
| | Previous Cycle[1] (N-1) | Current Cycle[1] (N) | | | |
| Power-Down | L | L | X | Maintain Power-Down | 14, 15 |
| | L | H | DESELECT or NOP | Power-Down Exit | 11,14 |
| Self-Refresh | L | L | X | Maintain Self-Refresh | 15,16 |
| | L | H | DESELECT or NOP | Self-Refresh Exit | 8,12,16 |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power-Down Entry | 11,13,14 |
| Reading | H | L | DESELECT or NOP | Power-Down Entry | 11,13,14,17 |
| Writing | H | L | DESELECT or NOP | Power-Down Entry | 11,13,14,17 |
| Precharging | H | L | DESELECT or NOP | Power-Down Entry | 11,13,14,17 |
| Refreshing | H | L | DESELECT or NOP | Precharge Power-Down Entry | 11 |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power-Down Entry | 11,13,14,18 |
| | H | L | REFRESH | Self-Refresh | 9,13,18 |
| For more details with all signals See 4.1 "Command Truth Table" on page 29. | | | | | 10 |

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions **See 4.15 "Self-Refresh Operation" on page 70** and **See 4.16 "Power-Down Modes" on page 72**.
14. The Power-Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

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## 4.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

## 4.4 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**

## 4.5 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on page 36

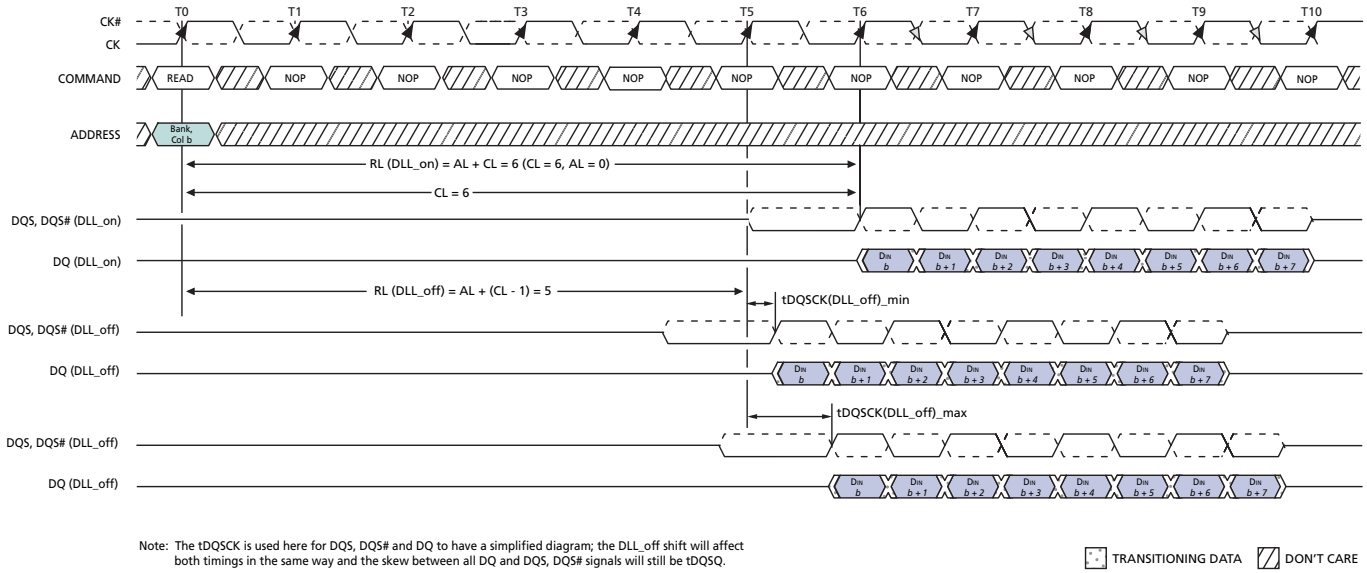
The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation have shown at following Timing Diagram (CL=6, BL=8):




Note: The tDQSCK is used here for DQS, DQS# and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, DQS# signals will still be tDQSQ.

**Figure 10 — DLL-off mode READ Timing Operation**

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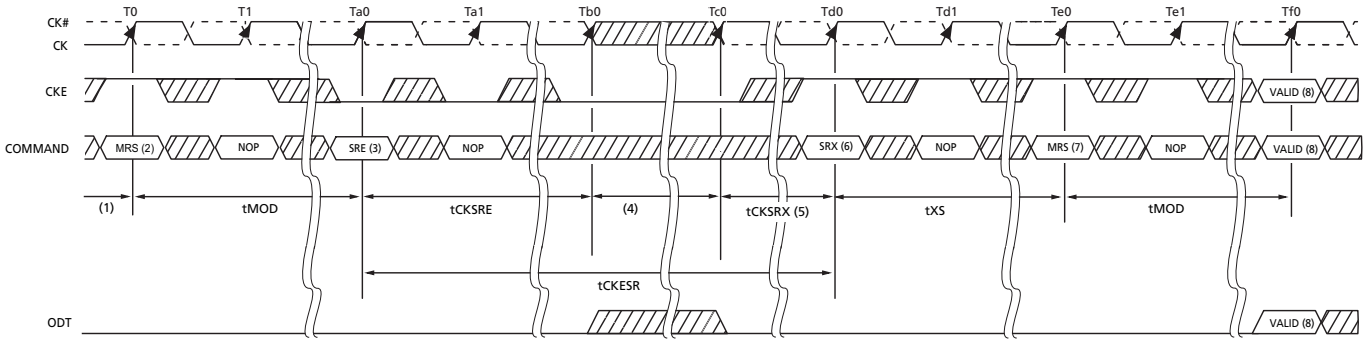
## 4.6 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0".

### 4.6.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with "Input clock frequency change" on page 36.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS)
9. Wait for tMOD, then DRAM is ready for next command.




ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High

NOTES:
1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR1 Bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

TIME BREAK  DON'T CARE

**Figure 11 — DLL Switch Sequence from DLL-on to DLL-off**

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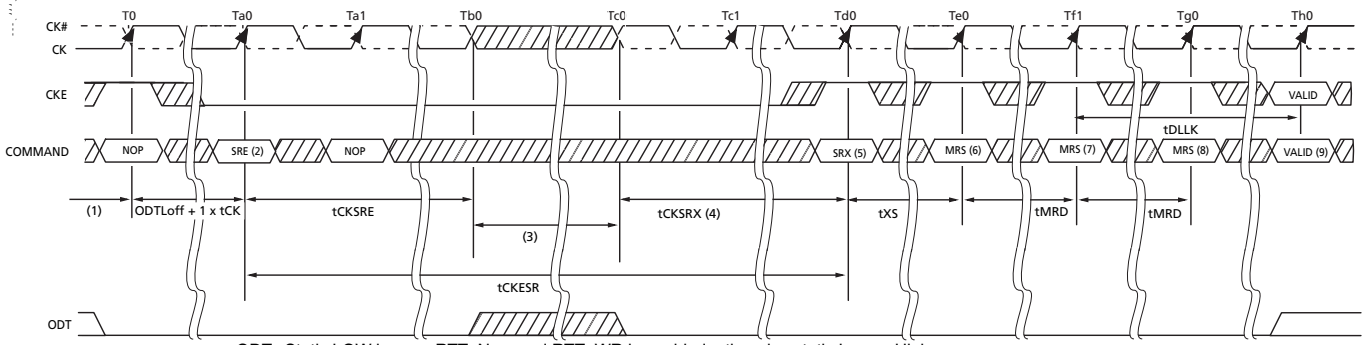
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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.6 DLL on/off switching procedure (Cont'd)**

### 4.6.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change" on page 36.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.




ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High

NOTES:
1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL on by MR1 A0=0
7. Update Mode registers
8. Any valid command

TIME BREAK  DON'T CARE

**Figure 12 — DLL Switch Sequence from DLL Off to DLL On**

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## 4.7 Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and $^{t}$CKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to $^{t}$CKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See 4.15 "Self-Refresh Operation" on page 70. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure" on page 34.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of $^{t}$CKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM $^{t}$CKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must

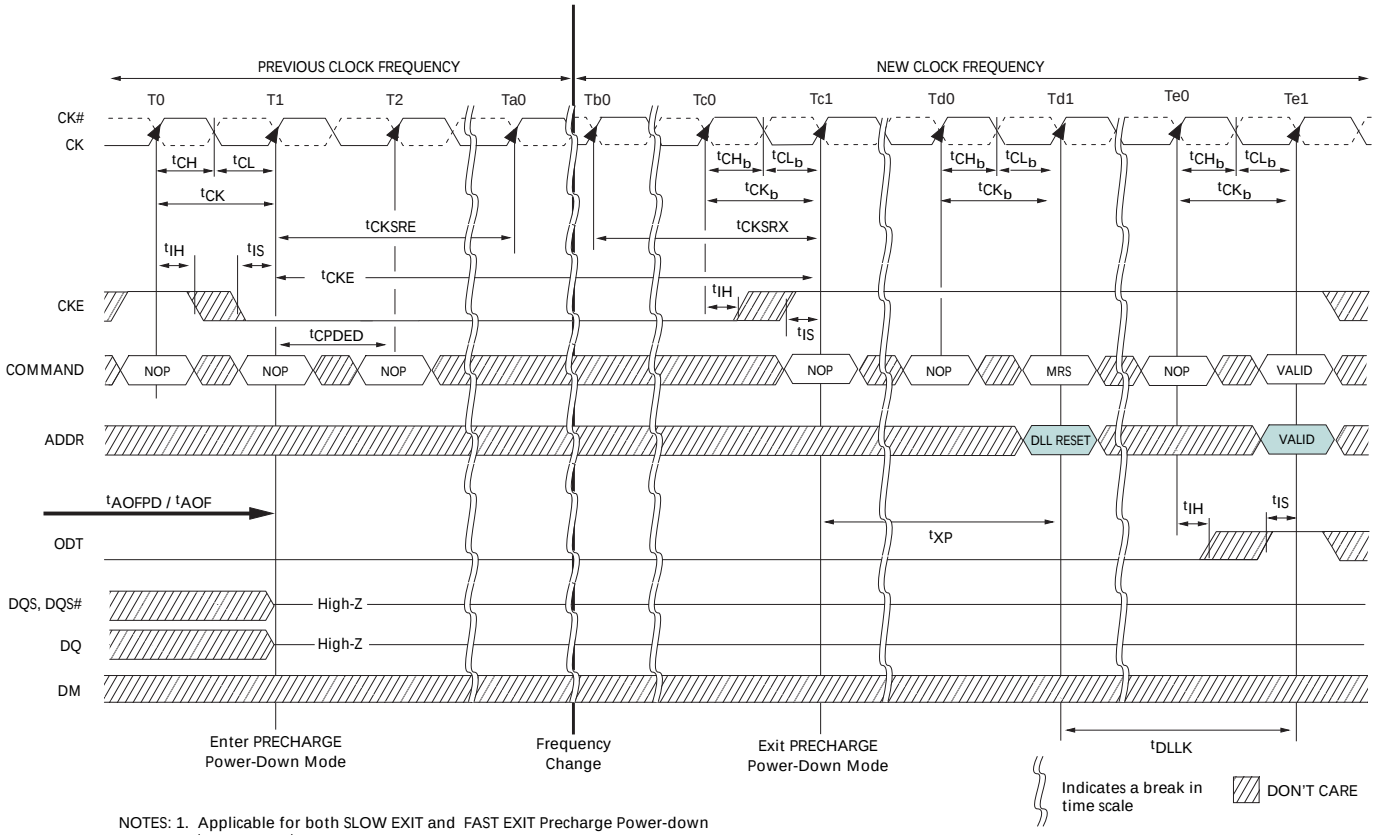
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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.7 Input clock frequency change (Cont'd)**

remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 13 on page 37.




NOTES: 1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
2. $^{t}$AOFPD and $^{t}$AOF must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 13. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

**Figure 13 — Change Frequency during Precharge Power-down**

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## 4.8 Write Leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limites provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 14.

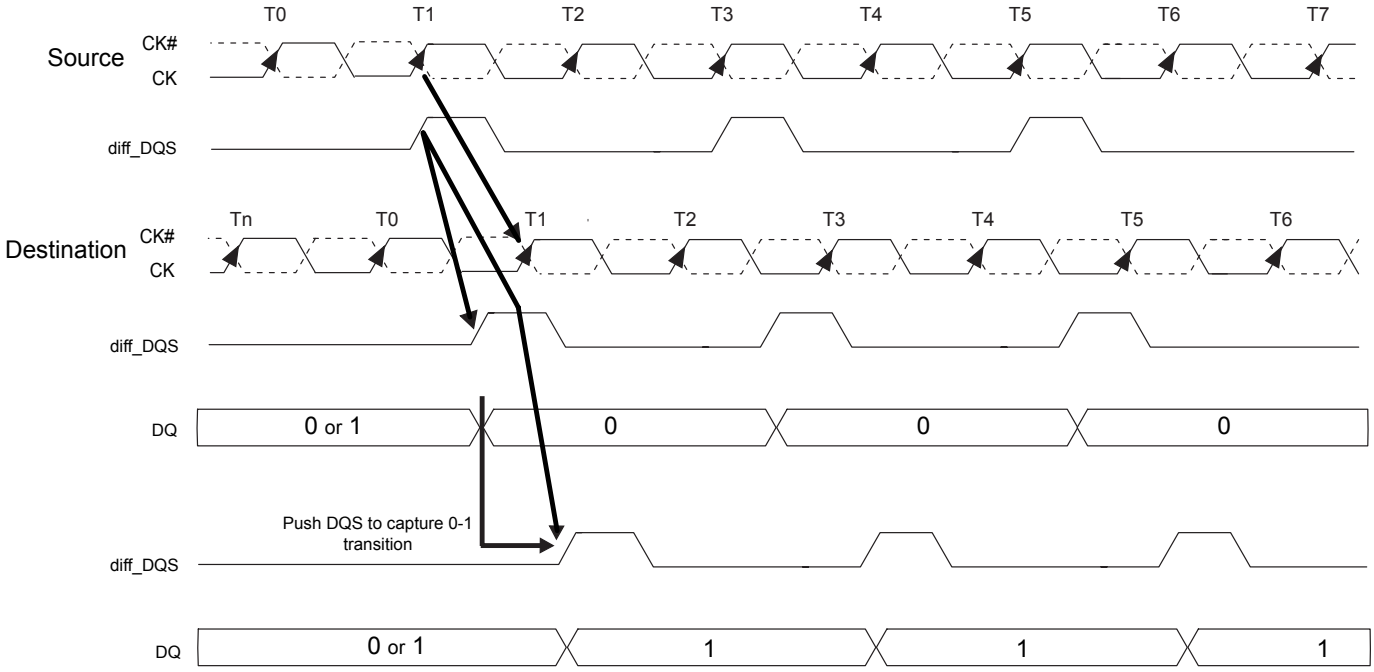



**Figure 14 — Write Leveling Concept**

DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

### 4.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 8). Note that in write leveling mode, only DQS/DQS# terminations are activated and deactivated via ODT pin not like normal operation (Table 9).

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**4.8 Write Leveling (Cont'd)**

**4.8.1 DRAM setting for write leveling & DRAM termination function in that mode (Cont'd)**

**Table 8 — MR setting involved in the leveling procedure**

| Function | MR1 | Enable | Disable |
|---|---|---|---|
| Write leveling enable | A7 | 1 | 0 |
| Output buffer mode (Qoff) | A12 | 0 | 1 |

**Table 9 — DRAM termination function in the leveling mode**

| ODT pin @DRAM | DQS/DQS# termination | DQs termination |
|---|---|---|
| De-asserted | Off | Off |
| Asserted | On | Off |

**Note:** In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

**4.8.2 Procedure Description**

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. tWLMRD(max) timing is controller dependent.

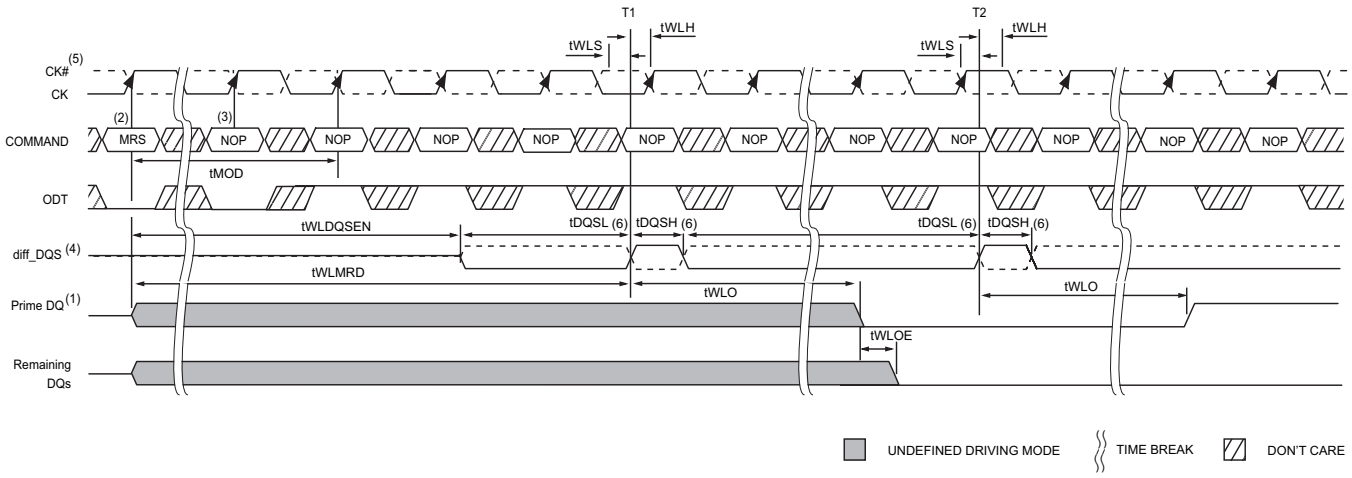
DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Figure 15 describes the timing diagram and parameters for the overall Write Leveling procedure.

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**4.8 Write Leveling (Cont'd)**
**4.8.2 Procedure Description (Cont'd)**




NOTES: 1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

**Figure 15 — Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2**

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.8 Write Leveling (Cont'd)**

### 4.8.3 Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1.After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).

2.Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).

3.After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).

4.After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

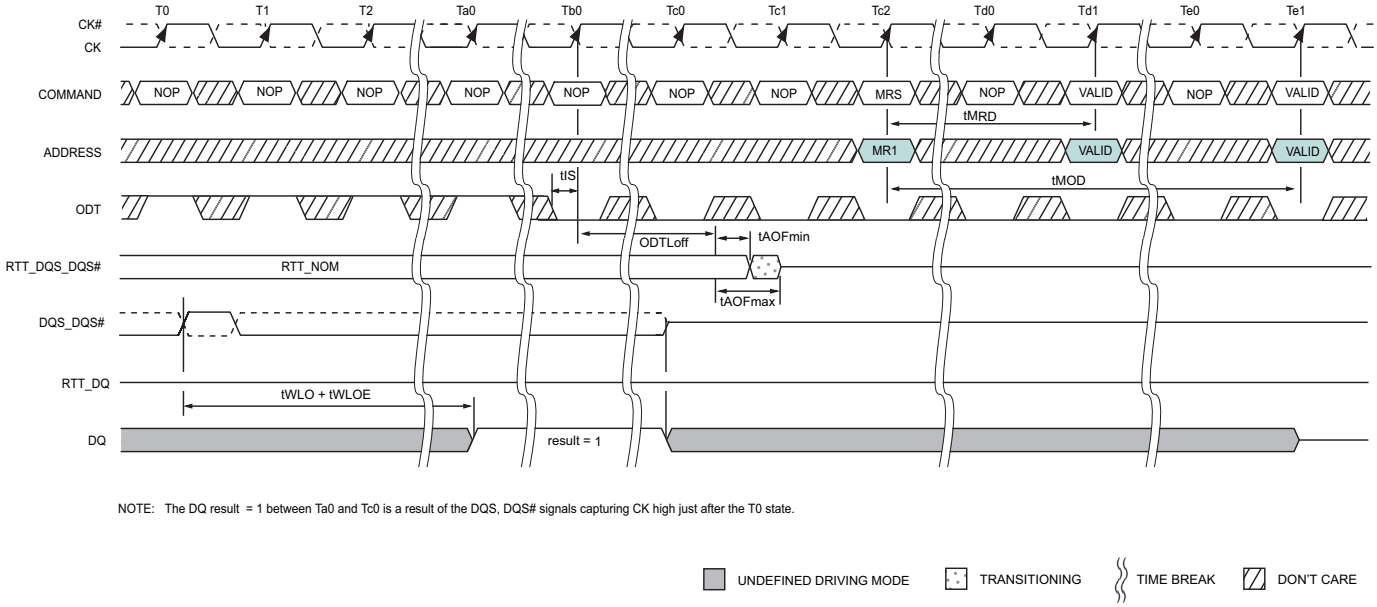



**Figure 16 — Timing details of Write leveling exit**

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## 4.9 Extended Temperature Usage

Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material:

a. Auto Self-refresh supported

b. Extended Temperature Range supported

c. Double refresh required for operation in the Extended Temperature Range (applies only for devices supporting the Extended Temperature Range**)**

**Table 10 — Mode Register Description**

| Field | Bits | Description |
|---|---|---|
| **ASR** | MR2 (A6) | **Auto Self-Refresh (ASR) (Optional)**<br>when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate $T_{OPER}$ during subsequent Self-Refresh operation<br><br>0 = Manual SR Reference (SRT)<br>1 = ASR enable (optional) |
| **SRT** | MR2 (A7) | **Self-Refresh Temperature (SRT) Range**<br>If ASR = 0, the SRT bit must be programmed to indicate $T_{OPER}$ during subsequent Self-Refresh operation<br>If ASR = 1, SRT bit must be set to $0_b$<br><br>0 = Normal operating temperature range<br>1 = Extended (optional) operating temperature range |

#### 4.9.0.1 Auto Self-Refresh mode - ASR Mode (optional)

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = $1_b$ and MR2 bit A7 = $0_b$. The DRAM will manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to $0_b$.

If the ASR mode is not enabled (MR2 bit.A6 = $0_b$), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Please refer to the supplier data sheet and/or the DIMM SPD for Extended Temperature Range and Auto Self-Refresh option availability.

### 4.9.1 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = $0_b$, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = $0_b$, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = $1_b$ then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to $0_b$ and the DRAM should not be operated outside the Normal Temperature Range.

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.9 Extended Temperature Usage (Cont'd)**

Please refer to the supplier data sheet and/or the DIMM SPD for Extended Temperature Range availability.

**Table 11 — Self-Refresh mode summary**

| MR2 A[6] | MR2 A[7] | Self-Refresh operation | Allowed Operating Temperature Range for Self-Refresh Mode |
|---|---|---|---|
| 0 | 0 | Self-refresh rate appropriate for the Normal Temperature Range | Normal (0 - 85 $^{o}$C) |
| 0 | 1 | Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details. | Normal and Extended (0 - 95 $^{o}$C) |
| 1 | 0 | ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent | Normal (0 - 85 $^{o}$C) |
| 1 | 0 | ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent | Normal and Extended (0 - 95 $^{o}$C) |
| 1 | 1 | Illegal | |

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## 4.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 17.

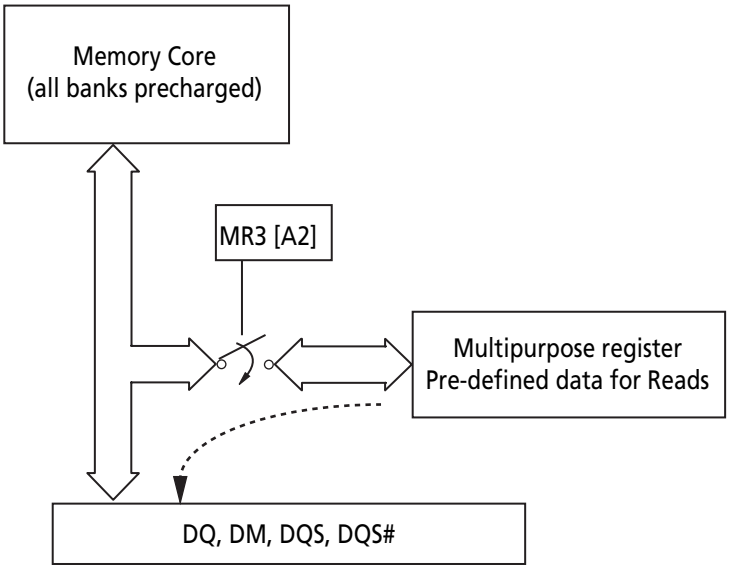



**Figure 17 — MPR Block Diagram**

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 12. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation when a RD or RDA command is issued is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 13. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

**Table 12 — MPR MR3 Register Definition**

| MR3 A[2] | MR3 A[1:0] | Function |
|---|---|---|
| MPR | MPR-Loc | |
| 0b | don't care (0b or 1b) | Normal operation, no MPR transaction.<br>All subsequent Reads will come from DRAM array.<br>All subsequent Write will go to DRAM array. |
| 1b | See Table 13 | Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0]. |

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.10 Multi Purpose Register (Cont'd)**

### 4.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
  - DQ[0] drives information from MPR.
  - DQ[3:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x8:
  - DQ[0] drives information from MPR.
  - DQ[7:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x16:
  - DQL[0] and DQU[0] drive information from MPR.
  - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order: 4,5,6,7 *)
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11, A13,... (if available): don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

**Note:** *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.10 Multi Purpose Register (Cont'd)**

### 4.10.2 MPR Register Address Definition

Table 13 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

**Table 13 — MPR MR3 Register Definition**

| MR3 A[2] | MR3 A[1:0] | Function | Burst Length | Read Address A[2:0] | Burst Order and Data Pattern |
|---|---|---|---|---|---|
| 1b | 00b | Read Predefined Pattern for System Calibration | BL8 | 000b | Burst order 0,1,2,3,4,5,6,7<br>Pre-defined Data Pattern [0,1,0,1,0,1,0,1] |
| | | | BC4 | 000b | Burst order 0,1,2,3<br>Pre-defined Data Pattern [0,1,0,1] |
| | | | BC4 | 100b | Burst order 4,5,6,7<br>Pre-defined Data Pattern [0,1,0,1] |
| 1b | 01b | RFU | BL8 | 000b | Burst order 0,1,2,3,4,5,6,7 |
| | | | BC4 | 000b | Burst order 0,1,2,3 |
| | | | BC4 | 100b | Burst order 4,5,6,7 |
| 1b | 10b | RFU | BL8 | 000b | Burst order 0,1,2,3,4,5,6,7 |
| | | | BC4 | 000b | Burst order 0,1,2,3 |
| | | | BC4 | 100b | Burst order 4,5,6,7 |
| 1b | 11b | RFU | BL8 | 000b | Burst order 0,1,2,3,4,5,6,7 |
| | | | BC4 | 000b | Burst order 0,1,2,3 |
| | | | BC4 | 100b | Burst order 4,5,6,7 |
| **Note:** Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent. | | | | | |

### 4.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600" on page 142.

### 4.10.4 Protocol Example

Protocol Example (This is one example):

Read out predetermined read-calibration pattern.

Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode "A2 = 1b" and "A[1:0] = 00b"
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
  - A[1:0] = '00'b (Data burst order is fixed starting at nibble, always 00b here)
  - A[2] = '0'b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12/BC = 1 (use regular burst length of 8)
  - All other address pins (including BA[2:0] and A10/AP): don't care

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- After RL = AL + CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode "A2 = 0b" and "A[1:0] = valid data but value are don't care"
  - All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with "regular" DRAM commands, like activate a memory bank for regular read or write access,...

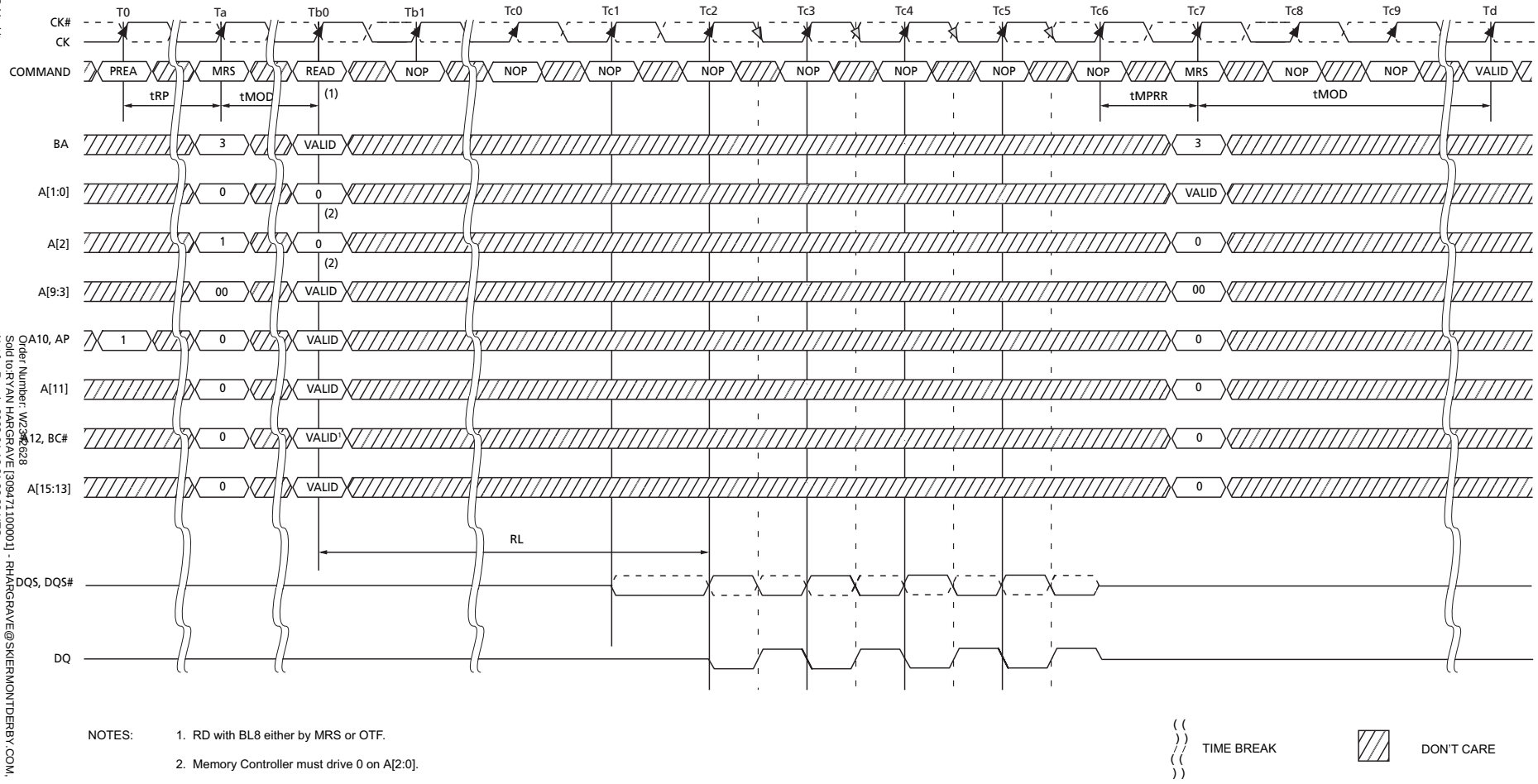


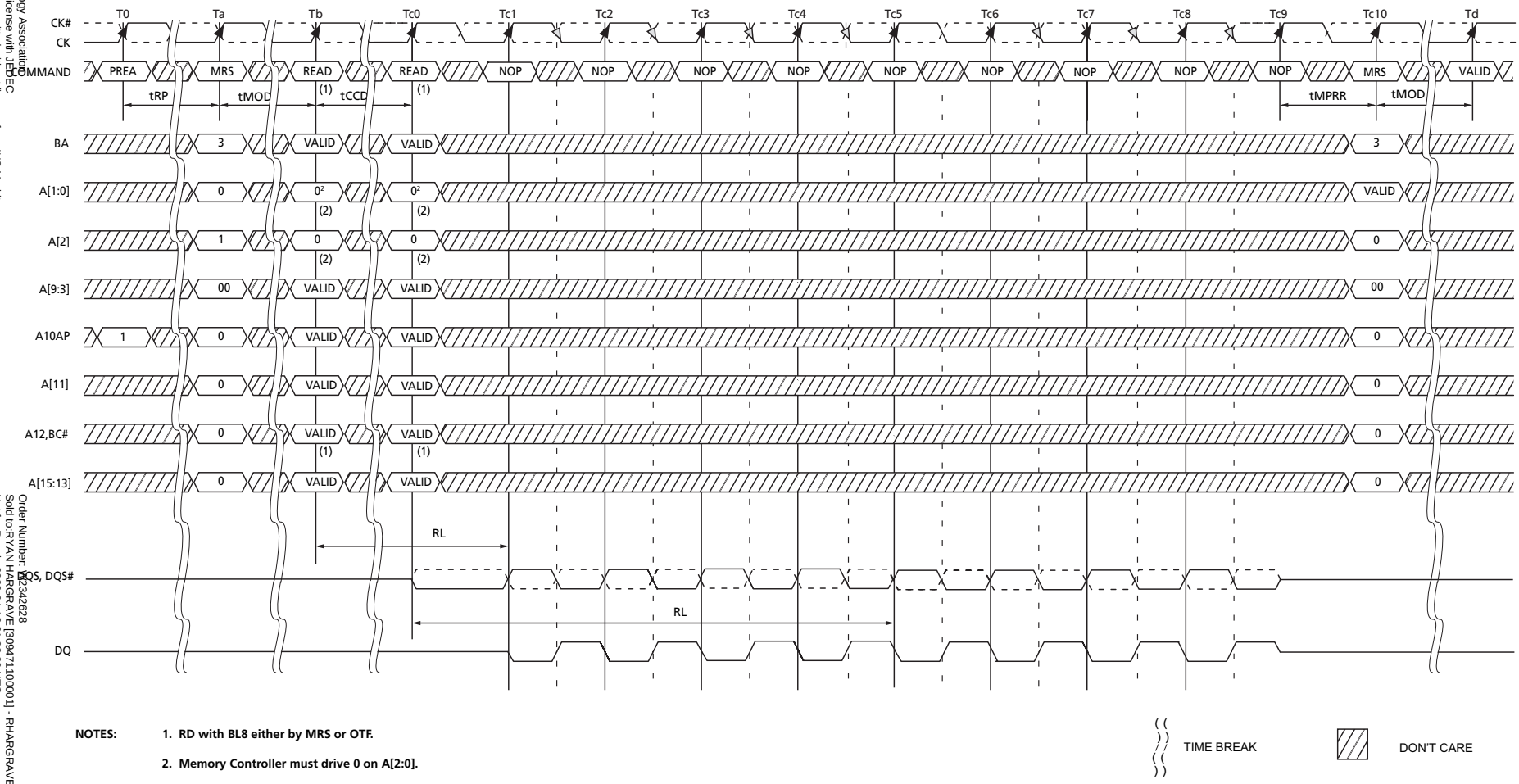

**Figure 18 — MPR Readout of predefined pattern, BL8 fixed burst order, single readout**

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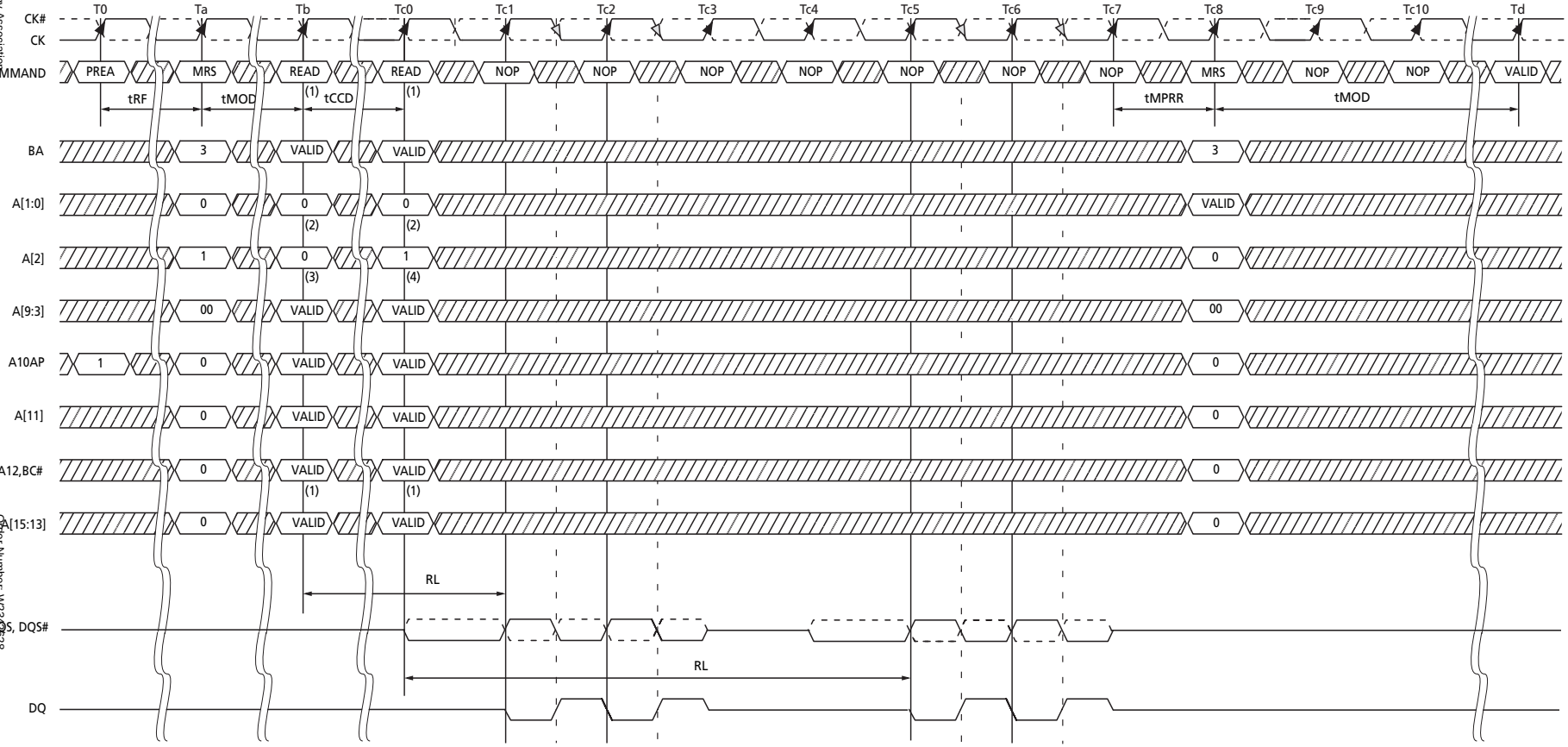
**4.10 Multi Purpose Register (Cont'd)**
**4.10.4 Protocol Example Cont'd)**




**NOTES:**
1. **RD with BL8 either by MRS or OTF.**
2. **Memory Controller must drive 0 on A[2:0].**

**Figure 19 — MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout**

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NOTES:
1. RD with BC4 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

TIME BREAK

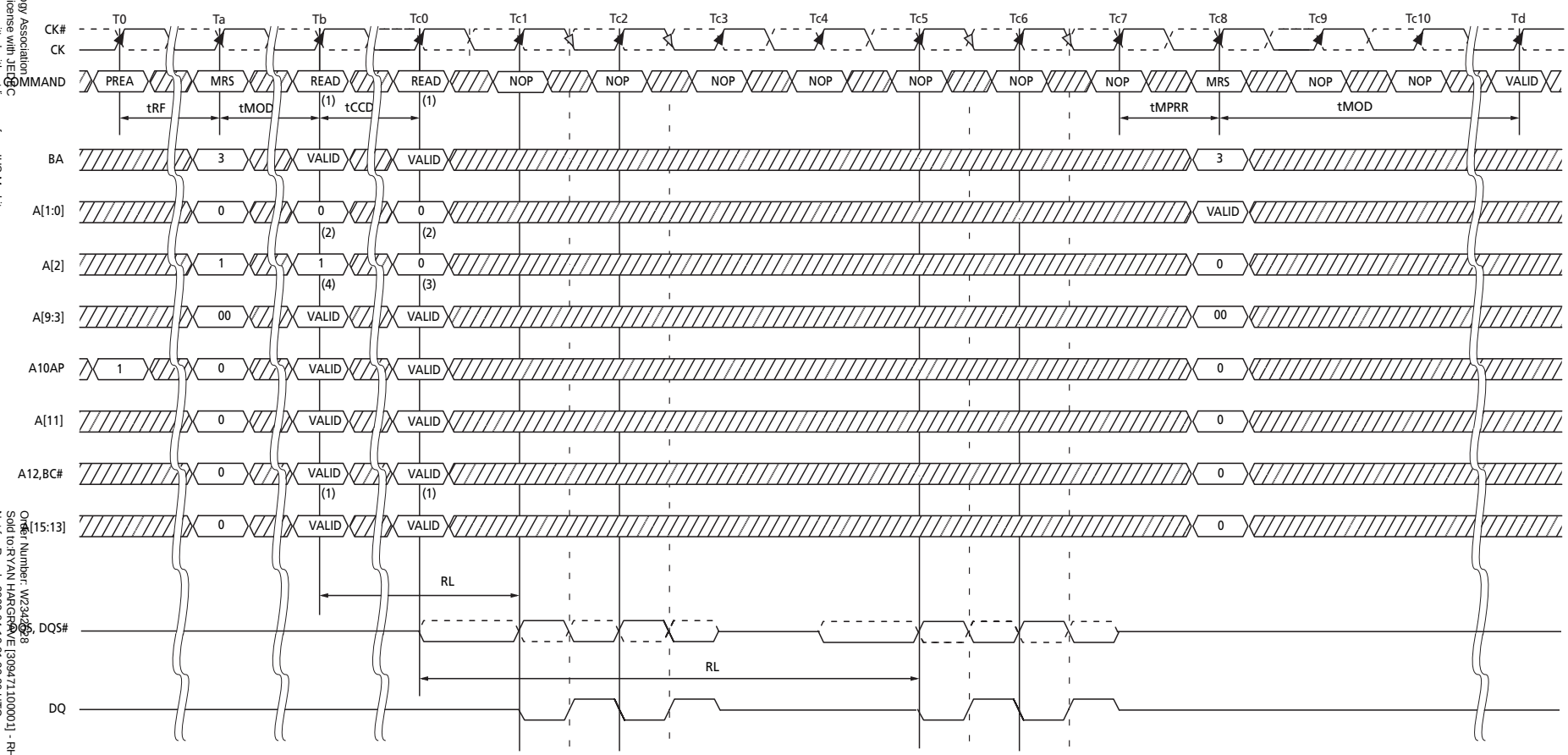
DON'T CARE

**Figure 20 — MPR Readout predefined pattern, BC4, lower nibble then upper nibble**



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NOTES:
1. RD with BC4 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

**Figure 21 — MPR Readout of predefined pattern, BC4, upper nibble then lower nibble**

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## 4.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

## 4.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

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## 4.13 READ Operation

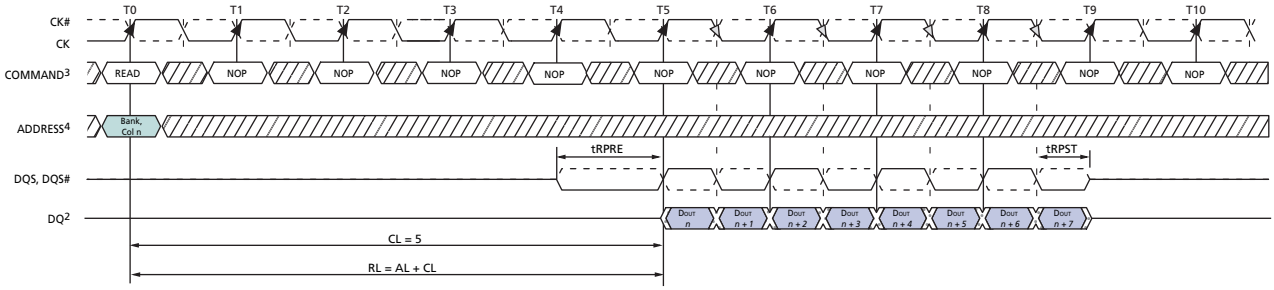
### 4.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

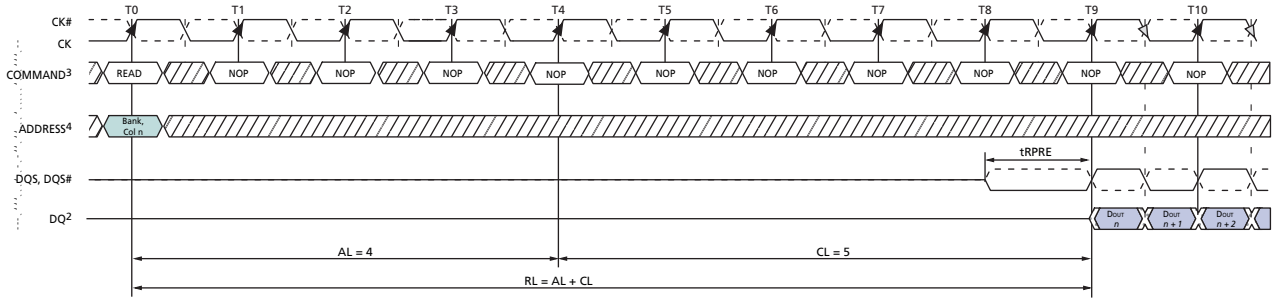
A12 is used only for burst length control, not as a column address.




**NOTES:** 1. BL8, RL = 5, AL = 0, CL = 5.
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

**Figure 22 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)**




**NOTES:** 1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

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**Figure 23 — READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8)**

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.13 READ Operation (Cont'd)**

### 4.13.2 READ Timing Definitions

Read timing is shown in Figure 24 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the DQS, DQS# differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, DQS# differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

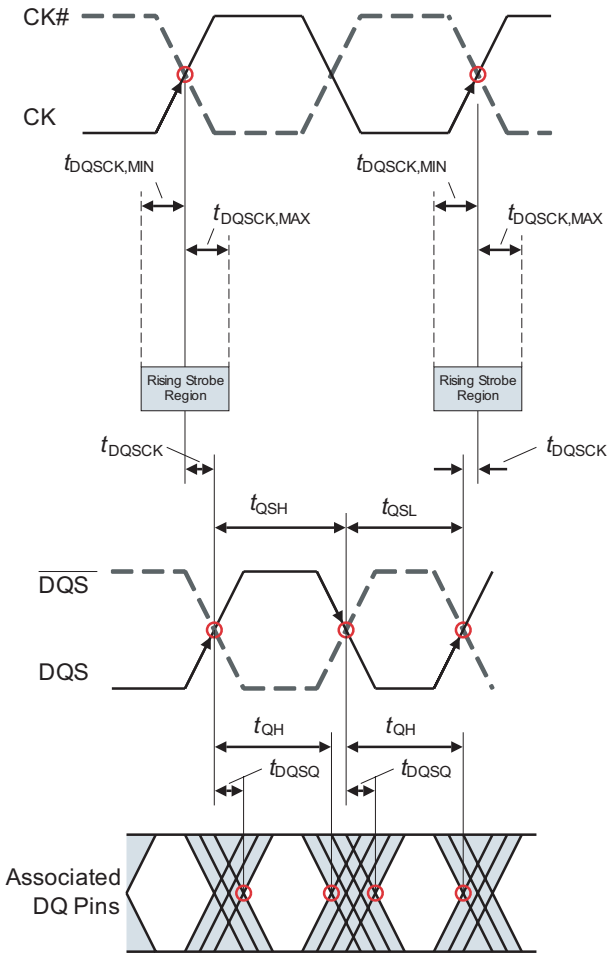



**Figure 24 — READ Timing Definition**

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**4.13 READ Operation (Cont'd)**
**4.13.2 READ Timing Definitions (Cont'd)**

#### 4.13.2.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 25 and is applied when the DLL is enabled and locked.

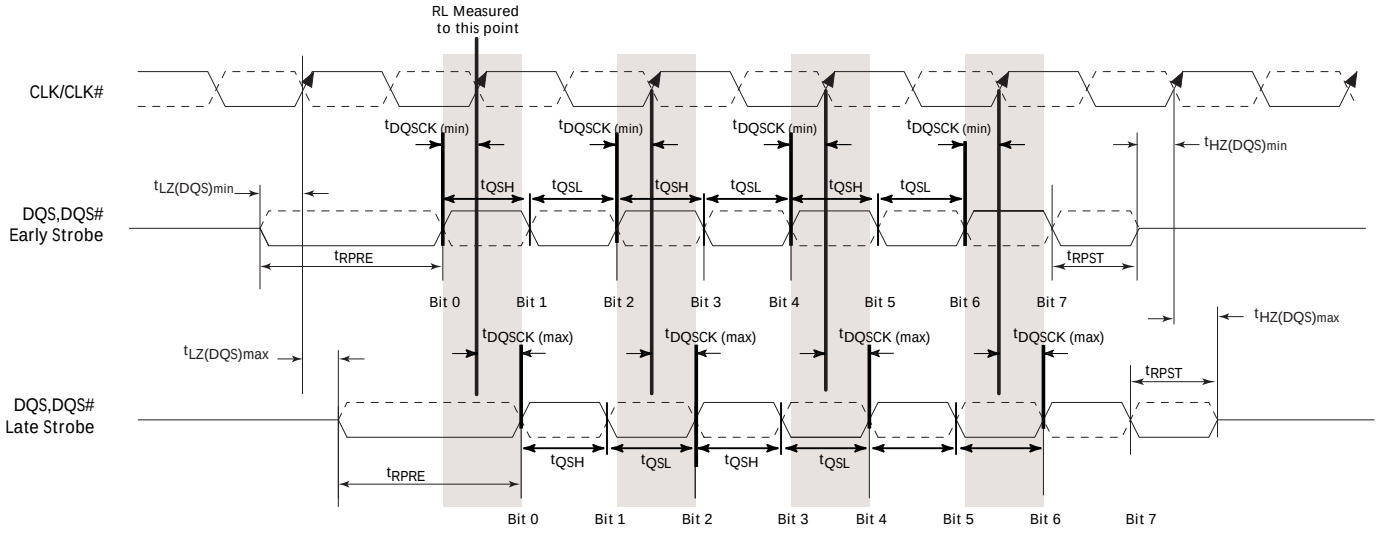
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

tLZ(DQS), tHZ(DQS) for preamble/postamble (see 4.13.2.3 and Figure 27)




**NOTES:**
1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
3. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case); However, they will tend to track each other.
4. The minimum pulse width of read preamble is defined by tRPRE(min). The minimum pulse width of read postamble is defined by tRPST(min).

**Figure 25 — Clock to Data Strobe Relationship**

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**4.13 READ Operation (Cont'd)**
**4.13.2 READ Timing Definitions (Cont'd)**

#### 4.13.2.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 26 and is applied when the DLL is enabled and locked.

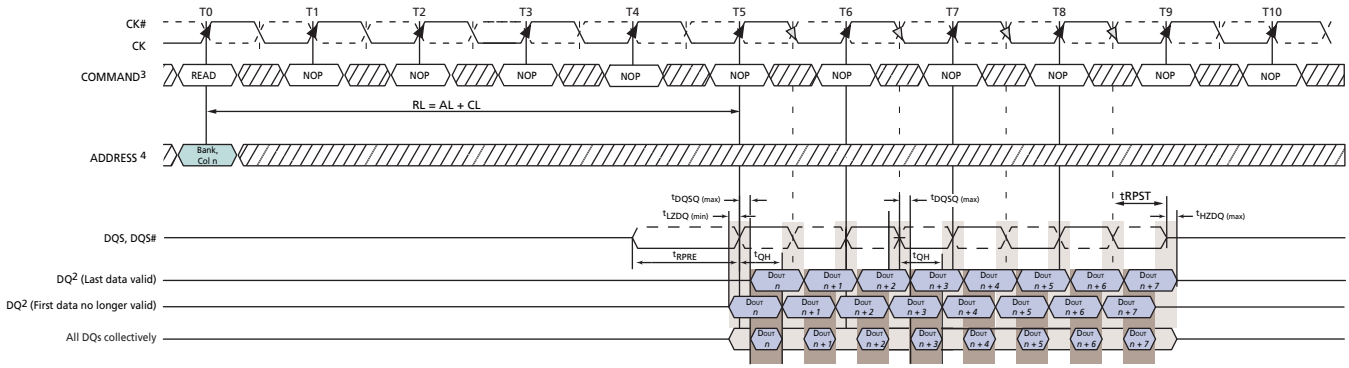
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined




**NOTES:** 1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS,DQS# to Data and does not define DQS,DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

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**Figure 26 — Data Strobe to Data Relationship**

#### 4.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 27 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the cal-

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**4.13 READ Operation (Cont'd)**
**4.13.2 READ Timing Definitions (Cont'd)**

culation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

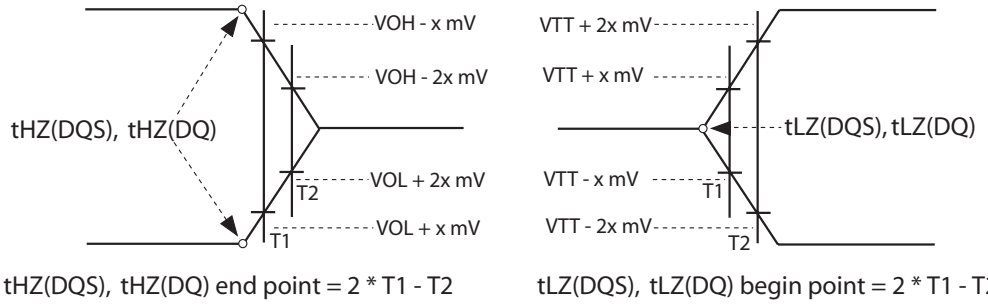



**Figure 27 — tLZ and tHZ method for calculating transitions and endpoints**

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**4.13 READ Operation (Cont'd)**
**4.13.2 READ Timing Definitions (Cont'd)**

#### 4.13.2.4 tRPRE Calculation

Method for calculating differential pulse widths for tRPRE is shown in Figure 28.

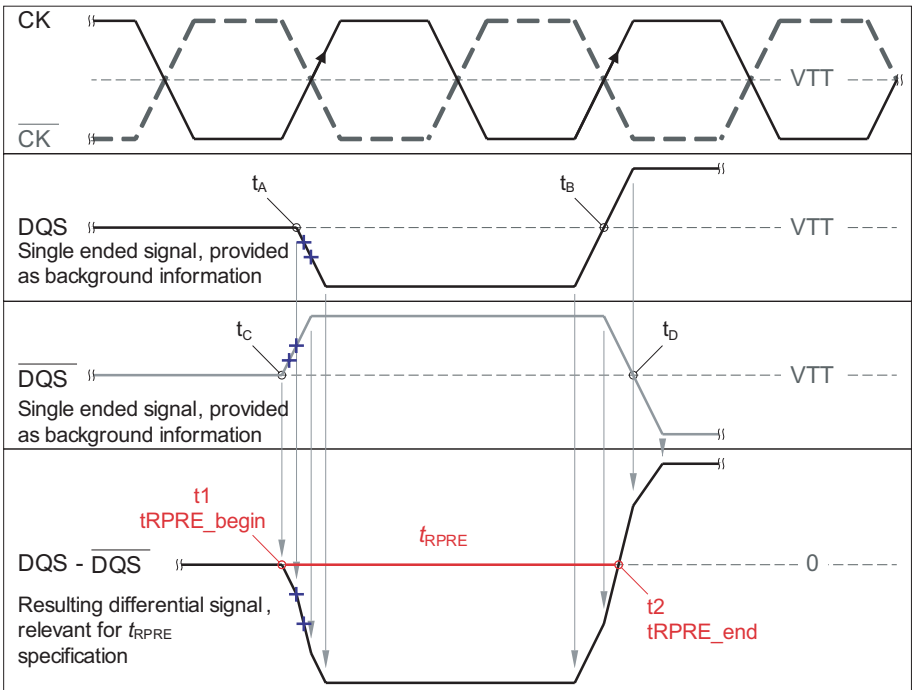



**Figure 28 — Method for calculating tRPRE transitions and endpoints**

#### 4.13.2.5 tRPST Calculation

Method for calculating differential pulse widths for tRPST.

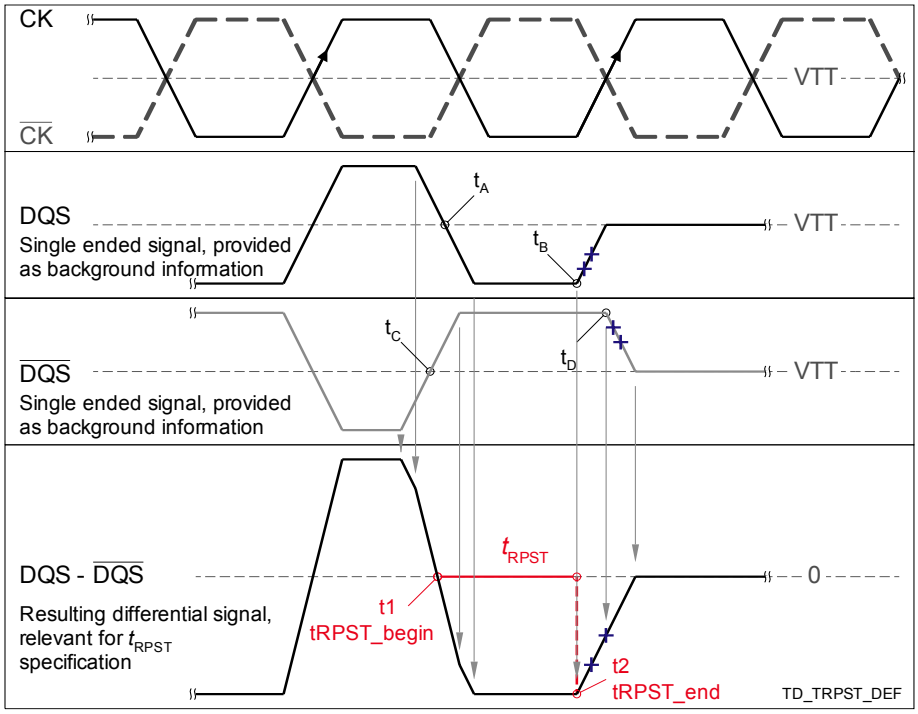
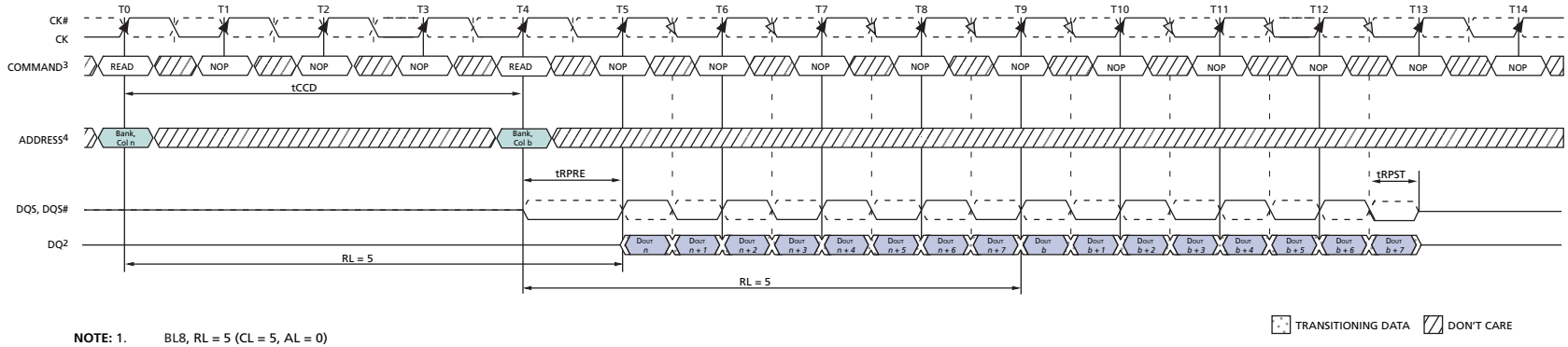



**Figure 29 — Method for calculating tRPST transitions and endpoints**

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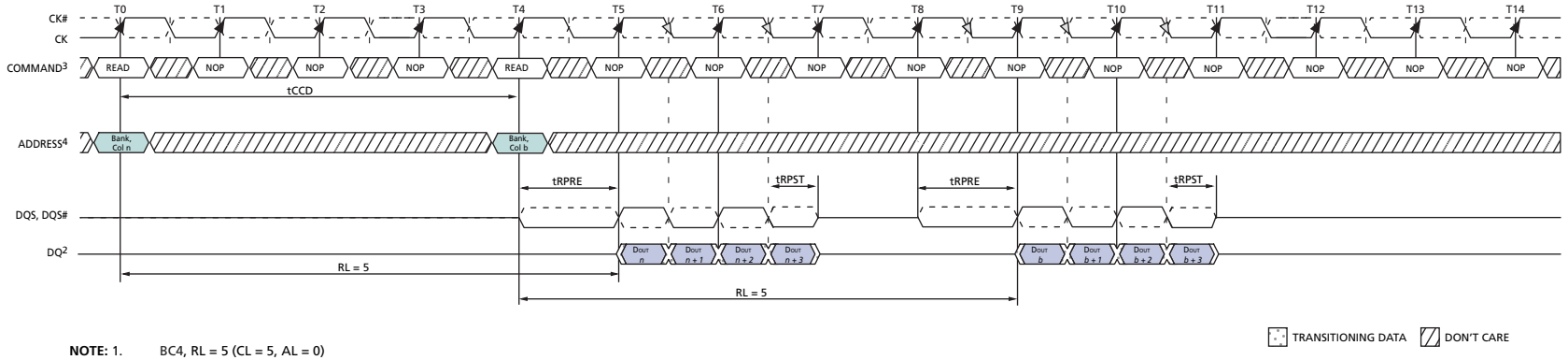
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**NOTE:** 1. BL8, RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.

## Figure 30 — READ (BL8) to READ (BL8)



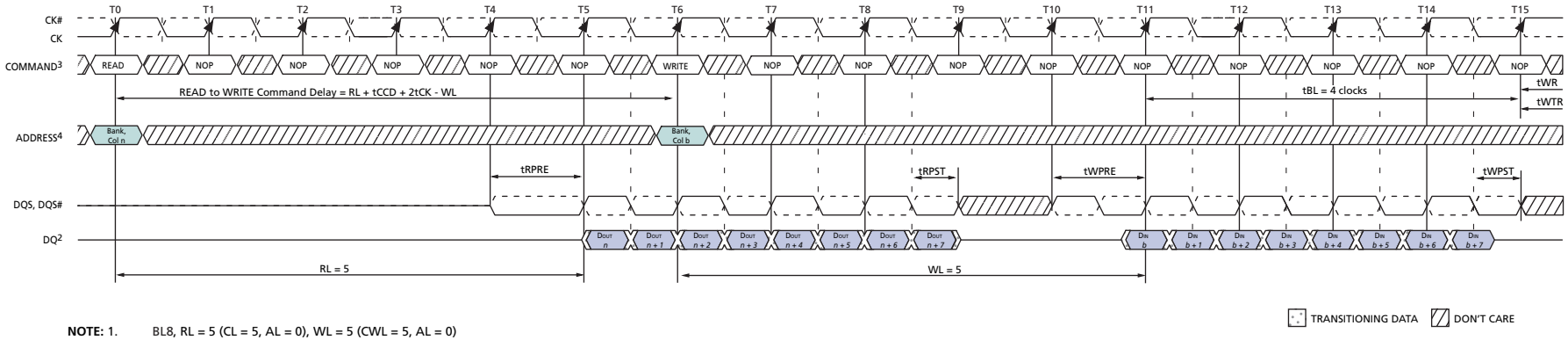

**NOTE:** 1. BC4, RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0 = 10] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

## Figure 31 — READ (BC4) to READ (BC4)

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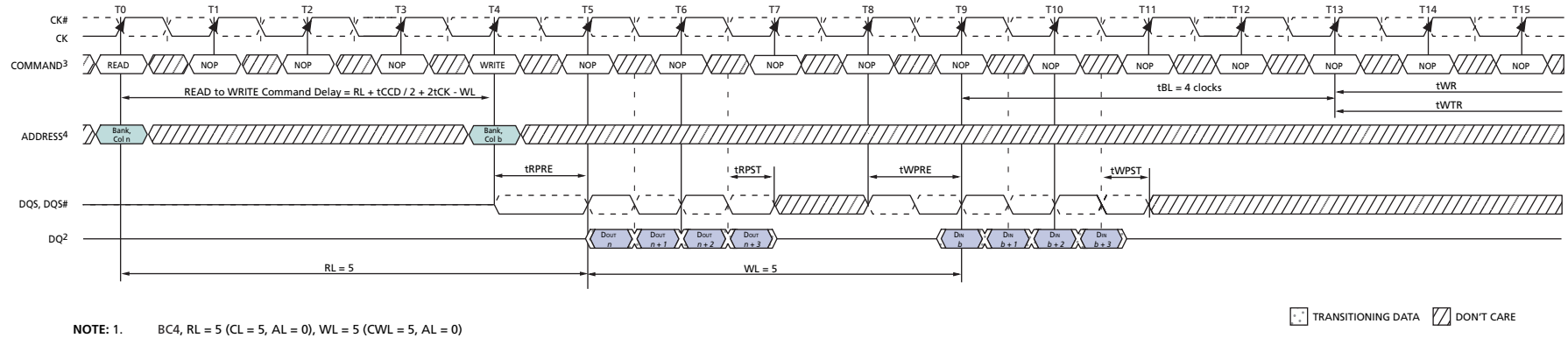
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**NOTE:** 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0 and WRITE command at T6.

**Figure 32 — READ (BL8) to WRITE (BL8)**




**NOTE:** 1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0 and WRITE command at T4.

**Figure 33 — READ (BC4) to WRITE (BC4) OTF**

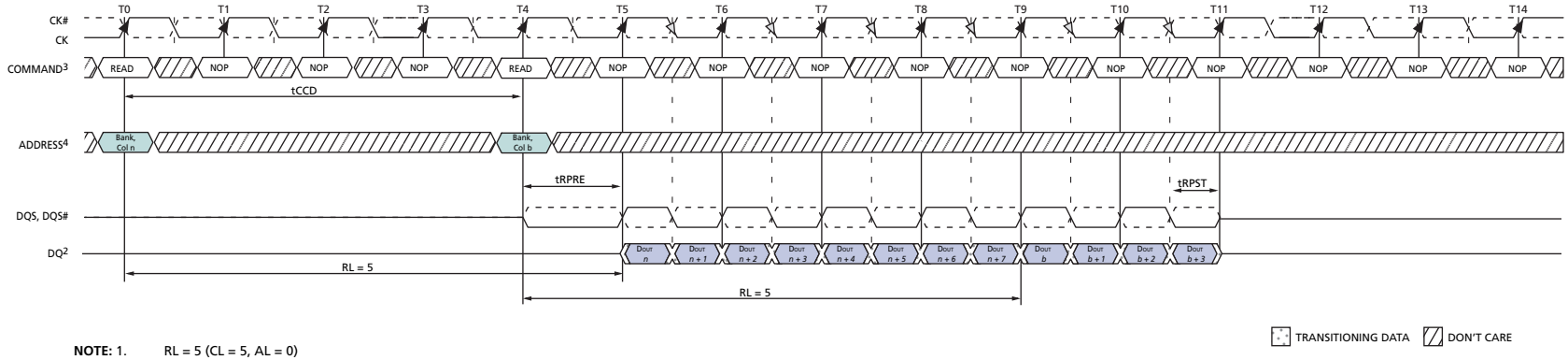


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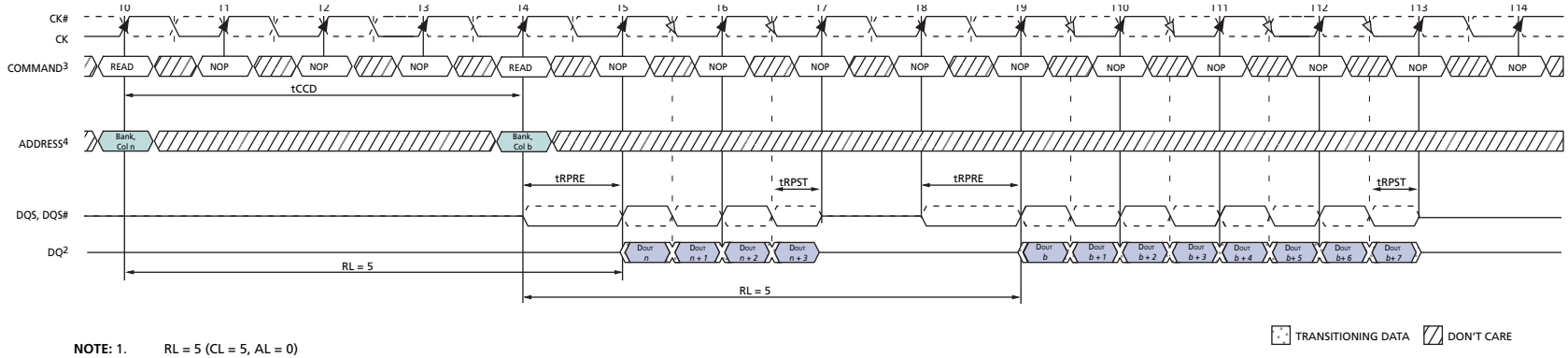
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**NOTE:** 1. RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T4.

**Figure 34 — READ (BL8) to READ (BC4) OTF**

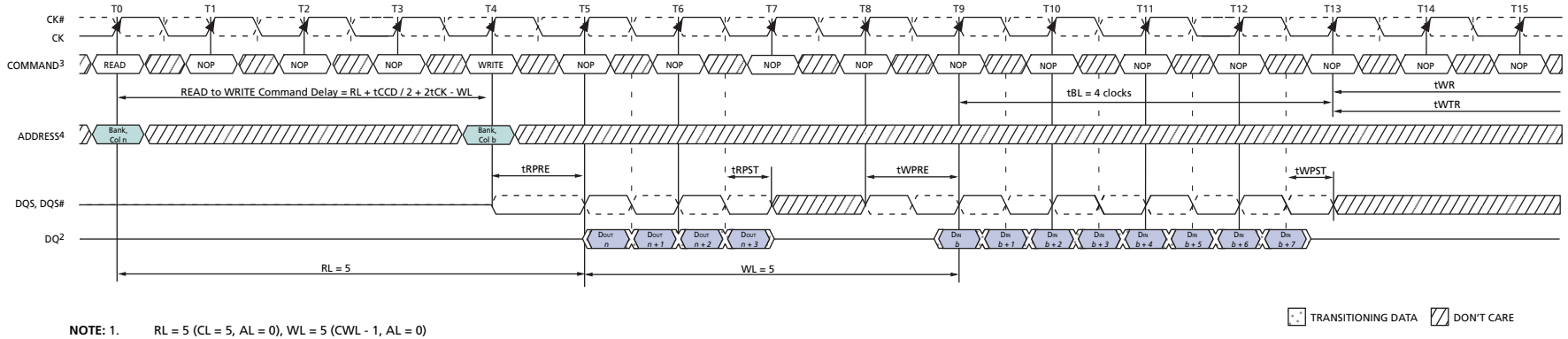



**NOTE:** 1. RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T4.

**Figure 35 — READ (BC4) to READ (BL8) OTF**

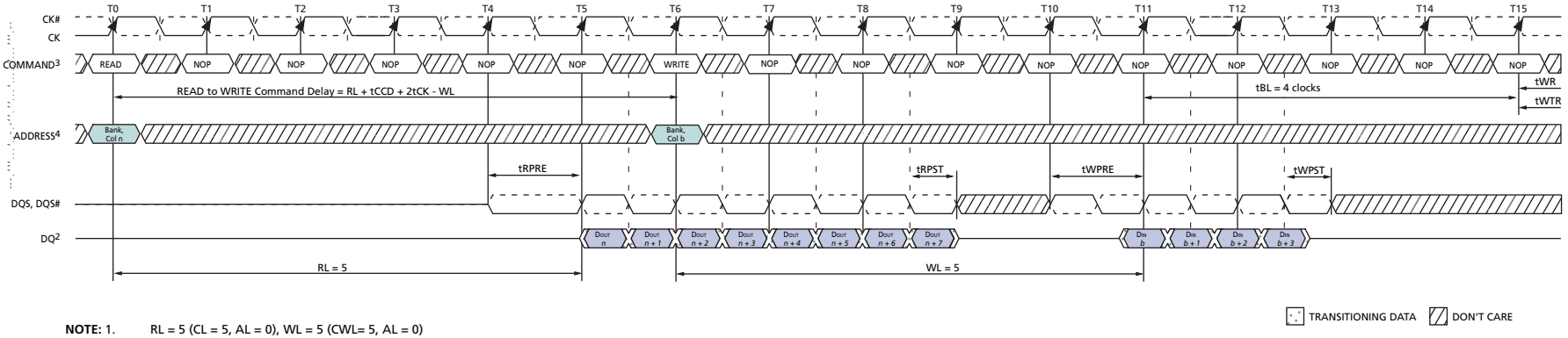
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**NOTE:** 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL - 1, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

**Figure 36 — READ (BC4) to WRITE (BL8) OTF**




**NOTE:** 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL= 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T6.

**Figure 37 — READ (BL8) to WRITE (BC4) OTF**



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## 4.14 WRITE Operation

### 4.14.1 DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

A12 is used only for burst length control, not as a column address.

### 4.14.2 WRITE Timing Violations

#### 4.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desireable for certain minor violations that the DRAM is guaranteed not to "hang up" and errors be limited to that particular operation.

For the following, it will be assumed that there are no timing violations w.r.t. to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

#### 4.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example (Figure 38 on page 63), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

#### 4.14.2.3 Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 4.14.2.4 on page 62) the relevant strobe edges for Write burst A are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fullfilled for a valid burst. For Write burst B the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

#### 4.14.2.4 Write Timing Parameters

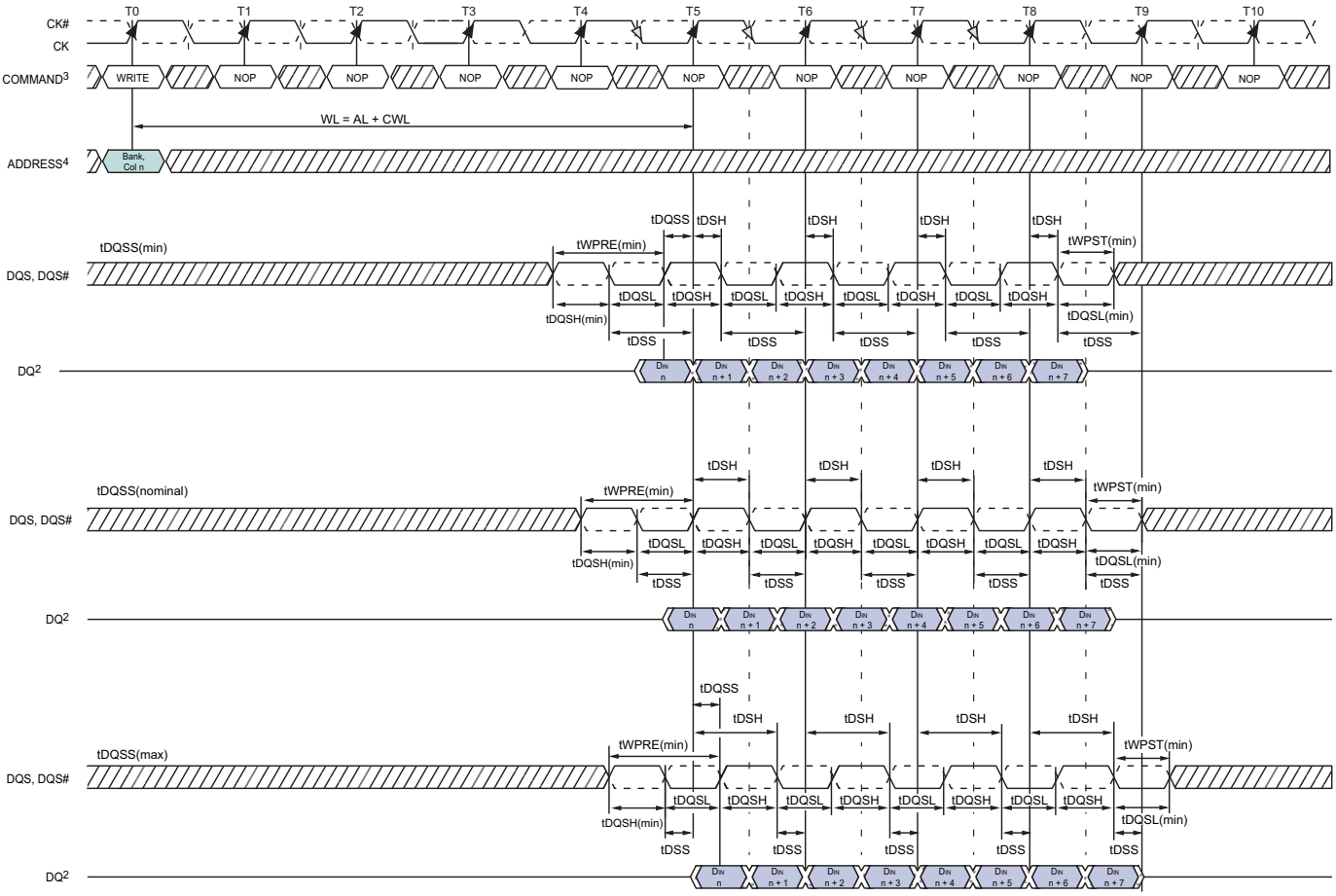
This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).]

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### 4.14 WRITE Operation (Cont'd)
### 4.14.2 Write Timing Parameters (Cont'd)




NOTE: 1. BL8, WL = 5 (AL = 0, CWL = 5)
2. $D_{IN}$ n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

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## Figure 38 — Write Timing Definition and Parameters

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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.14 WRITE Operation (Cont'd)**

### 4.14.3 tWPRE Calculation

Method for calculating differential pulse widths for tWPRE is shown in Figure 1.

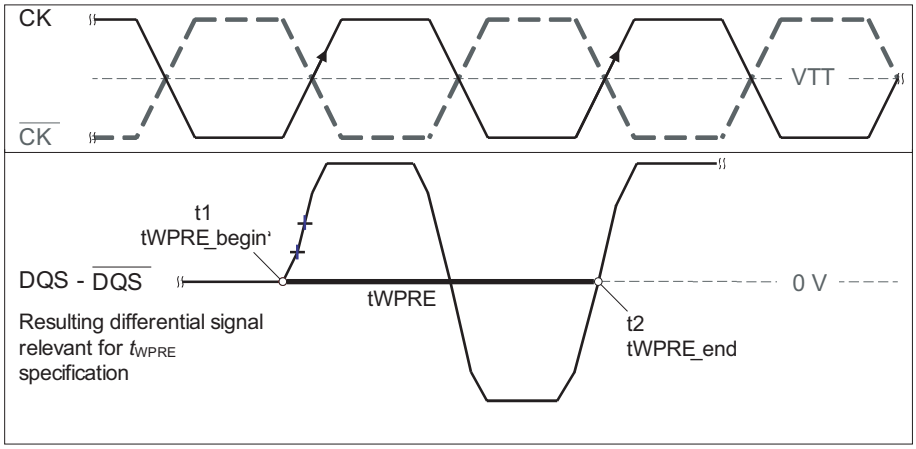



**Figure 39 — Method for calculating tWPRE transitions and endpoints**

### 4.14.4 tWPST Calculation

Method for calculating differential pulse widths for tWPST is shown in Figure 2.

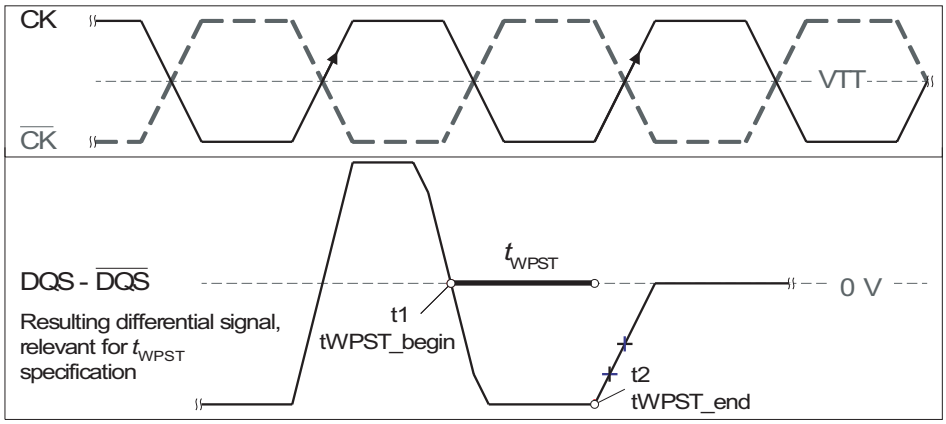


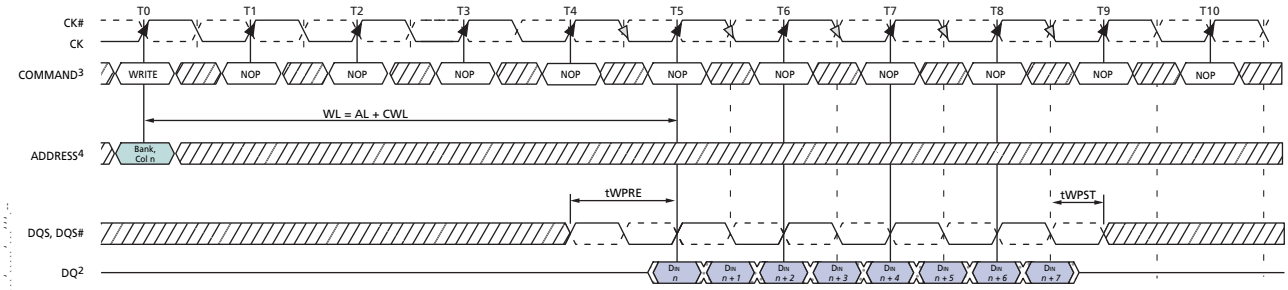

**Figure 40 — Method for calculating tWPST transitions and endpoints**

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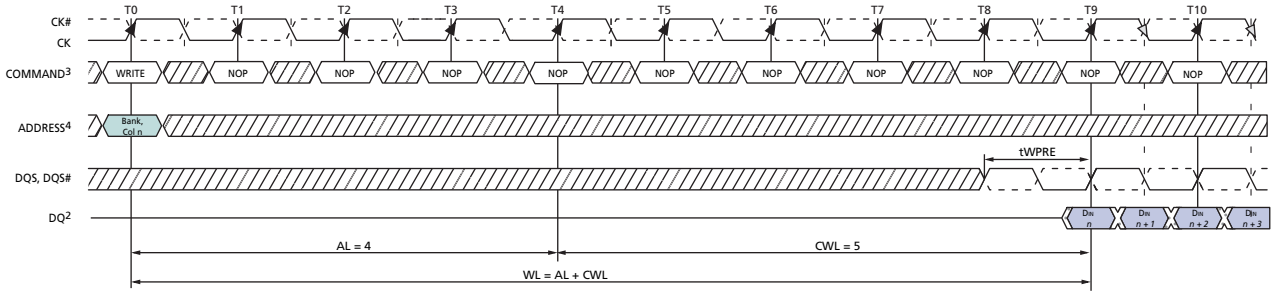
### 4.14 WRITE Operation (Cont'd)
### 4.14.4 tWPST Calculation (Cont'd)




**NOTE:** 1. BL8, WL = 5; AL = 0, CWL = 5.
2. DIN *n* = data-in from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

TRANSITIONING DATA DON'T CARE

**Figure 41 — WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)**




**NOTE:** 1. BL8, WL = 9; AL = (CL - 1), CL = 5, CWL = 5.
2. DIN *n* = data-in from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

TRANSITIONING DATA DON'T CARE

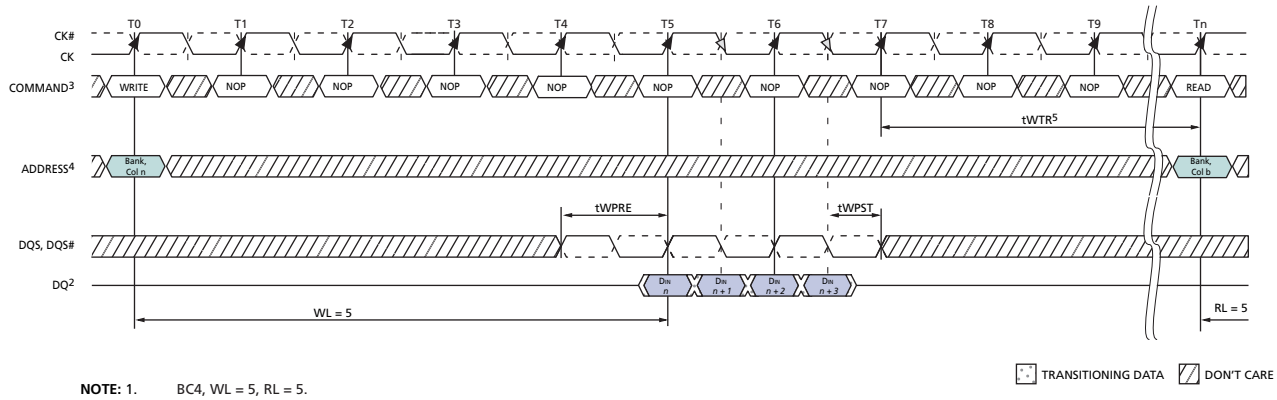
**Figure 42 — WRITE Burst Operation WL = 9 (AL = CL-1, CWL = 5, BL8)**

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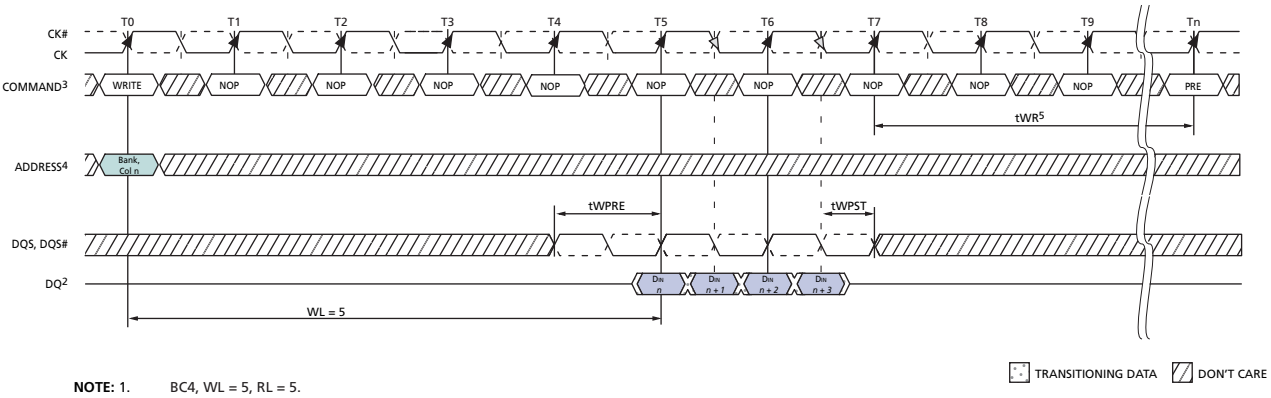
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### 4.14 WRITE Operation (Cont'd)
### 4.14.4 tWPST Calculation (Cont'd)




**NOTE:** 1. BC4, WL = 5, RL = 5.
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

## Figure 43 — WRITE (BC4) to READ (BC4) Operation



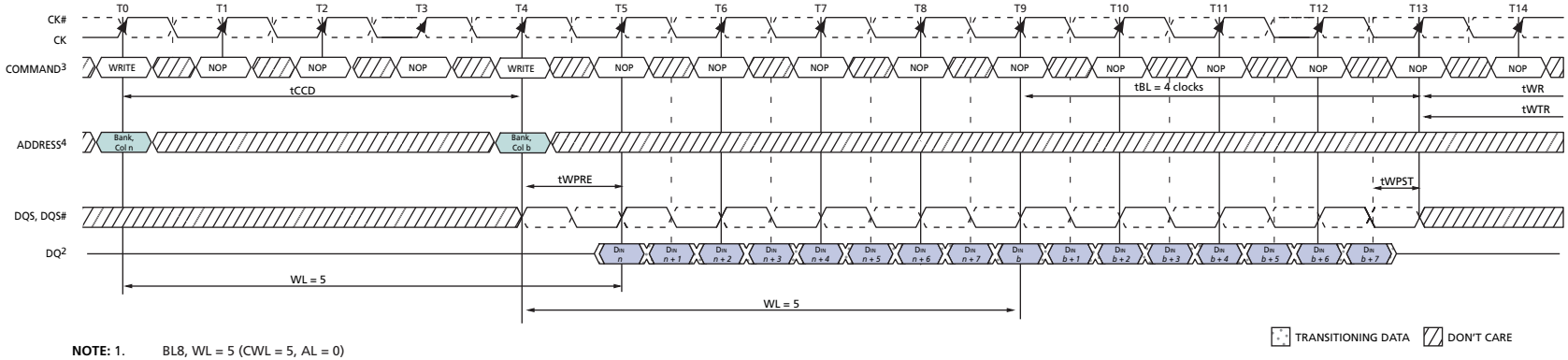

**NOTE:** 1. BC4, WL = 5, RL = 5.
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank .

## Figure 44 — WRITE (BC4) to PRECHARGE Operation

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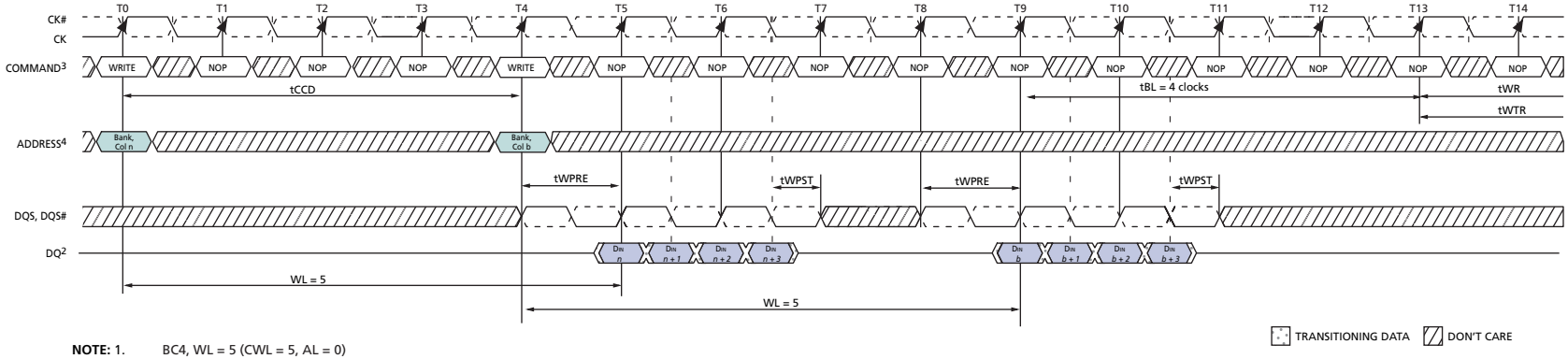
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**NOTE:** 1. BL8, WL = 5 (CWL = 5, AL = 0)
2. $D_{IN}$ *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T4.

## Figure 45 — WRITE (BL8) to WRITE (BL8)




**NOTE:** 1. BC4, WL = 5 (CWL = 5, AL = 0)
2. $D_{IN}$ *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0 and T4.

## Figure 46 — WRITE (BC4) to WRITE (BC4) OTF

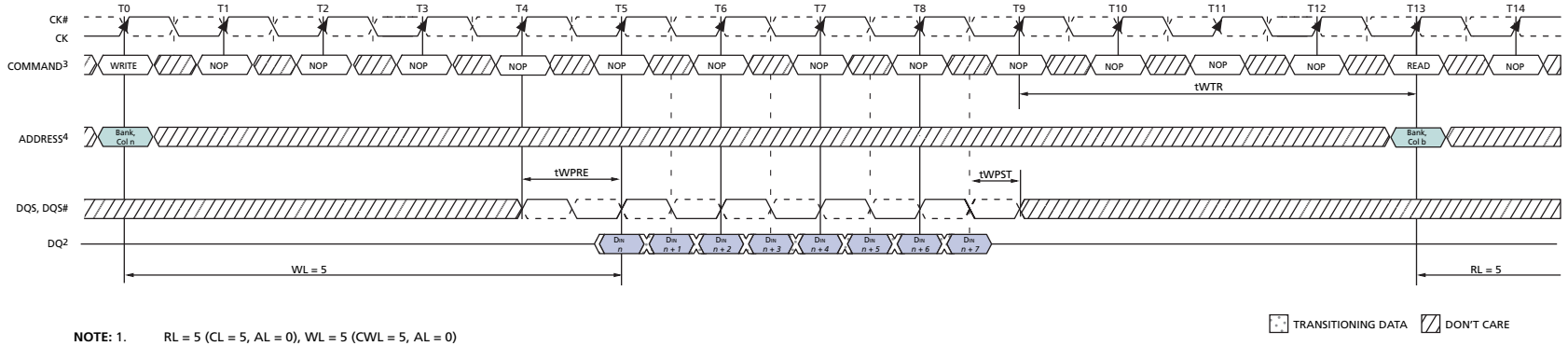


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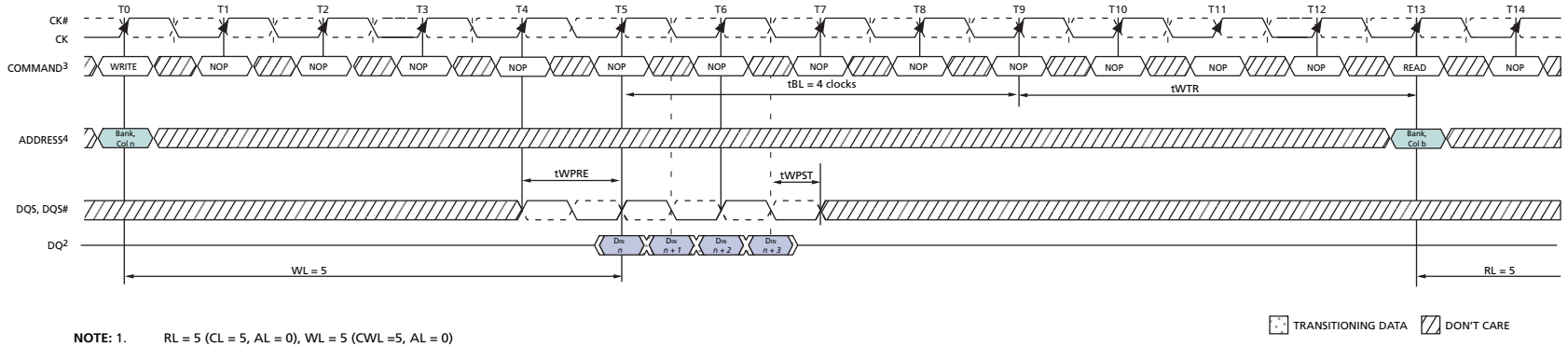
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**4.14 WRITE Operation (Cont'd)**
**4.14.4 tWPST Calculation (Cont'd)**




**NOTE:** 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on MR0[A1:0] and A12 status at T13.

**Figure 47 — WRITE (BL8) to READ (BC4/BL8) OTF**

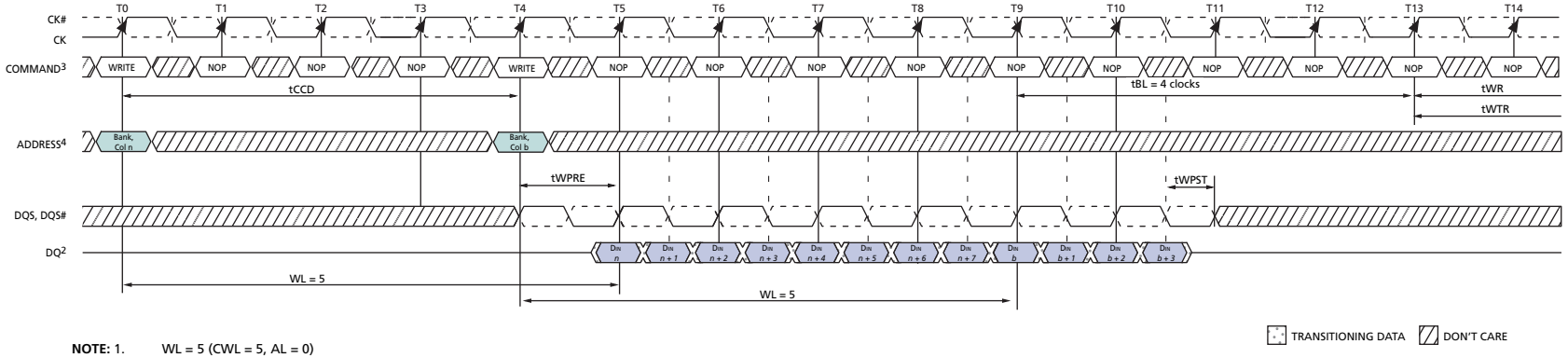



**NOTE:** 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on A12 status at T13.

**Figure 48 — WRITE (BC4) to READ (BC4/BL8) OTF**

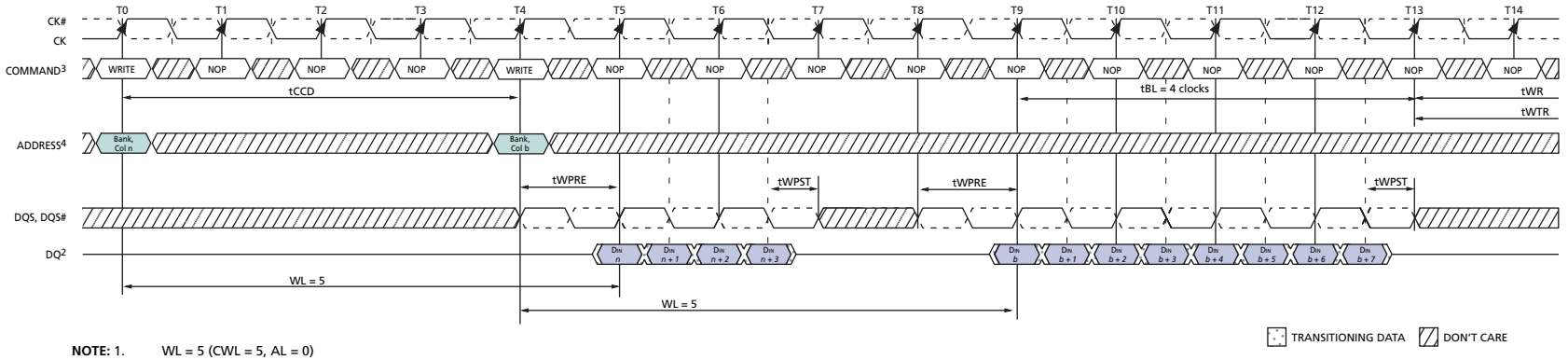
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**NOTE:** 1. WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T4.

**Figure 49 — WRITE (BL8) to WRITE (BC4) OTF**




**NOTE:** 1. WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

**Figure 50 — WRITE (BC4) to WRITE (BL8) OTF**



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## 4.15 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA and VRefDQ) must be at valid levels. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselct commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL.

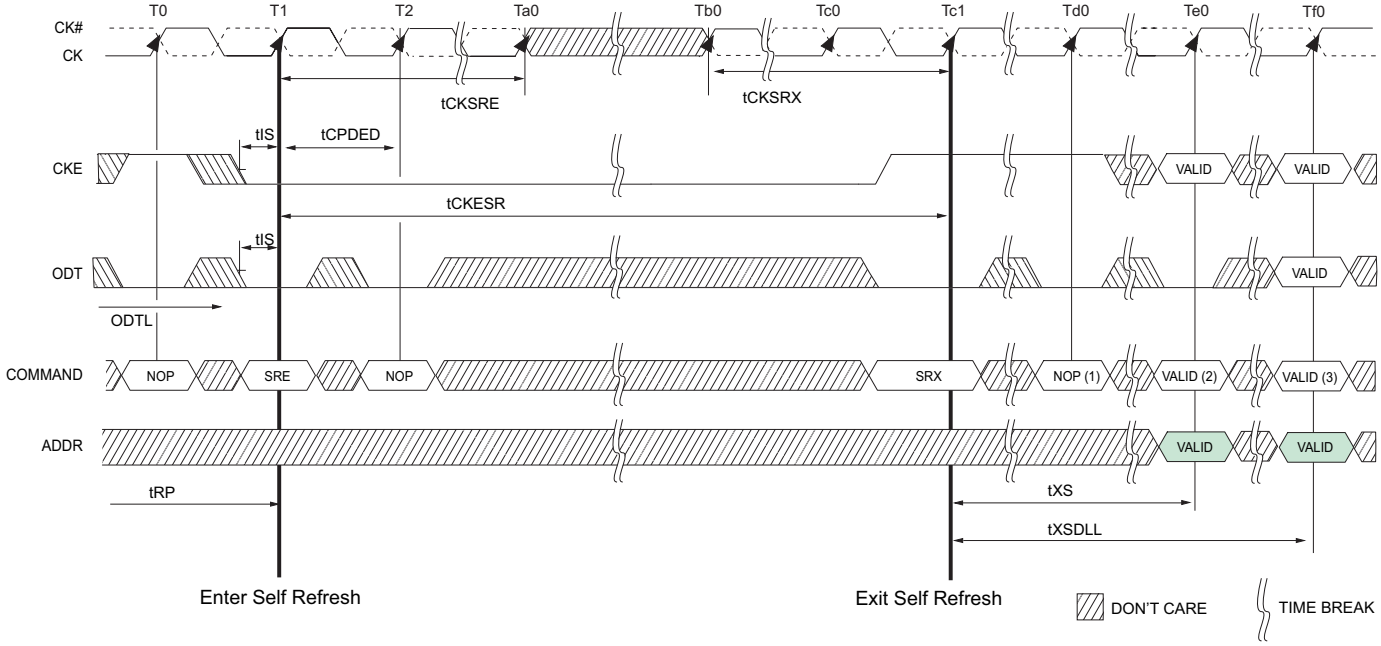
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**4 DDR3 SDRAM Command Description and Operation (Cont'd)**
**4.15 Self-Refresh Operation (Cont'd)**

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.




NOTES: 1. Only NOP or DES command.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

**Figure 51 — Self-Refresh Entry/Exit Timing**

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## 4.16 Power-Down Modes

### 4.16.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 52 through Figures 64 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

**Table 14 — Power-Down Entry Definitions**

| Status of DRAM | MRS bit A12 | DLL | PD Exit | Relevant Parameters |
|---|---|---|---|---|
| Active (A bank or more Open) | Don't Care | On | Fast | **tXP** to any valid command |
| Precharged (All banks Precharged) | 0 | Off | Slow | **tXP** to any valid command. Since it is in precharge state, commands here will be ACT, REF, MRS, PRE or PREA. **tXPDLL** to commands that need the DLL to operate, such as RD, RDA or ODT control line. |
| Precharged (All banks Precharged) | 1 | On | Fast | **tXP** to any valid command. |

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

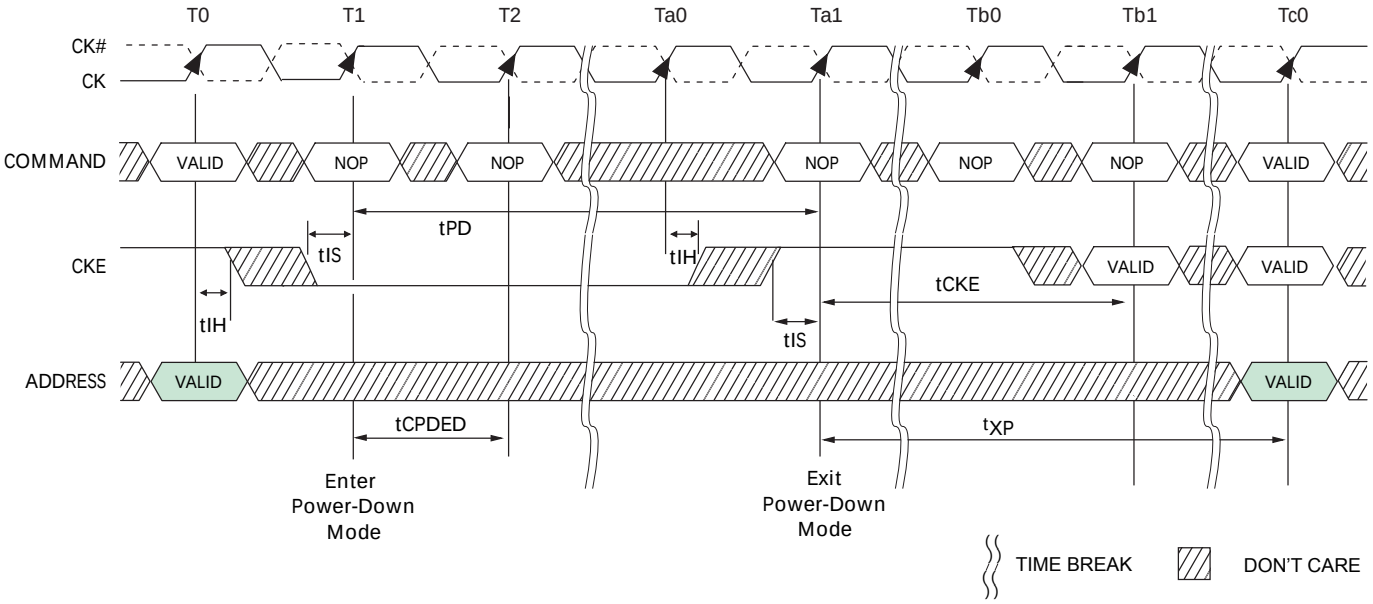
Active Power Down Entry and Exit timing diagram example is shown in Figure 52. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 53 through Figure 61. Additional clarifications are shown in Figure 62 through Figure 64.

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**4.16 Power-Down Modes (Cont'd)**
**4.16.1 Power-Down Entry and Exit (Cont'd)**




Note: VALID command at T0 is ACT, NOP, DES or PRE with still one bank remaining open after completion of the precharge command.

**Figure 52 — Active Power-Down Entry and Exit Timing Diagram**

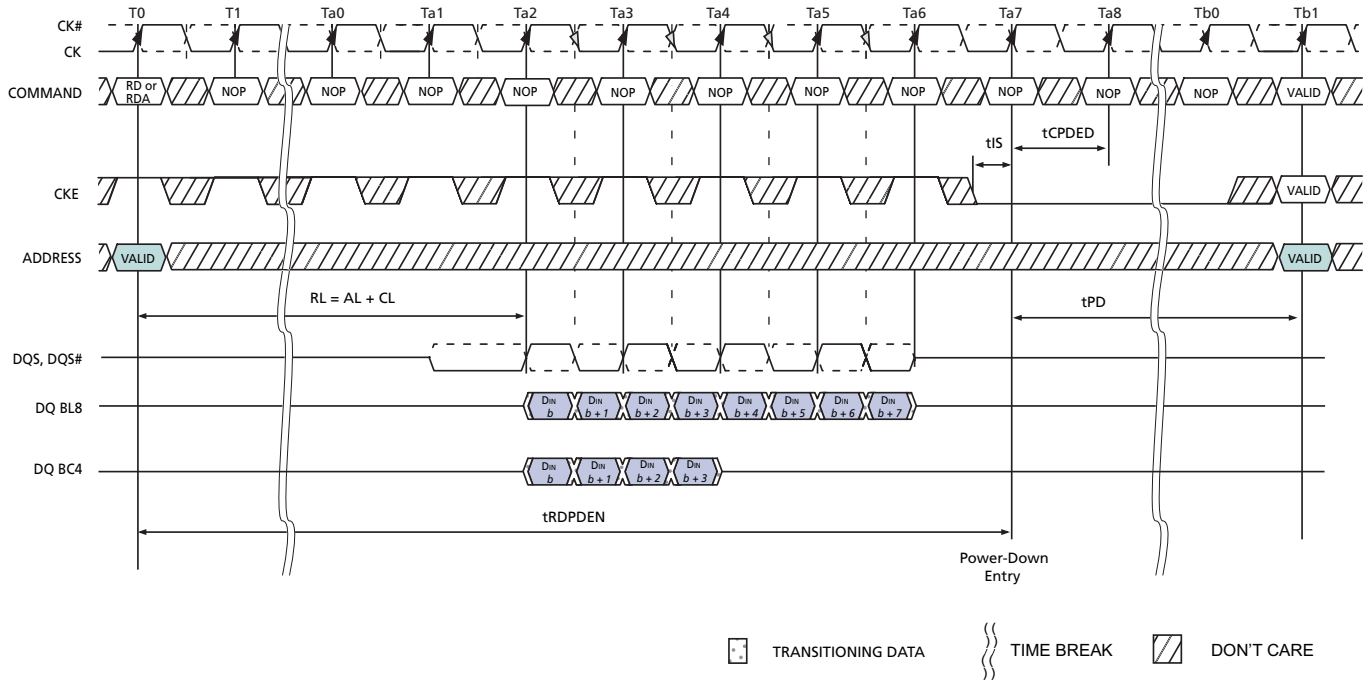


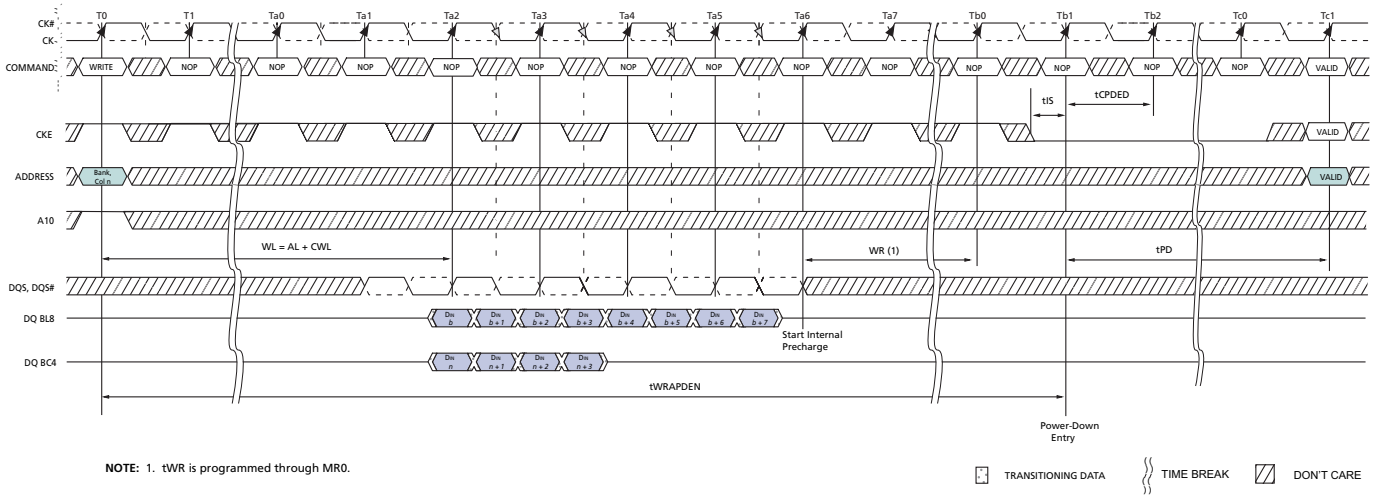

**Figure 53 — Power-Down Entry after Read and Read with Auto Precharge**

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### 4.16 Power-Down Modes (Cont'd)
### 4.16.1 Power-Down Entry and Exit (Cont'd)




**NOTE:** 1. tWR is programmed through MR0.

**Figure 54 — Power-Down Entry after Write with Auto Precharge**

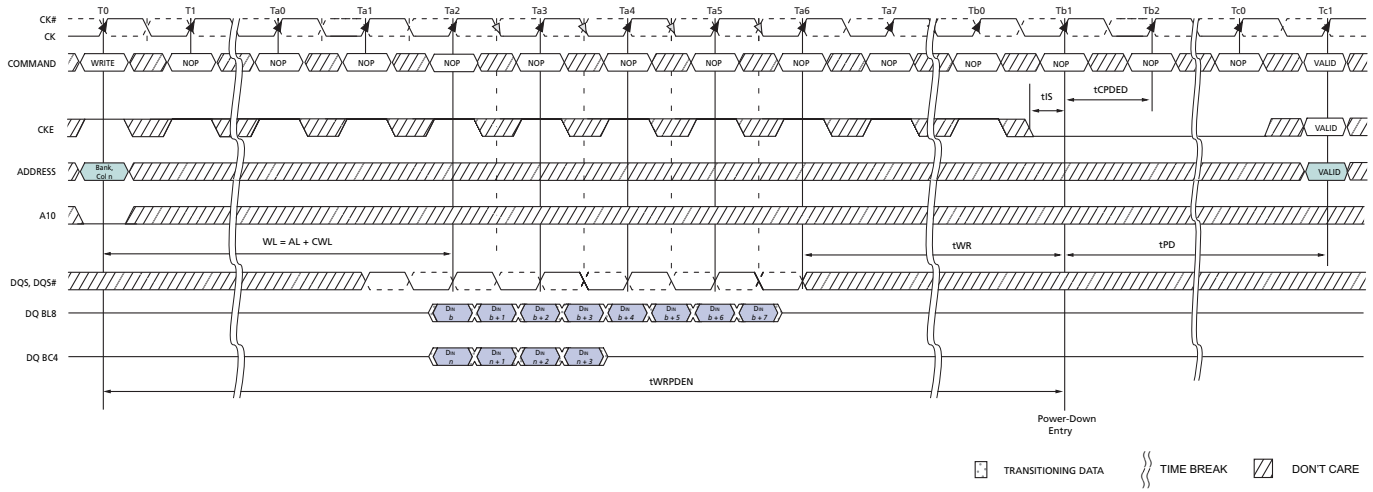



**Figure 55 — Power-Down Entry after Write**

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**4.16 Power-Down Modes (Cont'd)**
**4.16.1 Power-Down Entry and Exit (Cont'd)**

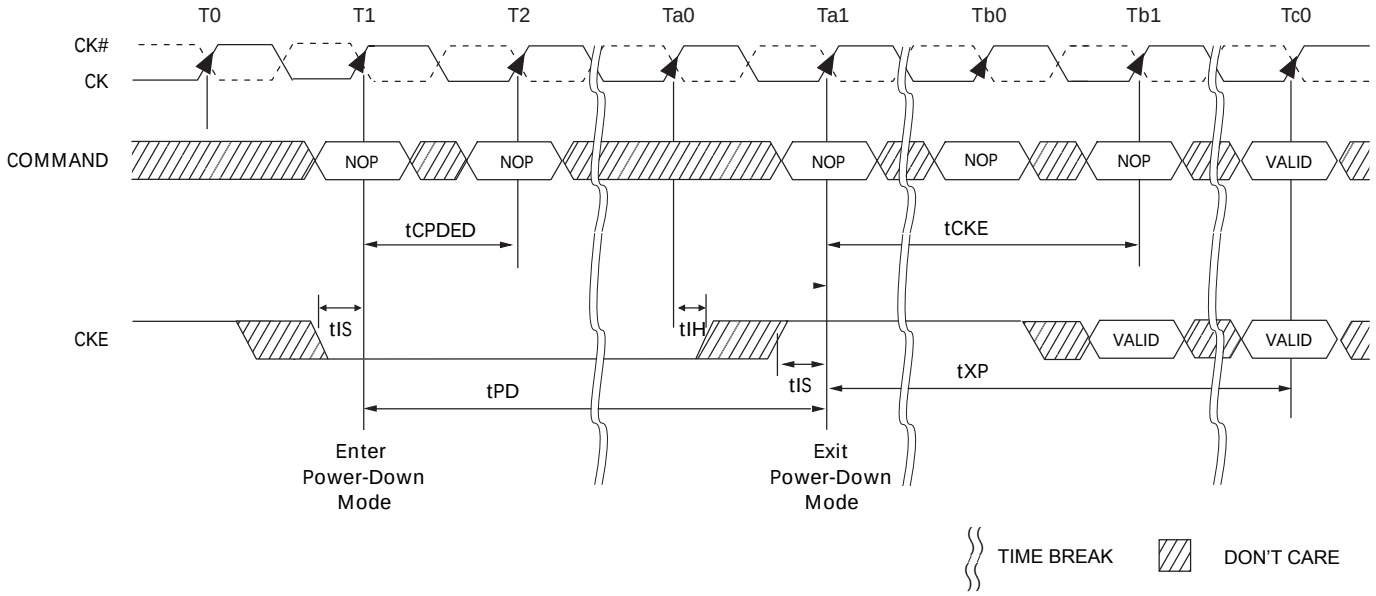



**Figure 56 — Precharge Power-Down (Fast Exit Mode) Entry and Exit**

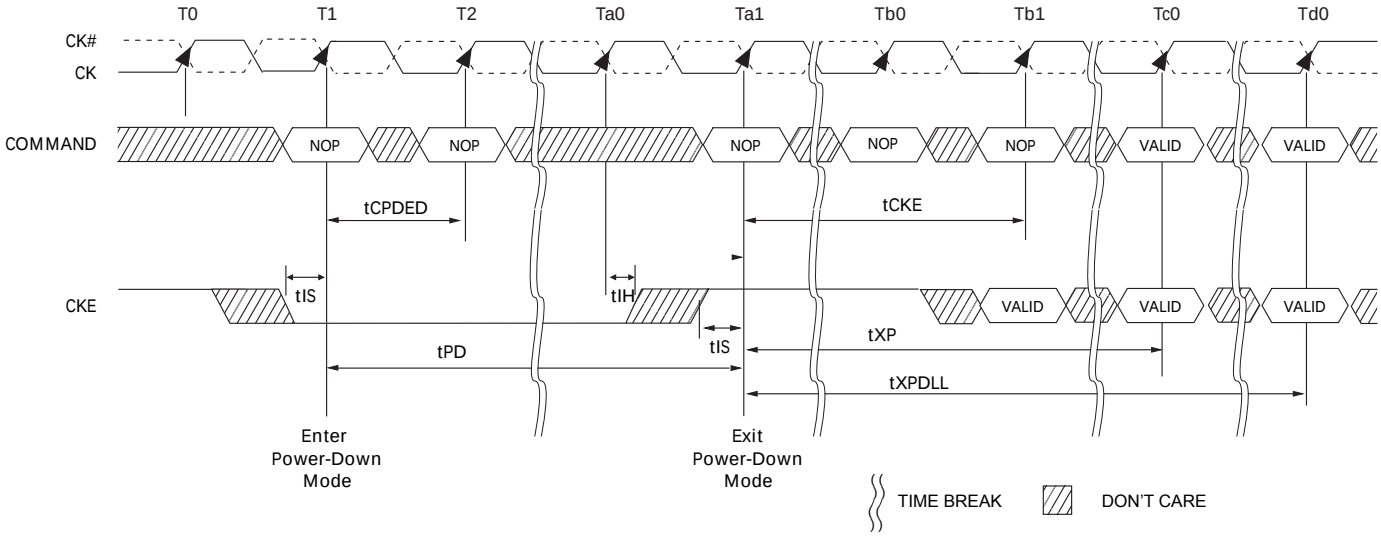



**Figure 57 — Precharge Power-Down (Slow Exit Mode) Entry and Exit**

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**4.16 Power-Down Modes (Cont'd)**
**4.16.1 Power-Down Entry and Exit (Cont'd)**

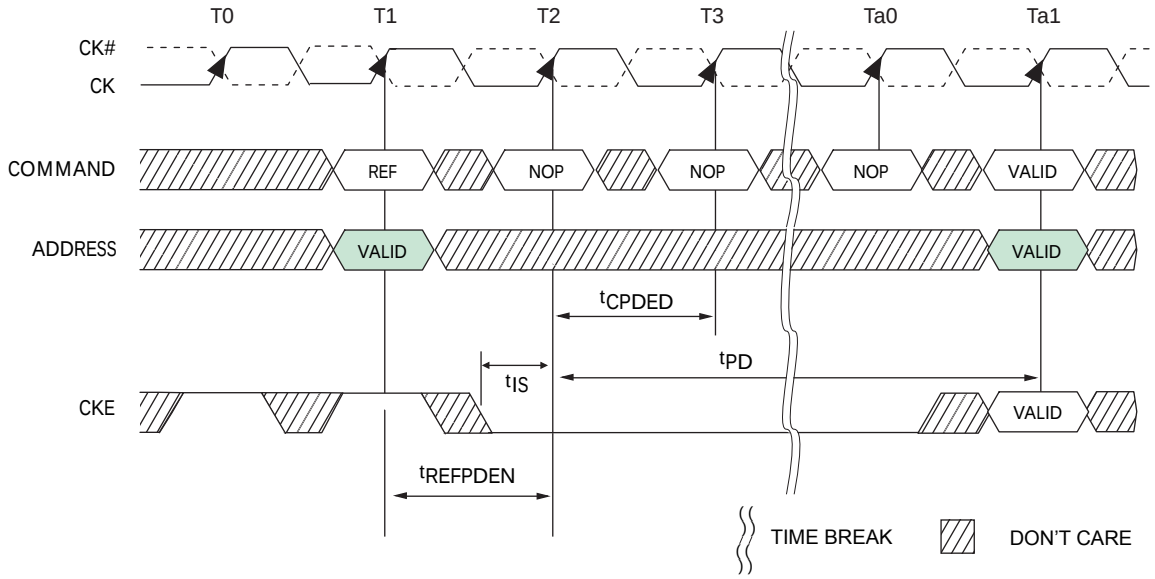



**Figure 58 — Refresh Command to Power-Down Entry**

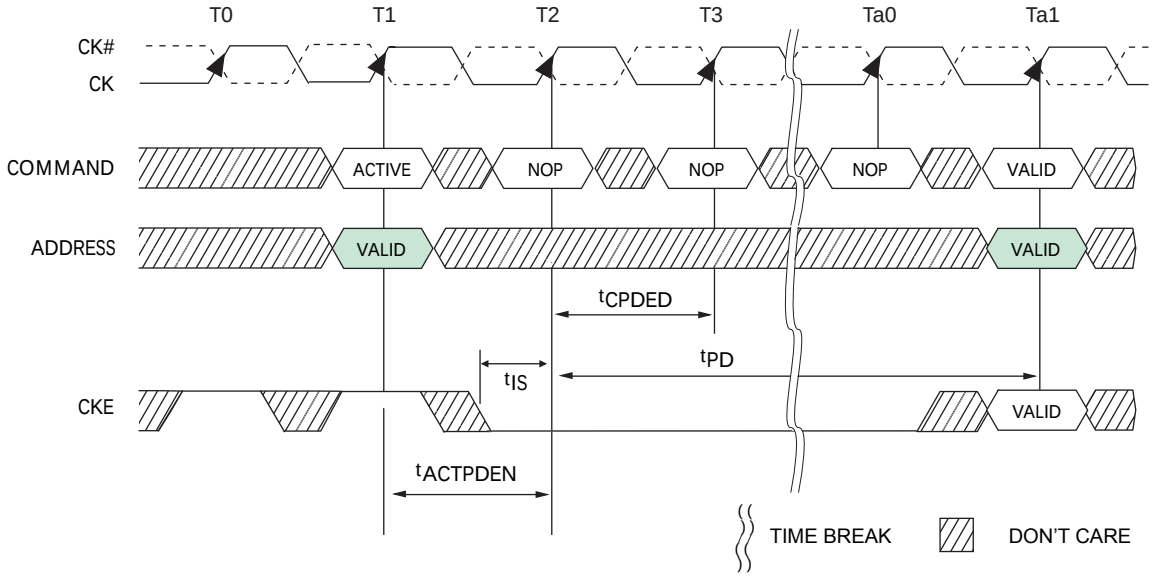



**Figure 59 — Active Command to Power-Down Entry**

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**4.16 Power-Down Modes (Cont'd)**
**4.16.1 Power-Down Entry and Exit (Cont'd)**

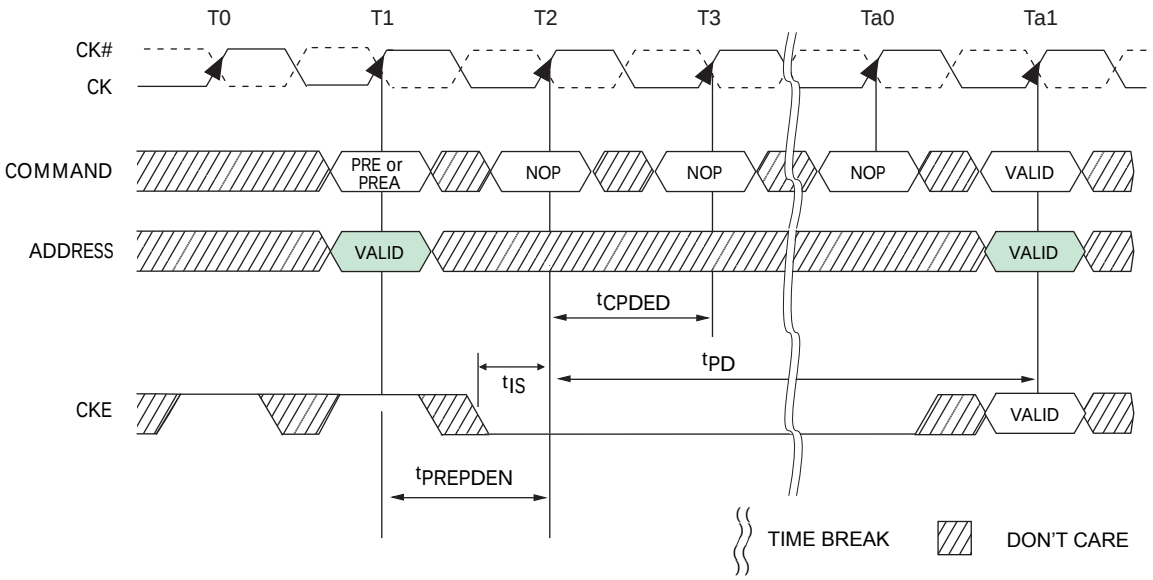



**Figure 60 — Precharge / Precharge all Command to Power-Down Entry**

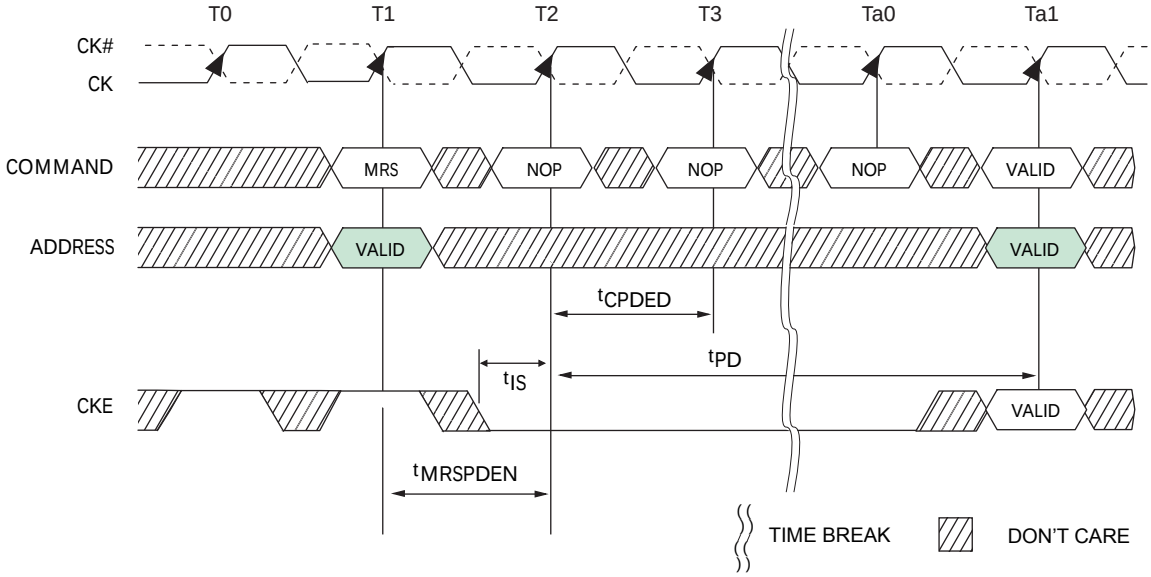



**Figure 61 — MRS Command to Power-Down Entry**

**4.16.2 Power-Down clarifications - Case 1**

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value

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**4.16 Power-Down Modes (Cont'd)**
**4.16.2 Power-Down clarifications - Case 1 (Cont'd)**

of parameter tCKE(min) as shown in Table 67, Timing Parameters by Speed Bin. A detailed example of Case 1 is shown in Figure 62.)

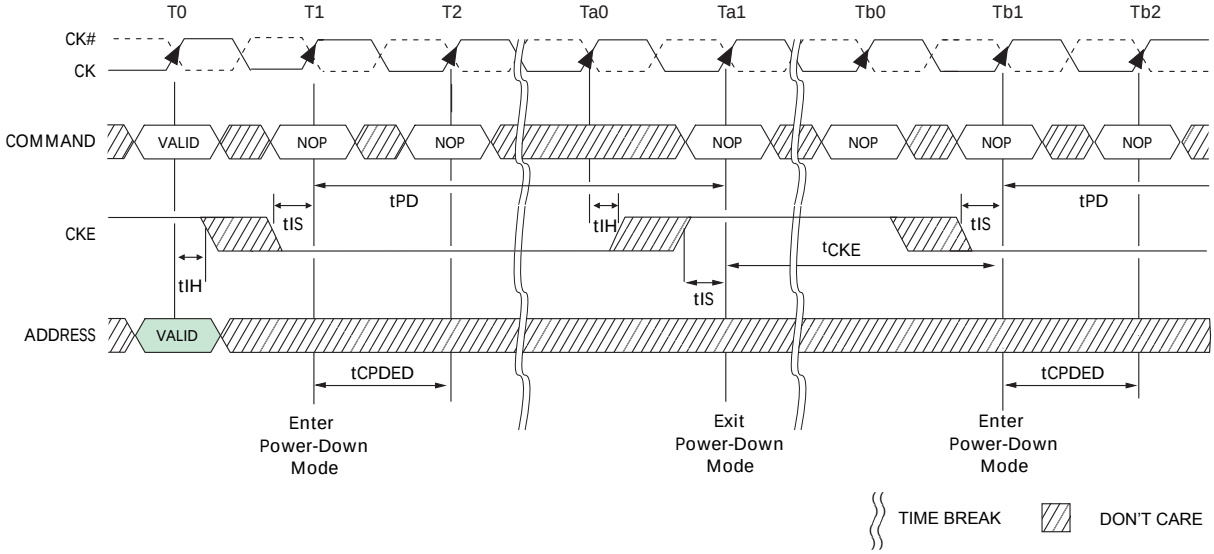



**Figure 62 — Power-Down Entry/Exit Clarifications - Case 1**

**4.16.3 Power-Down clarifications - Case 2**

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to tCKE in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met: 1) tXP must be satisfied before issuing the command. 2) tXPDLL must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 63.

)

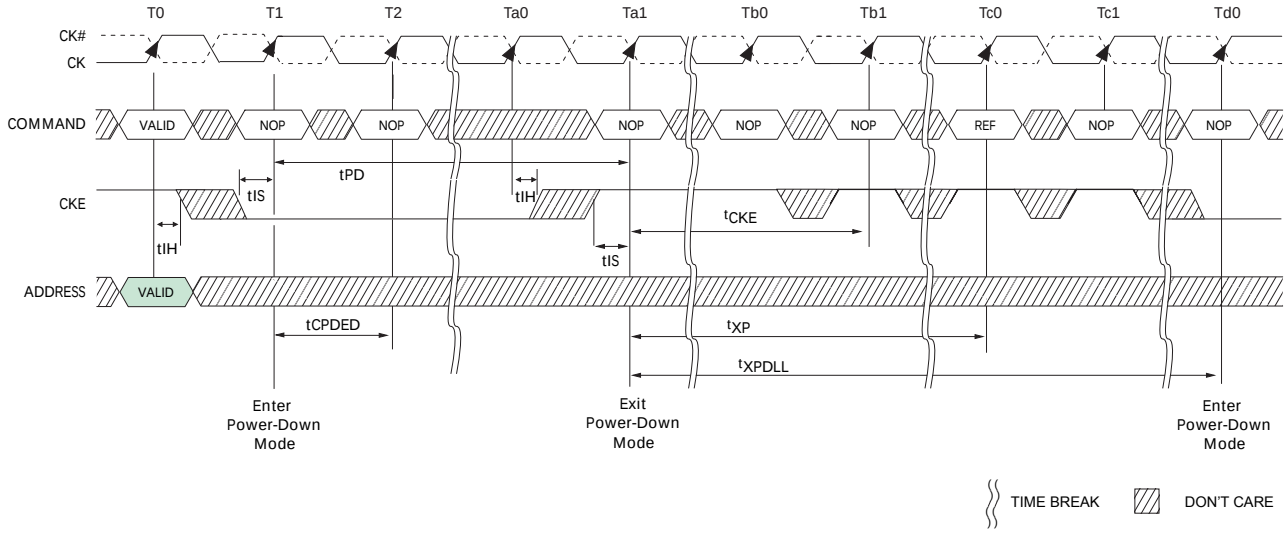



**Figure 63 — Power-Down Entry/Exit Clarifications - Case 2**

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**4.16 Power-Down Modes (Cont'd)**
**4.16.3 Power-Down clarifications - Case 2 (Cont'd)**

### 4.16.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until tRFC(min) from the Refresh command is satisfied. This means CKE can not be registered low twice within a tRFC(min) window. A detailed example of Case 3 is shown in Figure 64.

)

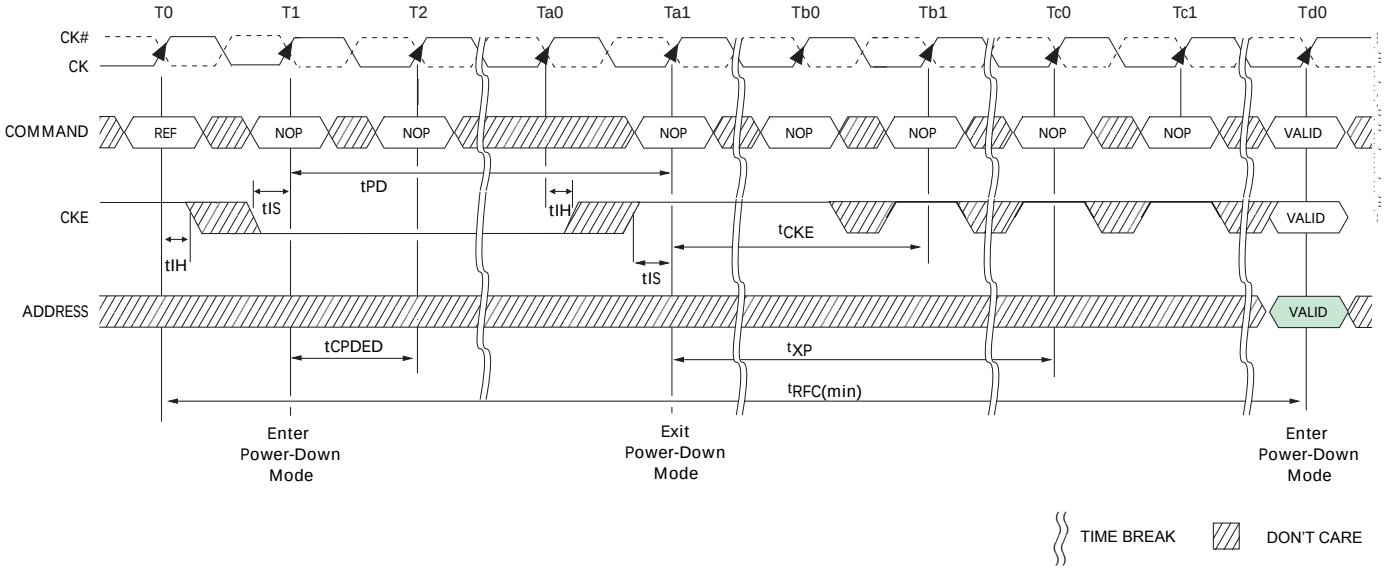



**Figure 64 — Power-Down Entry/Exit Clarifications - Case 3**

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# 5 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM for x4 and x8 configuration (and *TDQS, TDQS# for X8 configuration, when enabled via A11=1 in MR1)* via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document:

- The ODT control modes are described in 5.1.
- The ODT synchronous mode is described in 5.2
- The dynamic ODT feature is described in 5.3
- The ODT asynchronous mode is described in 5.4
- The transitions between ODT synchronous and asynchronous are described in 5.4.1 through 5.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 65.

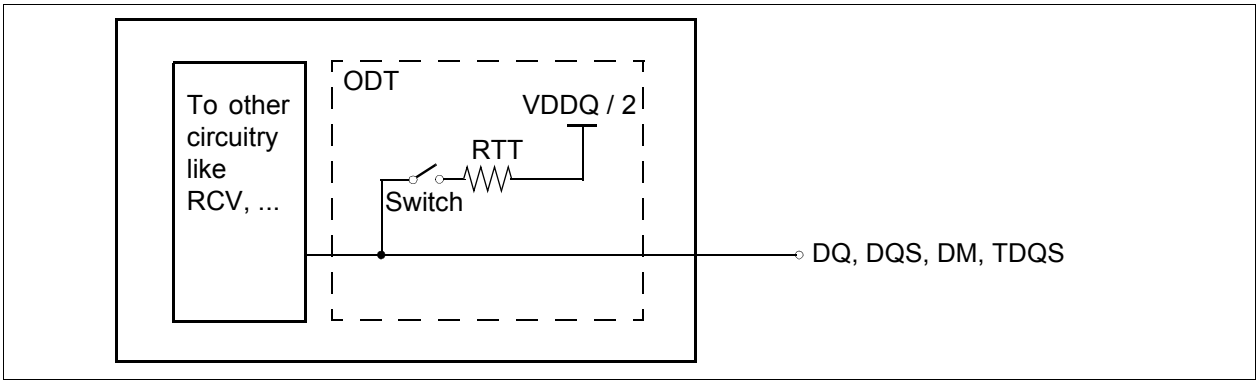



**Figure 65 — Functional Representation of ODT**

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 7 on page 22 and Figure 8 on page 25). The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

## 5.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if any of MR1 {A9, A6, A2} or MR2 {A10, A9} are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure  on page 22).

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 15.

**Table 15 — Termination Truth Table**

| ODT pin | DRAM Termination State |
|---|---|
| 0 | OFF |
| 1 | ON, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general) |

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**5 On-Die Termination (ODT) (Cont'd)**

## 5.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL - 2 .

### 5.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

**Table 16 — ODT Latency**

| Symbol | Parameter | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Unit |
|---|---|---|---|---|---|---|
| ODTLon | ODT turn on Latency | WL - 2 = CWL + AL - 2 | | | | $t_{CK}$ |
| ODTLoff | ODT turn off Latency | WL - 2 = CWL + AL - 2 | | | | |

### 5.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see also Figures 66):

ODTLon, ODTLoff, $t_{AON,min,max}$, $t_{AOF,min,max}$.

Minimum RTT turn-on time ($t_{AON}$min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time ($t_{AON}$max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time ($t_{AOF}$min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time ($t_{AOF}$max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 67). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

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**5.2 Synchronous ODT Mode (Cont'd)**
**5.2.2 Timing Parameters (Cont'd)**

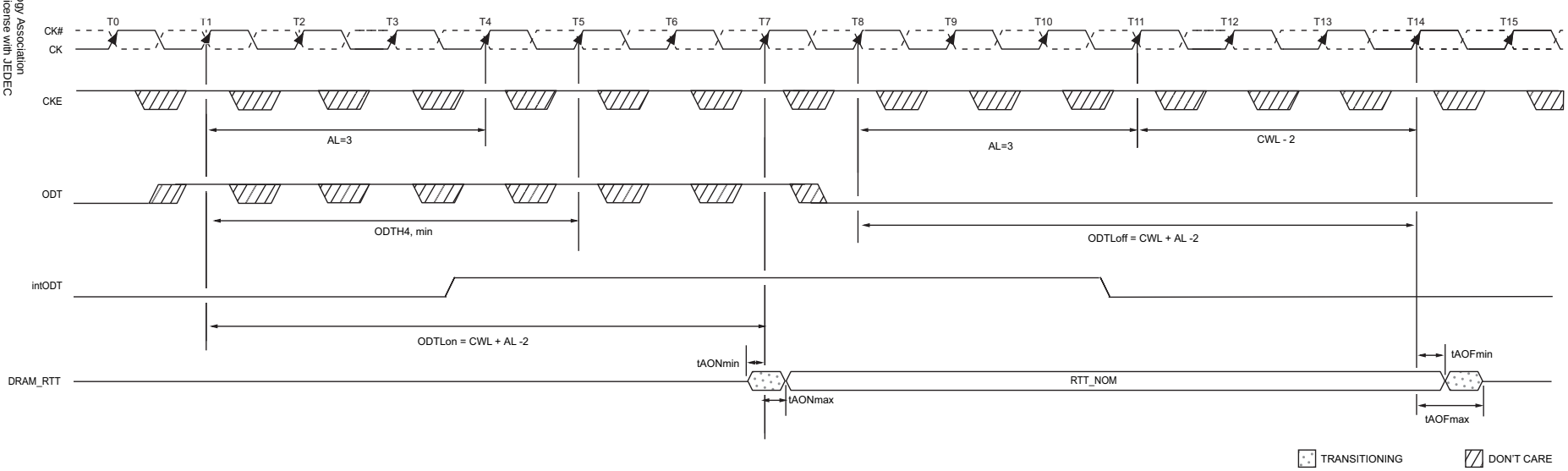



**Figure 66 — Synchronous ODT Timing Example for AL = 3; CWL = 5; ODTLon = AL + CWL - 2 = 6.0; ODTLoff = AL + CWL - 2 = 6**

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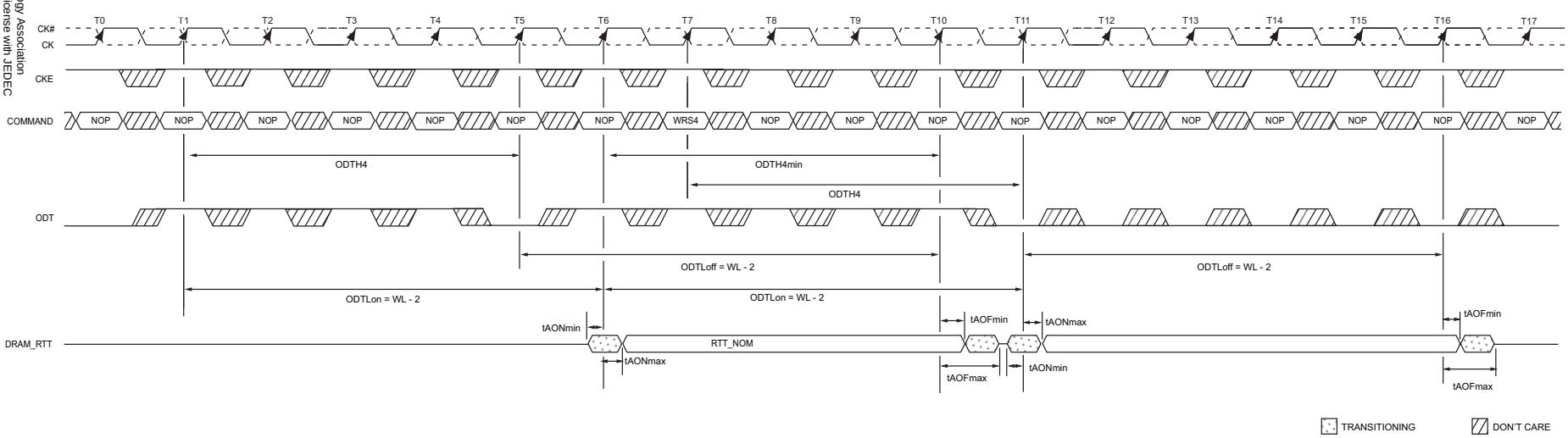



**Figure 67 — Synchronous ODT example with BL = 4, WL = 7.**

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL = 4) or ODTH8 (BL = 8) after Write command (T7 ). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6 ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

### 5.2.3 ODT during Reads

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the example below. As shown in Figure 68 below at cycle T15, DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e tHZ is early), then tAONmin timing may apply. If DRAM stops driving late (i.e tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 68.

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**5.2 Synchronous ODT Mode (Cont'd)**
**5.2.2 Timing Parameters (Cont'd)**

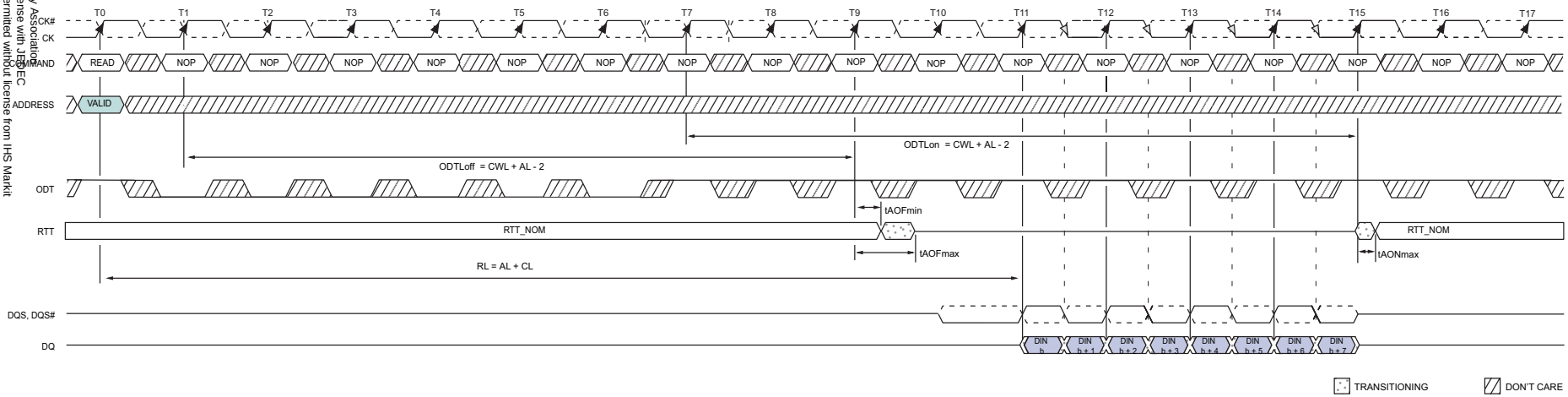



**Figure 68 — ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8)**

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## 5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

### 5.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to '1'. The function is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
  - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.
  - The value for RTT_WR is preselected via bits A[10,9] in MR2.
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 17 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 67). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

**Table 17 — Latencies and timing parameters relevant for Dynamic ODT**

| Name and Description | Abbr. | Defined from | Defined to | Definition for all DDR3 speed bins | Unit |
|---|---|---|---|---|---|
| ODT turn-on Latency | ODTLon | registering external ODT signal high | turning termination on | ODTLon = WL – 2 | $t_{CK}$ |
| ODT turn-off Latency | ODTLoff | registering external ODT signal low | turning termination off | ODTLoff = WL – 2 | $t_{CK}$ |
| ODT Latency for changing from RTT_Nom to RTT_WR | ODTLcnw | registering external write command | change RTT strength from RTT_Nom to RTT_WR | ODTLcnw = WL – 2 | $t_{CK}$ |
| ODT Latency for change from RTT_WR to RTT_Nom (BL = 4) | ODTLcwn4 | registering external write command | change RTT strength from RTT_WR to RTT_Nom | ODTLcwn4 = 4 + ODTLoff | $t_{CK}$ |

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**5.3 Dynamic ODT (Cont'd)**
**5.3.1 Functional Description (Cont'd)**

## Table 17 — Latencies and timing parameters relevant for Dynamic ODT

| Name and Description | Abbr. | Defined from | Defined to | Definition for all DDR3 speed bins | Unit |
|---|---|---|---|---|---|
| ODT Latency for change from RTT_WR to RTT_Nom (BL = 8) | ODTLcwn8 | registering external write command | change RTT strength from RTT_WR to RTT_Nom | ODTLcwn8 = 6 + ODTLoff | tCK(avg) |
| minimum ODT high time after ODT assertion | ODTH4 | registering ODT high | ODT registered low | ODTH4 = 4 | tCK(avg) |
| minimum ODT high time after Write (BL = 4) | ODTH4 | registering Write with ODT high | ODT registered low | ODTH4 = 4 | tCK(avg) |
| minimum ODT high time after Write (BL = 8) | ODTH8 | registering Write with ODT high | ODT registered low | ODTH8 = 6 | tCK(avg) |
| RTT change skew | $t_{ADC}$ | ODTLcnw ODTLcwn | RTT valid | $t_{ADC}$*(min) = 0.3 * tCK(avg)*<br>$t_{ADC}$*(max) = 0.7 * tCK(avg)* | tCK(avg) |

Note: tAOF,nom and tADC,nom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

### 5.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 18:

## Table 18 — Timing Diagrams for "Dynamic ODT"

| Figure and Page | Description |
|---|---|
| Figure 69 on page 87 | Figure 69, Dynamic ODT: Behavior with ODT being asserted before and after the write. |
| Figure 70 on page 87 | Figure 70, Dynamic ODT: Behavior without write command, AL = 0, CWL = 5. |
| Figure 71 on page 88 | Figure 71, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles. |
| Figure 72 on page 89 | Figure 72, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5. |
| Figure 73 on page 90 | Figure 73, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles. |

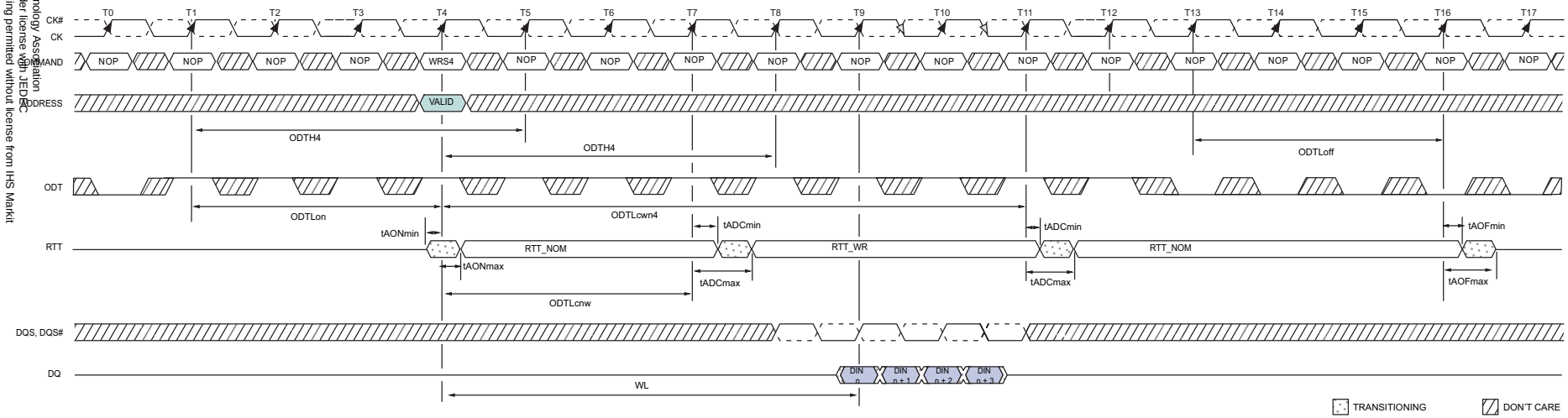
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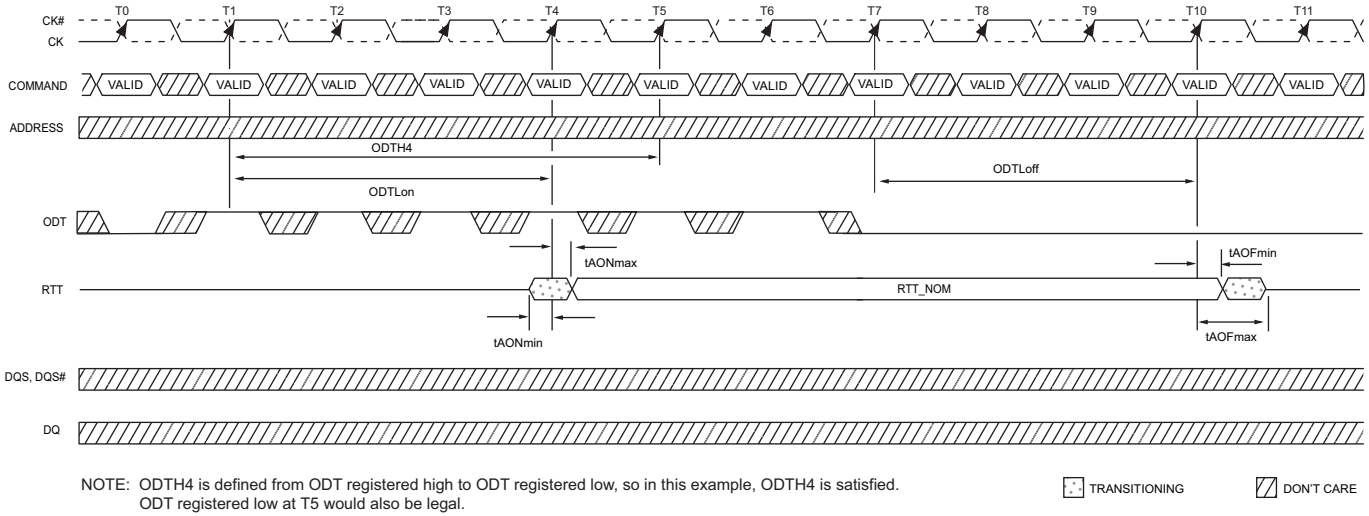
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NOTE: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODTH4 applies to first registering ODT high and to the registration of the Write command. In this example, ODTH4 would be satisfied if ODT went low at T8 (4 clocks after the Write command).

**Figure 69 — Dynamic ODT: Behavior with ODT being asserted before and after the write**




NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied. ODT registered low at T5 would also be legal.

**Figure 70 — Dynamic ODT: Behavior without write command, AL = 0, CWL = 5**

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**5.3 Dynamic ODT (Cont'd)**
**5.3.2 ODT Timing Diagrams (Cont'd)**

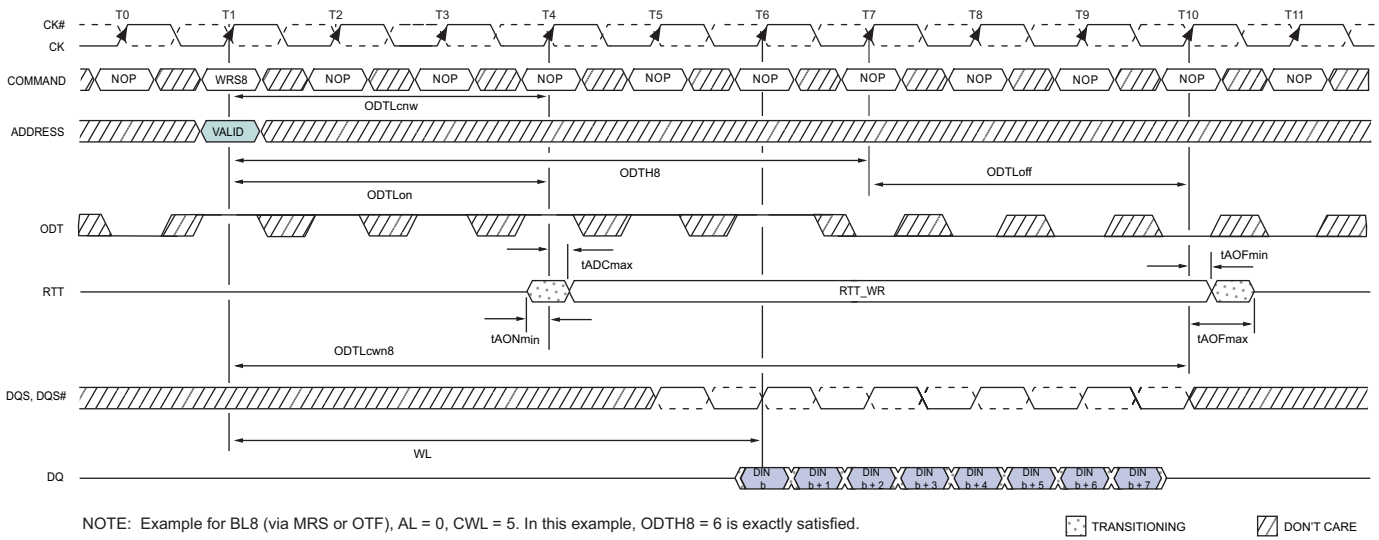
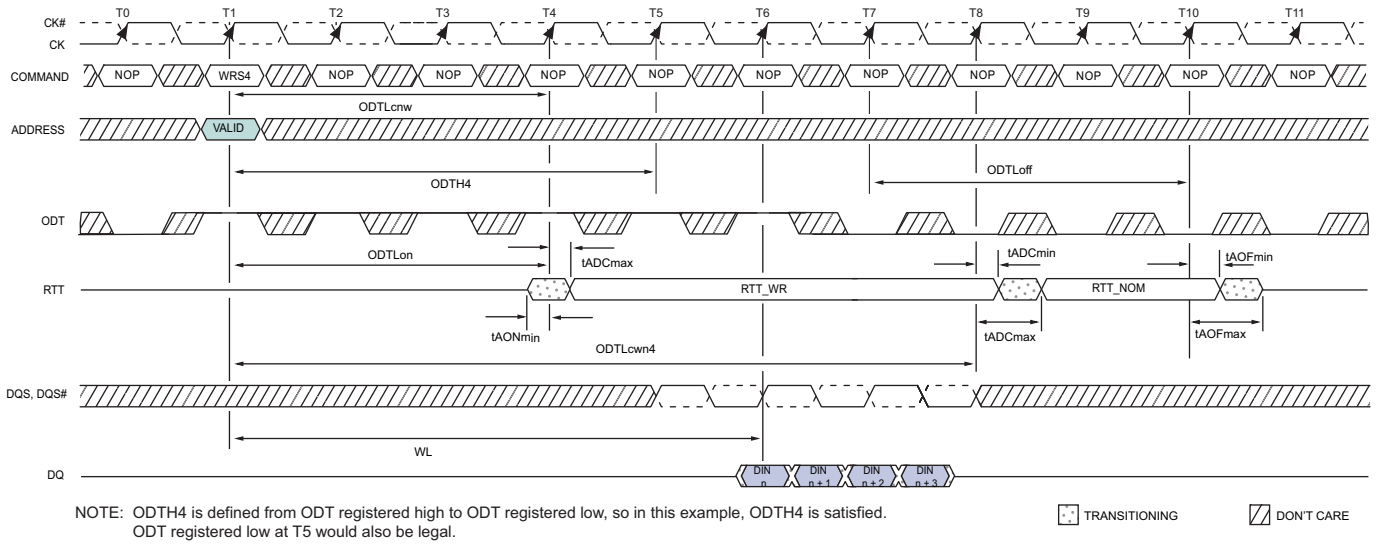



**Figure 71 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles**

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NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied. ODT registered low at T5 would also be legal.

**Figure 72 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.**

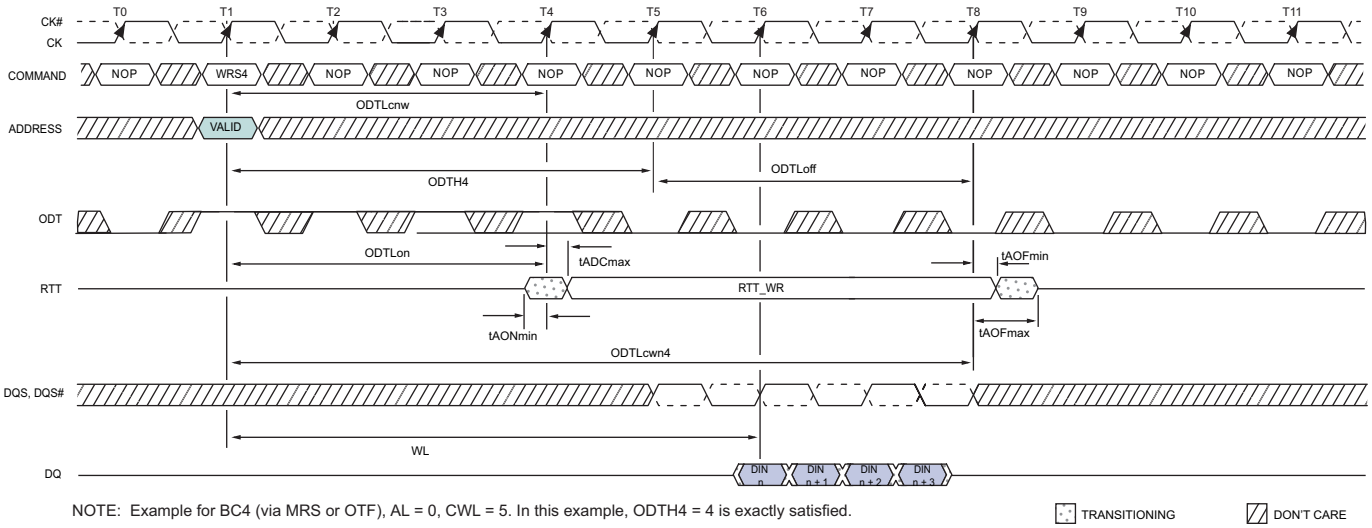


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**5.3 Dynamic ODT (Cont'd)**
**5.3.2 ODT Timing Diagrams (Cont'd)**




NOTE: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. In this example, ODTH4 = 4 is exactly satisfied.

**Figure 73 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles**

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## 5.4 Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently (comment: update editorially after everything is set and done...): Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see Figure 74): $t_{AONPD,min,max}$, $t_{AOFPD,min,max}$.

Minimum RTT turn-on time ($t_{AONPD}$min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time ($t_{AONPD}$max) is the point in time when the ODT resistance is fully on.

$t_{AONPD}$min and $t_{AONPD}$max are measured from ODT being sampled high.

Minimum RTT turn-off time ($t_{AOFPD}$min) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time ($t_{AOFPD}$max) is the point in time when the on-die termination has reached high impedance. $t_{AOFPD}$min and $t_{AOFPD}$max are measured from ODT being sampled low.

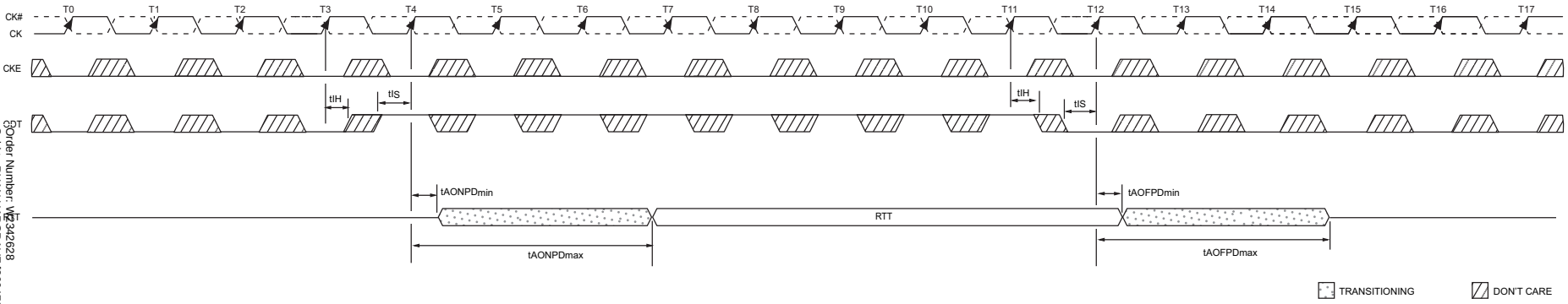



**Figure 74 — Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored**

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

**Table 19 — Asynchronous ODT Timing Parameters for all Speed Bins**

| Symbol | Description | min | max | Unit |
|---|---|---|---|---|
| $t_{AONPD}$ | Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | 1 | 9 | ns |
| $t_{AOFPD}$ | Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | 1 | 9 | ns |

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**5 On-Die Termination (ODT) (Cont'd)**
**5.4 Asynchronous ODT Mode (Cont'd)**

### 5.4.1 Synchronous to Asynchronous ODT Mode Transitions

**Table 20 — ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period**

| Description | min | max |
|---|---|---|
| ODT to RTT turn-on delay | min{ ODTLon * tCK + tAONmin; tAONPDmin } | max{ ODTLon * tCK + tAONmax; tAONPDmax } |
| | min{ (WL - 2) * tCK + tAONmin; tAONPDmin } | max{ (WL - 2) * tCK + tAONmax; tAONPDmax } |
| ODT to RTT turn-off delay | min{ ODTLoff * tCK +tAOFmin; tAOFPDmin } | max{ ODTLoff * tCK + tAOFmax; tAOFPDmax } |
| | min{ (WL - 2) * tCK +tAOFmin; tAOFPDmin } | max{ (WL - 2) * tCK + tAOFmax; tAOFPDmax } |
| tANPD | WL -1 | |

### 5.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

This transition period ends when CKE is first registered low and starts tANPD before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends tRFC(min) after the Refresh command. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered low.

ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD}$min and (ODTLon*$t_{CK}$ + $t_{AON}$min) and as late as the larger of $t_{AONPD}$max and (ODTLon*$t_{CK}$ + $t_{AON}$max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of $t_{AOFPD}$min and (ODTLoff*$t_{CK}$ + $t_{AOF}$min) and as late as the larger of $t_{AOFPD}$max and (ODTLoff*$t_{CK}$ + $t_{AOF}$max). See Figure 20 and Figure 75. Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 75 shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

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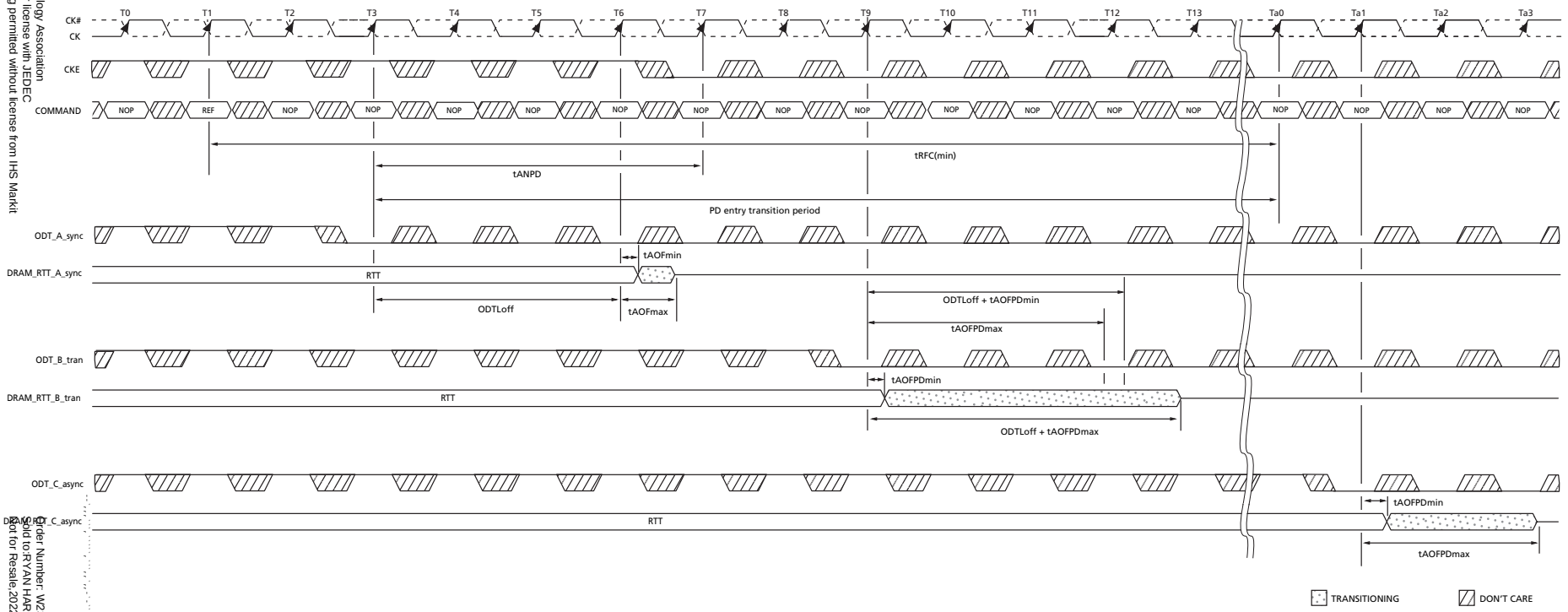



**Figure 75 — Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL = 0; CWL = 5; tANPD = WL - 1 = 4)**

### 5.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL - 1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD}$min and (ODTLon*$t_{CK}$ + $t_{AON}$min) and as late as the larger of $t_{AONPD}$max and (ODTLon*$t_{CK}$ + $t_{AON}$max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of $t_{AOFPD}$min and (ODTLoff*$t_{CK}$ + $t_{AOF}$min) and as late as the larger of $t_{AOFPD}$max and (ODTLoff*$t_{CK}$ + $t_{AOF}$max). See Table 20.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 76 shows the three different cases: ODT_C, asynchronous response before $t_{ANPD}$; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.



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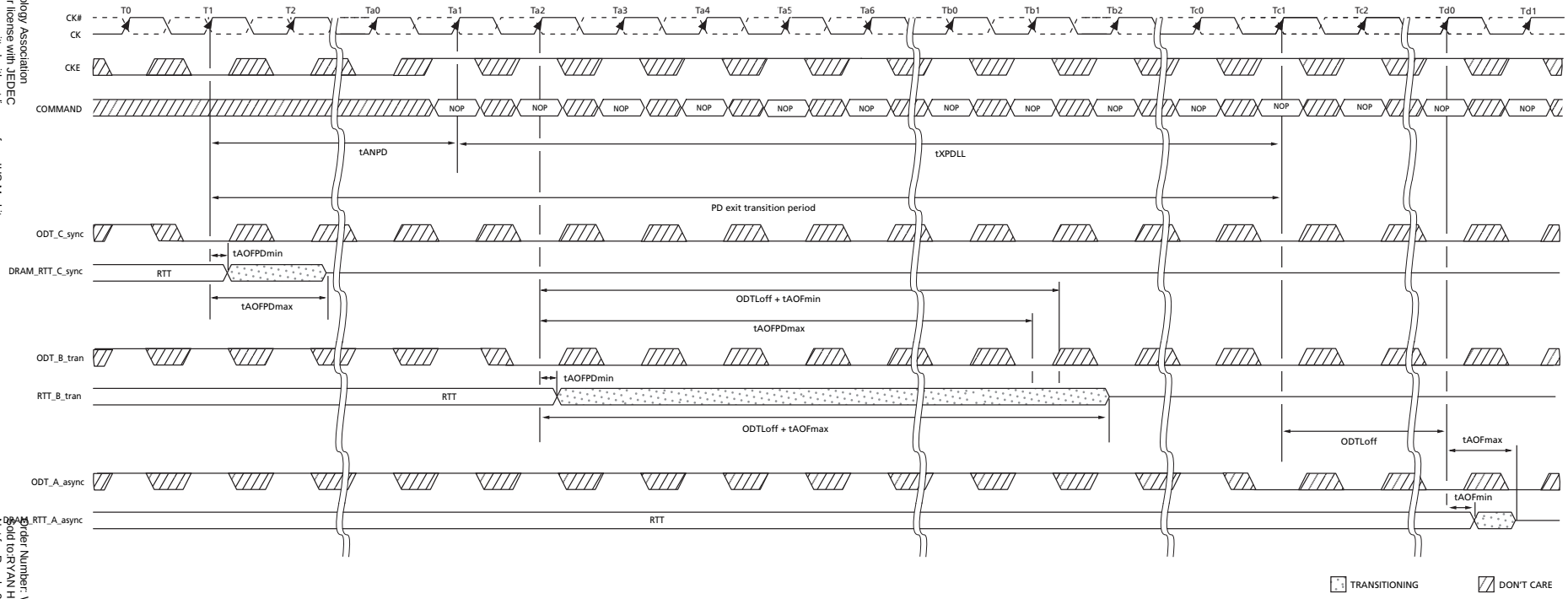



**Figure 76 — Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; tANPD = WL - 1 = 9)**

### 5.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap (see Figure 77). In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that in the bottom part of Figure 77 it is assumed that there was no Refresh command in progress when Idle state was entered.

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**5.4 Asynchronous ODT Mode (Cont'd)**

**5.4.4 Asynch to Synch ODT Mode during short CKE high and short CKE low periods (Cont'd)**

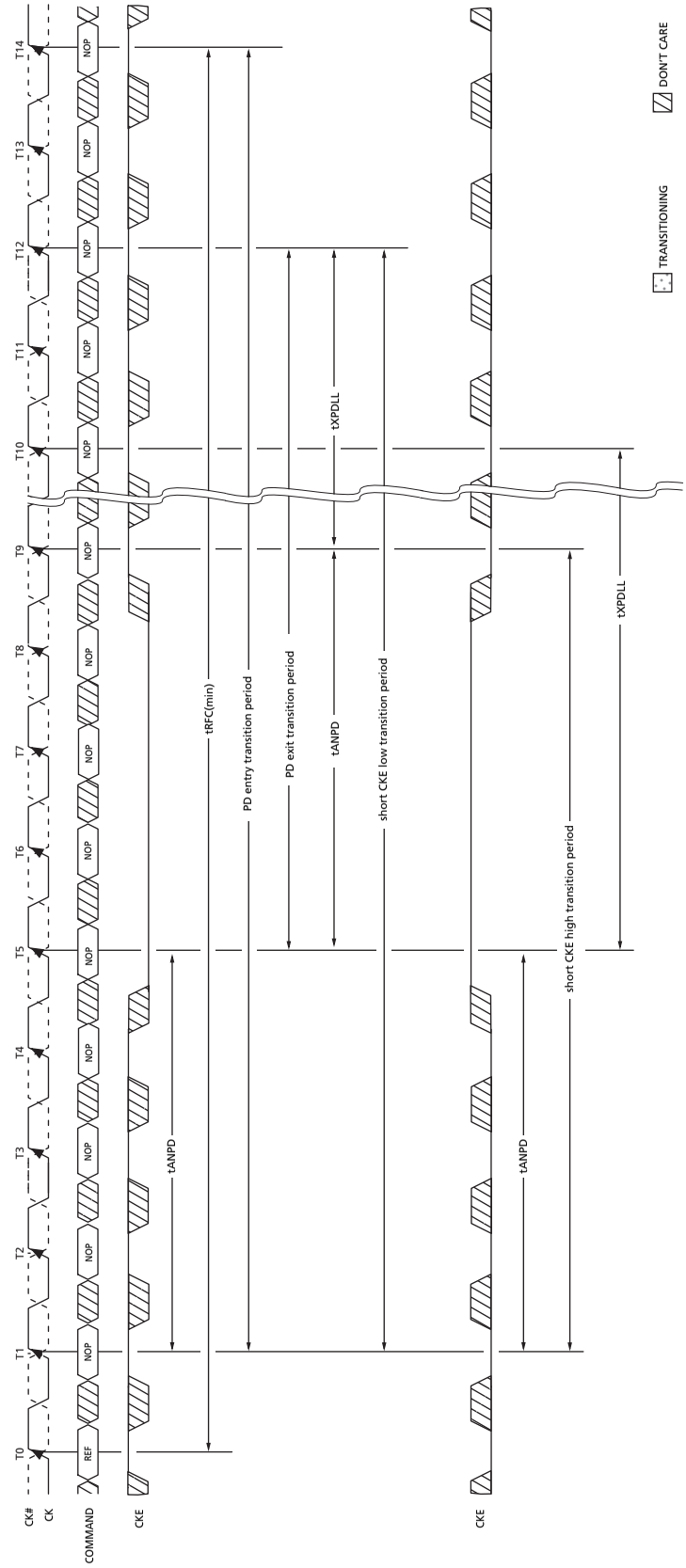



**Figure 77 — Transition period for short CKE cycles, entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4)**

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## 5.5 ZQ Calibration Commands

### 5.5.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See Table 6 — "Command Truth Table" on page 29 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

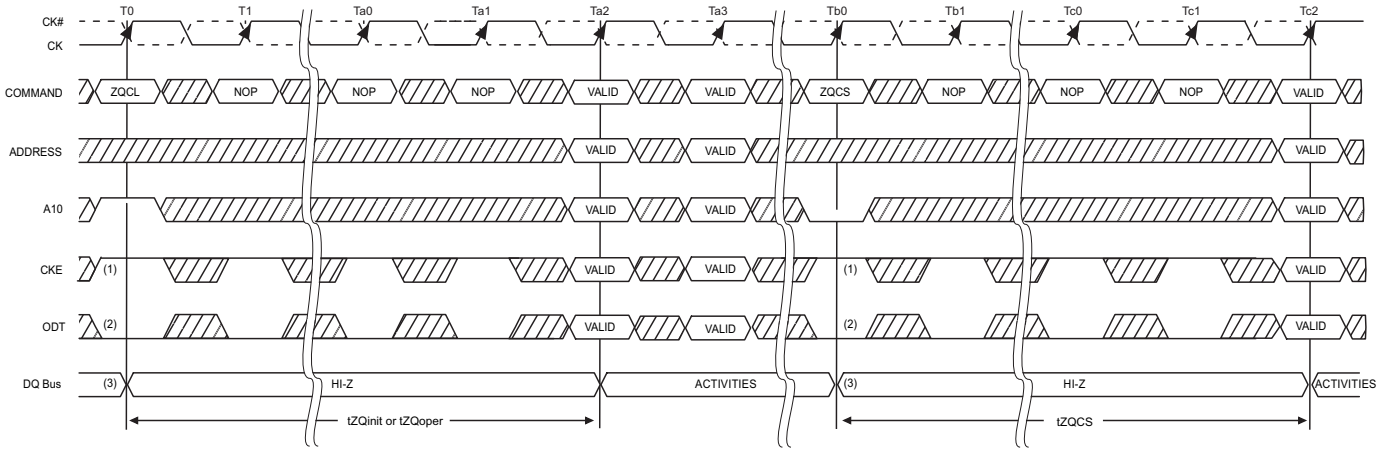
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**5 On-Die Termination (ODT) (Cont'd)**
**5.5 ZQ Calibration Commands (Cont'd)**

### 5.5.2 ZQ Calibration Timing




NOTES: 1. CKE must be continuously registered high during the calibration procedure.

2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.

3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

**Figure 78 — ZQ Calibration Timing**

### 5.5.3 ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited (See Table 61 — "Input / Output Capacitance" on page 141).

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# 6 Absolute Maximum Ratings

## 6.1 Absolute Maximum DC Ratings

**Table 21 — Absolute Maximum DC Ratings**

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | -0.4 V ~ 1.975 V | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.4 V ~ 1.975 V | V | 1,3 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to Vss | -0.4 V ~ 1.975 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1,2 |

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

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**6 Absolute Maximum Ratings (Cont'd)**

## 6.2 DRAM Component Operating Temperature Range

**Table 22 — Temperature Range**

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | $^{o}C$ | 1, 2 |
| | Extended Temperature Range (Optional) | 85 to 95 | $^{o}C$ | 1, 3 |

Notes:
1. Operating Temperature $T_{OPER}$ is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 $^{o}C$ under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 $^{o}C$ and 95 $^{o}C$ case temperature. Full specifications are supported in this range, but the following additional conditions apply:

   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = $0_b$ and MR2 A7 = $1_b$) or enable the optional Auto Self-Refresh mode (MR2 A6 = $1_b$ and MR2 A7 = $0_b$). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

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# 7 AC & DC Operating Conditions

## 7.1 Recommended DC Operating Conditions

**Table 23 — Recommended DC Operating Conditions**

| Symbol | Parameter | Rating | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $V_{DD}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1, 2 |
| $V_{DDQ}$ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V | 1, 2 |

Notes: 1.Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

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# 8 AC and DC Input Measurement Levels

## 8.1 AC and DC Logic Input Levels for Single-Ended Signals

### Table 24 — Single Ended AC and DC Input Levels

| Symbol | Parameter | DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| VIH(DC) | DC input logic high | Vref + 0.100 | VDD | V | 1 |
| VIL(DC) | DC input logic low | VSS | Vref - 0.100 | V | 1 |
| VIH(AC) | AC input logic high | Vref + 0.175 | - | V | 1, 2 |
| VIL(AC) | AC input logic low | - | Vref - 0.175 | V | 1, 2 |
| $V_{RefDQ(DC)}$ | Reference Voltage for DQ, DM inputs | 0.49 * VDD | 0.51 * VDD | V | 3, 4 |
| $V_{RefCA(DC)}$ | Reference Voltage for ADD, CMD inputs | 0.49 * VDD | 0.51 * VDD | V | 3, 4 |

Notes:
1. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
2. See 9.6 “Overshoot and Undershoot Specifications” on page 113.
3. The ac peak noise on $V_{Ref}$ may not allow $V_{Ref}$ to deviate from $V_{Ref(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages $V_{RefCA}$ and $V_{RefDQ}$ are illustrated in Figure 79. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. ($V_{Ref}$ stands for $V_{RefCA}$ and $V_{RefDQ}$ likewise).

$V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 24. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than +/- 1% VDD.

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**8 AC and DC Input Measurement Levels (Cont'd)**
**8.1 AC and DC Logic Input Levels for Single-Ended Signals (Cont'd)**

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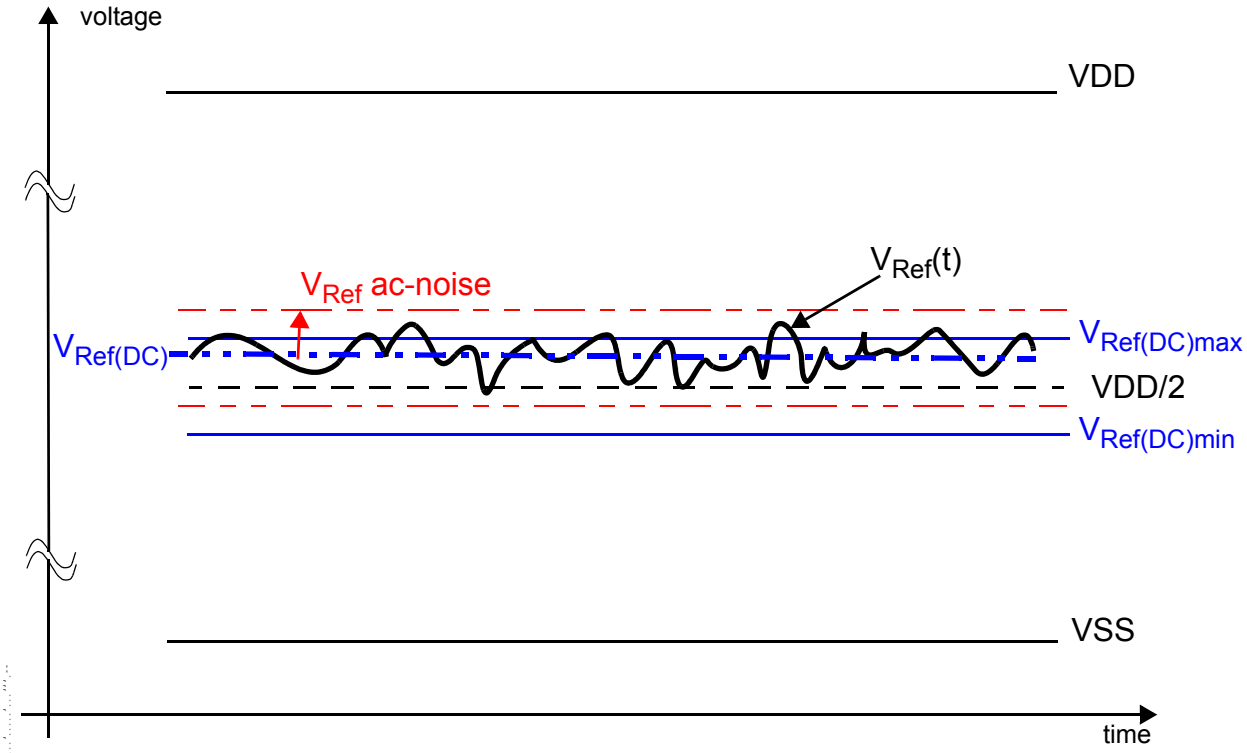



**Figure 79 — Illustration of $V_{Ref(DC)}$ tolerance and $V_{Ref}$ ac-noise limits**

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on $V_{Ref}$.

"$V_{Ref}$ " shall be understood as $V_{Ref(DC)}$, as defined in Figure 79.

This clarifies that dc-variations of $V_{Ref}$ affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with $V_{Ref}$ ac-noise. Timing and voltage effects due to ac-noise on $V_{Ref}$ up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

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## 8.2 AC and DC Logic Input Levels for Differential Signals

### 8.2.1 Differential signal definition

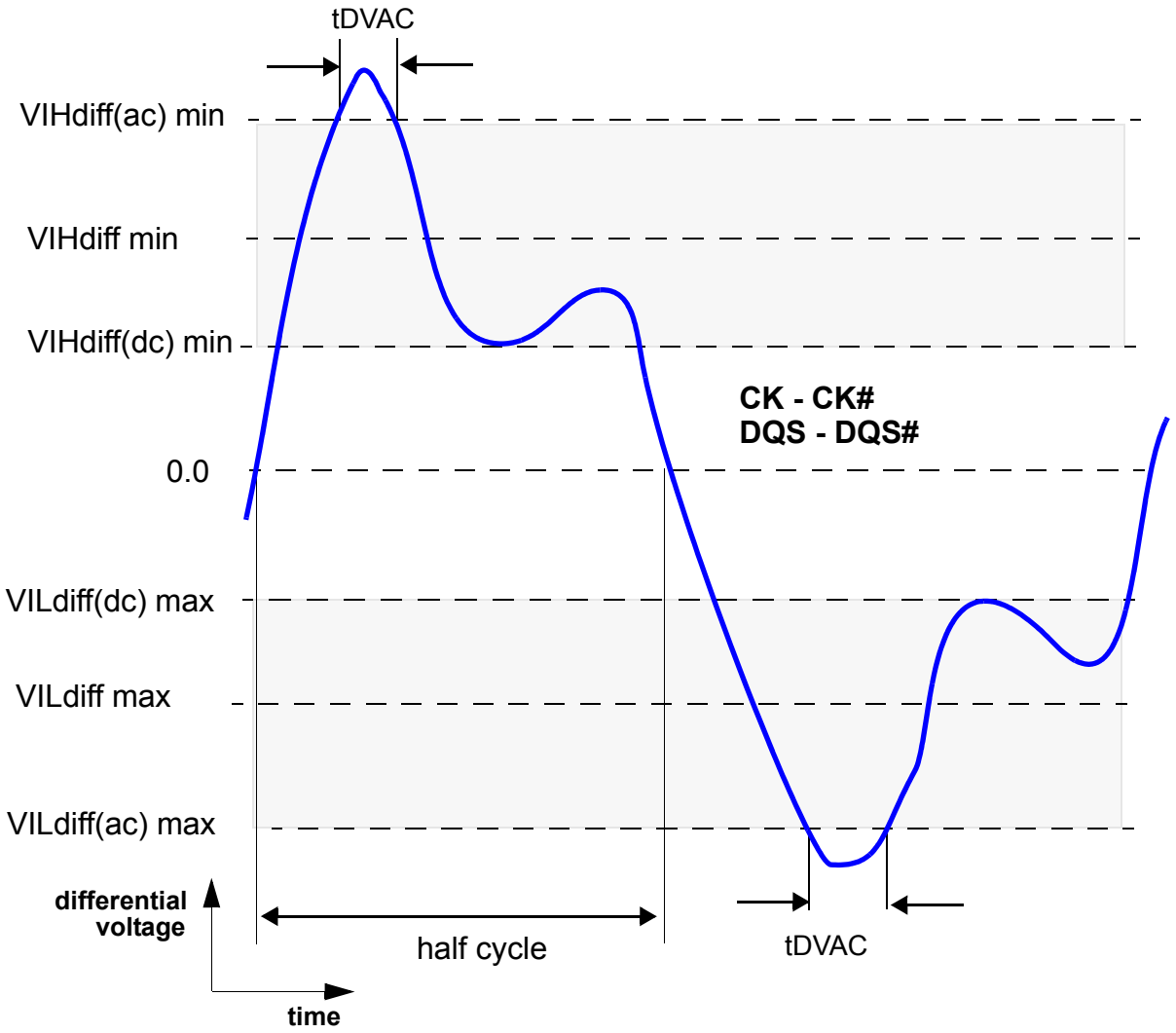



**Figure 80 — Definition of differntial ac-swing and "time above ac-level" $t_{DVAC}$**

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**8 AC and DC Input Measurement Levels (Cont'd)**
**8.2 AC and DC Logic Input Levels for Differential Signals (Cont'd)**

### 8.2.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

**Table 25 — Differential AC and DC Input Levels**

| Symbol | Parameter | DDR3-800, 1066, 1333, & 1600 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IHdiff}$ | Differential input high | + 0.200 | note 3 | V | 1 |
| $V_{ILdiff}$ | Differential input logic low | Note 3 | - 0.200 | V | 1 |
| $V_{IHdiff(ac)}$ | Differential input high ac | 2 x (VIH(ac) - Vref) | Note 3 | V | 2 |
| $V_{ILdiff(ac)}$ | Differential input low ac | note 3 | 2 x (Vref - VIL(ac)) | V | 2 |

1. Used to define a differential signal slew-rate.
2. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 113

**Table 26 — Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS#**

| Slew Rate [V/ns] | tDVAC [ps] @ \|VIH/Ldiff(ac)\| = 350mV | | tDVAC [ ps ] @ \|VIH/Ldiff(ac)\| = 300mV | |
|---|---|---|---|---|
| | min | max | min | max |
| > 4.0 | 75 | - | 175 | - |
| 4.0 | 57 | - | 170 | - |
| 3.0 | 50 | - | 167 | - |
| 2.0 | 38 | - | 163 | - |
| 1.8 | 34 | - | 162 | - |
| 1.6 | 29 | - | 161 | - |
| 1.4 | 22 | - | 159 | - |
| 1.2 | 13 | - | 155 | - |
| 1.0 | 0 | - | 150 | - |
| < 1.0 | 0 | - | 150 | - |

### 8.2.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels ( VIH(ac) / VIL(ac) ) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin / VSELmax (approximately the ac-levels ( VIH(ac) / VIL(ac) ) for DQ signals) in every half-cycle preceeding and following a valid transition.

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**8.2 AC and DC Logic Input Levels for Differential Signals (Cont'd)**
**8.2.3 Single-ended requirements for differential signals (Cont'd)**

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if VIH150(ac)/VIL150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and CK#

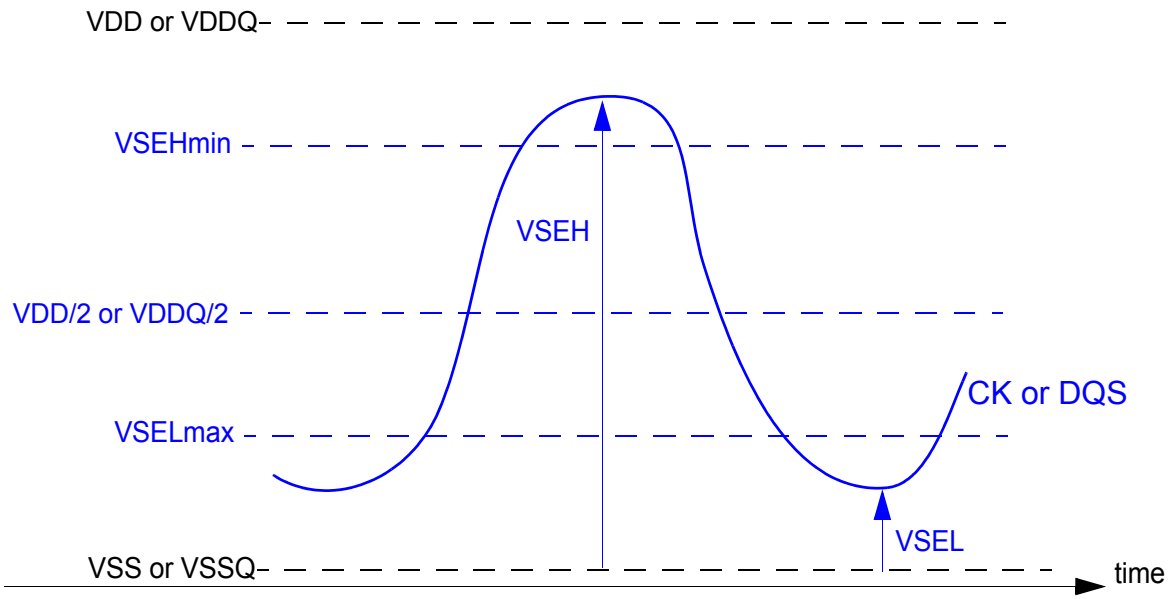



**Figure 81 — Single-ended requirement for differential signals.**

Note that while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

**Table 27 — Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#**

| Symbol | Parameter | DDR3-800, 1066, 1333, & 1600 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| VSEH | Single-ended highlevel for strobes | VIH(ac) - VREFDQ + VDDQ / 2 | note 3 | V | 1, 2 |
| | Single-ended high-level for CK, CK# | VIH(ac) - VREFCA + VDD / 2 | note 3 | V | 1, 2 |
| VSEL | Single-ended lowlevel for strobes | note 3 | VIL(ac) + VREFDQ - VDDQ / 2 | V | 1, 2 |
| | Single-ended lowlevel for CK, CK# | note 3 | VIL(ac) + VREFCA - VDD / 2 | V | 1, 2 |

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**8.2 AC and DC Logic Input Levels for Differential Signals (Cont'd)**
**8.2.3 Single-ended requirements for differential signals (Cont'd)**

**Table 27 — Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#**

| Symbol | Parameter | DDR3-800, 1066, 1333, & 1600 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| | 1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.<br>2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here<br>3. These values are not defined, however they single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 113 | | | | |

## 8.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 28. The differential input cross point voltage $V_{IX}$ is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

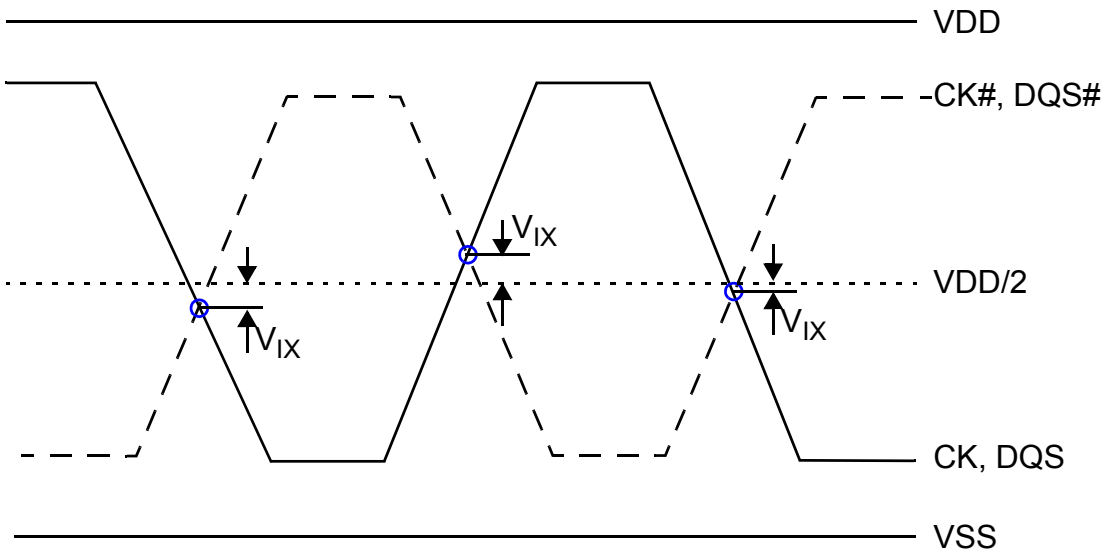



**Figure 82 — Vix Definition**

**Table 28 — Cross point voltage for differential input signals (CK, DQS)**

| Symbol | Parameter | DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IX}$ | Differential Input Cross Point Voltage relative to VDD/2 | - 150 | 150 | mV | |

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**8 AC and DC Input Measurement Levels (Cont'd)**

## 8.4 Slew Rate Definitions for Single Ended Input Signals

### 8.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

### 8.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef.

**Table 29 — Single-ended Input Slew Rate Definition**

| Description | Measured | | Defined by | Applicable for |
|---|---|---|---|---|
| | from | to | | |
| Input slew rate for rising edge | $V_{Ref}$ | $V_{IH(AC)min}$ | $\frac{V_{IH(AC)min} - V_{Ref}}{DeltaTRS}$ | Setup ($t_{IS}$, $t_{DS}$) |
| Input slew rate for falling edge | $V_{Ref}$ | $V_{IL(AC)max}$ | $\frac{V_{Ref} - V_{IL(AC)max}}{DeltaTFS}$ | |
| Input slew rate for rising edge | $V_{IL(DC)max}$ | $V_{Ref}$ | $\frac{V_{Ref} - V_{IL(DC)max}}{DeltaTFH}$ | Hold ($t_{IH}$, $t_{DH}$) |
| Input slew rate for falling edge | $V_{IH(DC)min}$ | $V_{Ref}$ | $\frac{V_{IH(DC)min} - V_{Ref}}{DeltaTRH}$ | |

This nominal slew rate applies for linear signal waveforms.

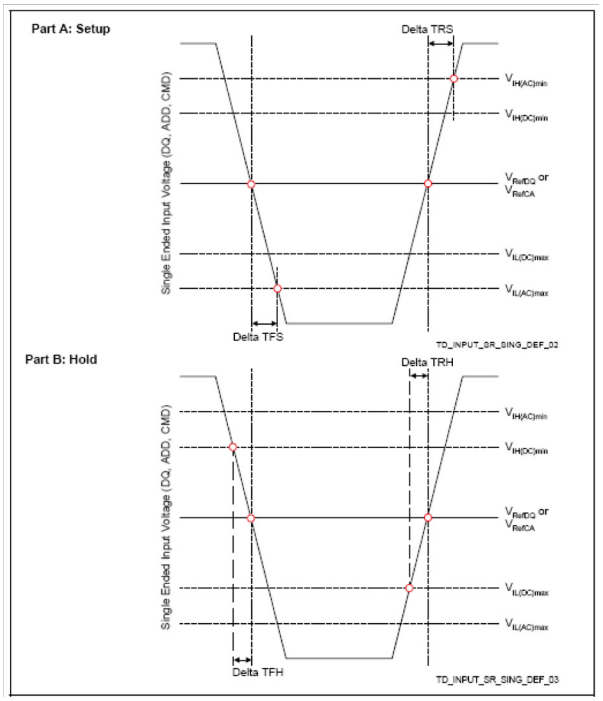



**Figure 83 — Input Nominal Slew Rate Definition for Single-Ended Signals**

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## 8.5 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table 30 and Figure 84.

**Table 30 — Differential Input Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential input slew rate for rising edge (CK - CK# and DQS - DQS#). | $V_{ILdiffmax}$ | $V_{ILdiffmin}$ | $\frac{V_{IHdiffmin} - V_{ILdiffmax}}{DeltaTRdiff}$ |
| Differential input slew rate for falling edge (CK - CK# and DQS - DQS#). | $V_{IHdiffmin}$ | $V_{IHdiffmax}$ | $\frac{V_{IHdiffmin} - V_{ILdiffmax}}{DeltaTFdiff}$ |
| **Note:** The differential signal (i.e. CK - CK# and DQS - DQS#) must be linear between these thresholds. | | | |

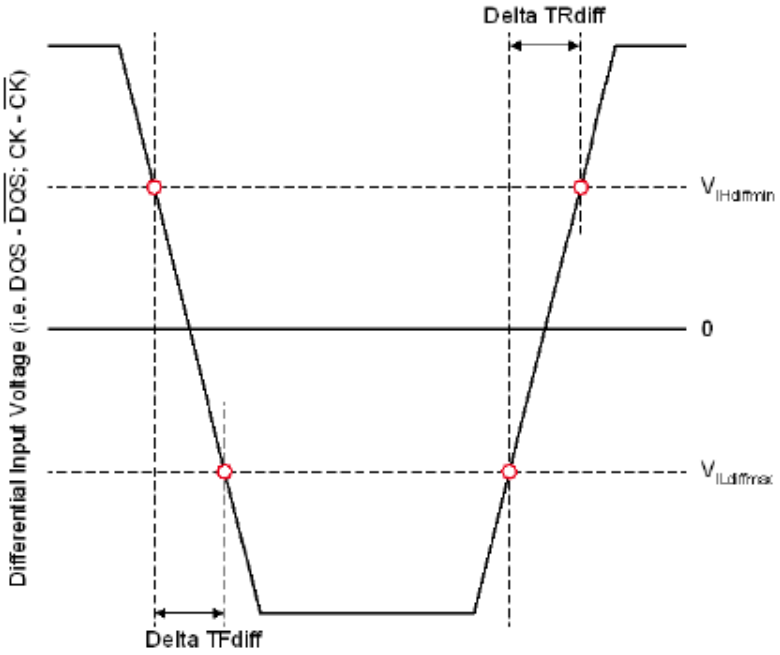



**Figure 84 — Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#**

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# 9 AC and DC Output Measurement Levels

## 9.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

**Table 31 — Single-ended AC and DC Output Levels**

| Symbol | Parameter | DDR3-800, 1066, 1333, and 1600 | Unit | Notes |
|---|---|---|---|---|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | 0.8 x $V_{DDQ}$ | V | |
| $V_{OM(DC)}$ | DC output mid measurement level (for IV curve linearity) | 0.5 x $V_{DDQ}$ | V | |
| $V_{OL(DC)}$ | DC output low measurement level (for IV curve linearity) | 0.2 x $V_{DDQ}$ | V | |
| $V_{OH(AC)}$ | AC output high measurement level (for output SR) | $V_{TT}$ + 0.1 x $V_{DDQ}$ | V | 1 |
| $V_{OL(AC)}$ | AC output low measurement level (for output SR) | $V_{TT}$ - 0.1 x $V_{DDQ}$ | V | 1 |

Notes: 1. The swing of ± 0.1 × $V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT}$ = $V_{DDQ}$/2.

## 9.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of differential signals.

**Table 32 — Differential AC and DC Output Levels**

| Symbol | Parameter | DDR3-800, 1066, 1333, and 1600 | Unit | Notes |
|---|---|---|---|---|
| $V_{OHdiff(AC)}$ | AC differential output high measurement level (for output SR) | + 0.2 x $V_{DDQ}$ | V | 1 |
| $V_{OLdiff(AC)}$ | AC differential output low measurement level (for output SR) | - 0.2 x $V_{DDQ}$ | V | 1 |

Notes: 1. The swing of ± 0.2 × $V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT}$ = $V_{DDQ}$/2 at each of the differential outputs.

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## 9.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 33 and Figure 85.

**Table 33 — Single-ended Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Single-ended output slew rate for rising edge | $V_{OL(AC)}$ | $V_{OH(AC)}$ | $\frac{V_{OH(AC)} - V_{OL(AC)}}{DeltaTRse}$ |
| Single-ended output slew rate for falling edge | $V_{OH(AC)}$ | $V_{OL(AC)}$ | $\frac{V_{OH(AC)} - V_{OL(AC)}}{DeltaTFse}$ |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |

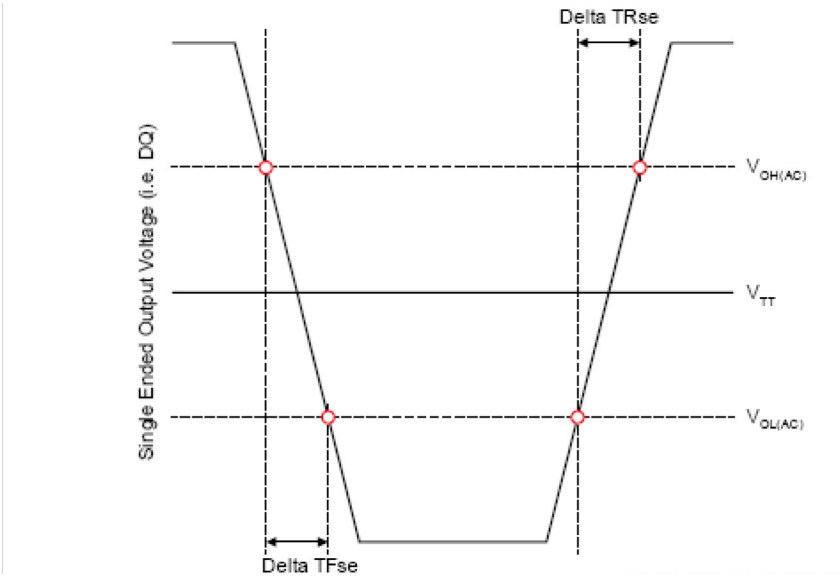



**Figure 85 — Single Ended Output Slew Rate Definition**

**Table 34 — Output Slew Rate (single-ended)**

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Single-ended Output Slew Rate | SRQse | 2.5 | 5 | 2.5 | 5 | 2.5 | 5 | TBD | 5 | V/ns |
| Description: SR: Slew Rate<br>**Q: Query Output (like in DQ, which stands for Data-in, Query-Output)**<br>**se: Single-ended Signals**<br>For Ron = RZQ/7 setting | | | | | | | | | | |

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**9 AC and DC Output Measurement Levels (Cont'd)**

## 9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 35 and Figure 86.

**Table 35 — Differential Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential output slew rate for rising edge | $V_{OLdiff(AC)}$ | $V_{OHdiff(AC)}$ | $\frac{V_{OHdiff(AC)} - V_{OLdiff(AC)}}{DeltaTRdiff}$ |
| Differential output slew rate for falling edge | $V_{OHdiff(AC)}$ | $V_{OLdiff(AC)}$ | $\frac{V_{OHdiff(AC)} - V_{OLdiff(AC)}}{DeltaTFdiff}$ |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |

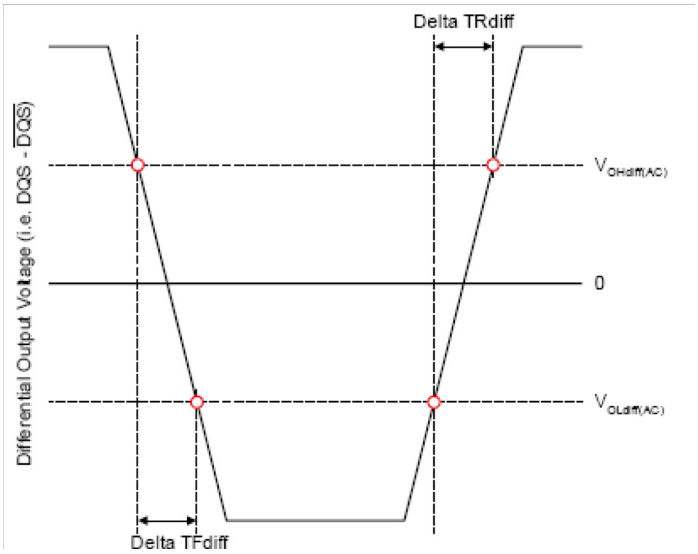



**Figure 86 — Differential Output Slew Rate Definition**

**Table 36 — Differential Output Slew Rate**

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Differential Output Slew Rate | SRQdiff | 5 | 10 | 5 | 10 | 5 | 10 | TBD | 10 | V/ns |
| Description:<br>SR: Slew Rate<br>Q: Query Output (like in DQ, which stands for Data-in, Query-Output)<br>diff: Differential Signals<br>For Ron = RZQ/7 setting | | | | | | | | | | |

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## 9.5 Reference Load for AC Timing and Output Slew Rate

Figure 87 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

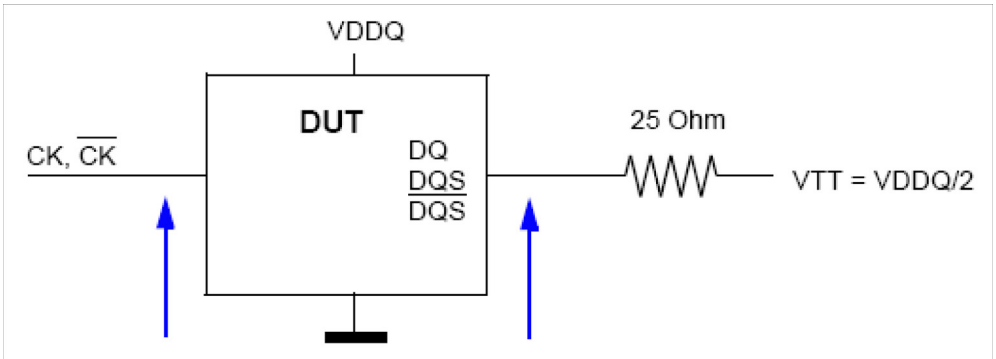



**Figure 87 — Reference Load for AC Timing and Output Slew Rate**

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**9 AC and DC Output Measurement Levels (Cont'd)**

## 9.6 Overshoot and Undershoot Specifications

### 9.6.1 Address and Control Overshoot and Undershoot Specifications

**Table 37 — AC Overshoot/Undershoot Specification for Address and Control Pins**

| | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Units |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area. (See Figure 88) | 0.4 | 0.4 | 0.4 | 0.4 | V |
| Maximum peak amplitude allowed for undershoot area. (See Figure 88) | 0.4 | 0.4 | 0.4 | 0.4 | V |
| Maximum overshoot area above VDD (See Figure 88) | 0.67 | 0.5 | 0.4 | 0.33 | V-ns |
| Maximum undershoot area below VSS (See Figure 88) | 0.67 | 0.5 | 0.4 | 0.33 | V-ns |
| (A0-A15, BA0-BA3, CS#, RAS#, CAS#, WE#, CKE, ODT) | | | | | |

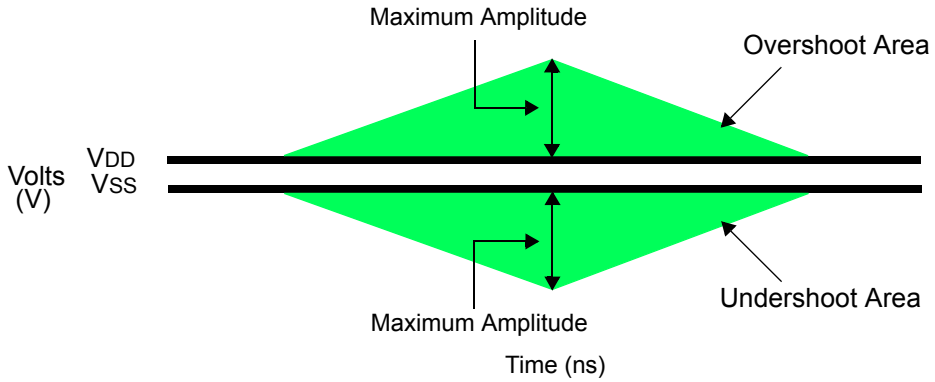



**Figure 88 — Address and Control Overshoot and Undershoot Definition**

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**9 AC and DC Output Measurement Levels (Cont'd)**
**9.6 Overshoot and Undershoot Specifications (Cont'd)**

### 9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

**Table 38 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask**

| | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Units |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area. (See Figure 89) | 0.4 | 0.4 | 0.4 | 0.4 | V |
| Maximum peak amplitude allowed for undershoot area. (See Figure 89) | 0.4 | 0.4 | 0.4 | 0.4 | V |
| Maximum overshoot area above VDDQ (See Figure 89) | 0.25 | 0.19 | 0.15 | 0.13 | V-ns |
| Maximum undershoot area below VSSQ (See Figure 89) | 0.25 | 0.19 | 0.15 | 0.13 | V-ns |
| (CK, CK#, DQ, DQS, DQS#, DM) | | | | | |

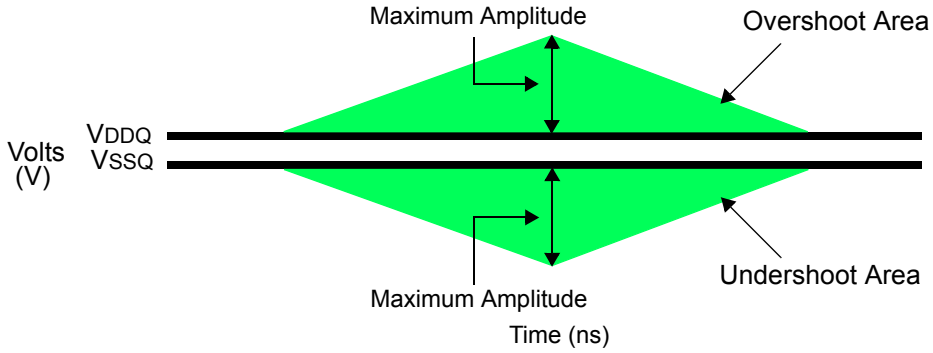



**Figure 89 — Clock, Data, Strobe and Mask Overshoot and Undershoot Definition**

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**9 AC and DC Output Measurement Levels (Cont'd)**

## 9.7 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure 90. Output driver impedance $RON$ is defined by the value of the external reference resistor RZQ as follows:

$RON_{34}$ = $R_{ZQ}$ / 7 (nominal 34.3 Ω ±10% with nominal $R_{ZQ}$ = 240 Ω)

The individual pull-up and pull-down resistors ($RON_{Pu}$ and $RON_{Pd}$) are defined as follows:

$$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ under the condition that $RON_{Pd}$ is turned off (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that $RON_{Pu}$ is turned off (2)

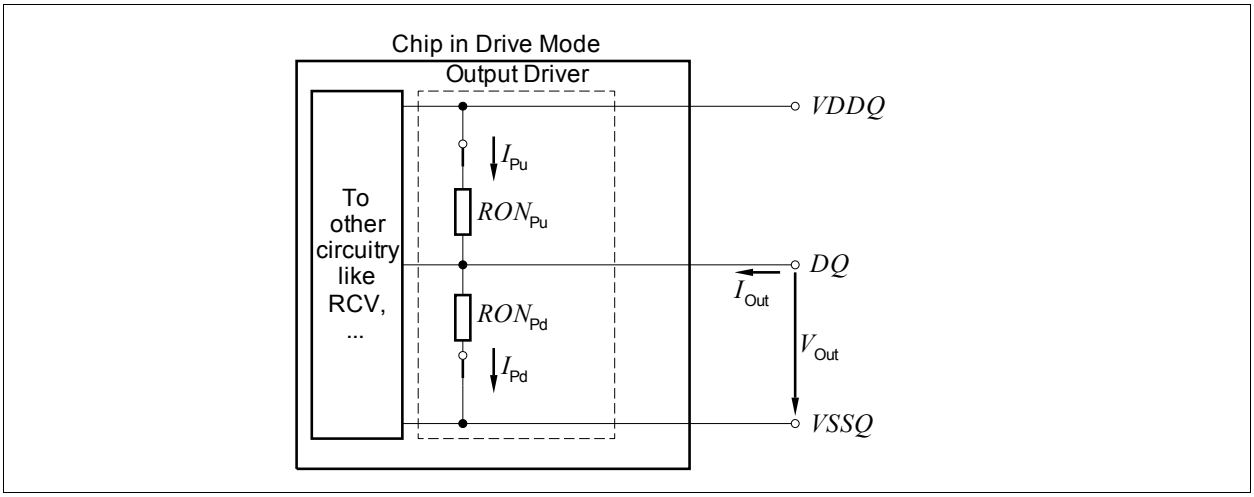



**Figure 90 — Output Driver: Definition of Voltages and Currents**

**Table 39 — Output Driver DC Electrical Characteristics, assuming $R_{ZQ}$ = 240 Ω ; entire operating temperature range; after proper ZQ calibration**

| $RON_{Nom}$ | Resistor | $V_{Out}$ | min | nom | max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 34 Ω | $RON_{34Pd}$ | $V_{OLdc}$ = 0.2 × $V_{DDQ}$ | 0.6 | 1.0 | 1.1 | $R_{ZQ}$/7 | 1, 2, 3 |
| | | $V_{OMdc}$ = 0.5 × $V_{DDQ}$ | 0.9 | 1.0 | 1.1 | $R_{ZQ}$/7 | 1, 2, 3 |
| | | $V_{OHdc}$ = 0.8 × $V_{DDQ}$ | 0.9 | 1.0 | 1.4 | $R_{ZQ}$/7 | 1, 2, 3 |
| | $RON_{34Pu}$ | $V_{OLdc}$ = 0.2 × $V_{DDQ}$ | 0.9 | 1.0 | 1.4 | $R_{ZQ}$/7 | 1, 2, 3 |
| | | $V_{OMdc}$ = 0.5 × $V_{DDQ}$ | 0.9 | 1.0 | 1.1 | $R_{ZQ}$/7 | 1, 2, 3 |
| | | $V_{OHdc}$ = 0.8 × $V_{DDQ}$ | 0.6 | 1.0 | 1.1 | $R_{ZQ}$/7 | 1, 2, 3 |
| Mismatch between pull-up and pull-down, $MM_{PuPd}$ | | $V_{OMdc}$ 0.5 × $V_{DDQ}$ | -10 | | +10 | % | 1, 2, 4 |

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or volt-

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**9 AC and DC Output Measurement Levels (Cont'd)**
**9.7 34 ohm Output Driver DC Electrical Characteristics (Cont'd)**

age changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.
4. Measurement definition for mismatch between pull-up and pull-down, $MM_{PuPd}$:
   Measure $RON_{Pu}$ and $RON_{Pd}$, both at 0.5 * $V_{DDQ}$:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

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**9 AC and DC Output Measurement Levels (Cont'd)**
**9.7 34 ohm Output Driver DC Electrical Characteristics (Cont'd)**

### 9.7.1 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 40 and Table 41.

**$\Delta$T = T - T(@calibration); $\Delta$V= VDDQ - VDDQ(@calibration); VDD = VDDQ**

**Note:** $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

## Table 40 — Output Driver Sensitivity Definition

| | min | max | unit |
|---|---|---|---|
| RONPU@ $V_{OHdc}$ | 0.6 - $dR_{ON}dTH*\|DT\|$ - $dR_{ON}dVH*\|DV\|$ | 1.1 + $dR_{ON}dTH*\|DT\|$ + $dR_{ON}dVH*\|DV\|$ | RZQ/7 |
| RON@ $V_{OMdc}$ | 0.9 - $dR_{ON}dTM*\|DT\|$ - $dR_{ON}dVM*\|DV\|$ | 1.1 + $dR_{ON}dTM*\|DT\|$ + $dR_{ON}dVM*\|DV\|$ | RZQ/7 |
| RONPD@ $V_{OLdc}$ | 0.6 - $dR_{ON}dTL*\|DT\|$ - $dR_{ON}dVL*\|DV\|$ | 1.1 + $dR_{ON}dTL*\|DT\|$ + $dR_{ON}dVL*\|DV\|$ | RZQ/7 |

## Table 41 — Output Driver Voltage and Temperature Sensitivity

| | min | max | unit |
|---|---|---|---|
| $dR_{ON}dTM$ | 0 | 1.5 | %/$^{o}$C |
| $dR_{ON}dVM$ | 0 | 0.15 | %/mV |
| $dR_{ON}dTL$ | 0 | 1.5 | %/$^{o}$C |
| $dR_{ON}dVL$ | 0 | TBD | %/mV |
| $dR_{ON}dTH$ | 0 | 1.5 | %/$^{o}$C |
| $dR_{ON}dVH$ | 0 | TBD | %/mV |

These parameters may not be subject to production test. They are verified by design and characterization.

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## 9.8 On-Die Termination (ODT) Levels and I-V Characteristics

### 9.8.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS/DQS# and TDQS/TDQS# (x8 devices only) pins.

A functional representation of the on-die termination is shown in Figure 91. The individual pull-up and pull-down resistors ($RTT_{Pu}$ and $RTT_{Pd}$) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|} \text{ under the condition that } RTT_{Pd} \text{ is turned off} \quad (3)$$

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|} \text{ under the condition that } RTT_{Pu} \text{ is turned off} \quad (4)$$

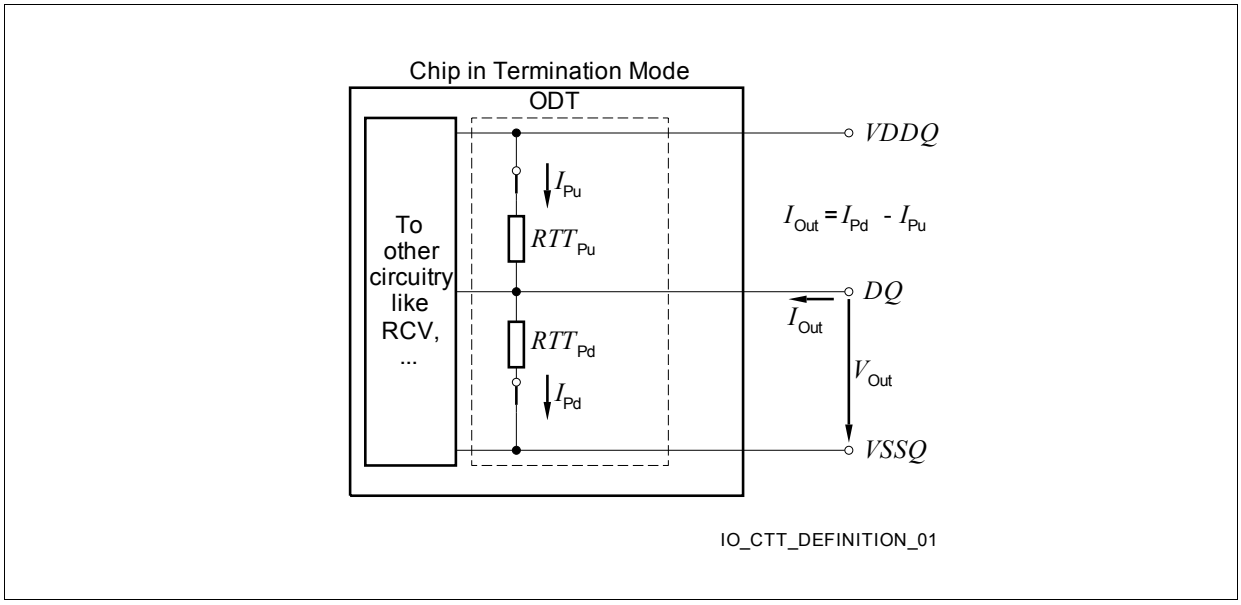



**Figure 91 — On-Die Termination: Definition of Voltages and Currents**

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**9 AC and DC Output Measurement Levels (Cont'd)**
**9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)**

### 9.8.2 ODT DC Electrical Characteristics

Table 42 provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60Pd120}$, $RTT_{60Pu120}$, $RTT_{120Pd240}$, $RTT_{120Pu240}$, $RTT_{40Pd80}$, $RTT_{40Pu80}$, $RTT_{30Pd60}$, $RTT_{30Pu60}$ , $RTT_{20Pd40}$, $RTT_{20Pu40}$ are not specification requirements, but can be used as design guide lines:

**Table 42 — ODT DC Electrical Characteristics, assuming $R_{ZQ}$ = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration**

| MR1 A9, A6, A2 | *RTT* | Resistor | $V_{Out}$ | min | nom | max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| 0, 1, 0 | 120 Ω | $RTT_{120Pd240}$ | $V_{OLdc}$ 0.2 × $V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | | 0.5 × $V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ 0.8 × $V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | $RTT_{120Pu240}$ | $V_{OLdc}$ 0.2 × $V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | | 0.5 × $V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ 0.8 × $V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}$ | 1, 2, 3, 4, |
| | | $RTT_{120}$ | $V_{IL(ac)}$ to $V_{IH(ac)}$ | 0.9 | 1.00 | 1.6 | $R_{ZQ}$/2 | 1, 2, 5, |
| 0, 0, 1 | 60 Ω | $RTT_{60Pd120}$ | $V_{OLdc}$ 0.2 × $V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | | 0.5 × $V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ 0.8 × $V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | $RTT_{60Pu120}$ | $V_{OLdc}$ 0.2 × $V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | | 0.5 × $V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ 0.8 × $V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}$/2 | 1, 2, 3, 4, |
| | | $RTT_{60}$ | $V_{IL(ac)}$ to $V_{IH(ac)}$ | 0.9 | 1.00 | 1.6 | $R_{ZQ}$/4 | 1, 2, 5, |

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**9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)**
**9.8.2 ODT DC Electrical Characteristics (Cont'd)**

**Table 42 — ODT DC Electrical Characteristics, assuming $R_{ZQ}$ = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration**

| MR1 A9, A6, A2 | *RTT* | Resistor | $V_{Out}$ | min | nom | max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| 0, 1, 1 | 40 Ω | $RTT_{40Pd80}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | $RTT_{40Pu80}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/3$ | 1, 2, 3, 4, |
| | | $RTT_{40}$ | $V_{IL(ac)}$ to $V_{IH(ac)}$ | 0.9 | 1.00 | 1.6 | $R_{ZQ}/6$ | 1, 2, 5, |
| 1, 0, 1 | 30 Ω | $RTT_{30Pd60}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | $RTT_{30Pu60}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/4$ | 1, 2, 3, 4, |
| | | $RTT_{30}$ | $V_{IL(ac)}$ to $V_{IH(ac)}$ | 0.9 | 1.00 | 1.6 | $R_{ZQ}/8$ | 1, 2, 5, |
| 1, 0, 0 | 20 Ω | $RTT_{20Pd40}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | $RTT_{20Pu40}$ | $V_{OLdc}$ $0.2 \times V_{DDQ}$ | 0.9 | 1.00 | 1.4 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | | $0.5 \times V_{DDQ}$ | 0.9 | 1.00 | 1.1 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | | $V_{OHdc}$ $0.8 \times V_{DDQ}$ | 0.6 | 1.00 | 1.1 | $R_{ZQ}/6$ | 1, 2, 3, 4, |
| | | $RTT_{20}$ | $V_{IL(ac)}$ to $V_{IH(ac)}$ | 0.9 | 1.00 | 1.6 | $R_{ZQ}/12$ | 1, 2, 5, |
| Deviation of $V_M$ w.r.t. $V_{DDQ}/2$, D$V_M$ | | | | -5 | | +5 | % | 1, 2, 5, 6, |

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.

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**9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)**
**9.8.2 ODT DC Electrical Characteristics (Cont'd)**

4. Not a specification requirement, but a design guide line.
5. Measurement definition for *RTT*:
   Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

6. Measurement definition for $V_M$ and D$V_M$:
   Measure voltage ($V_M$) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1\right) \times 100$$

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**9 AC and DC Output Measurement Levels (Cont'd)**
**9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)**

### 9.8.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 43 and Table 44.

DT = T - T(@calibration); DV= VDDQ - VDDQ(@calibration); VDD = VDDQ

**Table 43 — ODT Sensitivity Definition**

| | min | max | unit |
|---|---|---|---|
| RTT | 0.9 - $dR_{TT}dT^*\|\Delta T\|$ - $dR_{TT}dV^*\|\Delta V\|$ | 1.6 + $dR_{TT}dT^*\|\Delta T\|$ + $dR_{TT}dV^*\|\Delta V\|$ | RZQ/2,4,6,8,12 |

**Table 44 — ODT Voltage and Temperature Sensitivity**

| | min | max | unit |
|---|---|---|---|
| $dR_{TT}dT$ | 0 | 1.5 | %/°C |
| $dR_{TT}dV$ | 0 | 0.15 | %/mV |

These parameters may not be subject to production test. They are verified by design and characterization

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**9 AC and DC Output Measurement Levels (Cont'd)**

## 9.9 ODT Timing Definitions

### 9.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 92.

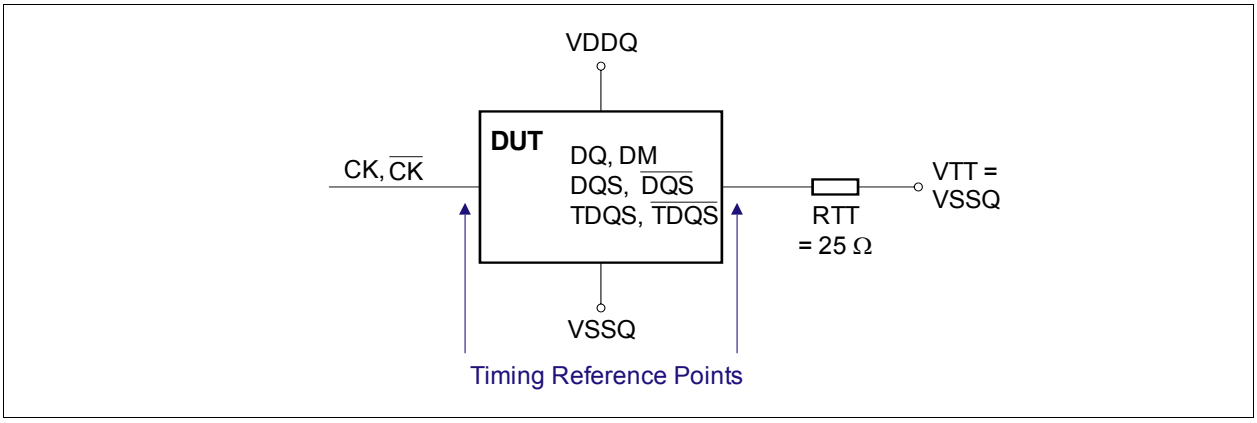



**Figure 92: ODT Timing Reference Load**

### 9.9.2 ODT Timing Definitions

Definitions for $t_{AON}$, $t_{AONPD}$, $t_{AOF}$, $t_{AOFPD}$ and $t_{ADC}$ are provided in Table 45 and subsequent figures. Measurement reference settings are provided in Table 46.

**Table 45 — ODT Timing Definitions**

| Symbol | Begin Point Definition | End Point Definition | Figure |
|---|---|---|---|
| $t_{AON}$ | Rising edge of CK - CK# defined by the end point of ODTLon | Extrapolated point at VSSQ | Figure 93 |
| $t_{AONPD}$ | Rising edge of CK - CK# with ODT being first registered high | Extrapolated point at VSSQ | Figure 94 |
| $t_{AOF}$ | Rising edge of CK - CK#defined by the end point of ODTLoff | End point: Extrapolated point at VRTT_Nom | Figure 95 |
| $t_{AOFPD}$ | Rising edge of CK - CK# with ODT being first registered low | End point: Extrapolated point at VRTT_Nom | Figure 96 |
| $t_{ADC}$ | Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8 | End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively | Figure 97 |

**Table 46 — Reference Settings for ODT Timing Measurements**

| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | $V_{SW1}$ [V] | $V_{SW2}$ [V] | Note |
|---|---|---|---|---|---|
| $t_{AON}$ | $R_{ZQ}/4$ | NA | 0.05 | 0.10 | |
| | $R_{ZQ}/12$ | NA | 0.10 | 0.20 | |
| $t_{AONPD}$ | $R_{ZQ}/4$ | NA | 0.05 | 0.10 | |
| | $R_{ZQ}/12$ | NA | 0.10 | 0.20 | |
| $t_{AOF}$ | $R_{ZQ}/4$ | NA | 0.05 | 0.10 | |
| | $R_{ZQ}/12$ | NA | 0.10 | 0.20 | |

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**9.9 ODT Timing Definitions (Cont'd)**
**9.9.2 ODT Timing Definitions (Cont'd)**

## Table 46 — Reference Settings for ODT Timing Measurements (Cont.)

| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | $V_{SW1}$ [V] | $V_{SW2}$ [V] | Note |
|---|---|---|---|---|---|
| $t_{AOFPD}$ | $R_{ZQ}/4$ | NA | 0.05 | 0.10 | |
| | $R_{ZQ}/12$ | NA | 0.10 | 0.20 | |
| $t_{ADC}$ | $R_{ZQ}/12$ | $R_{ZQ}/2$ | 0.20 | 0.30 | |

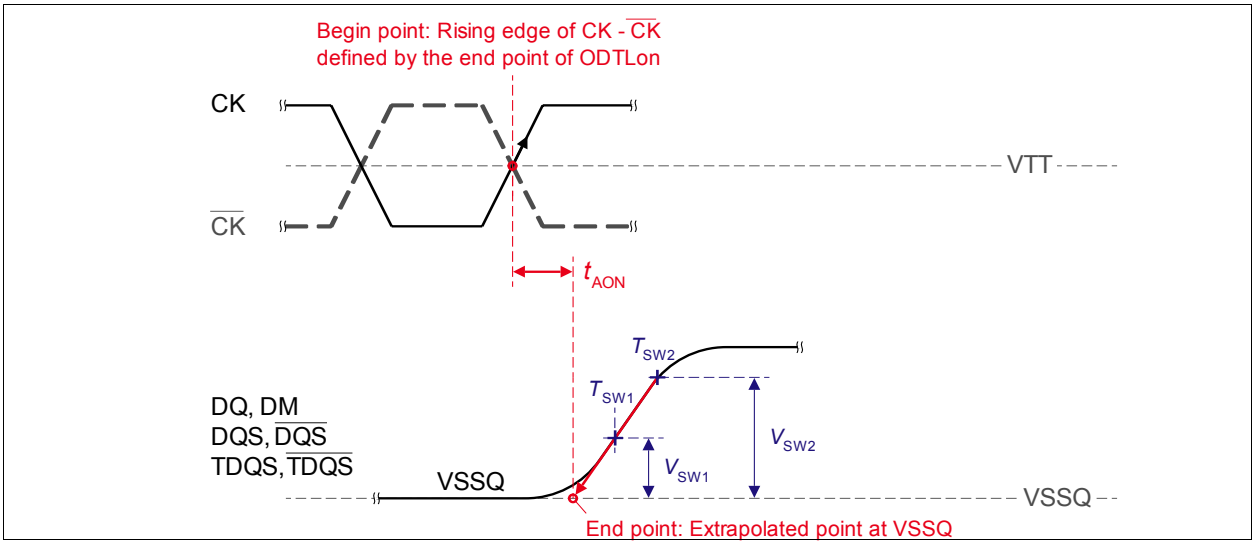



**Figure 93 — Definition of $t_{AON}$**

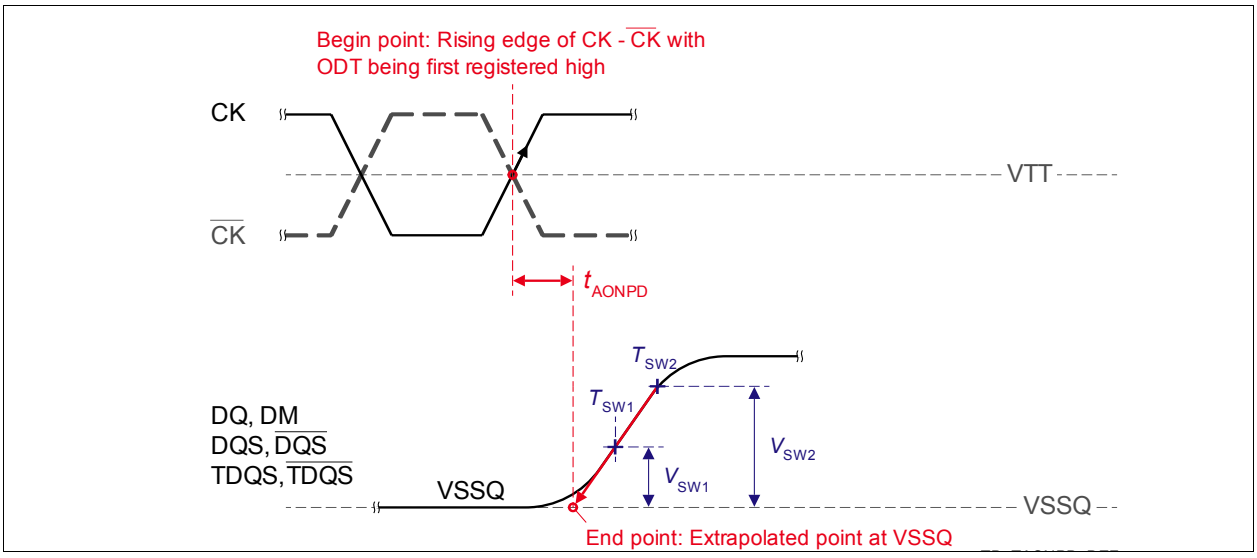



**Figure 94 — Definition of $t_{AONPD}$**

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**9.9 ODT Timing Definitions (Cont'd)**
**9.9.2 ODT Timing Definitions (Cont'd)**

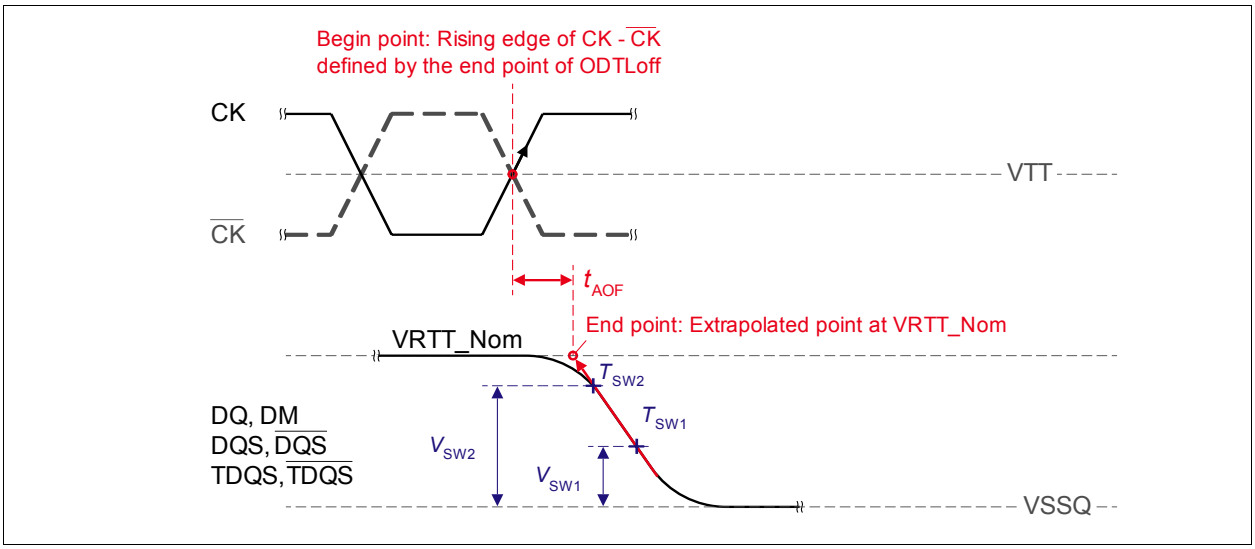



**Figure 95 — Definition of $t_{AOF}$**

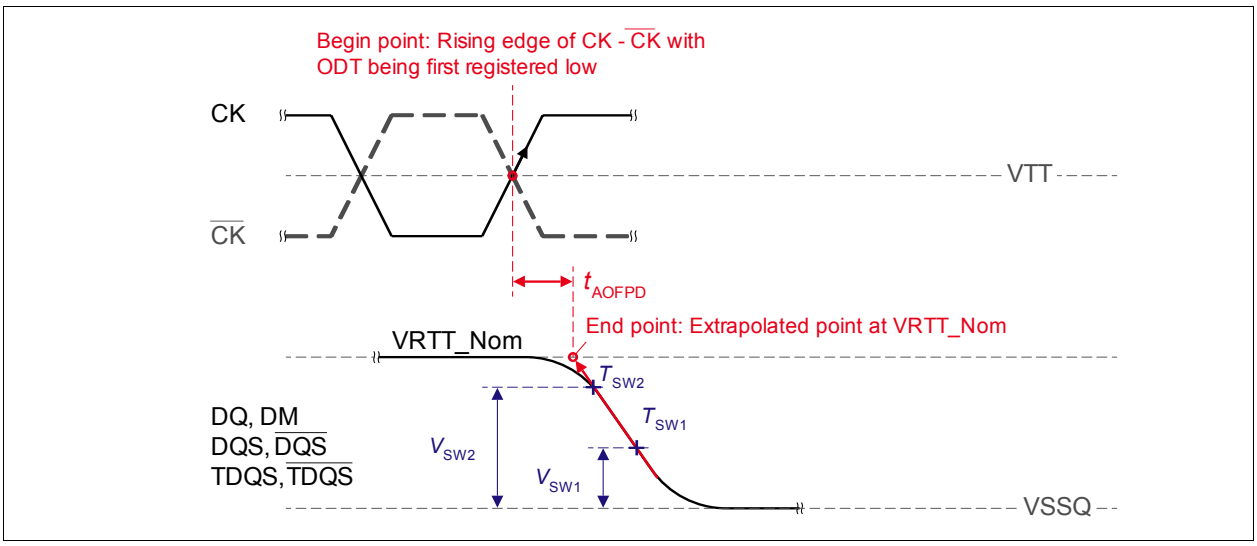



**Figure 96 — Definition of $t_{AOFPD}$**

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**9.9 ODT Timing Definitions (Cont'd)**
**9.9.2 ODT Timing Definitions (Cont'd)**

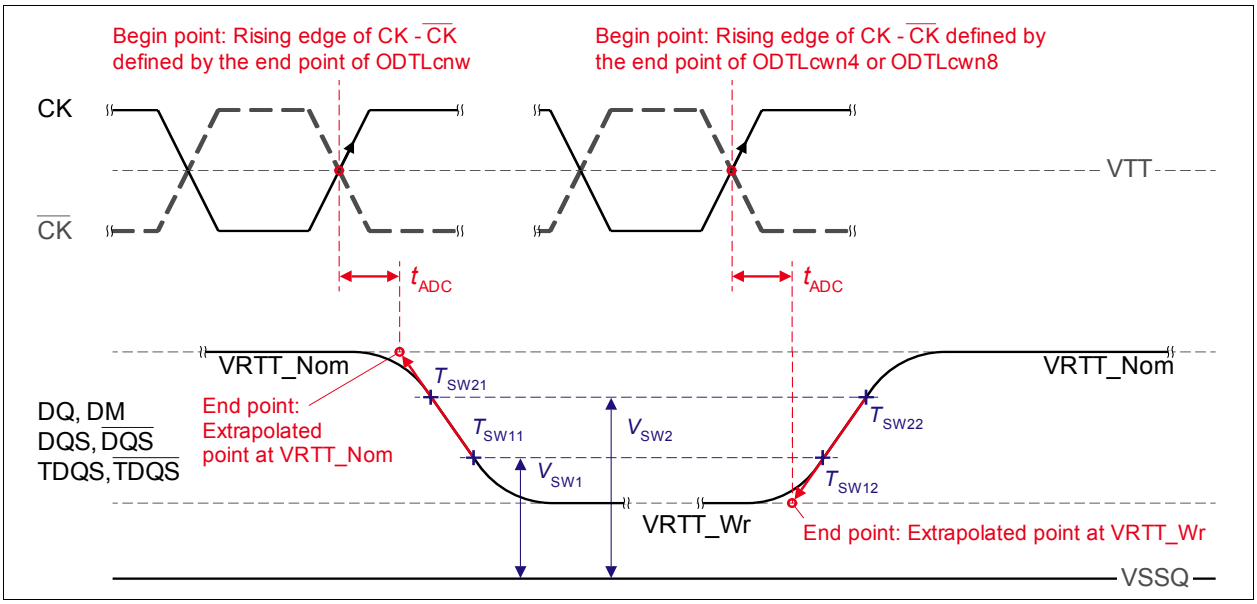



**Figure 97 — Definition of $t_{ADC}$**

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# 10 IDD Specification Parameters and Test Conditions

## 10.1 IDD Measurement Conditions

The following tables provide an overview about the IDD measurement conditions is provided as follows:

**Table 47 — Overview of Tables providing IDD Measurement Conditions and DRAM Behavior**

| Table number | Measurement Conditions |
|---|---|
| Table 51 on page 129 | IDD0 and IDD1 |
| Table 52 on page 131 | IDD2N, IDD2Q, IDD2P(0), IDD2P(1) |
| Table 53 on page 133 | IDD3N and IDD3P |
| Table 54 on page 134 | IDD4R, IDD4W, IDD7 |
| Table 55 on page 136 | IDD7 for different Speed Grades and different tRRD, tFAW conditions |
| Table 56 on page 137 | IDD5B |
| Table 57 on page 137 | IDD6, IDD6ET (optional), IDD6TC (optional) |

**Within the tables about IDD measurement conditions, the following definitions are used:**

- LOW is defined as VIN <= $V_{ILAC(max.)}$; HIGH is defined as VIN >= $V_{IHAC(min.)}$.
- STABLE is defined as inputs are stable at a HIGH or LOW level.
- FLOATING is defined as inputs are $V_{REF}$ = $V_{DDQ}$ / 2.
- SWITCHING is defined as described in Table 48 and Table 49.

**Table 48 — Definition of SWITCHING for Address and Command Input Signals**

| **SWITCHING** for **Address (row, column) and Command Signals (CS#, RAS#, CAS#, WE#)** is defined as: | |
|---|---|
| **Address (row, column)**: | If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value<br>(e.g. Ax $\overline{Ax}$ $\overline{Ax}$ Ax $\overline{Ax}$ $\overline{Ax}$ Ax $\overline{Ax}$ $\overline{Ax}$ Ax .....<br>please see each IDDx definition for details |
| **Bank address**: | If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details |
| **Command** (CS#, RAS#, CAS#, WE#): | Define D = {CS#, RAS#, CAS#, WE# } := {HIGH, LOW, LOW, LOW}<br>Define $\overline{D}$ = {CS#, RAS#, CAS#, WE# } := {HIGH, HIGH,HIGH,HIGH}<br><br>Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ...<br><br>If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective CS#, RAS#, CAS#, WE# levels of the necessary command.<br>See each IDDx definition for details and Figure 98 through Figure 100 as examples. |

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 49 — Definition of SWITCHING for Data (DQ)

| **SWITCHING** for **Data (DQ)** is defined as | |
|---|---|
| Data (DQ) | Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details.<br>See Figure 98 through Figure 100 as examples. |
| Data Masking (DM) | NO Switching; DM must be driven LOW all the time |

**Timing parameters are listed in the following table:**

## Table 50 — For IDD testing the following parameters are utilized.

| Parameter Bin | | DDR3-800 | | DDR3-1066 | | | DDR3-1333 | | | DDR3-1600 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 5-5-5 | 6-6-6 | 6-6-6 | 7-7-7 | 8-8-8 | 7-7-7 | 8-8-8 | 9-9-9 | 8-8-8 | 9-9-9 | 10-10-10 | |
| $t_{CKmin}$(IDD) | | 2.5 | | 1.875 | | | 1.5 | | | 1.25 | | | ns |
| CL(IDD) | | 5 | 6 | 6 | 7 | 8 | 7 | 8 | 9 | 8 | 9 | 10 | |
| $t_{RCDmin}$(IDD) | | 12.5 | 15 | 11.25 | 13.13 | 15 | 10.5 | 12 | 13.5 | 10 | 11.25 | 12.5 | ns |
| $t_{RCmin}$(IDD) | | 50 | 52.5 | 48.75 | 50.63 | 52.50 | 46.5 | 48 | 49.5 | 45 | 46.25 | 47.5 | ns |
| $t_{RASmin}$(IDD) | | 37.5 | 37.5 | 37.5 | 37.5 | 37.5 | 36 | 36 | 36 | 35 | 35 | 35 | ns |
| $t_{RPmin}$(IDD) | | 12.5 | 15 | 11.25 | 13.13 | 15 | 10.5 | 12 | 13.5 | 10 | 11.25 | 12.5 | ns |
| $t_{FAW}$(IDD) | x4/ x8 | 40 | 40 | 37.5 | 37.5 | 37.5 | 30 | 30 | 30 | 30 | 30 | 30 | ns |
| | x16 | 50 | 50 | 50 | 50 | 50 | 45 | 45 | 45 | 40 | 40 | 40 | ns |
| $t_{RRD}$(IDD) | x4/ x8 | 10 | 10 | 7.5 | 7.5 | 7.5 | 6.0 | 6.0 | 6.0 | 6.0 | 6.0 | 6.0 | ns |
| | x16 | 10 | 10 | 10 | 10 | 10 | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 | ns |
| $t_{RFC}$(IDD) - 512Mb | | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | ns |
| $t_{RFC}$(IDD) - 1 Gb | | 110 | 110 | 110 | 110 | 110 | 110 | 110 | 110 | 110 | 110 | 110 | ns |
| $t_{RFC}$(IDD) - 2 Gb | | 160 | 160 | 160 | 160 | 160 | 160 | 160 | 160 | 160 | 160 | 160 | ns |
| $t_{RFC}$(IDD) - 4 Gb | | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | ns |
| $t_{RFC}$(IDD) - 8 Gb | | 350 | 350 | 350 | 350 | 350 | 350 | 350 | 350 | 350 | 350 | 350 | ns |

**The following conditions apply:**

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric test conditions.
3. IDD parameters are specified with ODT and output buffer disabled (MR1 bit A12).

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 51 — IDD Measurement Conditions for IDD0 and IDD1

| **Current** | $I_{DD0}$ | $I_{DD1}$ |
|---|---|---|
| **Name** | **Operating Current 0<br>-> One Bank Activate<br>-> Precharge** | **Operating Current 1<br>-> One Bank Activate<br>-> Read<br>-> Precharge** |
| **Measurement Condition** | | |
| Timing Diagram Example | | Figure 98 |
| CKE | HIGH | HIGH |
| External Clock | on | on |
| $t_{CK}$ | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) |
| $t_{RC}$ | $t_{RCmin}$(IDD) | $t_{RCmin}$(IDD) |
| $t_{RAS}$ | $t_{RASmin}$(IDD) | $t_{RASmin}$(IDD) |
| $t_{RCD}$ | n.a. | $t_{RCDmin}$(IDD) |
| $t_{RRD}$ | n.a. | n.a. |
| CL | n.a. | CL(IDD) |
| AL | n.a. | 0 |
| CS# | HIGH between. Activate and Precharge Commands | HIGH between Activate, Read and Precharge |
| Command Inputs<br>(CS#, RAS#, CAS#, WE#) | SWITCHING as described in Table 48; only exceptions are Activate and Precharge commands; example of IDD0 pattern:<br><br>**A0**D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}$ **P0**<br>(DDR3-800: $t_{RAS}$ = 37.5ns between (A)ctivate and (P)recharge to bank 0;<br><br>Definition of D and $\overline{\text{D}}$: see Table 48) | SWITCHING as described in Table 48; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern:<br><br>**A0**D$\overline{\text{D}}\overline{\text{D}}$D**R0**D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}\overline{\text{D}}$D$\overline{\text{D}}$ **P0**<br>(DDR3-800 -555: $t_{RCD}$ = 12.5ns between (A)ctivate and (R)ead to bank **0**;<br><br>Definition of D and $\overline{\text{D}}$: see Table 48) |
| Row, Column Addresses | Row addresses SWITCHING as described in Table 48;<br><br>Address Input A10 must be LOW all the time! | Row addresses SWITCHING as described in Table 48;<br><br>Address Input A10 must be LOW all the time! |
| Bank Addresses | bank address is fixed (bank 0) | bank address is fixed (bank 0) |
| Data I/O | SWITCHING as described in Table 49 | Read Data: output data switches every clock, which means that Read data is stable during one clock cycle.<br>To achieve Iout = 0mA, the output buffer should be switched off by MR1 bit A12 set to "1".<br>When there is no read data burst from DRAM, the DQ I/O should be FLOATING. |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled | disabled |
| Burst length | n.a. | 8 fixed / MR0 bits [A1, A0] = {0,0} |

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 51 — IDD Measurement Conditions for IDD0 and IDD1

| Current | $I_{DD0}$ | $I_{DD1}$ |
|---|---|---|
| **Name** | **Operating Current 0<br>-> One Bank Activate<br>-> Precharge** | **Operating Current 1<br>-> One Bank Activate<br>-> Read<br>-> Precharge** |
| Active banks | one<br>ACT-PRE loop | one<br>ACT-RD-PRE loop |
| Idle banks | all other | all other |
| Precharge Power Down Mode<br>/<br>MR0 bit A12 | n.a. | n.a. |

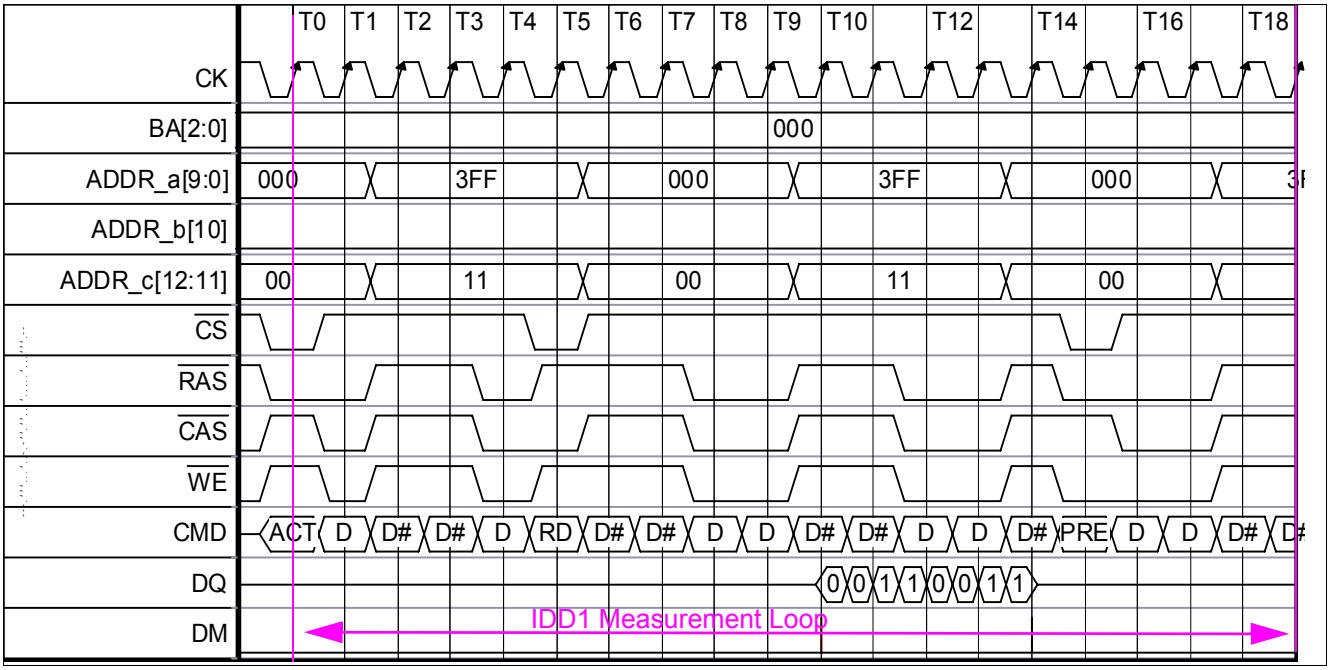



**Figure 98 — IDD1 Example (DDR3-800-555, 512Mb x8): Data DQ is shown but the output buffer should be switched off (per MR1 bit A12 ="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.**

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 52 — IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

| **Current** | $I_{DD2N}$ | $I_{DD2P}(1)$ [1] | $I_{DD2P}(0)$ | $I_{DD2Q}$ |
|---|---|---|---|---|
| **Name** | **Precharge Standby Current** | **Precharge Power Down Current Fast Exit - MR0 bit A12 = 1** | **Precharge Power Down Current Slow Exit - MR0 bit A12 = 0** | **Precharge Quiet Standby Current** |
| **Measurement Condition** | | | | |
| Timing Diagram Example | Figure 99 | | | |
| CKE | HIGH | LOW | LOW | HIGH |
| External Clock | on | on | on | on |
| $t_{CK}$ | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) |
| $t_{RC}$ | n.a. | n.a. | n.a. | n.a. |
| $t_{RAS}$ | n.a. | n.a. | n.a. | n.a. |
| $t_{RCD}$ | n.a. | n.a. | n.a. | n.a. |
| $t_{RRD}$ | n.a. | n.a. | n.a. | n.a. |
| CL | n.a. | n.a. | n.a. | n.a. |
| AL | n.a. | n.a. | n.a. | n.a. |
| CS# | HIGH | STABLE | STABLE | HIGH |
| Bank Address, Row Addr. and Command Inputs | SWITCHING as described in Table 48 | STABLE | STABLE | STABLE |
| Data inputs | SWITCHING | FLOATING | FLOATING | FLOATING |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 | off / 1 | off / 1 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled | disabled | disabled | disabled |
| Burst length | n.a. | n.a. | n.a. | n.a. |
| Active banks | none | none | none | none |
| Idle banks | all | all | all | all |
| Precharge Power Down Mode / MR0 bit A12[a] | n.a. | Fast Exit / 1 (any valid command after tXP[2]) | Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL) | n.a. |

NOTE:

1. In DDR3, the MR0 bit A12 defines DLL on/off behaviour ONLY for precharge power down. There are 2 different Precharge Power Down states possible: one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).
2. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

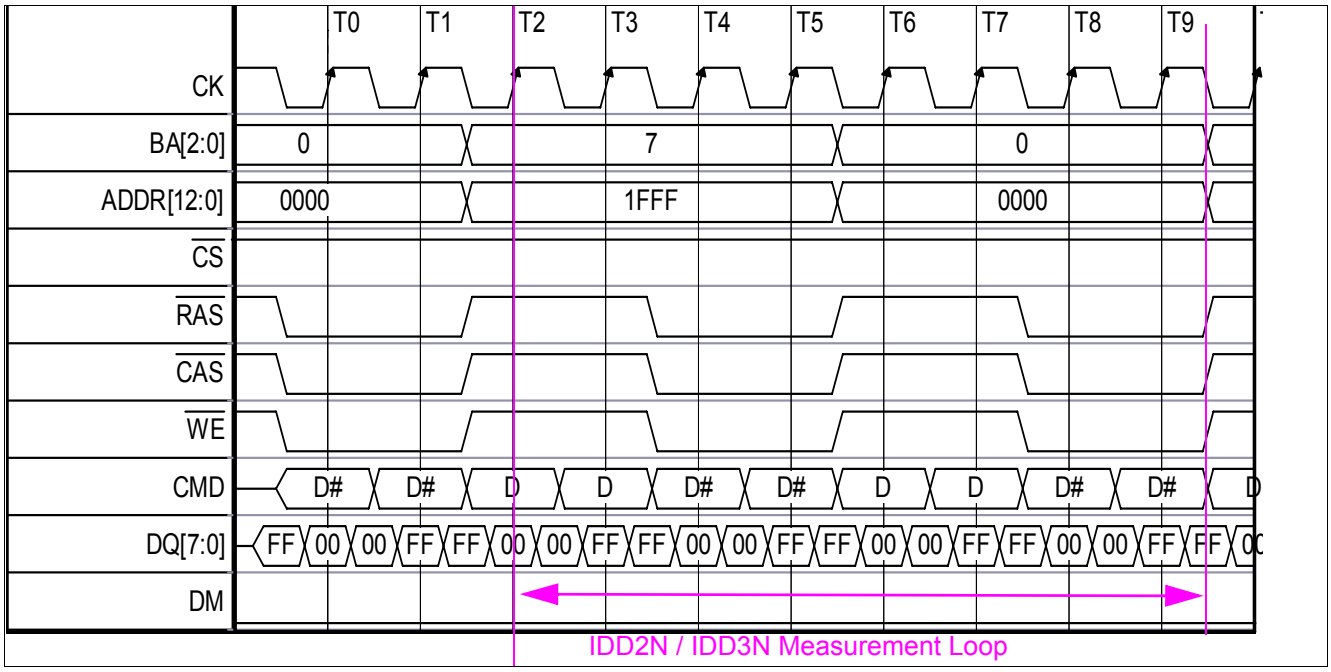



**Figure 99 — IDD2N / IDD3N Example (DDR3-800-555, 512Mb x8)**

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 53 — IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

| **Current** | **$I_{DD3N}$** | **$I_{DD3P}$** |
|---|---|---|
| **Name** | **Active Standby Current** | **Active Power-Down Current[1] Always Fast Exit** |
| **Measurement Condition** | | |
| Timing Diagram Example | Figure 99 | |
| CKE | HIGH | LOW |
| External Clock | on | on |
| $t_{CK}$ | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) |
| $t_{RC}$ | n.a. | n.a. |
| $t_{RAS}$ | n.a. | n.a. |
| $t_{RCD}$ | n.a. | n.a. |
| $t_{RRD}$ | n.a. | n.a. |
| CL | n.a. | n.a. |
| AL | n.a. | n.a. |
| CS# | HIGH | STABLE |
| Addr. and cmd Inputs | SWITCHING as described in Table 48 | STABLE |
| Data inputs | SWITCHING as described in Table 49 | FLOATING |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled | disabled |
| Burst length | n.a. | n.a. |
| Active banks | all | all |
| Idle banks | none | none |
| Precharge Power Down Mode / MR0 bit A12 [a] | n.a. | n.a. (Active Power Down Mode is always "Fast Exit" with DLL on |

NOTE:

1. DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MR0 bit A12 will not be used for active power down. Instead bit A12 will be used to switch between two different precharge power down modes.

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 54 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

| **Current** | $I_{DD4R}$ | $I_{DD4W}$ | $I_{DD7}$ |
|---|---|---|---|
| **Name** | **Operating Current Burst Read** | **Operating Current Burst Write** | **All Bank Interleave Read Current** |
| **Measurement Condition** | | | |
| Timing Diagram Example | Figure 100 | | |
| CKE | HIGH | HIGH | HIGH |
| External Clock | on | on | on |
| $t_{CK}$ | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) | $t_{CKmin}$(IDD) |
| $t_{RC}$ | n.a. | n.a. | $t_{RCmin}$(IDD) |
| $t_{RAS}$ | n.a. | n.a. | $t_{RASmin}$(IDD) |
| $t_{RCD}$ | n.a. | n.a. | $t_{RCDmin}$(IDD) |
| $t_{RRD}$ | n.a. | n.a. | $t_{RRDmin}$(IDD) |
| CL | CL(IDD) | CL(IDD) | CL(IDD) |
| AL | 0 | 0 | $t_{RCDmin}$ - 1 $t_{CK}$ |
| CS# | HIGH btw. valid cmds | HIGH btw. valid cmds | HIGH btw. valid cmds |
| Command Inputs CS#, RAS#, CAS#, WE# | SWITCHING as described in Table 48; exceptions are Read commands => IDD4R Pattern:<br><br>**R0**D$\overline{D}\overline{D}$**R1**D$\overline{D}\overline{D}$**R2**D$\overline{D}\overline{D}$**R3** .D$\overline{D}\overline{D}$ **R4** .....<br>Rx = Read from bank x; Definition of D and $\overline{D}$: see Table 48 | SWITCHING as described in Table 48; exceptions are Write commands => IDD4W Pattern:<br><br>**W0**D$\overline{D}\overline{D}$**W1**D$\overline{D}\overline{D}$**W2**D$\overline{D}\overline{D}$**W3** D$\overline{D}\overline{D}$ **W4** ...<br>Wx = Write to bank x; Definition of D and $\overline{D}$: see Table 48 | For patterns see Table 55 |
| Row, Colum Addresses | column addresses SWITCHING as described in Table 48;<br>Address Input A10 must be LOW all the time! | column addresses SWITCHING as described in Table 48;<br>Address Input A10 must be LOW all the time! | STABLE during DESELECTs |
| Bank Addresses | bank address cycling (0 -> 1 -> 2 -> 3 ...) | bank address cycling (0 -> 1 -> 2 -> 3 ...) | bank address cycling (0 -> 1 -> 2 -> 3 ...), see pattern in Table 55 |
| DQ I/O | Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle.<br><br>To achieve Iout = 0mA the output buffer should be switched off by MR1 bit A12 set to "1". | Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle.<br><br>DM is low all the time. | Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle.<br><br>To achieve Iout = 0mA the output buffer should be switched off by MR1 bit A12 set to "1". |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 | off / 1 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled | disabled | disabled |

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 54 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

| Current | $I_{DD4R}$ | $I_{DD4W}$ | $I_{DD7}$ |
|---|---|---|---|
| **Name** | **Operating Current Burst Read** | **Operating Current Burst Write** | **All Bank Interleave Read Current** |
| Burst length | 8 fixed / MR0 bits [A1, A0] = {0,0} | 8 fixed / MR0 bits [A1, A0] = {0,0} | 8 fixed / MR0 bits [A1, A0] = {0,0} |
| Active banks | all | all | all, rotational |
| Idle banks | none | none | none |
| Precharge Power Down Mode / MR0 bit A12 | n.a. | n.a. | n.a. |

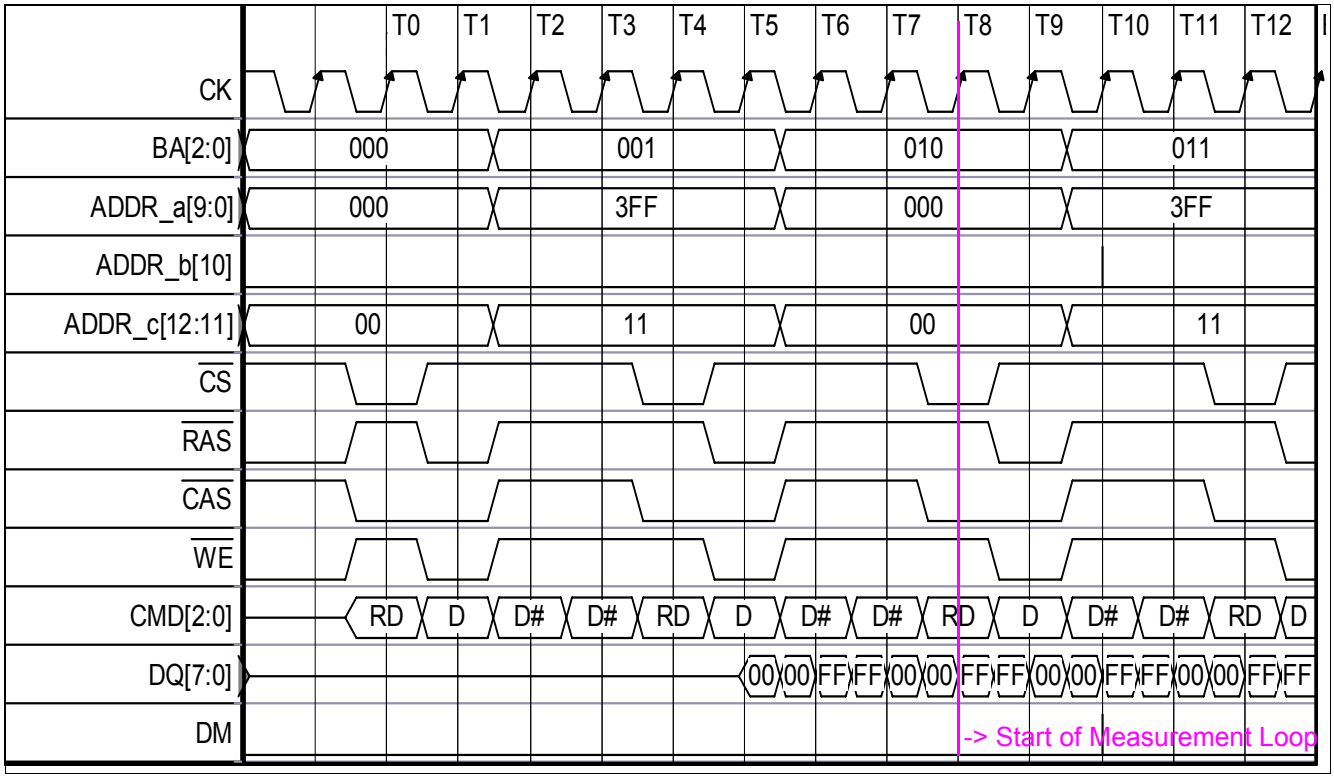



**Figure 100 — IDD4R Example (DDR3-800-555, 512Mb x8): data DQ is shown but the output buffer should be switched off (per MR1 bit A12="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.**

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 55 — IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

| Speed | Bin | Org. | tFAW | tFAW | tRRD | tRRD | IDD7 Pattern[1] |
|---|---|---|---|---|---|---|---|
| Mb/s | | | [ns] | [CLK] | [ns] | [CLK] | (Note this entire sequence is repeated.) |
| 800 | all | x4/x8 | 40 | 16 | 10 | 4 | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D |
| | all | x16 | 50 | 20 | 10 | 4 | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D |
| 1066 | all | x4/x8 | 37.5 | 20 | 7.5 | 4 | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D |
| | all | x16 | 50 | 27 | 10 | 6 | A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D |
| 1333 | all | x4/x8 | 30 | 20 | 6 | 4 | A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D |
| | all | x16 | 45 | 30 | 7.5 | 5 | A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D |
| 1600 | all | x4/x8 | 30 | 24 | 6 | 5 | A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D |
| | all | x16 | 40 | 32 | 7.5 | 6 | A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D D D D D D |

NOTE:

1. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 56 — IDD Measurement Conditions for IDD5B

| **Current** | $I_{DD5B}$ |
|---|---|
| **Name** | **Burst Refresh Current** |
| **Measurement Condition** | |
| CKE | HIGH |
| External Clock | on |
| $t_{CK}$ | $t_{CKmin}$(IDD) |
| $t_{RC}$ | n.a. |
| $t_{RAS}$ | n.a. |
| $t_{RCD}$ | n.a. |
| $t_{RRD}$ | n.a. |
| $t_{RFC}$ | $t_{RFCmin}$(IDD) |
| CL | n.a. |
| AL | n.a. |
| CS# | HIGH btw. valid cmds |
| Addr. and cmd Inputs | SWITCHING |
| Data inputs | SWITCHING |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled |
| Burst length | n.a. |
| Active banks | Refresh command every tRFC=tRFCmin |
| Idle banks | none |
| Precharge Power Down Mode / MR0 bit A12 | n.a. |

## Table 57 — IDD Measurement Conditions for IDD6, IDD6ET, and IDD6TC

| **Current** | $I_{DD6}$ | $I_{DD6ET\ (optional)}$ | $I_{DD6TC\ (optional)}$ |
|---|---|---|---|
| **Name** | **Self-Refresh Current Normal Temperature Range** $T_{CASE}$ = 0 .. 85 °C | **Self-Refresh Current Extended Temperature Range** [1] $T_{CASE}$ = 0 .. 95 °C | **Auto Self-Refresh Current**[1,2] $T_{CASE}$ - See Table |
| **Measurement Condition** | | | |
| Temperature | $T_{CASE}$ = 85 °C | $T_{CASE}$ = 95 °C | $T_{CASE}$ - See Table |
| Auto Self Refresh (ASR) / MR2 bit A6 | Disabled / "0" | Disabled / "0" | Enabled / "1" |
| Self Refresh Temperature Range (SRT) / MR2 bit A7 | Normal / "0" | Extended / "1" | Disabled / "0" |
| CKE | LOW | LOW | LOW |

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.1 IDD Measurement Conditions (Cont'd)**

## Table 57 — IDD Measurement Conditions for IDD6, IDD6ET, and IDD6TC

| **Current** | $I_{DD6}$ | $I_{DD6ET}$ **(optional)** | $I_{DD6TC}$ **(optional)** |
|---|---|---|---|
| **Name** | **Self-Refresh Current Normal Temperature Range** $T_{CASE}$ = 0 .. 85 °C | **Self-Refresh Current Extended Temperature Range** [1] $T_{CASE}$ = 0 .. 95 °C | **Auto Self-Refresh Current**[1,2] $T_{CASE}$ - See Table |
| External Clock | OFF; CK and $\overline{CK}$ at LOW | OFF; CK and $\overline{CK}$ at LOW | OFF; CK and $\overline{CK}$ at LOW |
| $t_{CK}$ | n.a. | n.a. | n.a. |
| $t_{RC}$ | n.a. | n.a. | n.a. |
| $t_{RAS}$ | n.a. | n.a. | n.a. |
| $t_{RCD}$ | n.a. | n.a. | n.a. |
| $t_{RRD}$ | n.a. | n.a. | n.a. |
| CL | n.a. | n.a. | n.a. |
| AL | n.a. | n.a. | n.a. |
| CS# | FLOATING | FLOATING | FLOATING |
| Command Inputs (CS#, RAS#, CAS#, WE#) | FLOATING | FLOATING | FLOATING |
| Row, Colum Addresses | FLOATING | FLOATING | FLOATING |
| Bank Addresses | FLOATING | FLOATING | FLOATING |
| Data I/O | FLOATING | FLOATING | FLOATING |
| Output Buffer DQ,DQS / MR1 bit A12 | off / 1 | off / 1 | off / 1 |
| Rtt_Nom, Rtt_WR | disabled | disabled | disabled |
| Burst length | n.a. | n.a. | n.a. |
| Active banks | all during self-refresh actions | all during self-refresh actions | all during self-refresh actions |
| Idle banks | all btw. Self-Refresh actions | all btw. Self-Refresh actions | all btw. Self-Refresh actions |
| Precharge Power Down Mode / MR0 bit A12 | n.a. | n.a. | n.a. |

NOTE:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.
2. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices supporting ASR support the Normal or Extended Temperature Range.

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**

## 10.2 IDD Specifications

**IDD values are for full operating range of voltage and temperature unless otherwise noted.**

**Table 58 — $I_{DD}$ Specification Example 512M DDR3**

| Speed Grade Bin | DDR3 - 800 5-5-5 | DDR3 - 1066 7-7-7 | DDR3 - 1333 8-8-8 | DDR3 - 1600 9-9-9 | Unit | Notes |
|---|---|---|---|---|---|---|
| **Symbol** | **Max.** | **Max.** | **Max.** | **Max.** | | |
| $I_{DD0}$ | | | | | mA | x4/x8 |
| | | | | | mA | x16 |
| $I_{DD1}$ | | | | | mA | x4/x8 |
| | | | | | mA | x16 |
| $I_{DD2P}$ (0) slow exit | | | | | mA | x4/x8/x16 |
| $I_{DD2P}$ (1) fast exit | | | | | mA | x4/x8/x16 |
| $I_{DD2N}$ | | | | | mA | x4/x8/x16 |
| $I_{DD2Q}$ | | | | | mA | x4/x8/x16 |
| $I_{DD3P}$ (fast exit) | | | | | mA | x4/x8/x16 |
| $I_{DD3N}$ | | | | | mA | x4/x8/x16 |
| $I_{DD4R}$ | | | | | mA | x4 |
| | | | | | mA | x8 |
| | | | | | mA | x16 |
| $I_{DD4W}$ | | | | | mA | x4 |
| | | | | | mA | x8 |
| | | | | | mA | x16 |
| $I_{DD5B}$ | | | | | mA | x4/x8/x16 |
| $I_{DD6}$ | | | | | mA | |
| $I_{DD6ET}$[1] | | | | | mA | |
| $I_{DD6TC}$[1] | | | | | mA | Refer to Table |
| $I_{DD7}$ | | | | | mA | x4/x8 |
| | | | | | mA | x16 |

NOTE:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

**Table 59 — $I_{DD6}$ Current Definition**

| Symbol | Parameter/Condition |
|---|---|
| $I_{DD6}$ | Normal Temperature Range Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 0. |
| $I_{DD6ET}$ | Extended Temperature Range Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6 = 0 and A7 = 1. |

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**10 IDD Specification Parameters and Test Conditions (Cont'd)**
**10.2 IDD Specifications (Cont'd)**

## Table 59 — $I_{DD6}$ Current Definition

| Symbol | Parameter/Condition |
|---|---|
| $I_{DD6TC}$ | Auto Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and CK# at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable when ASR is enabled by MR2 settings A6 = 1 and A7 = 0. |

## Table 60 — $I_{DD6}$ Specification

| Symbol | Temperature Range | Value | Unit | Notes |
|---|---|---|---|---|
| $I_{DD6}$ | 0 - 85 °C | | mA | 3,4 |
| $I_{DD6ET}$ | 0 - 95 °C | | mA | 5,6 |
| $I_{DD6TC}$ | 0 °C ~ $T_a$ | | mA | 6,7,8 |
| | $T_b$ ~ $T_y$ | | mA | 6,7,8 |
| | $T_z$ ~ $T_{OPERmax}$ | | mA | 6,7,8 |

1. *Some $I_{DD}$ currents are higher for x16 organization due to larger page-size architecture.*
2. *Max. values for $I_{DD}$ currents considering worst case conditions of process, temperature and voltage.*
3. *Applicable for MR2 settings A6=0 and A7=0.*
4. *Supplier data sheets include a max value for $I_{DD6}$.*
5. *Applicable for MR2 settings A6=0 and A7=1. $I_{DD6ET}$ is only specified for devices which support the Extended Temperature Range feature.*
6. *Refer to the supplier data sheet for the value specification method (e.g. max, typical) for $I_{DD6ET}$ and $I_{DD6TC}$*
7. *Applicable for MR2 settings A6=1 and A7=0. $I_{DD6TC}$ is only specified for devices which support the Auto Self Refresh feature.*
8. *The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of $T_{OPER}$. Refer to supplier data sheet for more information.*

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# 11 Input/Output Capacitance

## 11.1 Input/Output Capacitance

**Table 61 — Input / Output Capacitance**

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| Input/output capacitance (DQ,DM,DQS,DQS#, TDQS,TDQS#) | $C_{IO}$ | 1.5 | 3.0 | 1.5 | 3.0 | 1.5 | 2.5 | TBD | TBD | pF | 1,2,3 |
| Input capacitance, CK and CK# | $C_{CK}$ | 0.8 | 1.6 | 0.8 | 1.6 | 0.8 | 1.4 | 0.8 | 1.4 | pF | 2,3 |
| Input capacitance delta, CK and CK# | $C_{DCK}$ | 0 | 0.15 | 0 | 0.15 | 0 | 0.15 | 0 | 0.15 | pF | 2,3,4 |
| Input/output capacitance delta DQS and DQS# | $C_{DDQS}$ | 0 | 0.2 | 0 | 0.2 | 0 | 0.15 | 0 | 0.15 | pF | 2,3,5 |
| Input capacitance, (CTRL, ADD, CMD input-only pins) | $C_I$ | 0.75 | 1.5 | 0.75 | 1.5 | 0.75 | 1.3 | 0.75 | 1.3 | pF | 2,3,6 |
| Input capacitance delta, (All CTRL input-only pins | $C_{DI\_CTRL}$ | -0.5 | 0.3 | -0.5 | 0.3 | -0.4 | 0.2 | -0.4 | 0.2 | pF | 2,3,7, 8 |
| Input capacitance delta, (All ADD/ CMD input-only pins) | $C_{DI\_ADD\_CMD}$ | -0.5 | 0.5 | -0.5 | 0.5 | -0.4 | 0.4 | -0.4 | 0.4 | pF | 2,3,9, 10 |
| Input/output capacitance delta, DQ, DM, DQS, DQS#, TDQS, TDQS# | $C_{DIO}$ | -0.5 | 0.3 | -0.5 | 0.3 | -0.5 | 0.3 | -0.5 | 0.3 | pF | 2,3,11 |
| Input/output capacitance of ZQ pin | $C_{ZQ}$ | - | 3 | - | 3 | - | 3 | - | 3 | pF | 2,3,12 |

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of $C_{CK}$-$C_{CK}$#
5. Absolute value of $C_{IO}$(DQS)-$C_{IO}$(DQS#)
6. $C_I$ applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. $C_{DI\_CTRL}$ applies to ODT, CS# and CKE
8. $C_{DI\_CTRL}$=$C_I$(CTRL)-0.5*($C_I$(CLK)+$C_I$(CLK#))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#
10. $C_{DI\_ADD\_CMD}$=$C_I$(ADD_CMD) - 0.5*($C_I$(CLK)+$C_I$(CLK#))
11. $C_{DIO}$=$C_{IO}$(DQ,DM) - 0.5*($C_{IO}$(DQS)+$C_{IO}$(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

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# 12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600

## 12.1 Clock Specification

The jitter specified is a randon jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

### 12.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left( \sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

### 12.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

### 12.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left( \sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left( \sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

### 12.1.4 Definition for tJIT(per) and tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {$tCK_i$ - tCK(avg) where i = 1 to 200}.

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not subject to production test.

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**12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)**
**12.1 Clock Specification (Cont'd)**

### 12.1.5 Definition for tJIT(cc) and tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of $|\{tCK_{i+1} - tCK_i\}|$.

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not subject to production test.

### 12.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

## 12.2 Refresh parameters by device density

**Table 62 — Refresh parameters by device density**

| Parameter | Symbol | | 512Mb | 1Gb | 2Gb | 4Gb | 8Gb | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| REF command to ACT or REF command time | tRFC | | 90 | 110 | 160 | 300 | 350 | ns | |
| Average periodic refresh interval | tREFI | 0 °C ≤ $T_{CASE}$ ≤ 85 °C | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | µs | |
| | | 85 °C < $T_{CASE}$ ≤ 95 °C | 3.9 | 3.9 | 3.9 | 3.9 | 3.9 | µs | 1 |

Notes: 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

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## 12.3 Standard Speed Bins

**DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.**

### Table 63 — DDR3-800 Speed Bins

| For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 148. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Speed Bin** | | | **DDR3-800D** | | **DDR3-800E** | | **Unit** | **Notes** |
| **CL - nRCD - nRP** | | | **5-5-5** | | **6-6-6** | | | |
| **Parameter** | | **Symbol** | **min** | **max** | **min** | **max** | | |
| Internal read command to first data | | $t_{AA}$ | 12.5 | 20 | 15 | 20 | ns | |
| ACT to internal read or write delay time | | $t_{RCD}$ | 12.5 | — | 15 | — | ns | |
| PRE command period | | $t_{RP}$ | 12.5 | — | 15 | — | ns | |
| ACT to ACT or REF command period | | $t_{RC}$ | 50 | — | 52.5 | — | ns | |
| ACT to PRE command period | | $t_{RAS}$ | 37.5 | 9 * tREFI | 37.5 | 9 * tREFI | ns | |
| CL = 5 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | Reserved | | ns | 1,2,3,4, |
| CL = 6 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | ns | 1,2,3, |
| Supported CL Settings | | | 5, 6 | | 6 | | $n_{CK}$ | |
| Supported CWL Settings | | | 5 | | 5 | | $n_{CK}$ | |

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**12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)**
**12.3 Standard Speed Bins (Cont'd)**

## Table 64 — DDR3-1066 Speed Bins

| For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 148. | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Speed Bin** | | | **DDR3-1066E** | | **DDR3-1066F** | | **DDR3-1066G** | | **Unit** | **Note** |
| **CL - nRCD - nRP** | | | **6-6-6** | | **7-7-7** | | **8-8-8** | | | |
| **Parameter** | | **Symbol** | **min** | **max** | **min** | **max** | **min** | **max** | | |
| Internal read command to first data | | $t_{AA}$ | 11.25 | 20 | 13.125 | 20 | 15 | 20 | ns | |
| ACT to internal read or write delay time | | $t_{RCD}$ | 11.25 | — | 13.125 | — | 15 | — | ns | |
| PRE command period | | $t_{RP}$ | 11.25 | — | 13.125 | — | 15 | — | ns | |
| ACT to ACT or REF command period | | $t_{RC}$ | 48.75 | — | 50.625 | — | 52.5 | — | ns | |
| ACT to PRE command period | | $t_{RAS}$ | 37.5 | 9 * tREFI | 37.5 | 9 * tREFI | 37.5 | 9 * tREFI | ns | |
| CL = 5 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | Reserved | | Reserved | | ns | 1,2,3,4,6, |
| | CWL = 6 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | ns | 4, |
| CL = 6 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | ns | 1,2,3,6, |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | Reserved | | Reserved | | ns | 1,2,3,4, |
| CL = 7 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | ns | 4, |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | Reserved | | ns | 1,2,3,4, |
| CL = 8 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | ns | 4, |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | ns | 1,2,3, |
| Supported CL Settings | | | 5, 6, 7, 8 | | 6, 7, 8 | | 6, 8 | | $n_{CK}$ | |
| Supported CWL Settings | | | 5, 6 | | 5, 6 | | 5, 6 | | $n_{CK}$ | |

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**12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)**
**12.3 Standard Speed Bins (Cont'd)**

## Table 65 — DDR3-1333 Speed Bins

| For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 148. | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Speed Bin** | | | **DDR3-1333F (optional)** | | **DDR3-1333G** | | **DDR3-1333H** | | **DDR3-1333J (optional)** | | **Unit** | **Note** |
| **CL - nRCD - nRP** | | | **7-7-7** | | **8-8-8** | | **9-9-9** | | **10-10-10** | | | |
| **Parameter** | | **Symbol** | **min** | **max** | **min** | **max** | **min** | **max** | **min** | **max** | | |
| Internal read command to first | | $t_{AA}$ | 10.5 | 20 | 12 | 20 | 13.5 | 20 | 15 | 20 | ns | |
| ACT to internal read or write delay time | | $t_{RCD}$ | 10.5 | — | 12 | — | 13.5 | — | 15 | — | ns | |
| PRE command period | | $t_{RP}$ | 10.5 | — | 12 | — | 13.5 | — | 15 | — | ns | |
| ACT to ACT or REF command period | | $t_{RC}$ | 46.5 | — | 48 | — | 49.5 | — | 51 | — | ns | |
| ACT to PRE command period | | $t_{RAS}$ | 36 | 9 * tREFI | 36 | 9 * tREFI | 36 | 9 * tREFI | 36 | 9 * tREFI | ns | |
| CL = 5 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | Reserved | | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 6, 7 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| CL = 6 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | ns | 1,2,3,7 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | Reserved | | Reserved | | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 7 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| CL = 7 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | Reserved | | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | Reserved | | Reserved | | Reserved | | ns | 1,2,3,4 |
| CL = 8 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | ns | 1,2,3,7 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | Reserved | | Reserved | | ns | 1,2,3,4 |
| CL = 9 | CWL = 5, 6 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | Reserved | | ns | 1,2,3,4 |
| CL = 10 | CWL = 5, 6 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | ns | 1,2,3 |
| | | | (Optional) | | (Optional) | | (Optional) | | | | ns | 5 |
| Supported CL Settings | | | 5, 6, 7, 8, 9 | | 5, 6, 7, 8, 9 | | 6, 8, 9 | | 6, 8, 10 | | $n_{CK}$ | |
| Supported CWL Settings | | | 5, 6, 7 | | 5, 6, 7 | | 5, 6, 7 | | 5, 6, 7 | | $n_{CK}$ | |

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**12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)**
**12.3 Standard Speed Bins (Cont'd)**

## Table 66 — DDR3-1600 Speed Bins

| For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 148. | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Speed Bin** | | | **DDR3-1600G (optional)** | | **DDR3-1600H** | | **DDR3-1600J** | | **DDR3-1600K (optional)** | | **Unit** | **Note** |
| **CL - nRCD - nRP** | | | **8-8-8** | | **9-9-9** | | **10-10-10** | | **11-11-11** | | | |
| **Parameter** | | **Symbol** | **min** | **max** | **min** | **max** | **min** | **max** | **min** | **max** | | |
| Internal read command to first data | | $t_{AA}$ | 10 | 20 | 11.25 | 20 | 12.5 | 20 | 13.75 | 20 | ns | |
| ACT to internal read or write delay time | | $t_{RCD}$ | 10 | — | 11.25 | — | 12.5 | — | 13.75 | — | ns | |
| PRE command period | | $t_{RP}$ | 10 | — | 11.25 | — | 12.5 | — | 13.75 | — | ns | |
| ACT to ACT or REF command period | | $t_{RC}$ | 45 | — | 46.25 | — | 47.5 | — | 48.75 | — | ns | |
| ACT to PRE command period | | $t_{RAS}$ | 35 | 9 * tREFI | 35 | 9 * tREFI | 35 | 9 * tREFI | 35 | 9 * tREFI | ns | |
| CL = 5 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 6, 7, 8 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| CL = 6 | CWL = 5 | $t_{CK(AVG)}$ | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | ns | 1,2,3,8 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | Reserved | | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 7, 8 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| CL = 7 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | Reserved | | Reserved | | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 8 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| CL = 8 | CWL = 5 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 6 | $t_{CK(AVG)}$ | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | 1.875 | < 2.5 | ns | 1,2,3,8 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | Reserved | | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 8 | $t_{CK(AVG)}$ | 1.25 | < 1.5 | Reserved | | Reserved | | Reserved | | ns | 1,2,3,4 |
| CL = 9 | CWL = 5, 6 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | Reserved | | ns | 1,2,3,4,8 |
| | CWL = 8 | $t_{CK(AVG)}$ | 1.25 | < 1.5 | 1.25 | < 1.5 | Reserved | | Reserved | | ns | 1,2,3,4 |
| CL = 10 | CWL = 5, 6 | $t_{CK(AVG)}$ | Reserved | | Reserved | | Reserved | | Reserved | | ns | 4 |
| | CWL = 7 | $t_{CK(AVG)}$ | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | 1.5 | <1.875 | ns | 1,2,3,8 |
| | CWL = 8 | $t_{CK(AVG)}$ | 1.25 | < 1.5 | 1.25 | < 1.5 | 1.25 | < 1.5 | Reserved | | ns | 1,2,3,4 |

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**12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)**
**12.3 Standard Speed Bins (Cont'd)**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CL = 11 | CWL = 5, 6, 7 | $t_{CK(AVG)}$ | Reserved | | | Reserved | | | Reserved | | | Reserved | | | ns | 4 |
| | CWL = 8 | $t_{CK(AVG)}$ | 1.25 | < 1.5 | | 1.25 | < 1.5 | | 1.25 | < 1.5 | | 1.25 | < 1.5 | | ns | 1,2,3 |
| | | | (Optional) | | | (Optional) | | | (Optional) | | | | | | ns | 5 |
| Supported CL Settings | | | 5, 6, 7, 8, 9, 10 | | | 5, 6, 7, 8, 9, 10 | | | 5, 6, 7, 8, 9, 10 | | | 6, 8, 10, 11 | | | $n_{CK}$ | |
| Supported CWL Settings | | | 5, 6, 7, 8 | | | 5, 6, 7, 8 | | | 5, 6, 7, 8 | | | 5, 6, 7, 8 | | | $n_{CK}$ | |

### 12.3.1 Speed Bin Table Notes

Absolute Specification ($T_{OPER}$; $V_{DDQ}$ = $V_{DD}$ = 1.5V +/- 0.075 V);

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

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# 13 Electrical Characteristics and AC Timing

## Table 67 — Timing Parameters by Speed Bin

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| | | | | | | | | | | | |
| **Clock Timing** | | | | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK(DLL_OFF) | 8 | - | 8 | - | 8 | - | 8 | - | ns | 6 |
| Average Clock Period | tCK(avg) | See 12.3 “Standard Speed Bins” on page 144 | | | | | | | | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | tCK(avg) min + tJIT(per) min | tCK(avg) max + tJIT(per) max | tCK(avg) min + tJIT(per) min | tCK(avg) max + tJIT(per) max | tCK(avg) min + tJIT(per) min | tCK(avg) max + tJIT(per) max | tCK(avg) min + tJIT(per) min | tCK(avg) max + tJIT(per) max | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | 0.43 | - | 0.43 | - | 0.43 | - | tCK(avg) | 25 |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | 0.43 | - | 0.43 | - | 0.43 | - | tCK(avg) | 26 |
| Clock Period Jitter | JIT(per) | - 100 | 100 | - 90 | 90 | - 80 | 80 | -70 | 70 | ps | |
| Clock Period Jitter during DLL locking period | tJIT(per, lck) | - 90 | 90 | - 80 | 80 | - 70 | 70 | -60 | 60 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 200 | | 180 | | 160 | | 140 | | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc, lck) | 180 | | 160 | | 140 | | 120 | | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | - | - | - | - | - | - | ps | |
| Cumulative error across 2 cycles | tERR(2per) | - 147 | 147 | - 132 | 132 | - 118 | 118 | - 103 | 103 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | - 175 | 175 | - 157 | 157 | - 140 | 140 | - 122 | 122 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | - 194 | 194 | - 175 | 175 | - 155 | 155 | - 136 | 136 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | - 209 | 209 | - 188 | 188 | - 168 | 168 | - 147 | 147 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | - 222 | 222 | - 200 | 200 | - 177 | 177 | - 155 | 155 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | - 232 | 232 | - 209 | 209 | - 186 | 186 | - 163 | 163 | ps | |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| Cumulative error across 8 cycles | tERR(8per) | - 241 | 241 | - 217 | 217 | - 193 | 193 | - 169 | 169 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | - 249 | 249 | - 224 | 224 | - 200 | 200 | - 175 | 175 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | - 257 | 257 | - 231 | 231 | - 205 | 205 | - 180 | 180 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | - 263 | 263 | - 237 | 237 | - 210 | 210 | - 184 | 184 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | - 269 | 269 | - 242 | 242 | - 215 | 215 | - 188 | 188 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | $^{t}$ERR(nper)min = (1 + 0.68ln(n)) * $^{t}$JIT(per)min<br>$^{t}$ERR(nper)max = (1 + 0.68ln(n)) * $^{t}$JIT(per)max | | | | | | | | ps | 24 |
| **Data Timing** | | | | | | | | | | | |
| DQS, DQS# to DQ skew, per group, per access | tDQSQ | - | 200 | - | 150 | - | 125 | - | 100 | ps | 13 |
| DQ output hold time from DQS, DQS# | tQH | 0.38 | - | 0.38 | - | 0.38 | - | 0.38 | - | tCK(avg) | 13, b |
| DQ low-impedance time from CK, CK# | tLZ(DQ) | - 800 | 400 | - 600 | 300 | - 500 | 250 | - 450 | 225 | ps | 13, 14, a |
| DQ high impedance time from CK, CK# | tHZ(DQ) | - | 400 | - | 300 | - | 250 | - | 225 | ps | 13, 14, a |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) | 75 | | 25 | | TBD | | TBD | | ps | d, 17 |
| Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | tDH(base) | 150 | | 100 | | TBD | | TBD | | ps | d, 17 |
| **Data Strobe Timing** | | | | | | | | | | | |
| DQS,DQS# differential READ Preamble | tRPRE | 0.9 | Note 19 | 0.9 | Note 19 | 0.9 | Note 19 | 0.9 | Note 19 | tCK(avg) | 13, 19, b |
| DQS, DQS# differential READ Postamble | tRPST | 0.3 | Note 11 | 0.3 | Note 11 | 0.3 | Note 11 | 0.3 | Note 11 | tCK(avg) | 11, 13, b |
| DQS, DQS# differential output high time | tQSH | 0.38 | - | 0.38 | - | 0.40 | - | 0.40 | - | tCK(avg) | 13, b |
| DQS, DQS# differential output low time | tQSL | 0.38 | - | 0.38 | - | 0.40 | - | 0.40 | - | tCK(avg) | 13, b |
| DQS, DQS# differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | 0.9 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Postamble | tWPST | 0.3 | - | 0.3 | - | 0.3 | - | 0.3 | - | tCK(avg) | |
| DQS, DQS# rising edge output access time from rising CK, CK# | tDQSCK | - 400 | 400 | - 300 | 300 | - 255 | 255 | - 225 | 225 | ps | 13, a |
| DQS and DQS# low-impedance time (Referenced from RL - 1) | tLZ(DQS) | - 800 | 400 | - 600 | 300 | - 500 | 250 | - 450 | 225 | ps | 13, 14, a |
| DQS and DQS# high-impedance time (Referenced from RL + BL/2) | tHZ(DQS) | - | 400 | - | 300 | - | 250 | - | 225 | ps | 13, 14, a |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| DQS, DQS# differential input low pulse width | tDQSL | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK(avg) | |
| DQS, DQS# differential input high pulse width | tDQSH | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK(avg) | |
| DQS, DQS# rising edge to CK, CK# rising edge | tDQSS | - 0.25 | 0.25 | - 0.25 | 0.25 | - 0.25 | 0.25 | - 0.25 | 0.25 | tCK(avg) | c |
| DQS, DQS# falling edge setup time to CK, CK# rising edge | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | 0.2 | - | tCK(avg) | c |
| DQS, DQS# falling edge hold time from CK, CK# rising edge | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | 0.2 | - | tCK(avg) | c |
| **Command and Address Timing** | | | | | | | | | | | |
| DLL locking time | tDLLK | 512 | - | 512 | - | 512 | - | 512 | - | nCK | |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | | e |
| Delay from start of internal write transaction to internal read command | tWTR | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | | e, 18 |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | 15 | - | ns | e |
| Mode Register Set command cycle time | tMRD | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | max(12nCK, 15ns) | - | max(12nCK, 15ns) | - | max(12nCK, 15ns) | - | max(12nCK, 15ns) | - | | |
| ACT to internal read or write delay time | tRCD | Refer to Table 63 to Table 66 on pages pages 144 to pages 147 | | | | | | | | | e |
| PRE command period | tRP | Refer to Table 63 to Table 66 on pages pages 144 to pages 147 | | | | | | | | | e |
| ACT to ACT or REF command period | tRC | Refer to Table 63 to Table 66 on pages pages 144 to pages 147 | | | | | | | | | e |
| CAS# to CAS# command delay | tCCD | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup(tRP / tCK(avg)) | | | | | | | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 22 |
| ACTIVE to PRECHARGE command period | tRAS | See 12.3 "Standard Speed Bins" on page 144 | | | | | | | | | e |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max(4nCK, 10ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 6ns) | - | max(4nCK, 6ns) | - | | e |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | max(4nCK, 10ns) | - | max(4nCK, 10ns) | - | max(4nCK, 7.5ns) | - | max(4nCK, 7.5ns) | - | | e |
| Four activate window for 1KB page size | tFAW | 40 | - | 37.5 | - | 30 | - | 30 | - | ns | e |
| Four activate window for 2KB page size | tFAW | 50 | - | 50 | - | 45 | - | 40 | - | ns | e |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 200 | | 125 | | 65 | | TBD | | ps | b, 16 |
| Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 275 | | 200 | | 140 | | TBD | | ps | b, 16 |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) AC150 | - | - | - | - | 65 + 125 | | TBD + 125 | | ps | b, 16, 27 |
| **Calibration Timing** | | | | | | | | | | | |
| Power-up and RESET calibration time | tZQinit | 512 | - | 512 | - | 512 | - | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | 256 | - | 256 | - | 256 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 64 | - | 64 | - | 64 | - | 64 | - | nCK | 23 |
| **Reset Timing** | | | | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | | |
| **Self Refresh Timings** | | | | | | | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | max(5nCK, tRFC(min) + 10ns) | - | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKE(min) + 1 nCK | - | tCKE(min) + 1 nCK | - | tCKE(min) + 1 nCK | - | tCKE(min) + 1 nCK | - | | |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | max(5 nCK, 10 ns) | - | | |
| **Power Down Timings** | | | | | | | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max(3nCK, 7.5ns) | - | max(3nCK, 7.5ns) | - | max(3nCK, 6ns) | - | max(3nCK, 6ns) | - | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | max(10nCK, 24ns) | - | max(10nCK, 24ns) | - | max(10nCK, 24ns) | - | max(10nCK, 24ns) | - | | 2 |
| CKE minimum pulse width | tCKE | max(3nCK 7.5ns) | - | max(3nCK, 5.625ns) | - | max(3nCK, 5.625ns) | - | max(3nCK, 5ns) | - | | |
| Command pass disable delay | tCPDED | 1 | - | 1 | - | 1 | - | 1 | - | nCK | |
| Power Down Entry to Exit Timing | tPD | tCKE(min) | 9 * tREFI | tCKE(min) | 9 * tREFI | tCKE(min) | 9 * tREFI | tCKE(min) | 9 * tREFI | | 15 |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 20 |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 20 |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL + 4 + 1 | - | RL + 4 + 1 | - | RL + 4 + 1 | - | RL + 4 + 1 | - | nCK | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL + 4 + (tWR / tCK(avg)) | - | WL + 4 + (tWR / tCK(avg)) | - | WL + 4 + (tWR / tCK(avg)) | - | WL + 4 + (tWR / tCK(avg)) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL + 4 + WR + 1 | - | WL + 4 + WR + 1 | - | WL + 4 + WR + 1 | - | WL + 4 + WR + 1 | - | nCK | 10 |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | WL + 2 + (tWR / tCK(avg) ) | - | WL + 2 + (tWR / tCK(avg) ) | - | WL + 2 + (tWR / tCK(avg) ) | - | WL + 2 + (tWR / tCK(avg) ) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPDEN | WL + 2 + WR + 1 | - | WL + 2 + WR + 1 | - | WL + 2 + WR + 1 | - | WL + 2 + WR + 1 | - | nCK | 10 |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 20, 21 |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | | |
| **ODT Timings** | | | | | | | | | | | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | 6 | - | 6 | - | 6 | - | nCK | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 1 | 9 | 1 | 9 | 1 | 9 | 1 | 9 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 1 | 9 | 1 | 9 | 1 | 9 | 1 | 9 | ns | |
| RTT turn-on | tAON | -400 | 400 | -300 | 300 | -250 | 250 | -225 | 225 | ps | 7, a |
| RTT_Nom and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | 8, a |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | a |
| **Write Leveling Timings** | | | | | | | | | | | |
| First DQS/DQS# rising edge after write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | 40 | - | nCK | 3 |
| DQS/DQS# delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | 25 | - | nCK | 3 |
| Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing | tWLS | 325 | - | 245 | - | 195 | - | TBD | - | ps | |
| Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing | tWLH | 325 | - | 245 | - | 195 | - | TBD | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | 0 | 9 | 0 | 9 | 0 | 7.5 | ns | |

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## Table 67 — Timing Parameters by Speed Bin (Cont.)

**Note:** The following general notes from page 156 apply to Table 67: a

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | 0 | 2 | 0 | 2 | ns | |



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## 13.1 Jitter Notes

Specific Note a When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note b When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

Specific Note c These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.

Specific Note e For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

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**13 Electrical Characteristics and AC Timing (Cont'd)**

## 13.2 Timing Parameter Notes

Notes:

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON See 5.2.2 "Timing Parameters" on page 81.
8. For definition of RTT turn-off time tAOF See 5.2.2 "Timing Parameters" on page 81.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum postamble is bound by tHZDQS(max)
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 13.3 "Address / Command Setup, Hold and Derating" on page 159
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 13.4 "Data Setup, Hold and Slew Rate Derating" on page 166.
18. Start of internal write transaction is definited as follows:

    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by tLZDQS(min)
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXP-DLL(min) is also required. See 4.16.3 "Power-Down clarifications - Case 2" on page 78
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.2 Timing Parameter Notes (Cont'd)**

between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / $^{o}$C, VSens = 0.15% / mV, Tdriftrate = 1 $^{o}$C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

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## 13.3 Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 68) to the ΔtIS and ΔtIH derating value (see Table 69) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure Figure 101). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 103).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 102). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 104).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see Table 71).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 69, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

### Table 68 — ADD/CMD Setup and Hold Base-Values for 1V/ns

| Unit [ps] | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Reference |
|---|---|---|---|---|---|
| tIS(base) | 200 | 125 | 65 | TBD | $V_{IH/L(ac)}$ |
| tIH(base) | 275 | 200 | 140 | TBD | $V_{IH/L(dc)}$ |
| tIH(base) AC150 | - | - | 65 + 125 | TBD + 125 | $V_{IH/L(dc)}$ |

1. (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)
2. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.3 Address / Command Setup, Hold and Derating (Cont'd)**

## Table 69 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based

| ΔtIS, ΔtIH derating in [ps] AC/DC based<br>AC175 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CK,CK# Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| CMD/ ADD Slew rate V/ns | 2.0 | 88 | 50 | 88 | 50 | 88 | 50 | 96 | 58 | 104 | 66 | 112 | 74 | 120 | 84 | 128 | 100 |
| | 1.5 | 59 | 34 | 59 | 34 | 59 | 34 | 67 | 42 | 75 | 50 | 83 | 58 | 91 | 68 | 99 | 84 |
| | 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| | 0.9 | -2 | -4 | -2 | -4 | -2 | -4 | 6 | 4 | 14 | 12 | 22 | 20 | 30 | 30 | 38 | 46 |
| | 0.8 | -6 | -10 | -6 | -10 | -6 | -10 | 2 | -2 | 10 | 6 | 18 | 14 | 26 | 24 | 34 | 40 |
| | 0.7 | -11 | -16 | -11 | -16 | -11 | -16 | -3 | -8 | 5 | 0 | 13 | 8 | 21 | 18 | 29 | 34 |
| | 0.6 | -17 | -26 | -17 | -26 | -17 | -26 | -9 | -18 | -1 | -10 | 7 | -2 | 15 | 8 | 23 | 24 |
| | 0.5 | -35 | -40 | -35 | -40 | -35 | -40 | -27 | -32 | -19 | -24 | -11 | -16 | -2 | -6 | 5 | 10 |
| | 0.4 | -62 | -60 | -62 | -60 | -62 | -60 | -54 | -52 | -46 | -44 | -38 | -36 | -30 | -26 | -22 | -10 |

## Table 70 — Derating values DDR3-1333/1600 tIS/tIH - ac/dc based - Alternate AC150 Threshold

| ΔtIS, ΔtIH derating in [ps] AC/DC based<br>Alternate AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CK,CK# Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| CMD/ ADD Slew rate V/ns | 2.0 | 75 | 50 | 75 | 50 | 75 | 50 | 83 | 58 | 91 | 66 | 99 | 74 | 107 | 84 | 115 | 100 |
| | 1.5 | 50 | 34 | 50 | 34 | 50 | 34 | 58 | 42 | 66 | 50 | 74 | 58 | 82 | 68 | 90 | 84 |
| | 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| | 0.9 | 0 | -4 | 0 | -4 | 0 | -4 | 8 | 4 | 16 | 12 | 24 | 20 | 32 | 30 | 40 | 46 |
| | 0.8 | 0 | -10 | 0 | -10 | 0 | -10 | 8 | -2 | 16 | 6 | 24 | 14 | 32 | 24 | 40 | 40 |
| | 0.7 | 0 | -16 | 0 | -16 | 0 | -16 | 8 | -8 | 16 | 0 | 24 | 8 | 32 | 18 | 40 | 34 |
| | 0.6 | -1 | -26 | -1 | -26 | -1 | -26 | 7 | -18 | 15 | -10 | 23 | -2 | 31 | 8 | 39 | 24 |
| | 0.5 | -10 | -40 | -10 | -40 | -10 | -40 | -2 | -32 | 6 | -24 | 14 | -16 | 22 | -6 | 30 | 10 |
| | 0.4 | -25 | -60 | -25 | -60 | -25 | -60 | -17 | -52 | -9 | -44 | -1 | -36 | 7 | -26 | 15 | -10 |

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.3 Address / Command Setup, Hold and Derating (Cont'd)**

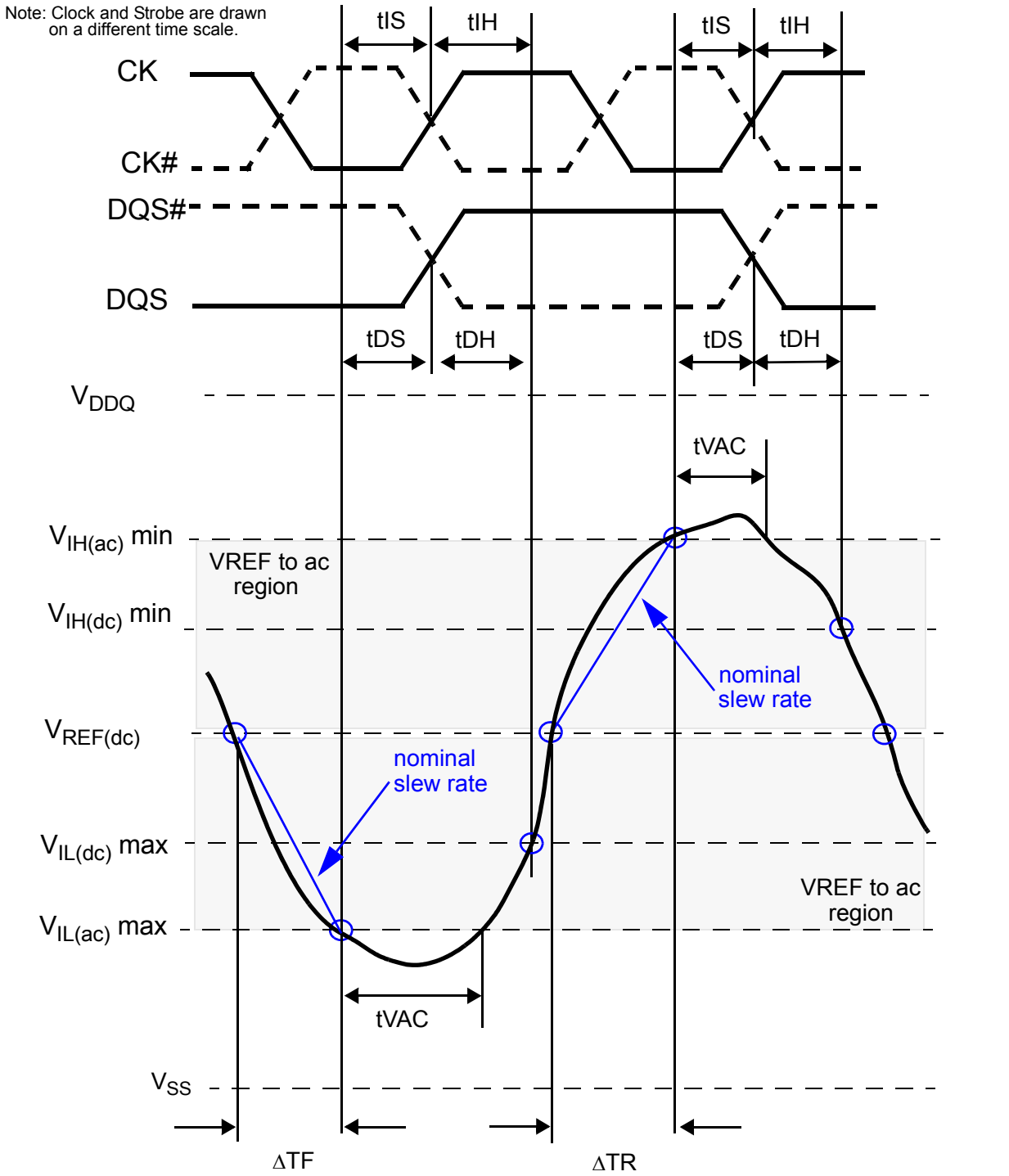
## Table 71 — Required time $t_{VAC}$ above VIH(ac) {below VIL(ac)} for valid transition

| Slew Rate [V/ns] | $t_{VAC}$ @ 175mV [ps] | | $t_{VAC}$ @ 150mV [ps] | |
|---|---|---|---|---|
| | min | max | min | max |
| > 2.0 | 75 | - | 175 | - |
| 2.0 | 57 | - | 170 | - |
| 1.5 | 50 | - | 167 | - |
| 1.0 | 38 | - | 163 | - |
| 0.9 | 34 | - | 162 | - |
| 0.8 | 29 | - | 161 | - |
| 0.7 | 22 | - | 159 | - |
| 0.6 | 13 | - | 155 | - |
| 0.5 | 0 | - | 150 | - |
| < 0.5 | 0 | - | 150 | - |

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.3 Address / Command Setup, Hold and Derating (Cont'd)**




$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

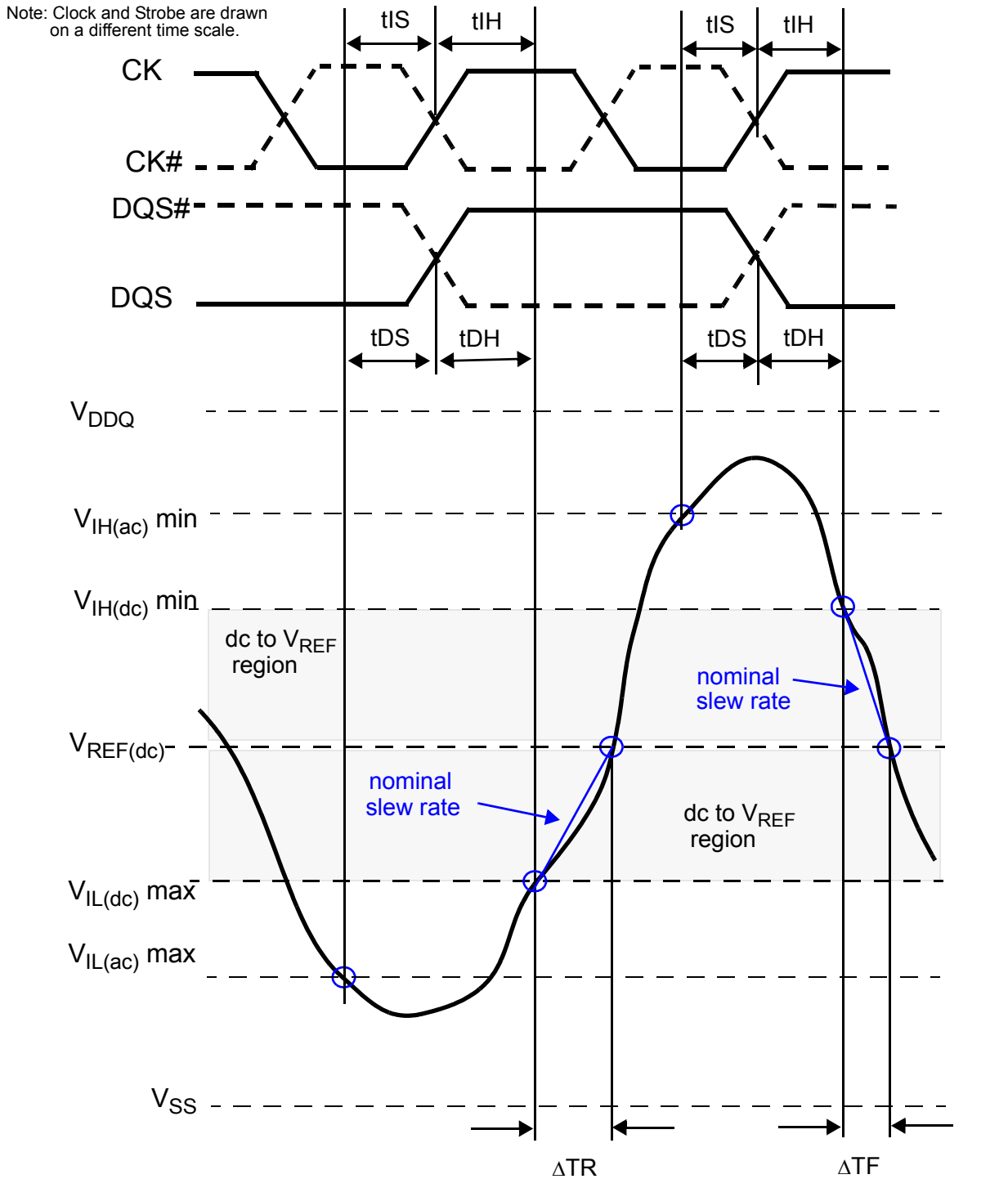
**Figure 101 — Illustration of nominal slew rate and $t_{VAC}$ for setup time $t_{DS}$ (for DQ with respect to strobe) and $t_{IS}$ (for ADD/CMD with respect to clock).**

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.3 Address / Command Setup, Hold and Derating (Cont'd)**




$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

**Figure 102 — Illustration of nominal slew rate for hold time $t_{DH}$ (for DQ with respect to strobe) and $t_{IH}$ (for ADD/CMD with respect to clock).**

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**13.3 Address / Command Setup, Hold and Derating (Cont'd)**

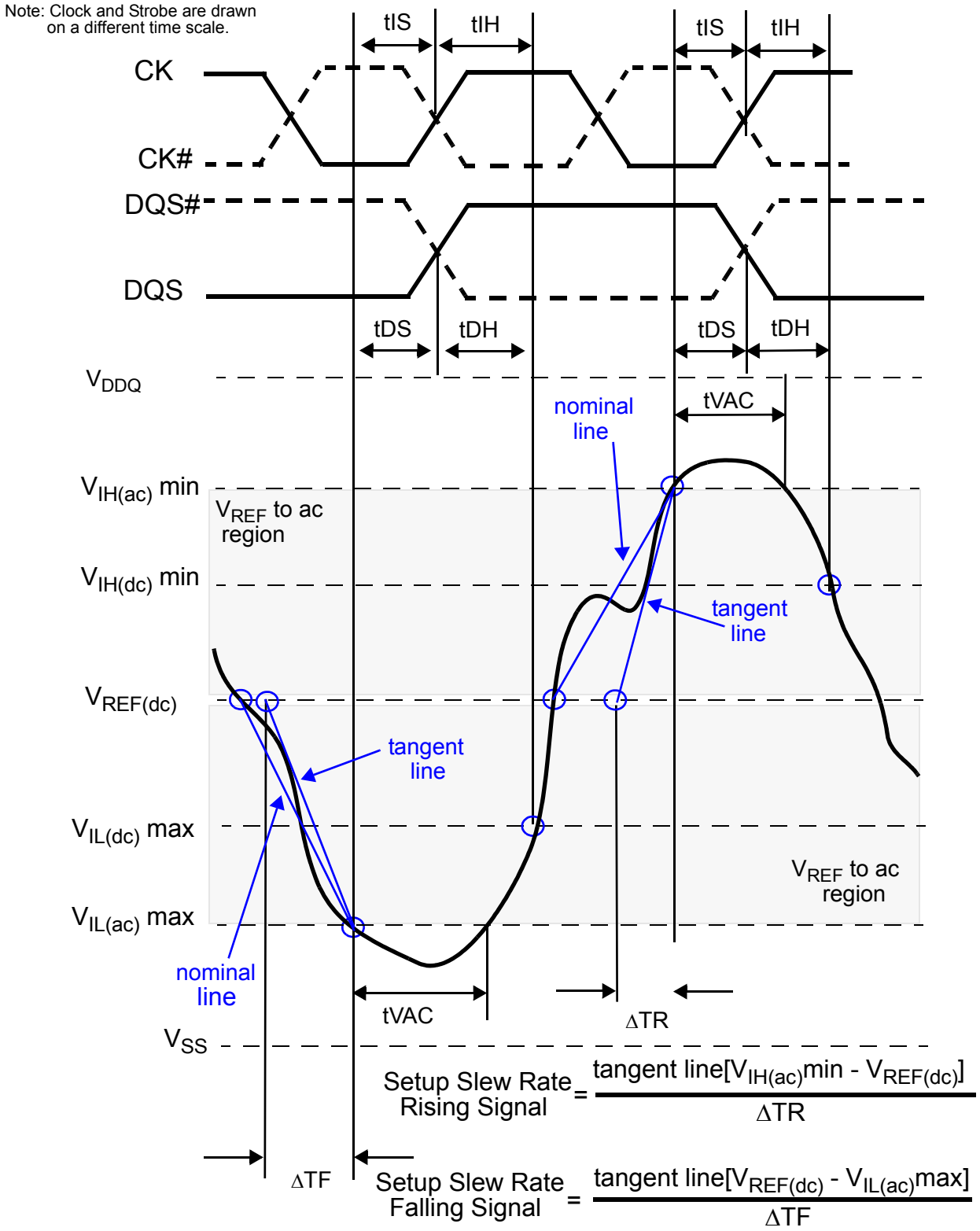



**Figure 103 — Illustration of tangent line for setup time $t_{DS}$ (for DQ with respect to strobe) and $t_{IS}$ (for ADD/CMD with respect to clock)**

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**13.3 Address / Command Setup, Hold and Derating (Cont'd)**

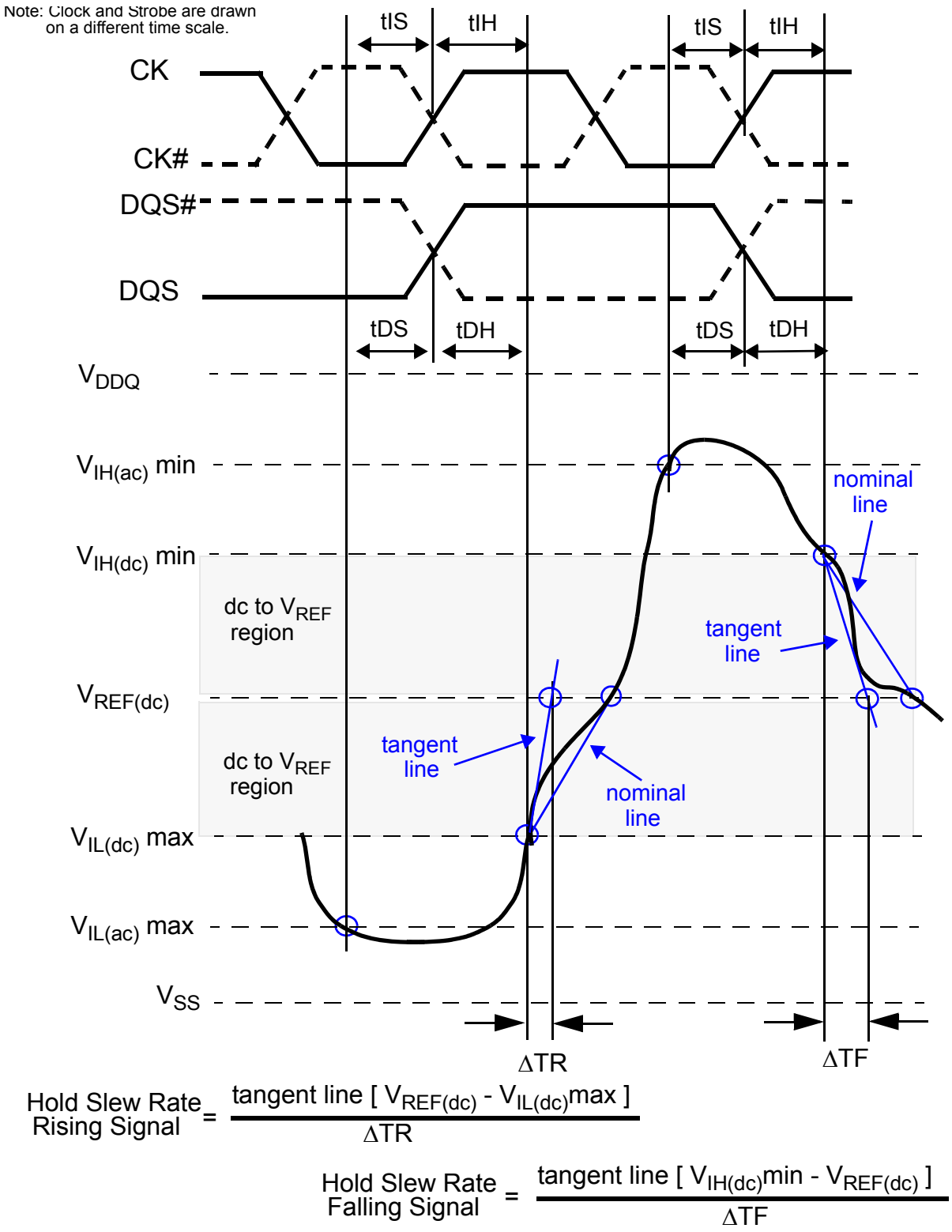



**Figure 104 — Illustration of tangent line for for hold time $t_{DH}$ (for DQ with respect to strobe) and $t_{IH}$ (for ADD/CMD with respect to clock)**

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## 13.4 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 72) to the ΔtDS and ΔtDH (see Table 73) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 105). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 107).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 106). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 108).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see Table 74).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

### Table 72 — Data Setup and Hold Base-Values

| Units [ps] | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Reference |
|---|---|---|---|---|---|
| tDS(base) | 75 | 25 | -10 | TBD | $V_{IH/L(ac)}$ |
| tDH(base) | 150 | 100 | 65 | TBD | $V_{IH/L(dc)}$ |

**Note:** (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)**

## Table 73 — Derating values DDR3-800/1066 tDS/tDH - ac/dc based

| ΔtDS, ΔDH derating in [ps] AC/DC based [1] | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DQS, DQS# Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH |
| DQ Slew rate V/ns | 2.0 | 88 | 50 | 88 | 50 | 88 | 50 | - | - | - | - | - | - | - | - | - | - |
| | 1.5 | 59 | 34 | 59 | 34 | 59 | 34 | 67 | 42 | - | - | - | - | - | - | - | - |
| | 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | - | - | - | - | - | - |
| | 0.9 | - | - | -2 | -4 | -2 | -4 | 6 | 4 | 14 | 12 | 22 | 20 | - | - | - | - |
| | 0.8 | - | - | - | - | -6 | -10 | 2 | -2 | 10 | 6 | 18 | 14 | 26 | 24 | - | - |
| | 0.7 | - | - | - | - | - | - | -3 | -8 | 5 | 0 | 13 | 8 | 21 | 18 | 29 | 34 |
| | 0.6 | - | - | - | - | - | - | - | - | -1 | -10 | 7 | -2 | 15 | 8 | 23 | 24 |
| | 0.5 | - | - | - | - | - | - | - | - | - | - | -11 | -16 | -2 | -6 | 5 | 10 |
| | 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | -30 | -26 | -22 | -10 |

NOTE:
1.Cell contents shaded in red are defined as 'not supported'.

## Table 74 — Required time $t_{VAC}$ above VIH(ac) {below VIL(ac)} for valid transition

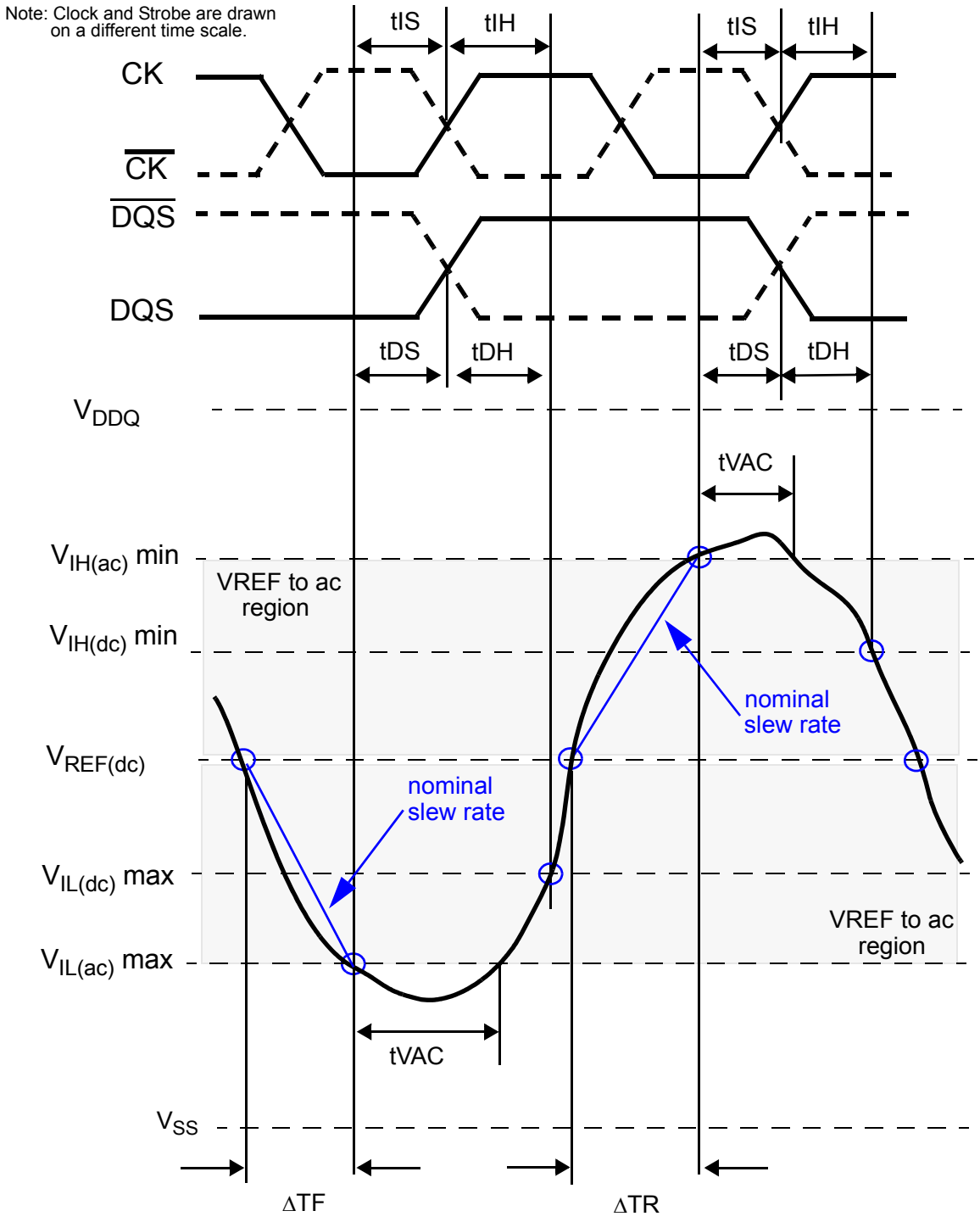
| Slew Rate [V/ns] | $t_{VAC}$ [ps] | |
|---|---|---|
| | min | max |
| > 2.0 | 75 | - |
| 2.0 | 57 | - |
| 1.5 | 50 | - |
| 1.0 | 38 | - |
| 0.9 | 34 | - |
| 0.8 | 29 | - |
| 0.7 | 22 | - |
| 0.6 | 13 | - |
| 0.5 | 0 | - |
| < 0.5 | 0 | - |

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)**




$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

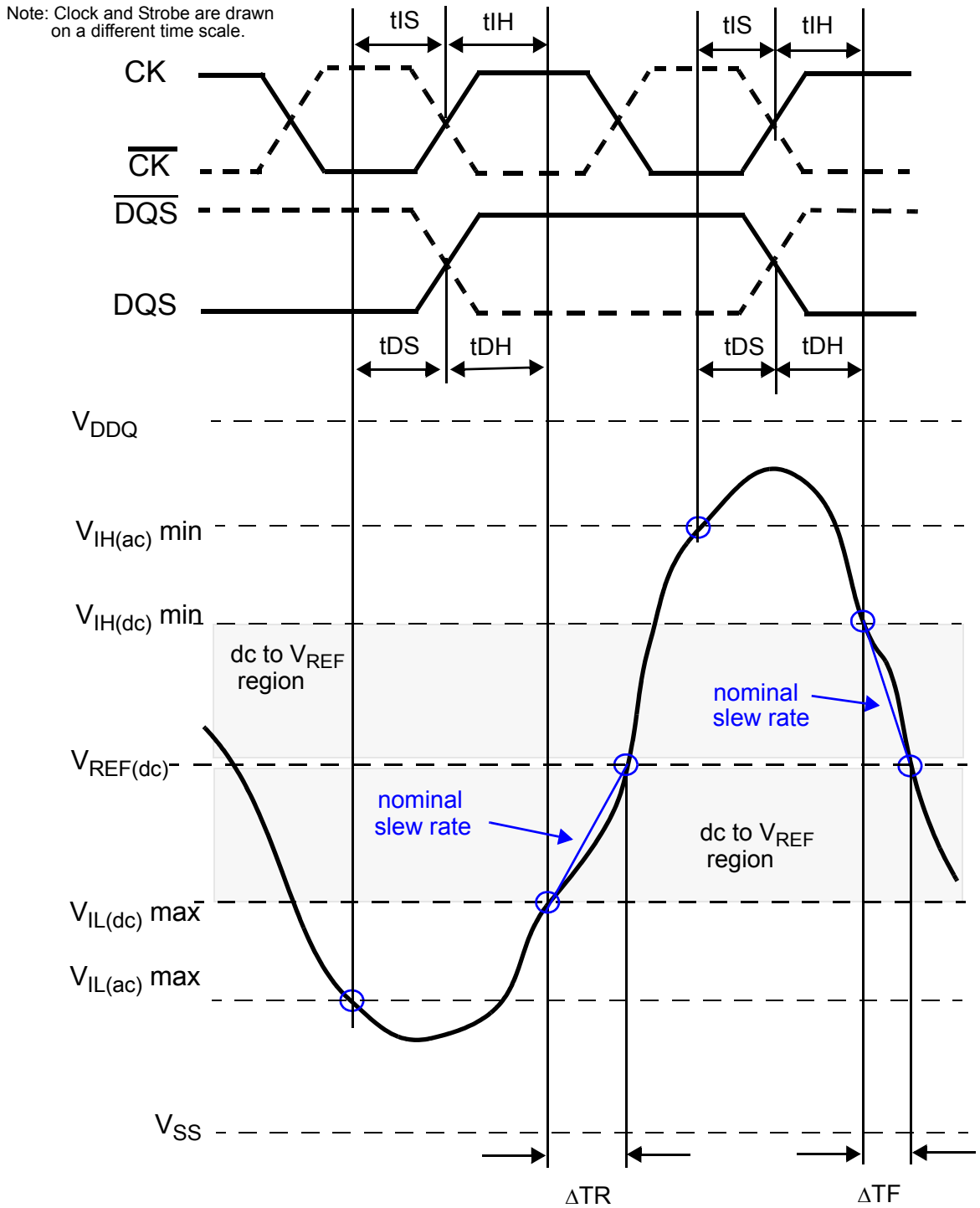
**Figure 105 — Illustration of nominal slew rate and $t_{VAC}$ for setup time $t_{DS}$ (for DQ with respect to strobe) and $t_{IS}$ (for ADD/CMD with respect to clock).**

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)**




$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

**Figure 106 — Illustration of nominal slew rate for hold time $t_{DH}$ (for DQ with respect to strobe) and $t_{IH}$ (for ADD/CMD with respect to clock).**

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)**

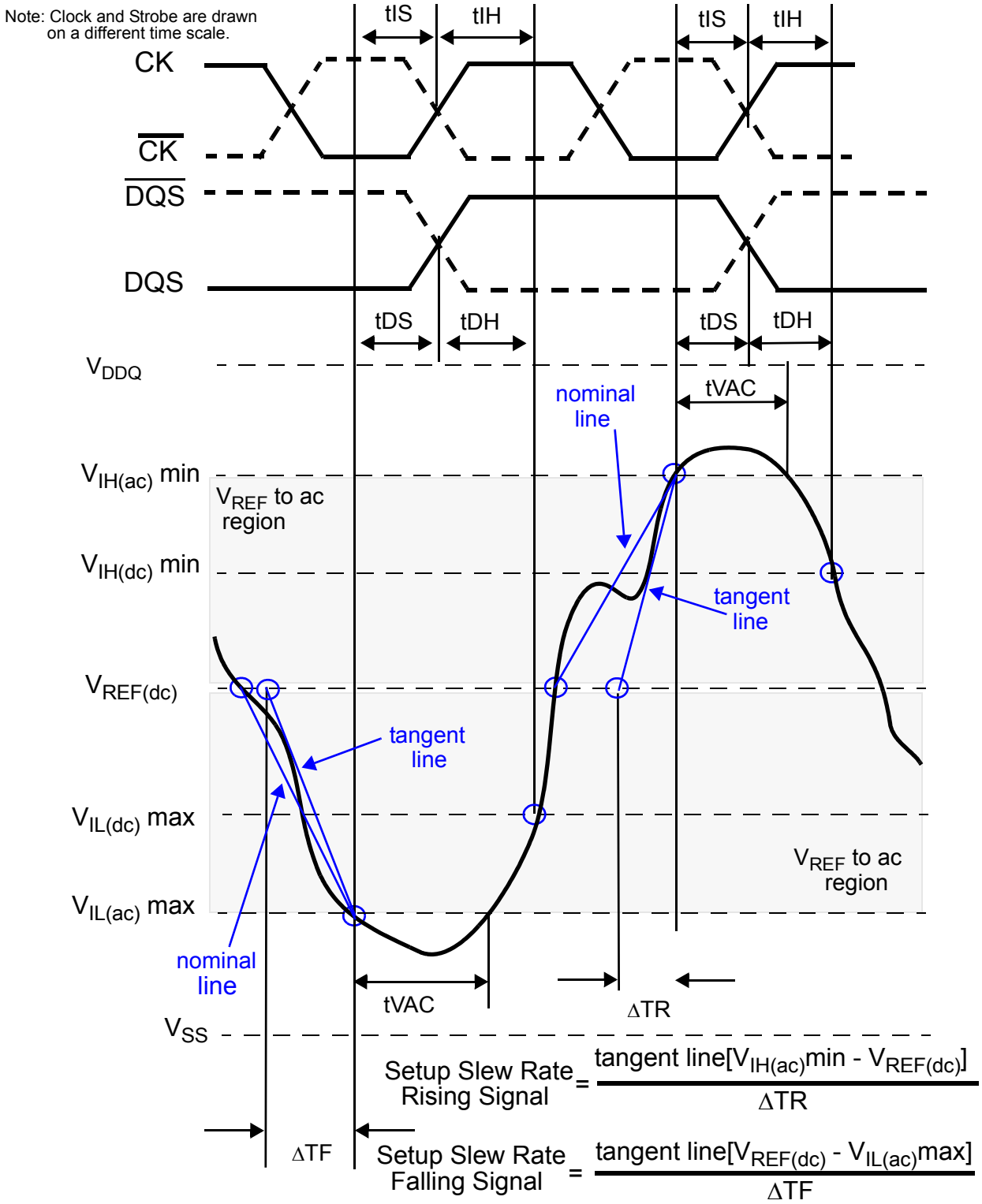



**Figure 107 — Illustration of tangent line for setup time $t_{DS}$ (for DQ with respect to strobe) and $t_{IS}$ (for ADD/CMD with respect to clock)**

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**13 Electrical Characteristics and AC Timing (Cont'd)**
**13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)**

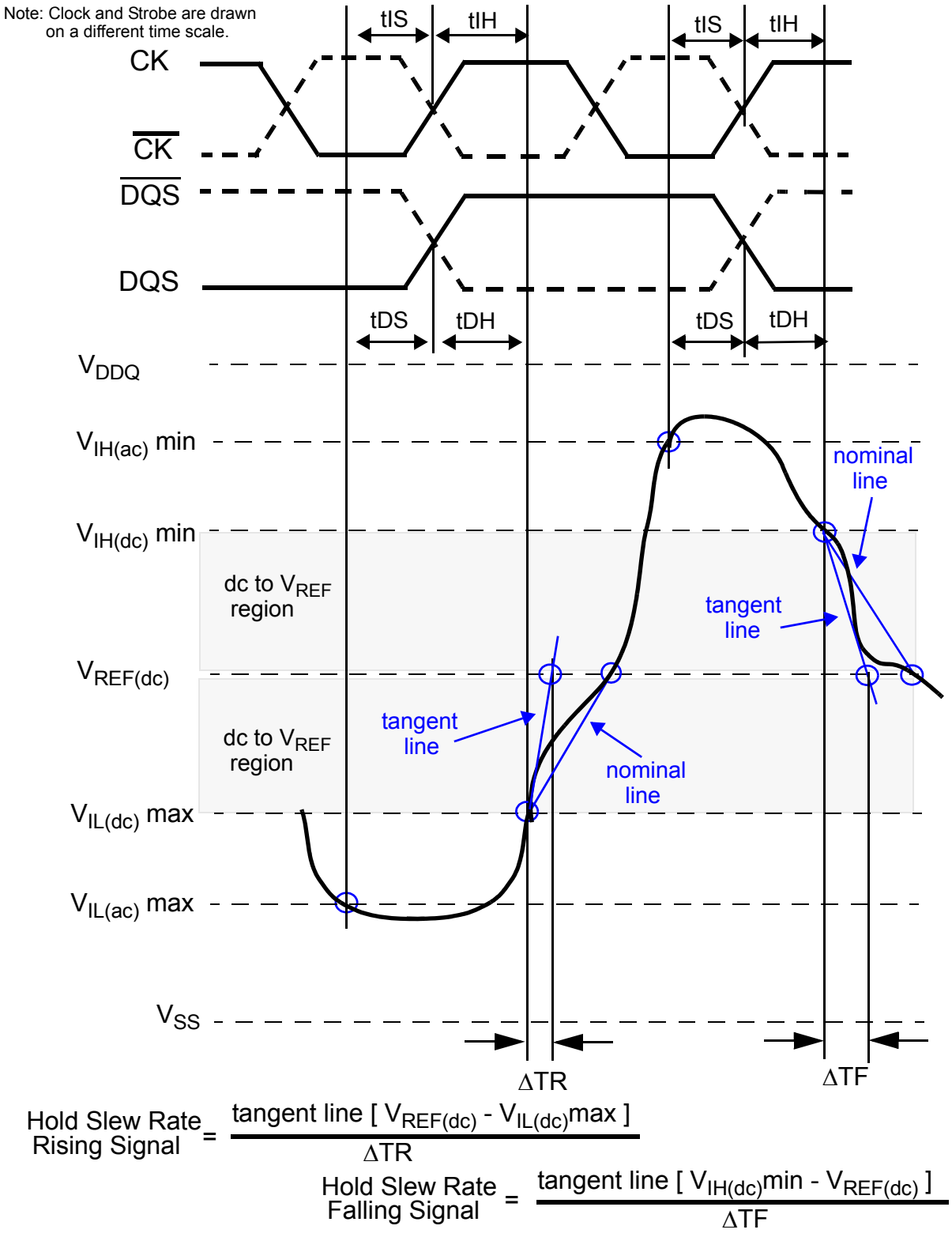



**Figure 108 — Illustration of tangent line for for hold time $t_{DH}$ (for DQ with respect to strobe) and $t_{IH}$ (for ADD/CMD with respect to clock)**

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## Annex A (informative) Differences between JESD79-3A, and JESD79-3.

This table briefly describes most of the changes made to this standard, JESD79-3A, compared to its predecessor, JESD79-3. Some editorial changes and format-updates of figures are not included.

| Page | Description of Change |
|---|---|
| 13 | Per JCB-07-070, DDR3 Specification<br>Updated Figure 1 – Simplified State Diagram<br>Updated Table 2 – State Diagram Command Definitions |
| 54 | Per JCB-07-070, DDR3 Specification<br>Updated Section 4.13.2.1 – READ Timing; Clock to Data Strobe relationship |
| 55 | Per JCB-07-070, DDR3 Specification<br>Updated Section 4.13.2.2 – READ Timing; Data Strobe to Data Strobe relationship |
| 57 | Per JCB-07-070, DDR3 Specification<br>Added Figure 28 – Method for calculationg tRPRE transitions and endpoints |
| 63 | Per JCB-07-070, DDR3 Specification<br>Removed Figure 40 – Write Timing Parameters<br>Moved Figure 45, renamed as Write Timing Definition and Parameters, to page 63, as Figure 38 |
| 64 | Per JCB-07-034, tWPRE, tWPST<br>Added Section 4.14.3 – tWPRE Calculation<br>Added Section 4.14.4 – tWPST Calculation |
| 72-79 | Per JCB-07-070, DDR3 Specification<br>Reorganized subsections 4.16.1 and 4.16.2, moving Figures 52-61 into 4.16.1 and making one subsection each (4.16.2, 3, and 4) for the power-down entry/exit clarification cases (1-3). |
| 75 | Per JCB-07-070, DDR3 Specification<br>Removed Figure 57 – Active Power-Down Entry and Exit Timing Diagram |
| 79 | Per JCB-07-070, DDR3 Specification<br>Removed Table 15 – Timing Values tXXXPDEN Parameters |
| 84 | Per JCB-07-036, ODT Read Timing<br>Updated Figure 68 – OCT must be disabled...during Reads... |
| 86 | Per JCB-07-036, ODT Read Timing<br>Updated Section 5.2.3 – ODT During READs |
| 96, 97 | Per JCB-07-067, ZQ Input Capacitance<br>Updated Section 5.5.1 – ZQ Calibration Description<br>Replaced Section 5.5.3. Is now: ZQ External Resistor Value, Tolerance, and Capacitance Loading |
| 97 | Per JCB-07-070, DDR3 Specification<br>Removed Table 22 – ZQ Calibration Command Truth Table |
| 101 | Per JCB-07-065, Vih(dc)max, Vil(dc)min<br>Updated Table 24 – Single Ended AC and DC Input Levels |
| 103-106 | Per JCB-07-068, Differention Signal Input Specification<br>Added Section 8.2 – AC and CD Logic Input Levels for Differential Signals |
| 128 | Per JCB-07-070, DDR3 Specification<br>Updated Table 50 – For IDD testing the followign parameters are utilized |

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| Page | Description of Change |
|---|---|
| 141 | Per JCB-07-038, Capacitance<br>Updated Table 61 – Input/Output Capacitance |
| 141 | Per JCB-07-067, ZQ Input Capacitance<br>Updated Table 61 – Input/Output Capacitance |
| 142, 143 | Per JCB-07-070, DDR3 Specification<br>Removed unnumbered tables from subsection 12.1. Moved subsection 12.2 material into 12.1. Renumbered subsequent subsections. |
| 149 | Per JCB-07-041, tJIT (duty) note modification<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 149, 150 | Per JCB-07-032, Cumulative Jitter<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 150 | Per JCB-07-034, tWPRE, tWPST<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 150 | Per JCB-07-040, Jitter Values for DDR3-1600<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 150 | Per JCB-07-029, Jitter Output Derating<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 150 | Per JCB-07-031, tDQSCK tQH<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 150 | Per JCB-07-066, tQSH, tQSL values<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 152 | Per JCB-07-042, tIS, tIH, DDR3-1333<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 154 | Per JCB-07-035, tWLS, tWLH<br>Updated Table 67 – Timing Parameters by Speed Bin |
| 156-158 | Per JCB-07-033, tCH (abs) and tCL (abs)<br>Removed Specific Note F from Table 67 – Timing Parameters by Speed Bin. This action included remvoing the Table – Min and Max SPEC values.<br>Removed Note 22 from Table 67 – Timing Parameters by Speed Bin<br>Added Notes 25 and 26 to Table 67 – Timing Parameters by Speed Bin |
| 157 | Per JCB-07-039, tZQCS<br>Added Note 23 |
| 157, 158 | Per JCB-07-039, tZQCS<br>Updated Note 23 of Table 67 – Timing Parameters by Speed Bin |
| 158 | Per JCB-07-042, tIS, tIH, DDR3-1333<br>Added Note 27 |
| 159 | Per JCB-07-027<br>Updated Table 68 – ADD/CMD Setup and Hold Base-Values for 1V/ns |

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This table briefly describes most of the changes made to this standard, JESD79-3A, compared to its predecessor, JESD79-3. Some editorial changes and format-updates of figures are not included.

| Page | Description of Change |
|---|---|
| 160 | Per JCB-07-027<br>Updated Table 69 – Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based<br>Added Table 70 – Derating values DDR3-1333/1600 tIS/tIH - ac/dc based - Alternate AC150 Threshold |
| 161 | Per JCB-07-027<br>Updated Table 71 – Required time $T_{VAC}$ above VIH(ac) [below VIL(ac)] for valid transition |
| 166 | Per JCB-07-037, tDS, tDH 1333<br>Updated Table 72 – Data Setup and Hold Base-Values |
| A-1 | Added Annex A (Informative) Differences between JESD79-3A and JESD79-3. |

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