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Paper 34
Entered: June 20, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00236
Patent 9,824,035 B2

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively, "Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1, 2, 6, 10–13, 21, and 22 ("the challenged claims") of U.S. Patent No. 9,824,035 B2 ("the '035 patent," Ex. 1001). Netlist, Inc. ("Patent Owner") timely filed a Preliminary Response (Paper 12, "Prelim. Resp."). On July 19, 2022, upon consideration of the Petition, Preliminary Response, and the cited evidence, we determined that Petitioner established a reasonable likelihood that it would prevail with respect to at least one of the challenged claims and instituted review to determine the patentability of the challenged claims on all grounds. Paper 16.

After institution, Patent Owner filed a Patent Owner Response (Paper 21, "PO Resp."), Petitioner filed a Reply (Paper 26, "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 27, "PO Sur-reply"). An oral hearing was held on April 19, 2023, and the hearing transcript is included in the record. Paper 33 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 (2019), addresses issues and evidence raised during the *inter partes* review. For the reasons that follow, Petitioner demonstrates by a preponderance of the evidence that claims 1, 10–13, and 21 of the '035 patent are unpatentable. However, we determine that Petitioner has not demonstrated that claims 2, 6 and 22 of the '035 patent are unpatentable.

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B. Related Proceedings

The parties identify the following matter as related to this case: *Netlist, Inc. v. Micron Technology, Inc., et al.*, Case No. 6:21-cv-00431-ADA (W.D. Tex.). Pet. 76; Paper 6, 1. Patent Owner states that matter was subsequently "transferred from the U.S. District Court for the Western District of Texas, Waco Division to the U.S. District Court for the Western District of Texas, Austin Division and docketed as" *Netlist, Inc. v. Micron Technology, Inc., et al.*, 1:22-cv-00136-LY (W.D. Tex.). Paper 6, 1.

Petitioner also identifies IPR2022-00237 as involving the child of the '035 patent. Pet. 77. Petitioner further identifies IPR2017-00730 as involving the parent of the '035 patent. *Id.* at 76.

C. The '035 Patent (Ex. 1001)

The '035 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 4:63–64.

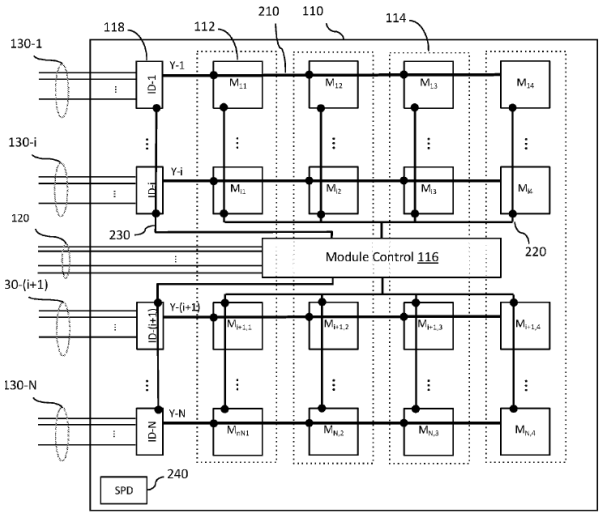

FIG. 2A

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As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:64–66, 6:1–5. Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:18–23. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, e.g., group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:28–30; *see id.* at 3:25–27, 6:14–17. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:14–17, 6:27–29. For example, as shown along the top of memory module 110, isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:19–22.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)." Ex. 1001, 3:28–30. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:27–32, 4:18–23, 4:64–67. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:60–63. And, "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:63–67.

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As can be seen in Figure 2A, and as the '035 patent explains, there are "unbalanced" lengths of control wires to respective memory devices which causes a "variation of the timing" of signals due to the variation in wire length. *See* Ex. 1001, 2:25–28; *see also id.* at 8:22–50. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "providing the correct control signal timing." *Id.* at 8:59–65. In particular, "isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation." *Id.* at 15:18–21. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to "properly time transmission" of a later read operation. *Id.* at 15:33–45.

D. Illustrative Claims

Claim 1, the sole independent claim of the '035 patent, is reproduced below with limitation identifiers in brackets corresponding to claim analysis headings in the Petition. *See* Pet. 17–38.

> 1. [a] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> [b] a module board having edge connections for coupling to respective signal lines in the memory bus;
>
> [c] a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and

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> [d] memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, [e] the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
>
> [f] a plurality of buffer circuits mounted on the module board in positions [g] corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, [h] the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and [i] logic configured to respond to the module control signals by enabling the data paths, [j] wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

Ex. 1001, 19:10–45.

E. Evidence

The Petition relies on the following references:

Reference	**Exhibit No.**
US 2010/0312925A1; filed June 3, 2010; published Dec. 9, 2010 ("Osanai").	1005
US 8,020,022B2; filed Sept. 12, 2008; issued Sept. 13, 2011 ("Tokuhiro").	1006
US 8,713,379B2; filed Nov. 22, 2011; issued Apr. 29, 2014 ("Takefman")	1007

In addition, Petitioner relies on the Declaration of Donald Alpert, Ph.D. (Ex. 1003) in support of its arguments. Patent Owner relies on the

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Declaration of Dr. Steven Przybylski (Ex. 2010). The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1, 2, 6, 10–13, 21, and 22 would have been unpatentable on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 2, 6, 10–13, 21, 22	103(a)[1]	Osanai, Tokuhiro
2	1, 2, 6, 12–13, 21	103(a)	Takefman, Tokuhiro
3	1, 2, 6, 12–13, 21	103(a)	Takefman, Tokuhiro, Osanai

Pet. 3–4.

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Because the '035 patent claims priority before this date, the pre-AIA version of § 103 applies.

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subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness.[2] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner's Declarant, Dr. Alpert, opines that:

> a person of ordinary skill in the art in the field of the Challenged Patent would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers . . . an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

Ex. 1003 ¶ 42; *see* Pet. 4–5.

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[2] Because neither party has introduced evidence or arguments regarding objective indicia of obviousness, this factor is moot and not addressed in our Decision.

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Patent Owner states that although it "disputes Petitioners' definition of the level of a person of ordinary skill in the art ('POSITA'), resolution of such dispute is not necessary for the Board to decide the validity of the challenged claims." PO Resp. 13.

We adopt Petitioner's proposed level of ordinary skill, except that we find that the phrase "at least" in Petitioner's proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine that a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and three years working in the field.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

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Petitioner proposes that we "use Patent Owner's proposed constructions" from the related proceedings. Pet. 10 (citing Ex. 1019). Patent Owner states that it does not seek construction of any terms in the '035 patent and "agrees with Petitioners that all terms of the '035 Patent have their plain and ordinary meaning." PO Resp. 13.

We determine no terms need to be construed to resolve the disputes between the parties.

D. Ground 1 – Obviousness over Osanai and Tokuhiro

Petitioner argues claims 1, 2, 6, 10–13, 21, and 22 of the '035 patent would have been obvious over Osanai and Tokuhiro. Pet. 17–48. Below we provide a brief overview of the prior art references and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Osanai (Ex. 1005)

Osanai relates to a memory module having memory chips and data register buffers arranged in a manner which shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is "a schematic diagram of a configuration of a memory module." *Id.* ¶ 20.

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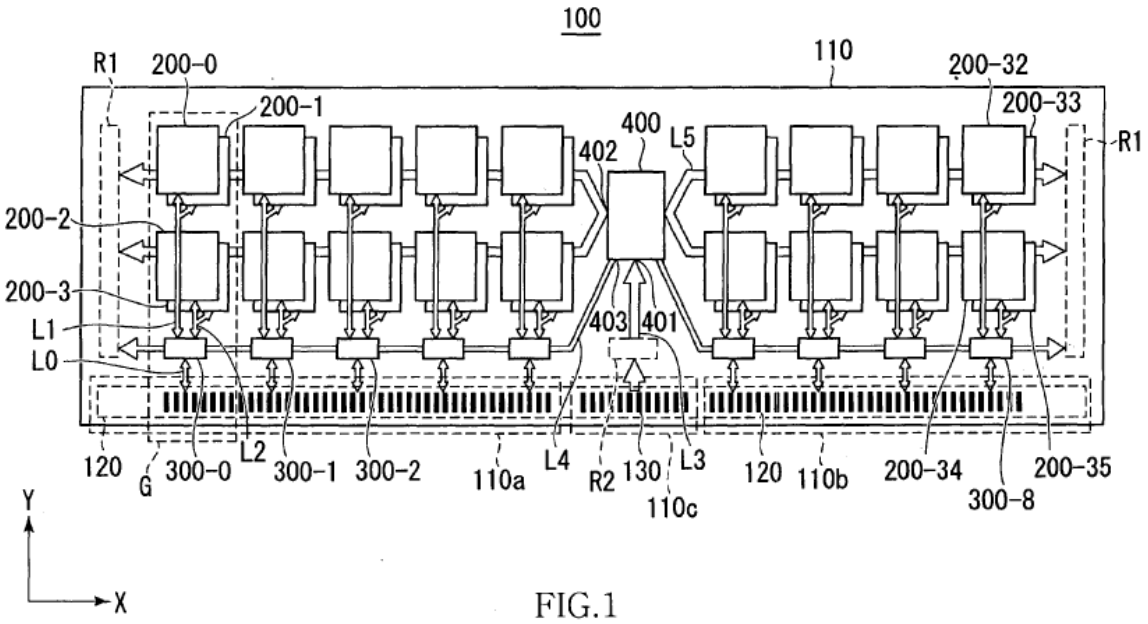

FIG.1

As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. Ex. 1005 ¶ 51. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 52. Still further, memory module 100 includes "data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" electrically connected to the connectors. *Id.* ¶¶ 53–54 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connectors 120 and the memory chips 200." *Id.* ¶ 109. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 26.

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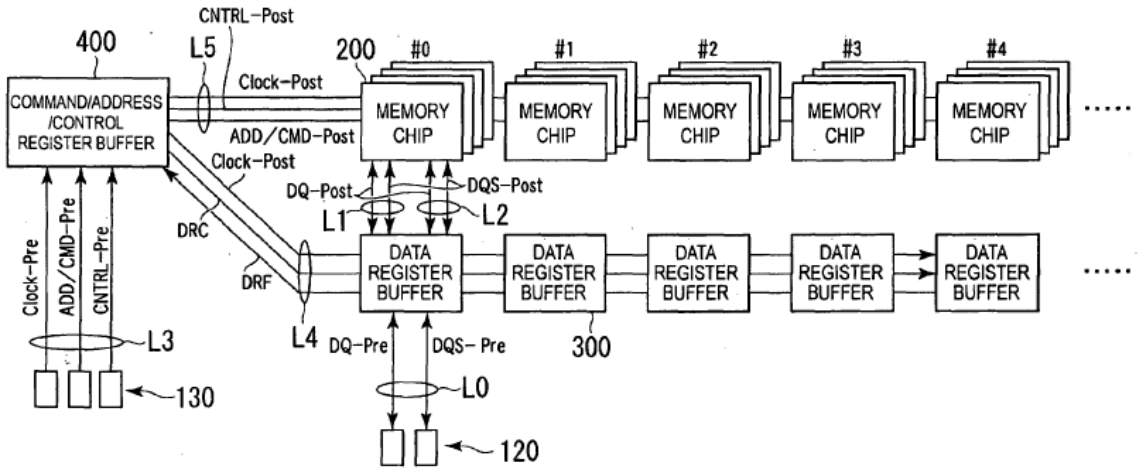

FIG.7

As shown in Figure 7, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 109. "[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post." *Id.* ¶ 110. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Osanai "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 146. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which is a block

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diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 89.

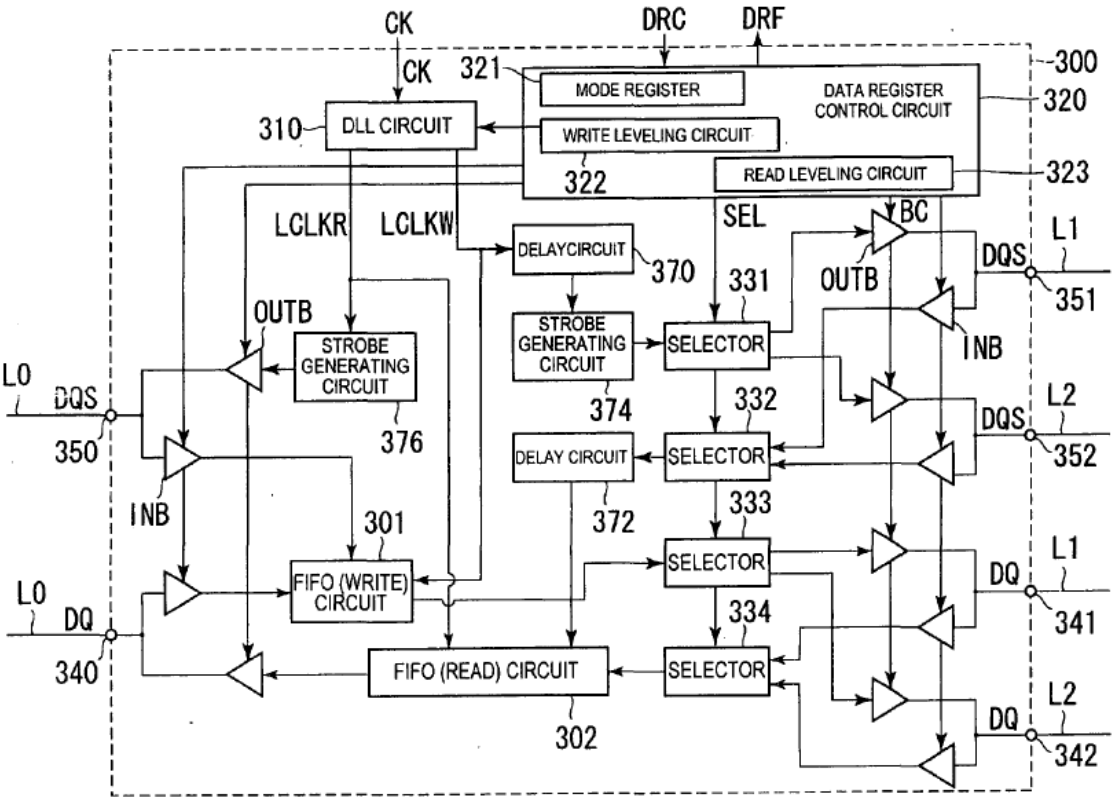

FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 151, 153. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a signal." *Id.* ¶ 146. For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 149. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 151.

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An exemplary read leveling operation also adjusts signal timing for a read operation. *See id.* ¶¶ 153–157. For example,

> read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 157.

2. *Tokuhiro (Ex. 1006)*

Tokuhiro relates to a memory control circuit having "a write leveling function and control[ing] read/write operations by supplying a clock signal to a plurality of memories." Ex. 1006, 3:16–20. Tokuhiro explains that, in memory interfaces, "a propagation delay is generated" because a "clock signal CK output from [a] memory controller 90 cannot reach all the [memory units] at the same time." *Id.* at 1:63–2:1. Tokuhiro further explains that delay is addressed through a write leveling function for "adjusting (compensating) a delay time" of "data strobe signal DQS." *Id.* at 2:10–18. The write level technique Tokuhiro describes "delaying, in [a] write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time." *Id.* at 3:16–26.

In one example, "during the write operation, [a] first variable delay circuit DW delays the data strobe signal DQS output to the SDRAM by the first delay time Dt1 that has been set based on the write leveling function."

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Ex. 1006, 14:66–15:2. Tokuhiro explains that a "delay time . . . calculated is provided as Delay (R)n. In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling." *Id.* at 16:19–23; *see id.* 16:1–18.

3. Analysis of Claim 1

a) Summary of Petitioner's Contentions

Petitioner provides detailed analysis arguing that Osanai teaches the preamble and limitations 1[b]–1[j]. Pet. 17–33. Petitioner supports its arguments with citations to Osanai and to the testimony of Dr. Alpert. *Id.* Patent Owner does not separately dispute Petitioner's contentions regarding any of these limitations except limitation 1[j]. *See generally* PO Resp. We summarize Petitioner's contentions for claim 1 below.

The preamble recites: "[a] memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines." Ex. 1001, 19:10–14. Petitioner identifies Osanai's memory module 100 as the recited "memory module," memory control hub 12 as the recited "memory controller," lines L0, L3 and 23, as the recited "memory bus," and lines L0, L3 along with data connectors 120 and command/address/control connectors 130 as the recited "signal lines." Pet. 17–21 (citing Ex. 1005 ¶¶ 54–55, 69–71, 75, 126, Figs. 1, 2; Ex. 1003 ¶¶ 73–80).

Limitation 1[b] recites "a module board having edge connections for coupling to respective signal lines in the memory bus." Ex. 1001, 19:15–16. Petitioner identifies data connectors 120 and 130, which Petitioner argues

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are located on the edge and connect the signal lines L0 and L3, as the claimed "edge connections for coupling to respective signal lines in the memory bus." Pet. 21–22 (citing Ex. 1003 ¶ 82; Ex. 1005 ¶ 54, Fig. 1).

Limitation 1[c] recites "a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals." Ex. 1001, 19:17–22. Petitioner identifies Osanai's command/address/control register buffer 400 as the claimed "module control device." Pet. 22–23 (citing Ex. 1005, ¶¶ 66, 101–103, Figs. 1, 6). Petitioner identifies memory controller 12 as the claimed "memory controller" and identifies the command/address/control signals that memory controller 12 sends to register buffer 400 as the recited "memory command signals." *Id.* at 23 (citing Ex. 1005 ¶¶ 53, 102; Ex. 1003 ¶ 86). In response to receiving the command/address/control signals, the register buffer 400 outputs address (ADD), command (CMD), clock (CLK) signals, which Petitioner identifies as the recited "module command signals" and also outputs control signals (CTRL), which Petitioner identifies as the recited "module control signal." *Id.* (citing Ex. 1005 ¶¶ 103, Fig. 6; Ex. 1003 ¶ 86). Petitioner additionally argues that register buffer 400 outputs DRC signals and CK signals, which Petitioner also identifies as the recited module control and module command signals. *Id.* (citing Ex. 1005 ¶¶ 66, 78–84, 93, 103, 105, 106, 132; Ex. 1003 ¶ 86). Petitioner relies on Dr. Alpert's testimony that explains that these signals are the recited "module control" and "command signals" for the first memory operation (read operation). *Id.* at 23–24 (citing Ex. 1003 ¶ 87).

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Limitation 1[d] recites "memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals." Ex. 1001, 19:23–25. Petitioner identifies memory chips 200 mounted on memory module 100 as the recited "memory devices mounted on the module board." Pet. 24 (citing Ex. 1005, Fig. 1; Ex. 1003 ¶ 90). Petitioner argues that memory chips 200 perform memory operations including read and write operations and thus "perform the first memory operation" as recited. *Id.* at 25 (citing Ex. 1005 ¶ 60, 90, 128–142; Ex. 1003 ¶ 90).

Limitation 1[e] recites "the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines." Ex. 1001, 19:25–28. Petitioner argues that Osanai's memory chips 200 are grouped into sets making "a plurality of sets of memory devices," as recited in claim 1. Pet. 25 (Ex. 1005 ¶ 58). Petitioner identifies lines L0 as the recited "plurality of sets of data/strobe signal lines" and argues that each group of memory devices has its own respective set of data/strobe L0 signal lines. *Id.* at 25–26 (citing Ex. 1005 ¶ 109, Figs. 5, 7; Ex. 1003 ¶ 94).

Limitation 1[f] recites "a plurality of buffer circuits mounted on the module board in positions." Ex. 1001, 19:20–21. Petitioner identifies Osanai's register buffers 300 mounted in memory module 100 as the recited "plurality of buffer circuits mounted on the module board in positions." Pet. 26–27 (citing Ex. 1005 ¶¶ 52, 61–62, 109, Fig. 1; Ex. 1003 ¶¶ 97–98). Petitioner argues that each data register buffer 300 is paired with a set of memory chips. *Id.* at 27 (citing Ex. 1005, ¶¶ 61–62, 109, Fig. 7; Ex. 1003 ¶ 98).

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Limitation 1[g] recites "[a plurality of buffer circuits] corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices." Ex. 1001, 19:30–35. Petitioner argues that each data register buffer 300 is located between L0 data lines (the data/strobe signal lines) and its respective memory chip group. *Id.* at 28 (citing Ex. 1005 ¶¶ 57–58, 109, Fig. 7; Ex. 1003 ¶ 102). Petitioner cites Osanai which describes that "the data register buffer 300 and [each group of] memory chips 200 are connected to each other with the data line L1 or L2" and argues that Lines L1 and L2 are coupled to the memory bus via their data buffer and respective connector for the L0 data lines. *Id.* at 29 (citing Ex. 1005 ¶ 109; Ex. 1003 ¶ 102). According to Petitioner, the memory chips are organized into groups, thereby teaching the recited "respective set of memory devices." *Id.* at 28–29 (citing Ex. 1005 ¶¶ 57–58; Ex. 1003 ¶ 102).

Limitation 1[h] recites "the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation." Ex. 1001, 19:35–37. Petitioner argues that each data register buffer 300 has data paths L1 and L2 connected to each memory chip group and that a person of ordinary skill would have understood these data paths include circuitry components in the data register buffer. Pet. 29–30 (citing Ex. 1005, ¶ 109, Figs. 1, 7; Ex. 1003 ¶ 105). The data paths through the circuitry of data register buffer 300 take in DQ-Pre and DQS-Pre signals and transmit DQ-Post and DQS-Post signals, which Petitioner argues are the recited "data and strobe signals" which are associated with memory operations. *Id.* at 29–31 (citing Ex. 1003 ¶¶ 105– 108; Ex. 1005 ¶¶ 60, 90, 97, 109–110, Figs. 1, 5, 7).

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Limitation 1[i] recites "logic configured to respond to the module control signals by enabling the data paths." Ex. 1001, 19:38–39. Petitioner argues that Osanai's data register control circuit 320 teaches the claimed "logic" and that this control circuit 320 enables different data paths for reading and writing operations depending on the DRC. Pet. 31–32 (citing Ex. 1005 ¶¶ 94, 96, 105, 106, 158, 163, Fig. 5; Ex. 1003 ¶ 111). Petitioner relies on Dr. Alpert's testimony explaining that a person of ordinary skill would have understood that data register control circuit 320 selects certain paths using SEL, INB, and OUTB signals, as well as selectors 331–334, and that this would have taught "logic configured to respond to the module control signals by enabling the data paths." *Id.* at 32–33 (citing Ex. 1003 ¶ 111).

Limitation 1[j] recites "wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information." Ex. 1001, 19:39–45. Petitioner argues that the combination of Osanai and Tokuhiro teaches this limitation. Pet. 33–38 (citing Ex. 1003 ¶¶ 117–122; Ex. 1005 ¶¶ 96, 110, 115–116, 146–164, Figs. 5, 7, 14A–17; Ex. 1006, 1:63–2:9, 2:46–49, 3:9–12, 3:16–26, 4:7–17, 16:1–28, claim 2). Petitioner acknowledges that while Osanai discloses the claimed "logic" it does not expressly disclose that the timing information is obtained during a second memory operation prior to the first memory operation. *Id.* at 33–34. Petitioner, therefore, relies on Tokuhiro for teaching this limitation, arguing that it would have been obvious to incorporate Tokuhiro's technique in Osanai's logic. *Id.* at 34.

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Specifically, Petitioner argues that Osanai discloses both read and write leveling techniques that make timing adjustments by using the module clock signal so that signals between the memory chips 200 and the data register buffer 300 are sent at the appropriate time. Pet. 34–36 (citing Ex. 1005 ¶ 96, 110, 115–116, 146–164, Figs. 5, 7; Ex. 1003 ¶¶ 115–118). According to Petitioner, a timing adjustment, such as a time delay based on the module clock signal, is used to create DQ-Post and DQS-Post and adjust write timing or read timing. *Id*. at 35. (citing Ex. 1005 ¶¶ 110, 149–157; Ex. 1003 ¶ 117). Thus, Petitioner argues Osanai discloses "obtaining timing information" based on a module clock signal received by each respective buffer circuit. *Id.* at 36 (citing Ex. 1003 ¶ 118).

Petitioner acknowledges, however, that Osanai does not explicitly disclose that the timing information is obtained "during a second memory operation prior to the first memory operation" as recited in limitation 1[j]. Petitioner turns to Tokuhiro to address this deficiency. Pet. 36. Petitioner argues that Tokuhiro also discloses read and write leveling techniques just as Osanai does and that Tokuhiro calculates a second delay time for the read operation based on the first delay time determined by the write level operation. *Id.* at 36–37 (citing Ex. 1006, 16:1–28). Consequently, Petitioner argues Tokuhiro teaches a delay unit that obtains a first delay time during a write leveling operation ("second memory operation") to use in its calculation of a second delay time ("obtaining timing information") used for a read operation ("first memory operation"). *Id.* at 37 (citing Ex. 1006, 3:16– 26, 16:1–28; Ex. 1003 ¶ 121); Pet. Reply 2.

Petitioner proposes to incorporate Tokuhiro's leveling technique of calculating a second delay time for read operations based on a first delay time determined by the write leveling operation with Osanai's system.

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Pet. 34–41. Petitioner argues that one of ordinary skill would have been motivated to use Tokuhiro's technique in Osanai's buffer leveling circuits for three reasons. The first is to reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling. Pet. 39 (citing Ex. 1003 ¶ 126). The second is to reduce power consumption and reduce circuit area, thereby reducing costs by increasing manufacturing yield. *Id.* at 40 (citing Ex. 1006, 24:26–29, 21:15–24:42, Figs. 16–17; Ex. 1003 ¶ 127). The third reason to combine Tokuhiro with Osanai is to improve signal fidelity, decrease timing skew among components and lower the load perceived by the memory controller. *Id.* at 40–41 (citing Ex. 1005 ¶¶ 4, 5, 75–76, 117–119, 176, 194; Ex. 1006, 1:63–2:28, 3:1–13; 3:16–26, 19:8–13, 19:25–33; Ex. 1003 ¶ 128).

b) Summary of Patent Owner's Arguments

Patent Owner makes several arguments. Nearly all of these arguments center around limitation 1[j] including whether the combination of Osanai and Tokuhiro teaches limitation 1[j] and whether a person of ordinary skill would have combined Osanai and Tokuhiro in the manner proposed by Petitioner. PO Resp. 13–45.

For example, Patent Owner argues that Tokuhiro's write leveling function does not teach the recited "second memory operation" because during Tokuhiro's write leveling function, no memory operations can be performed at all. PO Resp. 13–29.

Patent Owner further argues that Petitioners have not identified where Osanai teaches control of timing (1) of respective data and strobe signals (2) on the data paths (3) in accordance with the timing information as claim 1 requires. PO Resp. 31–33.

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Patent Owner raises several issues with the combination of Osanai and Tokuhiro that it alleges arise from "inherent inconsistencies" (PO Resp. 41) and incompatibilities between the two references. *Id.* at 35–42. For example, Patent Owner argues that "a POSITA would not have looked to Tokuhiro—which teaches improvements to an off-module memory controller—to improve functionality of Osanai's on-module components." *Id.* at 35. Patent Owner further argues that Tokuhiro is directed to solving a problem that does not exist in Osanai. *Id.* at 38. Tokuhiro centers on determining the delay for read data passing through variable delay circuits DR1 and DR2 which are not present in Osanai. *Id.* 38–39 (citing Ex. 1005 ¶¶ 90, 93, Fig. 5; Ex. 2010 ¶ 121).

Finally, Patent Owner argues that a person of ordinary skill would not have been motivated to combine Osanai and Tokuhiro. PO Resp. 42–45. Patent Owner argues that Petitioner is incorrect in contending that the combination of Osanai and Tokuhiro would reduce the number of steps needed to determine the read delay. *Id.* at 43. Patent Owner further argues that Petitioner is wrong in contending that incorporating Tokuhiro's write leveling technique into Osanai's module would reduce power consumption and circuit area. *Id.* at 43–45. Patent Owner finally argues that Petitioner has not shown that the combination would improve signal fidelity, decrease timing skew or lower the load on the memory controller. *Id.* at 45.

We analyze Petitioner's contentions in light of each one of these arguments, in turn, below.

c) Analysis

As explained above, nearly all the disputes and arguments between the parties center around limitation 1[j]. These disputes raise several issues

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which we analyze, in turn, below. Before doing so, however, we analyze Petitioner's contentions regarding the preamble and limitations 1[b]–1[i] which Patent Owner does not separately dispute.

As summarized above, Petitioner has provided a detailed analysis of each of these limitations with support from the disclosures of Osanai, Tokuhiro, and from the credible testimony of Dr. Alpert. We agree with and adopt Petitioner's contentions for the preamble[3] and limitations 1[b]–1[j].

For example, Osanai discloses a memory module 100 and a memory control hub 12 which we agree teach the "memory module" and "memory controller" recited in the preamble. Pet. 17–21 (citing Ex. 1005 ¶¶ 54–55, 69–71, 75, 126, Figs. 1, 2; Ex. 1003 ¶¶ 73–80). Osanai discloses that memory module 100 and memory control hub 12 are connected and that memory control hub 12 "functions as a memory controller for the memory module 100." Ex. 1005 ¶ 71. Dr. Alpert provides credible testimony that module 100 and a memory control hub 12 communicate using communication line 23, data lines L0 and command/address/control line L3 and that these three would be understood collectively to teach the recited "memory bus." Ex. 1003 ¶¶ 75–87 (citing Ex. 1005 ¶¶ 54–55, 75, 126, Figs. 1, 3).

Figure 1 of Osanai also depicts data connectors 120 and 130 which we agree would have taught one of skill the recited "edge connections" of limitation 1[b]. Dr. Alpert provides credible testimony that "POSITA would have recognized that these connectors are located at the edge of module 110

[3] Neither party argues that the preamble is limiting. Because we find that the evidence supports that Osanai teaches the preamble, we make no determination whether the preamble of claim 1 is limiting.

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and connect L0 and L3 lines to line 23 of the memory bus so they satisfy the claimed '*edge connections.*'" Ex. 1003 ¶ 82 (citing Ex. 1005 ¶ 54, Fig. 1).

Figure 1 of Osanai shows a command/address/control register buffer 400 mounted on memory module 100. We agree with Petitioner that this register buffer 400 teaches the "module control device mounted on the module board" recited in limitation 1[c]. Osanai discloses that register buffer 400 receives various signals, such as command signals, address signals, control signals, and clock signals. Ex. 1005 ¶ 66. Dr. Alpert provides credible testimony that these various signals teach the recited "memory command signals." Ex. 1003 ¶ 86. Osanai also discloses that register buffer 400 outputs address (ADD), command (CMD), clock (CK) and DRC signals. Ex. 1005 ¶ Fig. 6. Dr. Alpert provides credible testimony that these signals teach the recited "module command" and "module control" signals of limitation 1[c]. Ex. 1003 ¶¶ 86, 87.

Figure 1 of Osanai discloses multiple memory chips 200 mounted on memory module 100. We agree with Petitioner that these memory chips disclose the recited "memory devices mounted on the module board" of limitation 1[d]. Dr. Alpert provides credible testimony that these memory chips 200 perform memory operations including read and write operations. Ex. 1003 ¶¶ 90–91 (citing Ex. 1005 ¶¶ 60, 90, 128–142).

Osanai discloses that its memory chips are grouped and belong to different ranks. Ex. 1005 ¶ 58 ("In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other."). Dr. Alpert provides credible testimony that each group has its own

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respective set of data/strobe signal lines, L0 data lines and that this teaches the "memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines" recited in limitation 1[e]. Ex. 1003 ¶¶ 92–95 (citing Ex. 1005 ¶ 109, Fig. 7).

Figure 1 of Osanai discloses data register buffers 300 that are mounted in positions on the memory module 100. We agree with Petitioner that Osanai's data register buffers 300 teach the "plurality of buffer circuits mounted on the module board" recited in limitation 1[f]. Additionally, Dr. Alpert credibly testifies that, as shown in Figure 7 of Osanai, each data register buffer 300 is located between L0 data lines and its respective memory chip group and that data register buffer 300 and memory chips 200 are connected to each other with data lines L1 or L2. Ex. 1003 ¶¶ 101–102 (citing Ex. 1005 ¶¶ 57–58, 109, Fig. 7). Dr. Alpert testifies that these disclosures teach a plurality of buffer circuits "coupled between a respective set of data/strobe signal lines and a respective set of memory devices" as recited in limitation 1[g]. Ex. 1003 ¶¶ 100–103.

With respect to limitation 1[h], Dr. Alpert credibly testifies that "Figure 7 shows that each data register buffer 300 has '*data paths*' L1 and L2 connected to each memory chip group" and that these data paths include circuitry components in the data register buffer shown in Figure 5 of Osanai. Ex. 1003 ¶¶ 105–106 (citing Ex. 1005 ¶ 109, Figs. 1, 7). Dr. Alpert provides credible testimony that data register buffer 300 transmits data and strobe signals using these data paths. *Id.* ¶ 107 (citing Ex. 1005 ¶ 109). Specifically, Dr. Alpert asserts that data register buffer 300 receives the DQS-Pre and DQ-Pre signals on line L0 and transmits the DQS-Post and DQ-Post signals over lines L1 and L2 and that the DQ-Post and DQS-Post

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signals teach the recited "data and strobe signals" that are associated with "memory operations." *Id.* ¶¶ 107–108.

Figure 5 of Osanai illustrates a data register buffer 300 that includes a data register control circuit 320 which further includes read leveling and write leveling circuits 323 and 322. We agree with Petitioner that these circuits teach the recited "logic configured to respond to the module control signals by enabling data paths" recited in limitation 1[i]. Dr. Alpert provides credible testimony that "data register control circuit 320 selects (or '*enables*') certain paths using SEL, INB, and OUTB signals, as well as selectors 331–334, which supplies data DQ to input or output terminals, 341 and 342, to certain memory chips 200." Ex. 1003 ¶ 111 (citing Ex. 1005 ¶¶ 94, 97, Figs. 1, 5, 7).

Finally, with respect to limitation 1[j], we agree that the combination of Osanai and Tokuhiro teach the recited "wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information." Dr. Alpert provides credible testimony that Osanai discloses both read and write leveling techniques that make timing adjustments by using the module clock signal so that signals between the memory chips 200 and the data register buffer 300 are sent at the appropriate time. Ex. 1003 ¶ 115 (citing Ex. 1005 ¶¶ 96, 110, 146–164). Dr. Alpert further testifies that a timing adjustment, such as a time delay based on the module clock signal, is used to create DQ-Post and DQS-Post and adjust write timing or read timing. *Id.* ¶ 117 (citing Ex. 1005 ¶¶ 110, 149–157). Dr. Alpert explains that "Osanai does not, however, explicitly disclose that

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the timing information is obtained '*during a second memory operation prior to the first memory operation*,'" but that this limitation would have been obvious based on the teaching of Tokuhiro. *Id.* ¶ 119. Dr. Alpert credibly testifies that Tokuhiro also discloses read and write leveling techniques to compensate for different propagation delays and that Tokuhiro calculates a second delay time for the read operation based on the first delay time determined by the write level operation. *Id.* ¶¶ 120–121 (citing Ex. 1006, 2:46–49, 3:9–12, 16:1–28). Dr. Alpert therefore testifies that Tokuhiro teaches a delay unit that obtains a first delay time determined during a write leveling operation to use in its calculation of a second delay time ("obtaining timing information") used for a read operation. *Id.* ¶¶ 121–123 (citing Ex. 1006, 3:16–26).

Dr. Alpert provides credible testimony that one of ordinary skill would have been motivated to use Tokuhiro's technique in Osanai's buffer leveling circuits for three reasons. The first is to reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling. Ex. 1003 ¶ 126. The second is to reduce power consumption and reduce circuit area, thereby reducing costs by increasing manufacturing yield. *Id.* ¶ 127 (citing Ex. 1006, 24:26–29, 21:15–24:42, Figs. 16–17). The third reason to combine Tokuhiro with Osanai is to improve signal fidelity, decrease timing skew among components and lower the load perceived by the memory controller. Ex. 1003 ¶ 128 (citing Ex. 1005 ¶¶ 4, 5, 75–76, 117–119, 176, 194; Ex. 1006, 1:63–2:28, 3:1–13; 3:16–26, 19:8–13, 19:25–33).

For the aforementioned reasons, we agree with Petitioner that the combination of Osanai and Tokuhiro teaches the preamble and limitations 1[b]–1[j] of claim 1 even in light of Patent Owner's arguments. As we

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explained above, the arguments raised by Patent Owner relate to limitation 1[j] and to the motivation to combine Osanai and Tokuhiro. Below, we address Patent Owner's arguments and the issues raised by those arguments.

(1) Whether Write Leveling Teaches the Recited "Second Memory Operation"

Patent Owner argues that Tokuhiro does not disclose "obtain[ing] timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation." PO Resp. 13–29. Specifically, Patent Owner argues that Tokuhiro does not obtain timing information during a second memory operation because during Tokuhiro's write leveling function, no memory operations can be performed at all. *Id.* at 13.

Patent Owner argues that Tokuhiro uses a known write leveling mechanism described in the Joint Electron Device Engineering Counsel (JEDEC) DDR3 standard and does not purport to teach improvements to this known JEDEC write leveling mechanism. *Id.* at 17–20 (citing Ex. 1006, 1:22–26, 2:10–45). According to Patent Owner, during the write leveling mode described in the JEDEC DDR3 standard, the memory module is prohibited from performing any memory operations at the direction of the memory controller, or otherwise. *Id.* at 21–22 (citing Ex. 2003 at 38–41; Ex. 2004 at 39, 41, Fig. 14). Patent Owner explains that during the write leveling process the only operations that occur are NOP (No Operation) and DESELECT commands, which according to Patent Owner do not instruct the memory to do anything at all. *Id.* at 22–24 (citing Ex. 2014, 29–30, 32, Fig. 15; Ex. 2010 ¶¶ 78, 176). None of the commands that are issued during write leveling mode are "memory operations" under a plain and ordinary meaning of the term, argues Patent Owner. *Id.* at 24 (citing Ex. 2010 ¶ 77).

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Only after the write leveling mode ends can any memory operations resume. *Id.* at 25 (citing Ex. 2004, Fig. 16; Ex. 2010 ¶ 80).

Patent Owner further argues that the JEDEC standard's "Simplified State Diagram" confirms that no memory operations are performed during write leveling. PO Resp. 25 (citing Ex. 2014, Fig. 1; Ex. 2010 ¶ 81). Patent Owner argues that the state diagram shows that write leveling can only be entered from an idle state and that after exiting write leveling mode the device returns to an idle state. *Id.* Memory read and write operations, in contrast, can only be performed once the memory device enters an active state, according to Patent Owner. *Id.* at 25–26.

Patent Owner also emphasizes that the terms "write leveling" and "write operation" are not synonymous and that the write leveling procedure taught in Tokuhiro is not a write operation. PO Resp. 27 (citing Ex. 2011, 118:7–13, 150:17–21). Moreover, Patent Owner argues that not only are no memory operations allowed during Tokuhiro's write leveling procedure, but Tokuhiro's write leveling procedure itself is not a memory operation under a plain and ordinary meaning of the term. *Id.* at 28 (citing Ex. 2010 ¶ 86).

Thus, Patent Owner concludes, any timing information determined during Tokuhiro's write leveling is not obtained during a "second memory operation" as that term is used in the claims. PO Resp. 28.

Petitioner, in its Reply Brief, argues that "the evidence confirms that a 'write leveling operation' is a '*memory operation*.'" Pet. Reply 2. As support, Petitioner asserts that "[t]he '035 patent describes that '*memory operations*' include other memory operations beyond write and read operations" and that "the '035 patent describes that the claimed '*memory operations*' encompass various operations performed by memory in response to memory commands." *Id.* at 2 (citing Ex. 1001, 3:27–32).

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Petitioner emphasizes that Osanai's write leveling operation is triggered by a memory command, namely a Mode Register Set (MRS) command. *Id.* at 2–3 (citing Ex. 1005 ¶¶ 146–147; Ex. 2013, 13).

Petitioner also points out that the JEDEC standard, which Patent Owner relies on, "includes 'write leveling' in the subsection titled 'DDR3 SDRAM [i.e., Memory] Command Description and Operation'" and that the same exhibit confirms that Mode Register Set is a memory command included in a table that includes other undisputed memory commands, such as read, write, refresh, and precharge. Pet. Reply 3 (Ex. 2013, 12; Ex. 1022, 16:22–17:4).

Petitioner responds to Patent Owner's argument that write leveling is not a memory operation because only NOP and DESELECT commands are issued during the write leveling process by pointing out that even "regular read and write operations also use the same NOP and Deselect commands." Pet. Reply 4 (citing Ex. 1022, 57:16–58:4). Petitioner argues that NOP and Deselect commands do not affect memory operations already in progress such as a write leveling operation that use these commands. *Id.* (citing Ex. 2013, 11). Furthermore, Petitioner argues that MRS commands used to trigger the write leveling operation, write to mode registers located in the memory device, and thus, affect the memory itself. *Id.* at 5 (citing Ex. 2013, 12; Ex. 1022, 36:5–11, 32:12–16).

In its Sur-Reply, Patent Owner emphasizes that Petitioner does not dispute that "that Tokuhiro teaches a method of write leveling that was identified as prior art by the '035 Patent's specification," or that "during the write leveling procedure . . . only NOP or DESELECT command placeholders are allowed." PO Sur-reply, 1–2. Patent Owner also argues that the write leveling procedure cannot be equated to other operations or

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commands simply because it is listed in the same table or in the same section as these other operations and commands in the JEDEC standard. *Id*. at 3.

As can be seen from Petitioner's contentions and Patent Owner's arguments summarized above, a central dispute between the parties is whether Tokuhiro's write leveling function teaches the claimed "second memory operation." Having reviewed the evidence, we are persuaded by Petitioner's arguments that Tokuhiro's write leveling function teaches the "second memory operation." Petitioner's arguments are supported by disclosures from Tokuhiro and by Dr. Alpert's testimony.

We agree with Petitioner that the '035 Patent describes memory operations fairly broadly, stating that "[t]he memory module is operable to perform memory operations in response to memory commands (e.g. read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module." Ex. 1001, 3:27–32. As Petitioner argues, memory operations are described with an open-ended list of operations that go beyond simply read and write operations, and describes those operations as being performed by memory in response to memory commands from the memory controller. Petitioner shows that the write leveling operation is performed in response to a memory command such as the Mode Register Set (MRS) command and that memory devices receive this command to perform write leveling. Pet. Reply 3 (citing Ex. 1005 ¶¶ 146–147; Ex. 2013, 13).[4]

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[4] We note that Tokuhiro's description of its write leveling operation also supports Petitioner's argument that the write leveling operation is performed by its memory devices. *See* Ex. 1006, Fig. 7, 13:23–65 (explaining that during write leveling the memory devices (SDRAM) receive clock signals (CK) and data strobe signals (DQS) from the memory controller and output

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This demonstrates that a write leveling operation is performed by the memory devices in response to memory commands, consistent with the '035 patent's description of memory operations.

As mentioned above, Patent Owner argues that during the write leveling mode described in the JEDEC DDR3 standard, the memory module is prohibited from performing any memory operations and that during the write leveling process only NOP and DESELECT commands are issued, both of which do not instruct the memory to do anything. PO Resp. 20–25. This argument—that no *other* memory operations occur during write leveling—does not address whether the write leveling process itself is a memory operation. Petitioner demonstrates, supported by the JEDEC standard and by the deposition testimony of Dr. Przybylski, that read and write operations, which are both undisputedly memory operations, also include NOP commands. Pet. Reply 4 (citing Ex. 2013, 10; Ex. 1022, 57:16–58:4). Thus, the presence of NOP commands cannot, by itself, show that write leveling is not a memory operation. Furthermore, the JEDEC standard explains that although a NOP command "prevents unwanted commands" during idle or wait states "[o]perations already in progress are not affected." Thus, even though write leveling includes NOP commands, this does not prevent the write leveling operation itself from occurring.

Patent Owner does argue that write leveling is itself not a memory operation. *See* PO Resp. 28 ("The Board's Institution Decision asks whether Tokuhiro's write leveling procedure nevertheless teaches the recited '*second memory operation*' even though other memory operations are prohibited

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data signals (DQ) back to the controller, in order to measure timing and adjust delay times.

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from being performed during the procedure. Paper 16, 26. As described above, under the plain and ordinary meaning of the claim language as understood by a POSITA, the answer is clearly 'no.'"). But Patent Owner's argument is largely conclusory and only refers back to arguments showing that no *other* memory operations are performed during write leveling, rather than showing that write leveling itself is not a memory operation.

Patent Owner argues that the JEDEC standard's "Simplified State Diagram" also shows that write leveling is not a memory operation. PO Resp. 25–26 (citing Ex. 2014, Fig. 1, Ex. 2010 ¶ 81). We disagree. As Petitioner emphasizes, memory operations such as "refresh" and "precharge" are also depicted in the state diagram as occurring from idle state, just as is write leveling. Pet. Reply 5–6 (citing Ex. 1001, 3:27–32; Ex. 1022, 50:21–51:4). Furthermore, simply distinguishing write leveling from read or write operations does not sufficiently show that write leveling is not a memory operation since the '035 patent itself describes memory operations as broader than simply read and write operations.[5]

For the aforementioned reasons, we determine that Tokuhiro's write leveling function would have taught one of ordinary skill the "second memory operation" recited in claim 1.

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[5] Additionally, claim 2, which depends from claim 1, requires that the first and second memory operations be "memory read" and "memory write" operations, respectively. Ex. 1001, 19:46–48. Under the doctrine of claim differentiation, claim 1's recitation of "memory operation" is presumed to refer to operations broader than merely read and write operations. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 911 (Fed. Cir. 2004) ("[T]he presence of a dependent claim that adds a particular limitation raises a presumption that the limitation in question is not found in the independent claim.").

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(2) Control of Timing of Data and Strobe Signals on Data Paths

Patent Owner argues that Petitioners do not identify where Osanai teaches control of timing (1) of respective data and strobe signals (2) on the data paths (3) in accordance with the timing information, which Patent Owner argues is required by limitation 1[j]. PO Resp. 31–33. Patent Owner argues that Petitioner addresses this limitation only in a heading. *Id*. 30–31. Specifically, Patent Owner argues that Petitioner does not show that Osanai teaches that read leveling is used to control the timing of the respective data and strobe signals associated with a read operation on data paths L1 and L2. *Id*. at 31. Similarly, Patent Owner argues that Dr. Alpert also does not show where Osanai teaches control of timing of respective data and strobe signals on the data paths in accordance with the timing information. *Id.* at 32.

Moreover, Patent Owner argues Petitioner could not have argued that Osanai teaches this claim limitation because Osanai's read leveling process delays the internal signals that turn on Osanai's input buffers INB rather than controlling the timing of the read data and strobe signals themselves. *Id*. at 33–34 (citing Ex. 1005 ¶ 157; Ex. 2010 ¶ 105). Additionally, Patent Owner argues that the paths on which the INB input buffer controls signals are not "data paths" on which data and strobe signals associated with a read operation are transmitted. *Id.* at 35 (citing Ex. 2010 ¶ 107; Ex. 2011, 98:21–99:1).

Having reviewed the record in light of the parties' arguments, we determine that Petitioner has sufficiently demonstrated that the combination of Osanai and Tokuhiro teaches the control of timing of respective data and strobe signals on the data paths in accordance with the timing information obtained during a second memory operation, as we explain below.

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For limitation 1[h] we explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. *See* § II.D.3.c; Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110, Figs. 1, 5, 7). These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300. Pet. 30–31. Furthermore, we explained with respect to limitation 1[i] that Petitioner had demonstrated that Osanai's data register control circuit 320, which includes its read leveling and write leveling circuits 322 and 323, teaches the recited "logic . . . configured to respond to the module control signals by enabling the data paths." *See* § II.D.3.c; Pet. 31–33 (citing Ex. 1005 ¶¶ 94, 96, 105, 106, 158, 163, Fig. 5; Ex. 1003 ¶ 111). In its contentions for limitation 1[j] Petitioner explains that the read and write leveling circuits of Osanai make timing adjustments so that signals between the memory chips and the data register buffer are sent at the appropriate time. Pet. 34 (citing Ex. 1005 ¶¶ 110, 146). It is readily apparent from Petitioner's contentions that the signals referenced here in limitation 1[j], to which timing adjustments are made, are data and strobe signals associated with read and write operations referenced in Petitioner's contentions with respect to limitation 1[h], and thus the recited "memory operation." We therefore disagree with Patent Owner's argument that Petitioner has not identified where Osanai teaches the control of timing limitation.

Moreover, we disagree with Patent Owner's argument that Osanai's read leveling process, which delays the internal signals that turn on Osanai's input buffers INB, does not control the timing of the data and strobe signals. Osanai explains that in read leveling, the timing of read data output from the memory chips and the input timing of the read command is measured for

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each memory chip and "used in an adjustment of an activation timing of the input buffer circuit INB and the like." Ex. 1005 ¶ 157. But, as Petitioner points out, Osanai does so "in consideration of a propagation time of a signal." Ex. 1005 ¶ 146. Petitioner further indicates that Dr. Przbylski testified that the input buffers (INB) act as a gate allowing data and strobe signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of Osanai are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.

Patent Owner argues that any explanation provided by Petitioner related to Osanai's INB buffers and how they relate to accounting of delays due to propagation time of signals is a new and untimely theory. PO Sur-reply 6–8. Petitioner, however, explained in its Petition that Osanai's read and write leveling circuits make timing adjustments so that signals between the memory chips and the data register buffer are sent at the appropriate time. Pet. 34 (citing Ex. 1005 ¶¶ 96, 110, 146–164). It was Patent Owner who responded to Petitioner's contention by raising issues related to Osanai's input buffers INB. *See* PO Resp. 33–35. Petitioner responded to these issues by explaining how, even when considering the input buffers' role in accounting for the propagation delays, Osanai would have taught, to a person of ordinary skill, control of timing of the data and strobe signals associated with the read operation. Pet. Reply 7–10. Other than citing to Dr. Przbylski's deposition testimony, Petitioner does not rely on any new evidence or previously unidentified portions of Osanai in providing its explanation. Such arguments do not exceed the proper bounds of a responsive argument in a reply. *See Apple, Inc. v. Andrea Elec. Corp.*, 949 F.3d 697, 706–707 (Fed. Cir. 2020) (determining that responsive arguments

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in Apple's reply brief did not exceed the scope of a proper reply because "Apple's reply does not cite any new evidence or 'unidentified portions' of the . . . reference"); *Chamberlain Grp., Inc. v. One World Techs., Inc.*, 944 F.3d 919, 925 (Fed. Cir. 2019) ("Parties are not barred from elaborating on their arguments on issues previously raised.").

(3) Issues Related to the Alleged Inconsistencies between Osanai and Tokuhiro

Patent Owner raises several issues with the combination of Osanai and Tokuhiro that it alleges arise from "inherent inconsistencies" (PO Resp. 41) and incompatibilities between the two references (*Id.* at 35–42). We address these arguments next.

For example, Patent Owner argues that "a POSITA would not have looked to Tokuhiro—which teaches improvements to an <u>off-module memory controller</u>—to improve functionality of Osanai's <u>on-module components</u>." PO Resp. 35. Patent Owner emphasizes that Tokuhiro teaches how the CPU controls an off-module memory controller to eliminate the need for separate read leveling, while Osanai's memory controller (register buffer 400) is located on-module. *Id.* at 36–37 (citing Ex. 1006, 15:3–15, 16:9–22, 16:29–35). Patent Owner argues that Osanai teaches improvements to components of the memory module itself while Tokuhiro teaches improvements to an off-module controller but does not teach improvements to the memory modules themselves. *Id.* at 37–38.

Patent Owner further argues that Tokuhiro is directed to solving a problem that does not exist in Osanai. PO Resp. 38. Tokuhiro centers on determining the delay for read data passing through variable delay circuits DR1 and DR2 which are not present in Osanai. *Id.* 38–39 (citing Ex. 1005 ¶¶ 90, 93, Fig. 5; Ex. 2010 ¶ 121).

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Relatedly, Patent Owner argues that Petitioner has not shown how a person of ordinary skill would have modified Osanai in view of Tokuhiro or that it would be feasible to do so. PO Resp. 39. According to Patent Owner, any attempt to apply the teachings of Tokuhiro to Osanai would require substantial changes to Osanai's hardware without benefit. *Id.* at 39–40. For example, Patent Owner argues that Osanai's read leveling technique determines when to turn on the input buffers INB while Tokuhiro uses write leveling to determine the amount of time to delay data inside the memory controller. *Id.* at 40 (citing Ex. 2010 ¶ 124; Ex. 1006, 10:63–11:15; Ex. 1003 ¶ 157). According to Patent Owner, these two techniques—Osanai's turning on input buffers INB and Tokuhiro's delaying of data—are distinct and not interchangeable. *Id.* Similarly, Patent Owner argues that Osanai uses FIFO 302 to align read data while Tokuhiro uses delay circuits DR1 and DR2 to ensure read data arrives on time regardless of the phase relationship between the data arriving at the memory controller and when data has to go out to the CPU. *Id.* at 40 (citing Ex. 1005 ¶¶ 93, 97, 135; Ex. 1006, 15:16–32, 15:62–16:28; Ex. 2010 ¶ 125).

Patent Owner therefore concludes that Osanai's read leveling and Tokuhiro's adjustment of DR1 and DR2 based on write leveling results serve entirely different purposes, and their implementations are not substitutable. PO Resp. 41.

Having reviewed the evidence in light of the parties' arguments, we determine that Petitioner has sufficiently demonstrated that one of ordinary skill would have been able to combine Osanai and Tokuhiro in the way proposed by Petitioner and would have been able to overcome any differences between the two references. Petitioner's proposed modification involves using Tokuhiro's leveling technique in Osanai's data register

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control circuit 320. Pet. 38–39. Dr. Alpert provides credible testimony that modifying Osanai's data register buffer to incorporate Tokuhiro's technique would not have been beyond the skill of the ordinary artisan. Ex. 1003 ¶ 126.

Some of Patent Owner's arguments entail merely listing differences in the two references without sufficiently explaining why those differences would have prevented one of ordinary skill from combining the teachings of the two references. For example, Patent Owner argues that that "a POSITA would not have looked to Tokuhiro—which teaches improvements to an off-module memory controller—to improve functionality of Osanai's on-module components." PO Resp. 35. But Patent Owner does not explain why a technique used for an off-module controller could not have been used for an on-module controller or why any modifications required to make that technique work would have been beyond the skill of the ordinary artisan. On the other hand, relying on Dr. Alpert's testimony, Petitioner explains that Tokuhiro's leveling techniques would achieve the benefits of ensuring proper timing of signals even when Tokuhiro's technique is used for an off module controller. *See* Pet. Reply 14 (citing Ex. 1003 ¶ 128; Ex. 2011, 100:4–8, 54:21–24, 55:15–18).

As explained above, several of Patent Owner's arguments are based on the fact that Tokuhiro includes variable delay circuits DR1 and DR2 used to delay read data passing through them, while Osanai does not include such delay circuits and instead uses input buffers INB to account for any delays. PO Resp. 38–40. These arguments, however, assume Tokuhiro's variable delay circuitry would need to be bodily incorporated into or with Osanai's circuitry. "The test for obviousness [however] is not whether the features of a secondary reference may be bodily incorporated into the structure of the

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primary reference." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Petitioner is not required to physically incorporate Tokuhiro's variable delay circuits DR1 and DR2 into Osanai. Instead, Petitioner proposes to utilize Tokuhiro's teaching of determining the delay for read operations based on the delay calculated during a prior write leveling operation. Pet. 38–39 (citing Ex. 1003 ¶ 126). Petitioner explains that Osanai includes write leveling operations and that a person of ordinary skill would have been able to modify Osanai's write leveling to use Tokuhiro's leveling technique. *Id.* We determine that Petitioner has sufficiently explained the combination of the two references and that one of ordinary skill would have been able to combine the two even with the differences between the two references.

(4) Motivation to Combine

Patent Owner argues that Petitioner's proposed motivations to combine Osanai and Tokuhiro are inapposite. PO Resp. 42–45. Specifically, Patent Owner argues that Petitioner's assertion that combining Tokuhiro's write leveling technique into Osanai's module would reduce the number of steps to determine the read delay is unsupported. *Id.* at 43. Patent Owner argues that Dr. Alpert's testimony is insufficient and conclusory. *Id.*

Patent Owner further argues that Petitioner is wrong in contending that incorporating Tokuhiro's write leveling technique into Osanai's module would reduce power consumption and circuit area. PO Resp. 43–45. Patent Owner argues that the combination of Osanai and Tokuhiro would not reduce power consumption because Osanai does not include Tokuhiro's delay circuitry DR1 and DR2 and adding such circuitry would likely increase power consumption and circuit area. *Id.* at 44 (citing Ex. 2010

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¶ 131). Furthermore, Patent Owner argues that Tokuhiro merely states implementing its solution would not increase power consumption and circuit area but does not say that it would *reduce* those two aspects.

Finally, Patent Owner argues that Petitioner has not shown that the combination would improve signal fidelity, decrease timing skew or lower the load on the memory controller. PO Resp. 45. Patent Owner argues that Dr. Alpert's testimony in this regard is insufficient and conclusory. *Id.*

Having reviewed the evidence in light of the parties' arguments, we determine that Petitioner has sufficiently demonstrated that one of ordinary skill would have been motivated to combine Osanai and Tokuhiro in the way proposed by Petitioner. Petitioner provides sufficient support for its allegation that one of ordinary skill would have been motivated to combine Osanai and Tokuhiro. For example, Dr. Alpert credibly explains that "it would have been obvious to use Tokuhiro's teaching in Osanai's data register buffer to achieve the same benefit achieved by Tokuhiro's device, i.e., reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling." Ex. 1003 ¶ 126. This is because, as Dr. Alpert explains, Tokuhiro's leveling technique uses timing information determined during write leveling for write operations to determine the delay for subsequent read operations. *Id.* ¶ 122 (citing Ex. 1006, 3:16–26, 16:1–28). Thus, Tokuhiro's technique reduces the number of steps because it uses previous measurements and calculations from prior write leveling instead of making additional measurements and calculations to determine the delay for read operations.

As for reducing power consumption and circuit area, Tokuhiro itself states "[a]ccordingly, the delay times Dt1 and Dt2 from the input of the two signals to the output thereof can be efficiently set without increasing the

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power consumption and the area occupied by the apparatus." Ex. 1006, 24:26–29. Dr. Alpert provides credible testimony that Tokuhiro's leveling technique allows for "using a common structure for implementing write and read delays [that] would improve power consumption for Osanai." Ex. 1003 ¶ 127 (citing Ex. 1006, 21:15–24:42, Figs. 16, 17). We determine that evidence from Tokuhiro and Dr. Alpert sufficiently demonstrates that there would be benefits from using Tokuhiro's technique in combination with Osanai.

In terms of Petitioner's argument that combining Tokuhiro with Osanai would improve signal fidelity, decrease timing skew among components and lower the load perceived by the memory controller (Pet. 40–41), we agree with Patent Owner that the reasoning provided is somewhat conclusory. The portions of Tokuhiro cited in support of this argument do not mention signal fidelity or lowering load, although they do mention adjusting for timing skew. *See* Ex. 1006, 1:63–2:28. Overall, however, considering the other two reasons provided, we determine Petitioner has sufficiently demonstrated that a person of ordinary skill would have been motivated to combine Osanai and Tokuhiro.

In its Sur-reply, Patent Owner again argues that because Osanai uses input buffers for timing its write and read operations, rather than Tokuhiro's variable delay circuits DR1 and DR2 there would be no reduction of steps when Tokuhiro's technique is incorporated with Osanai. PO Sur-reply 15–16. Similarly, Patent Owner argues that there would be no reduction in power or circuit area because the combination would require the addition of Tokuhiro's variable delay circuits DR1 and DR2. PO Resp. 44 (citing Ex. 2010 ¶ 131). We disagree with these arguments for the same reasons explained above, namely that they assume Tokuhiro circuitry must be bodily

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incorporated into Osanai for one of ordinary skill to be able to use Tokuhiro's teachings in combination with Osanai. This, however, is not the standard for obviousness. *Keller*, 642 F.2d at 425.

d) Conclusion Regarding Claim 1

For the aforementioned reasons, we determine Petitioner has demonstrated by a preponderance of the evidence that Osanai and Tokuhiro teach the limitations of claim 1 and that claim 1 would have been obvious over the combination of Osanai and Tokuhiro.

4. Analysis of Claim 2

Claim 2 depends from claim 1 and recites "wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation." Ex. 1001, 19:46–48.

Petitioner contends that Osanai calculates the timing information in both the read and write operations, as evidenced by its read and write leveling circuits and that, when combined with Tokuhiro "Osanai's data register buffer obtains timing information during a '*write memory operation*' prior to the '*read memory operation*' because Tokuhiro's technique uses the timing information from the write operation for the read operation." Pet. 41–42 (citing Ex. Ex. 1006, 3:16–26, 16:14–23; 1003 ¶ 131).

Patent Owner does not separately dispute claim 2 and instead relies on its arguments for claim 1. PO Resp. 49. Nevertheless, we determine Petitioner has not sufficiently shown that the combination of Osanai and Tokuhiro teach the limitations of claim 2. As explained above, Petitioner identifies Tokuhiro's write leveling operation, not a write operation, as the recited "second memory operation." Pet. Reply 2 ("The proposed combination maps the read operation and write leveling operation to the

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claimed '*first*' and '*second memory operation*,' respectively."). Petitioner, however, does not provide sufficient evidence that Tokuhiro's write leveling operation teaches a "memory write operation" as recited in claim 2. As explained above with respect to claim 1, Patent Owner argues that a write leveling operation is not synonymous with a write operation. PO Resp. 27 (citing Ex. 2010 ¶¶ 83–84; Ex. 2011, 118:7–13). Patent Owner provides credible support for its contention from Dr. Przybylski's testimony that "the write leveling procedure as taught by Tokuhiro is not a write operation and does not include a write operation, as that term would be understood by a POSITA at the time of the invention." Ex. 2010 ¶ 83. Dr. Alpert, on the other hand, does not opine on whether a write leveling operation teaches a write operation in his Declaration. The only relevant testimony from Dr. Alpert on this topic comes from his deposition where he was asked "How do write leveling procedures in a write operation relate at all to a memory write operation, if at all?" Ex. 2011, 151:2–4. Dr. Alpert responded that "The write leveling procedure is a number of steps that do involve write leveling operations. And those write leveling operations, I believe do satisfy the claim requirements for a memory write operation." *Id*. at 151:5–9. But Dr. Alpert also testified at his deposition that a write operation and a write leveling procedure were distinct and not synonymous. *Id*. at 118:7–18 ("Q: You agree there is a distinction between a write operation and a write leveling procedure? . . . [Dr. Alpert]: Yes. I would agree in general there's a distinction between the – a write operation and a write leveling procedure. . . . Q: So the term 'write leveling procedure' is not synonymous with the term 'write operation'; correct? A: Yes, I would agree with that."). Without further citations to underlying evidence showing that write leveling would teach a write operation, Dr. Alpert's testimony, which

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is conclusory and contradictory, is insufficient to support the contentions that write leveling is a write operation.

In a footnote in its Reply Brief, Petitioner also argues that "Write leveling is a type of write operation because, for example, and as Netlist's expert admits, the MRS command instructs a memory device to write to its mode register." Pet. Reply 5, n. 1 (citing Ex. 1022, 36:5–11; Ex. 2013, 12–13). Here too, we find insufficient explanation and evidence why setting a bit in the mode register to initiate leveling mode would teach the recited "memory write operation" entailing writing data to memory.

On balance, we determine Petitioner has not presented sufficient evidence demonstrating by a preponderance of the evidence that a person of ordinary skill would have understood a write leveling procedure, as disclosed in Tokuhiro, to teach the recited "memory write operation" of claim 2.

5. *Analysis of Claim 6*

Claim 6 depends from claim 2 and recites

> wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output the respective data and strobe signals.

Ex. 1001, 20:1–7.

Petitioner argues "Osanai discloses a memory module with memory chips organized into multiple ranks. For example, Osanai discloses how the memory module organizes four memory chips 200 into a single group (or set), with one memory chip from each set belonging to a rank ("*the respective set of memory devices include one memory device from each of*

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the plurality of ranks.")." Pet. 42–43 (citing Ex. 1005 ¶¶ 57–58, 111; Ex. 1003 ¶ 133). Petitioner cites to portions of Osanai that explain that its memory module is a "4-Rank configuration" and that the "[m]emory chips in different ranks 'are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL.'" *Id.* at 43 (citing Ex. 1005 ¶¶ 57, 58, 111). Petitioner argues that in Osanai the chip select signals are used to choose memory chips for read/write operations. *Id.*; Ex. 1003 ¶ 133. Patent Owner does not separately dispute Petitioner's contentions regarding dependent claim 6. *See* PO Resp. 49.

Petitioner's contentions for claim 6 do not address the deficiency of their contentions for claim 2. Because we determined Petitioner has not sufficiently shown that the cited references teach the limitations of claim 2, we also, for the same reasons, determine Petitioner has not shown that the cited references teach the limitations of claim 6.

6. Analysis of Claim 10

Claim 10 depends directly from claim 1 and recites "wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte." Ex. 1001, 20:29–32. Petitioner contends that "Osanai expressly discloses that 'a single data register buffer 300 inputs and outputs 1-byte data . . . .'" Pet. 43 (citing Ex. 1005 ¶ 91; Ex. 1003 ¶ 136). Petitioner additionally contends that "[e]ach of Osanai's memory devices also has a data width of eight bits." *Id.* at 43–44 (citing Ex. 1005 ¶ 59). Patent Owner does not separately dispute Petitioner's contentions regarding claim 10. *See* PO Resp. 49.

We agree with Petitioner, that the aforementioned explicit teachings of Osanai disclose buffer circuits with a data width of 1 byte and memory

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devices with data widths of 1 byte (8 bits). Ex. 1005 ¶¶ 59, 91. We determine Petitioner has sufficiently demonstrated Osanai teaches the limitations of claim 10.

7. *Analysis of Claim 11*

Claim 11 depends from claim 10 and recites

> wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals.

Ex. 1001, 20:33–39.

Petitioner refers back to its contentions for claim 6, which recited similar limitations. Pet. 44 ("Osanai discloses this limitation for the same reasons specified in claim 6."). We summarize Petitioner's contentions for claim 6 here.

Petitioner argues "Osanai discloses a memory module with memory chips organized into multiple ranks. For example, Osanai discloses how the memory module organizes four memory chips 200 into a single group (or set), with one memory chip from each set belonging to a rank ('*the respective set of memory devices include one memory device from each of the plurality of ranks*.')." Pet. 42–43 (citing Ex. 1005 ¶¶ 57–58, 111; Ex. 1003 ¶ 133). Petitioner cites to portions of Osanai that explain that its memory module is a "4-Rank configuration" and that the "[m]emory chips in different ranks 'are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL.'" *Id.* at 43 (citing Ex. 1005 ¶¶ 57, 58, 111). Petitioner argues that in Osanai the chip select signals are used to choose memory chips for read/write operations.

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Id.; Ex. 1003 ¶ 133. Patent Owner does not separately dispute Petitioner's contentions regarding dependent claim 6 or dependent claim 11. *See* PO Resp. 49.

Having reviewed Petitioner's contentions and the underlying evidence we are persuaded that Osanai teaches the limitations of claim 11 for the reasons summarized above. Specifically, we agree that Osanai discloses memory devices that are arranged in a 4-Rank configuration where the ranks are activated using chip select and clock enable signals to receive or output the respective data and strobe signals. Ex. 1005 ¶ 57, Fig. 1; Ex. 1003 ¶¶ 133, 137. The 4-Rank configuration teaches that the memory devices are arranged in a plurality of ranks with at least one memory device from each rank. The disclosed chip select signals teach the recited "chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals."

Unlike claim 6, which depends from claim 2, claim 11 does not include a requirement that the first memory operation be a read operation and the second memory operation be a write operation. Thus, Petitioner's contentions for claim 11 do not suffer the same deficiencies as those for claim 6.

8. Analysis of Claim 12

Claim 12 depends from claim 1 and recites "wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits." Ex. 1001, 20:40–43.

Petitioner contends that Osanai's data register buffer 300 has a data width of 1 byte and each of Osanai's memory devices also has a data width of eight bits. Pet. 44 (citing Ex. 1005 ¶¶ 91, 59). According to Petitioner

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"Osanai explains, however, that the number of memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number'—that is, different data widths were envisioned by Osanai." *Id.* at 44–45 (citing Ex. 1005 ¶ 196; Ex. 1003 ¶ 139). Petitioner relies on Dr. Alpert's testimony that there would be motivation to modify Osanai's memory devices to use four bits instead of eight bits for four reasons: (1) four bits complies with commercial standardization of DDR3, (2) using four bits would reduce packaging costs, (3) implementing a data width of four bits instead of eight bits would simplify routing, allow for increased memory density, and potentially improve speed by having fewer devices connected to each data line (4) implementing a data width of 4 bits would simply arrange old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement." *Id.* at 45 (citing Ex. 1003 ¶ 140; Ex. 1013, 3).

Patent Owner argues that Osanai's statement that "memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number" relates to having more ranks rather than a suggestion to use data widths other than 8 bits. PO Resp. 46 (citing Ex. 1005 ¶ 196; 2010 ¶ 142). Patent Owner further argues that even if using 4 bits complies with the DDR3 standard, as Petitioner alleges, the DDR3 standard can "specify myriad features that may or may not function well, be compatible with a given disclosure, or provide motivation to a POSITA." *Id.* at 47. Patent Owner argues that the DDR3 standard shows that 4-bit and 8-bit devices are in the very same package, undercutting Petitioner's argument that using four bits would reduce packaging costs. *Id.* at 47 (citing Ex. 1013, 3–4; Ex. 2010 ¶ 144). Patent Owner argues that it is not inherently true that 4-bit modules have simpler routing than 8-bit modules, or that they have higher density or

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improve speed. *Id.* at 48 (citing Ex. 2010 ¶ 145). Finally, Patent Owner argues that "design complications resulting from splitting bus widths at the data register buffers would dissuade a POSITA from making the proposed modification, especially in the absence of a benefit from using 4-bit devices with 8-bit data register buffers." *Id.* at 49 (citing Ex. 2010 ¶ 146).

Having reviewed the record and the arguments, we are persuaded that, based on the teachings of Osanai and the knowledge of one of ordinary skill in the art, implementing a plurality of buffer circuits with a data width of 1 byte, and memory devices with a data width of 4 bits would have been obvious. Petitioner has demonstrated, and Patent Owner does not dispute, that Osanai teaches buffer circuits with a data width of 1 byte. Pet. 44 (citing Ex. 1005 ¶¶ 91, 59). Petitioner acknowledges, however, that Osanai teaches memory devices with a data width of 8 bits rather than 4 bits. Ex. 1005 ¶ 59 ("An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits)."). With regard to the memory devices, Petitioner has demonstrated that the JEDEC standard specifies both 4-bit and 8-bit data widths (Ex. 1013, 3–4). This shows that designing memory devices with either one of these widths was well known and in compliance with the industry wide standard. Dr. Alpert provides credible testimony that a 4-bit data width provides some benefits over an 8-bit data width and that at the very least choosing between the available selections would have been a matter of design choice with corresponding tradeoffs each yielding predictable and expected results. Ex. 1003 ¶ 140. We agree with Petitioner that the aforementioned evidence and reasoning is sufficient in demonstrating that 4-bit data width memory devices would have been obvious in light of the cited evidence and the knowledge of one of ordinary skill in the art.

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9. Analysis of Claim 13

Claim 13 depends from claim 12 and recites:

> wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to receive or output the respective data and strobe signals, the two memory devices being in the same rank.

Ex. 1001, 20:44–51.

Petitioner argues that "Osanai discloses a memory module with memory chips organized into multiple ranks, which are selected by the chip select (CS) or clock enable (CKE) signals, both of which are '*chip select signals.*'" Pet. 46 (citing Ex. 1005 ¶ 57; Ex. 1003 ¶ 143). Petitioner argues that using two chip select signals a memory controller may select up to two ranks of memory chips, that is selecting one memory chip from each selected rank. *Id.* (citing Ex. 1005 ¶ 57; Ex. 1007, 5:12–15; Ex. 1003 ¶ 143). Petitioner argues that one of skill in the art would have recognized that using the same chip select signals selects multiple memory chips from the same rank. *Id.* Ex. 1003 ¶ 143; Ex. 1005 ¶¶ 57, 58, 111. Patent Owner relies on its arguments for claim 12 and does not separately dispute dependent claim 13. *See* PO Resp. 49.

We are persuaded that Osanai teaches the limitations of claim 13 for the reasons summarized above. In addition, Dr. Alpert provides credible testimony supporting Petitioner's arguments. Ex. 1003 ¶ 143. Specifically, Dr. Alpert testifies that in light of Osanai's teachings, one of skill in the art would have recognized that using the chip select signals can select multiple memory chips from the same rank. *Id.* (citing Ex. 1005 ¶¶ 57, 58, 111).

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10. Analysis of Claim 21

Claim 21 depends from claim 1 and recites "wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device." Ex. 1001, 22:10–13. Petitioner contends that the command/address/control register buffer 400 sends clock signals or alternatively DRC signals ("one or more signals") to the data register buffer 300 ("buffer circuit"). Pet. 47 (citing Ex. 1005, Figs. 5, 7, 14A; Ex. 1003 ¶ 147). Petitioner contends that Osanai's read and write leveling circuitry use both these signals to adjust the read and write timing. *Id*. Patent Owner does not separately dispute Petitioner's contentions for claim 21. *See* PO Resp. 49.

Having reviewed Petitioner's contentions and the underlying evidence we are persuaded that Osanai teaches the limitations of claim 21 for the reasons summarized above. Dr. Alpert provides credible testimony that Osanai's read and write leveling circuitry use module clock signals (CK) ("one or more signals") to add time delays to create the data and strobe signals. Ex. 1003 ¶¶ 116–117.

11. Analysis of Claim 22

Claim 22 depends from claim 1 and recites "wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the memory controller." Ex. 1001, 22:14–17.

Petitioner contends "Osanai discloses that data register buffer 300 receives a DQS from the memory controller 12." Pet. 48 (citing Ex. 1005 ¶ 159, Fig. 2). Petitioner relies on Dr. Alpert's testimony as supporting the

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fact that "during a write operation (the '*second memory operation*'), the data register buffer 300 ('*each respective buffer circuit*') receives a DQS signal from memory controller 12 ('*at least one signal from the memory controller*')." *Id.* (citing Ex. 1003 ¶ 149). Patent Owner does not separately dispute Petitioner's contentions for claim 23. *See* PO Resp. 49.

Having reviewed Petitioner's contentions and the underlying evidence, we are not persuaded that Petitioner has sufficiently demonstrated that Osanai teaches the limitations of claim 22. Petitioner contends that "data register buffer 300 receives a DQS from the memory controller 12" but that it does so during a write operation. Pet. 48. Similarly, Dr. Alpert's testimony refers to the write operation when describing that the data register buffer 300 receives a DQS. Ex. 1003 ¶ 149. Petitioner, however, has identified the write leveling operation as the recited "second memory operation." Pet. Reply 2 ("The proposed combination maps the read operation and write leveling operation to the claimed '*first*' and '*second memory operation*,' respectively."). Petitioner does not provide sufficient explanation for why teachings regarding signals received during a write operation would teach a person of ordinary skill that those signals would be received during the write leveling operation relied upon by Petitioner as the recited "second memory operation" as well. As we explained in our analysis of claim 2, we do not agree that a write leveling operation would have taught a write operation to one of skill in the art. Thus, we determine Petitioner has not demonstrated that the relied upon references teach the limitations of claim 22.

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12. Conclusion – Obviousness over Osanai and Tokuhiro (Ground 1)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 10–13, and 21 of the '035 patent would have been obvious over Osanai and Tokuhiro. We are not persuaded that Petitioner has sufficiently demonstrated by a preponderance of the evidence that claims 2, 6, and 22 would have been obvious over Osanai and Tokuhiro.

E. Ground 2 – Obviousness over Takefman and Tokuhiro

Petitioner argues claims 1, 2, 6, 12–13, and 21 of the '035 patent would have been obvious over Takefman and Tokuhiro. Pet. 48–70. Below we provide a brief overview of the prior art references and then analyze Petitioner's contentions in light of Patent Owner's arguments. For the reasons discussed below, we determine Petitioner has not shown that the combination of Takefman and Tokuhiro teaches limitation 1[c] and 1[d].

1. Takefman (Ex. 1007)

Takefman relates to a computer interface which uses a memory bus to connect a computer processing unit and a memory device. Ex. 1007, 1:48–55. Figure 3, reproduced below, is a block diagram of a "TerraDIMM," a type of memory device. *Id.* at 2:5–6; *see id.* at 4:9, 4:27–29.

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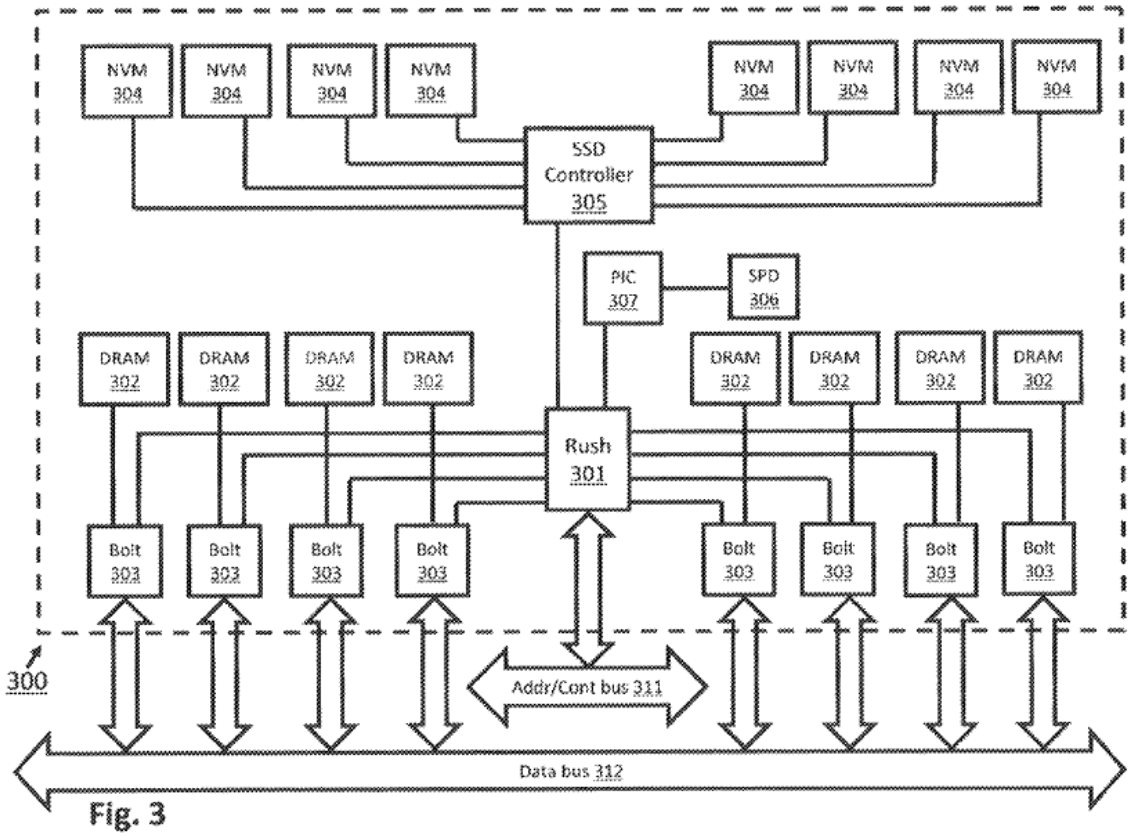

Fig. 3

As shown in Figure 3, "TeraDIMM 300 includes an ASIC 301, herein the 'Rush,' a rank of DRAM devices 302, a number of data buffer devices 303, herein 'Bolt' devices, a rank of [non-volatile memory (NVM)] devices 304, [solid state disk (SSD)] controller 305, [serial presence detect (SPD)] 306, and a PIC microcontroller 307." Ex. 1007, 5:53–59. Further, "address/control bus 311 is connected to the Rush 301 while the main memory bus 312 is separated from the on-DIMM memory bus by the Bolt devices 303." *Id.* at 5:67–6:3. Still further, "Rush 301 also includes control circuitry for the Bolt devices 303" and "SSD controller 305 manages the flow of data going to and from the NVM devices 304." *Id.* at 5:62–66.

Takefman explains that

> [e]ach of the Bolt devices include three DDR-3 ports . . . that allow the host port (connected to the memory bus) to connect to any of the three DDR-3 ports. Furthermore, each port of the DDR-3 ports can be tri-stated and can signal using DDR-3

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> DQ/DQS signaling. Bolt devices 303 provide retiming of data bursts from the computer system to/from the DRAM devices 302 or Rush 301. Bolt devices 303 also provide a separation that allows on-DIMM DMA (direct memory access) to occur between the DRAM devices 302 and the Rush 301.

Id. at 6:4–13.

Takefman further explains that

> [o]ne aspect to the Rush 301 data interface is the inclusion of per-lane delay compensation circuits that, for instance, provide programmable launch times and lane de-skew on receive. Because of the difference in the distances between the Bolt devices 303 and the Rush 301 and the Bolt devices 303 and the DRAM devices 302, the TeraDIMM may arrange its launch time Such that its data arrives at an appropriate time.

Id. at 6:14–20.

2. *Analysis of Claim 1*

As mentioned above, we determine Petitioner has not shown that the combination of Takefman and Tokuhiro teaches limitations 1[c] and 1[d]. Because this determination is dispositive of Petitioner's challenge over Takefman and Tokuhiro, we begin by directly analyzing limitations 1[c] and 1[d].

a) *Summary of Petitioner's Contentions*

Limitation 1[c] recites:

> a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals.

Ex. 1001, 19:17–22. Petitioner identifies Rush 301 as the recited "module control device" and argues that it is configured to receive memory

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commands, such as read and write commands, directly from the address/control bus 311. Pet. 53–54 (citing Ex. 1003 ¶ 164; Ex. 1007, 1:58–3:6, 5:44–47, 5:67–6:3, 19:38–46, 21:11–48, 21:49–22:15, Fig. 3). Petitioner argues that a person of ordinary skill would have understood that DRAM is used for writing, storing, and reading data Petitioner argues that "a POSITA would have recognized that Rush 301 receives commands from the Takefman's northbridge 106" and that "[a]fter receiving those commands, such a person would also have understood that Rush 301 outputs 'module command' and 'control signals' for the first memory operation (a read operation)." Pet. 55 (citing Ex. 1003 ¶ 164; Ex. 1007, 2:58–3:40).

Limitation 1[d] recites "memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals." Ex. 1001, 19:23–25. Petitioner identifies DRAM 302 as the recited "memory devices" and memory module 300 as the recited "module board" and argues that a person of ordinary skill would have recognized DRAM 302 receives "module command signals" from Rush 301 that instruct the DRAM to perform certain operations such as a write operation. Pet. 56 (citing Ex. 1007, 19:38–46, 21:49–22:15; Ex. 1003 ¶ 168).

b) Summary of Patent Owner's Arguments

Patent Owner argues "Petitioners wholly fail to allege, much less show, where Takefman discloses that Rush 301 outputs any claimed '*module command signals*' to any memory device or any claimed '*module control signals*' to any claimed buffer." PO Resp. 50–51. Patent Owner emphasizes that Petitioner's analysis for the "module command signals" and "module control signals" limitations is limited to "**<u>one sentence total</u>**" and is

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conclusory with Dr. Alpert merely repeating the same language found in the Petition itself. *Id*. at 51 (citing Ex. 1003 ¶ 164). Patent Owner also argues that Takefman's Rush 301 does not communicate directly with DRAM 302 devices and instead only communicates with the Bolt 303 devices. *Id*. at 51 (citing Ex. 1007, Fig. 3; Ex. 2010 ¶ 158). With respect to limitation 1[d], Patent Owner argues "Petitioners do not attempt to show that DRAM 302 performs any '*memory operation*' '*in response to the module command signals*' as required by the claims—because Petitioners have not identified any '*module command signals*' at all." PO Resp. 53.

Petitioner responds that claim 1 does not require a direct connection between the module control device (Takefman's Rush 301) and the claimed memory devices (Takefman's DRAM 302). Pet. Reply 20. Further, Petitioner argues that Takefman's Rush 301 receives memory commands, such as read and write commands, from northbridge 106 and that "[a]fter doing so, and as Dr. Alpert explains, a POSITA would have understood that Rush 301 outputs '*module command*' and '*module control signals*' destined for a '*memory device*' to perform operations, such as read and write operations." Pet. Reply 21 (citing Pet. 55; Ex. 1003 ¶ 164).

c) Analysis

Having reviewed the record and contentions, we agree with Patent Owner that Petitioner's arguments are insufficient in showing that Takefman teaches the recited "module command signals" and "module control signals." The totality of Petitioner's contentions regarding the "module command signals" and "module control signals" consists of Petitioner arguing that Takefman's Rush 301 receives read and write commands from the northbridge 106 via the address/control bus for DRAM 302. Pet. 54

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(citing Ex. 1007, 1:58–3:6, 5:44–47, 5:67–6:3, 19:38–46, 21:11–48, 21:49–22:15, Fig. 3). Petitioner then summarily concludes that a person of ordinary skill would have understood that Rush 301 outputs "module command" and "control signals" for the first memory operation. *Id.* at 55 (citing Ex. 1003 ¶ 164). In doing so, Petitioner does not cite to anything in Takefman itself to support its contention that Rush 301 outputs the module command and module control signals when it receives the read and write commands from the northbridge 106. Instead, Petitioner relies only on Dr. Alpert's testimony. Dr. Alpert, however, merely repeats Petitioner's contentions without providing any additional technical details or citing to any underlying evidence. *See* Ex. 1003 ¶ 164. Such testimony is entitled to little weight. *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) ("This court's opinions have repeatedly recognized that conclusory expert testimony is inadequate to support an obviousness determination on substantial evidence review"); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-000624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential); 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."). Because Dr. Alpert merely repeats Petitioner's contentions, no explanation is provided to make up for the lack of direct evidence that Takefman discloses any signals output from Rush 301. Specifically, no explanation is provided why signals are output from Rush 301, and why those signals would teach the two types of recited signals: (1) "module command signals" and (2) "module control signals."

At the oral hearing, Petitioner addressed Patent Owner's argument by stating "Takefman's figure only showed that it [the module command and control signals] can come from one place, from Rush. . . . But [module

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command and control] signals have to come from Rush." Tr. at 53:9–12. This argument, that the module command and control signals must necessarily exist and be output from Rush 301, was not made in the Petition, Petitioner's Reply, or in Dr. Alpert's Declaration, and is, therefore, untimely. Petitioner has the burden to demonstrate sufficiently in the Petition that the cited prior art renders the challenged claims unpatentable, including showing that the Petition's contentions are supported by evidence. *See* 35 U.S.C. § 314(a); *see also Harmonic Inc.*, 815 F.3d at 1363 (Fed. Cir. 2016) ("In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." (emphases added) (citing 35 U.S.C. § 312(a)(3))); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (requiring "the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" (emphases added)). Moreover, even if we were to consider such an argument, Petitioner would still have to provide some explanation and evidence for why those signals must exist, why they must necessarily be output from Rush 301, and why those signals must include both module command and module control signals. Such an explanation is missing from the record.

In summary, Petitioner provides evidence that Rush 301 receives read and write commands from the northbridge 106 and that a person of ordinary skill would understand these commands are for DRAM 302. Pet. 53–55. From this Petitioner summarily concludes that Rush 301 outputs module command signals and module control signals without any support from Takefman itself or from non-conclusory expert testimony. *Id.* at 55. We agree with Patent Owner that, under these circumstances, Petitioner has not

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carried its burden in demonstrating that Takefman teaches limitations 1[c] and 1[d].

3. Analysis of Dependent Claims 2, 6, 12–13, and 21

Claims 2, 6, 12–13, and 21 depend either directly or indirectly from independent claim 1. A review of Petitioner's contentions for these dependent claims shows that these contentions do not remedy the aforementioned deficiencies regarding the module command and control signal limitations of claim 1. Accordingly, we determine Petitioner has not demonstrated by a preponderance of the evidence that the combination of Takefman and Tokuhiro teach the limitations of dependent claims 2, 6, 12–13, and 21.

4. Conclusion – Obviousness over Takefman and Tokuhiro (Ground 2)

Accordingly, having considered the arguments and evidence, we are not persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 2, 6, 12–13, and 21 of the '035 patent would have been obvious over Takefman and Tokuhiro.

F. Ground 3 - Obviousness over Takefman, Tokuhiro, and Osanai

Petitioner argues claims 1, 2, 6, 12–13, and 21 of the '035 patent would have been obvious over Takefman, Tokuhiro and Osanai. Pet. 70–71. Petitioner's Ground 3 challenge is based on its Ground 2 challenge over Takefman and Tokuhiro, except that Petitioner explicitly relies on Osanai for certain limitations "[t]o the extent that Netlist argues that the proposed modifications would not be obvious over Takefman in view of Tokuhiro." Pet. 71. Specifically, Petitioner relies on Osanai for the following: (1) teaching that Takefman's data bus 312 would include "data/strobe signal

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lines;" (2) to incorporate read and write leveling circuitries like those in Osanai to teach "logic configured to obtain timing information based on one or more signals received by the each respective buffer circuit and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information;" (3) modify Takefman's memory module so that "each of the plurality of buffer circuits has a data width of 1 byte, and [] each of the memory devices has a data width of 4 bits." *Id*. at 70–71.

As can be seen, Petitioner does not rely on Osanai for teaching "module command" and "module control" signals and its Ground 3 challenge does not remedy the deficiencies that we identified in its contentions regarding these limitations in Ground 2. For the reasons explained above with respect to Ground 2, we determine Petitioner has not demonstrated, by a preponderance of the evidence, that claims 1, 2, 6, 12–13, and 21 of the '035 patent would have been obvious over Takefman, Tokuhiro, and Osanai.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that claims 1, 10–13, and 21 of the '035 patent are unpatentable. Petitioner has not demonstrated by a preponderance of the evidence that claims 2, 6, and 22 of the '035 patent are unpatentable.[6]

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[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application

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Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1, 2, 6, 10–13, 21, 22	103(a)	Osanai, Tokuhiro	1, 10–13, 21	2, 6, 22
1, 2, 6, 12–13, 21	103(a)	Takefman, Tokuhiro		1, 2, 6, 12–13, 21
1, 2, 6, 12–13, 21	103(a)	Takefman, Tokuhiro, Osanai		1, 2, 6, 12–13, 21
Overall Outcome			1, 10–13, 21	2, 6, 22

IV. ORDER

For the foregoing reasons, it is

ORDERED that claims 1, 10–13, 21 of the '035 patent are held to be unpatentable;

ORDERED that claims 2, 6, and 22 are not held to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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