

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00847
Patent No. 10,268,608

PATENT OWNER RESPONSE

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TABLE OF CONTENTS

	<u>Page</u>
I. INTRODUCTION	1
II. TECHNICAL OVERVIEW	4
III. THE '608 PATENT	7
IV. SKILL LEVEL OF A POSA	12
V. THE PRIOR ART	12
A. Hiraishi (EX1005)	12
1. General Architecture	12
2. Hiraishi's Read/Write Leveling Functions	14
B. Tokuhiko (EX1006)	16
VI. THE CHALLENGED CLAIMS ARE NOT OBVIOUS IN LIGHT OF GROUND 1 REFERENCES	18
A. The Recited "Data Path" Does Not Include Strobe Signal Lines	19
B. Petitioner Fails to Identify a Delay Circuit in the "Data Path"	26
1. The Delayed Signal Must Be "Through the Data Path" And Delayed by a "Delay Circuit" in the "Data Path"	26
2. The Petitioner Has Not Established That Hiraishi Discloses the Recited "Delay Circuit" or Delaying a "Signal through the Data Path"	28
(a) The Alleged "Delay Circuit" for Write Operations Does Not Satisfy the Limitation	29
(b) The Alleged "Delay Circuit" for Read Operations	36
3. Alleged Admissions From Prior Proceeding	40

C.	Hiraishi's WL Re-timing Is Not Based on the Results of Hiraishi's S4 Write Leveling and Does Not Satisfy Element 1[f]	40
1.	Hiraishi's S-4 Write Leveling Operations Adjust the Timing of DQS to Align with the Clock.....	41
2.	Hiraishi's WL Re-timing Addresses Flight Delays for Write Operations by Adding a Clock Cycle of Latency	46
D.	Hiraishi's CL Re-Timing Is Not Based on the Results of S-4 Read Leveling and Does Not Satisfy Element 1[f]	52
1.	Hiraishi's S4 Read Leveling Operations Adjust the Activation Timing of Hiraishi's Input Buffers Which the Petition Contends are Tristate Buffers.....	53
2.	Hiraishi's CL Re-timing Addresses Flight Delays for Read Operations By Adding a Clock Cycle of Latency	55
VII.	THE PETITIONER FAILED TO ESTABLISH THAT ANY CLAIM OF THE '608 PATENT IS UNPATENTABLE UNDER GROUND 2	58
A.	Petitioner Has Failed To Establish That Ground 2 Has a Delay Circuit in the Data Path.....	58
B.	A POSA Would Not Have Had a Reasonable Chance of Successfully Achieving the Claimed Invention Based on the Proposed Modification to Hiraishi	60
1.	The Added Delay Element is Inoperable	60
2.	There is No Motivation to Use the New Delayed DQS Signal to Clock Data Out from Hiraishi's FIFO, Which Would Not Be Expected to Reliably Synchronize DQS/DQ Signals	65
C.	Petitioner's Motivation Arguments Do Not Support the Combination of Hiraishi and Tokuhiro, as Proposed.....	71

1.	Petitioner’s Motivation Arguments Do Not Motivate Deviating From Hiraishi’s and Tokuhiro’s Disclosures of Using Delay Elements in a Memory Controller.....	71
2.	Petitioner’s Arguments for Moving Tokuhiro’s Delay Elements Are Unsupported and Contrary to General Knowledge in the Art.....	72
3.	Petitioner’s Motivation Arguments Are Conclusory and Unsupported	80
VIII.	CONCLUSION.....	83

TABLE OF AUTHORITIES

	Page(s)
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<i>Arctic Cat Inc. v. Polaris Indus., Inc.</i> , 795 F. App'x. 827 (Fed. Cir. 2019)	63, 81
<i>In re Fritch</i> , 972 F.2d 1260 (Fed. Cir. 1992)	64
<i>In re Sponnoble</i> , 405 F.2d 578 (CCPA 1969)	64
<i>Tec Air, Inc. v. Denso Mtg. Michigan Inc.</i> , 192 F.3d 1353 (Fed. Cir. 1999)	64
<i>Winner Int'l. Royalty Corp. v. Wang</i> , 202 F.3d 1340 (2000)	82
Other Authorities	
IPR2017-00730, Paper 8	3, 53

EXHIBIT LIST

Exhibit No.	Document
EX2001	Statutory Disclaimer for 15/820,076
EX2002	Power of Attorney and Filing Receipt for 15/820,076
EX2003	IPR2022-00237 IPR Petition
EX2004	U.S. Publication No. 2010/0312925 (Osanai)
EX2005	IPR2022-00711 Record of Oral Hearing
EX2006	IPR2022-00237 DECISION Denying Institution of IPR
EX2007	IPR2022-0711 IPR Petition
EX2008	U.S. Patent No. 8,713,379 (Takeman)
EX2009	IPR2022-00237 Petitioner's Request for Rehearing
EX2010	IPR2022-00237 DECISION Denying Petitioner's Request for Rehearing
EX2011	IPR2022-00237 Declaration of Donald Alpert, Ph.D.
EX2012 (New)	Deposition Transcript of Robert Wedig
EX2013 (New)	Declaration of Dr. William Mangione-Smith
EX2014 (New)	JEDEC STANDARD, DDR2 SDRAM SPECIFICATION (JESD79-2F) (November 2009)
EX2015 (New)	JEDEC STANDARD, DDR3 SDRAM Standard (JESD79-3F) (Revision of JESD79-3E, July 2010) (July 2012)
EX2016 (New)	Deposition of Robert Wedig in IPR2022-00711 (506 IPR)
EX2017 (New)	Electronics Cooling, Challenges In Thermal Management Of Memory Modules
EX2018 (New)	JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification (JES79) (June 2000)
EX2019 (New)	JEDEC STANDARD, DDR3 SDRAM Specification (JESD79-3A) (Revision of JESD79-3) (September 2007)

EX2020 (New)	Petition for Inter Partes Review of U.S. Patent No. 10,860,506 (IPR2022-00711)
EX2021 (New)	Final Written Decision (IPR2022-00711)
EX2022 (New)	DECISION Denying Patent Owner's Request on Rehearing of Final Written Decision (IPR2022-00711)
EX2023 (New)	Final Written Decision (IPR2022-00236)

STATEMENT OF MATERIAL FACTS IN DISPUTE

Petitioner did not submit a statement of material facts in this Petition. Accordingly, no response is due pursuant to 37 C.F.R. § 42.23(a), and no facts are admitted.

I. INTRODUCTION

The asserted claims require “*a data path corresponding to each data signal line* in the respective set of data/strobe signal lines” wherein the each recited “data path ... includes ... a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.” Pet. xiii, 1[e]-1[f]. As the Board noted at institution, “Petitioner has identified portions of Hiraishi that includes portions of data and data strobe signal lines as part of the claimed ‘data path.’” Institution Decision (“ID”), 30-31. Petitioner highlighted the relied-on data strobe signal lines for write operations in its annotated figure below in orange cross-hatching. That expansive read is needed in order to accommodate a delay circuit with components—including Hiraishi’s DLL circuit, delay circuits 370 and 372, and strobe generating circuits 374 and 376—that are not on the data (DQ) signal lines and delay signals (such as strobe signals and clock signals) which do not pass “through the data path.”

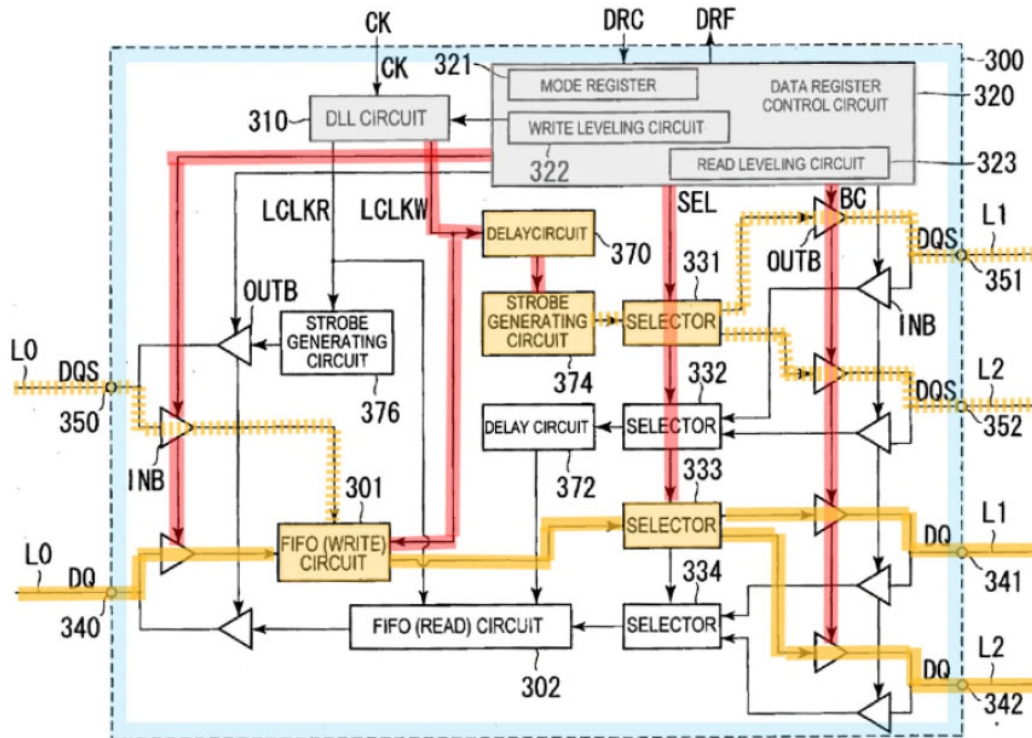


FIG. 5

Petitioner also fails to establish that Hiraishi's FIFOs are the claimed delay circuit. First, Petitioner does not contend that Hiraishi's FIFO circuits alone can be the claimed delay circuit. Second, to the extent that Hiraishi's FIFOs' re-timing of data signals is considered a delay, it is done "in synchronization with the internal clock LCLKR" or LCLKW, which are derivatives of the system CK(IN) received by the data register buffer. EX1005, [0130], [0135]. The claims, however, require the delay circuit be "configured to delay a signal through the data path ... *in response to at least one of the module control signals.*" Clock signals are not module control signals, nor does Petitioner contend they are. Pet., 39 (identifying DRC as module control signals). Third, Hiraishi's re-timing—as the Board previously found—is

unrelated to read and write leveling. *See* IPR2017-00730, Paper 8 (“the ’632 Decision”), 14. Thus, even if read/write leveling determines some amounts of delay in response to a module control signal as Petitioner contends, the FIFOs (nor any other components) are configured to delay DQ signals through the data path by that amount as required by element 1[f]. Rather, Hiraishi’s re-timing just increases the latency to the next clock cycle regardless of the amount of DQS adjustment determined in S4 leveling. *See* EX1005, [0130], [0135].

Indeed, Hiraishi only states that its S4 write leveling process “changes the output timing of the data strobe signal DQS” EX1005, [0145]. As for read leveling, as the Board previously observed, it is to “find a time A from an input timing of the read command Read ... until the read data DQ is input” for “use[] in an adjustment of an activation timing of the input buffer circuit INB and the like.” *Id.*, [0151]; *see* ’632 Decision, 10, 13. INB, however, is identified by Petitioner as satisfying a separate claim element (tristate buffer) and is not part of the delay circuit. Simply put, the results of read/write leveling are not used to delay signals through the data paths (*i.e.* DQ signals through DQ lines). *Contra* Pet. 43-44, 47, 51.

Butt does not cure this deficiency and is not cited for any particular disclosure, but is only cited for alleged understanding of Hiraishi.

Tokuhiro likewise does not cure Hiraishi’s deficiencies because the DR-1 delay element that Petitioner proposes to add from Tokuhiro is in strobe generating

circuit 376, which is not on any of the DQ lines and therefore cannot satisfy the requirement for the delay circuit and does not delay a signal through any data path.

See below.

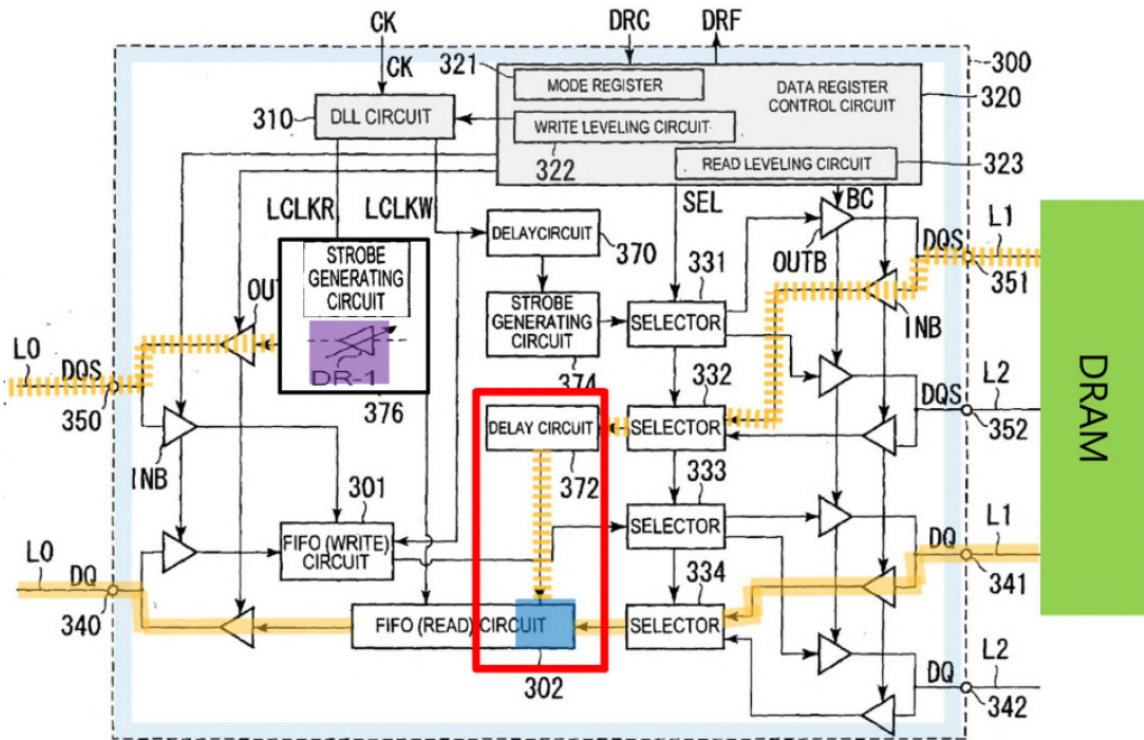


FIG. 5

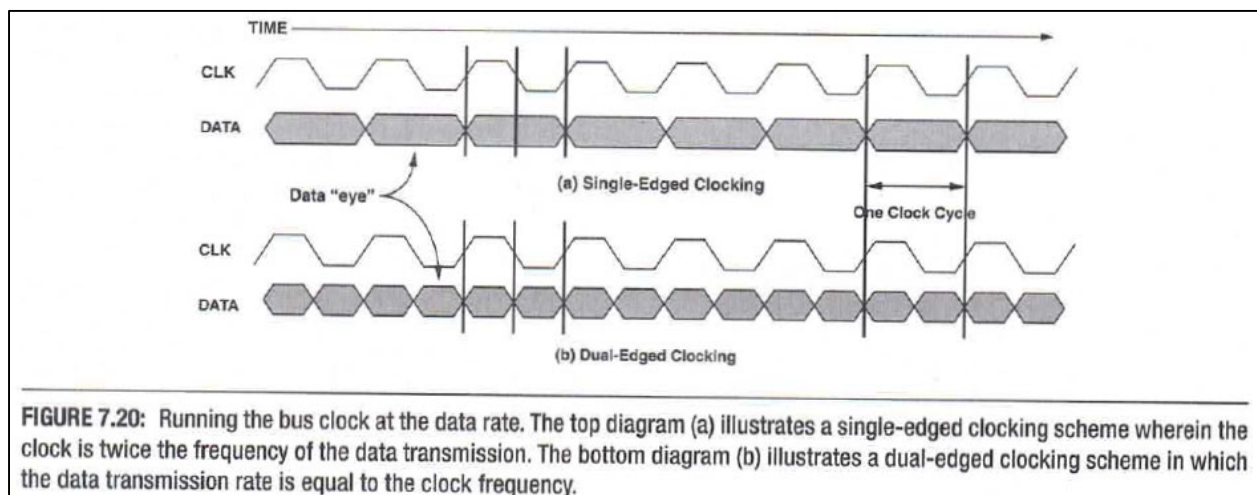
For these and additional reasons stated in more detail below, Petitioner's challenges fail.

II. TECHNICAL OVERVIEW

A DRAM system is a type of computer memory that comprises a memory controller and a number of DRAMs organized into memory modules, which are printed circuit boards containing a number of DRAMs. EX1021, 11; EX2013, ¶17.

The most common type of DRAM is synchronous DRAM, or SDRAM, which uses a system-level clock to time all actions, i.e., command and data transmissions. EX1021, 332. Most modern SDRAM is “Double Data Rate” (DDR) memory. Unlike single data rate SDRAM which transmits data (a ‘data period’) once per clock cycle, DDR SDRAM uses both the rising edge and the falling edge of the clock cycle to transmit data, effectively doubling the amount of data transmitted in a given clock cycle. *See id.*, 333; Figure 7.20 below.

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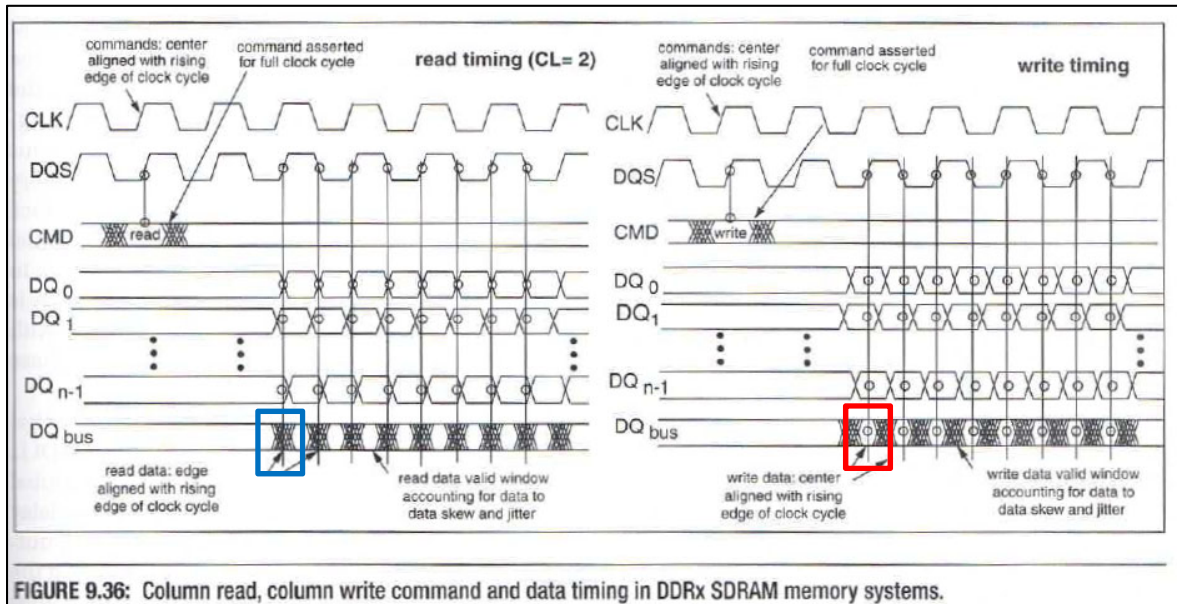
Id., 334; EX2013, ¶¶18-20.

A drawback of the dual-edged clocking scheme of DDR is that it has fewer clock edges available to synchronize transmissions. EX1021, 334. Consequently, DDR SDRAM uses a special type of signal, called a strobe signal or “DQS” signal, to ensure accurate timing for driving and sampling/capturing incoming data. *See id.* Generally, strobe signals indicate that another signal (e.g., data or command) is

present and valid. *See id.*, 318, fn 1. This allows the system to distinguish each data transmission accurately in a clock cycle, which facilitates the accurate reception of data. EX2013, ¶21. Timing of strobe signals, however, does not affect timing of the data signal, just the accuracy in capturing data. *See id.*

DQ and DQS signals are sent via distinct signal lines in order for the DQS signals to serve their purpose of ensuring accurate timing for sampling/capturing DQ data. EX2012 (Wedig), 54:11-12 (“DQS lines work to provide information as to when the DQ lines are valid.”). For example, the DDR standard requires a center-aligned strobe signal be provided by the memory controller for all DRAM *writes*, which enables the DRAMs to sample/latch in the incoming DQ data signals. EX1021, 405 (“[T]he DRAM memory controller delays the DQS signal by 90° relative to write data. The DRAM devices then latch in data relative to each edge of the DQS signal without shifting or delaying the data.”). For DRAM *reads*, however, the strobe signal is provided by the DRAMs edge-aligned with the data and system clock, which means the memory controller must provide a mechanism for generating a center-aligned DQS signal in order to sample the received DQ read data. EX1021, 334, 406 (“[T]he DRAM memory controller must also adjust the phase relationship between read data and the DQS signal so that valid data can be latched in the center of the valid data window despite the fact that the DRAM devices place read data onto the data bus with the same phase relative to the DQS signal.”); EX2013, ¶¶22-

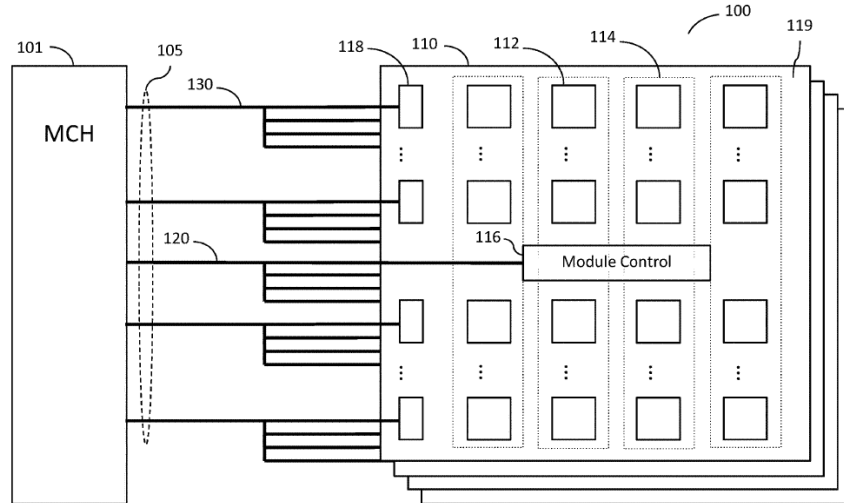
23; EX1019, 34; EX2015, 13. The differences between read and write timing are illustrated below in Figure 9.36.



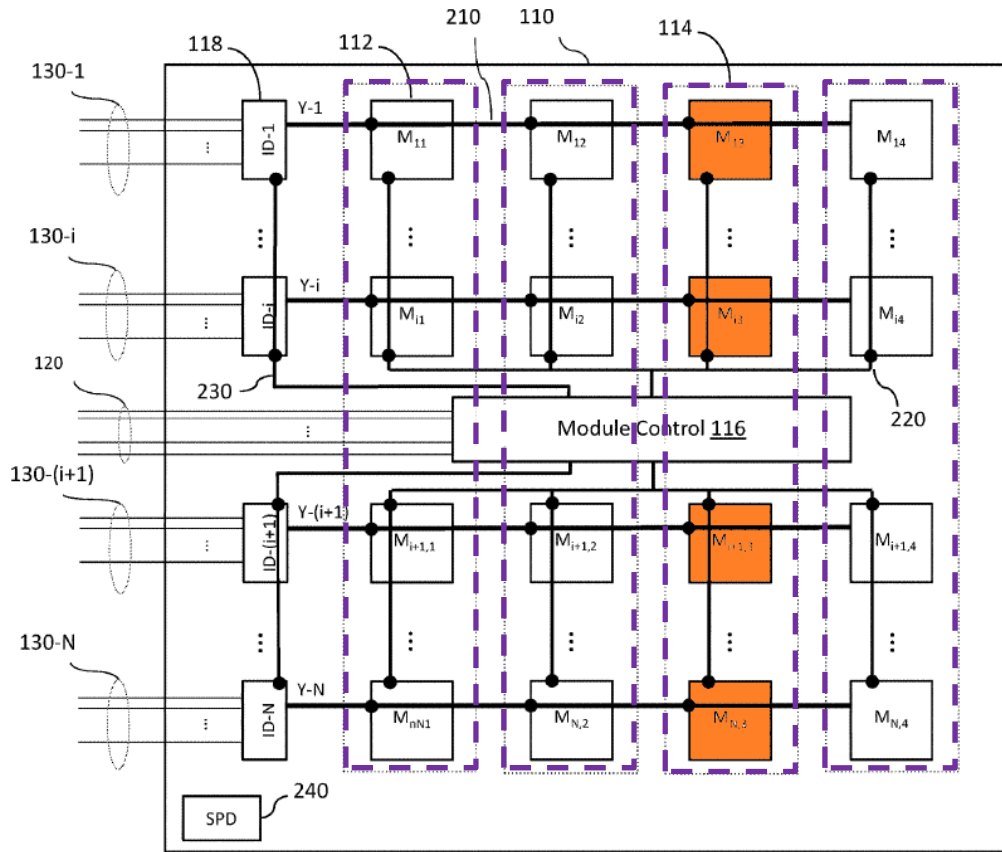
EX1021, 405. This is also reflected directly in the DDR standard. *see also* EX2014, 13 (strobe signal is “[e]dge-aligned with read data, centered in write data”); Figure 31, page 33 (showing edge-aligned DQ and DQS for read command and quarter-clock cycle (90 degree) offset DQ and DQS (center-aligned) for write comment). EX2013, ¶¶24-25.

III. THE '608 PATENT

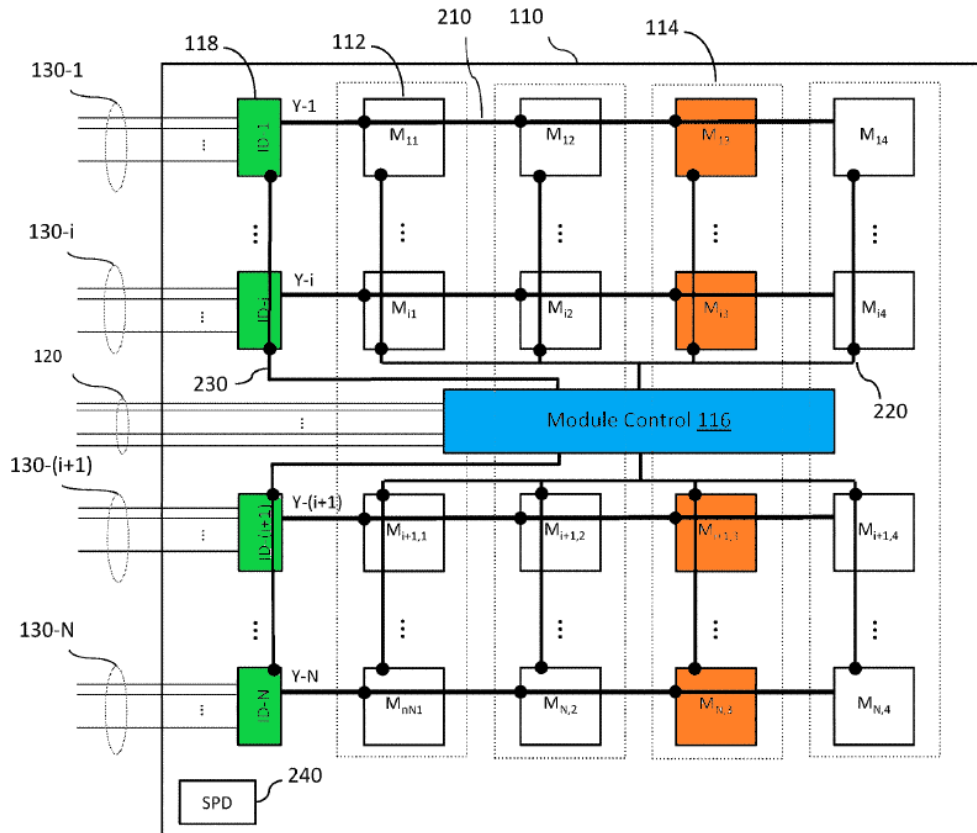
The '608 patent generally relates to memory systems 100 which comprise a memory controller (MCH) 101 and memory modules 110 coupled to the MCH 101 by a memory bus 105. EX1001, 4:20-22.

**FIG. 1**

The memory bus 105 includes control/address (C/A) signal lines 120 and data strobe signal lines 130. *See id.*, 4:23-25. As shown with reference to FIG. 2A below, each memory module 110 includes a plurality of memory devices 112 (highlighted in orange) organized in a plurality of ranks 114 (highlighted in dashed purple line). *See id.*, 4:25-27; EX2013, ¶¶26-27.

**FIG. 2A**

Each memory module 110 includes a module control device 116 (highlighted in blue below) and a plurality of buffers 118 (also referred to as “isolation devices”) (highlighted in green below). EX1001, 4:27-32.



- 10 -

Each buffer (isolation devices 118) includes a command processing circuit that decodes received module control signals and module clock signal and controls a data path in the buffer in accordance with the module control signals and the module clock signal. *See id.*, cl. 1 (19:45-49); 12:3-19. The data path for each data signal line includes a tristate buffer controlled by the command processing circuit. *See id.*, cl. 1 (19:49-51); 12:19-26.

The buffer circuits 118 include a delay control circuit 650 that determines an amount of delay to apply to signal(s) through the data path after receiving one of the module control signals and a DQ signal. *See id.*, 10:11-21, 11:8-13, 12:14-37, 15:23-26, 16:10-12; EX2013, ¶32. The '608 patent describes the need to overcome limitations of prior art memory modules and the complications posed by increasing memory density and memory speed on the memory module. EX2013, ¶33. For example, the specification describes the limitations of conventional read and write leveling mechanisms that were known in the prior art and used to compensate for unbalanced wire lengths. EX1001, 2:28-35, 15:21-22. The '608 patent describes mechanisms for buffering command, address, and data via a module control device, buffer circuits, and memory devices located on the memory module, collectively resulting in modules with higher capacity and higher performance. EX2013, ¶34.

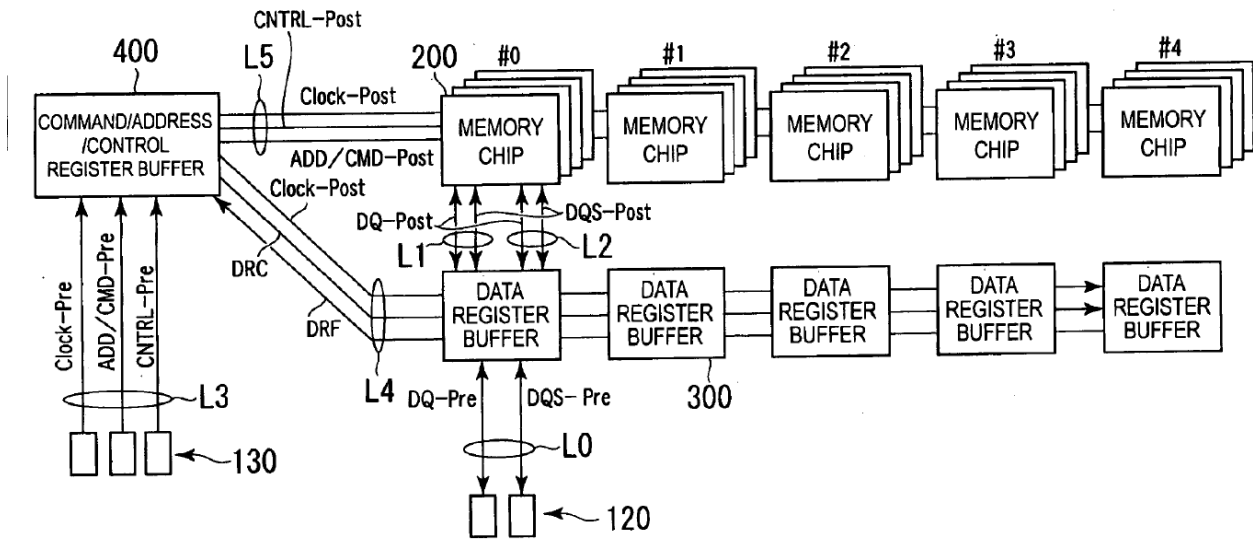


FIG. 7

The data connectors 120 and each of the data register buffers 300 are connected via data/strobe signal lines L0, and each of the data register buffers 300 and the corresponding memory chips 200 are connected to each other via data/strobe signals lines L1 or L2. *See id.* Data/strobe signal lines L0-L2, each consisting of one DQS and multiple DQ lines, transfer data and data strobe signals between the memory controller, data register buffers 300 and memory chips 200, respectively. *See id.*, [0048]; EX2013, ¶¶40-45.

2. Hiraishi's Read/Write Leveling Functions

Hiraishi performs two types of read and write leveling adjustments (S4 and S5) during initialization, before any read/write operation begins. EX1005, [0104]; EX2012, 57:3-10, 67:5-15; EX1005, Fig. 13 (S4 and S5).

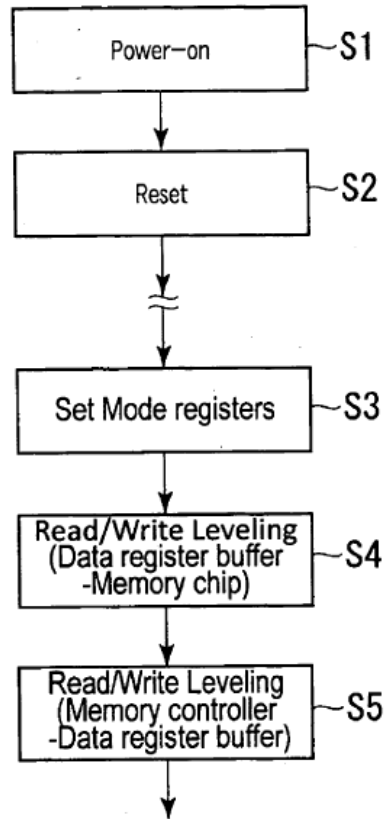
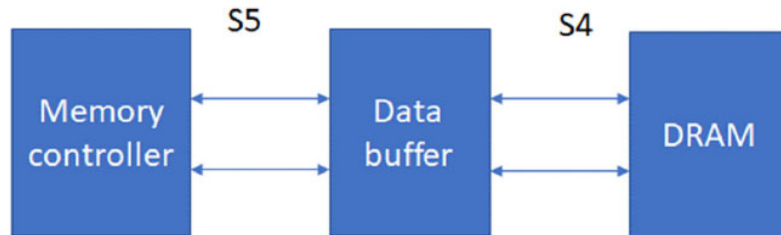


FIG.13

FIG. 13 is a flowchart for explaining the initialization of the memory module 100 at the time of activation. *See id.*, [0138]. The Petition cites to Hiraishi's S4 leveling for Ground 1, which accounts for flight time between the memory chips 200 and the data register buffers 300. *See id.*, [0142]-[0151]; EX2013, ¶¶46-47.

Hiraishi also describes S5 read leveling and write leveling functions to account for the flight time between the memory controller 12 and the data register buffers 300, at issue under Ground 2. EX1005, [0152]-[0161]; EX2013, ¶¶48, 58.



Hiraishi's S4 and S5 leveling are performed by different circuitry. S4 leveling is performed by write leveling circuit 322 and read leveling circuit 323 in the data register buffer 300. See EX1005, Fig. 5 (annotated and reproduced below).

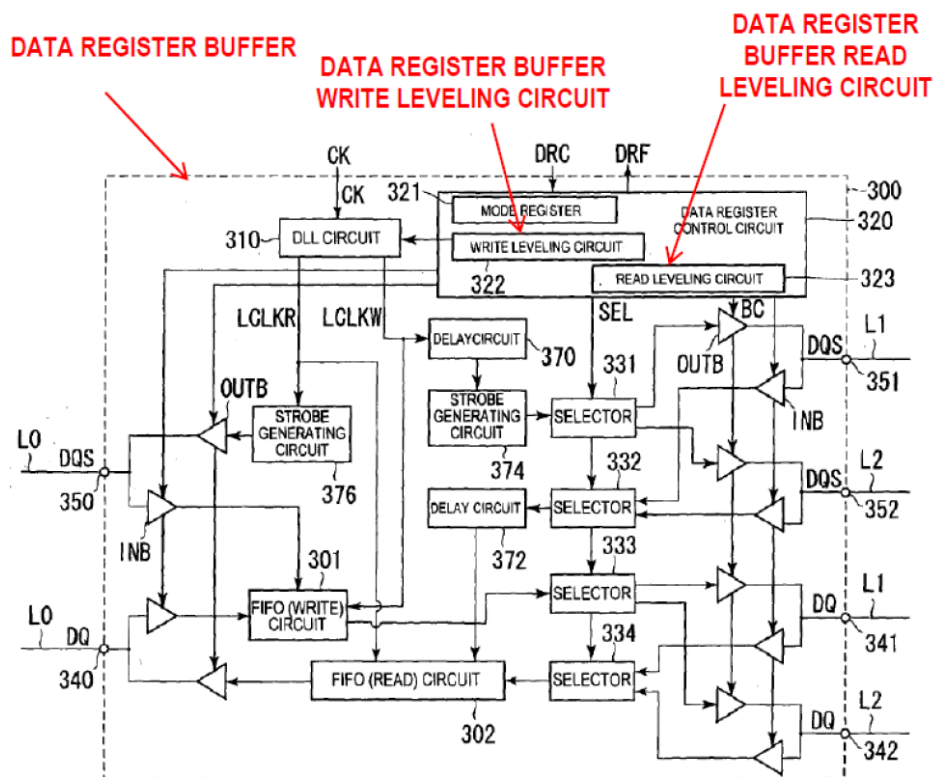


FIG.5

S5 leveling, in contrast, is performed by write leveling circuit 12a and read leveling circuit 12b in the memory controller 12. *See id.*, Fig. 2 (annotated and reproduced below), [0152]; EX2013, ¶49.

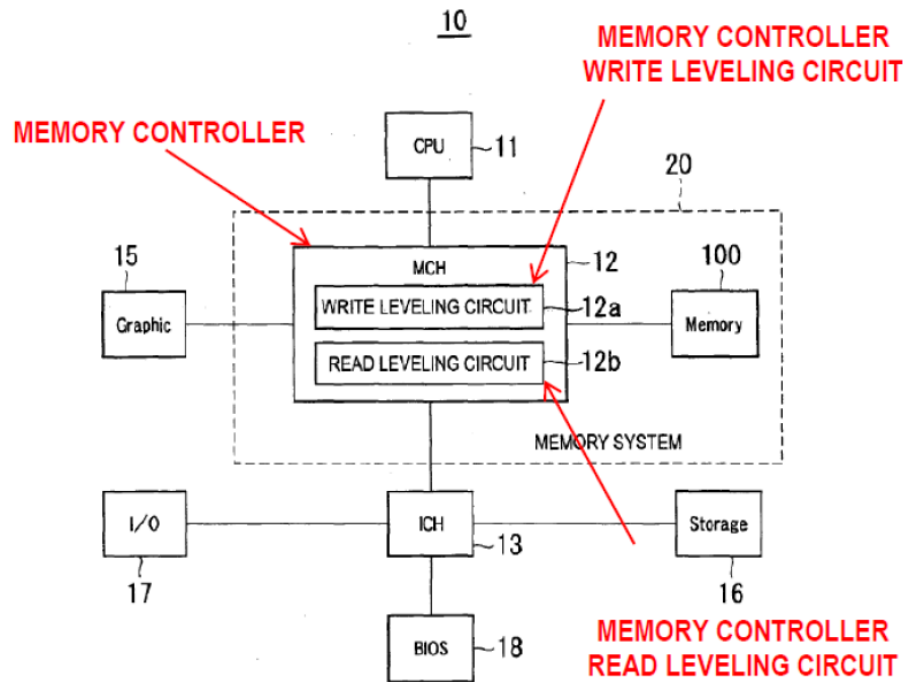


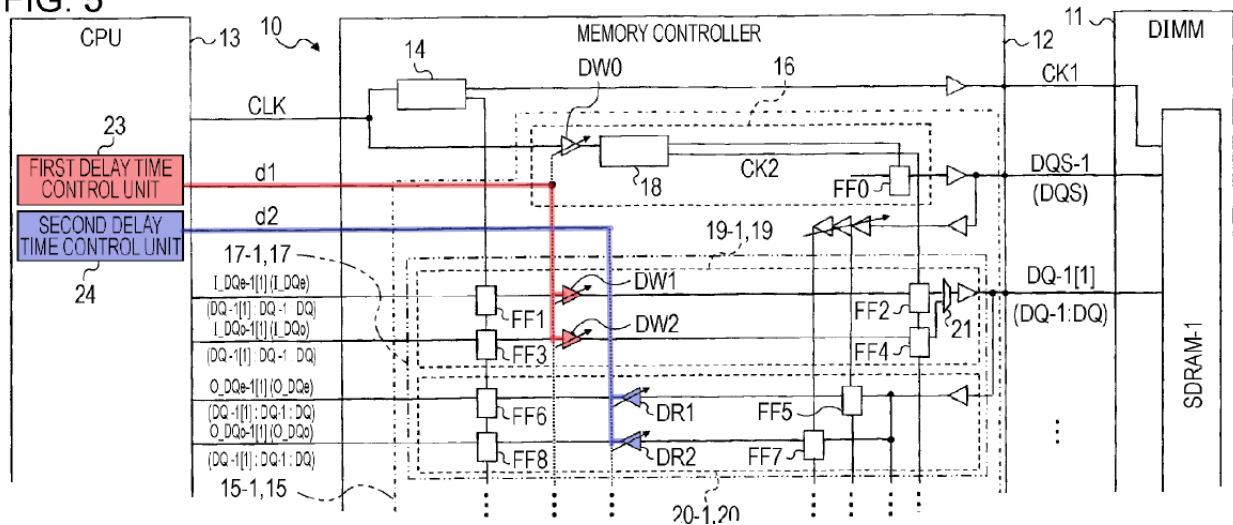
FIG.2

B. Tokuhito (EX1006)

Tokuhito discloses a fly-by topology for command/address/clock wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11. EX1006, 5:24-30. Tokuhito purports to describe an improved *off-module* memory controller that incorporates known write leveling mechanisms, as disclosed in the JEDEC DDR3 SDRAM Standard, JESD79-3. *See id.*, 1:22-32; 2:10-18; 2:46-49; 2:54-59; EX2013, ¶64. Tokuhito's memory controller performs a write

leveling operation to account for different flight times to different memory devices and to delay the respective data strobe signals accordingly so that strobe signals and clock signal from the system memory controller will arrive at respective SDRAMs on the memory module at substantially the same time. EX1006, 2:39-45, 12:59-63; EX2013, ¶65. These delays are determined by, and carried out under the control of, a first delay time control unit 23 (highlighted in red below) and second delay time control unit 24 (highlighted in blue below) *located in the computer's CPU 13*. See e.g., EX1006, FIGs. 4-6, 8, 9, 12-15. The CPU's first and second delay time control units 23 and 24 output control signals on dedicated control signal lines d1 and d2 to control variable delay circuits DW and DR in the memory controller 12. EX2013, ¶¶66-67.

FIG. 5



VI. THE CHALLENGED CLAIMS ARE NOT OBVIOUS IN LIGHT OF GROUND 1 REFERENCES

The recited claims each require a “data path” in a buffer circuit that “correspond[s] to each data signal line in [a] respective set of data/strobe signal lines” wherein “the data path ... includes ... a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.” The alleged data path identified for Ground 1, however, improperly includes strobe signal lines, as confirmed by Petitioners’ expert, Dr. Wedig. EX2012, 40:11-16, 40:21-41:1. Relatedly, the delay circuit identified by Petitioner encompasses circuits that are indisputably *not* on the data lines (*i.e.*, not “include[d] by the data path”) for delaying signals that are *not* “through the data path.” *Contra*, EX1001, 1[f]. Simply put, the Petition fails to map the claim limitations as recited by the claims. Moreover, for element 1[f], Petitioners relies on “re-timing” based allegedly on results from read/write leveling. Pet., 45-46, 47, 51. However, any change in read/write latency during re-timing is unrelated to the read/writing leveling and the amount is not determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 in response to DRC as contended (Pet., 47, 51) because the buffer simply increases the latency by one clock cycle to compensate for the different flight times. *See* §§VI.C-VI.D. For these and reasons below, Ground 1 fails.

A. The Recited “Data Path” Does Not Include Strobe Signal Lines

Each claimed “data path” “correspond[s] to each data signal line in the respective set of data/strobe signal lines.” EX1001, 19:43-45. The Board invited the parties to address whether a POSA “would view the portions of Hiraishi that Petitioner relies upon [as] teach[ing] the ‘data path’ as claimed.” ID, 30-31.

A POSA would not because Petitioner’s theory requires that sections of Hiraishi’s DQS strobe signal line(s)—instead of just data (DQ) signal lines—be included in the “data path.” Pet., 33-34, 36, 38, 43-47, 50-51; ID 30 (“Petitioner has identified portions of Hiraishi that includes portions of data and data strobe signal lines as part of the claimed ‘data path’....”). Dr. Wedig confirmed as much.

Q. What is the data path through Hiraishi's buffer shown in Figure 5?

A. So it’s at least all of the orange lines both solid and hashed shown in the two depictions of Figure 5 on page 98 of my declaration.

EX2012, 40:11-16 (objection omitted).

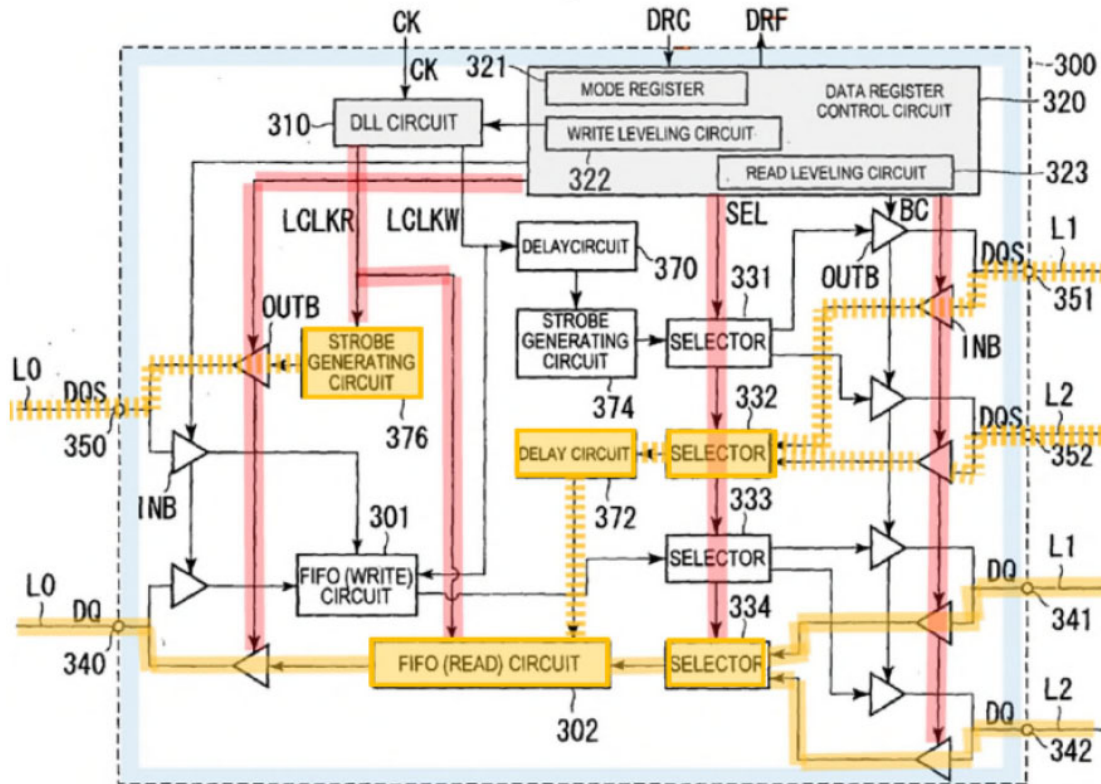


FIG.5

EX1003, p. 98; EX2012, 40:21-41:1. But the claims clearly exclude strobe signals lines from the recited “data path,” which “correspond[s] to *each data signal line* in the respective set of data/strobe signal lines.” EX1001, 19:43-45. Hence, a POSITA would not view the portions of Hiraishi that Petitioner relies upon—which include strobe signal lines—as teaching the claimed “data path.” EX2013, ¶¶70-78.¹ The patent distinguishes between data signal lines and strobe signal lines as well as

¹ Further, Hiraishi’s L1/L2 each comprise 8 data signal lines for one byte of data and are therefore not a data path corresponding “to each data signal line.” Hiraishi, [0053].

between data paths corresponding to respective data signal carrying data signals and strobe paths carrying strobe signals.

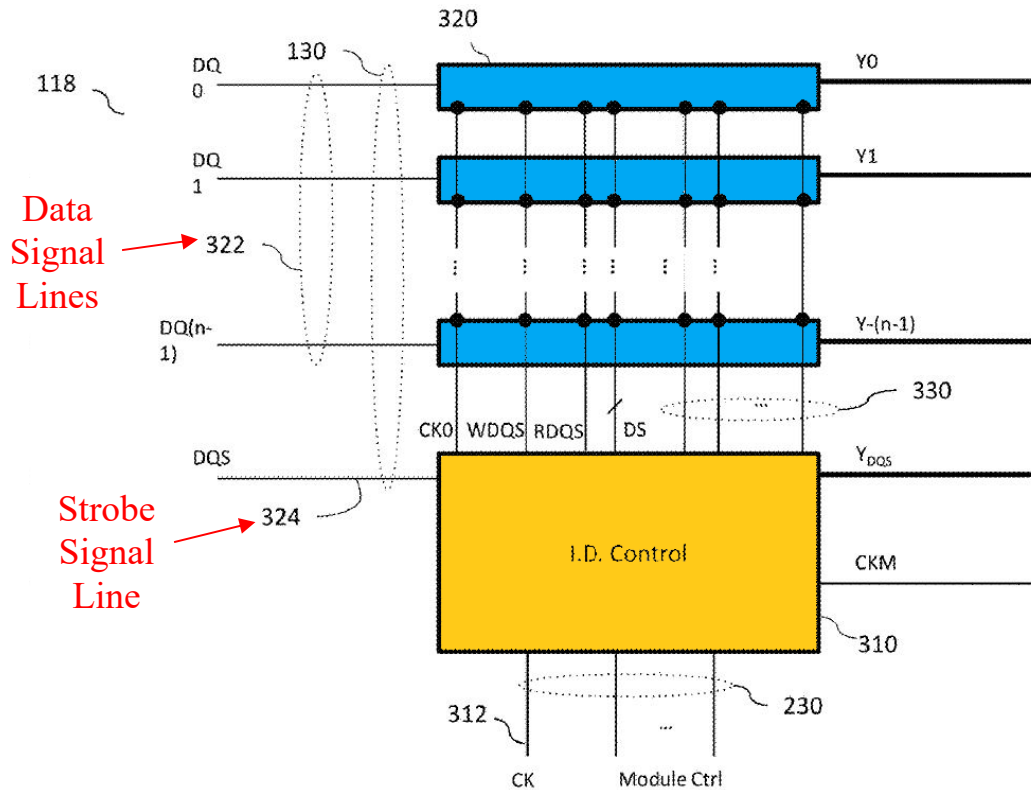


FIG. 3

For example, as shown in FIG. 3 of an isolation device (aka buffer circuit 118), “each group of signal lines 130 include a set of n *data (DQ) signal lines 322* each for transmitting one of a set of data signals $DQ_0, DQ_1, \dots, DQ_{n-1}$, and at least one *strobe (DQS) signal line 324* for transmitting at least one strobe signal DQS.” EX1001, 10:31-35. The '608 patent also distinguishes between strobe paths (associated with strobe signal lines (e.g., 324) and data paths (associated with data signal lines (e.g., 322) and discloses using separate circuitry for routing along such

paths. For example, FIG. 15 below is a DQS routing circuit 620 for DQS 324 to be provided between a first DQS pin 1501 and one of a second DQS pin 1502A or third DQS pin 1502B. *See id.*, 16:47-17:22.

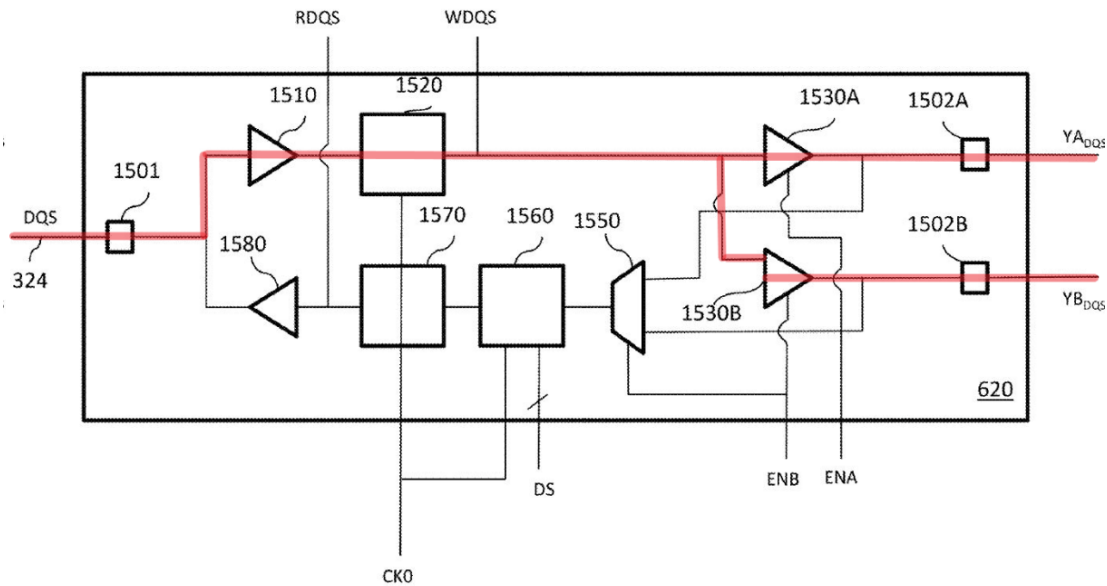


FIG. 15

As annotated by the red lines above, there is a “***first write strobe path***” coupled between the first DQS pin 1501 and the second DQS pin 1502A and a ***second write strobe path*** coupled between the first DQS pin 1501 and the third DQS pin 1502B.” *Id.*, 16:53-57; 16:57-17:7 (describing components along first and second write strobe paths for processing DQS signals); 17:8-22 (describing first and second ***read strobe paths*** and related components). Conversely, FIG. 16 below is a DQ routing circuit

320 for DQ signal 130 to be provided between a first DQ pin 1601 and one of a second DQ pin 1602A or third DQ pin 1602B. *See id.*, 17:23-60.

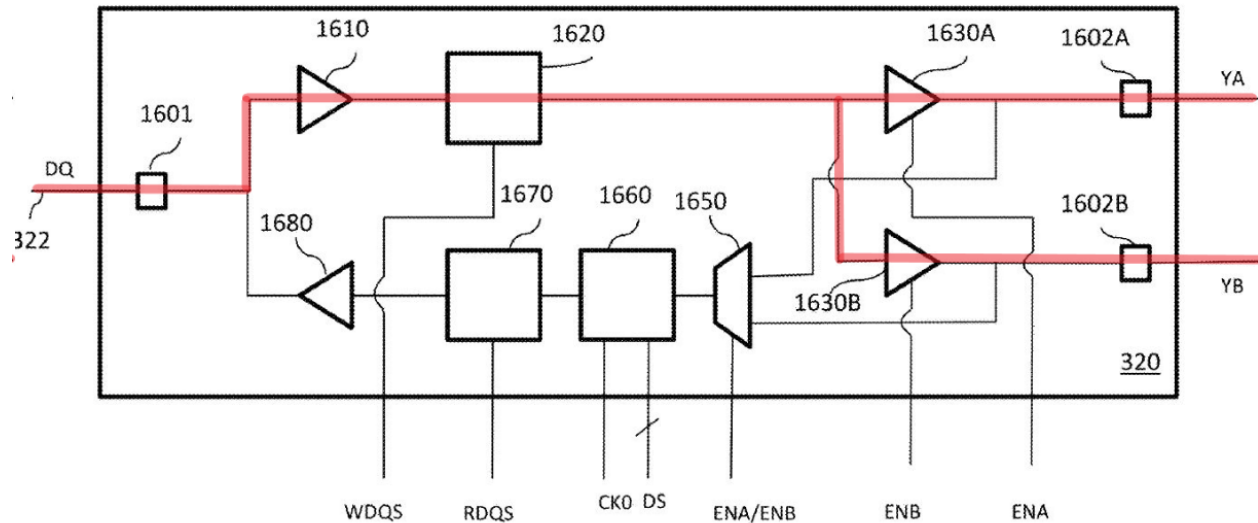


FIG. 16

As illustrated by the redlines in FIG. 16 above, there is a “**first write data path**” coupled between the first DQ pin 1601 and the second DQ pin 1602A and a **second write data path** coupled between the first DQ pin 1601 and the third DQ pin 1602B.” *Id.*, 17:29-33; 17:33-47 (describing components along first and second write data paths for processing DQ signals); 17:48-60 (describing first and second **read data paths** and related components) (*see* FIG. 16 *infra* §VI.B.1 annotated to show read path).

Thus, the specification makes clear that strobe signal lines form a strobe path and data signal lines form a data path, as is also reflect in the claim language. As

such, each recited “data path” corresponds to a data signal line carrying data signals, not to a strobe signal lines carrying strobe signals. EX2013, ¶¶70-78. Thus, any reliance by the Petitioner on a “data path” comprising segments of Hiraishi’s strobe signal line(s) fails as a matter of fact.

Butt does not cure the deficiency because (1) Butt is only used to support Petitioner’s interpretation of Hiraishi; and (2) Butt too distinguishes between signal lines that carry DQ data and signal lines that carry DQS strobe signals. *See below* (showing solid orange lines for DQ data signals and cross-hatched lines for DQS strobe signals).

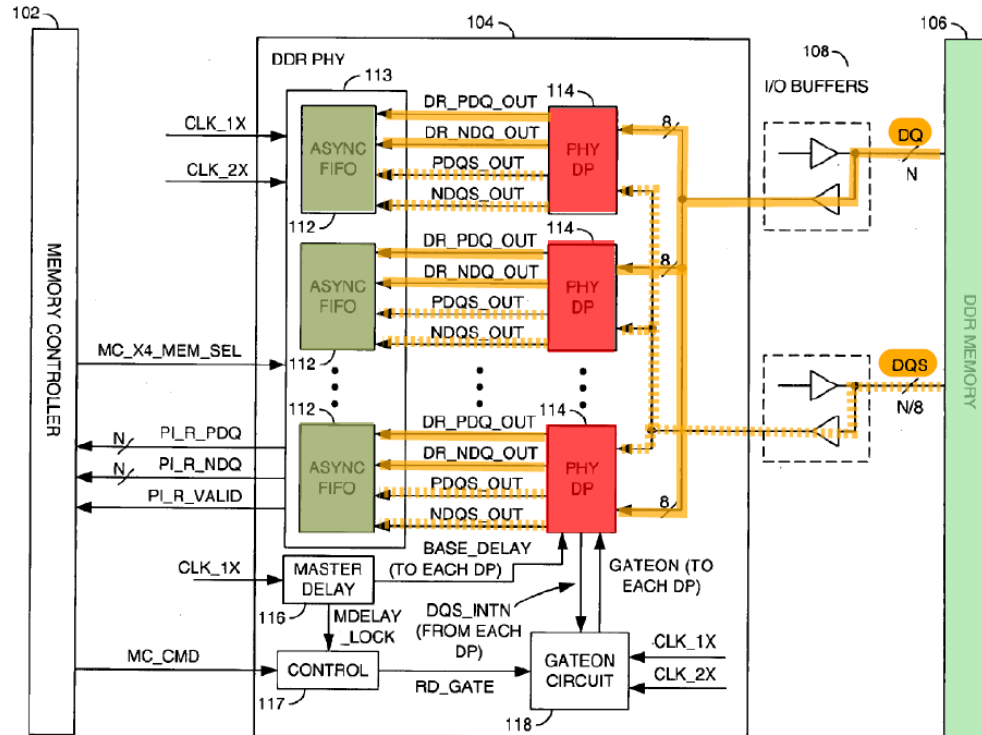


FIG. 2

Pet., 35 (citing EX1029, Fig. 2).

It does not matter how Butt defines its “datapath” because the term “data path” is to be understood in light of the ‘608 patent and not according to Butt. As explained above, the claim language restricts a “data path” to one corresponding to a “data signal line” in a respective “set of data/strobe signal lines,” consistent with the specification. EX1001, 19:43-45. Nothing in Butt suggests that data signal lines include strobe signal lines. In contrast, Butt maintains separate data signal lines for DQ and strobe signal lines for DQS. See EX1029, FIG. 3A (showing separate DQ lines (yellow) and DQS lines (turquoise) in “datapaths 114”); EX2013, ¶¶79-81.

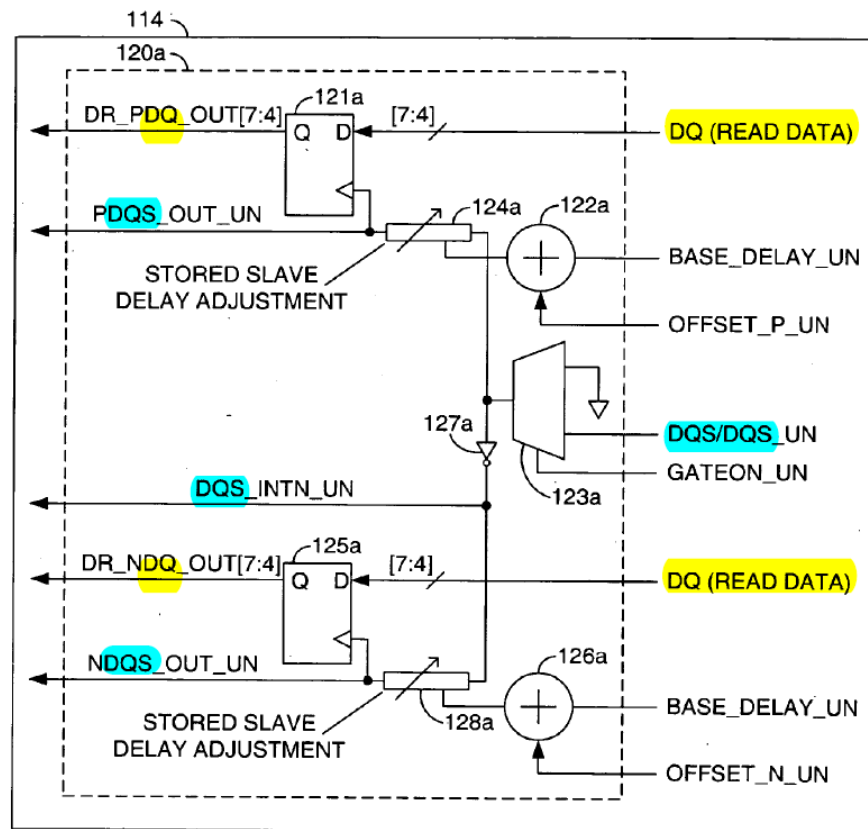


FIG. 3A

Nor is there any evidence that a data signal travels over a strobe signal line, or that a strobe signal travels over a data signal line such that strobe signal lines may be regarded as data signal lines and vice versa. Dr. Wedig so confirmed. EX2012, 52:8-17 (testifying that neither Hiraishi nor Butt transmits strobe signals over data signal lines); 54:3-7 (“Q. Do strobe signals ever travel over DQ signal lines? A. No, not in -- not in normal traditional memory module designs.”) (objection omitted).

B. Petitioner Fails to Identify a Delay Circuit in the “Data Path”

1. The Delayed Signal Must Be “Through the Data Path” And Delayed by a “Delay Circuit” in the “Data Path”

Claim 1 further recites that “*the data path* corresponding to the each data signal line *includes ... a delay circuit* configured to *delay a signal through the data path*” The plain language makes clear that the delayed signal is through a data path, which corresponds to a data signal line carrying data signals as described above. EX2013, ¶82. This delay is effected by a delay circuit in the data path. The disclosure of the ’608 patent is in accord.

For example, in the DQ routing circuit 320 of the ’608 patent annotated below, there exist write and read data paths coupled between the first DQ pin 1601, on the one side, and either of the second and third DQ pins 1602A/B, on the other side. See EX1001, 17:29-60. As also shown above, a delay circuit 1660 [green] is in a read data path [red], e.g., a read data path between first DQ pin 1601 and second/third

DQ pins 1602A/B, and is described in the specification as delaying a “selected read data signal ... by an amount controlled by the delay signal DS.” *Id.*, 17:54-55.

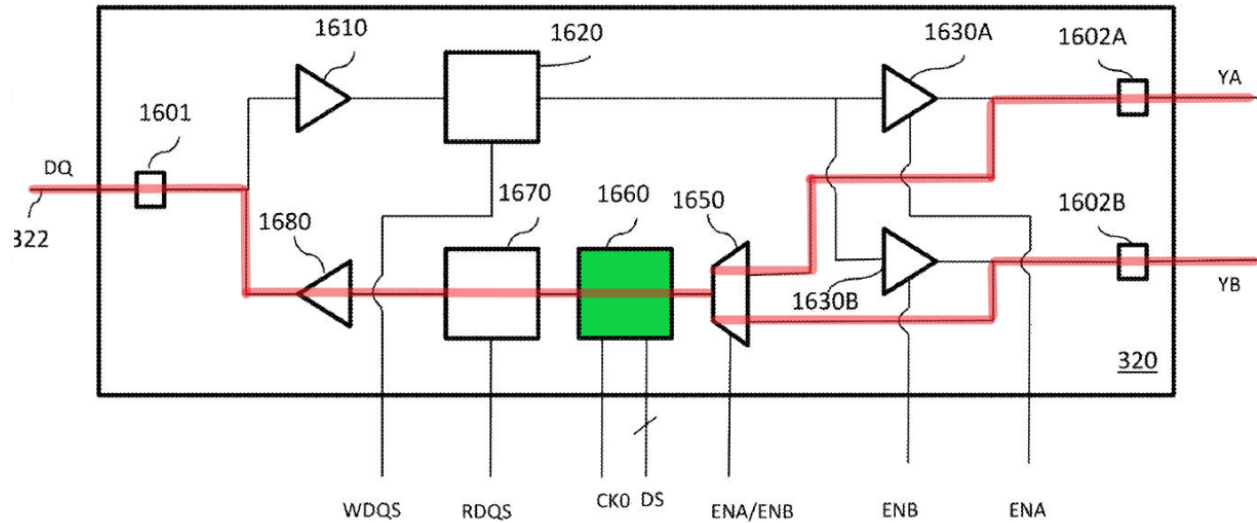


FIG. 16

Thus, consistent with the claims, a POSA would understand the recited “delay circuit” resides in the corresponding buffer circuit’s data path, and not in a non-data path (e.g., a strobe path or clock signal path). EX2013, ¶82. As detailed below, this defect is fatal to the challenge because the Petition expressly maps the recited “delay circuit” to components on Hiraishi’s strobe and clock signal lines, and identifies signals through these non-DQ signal lines as “signal(s) through the data path.”

Butt does not cure the deficiency because for Ground 1, only the disclosure of Hiraishi is relied on to allege that the limitations are satisfied by the prior art. EX2013, ¶83. In particular, Butt’s sampling optimization process is not relied on to satisfy any claim limitation (the claims do not recite a sampling operation). Instead,

as the Board recognized, “Hiraishi is the main reference relied upon for the teachings of the claim limitations, and Butt is used to provide further explanations or interpretations of the teachings of Hiraishi and/or to explain the knowledge of one of ordinary skill in the art.” ID, 11-12.

2. The Petitioner Has Not Established That Hiraishi Discloses the Recited “Delay Circuit” or Delaying a “Signal through the Data Path”

For Element 1[f], Petitioner expressly identifies the *combination* of Hiraishi’s “DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376.” Pet. 39; 47 (“Ground 1’s delay circuit for write operations includes the *Write FIFO 301* delaying the write data signal, *delay circuit 370* delaying the LCLKW signal, *the strobe generating circuit 374* generating a delayed strobe signal that is in synch with the delayed write data, and *DLL circuit 310* generating the LCLKW signal for timing the output of the delayed data and strobe signals.”); 51 (listing components of the alleged “delay circuit” for read operations).

Dr. Wedig confirmed that his analysis is based on this combination, and not just a part of the identified components.² EX2012, 17:23-18:5 (“I believe that all of

² That is, even if the Write FIFO 301 or read FIFO 302 is on a data path, the Petitioner does not (and cannot) rely on that alone to satisfy the claimed functionality

those different parts make up the delay circuit, so I guess yes, *it's a combination of those*. I mean, *they all work together to implement the delay circuit.*"); 20:10-16; EX2013, ¶85.

Petitioners had to rely on this *combination* of components in order to piece together a “circuit” which it can then allege performs the functions of the claimed “delay circuit,” although even then the “combination” fails to do so as described below. To prevail, Petitioner must establish that (1) its combined “delay circuit” is in the data path, (2) that a signal being delayed is “through the data path,” and (3) that the delay is “in response to at least one of the module control signals.” It cannot do so.

**(a) The Alleged “Delay Circuit” for Write Operations
Does Not Satisfy the Limitation**

(i) The Delay Circuit 370

One component of Petitioner’s alleged “delay circuit” is Hiraishi’s delay circuit 370 that allegedly delays the LCLKW local clock signal. Pet., 39, 47. This does not satisfy Element 1[f] because (1) any delay the delay circuit 370 imparts is not “in response to at least one of the module control signals,” and (2) the delay circuit 370 is not in a data path and does not “delay a signal through the data path.”

of the “delay circuit” of Element 1[f]. See §§VI.B.2(a)(iv), VI.B.2(b)(iv), VI.C-VI.D.

First, a POSA would understand that the delay imparted to LCLKW by delay circuit 370 is not in response to the DRC signals (the alleged “module control signals”) received by Hiraishi’s data buffer because it is a predetermined fixed delay of about 90 degrees (or ¼ clock cycle) for obtaining a DQS from strobe generating circuit 374 that is center-aligned with the write data on data lines L1 or L2 so that the write data can be correctly sampled by the memory chips 200. EX2013, ¶¶88-89. The delay circuit 370 is not delaying the LCLKW “in response to at least one of the module control signals” also because the only input to delay circuit 370 is LCLKW. *Id.*; EX1005, FIG. 5, [0091]. That is, the delay circuit 370 does not receive any control signals at all. *Id.* Moreover, the delay circuit 370 does not participate in Hiraishi’s S-4 write leveling operation or operate based on the results from the leveling operation since it only applies a fixed offset. EX2013, ¶¶88-89.

If anything, the delay circuit 370 causes the fixed delay in response to the local clock LCLKW, which is based on the system clock CK that Petitioner identifies as a module clock signal. Pet., 32-33, 37-38; EX2013, ¶90. The claims differentiate between the “module control signals” and the separately-recited “module clock signal,” and Petitioner does not suggest that the “module control signals” (mapped to DRC) can be a clock signal. EX1003, ¶85 (“[A] Skilled Artisan would have understood that the claim term ‘module control signals’ includes signals that the module controller ... derived from the ‘memory command signals’ and provided to

buffer circuits to control their operations.”)(citing EX1001, 4:27-30); *see also* EX1001, 3:47-50 (stating that the module control signals “are transmitted by the module control device to the buffer circuits via module control signal lines”); 5:43-51.

Second, Dr. Wedig confirmed that the delay circuit 370 delays the local clock signal LCLKW. EX2012, 64:24-66:5. And, the LCLKW is not “a signal through the data path,” nor is it even identified as such by Petitioner. For example, for a write operation in Hiraishi, the Petition defines the “data path” in orange below. “Fig.5 (below, showing write data paths, orange).” Pet., 46.

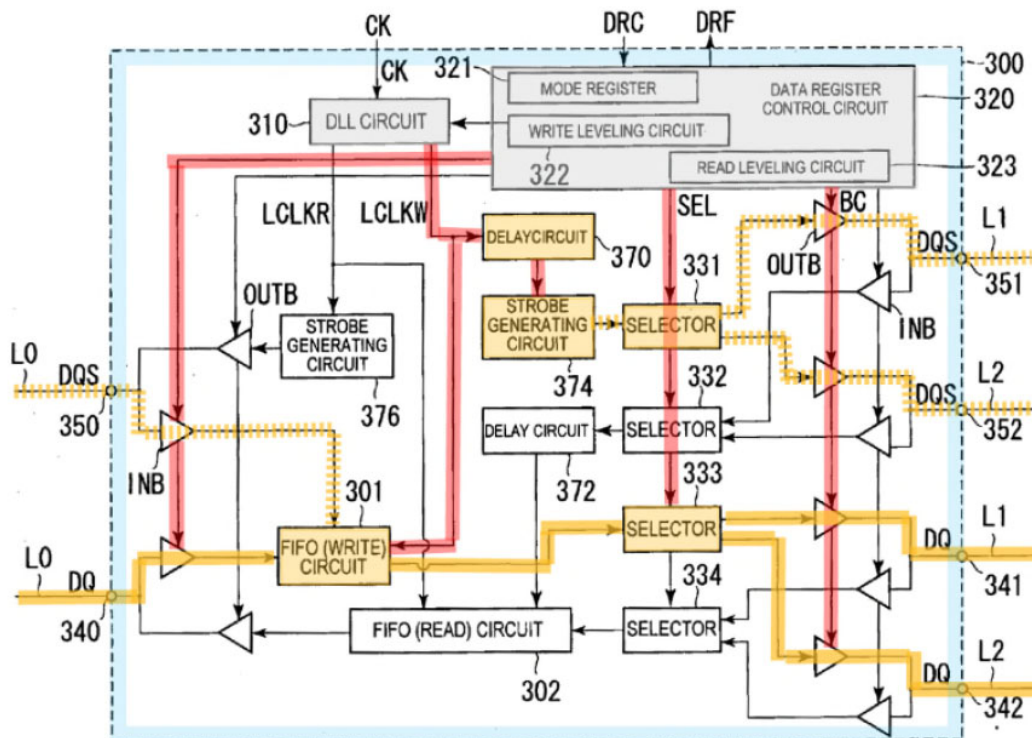


FIG.5

Pet., 47. As Petitioner’s own annotation shows, the LCLKW travels along a red line and is not through what Petitioners contend is the data path (orange). And certainly, it does not go through any of the DQ lines.

Q. How about the red -- I guess red lines? Are those part of the data path?

A. No, they're not. They're not part of the data path.

...

Q. How about the CLK signals LCLKR and LCLKW are those part of the data path through Hiraishi's data buffer?

A. No. They're not.

EX2012, 41:2-5, 42:1-4, 41:6-25.

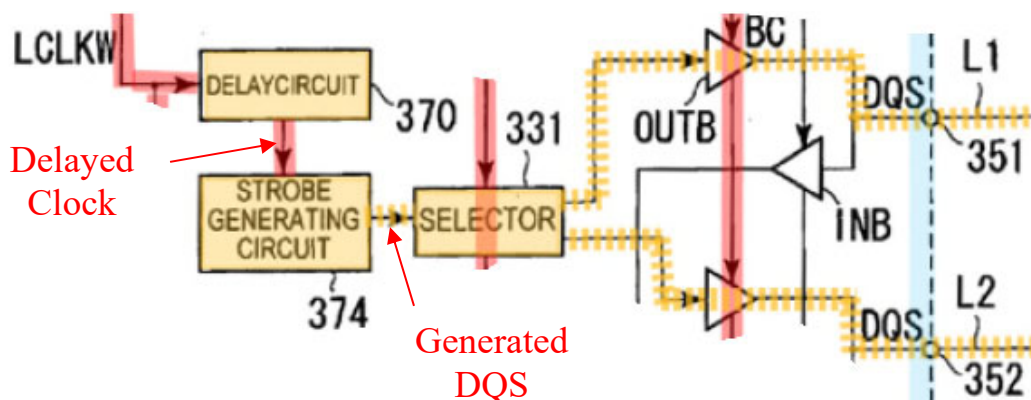
Thus, even under Petitioners’ theory, the local clock signal (LCLKW) is not “through” the claimed “data path” as required by the claims. *See supra*, §VI.A; EX2013, ¶91. This defect is dispositive as to Ground 1 because the claims require that the “delay circuit” (which is alleged to include the delay circuit 370) be in the data path and that the signal being delayed be “through the data path.”

(ii) The Strobe Generating Circuit 374

Another component of Petitioner’s alleged “delay circuit” is Hiraishi’s strobe generating circuit 374. Pet., 39, 47. However, Hiraishi’s strobe generating circuit 374 (1) is not in a data path and does not delay any signal, least of all a signal through a data path, and (2) does not operate “in response to at least one of the module control signals.”

First, as Hiraishi explains, the “strobe generating circuit 374 **generates a data strobe signal DQS** to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.” EX1005, [0084]. Thus, circuit 374 generates a new signal, as opposed to delaying a signal. A POSA would understand that delaying a signal means that a same signal is inputted to and outputted from a delay circuit but with the timing of the output signal adjusted compared to a previous timing of the input. EX2013, ¶93. A newly-generated signal, however, does not have a previous timing (since it did not exist), and therefore cannot be delayed. As Dr. Mangione-Smith confirms, the creation of a signal does not delay the signal. EX2013, ¶93.

Furthermore, neither the input to nor output from the strobe generating circuit 374 involve a signal “through the data path.” Instead, the strobe generating circuit 374 receives only a 90-degree delayed clock signal from circuit 370, and provides a strobe signal to selector 331, neither of which is a signal “through [a] data path” that corresponds to a “data [DQ] signal line in the respective set of data [DQ]/strobe [DQS] signal lines,” as required by the claims. *See supra*, §VI.A; EX2013, ¶94.



This fact is dispositive because the claims require that the “delay circuit” (alleged to include the strobe generating circuit 374) be on the data path and that the signal being delayed be “through the data path.”

Second, the strobe generating circuit 374 generates the new DQS signal *in response to* an internal *clock* LCLKW (i.e., “in synchronization with an internal clock LCLKW”). EX2013, ¶95. As noted above, the claims distinguishes a “module control signals” from a “module clock signal.” See Pet., 32, 37-38; see also §§III, VI.B.2(a)(i). Neither the Petition nor Dr. Wedig’s declaration contends that a clock signal is a module control signal.

(iii) The DLL Circuit 310

The Petition also expressly relies on Hiraishi’s DLL 310 as being part of the recited “delay circuit.” Pet., 39, 47. However, neither the Petition nor Dr. Wedig’s testimony establish that the DLL circuit 310 is in the data path or delays “a signal through the data path.” For example, the Petition purports to show the alleged “write

data path” in orange in the annotated diagram below, but omits the DLL circuit 310 from the “orange” path. Pet., 34.

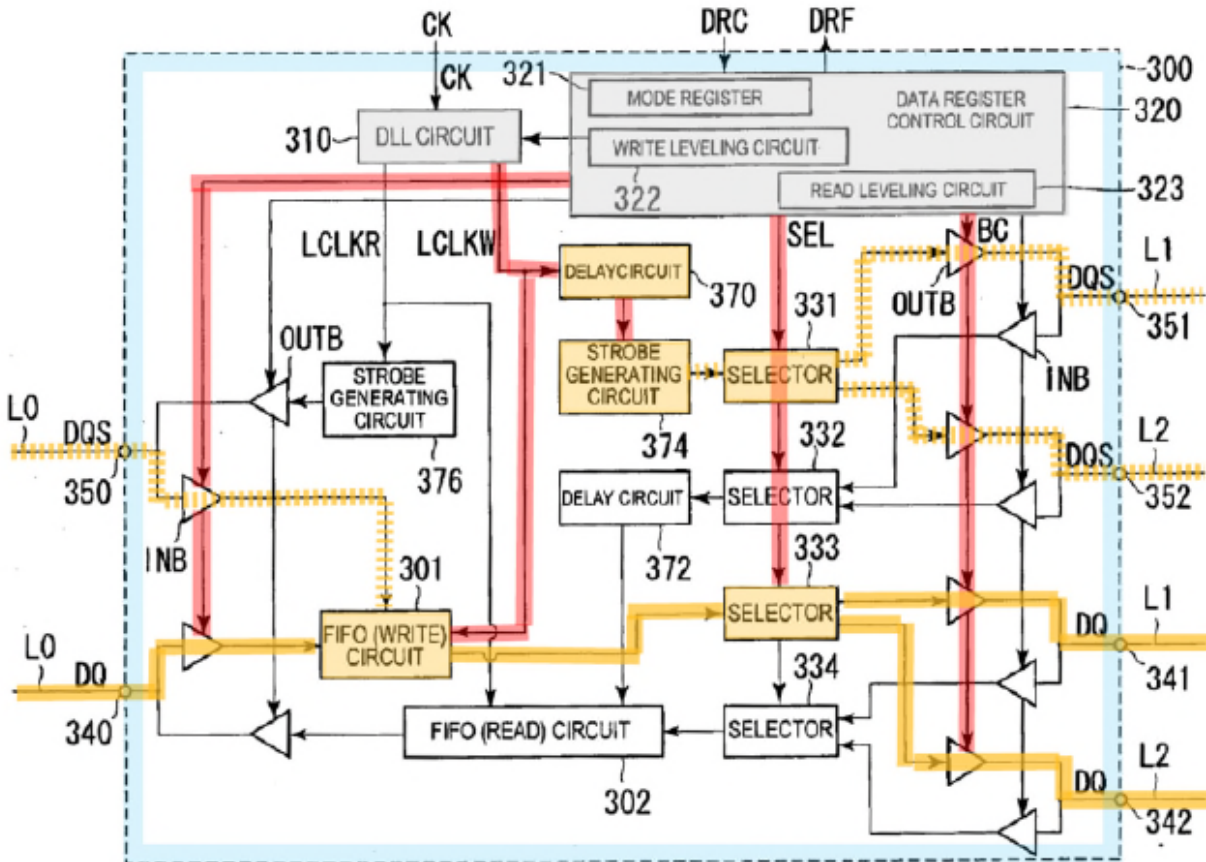


FIG.5

Pet., 46-47. Dr. Wedig confirmed that the DLL is **not** in the data path. EX2012 42:24-43:1 (“Q. Is the DLL circuit 310 part of the data path through Hiraishi's data buffer? A. No, it's not.”); EX2013, ¶¶96-97.

Nor is the CK signal inputted to DLL circuit or the LCLKW output from the DLL circuit “a signal through the data path,” even under Petitioner’s theory. EX2013, ¶98. In Petitioner’s annotated Fig. 5 from Hiraishi above, neither CK nor

LCLKW are identified in orange. This is confirmed by Dr. Wedig. *See* EX2012, 41:2-25 (red lines not part of data path), 42:1-4 (LCLKW not part of data path).

Indeed, a POSA would not understand CK, the DLL 310, or LCLKW as being on or through a “data path” that “correspond[s] to each data signal line in the respective set of data / strobe signal lines,” as recited in claim 1. EX2013, ¶¶96-99. That a clock signal is not part of the data path is also consistent with the ’608 patent, as described above. *See* EX1001, FIG. 16, 17:23-47; *see supra* §VI.A.

(iv) Write FIFO 301

Petitioner has also not established that Write FIFO 301 delays a signal through the data path “in response to at least one of the module control signals.” Data is sampled in FIFO 301 using the incoming DQS signal from strobe signal line 350, and is clocked out based on the internal clock LCLKW. EX2013, ¶100. Neither the Petition nor Dr. Wedig contend that a DQS signal or a clock signal is a module control signal. They are not. EX2013, ¶¶89-90, 100.

(v) Conclusion

Thus, the Petitioner has not established that the combination of Hiraishi’s (1) Write FIFO 301 (2) delay circuit 370, (3) strobe generating circuit 374, and (4) DLL circuit 310 is a “delay circuit” on a data path that delays “a signal through the data path.”

(b) The Alleged “Delay Circuit” for Read Operations

The Petition and Dr. Wedig rely on a similar combination of Hiraishi's components as being the recited "delay circuit" for read operations. Pet., 51; EX2012, 16:21-17:5; 20:10-16. For reasons similar to those for the write operations, these circuit components do not satisfy the requirements for the claimed "delay circuit" and the associated signals are not "through the data path."

(i) The Delay Circuit 372

Hirasishi's delay circuit 372 for read operations does not impart a delay "in response to at least one of the module control signals," and (2) is not in a data path and does not delay "a signal through the data path."

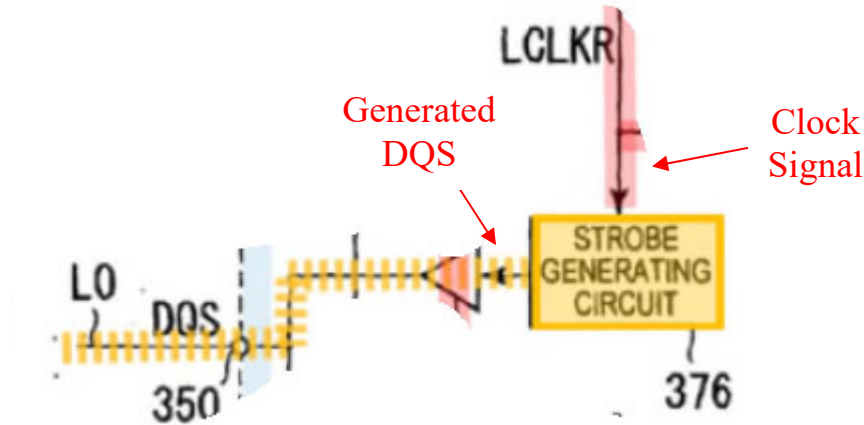
First, the delay circuit 372 applies a fixed delay of "about 90 degrees" to a strobe signal. EX1005, [0091] ("A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372."); EX2012, 22:25-23:2 ("Q. Okay. And for the delay circuit 372, that delays an input strobe signal; right? A. Yes, it does."). A POSA would recognize that this fixed delay relates to center-aligning the DQS signal in order to sample the incoming read data in the FIFO circuit. Dr. Wedig agrees. EX1003, ¶223. Thus, the delay imparted to the incoming DQS by delay circuit 372 is not in response to the DRC signals received by Hiraishi's data buffer (the alleged "module control signals") because it is a predetermined fixed delay that results in the DQS being offset by ~90 degrees from the DQ read data. This is also clear from the fact that the only input to delay circuit 372 is the DQS

signal, which is not a control signal. Moreover, the delay circuit 372 does not participate in Hiraishi's S-4 read leveling operation or operate based on the results from the leveling operation since it only applies a fixed offset. EX2013, ¶103.

Second, the delay circuit 372 is in the strobe path, not the data path, and delays a DQS signal, not a “signal through the data [DQ] path.” EX2013, ¶104. As described above in §VI.A, a POSA would understand that both the claim language and specification are clear that the recited “data path” correspond to data signal lines carrying data signals, not to strobe signal lines carrying strobe signals. Thus, Petitioner's reliance on Hiraishi's delay circuit 372 further dooms the challenge because the claims require that the “delay circuit” (which allegedly includes the delay circuit 372) to be on a data [DQ] path and that the signal being delayed is “through the data path.”

(ii) The Strobe Generating Circuit 376

Petitioner's alleged delay circuit also includes Hiraishi's strobe generating circuit 376. Pet., 39, 51. For the same reasons as for the strobe generating circuit 374, Hiraishi's strobe generating circuit 376 (1) is not in a data path and does not delay any signal, least of “a signal through the data path” and (2) does not operate “in response to at least one of the module control signals” since the input LCLKR signal is a local clock, and not a control signal. *See supra*, §VI.B.2(a)(ii); EX2013, ¶105.



(iii) The DLL Circuit 310

The DLL 310 generating the local read clock signal (LCLKR) does not satisfy Element 1[f] because neither the CK signal provided to the DLL 310 nor the output LCLKR are signals on the “data path,” as described above in §VI.B.2(a)(iii).

(iv) Read FIFO 302

Petitioner has also not established that Read FIFO 302 delays a signal through the data path “in response to at least one of the module control signals.” Data is sampled in FIFO 302 using a delayed DQS signal from delay circuit 372, and is clocked out based on the internal clock. EX2013, ¶107. Neither the Petition nor Dr. Wedig contend that a DQS signal or a clock signal used to operate the FIFO is a module control signal. They are not. EX2013, ¶¶89-90, 107.

(v) Conclusion

Thus, the Petitioner has not established that the combination of Hiraishi’s (1) Read FIFO 302 (2) delay circuit 372, (3) strobe generating circuit 376, and (4) DLL

circuit 310 is a “delay circuit” on a data path that delays a signal through the data path.

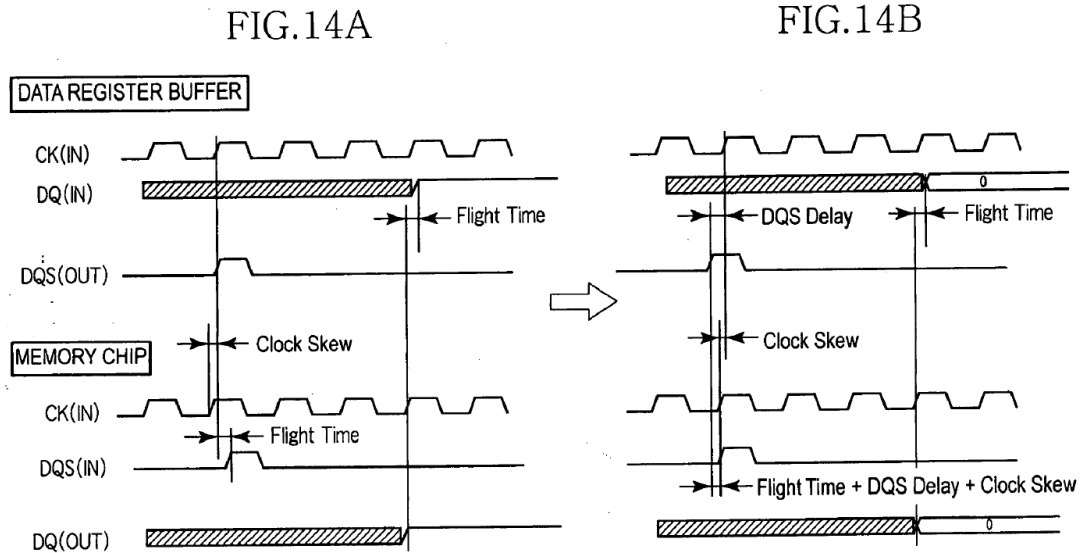
3. Alleged Admissions From Prior Proceeding

Netlist never admitted that Hiraishi’s S4 read leveling discloses the “delay circuit” of Element 1[f]. *Contra* Pet., 51-53. The annotated FIG. 15 from Saito simply illustrates that there exists a flight time difference as to when DQ/DQS signals arrive at the data buffer from different memory devices, and that this flight time difference is addressed by an internal re-timing operation which increases the latency by one clock cycle. That, however, does not satisfy Element 1[f], as explained in Sections VI.2.(a)(iv) and VI.2.(b)(iv) above and Sections VI.C-VI.D below.

C. Hiraishi’s WL Re-timing Is Not Based on the Results of Hiraishi’s S4 Write Leveling and Does Not Satisfy Element 1[f]

The Petition argues that “Hiraishi’s data register buffer 300 determines delays through the data path for read and write operations by respective read and write leveling operations during initialization in response to control signals from the command/address/control register 400, and applies those delays on the data/strobe signals for read and write operations during normal operation in response to read and write commands received from the command/address/control register 400....” Pet., 43-44, 53. The Petition is wrong. Hiraishi’s S-4 write leveling is unrelated to its re-timing operations, and the results of S-4 write leveling are used to align the output

DQS signal to the system clock signal CK. The Petition cites Figures 14A-B, but it does not explain how this and the associated text suggest delaying DQ signals given that they show no change in DQ timing before and after S4 write leveling.

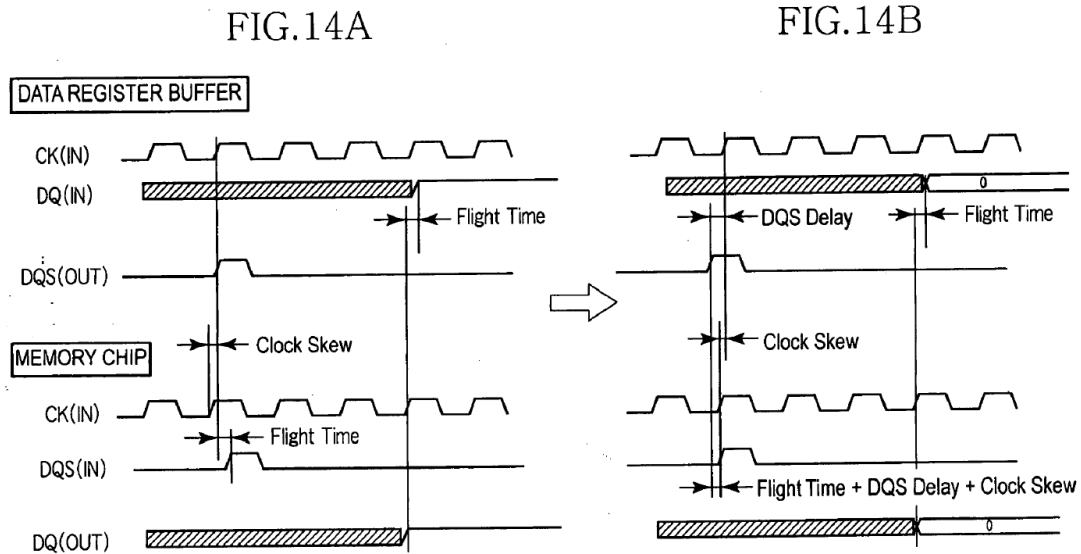


This is not a technicality or nuance: Hiraishi separately addresses flight time differences in DQ by globally increasing the latency value by one clock cycle (e.g., to WL=5 and CL=6). See *infra* Section VI.C.2-VI.D.2. As a result, re-timing does not delay a signal through a data path by an amount determined in the write leveling as contended, and there is no showing that the delay is by an amount determined by the data buffer's processing circuitry in response to module control signals, as required by Element 1[f].

1. Hiraishi's S-4 Write Leveling Operations Adjust the Timing of DQS to Align with the Clock

There is no evidence that Hiraishi's S4 write leveling involves a write FIFO (since there is no write data from the system, only "signal ... from the data

input/output terminal 204” of the memory chip 200) or delays a signal through a data path (since it adjusts DQS timing). EX1005, [0144]-[0145]. Instead, Hiraishi’s S-4 write leveling, performed by write leveling circuit 322, accounts for mismatches between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. EX1005, [0142]-[0146]; EX2013, ¶¶108-109; EX2012, 60:7-12 (“So what happens in S4 write leveling -- we are now looking at the relationship between the CLK and the DQS signal that appears at the input to the memory device. We want that to now be in synch.”). Hiraishi describes the S4 write leveling process in connection with FIGs. 14A-14B below.



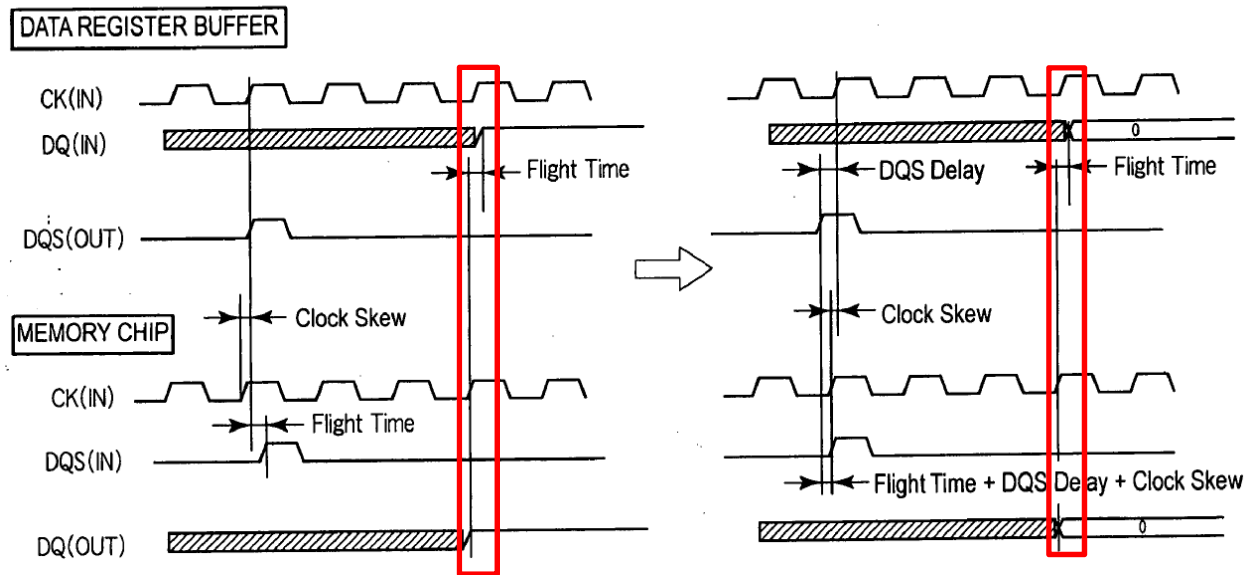
Specifically, “[i]n the write leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 14A, the data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK.” EX1005, [0143]. But “[b]ecause it takes a certain amount of propagation time until

the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” *Id.*, [0143]. To compensate, “[t]he write leveling circuit 322 of *the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift.*” *Id.*, [0145]. Based on Hiraishi’s S4 write leveling, “the data register buffer 300 can find a timing to output the data strobe signal DQS based on the input clock signal *CK*” and “the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.” *Id.*, [0146]. The Petition alleges that “delays determined during write leveling are stored in the data register buffer 300 and applied by the control circuit 320 to delay both the data and data strobe signals during subsequent write operations” Pet., 45-46.

Hiraishi states instead that “[u]pon completing the write leveling operation in this manner, the phases of *the clock signal CK and the data strobe signal DQS* input to the memory chip 200 are substantially matched with each other.” EX1005, [0146]. Hiraishi does not allege that the result of the write leveling would be used to “delay ... the data ... signals” or “to ensure that the standard *data to strobe timing* requirements are met at the memory devices,” as Petitioner alleges. Indeed, Petitioner does not explain why write leveling affects the timing of DQ at all: DQ(IN) and DQ(OUT) are unchanged in FIGs. 14A-14B below.

FIG.14A

FIG.14B



EX1005, [0027] (“FIGS. 14A and 14B are timing charts for explaining the write **leveling** operation between the data register buffer 300 and the memory chip 200, where FIG. 14A is a timing chart at the time of starting the leveling and FIG. 14B is a timing chart at the time of ending the leveling.”); EX2013, ¶110. Nor has Petitioner explained why the amount of DQS timing adjustment is determined in response to a module control signal. *See* EX1005, [0139]-[0145] (no reference to DRC or another signal generated in response to system command signals received via the set of C/A signal lines as required by 1[b], 1[e]).

Figure 12, “a timing chart for explaining the **write operation** of the memory module 100 ...,” also makes clear that the results of Hiraishi’s S4 write leveling are not used for re-timing DQ. Specifically, FIG. 12 describes a normal write operation that occurs **after** Hiraishi performs its write leveling during initialization. EX1005,

[0138] (“FIG. 13 is a flowchart for explaining the initializing operation of the memory module 100 at the time of activation.”).

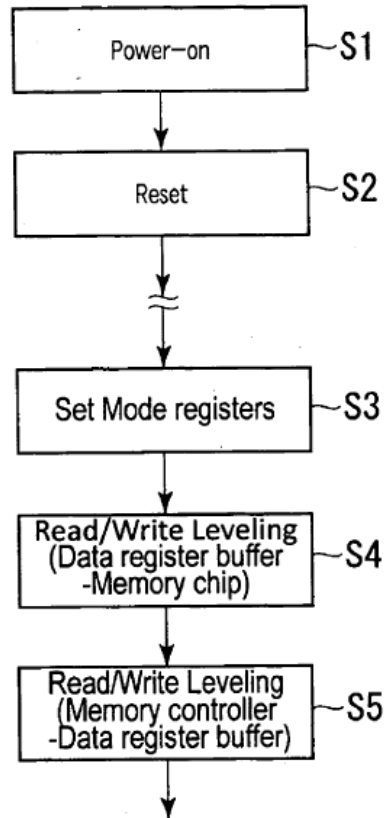


FIG.13

As shown in Figure 12, the CK(IN) and DQS(IN) to the memory chip are aligned (highlighted in red), thanks to Hiraishi's S4 write leveling. Shown separately from this CK-DQS alignment is the DQ data re-timing from a write latency of 4 clock cycles (WL=4) to one of 5 clock cycles (WL=5) (highlighted in green).

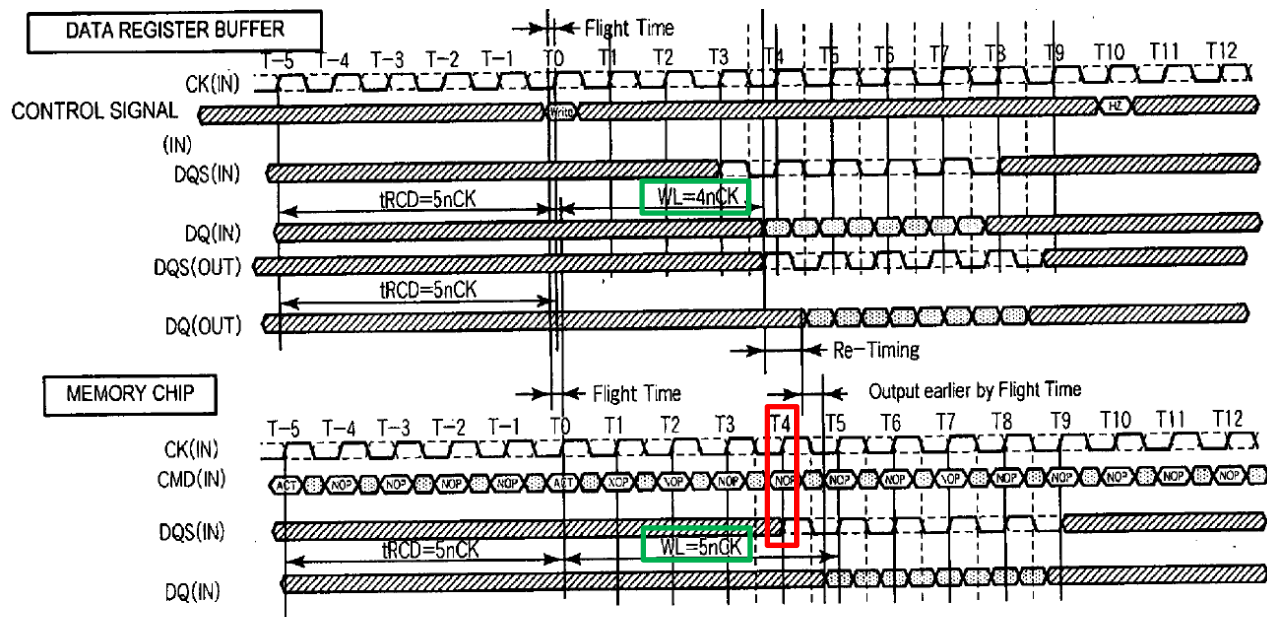


FIG.12

Thus, a POSA would understand that re-timing of DQ signals is separate and distinct from using Hiraishi's S4 write leveling results used to align CK(IN) and DQS(IN). That is, a POSA would not understand that S4 write leveling results are used for re-timing in FIFO as Petitioner contends. EX2013, ¶¶110-115.

2. Hiraishi's WL Re-timing Addresses Flight Delays for Write Operations by Adding a Clock Cycle of Latency

Hiraishi says little about its re-timing operation, and the Petition does not purport to explain how it functions or how it allegedly relates to Hiraishi's leveling. Hiraishi states that, for the write operation of FIG. 12, "the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data." EX1005, [0133]. See below.

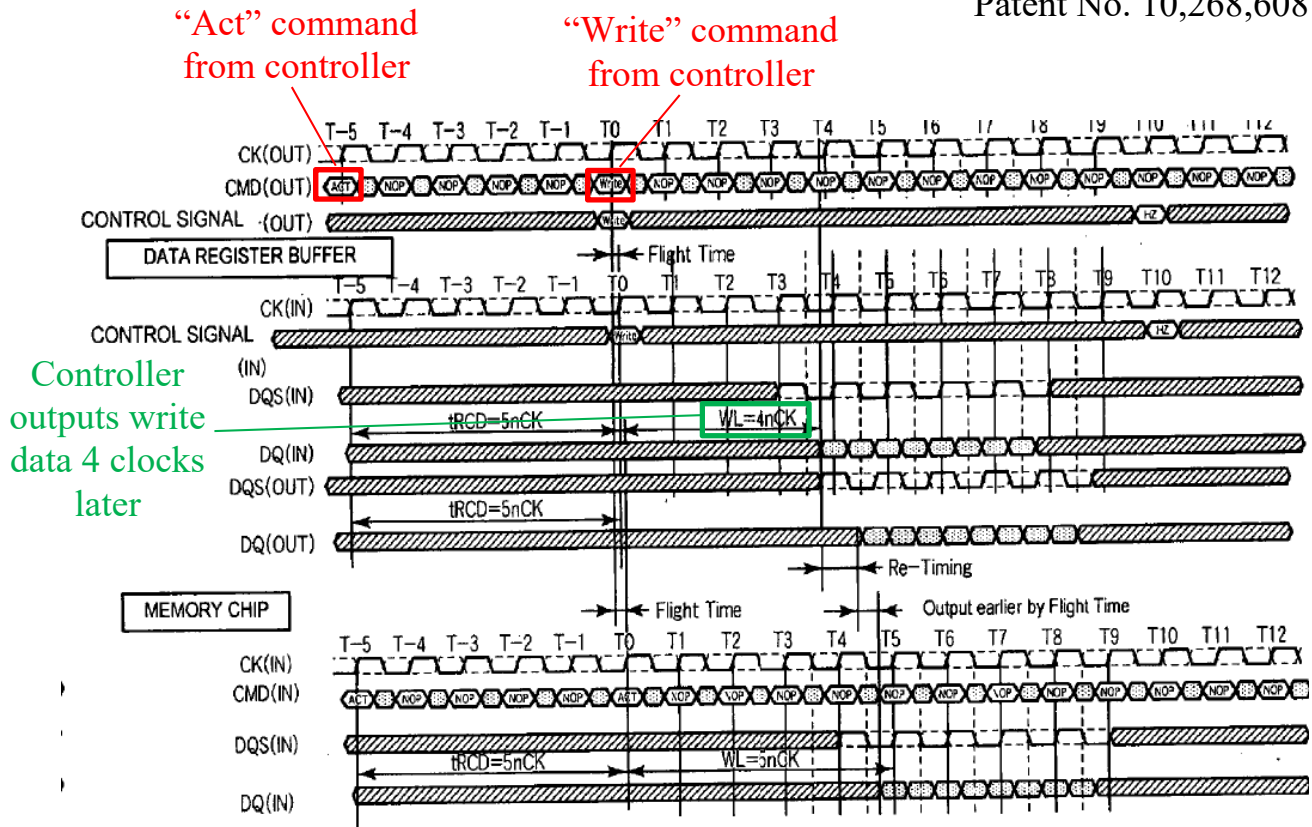


FIG.12

Thereafter, the "data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 [and] then performs a re-timing *in synchronization with the internal clock LCLKW*³ using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS." EX1005, [0135]. See below.

³ Write leveling, however, changes the output DQS's timing "*by displacing the internal clock LCLKW based on the direction of the phase shift.*" EX1005, [0145].

That is another indication that retiming and S-4 leveling are unrelated.

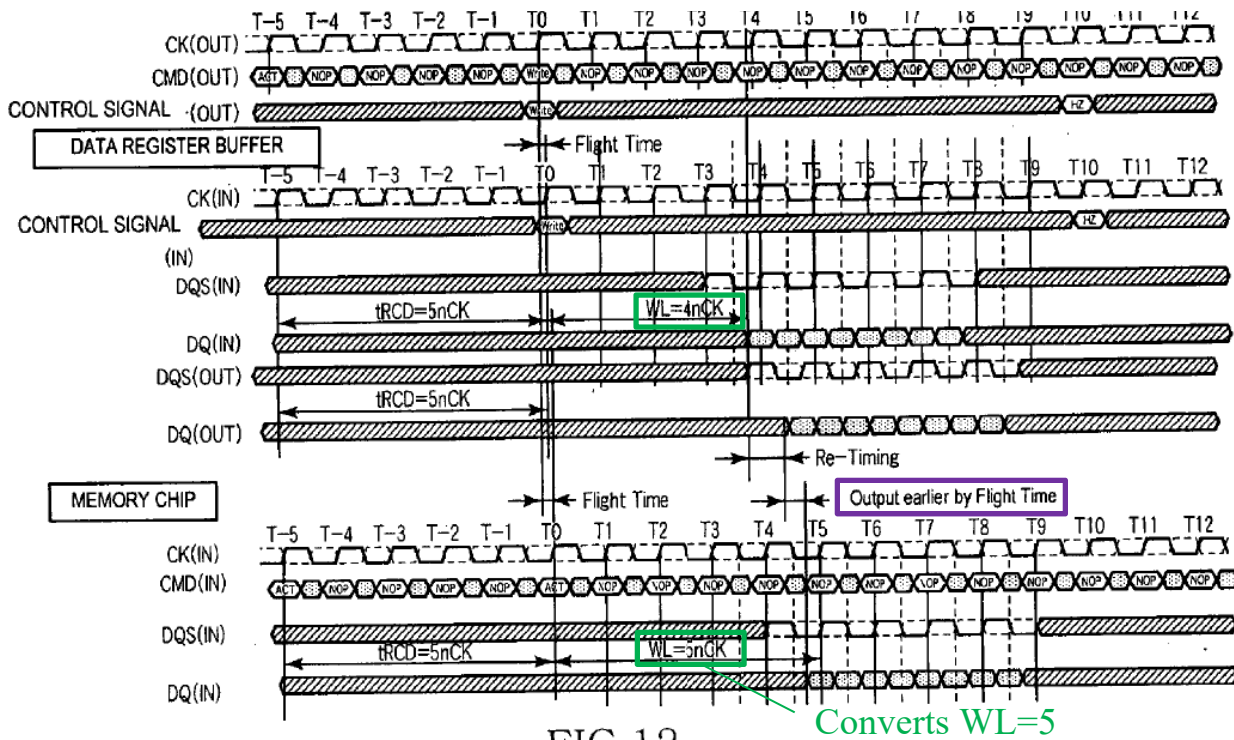


FIG. 12

Hiraishi explains that “there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200.” EX1005, [0136] (above in purple). This “predetermined time difference (Flight Time)” causes “the data register buffer 300 [to] output[] the write data DQ earlier by an amount equivalent to the Flight Time.” *Id.* Hiraishi’s re-timing operation accounts for these time differences by converting the internal latency to the next clock cycle. EX2013, ¶¶116-119. By resetting internal latency to the next clock cycle, Hiraishi’s buffer circuit need not compute individual delays and hence does not “delay a signal through the data path *by an amount determined by the command processing*

circuit,” as recited in Element [1f]. Notably, the Petition does not explain how lengthening WL by one clock cycle relates to any determination by the data register control circuit 320 or logic in DLL (the alleged command processing circuit).

Petitioner alleges that “Hiraishi only shows fly-by delays less than one clock cycle.” Pet., 81; *see also* Pet. 80, heading (c). A POSA would therefore understand that Hiraishi can account for all delays by simply resetting latency to the next clock cycle for all buffer circuits. EX2013, ¶¶120-126. That is, under Petitioner’s reading of Hiraishi, setting the buffer’s latency to the next higher clock cycle would adequately address all possible flight delays. *See Id.* Indeed, because latency delays are set in full clock cycles, it would make no sense to determine individual delays and add corresponding fractional clock cycles to WL or RL. EX2013, ¶127.

Dr. Wedig also confirmed that in each of Hiraishi’s re-timing examples, the latency is set to the next clock cycle. *See* EX2012, 72:19-21 (“So you’re correct that in these examples, it changes the write latency and the read latency to add one more CLK cycle.”). In other words, the amount of delay that may occur is not computed or otherwise determined by the buffer’s command processing circuit because, as Dr. Wedig confirmed, all the memory chips, the data buffer and the data register buffer receive the same “system-level CLK” and have a common understanding of timing. EX2012, 74:9-24; EX2013, ¶126. As a result, regardless of individual flight time or

which memory chip is at issue, the data can be all output at the same time by increasing the latency to the next clock cycle. EX2012, 74:25-75:14.

In the context of FIG. 15, Dr. Wedig explained that in order for the data buffer to output data at the same time T, the buffer is “going to hold the data, if it came in early, and then it's going to output it at T6. And if it comes into the data buffer later, then it's going to hold it until it gets to T6 in this example.” EX2012, 76:13-77:7. This involves no determination of delays by the buffer’s command processing circuit (allegedly data register control circuit 320 or logic in DLL circuit 310). EX2013, ¶128. Instead, as Dr. Wedig went on to explain, “the DLL circuit gives you the timing for the chip. So yeah, so it’s going to generate the CLK so – so after it’s held it the appropriate amount of time, it will [clock] it out at T6. And yeah, the DLL circuit is in charge of making that CLK.” EX2012, 78:10-24. This occurs at the same time T across all of Hiraishi’s buffers, as Dr. Wedig confirmed. EX2012, 78:25-79:8.

The fact that the same time T applies across buffers is reflected in Hiraishi’s FIG. 15 which uses the same CK(IN) clock timing for different buffers.⁴

⁴ There is no showing that LCLKW/LCLKR is delayed by an amount determined by data register control circuit or DLL logic in response to a module control signal either.

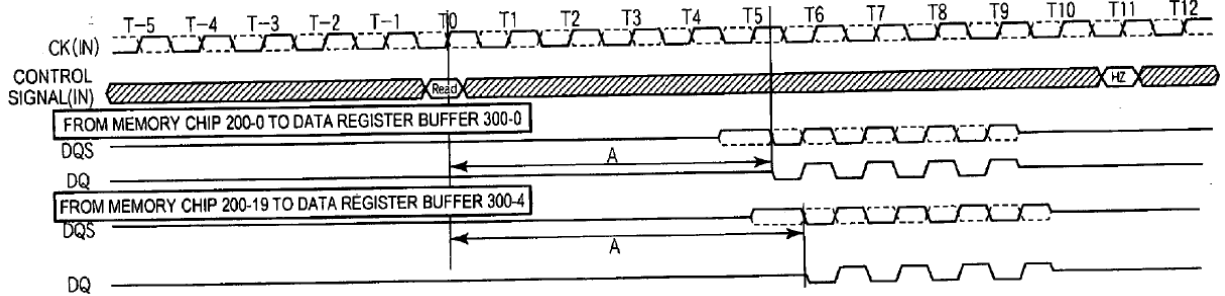


FIG.15

EX2013, ¶¶129-130.

Dr. Wedig confirmed that, in reference to FIG. 15 above, the same system clock CK is used for different memory chips and different data buffers. EX2012, 144:5-21.⁵

The fact that Hiraishi's data buffer does not determine an amount of delay is also consistent with the Board's prior decision in IPR2017-00730. There, the Board was asked to consider Hiraishi's re-timing operations in the context of an IPR against the related '632 patent. The Board determined that Saito—which is substantially the same as Hiraishi—does not perform re-timing in accordance with “any time interval determined during read/*write* leveling.” See '632 Decision, 14. In fact, the Board

⁵ While Dr. Wedig later testified on re-direct, and after discussing his testimony with Petitioner's lawyers, that Hiraishi's data buffers have different T values, Hiraishi shows otherwise in FIG. 15 above.

found that Saito does not explain how its latency parameter was chosen. *See id.*, 12.⁶ Nor does the Petition. Moreover, the Board expressly rejected the notion that Hiraishi’s re-timing is related to leveling. *See id.*, 12-13.

Thus, Hiraishi’s re-timing addresses flight-time delays by increasing latency by one clock cycle instead of relying on write leveling result. It therefore does not “delay a signal through the data path by an amount determined by the command processing circuit,” as recited in Element 1[f].

D. Hiraishi’s CL Re-Timing Is Not Based on the Results of S-4 Read Leveling and Does Not Satisfy Element 1[f]

For Element 1[f], the Petition separately argues that delays determined during Hiraishi’s S-4 read leveling are used to re-time DQ/DQS signals during subsequent read operations. Pet., 48-51. As found by the Board, Hiraishi’s S-4 read leveling is unrelated to its CL re-timing operations, and the results of S-4 read leveling is used to adjust the activation timing of the input buffers, not to re-time the DQ/DQS signals as alleged. ’632 Decision, 12-14. Moreover, neither Hiraishi’s S-4 read leveling nor its CL re-timing, alone or in combination, determines “an amount of

⁶ The latency parameter at issue was CL because the claims related to a “read latency parameter.” However, the Petitioner relied on both Saito’s write and read leveling operations (*id.* 10), and the Board expressly extending its reasoning to write leveling. *See id.*, 14.

delay for a signal through a data path by an amount determined by the data buffer's processing circuitry," as recited required by Element 1[f].

1. Hiraishi's S4 Read Leveling Operations Adjust the Activation Timing of Hiraishi's Input Buffers Which the Petition Contends are Tristate Buffers

Hiraishi's S4 read leveling determines when its input buffers INB are activated to receive read data signals and strobe signals coming from memory chips 200 over L1 and L2 via terminals 341, 342, 351, and 352. EX1005, [0140], [0147-151], Fig. 15; EX2013, ¶133; EX2016 (506 IPR), 59:4-18 (Dr. Wedig confirming that Hiraishi's read leveling adjusts the activation timing of the input buffers).⁷ The data register control circuit 320 (which includes read leveling circuit 323) turns on input buffers for DQ/DQS signals before the expected arrival of the data and strobe signals. EX1005, FIG. 5, [0088], [0151]; EX2013, ¶¶133-135; IPR2017-00730, Paper 8 at 12-13 (finding that "the time interval determined during the read leveling operation by read leveling circuit 323 ... determines a 'time A' that is used to adjust timing of 'the input buffer circuit INB and the like.'"). Hiraishi's read leveling adjusts the timing of when the input buffers INB are turned on so they are active

⁷ Dr. Wedig testified in connection with an IPR filed against the parent to the '608 patent which also relied on Hiraishi. Dr. Wedig confirmed that his understanding of Hiraishi has not changed. EX2012, 15:5-12, 16:7-14.

when data arrives. EX1005, [0151] (“The time is ... used in an adjustment of an activation timing of the input buffer circuit INB and the like.”).

But the timing adjustment for INB based on S-4 read leveling does not disclose a delay circuit for delaying a signaling through a data path because:

- *first*, Petitioner maps INB to a separate claim element, tristate buffer on the data path, and not to the delay circuit. Pet., 42-43 (“Hiraishi teaches that these OUTB and INB buffers are tri-state buffers.”); EX2012, 31:23-25 (“Q. And so those tristate buffers, those OUTB and INB buffers, are those part of the delay circuit as well? A. No, they're not.”). Thus, any alleged delay resulting from the timing adjustment to the INB buffers would at best be a timing adjustment for recited “tristate buffer,” not for the “delay circuit,” per Element 1[f]; EX2013, ¶137.
- *Second*, adjusting the activation timing of Hiraishi’s INB buffers does not impact or result in any delay to DQ. Moreover, because the DQ data has not yet been sample/registered by the FIFO circuit, the FIFO cannot delay the DQ data by any specific or replicable amount. EX2013, ¶136.

Thus, a POSA would not understand that the results of Hiraishi’s S4 read are used in Hiraishi’s CL re-timing, as Petitioner contends.

2. Hiraishi's CL Re-timing Addresses Flight Delays for Read Operations By Adding a Clock Cycle of Latency

The Petition cites to FIG. 11 as allegedly showing that Hiraishi discloses “[r]ead [that] determines delays (“Re-Timing”),” specifically alleging that “the DQ/DQS read delays are determined as the difference between the time of data output at CL=6 and time A of data arrival.” Pet., 48-49. But that is not what Hiraishi discloses. Hiraishi has a simple solution to the issue as described above—setting buffer latency to the next clock cycle, for all memory devices, which effectively eliminates the need to determine any individual delay amounts. *See supra*, Section VI.C.2. In specific, Hiraishi illustrates how the memory device’s read latency CL=5 is converted by the data buffer into a read latency CL=6 by outputting the data exactly one clock cycle later. See below.

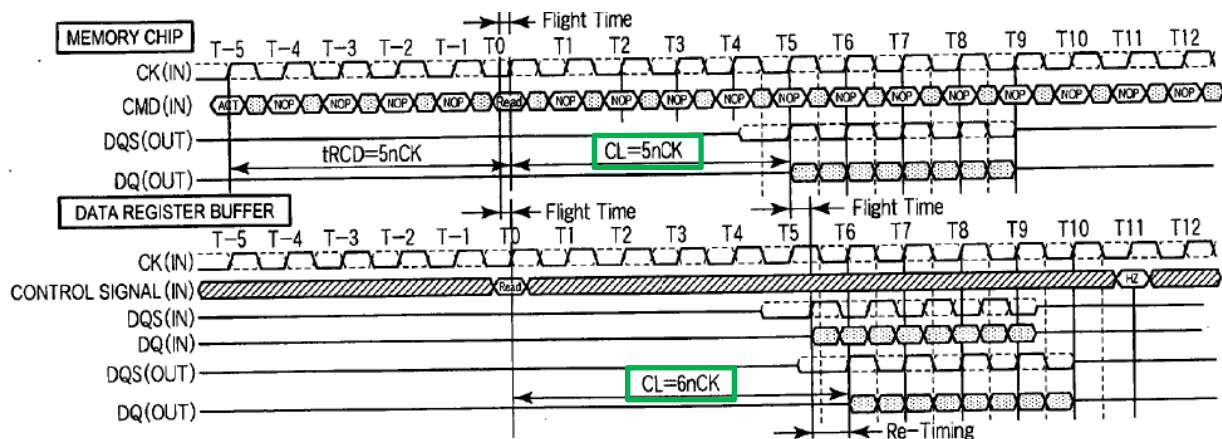


FIG. 11

EX1005, FIG. 11 (partially reproduced and annotated); EX2013, ¶139.

Hiraishi explains that “there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.” EX1005, [0129]. This predetermined time different (or flight time) varies as between different memory devices as shown by Time A below where the DQ/DQS received by the data buffer from memory chip 200-0 is different than Time A for the DQ/DQS received from memory chip 200-19).

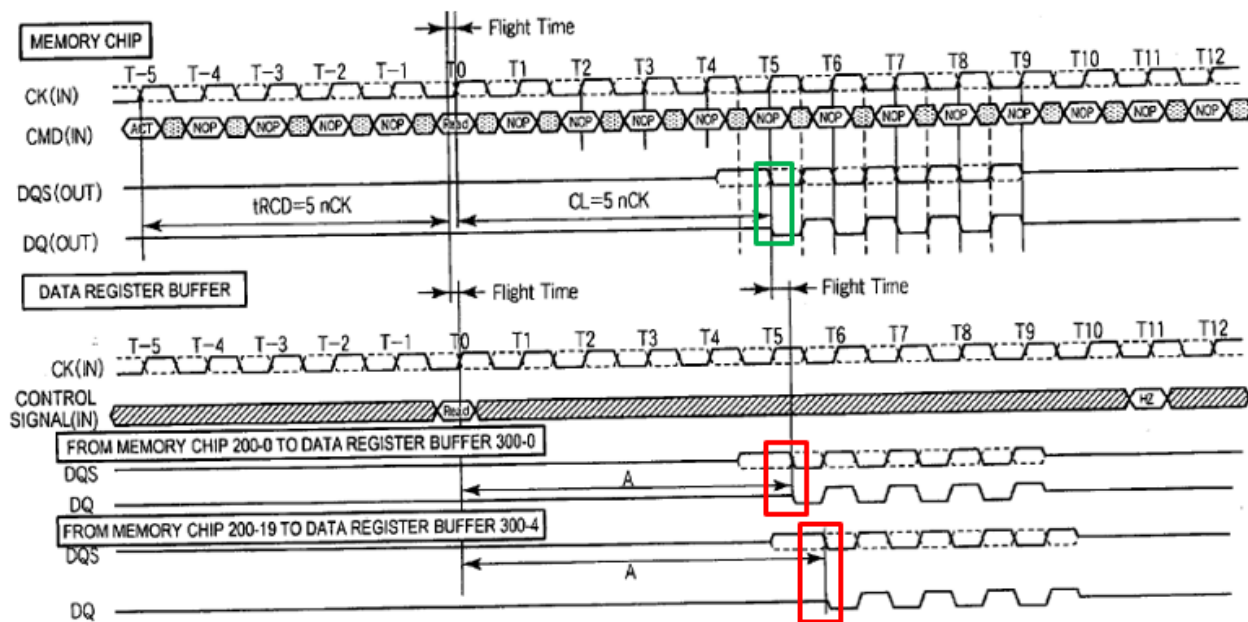


FIG.15

EX1005, FIG. 15; EX2013, ¶140. However, rather than trying to account for these timing differences by determining specific signal delays for each memory device, Hiraishi uses a re-timing operation which sets all buffer latencies to the next clock

cycle because CL's are set in whole cycles and it would not make sense to determine individual delays and add fractional clock cycles to CL. EX2013, ¶127. Specifically, Hiraishi discloses

[T]he data register buffer 300 *performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6*, and outputs the read data DQ and the data strobe signal DQS. *With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.*

EX1005, [0130].

This “re-timing” causes both the read data (DQ(OUT)) and the corresponding strobe signal (DQS(OUT)) to begin outputting from the data register buffer 300 exactly 6 clock cycles after T0, effectively ensuring synchronization regardless of the flight time for the memory device from which the read data is received. EX2013, ¶141.

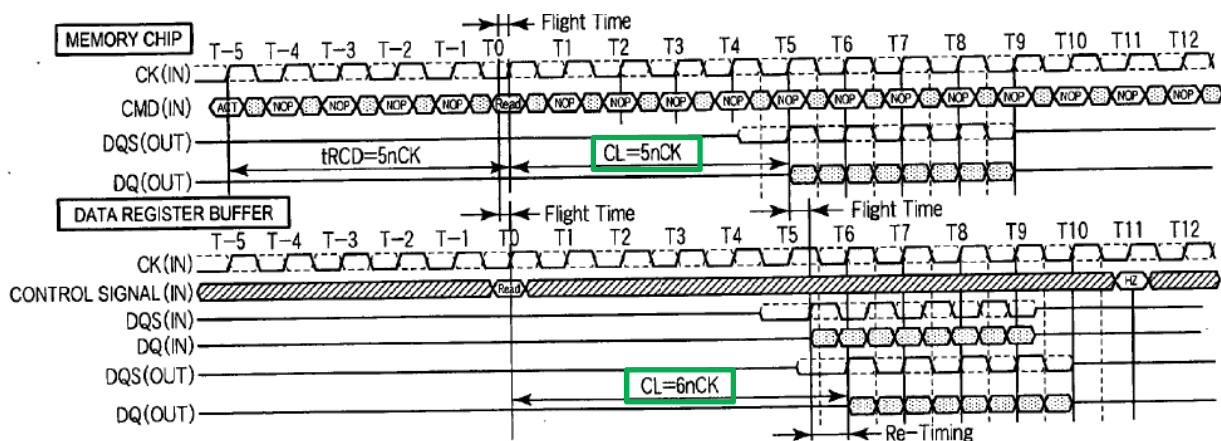


FIG. 11

EX1005, FIG. 11 (partially reproduced and annotated to show data buffer converting CL=5 to CL=6). This is consistent with the Board's findings in IPR2017-00730 for the related '632 patent that Saito (substantially the same as Hiraishi) "does not explain how CL=6 was chosen" (*Id.*, 12). The Board rejected the notion that Saito/Hiraishi's re-timing is related to read leveling. *See id.* at 12-13 ("Petitioner argues that [Saito's re-timing] is related to the time interval determined during read leveling operation by read leveling circuit 323, but that operation determines a "time A" that is used to adjust timing of 'the *input buffer circuit INB* and the like.'") (original emphasis included).

Thus, in addition to the fact that Hiraishi's re-timing operation of FIG. 11 does not use the result of the S-4 read leveling process, there has been no showing that it "delay[s] a signal through the data path by an amount determined by the command processing circuit," as recited in Element [1f].

VII. THE PETITIONER FAILED TO ESTABLISH THAT ANY CLAIM OF THE '608 PATENT IS UNPATENTABLE UNDER GROUND 2

A. Petitioner Has Failed To Establish That Ground 2 Has a Delay Circuit in the Data Path

Petitioner's theories for Ground 2 are both based on adding a delay element DR-1 found in Tokuhiro's memory controller to Hiraishi's data buffer, as shown below.

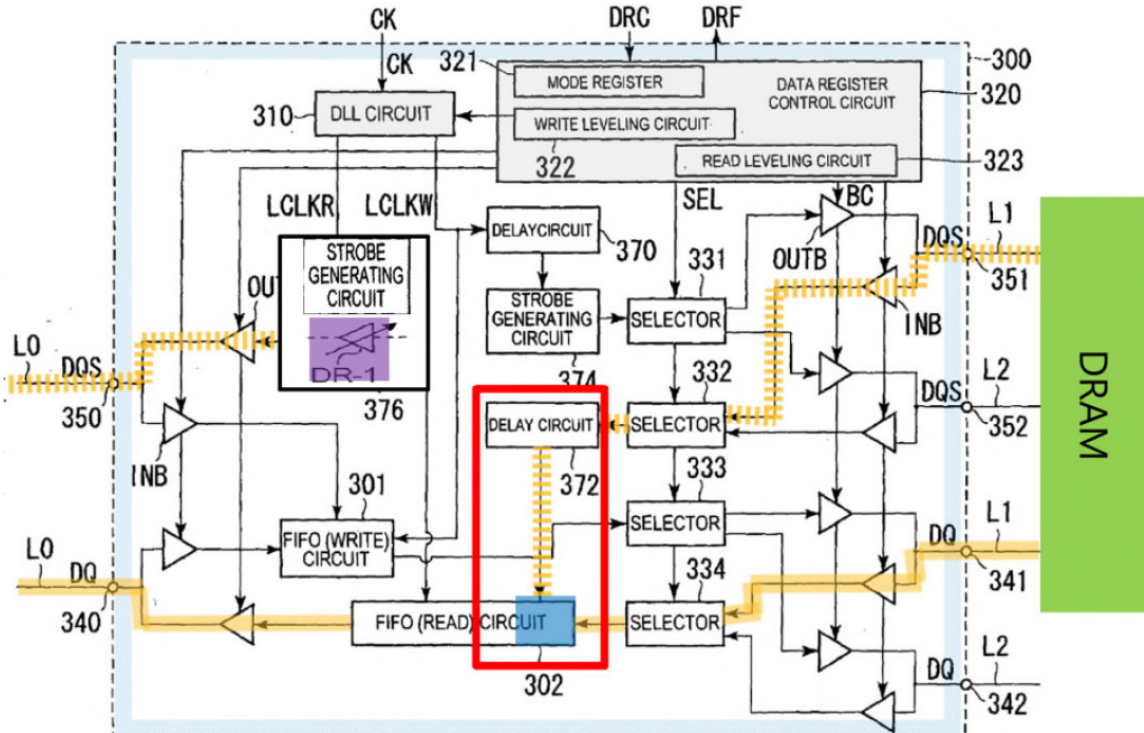


FIG. 5

Pet., 89. The Petition argues that “[i]n this combination, Tokuhiro’s read delay functionality (DR-1, purple) is added to Hiraishi’s data buffer to remove the large fly-by delays. Based on Tokuhiro’s teachings, the read delay circuit DR-1 (purple) is added to the Strobe Generating Circuit 376 to delay both the strobe signal DQS 350 and the signal clocking out data⁸ from FIFO (Read) Circuit 302 so that the delayed data DQ 340 from the Read FIFO is in sync with the delayed strobe 350.” *Id.* But the newly added delay element DR1 is **not** in the DQ data path, as required

⁸ Tokuhiro’s delay circuits do not delay any clock signals, so a POSITA would not have applied Tokuhiro’s teaching to delay a clock signal. EX2013, ¶144.

by the recited “delay circuit.” *See Supra*, Section VI.A. Nor are the allegedly delayed DQS 350 or the signal clocking out data “through the data path” because they do not pass through data (DQ) signal lines. EX2013, ¶¶91, 143-144. The combination therefore does not cure the deficiency in the base references and Ground 2 fails.

B. A POSA Would Not Have Had a Reasonable Chance of Successfully Achieving the Claimed Invention Based on the Proposed Modification to Hiraishi

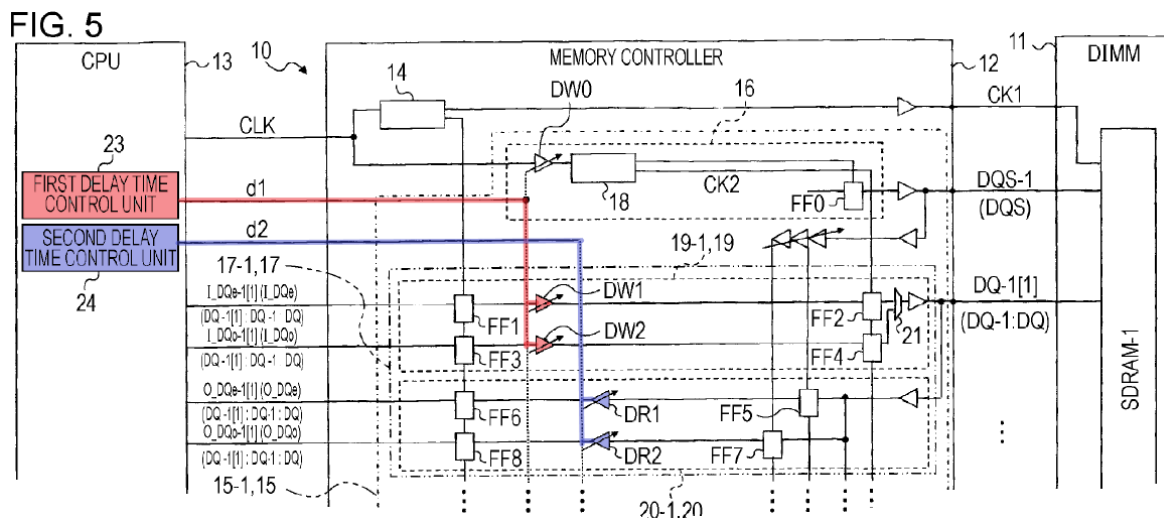
Moving Tokuhiko’s DR-1 delay element from the memory controller into Hiraishi’s data buffer is purely hindsight driven. For example, Dr. Wedig admitted in the related ’506 IPR that he had never seen a reference that didn’t use the memory controller to adjust for fly-by delays seen by the memory controller. EX2016, 171:15-21. Likewise for the “second implementation” that supposedly adds Tokuhiko’s teaching to Hiraishi’s “module controller,” (Petition, 91-92) Dr. Wedig admitted that he had never seen a reference describing a “module controller” being used to program a delay element for read/write leveling. EX2016, 194:18-21.

Regardless, Petitioner has failed to establish a reasonable expectation of success (or shown that the combination would be operable) for at least the following two reasons.

1. The Added Delay Element is Inoperable

Tokuhiko’s read and write leveling are controlled by the computer’s main CPU, as Dr. Wedig confirmed. EX2012, 92:2-4, 93:6-9; EX2013, ¶147. In Tokuhiko,

these operations are performed by the first delay time control unit 23 (highlighted in red below) and second delay time control unit 24 (highlighted in purple below), which are part of the *computer's CPU 13*, and which also provides the respective control signals d1 and d2 to control the variable delay circuits DW and DR in the memory controller 12 in all of the channels, in order to set the respective delays. *See id.*; *see also* EX1006, 12:34-58; 13:55-14:2; 15:3-19.



This architecture, in which Tokuhiro's delay elements (DW and DR) in all of the channels are connected over dedicated CPU control lines on which control signals d1 and d2 from all of the channels are provided to the various delay elements, explains why Tokuhiro can accommodate variable delay elements and determine the read delays using, not just the respective write delays, but also the maximum of write delays among all of the channels. EX2012, 92:25-93:4 ("Q. ... [S]o the signal line d1 is dedicated to the DW delay elements and control signal line d2 is *dedicated* to

the DR control elements? A. That's the way Tokuhiro implemented it, yes.”); EX2013, ¶¶147-149.

But in the Petitioner’s combined diagram, reproduced below, the only input to the delay element DR-1 is the local clock signal LCLKR, which is not a “control signal” or are otherwise capable of operating a variable delay element. EX2013, ¶¶150-154.

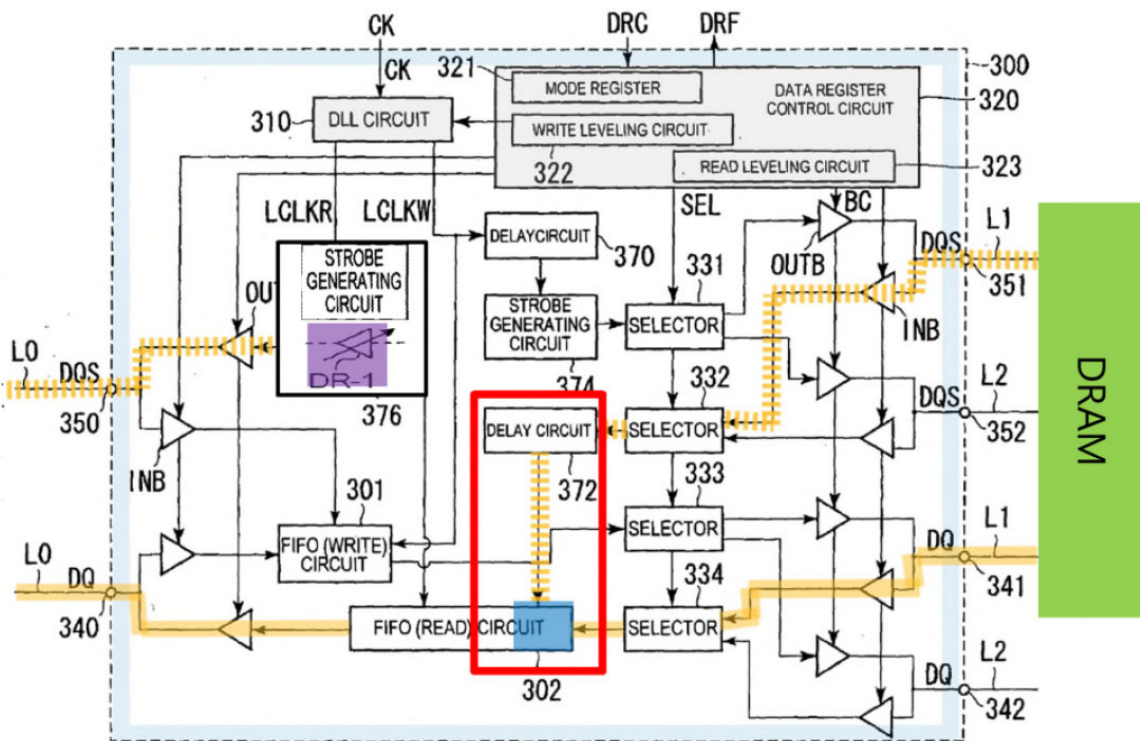


FIG.5

Petition, 89 (annotating Hiraishi’s FIG. 5). It also does not explain how the required circuitry can be or should be included when DR is used instead of or in addition to the Read FIFO. Pet., 90.

Moreover, Petitioner does not explain what—let alone how—relevant control signals should be provided to operate DR-1. For example, Petitioner does not allege that Hiraishi’s main CPU (CPU 11) is providing such a control signal. Petitioner also does not propose to further modify Hiraishi’s memory controller or “module controller” to provide control signal lines to the data register buffers 300, nor could it. This is because, unlike in Tokuhiko where control is carried out at the CPU level, in Hiraishi this would require adding further control signaling lines between the memory controller or “module controller” and each of Hiraishi’s *nine* data register buffers 300-0 through 300-8, to follow Tokuhiko’s teaching of implementing control of the delay elements via dedicated control signal lines d1 and d2 in order to carry out Tokuhiko’s delay algorithm, as Dr. Wedig confirmed. EX2012, 92:25-93:4; EX2013, ¶¶150-155. This would add substantial complexity which the Petitioner cannot justify and defeats a purported reason to combine (stated on Pet. 91). EX2013, ¶156 (explaining complexity such as non-compliance with JEDEC DIMM pinouts, increased physical size and power consumption for routing and operating the additional wires); see *Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App’x. 827 (Fed. Cir. 2019) (“The Board must weigh the benefits and drawbacks of the modification against each other, to determine whether there would be a motivation to combine.”).

In sum, Petitioner has failed to provide any competent evidence or reasoning that a POSA would have had a reasonable expectation of implementing the claimed delay features because Tokuhiro's delay element is not provided with any control signal which is required for its algorithm to operate, per Tokuhiro's express teachings. EX2013, ¶¶147-157. See *Tec Air, Inc. v. Denso Mtg. Michigan Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999) ("If when combined, the references 'would produce a seemingly inoperative device,' then they teach away from their combination.") (quoting *In re Spinnoble*, 405 F.2d 578, 587 (CCPA 1969)); *In re Fritch*, 972 F.2d 1260, 1265 n.12 (Fed. Cir. 1992) (explaining that a proposed modification is inappropriate for obviousness "when the modification render[s] the prior art reference inoperable for its intended purpose"). To be clear, this is not a dispute about bodily incorporation of two references, but to explain why the combination cannot implement Tokuhiro's algorithm as argued. The Petition simply fails to analyze whether the specific feature it seeks to combine is operable in the combination, or that a POSA would have a reasonable expectation of implementing the claimed invention.

2. There is No Motivation to Use the New Delayed DQS Signal to Clock Data Out from Hiraishi's FIFO, Which Would Not Be Expected to Reliably Synchronize DQS/DQ Signals

Petitioner purports to include Tokuhiro's DR1 to time the read data output from the read FIFO. Pet., 89-91. Hiraishi discloses using a local clock LCLKR to clock read data out of the FIFO (Read) 302, as highlighted in red below.⁹

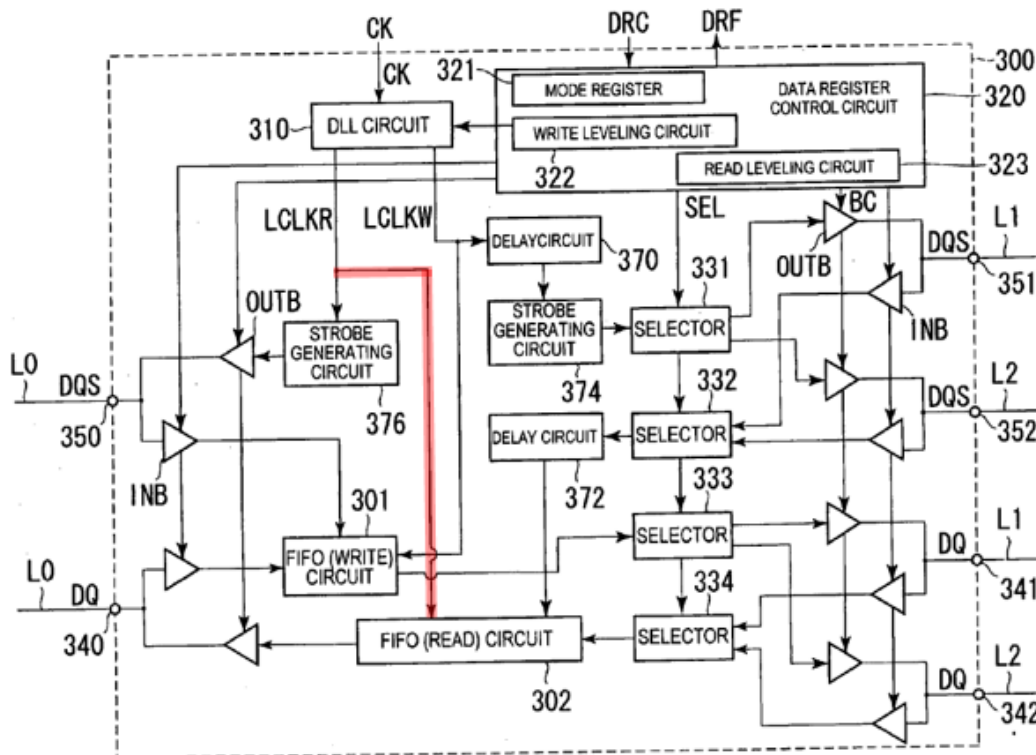


FIG. 5

EX1005, [0087] (“An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310.”).

⁹ The DQS signal from delay circuit 372 is for sampling the data inputted to the read FIFO, and does not control when the data is clocked out. EX2013, ¶159.

Petitioner, however, inexplicably replaces the local clock LCLKR signal in its proposed combination with the DQS signal from Hiriashi's modified strobe generating circuit 376, as show in **green** below.

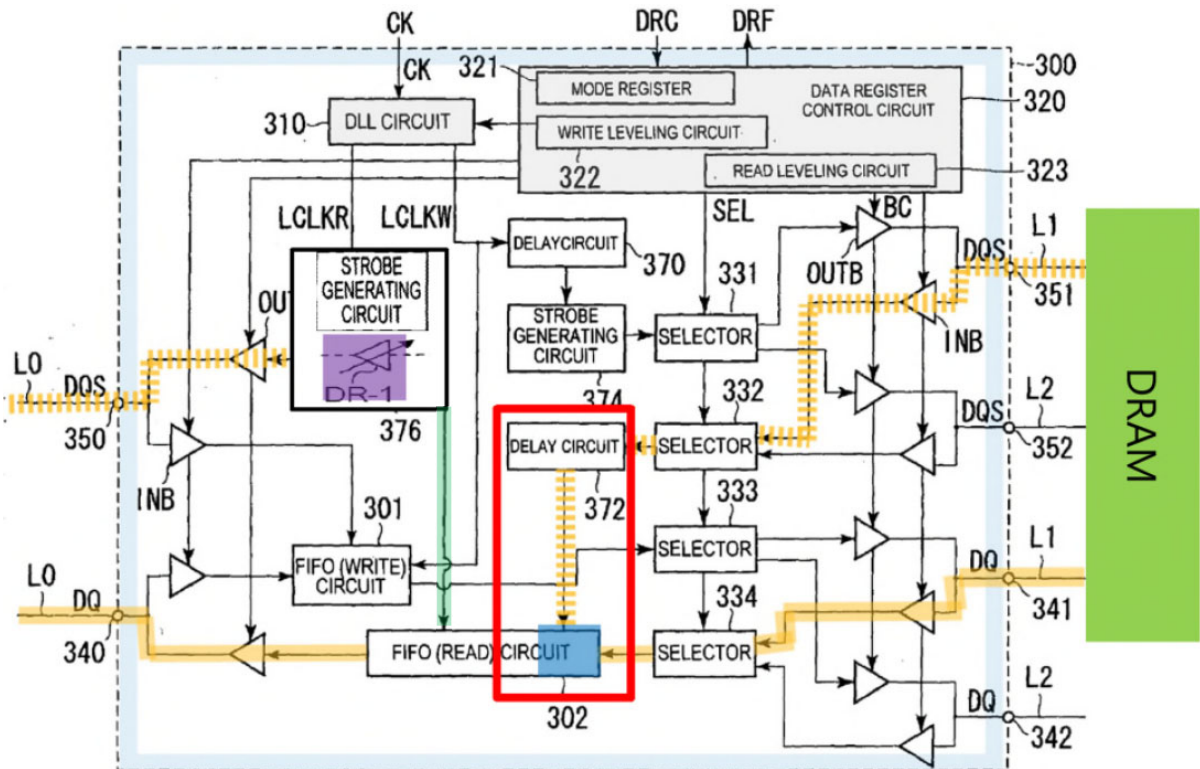


FIG. 5

Pet., 89. Dr. Wedig confirmed that the newly added green line from the modified strobe generating circuit 376 is a DQS signal delayed by DR-1 that is being provided to clock data out from FIFO 302. EX2012, 90:15-91:18.

Even if one were to accept Petitioner's reasons for including Tokuhiro's DR1 in Hiraishi, there is still no explanation, let alone evidence, supporting this *further* substitution of a delayed strobe from delay element DR1 in place of Hiraishi's local

clock LCLKR signal to clock data out. This hindsight modification is inconsistent with Hiraishi's operations. EX1005, [0087]; EX2013, ¶162.

As shown below, for both read and write operations, Hiraishi relies exclusively on local clocks to time the corresponding data from FIFOs and strobe generators, so that the data output from the FIFOs is properly aligned with the strobe from the strobe generators, as shown in Hiraishi FIG. 11 and as required by the applicable standard. EX2013, ¶162.

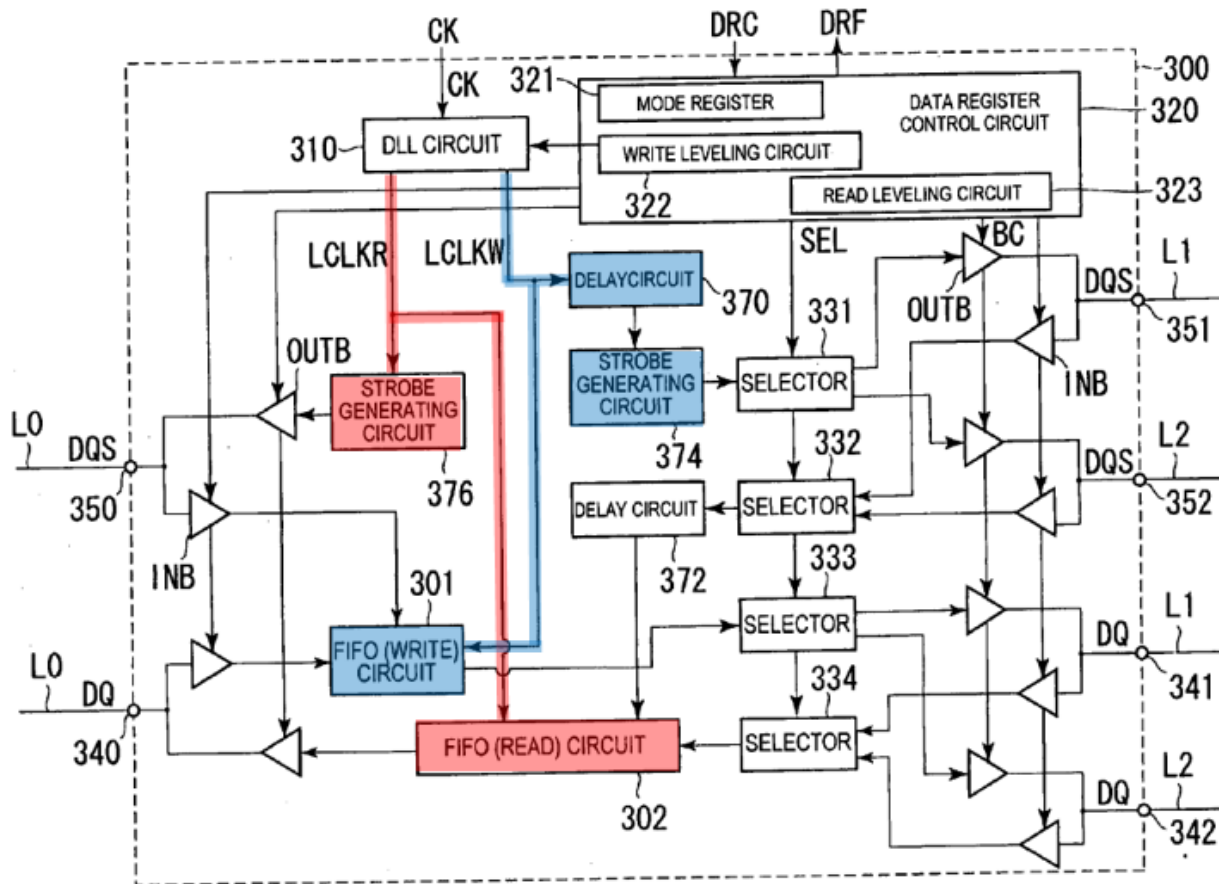
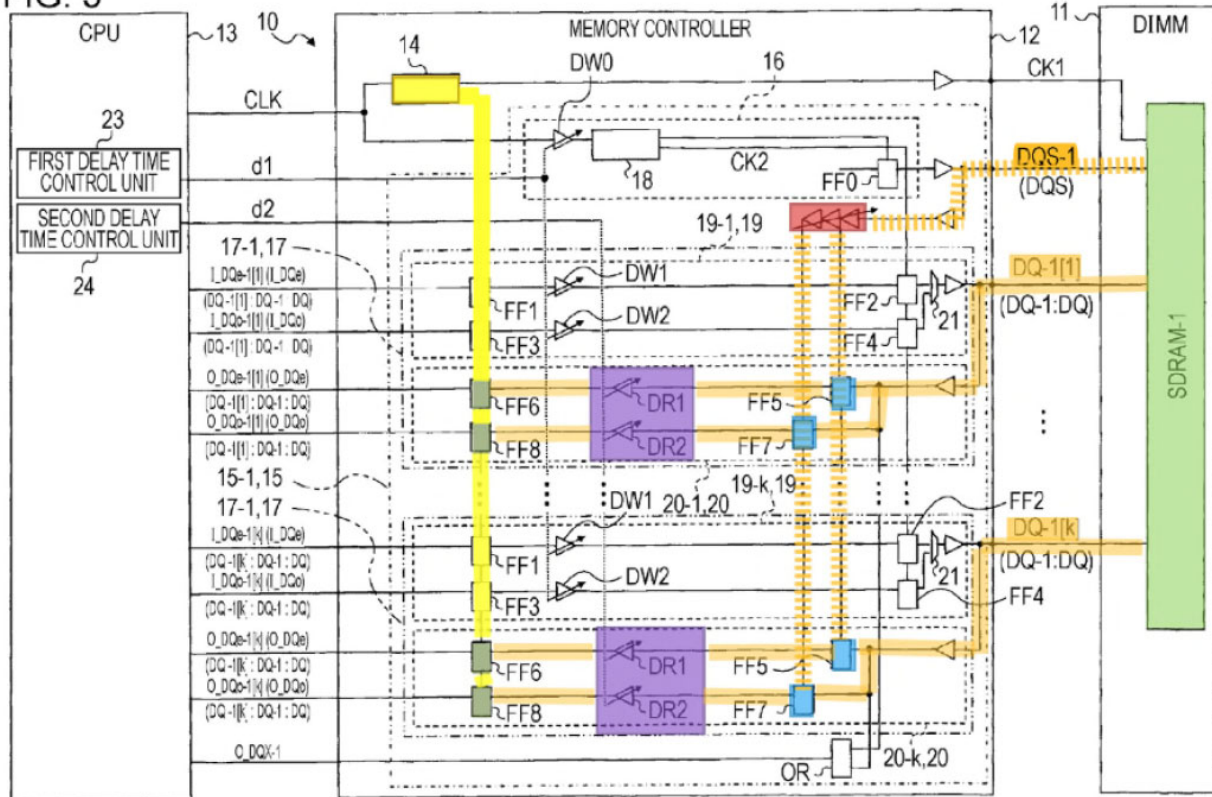


FIG.5

Tokuhiro also exclusively uses a local clock signal from clock signal generator 14 to output data from Tokuhiro's flip-flops. EX2013, ¶163; EX1006,

FIG. 5



Like Hiraishi's use of the system clock CK to generate local clocks LCLKR and LCLKW, Tokuhiro discloses that "[t]he first clock signal generator 14 generates and outputs the clock signal CK1 having a predetermined cycle based on a clock signal CLK input from a CPU 13." EX1006, 6:17-19. Tokuhiro further explains that, "[t]he flip-flop FF6 outputs the third data signal O_DQe, which is input from the second variable delay circuit DR1, to the CPU 13 (described later) when the clock signal CK1 generated from the first clock signal generator 14 is input." *Id.*,

11:28-31; EX2013, ¶164. Thus, both Hiraishi and Tokuhiro expressly rely on clock signals, not DQS signals, to clock data out of a data storage. This is for good reasons, consistent with the practice in the field. DQS signals cannot be used to clock out data from a FIFO, and Petitioner has not shown otherwise. Unlike a clock signal, DQS signals includes a “Pre-amble” (tRPRE) and “Post-amble” (tRPST) which would cause additional bits to be clocked out due to the additional transitions at the edges of the pre- and post-ambles. EX2013, ¶165. See below.

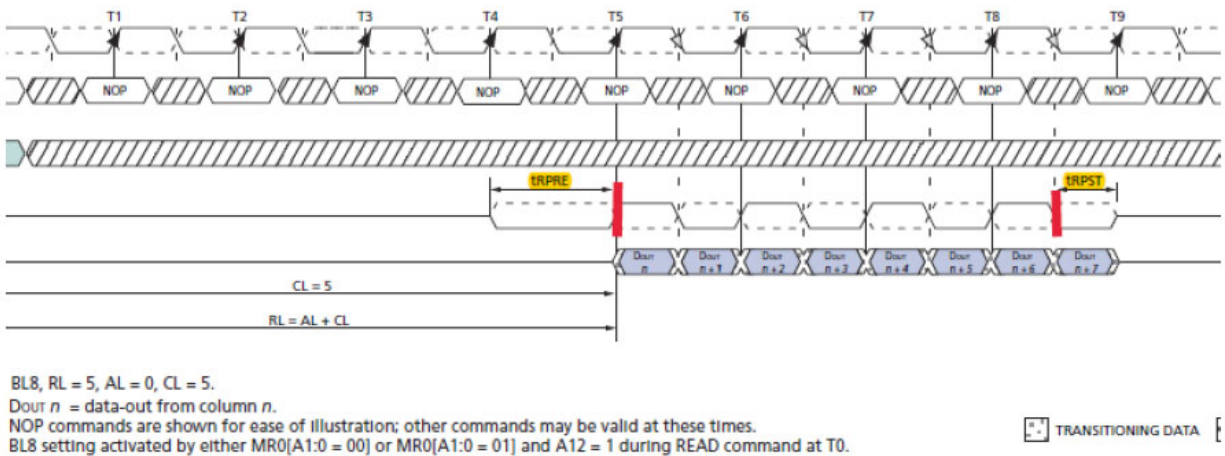


Figure 25 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)

EX1020, 56.

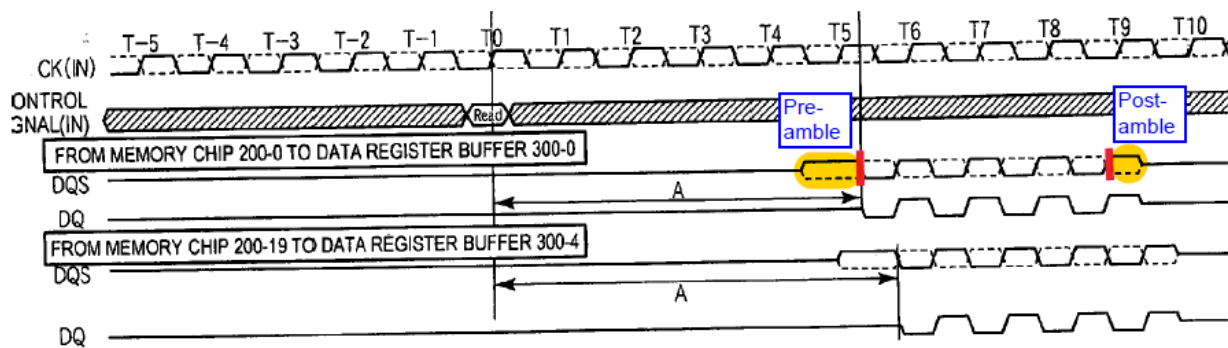


FIG.15

EX1005, FIG. 15 (annotated).

As shown above, attempting to clock out data from Hiraishi's FIFO with a DQS signal would mean the data is being clocked out at every edge of the DQS signal including the edge ending the preamble, which in all likelihood will not be the correct timing at least as a result of the pre- and post-amble bits which are not present on a clock signal. EX2013, ¶166. This is why Hiraishi and Tokuhiko use a clock signal to clock out data from the FIFO. *Id.* Yet, Petitioner does not address this at all, let alone explain why it would not lead to system failure. The prior art does not teach this approach and a POSA would not use that approach or reasonably expect that DQS would provide a reliable mechanism to clock out the data or synchronize the DQS/DQ signals at the data buffer output. *Id.*

In sum, Petitioner fails to provide any motivation for the further modification of using the newly created DQS from DR1 in the strobe generating circuit 376 (that is off the data path) to clock out the read data from the FIFO instead of following the known approach of using a local clock signal. Petitioner's piecemeal modifications of Hiraishi are clearly the product of impermissible hindsight, and do not support obviousness.

C. Petitioner's Motivation Arguments Do Not Support the Combination of Hiraishi and Tokuhito, as Proposed

1. Petitioner's Motivation Arguments Do Not Motivate Deviating From Hiraishi's and Tokuhito's Disclosures of Using Delay Elements in a Memory Controller

Petitioner advances three alleged motivations in support of its proposed Hiraishi-Tokuhito combination.” *First*, to use “Tokuhito’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet., 76. *Second*, to remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 79. Tokuhito won’t solve the alleged problem as explained below. *Third*, to remove “fly-by delays that are greater than one clock cycle.” Pet., 80. But even assuming each of Petitioner’s alleged motivations are correct (they are not as explained below in §VII.C.3), a POSA would still not have been motivated to deviate from Tokuhito and Hiraishi’s express disclosure by moving Tokuhito’s delay element out of the memory controller and into the data buffer.

As detailed above, Tokuhito relies on delay elements in a memory controller programmed by the system’s main CPU (CPU 13). *See supra*, V.B, VII.B.1. A memory controller is in a host outside a claimed memory module. However, Petitioner does not propose to add Tokuhito’s delay element DR-1 to Hiraishi’s memory controller 12, or to program that delay element DR-1 with Hiraishi’s CPU

11. Instead, Petitioner proposes adding the delay element DR-1 to Hiraishi's data buffer. Pet., 91-92. But this modification is unconnected to any of Petitioner's stated motivations above because the same alleged benefits would have been achieved if DR1 is implemented in Hiraishi's memory controller. EX2013, ¶168. This, coupled with the lack of any teaching of the type of implementation proposed by Petitioners, is fatal to the obviousness theory. The three alleged reasons to combine does not explain why a POSA would have deviated from the references' express disclosures of using delay elements in the memory controller, especially when Hiraishi already has both a memory controller 12 that performs leveling and a CPU 13 connected directly thereto. EX2013, ¶¶168-170. This is also not an "obvious to try" scenario—there are specific reasons not to deviate from Hiraishi's and Tokuhiro's memory-controller-based approach, as explained below.

2. Petitioner's Arguments for Moving Tokuhiro's Delay Elements Are Unsupported and Contrary to General Knowledge in the Art

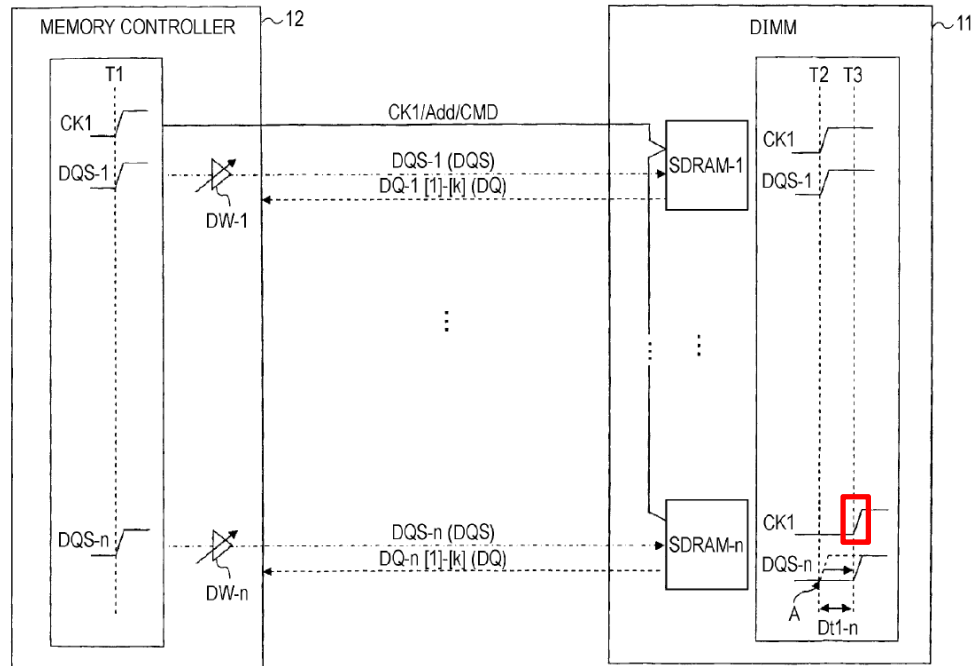
Petitioner also argues that (1) "[a] POSITA would have understood that this combination avoids the memory controller having to manage large fly-by delays of read data during either the training or normal operation, thus requiring less circuitry and functionality for implementation, such as extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles," and (2) "that large fly-by delays are removed on the module at the first practically available

location (the data buffers, since JEDEC-compliant memory devices would not have such delay elements), preventing the rest of the system from having to manage those large fly-by delays.” Pet., 91. But this reasoning, regurgitated by Dr. Wedig without support (EX1003, ¶¶265-266), does not hold up under closer inspection.

First, contrary to its assertion, Tokuhiro does not disclose accounting for delays greater than one clock cycle. While Petitioner cites to a passage in Tokuhiro that discusses delays becoming “greater than a typical data period of the DDR3 memory interface” (EX1003, ¶¶101, 230, 252), Tokuhiro’s “data period” refers to *one-half* clock cycle in a double-date-rate system (DDR3). EX2013, ¶¶172-174. Also, because of Tokuhiro’s “gradually prolong[ing] the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time” (EX1006, 13:55-60), the process can only align the DQS with the next up or down clock edge, which would necessarily occur in less than one clock cycle. EX2013, ¶175. As Dr. Mangione-Smith explains, this “incremental increase in delay time will continue until the process detects a clock transition. But because all clock rising edges look the same and all clock falling edges look the same, the process will not know to skip a clock edge and align the DQS to the next clock edge in order to correct for a greater than one clock cycle delay.” *Id.* This is clearly seen in FIG. 7,

for example, which shows DQS-n being aligned with the next clock edge that the system detects (in this case T3). EX2013, ¶176.

FIG. 7



Second, Hiraishi's memory controller 12 is on the computer's motherboard 12, not on the memory module 100. EX2013, ¶177.

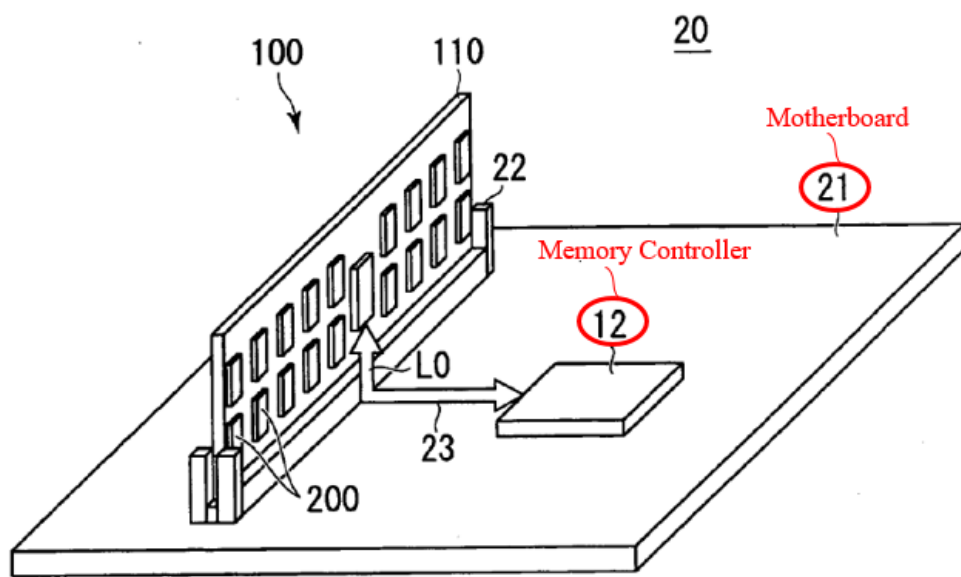
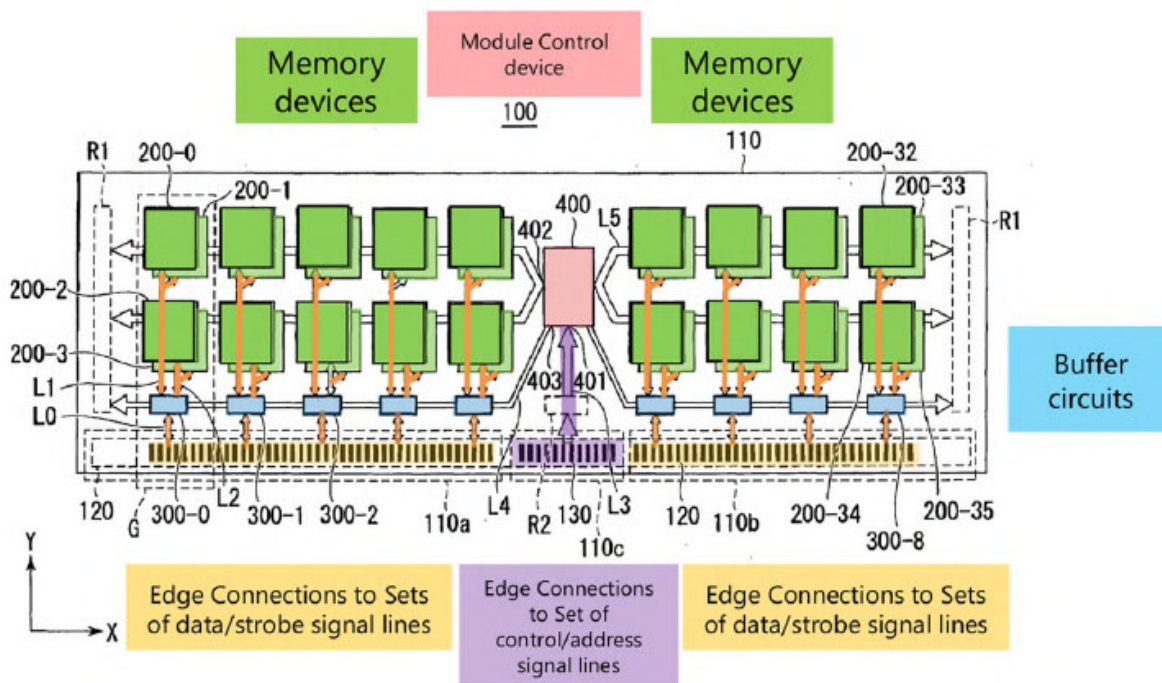


FIG.3

In contrast, Hiraishi's data buffers 300 reside directly on the memory module 100, as shown below (light blue). EX2013, ¶178.



Pet., 59.

A POSA would understand that the memory controller, being on the motherboard, is far less space-constrained than the memory module, as Dr. Wedig confirmed in the related '506 IPR. EX2016, 143:5-144:2; EX2013, ¶179. Moreover, Dr. Wedig confirmed that the JEDEC standards “specify pretty exacting what the size of the memory module should be,” but do not prescribe dimensions for the size of the memory controller. EX2016, 94:11-22; EX2016, 142:15-24. Thus, the last place a POSA would be motivated to add extra logic and circuitry would be to a component (here, the data buffer) which is competing with the memory devices for limited space. *See id.* The limited space coupled with intense computing is also detrimental to heat dissipation. EX2013, ¶179; EX2017 (electronic cooling).

Third, there is also the non-trivial matter of Tokuhiro's delay elements needing to be programmed. EX2013, ¶181. Tokuhiro teaches that its delay circuits are programmed over dedicated control signal lines d1 and d2 (*see supra* §VII.B.1), but Petitioner does not propose a different control mechanism in the combination. Thus, based on Tokuhiro's implementation, the combination would also require running an additional control signal line to each of the delay elements added to Hiraishi's *nine* data buffers. This would significantly complicate the circuitry and add to space constraint, which Petitioner failed to consider. EX2013, ¶¶155-156, 181.

Fourth, there are significant advantages of having Tokuhiro's delay elements implemented in the memory controller. As taught in Tokuhiro, the delays are determined in a process in which "the first delay time control unit 23 ... gradually prolongs the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signals DQS-n are input to the n-channel SDRAM-n substantially at the same time." EX1006, 13:55-60. This process would be significantly less complex if performed when the first delay time control unit 23 and the first variable delay circuit DW-n are on the same side of the data bus, due in no small part to the fact that the memory controller can only communicate with the memory module following DDR signaling protocols, while CPU/memory controller communications do not. EX1006, 5:57 ("The memory controller 12 is a DDR3

(Double Data Rate 3) memory interface”); EX2013, ¶184. This can be avoided by simply implementing Tokuhiro’s delay elements as Tokuhiro intended—in the memory controller. *See id.*

Moreover, Dr. Wedig cites to Giovannini in support of his argument that large fly-by delays were a problem. But, as Dr. Wedig himself explains, “[t]o solve this known problem of fly-by delays that are larger than a clock cycle, Giovannini discloses a special, *FIFO-based circuitry in the memory controller.*” EX1003, ¶ 253. Thus, Petitioner’s own evidence, including specifically Hiraishi, Tokuhiro and now Giovannini, rely on the *memory controller* to remove fly-by delays, which is consistent with the fact that a POSA would understand that the memory controller is the lesser space-constrained component (as compared to the DIMM) in which to add the required logic and circuitry. EX2013, ¶180. In this regard, it is telling that Dr. Wedig testified in the 506 IPR that he has never seen a reference that doesn’t rely on the memory controller to adjust for fly-by delays. EX2016, 177:14-19. Yet, that is exactly what Petitioner is attempting to create here—something that the record of evidence has not established existed in prior art. Nor is there any evidence that moving DR from the host side onto the memory module side would yield the same outcome given that one is the receiving side of the data and the other is the transmitter side. If moving Tokuhiro’s delay elements out of the memory controller

isn't a clear example of hindsight reconstruction, then it's hard to imagine what would be.

The combination does not significantly reduce the leveling burden on the memory controller, as Dr. Wedig confirmed in the '506 IPR.

Q. In the combination of Hiraishi and Tokuhiro, Hiraishi's memory controller is still adjusting the incoming data so that it is being captured in the valid data eye?

A. Yeah, just like it was before. I mean, there's no -- you had to do that when you did before you ever added Tokuhiro.

EX2016, 181:9-15. And in this proceeding, he similarly confirmed that even in the Hiraishi-Tokuhiro combination the memory controller might have “to do some clean-up, some slight adjustment” for flight time, and in any event would have to include a delay element for adjusting DQS by 90 degrees. EX2012, 105:24-106:1, 106:4-107:10. As such, there is no evidence that the proposed modification would reduce the logic and circuitry in the memory controller compared to implementing DR in the memory controller. For instance, implementing DR1 in memory controller would also rid of the need for a special FIFO. At any rate, a FIFO would still be needed under Dr. Wedig's own theory, as stated above. EX2016, 181:9-15; EX2013, ¶¶182, 185. The fact is that Petitioner's proposed combination does not eliminate any of the leveling logic and circuitry from the memory controller 12—it just self-servingly splits it up between Hiraishi's memory controller and data buffer in an

effort to fabricate a memory system that purports to read on the claims of the '608 patent. This isn't a design choice or "obvious to try." Not only is it something Dr. Wedig has ever seen done, it is at odds with basic logic and contrary the JEDEC committee intentionally shifting much of the burden of timing synchronization to the memory controller. EX2013, ¶¶182, 186.

3. Petitioner's Motivation Arguments Are Conclusory and Unsupported

As noted above, Petitioner advances three reasons for combining Hiraishi and Tokuhiko. Each of Petitioner's reasons are conclusory and unsupported, however, and none require moving Tokuhiko's delay element out of the memory controller, as has been proposed. Thus, Petitioner has not shown that a POSA would have been motivated to undertake the combination.

Calculating Read Delays Based on Write Operations (Pet., 73-78): The Petition alleges that performing read leveling operations independently from write leveling, as in Hiraishi, requires time and corresponding circuitry, thus motivating the use of Tokuhiko's technique of setting the read delays based on the write delays. Pet., 76. Even if true, that reasoning would at best motivate a POSA to implement Tokuhiko's technique as Tokuhiko discloses—using DR delay elements in the memory controller which are programmed by the CPU. As the combination has been proposed, however, the result would be an *increase* in the overall time and circuitry required. This is because, the proposed combination requires the "memory

controller” (first implementation) or the “module controller” (second implementation) to transmit signals to each of delay elements that have been added to Hiraishi’s *nine* different data buffers which would have otherwise been internal to the memory controller. EX2013, ¶¶188-189; EX2016, 174:7-11. In particular, as Dr. Wedig testified in the ’506 IPR, each of those nine data buffers would individually be detecting delays, measuring the delays, providing feedback to the module controller or memory controller, depending on the implementation, and then writing the delay into the nine DR-1 elements. EX2016, 151:2-13 (“[Y]ou would need to be able to provide some feedback to the module controller.”); 152:17-23 (“[Y]ou might need to modify some of it to be able to detect the delay, to be able to measure the delay, and then you need to be able to rewrite the -- you need to be able to write the delay for the read path into DR1.... You would need to be able to do calculations on what the read delay would be, and you would need to be able to write the value into the read delay driver.”). That these operations are now spread out over nine different components (data buffers) under the direction of the memory controller or module controller, instead of being all contained in the memory controller itself, as Hiraishi describes, necessarily means the number of signaling steps needed for Hiraishi to perform its leveling would increase, not decrease. EX2013, ¶¶188-189. This does not support obviousness. *See Arctic Cat*, 795 F. App’x. at 833 (“The Board must weigh the benefits and drawbacks of the

modification against each other, to determine whether there would be a motivation to combine.”); *Winner Int’l. Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (2000) (“[T]he benefits, both lost and gained, should be weighed against one another.”).

Read data arriving at memory controller at same time (Pet., 79): Hiraishi’s read data is all output from the data buffers at T6 (*infra* §VI.D.2) such that if, as Tokuhiro assumes, the data signal lines between the memory controller and DIMM are of “the same length” (EX1006, 5:52-53), they would have arrived at the memory controller at same time. EX2013, ¶190. The different arrival time would be due to different lengths and Tokuhiro does not provide a solution. Further, Petitioner provides no reason why a POSA would desire to remove fly-by delays on the module side, while a POSA would recognize that the memory controller would remove fly-by delays for both write and read (not using different mechanisms for write and read), and that the controller is the most capable component to handle signal processing and to manage timing adjustments. *See id*; EX2012, 96:8-13 (confirming that Tokuhiro’s delay elements make all data appear to arrive at the same time, T10). Further, Dr. Wedig confirmed that delay elements would be necessary in the memory controller at least to account for residual delays. EX2012, 105:24-106:1, 106:4-107:10; EX2013, ¶¶185.

Removing fly-by delays greater than one clock cycle (Pet., 80-82): Petitioner is incorrect in its assertion that Tokuhiro addresses fly-by delays greater than one

clock cycle. Tokuhiro's "data period" refers to one-half clock cycle in a double-date-rate system. EX2013, ¶¶172-176, 191. Indeed, as explained above, Tokuhiro cannot address fly-by delays that are more than one clock cycle because Tokuhiro "gradually prolong[s] the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time" (EX1006, 13:55-60) such that the process can only align the DQS with the next up or down clock edge. *See id.* This method cannot detect or address fly-by delays of greater than one clock cycle, as described above in Section VII.C.2. *Id.* Finally, there is no reason provided for why this reason would have motivated a POSA to move the delay elements out of the memory controller.

VIII. CONCLUSION

Based on the foregoing, the Board should find the claims not unpatentable.

Case No. IPR2023-00847

Patent No. 10,268,608

Dated: March 29, 2024

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I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Response contains 13,991 words, excluding the words in the table of contents, table of authorities, exhibit list, this certificate of word count, and certificate of service. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/s/Jonathan M. Lindsay
Jonathan M. Lindsay

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on March 29, 2024, a complete copy of the foregoing document **PATENT OWNER RESPONSE** and **EXHIBITS 2012– 2023** were served by electronic mail, as agreed to by the parties, upon the following:

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