Paper No. 23

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

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IPR2023-00847
Patent 10,268,608 B2

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# PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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## EXHIBIT LIST

| Exhibit # | Description |
|---|---|
| 1001 | U.S. Patent No. 10,268,608 |
| 1002 | File History of U.S. Patent No. 10,268,608 |
| 1003 | Declaration of Dr. Robert Wedig |
| 1004 | Curriculum Vitae of Dr. Robert Wedig |
| 1005 | U.S. Patent Pub. No. US2010/0312956 to Hiraishi |
| 1006 | U.S. Patent No. 8,020,022 to Tokuhiro |
| 1007 | U.S. Patent Pub. No. 2006/0277355 by Ellsberry |
| 1008 | U.S. Patent No. 6,184,701 to Kim |
| 1009 | U.S. Patent No. 8,566,516 to Schakel |
| 1010 | File History of U.S. Patent No. 9,128,632 |
| 1011 | File History of U.S. Patent No. 9,563,587 |
| 1012 | *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition) |
| 1013 | *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response) |
| 1014 | *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution) |
| 1015 | *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision) |
| 1016 | U.S. Patent Pub. No. 2011/0062999 to Nimaiyar |
| 1017 | Declaration of Julie Carlson for JEDEC Standard 21-C |

| Exhibit # | Description |
|---|---|
| 1018 | JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002) |
| 1019 | Declaration of Julie Carlson for JESD79-3C |
| 1020 | JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008) |
| 1021 | Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts) |
| 1022 | Harold S. Stone, Microcomputer Interfacing (1982) |
| 1023 | Microsoft Computer Dictionary (5th ed. 2002) |
| 1024 | U.S. Patent No. 9,263,103 to Giovannini |
| 1025 | U.S. App. No. 61/676,883 (provisional application to ’632 Patent) |
| 1026 | U.S. Patent No. 8,565,033 to Manohararajah |
| 1027 | U.S. Patent No. 7,808,849 to Swain |
| 1028 | U.S. Patent No. 6,906,555 to Ma |
| 1029 | U.S. Patent Pub. No. 2007/0008791 to Butt |
| 1030 | U.S. Patent No. 7,036,053 to Zumkehr |
| 1031 | U.S. Patent No. 9,824,035 |
| 1032 | File History of U.S. Patent No. 9,824,035 |
| 1033 | U.S. Patent No. 5,036,221 to Brucculeri |
| 1034 | U.S. Patent No. 9,536,579 to Iijima |
| 1035 | *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021) |

| Exhibit # | Description |
|---|---|
| 1036 | Order Transferring Cases to the Austin Division, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Feb. 14, 2022) |
| 1037 | Joint Claim Construction Statement, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Apr. 14, 2022) |
| 1038 | Order on Motion to Stay, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. May 11, 2022) |
| 1039 | [intentionally omitted] |
| 1040 | Decision Granting Institution of *Inter Partes* Review, *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 16 (PTAB July 19, 2022) (U.S. Patent No. 9,824,035) |
| 1041 | Decision Denying Institution of *Inter Partes* Review, *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237, Paper 15 (PTAB July 19, 2022) (U.S. Patent No. 10,268,608) |
| 1042 | [intentionally omitted] |
| 1043 | [intentionally omitted] |
| 1044 | Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021) (asserting U.S. Patent No. 10,860,506) |
| 1045 | First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. May 3, 2022) |
| 1046 | U.S. Patent No. 10,860,506 |
| 1047 | Decision Granting Institution of *Inter Partes* Review, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00711, Paper 14 (PTAB Oct. 21, 2022) (U.S. Patent No. 10,860,506) |

| Exhibit # | Description |
|---|---|
| 1048 | Joint 4-3 Claim Construction and Prehearing Statement, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Aug. 19, 2022 and Aug. 23, 2022) |
| 1049 | Joint Claim Construction Chart Pursuant to P.R. 4-5(d), *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Sept. 30, 2022) |
| 1050 | Claim Construction Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 14, 2022) |
| 1051 | Defendants' Objections to Claim Construction Memorandum Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 29, 2022) |
| 1052 | File History of U.S. Patent No. 10,860,506 |
| 1053 | Complaint, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (asserting U.S. Patent No. 10,860,506) |
| 1054 | Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 1, 2022) |
| 1055 | First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Aug. 15, 2022) |
| 1056 | Netlist's motion to amend its complaint to assert U.S. Patent No. 10,268,608, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023) |
| 1057 | Netlist's proposed Second Amended Complaint asserting U.S. Patent No. 10,268,608 in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023) |
| 1058 | JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019) |
| 1059 [NEW] | JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (Exhibit 1053 in IPR2022-00711) |

| Exhibit # | Description |
|---|---|
| 1060 | [intentionally omitted] |
| 1061 | [intentionally omitted] |
| 1062 | [intentionally omitted] |
| 1063 | *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022) |
| 1064 | Federal Court Management Statistics (June 30, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2> |
| 1065 | Email from counsel for Samsung to counsel for Patent Owner re: stipulation not to pursue certain invalidity defenses if an IPR proceeding is instituted |
| 1066 | Final Written Decision, *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 34 (PTAB June 20, 2023) (U.S. Patent No. 9,824,035) |
| 1067 | Decision Granting Petitioner's Request on Rehearing of Final Written Decision, *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 36 (PTAB August 16, 2023) (U.S. Patent No. 9,824,035) |
| 1068 | Final Written Decision, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, IPR2022-00711, Paper 42 (PTAB Oct. 17, 2023) (U.S. Patent No. 10,860,506) |
| 1069 [NEW] | S4 and S5 read/write leveling in Hiraishi (EX1005) |
| 1070 [NEW] | S4 read leveling in Hiraishi (EX1005) |
| 1071 [NEW] | S4 write leveling in Hiraishi (EX1005) |

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| 1072 [NEW] | Errata to the deposition of Robert Wedig on March 12, 2024 (EX2012) |
| 1073 [NEW] | Errata to the deposition of Robert Wedig on January 19, 2023, in IPR2022-00711 (EX2016) |
| 1074 [NEW] | Transcript of Deposition of Dr. William Mangione-Smith (June 4, 2024) |
| 1075 [NEW] | Transcript of Deposition of Dr. William Mangione-Smith on May 4, 2023 (Exhibit 1046 in IPR2022-00711) |
| 1076 [NEW] | Declaration of Dr. William Mangione-Smith on January 31, 2023 (Exhibit 2006 in IPR2022-00711) |
| 1077 [NEW] | Netlist's Technology Tutorial (Exhibit 1047 in IPR2022-00711) |
| 1078 [NEW] | Figure 2C of the '608 Patent showing horizontal flight time delays for control and clock signals (EX1001) |
| 1079 [NEW] | Figure 7 in Hiraishi showing horizontal flight time delays for control and clock signals (EX1005) |
| 1080 [NEW] | Figure 15–16 in the '608 Patent (EX1001) |
| 1081 [NEW] | Figure 12 in Hiraishi after S4 write leveling (EX1005) |
| 1082 [NEW] | Figure 15 in Hiraishi and vertical flight time delays for read data (EX1005) |
| 1083 [NEW] | Figure 12 in Hiraishi and vertical flight time delays for write data (EX1005) |
| 1084 [NEW] | U.S. Patent No. 7,215,584 to Butt et al. (incorporated by reference in [0047] of Exhibit 1029) |

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|---|---|
| 1085 [NEW] | Presentation on read leveling and write leveling for DDR3 memory modules (2008) |
| 1086 [NEW] | Netlist's demonstratives for oral argument (Exhibit 2013 in IPR2022-00711) |
| 1087 [NEW] | Dictionary definition for "path" |
| 1088 [NEW] | Inter Partes Review Certificate for U.S. Patent No. 9,824,035 (cancelling claims 1, 10-13, 21, 22) |
| 2001 | Statutory Disclaimer for 15/820,076 |
| 2002 | Power of Attorney and Filing Receipt for 15/820,076 |
| 2003 | IPR2022-00237 IPR Petition |
| 2004 | U.S. Publication No. 2010/0312925 (Osanai) |
| 2005 | IPR2022-00711 Record of Oral Hearing |
| 2006 | IPR2022-00237 DECISION Denying Institution of IPR |
| 2007 | IPR2022-0711 IPR Petition |
| 2008 | U.S. Patent No. 8,713,379 (Takeman) |
| 2009 | IPR2022-00237 Petitioner's Request for Rehearing |
| 2010 | IPR2022-00237 DECISION Denying Petitioner's Request for Rehearing |
| 2011 | IPR2022-00237 Declaration of Donald Alpert, Ph.D. |
| 2012 | Deposition Transcript of Robert Wedig |
| 2013 | Declaration of Dr. William Mangione-Smith |
| 2014 | JEDEC STANDARD, DDR2 SDRAM SPECIFICATION (JESD79-2F) (November 2009) (Exhibit 2002 in IPR2022-00711) |

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|---|---|
| 2015 | JEDEC STANDARD, DDR3 SDRAM Standard (JESD79-3F) (Revision of JESD79-3E, July 2010) (July 2012) |
| 2016 | Deposition of Robert Wedig in IPR2022-00711 (506 IPR) |
| 2017 | Electronics Cooling, Challenges In Thermal Management Of Memory Modules |
| 2018 | JEDEC STANDARD, Double Date Rate (DDR) SDRAM Specification (JES79) (June 2000) |
| 2019 | JEDEC STANDARD, DDR3 SDRAM Specification (JESD79-3A) (Revision of JESD79-3) (September 2007) |
| 2020 | Petition for Inter Partes Review of U.S. Patent No. 10,860,506 (IPR2022-00711) |
| 2021 | Final Written Decision (IPR2022-00711) |
| 2022 | DECISION Denying Patent Owner's Request on Rehearing of Final Written Decision (IPR2022-00711) |
| 2023 | Final Written Decision (IPR2022-00236) |

## CLAIM LISTING

| Ref. # | Listing of Challenged Claims |
|---|---|
| **1[pre]** | 1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: |
| **1[a]** | a module board having edge connections for coupling to respective signal lines in the memory bus; |
| **1[b]** | a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and |
| **1[c]** | memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and |
| **1[d]** | a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, |
| **1[e]** | wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, |
| **1[f]** | wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. |

| Ref. # | Listing of Challenged Claims |
|---|---|
| **2[a]** | 2. The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, |
| **2[b]** | wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, |
| **2[c]** | wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, |
| **2[d]** | wherein the at least one of the module control signals include at least one of the first set of module control signals, and |
| **2[e]** | wherein the signal through the data path is a signal associated with the second memory operation. |
| **3[a]** | 3. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, |
| **3[b]** | wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and |
| **3[c]** | wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation. |
| **4** | 4. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte. |
| **5** | 5. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits. |

| Ref. # | Listing of Challenged Claims |
|---|---|
| ~~6~~[†] | 6. The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal. |
| ~~7~~ | 7. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte. |
| ~~8~~ | 8. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits. |
| ~~9[a]~~ | 9. The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, |
| ~~9[b]~~ | wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices. |
| ~~10[a]~~ | 10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, |
| ~~10[b]~~ | the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal. |
| ~~11~~ | 11. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte. |
| ~~12~~ | 12. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits. |

[†] Claims 6-12 were disclaimed after the Petition was filed. *See* EX2001.

# I. INTRODUCTION

Netlist's Patent Owner Response ("POR") merely repeats arguments already rejected by the Institution Decision ("ID") and previous Final Written Decisions against Netlist.

# II. ARGUMENT

## A. Ground 1 (POR 1-4, 18-58)

### 1. Netlist's attempt to exclude "strobe signal lines" from the claimed "*data path*" (POR 1-4, 18-40) is precluded by the Final Written Decision in IPR2022-00236 (EX1066)

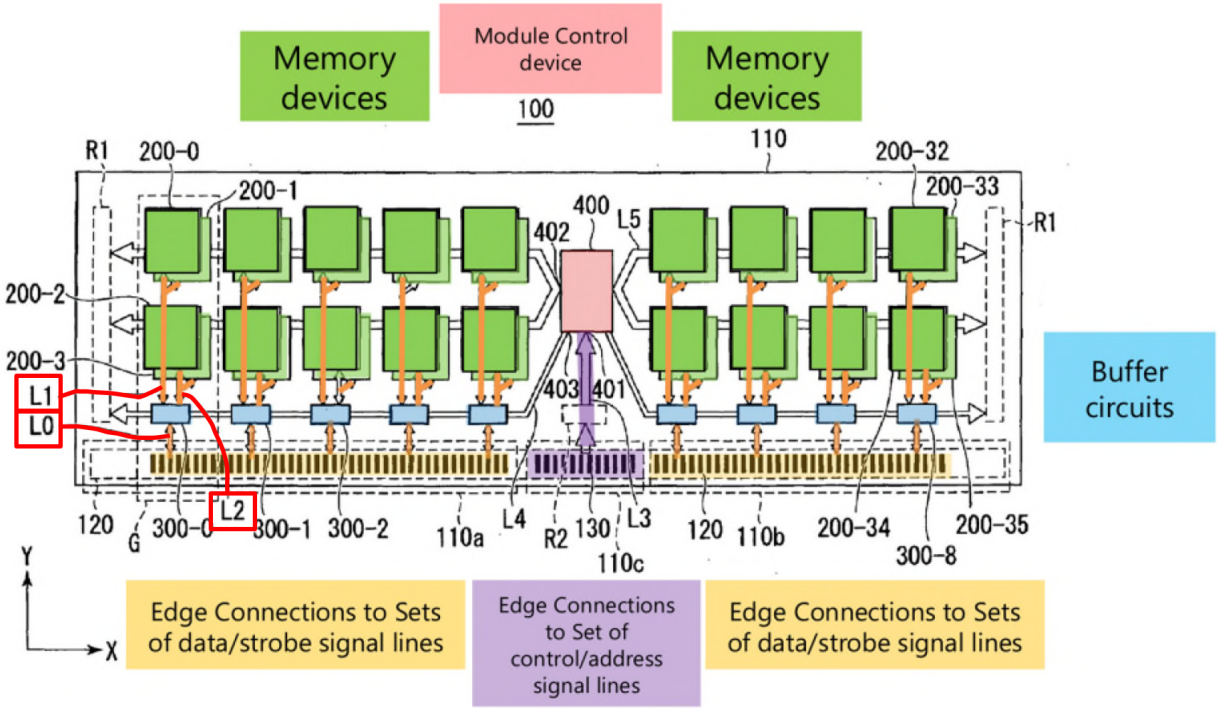
Netlist's attempt to exclude "strobe signal lines" from the claimed "*data path*" (POR 1-4, 18-40) is precluded by the Board's recent Final Written Decision in IPR2022-00236 involving the '035 patent, EX1031; Pet. 6, which is the parent of the '608 Patent here and expressly claims strobe signals on the "*data paths*":

| **IPR2022-00236 ('035 Patent)**<br>EX1066, 5-7, 22-43, 46-52; EX1067 | **'608 Patent**<br>Pet. 39-53, 98-101 |
|---|---|
| [**1.j**]…***control timing of the respective data and <u>strobe</u> signals on the <u>data paths</u>***….[1] | [**1.f**]…***delay circuit configured to delay a signal through the <u>data path</u>***…. |

In IPR2022-00236, the Board relied on "Osanai," EX2004, which Netlist admits is "the same as Hiraishi [EX1005 in this IPR] in all material respects." Paper 6, p.5. The Board specifically found that "the read and write leveling circuits of [<u>Hiraishi</u>]

[1] All emphases in quotes and color annotations in figures have been added.

make timing adjustments," in response to the "DRC" module control signal, "so that ***[data and strobe] signals*** between the memory chips and the data register buffer are sent at the appropriate time," and "these disclosures of [Hiraishi] are sufficient to teach ***controlling the timing of data and strobe signals on the data paths*** on which those signals travel." EX1066, 35-36, 52. The "data paths" the Board relied upon include what Samsung relies upon here. Specifically, the Board found that "each buffer circuit…includes ***data paths*** for transmitting ***data and strobe signals***" and "[t]hese ***data paths connect lines L0 to lines L1 and L2***." EX1066, 35; *see also id*. 25-26. The Petition relied on these same data paths connecting L0 to L1/L2 (highlighted in orange):



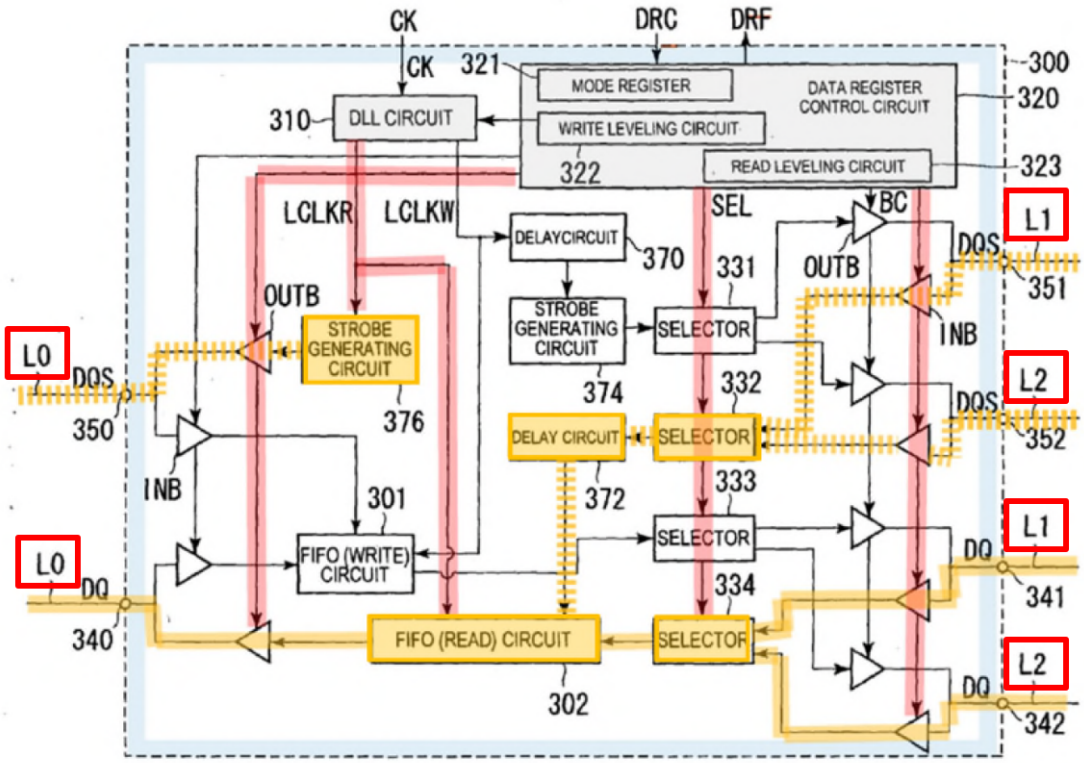

CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
SEL
BC
L1
DELAYCIRCUIT
370
331
OUTB
DQS
351
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
L0
DQS
350
374
332
L2
DQS
352
376
DELAY CIRCUIT
SELECTOR
INB
372
333
301
SELECTOR
L1
L0
FIFO (WRITE) CIRCUIT
DQ
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
302
342

FIG.5

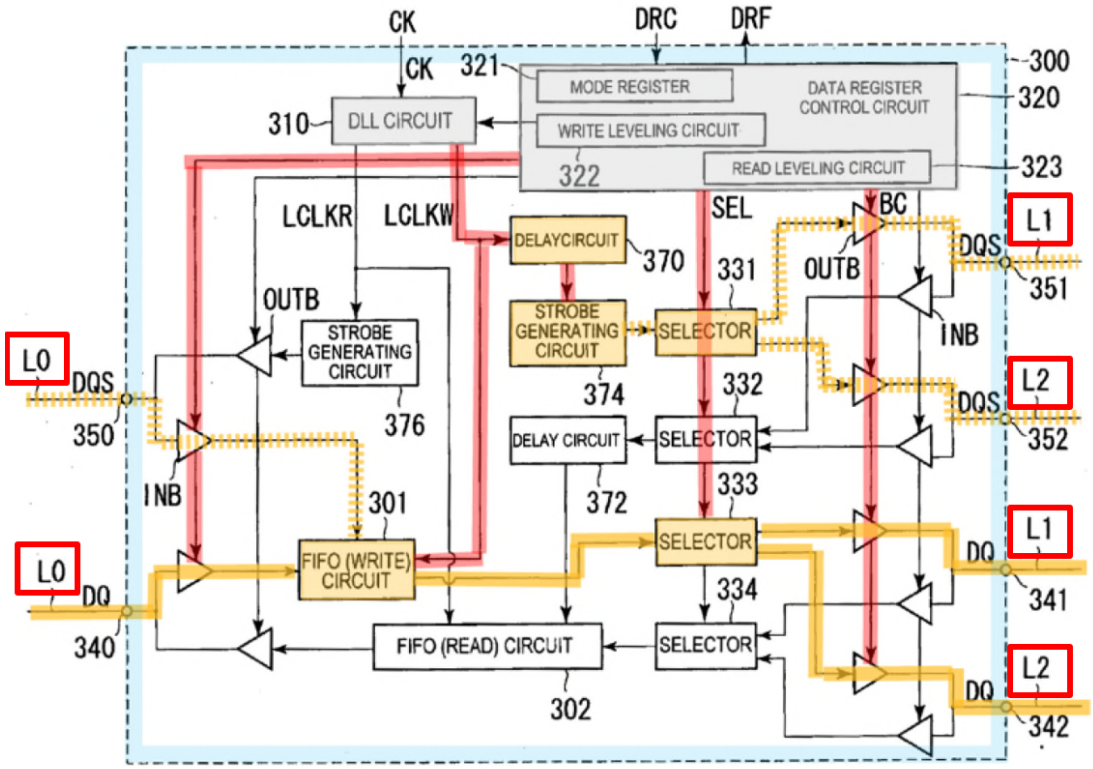

CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
SEL
BC
L1
DELAYCIRCUIT
370
331
OUTB
DQS
351
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
L0
DQS
350
374
332
L2
DQS
352
376
DELAY CIRCUIT
SELECTOR
INB
372
333
301
SELECTOR
L1
L0
FIFO (WRITE) CIRCUIT
DQ
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
302
342

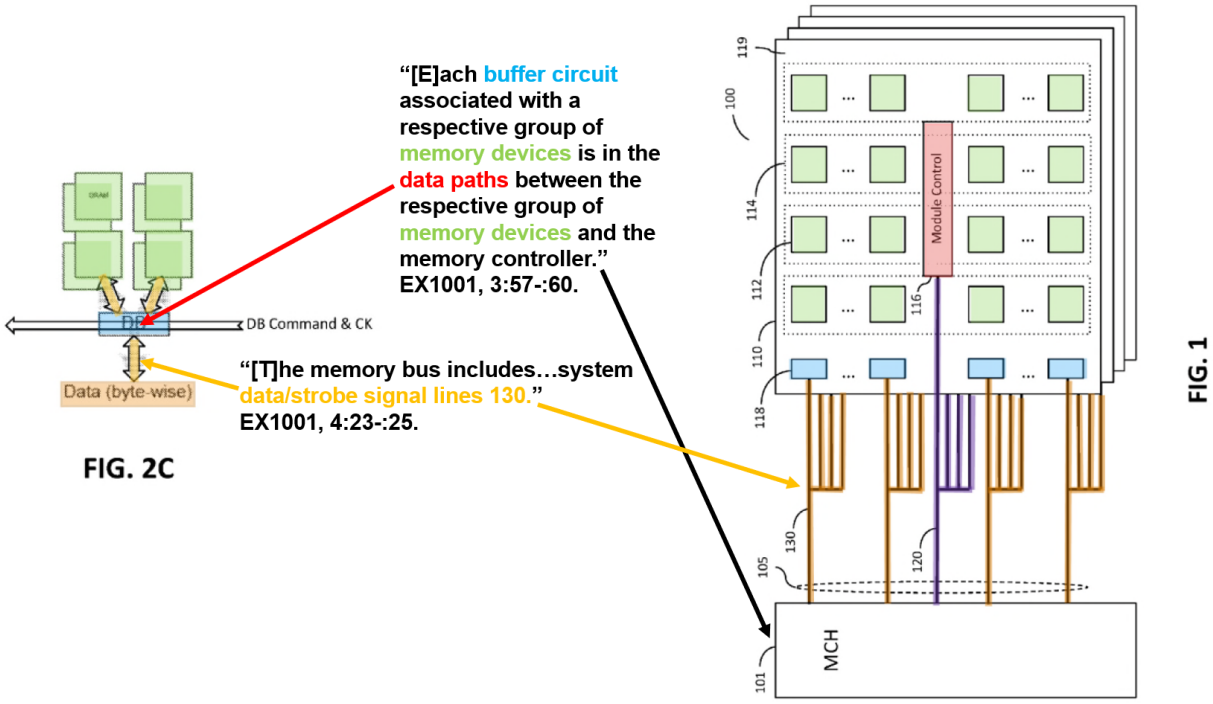
FIG.5

Pet. 15, 33-35; ID 26-27; EX1003, ¶¶142-47; EX2012, 39:7-41:1, 44:22-46:2, 52:8-53:9, 113:24-120:1, 134:8-137:22.

The Board's Final Written Decision above (and the cancellation of claims 1, 10-13, and 21-22 of the '035 patent, EX1088) precludes Netlist's arguments here. *See* 37 C.F.R. §42.73(d)(3); *Google LLC v. Hammond Dev. Int'l, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022); *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, 11-17, 18-19, 33 (PTAB July 16, 2019); *see also B & B Hardware, Inc. v. Hargis Indus., Inc.*, 575 U.S. 138, 148 (2015) (following the Restatement); Restatement (Second) of Judgments §§13, 27; *SSIH Equip. S.A. v. ITC*, 718 F.2d 365, 370 (Fed. Cir. 1983).

### 2. The claimed "*data path*" includes strobe signals, as confirmed by dependent claim 10, the related '035 patent in IPR2022-00236, and the ordinary meaning in the art as shown by <u>Butt</u> and <u>Hiraishi</u> (POR 18-26)

Netlist improperly tries to conflate the claimed "*data path*" in limitation [1.e] with the "*data signal line*," which is a separate limitation in [1.pre]. POR 18-26. As shown by the annotations of the '608 Patent below, the claimed "*data path*" through the "*buffer circuit*" (in blue) is ***not*** the claimed "*data signal line*," which is a physical wire below it (e.g., "data/strobe signal lines 130" in orange):



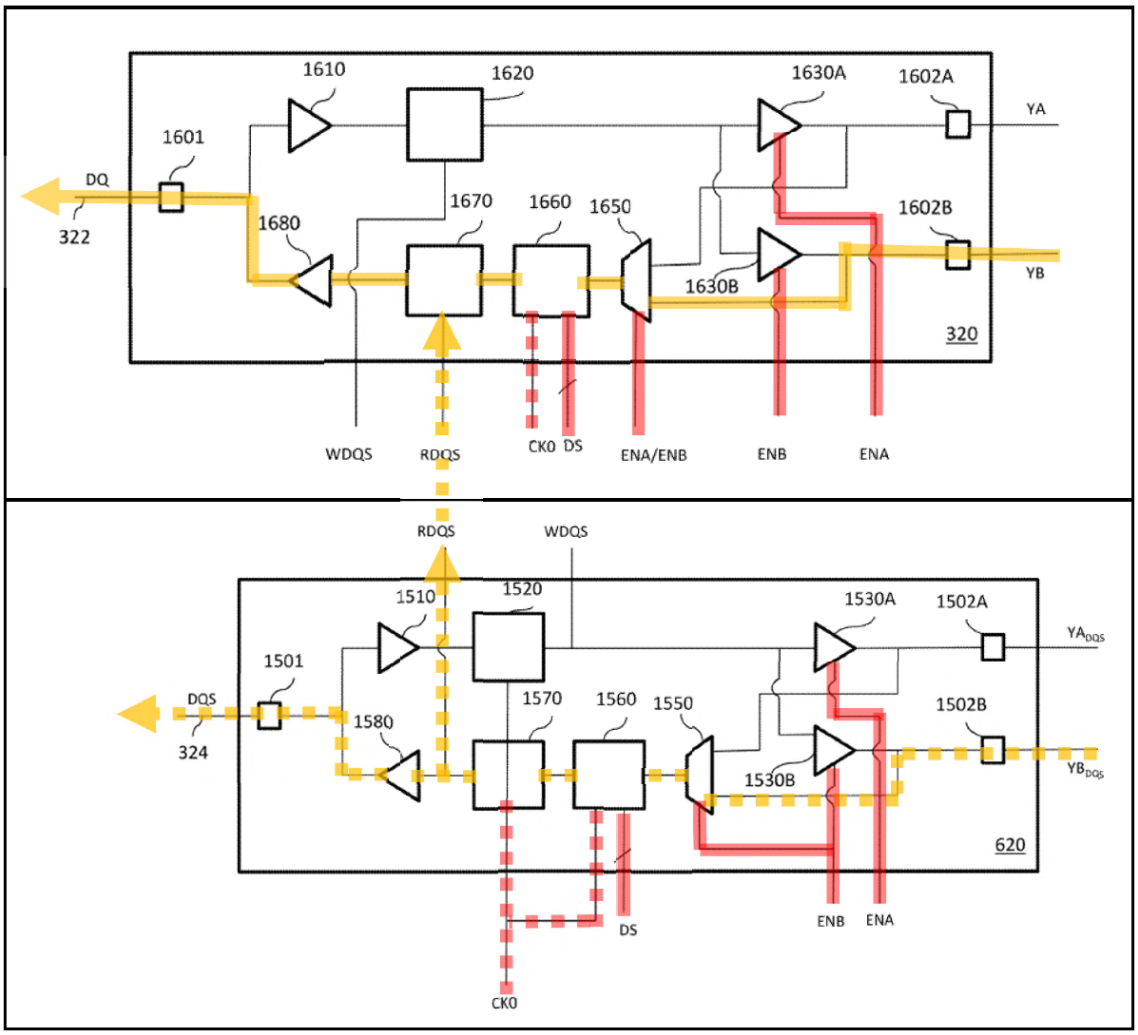

Pet. 3-4; EX1001, 3:57-:60, 4:23-:25, Figs.1, 2C. While the claimed "*data path*" through each "*buffer circuit*" illustrated above "***correspond[s]*** *to each data signal line*" as required by [1.e], that does not mean the "*data path*" ***is*** a "*data signal line*" as Netlist suggests. POR 20-23. To the contrary, a "*data path*" is a broader concept, consistent with the dictionary definition for "path," which is "the course or direction in which a…thing is moving," EX1087. And consistent with that broad concept, as the specification explains, "***each buffer circuit*** [blue above]…***is in the data paths*** between the respective group of memory devices [green above] and the memory controller [MCH at the bottom above]." EX1001, 3:57-:60; *see also id.* 6:59-:62, 15:17-:19 (same); EX2012, 47:20-48:2.

Consistent with the specification above, which teaches that the ***entire*** buffer

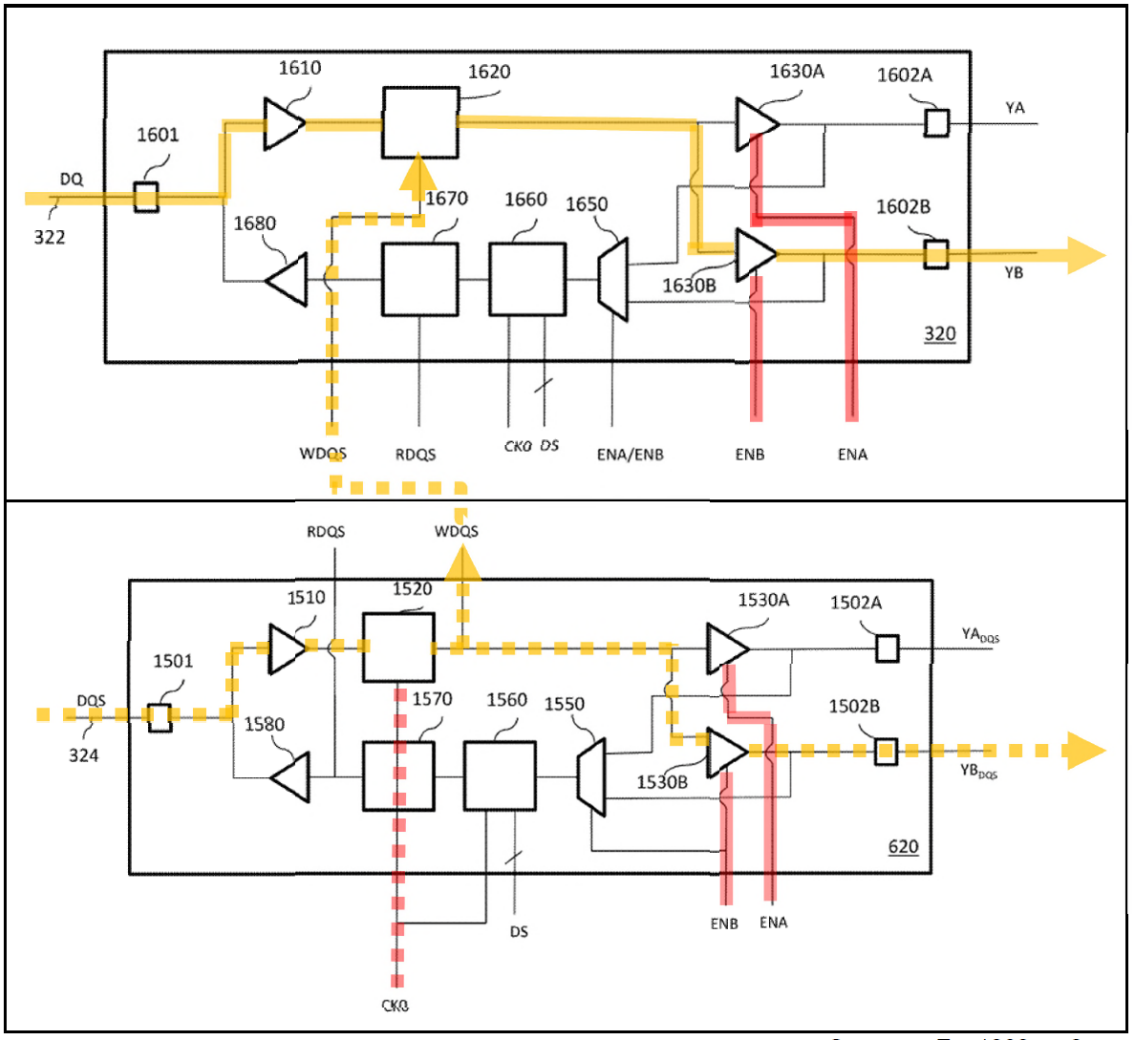
circuit is in the "data path," dependent claim 10 directly refutes Netlist's argument that the "*data path*" cannot include "data strobe signal lines": "wherein the each respective buffer circuit includes a first ***data path*** ***for transmitting a strobe signal***…." Pet. xv, 67-71; EX2012, 45:7-46:2, 49:22-50:13, 144:22-145:10. An example of such a buffer circuit is shown in Figure 3, which Netlist admits includes ***both*** DQ data signals ***and DQS strobe*** signals going through the buffer, *see* POR 21; EX1001, 2:46-:47, 8:4-:8, 10:31-:61. Claim [1.j] of the related '035 patent discussed above (p.1) also refutes Netlist's argument: "***data and strobe signals on the data paths***." EX1031, 19:44. And Netlist's own expert admitted that the related '506 patent (EX1046, a continuation of the '608 Patent) discloses "***a strobe signal through the data path***." EX1076, ¶34; EX1074, 20:24-22:11.

Netlist argues its construction is supported by Figures 15-16 (which, like Figure 3, illustrate an exemplary buffer circuit, EX1001, 3:11-:13). POR 22-23. That is incorrect. Figure 15-16 are shown below:

## Read direction — ’608 Patent (EX1001) Figures 16 & 15



**Write direction — '608 Patent (EX1001) Figures 16 & 15**



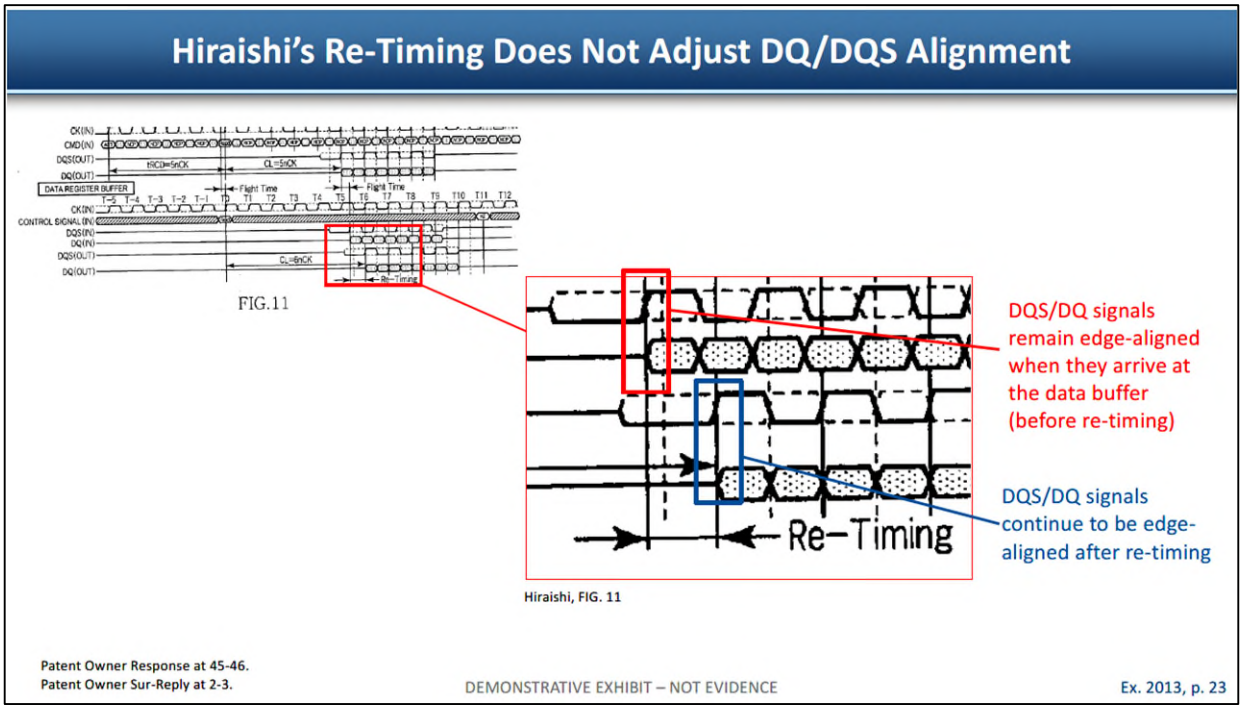

EX1080, 1-2; EX1074, 146:3-147:9, 173:7-174:2; EX1001, 16:47-17:60 & Figs.15-16; Pet. 67-71. Netlist argues that Figures 15-16 above distinguish between the "***[first]/[second] [read]/[write] <u>data</u> path[s]***," shown as a solid orange horizontal line above, and the "***[first]/[second] [read]/[write] <u>strobe</u> path[s]***," shown as a dashed orange horizontal line above. POR 21-22. But those are just ***eight subparts*** of the broader "*data path*" through the buffer circuit, which includes ***both*** data ***and*** strobe signals that travel together (as shown by the orange

arrows above), and ***all eight*** subparts of the "*data path*" through Figures 15-16 "*correspond[]*" to the "*data signal line*" (322 above left) "*in the respective set of data/strobe signal lines*" (322 and 324 above left), as required by [1.e]. Furthermore, the Federal Circuit has "repeatedly warned against confining the claims to [specific] embodiments," such as Figure 16, especially when the specification uses the term "data path" more broadly as discussed above (pp.4-6). *Weber, Inc. v. Provisur Techs., Inc.*, 492 F.4th 1059, 1070 (Fed. Cir. 2024) (reversing narrow construction).

Netlist's attempt to divorce the claimed "*strobe signal*" from the "*data path*" is contrary to the testimony of both experts that it was known in the art that the strobe signal (DQS) is ***essential*** to the transmission of the data signal (DQ), which is why both signals ***must travel together*** within a "***very tight tolerance***." EX1074, 134:4-136:24, 137:8-138:3, 139:13-:24 (discussing EX1020, 59, 164);[2] EX1074, 141:11-142:19 (discussing EX1020, 68); EX1074, 91:10-:24, 92:16-93:13, 99:3-100:4 (discussing EX1021, 333-34); EX2012, 51:22-52:7, 54:8-55:10 ("essential").

[2] Netlist's expert agreed a POSITA would be familiar with EX1020, the JEDEC standard for DDR3 memory devices. EX1074, 29:10-30:10, 42:1-47:21 (discussing EX2014, EX2015, EX2018, EX2019, EX1020, EX1059, EX1018), 49:20-54:15 (discussing EX1077, 3-6 and EX2015, 141).

Netlist itself admits that "DQS signals…***ensur[e]*** accurate timing for sampling/capturing DQ data," POR 6, and Netlist has argued that the DQ/DQS signals ***must*** remain aligned with each other:




EX1086, 22-23.

Consistent with the above knowledge, the Butt prior art reference expressly teaches that a "data path" (e.g., 114 below) includes ***both*** a DQS strobe signal (dashed orange) ***and*** the corresponding DQ data signals (solid orange):

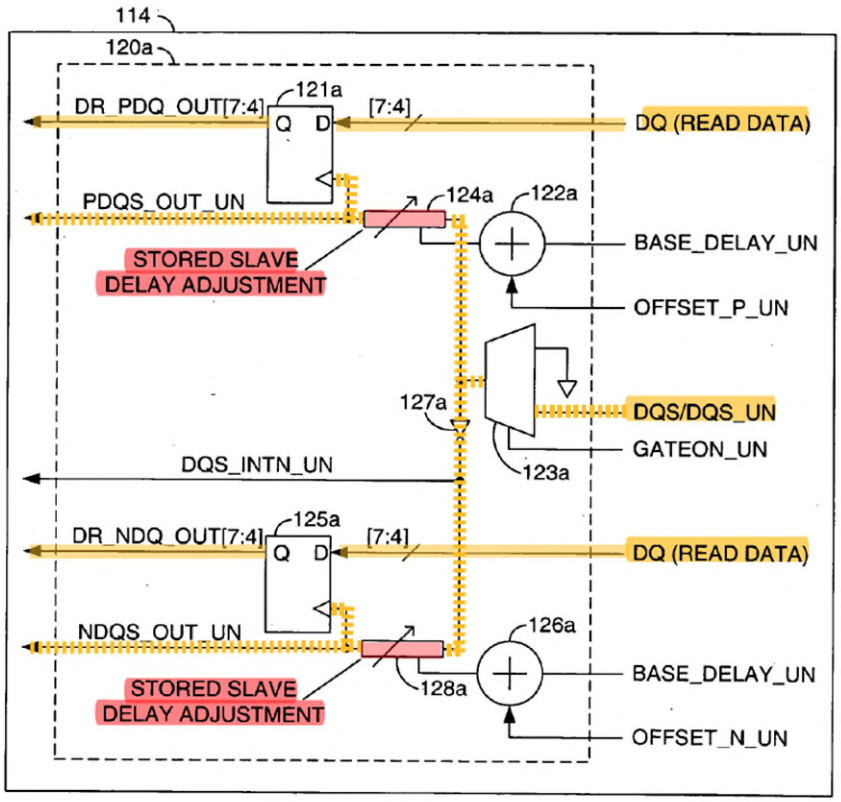



FIG. 3A

Pet. 36; EX1029, Figs.2-3, [0017]; EX1074, 179:22-181:14. Similarly, the Hiraishi prior-art reference expressly teaches that "***data*** lines" L0, L1, and L2 (below, and also discussed above, pp.2-3) include ***both*** DQS strobe signals (below right) ***and*** the corresponding DQ data signals (below left):

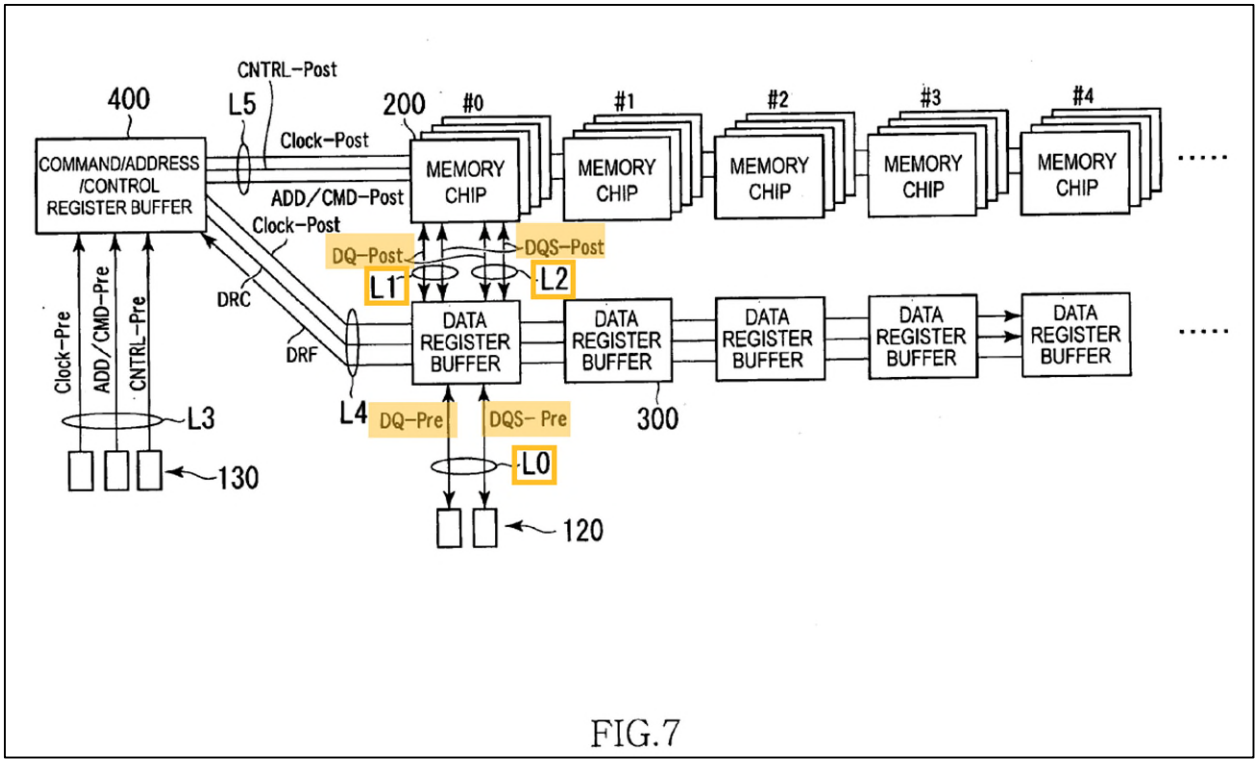



FIG.7

EX1005, [0103], Fig.7; Pet. 32-34; EX1074, 225:11-226:4.

For at least these reasons, Netlist's attempt to exclude "strobe signal lines" from the claimed "*data path*" is incorrect.

### 3. Even under Netlist's narrower construction, Ground 1 renders obvious a "*delay circuit*" (e.g., the FIFOs in Hiraishi and Butt), in the "*data path*," that delays DQ data signals through that "*data path*," by an amount determined in response to "*module control signals*" (e.g., DRC) (POR 26-40)

Netlist argues that Hiraishi's "*delay circuit*" is not on the "*data path*" under Netlist's narrow construction that excludes "strobe signals lines." *See* POR 26-40. But that construction is incorrect, as explained above (pp.1-12). Furthermore, even under Netlist's narrow construction that focuses on the ***data*** signals (and ignores

the related strobe signals), the Board has already ruled against Netlist on this issue and concluded that Hiraishi teaches "***controlling the timing of data and strobe signals on the data paths***" as part of read and write leveling in response to the "DRC" module control signal, EX1066, 35-36, 52, which is now binding against Netlist as discussed above (pp.1-4). Indeed, as the Petition illustrated below, Hiraishi's Figure 5 (first below), which Netlist does not dispute delays the DQ data signals (solid orange line), directly corresponds to what Netlist identifies as the preferred embodiment of the "*delay circuit*" on the "*data path*" (Figure 16 of the '608 Patent, second below), *see* POR 27.

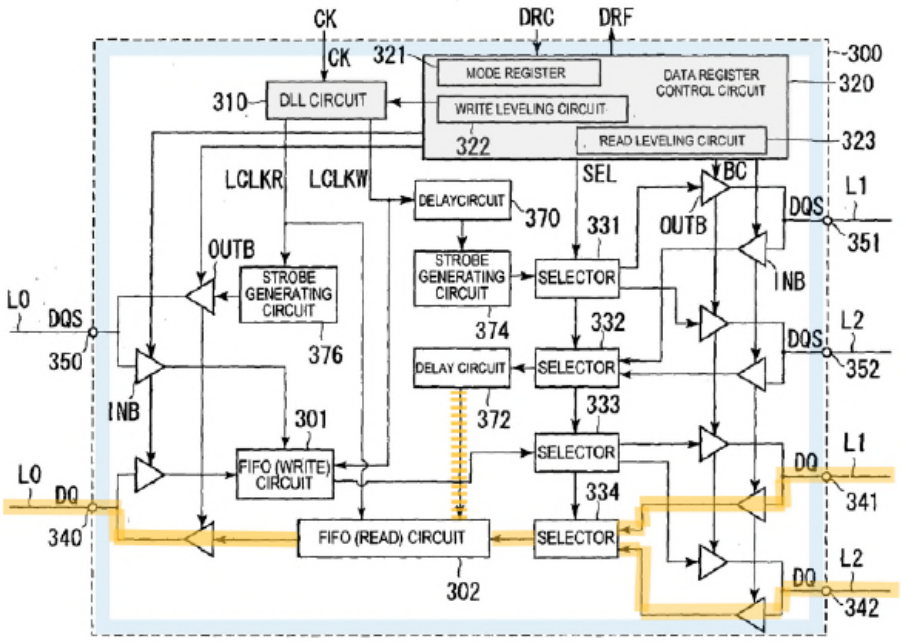



FIG.5

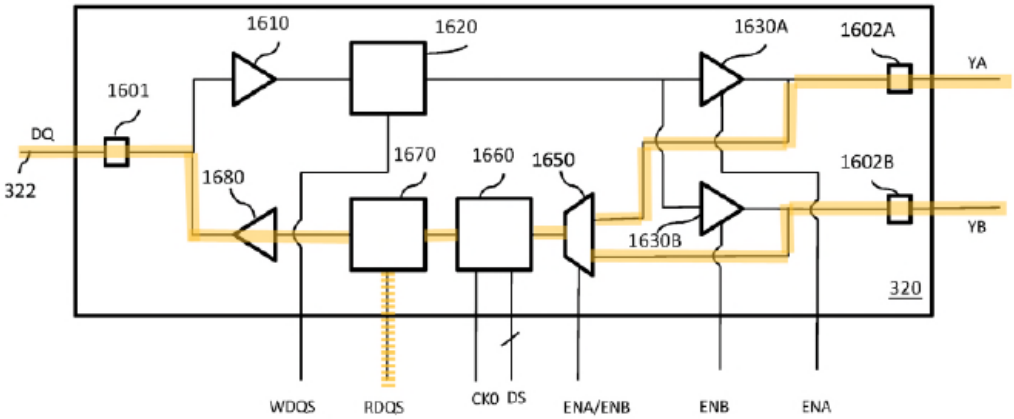



**FIG. 16**

Pet. 70; EX1080, 1; EX1074, 150:9-151:8, 153:2-155:19, 173:7-:15. The annotation above is for the read direction, but Hiraishi's Figure 5 also matches Figure 16 of the '608 Patent in the write direction, *see* Pet. 47; EX1080, 2; EX1074, 160:21-161:23, 173:16-174:2. Thus regardless of how exactly Netlist

tries to construe "*data path*" or "*delay circuit*," Hiraishi's Figure 5 above renders obvious that claim language because it is substantially identical to Figure 16 of the '608 Patent, which Netlist admits embodies the claim language, *see* POR 27.

For example, as shown above, Hiraishi's Read FIFO 302 is on the DQ data line and delays the DQ data signal, thus satisfying even Netlist's unreasonably narrow construction of "*data path*" and "*delay circuit*." Pet. 48-53; EX1005, [0130] ("re-timing…using the FIFO (Read) circuit 302"). The same is true in the write direction. Pet. 39-47; EX1005, [0135] ("re-timing…using the FIFO (Write) circuit 301").

In response, Netlist goes through an elaborate line-drawing exercise to argue that ***other necessary components*** connected to Hiraishi's FIFOs 301/302 above — including delay circuit 370/372, strobe generating circuit 374/376, and DLL circuit 310 — are not drawn as being physically on top of the DQ data line, and thus supposedly are not "on" the "*data path*." POR 28-40. But the same is true of Figure 16 of the '608 Patent, where ***other necessary components*** connected to 1660/1670 (in the read direction) and 1620 (in the write direction) are not drawn as being physically on top of the DQ data line, including all of Figure 15 (which generates and supplies the WDQS and RDQS signals that control the delay in 1620 and 1670, *see* EX1080; EX1074, 150:9-151:8, 154:6-155:19, 160:21-161:23, 163:8-:24), and various components in Figure 6 (which generate and supply the

CK0 and DS signals that control the delay in 1660, *see* EX1001, 12:3-:37, Fig.6; EX1074, 153:2-154:5, 163:8-:24, 168:23-170:7). Thus, the more reasonable interpretation of the claim language, as taught by the '608 Patent, is that the "*delay circuit*" does not need to be ***entirely*** physically on top of the DQ data line, and that the term "*data path*" is broad enough to include the "*delay circuit*" no matter where it is physically located within the buffer circuit. Pet. 39-53; EX2012, 134:8-137:22; EX1057, 58 ("example…delay circuit"). But even under Netlist's unreasonably narrow construction, Hiraishi's FIFOs 301/302 are physically on the DQ data line that they are delaying, as discussed and shown above (pp.14-15), rendering obvious a "*delay circuit*" on the "*data path*."

Furthermore, Netlist completely ignores Butt, *see* POR 27-28, which is part of Ground 1 and which further renders obvious a "*delay circuit*" (including FIFOs 112 in Figure 2 of Butt) in the "*data path*," *see* Pet. 33-41 ("a POSITA…would have been motivated to implement Butt's ***data path*** controlling technique in Hiraishi's data register buffer"); EX1029, Figs.2-3; EX1074, 181:19-183:1, 184:1-190:7, 199:2-200:2, 201:14-202:5; EX1084, Figs.2-3, 14.

Netlist also contends that Hiraishi's FIFOs 301/302 do not delay the data signal "*by an amount determined by the command processing circuit* ***in response to*** *at least one of* ***the module control signals***" as required by [1.f]. POR 29-31, 34, 36, 37, 39. But the Board has already rejected this argument, correctly concluding

that the "DRC" signal identified in the Petition (shown below in a brown box) causes Hiraishi's data buffer to perform read and write leveling, which determines the amount of delay that is applied to the "***data and strobe signals on the data paths***." EX1066, 35-36, 52; Pet. 44-47 ("write leveling…performed during initialization in response to ***module control signals (e.g., DRC*** conveying 'mode switching' or 'mode register set' commands)"),[3] 48-51 (similar for read).

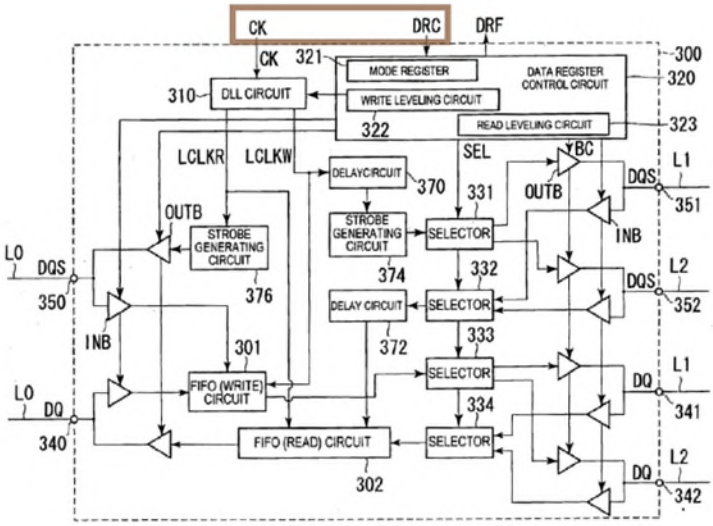



FIG.5

[3] A "Mode Register Set" (MRS) command was the standard command in the JEDEC DDR3 standard to perform read and write leveling during initialization (before normal operation). EX1074, 104:21-107:8 (discussing MRS command, EX1020, 18-19, 33), 119:20-123:7 (discussing write leveling, EX1020, 26, 42), 123:8-128:21 (discussing read leveling, EX1020, 31, 48, 50-51), 79:23-80:14, 89:6-90:9 (discussing need in DDR3 for read and write leveling, EX1085, 7, 9).

Pet. 32-33.

Netlist incorrectly suggests that the claim language "*in response to*" could only be satisfied if Hiraishi's "*module control signals*" (e.g., DRC) are connected ***directly*** to each and every component of the "*delay circuit*," including the FIFOs 301/302. POR 29-31, 34, 36, 37, 39. But claim [1.f] only requires that the "***amount [of delay] determined by the command processing circuit*** [e.g., Data Register Control Circuit 320, *see* Pet. 37-51] ***[be] in response to*** *at least one of the module control signals* [e.g., DRC]," not that every component of the "*delay circuit*" must respond ***directly*** to DRC ("*module control signals*"). As explained in the Petition, there is a two-step process that satisfies [1.f]: First, during initialization, the DRC signal causes the Data Register Control Circuit 320 to perform S4 read/write leveling, which determines and stores the ***variable***[4] amount of delay needed (as shown in Figures 14-15 of Hiraishi), and second, during normal operation (e.g., in response to a read/write command transmitted via DRC), that stored delay amount is used to control the "*delay circuit*" to delay (i.e., "re-tim[e]") both the DQ data signals (e.g., using the FIFOs 301/302) and the DQS

[4] The delay is not "fixed," as incorrectly stated by Netlist, POR 30, 37-38, but instead ***varies*** depending on the "flight time" of the data and strobe signals, as explained in the Petition and discussed further below (pp.20-32).

strobe signals associated with that normal read/write command (as shown in Figures 11-12 of Hiraishi). Pet. 37-51; EX1070 (Figures 11 & 15); EX1071 (Figure 14); EX1081 (Figure 12).

Again Hiraishi's disclosure is very similar to the '608 Patent, which discloses "*module control signals*" ("DB Command Signals (MCS)" in Figures 6 and 19, below right) that do ***not*** connect directly to the "*delay circuit*" in Figure 16 (which according to Netlist is 1660/1670 in the read direction, and 1620 in the write direction, *see* POR 27). Instead, the alleged "*delay circuit*" in Figure 16 is directly controlled by WDQS, RDQS, CK0, and DS — similar to the strobe signals and the LCLKR/LCLKW clock signals that control Hiraishi's FIFOs 301/302.

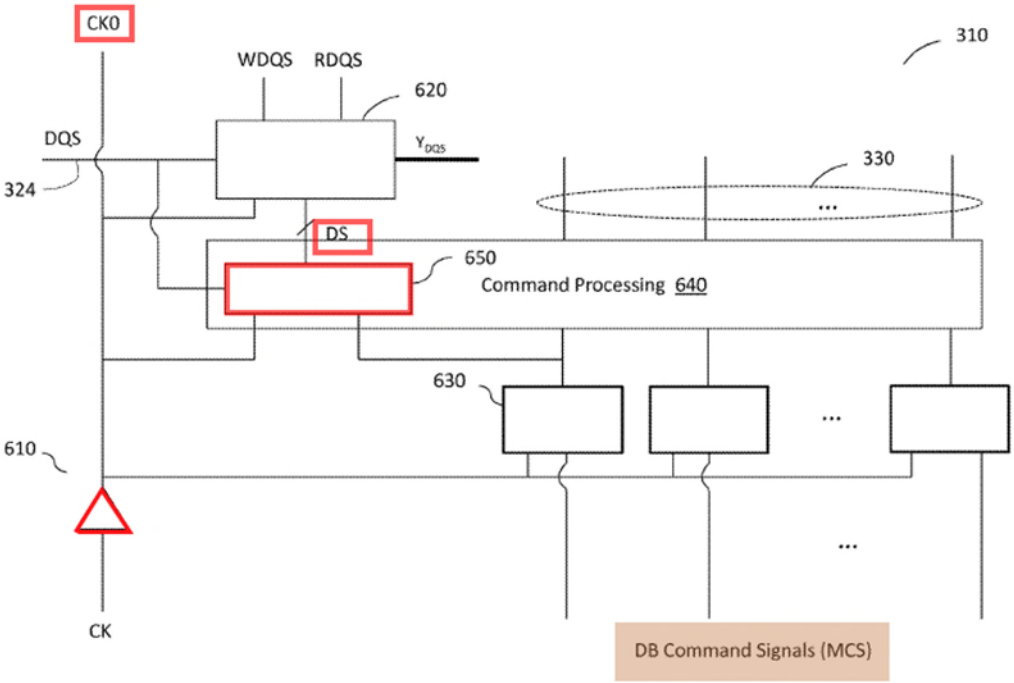



**FIG. 6**

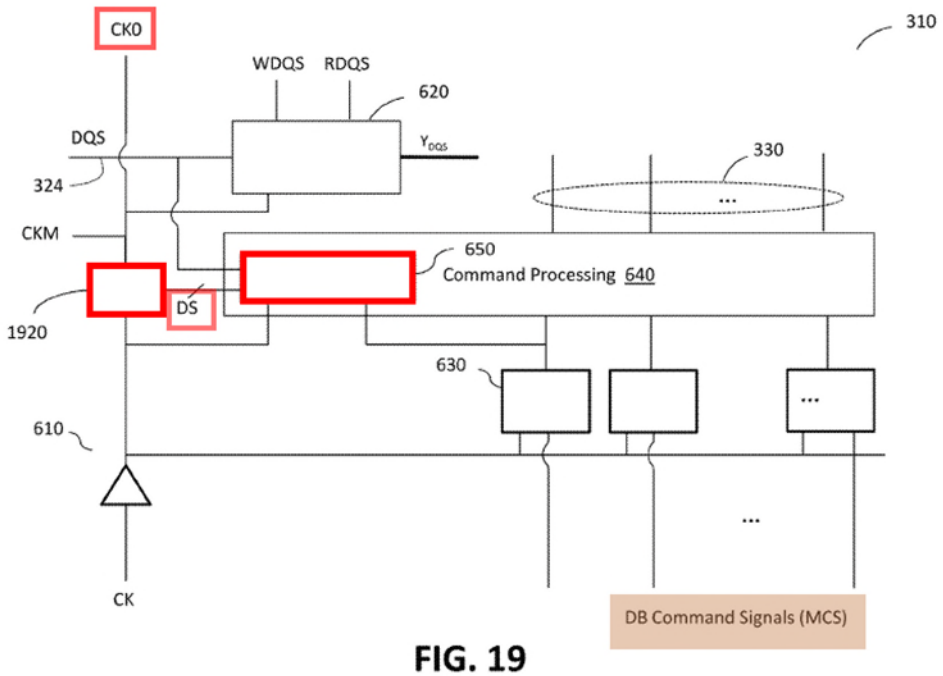


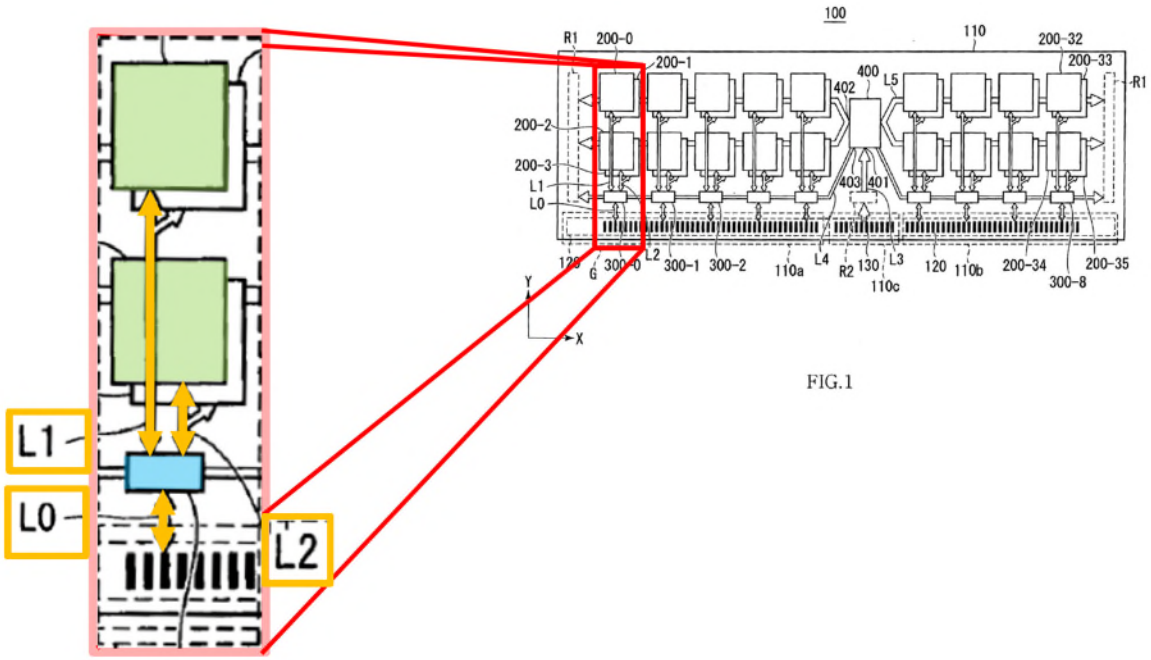

FIG. 19

EX1001, 12:3-:37, 18:65-19:11, Figs. 2C, 6, 19; EX1074, 167:4-173:3.

### 4. The "re-timing" by Hiraishi's data buffer is the result of S4 read/write leveling, which does not simply add one clock cycle of latency (POR 40-58)

Netlist incorrectly asserts that Hiraishi's S4 read/write leveling simply causes the data buffer to add a ***fixed*** delay of one clock cycle. POR 40-58. That is completely wrong, as explained in detail by the Petition, Pet. 39-53, and admitted by Netlist's expert as discussed below.

S4 read/write leveling by the data buffer (blue below) determines a ***variable*** amount of delay, which is needed because data line L1 to the upper memory chip is longer than data line L2 to the lower memory chip, as shown in orange below, resulting in longer "flight time" delays for the DQ data and DQS strobe signals:




*See* Pet. 31-32; EX1005, [0055-56], Fig.1. Netlist's expert concedes that the vertical "flight time" delay for L1 will be greater than for L2. EX1074, 208:3-:15, 210:24-211:22, 217:2-:16, 223:20-224:4.

As shown in Figures 14-15 of Hiraishi, during ***initialization***, S4 read/write leveling ***measures*** the different vertical delays (e.g., "Flight Time" in green below), as Netlist's expert admitted:

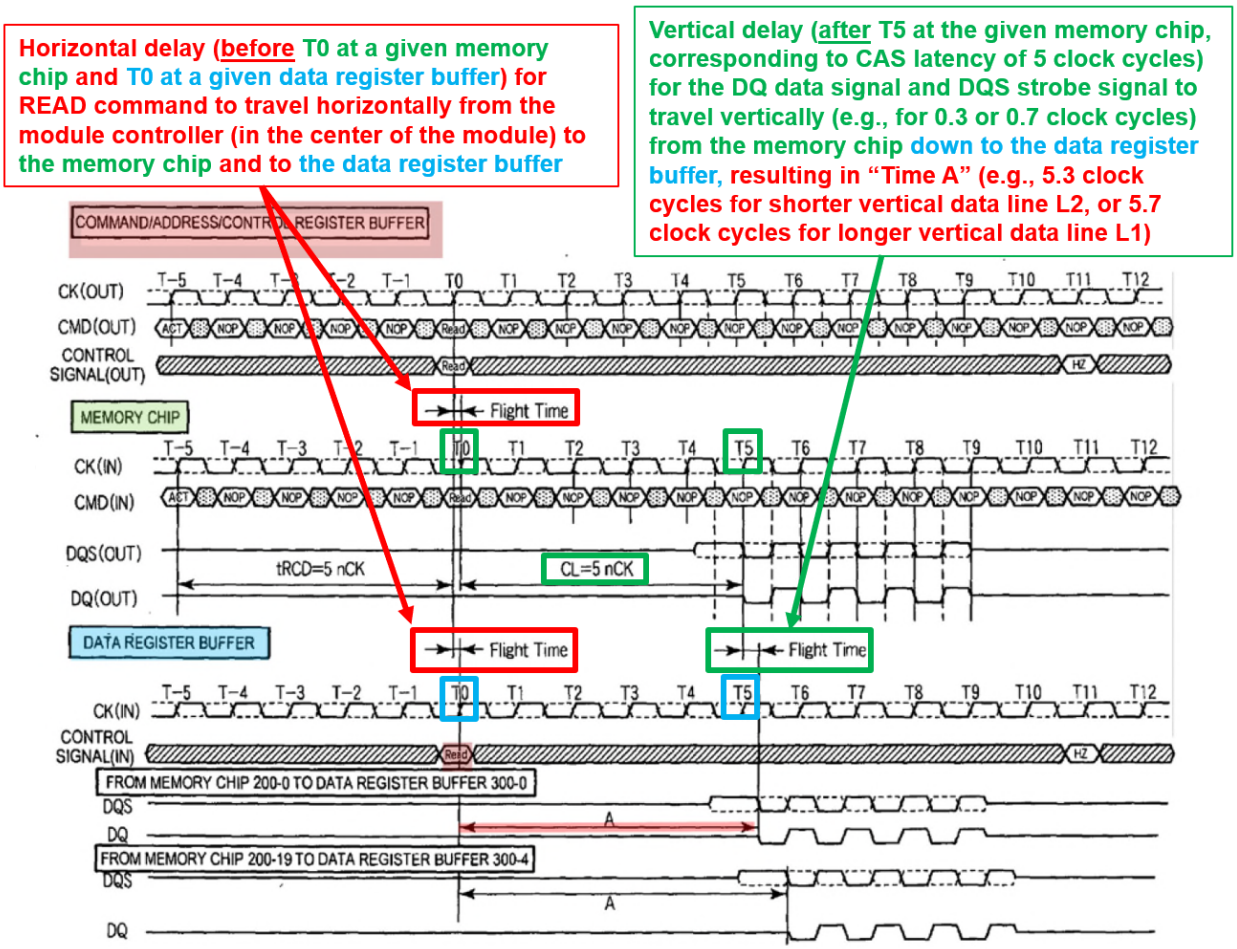



FIG.15

Pet. 75 (annotated with admissions by Netlist's expert, EX1074, 218:8-224:4);[5] *see*

[5] The numbering for the groups of memory chips and data buffers is different in Figures 1 and 7. EX1003, 83 n.2; EX2012, 120:8-122:14; EX1074, 224:13-225:10. But it is clear that a shorter "flight time" delay corresponds to the shorter data line L2, not the longer data line L1. EX1074, 208:3-:15, 217:2-:16, 223:20-224:4.

*also* Pet. 48-49; EX1070; EX1074, 214:17-215:17; *supra* p.17, note 3. The DQ data and DQS strobe signals travel together on L1 or L2 as discussed above (pp.9-12), so for purposes of ***measuring*** the vertical "flight time" delay for S4 write leveling, it is sufficient to just measure the delay for the DQS strobe signal, *see* EX1071 (Figure 14).[6]

The delays measured by S4 read/write leveling are then "stored" in Data Register Control Circuit 320 for future use by the "*delay circuit*" during normal operations. EX1005, [0146], [0151] ("stored"); Pet. 45-46, 49-50.

Then, as shown in Figures 11-12 of Hiraishi, the previously "stored" delays are used by the "*delay circuit*" in the data buffer during normal read/write operations to "re-tim[e]" ***both*** the DQ data ***and*** DQS strobe signals (since they must stay aligned, as Netlist admitted above, pp.9-12). *See* EX1070 (Figure 11); EX1081 (Figure 12); EX2012, 63:25-64:12. Netlist concedes "read leveling adjusts the timing of when the input buffers INB are turned on," but suggests read/write leveling does not also delay the DQ data and DQS strobe signals using

[6] Netlist incorrectly asserts the "Petition…does not explain how [write leveling in Figures 14A-B] suggest delaying ***DQ [data]*** signals." POR 41. That is shown by Figure 12, discussed below and in the Petition, Pet. 46 ("showing 'Re-timing' (blue box) of both ***data*** and strobe"); EX1081.

the Read/Write FIFOs. POR 53-54. That is incorrect. EX1005, [0130], [0135] ("re-timing…using the FIFO"); Pet. 39-51. For example, as illustrated in more detail in the figures below, if the "flight time" delay on L2 was measured as 0.3 clock cycles, then the data buffer adds a delay of 0.7 clock cycles to ***both*** the DQ data ***and*** DQS strobe signals, resulting in a combined delay of 0.7+0.3=1.0 clock cycle for the signals to travel across L2 ***and*** across the buffer. Pet. 48-49; EX2012, 127:19-134:1. The data buffer does ***not*** simply add a ***fixed*** delay of "***one***" clock cycle, as Netlist incorrectly asserts, POR 45-51, which in this example would result in a combined delay of 1.3 clock cycles. EX2012, 79:15-80:3 ("I want to make sure we're clear on this. We don't just delay one [clock] cycle").[7] Indeed, that

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[7] Netlist also incorrectly asserts that the "***same T*** applies ***across*** buffers" (in the horizontal direction) because the "same system clock CK [i.e., CK(OUT)] is used." POR 50-51 & n.5. That is incorrect, as Netlist's expert admitted above with Figure 15 (p.22), because the ***horizontal*** "flight time" (or "fly by") delay for the clock and command signals (shown in the red rectangle above, p.22) occurs ***before*** T0 in the ***vertical*** direction at a given memory chip and data buffer (i.e., the T0 at CK(IN) in blue and green above, p.22), EX2012, 124:8-127:18, 141:18-142:17. By way of analogy, each data buffer is in a different time zone (e.g., Pacific, Central, Eastern) given the horizontal delay of the clock and command signals, and thus T0 (e.g.,

would be contrary to the JEDEC standard which requires ***integer*** latency values and expressly "does ***not*** support any half-clock latencies." EX1020, 24, 30; EX1074, 108:6-118:7, 131:13-132:4 (discussing EX1020, 23, 24, 27, 29-30, 56, 59, 71).

Below is an example of S4 read leveling in Figure 15 measuring a vertical "flight time" delay of approximately 0.3 clock cycles (e.g., on shorter data line L2). In this example, the memory chip (green) receives a read command at T0; the memory chip outputs data at T5 in accordance with a previously set CAS latency of CL=5;[8] and then the data arrives at the data buffer (blue) at about T5.3 given the vertical "flight time" delay of about 0.3 clock cycles:

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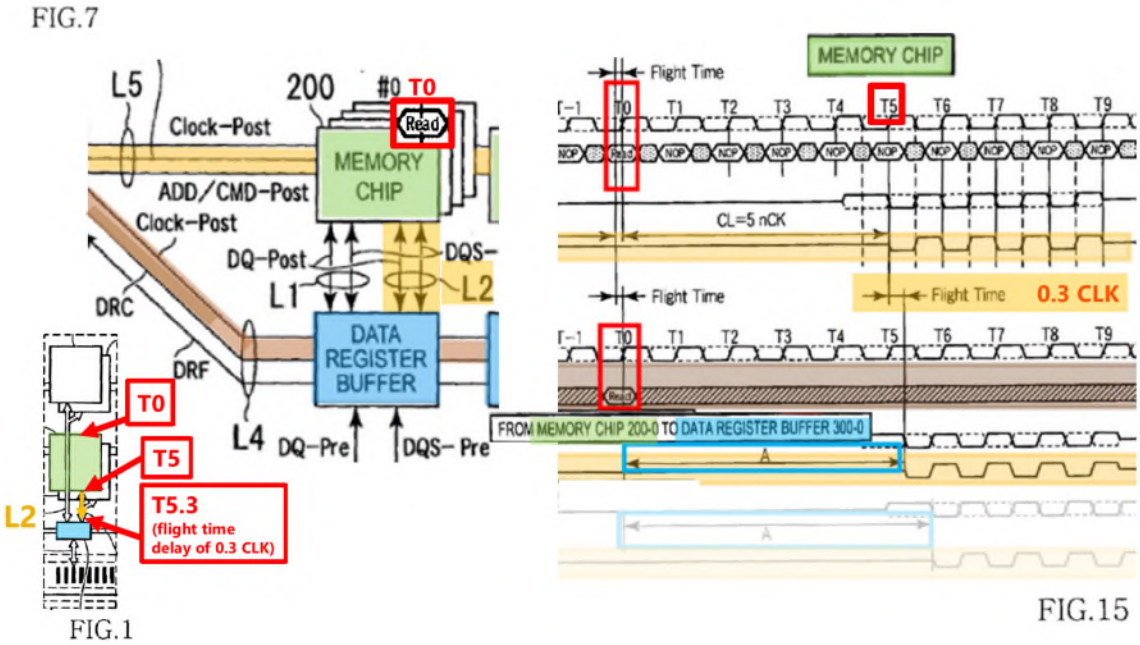
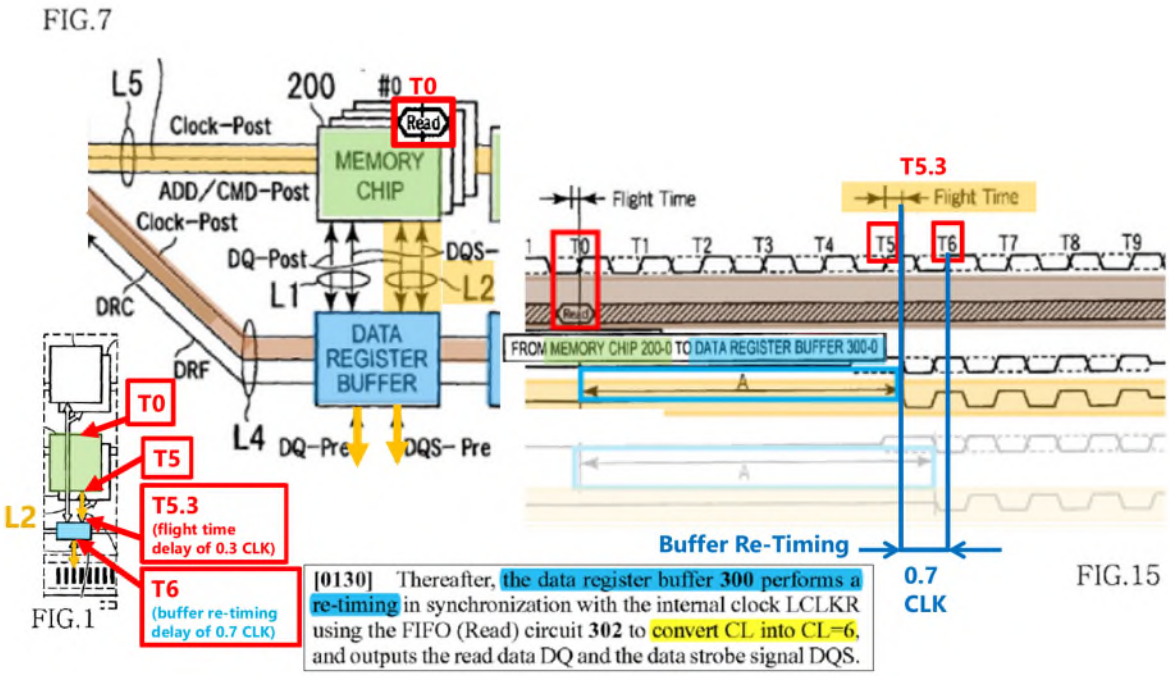
midnight) at one data buffer differs from T0 at another data buffer from the standpoint of the system clock CK(OUT) (e.g., Greenwich Mean Time). This is illustrated below (pp.38-43). EX1078; EX1079.

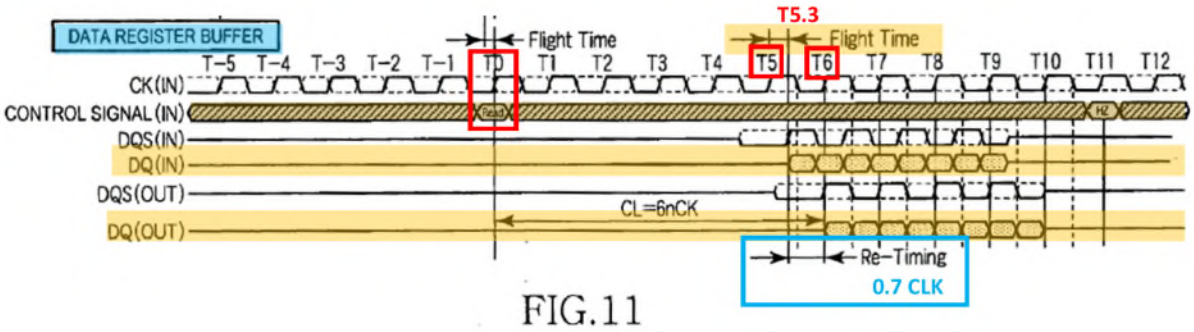
[8] CAS latency ("CL") is a standard JEDEC parameter, measured in ***integer*** clock cycles (e.g., 5, 6, or 7 clock cycles), that is "programmed at system initialization." EX1021, 342; EX1074, 102:18-104:14, 107:10-118:7, 131:13-132:4 (discussing EX1020, 23, 24, 27, 29-30, 56, 59, 71).




EX1082, 1. Then, during a normal read operation, as shown below, "the data register buffer 300 performs a retiming" by delaying the data and strobe signals in the data path by approximately ***0.7 clock cycles*** (given the previously measured "flight time" delay of 0.3) so that the data buffer outputs those signals at T6 (i.e., T5.3+0.7), corresponding to a CAS latency of CL=6. EX1005, [0130] ("convert CL into CL=6"); EX2012, 131:19-134:1.

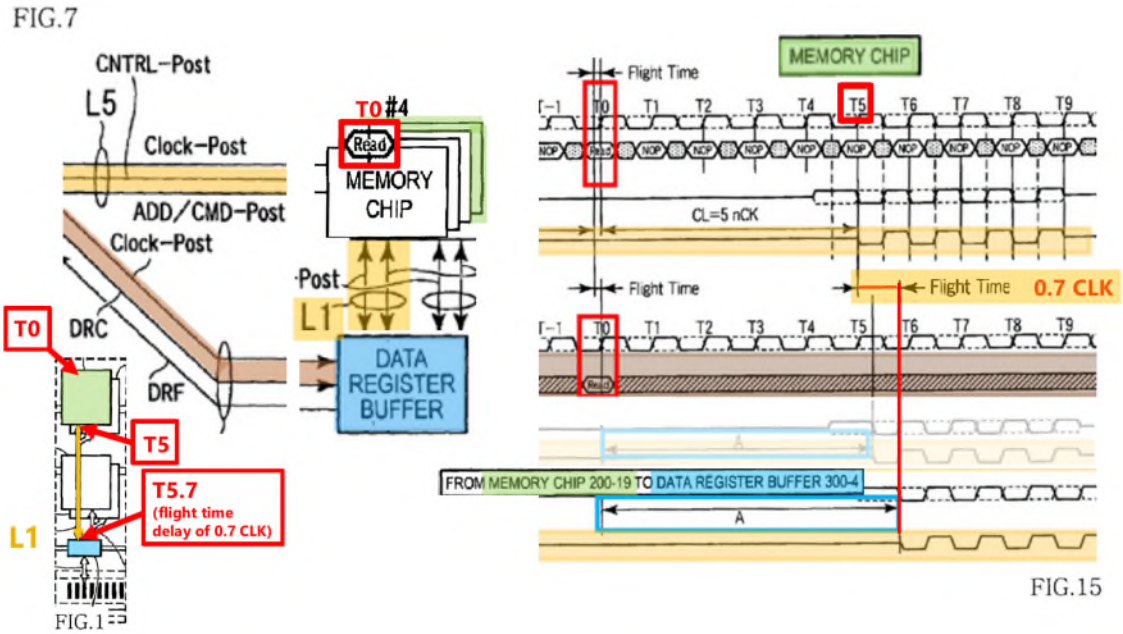



EX1082, 2. Hiraishi's Figure 11 (below in part) confirms that in this example, the data register buffer (blue) adds a delay of ***0.7 clock cycles***:

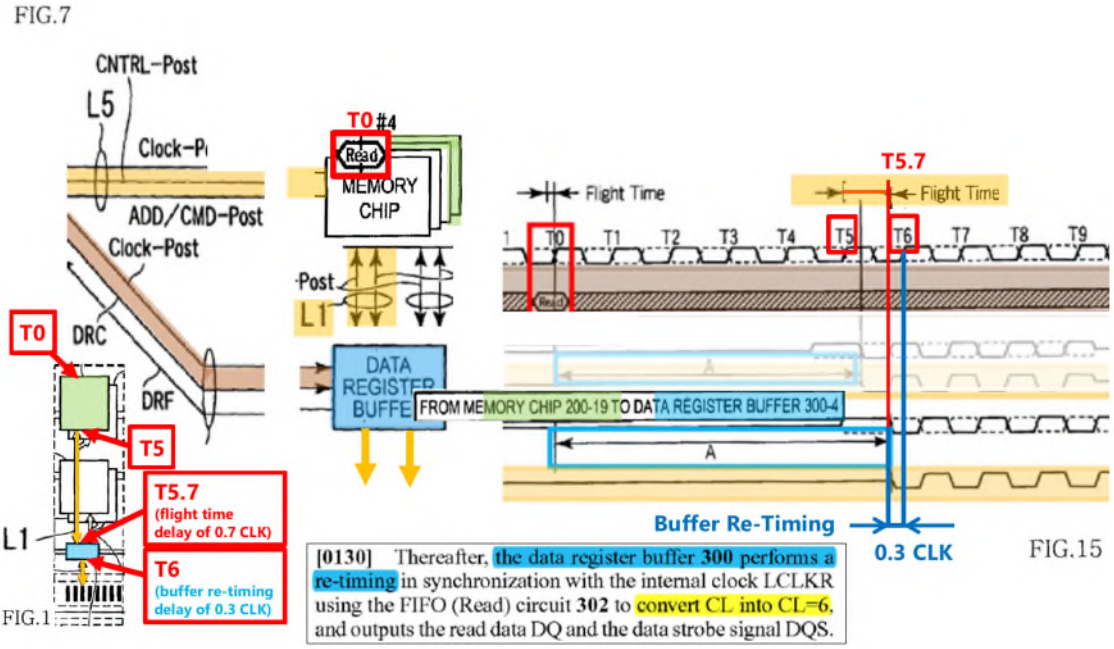



EX1005, Fig.11; EX1070.

Below is an example of S4 read leveling in Figure 15 measuring a vertical "flight time" delay of approximately 0.7 clock cycles (e.g., on longer data line L1):




EX1082, 3. As shown below, in this example the data buffer only delays the data and strobe signals in the data path by ***0.3 clock cycles*** (given the previously measured "flight time" delay of 0.7). EX1005, [0130] ("convert CL into CL=6"); EX2012, 131:19-134:1.

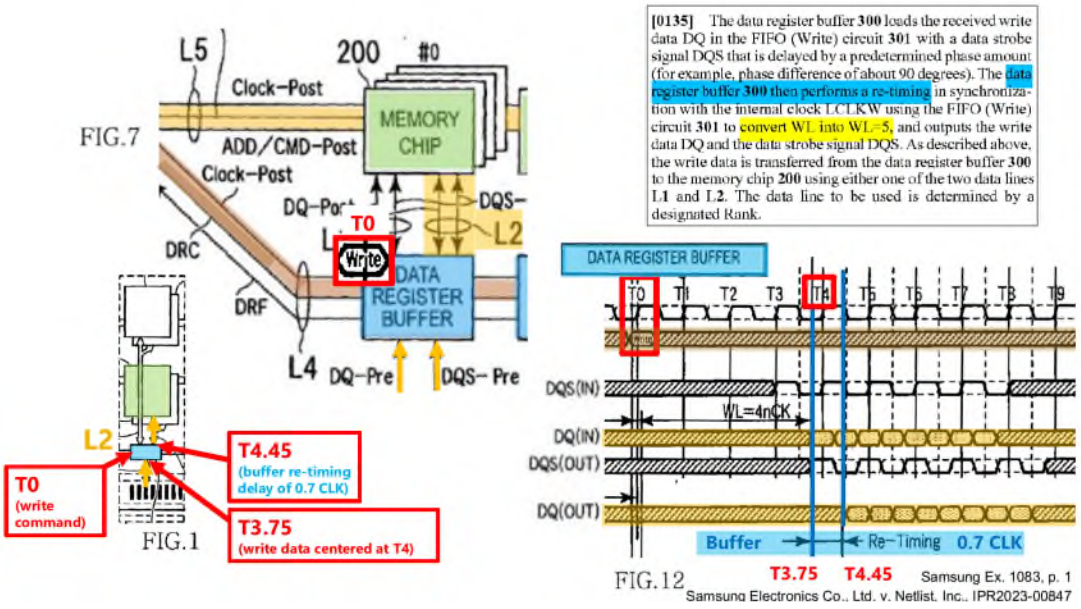


EX1082, 4.

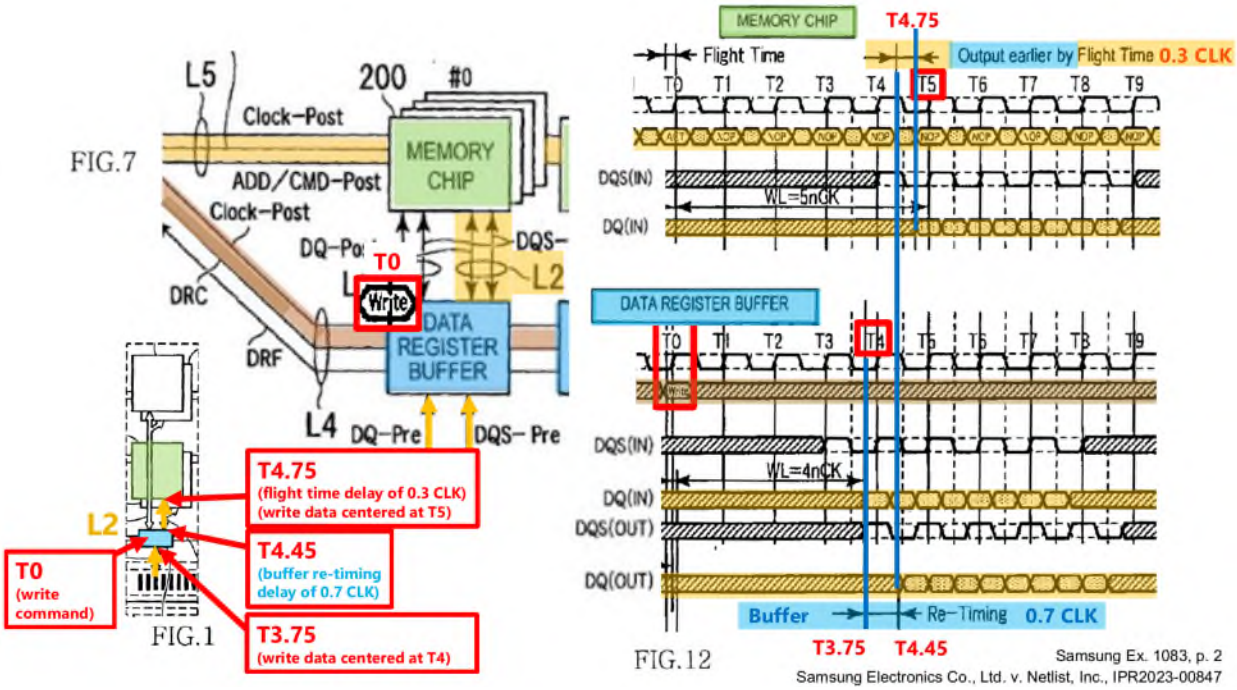
Below is an example where S4 write leveling measured a "flight time" delay of 0.3 clock cycles on the shorter data line L2. Then, as shown in Figure 12, during a normal write operation, the data buffer (blue) and memory chip (green) receive a write command at T0; in accordance with a previously set write latency of WL=4,[9] the data buffer starts receiving the first piece of write data at T3.75 so that it is center-aligned[10] at T4; then "[t]he data register buffer 300…performs a re-timing" by delaying the data and strobe signals in the data path by ***0.7 clock cycles*** (until T4.45) as shown below:

[9] Write latency (WL) is an ***integer*** value similar to CAS latency (CL) discussed above (p.25, n.8).

[10] Write data is center-aligned with the DQS strobe signal, while read data is edge-aligned. EX1074, 117:12-118:7 (discussing EX1020, 71), 116:25-117:8 (discussing EX1020, 56).




EX1083, 1. Next, the write data output by the data buffer has a flight-time delay of about 0.3 clock cycles, meaning it arrives at the memory chip at T4.75 and is center-aligned at T5, corresponding to a write latency of WL=5 as shown below. EX1005, [0135] ("convert WL into WL=5").



EX1083, 2.

Netlist cites the Board's denial of ***institution*** in IPR2017-00730, EX1014, 10-14, to argue that Hiraishi's read/write leveling does not ***delay*** signals through the data path, POR, 3, 51-52, 58. But IPR2017-00730 involved a different petitioner, patent, and claim language that required the buffer "***to time transmission of***…***read data signals***…in accordance with the time interval." EX1014, 10. Accordingly, the Board focused on whether the data buffer adjusted the time when read data was ***transmitted (i.e., output)***, and the Board concluded that read data was ***output*** at a given time (e.g., T6 corresponding to "re-timing to CL=6") which does not change as a result of read or write leveling. EX1014, 12-13 ("[Hiraishi] does not teach time A being used to adjust timing of data ***output*** by the buffer circuit…as recited in the claim."). The '608 Patent claims, in contrast, require the data buffer "***to delay a signal through*** the data path ***by an amount*** determined by the command processing circuit." The Board never disputed that the ***amount of delay*** applied by Hiraishi's data buffer ***is*** determined by read or write leveling. EX1014, 10-14. In fact, the Board expressly found that Hiraishi's write leveling "determines an amount of time by which to shift the output." EX1014, 10. Thus, the Board's decision does not conflict with any of Petitioner's arguments above, nor does it conflict with the Board's later ***Final*** Written Decision in IPR2022-00236, which is binding against Netlist and expressly agreed that

Hiraishi's read/write leveling ***does*** delay signals through the data path (pp.1-4).

### B. Ground 2 (POR 58-83)

With respect to Ground 2 (POR 58-83), Netlist repeats its erroneous arguments about Ground 1, discussed above, and relies on arguments about Tokuhiro that the Board already rejected in IPR2022-00236, *see* EX1066, 26-43, which Netlist is precluded from relitigating here as discussed above (p.4).

#### 1. Ground 2 has a "*delay circuit*" in the "*data path*" (POR 58-60)

Netlist argues that the functionality of Tokuhiro's delay element DR-1 (purple below), in the combination with Hiraishi, "is ***not*** in the DQ data path":

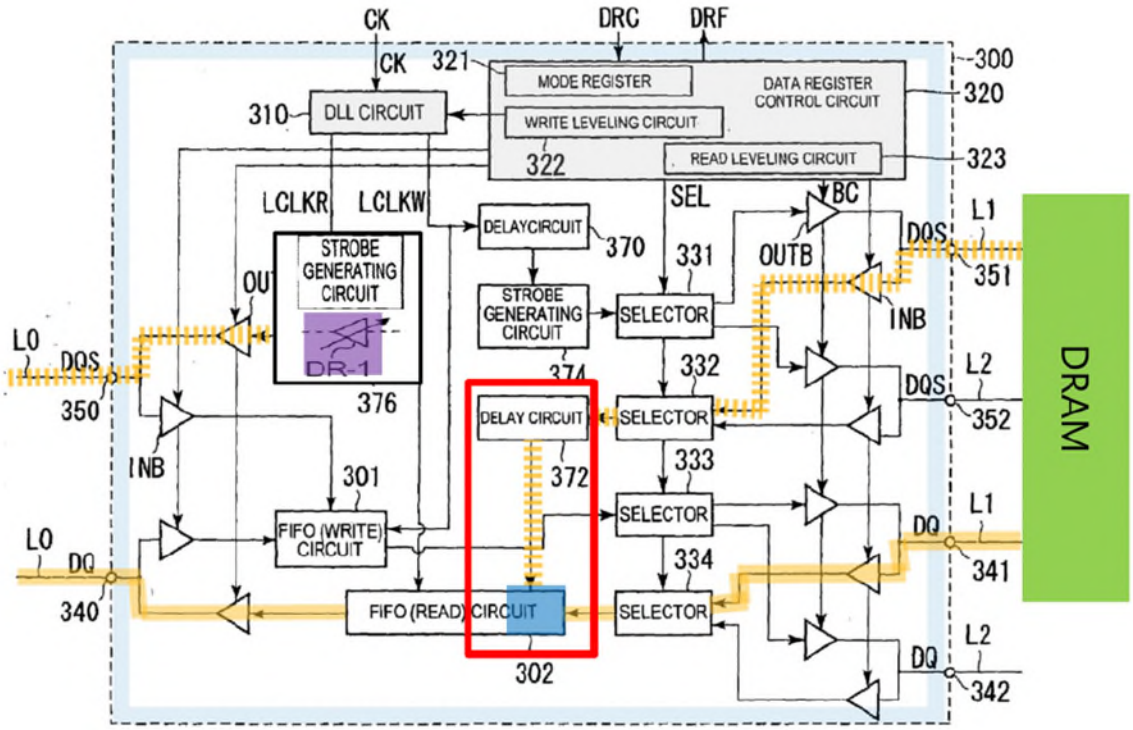



FIG.5

POR 59 (citing Pet. 89). But that argument is based on Netlist's erroneous claim

constructions where the "*data path*" excludes ***strobe*** signals, and the ***entire*** "*delay circuit*" must be physically on top of the DQ data line (solid orange above), which is incorrect as discussed above (pp.1-16). In any event, Ground 2 satisfies even Netlist's unreasonably narrow claim constructions because the Read FIFO 302 above is physically on the DQ data line and delays the DQ data signals, as discussed above (pp.12-16). And Netlist completely ignores the alternative combination for Ground 2 where "delay elements similar to Tokuhiro's DR elements can be used ***instead of***…Hiraishi's FIFO circuit for delaying the read ***data***," Pet. 90; EX1066, 39-40 (rejecting Netlist's "bodily incorporat[ion]" arguments against this combination); EX1074, 164:14-:18.

#### 2. Netlist's arguments about expectation of success are incorrect and precluded by IPR2022-00236 (POR 60-70)

Netlist also argues that the combination of Hiraishi and Tokuhiro would not work. POR 60-70. The Board has already rejected these arguments as improper "bodily incorporat[ion]" arguments, EX1066, 37-40, so Netlist is precluded from relitigating them as discussed above (p.4).

First, Netlist argues that removing fly-by delays cannot be done in a data buffer and must be done by the "memory controller" or "CPU" in the host computer. POR 60-64. To the contrary, Hiraishi expressly teaches using the "***data register buffers***" to remove delays as part of S4 read/write leveling, *see* Pet. 82-98, which the Board has already determined had a reasonable expectation of success

with Tokuhiro, EX1066, 37-40, and which can be ***in addition*** to any leveling performed by the "memory controller" as part of S5 leveling, EX1069; EX1005, Fig.13; EX1074, 248:9-251:15; EX2012, 56:17-58:3, 105:8-107:14, 108:24-109:13. The Board has also rejected Netlist's arguments that various "signal[s]" are not expressly shown in Hiraishi's Figure 5 and thus the combination would not work. POR 62-63; EX1068, 16-17. Netlist's own figures are missing similar signals. EX1074, 149:15-150:8, 157:9-:16; EX1080.

Next, Netlist argues that the illustration for Ground 2 shows a ***DQS strobe signal*** to sample the Read FIFO 302, instead of a ***clock*** signal like LCLKR. POR 65-70. This is another improper "bodily incorporat[ion]" argument. EX1066, 39-40. Either type of signal can be used, as Netlist's expert admitted: "***clocks*** are often used for sampling and, similarly, ***strobe*** signals are often used to control sampling." EX1074, 154:15-:22. Butt also confirms that a DQS strobe signal (PDQS_OUT/NDQS_OUT, dashed orange) can be used to control a FIFO (112, olive):

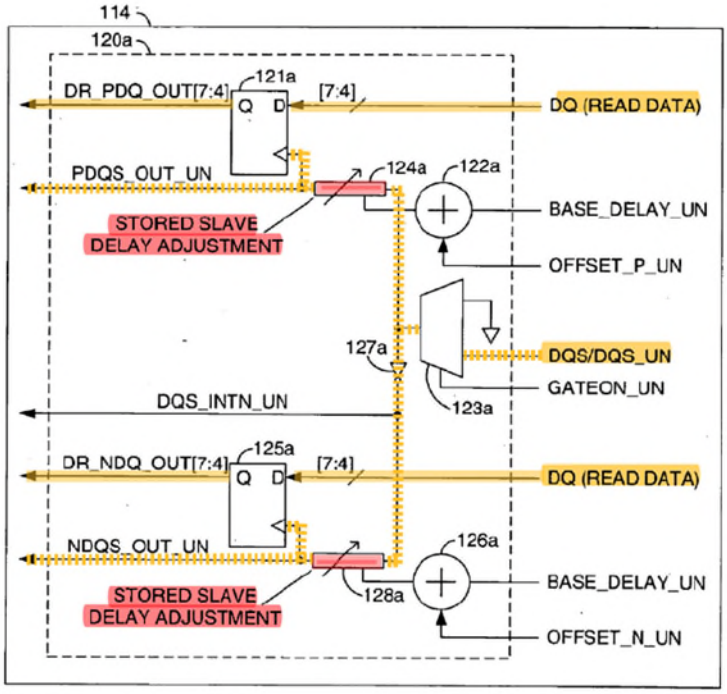

114
120a
121a
DR_PDQ_OUT[7:4]
Q D
[7:4]
DQ (READ DATA)
PDQS_OUT_UN
124a
122a
STORED SLAVE
DELAY ADJUSTMENT
BASE_DELAY_UN
OFFSET_P_UN
127a
DQS/DQS_UN
GATEON_UN
123a
DQS_INTN_UN
125a
DR_NDQ_OUT[7:4]
Q D
[7:4]
DQ (READ DATA)
NDQS_OUT_UN
126a
STORED SLAVE
DELAY ADJUSTMENT
128a
BASE_DELAY_UN
OFFSET_N_UN

FIG. 3A

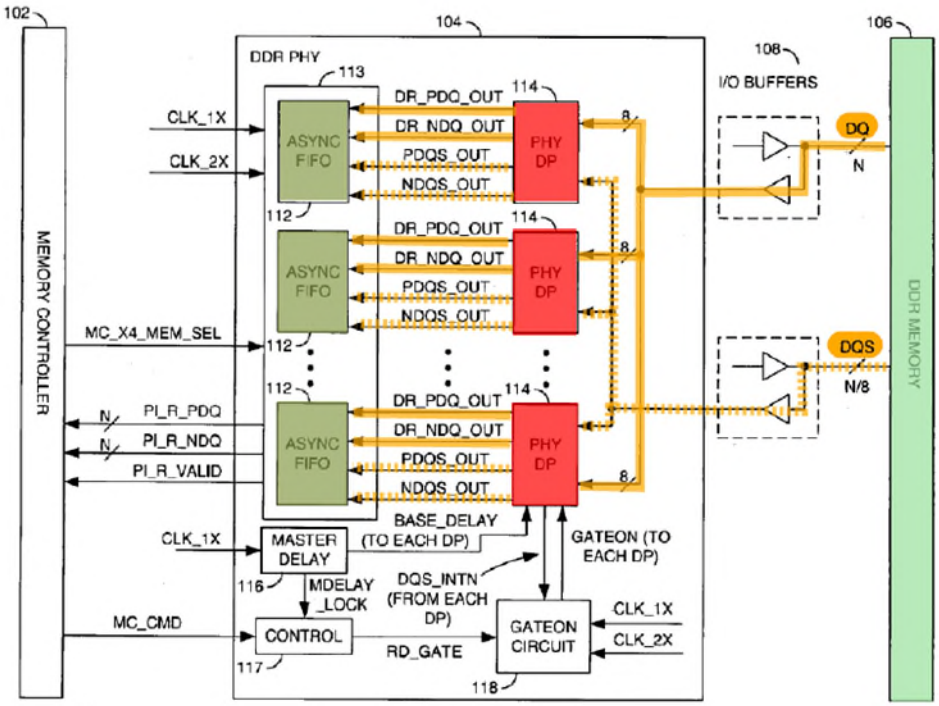
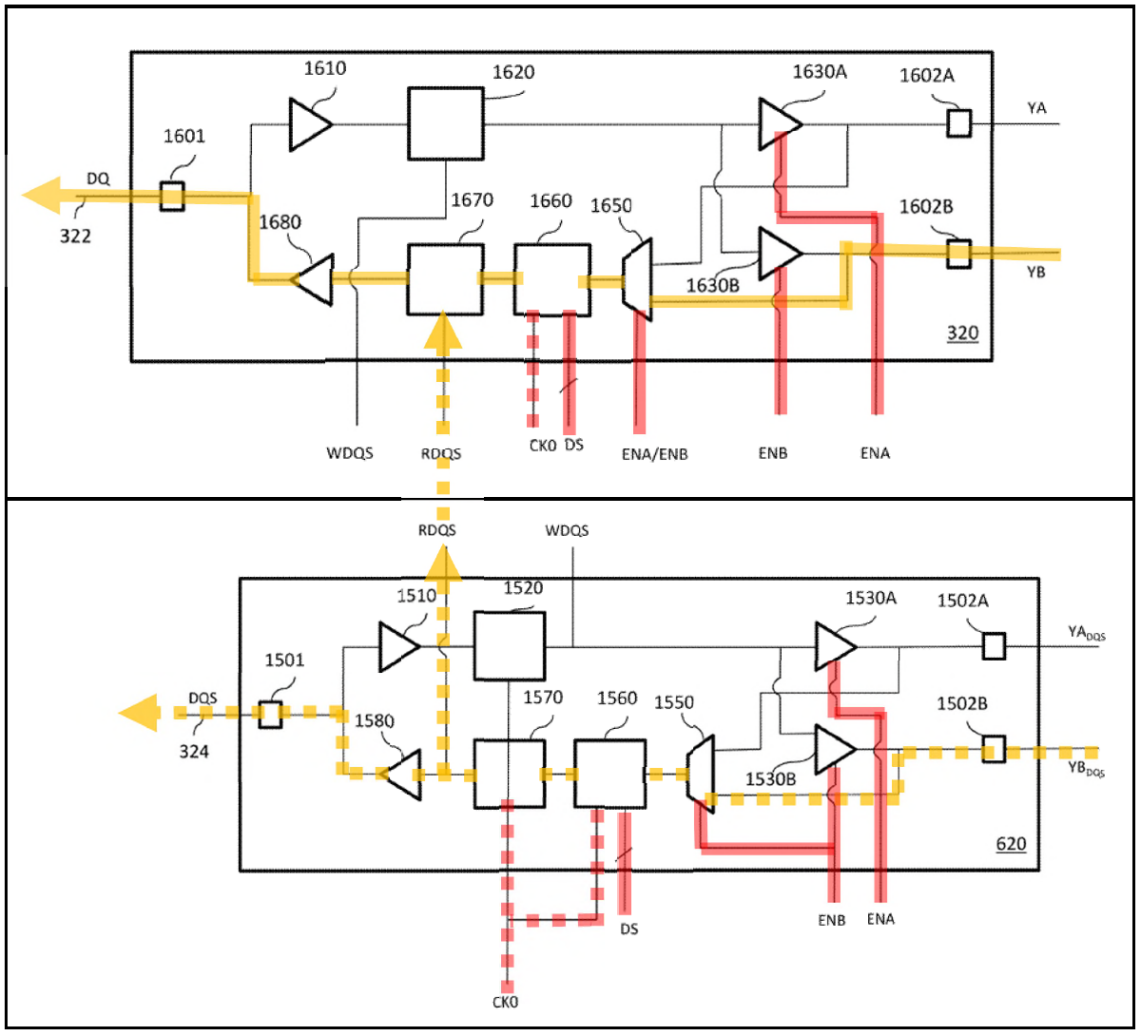

102
MEMORY CONTROLLER
104
DDR PHY
113
CLK_1X
CLK_2X
ASYNC FIFO
112
DR_PDQ_OUT
DR_NDQ_OUT
PDQS_OUT
NDQS_OUT
114
PHY DP
8
MC_X4_MEM_SEL
PI_R_PDQ
PI_R_NDQ
PI_R_VALID
N
CLK_1X
MASTER DELAY
116
BASE_DELAY (TO EACH DP)
GATEON (TO EACH DP)
MDELAY _LOCK
DQS_INTN (FROM EACH DP)
MC_CMD
CONTROL
117
RD_GATE
GATEON CIRCUIT
118
CLK_1X
CLK_2X
108
I/O BUFFERS
DQ
N
DQS
N/8
106
DDR MEMORY

FIG. 2

Pet. 35-36; EX1029, [0019], Figs.3A, 2; EX2012, 138:16-139:1; EX1074, 181:19-183:1. Netlist argues that the "Pre-amble" and "Post-amble" of the DQS strobe would prevent "clock[ing] out data from a FIFO," POR 69, but Butt teaches using a GATEON signal to "gate" or "block" the preamble and postamble of the DQS strobe signal, so that it can be used to "clock[]" the FIFO. EX1029, [0019], [0047]; EX1074, 181:19-183:1, 184:1-190:7, 191:20-193:15, 199:2-200:2, 201:14-202:5; EX1084, Figs.2-3, 14.

Netlist is improperly trying to distinguish the prior art based on technical details that are neither "claim[ed]" nor "disclos[ed]" in the '608 Patent. *Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-001427, Paper 48, 35-36 (PTAB Apr. 1, 2024). Indeed, the '608 Patent shows both a ***clock*** (dashed red) and a ***strobe*** (dashed orange) being used to sample different signals, without any explanation of the technical details of the difference, as Netlist's expert admitted:

**Read direction — '608 Patent (EX1001) Figures 16 & 15**




EX1080, 1; EX1074, 149:4-:10, 150:9-:19, 154:6-155:19; *see also* EX1080, 2; EX1074, 157:17-:22, 158:24-159:1 ("the disclosure…is pretty thin"), 161:14-:23.

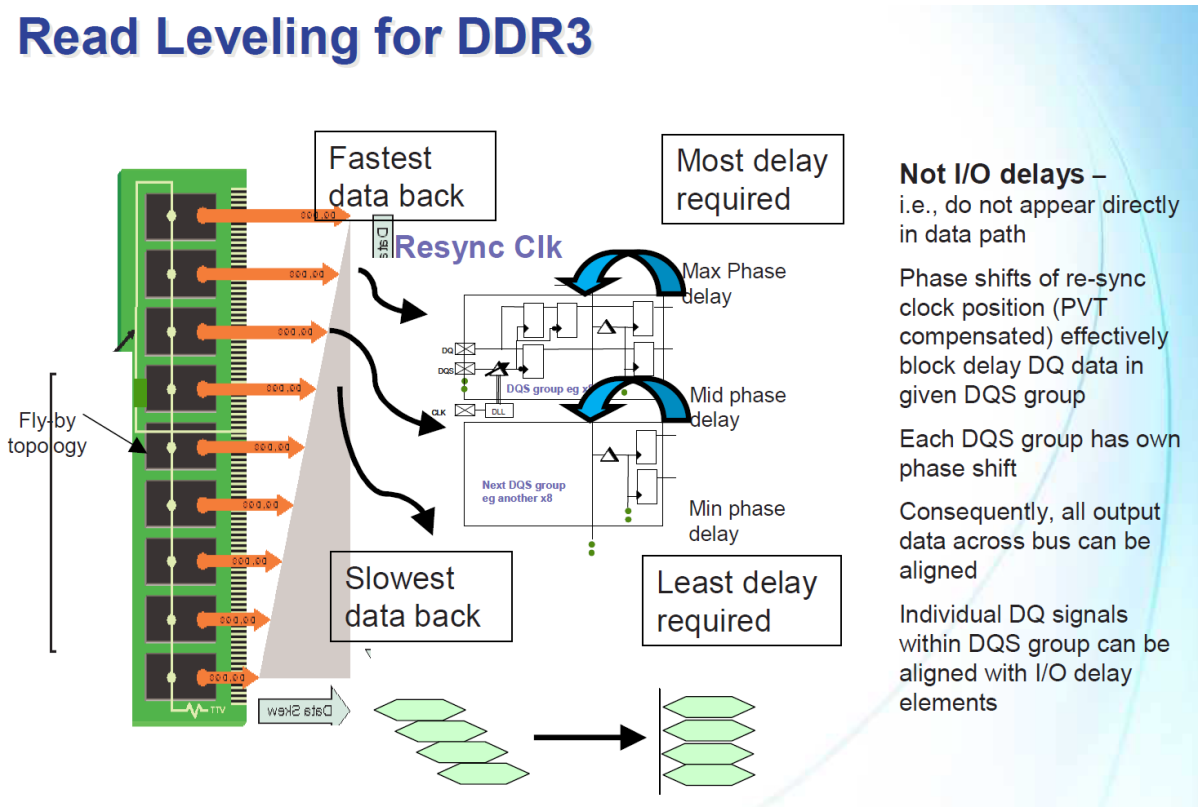
### 3. Netlist's arguments about motivation to combine are incorrect and precluded by IPR2022-00236 (POR 71-83)

Netlist completely ignored the motivations for the specific combination in Ground 2. *See* POR 71-83 (ignoring Pet. 82-91). Instead Netlist argues that there would be no motivation to combine Hiraishi and Tokuhiro in general, POR 71-83,

but the Board has already rejected that argument, EX1066, 40-43, so Netlist is precluded from relitigating that issue here as discussed above (p.4). Netlist's arguments are also wrong:

**a) <u>Hiraishi</u> and <u>Tokuhiro</u> are analogous art to the '608 Patent, each directed to the problems of "fly-by" (or "flight time") delays on a memory module**

The Petition provided multiple motivations to combine. Pet. 72-82. Netlist's expert made important admissions supporting those motivations. He conceded that JEDEC's DDR3 standard adopted a "***fly-by topology*** for the commands, addresses, control signals, and clocks," EX1020, 42, resulting in a skew of the data that needed to be corrected with read/write leveling, as illustrated below:

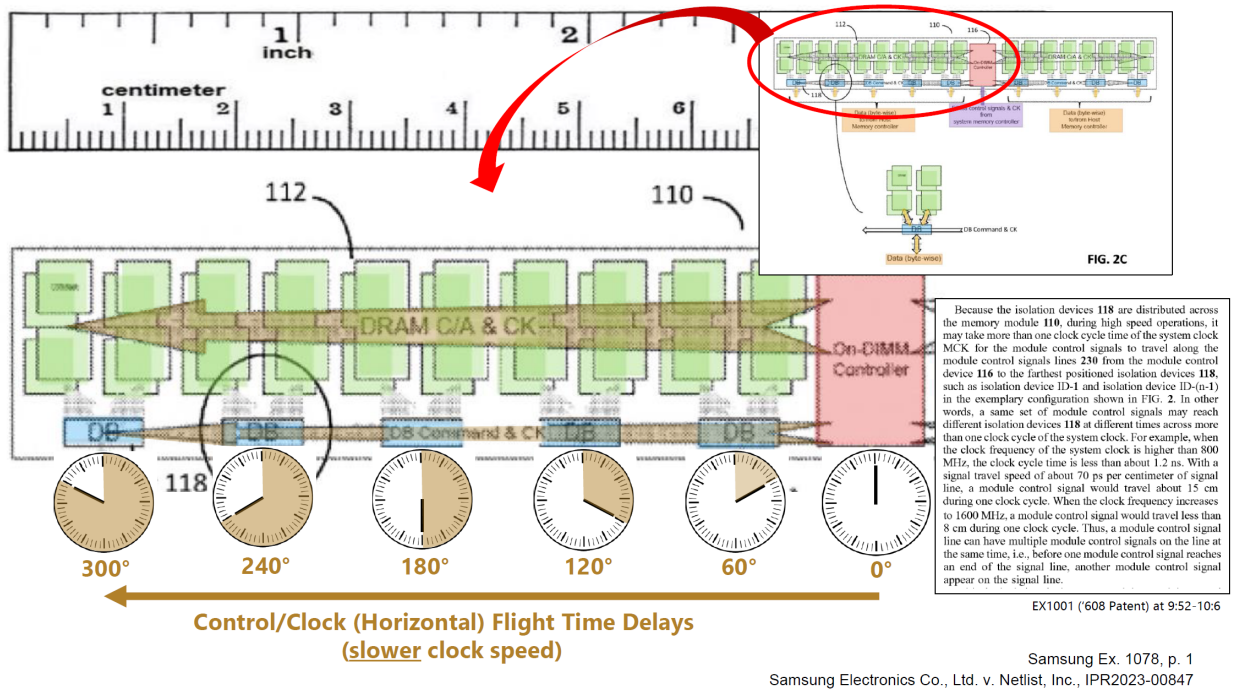



EX1085, 7;[11] EX1074, 79:23-80:14, 89:6-90:9 (discussing need in DDR3 for read and write leveling, EX1085, 7, 9).

He conceded that both the ’608 Patent and Hiraishi also have the DDR3-

[11] The module illustrated above is a UDIMM, so the fly-by is across the entire module, whereas with the ’608 Patent and Hiraishi, the fly-by is from the center to the sides because they have a register in the center for the address/command/clock signals like an RDIMM. EX1077, 7-8; EX1074, 55:21-58:24.

style fly-by topology, resulting in "fly-by" or "flight time" delays[12] in the horizontal direction for address/control/clock signals, as shown below, similar to Tokuhiro as explained in the Petition, Pet. 79-91.




EX1078, 1 ('608 Patent, Fig.2C); EX1001, 8:22-:35; EX1074, 66:3-67:18.

[12] The experts often used the words "fly-by delay" and "flight time delay" interchangeably. EX1074, 64:25-66:2.

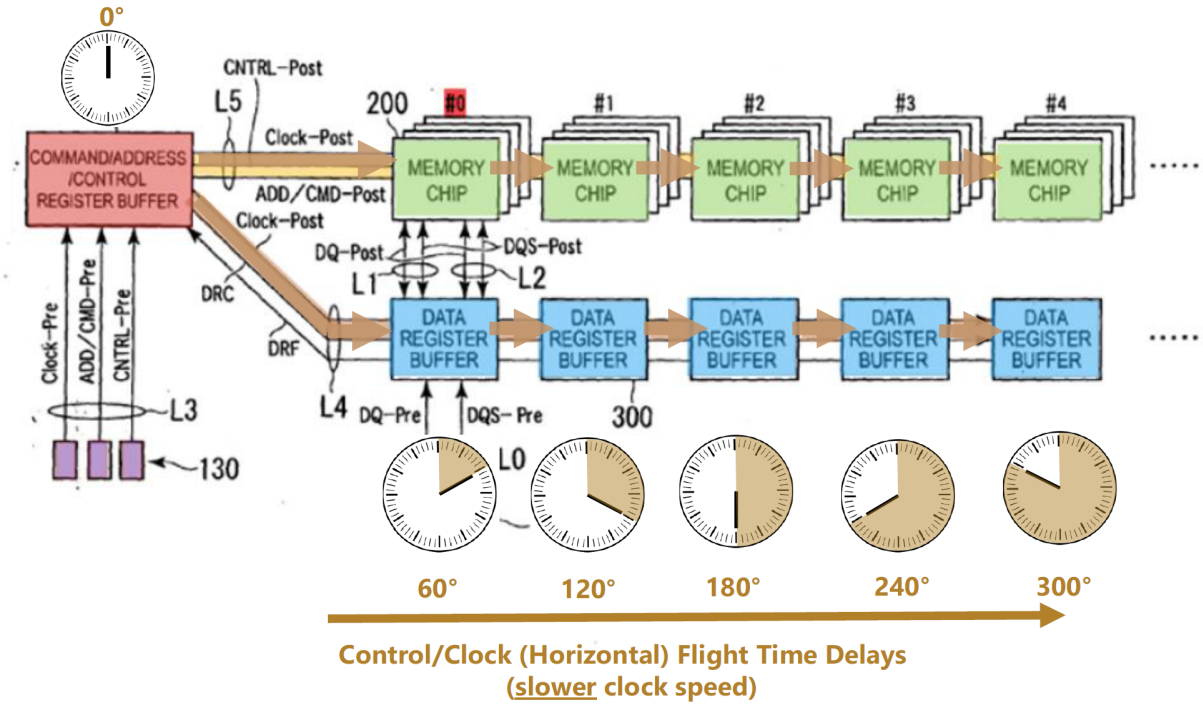
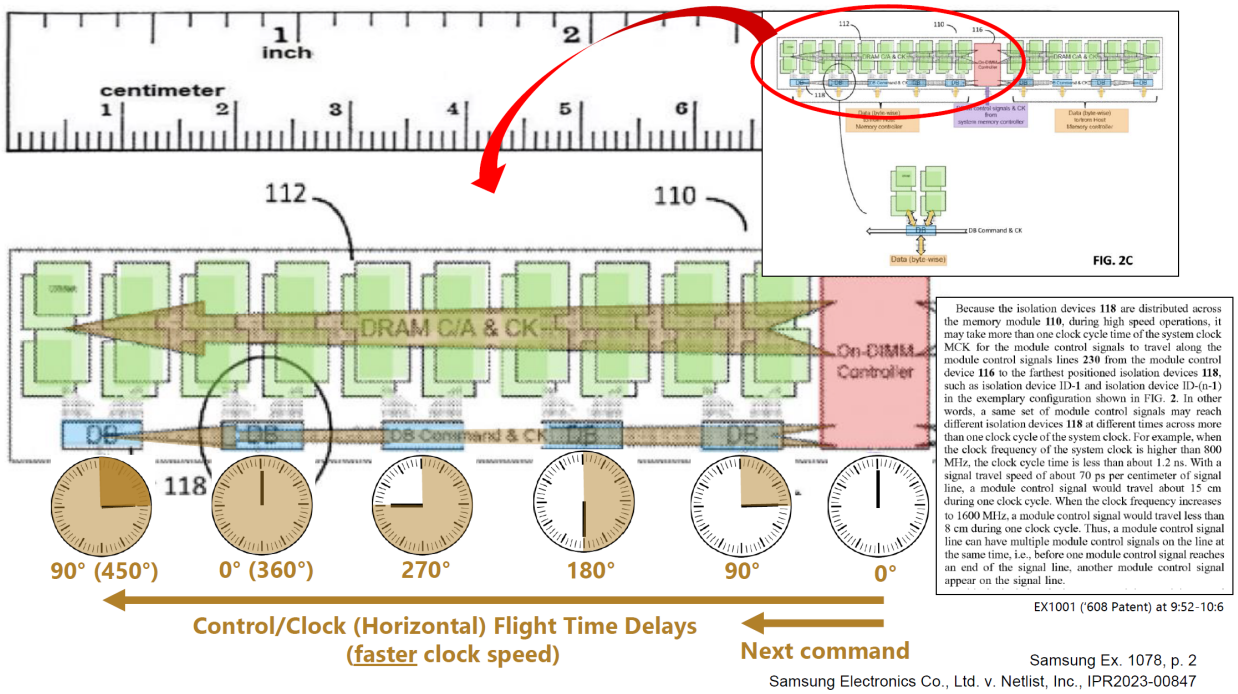



FIG.7

Samsung Ex. 1079, p. 1
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

EX1079, 1 (Hiraishi, Fig.7); EX1074, 68:17-69:15.

And he conceded that as the DDR3 clock speeds got faster (e.g., less than 1ns, which is one billionth of a second, *see* EX1074, 52:24-54:15 (discussing EX1077, 5, and EX2015, 141)), the horizontal delays could be ***greater*** than one clock cycle, meaning that "before one module control signal reaches an end of the signal line, another module control signal appear on the signal line," EX1001, 9:52-10:6, as illustrated below:




EX1078, 2; EX1074, 60:23-64:24, 67:19-68:16.

He also conceded that horizontal delays greater than one clock cycle were not invented by Netlist, but rather are just a matter of physics, as was known in the art, EX1074, 242:19-244:18; EX1024, 4:61-:64, 5:26-:31, and thus such delays would also be a problem for Hiraishi, as shown below:

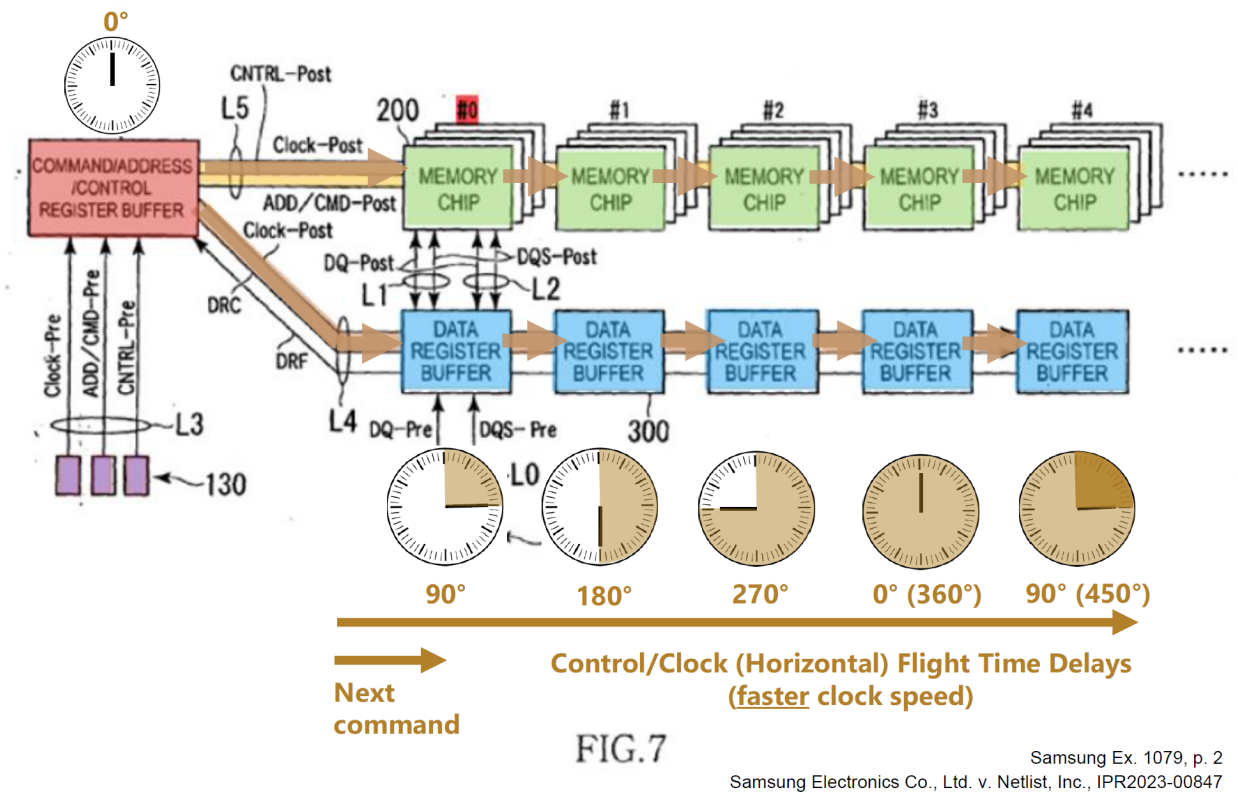



FIG.7

Samsung Ex. 1079, p. 2
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

EX1079, 2; EX1074, 69:17-70:14.

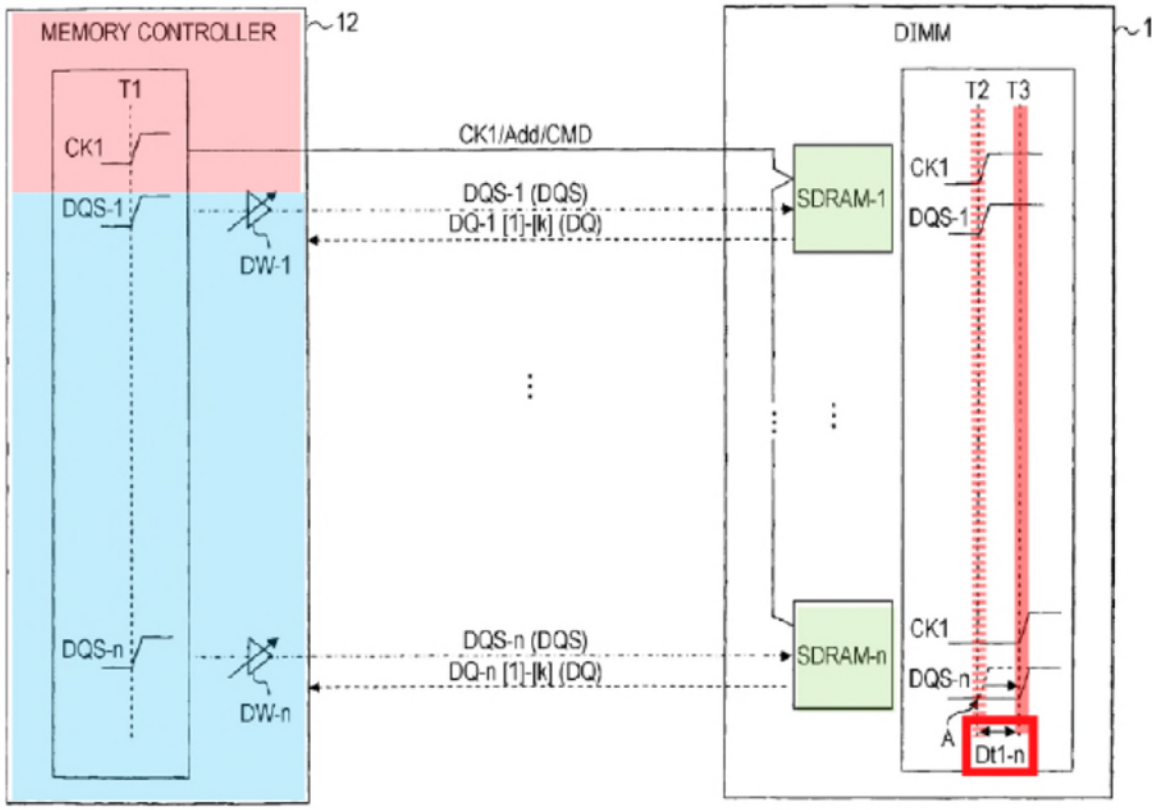
As shown above on the right, after 360°, a clock repeats itself, meaning 450° looks like 90°. EX1074, 70:15-71:21. Netlist's expert conceded that Hiraishi does not disclose a solution to delays greater than one clock cycle. EX1074, 69:17-70:14, 231:13-233:4; EX2012, 70:23-71:7, 79:15-80:16. But Tokuhiro discloses a solution, thus providing a motivation to combine to solve this problem. Pet. 80-82; EX1074, 178:8-179:12 (discussing EX1006, 14:55-:58 & Fig.7).

**b) Netlist's arguments are incorrect**

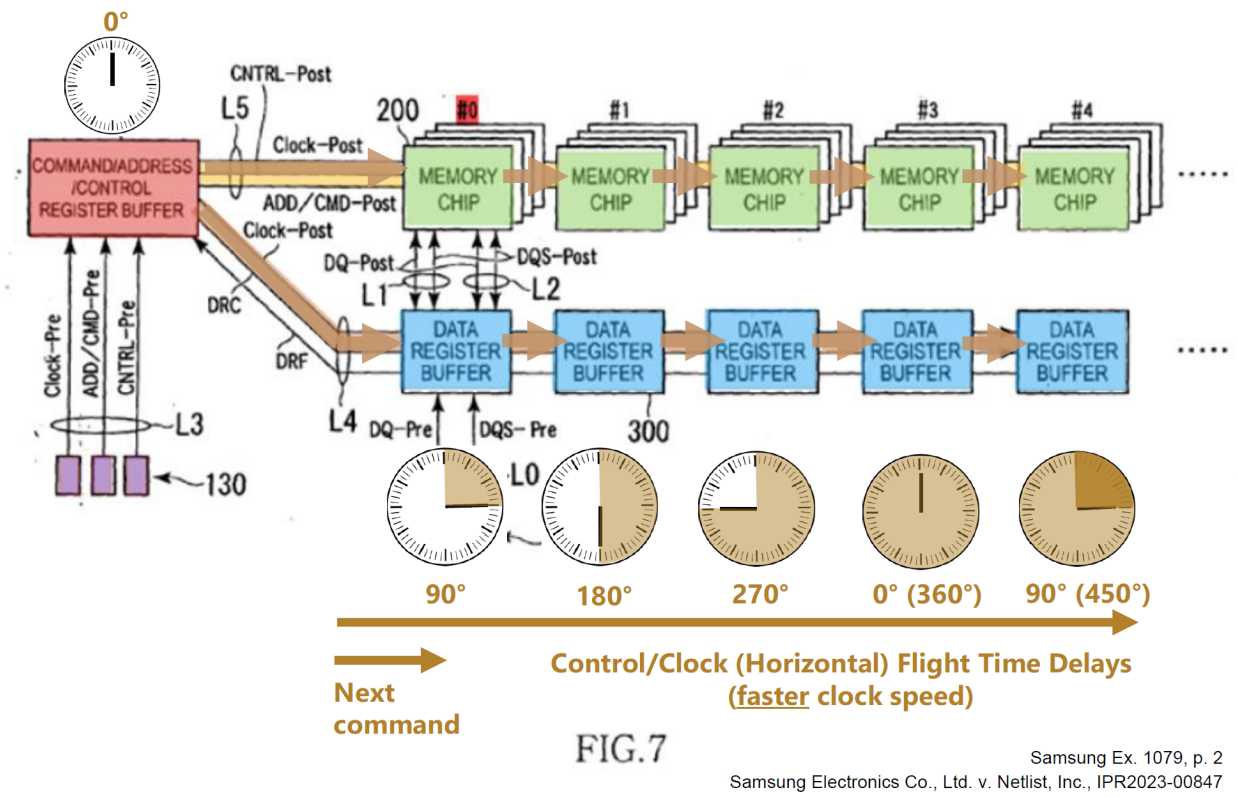
Netlist argues that "Tokuhiro does not disclose accounting for delays greater than one clock cycle." POR 73-74. To the contrary, Tokuhiro addresses delays

"on the order of 1ns," EX1006, 3:9-:12, which as discussed above can result in a delay of greater than one clock cycle (pp.41-43), and Tokuhiro discloses a technique for handling them: "***delay times Dt1-1 to Dt1-n*** corresponding respectively to the SDRAM-1 to the SDRAM-n are ***set so as to become longer gradually*** in the order from…SDRAM-1 toward…SDRAM-n." EX1006, 14:55-:58 & Fig.7 (below); EX1074, 178:8-179:12.

FIG. 7




Setting the delays "gradually" ***longer*** takes into account delays greater than one clock cycle, because if the delays are 90°, 180°, and 270°, then the next delay must be 360° not 0°, and the delay after that must be 450° not 90°:




EX1079, 2.

Second, Netlist argues that a data buffer is "space-constrained," POR 74-76, but Hiraishi's data buffer ***already*** has read/write leveling circuitry, so adding Tokuhiro's functionality would be straightforward and require limited change. Furthermore, there are no claim limitations nor disclosure concerning space limitations, EX2012, 139:12-140:8, and JEDEC taught that data buffers could include a lot of functionality, EX1077, 9; EX1059, 15; EX1074, 22:13-24:2, 45:19-47:1, 48:15-49:6, 59:2-60:21; EX1075, 75:6-:18, 246:13-259:11.

Third, Netlist argues Tokuhiro requires dedicated control lines, POR 77, but Hiraishi already has the control lines DRC (brown) and DRF on the module, Pet.

20-25, 32-33, 37-39, 44-45, 49, 97-98, 106-08.

Fourth, Netlist argues (similar to above, p.34) that there are advantages to using the memory controller instead of the data buffer, POR 77-80, but the combination need not be the "best option," just a "suitable option," *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023), and it is one of two "finite" solutions, Pet. 82-83, that takes advantage of Hiraishi's existing FIFOs in the data buffer.

Next, Netlist argues it would "increase…circuitry" to use ***nine*** data buffers instead of ***one*** memory controller, POR 80-82, but Hiraishi already provides all that circuitry and control signals (e.g., DRC), Pet. 20-25, 94-98 ("no changes to…the memory controller").

Next, Netlist incorrectly asserts Hiraishi does not need read leveling because "read data is all ***output***…at T6." POR 82. That is wrong because "T6" is different at each memory device given the "fly-by" topology discussed above (pp.24 n.7, 38-39), resulting in skew, Pet. 80-81 (e.g., "T9" to "T10").

Finally, Netlist repeats the argument that Tokuhiro cannot handle delays greater than one clock cycle, POR 82-83, which is wrong as addressed above (pp.43-45).

## III. CONCLUSION

For the reasons set forth above and in the Petition, Samsung respectfully

requests that remaining claims 1-5 be found unpatentable.

Dated: June 21, 2024

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*Samsung Electronics Co., Ltd.*

## CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Reply to Patent Owner's Response** complies with the type-volume limitations of 37 C.F.R. § 42.24(c)(1) because it contains 5,596 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the reply exempted by 37 C.F.R. § 42.24(c).

Dated: June 21, 2024

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## CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 21st day of June, 2024, **Petitioner's Reply to Patent Owner's Response** and **Exhibits 1059 and 1069–88** were served by email on the following counsel for Patent Owner:

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