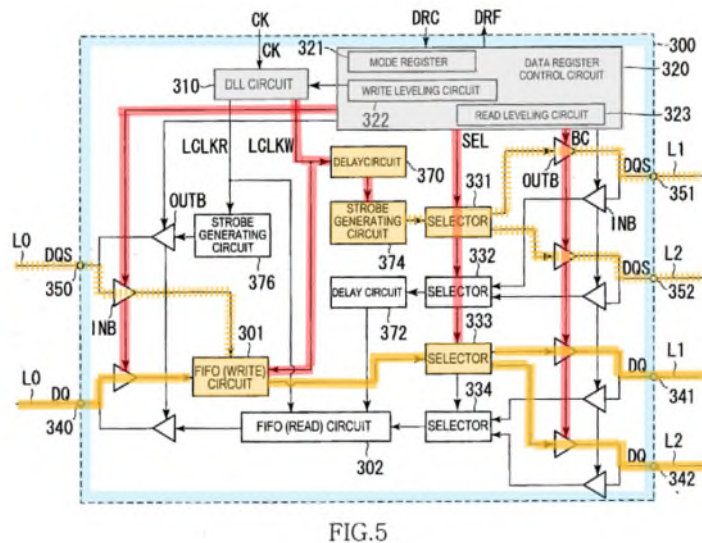
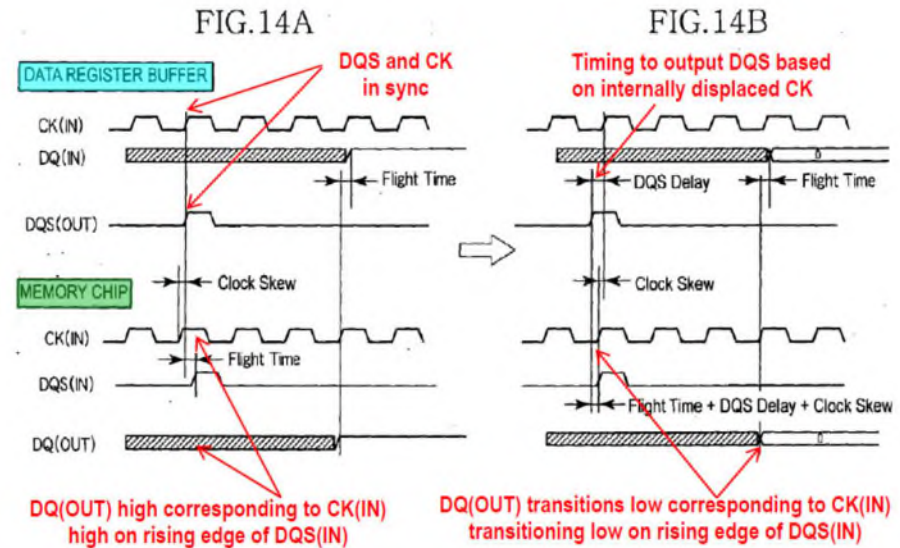


Hiraishi (EX1005)



S4 write leveling →

Memory Chip



[0142] FIGS. 14A and 14B are timing charts for explaining the write leveling operation between the data register buffer 300 and the memory chip 200, where FIG. 14A is a timing chart at the time of starting the leveling and FIG. 14B is a timing chart at the time of ending the leveling. This operation is performed by the write leveling circuit 322 shown in FIG. 5.

[0143] In the write leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 14A, the data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK. The clock signal CK is a signal that is supplied from the command/address/control register buffer 400, which is also supplied to the memory chip 200 as described above. Because it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.

[0144] In the example in FIG. 14A, there is shown a case that a logical level of the clock signal CK at a rising edge of the data strobe signal DQS is "High level". In response to the logical level of the clock signal CK, the memory chip 200 outputs a signal DQ of "High level" from the data input/output terminal 204. The signal DQ is input to the data register buffer 300, by which the data register buffer 300 can find a direction of phase shift of the clock signal CK and the data strobe signal DQS.

[0145] The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift. In the example shown in FIG. 14A, because the data strobe signal DQS is retarded as compared to a rising edge of the clock signal CK reaching the memory chip 200, the data register buffer 300 advances the output timing of the data strobe signal DQS.

[0146] By repeating the above operation, as shown in FIG. 14B, the logical level of the clock signal CK is changed to "Low level" at the rising edge of the data strobe signal DQS on the memory chip 200 side. This leads to an end of the write leveling operation, and the data register buffer 300 can find a timing to output the data strobe signal DQS based on the input clock signal CK. A result of the write leveling operation is stored in the data register control circuit 320 in the data register buffer 300. Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.