

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2023-00847

Patent 10,268,608 B2

**ERRATA TO THE DEPOSITION OF
ROBERT WEDIG (MARCH 12, 2024)**

I, ROBERT WEDIG, have read the transcript of my deposition taken on March 12, 2024. Listed below are changes to the transcript that I wish to make and the reasons for making them:

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
19:4	delayed <u>CLK</u>	delayed <u>clock</u>	Typographical error
20:7–:8	the <u>CLK</u>	the <u>clock</u>	Typographical error
20:21	a <u>CLK</u> signal	a <u>clock</u> signal	Typographical error
22:2	local <u>CLK</u> signal	local <u>clock</u> signal	Typographical error
40:11–:16	Q. BY MR. LINDSAY: What is the data path through Hiraishi's buffer shown in Figure 5? MR. CHANDLER: Objection. Form. THE WITNESS: So it's -- it's at least all of the orange lines, both solid and hashed, shown in the two depictions of Figure 5 on page 98 of my declaration.	[see note]	No change, but this was further clarified at 44:22–48:11, 49:24–50:13, 113:24–120:1, 134:8–137:22, 144:22–152:2.
42:1	the <u>CLK</u> signals	the <u>clock</u> signals	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
42:21–43:1	Q. Is the data register control circuit 320 part of the data path through Hiraishi's data buffer? A. No, it's not. Q. Is the DLL circuit 310 part of the data path through Hiraishi's data buffer? A. No, it's not.	[see note]	No change, but this was further clarified at 44:22–48:11, 49:24–50:13, 134:8–137:22, 144:22–152:2.
52:1	a <u>CLK</u> signal	a <u>clock</u> signal	Typographical error
52:6–:7	not a <u>CLK</u> , as at least I define a <u>CLK</u>	not a <u>clock</u> , as at least I define a <u>clock</u>	Typographical error
55:15	a <u>CLK</u> edge	a <u>clock</u> edge	Typographical error
58:18	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
59:6	the <u>CLK</u>	the <u>clock</u>	Typographical error
59:21–:22	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
60:10 60:21 60:24 61:5 61:10	the <u>CLK</u>	the <u>clock</u>	Typographical error
61:17–:18	<u>right</u> leveling	<u>write</u> leveling	Typographical error
61:19	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
61:21–:22	fly-by <u>clause</u>	fly-by <u>delays</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
62:2 62:4 62:9 62:11 62:18 62:22 63:3	[t]he <u>CLK</u>	[t]he <u>clock</u>	Typographical error
63:5	that <u>CLK</u>	that <u>clock</u>	Typographical error
63:18	the <u>SKU</u>	the <u>skew</u>	Typographical error
64:1	<u>right</u> leveling	<u>write</u> leveling	Typographical error
65:23	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
68:16 68:19 68:23 68:23–:24 69:11 69:19 70:3 70:4	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
70:14–:20	Q....But the two examples that Hiraishi gives, both those examples increase the latency by exactly one <u>CLK</u> cycle. MR. CHANDLER: Objection. Form. THE WITNESS: You're correct that the examples they give extend it by one <u>CLK</u> cycle. But as I said, I don't think Hiraishi is limited to that.	Q....But the two examples that Hiraishi gives, both those examples increase the latency by exactly one <u>clock</u> cycle. MR. CHANDLER: Objection. Form. THE WITNESS: You're correct that the examples they give extend it by one <u>clock</u> cycle. But as I said, I don't think Hiraishi is limited to that.	Typographical errors, and this was further clarified at 71:8–74:8, 127:19–134:1.
70:24–:25 71:5 71:10 71:13 71:18 71:22–:23 72:13 72:21 72:22	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error
73:20	memory <u>buff</u>	memory <u>buffer</u>	Typographical error
73:25 73:25–74:1	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error

74:9--:24	Q. So the <u>CLK</u> signal, CK(IN), that's along the top there, that's -- is that a system <u>CLK</u> that's available to all the memory chips, the data buffer and a register, I guess, which isn't really shown, but it's a system-level <u>CLK</u>; is that correct? A. Yes, that's correct. That same <u>CLK</u> is given to the memory chip -- the <u>CLK</u> that's given to the memory chip is the same <u>CLK</u> provided to the data register buffer. It's a system-level <u>CLK</u>. Q. So -- so the data buffer and the memory chips will know when they are at T5 or T6? In other words, it would be a common -- in other words, it would be the common understanding of where in the operation all the devices are? MR. CHANDLER: Objection. Form.	Q. So the <u>clock</u> signal, CK(IN), that's along the top there, that's -- is that a system <u>clock</u> that's available to all the memory chips, the data buffer and a register, I guess, which isn't really shown, but it's a system-level <u>clock</u>; is that correct? A. Yes, that's correct. That same <u>clock</u> is given to the memory chip -- the <u>clock</u> that's given to the memory chip is the same <u>clock</u> provided to the data register buffer. It's a system-level <u>clock</u>. Q. So -- so the data buffer and the memory chips will know when they are at T5 or T6? In other words, it would be a common -- in other words, it would be the common understanding of where in the operation all the devices are? MR. CHANDLER: Objection. Form.	Typographical errors, and this was further clarified at 82:10--84:12, 126:1--127:18, 141:11--144:21.
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
	THE WITNESS: Yeah, that's correct.	THE WITNESS: Yeah, that's correct.	

74:25– 75:16	Q. BY MR. LINDSAY: And so we were just talking about the fact that memory chip 200-0 has a much shorter flight time delay because it's closer than memory chip 200-19, which has a longer delay and -- in order to -- in order to output data at the same time. So to -- A. Uh-huh. Q. -- accommodate that different delay, the data buffer then is outputting it all at T6? MR. CHANDLER: Objection. Form. Q. BY MR. LINDSAY: Regardless of where it came from, it -- it would be output at T6? MR. CHANDLER: Objection. Form. THE WITNESS: Yeah, it <u>output</u> to T6. So they're all <u>outputs</u> at the same time. So that's why -- that's why their delay is necessary, to be inserted based on the	Q. BY MR. LINDSAY: And so we were just talking about the fact that memory chip 200-0 has a much shorter flight time delay because it's closer than memory chip 200-19, which has a longer delay and -- in order to -- in order to output data at the same time. So to -- A. Uh-huh. Q. -- accommodate that different delay, the data buffer then is outputting it all at T6? MR. CHANDLER: Objection. Form. Q. BY MR. LINDSAY: Regardless of where it came from, it -- it would be output at T6? MR. CHANDLER: Objection. Form. THE WITNESS: Yeah, it <u>outputs</u> at T6. So they're all <u>output</u> at the same time. So that's why -- that's why their delay is necessary, to be inserted based on the	Typographical errors, and this was further clarified at 82:10–84:12, 120:8–125:25.
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
	different times at which the data is returned.	different times at which the data is returned.	
76:19–:20	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
78:14	the system <u>CLK</u>	the system <u>clock</u>	Typographical error
78:21 78:23 78:24 79:2 79:6	<u>CLK</u>	<u>clock</u>	Typographical error
79:17 79:21 80:1–:2 80:5 80:9 80:14 81:8 81:11 81:12 81:16 82:17 82:24 83:2 83:7	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
84:25– 85:10	Q. And does Butt delay or advance the DQ data signal as well? MR. CHANDLER: Objection. Form. THE WITNESS: Well, it -- you know, well, Butt teaches primarily -- I mean, it -- when Butt teaches the optimization, it is in order to allow you to sample the -- the DQ signal in the best position. So you're moving the DQS while holding the DQ the same. So it -- you're trying to get right in the -- right in the middle, the best, most optimal spot to where you want to sample the valid data.	[see note]	No change, but this was further clarified at 138:16–139:1.
89:18 89:24–:25 90:2 90:6	<u>CLK</u> signal	<u>clock</u> signal	Typographical error
91:16	<u>CLK</u> the data out	<u>clock</u> the data out	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
94:11–:19	Q. So if I wanted to make a bigger, you know -- you know, DDR memory module, that would not be compliant with the JEDEC standard if it exceeded their -- their prescribed dimensions for memory modules of that -- of that type? MR. CHANDLER: Objection. Form. THE WITNESS: Yeah, it's correct. They specify -- they specify pretty exacting what the size of the -- of the memory module should be.	[see note]	No change, but this was further clarified at 139:9–140:8.
100:4	a <u>CLK</u>	a <u>clock</u>	Typographical error
104:6	the <u>CLK</u>	the <u>clock</u>	Typographical error
113:3	<u>right</u> leveling	<u>write</u> leveling	Typographical error
113:11	Exhibit <u>13</u>	Exhibit <u>1013</u>	Typographical error
114:5	<u>right</u> leveling	<u>write</u> leveling	Typographical error
115:6–:7	between the DQ and DQS lines <u>in</u> the read leveling circuit 323?	between the DQ and DQS lines <u>and</u> the read leveling circuit 323?	Typographical error
117:4 117:5	<u>releveling</u> process	<u>read leveling</u> process	Typographical error
118:21–:22	<u>right</u> leveling	<u>write</u> leveling	Typographical error

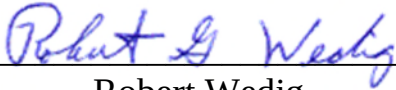
<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
118:25	the <u>CLK</u> line	the <u>clock</u> line	Typographical error
119:9 119:11–:12 119:19	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
123:2 123:10	the <u>CLK</u> signal	the <u>clock</u> signal	Typographical error
123:14	<u>CLK</u>	<u>clock</u>	Typographical error
126:2–:3 126:7 126:9 126:9–:10 126:14 126:16	system level <u>CLK</u>	system level <u>clock</u>	Typographical error
126:21 127:1 127:8 127:10 127:11 127:14 127:17	<u>CLK</u>	<u>clock</u>	Typographical error
127:22–:23	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error
128:12–:13	from the module control device in <u>read</u> out to the left	from the module control device in <u>red</u> , out to the left	Typographical error
131:4 131:6 131:16 132:5 132:12	<u>CLK</u> cycle[s]	<u>clock</u> cycle[s]	Typographical error
133:14 133:16 137:12	<u>CLK</u> [s]	<u>clock</u> [s]	Typographical error
141:12	system <u>CLK</u> CK	system <u>clock</u> CK	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
141:23	system <u>CLK</u>	system <u>clock</u>	Typographical error
142:1	<u>CLK</u>	<u>clock</u>	Typographical error
142:4--:6	when you see <u>CLK (IN)</u> , that's the <u>CLK</u> at the time that it's at that particular <u>module</u>	when you see <u>CK(IN)</u> , that's the <u>clock</u> at the time that it's at that particular <u>component</u>	Typographical errors, and I clarified in the next answer that instead of "module" it would be more precise to say "component"
142:12--:13 142:16	<u>CLK(IN)</u>	<u>CK(IN)</u>	Typographical error
142:16	<u>CLK</u> signal	<u>clock</u> signal	Typographical error
142:25	<u>CLK</u>	<u>clock</u>	Typographical error
143:20	system <u>CLK CK (IN)</u>	system <u>clock CK(IN)</u>	Typographical error
144:5	system <u>CLK CK</u>	system <u>clock CK</u>	Typographical error
144:12	system <u>CLK</u>	system <u>clock</u>	Typographical error
145:21 145:22	<u>CLK</u> signals	<u>clock</u> signals	Typographical error
146:5 146:20 146:22 148:6	<u>CLK</u>	<u>clock</u>	Typographical error
148:11	<u>CLK</u> signal CK	<u>clock</u> signal CK	Typographical error
148:22	<u>CLK</u> signal	<u>clock</u> signal	Typographical error

I hereby certify that the transcript of my deposition on March 12, 2024, as corrected above, is a true and accurate transcription of my testimony.

I, Robert Wedig, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: March 25, 2024


Robert Wedig