

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2022-00711

Patent 10,860,506

**ERRATA TO THE DEPOSITION OF
ROBERT WEDIG (JANUARY 19, 2023)**

I, ROBERT WEDIG, have read the transcript of my deposition taken on January 19, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
1:15	<u>Videotaped</u> deposition	Deposition	I don't think there was a videographer
32:19--:23	Q. Does JEDEC have restrictions against labeling components that are not -- with DDR2 designations when they are non-compliant? A. No, I don't know. That's not -- <u>that's a</u> technical question.	Q. Does JEDEC have restrictions against labeling components that are not -- with DDR2 designations when they are non-compliant? A. No, I don't know. That's not -- <u>that's not a technical</u> question.	Typographical error
33:18--:19	I think that you need to have -- you <u>need have to</u> some teaching of it.	I think that you need to have -- you <u>need to have</u> some teaching of it.	Typographical error
48:15--:20	Q....In 2005, was DDR2 the prevalent standard for memory modules? A. I know that DDR2 existed. I'm not sure exactly when DDR3 came out. I <u>can just say that was it prevalent?</u> The best I can say is that DDR2 existed in that time frame.	Q....In 2005, was DDR2 the prevalent standard for memory modules? A. I know that DDR2 existed. I'm not sure exactly when DDR3 came out. I <u>can't just say that it was prevalent.</u> The best I can say is that DDR2 existed in that time frame.	Typographical errors

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
52:11	DD3 compliant memory	DDR3 compliant memory	Typographical error
56:19	As I said, <u>would I hope so.</u>	As I said, <u>I would hope so.</u>	Typographical error
62:23–63:3	One of ordinary skill would know the -- one of ordinary skill would know the individual components that are available in the JEDEC standard <u>from</u> doing read leveling, and they would know how to utilize those individual components in order to perform read leveling.	One of ordinary skill would know the -- one of ordinary skill would know the individual components that are available in the JEDEC standard <u>for</u> doing read leveling, and they would know how to utilize those individual components in order to perform read leveling.	Typographical error
65:8–:14	Q. What support have you pointed to the idea that read leveling includes centering data? A. Well, first, I pointed to the "by about 90 degrees," first of all. The words " <u>and the such</u> ," " <u>and the such</u> " meaning we need to do more than that. And I'm also relying on the knowledge of one of ordinary skill.	Q. What support have you pointed to the idea that read leveling includes centering data? A. Well, first, I pointed to the "by about 90 degrees," first of all. The words " <u>and the like</u> ," " <u>and the like</u> " meaning we need to do more than that. And I'm also relying on the knowledge of one of ordinary skill.	I misspoke. I provided the correct quote earlier, for example, at 60:1–:3, 60:8–:12, 60:19–61:4, 61:10–62:9, 63:22–64:1.

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
74:19–:25	So what happens is, as it's described in Hiraishi, that the <u>data buffer</u> outputs a clock signal, and at the same time it issues an ACT and a read command. So that's shown at the top of <u>Figure 7</u> . I don't know if you want me to share my screen to show <u>Figure 7</u> .	So what happens is, as it's described in Hiraishi, that the <u>memory controller</u> outputs a clock signal, and at the same time it issues an ACT and a read command. So that's shown at the top of <u>Figure 17</u> . I don't know if you want me to share my screen to show <u>Figure 17</u> .	Typographical errors and I misspoke (saying “data buffer” instead of “memory controller”).

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
75:3-:19	Okay. All right. So it outputs the ACT, and then five clocks later it outputs the read command. Then the data buffer receives the read command from the module controller, with a slight flight time delay. And then there is -- that then causes the data buffer, after a lapse, after a CAS latency, it outputs dummy data to the memory controller. It comes straight from the <u>memory controller</u>, not from the memory chip. And so what it does is it comes out six clocks later if you have a CAS latency of six clocks. So then the memory controller receives that data and it determines from the delay, the fly-by delay that is inherent or part of the data buffer communication.	Okay. All right. So it outputs the ACT, and then five clocks later it outputs the read command. Then the data buffer receives the read command from the module controller, with a slight flight time delay. And then there is -- that then causes the data buffer, after a lapse, after a CAS latency, it outputs dummy data to the memory controller. It comes straight from the <u>data buffer</u>, not from the memory chip. And so what it does is it comes out six clocks later if you have a CAS latency of six clocks. So then the memory controller receives that data and it determines from the delay, the fly-by delay that is inherent or part of the data buffer communication.	I misspoke.

83:8–84:3	Q. Okay. So read leveling between the memory controller and the data buffer is initiated in the memory controller, not the register buffer 400? A. That's correct. Q. Okay. So in neither S4 nor S5 leveling is the register buffer 400 initiating those operations? A. Well, yeah. There is no instruction in Hiraishi on the module controller doing any initiation of S4 or S5 read leveling. <u>As I said</u>, you know, the module controller -- I'm sorry, the data buffer is going to have to get some notification that it's time to do write leveling or read leveling. So, you know, I don't -- it's simply not taught as to where that comes from.	[see note]	This was clarified at 81:18–82:12, 97:15–:21.
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
102:12–:14	Well, the data comes into the FIFO from the DQ signals, through the selector, <u>34</u> , and it goes into the FIFO. You see that in Figure 5.	Well, the data comes into the FIFO from the DQ signals, through the selector, <u>334</u> , and it goes into the FIFO. You see that in Figure 5.	Typographical error

104:14– 106:1	Q. What about the red line, though, coming down into the FIFO, couldn't that be sampling the read data? A. The LCLKR signal is what you are referring to? Q. Yes. A. Yeah, that's not -- that's not what's taught. In fact, you have to -- you've got to accept it in, and then the FIFO delays it, and then you have to read it out. First of all, it would be impossible to sample the data with the LCLKR, because the LCLKR doesn't know whether the data is valid. It's only the DQS signal that tells you when the value on the DQ signal is valid. So it's got to be the DQS signal. <u>LQR</u> would not know when the data is valid. Until it gets into the FIFO and now it's being passed down the line, and it takes that value after it's been captured	Q. What about the red line, though, coming down into the FIFO, couldn't that be sampling the read data? A. The LCLKR signal is what you are referring to? Q. Yes. A. Yeah, that's not -- that's not what's taught. In fact, you have to -- you've got to accept it in, and then the FIFO delays it, and then you have to read it out. First of all, it would be impossible to sample the data with the LCLKR, because the LCLKR doesn't know whether the data is valid. It's only the DQS signal that tells you when the value on the DQ signal is valid. So it's got to be the DQS signal. <u>LCLKR</u> would not know when the data is valid. Until it gets into the FIFO and now it's being passed down the line, and it takes that value after it's	Typographical errors, and this testimony was further clarified at 93:24–94:2, 219:1–222:3.
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
	already, then <u>LQR</u> passes it out to the memory controller. ... Q. So that signal clocking out the data cannot sample the data? ... A. No, it can't, because it doesn't know when the data is there, until it's gotten into the FIFO. LCLKR does not know if the data on the -- it does not know if the value on the <u>DQS</u> signal holds a valid value. That information is provided by DQS. So DQS transitions, it becomes active, when the data is valid. So you have to use DQS.	been captured already, then <u>LCLKR</u> passes it out to the memory controller. ... Q. So that signal clocking out the data cannot sample the data? ... A. No, it can't, because it doesn't know when the data is there, until it's gotten into the FIFO. LCLKR does not know if the data on the -- it does not know if the value on the <u>DQ</u> signal holds a valid value. That information is provided by DQS. So DQS transitions, it becomes active, when the data is valid. So you have to use DQS.	

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
110:9–:20	What that means is that this device can be sold and would be considered operating within its bounds if the DQS signal were activated, and then up to 200 picoseconds later the <u>DQS signal</u> were activated on the output of the pins of this memory device. So there can be a skew that is a difference in time between when the DQS signal activates and the DQ signal activates up to 200 picoseconds, and it would still be considered operating within the margins of the manufacturer's specifications.	What that means is that this device can be sold and would be considered operating within its bounds if the DQS signal were activated, and then up to 200 picoseconds later the <u>DQ signal</u> were activated on the output of the pins of this memory device. So there can be a skew that is a difference in time between when the DQS signal activates and the DQ signal activates up to 200 picoseconds, and it would still be considered operating within the margins of the manufacturer's specifications.	Typographical error
120:11–:14	And so already we know that a JEDEC-compliant device is going to be putting out data <u>in</u> the data strobe that are 200 picoseconds -- up to 200 picoseconds off from each other.	And so already we know that a JEDEC-compliant device is going to be putting out data <u>and</u> the data strobe that are 200 picoseconds -- up to 200 picoseconds off from each other.	Typographical error

136:6–:22	So additional circuitry? I don't think there's any additional circuitry because Hiraishi already discusses it. But if you feel that that's not the case, <u>then Butt would use the circuitry and would use the logic, and you'd teaching</u> from Butt in order to be able to implement the mechanisms needed to perform this fine-tuning. So I don't think it's additional circuitry because I think Hiraishi already implied that you had it. But if you feel that Hiraishi did not have it, then you would combine Butt with it. Again, I'm just <u>accepting. If</u> you don't buy the fact that it already was built into Hiraishi, then it would be an addition to be able to add the teachings of Butt, and it would be the circuitry that is discussed in Butt in order to help make	So additional circuitry? I don't think there's any additional circuitry because Hiraishi already discusses it. But if you feel that that's not the case, <u>then you would use the circuitry and would use the logic, and the teaching</u> from Butt in order to be able to implement the mechanisms needed to perform this fine-tuning. So I don't think it's additional circuitry because I think Hiraishi already implied that you had it. But if you feel that Hiraishi did not have it, then you would combine Butt with it. Again, I'm just <u>accepting, if</u> you don't buy the fact that it already was built into Hiraishi, then it would be an addition to be able to add the teachings of Butt, and it would be the circuitry that is discussed in Butt in order to help make	Typographical errors
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
	this fine-tuning mechanism obvious.	this fine-tuning mechanism obvious.	
150:16– 151:1	Q. Okay. And then that purple line that's coming out of DR1 and is going down to FIFO 302, what is that? A. That is the signal that is the delayed <u>DRQ</u> that would pass the -- that would read out the data from the FIFO once the DR -- sorry, once the DQS has been activated, the delayed DQS has been activated. Q. So the purple line that's going down from DR1 to FIFO 302, that's clocking out the read data then from 302? A. That's correct.	Q. Okay. And then that purple line that's coming out of DR1 and is going down to FIFO 302, what is that? A. That is the signal that is the delayed <u>DQS</u> that would pass the -- that would read out the data from the FIFO once the DR -- sorry, once the DQS has been activated, the delayed DQS has been activated. Q. So the purple line that's going down from DR1 to FIFO 302, that's clocking out the read data then from 302? A. That's correct.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
172:17–:23	Q. But Tokuhiro detects that delay in the memory controller. Why isn't that the most logical place to put it? A. Because as I said, in this particular system -- see, Tokuhiro did not have a data buffer, so the fly-by delay that it was detecting was out at the memory <u>module</u>.	Q. But Tokuhiro detects that delay in the memory controller. Why isn't that the most logical place to put it? A. Because as I said, in this particular system -- see, Tokuhiro did not have a data buffer, so the fly-by delay that it was detecting was out at the memory <u>devices</u>.	I misspoke. I explained the same point at 171:10–:13.
175:4–:11	As I said, it makes the most sense to put it in the place where you want to do the delay, where you are measuring the delay, especially it has to be there because in order to be able to transmit the information both ways, be able to do the read leveling and the write leveling, it all has to be together, and that, as I said, more <u>sufficiently</u> would be in the data buffer.	As I said, it makes the most sense to put it in the place where you want to do the delay, where you are measuring the delay, especially it has to be there because in order to be able to transmit the information both ways, be able to do the read leveling and the write leveling, it all has to be together, and that, as I said, more <u>efficiently</u> would be in the data buffer.	Typographical error

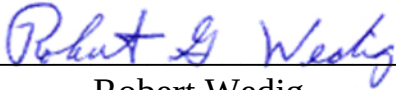
<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
179:22–:25	So then in Paragraph 313, you mention that the memory controller will still require <u>retraining</u> to activate the input buffers in time and adjusting the phase of the local clock.	So then in Paragraph 313, you mention that the memory controller will still require <u>read training</u> to activate the input buffers in time and adjusting the phase of the local clock.	Typographical error
184:18–:21	And so it seems to me that it's a trivial circuit modification to add write information into the measuring circuit versus read information. It's just a matter of adding one <u>multiplex</u> .	And so it seems to me that it's a trivial circuit modification to add write information into the measuring circuit versus read information. It's just a matter of adding one <u>multiplexor</u> .	Typographical error
194:5–:10	Q. You could put it in the memory controller. That's where Tokuhiro puts it. A. I don't think that would change anything. Yeah. I think it would be a lot less efficient because you've already got these <u>immediate</u> communications.	Q. You could put it in the memory controller. That's where Tokuhiro puts it. A. I don't think that would change anything. Yeah. I think it would be a lot less efficient because you've already got these <u>intermediate</u> communications.	Typographical error
207:3	that's explicitly <u>where</u> I say	that's explicitly <u>what</u> I say	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
207:14-:18	Q. But the generation of the control signal that programs the read delay in your two implementations does not come from the CPU, right? A. That's not <u>to suggest a</u> combination that I'm talking about. Q. And why did you not suggest carrying it out as Tokuhiro does, using the CPU to program the delay elements? A. I don't think it matters.	Q. But the generation of the control signal that programs the read delay in your two implementations does not come from the CPU, right? A. That's not <u>a suggested</u> combination that I'm talking about. Q. And why did you not suggest carrying it out as Tokuhiro does, using the CPU to program the delay elements? A. I don't think it matters.	Typographical error

I hereby certify that the transcript of my deposition on January 19, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Robert Wedig, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: January 29, 2023


Robert Wedig